

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00792
Patent 11,468,957 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6 and issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Micron Technology, Inc. (“Petitioner”) does not show by a preponderance of the evidence that claims 1–6 (the “challenged claims”) of U.S. Patent No. 11,468,957 B2 (“the ’957 patent,” Ex. 1001) are unpatentable.

A. Procedural Background

Petitioner filed a Petition to institute an *inter partes* review of claims 1–6 of the ’957 patent. Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 11. Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of claims 1–6 on the grounds advanced in the Petition. Paper 13 (“Institution Decision” or “Dec.”). After institution of trial, Patent Owner filed a Patent Owner Response (“PO Resp.,” Paper 17), Petitioner filed a Reply (“Pet. Reply,” Paper 20), and Patent Owner filed a Sur-reply (“PO Sur-reply,” Paper 22).

We held an oral hearing on August 7, 2025, and a transcript is included in the record. Paper 32 (“Tr.”).

B. Real Parties in Interest

Petitioner identifies “Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 4. Patent Owner identifies itself as the real party in interest. Paper 3 (Mandatory Notice), 2.

C. Related Matters

The parties indicate that the '957 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 4; Paper 3, 2.

D. The '957 Patent

The '957 patent, titled “Architecture and Method for NAND Memory Operation,” relates to “apparatuses and methods for verifying/reading memory cells of a 3D-NAND memory device to reduce hot carrier injection (HCI)-induced edge summation (ESUM) loss, and reduce power consumption during verifying/reading the memory cells of the 3D-NAND memory device.” Ex. 1001, code (54), 1:44–49. The memory device includes a first memory cell string and second memory cell string, each of which includes a bottom-select-gate (“BSG”) transistor, memory cells, and a top-select-gate (“TSG”) transistor connected in series. *Id.* at 4:12–20. The '957 patent teaches that processing circuitry is configured to apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, where the selected memory cell can be programmed and arranged between a first adjacent memory cell and a second adjacent memory cell. *Id.* at 4:20–25. The processing circuitry also applies, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed. *Id.* at 4:25–29. The '957 patent further teaches that, in the verify stage, the processing circuitry applies a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string, and a second bias voltage on the gate terminal at the at least one memory cell of the first memory cell string that is not programmed. *Id.* at 4:29–35. The second bias voltage can be smaller than the first bias voltage. *Id.* at 4:35–36.

E. Challenged Claims

Petitioner challenges claims 1–6 of the '957 patent. Claim 1, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

1. [1.PRE] An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select gate (BSG) transistor, memory cells, and top-select gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:

[1.A] processing circuitry configured to:

[1.a] apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

[1.b] apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

[1.c] apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

[1.d] apply, in a verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

Ex. 1001, 17:32–56 (bracketed material added).

F. Asserted Grounds

Petitioner asserts that claims 1–6 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6	103 ¹	Hongtao, ² Yu ³
1–6	102	Suzuki ⁴
1–6	103	Costa, ⁵ Seo ⁶

Pet. 8. Petitioner relies on the Declarations of David Kuan-Yu Liu (Ex. 1003; Ex. 1027) in support of its contentions. Patent Owner relies on the Declaration of Steven Przybylski, Ph.D. (Ex. 2003).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “a bachelor of science degree in electrical engineering or a similar discipline” with “4–5 years of professional experience working with (e.g., researching, designing, or developing) NAND flash memory devices (including issues relating to the operation, e.g., reading of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 19–20 (citing Ex. 1003 ¶¶ 35–39). Patent Owner states

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’031 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

² Hongtao, CN 109065091 A, published Dec. 21, 2018 (Ex. 1005).

³ Yu, US 2019/0198117 A1, published June 27, 2019 (Ex. 1006).

⁴ Suzuki, US 2021/0082505 A1, published Mar. 18, 2021 (Ex. 1007).

⁵ Costa, US 2018/0012667 A1, published Jan. 11, 2018 (Ex. 1008).

⁶ Seo, US 2021/0027848 A1, published Jan. 28, 2021 (Ex. 1009).

that it does not object to the definition of a POSITA proffered by Petitioner. PO Resp. 11 (citing Pet. 19–20).

In the Institution Decision, we adopted the assessment offered by Petitioner. Dec. 5–6. Because Petitioner’s definition of the level of skill in the art is consistent with the ’957 patent and the asserted prior art, we maintain it for purposes of this Final Written Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. Dr. Przybylski’s Testimony

Petitioner argues that Dr. Przybylski’s testimony is entitled to little weight. Pet. Reply 31–32. In particular, Petitioner argues that Dr. Przybylski declaration “merely parrots PO’s Response through conclusory remarks, including words copied from the Response and then altered.” *Id.* at 31. Petitioner also argues that “the record plainly contradicts his opinions” and that Dr. Przybylski’s “testimony is disingenuous.” *Id.* at 31–32. Patent Owner disagrees, and argues that “Dr. Przybylski’s testimony is well supported by the record” and “does not rely on attempts to conflate distinct concepts” or rewrite the claim language. PO Sur-reply 25–26.

It is within our discretion to assign the appropriate weight to Dr. Przybylski’s testimony. *See, e.g., Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding that the Board has discretion to give more weight to one item of evidence over another “unless no reasonable trier of fact could have done so”); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) (“[T]he Board is entitled to weigh the declaration and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.”). On this record, we decline to generally discount Dr. Przybylski’s based on Petitioner’s contentions. When assigning

weight to a declarant's testimony, we consider the underlying facts or data upon which the testimony is based. *See* PTAB Consolidated Trial Practice Guide 40–41 (Nov. 2019). In our analysis of the asserted grounds of unpatentability, we weigh Dr. Przybylski's testimony accordingly.

C. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Based on our review of the complete trial record and the arguments raised by the parties, we determine that it is not necessary to expressly construe any claim terms to resolve the parties' dispute. *Realtime Data*, 912 F.3d at 1375.

D. Asserted Obviousness over Hongtao and Yu

Petitioner contends that claims 1–6 would have been obvious over the combined teachings of Hongtao and Yu. Pet. 27–74.

1. Overview of Hongtao

Hongtao relates to a reading method of 3D NAND flash memory that reduces read interference and improves the accuracy of read data during the reading process. Ex. 1005 ¶¶ 1, 4.

Figure 1 is reproduced below.

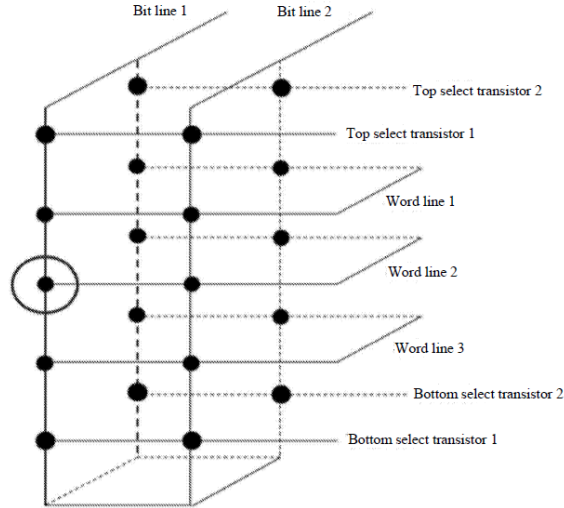


Figure1

Figure 1 is a diagram of one embodiment of the 3D NAND storage structure described in Hongtao. Ex. 1005 ¶ 13. Hongtao's 3D NAND storage structure includes multiple memory cells (black dots) arranged in an array to form multiple memory strings, with a top select transistor connected to the bit line at the top of each memory string. *Id.* ¶ 18. The transistor at the bottom of the memory string is a bottom select transistor. *Id.* Multiple memory cells located in the same layer form a memory row, and the gates of the memory cells located in different memory strings but the same memory row are physically connected and are connected to the same word line. *Id.*

Hongtao teaches that, to read the information of the memory cell circled in Figure 1 above, a driving voltage is applied to bit lines 1 and 2, top select transistor 1 and bottom select transistor 1 of the selected string where the memory cell is located are turned on, and a conduction voltage is applied to word lines 1 and 3 of the unselected rows other than the row where the memory cell is located in order to run on the channel of the selected string. Ex. 1005 ¶ 19. Top select transistor 2 and bottom select transistor 2 of the

unselected string are turned off, the channels of the other unselected string are prevented from being turned on. *Id.* A read voltage is applied to word line 2 of the selected row to read the information in the selected memory cell. *Id.* Hongtao explains that the conduction voltage applied to word lines 1 and 3 of the unselected row will generate a potential via channel coupling in all memory cells connected to word lines 1 and 3, causing hot carrier injection crosstalk that “causes the electrons stored in other unselected memory cells to drift, resulting in changes in the data stored in the unselected memory cells, as well as problems such as drift in the data in the selected memory cell that is read.” *Id.* ¶ 20.

Hongtao describes an embodiment in which there is pre-conduction phase to turn on the channels of the selected and unselected strings before reading the memory cell. Ex. 1005 ¶ 22. In the pre-conduction stage, a pre-conduction voltage is applied to both the selected and unselected word line to turn on the channels of the selected and unselected strings. *Id.* ¶ 23. The top select transistor and the bottom select transistor of both the selected and unselected strings are both turned on, and, at the same time, the bit line remains at a low potential, for example, 0 V. *Id.* The channels are connected to the bit line, and the channel potential will remain at the same low potential as the bit line. *Id.* In this way, Hongtao teaches, the channels of the selected and unselected strings will not generate voltage coupling due to changes in the word line voltage, “thereby avoiding the problem of hot carrier injection crosstalk caused when a conduction voltage is applied to the word line of an unselected memory cell.” *Id.*

Hongtao further teaches that, in the reading phase, a driving voltage is applied to the bit line, and a disconnection voltage is applied to the top select transistor and bottom select transistor of the unselected string to disconnect

the channel of the unselected string from the bit line, and the channel potential of the unselected string is locked to a low potential of 0 V.

Ex. 1005 ¶ 24. A conduction voltage is applied to the top select transistor and the bottom select transistor of the selected string, so that the channel of the selected string is connected to the bit line, and the channel of the selected string is equal to the driving voltage on the bit line. *Id.* ¶ 25. The conduction voltage is applied to the gates of the unselected memory cells on the selected string through the unselected word lines, and the unselected memory cells will withstand read interference caused by the “conduction voltage – driving voltage.” *Id.*

Hongtao explains the read interference is positively related to the voltage causing read interference, such that the read interference is stronger when the voltage is greater. Ex. 1005 ¶ 26. In the embodiment described above, “the read interference caused by the ‘conduction voltage – driving voltage’ suffered by the unselected memory cells on the selected string is smaller than the read interference suffered by the memory cells on the unselected string.” *Id.*

2. Overview of Yu

Yu relates generally to semiconductor integrated circuits, and more particularly describes a method of programming in a nonvolatile memory device, as well as a nonvolatile memory device, capable of reducing disturbance on unselected memory cells during a program operation.

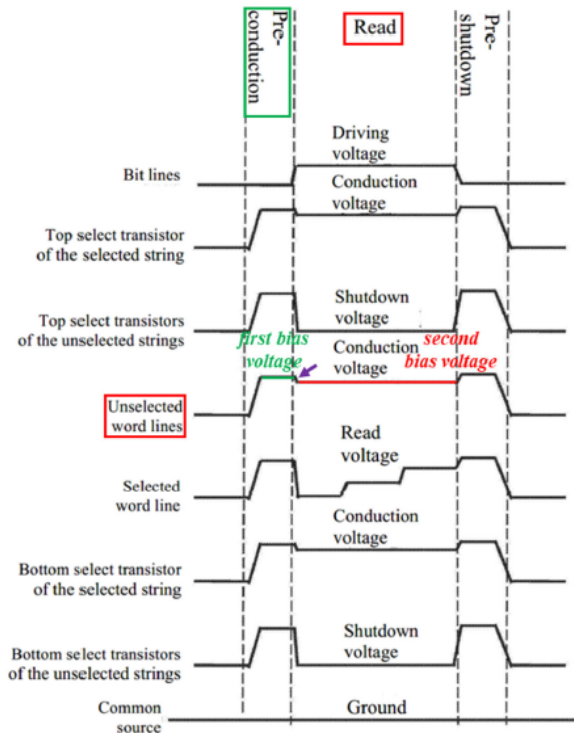
Ex. 1006 ¶¶ 2, 5, 6. Yu describes a memory block provided with a plurality of sub blocks disposed in a vertical direction, which includes a plurality of cell strings each including a plurality of memory cells connected in series. *Id.* ¶ 7. A plurality of intermediate switching transistors is disposed in a boundary portion between two adjacent sub blocks in the vertical direction,

each of which is selectively activated based on a program address during a program operation. *Id.* Yu teaches that the program operation can be performed in an upward direction from a lowest word line, such that as the data stored in the memory block increase, the data may be filled in erased cells in the upward direction from bottom to top. *Id.* ¶ 115. Yu also teaches the converse; that is, as the data stored in the memory block increase, the data may be filled in erased cells in the downward direction from top to bottom. *Id.* ¶ 130.

3. Analysis

Petitioner contends that Hongtao and Yu teach all of the limitations of independent claim 1. Pet. 27–40. Patent Owner responds that “Hongtao in view of Yu does not disclose or render obvious applying ‘first bias’ and ‘first verify’ voltages during a ‘pre-verify’ stage” as recited in limitations [1.a] and [1.b], or “applying a ‘second bias voltage’ smaller than a ‘first bias voltage’ on a gate terminal of a not programmed memory cell” as recited in limitation [1.d]. PO Resp. 27. We focus our analysis on limitation [1.d], as it is dispositive of the controversy between the parties.

Limitation [1.d] recites applying, “in the verify stage, a second bias voltage on the gate terminal of at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.” Ex. 1001, 17:52–56. Petitioner contends that Hongtao “discloses applying *a second bias voltage* (a conduction voltage) on the same cell through the same unselected word lines *in the verify stage* (the read phase).” Pet. 39–40 (citing Ex. 1005 ¶¶ 19, 25, Fig. 2). Petitioner provides an annotated version of Hongtao’s Figure 2, reproduced below, to illustrate its contentions. *Id.*



Annotated Figure 2 is a timing diagram for reading a 3D NAND memory cell described in Hongtao, with Petitioner’s additions of a green box around the “Pre-conduction” label and a red box around the “Read” label at the top of the diagram, a red box around the “Unselected word lines” label on the left of the diagram, a green line labeled “first bias voltage” and red line labeled “second bias voltage” on portions of the line labeled “Unselected word lines,” and a purple arrow pointing to where the green “first bias voltage” line meets the red “second bias voltage” line. Ex. 1005 ¶ 14. Petitioner contends that, “[a]s indicated by the purple arrow, the voltage signal applied to the unselected word lines ramps down from the pre-conduction voltage to reach the conduction voltage,” and, “[t]hus, *the second bias voltage is smaller than the first bias voltage.*” Pet. 40 (citing Ex. 1003 ¶ 120). Petitioner further contends that “Hongtao explains that ‘the greater the conduction voltage, the greater the read disturbance to the memory

cell,” and “[a]ccordingly, the conduction voltage is reduced during the read phase to reduce read disturbance.” *Id.* (citing Ex. 1005 ¶¶ 24–26; Ex. 1003 ¶¶ 118–120).

Patent Owner responds that “Fig. 2 of Hongtao would not have suggested to a POSITA that an applied ‘second bias voltage on a gate terminal’ is smaller than an applied ‘first bias voltage on a gate terminal’” as required by the ’957 patent. PO Resp. 32. Patent Owner argues that “Figure 2 of Hongtao depicts target voltages applied to word lines, rather than the resulting voltages applied on gate terminals of the memory cells.” *Id.* Patent Owner also argues that Hongtao does not teach or suggest that Figure 2 depicts the actual voltages applied on the gate terminals of the memory cells, or provide the details necessary to infer how the voltages applied on the gate terminals would develop over time. *Id.* at 38.

The parties’ declarants provide different interpretations of Hongtao’s Figure 2. *See, e.g.*, Ex. 1003 ¶¶ 116–120; Ex. 1027 ¶¶ 16–51; Ex. 2003 ¶¶ 88–103. Referring to annotated Figure 2 of Hongtao (reproduced above), Petitioner’s declarant Dr. Liu testifies that, “[a]s indicated by the purple arrow, the voltage applied to the unselected word lines ramps down from the pre-conduction voltage to reach the conduction voltage.” Ex. 1003 ¶ 120.

Dr. Liu explains:

I note Hongtao explains why the unselected word lines voltage is dropped. Specifically, Hongtao discloses that ‘the greater the conduction voltage, the greater the read disturbance to the memory cell.’ [Ex. 1005], [0026]; *see also id.*, [0024]–[0025]. Accordingly, the conduction voltage is reduced during the read phase to reduce read disturbance. I note that Hongtao discloses this read disturbance is a function of the (conductance voltage – *channel* voltage), with the channel voltage being the driving voltage for the selected string and 0V for the unselected string. Lowering the conduction voltage on the unselected word lines

alleviates the read disturbance of the unselected memory cell for both the selected string and the unselected string during the longer period of the read phase. Of course, this voltage cannot be dropped to zero, because it has to turn on the transistor. And this is why it drops only slightly.

Id.

Patent Owner's declarant Dr. Przybylski, on the other hand, asserts that "a POSITA would have understood Figure 2 of Hongtao to be describing the target voltages applied to word lines, rather than the resulting bias voltages that are actually applied on the gate terminals of the memory cells." Ex. 2003 ¶ 93. In particular, Dr. Przybylski testifies that "Hongtao does not address the fact that the voltages applied to gate voltages need time to develop over time" and "does not provide sufficient information to ascertain the actual bias voltages that will be applied on the gate terminals of the memory cells over time." *Id.* ¶ 96. Dr. Przybylski explains:

[T]he waveforms illustrated in Figure 2 of Hongtao depict steep slew rates (i.e., change of rates of voltage through time), straight lines, and sudden changes signifying target voltages—all of which indicate that Hongtao is illustrating target voltages, rather than the resulting voltages that develop over time on the gate terminals of the memory cells. Furthermore, Hongtao also fails to disclose any of the other details that would be needed to determine how the gate voltages develop over time, such as the architecture of the device and the length of the pre-conduction period. *Cf.* '957 Patent, 11:58–12:9, 12:10–27 (discussing that bias voltages require enough time to progress fully and providing examples).

Id. Dr. Przybylski further testifies:

There are other reasons a POSITA looking at Figure 2 of Hongtao would expect the resulting voltages applied on the gate terminals of the memory cells to remain the same between the pre-conduction phase and the reading phase. Changing the bias voltage can also alter the voltages in the strings of memory cells

due to capacitive couplings, and create transient currents running down the length of the string that potentially interfere with normal operation of the memory array. Indeed, these transient currents could create false readings of the selected memory cell. Accordingly, it would be expected that the voltages of the type illustrated in Figure 2 of Hongtao would result in voltages applied on the gate terminals of the memory cell that are maintained at a fixed level when going into a reading phase from the pre-conduction phase.

Id. ¶ 99.

It is Petitioner’s burden to establish facts supporting its challenge that claim 1 would have been obvious over the combined teachings of Hongtao and Yu by a preponderance of the evidence. 35 U.S.C. § 316(e) (2018); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). After considering the parties’ arguments and evidence of record, and weighing the testimony of Dr. Liu and Dr. Przybylski, we are not persuaded that Petitioner meets its burden of establishing, by a preponderance of the evidence, that Hongtao teaches or suggests applying a second bias voltage that is smaller than the first bias voltage in the verify stage as recited in limitation [1.d].

Hongtao is silent with respect to the magnitudes of the pre-conduction and conduction voltages. Hongtao teaches that “a pre-conduction voltage is applied to both the unselected word line and the selected word line to turn on the channels of the selected string and the unselected string.” Ex. 1005 ¶ 23. Hongtao then teaches that, in the reading phase, “[t]he gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines.” *Id.* ¶ 25. Hongtao, however,

neither provides values for the pre-conduction and conduction voltages, nor describes the magnitudes of the pre-conduction and conduction relative to each other. *See id.* ¶¶ 21–26. Petitioner and Dr. Liu point to Hongtao’s statement that “the greater the conduction voltage, the greater the read disturbance” to support its contention that the conduction voltage is smaller than the pre-conduction voltage, but that statement refers to the relationship between conduction voltage and the read interference it causes and does not compare the conduction voltage to the pre-conduction voltage. *See* Pet. 40 (citing Ex. 1005 ¶ 26); Ex. 1003 ¶ 120 (citing Ex. 1005 ¶ 26).

We also find credible Dr. Przybylski’s testimony that Hongtao lacks the details needed to determine how the gate voltages develop over time, in particular the length of the pre-conduction period. *See* Ex. 2003 ¶ 96. Dr. Przybylski’s testimony is consistent with the ’957 patent’s teaching that when the pre-pulse time is long enough that the bias voltages are fully developed before the TSG transistor is switched off at the unselected memory cell string, hot carrier injection “may not be generated from the selected memory cell to the upper adjacent memory cell of the selected memory cell in the selected memory cell.” Ex. 1001, 11:60–12:1. In contrast, when the pre-pulse time is insufficient for the bias voltages to fully develop, hot carrier injection may be generated. *Id.* at 12:1–9.

And we are not persuaded that Petitioner and Dr. Liu sufficiently rebut Dr. Przybylski’s persuasive testimony that casts doubt on Petitioner’s contention that Hongtao teaches a second bias voltage that is smaller than a first bias voltage as recited in limitation [1.d]. For example, Dr. Liu’s testimony that Hongtao teaches applying voltages on gate terminals does not adequately address Patent Owner’s argument and Dr. Przybylski’s testimony that Hongtao depicts target values for the word line voltages instead of the

resulting voltages that develop on the gate terminals of the memory cells. *See* Ex. 1027 ¶¶ 16–40. Neither Petitioner nor Dr. Liu adequately establish that Hongtao’s applied voltages are sufficiently developed such that the pre-conduction voltage actually is bigger than the conduction voltage.

Petitioner’s argument that Hongtao teaches or discloses a second bias voltage that is smaller than the first bias voltage hinges on a POSITA’s interpretation of Hongtao’s Figure 2. In light of Hongtao’s dearth of details regarding the absolute or relative magnitudes of the pre-conduction and conduction voltages, and Dr. Przybylski’s unrebutted testimony that Hongtao does not provide sufficient information to ascertain the actual bias voltages that will be applied on the gate terminals of the memory cells over time, we are not persuaded that Petitioner carries its burden of establishing that Hongtao discloses limitation [1.d].

For these reasons, we determine that Petitioner does not establish by a preponderance of the evidence, that independent claim 1, and claims 2–6 that depend, directly or indirectly, therefrom, would have been obvious over the combined teachings of Hongtao and Yu.

E. Asserted Anticipation by Suzuki

Petitioner contends that claims 1–6 are anticipated by Suzuki. Pet. 74–103.

1. Overview of Suzuki

Suzuki “relate[s] generally to a semiconductor memory device.” Ex. 1007 ¶ 2. Suzuki’s semiconductor memory device includes first and second drain select transistors, first and second source select transistors, first through fourth memory cell transistors, first and second bit lines, first through third select gate line, first and second word lines, and a controller. *Id.* ¶ 28. Suzuki teaches that “[t]he controller is configured to execute a

write operation including multiple iterations of a program loop,” and “is configured to execute, in the program loop, a program operation, a recovery operation and a verify operation in sequence.” *Id.*

Figure 11 is reproduced below.

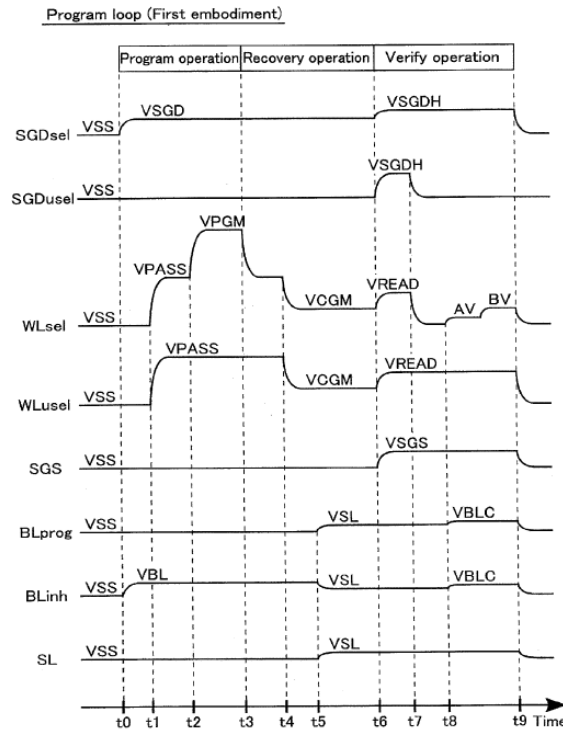


FIG. 11

Figure 11 is a timing chart illustrating an example program loop in a write operation of a semiconductor memory device described in Suzuki. Ex. 1007 ¶¶ 14, 130. Suzuki explains that, specifically, Figure 11 shows “changes in respective voltages of the select gate lines SGDsel and SGDusel, the word lines WLsel and WLusel, the select gate line SGS, the bit lines BLprog and BLinh, and the source line SL, in a program loop.” *Id.* ¶ 130. Suzuki further explains that “[i]t is assumed that the respective voltages of the select gate lines SGD and SGS, word line WL, bit line BL, and source line SL before the processing of the program loop are VSS (e.g., 0V).” *Id.*

In the program loop, a sequencer executes the process of t0 to t9 in sequence, where time t0 to t3 corresponds to a program operation, time t3 to t6 corresponds to a recovery operation, and time t6 to t9 corresponds to a verify operation. Ex. 1007 ¶ 130. At time t0, voltage VGSD is applied to select gate line SGDsel, and voltage VBL is applied to a program-inhibited bit line BLinh. *Id.* ¶ 131. VGSD and VBL are at higher voltages than VSS; for example VGSD is 4V, and VBL is 2V. *Id.* ¶ 133. At time t1, voltage VPASS (which is higher than VGSD and is, for example, 10V) is applied to each of the word lines WLsel and WLusel. *Id.* ¶ 134. At time t2, program voltage VPGM (which is, for example, 20V) is applied to word line WLsel. *Id.* ¶ 135. At time t3, VPASS is applied to word line WLsel, and the voltage of WLsel drops; at t4, voltage VGCM, which is lower than VPASS and is, for example, 3V–5V, is applied to each of the word lines WLsel and WLusel. *Id.* ¶ 138. Voltage VSL, which, for example, is 1v, is applied to bit lines BLsel and BLinh and source line SL at time t5. *Id.* ¶ 139. At time t6, voltage VGSDH is applied to select gate lines SGDsel and SDGusel, voltage VREAD is applied to word lines WLsel and WLusel, and voltage VSGS is applied to select gate line SGS. *Id.* ¶ 142. VSGDH is a higher voltage than VGSD and is, for example, 6V; VREAD is a higher voltage than VCGM and is, for example, 8V; and VSGS is a voltage higher than VSS and is, for example, 6V. *Id.* At time t7, VSS is applied to select gate line SGDusel and word line WLsel. *Id.* ¶ 143. At time t8, verify voltages AV and BV in order to word line WLsel, and voltage VBLC (for example, 1.5V) is applied to bit line BL. *Id.* ¶ 144. At time t9, VSS is applied to select gate line SGDsel, word lines WLsel and WLusel, bit lines BLprog and BLinh, and source line SL, which allows the voltage of each interconnect to return to the state before the start of the program loop. *Id.* ¶ 145. Suzuki

teaches that the recovery operation “has a period in which at minimum VGSD is applied to the select gate line SGDsel and VSL is applied to the bit line BLprog,” and “[t]he type and the number of verify voltages used in the verify operation can vary based on the write data and the progress status of the program loop.” *Id.* ¶ 146.

2. Analysis

Petitioner contends that Suzuki discloses all of the limitations of independent claim 1. Pet. 74–84. Patent Owner responds that “Suzuki does not disclose a ‘first bias voltage’ in a ‘pre-verify stage’ and a smaller ‘second bias voltage’ in a ‘verify stage’” as recited in limitations [1.b] and [1.d]. PO Resp. 48. We focus our analysis on limitation [1.b], as it is dispositive of the controversy between the parties.

Limitation [1.b] recites, in relevant part, that the processing circuitry is configured to “apply, in a pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed.” Ex. 1001, 17:46–48. Petitioner contends that Suzuki teaches that voltage VPASS (the recited “first bias voltage”) is applied to non-selected word lines (“WLuse1”) “in a pre-verify stage.” Pet. 81 (citing Ex. 1007 ¶ 134, Fig. 11). Petitioner also contends that “[t]he unselected word lines are coupled to, e.g., unselected memory cells MT5 through MT7” in Suzuki’s first embodiment, and, “[t]hus, Suzuki discloses applying a *first bias voltage* (VPASS) on ... at least one memory cell (e.g., MT6 or MT7) of the first memory cell string (the selected string).” *Id.* at 81–82 (emphasis and alterations in original). Petitioner further contends that, “[i]n Suzuki’s embodiment, memory cell MT10 is at the end of the source line side” and “the program operation may proceed ‘from cell units CU on the source line SL side in sequence’” such that when memory cell “MT4 is selected for

programming verification, MT6 and MT7 are not programmed.” *Id.* at 82 (citing Ex. 1007 ¶¶ 116, 140, Fig. 2; Ex. 1003 ¶¶ 207–208).

Patent Owner argues that “Suzuki does not disclose a first bias voltage during a ‘pre-verify stage,’ wherein the first bias voltage is larger than the second bias voltage.” PO Resp. 50. To illustrate its contentions, Patent Owner provides an annotated version of Suzuki’s Figure 11, reproduced below.

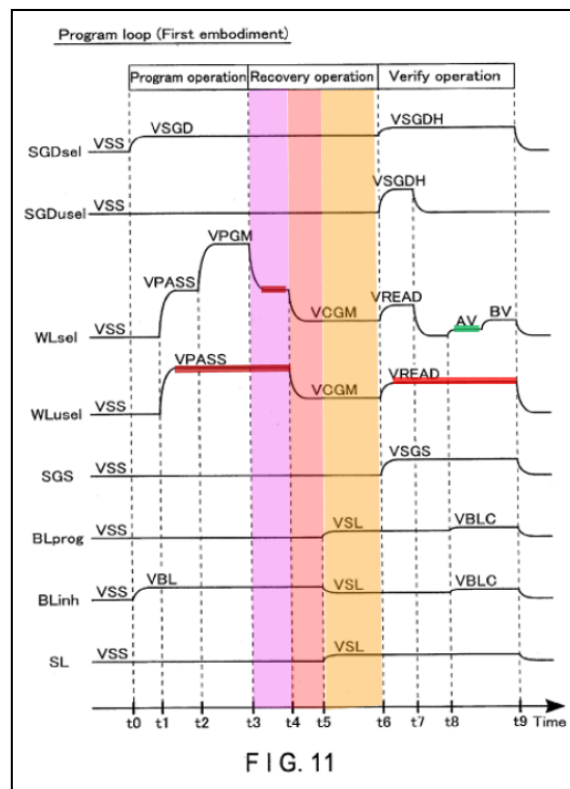


Figure 11 is a timing chart illustrating the first embodiment of a program loop described in Suzuki, with Patent Owner’s addition of red lines on the portion of VPASS between VPGM and VCGM on WLsel and on VPASS and VREAD on WLusel, a green line on a portion of WLsel labeled “AV,” and purple, pink, and orange shading to time periods t3 to t4, t-4 to t-5, and t-5 to 5-6, respectively. Ex. 1007 ¶ 14, Fig. 11; PO Resp. 52. Patent Owner asserts that “the recovery operation includes a period from t3–t4 which is an

end operation of the program operation, a period from t5–t6 with distinct voltages that acts as a ready operation of the verify operation, and a period from t4–t5 which is a transition period between the two.” PO Resp. 51 (citing Ex. 1007 ¶ 131); *see also id.* at 51–52 (“[These different parts of the recovery operation are related to the different voltages applied to each one.” (citing Ex. 2003 ¶ 125)).

Referring to annotated Figure 11, Patent Owner argues that the VPASS voltage applied on WL_{use1} in time period t1 to t4 “begins during a programming operation, is maintained for a brief period afterwards, and serves no purpose related to the subsequent ‘verify operation’ from” time period t6 to t9. PO Resp. 54 (citing Ex. 1007 ¶¶ 131, 133–135, 137, Fig. 11). Because the waveforms described in Figure 11 for time period t3 t4 mirror the voltages used during time period t1 to t2 at the start of the programming operation, Patent Owner argues that time period t3 to t4 is not a “pre-verify stage” as recited in limitation [1.b]. *Id.* (citing Ex. 1007, Fig. 11). Therefore, Patent Owner argues, VPASS in time period t3 to t4 is not a “first bias voltage” as Petitioner contends. *Id.*

After considering the complete record, we are not persuaded that Petitioner sufficiently establishes that Suzuki discloses “in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed” as recited in claim 1.

Suzuki teaches that the recovery operation in time period t3 to t6 “is an operation in which an end operation of the program operation and the ready operation of the verify operation are combined.” Ex. 1007 ¶ 131. That part of time period t3 to t6 is the end of the program operation and part of time period t3 to t6 is the ready operation of the verify operation is evident from Suzuki’s description of the voltage applied in each time period.

The VPASS voltage on WL_{sel} is first applied at time t₁ during the programming operation and does not change until time t₄, indicating the end of the program operation. *Id.* ¶¶ 134–140, Fig. 11.

Suzuki also teaches that voltage VCGM is applied at time t₄ to word lines WL_{sel} and WL_{usel}. Ex. 1007 ¶ 138. Thus, both VPASS and VCGM are applied to word lines WL_{usel} during the recovery operation in time period t₃–t₆. *Id.* at Fig. 11. Suzuki explains that “[w]hen VCGM is applied to the word lines WL_{sel} and WL_{usel}, the channel voltage of the NAND string NS, which is in the floating state, drops due to the coupling between the channel and the control gate.” *Id.* ¶ 138. Suzuki further explains that, as a result of the application of VCGM at t₅, “electrons remaining inside the channel of the NAND string NS coupled to the bit line BL_{prog} are pulled out to the bit lines BL, based on the fact that VSL has been applied to the program target bit line BL_{prog}.” *Id.* ¶ 140. Suzuki teaches that VCGM is a lower voltage than VPASS, and VREAD is a higher voltage than VCGM. *Id.* ¶¶ 138, 142.

In light of these disclosures in Suzuki, Petitioner does not adequately explain why VPASS corresponds to a “first bias voltage” in the “pre-verify stage.” In particular, neither Petitioner nor Dr. Liu sufficiently addresses the application of voltage VCGM to WL_{sel} and WL_{usel} immediately prior to the verification operation. In contrast, Dr. Przybylski explains:

Notably, the voltage applied during the time period t₃–t₄, across all the various different word lines, are the same as the voltages applied from t₁–t₂ at the start of the programming operation when the device begins boosting. *See* Suzuki, Fig. 11. These voltages are indicative of an “end operation of the program operation” which occurs as the device begins to recover from the high VPGM voltages applied during the programming operation. *See* Suzuki, Fig. 11. Moreover, the voltages applied from the

time period t3–t4 do not themselves help prepare the device for a verify operation, and most of the voltages being applied during that time period—including the voltages applied to the selected word lines, unselected word lines, bit lines (BLprog and BLinh) and source lines (SL)—are replaced with other values prior to the verify operation that takes place from time period t6–t9.

Ex. 2003 ¶ 126. Dr. Przybylski further explains:

At time t3, the only change from the programming operation is that the voltage applied on the selected word line (WLsel) drops from programming voltage “VPGM” that was used to program the selected word line to the same “VPASS” that was applied from time period t1–t2. *See* Suzuki, [0133]–[0135], [0137]. The remaining voltages, including the bit line voltage on the “program-inhibited bit line BLinh” that inhibits unselected memory strings from unintentional programming, remain the same. *Id.* In contrast, the period from t5–t6 is a ready operation of the verify operation. This is when voltages are applied in order to prepare the device for the verify operation beginning at t6.

Id. ¶ 127 (emphasis omitted).

Based on Suzuki’s disclosures and Dr. Przybylski’s testimony, we are persuaded that Suzuki’s “recovery operation” includes the end operation of the program operation from time period t3 to t4, and a separate ready operation of the verify operation from time period t5 to t6. Ex. 1007 ¶¶ 131–140; Ex. 2003 ¶¶ 125–131. As a result, we disagree with Petitioner that Suzuki’s entire recovery operation (time period t3 to t6) is a “pre-verification stage.” *See* Pet. 81–82; Ex. 1003 ¶¶ 205–206; Ex. 1027 ¶¶ 81–82. Because VPASS is applied during the end operation of the programming operation in time period t3 to t4 (and not the ready operation of the verify operation in time period t5 to t6), we are not persuaded that Petitioner sufficiently establishes that VPASS is “a first bias voltage” applied “in the pre-verify stage” as recited in claim 1.

For the reasons set forth above, we determine that Petitioner does not establish by a preponderance of the evidence, that independent claim 1, and claims 2–6 depend, directly or indirectly, therefrom, are anticipated by Suzuki.

F. Obviousness over Costa and Seo

Petitioner contends that claims 1–6 would have been obvious over the combined teachings of Costa and Seo. Pet. 103–131.

1. Overview of Costa

Costa “is directed to reducing errors when sensing in non-volatile memory.” Ex. 1008 ¶ 28. Costa teaches that “[r]ead or verify operations are performed using bias conditions that are dependent on the position of a selected memory cell within a group of non-volatile memory cells.” *Id.* Costa explains that “[d]uring sensing, the selected memory cell receives a read or verify voltage, referred to as a reference voltage, while the remaining memory cells receive a read or verify pass voltage that, for at least a subset of the memory cells in the group, is applied dependent upon the position of the selected memory cell in the group.” *Id.* In particular, Costa teaches “the disclosed technology varies the pass voltage applied to at least a subset of the memory cells of the group during sensing based on the memory cell selected for programming.” *Id.* ¶ 30. As an example, Costa teaches that, during program verification, the pass voltage “is increased as programming progresses from memory cells nearest a first select gate, such as a source select gate coupled to a source line, toward a second select gate such as drain select gate coupled to a bit line for the group.” *Id.* According to Costa, “[t]he increased pass voltage increases the channel conductance when programming later programmed memory cells” so that “the final distribution of threshold voltages for the group of memory cells may be more consistent

and narrow,” and “causes the channel to have a similar resistance when programming all of the memory cells of the group.” *Id.*

Costa describes an embodiment where “a group of memory cells, or group of word lines for a block of memory cells including the group, is partitioned into ranges or zones of one or more memory cells of the group.” Ex. 1008 ¶ 32. Costa teaches that “[o]ne or more control circuits apply bias conditions for sensing to the group that are based on the zone associated with the selected memory group or word line.” *Id.* Costa further teaches that “[g]enerally, a lower pass voltage is applied to these memory cells when the selected word line is a lower zone corresponding to earlier programmed memory cells closer to a first select line,” and “[t]he pass voltage is increased for higher zones corresponding to later programmed memory cells closer to a second select line.” *Id.* Costa also describes an embodiment where “the system applies a pass voltage to the subset of memory cells that is dependent upon the reference voltage applied to the selected word lines.” *Id.* ¶ 35. “For example, the system may use a lower pass voltage for the subset of memory cells when applying a higher read or verify reference voltage to a selected word line and a higher pass voltage when applying a lower read or verify reference voltage.” *Id.* Costa teaches that “[t]he higher reference voltage applied to the selected word line may increase the channel conductance such that a lower pass voltage can be applied to the subset of memory cells while maintaining sufficient channel conductance for sensing.” *Id.*

2. Overview of Seo

Seo is “directed to a memory device capable of improving a disturb phenomenon of an unselected memory string during a read operation.”

Ex. 1009 ¶ 8. The memory device includes a memory cell array having a

plurality of memory strings, a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation. *Id.* ¶ 9. “The memory device also includes control logic configured to control the voltage generating circuit to generate” first and second drain select line voltage applied to first and second unselected memory strings “among the unselected memory strings during the read operation, wherein the second drain select line voltage is different from the first drain select line voltage.” *Id.* Seo teaches that the second drain line voltage can be “at a potential level lower than the” potential level of the first drain line voltage. *Id.* ¶ 10.

Seo describes a read operation where a first voltage V1 is applied to first drain select line DSL0 and first source select line SSL0 corresponding to a selected memory string ST, and a second voltage V2 is applied to second drain select line DSL1 corresponding to the unselected memory string that shares first select source line SSL0, during a first time period t1. Ex. 1009 ¶ 88. Seo teaches that “second voltage V2 may have the same potential level as the first voltage level V1.” *Id.* Seo further teaches that “[s]ubsequently, the pass voltage Vpass may be applied to unselected word lines Unsel WLs,” then “the read voltage Vread may be applied to a selected word line Sel WL during a second time period t2.” *Id.* ¶¶ 89–90.

3. Analysis

Petitioner contends that the combined teachings of Costa and Seo disclose all of the limitations of claim 1. Pet. 103–112. Patent Owner responds that neither Costa nor Seo discloses or renders obvious a “pre-verify stage,” or that a POSITA would have been motivated to apply Seo’s teachings to Costa to render obvious a verify operation that includes a

distinct “pre-verify stage.” PO Resp. 59–61. Patent Owner also argues that the combined teachings of Costa and Seo do not disclose or render obvious “a first bias voltage” and “the second bias voltage is smaller than the first bias voltage” as recited in limitations [1.b] and [1.d]. *Id.* at 61–68.

Petitioner contends that “Costa discloses using its read operations to verify programming” and “the same selected cell is programmed and then verified.” Pet. 106 (citing Ex. 1008 ¶¶ 86–87, 93–94, Fig. 6). Petitioner further contends that Seo’s “first time period t_1 preceding a read/verify period t_2 ” is the “pre-verify stage” recited in the Challenged Claims. *Id.* at 106–107 (citing Ex. 1009 ¶ 90, Fig. 8); Ex. 1003 ¶ 249.

Seo teaches that the read operation includes the steps of selecting a page and memory string, setting the select transistor line voltage of the unselected memory string and apply period thereof, applying voltage to select lines of the unselected memory string, and applying the read voltage. Ex. 1009, Fig. 7. These voltage signals are illustrated in Seo’s Figure 8, reproduced below.

FIG. 8

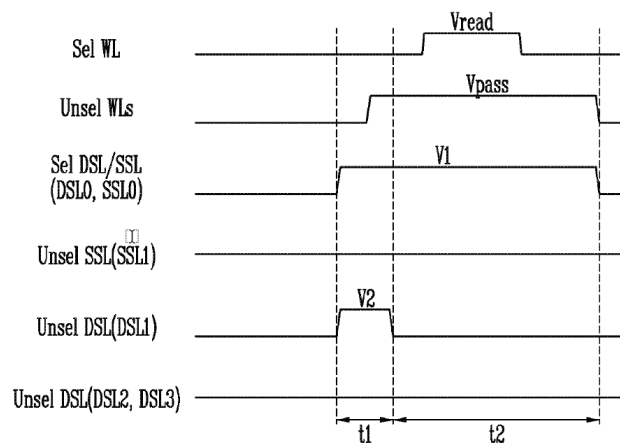


Figure 8 is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to an

embodiment described in Seo. *Id.* ¶ 19. During first time period t1, “second voltage V2 may be applied to the second drain select line DSL1 corresponding to the unselected memory string which shares the first source select line SSL0 with the selected memory string.” *Id.* ¶ 88. Also during first time period t1, pass voltage Vpass is applied to unselected word line Unsel WLs. *Id.* ¶ 89. At time period t2, “read voltage Vread may be applied to a selected word line Sel WL.” *Id.* ¶ 90.

Although Seo’s read operation includes two time periods during which different voltages are applied, we are not directed to, nor do we discern, any teachings in Seo that time period t1 is a pre-verify stage that is distinct from the verify/read stage. In that regard, Dr. Liu testifies that “Seo discloses *apply[ing], in a pre-verify stage* (a first time period t1 preceding a read/verify period t2)” without further explanation. Ex. 1003 ¶ 249 (alteration in original). As a result, we are not persuaded that Petitioner sufficiently establishes that Seo’s time period t1 is a pre-verify stage that is distinct from a verify/read stage.

For the reasons set forth above, we determine that Petitioner does not establish by a preponderance of the evidence, that independent claim 1, and claims 2–6 that depend, directly or indirectly, therefrom, would have been obvious over the combined teachings of Costa and Seo.

III. CONCLUSION

After reviewing the parties’ arguments and weighing the evidence offered by both parties, we determine that Petitioner does not show by a preponderance of the evidence that claims 1–6 of the ’957 patent would have been obvious over the combined teachings of Hongtao and Yu, or Costa and Seo. We also determine that Petitioner does not show by a preponderance of the evidence that claims 1–6 are anticipated by Suzuki.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–6	103	Hongtao, Yu		1–6
1–6	102	Suzuki		1–6
1–6	103	Costa, Seo		1–6
Overall Outcome				1–6

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not shown by a preponderance of the evidence that claims 1–6 of the '957 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

FOR PETITIONER:

Jeremy Lang
K. Herman
Travis Jensen
Johannes Hsu
ORRICK, HERRINGTON & SUTCLIFFE LLP
ptabdocketjl2@orrick.com
p52ptabdocket@orrick.com
t61ptabdocket@orrick.com
ptabdocketj1h1@orrick.com

FOR PATENT OWNER:

Christopher Bonny
Andrew Radsch
ROPES & GRAY LLP
christopher.bonny@ropesgray.com
andrew.radsch@ropesgray.com