

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00793
U.S. Patent No. 11,600,342
Issue Date: May 19, 2020

Title: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,600,342
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,600,342 to Chen et al.
1002	File History of U.S. Patent No. 11,600,342 to Chen et al.
1003	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
1004	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
1005	U.S. Patent Publ. No. 2021/0027848 A1 to Seo (“Seo”)
1006	U.S. Patent Publ. No. 2015/0003169 A1 to Nam et al. (“Nam”)
1007	Choi et al., “Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory,” 2016 Symposium on VLSI Technology, Digest of Technical Papers, 78-79 (“Choi”)
1008	U.S. Patent Publ. No. 2012/0151301 A1 to Izumi et al. (“Izumi”)
1009	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1010	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1011	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1012	U.S. Patent No. 9,589,978 to Yip
1013	Aritome, “NAND Flash Memory Technologies” (2016)
1014	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017

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Exhibit	Description
1015	U.S. Patent Publ. No. 2020/0168276 A1 to Yang
1016	U.S. Patent No. 9,620,233 to Dong et al.
1017	Micheloni, “3D Flash Memories” (2016)
1018	U.S Patent No. 10,276,251 B1 to Lobana et al.
1019	U.S Patent No. 9,361,993 B1 to Chen et al.
1020	Affidavit of Nathaniel E. Frank-White (Internet Archive) re Choi Reference (Ex. 1007)
1021	Declaration of Gordon MacPherson (IEEE) re Choi Reference (Ex. 1007)
1022	Certified File History of U.S. Patent No. 10,403,637 to Lue
1023	Wu et al., “Multiscale simulation of lateral charge loss in Si ₃ N ₄ 3D NAND flash based on density functional theory,” Journal of Physics D: Applied Physics, vol. 52, no. 39, 395103, 2019
1024	U.S. Patent Publ. No. 2019/0198117 A1 to Yu et al.
1025	U.S. Patent No. 10,121,529 B2 to Lee
1026	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1027	U.S. Patent Publ. No. 2020/0395372 A1 to Seo et al.
1028	U.S. Patent Publ. No. 2019/0348122 A1 to Ko et al.
1029	U.S. Patent Publ. No. 2016/0293271 A1 to Won et al.

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:
[1.A]	applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period;
[1.B]	applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and
[1.C]	applying, on an unselected word line, a pass voltage during the first time period and the second time period,
[1.D]	wherein the read-verification operation removes fast charges of the target memory cell during the first time period.
Claim 2:	
[2.A]	The method of claim 1, further comprising: applying, on a selected top select gate of a selected memory string containing the target memory cell, a top select gate voltage during the first time period and the second time period; and
[2.B]	applying, on a lower select gate of the selected memory string containing the target memory cell, a lower select gate voltage during the first time period and the second time period.

Ref. #	Listing of Challenged Claims
Claim 3:	
[3]	The method of claim 2, wherein the applying the top select gate voltage comprises electrically connecting the selected memory string to a bit line; and the applying the lower select gate voltage comprises electrically connecting the selected memory string to an array common source.
Claim 4:	
[4]	The method of claim 2, wherein the applying the pass voltage comprises applying the pass voltage with a delay period after the selected top select gate and the lower select gate are at the top select gate voltage and the lower select gate voltage, respectively.
Claim 5:	
[5]	The method of claim 1, further comprising: measuring a threshold voltage of the target memory cell during the second time period.
Claim 6:	
[6]	The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell.
Claim 8:	
[8]	The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is lower than a threshold voltage of an unselected memory cell.
Claim 9:	
[9]	The method of claim 1, wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V.

Ref. #	Listing of Challenged Claims
Claim 10:	
[10]	The method of claim 1, wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V.
Claim 11:	
[11]	The method of claim 1, wherein applying the off voltage comprises applying a voltage about 0V.
Claim 12:	
[12]	The method of claim 1, wherein the removing the fast charges comprises: removing the fast charges from a storage layer of the target memory cell.
Claim 13:	
[13]	The method of claim 1, wherein the removing the fast charges comprises: removing electrical charges from shallow traps in the storage layer of the target memory cell.
Claim 14:	
[14]	The method of claim 1, wherein the removing the fast charges comprises: removing the fast charges from the target memory cell to a neighboring unselected memory cell.
Claim 15:	
[15]	The method of claim 1, wherein conducting the read-verification operation comprises conducting a failed bit count in parallel.
Claim 16:	
[16.PRE]	A three-dimensional (3D) memory device, comprising:
[16.A]	a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein:

Ref. #	Listing of Challenged Claims
[16.A.i]	each memory string comprises a plurality of memory cells; and
[16.A.ii]	each memory cell is addressable through a word line and a bit line; and
[16.B]	a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:
[16.B.i]	apply, on an unselected top select gate of an unselected memory string, a prepare voltage during the first time period and an off voltage during a second time period;
[16.B.ii]	apply, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and
[16.B.iii]	apply, on an unselected word line, a pass voltage during the first time period and the second time period.
Claim 17:	
[17]	The 3D memory device of claim 16, wherein the circuit is further configured to: electrically connect a selected memory string containing the target memory cell to the bit line and an array common source by applying a top select gate voltage on a selected top select gate and applying a lower select gate voltage on a lower select gate during the first time period and the second time period.
Claim 18:	
[18]	The 3D memory device of claim 17, wherein to remove the fast charges of the target memory cell, the circuit is further configured to: apply the top select gate voltage on the selected top select gate and the lower select gate voltage on the lower select gate before applying the pass voltage on the unselected word line.

Ref. #	Listing of Challenged Claims
Claim 19:	
[19.PRE]	The 3D memory device of claim 16, wherein each memory string comprises:
[19.A]	a channel hole;
[19.B]	a core filling film in a center of the channel hole;
[19.C]	a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and
[19.D]	a channel layer sandwiched between the memory film and the core filling film.
Claim 20:	
[20]	The 3D memory device claim 19, wherein the circuit is further configured to remove the fast charges from a portion of the storage layer associated with the target memory cell.

I. INTRODUCTION

Petitioner Micron Technology, Inc. (“Petitioner”) respectfully requests *inter partes* review of claims 1-6 and 8-20 (the “Challenged Claims”) of U.S. Patent No. 11,600,342 (the “’342 patent”) assigned to Yangtze Memory Technologies Co., Ltd (“Patent Owner” or “PO”). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim.

The ’342 patent relates to a charge-trap 3D NAND memory device. The ’342 patent purports to address a fast-charge loss problem. Fast-charge loss involves—over time—the escape of shallowly-trapped particles from the charge-trap layer of a memory cell. Because of fast-charge loss, a read operation after a program operation may produce different results depending on *when* the read operation occurs. The ’342 patent purports to address this problem by removing fast charges during a “read-prepare” period before a read. Specifically, as shown below, the ’342 patent teaches (1) applying a voltage on an unselected word line, (2) grounding the selected word line, and (3) applying a voltage on an unselected string. The ’342 patent alleges that this creates an electrical field that causes the fast charges to de-trap. The Examiner allowed the claims because of (1) above.

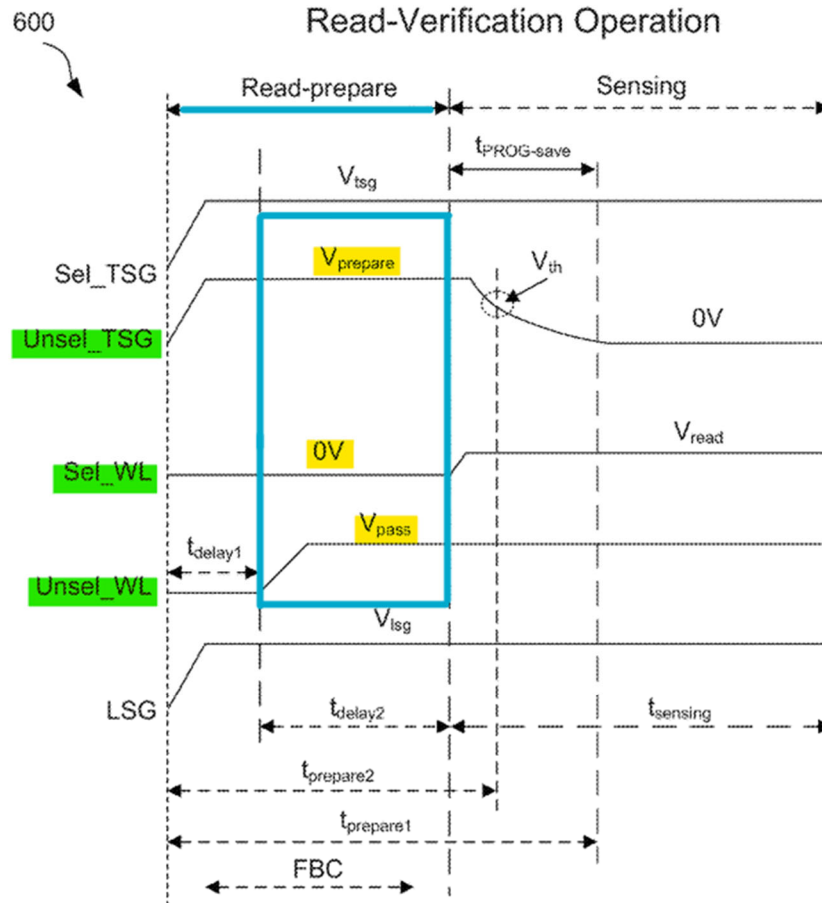


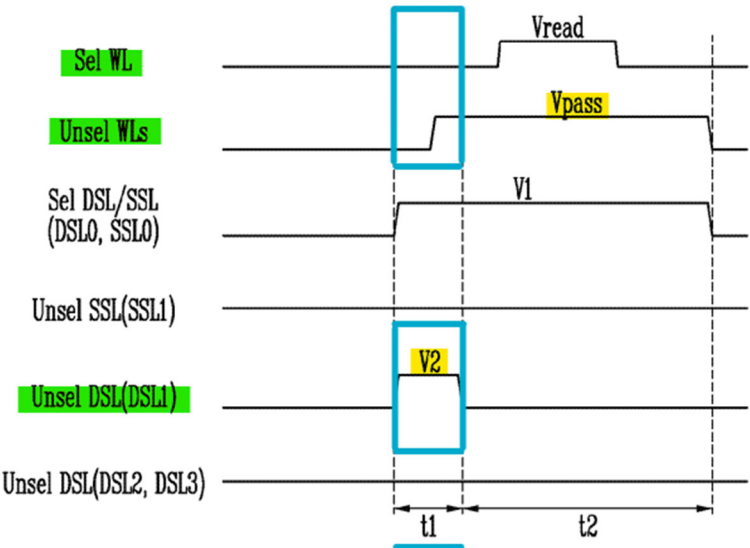
Fig. 6

Ex. 1001, FIG. 6 (annotated).

The Petition focuses on three references: Seo, Nam, and Choi. Seo and Nam disclose the heart of the '342 patent: the creation of an electrical field during a pre-read period. Choi explains that this electric field removes fast charges. These references were not cited or discussed during prosecution.

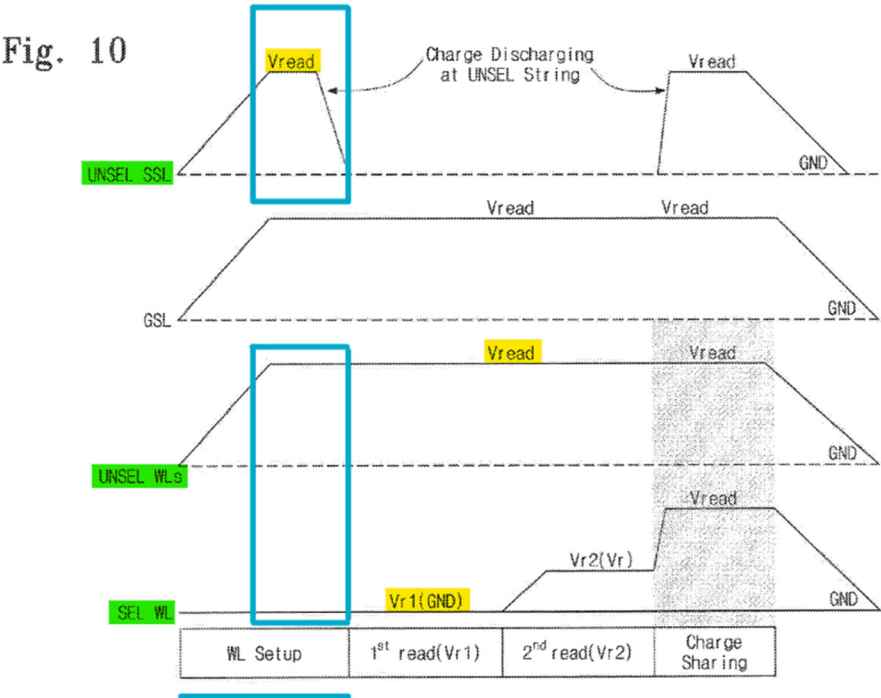
Just like the '342 patent, Seo creates an electric field before a read operation using the unselected word lines, selected word line, and unselected string:

FIG. 8



Seo, FIG. 8 (annotated).

Nam discloses the same:



Nam, FIG. 10 (annotated).

Choi teaches what removes fast charges: “a large lateral electric field.” Choi, 2:16-18. To the extent PO argues that a reference must expressly describe fast-charge removal (which is incorrect), this Petition combines each of Seo and Nam with Choi.

This Petition also relies on Izumi, which discloses the well-known technique of counting failed bits, for dependent claim 15.

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable as obvious under §103.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

PO has asserted the '342 patent and U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, and 11,501,822 in a co-pending litigation, *Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed Nov. 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378, IPR2024-00788, Petition for *Inter Partes*

Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342

Review of U.S. Patent No. 10,861,872, IPR2024-00789, Petition for *Inter Partes*

Review of U.S. Patent No. 10,868,031, IPR2024-00790, Petition for *Inter Partes*

Review of U.S. Patent No. 10,937,806, IPR2024-00791, Petition for *Inter Partes*

Review of U.S. Patent No. 10,950,623, IPR2024-00794, Petition for *Inter Partes*

Review of U.S. Patent No. 11,468,957, IPR2024-00792, and Petition for *Inter Partes*

Review of U.S. Patent No. 11,501,822, IPR2024-00795.

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

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PTABDocketJ3B3@orrick.com, PTABDocketJ1H1@orrick.com, and micron-

ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the '342 patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Micron was served with a Complaint alleging infringement of the '342 patent on November 14, 2023.

B. Identification of Challenged Claims and Statement of Precise Relief Requested

This Petition assumes that the '342 patent is entitled to the earliest priority date that it lists: October 23, 2019.

Petitioner relies on the following references: (1) U.S. Publ. 2021/0027848A1 (Ex. 1005, "Seo"), (2) U.S. Publ. 2015/0003169A1 (Ex. 1006, "Nam"), (3) *Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory*, 2016 Symposium on VLSI Technology, Digest of Technical Papers, 78-79 (Ex. 1007, "Choi"), and (4) U.S. Publ. 2012/0151301A1 (Ex. 1008, "Izumi"). These references are all prior art. See §VIII.

Petitioner challenges the claims on the following grounds:

Ground 1: Claims 1–6, 8–14, and 16–20 are obvious over Seo in view of Choi;

Ground 2: Claim 15 is obvious over Seo in view of Choi and Izumi;

Ground 3: Claims 1–3, 5–6, 8–14, 16–17, and 19–20 are obvious over Nam in view of Choi; and

Ground 4: Claim 15 is obvious over Nam in view of Choi and Izumi.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds for a §314 Discretionary Denial

There is a pending district court action involving the '342 Patent. Petitioner submits that it presents a compelling case of unpatentability and that the Board should not discretionarily deny. 6/21/22 Interim Procedure, 2, 4–5.

Further, the *Fintiv* factors weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“*Fintiv*”).

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group - Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 12 (similar).

2. Proximity of the Court's Trial Date

On February 22, 2024, the district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1009. As a result, if IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1010 (statistics indicating it takes on average 48.9 months to reach trial in the district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are months away from completing the exchange of infringement and invalidity contentions and have not taken any depositions. Fact discovery is in its infancy. Claim construction and expert discovery has yet to begin. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Against eight patents, Petitioner did so, filing approximately five months after being served with the original complaint and approximately two months after the filing of an amended complaint. *See* Ex. 1011. This also weighs strongly in favor of institution.

4. Issue Overlap

It is not yet possible to determine the amount of overlap. Regardless, should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense based on any ground in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

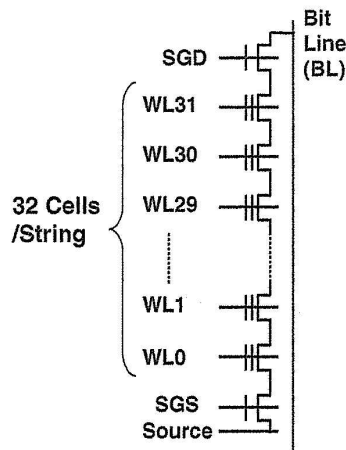
Neither Patent Owner nor the Examiner cited or discussed Seo, Nam, Choi, or Izumi during prosecution of the '342 patent. *See generally* Ex. 1002. Further, these references present noncumulative invalidity arguments, because each discloses applying a voltage on the unselected word lines during a pre-read period, unlike the prior art on which the Examiner relied. §V.C.

V. THE '342 PATENT

A. Technology Background

1. NAND Flash Structure

“Flash memory” is a form of “non-volatile memory.” Ex. 1012, 1:24-26 *see also* Ex. 1003 (“Liu”¹), ¶¶ 41-63. Flash memory cells, e.g., NAND cells, are arranged in “strings” with multiple cells “connected in series.” Ex. 1013, 38. The cells are surrounded by “select transistors (SGD, SGS),” one on the top (usually, drain side) and one on the bottom (usually, source side). *Id.*, 38-39. One such string is shown below:

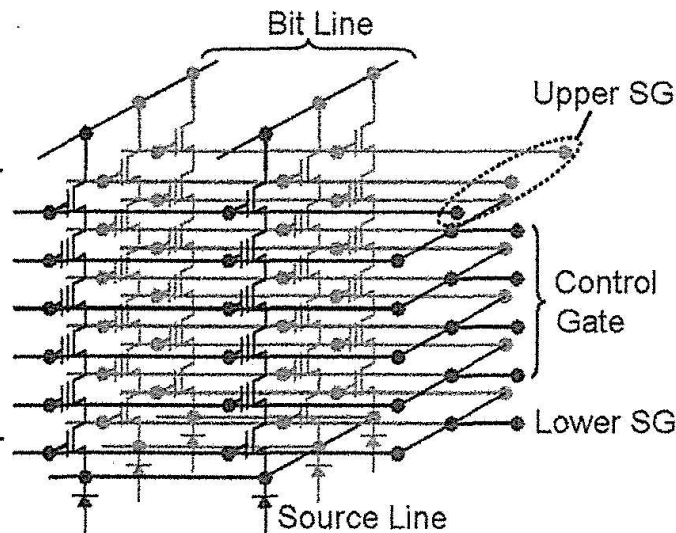


Id., 39.

Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. Ex. 1013, 38. But “three-dimensional (3D) NAND flash cells”

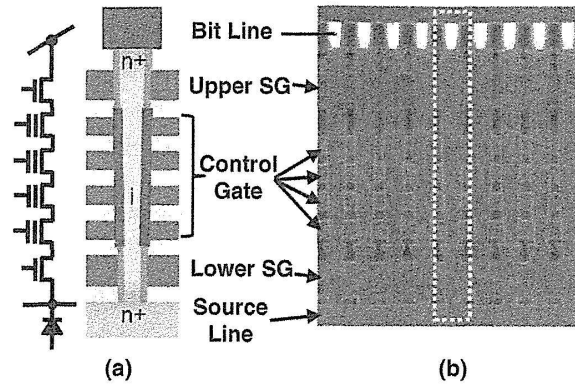
¹ David Kuan-Yu Liu, Ph.D. is a leading expert in the physics of read and interference issues in memories.

were developed. *Id.*, 292. 3D NAND structure is like “turning the 2D NAND string upside,” “resulting” in a “vertical channel.” Ex. 1014, 3. Memory cells (comprising transistors) are formed vertically by stacking alternating layers of metal and dielectric (e.g., oxide such as SiO₂) around a cylindrical pillar. Ex. 1013, 294-95. Each metal layer acts as the control gate (gate terminal) of a transistor. *Id.*, 295. Multiple such vertical pillars/channels are then repeated in a three-dimensional array:

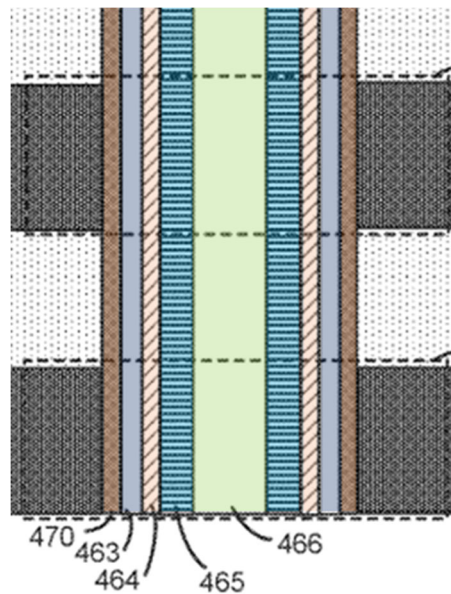


Id., 296. A particular vertical memory cell is selected using a word line and bit line, along with the select gates. *Id.*, 295-97.

An example 3D NAND vertical memory cell string with a charge-trapping layer is shown below:



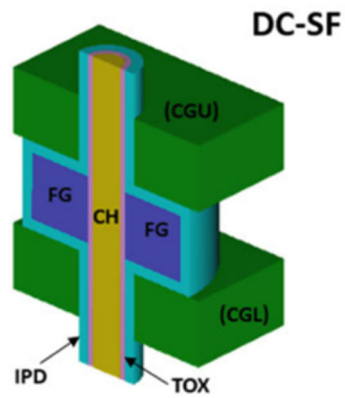
Ex. 1013, 296. The ONO sidewall of a memory-string pillar can comprise an oxide blocking layer (e.g., 470 below), a nitride charge-trapping or storage layer (463), and an oxide tunneling layer (464). Ex. 1015, [0083], Ex. 1016, 13:19-26.



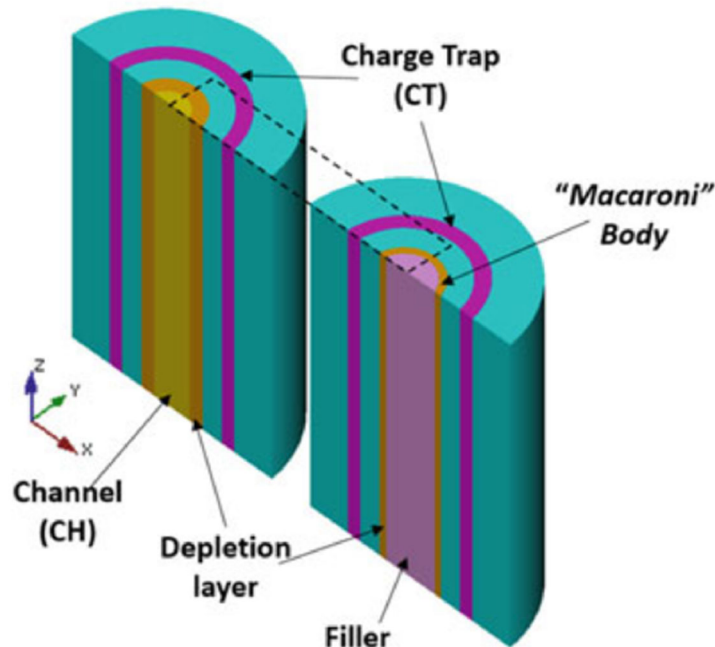
Ex. 1015, FIG. 4E (partial) (annotated).

The two most common types of 3D Flash memory cells are conductive floating gate memory cells and charge-trap memory cells. Because of the conductive

floating gates, the vertical memory string for this type is made with separated floating gates:



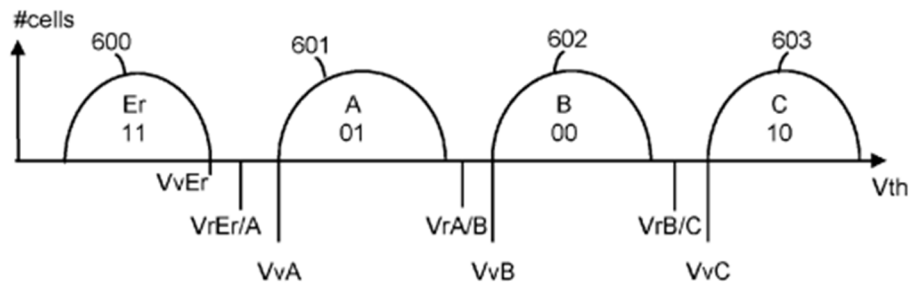
Ex. 1017, 145. Charge-trap technology, however, employs a non-conductive data storage portion, e.g., silicon nitride, and thus the charge-trap layer is not separated and merely extends through the entire vertical string:



Id., 106.

2. 3D NAND Flash Operation

A memory cell is programmed to store a data state, which corresponds to a threshold voltage (V_{th}), by storing some amount of charge in its charge-storage material. A two-bit-per-cell NAND memory may have a V_{th} -versus-data-state distribution:



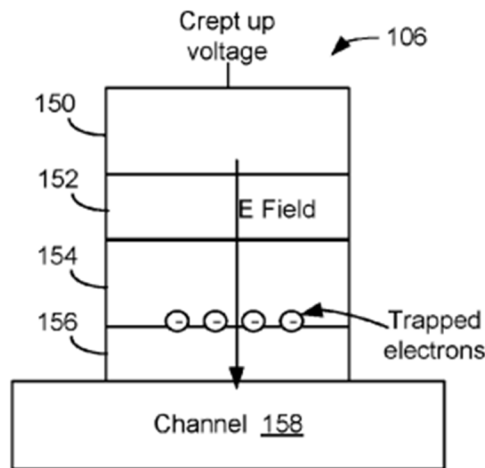
Ex. 1016, FIG. 6. The threshold value of the erase state is typically a negative value, while the data states are positive values. Ex. 1013, 312.

During read operations, all cell transistors on a selected memory string except the selected cell to be read are given a pass voltage that is higher than the highest V_{th} of all possible data states. Ex. 1016, 3:21-27, 3:33-37. A read voltage between two data states is applied to the control gate of the selected cell to determine its state. *Id.*, 3:10-29, 9:66-10:15, 14:31-37; Liu, ¶¶ 64-65.

NAND device programming involves a cycle: a programming pulse, a read operation to verify programming success, and then if necessary, repeating the process until reaching the correct data state. Ex. 1018, 10:43-47; Ex. 1019, 11:50-

52. This verify operation can be identical to the read operation described above (using a verify voltage). Ex. 1018, 16:16-21; Ex. 1019, 17:10-13; Liu, ¶ 67.

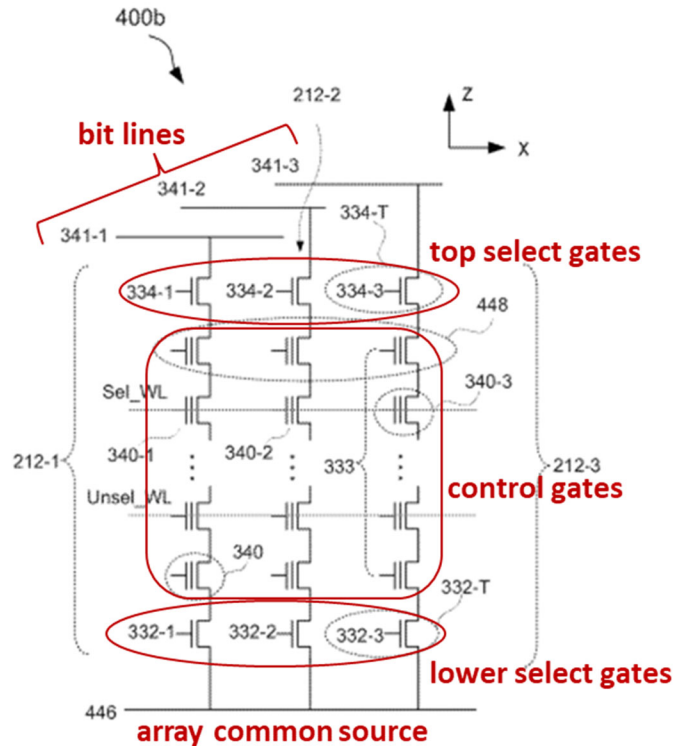
Data storage using charge trap technology has a drawback in that charges may escape (i.e., de-trap) over time. Ex. 1013, 327. Electric fields can cause de-trapping which, over time, can alter the intended data state. *Id.*, Ex. 1016, 3:52-59, 17:12-17.



Ex. 1016, FIG. 1A; Liu, ¶ 68.

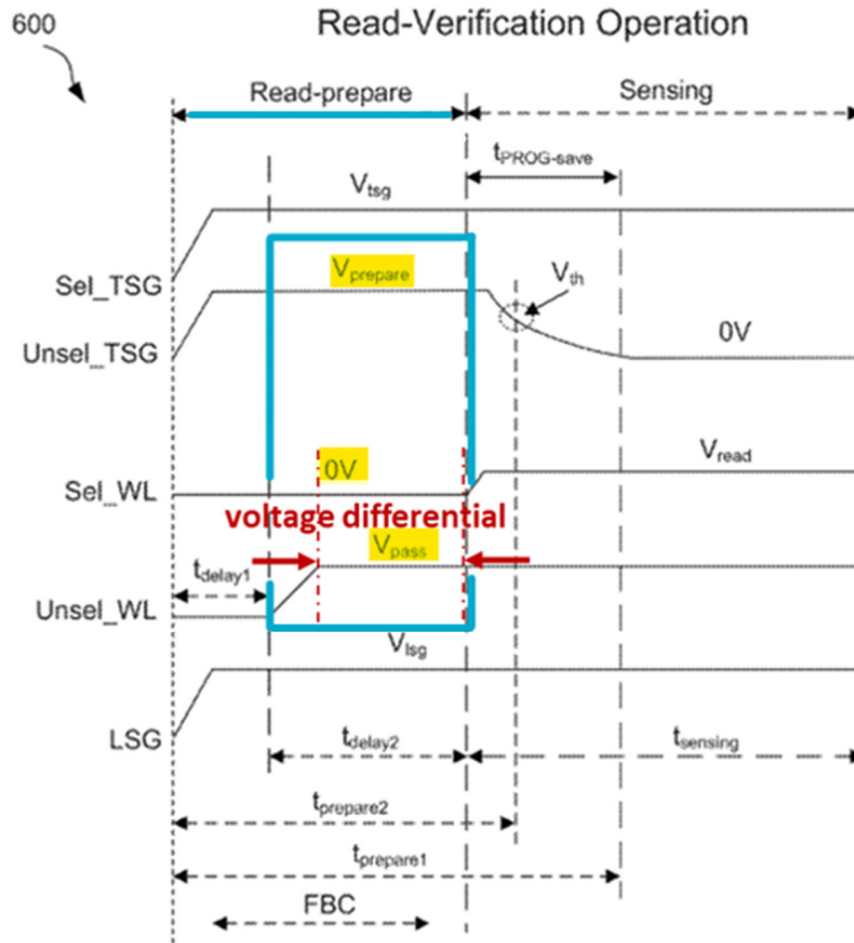
B. Overview of the Patent

The '342 patent relates to a read-verification operation for charge-trapping 3D NAND. Ex. 1001, Abstract, 1:29-32, 7:15-22. The 3D NAND has a conventional structure:



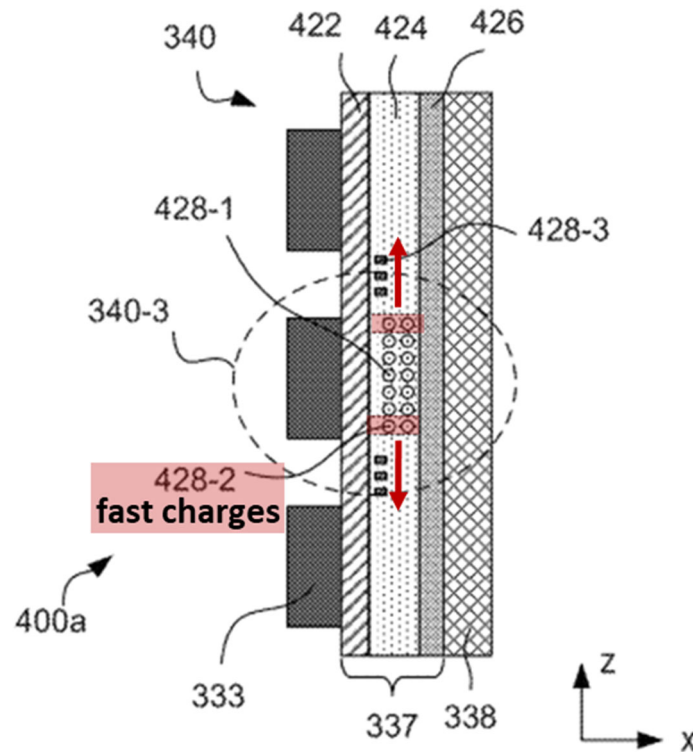
Id., FIG. 4B (annotated); 7:51-8:4.

The '342 patent acknowledges the problem of de-trapping in charge-trap memories, i.e., the de-trapping after a program can create read errors. Ex. 1001, 1:29-36. It purports to address this drawback by “removing fast charges of the target memory cell at a read-prepare step” before a read/sensing operation. *Id.*, Abstract, FIGs. 6-8. “Removing the fast charges of the target memory cell includes applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).” *Id.*



Id., FIG. 6 (annotations added). The prepare voltage turns on the unselected top select gate (Unsel_TSG), i.e., the unselected string. *Id.*, 8:67, 12:56-62. The pass voltage, which is applied to Unsel_WL during the read-prepare and sensing periods, is a term of art and turns on the unselected word lines (Unsel_WL). Liu, ¶ 75.

The differential between V_{off} on a selected word line and V_{pass} on neighboring, unselected word lines generates an electric field, which exerts a force to “de-trap the fast charges 428-2 from the shallow traps, pull[ing] them towards the neighboring unselected memory cells.” Ex. 1001, 12:24-34.



Id., FIG. 4A (annotated); Liu, ¶ 76.

C. Prosecution History

During prosecution, the claims were rejected as anticipated by U.S. Publication 2019/0371394 (to Yang). Ex. 1002, 271-274. Applicant successfully distinguished Yang by arguing that during the first time period, zero volts is “applied” to the “unselected word lines.” *Id.*, 311-312, 321-323.

VI. CLAIM CONSTRUCTION

The Board applies the same *Phillips* claim construction standard used by district courts. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). For purposes of this petition, Petitioner submits that the ’342 patent’s claim terms

do not require further construction and can be afforded their plain and ordinary meaning.

This Petition, however, addresses the claims' use of "applying" voltages "during" particular "time period[s]." The '342 patent makes clear that the claims do not require applying these voltages throughout a given time period. For example, claim 1 recites "applying, on an unselected word line, a pass voltage during the first time period..." Ex. 1001, Claim 1. As recited in dependent claim 4 and as can be seen below, the pass voltage V_{pass} is not applied throughout the first ("Read-prepare") time period:

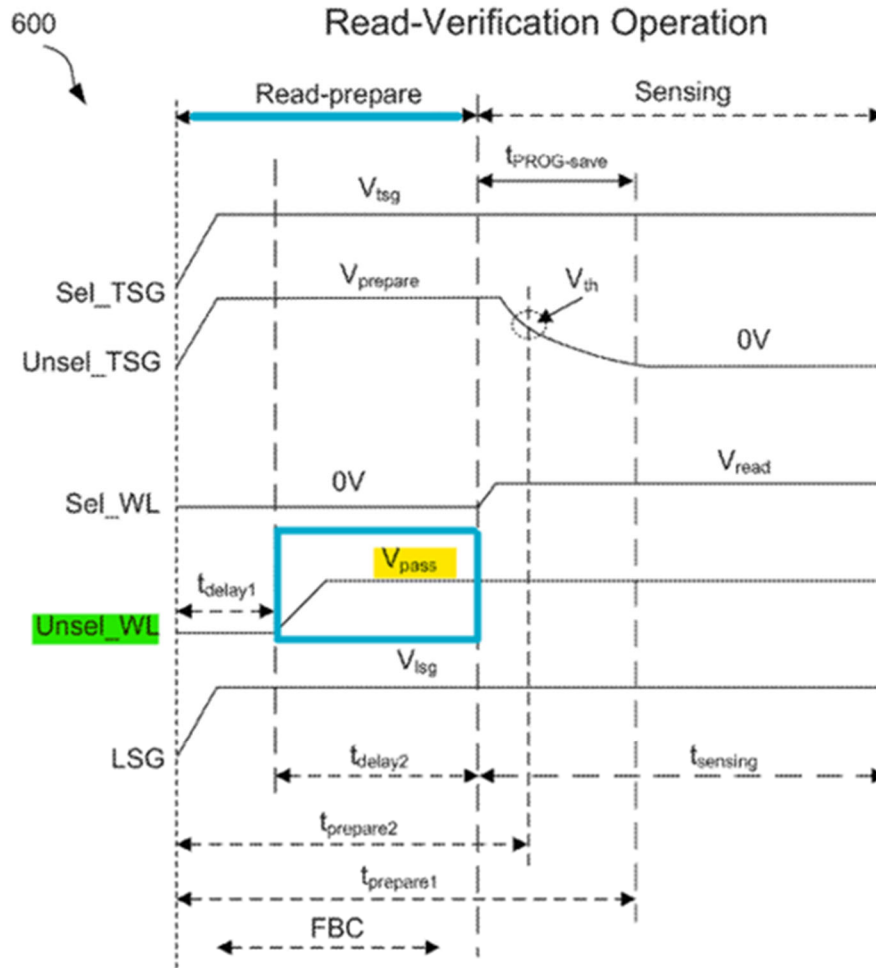


Fig. 6

Id., FIG. 6; *see also id.*, Claim 4 (reciting the corresponding “delay period”); Liu, ¶¶ 83-86.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '342 patent would have had a master's degree in electrical engineering or a similar discipline, along with 4-5 years of professional experience working with (e.g., researching, designing, or developing) NAND flash

memory devices (including issues relating to the operation, e.g., reading of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). Liu, ¶¶ 35-39.

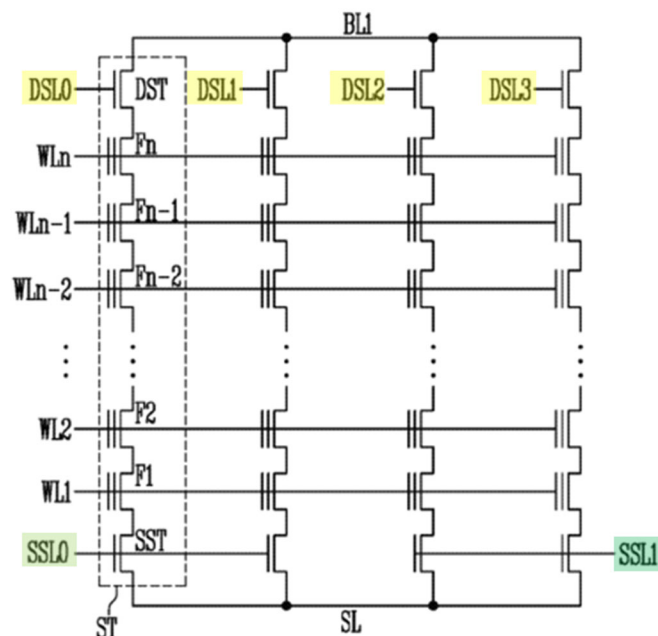
VIII. PRIOR ART OVERVIEW

A. Seo

Seo was filed on October 18, 2019, and was published on January 28, 2021.

Seo, Cover. Seo is prior art under 35 U.S.C. §§102(a)(1)-(2) (AIA).

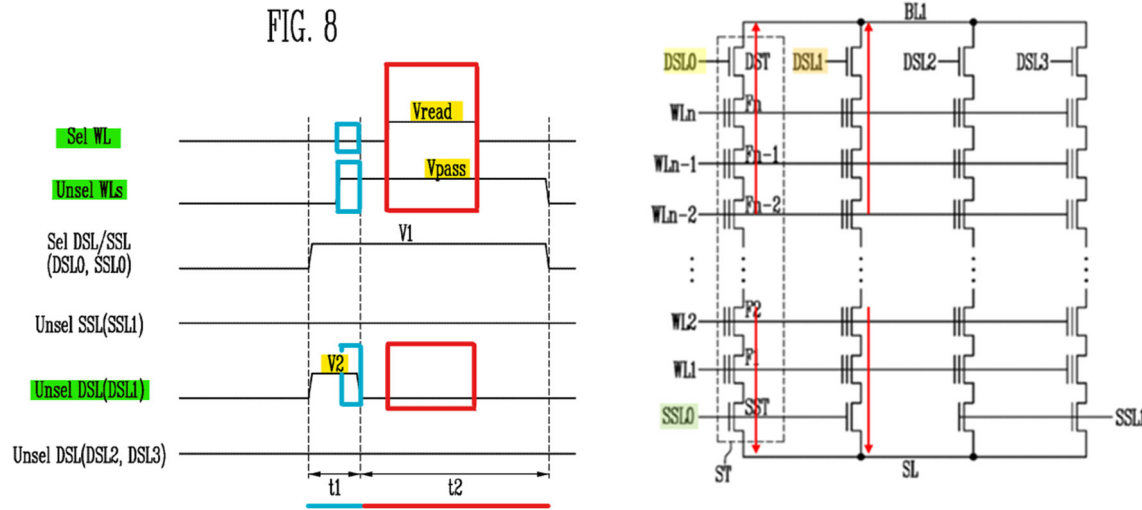
Seo is directed to read operations of nonvolatile memory devices such as 3D NAND flash memory. Seo, Abstract, [0004]-[0007]; Liu, ¶¶ 89-93. Seo’s memory devices comprise memory strings with individual drain select lines (“DSL”) and partially shared source select lines (“SSL”).



Seo, FIG. 4 (annotated).

Seo is focused on reducing a disturbance known as hot carrier injection (“HCI”) occurring on an unselected memory string during read operations. Seo, [0008], [0048]. Specifically, the high gate voltage on unselected memory cells can cause hot electrons to be injected into an adjacent cell and disturb its data state. Ex. 1013, 254. By applying DSL and SSL voltages *before* the read operation, Seo controls channel voltages of the relevant memory strings via coupling to bit lines and source lines, reducing HCI. Seo, [0048], [0088]-[0089]; Liu, ¶ 91.

As shown below, during t1, (1) a high pass voltage is applied to the unselected word line (“Unsel WLS”), (2) an off voltage, ground, is applied to the selected word line (“Sel WL”), and (3) a high prepare voltage, V2, is applied to the unselected string (“Unsel DSL”). During t2, (1) a high pass voltage is applied to the unselected word line, (2) a read voltage, Vread, is applied to the selected word line, and (3) an off voltage, ground, is applied to the unselected string.



Seo, FIGs. 8, 4 (annotated).

Seo's method creates an electric field that removes fast charges, just like the '342 patent. Liu, ¶ 93.

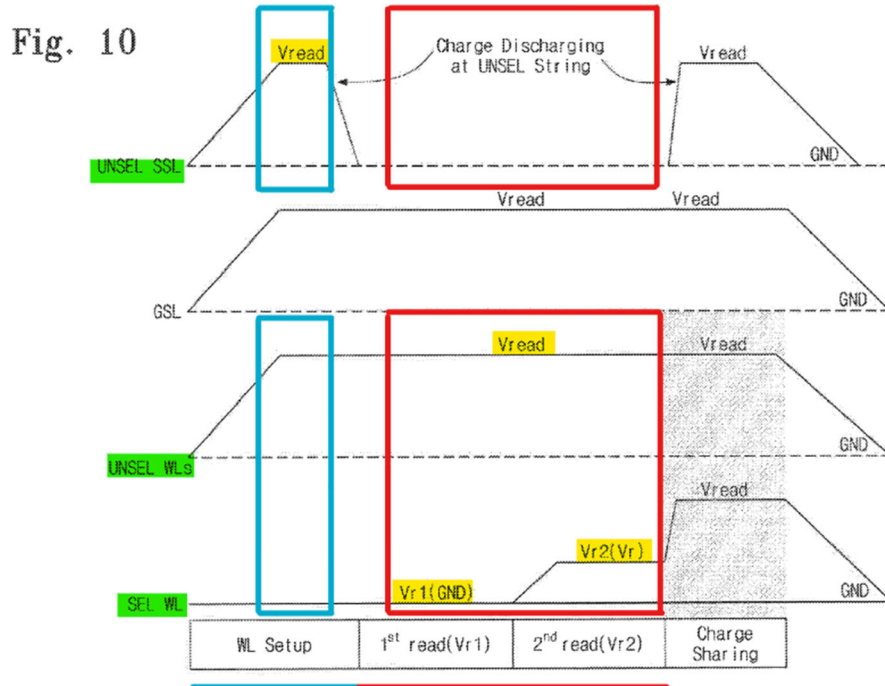
B. Nam

Nam was published on January 1, 2015. Nam, Cover. Nam is prior art under 35 U.S.C. §§102(a)(1)-(2) (AIA).

Nam relates to read-verify operations of conventional 3D NAND flash memory devices. Nam, Abstract, [0029], [0065], [0155], [0164], Fig. 2A; *See* Liu, ¶¶ 94-98. Nam discloses immune disturbance read modes to control channel charges before and after read operations, though Nam's focus is on the post-read period. Nam, [0070].

As shown below, during WL Setup, (1) a high pass voltage, Vread, is applied to the unselected word line ("Unsel WLS"), (2) an off voltage, ground, is applied to the selected word line ("Sel WL"), and (3) a high prepare voltage, Vread, is applied

to the unselected string (“Unsel SSL”). During the 1st and 2nd read period, (1) a high pass voltage, V_{read} , is applied to the unselected word line, (2) read voltages, V_{r1} and V_{r2} , are applied to the selected word line, and (3) an off voltage, ground, is applied to the unselected string.



Nam, FIG. 10 (annotated).

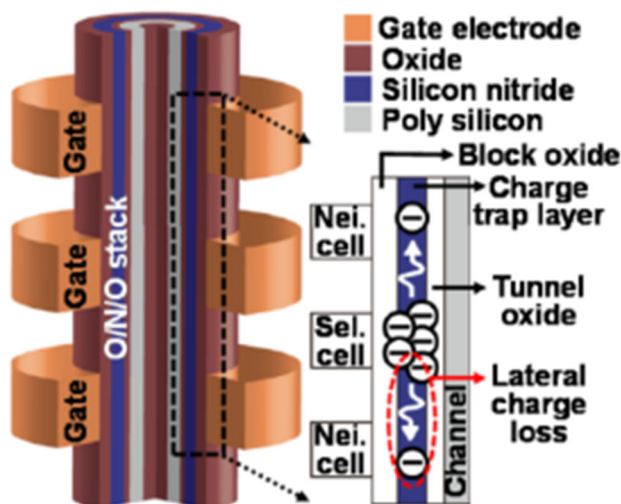
Nam’s method creates an electric field that removes fast charges, just like the ’342 patent. Liu, ¶ 98.

C. Choi

Choi was presented at the IEEE 2016 Symposium on VLSI Technology Digest of Technical Papers. Choi; Ex. 1020, Ex. B. Choi was published online at IEEE Xplore on September 22, 2016. Ex. 1021. This Symposium is an annual event

dating back decades. *See Nanya Tech. Corp. v. Lone Star Silicon Innovations, LLC*, IPR2018-00062, Paper 7 at 2, 4 n.3 (PTAB Apr. 25, 2018) (instituting trial based on a paper from the 1999 counterpart publication). The Symposium was announced and discussed on industry websites and on social media in advance and its program was archived. Ex. 1020, Exs. A-B. Choi is cited in pre-'342 patent publication and non-patent literature. Exs. 1022-1023. Choi is prior art to the '342 patent under 35 U.S.C. §102(a)(1) (AIA) and was publicly and readily accessible by a POSITA before 2019. Liu, ¶ 99.

Choi documents an evaluation of fast-charge loss in charge-trap 3D NAND Flash memory.



Choi, FIG. 1 (annotation in original).

Choi evaluates fast-charge loss, which occurs within seconds of cell programming (which Choi refers to as “early retention”²) and which causes undesirable drifts in threshold voltages. Choi, 1:16-24. Choi found that lateral fast-charge loss (i.e., in a direction parallel to the length of a memory string) is the “primar[y]” mechanism of early retention. *Id.*, 1:26-32, 2:48-52, 1:9-12. Choi explains that “a large lateral electric field is generated at the edge of the cell in which there is a greater chance for stored charges in a charge trap layer to spread laterally.” *Id.*, 2:16-18. “[T]he edge of the cell” refers to an interface with an adjacent cell, as Figure 1 above illustrates. Thus, the charges move to neighboring cells. Liu, ¶¶ 99-103.

As shown below, within “a few sec[onds]” after programming, the threshold voltage may shift and lead to “a verification fail.”

² Choi discusses “fast charge loss within a few seconds, which is referred to as early retention.” Choi, Abstract.

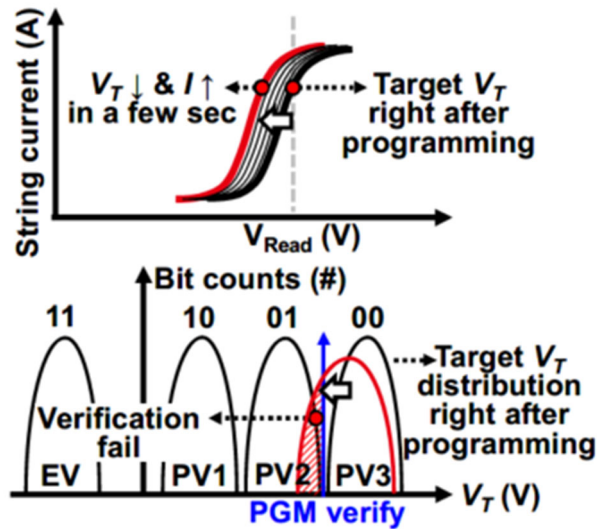


Fig. 2. Schematic of the early retention and its effect on V_T and I . The early retention threatens the MLC capability and the tight V_T distribution.

Choi, Fig. 2. Fast-charge loss is an issue because the threshold value being verified will change unless fast-charge loss occurs before verification. Liu, ¶ 104.

D. Izumi

Izumi was published on June 14, 2012. Izumi, Cover. Izumi is prior art under 35 U.S.C. §§102(a)(1)-(2) (AIA).

Izumi also is directed to read operations of nonvolatile charge-storage memory devices such as NAND flash. Izumi, Abstract, [0003], [0018], [0041], Fig. 2. To reduce power consumption, during read-verification operations, Izumi's method counts the number of failed bits and selectively activates only the necessary ECC circuitry. *Id.*, [0003]-[0004], [0077], [0081]-[0084]; Liu, ¶ 106.

IX. THE '342 PATENT'S CLAIMS ARE OBVIOUS

A. ***Ground 1: Claims 1-6, 8-14, and 16-20 Are Obvious Over Seo in View of Choi***

Seo in view of Choi and the knowledge of a POSITA renders claims 1-6, 8-14, and 16-20 obvious. Liu, ¶¶ 107-08.

1. **Claim 1**

[1.Pre] “A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:”

To the extent the preamble is limiting, Seo discloses, or at least renders obvious, the preamble.

Seo discloses a method of reading a “[*m*]emory device” with “a *memory cell* array” (Seo, Abstract),³ which is “*three-dimensionally* structured.” *Id.*, [0050]; *see also* [0004] (“Flash memory,” as “NOR” or “NAND”), [0006] (“Flash memory,” including “*three-dimensional semiconductor devices*.” Thus, Seo discloses 3D Flash memories. Liu, ¶¶ 109-11.

Seo’s “memory cells” are “*read*” by a “*read operation*.” Seo, Abstract; [0072]. Seo’s read operation is on a *target memory cell*, i.e., at the intersection of the selected word line (“Sel WL”) and “selected memory string.” *Id.*, [0089]-[0090], FIG 5, §V.A.1-2. Thus, Seo discloses *[a] method for conducting a read-verification*

³ Emphasis added unless otherwise noted.

*operation on a target memory cell in a three-dimensional (3D) memory device.*⁴ Liu, ¶ 112.

Seo would have been understood to disclose its read operation for verification. Liu, ¶¶ 113-17. Seo generally discloses its read operation, and as was well known, a fundamental use of a read operation was for verification after a program. *See* §V.A.2. What’s more, Seo discloses embodying its invention in devices that “program.” Seo, [0108]. Verification is necessarily part of programming in flash memories, and thus Seo would have been understood to disclose using its read operation after the “program operations” that it references. *See* §V.A.2.

At the very minimum, Seo in view of Choi renders it obvious to perform Seo’s read operation immediately after a program operation to verify successful programming. *See* Choi, FIG. 2 (verification), §IX.A.19 (motivations).

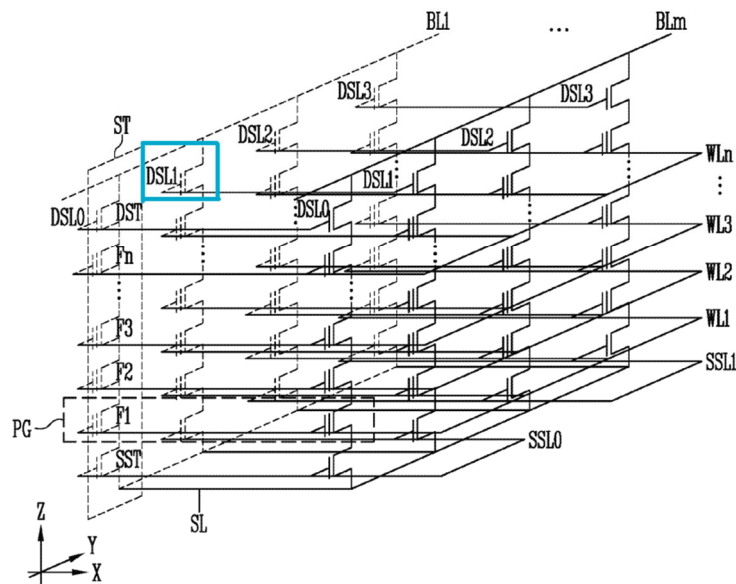
[1.A] “applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period”

Seo discloses this limitation.

In Seo, each “drain select transistor” (“DST”), to which a “drain select line[]” (“DSL”) connects, is a *top select gate of a ... memory string*. Seo, [0048], [0055].

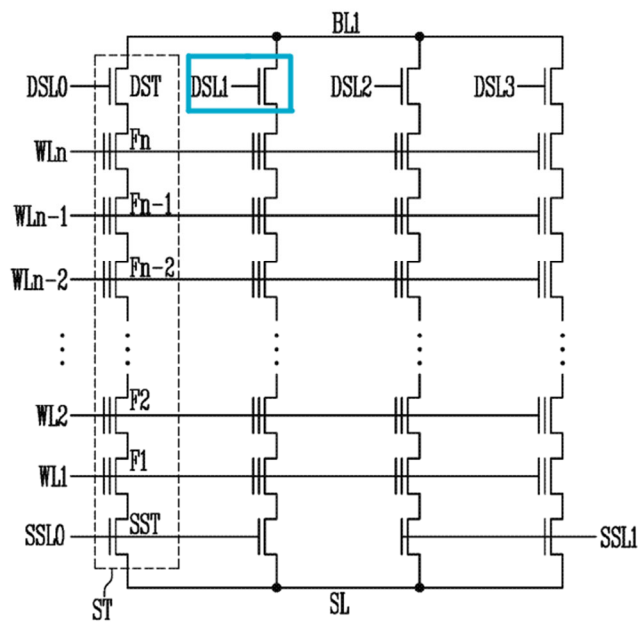
⁴ For clarity, the claim mapping portion uses red italics for claim language.

FIG. 3



Id., FIG. 3 (annotated).

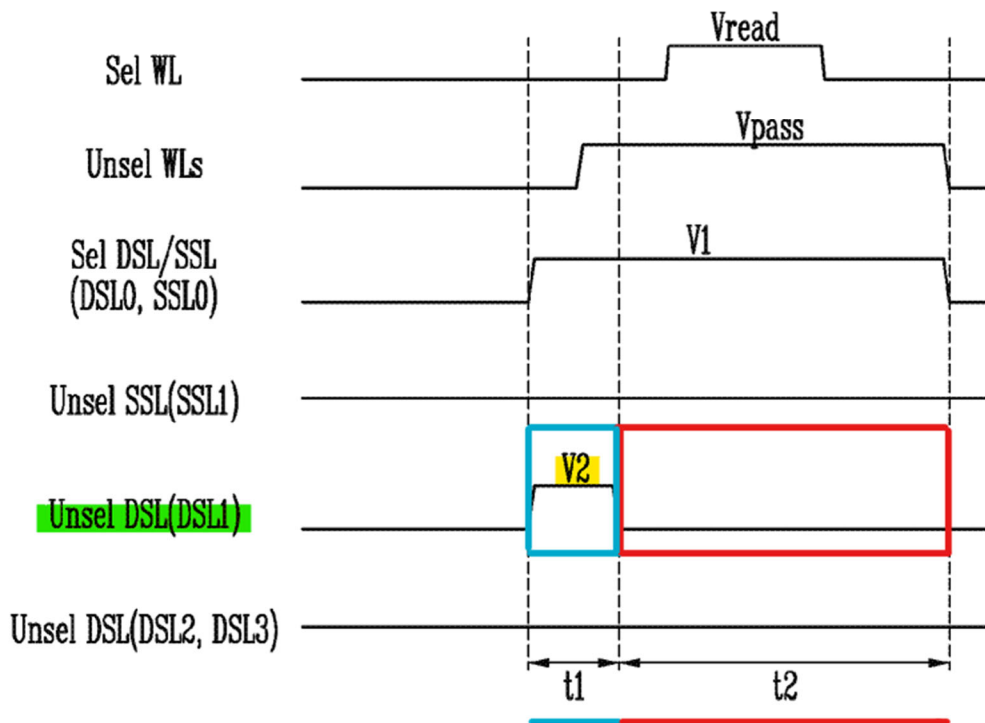
FIG. 4



Id., FIG. 4 (annotated).

Figure 8, shown below, illustrates a read operation. Seo, [0086]. t_1 corresponds to *a first time period* and t_2 corresponds to *a second time period*. As part of the read operation, a “voltage V2”—the *prepare voltage*—is *applied* to “DSL1” that “correspond[s] to the unselected memory string.” *Id.*, [0088]. This voltage turns on DSL1 (*id.*) as does the ’342 patent’s *prepare voltage* (Ex. 1001, 12:56-62). The voltage application on an unselected DSL occurs *during* (at a point in the course of) the *first time period* (“ t_1 ”)—followed by a low voltage, e.g., ground (V_{ss}) being applied—*an off voltage*—*during a second time period* (“ t_2 ”).

FIG. 8



Seo, FIG. 8 (annotated), [0075], [0088]-[0089].

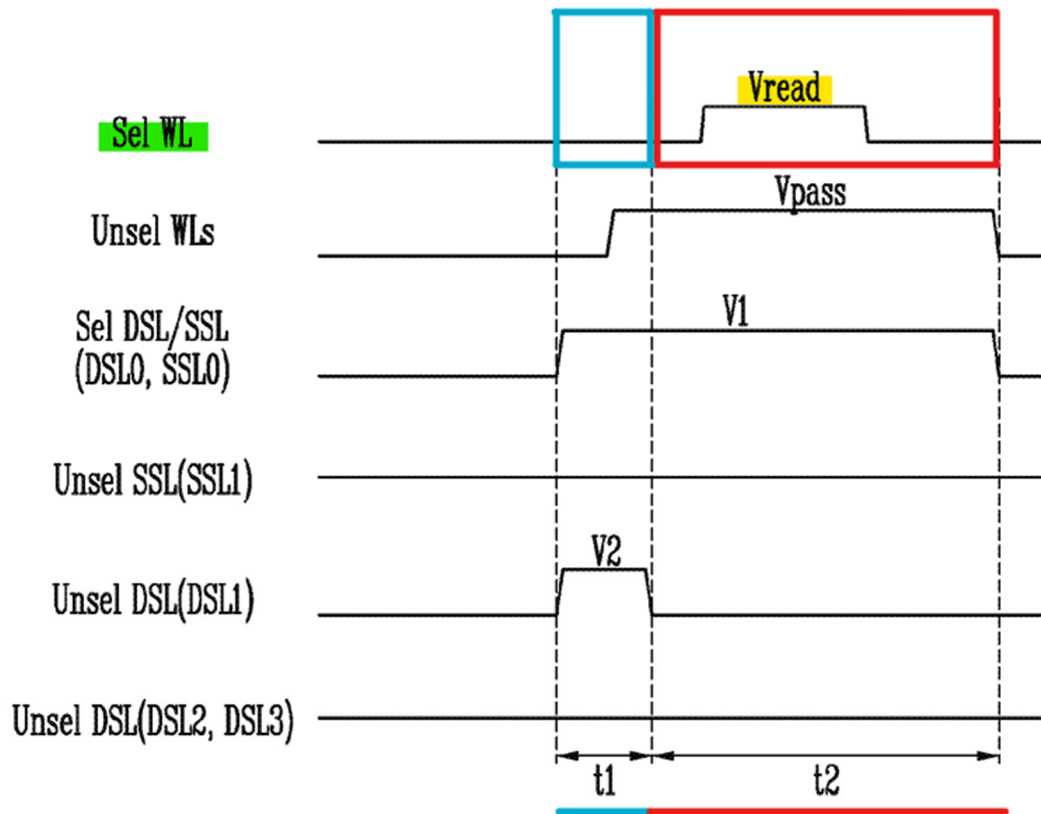
Thus, Seo discloses *applying, on an unselected top select gate of an unselected memory string* (e.g., Unsel DSL (DSL1)), *a prepare voltage during a first time period* (e.g., V2 during t1) *and an off voltage during a second time period* (e.g., off voltage during t2). Liu, ¶¶ 118-22.

[1.B] “applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period;”

Seo discloses this limitation.

As shown below, a zero voltage—an *off voltage*—is applied to a *selected word line* (“Sel WL”) during “t1” (the *first time period*), and the “*read voltage Vread* may [then] be *applied*” during “t2” (the *second time period*). Seo, [0088]-[0090].

FIG. 8



Id., FIG. 8 (annotated).

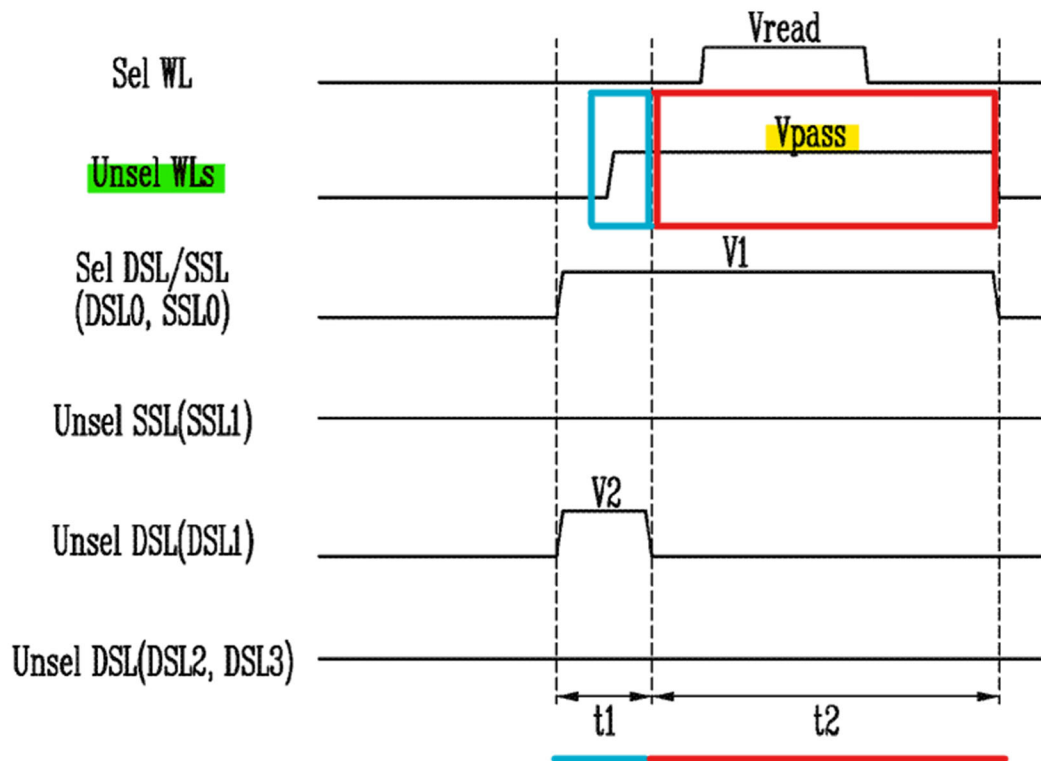
Thus, Seo discloses *applying, on a selected word line associated with the target memory cell* (e.g., Sel WL), *the off voltage during the first time period* (0 volts during t1) *and a read voltage during the second time period* (Vread during t2). Liu, ¶¶ 123-25.

[1.C] “applying, on an unselected word line, a pass voltage during the first time period and the second time period,”

Seo discloses this limitation.

Seo discloses that a “*pass voltage* V_{pass} ” is applied to “*unselected word lines*” (“Unsel WLs”) during the *first* and *second time periods*, t_1 - t_2 . Seo, [0082], [0083], [0089].

FIG. 8



Id., FIG. 8 (annotated).

Thus, Seo discloses *applying, on an unselected word line* (e.g., Unsel WLs), *a pass voltage during the first time period and the second time period* (e.g., V_{pass} during t_1 and t_2). Liu, ¶¶ 126-28.

[1.D] “wherein the read-verification operation removes fast charges of the target memory cell during the first time period.”

Seo discloses this limitation or, at least, renders it obvious in view of Choi.

In the context of charge-trap memories, the ’342 patent discloses that “[r]emoving the fast charges of the target memory cell includes” applying the voltages of limitations [1.A]-[1.C]. Ex. 1001, Abstract. As §§IX.A.1[1.A]-[1.C] demonstrate, Seo discloses these voltages. Specifically, Seo teaches having a higher voltage on unselected WLs (e.g., adjacent WLs to the selected WL) *during the first time period*. §§IX.A.1.[1.B]-[1.C]. As the ’342 patent recognizes, this voltage differential removes fast charges. See Ex. 1001, 12:24-34, VII.C; Liu, ¶¶ 129-31.

Seo discloses, or would have been understood to disclose, charge-trap 3D memories. Liu, ¶¶ 133-36. Recall that Seo discloses that its read operation is for a 3D Flash memory device. §IX.A.1[1.Pre]. Charge-trap memory is a type of 3D memory device, and what’s more, suffers from the “disturb phenomenon” that Seo specifically addresses (Seo, [0008]). Ex. 1017, 101, 108. And a charge-trap memory was one of two basic types of 3D Flash memory devices. *Id.*, 101, 144. Indeed, charge-trap memories were incredibly popular, textbook material in 2019. *Id.*, 101. Thus, Seo discloses, and would have been understood to disclose, performing its read operation on charge-trap memories, which removes fast charges. Liu, ¶ 136.

To the extent that PO argues that Seo does not disclose a “charge-trap” memory or removal of “fast charges” (which is incorrect), Seo in view of Choi

renders obvious claim [1.D], because it would have been obvious to employ Seo's read operation in a 3D charge-trap memory with the knowledge that it removes fast charges in view of Choi. *See* §IX.A.19. Choi specifically discloses a "3-D NAND flash memory with a charge trap layer." Choi, 1:16-17. Choi addresses the issue of "early retention (fast charge loss within a few seconds)." *Id.*, Title. "[S]hallowly trapped electrons" are more likely to be lost due to lateral movement when "a large lateral electric field is generated at the edge of the [memory] cell," i.e., near the interfaces with adjacent cells. *Id.*, 1:28-29, 2:4-25, FIG. 1. The lateral electron movement from the selected memory cell to its neighboring memory cells (labeled "[l]ateral charge loss" though appearing vertically in the figure due to the orientation of the memory string) is shown below:

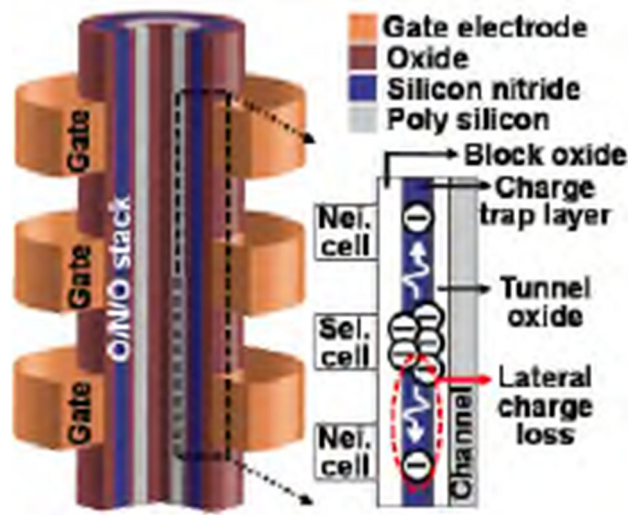


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Id., FIG. 1 (annotation in original). Seo creates such “a large lateral electric field.” Accordingly, it would have been obvious to employ Seo’s read operation in Choi’s charge-trap memory with Choi’s express disclosure of removing fast charges. Liu, ¶¶ 137-38; §IX.A.19.

Accordingly, Seo discloses, or at least in view of Choi renders obvious, *wherein the read-verification operation removes fast charges of the target memory cell during the first time period* (e.g., voltage differential on the WLs during t1 creates an electric field that removes charges from charge-trap memory cells). This removal would occur any time a read occurs within a few seconds of a program operation, e.g., during verification. Choi, 1:2-5; Liu, ¶ 139.

2. Claim 2

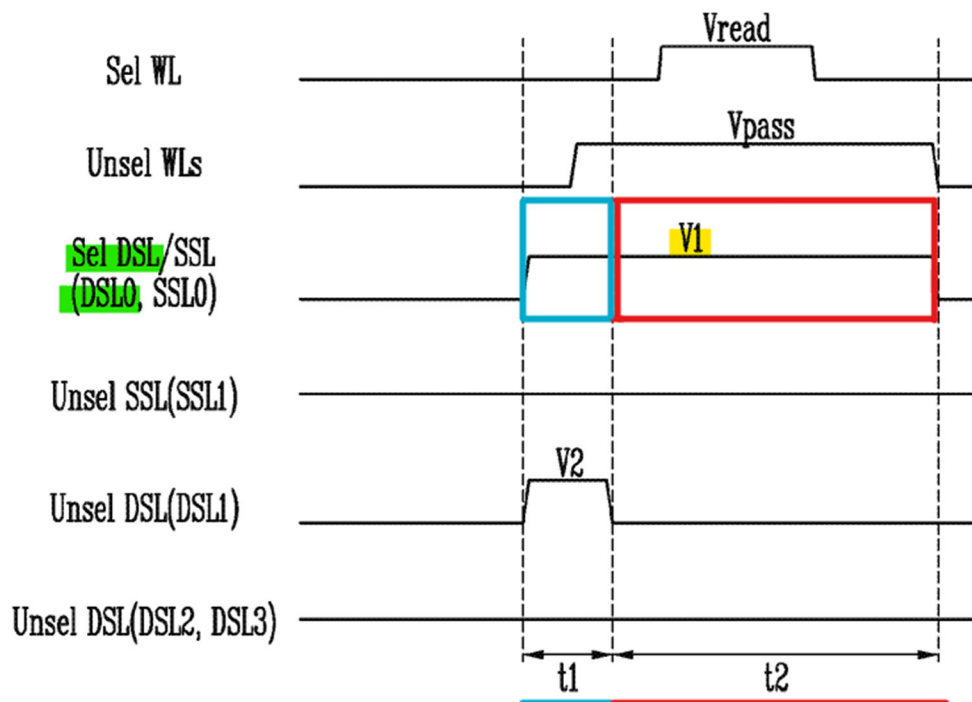
Claim 2 depends from claim 1 and further requires:

[2.A] “applying, on a selected top select gate of a selected memory string containing the target memory cell, a top select gate voltage during the first time period and the second time period;”

Seo discloses this limitation.

Recall that Seo’s DSLs connect to the *top select gate[s]*, DSTs. See Limitation [1.A]; Seo, [0074]. *[D]uring the first time period and the second time period*, a “voltage V1 may be applied” to “DSL0” that “correspond[s] to [the] selected memory string ST,” which turns on the transistor. *Id.*, [0088].

FIG. 8



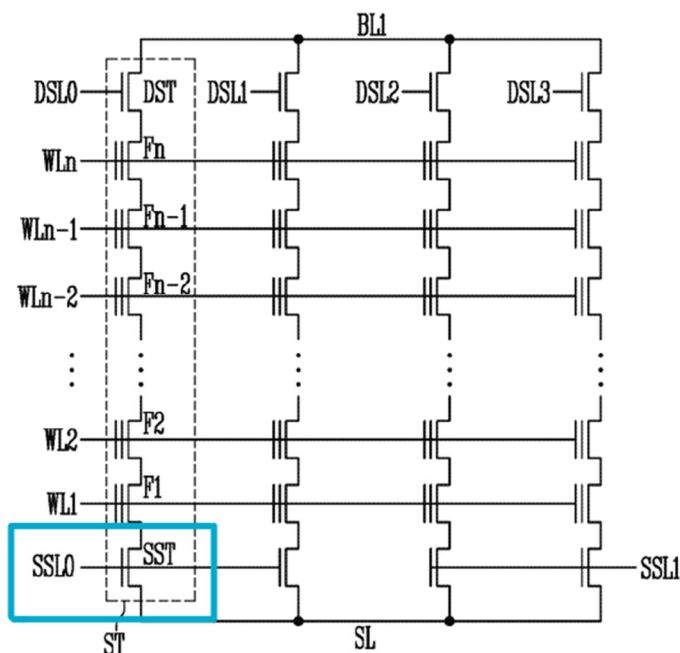
Id., FIG. 8 (annotated).; Liu, ¶¶ 141-42.

[2.B] “applying, on a lower select gate of the selected memory string containing the target memory cell, a lower select gate voltage⁵ during the first time period and the second time period.”

Seo discloses this limitation.

Seo discloses “source select transistor[s]” (each a “SST”), i.e., *lower select gate[s]*, to which “source select line[s]” (“SSL”) connect. Seo, [0055].

FIG. 4

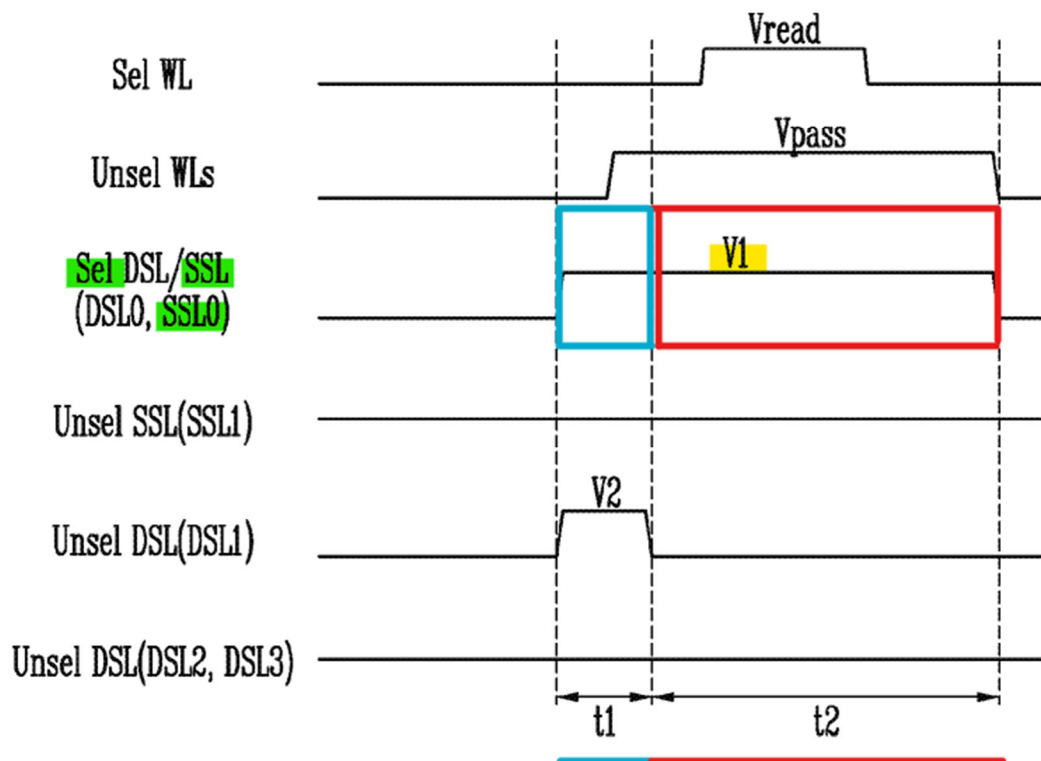


Id., FIG. 4 (annotated).

⁵ For both select gates, the '342 patent provides examples of 4-7 voltages, which turn on the respective transistors. Ex. 1001, 2:9-12, 11:11-27. The V1 voltage of Seo does the same. Seo, [0088].

As part of the read operation, *during the first time period and the second time period*, a “**voltage V1**” is applied to “the first source select line SSL0” that “correspond[s] to [the] *selected memory string ST*” (“Sel SSL”). See, [0088]; *see also id.*, [0079].

FIG. 8



Id., FIG. 8 (annotated); Liu, ¶¶ 143-45.

3. Claim 3

Claim 3 depends from claim 2 and further requires:

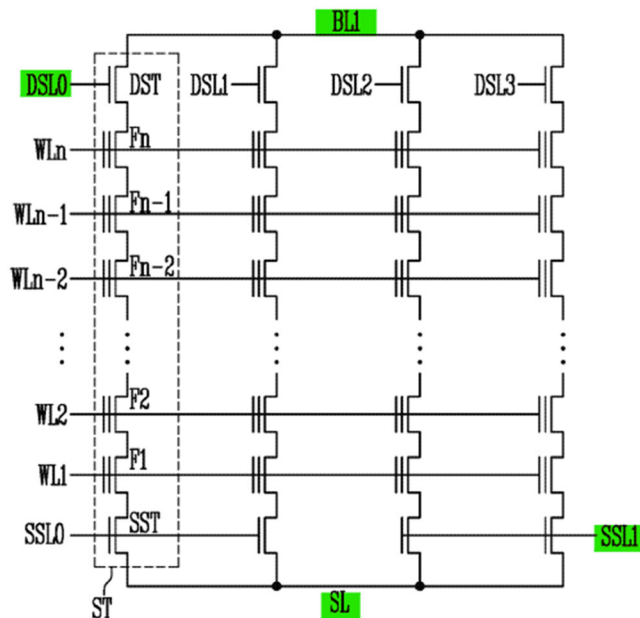
[3] “wherein the applying the top select gate voltage comprises electrically connecting the selected memory string to a bit line; and the applying the lower select gate voltage comprises electrically connecting the selected memory string to an array common source.”

Seo discloses this limitation.

Recall that the *top select gate* corresponds to Seo’s DST (coupled to DSL), and the *lower select gate* corresponds to Seo’s SST (coupled to SSL). Limitations [1.A], [2.B].

The DSL couples the memory string to a “bit line,” and the SSL couples the memory string to a common “source line.” Seo, [0038], [0055].

FIG. 4



Id., FIG. 4 (annotated). *[A]pplying the top select gate voltage (V1) electrically connect[s] the selected memory string (selected memory string ST) to a bit line*

(BL1); and the applying the lower select gate voltage (V1) comprises electrically connecting the selected memory string (selected memory string ST) to an array common source (SL). *Id.*, [0088] (“V1 may be a voltage to turn on” the drain/source transistors); Limitation [2.A, B], Seo, FIG. 8.

As shown above, the “source line” is an *array common source* because the source is common to the array. *Id.*, see also *id.*, FIG. 3. This is just like the *array common source* (446) of the '342 patent.

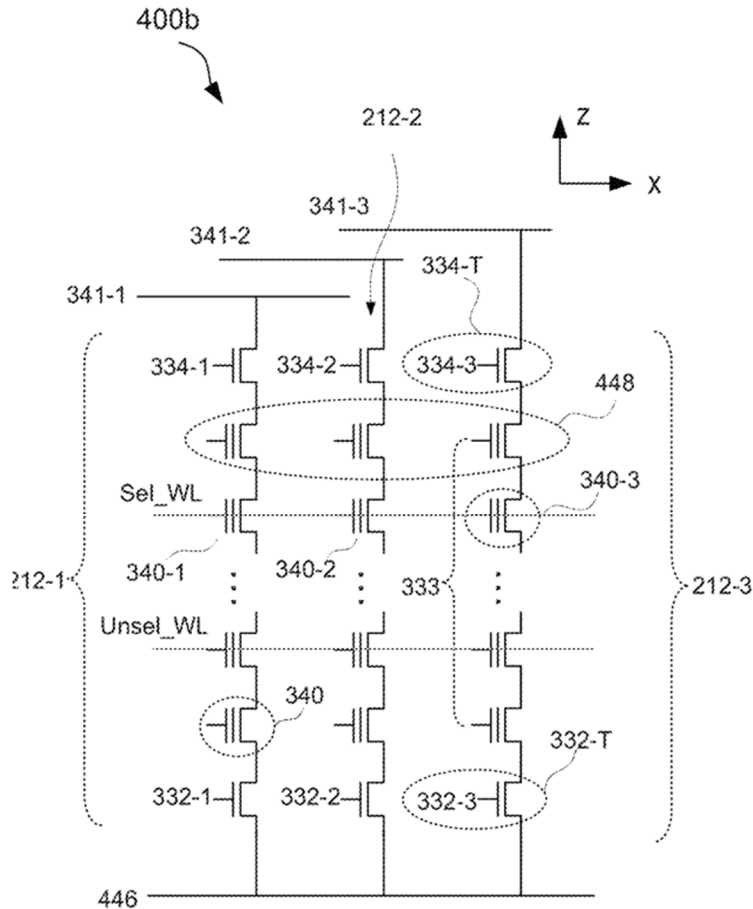


Fig. 4B

Ex. 1001, FIG 4B, 8:1-4; Liu, ¶¶ 147-50.

4. Claim 4

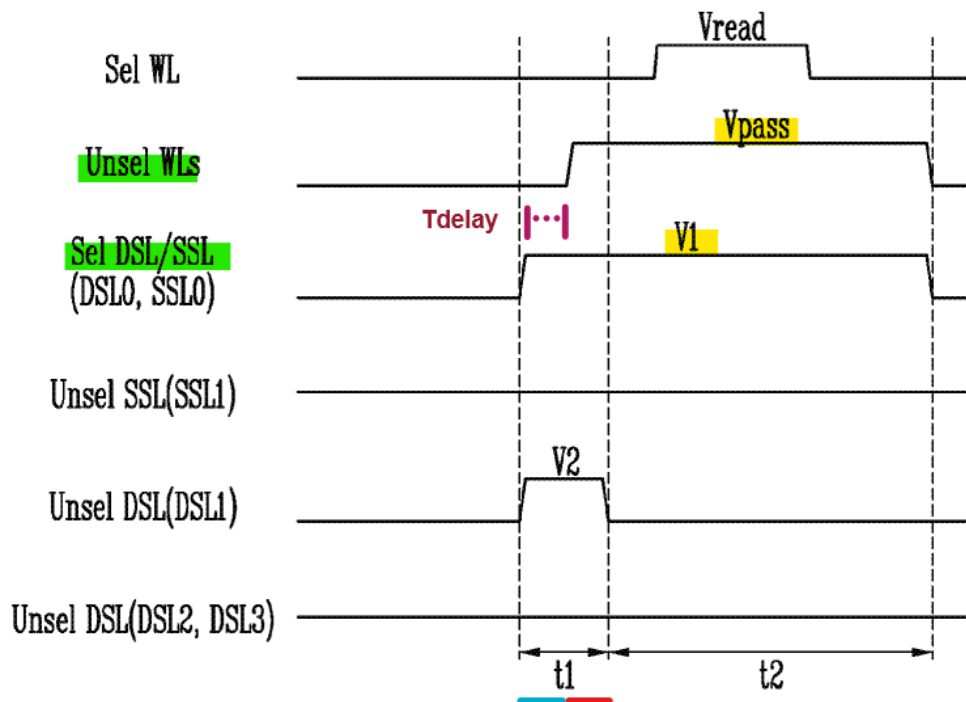
Claim 4 depends from claim 2 and further requires:

[4] “wherein the applying the pass voltage comprises applying the pass voltage with a delay period after the selected top select gate and the lower select gate are at the top select gate voltage and the lower select gate voltage, respectively.”

Seo discloses this limitation.

Seo discloses *applying the pass voltage* on an unselected word line (V_{pass}), and $V1$ on both the *selected TSG* and *selected LSG*. See Limitations [1.C], [2.A], [2.B]. This “ V_{pass} ” is “applied” “subsequently” to voltage $V1$ —indicative of the *delay period*. Seo, [0089].

FIG. 8



Id., FIG. 8 (annotated); Liu, ¶¶ 152-53.

5. Claim 5

Claim 5 depends from claim 1 and further requires:

[5] “measuring a threshold voltage of the target memory cell during the second time period.”

Seo discloses this limitation.

The '342 patent correlates this limitation with a read operation. Ex. 1001, 10:60-11:3 (using a Vread voltage to “read or measure” the threshold voltage).

Seo discloses, or renders obvious in view of Choi, a read-verification operation. *See* Limitation [1.Pre]. More specifically, Seo discloses measuring *a threshold voltage* by applying “Vread” “during a second time period t2” to “Sel WL,” which is connected to the target memory cell (*see* limitation [1.B]). Seo, [0090]; Liu, ¶¶ 155-57.

6. Claim 6

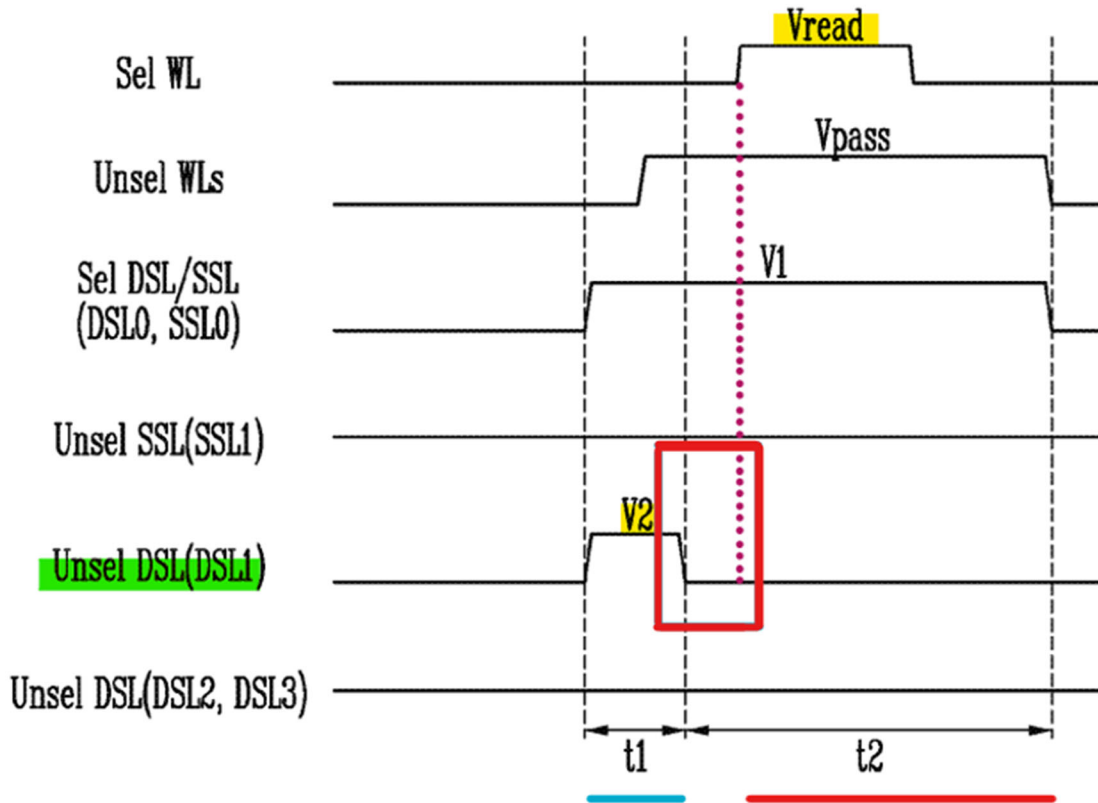
Claim 6 depends from claim 1 and further requires:

[6] “wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell”

Seo discloses, or at least renders obvious, this limitation.

Seo’s *read voltage* is Vread on Sel WL, and the voltage of the unselected top select gate is Seo’s Unsel DSL. *See* limitations [1.A]-[1.B]. Accordingly, this limitation corresponds to the below:

FIG. 8



Seo, FIG. 8 (annotated). When *applying the read voltage* occurs, the voltage on *the unselected top select gate* (Unsel DSL1) is 0V. As described below, it would have been understood, or at least obvious, that 0V is *higher than a threshold voltage of an unselected memory cell*, e.g., an erased cell. Liu, ¶¶ 159-66.

As an initial matter, recall that programmed memory cells typically have a positive threshold voltage, and erased memory cells have a negative threshold voltage. See §V.A.2; Liu, ¶¶ 65, 167.

An erase operation will erase the entire block, i.e., an array of memory strings. Ex. 1017, 91-93; *see also* Seo, [0108] (recognizing “erase”). Thus, after an erase and the first programming operation, there will necessarily be erased and programmed unselected cell(s).

Further, after the erase, the programming will typically occur from top to bottom or from bottom to top, e.g., program the lowest row of memory cells, then the next one up, etc. Ex. 1024, [0115], [0130]. After the first program, a program operation will involve both unselected programmed and erased cells.

Each approach, bottom to top or top to bottom, was an obvious implementation of Seo. Such techniques were conventional (see above). Further, each approach was beneficial. First, each approach provides for easily knowing the state of the rows above and below the selected row, enabling access operations that reduce disturb issues. Ex. 1025, 8:18-53. Second, a sequential program order simplifies controller decoding operation. Third, it would be necessary to implement a programming scheme for Seo’s device, and these sequential programming schemes were well understood. Each approach was highly predictable and routine to implement, because each approach merely involves using a pointer that increments either up or down. Liu, ¶¶ 164-65.

With either approach, a read on any but the most top or the most bottom row involves unselected memory cells that are erased (e.g., above) and programmed

(e.g., below). Thus, *an unselected memory cell*, e.g., an erased cell, will have a negative threshold voltage, and *a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell*.

7. Claim 8⁶

Seo discloses, or at least renders obvious, the additional limitation of claim 8.

This limitation is identical to claim 6 except that it requires the *unselected top select gate* voltage to be *lower*, instead of higher, than *an unselected cell[s] threshold voltage*.

The claim refers to when *the unselected top select gate* (Unsel DSL1) is 0V. See Limitation [6]. As described above, it would have been understood, and certainly obvious, that unselected rows will include programmed cells, in which case *the unselected top select gate* is *lower* than the threshold voltage of the programmed, unselected memory cells (positive values). See §IX.A.6; Liu, ¶¶ 169-71.

8. Claim 9

Claim 9 depends from claim 1 and further requires that:

[9] “wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V”

Seo discloses, or at least renders obvious, this limitation.

⁶ For limitations that are substantively similar as prior limitations, the following cites to the Listing of Challenged Claims.

Seo's prepare voltage turns on the transistor. In this 3D memory context, such a voltage would have been above 4.5V. *E.g.*, Ex. 1013, 333. Thus, it would have been understood, and at least obvious, that Seo's voltage, which turns on the transistor (*see* limitation [1.A]), is within the range of 4V to 7V. Liu, ¶¶ 173-75.

9. Claim 10

Claim 10 depends from claim 1 and further requires that:

[10] “wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V.”

Seo's pass voltage in this 3D memory context was ordinarily around 7V. *E.g.*, §IX.C.9 (demonstrating PHOSITA's knowledge of pass voltages for 3D Flash NAND). Thus, it would have been understood, and at least obvious, that Seo's voltage, which is a pass voltage (*see* limitation [1.D]), is within the range of 5V to 9V. Liu, ¶ 176.

10. Claim 11

Claim 11 depends from claim 1 and further requires:

[11] “wherein applying the off voltage comprises applying a voltage about 0V.”

Seo discloses, or at least renders obvious, this limitation.

Seo discloses an *off voltage*. Limitations [1.A, B]. Seo discusses turning off transistors, including the select gates, with ground or another voltage. Seo, [0075] (“ground voltage V_{ss} ”). A POSITA would have understood, and certainly found

obvious, that ground includes *0V*. Liu, ¶¶ 178-79; *see also* IX.C.10 (ground as 0 volts).

11. Claim 12

Claim 12 depends from claim 1 and further requires:

[12] “wherein the removing the fast charges comprises: removing the fast charges from a storage layer of the target memory cell.”

Seo discloses this limitation, or in view of Choi, renders it obvious.

As the above demonstrates, Seo discloses, or in view of Choi renders obvious, a charge-trap memory device and the removal of fast charges; such removal occurs in the storage layer, e.g., silicon nitride, of such a memory. *See* §IX.A.1[1.D]; Choi, Introduction (“charge trap layer (SiN)”); Liu, ¶¶ 181-82.

12. Claim 13

Seo discloses the additional limitation of claim 13, or in view of Choi, renders it obvious.

Claim 13 adds to claim 12 removal from *shallow traps*.

As the above demonstrates, Seo discloses, or in view of Choi, renders obvious a charge-trap memory device and the removal of fast charges (electrical charges); such removal occurs in shallow traps in the storage layer, e.g., silicon nitride, of such a memory. *See* §IX.A.1[1.D]; Choi, Introduction (“shallowly trapped”); Liu, ¶¶ 184-85.

13. Claim 14

Seo discloses, or at least renders obvious in view of Choi, the additional limitation of claim 14.

Claim 14 adds removal to *neighboring* cells.

As the above demonstrates, Seo discloses, or in view of Choi, renders obvious, a charge-trap memory device and the removal of fast charges; such removal includes *from the target memory cell to a neighboring unselected memory cell*. See §IX.A.1[1.D]; Choi, 2:16-18 (“spread laterally”); Liu, ¶¶ 187-88. The voltage differential in Seo’s read operation (between the adjacent and selected wordline) pushes charges from the target cell to a neighboring cell, shown below as “lateral charge loss”:

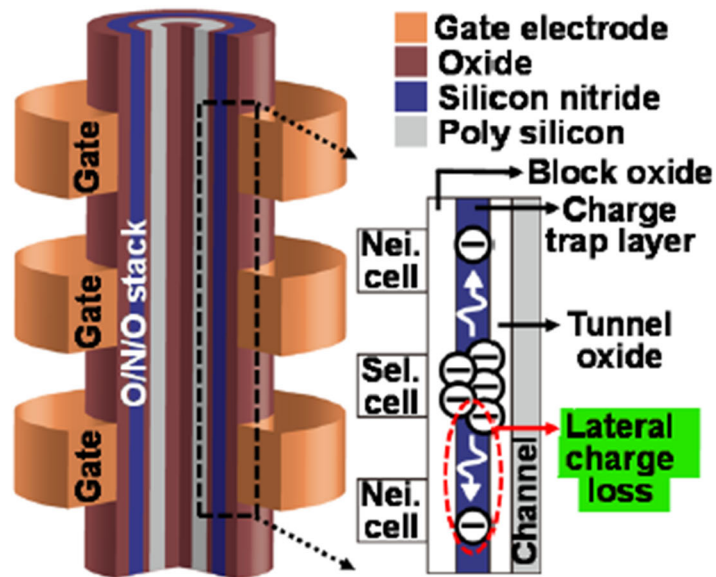


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Choi, FIG. 1 (green highlight added).

14. Claim 16

Claim 16 is an independent claim and requires:

[16.Pre]

[1.Pre] includes this preamble and, to the extent this preamble is limiting, is met for the same reasons. *See* §IX.A.1[1.Pre]; Liu, ¶ 190.

[16.A] “a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein:”

Seo discloses, or at least renders obvious in view of Choi, this limitation.

Seo's memory device includes a *memory array, comprising a plurality of memory strings extending vertically*. Seo teaches that its “three-dimensional semiconductor devices” includes “memory strings” that “are vertically formed on a semiconductor substrate.” Seo, [0006], [0007], [0051].

While Seo does not expressly disclose a *film stack of alternating conductive and dielectric layers*, a POSITA would have understood Seo to disclose such. By the filing date of the '342 patent, a stack of alternating gate (conductive) and insulating layers (made with a dielectric material, e.g., silicon dioxide) was a basic building block of 3D NAND Flash memory. Ex. 1013, 299-300; Liu, ¶¶ 192-93. This would have been the understood implementation in Seo considering Seo's disclosure of 3D memory and vertically “stacked” “memory cells.” Seo, [0051], FIG. 2.

Alternatively, Seo in view of Choi renders the *film stack* obvious. Choi shows a “device structure” of a “WL stacked tube-type” three-dimensional “NAND flash memory.” Choi, FIG. 5, 1:41-43. The film stack comprises alternating SiO₂ and MG layers. *Id.*, FIG. 5. A POSITA would have recognized that SiO₂ (silicon dioxide) is a dielectric material and MG (metal gate) is a conductive material. Liu, ¶ 194.

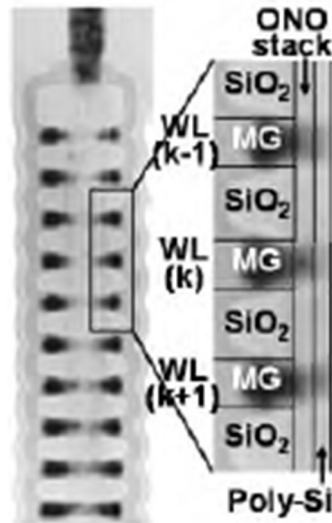


Fig. 5. TEM image of the tube-type 2y WL stacked 3-D NAND flash memory used in this work.

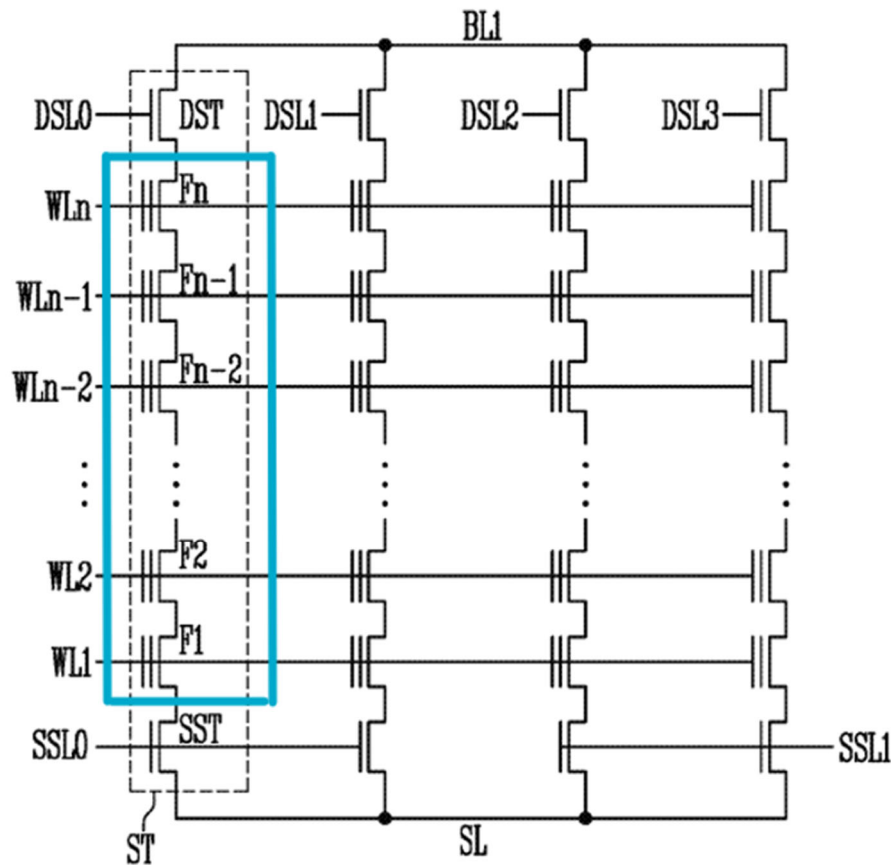
Choi, FIG. 5; *see* IX.A.19 (motivation).

[16.A.i] “each memory string comprises a plurality of memory cells; and”

Seo discloses this limitation.

“Each of the plurality of *memory strings*” “may include...first to nth *memory cells* F1 to Fn[.]” Seo, [0062], [0007], [0055].

FIG. 4



Id., FIG. 4 (annotated); Liu, ¶ 195-96.

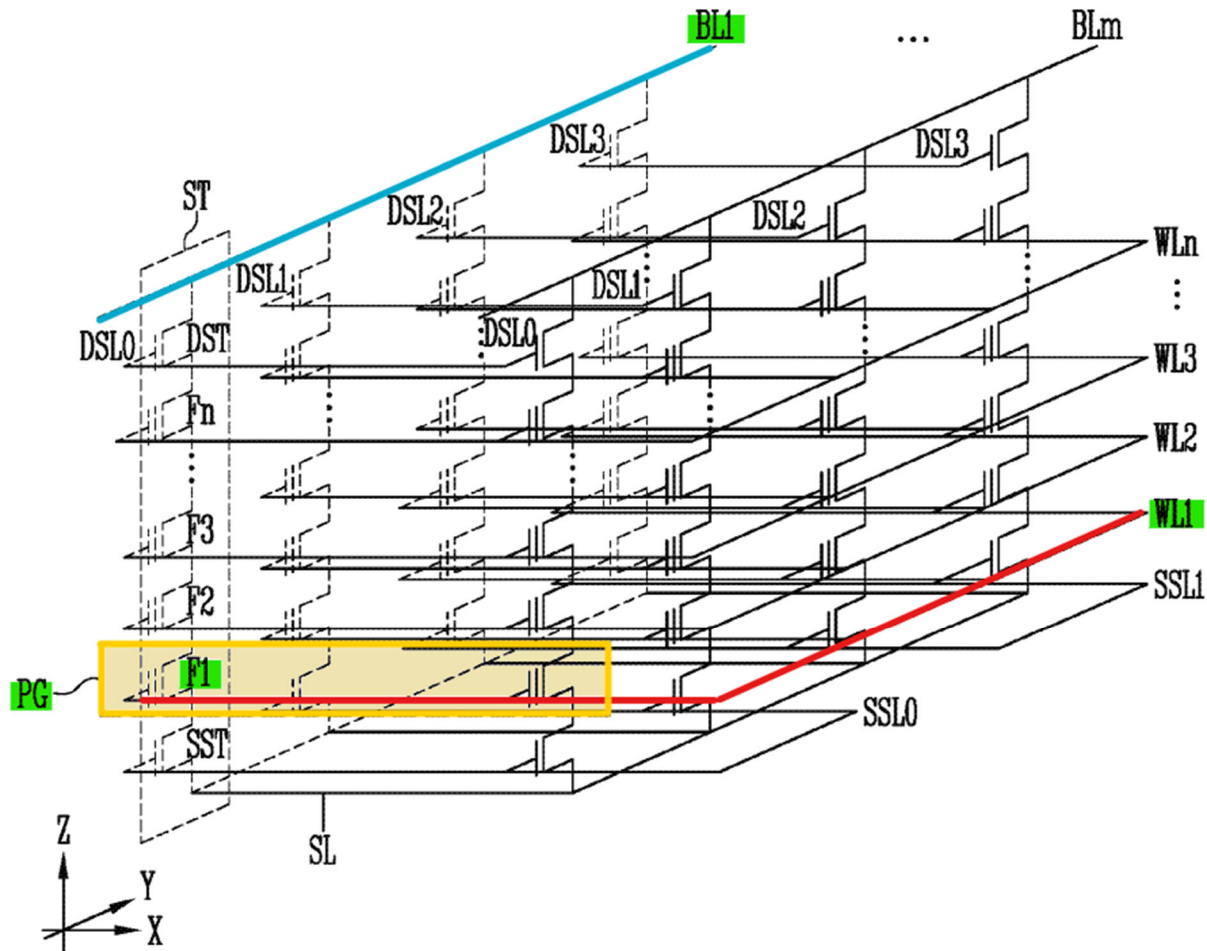
[16.A.ii] “each memory cell is addressable through a word line and a bit line; and”

Seo discloses this limitation.

Seo’s memory device can select “a page and memory strings to perform the read operation” on a memory block. Seo, [0073]. A page corresponds to *word line*.

Id., [0058]. To select memory strings (*id.*) on this page, a *bit line* is used since each

memory string is coupled to one of *bit lines* BL1 to BLm. *Id.*, [0044] (page buffers are coupled to the memory cell array through bit lines); [0074]; Liu, ¶ 198.

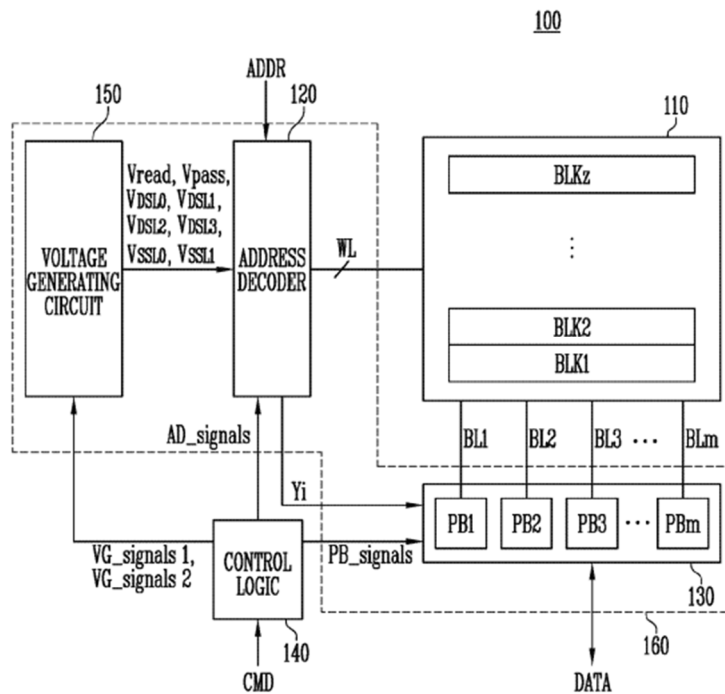


Seo, FIG. 3 (annotated).

[16.B] “a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:”

As to *a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation*, the high-level components of Seo are shown below:

FIG. 1



Seo, FIG 1. The “control logic 140” controls other circuitry, including the control of the voltages applied to the various array elements, and effectuates the read operation. *Id.*, [0047].

As to *for removing fast charges during a first time period*, see §IX.A.1[1.D];

Liu, ¶¶ 199-02,

[16.B.i]

This limitation is identical to Limitation [1.A] except for using “apply” instead of “applying.” See §IX.A.1[1.A].

[16.B.ii]

This limitation is identical to Limitation [1.B] except for using “apply” instead of “applying.” *See* §IX.A.1[1.B].

[16.B.iii]

This limitation is identical to Limitation [1.C] except for using “apply” instead of “applying.” *See* §IX.A.1[1.C].

15. Claim 17

This limitation is substantively the same as claims 2 and 3, namely, requiring (here by the *circuit*) that top and lower select gate voltages create connections, respectively, to the bit line and array common source. *See* §IX.A.2-3 (as to *circuit*, *see* §IX.A.14[16.B]).

16. Claim 18

This additional limitation is substantively identical to that of claim 4 (but uses “before” instead of “delay”). *See* §IX.A.4.

17. Claim 19

Claim 19 depends from claim 16 and further requires:

[19.A] “a channel hole”

Seo in view of Choi renders this limitation obvious.

Choi’s “tube-type” three-dimensional “NAND flash memory” has the *channel hole*:

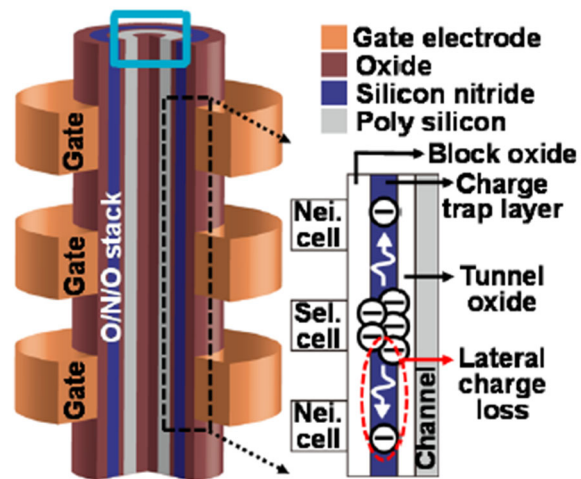


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Choi, FIG. 1 (annotated); Liu, ¶¶ 209-10.

[19.B] “a core filling film in a center of the channel hole;”

Seo in view of Choi renders this limitation obvious.

Within Choi’s “channel hole” there is a *core filling film* (i.e., oxide, with polysilicon surrounding it) in the center:

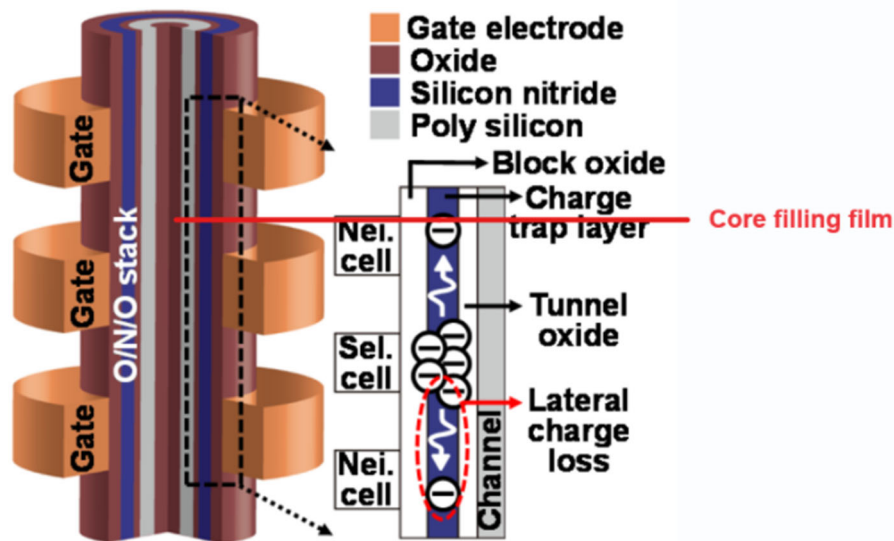


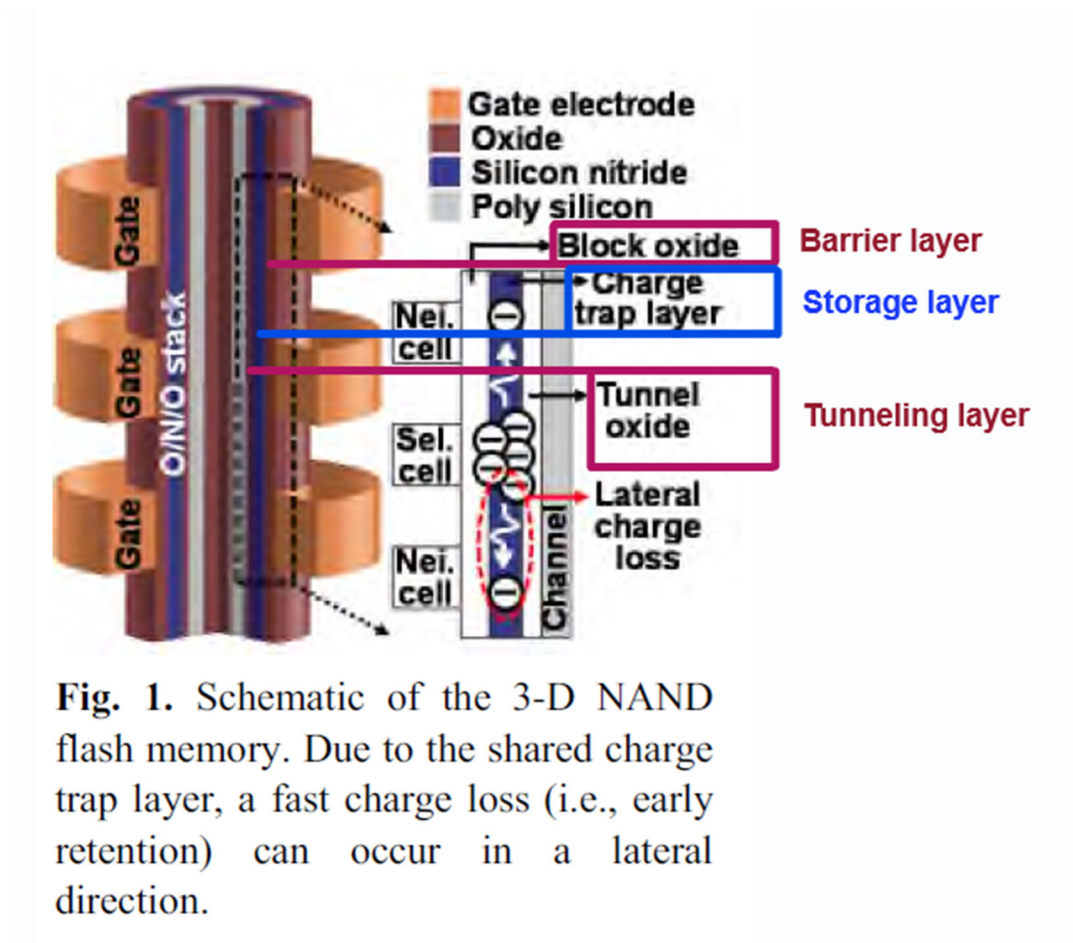
Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Choi, FIG. 1 (annotated); Liu, ¶¶ 211-12.

[19.C] “a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and”

Seo in view of Choi renders this limitation obvious.

Choi’s “3-D NAND flash memory” includes all three of the layers on the sidewall of the channel hole as shown below: the inner maroon-colored “Tunnel Oxide” is a *tunneling layer*; the blue-colored “Silicon nitride” is the *storage layer* (“charge trap layer”); and the outer maroon-colored “Block Oxide” is a *barrier layer*.

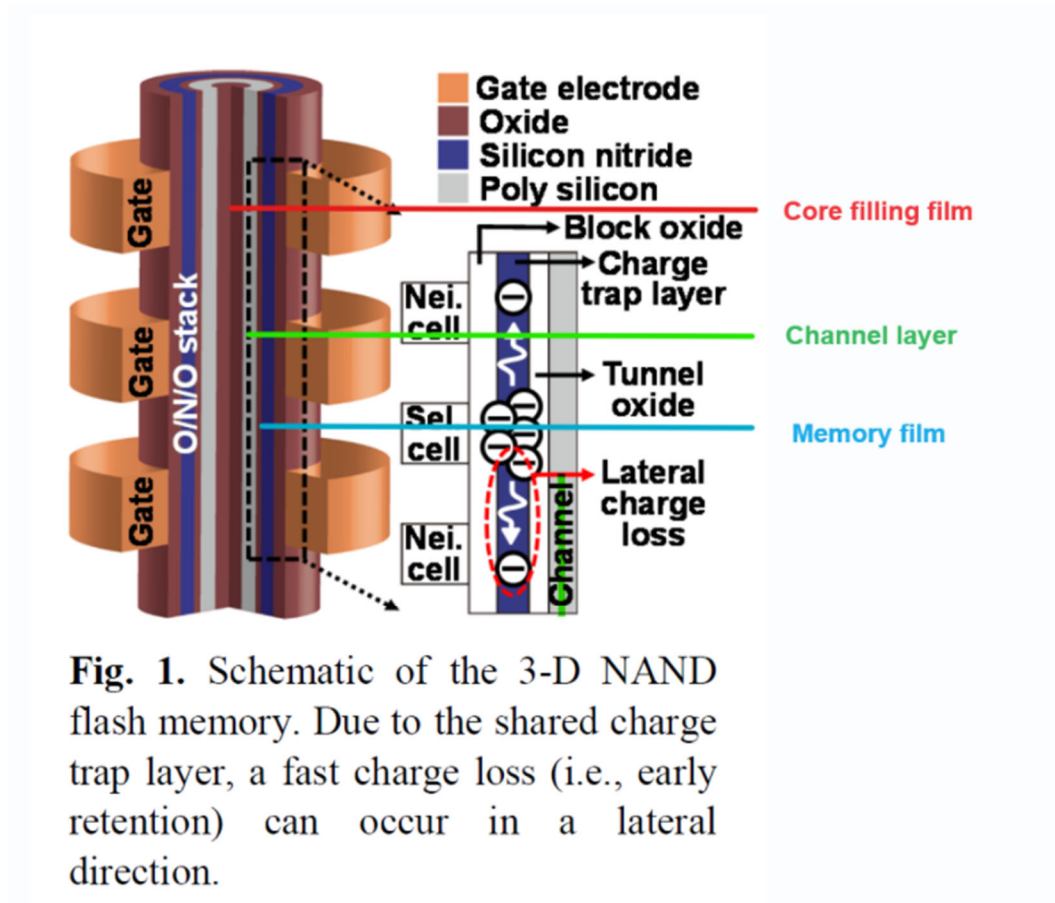


Choi, FIG. 1 (annotated); Liu, ¶¶ 213-14.

[19.D] “a channel layer sandwiched between the memory film and the core filling film.”

Seo in view of Choi renders this limitation obvious.

Choi’s *channel layer* (polysilicon) in gray-coloring (and green annotation) below, is *sandwiched between* the *memory film* (see limitation [19.C] (the ONO film marked with light blue annotation)) *and the core filling film* (see limitation [19.B] (the maroon oxide marked with the red annotation)):



Choi, FIG.1 (annotated); Liu, ¶¶ 215-16.

18. Claim 20

This limitation is substantively the same as claim 12 (except recites *circuit*).

See §IX.A.11 (as to *circuit*, see limitation [16.B]).

19. Motivation to Combine

A POSITA would have been motivated, with a reasonable expectation of success, to apply Choi's teachings to Seo regarding: (1) charge trap memory and stack teachings (alternating gate/dielectric layers), and (2) verification and fast charge removal.

As an initial matter, both Seo and Choi address issues in the field of 3D NAND flash memory, and more specifically, read operations. Seo, Abstract; Choi, 1:14-26. And Choi describes the physics underlying certain of these issues (fast charges). What's more, Seo is a patent application assigned to SK Hynix Inc., and many of Choi's authors are from SK Hynix's research center. *See* Seo, Cover; Choi, Cover. Thus, a POSITA would have been motivated to consider Choi to understand and improve on Seo's memory device. Liu, ¶¶ 219-20.

As to Choi's charge trap memory and stack: first, while Seo does not describe in detail its 3D NAND memory cells, Choi does. Choi recognizes the promise of charge-trap technology and stacked 3D NAND memories while addressing the challenges thereof, and thus a POSITA would have considered Choi to implement the basic structure of Seo's 3D NAND memory. Choi, 1:16-20; Liu, ¶ 221. Second, before 2019, "most of 3D memories [were] based on 'charge trap' cells." Ex. 1017, 15. Charge-trap technology was thought to be more "scalable than floating gate." *Id.* Thus, a POSITA would have been motivated to consider Choi's popular 3D memory implementation. Liu, ¶ 222. Third, Seo's read operation creates a voltage differential. §IX.A.1[1.D]. Choi teaches that this voltage differential de-traps fast charges from the charge-trap layer. Liu, ¶ 223. And Seo's disclosure of reducing read disturbance is also directly applicable to a charge-trap device. Thus, a POSITA would have been motivated to consider applying Choi's charge-trap memory

teachings to Seo's read operation, given the benefits of Seo's read operation to charge-trap memories. Liu, ¶¶ 223-24.

A POSITA would have had a reasonable expectation of success in applying Choi's structural teachings to Seo. Liu, ¶¶ 225-28. First, before 2019, charge-trap memory was the norm for 3D memory. Ex. 1017, 15. Second, Seo already graphically depicts a 3D memory architecture with, effectively, gate layers and memory pillars. Seo, FIG. 3. Third, not only were such structures known, but Choi illustrates that the device physics were also known.

As to Choi's read-verification step and fast charge removal teachings: first, both Seo and Choi address issues relating to the reliability of read operations. Seo, [0008]; Choi, 1:16-26. A POSITA considering the reliability issues in Seo would have been motivated to consider references that address the same issue. Liu, ¶ 229. Second, while Seo focuses on hot-charge injection ("HCI"), Choi focuses on fast-charge loss. *See* §§VIII.A, VIII.C. Both issues were well known to a POSITA. Thus, knowing that Seo only expressly addresses HCI, a POSITA would have been motivated to consider Choi's teachings regarding an additional reliability issue. Liu, ¶ 230. Third, Seo's read operation in t1 creates a voltage differential. *See* §IX.A.1[1.D]. A POSITA would have been motivated to consider the effect of this voltage differential, which Choi explains. And Choi expressly teaches this effect in the context of program-verify operations. Choi, FIG. 2; Liu, ¶ 234. Fourth, Choi

describes a use case for Seo's read operation and teaches that Seo's read operation would be beneficial to verify after programming. For example, Choi found that lateral fast-charge loss was critical for de-trapping, and thus a POSITA would have recognized that Seo's lateral-electric-field-inducing voltage differential was a particularly good mechanism for removing fast charges. Further, Choi describes that because of fast charge loss, a typical read-verify may be unsuccessful. Choi, FIG. 2. This is because the threshold may shift after verification. *Id.* Thus, a POSITA would have recognized that using Seo's read operation to verify, which removes the fast charges, would result in a more accurate verification, because any threshold shifting would occur before verification. Liu, ¶ 232.

Importantly, a POSITA also knew that a read operation was applicable to "the normal read operation" or "the verification read operation for verifying the success of the program operation." Ex. 1028, [0103]. And there was great benefit to using the same fundamental read operation for both purposes, because one finely tunes the read to avoid read interference issues, and there is no reason to "reinvent the wheel." Thus, the ordinary knowledge of a POSITA also supports applying Seo's read as a verification operation. Liu, ¶ 233-35.

A POSITA would have had a reasonable expectation of success in applying Choi's read-verification and fast-charge-removal teachings to Seo. First, as explained above, Seo's memory is structurally similar to Choi's from a high-level

perspective. Second, Choi teaches the device physics of Seo's read operation as it relates to fast charges, thus detailing Seo's operational characteristics. Third, Choi makes clear that Seo's read operation would remediate fast charge issues in a verification that occurs close in time to a program operation. Fourth, it was known how to use a read operation for verification (e.g., the read voltage (used as the verify voltage) may be slightly adjusted, while leaving the other voltages the same), which was conventional. *See* Ex. 1029, [0181], Ex. 1019, 25:2-8; Ex. 1028, [0054]-[0055]. Liu, ¶¶ 236-40.

B. Ground 2: Claim 15 Is Obvious Over Seo in View of Choi and Izumi

1. Claim 15

Claim 15 depends from claim 1 and further requires:

[15] “wherein conducting the read-verification operation comprises conducting a failed bit count in parallel.”

Seo in view of Choi and Izumi renders this additional limitation obvious.

Izumi discloses this additional limitation. It defines a *fail bit* as a data bit whose write value differs from its read value. Izumi, [0076]. A read operation can occur “[a]t the same time” as *fail-bit counts* are acquired during a write operation to determine whether to activate one or both ECC circuits. *Id.*, [0077]-[0079]. And “*fail-bit counts* . . . are updated during a read operation.” *Id.*, [0076]. More specifically, “[w]hen a data read operation starts, the operation controller 506 acquires previous *fail-bit counts* ... *simultaneously* with reading of data...,” and the

counts are then updated. *Id.*, [0081], [0084], FIG. 8 (steps S310, S370). Accordingly, a POSITA would have understood that *failed-bit counts* can be acquired and updated during a read operation following a write operation, *i.e.*, *conduct[ed] in parallel* to a *read-verification operation*. Liu, ¶¶ 241-45. Further, similar to the '342 patent, additional write operations may occur after failed bits are counted. *Compare* Ex. 1001, 14:5-6 with Izumi, [0079].

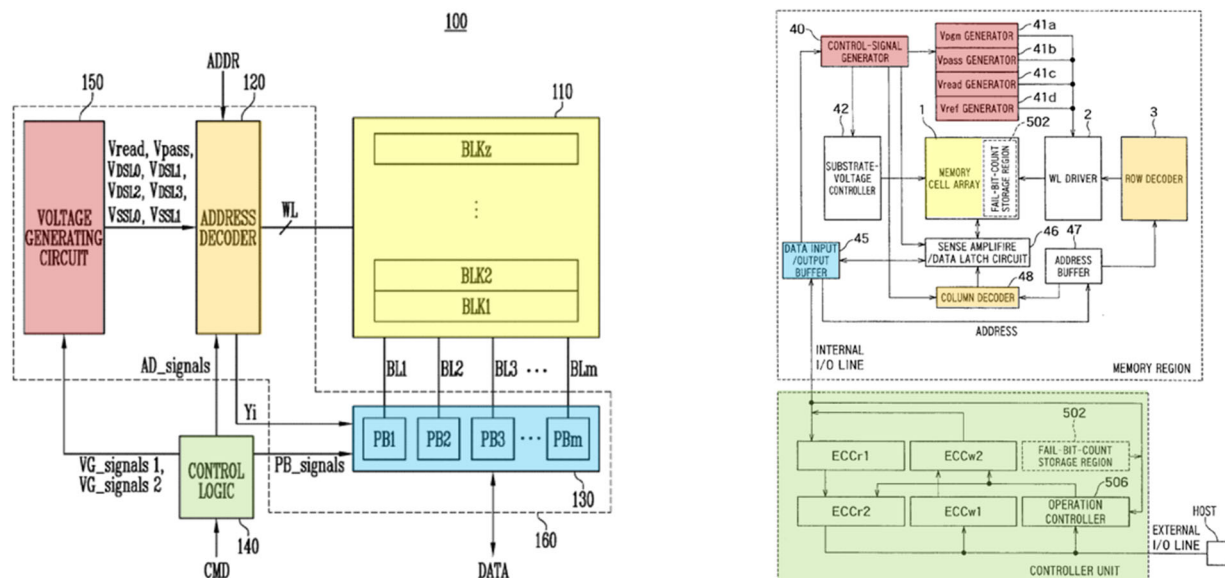
A POSITA would have been motivated to combine Seo with Izumi's failed-bit count for several reasons.

First, a POSITA would have been motivated to incorporate Izumi's failed-bit count teachings into Seo because it was common knowledge that failed bits impact 3D NAND like Seo's. Ex. 1017, 47-50. And Seo's mitigation of read-disturb effects does not solve the problem of memory cells that will ultimately fail. *Id.*, 47. A POSITA would have known that ECC used in Izumi was a well-known mechanism for detecting and correcting failed bits and would have been motivated to use it to address failed bits on Seo's devices. Izumi, [0003]-[0004]; Liu, ¶¶ 246-47.

Second, Izumi's approach reduces power consumption by selectively activating one or two ECC circuits. Izumi, [0078], [0082]. A POSITA would have found Izumi's low-power ECC techniques desirable. Liu, ¶ 248.

Additionally, a POSITA would have naturally looked to Izumi because both Seo and Izumi are in the same field (NAND) and involve the same high-level

functions (access operation reliability). More specifically, Izumi applies its failed-bit-count method to a memory like Seo's: a NAND flash using charge-trapping technology, and a memory array comprising bit lines and word lines and partitioned into pages. Izumi, Abstract, [0003], [0018], [0041]. Both disclose memory devices comprising the same components including address decoders, control logic, and buffers:



Seo, FIG. 1; Izumi, FIG. 6 (both annotated). Although Izumi discloses a 2D NAND flash, a POSITA would have known that failed bits are a concern regardless of the dimensionality of the flash, and that Izumi's failed-bit-count and ECC techniques also apply to 3D NAND flash. Liu, ¶ 249.

A POSITA would have had a reasonable expectation of success of applying Izumi's teachings to Seo. First, using ECC to correct failed bits, as Izumi does, was textbook material. Ex. 1017, 50. Second, the components Izumi uses for ECC such

as the ECC circuits and failed-bit-count storage can reside in the control logic and a partition of the memory array, components common to Seo's and Izumi's memory devices (see above figures). Liu, ¶¶ 250-52.

As explained above, Choi simply renders explicit a POSITA's understanding that Seo's read-verification operations remove fast charges and does not impact this combination. *See* §IX.A.1[1.D]; Liu, ¶ 253.

C. Ground 3: Claims 1-3, 5-6, 8-14, 16-17, and 19-20 Are Obvious Over Nam in View of Choi

Nam in view of Choi and the knowledge of a POSITA renders claims 1-3, 5-6, 8-14, 16-17, and 19-20 obvious. Liu, ¶ 255.

1. Explanation of Figures

This Ground focuses on Nam's "immune disturbance read operation" as largely set forth in Figure 10 and its accompanying description. As Nam discloses, however, "the inventive concept [is] more fully described with reference to FIGS. 1 to 10."⁷ Nam, [0147]. Other figures in Nam, e.g., Figure 19, also describe use cases of Nam's "immune disturbance read operation." *Id.*, [0155]-[0156]. Thus, this Ground cites to various figures of Nam.

⁷ In each description of Figures 6-10, the specification states that it is "an exemplary embodiment of the inventive concept." Nam, [0147]. However, as this Section explains, each of these figures builds upon the preceding figures.

Figures 1-3 and 5 depict exemplary structural aspects of Nam's memory array. Nam, [0033]-[0036], [0038]. Figure 3 also illustrates a prior art pre-sensing and sensing⁸ scheme. *Id.*, [0094]-[0096]. In various places, the specification refers back to Figure 3, because Nam's immune disturbance read operation uses Figure 3's prior art sensing scheme (whereas Nam's focus is on the phases before and after sensing).⁹ *Id.*, [0122]. Figure 5 also illustrates the physics of charge sharing among memory cells. *Id.*, [0099]-[0100]. Figure 4 depicts exemplary threshold and erase voltage values. *Id.*, [0098].

Figures 6-10 effectively provide a build that adds different signals in describing the immune disturbance read operation over four time periods: (1) WL Setup (pre-sensing), (2) 1st and 2nd reads (sensing), (3) Charge Share, and (4) Recovery. Nam, FIGs. 6-10. Relevant to this Ground are the first two periods: (1) WL Setup (pre-sensing), and (2) 1st and 2nd reads (sensing). *Id.* Figure 6 effectively starts the build in disclosing the immune disturbance read operation with respect to

⁸ The sensing phase measures the threshold value of the target memory cell. Nam, [0096], Liu, ¶ 259.

⁹ Figure 3 includes an error in indicating that the bottom select gate would be at ground during sensing. Other figures on which this Ground relies demonstrate that the bottom select gate is at a *pass* voltage during sensing. Liu, ¶ 259.

voltages on “UNSEL WLs” (unselected word lines) and “SEL WL” (selected word line), and the signals on these lines are identical for Figures 6-10 with respect to the first two periods. *Id.*, FIG. 6. Figures 7-9 distinguish between the UNSEL WLs for different treatment in the Charge Sharing and Recovery periods (periods that are not relevant to this Ground). *Id.*, FIGs. 7-9. Figure 9 also illustrates the waveform of “SEL SSL” (selected top select gate) and “GSL” (bottom select gate) voltages. *Id.*, FIG. 9. Figure 10 further depicts the “UNSEL SSL” (unselected top gate). *Id.*, FIG. 10, [0122] (“Referring to FIG. 10, an immune disturbance read operation on unselected string selection lines UNSEL SSL *may further include* applying ... to ... UNSEL SSL”). Figure 10, however, omits the “SEL SSL” (selected top select gate) waveform from Figure 9.¹⁰ *Id.*; Liu, ¶¶ 256-67.

2. Claim 1

[1.Pre] “A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:”

To the extent the preamble is limiting, Nam discloses it.

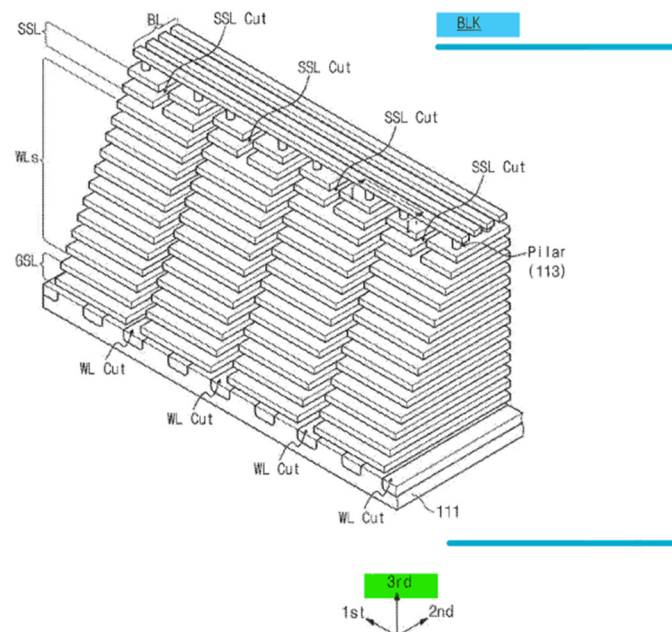
First, Nam teaches: “[a] method of reading a nonvolatile memory device” that includes the step of “sensing a state of a memory cell.” Nam, Abstract. Nam discloses that its read operation (“immune disturbance read operation”) is applicable

¹⁰ In any event, it goes without saying that SEL SSL is high during the read operation as well, because it is necessary to read the memory cells. Liu, ¶ 267.

after a program operation, e.g., a *read-verification operation*. *Id.*, [0026] (“a verification read operation”), [0155] (“immune disturbance read operation may be selectively performed at a program verification operation”), FIG. 19. The operation occurs on “memory cells corresponding to the selected word line WLm-3 and the selected string selection line SSL1,” i.e., a *target memory cell*. *Id.*, [0096]; Liu, ¶¶ 268-71.

Second, Nam’s discloses that its operations are applicable to a *three-dimensional* memory device. Nam, [0029] (“vertical NAND flash memory”), [0065] (“[e]ach of the memory blocks” may “have a *three-dimensional* structure”).

Fig. 2A



Id., FIG. 2A (annotated). Thus, Nam discloses *a method for conducting a read-verification operation* (e.g., an immune disturbance read operation) *on the memory*

cells connected with the selected word line may be performed on a target memory cell (e.g., memory cell connected to a selected word line/string) *in a three-dimensional (3D) memory device* (e.g., three-dimensional memory). Liu, ¶ 272.

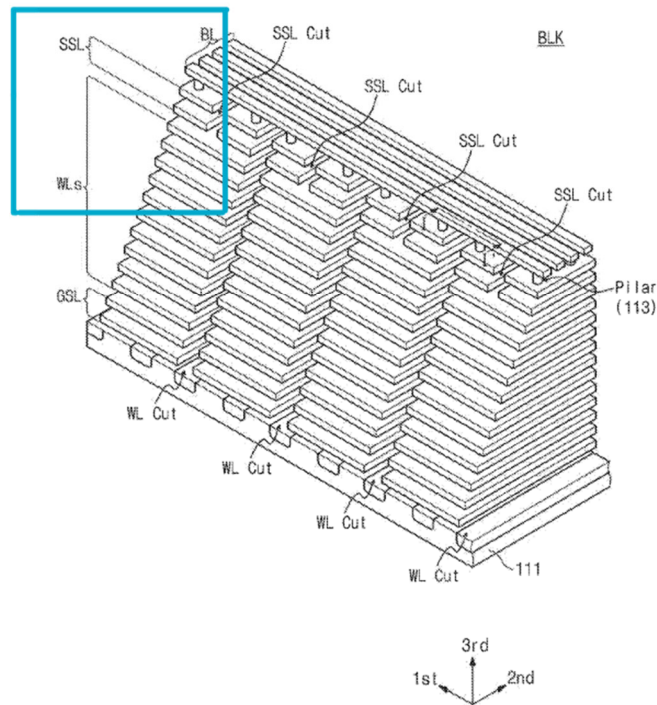
[1.A] “applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period”

Nam discloses this limitation.

As an initial matter, Nam refers to the *top select gate* as a “string selection line SSL.” Nam, [0064].¹¹ As shown below, the SSL layers reside at the top of the memory stack and select string(s).

¹¹ At times, Nam refers to “string selection transistors,” which are the individual transistors of the SSL layers. Nam, [0133]; Liu, ¶ 274, n.3. But typically, Nam simply refers to applying voltages to the SSL, which this Petition will refer to when discussing applying the relevant voltages to the select gate layers.

Fig. 2A

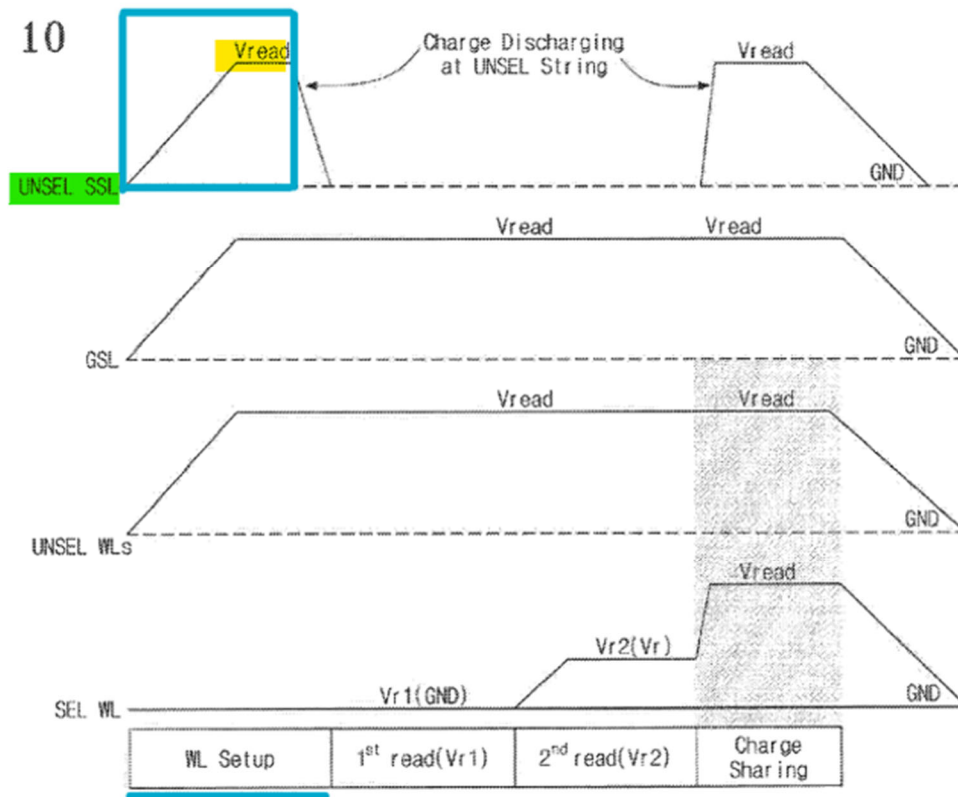


Nam, FIG. 2A (annotated), [0076].

“FIG. 10 is a timing diagram illustrating an immune disturbance read operation according to an exemplary embodiment of the inventive concept.” Nam, [0122]. As shown below, Figure 10 includes *a first time period*, i.e., “WL Setup,” and *a second time period*, i.e., “1st read[Vr1]” and “2nd read[Vr2].” *Id.*, [0104].

During *a first time period*, “the read pass voltage Vread may be applied to unselected string selection lines UNSEL SSL before a sensing operation (e.g., before the 1st read and 2nd read).” Nam, [0122].

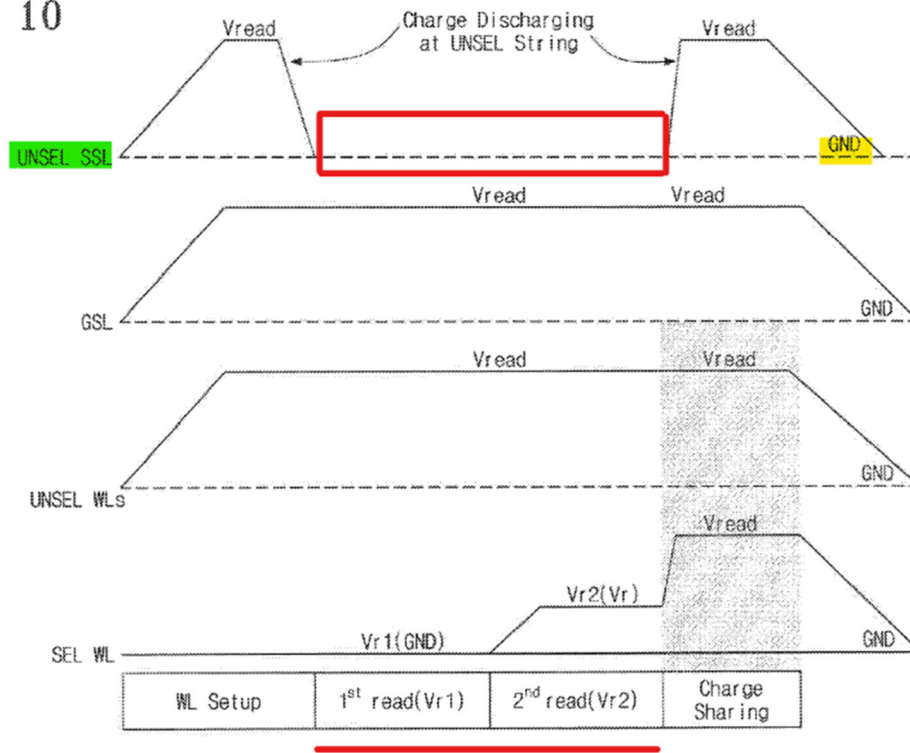
Fig. 10



Id., FIG. 10 (annotated.). While not a requirement, Nam’s V_{read} pass voltage is within the exemplary ’342 range (Ex. 1001, 2:40-44). Nam, [0098] (“ V_{read} may be about 7V”). Also, like Figure 6 of the ’342 patent, Nam’s V_{read} pass voltage is greater than the voltage applied to the selected word line during the reading phase. Compare Ex. 1001, FIG. 6 ($V_{prepare}$ versus V_{read}), with Nam, FIG. 10 (V_{read} versus $Vr2(Vr)$; see also Liu, ¶¶ 273-77.

Further, during *a second time period*, Nam discloses applying an *off voltage*—namely, GND (ground)—to unselected string selection lines UNSEL SSL.

Fig. 10



Nam, FIG. 10 (annotated). Ground is an *off voltage* because it does not turn on the transistor. *Id.*, [0098] (compare with voltage that turns on transistor); Liu, ¶ 278.

Note that the description of Figure 10 states: “[a]n operation of applying the read pass voltage *Vread* to unselected string selection lines UNSEL SSL at a sensing operation *may be substantially the same as that described with reference to FIG. 3, and a description thereof is thus omitted.*” Nam, [0122]. There, and as shown above,¹² Nam discloses that application of *Vread* terminates when the sensing

¹² The applied voltage transitions from *Vread* to ground at the start of the sensing period (1st and 2nd reads) and then after sensing, transitions from *ground* to *Vread*,

operation begins: “after boosting charges of the unselected strings ST2 to ST4 are discharged or shared, bit lines BL_i and BL_{i+1} may be pre-charged, ***a ground voltage GND may be applied to the unselected string selection lines*** SSL2, SSL3 and SSL4, a read voltage V_r may be applied to the selected word line WL_{m-3}, and the read pass voltage V_{read} may be applied to the remaining word lines WL0 to WL_{m-4} and WL_{m-2} to WL_m. ***Under this bias condition, a sensing operation may be performed***” *Id.*, [0096]; Liu, ¶¶ 279-83.

Thus, Nam discloses *applying, on an unselected top select gate of an unselected memory string* (e.g., UNSEL SSL), *a prepare voltage during a first time period* (e.g., V_{read} during WL Setup) *and an off voltage during a second time period* (e.g., GND during 1st and 2nd read periods).

[1.B] “applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period;”

Nam discloses this limitation.

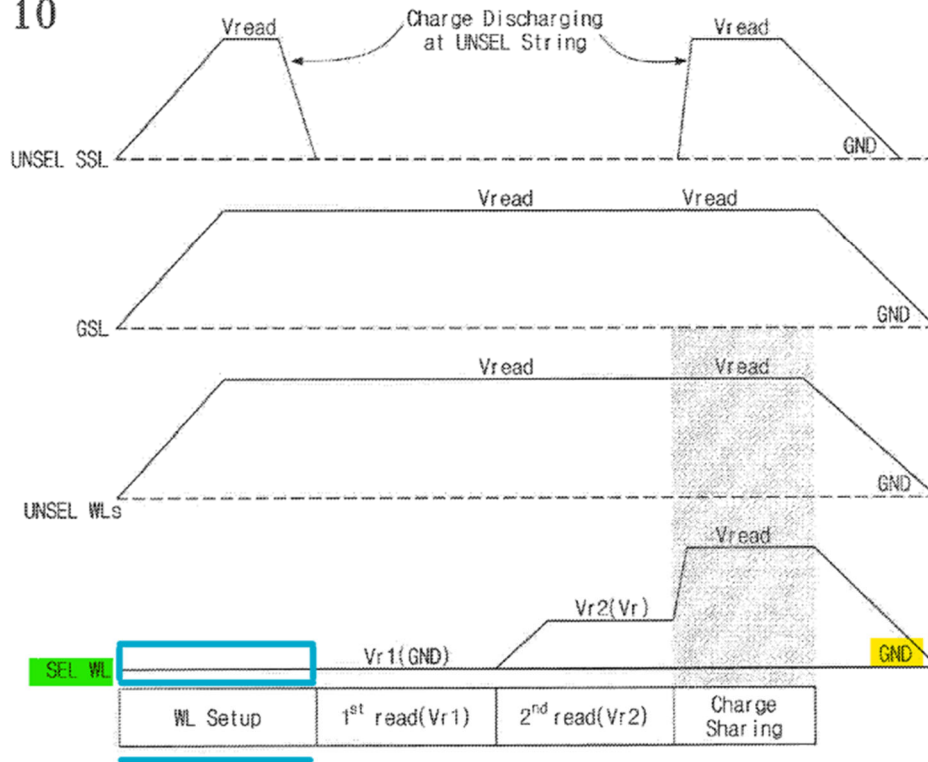
Nam describes how the “data stored” within a *memory cell* can be “determined through read operations.” Nam, [0104]. This “read operation” occurs on “memory

further demonstrating that during the sensing, “a ground voltage GND may be applied to the unselected string selection lines.” Nam, [0096], FIG. 10; Liu, ¶¶ 281-82.

cells” that correspond to “the selected wordline” (i.e., *selected word line associated with the target memory cell*), *id.*, [0094]-[0096] (“a sensing operation may be performed to detect on or off states of memory cells corresponding to the selected word line”).

Nam discloses how “[i]n the word line setup section WL Setup [*the first time period*], a ground voltage GND may be applied to a selected word line SEL WL.”¹³ Nam, [0105].

Fig. 10

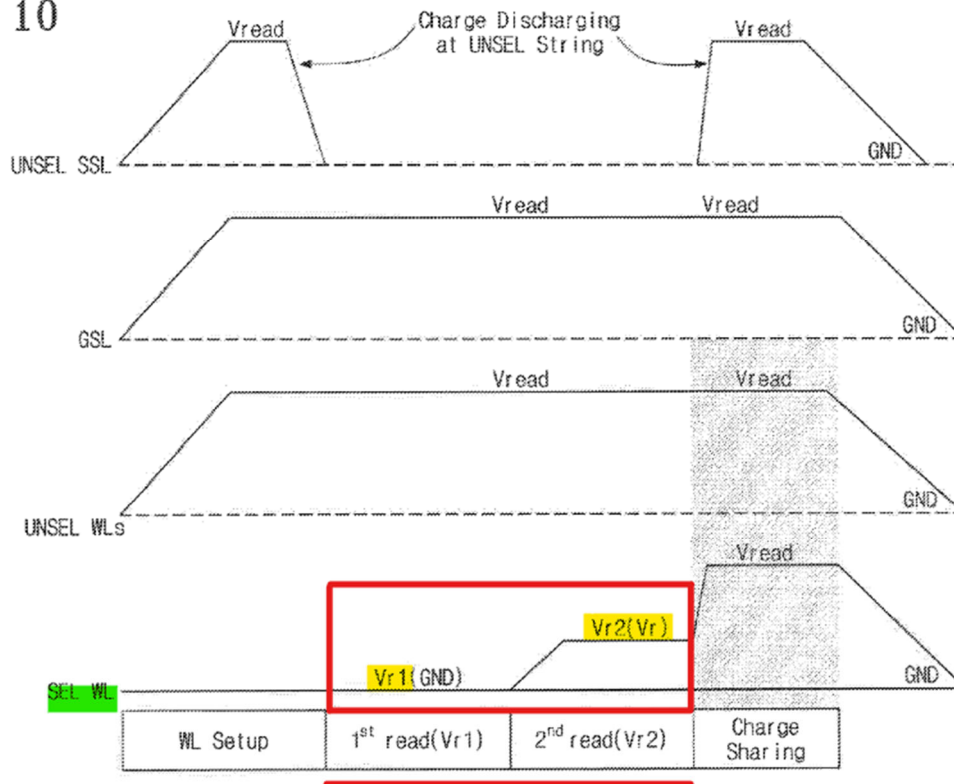


Id., FIG. 10 (annotated).

¹³ GND may be 0 volts. Nam, [0100].

Next, in the “first read section read” and “second read section” (*the second time period*), a “sensing operation may be performed.” Nam, [0106]. This involves applying a “read voltage V_r ,” such as “a first read voltage V_{r1} ” and “a second read voltage V_{r2} ” to the selected wordline. *Id.*, [0096], [0104], [0106].

Fig. 10



Id., FIG. 10 (annotated).

Thus, Nam discloses *applying, on a selected word line associated with the target memory cell* (e.g., SEL WL), *the off voltage during the first time period* (e.g., Ground during WL Setup) *and a read voltage during the second time period* (e.g.,

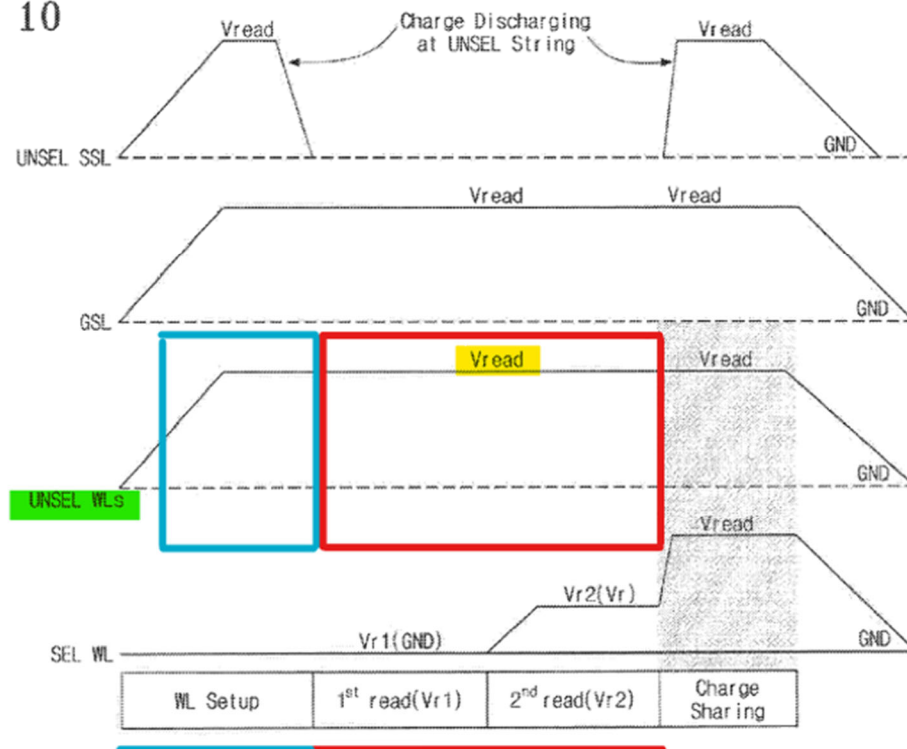
Vr1(GND) during 1st read period and Vr2(Vr) during 2nd read period). Liu, ¶¶ 284-88.

[1.C] “applying, on an unselected word line, a pass voltage during the first time period and the second time period,”

Nam discloses this limitation.

During both the WL Setup (*the first time period*) and the 1st and 2nd reads (*the second time period*), Nam discloses that a “read pass voltage Vread may be applied to the remaining word lines,” i.e., *unselected word lines*. Nam, [0096], [0105] (“[i]n the word line setup section WL Setup [*the first time period*], . . . a read pass Vread voltage may be applied to unselected word lines UNSEL WLs”).

Fig. 10



Id., FIG. 10 (annotated).

Thus, Nam discloses *applying, on an unselected word line* (e.g., UNSEL WLs), *a pass voltage during the first time period and the second time period* (e.g., read pass Vread during WL Setup, and 1st and 2nd reads). Liu, ¶¶ 289-91.

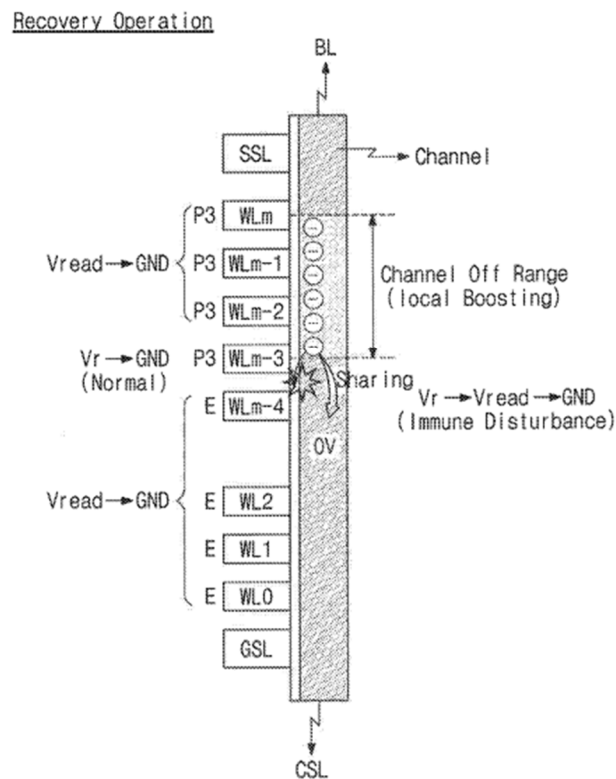
[1.D] “wherein the read-verification operation removes fast charges of the target memory cell during the first time period”

Nam discloses this limitation or, at a minimum, renders it obvious in view of Choi.

As an initial matter, Nam discloses several times that its memory may include charge-trap memory cells. Liu, ¶¶ 293-97.

First, Nam broadly describes its memory as applicable to “NAND flash memory.” Nam, [0164], Claim 24. NAND flash memory includes charge-trap memory cells. Ex. 1017, 101. Second, Nam depicts a charge-trap device:

Fig. 5



Nam, FIG. 5, [0099]. As shown above, the 3D vertical channel includes a solid, continuous memory channel, unlike conductive gate memories. Ex. 1017, 105, 145-48.

At a minimum, given these multiple disclosures, a POSITA would have found that Nam's teachings are applicable to charge-trap devices. §IX.A.1.[1.D] discusses that charge-trap memories were obvious in view of disclosures relating to 3D Flash, which Nam discloses. *See* §IX.C.2[1.Pre]; Liu, ¶ 297.

Next, as described above, Nam teaches the requisite waveforms for the claimed *read-verification operation*. See limitations [1.A]-[1.C]. Specifically, Nam

teaches having a higher voltage on unselected WLs (including WLs adjacent to the selected WL) relative to the selected WL during the *first time period*, WL Setup. *Id.* In charge trap devices, this creates a lateral electric field that removes fast charges. *See* Ex. 1001, 12:24-34; *see also* §VIII.C; Liu, ¶ 298.

To the extent that PO argues that Nam is deficient because it does not recite removing fast charges, Nam in view of Choi render this limitation obvious. *See* §IX.C.18. Choi expressly teaches that voltage differential removes fast charges. *See* §IX.A.1[1.D]. Thus, in view of Choi, a POSITA would have understood that Nam's read-verification operation removes fast charges in a charge-trap memory. Liu, ¶ 299.

Accordingly, Nam discloses, or at least in view of Choi renders obvious, *wherein the read-verification operation removes fast charges of the target memory cell during the first time period* (e.g., voltage differential from the read-verification operation removes charge from Nam's charge trap memory cells). Liu, ¶ 300.

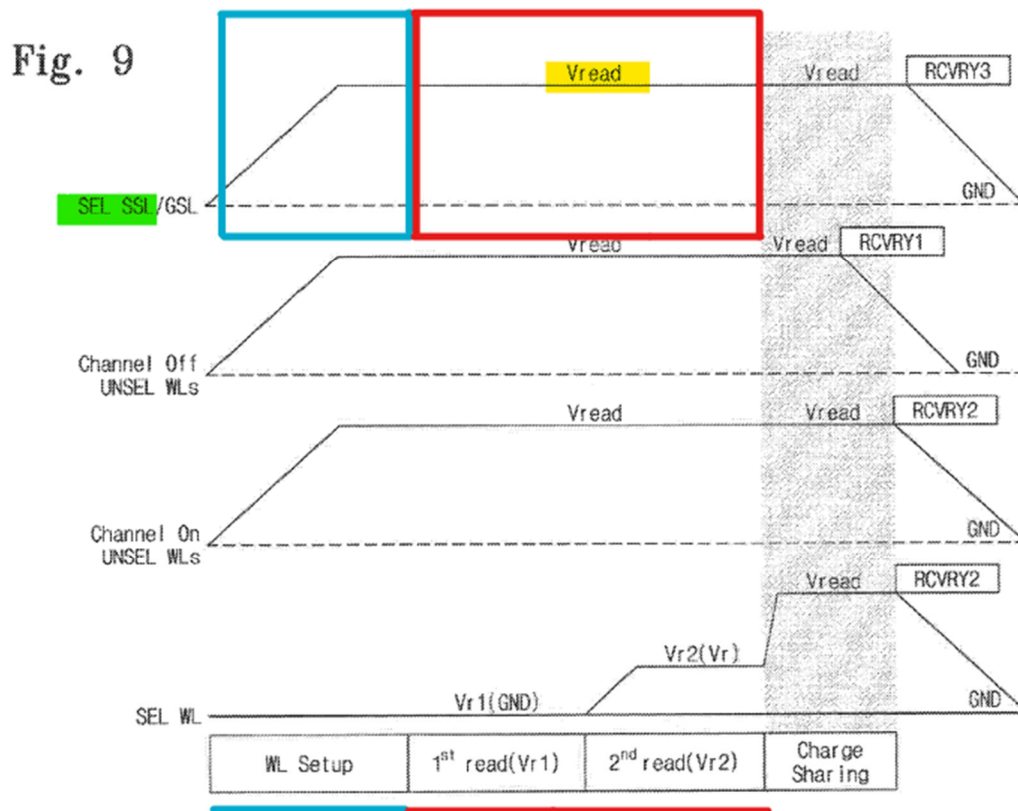
3. Claim 2

Claim 2 depends from claim 1 and further requires:

[2.A] “applying, on a selected top select gate of a selected memory string containing the target memory cell, a top select gate voltage during the first time period and the second time period;”

Nam discloses this limitation.

The SSL (which includes SSTs as respective gate transistors) is the *top select gate* of Nam. See §IX.C.2[1.A]; Nam, [0090]. Figure 9 shows the *selected top gate of the selected memory string containing the target cell* (SEL SSL) waveform during Nam's read operation of Figure 10. See §§IX.C.1, IX.C.2[1.C]. During *the first time period and the second time period* (e.g., WL Setup, and 1st and 2nd read), Vread (*a top select gate voltage*) is applied to SEL SSL:



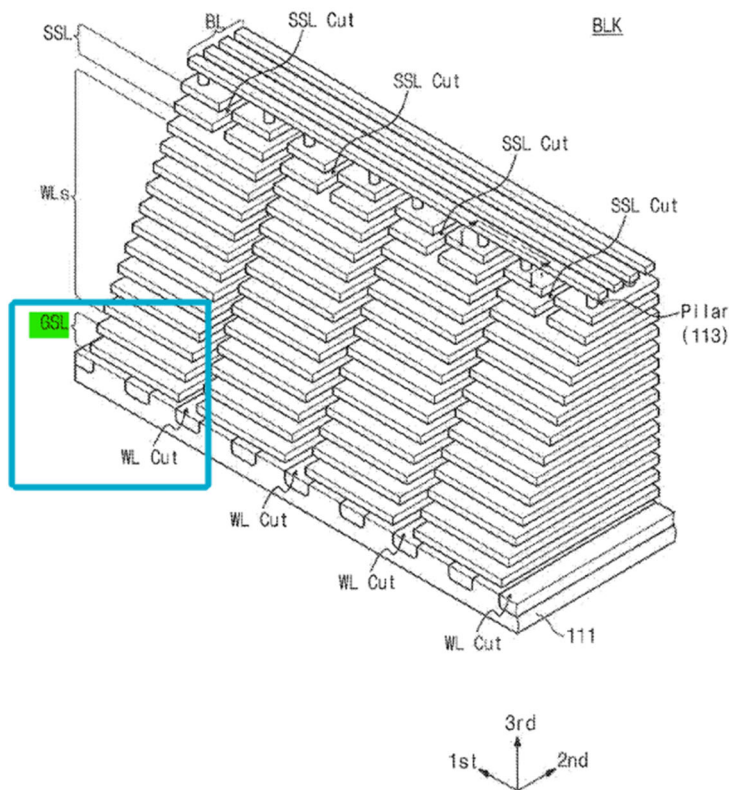
Nam, FIG. 9 (annotated); Liu, ¶¶ 302-03. Vread turns on the transistor. Nam, [0098].

[2.B] “applying, on a lower select gate of the selected memory string containing the target memory cell, a lower select gate voltage during the first time period and the second time period.”

Nam discloses this limitation.

The *lower select gate of the selected memory string containing the target memory cells* is Nam’s GSL:

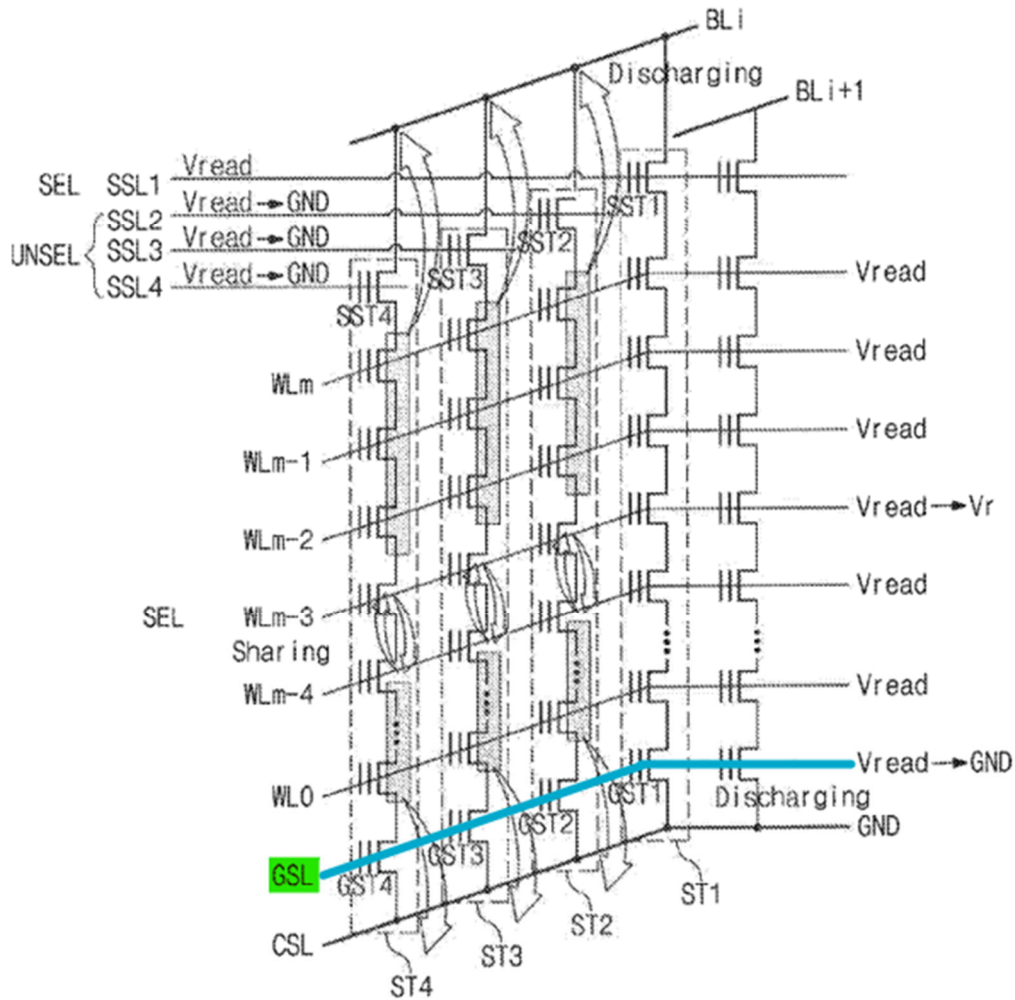
Fig. 2A



Nam, FIG. 2A (annotated), [0065], [0076]. As shown above and below, Nam does not refer to “selected” GSL or “unselected” GSL, because the GSL (unlike the SSL) is *shared* among what Nam refers to as the selected and unselected strings:

Fig. 3

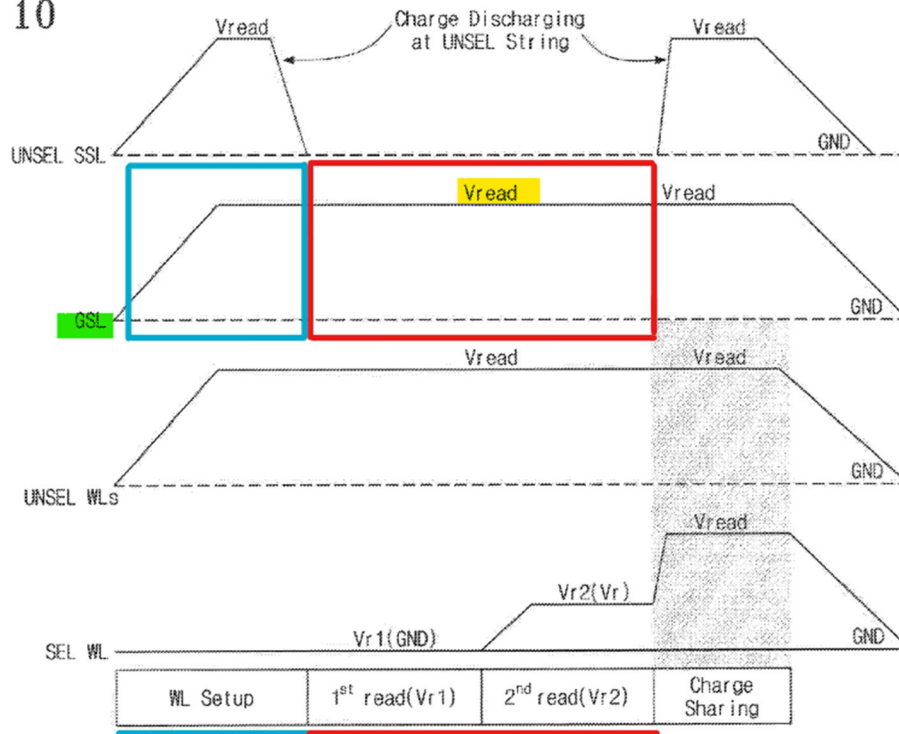
(Prior Art)



Id., FIG. 3 (annotated).

And, as further shown below, during *the first time period and the second time period*, Vread (*a lower select gate voltage*) is applied to the GST:

Fig. 10



Nam, FIG. 10 (annotated); Liu, ¶¶ 304-06. Vread turns on the transistor. Nam, [0098].

4. Claim 3

Claim 3 depends from claim 2 and further requires:

[3] “wherein the applying the top select gate voltage comprises electrically connecting the selected memory string to a bit line; and the applying the lower select gate voltage comprises electrically connecting the selected memory string to an array common source”

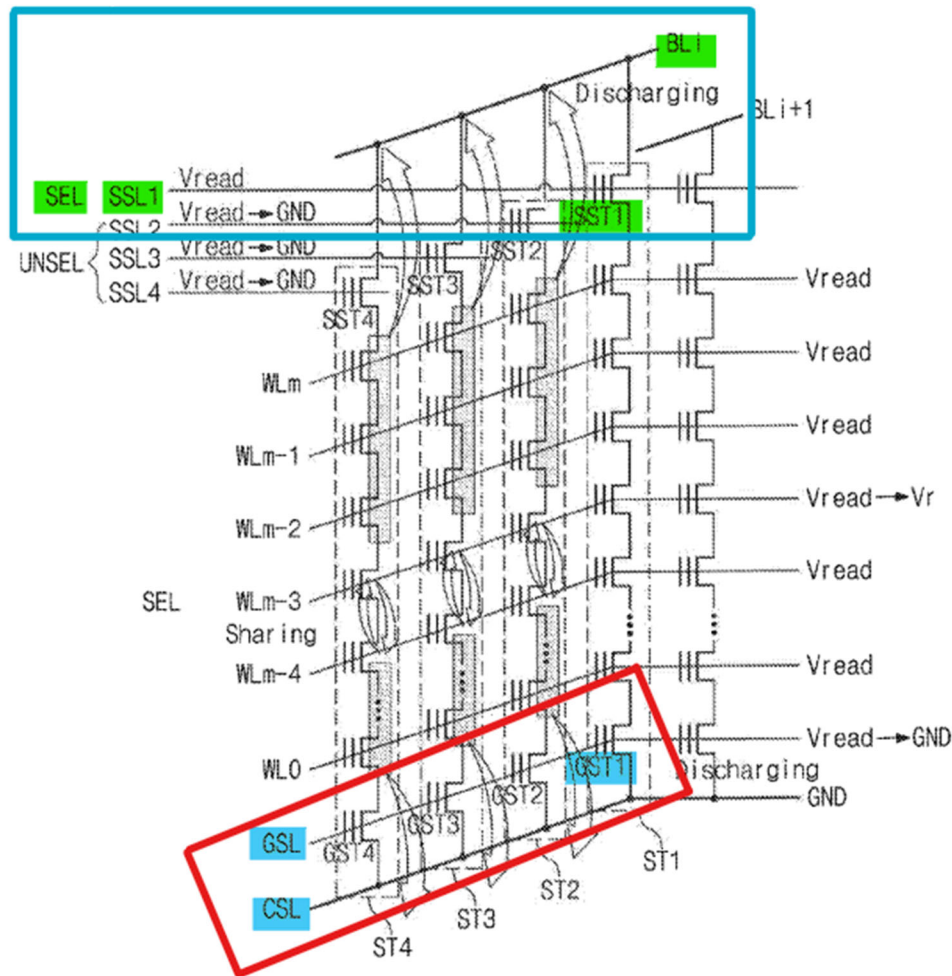
Nam discloses this limitation.

First, *applying the top select gate voltage* and *applying the lower select gate voltage* in Nam entails applying Vread (see limitation [2.A, 2.B]), which turns on

the transistors. Nam, [0098]. As shown below, turning on *the top select gate* connects the memory string to the *bit line* and turning on *the lower select gate* connects the memory string to an *array common source* (“CSL”) (due to creating conductive paths between these elements).

Fig. 3

(Prior Art)



Id., FIG. 3 (annotated); [0094] (“bit line BL_i is connected with four strings ST1 to ST4.”); [0100] (“the channel ... is connected with a common source line CSL”).

As to an *array common source*, Nam’s “common source line” defines an array (a portion of the overall memory) and is thus an *array common source*. Each array includes a common source line, and those common source lines connect together to form a *single* common source for the device. *Id.*, [0076] (“common source lines . . . may be interconnected.”). Liu, ¶ 309.

5. Claim 5

Claim 5 depends from claim 1 and further requires:

[5] “measuring a threshold voltage of the target memory cell during the second time period.”

Nam discloses this limitation.

As §IX.A.5 demonstrates, this limitation corresponds to a read operation.

Nam discloses a read operation that *measure[s] a threshold voltage of the target memory cell*, e.g., measuring whether the *threshold voltage* in Nam’s *target memory cell* is P1 or P3. Nam, [0096], [0098] (measuring with “a ground voltage GND” and “read voltage V_r ”). Nam’s *second time period* is the sensing phase (see the 1st read and 2nd read period). See §IX.C.2[1.B]; Liu, ¶¶ 311-12.

6. Claim 6

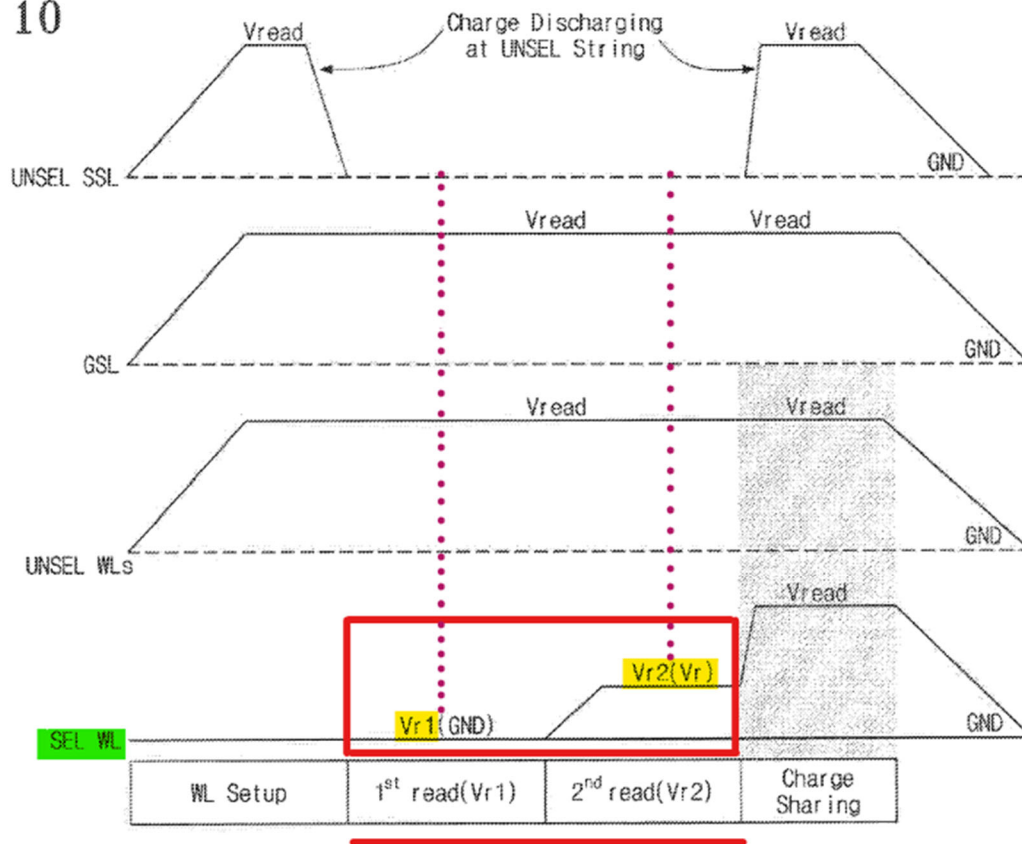
Claim 6 depends from claim 1 and further requires:

[6] “wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell”

Nam discloses, or at least renders obvious, this limitation.

Recall that *applying the read voltage during the second time*, and more specifically, *applying the read voltage*, refers to when V_{r1} and V_{r2} are applied. See §IX.C.2[1.B].

Fig. 10



Nam, FIG. 10 (annotated); limitation [1.B].

When this occurs, the *voltage of the unselected top select gate* is 0 volts. As §IX.A.6 explains, because of a block erase, there will be unselected memory cells that have threshold voltages corresponding to E, P1, P2, and P3 (after the programming progresses past the first row) and both bottom to top and top to bottom programming was obvious. Nam, [0098] (showing that E is negative and P1-3 is

positive), FIG. 4 (threshold states); Ex. 1017, 91-93 (conventional block erase); *see also* Nam, [0024] (“program/erase cycle” of block); Ex. 1024, [0115], [0130] (bottom up or top to bottom programming); Ex. 1025, 8:18-53 (benefits of knowing row states).

Thus, some of the unselected memory cells will be in the erase state, and 0 volts is higher than the erase state. Liu, ¶¶ 314-16.

7. Claim 8

Nam discloses the additional limitation of claim 8.

This limitation is identical to claim 6 except that it requires the *unselected top select gate* voltage to be *lower*, instead of higher, than *an unselected cell[s] threshold voltage*.

The claim refers to when *the unselected top select gate* is 0V. *See* §IX.C.6. As described above, it would have been understood, and certainly obvious, that unselected rows will include programmed cells, in which case *the unselected top select gate* is *lower* than the threshold voltage of the programmed, unselected memory cells (positive values). *See* §IX.C.6; Liu, ¶¶ 317-22.

Note that Nam discloses that *unselected memory cell[s]* may be programmed. *Id.*, [0095] (“To share boosting charges of the unselected strings ST2 to ST4 before a sensing operation, a read pass voltage *Vread* may be applied to the selected word line *W_{Lm-3}*.”). Liu, ¶ 320.

8. Claim 9

Claim 9 depends from claim 1 and further requires that:

[9] “wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V”

Nam discloses this limitation.

Nam discloses that the “read pass voltage,” i.e., *the prepare voltage*, “may be about 7V.” Nam, [0098]; §IX.C.2[1.A]; Liu, ¶¶ 324-25.

9. Claim 10

Claim 10 depends from claim 1 and further requires:

[10] “wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V”

Nam discloses this limitation.

Nam discloses that the “read pass voltage,” i.e., *the pass voltage*, “may be about 7V.” Nam, [0098]; §IX.C.2.[1.C]; Liu, ¶¶ 327-28.

10. Claim 11

Claim 11 depends from claim 1 and further requires:

[11] “wherein applying the off voltage comprises applying a voltage about 0V.”

Nam discloses this limitation.

Nam discloses that its “ground voltage GND,” i.e., *off voltage*, is, “e.g., 0V.” Nam, [0100]; §IX.C.2[1.C]; Liu, ¶¶ 330-31.

11. Claim 12

Claim 12 depends from claim 1 and further requires:

[12] “wherein the removing the fast charges comprises: removing the fast charges from a storage layer of the target memory cell.”

Nam discloses this limitation, or at least in view of Choi renders it obvious.

Claim 12 involves removing charges trapped in shallow traps of a storage layer (charge-trap layer), e.g., silicon nitride, of the target memory cell. §VIII.C. Nam discloses or renders obvious a charge-trap memory device (*see* §IX.C.2[1.D]). Choi likewise teaches a charge-trapping device and discloses that an electric field removes fast charges. Choi, 1:2-12, 1:13-39. Nam’s voltage differential creates such an electric field to remove fast charges (*see* §IX.C.2[1.D]) and thus removes charges from “shallow[] trap[s] ... in a charge trap layer.” Choi, 1:13-39; Liu, ¶¶ 333-35.

12. Claim 13

Nam discloses the additional limitation of claim 13, or at least renders it obvious in view of Choi.

Claims 13 and 12 are substantively identical because the ’342 patent refers to “charges trapped in shallow traps” as “fast charges.” Ex. 1001, 1:33. Thus, Nam in view of Choi renders claim 13 obvious for the same reasons. *See* §IX.C.11; Liu, ¶ 338.

13. Claim 14

Nam discloses the additional limitation of claim 14, or at least renders it obvious in view of Choi.

A POSITA would have understood Nam to disclose this claim for the same reasons set forth in §IX.C.2[1.D]. Namely, Nam discloses a voltage differential (between a selected and adjacent unselected cell) that generates an electric field to move fast charges towards the unselected cell. *See* §§VIII.B-C, IX.C.2[1.D].

Nam in view of Choi—with its express disclosure of *removing fast charges*—also renders obvious this additional limitation. Choi expressly teaches “lateral charge loss”—which involves moving fast charges from the selected cell to a neighboring, unselected cell is the result of Nam’s voltage differential. Choi, 2:14-17; Liu, ¶ 341.

14. Claim 16

Claim 16 is an independent claim and requires:

[16.Pre]

[1.Pre] includes this preamble and, to the extent this preamble is limiting, is met for the same reasons. *See* §IX.C.2[1.Pre]; Liu, ¶ 343.

[16.A] “a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein:”

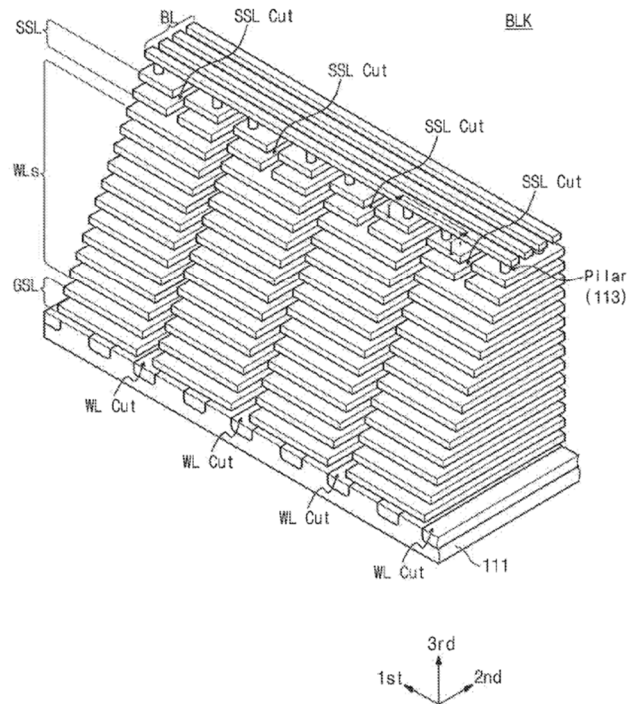
Nam discloses this limitation.

First, Nam discloses “a memory cell array” that includes “plurality of memory blocks.” Nam, [0063]-[0064], FIG. 1.

Second, the memory blocks “include a plurality of strings,” each of which include “a plurality of memory cells.” Nam, [0065].

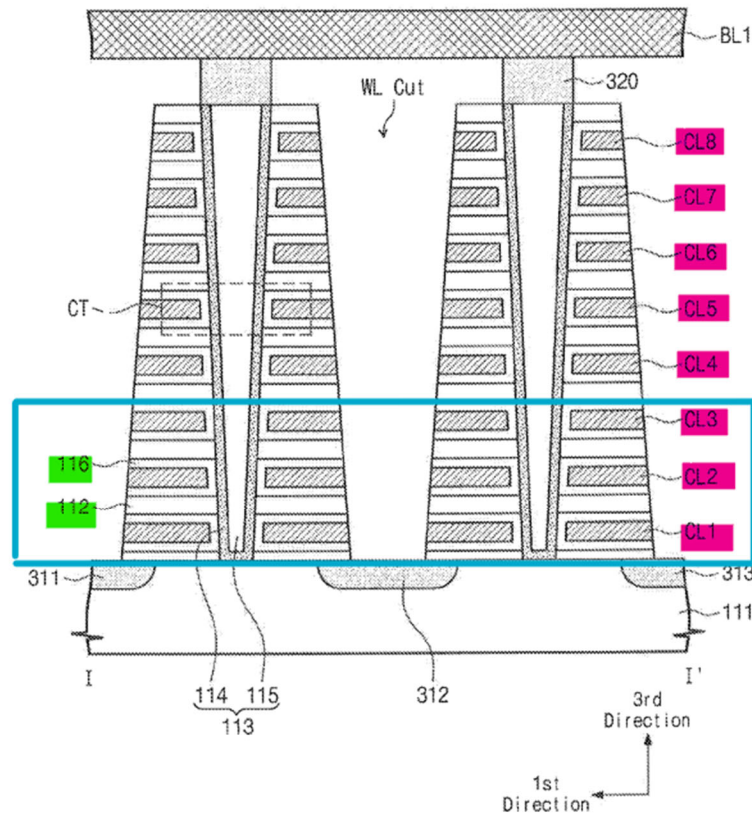
Third, as shown below, Nam discloses a 3D memory stack:

Fig. 2A



Nam, FIG. 2A. The above figure depicts the basic alternating stack of dielectric and conductive layers of a 3D NAND flash memory. *Id.*, [0164], Liu, ¶ 348. With reference to FIG. 2B below, Nam further discloses that “a plurality of insulation materials 112 may be provided sequentially along a third direction.” Nam, [0082]. These may be an oxide. *Id.* Additionally, “[i]nsulation films 116 may be provided on exposed surfaces of the insulation materials 112” *Id.*, [0086]. And, in spaces “between” these insulation film layers, “conductive materials CL1 to CL8” are “placed[.]” *Id.*, [0088], [0092].

Fig. 2B



Id., FIG. 2B (annotated).

Finally, Nam discloses that “[a] string may be formed by making a pillar 113 connected with a bit line BL penetrating the at least one string selection line SSL, the word lines WLs, and the at least one ground selection line GSL.” Nam, [0076], Liu, ¶¶ 344-49. That is, these *memory strings extend vertically* through the *film stack*. *Id.*

[16.A.i] “each memory string comprises a plurality of memory cells; and”

Nam discloses this limitation.

Nam discloses a “a plurality of *strings*,” each of which include “a *plurality of memory cells*.” Nam, [0065]; Liu, ¶ 351.

[16.A.ii] “each memory cell is addressable through a word line and a bit line; and”

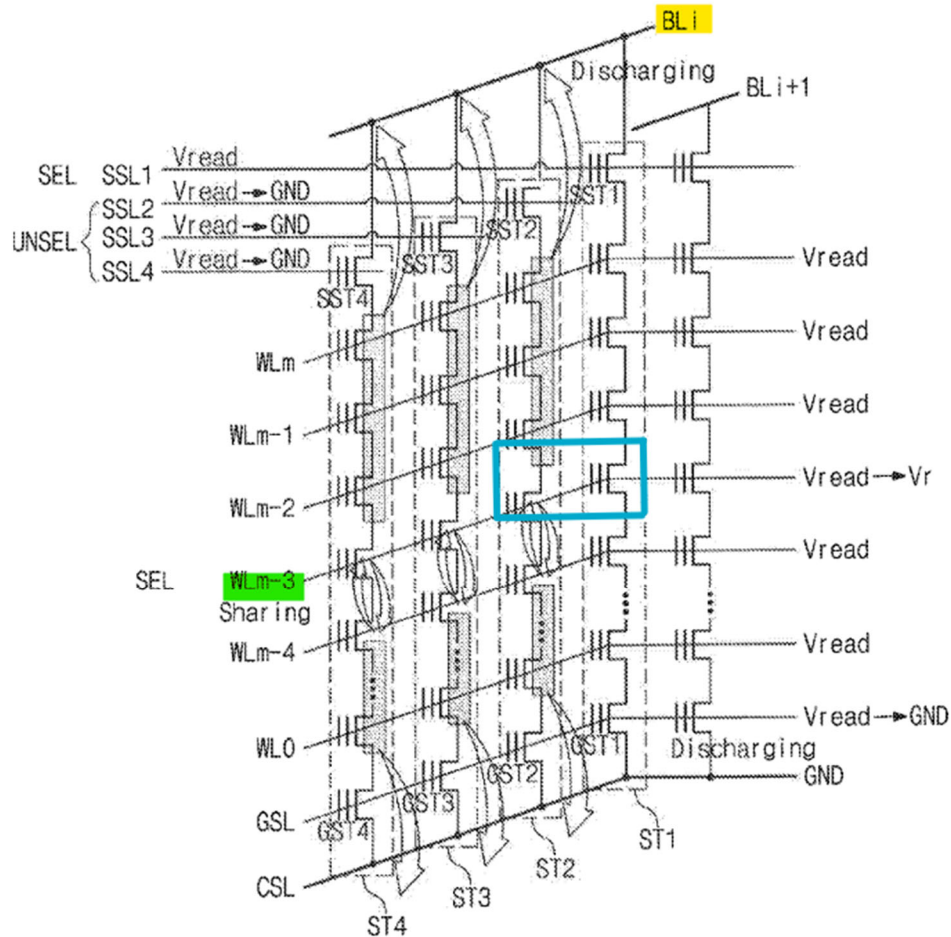
Nam discloses this limitation.

Nam’s memory device contains an “address decoder 120.” Nam, [0063]. Nam’s memory array can be “connected to the address decoder” via “word lines WLs.” *Id.*, [0064], [0094], [0096]. Similarly, the “memory cell array” can be “connected to the input/output circuit 130” via “bit lines BLs.” *Id.*, [0064]. In other words, the address decoder receives an external address and uses the word lines and bit lines to access the array. *Id.*, [0066]-[0067]; Liu, ¶ 353.

Further, *each memory cell is addressable through a word line and a bit line* as shown below:

Fig. 3

(Prior Art)



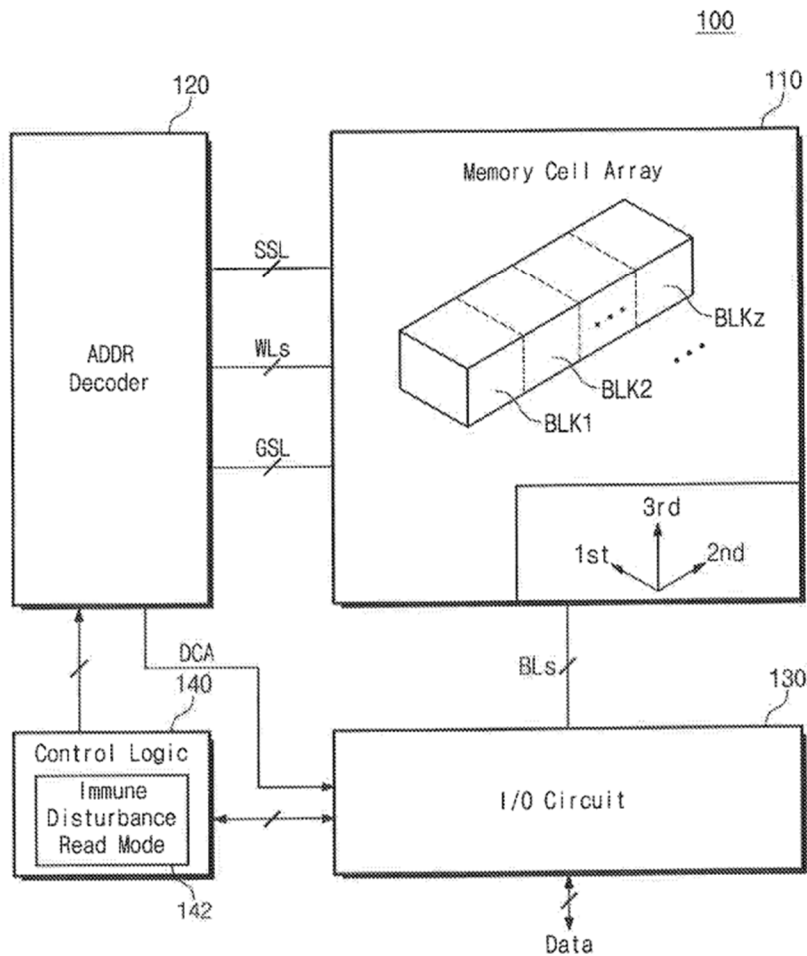
Nam, FIG. 3 (annotated); Liu, ¶ 354.

[16.B] “a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:”

Nam discloses, or at least renders obvious, this limitation.

As to *a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation*, the high-level components of Nam are shown below:

Fig. 1



Nam, FIG 1. Nam discloses that “[t]he control logic 140 may control an overall operation of the nonvolatile memory device 100 including ... a read operation....” *Id.*, [0069]. This includes applying voltages to conduct a read-verification operation on a memory cell. *See* §IX.C.2. Thus, Nam discloses *a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation*. *See* §IX.C.2 (describing disclosures of read-verification operation); Liu, ¶ 356.

As to *for removing fast charges during a first time period*, see §IX.C.2.[1.D]
(describing that fast charge loss occurs during WL Setup, i.e., *the first time period*).

[16.B.i]

This limitation is identical to Limitation [1.A] except for using “apply” instead of “applying.” See §IX.C.2[1.A].

[16.B.ii]

This limitation is identical to Limitation [1.B] except for using “apply” instead of “applying.” See §IX.C.2[1.B].

[16.B.iii]

This limitation is identical to Limitation [1.C] except for using “apply” instead of “applying.” See §IX.C.2[1.C].

15. Claim 17

This limitation is substantively the same as claims 2 and 3, namely, requiring (here by the *circuit*) that top and lower select gate voltages create connections, respectively, to the bit line and array common source. See §IX.C.3-4 (as to *circuit*, see §IX.C.14[16.B]).

16. Claim 19

Claim 19 depends from claim 16 and further requires:

[19.A] “a channel hole”

[19.B] “a core filling film in a center of the channel hole;”

[19.C] “a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and”

[19.D] “a channel layer sandwiched between the memory film and the core filling film.”

Nam in view of Choi renders these additional limitations obvious for the same reasons that Seo in view of Choi renders them obvious; namely, Choi discloses these additional limitations. *See* §IX.A.17.

17. Claim 20

This limitation is substantively the same as claim 12 (except recites *circuit*). *See* §IX.C.11 (as to *circuit*, *see* §IX.C.14[16.B]).

18. Motivation to Combine

A POSITA would have been motivated, with a reasonable expectation of success, to apply Choi’s teachings to Nam regarding fast charge removal and charge-trap memory cells.

First, both Nam and Choi address issues in the field of 3D NAND flash memory, and more specifically, read operations. Nam, [0013]-[0017], [0030]; Choi, 1:14-26. And Choi describes the physics underlying certain of these issues (fast charges). Thus, a POSITA would have been motivated to consider Choi to understand and improve on Nam’s memory device. Liu, ¶ 368.

Second, Nam focuses on post-read disturbance while Choi focuses on fast-charge loss. *See* §§VIII.B-C. In other words, Choi's teachings are particularly instructive to Nam's WL Setup, which Nam does not detail. Thus, a POSITA would have been motivated to consider Choi's teachings to improve and understand issues relating to the WL Setup period. Liu, ¶ 369.

Third, Nam creates a voltage differential by applying a higher voltage on unselected word lines than on the selected word lines during the first time period (WL Setup). *See* §IX.C.2[1.D]. A POSITA would have been motivated to consider the effect of this, which Choi addresses. And Choi expressly teaches the effect in the context of program-verify operations. Choi, FIG. 2; Liu, ¶ 370.

Fourth, while Nam does not detail its charge-trap memory cell disclosures, Choi details the various components. Choi also details the advantages of charge-trap memories. *See* §IX.A.19; Liu, ¶ 371.

A POSITA would have had a reasonable expectation of success in applying Choi's fast-charge-removal and charge-trap memory cell teachings to Nam. Liu, ¶¶ 372-76. First, Nam's memory is structurally similar to Choi's from a high-level perspective. *Compare* Nam, FIGs. 2A, 2B, 5 *with* Choi, FIGs. 1, 5. Second, Choi teaches the device physics of Nam's read operation as it relates to fast charges, thus detailing Nam's operational characteristics. Third, Choi makes clear that Nam's read operation would remediate fast charge issues in a verification that occurs close

in time to a program operation. Finally, charge-trap memories were textbook material in 2019. *See* §IX.A.19.

D. Ground 4: Claim 15 Is Obvious Over Nam in View of Choi and Izumi

1. Claim 15

Claim 15 depends from claim 1 and further requires:

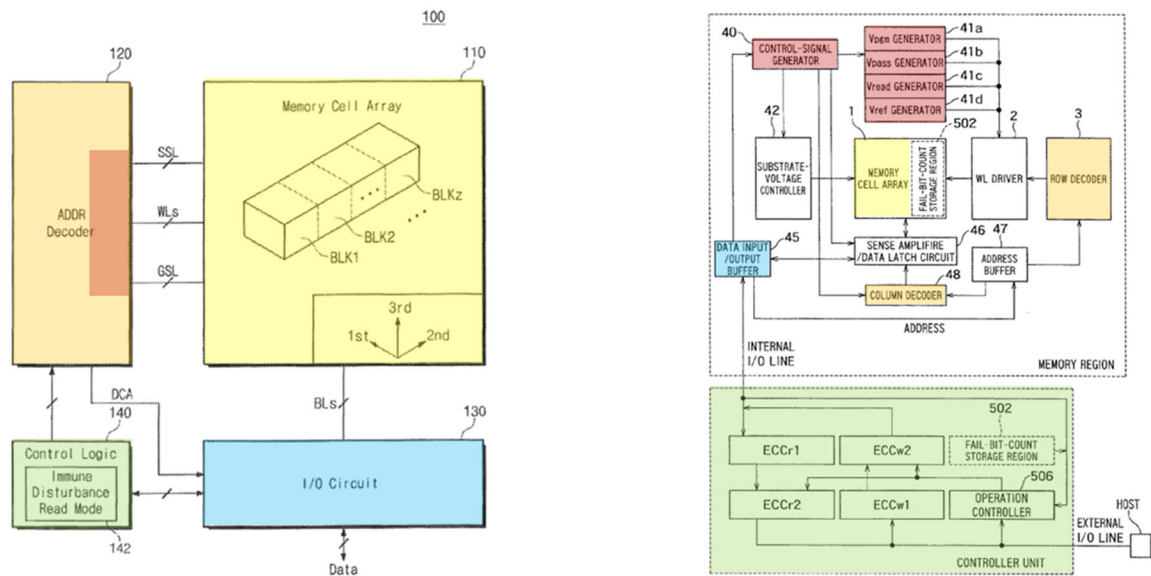
[15] “wherein conducting the read-verification operation comprises conducting a failed bit count in parallel.”

Nam in view of Choi and Izumi renders this additional limitation obvious for the same reason that Seo in view of Choi and Izumi renders it obvious. §IX.B.1 (see Izumi disclosures of this limitation).

Furthermore, a POSITA would have found it obvious to combine Nam with Izumi. First, a POSITA would have been motivated to incorporate Izumi’s failed-bit count into Nam because Izumi teaches an improvement over Nam’s existing ECC embodiment. It was common knowledge that read operations of nonvolatile NAND memory devices were subject to various factors affecting their accuracy. *See, e.g.,* Nam, [0159]; Choi, 1:16-20; Liu, ¶ 379. Nam’s disclosure regarding both read-disturb-effect improvement and ECC shows that both are desirable to improve read-operation reliability. A POSITA would have known that ECC used in both Nam and Izumi was a well-known mechanism for detecting and correcting failed bits. Izumi, [0003]-[0004]; Liu, ¶ 379. Importantly, Izumi teaches an approach of selectively activating one or two ECC circuits to tailor ECC capability to the device condition,

reducing power consumption. Izumi, [0078], [0082]. Thus, a POSITA would have found Izumi's low-power ECC techniques a desirable improvement to Nam's ECC circuits. Liu, ¶ 379. This would have been an obvious extension of Nam's existing hardware and purpose. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (noting how "predictable variation[s]" of the prior art's teachings are obvious).

Additionally, not only would a POSITA have recognized the benefits of Izumi's teachings, that POSITA naturally would have looked to Izumi because both Nam and Izumi are in the same field and involve the same high-level functions. Both references are in the same field (NAND flash memory). Both disclose memory devices comprising the same components, e.g., a decoder and control logic:



Nam, FIG. 1; Izumi, FIG. 6 (both annotated). Both aim to improve read-operation accuracy. Nam, [0062], [0069]; Izumi, [0003]-[0004]. Although Izumi discloses a 2D NAND flash, a POSITA would have known that failed bits are a concern

regardless of the dimensionality of the flash, and that Izumi's failed-bit-count and ECC techniques also apply to 3D NAND flash. Liu, ¶ 380. Indeed, Nam discloses an ECC circuit in its memory devices. Nam, FIG. 22, [0171]-[0173].

Considering these analogous objectives and designs, a POSITA would have found it obvious that Izumi's disclosure of failed-bit counting and ECC can be incorporated with Nam's ECC circuit. Liu, ¶ 381. And a POSITA would have had a reasonable expectation of success combining them because they disclose analogous and compatible components, and both disclose using ECC for failed-bit correction. Thus, combining their known techniques on a conventional NAND device would have a predictable result.

As explained above, Choi simply renders explicit a POSITA's understanding that Nam's read-verification operations remove fast charges, and thus has no impact on the combination. Liu, ¶ 382.

X. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XI. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests institution of IPR and cancellation of claims 1-6 and 8-20.

Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,774 words.

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on April 26, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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