PTO/AIA/15 (10-17)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4123.0850002
First Named Inventor	Zilong CHEN
Title	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. ☐ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification** [*Total Pages* 25] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. ☑ **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 8]
6. **Inventor's Oath or Declaration** [*Total Pages* 4] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☐ Newly executed (original or copy)
   b. ☑ A copy from a prior application (37 CFR 1.63(d))
7. ☑ **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   ☐ Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

ACCOMPANYING APPLICATION PAPERS

10. ☐ **Assignment Papers** (cover sheet & document(s)) Name of Assignee Yangtze Memory Technologies Co., Ltd.
11. ☐ **37 CFR 3.73(c) Statement** (*when there is an assignee*) ☑ **Power of Attorney**
12. ☐ **English Translation Document** (*if applicable*)
13. ☑ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
14. ☐ **Preliminary Amendment**
15. ☐ **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. ☐ **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. ☐ **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. ☑ **Other:** Authorization for Extension of Time under 37 CFR 1.136(a)(3)

*Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 26111 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Donald J. Featherstone/	Date	5/19/21
Name (Print/Type)	Donald J. Featherstone	Registration No. (Attorney/Agent)	33,876

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0850002
	Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zilong		CHEN	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.
Address 2	No. 88 Weilai 3rd Rd, East Lake High-Tech Dev Zone

City	Wuhan, Hubei	State/Province	
Postal Code		Country [i]	CN

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xiang		FU	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.
Address 2	No. 88 Weilai 3rd Rd, East Lake High-Tech Dev Zone

City	Wuhan, Hubei	State/Province	
Postal Code		Country [i]	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Micron Ex. 1002, p. 2
Micron v. YMTC
IPR2024-00793

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0850002
	Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY	

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	26111		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		
Attorney Docket Number	4123.0850002	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	26111		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0850002
	Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16729838	2019-12-30
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16729838	Continuation of	PCT/CN2019/112728	2019-10-23

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Micron Ex. 1002, p. 4
Micron v. YMTC
IPR2024-00793

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0850002
	Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0850002
	Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	No. 88 Weilai 3rd Rd, East Lake High-Tech Dev Zone		
Address 2			
City	Wuhan, Hubei	**State/Province**	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0850002
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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Yangtze Memory Technologies Co., Ltd.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	No. 88 Weilai 3rd Rd, East Lake High-Tech Dev Zone		
Address 2			
City	Wuhan, Hubei	**State/Province**	
Country i	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Donald J. Featherstone/			Date (YYYY-MM-DD)	2021-05-19
First Name	Donald J.	Last Name	Featherstone	Registration Number	33,876

Additional Signature may be generated within this form by selecting the Add button. Add

Micron Ex. 1002, p. 7
Micron v. YMTC
IPR2024-00793

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0850002
	Application Number	
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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Micron Ex. 1002, p. 9
Micron v. YMTC
IPR2024-00793

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/729,838

filed on December 30, 2019

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is No. 88 Weilai 3rd Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**, for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

Micron Ex. 1002, p. 10
Micron v. YMTC
IPR2024-00793

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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32766-09/03/2020 10:28

Micron Ex. 1002, p. 11
Micron v. YMTC
IPR2024-00793

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Zilong CHEN** Date: 2020-03-09

Signature of Inventor: Zilong CHEN

LEGAL NAME OF INVENTOR

Inventor: **Xiang FU** Date: 2020-03-09

Signature of Inventor: Xiang Fu

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Micron Ex. 1002, p. 12
Micron v. YMTC
IPR2024-00793

SCHEDULE A

UNITED STATES PATENTS, UNITED STATES PATENT APPLICATIONS AND INTERNATIONAL APPLICATIONS THAT DESIGNATE THE UNITED STATES

Application No.	Filing Date	Patent No.	Issue Date
PCT/CN2019/112728	October 23, 2019		

OTHER INTERNATIONAL APPLICATIONS AND PATENTS

Country	Application No.	Filing Date

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Micron Ex. 1002, p. 13
Micron v. YMTC
IPR2024-00793

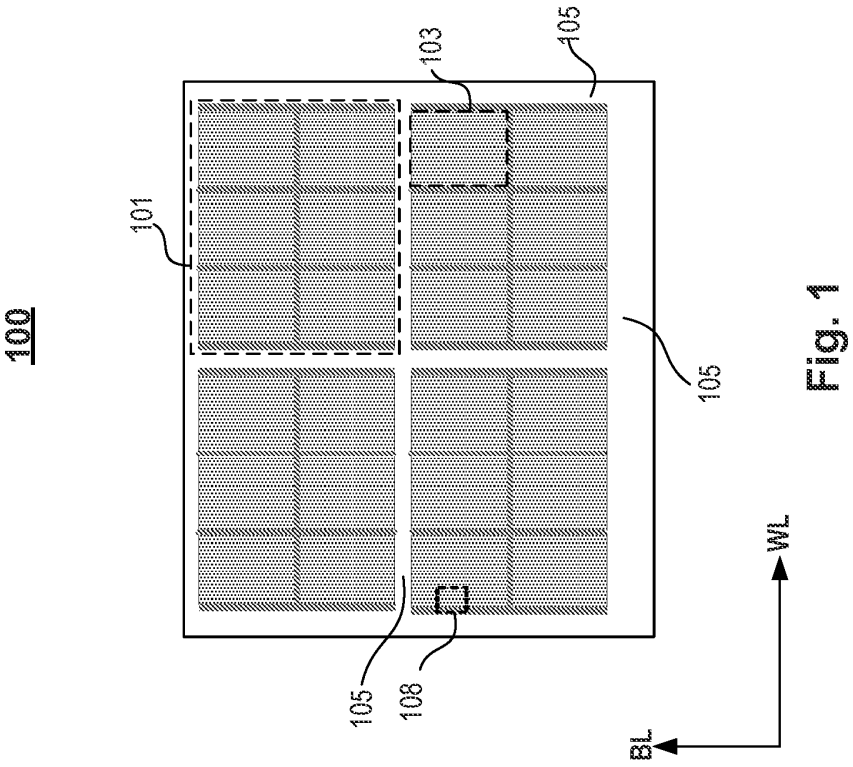


Fig. 1

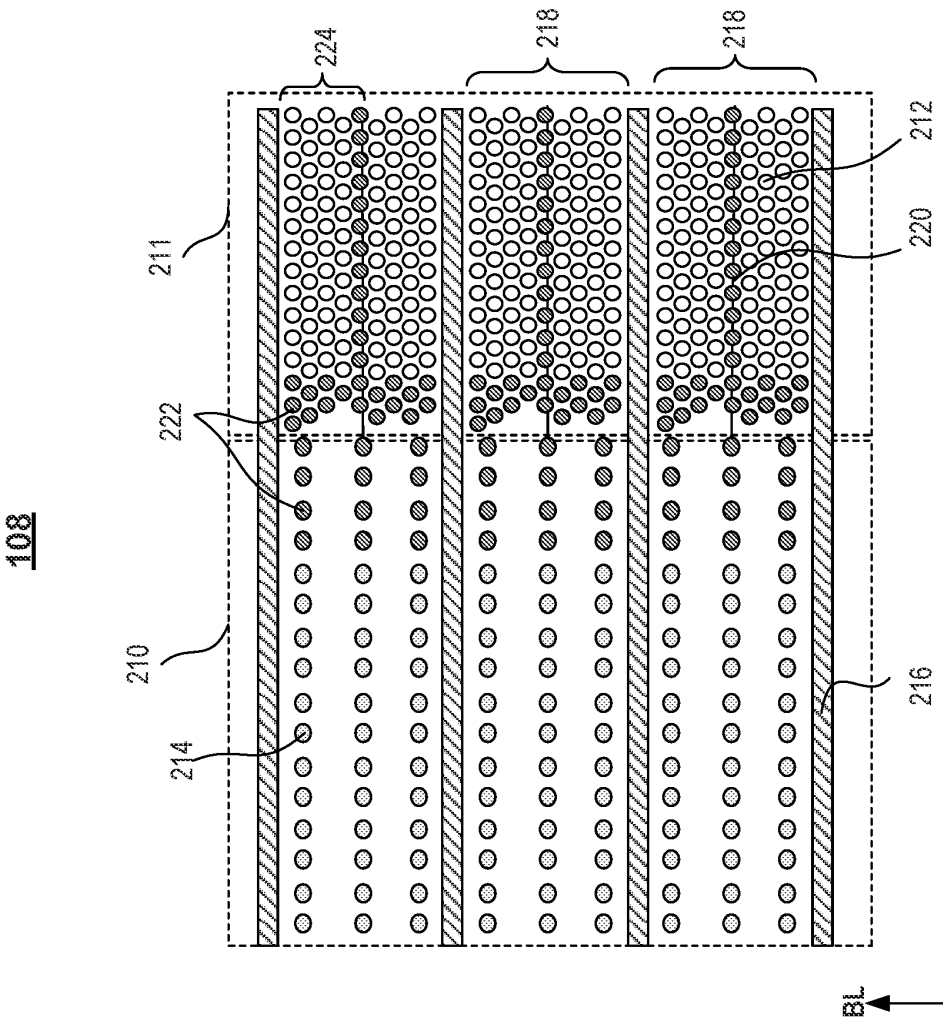


Fig. 2

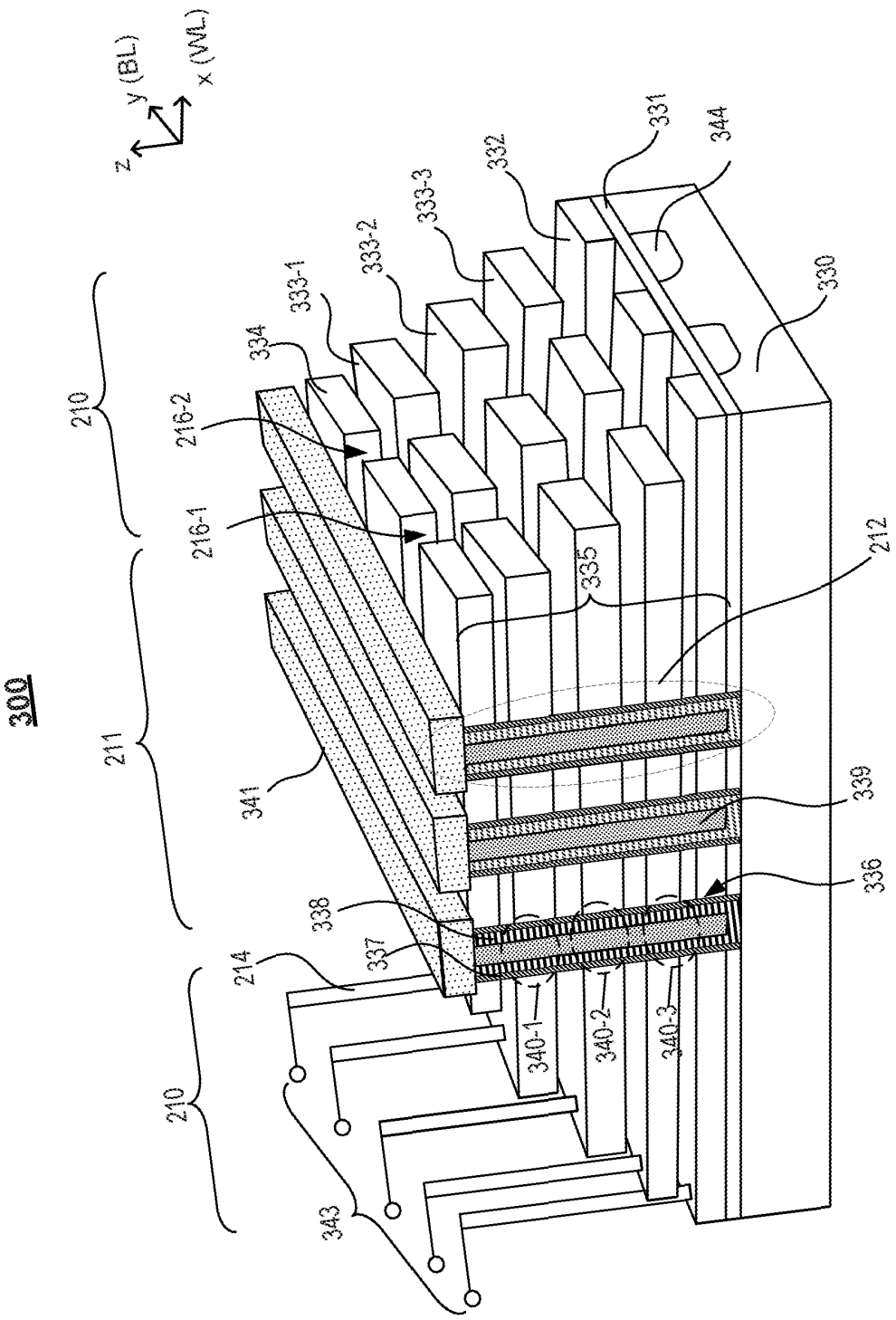

300
z
y (BL)
x (WL)
210
211
210
216-2
216-1
334
333-1
333-2
333-3
332
331
344
330
335
212
341
339
336
338
337
214
340-1
340-2
340-3
343

Fig. 3

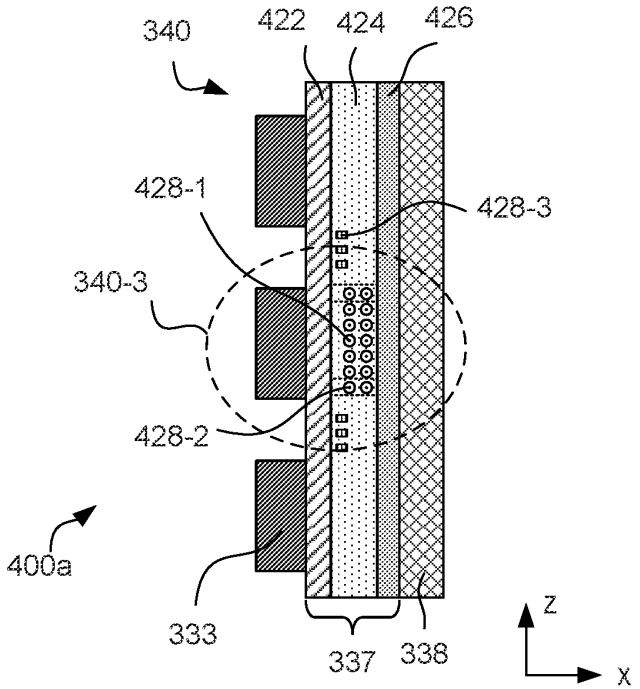


Fig. 4A

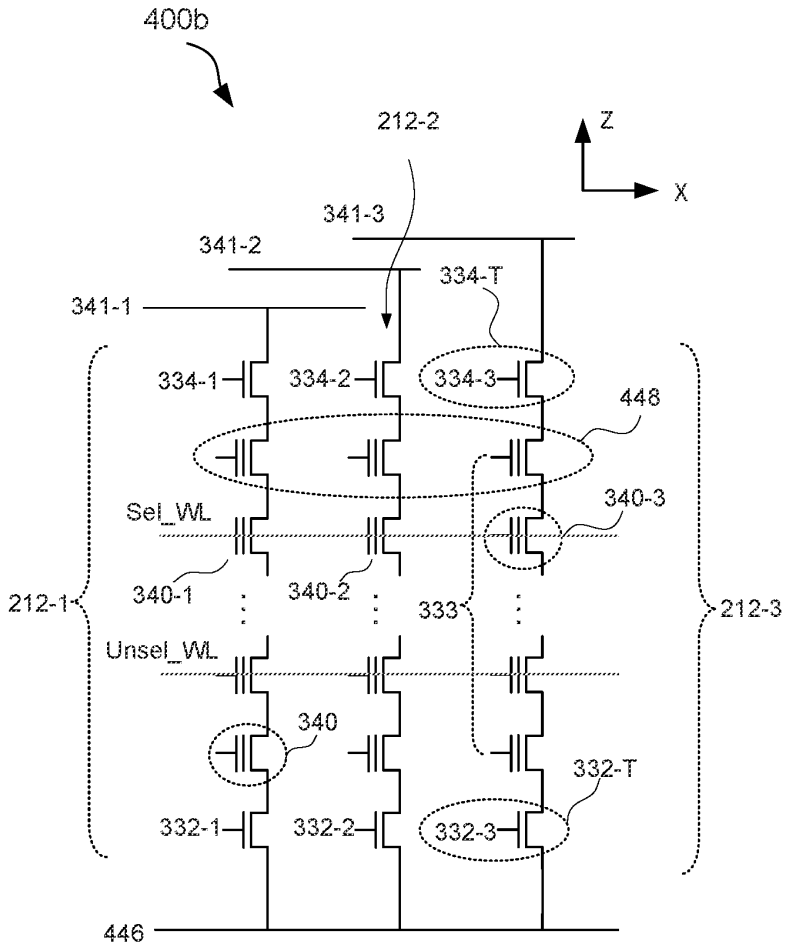


Fig. 4B

Micron Ex. 1002, p. 17
Micron v. YMTC
IPR2024-00793

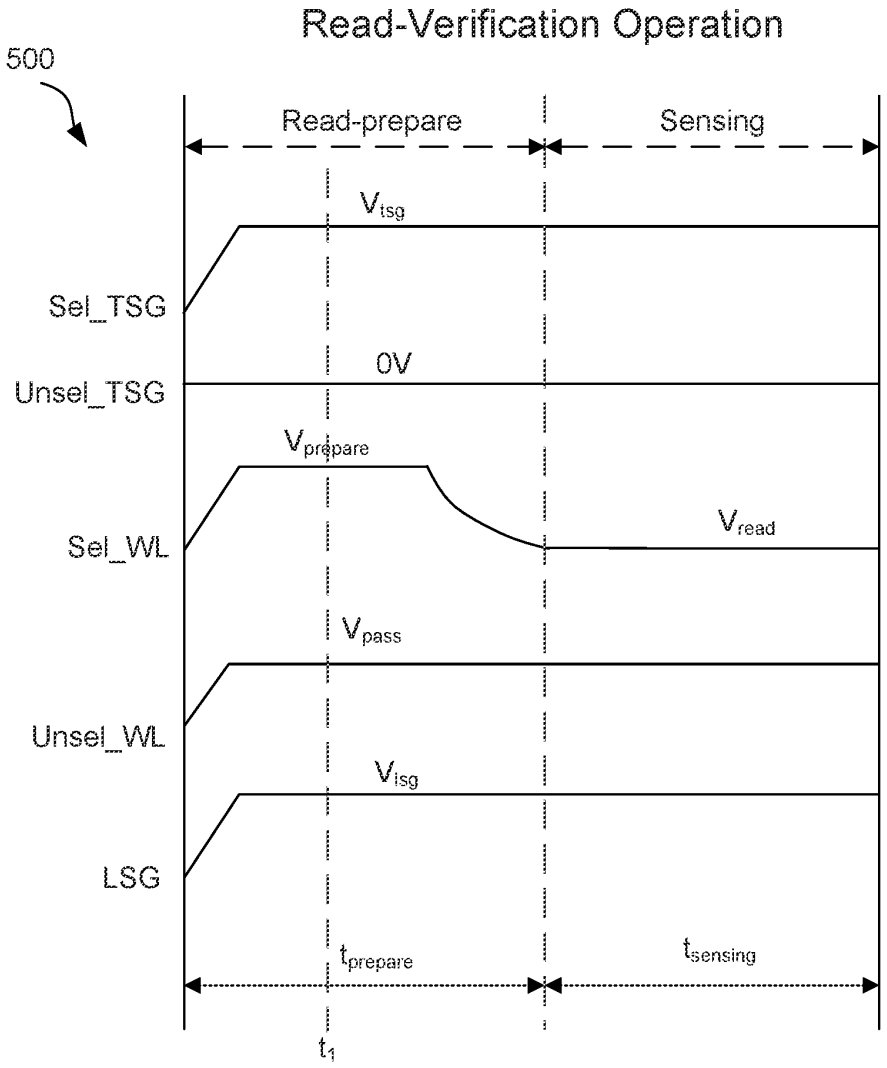


Fig. 5

Micron Ex. 1002, p. 18
Micron v. YMTC
IPR2024-00793

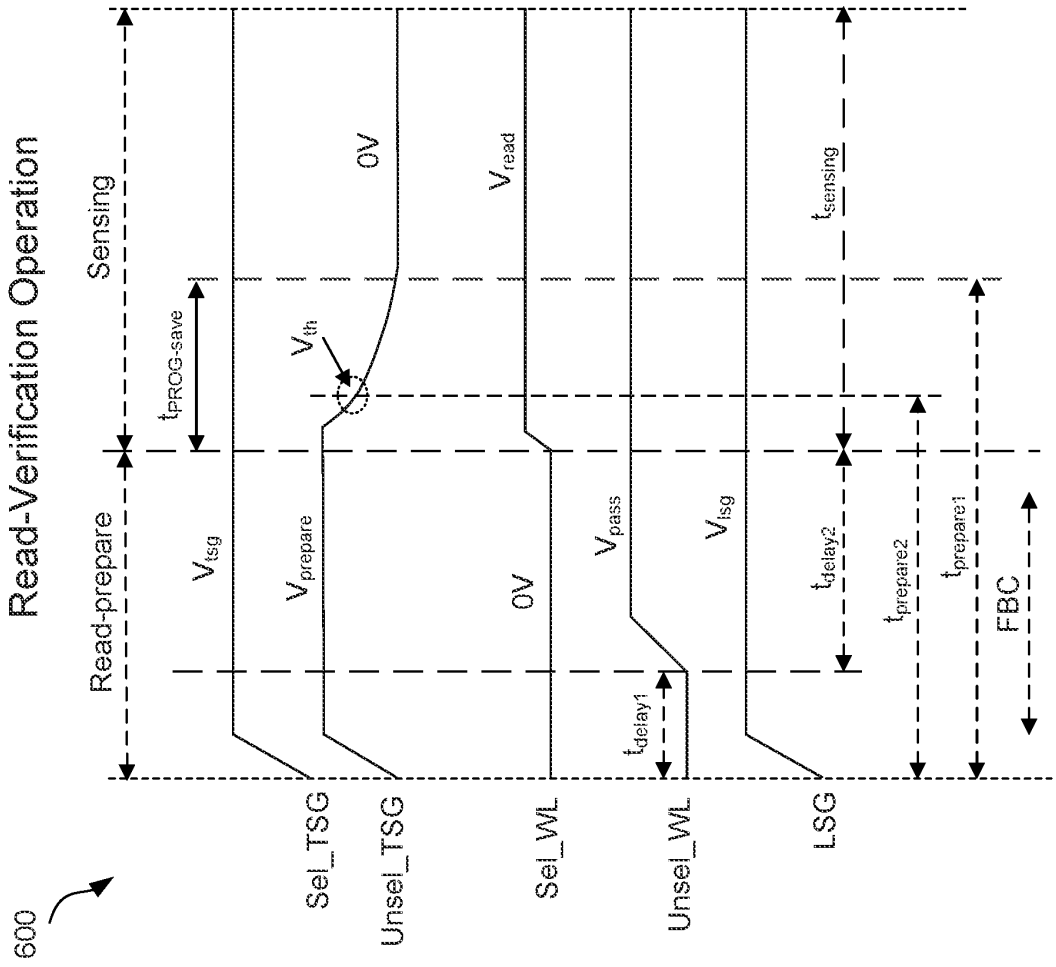

Read-Verification Operation
600
Read-prepare
Sensing
$t_{PROG-save}$
V_{tsg}
$V_{prepare}$
0V
V_{th}
V_{read}
$t_{sensing}$
0V
V_{pass}
V_{lsg}
t_{delay2}
$t_{prepare2}$
$t_{prepare1}$
FBC
t_{delay1}
Sel_TSG
Unsel_TSG
Sel_WL
Unsel_WL
LSG

Fig. 6

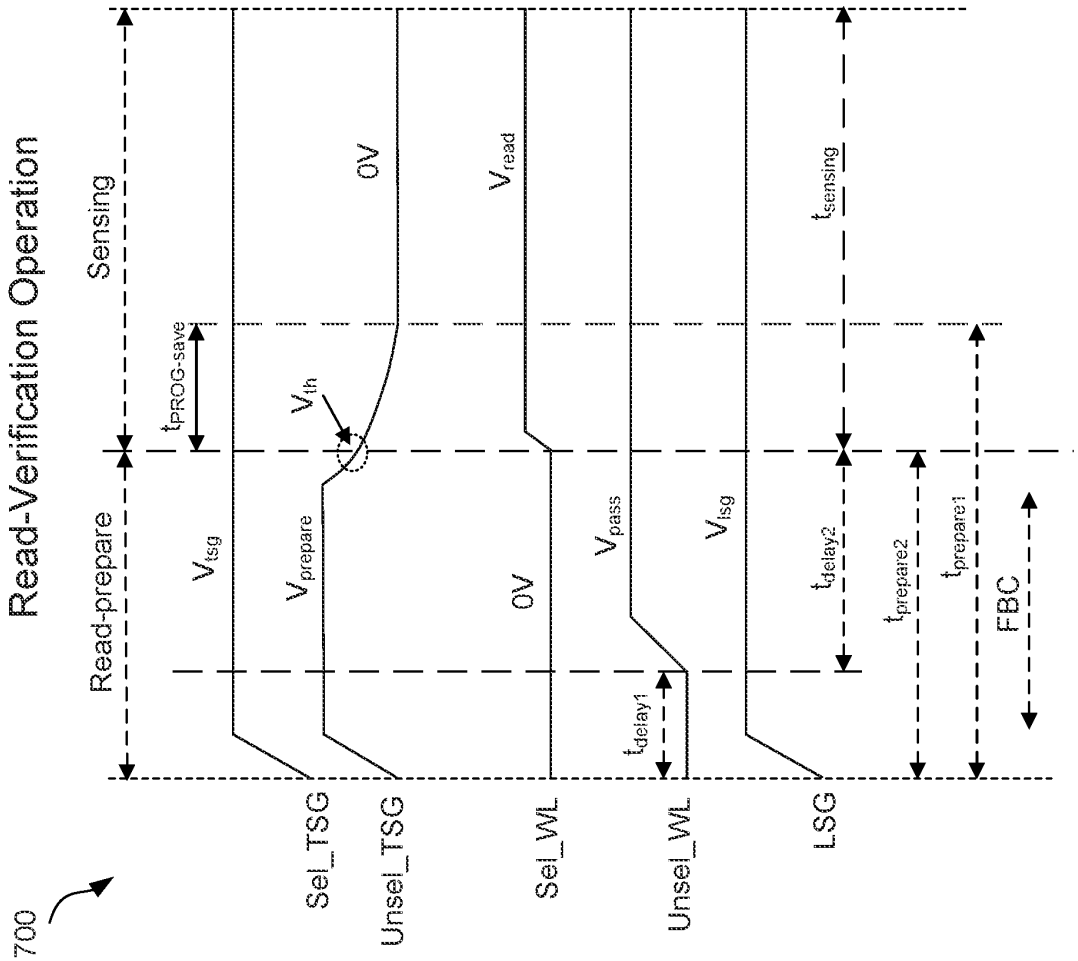

Read-Verification Operation
700
Read-prepare
Sensing
$t_{PROG-save}$
V_{tsg}
$V_{prepare}$
V_{th}
0V
V_{read}
0V
V_{pass}
V_{lsg}
$t_{sensing}$
t_{delay2}
$t_{prepare2}$
$t_{prepare1}$
FBC
t_{delay1}
Sel_TSG
Unsel_TSG
Sel_WL
Unsel_WL
LSG

Fig. 7

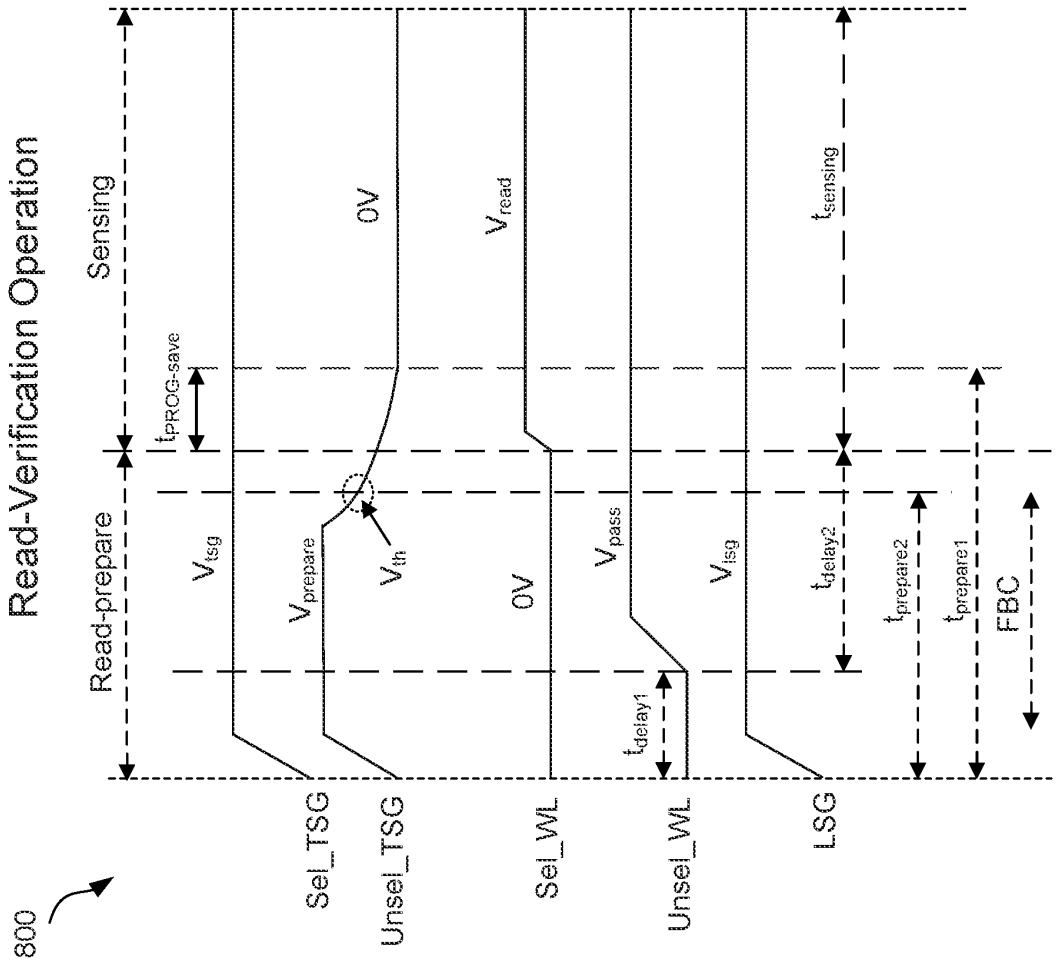

Read-Verification Operation
800
Read-prepare
Sensing
$t_{PROG-save}$
V_{tsg}
$V_{prepare}$
V_{th}
0V
V_{read}
0V
V_{pass}
V_{lsg}
t_{delay1}
t_{delay2}
$t_{prepare2}$
$t_{prepare1}$
FBC
$t_{sensing}$
Sel_TSG
Unsel_TSG
Sel_WL
Unsel_WL
LSG

Fig. 8

ABSTRACT

A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device includes removing fast charges of the target memory cell at a read-prepare step and measuring a threshold voltage of the target memory cell at a sensing step. Removing the fast charges of the target memory cell includes applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).

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Micron Ex. 1002, p. 22
Micron v. YMTC
IPR2024-00793

WHAT IS CLAIMED IS:

1. A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:

applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period;

applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and

applying, on an unselected word line, a pass voltage during the first time period and the second time period,

wherein the read-verification operation removes fast charges of the target memory cell during the first time period.

2. The method of claim 1, further comprising:

applying, on a selected top select gate of a selected memory string containing the target memory cell, a top select gate voltage during the first time period and the second time period; and

applying, on a lower select gate of the selected memory string containing the target memory cell, a lower select gate voltage during the first time period and the second time period.

3. The method of claim 2, wherein the applying the top select gate voltage comprises electrically connecting the selected memory string to a bit line; and the applying the lower select gate voltage comprises electrically connecting the selected memory string to an array common source.

4. The method of claim 2, wherein the applying the pass voltage comprises applying the pass voltage with a delay period after the selected top select gate and the lower select gate are at the top select gate voltage and the lower select gate voltage, respectively.

5. The method of claim 1, further comprising:

measuring a threshold voltage of the target memory cell during the second time period.

Micron Ex. 1002, p. 23
Micron v. YMTC
IPR2024-00793

6. The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell.

7. The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell.

8. The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is lower than a threshold voltage of an unselected memory cell.

9. The method of claim 1, wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V.

10. The method of claim 1, wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V.

11. The method of claim 1, wherein applying the off voltage comprises applying a voltage about 0V.

12. The method of claim 1, wherein the removing the fast charges comprises:

removing the fast charges from a storage layer of the target memory cell.

13. The method of claim 1, wherein the removing the fast charges comprises:

removing electrical charges from shallow traps in the storage layer of the target memory cell.

14. The method of claim 1, wherein the removing the fast charges comprises:

removing the fast charges from the target memory cell to a neighboring unselected memory cell.

15. The method of claim 1, wherein conducting the read-verification operation comprises conducting a failed bit count in parallel.

Micron Ex. 1002, p. 24
Micron v. YMTC
IPR2024-00793

16. A three-dimensional (3D) memory device, comprising:

a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein:

each memory string comprises a plurality of memory cells; and

each memory cell is addressable through a word line and a bit line; and

a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:

apply, on an unselected top select gate of an unselected memory string, a prepare voltage during the first time period and an off voltage during a second time period;

apply, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and

apply, on an unselected word line, a pass voltage during the first time period and the second time period.

17. The 3D memory device of claim 16, wherein the circuit is further configured to:

electrically connect a selected memory string containing the target memory cell to the bit line and an array common source by applying a top select gate voltage on a selected top select gate and applying a lower select gate voltage on a lower select gate during the first time period and the second time period.

18. The 3D memory device of claim 17, wherein to remove the fast charges of the target memory cell, the circuit is further configured to:

apply the top select gate voltage on the selected top select gate and the lower select gate voltage on the lower select gate before applying the pass voltage on the unselected word line.

19. The 3D memory device of claim 16, wherein each memory string comprises:

a channel hole;

a core filling film in a center of the channel hole;

Micron Ex. 1002, p. 25
Micron v. YMTC
IPR2024-00793

a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and

a channel layer sandwiched between the memory film and the core filling film.

20. The 3D memory device claim 19, wherein the circuit is further configured to remove the fast charges from a portion of the storage layer associated with the target memory cell.

Micron Ex. 1002, p. 26
Micron v. YMTC
IPR2024-00793

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS AND INCORPORATION BY REFERENCE

[0001] This application is a continuation of U.S. patent application No. 16/729,838 filed on December 30, 2019 and titled "Method for Reading Three-Dimensional Flash Memory," which claims priority to PCT/CN2019/112728 filed on October 23, 2019, both of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a method for reading a three-dimensional (3D) memory.

BACKGROUND

[0003] As memory devices are shrinking to smaller die size to reduce manufacturing cost and increase storage density, scaling of planar memory cells faces challenges due to process technology limitations and reliability issues. A three-dimensional (3D) memory architecture can address the density and performance limitation in planar memory cells.

[0004] In a 3D NAND flash memory, memory cells can be programmed for data storage based on charge-trapping technology. The storage information of a memory cell depends on the amount of charge trapped in a storage layer. However, fast charges, *i.e.*, charges trapped in shallow traps, can be easily lost. Therefore, the threshold voltage determining the stored information can be different between write and read operations. Accordingly, a read-prepare step is included in a read-verification operation after programming to remove the fast charges and verify the threshold voltage of the memory cell. Fast charge loss depending on the intrinsic de-trapping process in the storage layer can be long, making the read-verification operation inefficient. Therefore, a need exists for a method to accelerate fast charge loss so that threshold voltage or storage information of the memory cell can be verified or read more accurately and efficiently.

BRIEF SUMMARY

[0005] Embodiments of a method for conducting read-verification operation of a memory cell in a three-dimensional (3D) memory device is described in the present disclosure.

[0006] One aspect of the present disclosure provides a method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device. The method includes removing fast charges of the target memory cell at a read-prepare step, which includes applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL). The method also includes measuring a threshold voltage of the target memory cell at a sensing step.

[0007] In some embodiments, the method further includes applying a top select gate voltage (V_{tsg}) on a selected top select gate (Sel_TSG) of a selected memory string containing the target memory cell, and applying a lower select gate voltage (V_{lsg}) on a lower select gate (LSG) of the selected memory string containing the target memory cell.

[0008] In some embodiments, applying the top select gate voltage (V_{tsg}) includes electrically connecting the selected memory string to a bit line. In some embodiments, applying the lower select gate voltage (V_{lsg}) includes electrically connecting the selected memory string to an array common source.

[0009] In some embodiments, applying the top select gate voltage (V_{tsg}) includes applying a voltage between 4V to 7V. In some embodiments, applying the lower select gate voltage (V_{lsg}) includes applying a voltage between 4V to 7V.

[0010] In some embodiments, applying the pass voltage (V_{pass}) includes applying the pass voltage with a delay period after the selected top select gate (Sel_TSG) and the lower select gate (LSG) are at the top select gate voltage (V_{tsg}) and the lower select gate voltage (V_{lsg}), respectively.

[0011] In some embodiments, measuring the threshold voltage includes applying a read voltage (V_{read}) on the selected word line (Sel_WL). In some embodiments, applying the read voltage (V_{read}) includes applying a voltage between 0 to 2V. In some embodiments, applying the read voltage (V_{read}) includes applying a second off voltage on the unselected word line

Micron Ex. 1002, p. 28
Micron v. YMTC
IPR2024-00793

(Unsel_WL). In some embodiments, applying the second off voltage on the unselected word line (Unsel_WL) includes applying a 0V.

[0012] In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is higher than a threshold voltage of an unselected memory cell. In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) equals to a threshold voltage of an unselected memory cell. In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is lower than a threshold voltage of an unselected memory cell.

[0013] In some embodiments, applying the prepare voltage ($V_{prepare}$) includes applying a voltage between 4V to 7V. In some embodiments, applying the first off voltage (V_{off}) includes applying a 0V. In some embodiments, applying the pass voltage (V_{pass}) includes applying a voltage between 5V to 9V.

In some embodiments, removing the fast charges includes removing the fast charges from a storage layer of the target memory cell of a selected memory string, wherein the selected memory string includes a channel hole penetrating vertically through a film stack of alternating conductive and dielectric layers, a core filling film in a center of the channel hole, and a memory film covering a sidewall of the channel hole. The selected memory string also includes a channel layer sandwiched between the memory film and the core filling film. In some embodiments, the memory film includes a barrier layer, the storage layer and a tunneling layer.

[0014] In some embodiments, removing the fast charges includes removing electrical charges from shallow traps in the storage layer of the target memory cell.

[0015] In some embodiments, removing the fast charges includes removing the fast charges from the target memory cell to a neighboring unselected memory cell.

[0016] In some embodiments, conducting the read-verification operation comprises conducting the read-prepare step and conducting a failed bit count in parallel.

[0017] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

Micron Ex. 1002, p. 29
Micron v. YMTC
IPR2024-00793

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0019] Fig. 1 illustrates a schematic top-down view of an exemplary three-dimensional (3D) memory die, according to some embodiments of the present disclosure.

[0020] Fig. 2 illustrates a schematic top-down view of a region of 3D memory die, according to some embodiments of the present disclosure.

[0021] Fig. 3 illustrates a perspective view of a portion of an exemplary 3D memory array structure, in accordance with some embodiments of the present disclosure.

[0022] Fig. 4A illustrates a cross-sectional view of 3D memory cells, according to some embodiments of the present disclosure.

[0023] Fig. 4B illustrates a schematic diagram of a 3D memory array, according to some embodiments of the present disclosure.

[0024] Fig. 5 illustrates a timing diagram of a read-verification operation with a prepare voltage (pre-pulse) applied on a selected word line, according to some embodiments of the present disclosure.

[0025] Figs. 6-8 illustrate timing diagrams of read-verification operations with accelerated fast charge loss, according to some embodiments of the present disclosure.

[0026] The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

[0027] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

Micron Ex. 1002, p. 30
Micron v. YMTC
IPR2024-00793

DETAILED DESCRIPTION

[0028] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0029] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0030] In general, terminology can be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term "based on" can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0031] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something, but also includes the meaning of "on" something with an intermediate feature or a layer there between. Moreover, "above" or "over" not only means

Micron Ex. 1002, p. 31
Micron v. YMTC
IPR2024-00793

"above" or "over" something, but can also include the meaning it is "above" or "over" something with no intermediate feature or layer there between (i.e., directly on something).

[0032] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, can be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or process step in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0033] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate includes a "top" surface and a "bottom" surface. The top surface of the substrate is typically where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate unless stated otherwise. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0034] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, there above, and/or there below. A layer can include multiple layers. For

Micron Ex. 1002, p. 32
Micron v. YMTC
IPR2024-00793

example, an interconnect layer can include one or more conductive and contact layers (in which contacts, interconnect lines, and/or vertical interconnect accesses (VIAs) are formed) and one or more dielectric layers.

[0035] In the present disclosure, for ease of description, "tier" is used to refer to elements of substantially the same height along the vertical direction. For example, a word line and the underlying gate dielectric layer can be referred to as "a tier," a word line and the underlying insulating layer can together be referred to as "a tier," word lines of substantially the same height can be referred to as "a tier of word lines" or similar, and so on.

[0036] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process step, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0037] In the present disclosure, the term "horizontal/horizontally/lateral/laterally" means nominally parallel to a lateral surface of a substrate, and the term "vertical" or "vertically" means nominally perpendicular to the lateral surface of a substrate.

[0038] As used herein, the term "3D memory" refers to a three-dimensional (3D) semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate.

[0039] Fig. 1 illustrates a top-down view of an exemplary three-dimensional (3D) memory device 100, according to some embodiments of the present disclosure. The 3D memory device 100 can be a memory chip (package), a memory die or any portion of a memory die, and can include one or more memory planes 101, each of which can include a plurality of memory blocks 103. Identical and concurrent operations can take place at each memory plane 101. The memory block 103, which can be megabytes (MB) in size, is the smallest size to carry out erase operations. Shown in Fig. 1, the exemplary 3D memory device 100 includes four memory planes 101 and each memory plane 101 includes six memory blocks

Micron Ex. 1002, p. 33
Micron v. YMTC
IPR2024-00793

103. Each memory block 103 can include a plurality of memory cells, where each memory cell can be addressed through interconnections such as bit lines and word lines. The bit lines and word lines can be laid out perpendicularly (e.g., in rows and columns, respectively), forming an array of metal lines. The direction of bit lines and word lines are labeled as "BL" and "WL" in Fig. 1. In this disclosure, memory block 103 is also referred to as a "memory array" or "array." The memory array is the core area in a memory device, performing storage functions.

[0040] The 3D memory device 100 also includes a periphery region 105, an area surrounding memory planes 101. The periphery region 105 contains many digital, analog, and/or mixed-signal circuits to support functions of the memory array, for example, page buffers, row and column decoders and sense amplifiers. Peripheral circuits use active and/or passive semiconductor devices, such as transistors, diodes, capacitors, resistors, etc., as would be apparent to a person of ordinary skill in the art.

[0041] It is noted that, the arrangement of the memory planes 101 in the 3D memory device 100 and the arrangement of the memory blocks 103 in each memory plane 101 illustrated in Fig. 1 are only used as an example, which does not limit the scope of the present disclosure.

[0042] Referring to Fig. 2, an enlarged top-down view of a region 108 in Fig. 1 is illustrated, according to some embodiments of the present disclosure. The region 108 of the 3D memory device 100 can include a staircase region 210 and a channel structure region 211. The channel structure region 211 can include an array of memory strings 212, each including a plurality of stacked memory cells. The staircase region 210 can include a staircase structure and an array of contact structures 214 formed on the staircase structure. In some embodiments, a plurality of slit structures 216, extending in WL direction across the channel structure region 211 and the staircase region 210, can divide a memory block into multiple memory fingers 218. At least some slit structures 216 can function as the common source contact (e.g., array common source) for an array of memory strings 212 in channel structure regions 211. A top select gate cut 220 can be disposed, for example, in the middle of each memory finger 218 to divide a top select gate (TSG) of the memory finger 218 into two portions, and thereby can divide a memory finger into two memory slices 224, where memory cells in a memory slice 224 that share the same word line form a programmable (read/write) memory page. While erase operation of a 3D NAND memory can be carried out

Micron Ex. 1002, p. 34
Micron v. YMTC
IPR2024-00793

at memory block level, read and write operations can be carried out at memory page level. A memory page can be kilobytes (KB) in size. In some embodiments, region 108 also includes dummy memory strings 222 for process variation control during fabrication and/or for additional mechanical support.

[0043] Fig. 3 illustrates a perspective view of a portion of an exemplary three-dimensional (3D) memory array structure 300, according to some embodiments of the present disclosure. The memory array structure 300 includes a substrate 330, an insulating film 331 over the substrate 330, a tier of lower select gates (LSGs) 332 over the insulating film 331, and a plurality of tiers of control gates 333, also referred to as "word lines (WLs)," stacking on top of the LSGs 332 to form a film stack 335 of alternating conductive and dielectric layers. The dielectric layers adjacent to the tiers of control gates are not shown in Fig. 3 for clarity.

[0044] The control gates of each tier are separated by slit structures 216-1 and 216-2 through the film stack 335. The memory array structure 300 also includes a tier of top select gates (TSGs) 334 over the stack of control gates 333. The stack of TSG 334, control gates 333 and LSG 332 is also referred to as "gate electrodes." The memory array structure 300 further includes memory strings 212 and doped source line regions 344 in portions of substrate 330 between adjacent LSGs 332. Each memory strings 212 includes a channel hole 336 extending through the insulating film 331 and the film stack 335 of alternating conductive and dielectric layers. Memory strings 212 also includes a memory film 337 on a sidewall of the channel hole 336, a channel layer 338 over the memory film 337, and a core filling film 339 surrounded by the channel layer 338. A memory cell 340 can be formed at the intersection of the control gate 333 and the memory string 212. The memory array structure 300 further includes a plurality of bit lines (BLs) 341 connected with the memory strings 212 over the TSGs 334. The memory array structure 300 also includes a plurality of metal interconnect lines 343 connected with the gate electrodes through a plurality of contact structures 214. The edge of the film stack 335 is configured in a shape of staircase to allow an electrical connection to each tier of the gate electrodes.

[0045] In Fig. 3, for illustrative purposes, three tiers of control gates 333-1, 333-2, and 333-3 are shown together with one tier of TSG 334 and one tier of LSG 332. In this example, each memory string 212 can include three memory cells 340-1, 340-2 and 340-3, corresponding to the control gates 333-1, 333-2 and 333-3, respectively. In some embodiments, the number of

Micron Ex. 1002, p. 35
Micron v. YMTC
IPR2024-00793

control gates and the number of memory cells can be more than three to increase storage capacity. The memory array structure 300 can also include other structures, for example, TSG cut, common source contact (i.e., array common source) and dummy memory string. These structures are not shown in Fig. 3 for simplicity.

[0046] While floating gate memory cells has been traditionally utilized in flash memories, technology based on charge trapping has demonstrated more scaling ability and higher intrinsic reliability. Three-dimensional NAND using charge trapping technology has been developed for high density storage, where the storage information (*e.g.*, threshold voltage V_{th} of the memory cell) depends on the amount of charge trapped in a storage layer.

[0047] Fig. 4A illustrates a schematic cross-section of a 3D NAND memory 400a, which includes memory cells similar to the memory cell 340 in Fig. 3. The memory cell 340-3 includes a control gate (*e.g.*, the control gate 333), a memory film (*e.g.*, the memory film 337) and a channel layer (*e.g.*, the channel layer 338, also referred to as the channel).

[0048] In a 3D NAND memory, the memory film 337 can be disposed on a sidewall of each channel hole 336 (illustrated in Fig. 3). In some embodiments, the memory film 337 can include a barrier layer 422, a storage layer 424, and a tunneling layer 426. The barrier layer 422 can be used to block the movement of electronic charges 428 between the control gate 333 and the storage layer 424. The barrier layer 422 can include silicon oxide and high dielectric constant (high-k) dielectrics, for example, aluminum oxide. The storage layer 424 can be used to store electronic charges 428 and can include silicon nitride. The storage and/or removal of charges in the storage layer 424 can impact the on/off state and/or a conductance of the channel layer 338. The tunneling layer 426 can be used to control the tunneling of electronic charges 428 (electrons or holes) between the channel layer 338 and the storage layer 424. The tunneling layer 426 can be silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In a 3D NAND memory, the channel layer 338 can be disposed on a sidewall of the memory film 337 in the channel hole 336 (in Fig. 3.) The channel layer 338 can include amorphous silicon, polycrystalline silicon, and/or monocrystalline silicon.

[0049] Fig. 4B shows a schematic circuit diagram of a 3D memory array 400b. As described previously, the 3D memory array 400b includes a plurality of memory strings 212, each memory string 212 having a plurality of stacked memory cells 340. The memory string 212 also includes at least one field effect transistor (*e.g.*, MOSFET) at each end, which is

Micron Ex. 1002, p. 36
Micron v. YMTC
IPR2024-00793

controlled by the lower select gate (LSG) 332 and the top select gate (TSG) 334, respectively. And the two respective transistors are referred to as lower and top select transistors 332-T and 334-T. The stacked memory cells 340 can be controlled by the control gates 333, where the control gates 333 are connected to word lines (not shown) of the 3D memory array 400b. The drain terminal of the top select transistor 334-T can be connected to the bit lines (*e.g.*, the bit line 341-1, 341-2, 341-3, etc.), and the source terminal of the lower select transistor 332-T can be connected to the doped source line region 344 (*see* Fig. 3), from where an array common source (ACS) 446 can be formed. The array common source 446 can be shared by the memory strings 212 in an entire memory block, and is also referred to as the common source line.

[0050] Referring to Figs. 4A and 4B, in a NAND memory, read and write operations can be performed in a memory page, for example memory page 448, which includes memory cells sharing the same word line. In a NAND memory, each memory cell can be in an erased state or a programmed state. Initially, all memory cells in a block can be reset to the erased state as logic "1" by applying, for example, a negative voltage between the control gates 333 and source terminals of the memory cells (*e.g.*, the array common source 446) such that all the electronic charges 428 in the storage layers 424 of the memory cells can be removed. At the erased state, the threshold voltage V_{th} of the memory cells 340 can be reset to the lowest value, and the corresponding current flowing through the memory cells 340 between the source terminal (*e.g.*, the array common source 446) and the drain terminal (*e.g.*, the bit lines 341) can be at the highest level for a given bias on the word lines.

[0051] During programming (*i.e.*, writing), a high positive voltage pulse (*e.g.*, 12V to 18V) can be applied on the control gate 333 such that electronic charges 428 (*e.g.*, electrons) can be injected into the storage layer 424 of the memory cell 340, where the electronic charges 428-1 and 428-2 can be randomly captured by deep and shallow traps, respectively. After programming, the threshold voltage V_{th} of the memory cell 340 can be raised to a higher value than that of the erased state. At a higher threshold voltage V_{th}, the current flowing through the source and drain terminals of the memory cell can be at a reduced level for a given bias on the word lines. By measuring (*i.e.*, reading) the memory cell current, the threshold voltage V_{th} and thereby the state of the memory cell 340 can be determined accordingly.

Micron Ex. 1002, p. 37
Micron v. YMTC
IPR2024-00793

[0052] With multi-level-cell or triple-level-cell technology, each memory cell 340 can have multiple programed states, *i.e.*, multiple values of threshold voltages V_{th}. After every programming pulse, a read-verification operation can be performed to check the state of the memory cell. As such, each memory cell 340 can store multiple bits, leading to significant increase of storage capacity.

[0053] For memory cell 340 in a programmed state, electronic charges 428-1 and 428-2 located within the proximity of control gate 333 can affect threshold voltage V_{th} of the memory cell 340. The electronic charges 428-3 located beyond the electric field from control gate 333, and therefore have little impact on the threshold voltage V_{th} of the memory cell. In addition, electronic charges 428-2 captured by shallow traps in the storage layer 424 can be easily de-trapped, and can thereby cause initial threshold-voltage (V_{th}) shift (IVS) during storage period. This process is also referred to as fast charge loss. For programmed state at higher threshold voltage V_{th}, IVS can be larger due to larger amount of electronic charges injected to the storage layer, which results in larger number of electronic charges 428-2 captured by shallow traps (also referred to as fast charges).

[0054] Due to IVS, the programmed state immediately after writing cannot reflect the target threshold voltage V_{th} of the memory cell 340 in real applications. Applying the fake high threshold voltage V_{th} can cause high bit-error-rate in the memory. Therefore, it is necessary to de-trap and remove fast charges prior to read operation such that the V_{th} distribution profile of each programmed state can be more accurately determined.

[0055] Fig. 5 illustrates a timing diagram of a read-verification operation 500 with a prepare voltage (pre-pulse) applied on a selected word line, according to some embodiments of the present disclosure. The read-verification operation 500 can reduce read disturb for unselected memory strings in a 3D NAND memory. Read disturb can occur when the threshold voltage V_{th} (*i.e.*, the programmed state) of an unselected memory cell is changed or disturbed during read or read-verification of a selected memory cell. In some embodiments, the read-verification operation 500 includes two steps, *i.e.*, a read-prepare step and a sensing step, having duration of $t_{prepare}$ and $t_{sensing}$, respectively. The timing diagram of a selected top select gate (Sel_TSG), unselected top select gates (Unsel_TSG), a selected word line (Sel_WL), unselected word lines (Unsel_WL) and the lower select gate (LSG) are shown in Fig. 5.

Micron Ex. 1002, p. 38
Micron v. YMTC
IPR2024-00793

[0056] The read-verification operation 500 starts with the read-prepare step. The TSG 334 and the LSG 332 of a selected memory string, for example TSG 334-3 and LSG 332-3 of a selected memory string 212-3 in Fig. 4B, can be applied with a top select gate voltage V_{tsg} and a lower select gate voltage V_{lsg}. A corresponding top select transistor 334-T and a lower select transistor 332-T of the selected memory string 212-3 can be switched on. The top and lower select gate voltages V_{tsg} and V_{lsg} can be in a range between 4V to 7V. Accordingly, a current path through the stacked memory cells 340 can be established for the selected memory string 212-3. For example, the current flowing through the selected memory string 212-3 can be detected from the bit line 341-3 and the array common source 446 that are electrically connected with the selected memory string 212-3.

[0057] For the read-verification operation 500, the TSG of unselected memory strings (Unsel-TSG), for example TSG 334-1 of memory string 212-1 in Fig. 4B, can be applied with a first off voltage (V_{off}), for example 0V, to switch off a corresponding top select transistor 334-T. Current path between the unselected memory strings 212-1 and bit lines 341-1 can be disconnected. Therefore, the channel of selected memory string 212-3 and unselected memory strings 212-1 can be electrically isolated.

[0058] It is noted that there is a delay for the voltages to ramp up during the read-prepare step. This delay can be caused by parasitic capacitors and resistors, and is well-known for a person skilled in the art. Although a memory string is selected and used as an example to describe read-verification operation herein, it is noted that a plurality of memory strings, for example, a memory finger can be selected and operated in a similar way.

[0059] Referring again to Figs. 4A, 4B and 5, to verify a target memory cell 340-3 in the selected memory string 212-3, a selected word line (*e.g.*, Sel_WL in Fig. 4B) can be applied with a prepare voltage $V_{prepare}$ (also referred to as pre-pulse), while other word lines not selected (*e.g.*, Unsel_WL in Fig. 4B) can be applied with a pass voltage V_{pass}. The selected word line are electrically connected to the control gate 333 of the target memory cell 340-3. The prepare voltage $V_{prepare}$ can be in a range between 4V to 7V, and the pass voltage V_{pass} can be in a range between 5V to 9V. The pass voltage V_{pass} can be higher than the highest threshold voltage of the programmed states such that the memory cells on the selected memory string 212-3 can be fully switched on. When the prepare voltage $V_{prepare}$ is applied on the selected word line Sel_WL, the target memory cell 340-3 can also be switched on.

Micron Ex. 1002, p. 39
Micron v. YMTC
IPR2024-00793

Therefore, at time t_1, the top and lower select transistors 334-T and 332-T, and all memory cells 340 of the selected memory string 212-3 are switched on. Current flows between the bit line 341-3 and the array common source 446 via the channel layer of the selected memory string 212-3. As current flowing through the channel layer 338 forming a conductive path, de-trapped fast charges 428-2 from the storage layer 424 can be removed through the conductive path. However, fast charge loss can be a slow process, which is shown in the timing diagram of the selected word line (Sel_WL) in Fig. 5.

[0060] In some embodiments, fast charges 428-2 can also be removed by thermal annealing or by implementing soft erase with a low negative voltage on the control gate. However, the read-prepare step generally can take a long time and thus impact the efficiency of the read-verification operation. Therefore, a need exists for a read-verification operation to provide accelerated fast charge loss and shorten read-prepare step.

[0061] In some embodiments, the read-prepare step can reduce read disturb for the unselected memory strings, for example, memory strings 212-1 and 212-2 in Fig. 4B. As described above, the unselected top select gates (Unsel_TSG) for unselected memory strings (e.g., TSG 334-1 of memory string 212-1) can be applied with the first off voltage (V_{off}), *e.g.*, 0V, to switch off the corresponding top select transistors 334-T and disconnect from the bit lines (e.g., bit line 341-1) as depicted in Fig. 4B. In some embodiments, the lower select gates (LSG) of the unselected memory strings (e.g., LSG 332-1) are applied with the lower select gate voltage V_{lsg} such that the lower select transistors 332-T are switched on. By applying the prepare voltage $V_{prepare}$ on the selected word line (Sel_WL), corresponding memory cells (e.g., memory cells 340-1, 340-2, 340-3, etc.) can be switched on if the prepare voltage $V_{prepare}$ is selected to be higher than the threshold voltages of the programmed states of the memory cells. In this example, the channel of the memory cells of the unselected memory strings (*e.g.*, memory cells 340-1) can be electrically connected to the array common source 446 to maintain at a predetermined potential, *e.g.*, ground.

[0062] In an example that the prepare voltage $V_{prepare}$ is not applied on the selected word line (Sel_WL), the memory cells corresponding to the selected word line (*e.g.*, the memory cell 340-1 of memory string 212-1) may not be fully switched on (*e.g.*, a voltage applied on the selected word line is lower than the threshold voltage V_{th} of the memory cell 340-1). Upper memory cells, *i.e.*, memory cells located between the bit line (*e.g.*, bit line 341-1) and the

Micron Ex. 1002, p. 40
Micron v. YMTC
IPR2024-00793

selected word line (Sel_WL) of the unselected memory string (*e.g.*, memory string 212-1), can have floating channels, where the channel layer is not electrically connected to the bit lines 341 or the common array source 446. Channel potential of the upper memory cells of the unselected memory string (e.g., memory string 212-1) can vary randomly. Memory cells with floating channel can suffer charge loss due to an unknown electrical field between the control gate 333 and the channel layer 338 (*see* Fig. 4A). The trapped charges 428 and thereby the threshold voltages V_{th} (*i.e.*, programmed states) of the memory cells can be changed or disturbed, where the change can be significant with the increased number of reading operation. By introducing the read_prepare step prior to the sensing step, as described previously, read disturb on the unselected memory strings can be reduced.

[0063] After the read_prepare step, the voltage bias on the selected word line (Sel_WL) can be reduced from the prepare voltage $V_{prepare}$ to a read voltage V_{read} to sense (*i.e.*, read or measure) the threshold voltage V_{th} of the target memory cell. The read voltage V_{read} can be in a range between 0V to 2V. For the target memory cell programmed with threshold voltage V_{th} lower than the read voltage V_{read}, the target memory cell can be switch on and form a conductive path in the channel layer 338. If the threshold voltage V_{th} is higher than the read voltage V_{read}, the channel of the target memory cell is switched off. The programmed state of the target memory cell can be determined accordingly. It is noted that the transition period from the prepare voltage $V_{prepare}$ to the read voltage V_{read} is a slow process due to parasitic capacitance and resistance as well as slow de-trapping process of fast trap loss. The sensing step can start after the Sel_WL reach the read voltage V_{read}, which increases the overall duration $t_{prepare}$ of read-prepare step.

[0064] Fig. 6 illustrates a read-verification operation 600 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 600 also includes the read-prepare step and the sensing step. During the read-prepare step of the read-verification operation 600, the Sel_TSG and the LSG can be applied with the top and lower select gate voltages V_{tsg} and V_{lsg}, respectively, to switch on the top and lower select transistors 334-T and 332-T (in Fig. 4B), similar to those used in the read-verification operation 500 in Fig. 5. However, unlike the read-verification operation 500, the Unsel_TSG of the read-verification operation 600 is applied with the prepare voltage $V_{prepare}$ during the read-prepare step. Accordingly, the

Micron Ex. 1002, p. 41
Micron v. YMTC
IPR2024-00793

selected and unselected memory strings can all be electrically accessed from the bit line 341 and the array common source 446.

[0065] In some embodiments, during the read-prepare step of the read-verification operation 600, the selected memory cell can be switched off by applying a second off voltage, *e.g.*, 0V on the selected WL (*i.e.*, Sel_WL). The unselected memory cells (*i.e.*, Unsel_WL) can be switched on with the pass voltage V_{pass} after a delay period t_{delay1}. During the delay period t_{delay1}, all select transistors controlled by Sel_TSG, Unsel_TSG and LSG are turned on with applied voltages V_{tsg}, $V_{prepare}$ and V_{lsg} and thus the channel of the memory string 212 can be electrically connected to the bit line 341 and the array common source 446 (shown in Fig. 4B), and can be maintained at a potential adjustable by a voltage of the bit line 341. When the Unsel_WL is applied with the pass voltage V_{pass}, all the unselected memory cells of the selected memory string are switched on. Therefore, the channel of the selected memory cell can be electrically connected to the bit line 341 through upper memory cells and to the array common source 446 through the lower memory cells. The channel of the selected memory cell can thereby be held at a potential adjustable by the voltage of the bit line 341 and the array common source 446.

[0066] In some embodiments, the delay period t_{delay1} is implemented such that the channel of the memory string 212 is not electrically isolated from the bit line 341 or the array common source 446 before Unsel_WL can be ramped up from 0V to the pass voltage V_{pass}. Referring to Fig. 4B and Fig. 6, if the Unsel_WL is applied with the pass voltage V_{pass} before the Sel_TSG reach the top select gate voltage V_{tsg} or Unsel_TSG reach the prepare voltage $V_{prepare}$, the top select transistors are off and upper portion of the channel layer 338 that is located close to the bit line 341 becomes a floating node. More specifically upper memory cells located between the bit line and the selected memory cell can have a floating channel potential. Similarly, if the Unsel_WL is applied with the pass voltage V_{pass} before the LSG ramps up to the lower select gate voltage V_{lsg} to switch on the lower select transistor, lower portion of the channel layer 338 that is located close to the array common source 446 becomes a floating node. More specifically lower memory cells located between the bit line and the selected memory cell can have a floating channel potential. When floating, channel potential of the memory cells can be boosted by the pass voltage V_{pass} of the Unsel_WL through coupled capacitance. The boosted channel potential of the unselected memory cells

Micron Ex. 1002, p. 42
Micron v. YMTC
IPR2024-00793

can influence the channel potential of the neighboring selected memory cell and influence fast charge removing process. By introducing the delay period t_{delay1}, the aforementioned self-boosting effect or read disturb on the selected or unselected memory cell can be avoided.

[0067] In some embodiments, the read-prepare step also includes a delay period t_{delay2}, a duration between ramping up the pass voltage V_{pass} of Unsel_WL and the read voltage V_{read} of the Sel_WL. During the delay period t_{delay2}, the voltage of Sel_WL is kept at 0V while the voltage of Unsel_WL is raised from 0V to the pass voltage V_{pass}. As discussed previously, the pass voltage V_{pass} is applied on the Unsel_WL after the top and lower select transistors are switched on with applied voltages V_{tsg}, $V_{prepare}$ and V_{lsg} on Sel_TSG, Unsel-TSG and LSG, respectively. As such, the selected memory cell is switched off while unselected memory cells are switched on. Referring back to Fig. 4A, while the selected memory cell 340-3 is switched off, the neighboring unselected memory cells 340 are switched on. Between the selected memory cell 340-3 with a 0V gate bias and the neighboring unselected memory cells 340 with a gate bias of the pass voltage V_{pass}, an electric field parallel to the channel can be established accordingly. The electric field between the neighboring selected and unselected word line can also extend into the charge storage layer 424, the tunneling layer 426 and the channel layer 338. The electric field can generate an electric force on the fast charges 428-2 captured in the storage layer 424. The electric force can de-trap the fast charges 428-2 from the shallow traps, pull them towards the neighboring unselected memory cells. The fast charges can then be recombined with charges of opposite sign or be removed through the conductive path established in the channel of the unselected memory cells. As a result, fast charges 428-2 in the storage layer 424 of the selected memory cell 340-3 can be removed through electric field from neighboring unselected memory cells.

[0068] Referring again to Fig. 6, the duration of the read-prepare step of the read-verification operation 600 includes the sum of the delay period t_{delay1} and t_{delay2}. Both t_{delay1} and t_{delay2} can be pre-determined values.

[0069] In some embodiments, after the read-prepare step, the read voltage V_{read} is applied on the Sel_WL to start the sensing step and BL pre-charge. The sensing step has a duration of $t_{sensing}$, which can also be a predetermined value. During the sensing step, a voltage of 0V is applied on the Unsel_TSG, which switches off the unselected top select gates and electrically isolates the channel of selected memory string from the channel of unselected memory

Micron Ex. 1002, p. 43
Micron v. YMTC
IPR2024-00793

strings. Similar to the read-verification operation 500 (in Fig. 5), the ramping-down process from the prepare voltage $V_{prepare}$ to 0V has a delay time, resulting from parasitic resistance and capacitance of the 3D memory structure. To switch on the memory cells, the prepare voltage $V_{prepare}$ can be set higher than the threshold voltage V_{th} of the memory cell. When the voltage of Unsel_TSG ramping down from the prepare voltage $V_{prepare}$ to below V_{th}, the top select transistors of the unselected memory strings are switched off accordingly. The read-verification operation 600 has a duration $t_{prepare2}$ from the beginning of the read-prepare step to the moment that the Unsel_TSG drops to below V_{th}. In the other words, the duration $t_{prepare2}$ is the minimum time requirement for turning off the Unsel_TSG in the read-verification operation 600. The read-verification operation 600 has a duration $t_{prepare1}$ from the beginning of the read-prepare step to the moment that the Unsel_TSG reaches 0V. For read-verification operation 600, duration of the read-prepare step, *i.e.*, $t_{delay1}+t_{delay2}$ is less than $t_{prepare2}$. The sensing step and BL pre-charge start when Unsel_TSG is above V_{th} and the unselected top select transistor is still on. This operation can provide a minimum time used for the read-prepare step, although more power is consumed. The time saved $t_{PROG\text{-}save}$ is a difference between $t_{prepare1}$ and $t_{delay1}+t_{delay2}$.

[0070] Fig. 7 illustrates a read-verification operation 700 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 700 is similar to the read-verification operation 600, except having a duration of the read-prepare step (*i.e.*, $t_{delay1}+t_{delay2}$) equals $t_{prepare2}$, the minimum time requirement for turning off the Unsel_TSG. In the read-verification operation 700, the sensing step and BL pre-charge start when the unselected top select transistors are just turned off. Still, the time saved $t_{PROG\text{-}save}$ can be expressed as the difference between $t_{prepare1}$ and $t_{delay1}+t_{delay2}$, as shown in Fig. 7. This operation can be sped-up, and thus improved, without consuming more power.

[0071] Fig. 8 illustrates a read-verification operation 800 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 800 is similar to the read-verification operation 600, except having a duration of the read-prepare step (*i.e.*, $t_{delay1}+t_{delay2}$) more than $t_{prepare2}$, the minimum time requirement for turning off the Unsel_TSG. In the read-verification operation 800, the sensing step and BL pre-charge start after the unselected top select

Micron Ex. 1002, p. 44
Micron v. YMTC
IPR2024-00793

transistors are turned off. The time saved $t_{PROG\text{-}save}$ can also be expressed as the difference between $t_{prepare1}$ and $t_{delay1}+t_{delay2}$, as shown in Fig. 8. This operation can allow more time for removing fast charges.

[0072] As described above, accelerating fast charge loss in a 3D NAND flash memory can be achieved by applying the prepare voltage $V_{prepare}$ on Unsel_TSG, the pass voltage V_{pass} on the Unsel_WL, and 0V on the Sel-WL at the read-prepare step. The threshold voltage V_{th} of the target memory cell, associated with the Sel_WL, can be stabilized before the sensing step such that the verified storage data can be more reliable.

[0073] In addition, the read-verification operation described above can greatly reduce the time required at the read-prepare step. The fast charges can be removed by electric field generated between Sel_WL and neighboring Unsel_TSG. After fast charge removal, the sensing step starts when the voltage on Sel_WL is switched from 0V to the read voltage V_{read}, without the need to wait for the Unsel-TSG to ramp down from the prepare voltage $V_{prepare}$ to 0V. Therefore, the duration of read-prepare step can be shortened, *i.e.*, $t_{delay1}+t_{delay2} < t_{prepare1}$, where $t_{PROG\text{-}save} = t_{prepare1}-t_{delay1}-t_{delay2}$ is the time saved.

[0074] 3D NAND flash memory with multi-level-cells typically uses an algorithm with incremental step pulses to program the memory cells. After every program pulse, a read-verification operation is performed to check the state of the memory cells. When the memory cell reaches the target state (*i.e.*, target threshold voltage), the program will be stopped. In the meantime, the memory cells not programed to the target state are calculated towards failed bit count (FBC), where the FBC can be executed in parallel to the read-verification operation to save the time of the entire programming cycle. As shown in Figs. 6-8, FBC operation can be performed in parallel with the read-prepare step. In some embodiments, duration of the FBC operation can be shorter than the duration of the read-prepare step, and the FBC operation can be incorporated within the read-prepare step starting at any suitable time. The failed memory cells can be programmed again to the target memory state accordingly.

[0075] In summary, the present disclosure provides a method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, where the method includes removing fast charges of the target memory cell at a read-prepare step and measuring a threshold voltage of the target memory cell at a sensing step. Removing the fast charges of the target memory cell includes applying a prepare voltage ($V_{prepare}$) on an

Micron Ex. 1002, p. 45
Micron v. YMTC
IPR2024-00793

unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).

[0076] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt, for various applications, such specific embodiments, without undue experimentation, and without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0077] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0078] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0079] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

Micron Ex. 1002, p. 46
Micron v. YMTC
IPR2024-00793

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Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Zilong CHEN
Title	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
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Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 26111

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number: 26111

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

✓ 1 **SIGNATURE of Applicant for Patent**

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Simon Shi-Ning Yang		
Title	CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: CHEN *et al.*	Confirmation No.: To Be Assigned
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: To Be Assigned
Application No.: To Be Assigned	Examiner: To Be Assigned
Filing Date: To Be Assigned	Atty. Docket: 4123.0850002

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on the accompanying IDS Form PTO/SB/08a equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. § 1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Form based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart[1] foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office

---

[1] The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

Micron Ex. 1002, p. 50
Micron v. YMTC
IPR2024-00793

Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. The required fee is provided through online credit card payment authorization in the amount of $240.00 in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of $240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

Micron Ex. 1002, p. 51
Micron v. YMTC
IPR2024-00793

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

Micron Ex. 1002, p. 52
Micron v. YMTC
IPR2024-00793

☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

☒ 7. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **FP3** (CN 109390012 A) appears to describe a "method and apparatus for removing electrons from oxide layer surface of floating gate memory," as noted in the attached English-language translation of the abstract.

Document **US4** (2012/0275223 A1) is submitted herewith as the English-language counterpart of document **FP1** (CN 102760490 A).

Document **US3** (10,121,554 B2) is submitted herewith as the English-language counterpart of document **FP2** (CN 108140415 A).

☒ 8. In accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications cited as document **US1-US6** on the attached IDS Form are submitted.

☒ 9. Copies of the **FP1-FP3** documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 16/729,838, filed December 30, 2019 (pending), which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

Micron Ex. 1002, p. 53
Micron v. YMTC
IPR2024-00793

☒ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No. 16/729,838, filed December 30, 2019 (pending) in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No._____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Micron Ex. 1002, p. 54
Micron v. YMTC
IPR2024-00793

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: May 19, 2021

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

Micron Ex. 1002, p. 55
Micron v. YMTC
IPR2024-00793

PTO/SB/08a (07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Zilong CHEN
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0850002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	US- 2012/0275223 A1	11-01-2012	Baek	
	US2	US- 2013/0128667 A1	05-23-2013	Lee et al.	
	US3	US- 2013/0339603 A1	12-19-2013	Zhu et al.	
	US4	US- 2015/0179269 A1	06-25-2015	Lee	
	US5	US- 2019/0333590 A1	10-31-2019	Lee	
	US6	US- 2021/0125674 A1	04-29-2021	Chen et al.	
	US7	US- 9,607,707 B1	03-28-2017	Pang et al.	
	US8	US- 9,704,587 B1	07-11-2017	Park	
	US9	US- 10,121,554 B2	11-06-2018	Harari	
		US-			
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		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]–Number[4]–Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	FP1	CN 102760490 A	10-31-2012	SK HYNIX INC		
	FP2	CN 108140415 A	06-08-2018	SUNRISE MEMORY CORP		
	FP3	CN 109390012 A	02-26-2019	GIGADEVICE SEMICONDUCTOR		✓
	FP4	CN 109979515 A	07-05-2019	YANGTZE MEMORY TECH CO LT		✓

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08b (07-09)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Zilong CHEN
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0850002

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2019/112728, mailed July 22, 2020; 6 pages.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference **P2019TC931**	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. **PCT/CN2019/112728**	International filing date *(day/month/year)* **23 October 2019**	(Earliest) Priority Date *(day/month/year)*
Applicant **YANGTZE MEMORY TECHNOLOGIES CO., LTD.**		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of:

   ☑ the international application in the language in which it was filed.

   ☐ a translation of the international application into ..... which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

   ☑ the text is approved as submitted by the applicant.

   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

   ☑ the text is approved as submitted by the applicant.

   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

   a. the figure of the **drawings** to be published with the abstract is Figure No. 6

   ☑ as suggested by the applicant.

   ☐ as selected by this Authority, because the applicant failed to suggest a figure.

   ☐ as selected by this Authority, because this figure better characterizes the invention.

   b. ☐ none of the figures is to be published with the abstract.

Micron Ex. 1002, p. 58
Micron v. YMTC
IPR2024-00793

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/112728

A. CLASSIFICATION OF SUBJECT MATTER

G11C 16/04(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI;EPODOC;CNPAT;CNKI;IEEE:read,verification,memory,target,three,address,top, dimensional,removing,fast,charge,read, prepare,apply,voltage,unselect,sensing, off,word,line,string,threshold,gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013339603 A1 (ZHU, Feng et al.) 19 December 2013 (2013-12-19) description, paragraphs 0004-0085	1-20
A	US 2013128667 A1 (APLUS FLASH TECHNOLOGY, INC.) 23 May 2013 (2013-05-23) the whole document	1-20
A	US 2015179269 A1 (APLUS FLASH TECHNOLOGY, INC.) 25 June 2015 (2015-06-25) the whole document	1-20
A	CN 109979515 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 05 July 2019 (2019-07-05) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 July 2020	**22 July 2020**

Name and mailing address of the ISA/CN	Authorized officer
National Intellectual Property Administration, PRC **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**LI,Meng**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53961536**

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2019/112728

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2013339603	A1	19 December 2013	WO	2013095667	A1	27 June 2013
				CN	104115231	A	22 October 2014
US	2013128667	A1	23 May 2013	WO	2013075067	A1	23 May 2013
US	2015179269	A1	25 June 2015	WO	2015100434	A2	02 July 2015
CN	109979515	A	05 July 2019		None		

Form PCT/ISA/210 (patent family annex) (January 2015)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
100013
China 10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing

NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	**22 July 2020**
Applicant's or agent's file reference	**FOR FURTHER ACTION** See paragraph 2 below
P2019TC931	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CN2019/112728	**23 October 2019**	

International Patent Classification (IPC) or both national classification and IPC
G11C 16/04(2006.01)i

Applicant
YANGTZE MEMORY TECHNOLOGIES CO., LTD.

1. This opinion contains indications relating to the following items:

- [✓] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [✓] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/	Date of completion of this opinion	Authorized officer
National Intellectual Property Administration, PRC **China 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088**	**17 July 2020**	**LI,Meng**
Facsimile No. **(86—10) 62019451**		Telephone No. **86-(10)-53961536**

Form PCT/ISA/237 (Cover sheet) (January 2015)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2019/112728

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - [✓] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a)).

3. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
   - a. [ ] forming part of the international application as filed:
     - [ ] in the form of an Annex C/ST.25 text file.
     - [ ] on paper or in the form of an image file.
   - b. [ ] furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
   - c. [ ] furnished subsequent to the international filing date for the purposes of international search only:
     - [ ] in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
     - [ ] on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Micron Ex. 1002, p. 62
Micron v. YMTC
IPR2024-00793

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2019/112728

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	None	NO
Inventive step (IS)	Claims	1-20	YES
	Claims	None	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	None	NO

2. Citations and explanations :

[1] 1. The document is cited as follows:

[2] D1: US 20130339603 A1 19 Dec. 2013(19.12.2013)

[3] 2. Novelty and Inventive step

[4] D1 is regarded as being the prior art closest to claim 1 and discloses the following features (see description, paragraphs 0004-0085): in conventional flash memory techniques such as for NAND flash, there are at least two significant constraints which limit cycling capability: intrinsic charge loss/quick charge loss. In an MLC storage scheme, a memory cell has four or more levels of threshold voltage (Vt) distribution for accommodating at least two bits, so RWB is comparatively tight. A flash memory cell may, for example, be programmed by inducing hot electron injection or Fowler-Nordheim tunneling from the channel region to FG 108 through the gate oxide by applying a relatively high control gate voltage and nominal drain voltage. The voltage at control gate 110 determines the amount of charge residing on FG 108 after programming. Control engine 436 may manage access to memory array 422----e.g. via control of X decoder 428, Y decoder 430 and a voltage switch 438. Voltage switch 438 may control various voltage levels necessary to read, program and/or erase data in memory array 422. By way of illustration and not limitation, voltage switch may operate based on one or more of a device power supply Vcc, a ground Vss and a program/erase voltage Vpp for programming or erasing data stored within memory array 422.

[5] The different features between claim 1 and D1 include: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage on an unselected top select gate of an unselected memory string; applying a first off voltage on a selected word line associated with the target memory cell; and applying a pass voltage on an unselected word line; and measuring a threshold voltage of the target memory cell at a sensing step.

[6] Therefore, claim 1 is novel in the sense of PCT Article 33(2).

[7] However, the different features between the solution of claim 1 and the disclosure of D1 are neither known from, nor rendered obviously by, the available prior art. Therefore, claim 1 involves an inventive step in the sense of PCT Article 33(3).

[8] Claims 2-20 are directly or indirectly dependent on claim 1. Therefore, claims 2-20 are novel in the sense of PCT Article 33(2), and involve an inventive step in the sense of PCT Article 33(3).

[9] 3. Industrial Applicability

[10] Claims 1-20 can find industrial applicability in the technical field of memory, and thus meet the requirements of PCT Article 33(4).

Micron Ex. 1002, p. 63
Micron v. YMTC
IPR2024-00793

Espacenet

Bibliographic data: CN109979515 (A) — 2019-07-05

Memory programming method and related device

Inventor(s): LIU HONGTAO; HUANG YING; WEI WENZHE; WANG MING ± (刘红涛, ; 黄莹, ; 魏文喆, ; 王明)

Applicant(s): YANGTZE MEMORY TECH CO LTD ± (长江存储科技有限责任公司)

Classification: **- international:** *G11C16/34*
- cooperative: G11C16/3459 (CN)

Application number: CN201910228457 20190325 Global Dossier

Priority number (s): CN201910228457 20190325

Abstract of CN109979515 (A)

The invention discloses a memory programming method and a related device, wherein the method comprises the following steps of judging whether a storage unit of a memory meets a second preset conditionor not after the storage unit of the memory is programmed to meet the first preset condition; and performing programming again on the memory cells which do not meet the second preset condition. Therefore, the distribution range of the whole programming state is reduced, and the reading window between states is increased, so that all the programming states have better retention characteristics.

Micron Ex. 1002, p. 64
Micron v. YMTC
IPR2024-00793

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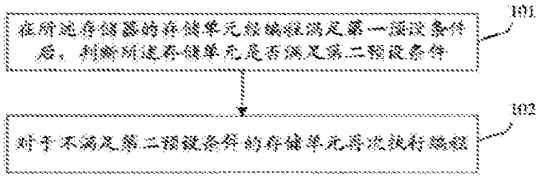
权利要求书1页 说明书6页 附图6页

(54)发明名称

一种存储器编程方法及相关装置

(57)摘要

本发明公开了一种存储器编程方法及相关装置，其中，所述存储器编程方法包括以下步骤：在所述存储器的存储单元经编程满足第一预设条件后，判断所述存储单元是否满足第二预设条件；对于不满足第二预设条件的存储单元再次执行编程。如此，缩小了整个编程态的分布范围，增加了态与态之间的读窗口，使所有编程态具有更好的保持特性。



CN 109979515 A

Micron Ex. 1002, p. 65
Micron v. YMTC
IPR2024-00793

1.一种存储器编程方法，其特征在于，所述方法包括以下步骤：

在所述存储器的存储单元经编程满足第一预设条件后，判断所述存储单元是否满足第二预设条件；

对于不满足第二预设条件的存储单元再次执行编程。

2.根据权利要求1所述的方法，其特征在于，所述第一预设条件为所述存储单元的阈值电压大于等于第一目标阈值；所述第二预设条件为所述存储单元的阈值电压大于等于第二目标阈值；其中，所述第二目标阈值大于等于所述第一目标阈值。

3.根据权利要求1所述的方法，其特征在于，所述存储器编程为步进式脉冲编程(ISPP)，在所述存储器的存储单元经编程满足第一预设条件后，所述方法还包括以下步骤：

在下一脉冲对所述存储单元执行编程抑制；

在所述编程抑制步骤的下一脉冲判断所述存储单元是否满足第二预设条件。

4.根据权利要求1所述的方法，其特征在于，所述方法还包括以下步骤：

在所述再次执行编程的步骤后，对所述存储单元执行编程抑制直至编程结束。

5.根据权利要求1所述的方法，其特征在于，在所述存储单元满足第一预设条件前执行的所述编程过程中，所述存储单元的位线上加载第一预设电压；在对所述不满足第二预设条件的存储单元再次执行编程时，所述存储单元的位线上加载第二预设电压；其中，所述第二预设电压大于所述第一预设电压。

6.一种存储器编程控制装置，其特征在于，所述装置包括：

判断模块，用于在所述存储器的存储单元经编程满足第一预设条件后，判断所述存储单元是否满足第二预设条件；

控制模块，用于对于不满足第二预设条件的存储单元，控制对其再次执行编程。

7.根据权利要求6所述的装置，其特征在于，所述第一预设条件为所述存储单元的阈值电压大于等于第一目标阈值；所述第二预设条件为所述存储单元的阈值电压大于等于第二目标阈值；其中，所述第二目标阈值大于等于所述第一目标阈值。

8.根据权利要求6所述的装置，其特征在于，所述存储器编程为步进式脉冲编程，

所述控制模块，还用于在所述存储器的存储单元经编程满足第一预设条件后，在下一脉冲对所述存储单元执行编程抑制；

所述判断模块，具体用于在所述编程抑制步骤的下一脉冲判断所述存储单元是否满足第二预设条件。

9.根据权利要求6所述的装置，其特征在于，所述控制模块，还用于在所述再次执行编程的步骤后，对所述存储单元执行编程抑制直至编程结束。

10.根据权利要求6所述的装置，其特征在于，所述控制模块，还用于在所述存储单元满足第一预设条件前执行的所述编程过程中，控制所述存储单元的位线上加载第一预设电压；在对所述不满足第二预设条件的存储单元再次执行编程时，控制所述存储单元的位线上加载第二预设电压；其中，所述第二预设电压大于所述第一预设电压。

Micron Ex. 1002, p. 66
Micron v. YMTC
IPR2024-00793

一种存储器编程方法及相关装置

技术领域

[0001] 本发明涉及存储器件技术领域，尤其涉及一种存储器编程方法及相关装置。

背景技术

[0002] 存储器(Memory)是现代信息技术中用于保存信息的记忆设备。作为一种典型的非易失性半导体存储器，已知的NAND(Not-And，与非型)闪存器由于具有较高的存储密度、可控的生产成本、合适的编擦速度及保持特性，已经成为存储市场中的主流产品。

[0003] 在对存储器的各存储单元进行编程后，使各存储单元的阈值电压改变，从而实现信息存储。然而，在实际读取的编程态的分布中发现，总会有一些存储单元在编程后的阈值低于目标阈值，使存储器整体的阈值分布范围变宽。研究发现，出现上述问题的很大一部分原因是编程后的快速电荷泄漏，这主要是由于在编程过程中有一部分电子是存储在隧穿层或者存储层的浅能级，而这部分电子很快就会跑回到沟道中，造成存储单元阈值电压下降。这一过程发生很快，实际产品中情况也较为复杂，但最后的结果基本都是造成整个编程态的分布变宽，最终导致态与态之间的读窗口变小。

[0004] 由此可见，如何缩小编程态的分布范围成为本领域现阶段亟需解决的技术问题之一。

发明内容

[0005] 有鉴于此，本发明的主要目的在于提供一种存储器编程方法及相关装置。

[0006] 为达到上述目的，本发明的技术方案是这样实现的：

[0007] 本发明实施例提供了一种存储器编程方法，所述方法包括以下步骤：

[0008] 在所述存储器的存储单元经编程满足第一预设条件后，判断所述存储单元是否满足第二预设条件；

[0009] 对于不满足第二预设条件的存储单元再次执行编程。

[0010] 上述方案中，所述第一预设条件为所述存储单元的阈值电压大于等于第一目标阈值；所述第二预设条件为所述存储单元的阈值电压大于等于第二目标阈值；其中，所述第二目标阈值大于等于所述第一目标阈值。

[0011] 上述方案中，所述存储器编程为步进式脉冲编程(ISPP)，在所述存储器的存储单元经编程满足第一预设条件后，所述方法还包括以下步骤：

[0012] 在下一脉冲对所述存储单元执行编程抑制；

[0013] 在所述编程抑制步骤的下一脉冲判断所述存储单元是否满足第二预设条件。

[0014] 上述方案中，所述方法还包括以下步骤：

[0015] 在所述再次执行编程的步骤后，对所述存储单元执行编程抑制直至编程结束。

[0016] 上述方案中，在所述存储单元满足第一预设条件前执行的所述编程过程中，所述存储单元的位线上加载第一预设电压；在对所述不满足第二预设条件的存储单元再次执行编程时，所述存储单元的位线上加载第二预设电压；其中，所述第二预设电压大于所述第一

Micron Ex. 1002, p. 67
Micron v. YMTC
IPR2024-00793

预设电压。

[0017] 本发明实施例还提供了一种存储器编程控制装置，所述装置包括：

[0018] 判断模块，用于在所述存储器的存储单元经编程满足第一预设条件后，判断所述存储单元是否满足第二预设条件；

[0019] 控制模块，用于对于不满足第二预设条件的存储单元，控制对其再次执行编程。

[0020] 上述方案中，所述第一预设条件为所述存储单元的阈值电压大于等于第一目标阈值；所述第二预设条件为所述存储单元的阈值电压大于等于第二目标阈值；其中，所述第二目标阈值大于等于所述第一目标阈值。

[0021] 上述方案中，所述存储器编程为步进式脉冲编程，

[0022] 所述控制模块，还用于在所述存储器的存储单元经编程满足第一预设条件后，在下一脉冲对所述存储单元执行编程抑制；

[0023] 所述判断模块，具体用于在所述编程抑制步骤的下一脉冲判断所述存储单元是否满足第二预设条件。

[0024] 上述方案中，所述控制模块，还用于在所述再次执行编程的步骤后，对所述存储单元执行编程抑制直至编程结束。

[0025] 上述方案中，所述控制模块，还用于在所述存储单元满足第一预设条件前执行的所述编程过程中，控制所述存储单元的位线上加载第一预设电压；在对所述不满足第二预设条件的存储单元再次执行编程时，控制所述存储单元的位线上加载第二预设电压；其中，所述第二预设电压大于所述第一预设电压。

[0026] 本发明实施例所提供的存储器编程方法及相关装置，所述存储器编程方法包括以下步骤：在所述存储器的存储单元经编程满足第一预设条件后，判断所述存储单元是否满足第二预设条件；对于不满足第二预设条件的存储单元再次执行编程。如此，缩小了整个编程态的分布范围，增加了态与态之间的读窗口，使所有编程态具有更好的保持特性。

附图说明

[0027] 图1为相关技术中存储器编程方法的流程示意图；

[0028] 图2为相关技术中编程操作期间施加到存储单元上的电压示意图；

[0029] 图3a-3b为相关技术中编程操作期间的时序图；

[0030] 图4为实际存储器某一页中某个编程态在ISPP的多次编程步骤中的阈值电压分布图；

[0031] 图5为本发明实施例提供的存储器编程方法的流程示意图；

[0032] 图6为本发明实施例中再次编程操作期间的时序图；

[0033] 图7为本发明具体示例提供的存储器编程方法的流程示意图；

[0034] 图8为本发明具体示例提供的编程操作期间施加到存储单元上的电压示意图；

[0035] 图9为采用本发明实施例提供的编程方法进行编程的各阶段存储单元的阈值电压分布图；

[0036] 图10为多值存储单元(MLC)采用本发明实施例提供的编程方法与采用相关技术编程方法进行编程的存储单元阈值电压分布对比图；

[0037] 图11为本发明实施例提供的存储器编程控制装置的结构示意图。

Micron Ex. 1002, p. 68
Micron v. YMTC
IPR2024-00793

具体实施方式

[0038] 下面将参照附图更详细地描述本发明公开的示例性实施方式。虽然附图中显示了本发明的示例性实施方式，然而应当理解，可以以各种形式实现本发明，而不应被这里阐述的具体实施方式所限制。相反，提供这些实施方式是为了能够更透彻地理解本发明，并且能够将本发明公开的范围完整的传达给本领域的技术人员。

[0039] 在下文的描述中，给出了大量具体的细节以便提供对本发明更为彻底的理解。然而，对于本领域技术人员而言显而易见的是，本发明可以无需一个或多个这些细节而得以实施。在其他的例子中，为了避免与本发明发生混淆，对于本领域公知的一些技术特征未进行描述；即，这里不描述实际实施例的全部特征，不详细描述公知的功能和结构。

[0040] 为了彻底理解本发明，将在下列的描述中提出详细的步骤以及详细的结构，以便阐释本发明的技术方案。本发明的较佳实施例详细描述如下，然而除了这些详细描述外，本发明还可以具有其他实施方式。

[0041] 图1为相关技术中存储器编程方法的流程示意图；图2为相关技术中编程操作期间施加到存储单元上的电压示意图。如图所示，相关技术中采用步进式脉冲编程(Increment Step Pulse Program，ISPP)进行写操作。对于NAND闪存器而言，写操作是以页为单位进行的；以一个页里面的某个存储单元为例，开始编程后，先在该存储单元上加载一个起始编程电压，然后验证是否编写到目标阈值；如果没有达到目标阈值，再用高一些的电压编写一下；重复以上过程，直到在验证步骤中发现这个存储单元的阈值电压已经被编写达到目标阈值，此时，该存储单元编程完成，在后续时间内该存储单元上施加编程抑制电压，使其不再被编程；当这个页所有存储单元的阈值电压均编写到目标阈值时，整个页的编写过程结束。

[0042] 图3a-3b示出了相关技术中编程操作期间的时序图。如图所示，在编程时，选中的字线上加载编程电压，非选中的字线上加载导通电压，选中单元串的上选择管加载开启电压而打开，从而使选中字线的低电位传导到沟道，如此实现编程操作；当编程抑制时，在该单元串的位线上加载一个编程抑制电压，即从低电位变为高电位，使上选择管关断，沟道浮空，从而对应的选中字线上的存储单元不会再被编程。

[0043] 图4为实际存储器某一页中某个编程态在ISPP的多次编程步骤中的阈值电压分布图。图中各曲线分别表示ISPP中一次编程后各存储单元阈值电压的分布状况，即各阈值电压与具有该阈值电压的存储单元的数目之间的关系。具体地，图中每一曲线的峰值处所对应的阈值电压为最多数量存储单元具有的阈值电压。从图中可以看出，随着编程次数(编程脉冲)增加，存储单元整体阈值电压越来越高；当一部分存储单元达到目标阈值时，这部分存储单元就会被编程抑制；而未达到目标阈值的存储单元继续编程，阈值电压继续升高，最终整个编程态的分布开始压缩变窄(主图中最右侧曲线)，直至所有存储单元的阈值电压超过目标阈值，编程结束。图4中虚线框内子图示出了所有存储单元的阈值电压超过目标阈值后，经过时间变化各存储单元阈值电压的分布状况；从图中可以看出，随着时间延长，一部分存储单元的阈值电压逐渐降低，并低于目标阈值，从而使得整体分布变宽。研究发现，出现上述问题的很大一部分原因是编程后的快速电荷泄漏，这主要是由于在编程过程中有一部分电子是存储在隧穿层或者存储层的浅能级，而这部分电子很快就会跑回到沟道中，造成存储单元阈值电压下降。这一过程发生很快，实际产品中情况也较为复杂，但最后的结果

Micron Ex. 1002, p. 69
Micron v. YMTC
IPR2024-00793

基本都是造成整个编程态的分布变宽，最终导致态与态之间的读窗口变小。

[0044] 基于此，本发明实施例提供了一种存储器编程方法；具体请参见附图5。如图所示，所述方法包括以下步骤：

[0045] 步骤101、在所述存储器的存储单元经编程满足第一预设条件后，判断所述存储单元是否满足第二预设条件；

[0046] 步骤102、对于不满足第二预设条件的存储单元再次执行编程。

[0047] 可以理解地，在存储单元已满足第一预设条件之后，对已编程的存储单元再次进行验证，并对不满足条件的部分存储单元再次编程，从而提高了这一部分存储单元的阈值电压，减小了其与满足第二预设条件的存储单元之间阈值电压的差距，因此缩小了整个编程态的分布范围，增加了态与态之间的读窗口，使所有编程态具有更好的保持特性。

[0048] 在一具体实施例中，所述第一预设条件为所述存储单元的阈值电压大于等于第一目标阈值；所述第二预设条件为所述存储单元的阈值电压大于等于第二目标阈值；其中，所述第二目标阈值大于等于所述第一目标阈值。

[0049] 可以理解地，所述第一预设条件即为所述存储单元经验证表明已被编程；所述第一目标阈值即为存储单元实际需要被编程到的阈值电压位置。以上编程步骤可以采用本领域中常规编程方法实现，这里不予详述。

[0050] 在一可选实施例中，所述第二目标阈值可以等于所述第一目标阈值；即可以采用相同的预设条件，在获知(经判断/验证后得到)存储单元经编程已经满足第一预设条件之后，再进行一次判断/验证，这时距离上一次判断/验证已经经过一定时间，而由于电荷泄露速度很快，此时，已经有一部分存储单元无法满足第一预设条件，针对这部分存储单元再次执行编程，以缩小编程态分布范围。

[0051] 在另一可选实施例中，所述第二目标阈值可以大于所述第一目标阈值，即可以采用要求更高的预设条件，对已经无法满足第一预设条件以及有可能/即将无法满足第一预设条件的存储单元，均执行再次编程，从而为编程态分布变化设置预留量，达到即便有快速的电荷损失带来阈值下降，也不会降到目标阈值以下的技术效果。

[0052] 在一实施例中，所述存储器编程为步进式脉冲编程，在所述存储器的存储单元经编程满足第一预设条件后，所述方法还包括以下步骤：在下一脉冲对所述存储单元执行编程抑制；在所述编程抑制步骤的下一脉冲判断所述存储单元是否满足第二预设条件。

[0053] 可以理解地，本发明实施例优选在存储单元经编程满足第一预设条件后，尽快执行判断与再次编程操作，从而节省编程时长。

[0054] 在一实施例中，所述方法还包括以下步骤：在所述再次执行编程的步骤后，对所述存储单元执行编程抑制直至编程结束。在本实施例中，在再次执行编程的步骤后，不再进行判断/验证，直接执行编程抑制直至整个页的编程结束，从而节省编程时长。

[0055] 可以理解地，对于经判断满足第二预设条件的存储单元，执行编程抑制直至编程结束。

[0056] 在一实施例中，在所述存储单元满足第一预设条件前执行的所述编程过程中，所述存储单元的位线上加载第一预设电压；在对所述不满足第二预设条件的存储单元再次执行编程时，所述存储单元的位线上加载第二预设电压；其中，所述第二预设电压大于所述第一预设电压。

Micron Ex. 1002, p. 70
Micron v. YMTC
IPR2024-00793

[0057] 图6示出了本发明实施例中再次编程操作期间的时序图。在实际应用中，为了配合不满足第二预设条件的存储单元的再次编程操作，还需要对波形电压配置上做修改。在所述存储单元满足第一预设条件前执行的所述编程过程中，即常规ISPP过程中，在所述存储单元的位线上通过加载低电位(第一预设电压)；而由于再次编程的编程电压要高于通过第一预设条件之前的编程电压，为了防止过编程，选中位线在再次编程的时候不能再加载低电位，而需要加载一个大于所述第一预设电压的电压。这个电压可以增加编程单元的沟道电势，减少沟道和栅极(字线)之间的电压差，从而降低编程速度，防止过编程。

[0058] 此外，可以理解地，所述第二预设电压还应当小于编程抑制电压，从而避免产生编程抑制；即所述第二预设电压是介于低电位和编程抑制电压之间的一个电压。

[0059] 下面结合具体示例对本发明再作进一步详细的说明：图7为本发明具体示例提供的存储器编程方法的流程示意图；图8为本发明具体示例提供的编程操作期间施加到存储单元上的电压示意图。

[0060] 结合图7与图8所示，本发明具体示例采用步进式脉冲编程进行写操作。以NAND闪存器某一页里面的某个存储单元为例，开始编程后，先在该存储单元上加载一个起始编程电压，然后执行验证一，判断所述存储单元是否编写到第一目标阈值；如果没有达到第一目标阈值，再用高一些的电压继续编程；重复以上过程，直到在验证一步骤中发现这个存储单元的阈值电压已经被编写达到第一目标阈值；在下一脉冲对所述存储单元执行编程抑制；在所述编程抑制步骤的下一脉冲执行验证二，判断所述存储单元是否编写到第二目标阈值；如果没有达到第二目标阈值，再在下一脉冲用高一些的电压再次编程；接下来，考虑到编程时长，不再进行验证，直接对所述存储单元执行编程抑制直至编程结束；如果验证二中，所述存储单元的阈值电压达到第二目标阈值，则继续编程抑制直至编程结束。

[0061] 图9为采用本发明实施例提供的编程方法进行编程的各阶段存储单元的阈值电压分布图。从图中可以看出，通过验证一时所有存储单元的阈值电压均超过目标阈值，编程态的分布范围较窄；通过验证一时，已经有存储单元的阈值电压发生下降，此时，编程态的分布范围变宽；而在经过再次编程后，一部分存储单元的阈值电压由于再次编程而升高，从而缩小了整个编程态的分布范围。

[0062] 图10为多值存储单元(MLC)采用本发明实施例提供的编程方法与采用相关技术编程方法进行编程的存储单元阈值电压分布对比图。从图中可以看出，采用本发明实施例提供的编程方法进行编程，获得的存储单元阈值电压分布更窄，因此，可以提高存储器的读窗口和保持特性。

[0063] 在本发明的上下文中，所述存储器可以为三维存储器；进一步地，为可以3D NAND闪存器。所述存储器包括但不限于浮栅结构以及电荷俘获结构。此外，本发明各实施例适用于单值存储单元(SLC)、MLC、三位存储单元(TLC)或者更多位存储单元。

[0064] 基于上述方法，并结合图11，本发明实施例还提供了一种存储器编程控制装置10。如图所示，所述装置10包括：

[0065] 判断模块11，用于在所述存储器的存储单元经编程满足第一预设条件后，判断所述存储单元是否满足第二预设条件；

[0066] 控制模块12，用于对于不满足第二预设条件的存储单元，控制对其再次执行编程。

[0067] 在一实施例中，所述第一预设条件为所述存储单元的阈值电压大于等于第一目标

Micron Ex. 1002, p. 71
Micron v. YMTC
IPR2024-00793

阈值；所述第二预设条件为所述存储单元的阈值电压大于等于第二目标阈值；其中，所述第二目标阈值大于等于所述第一目标阈值。

[0068] 在一实施例中，所述存储器编程为步进式脉冲编程，

[0069] 所述控制模块12，还用于在所述存储器的存储单元经编程满足第一预设条件后，在下一脉冲对所述存储单元执行编程抑制；

[0070] 所述判断模块11，具体用于在所述编程抑制步骤的下一脉冲判断所述存储单元是否满足第二预设条件。

[0071] 在一实施例中，所述控制模块12，还用于在所述再次执行编程的步骤后，对所述存储单元执行编程抑制直至编程结束。

[0072] 在一实施例中，所述控制模块12，还用于在所述存储单元满足第一预设条件前执行的所述编程过程中，控制所述存储单元的位线上加载第一预设电压；在对所述不满足第二预设条件的存储单元再次执行编程时，控制所述存储单元的位线上加载第二预设电压；其中，所述第二预设电压大于所述第一预设电压。

[0073] 需要说明的是，本发明提供的存储器编程控制装置实施例与存储器编程方法实施例属于同一构思；各实施例所记载的技术方案中各技术特征之间，在不冲突的情况下，可以任意组合。

[0074] 以上所述，仅为本发明的较佳实施例而已，并非用于限定本发明的保护范围，凡在本发明的精神和原则之内所作的任何修改、等同替换和改进等，均应包含在本发明的保护范围之内。

Micron Ex. 1002, p. 72
Micron v. YMTC
IPR2024-00793

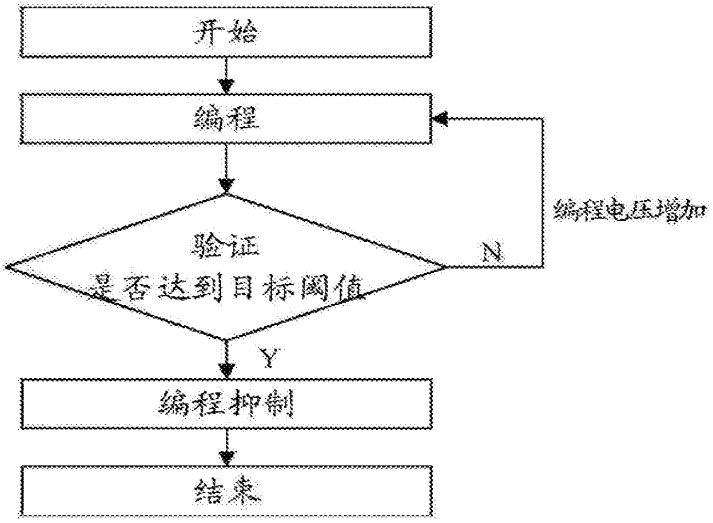


图1

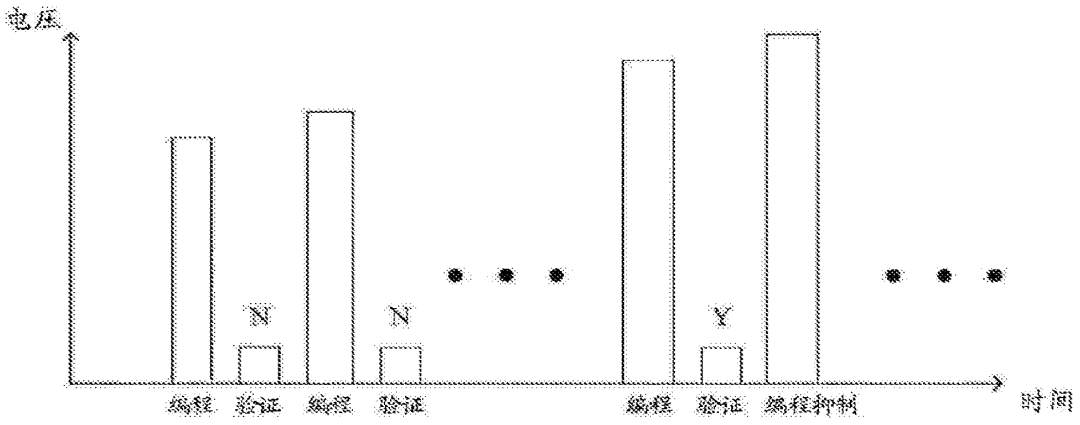


图2

Micron Ex. 1002, p. 73
Micron v. YMTC
IPR2024-00793

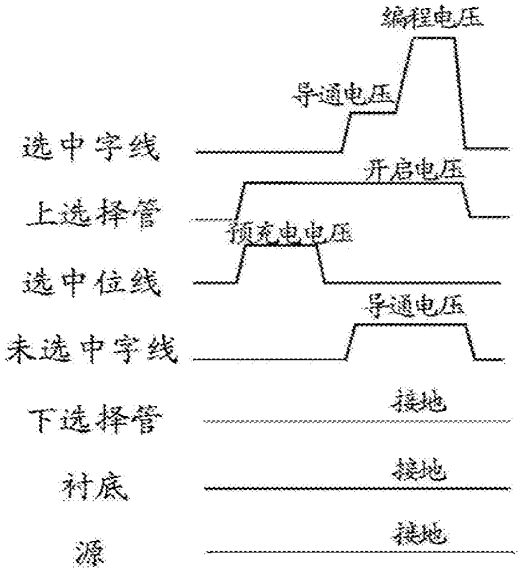


图3a

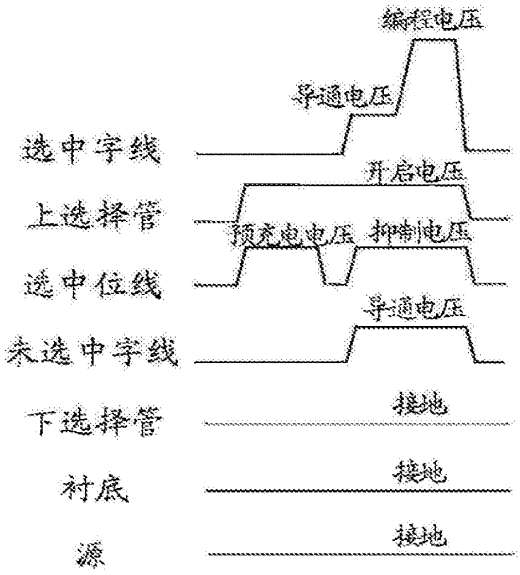


图3b

Micron Ex. 1002, p. 74
Micron v. YMTC
IPR2024-00793

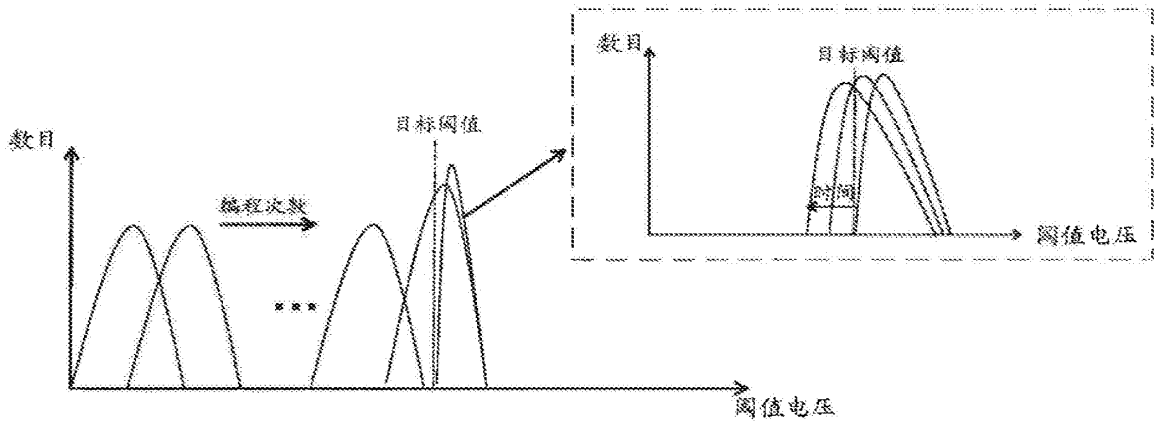


图4

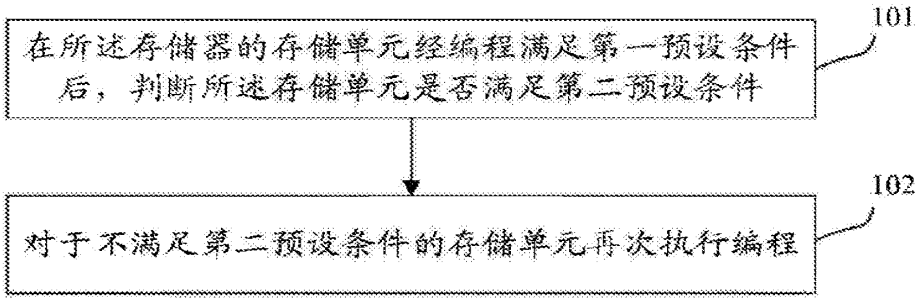


图5

Micron Ex. 1002, p. 75
Micron v. YMTC
IPR2024-00793

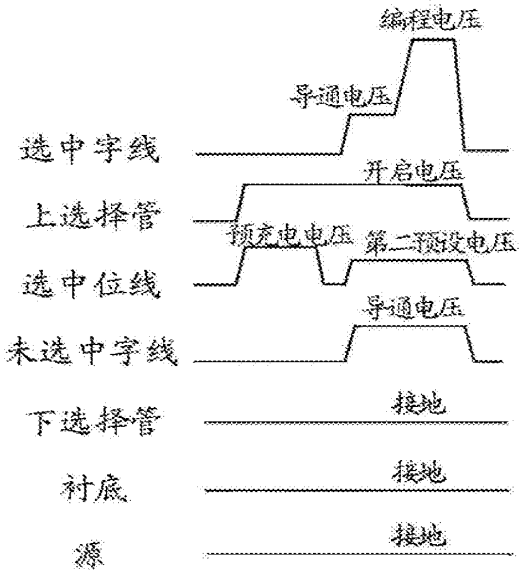


图6

Micron Ex. 1002, p. 76
Micron v. YMTC
IPR2024-00793

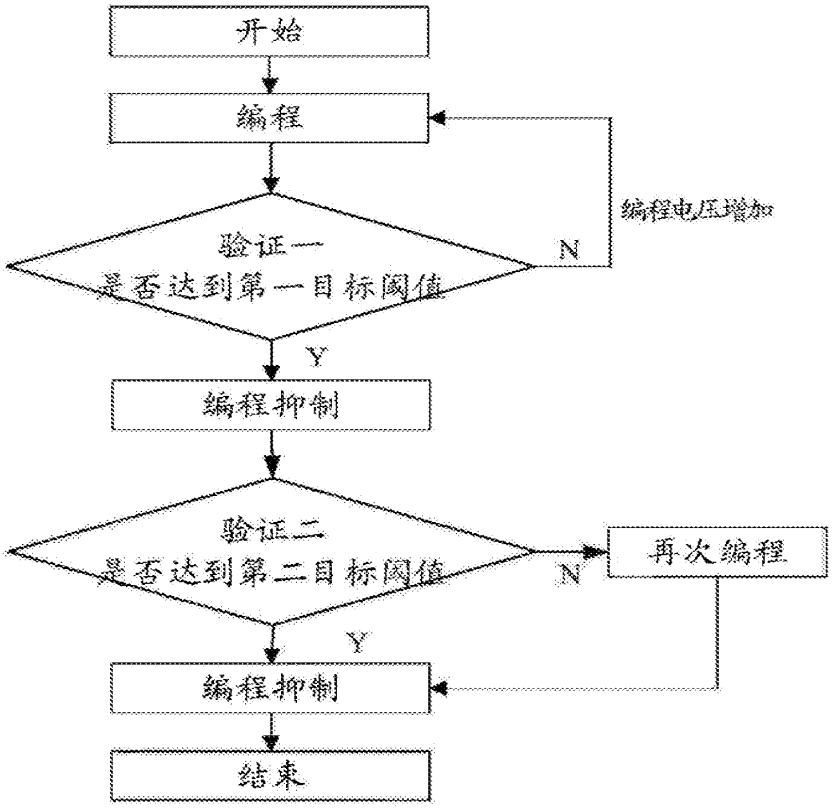


图7

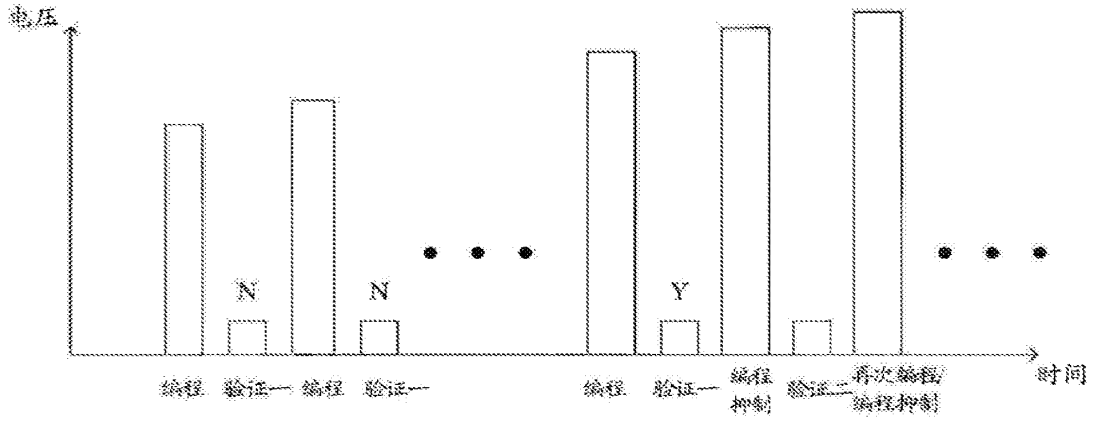


图8

Micron Ex. 1002, p. 77
Micron v. YMTC
IPR2024-00793

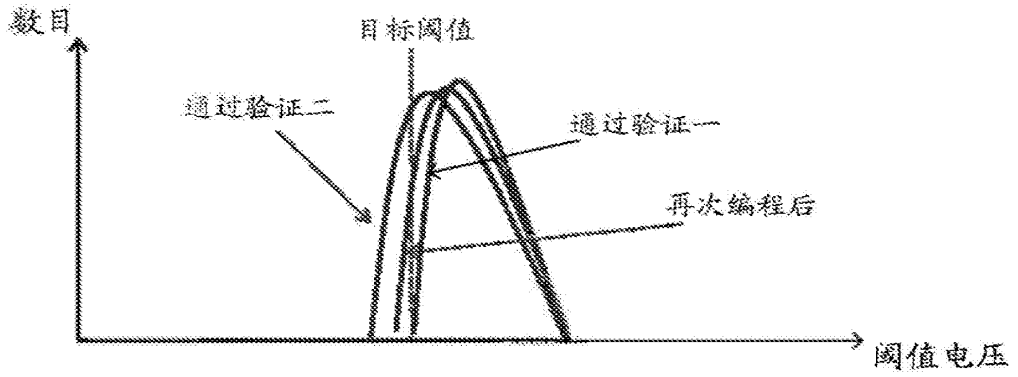


图9

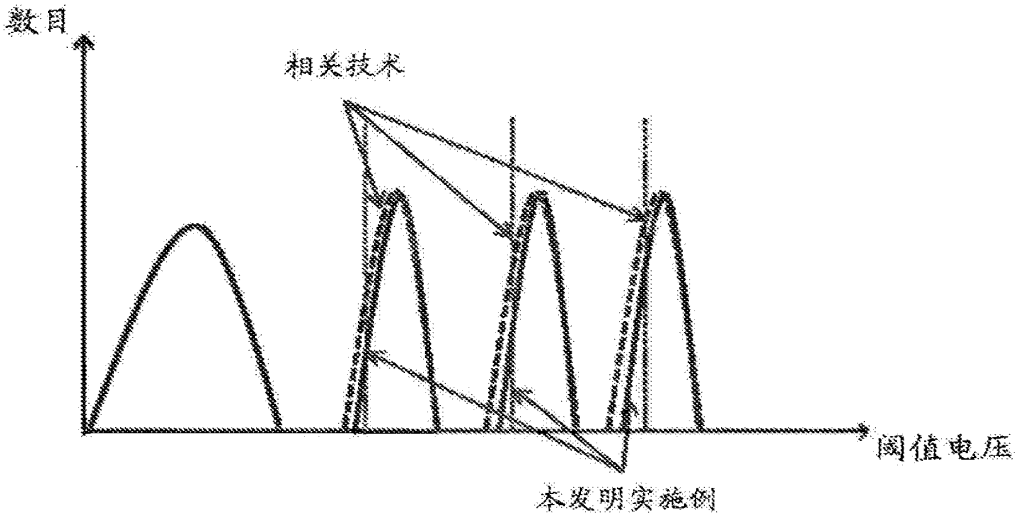


图10

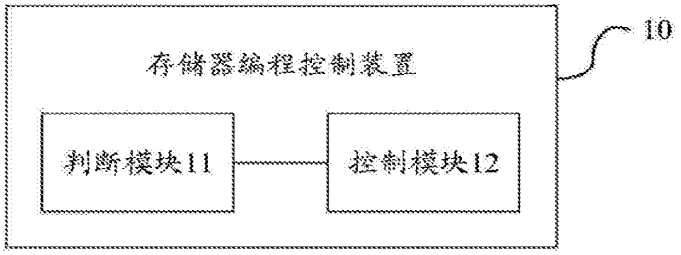


图11

Micron Ex. 1002, p. 78
Micron v. YMTC
IPR2024-00793

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Filer:	Donald J. Featherstone/Julia Vang
Attorney Docket Number:	4123.0850002

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1820**

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Confirmation Number:	8686
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First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Donald J. Featherstone/Julia Vang
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Application Type:	Utility under 35 USC 111(a)

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Payment Type	CARD
Payment was successfully received in RAM	$1820
RAM confirmation Number	E20215IH20340027
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2021-05-21-Cover-Letter-4123-0850002.pdf	288493 0aa108e04aa96396a3aa87d3379a042ca1b29e24	no	2
Warnings:					
Information:					
2	Transmittal of New Application	2021-05-19-Utility-Transmittal-4123-0850002.PDF	362568 878fe6a49cc47f6d841926a927939cb8d0fbdec4	no	1
Warnings:					
Information:					
3	Application Data Sheet	2021-05-19-ADS-4123-0850002.PDF	1256346 1ea217740114533eea8ac15fc4cb6f8c3f12811c	no	8
Warnings:					
Information:					
4	Oath or Declaration filed	2021-05-19-Declaration-Assignment-4123-0850002.PDF	124384 21efce808c5b235197ba2fa1bf0ac08e5a4a8805	no	4
Warnings:					
Information:					
5		2021-05-19-Utility-Application-4123-0850002.PDF	394120 afe926a00b7c6430c1295f36e42ee4f96a627ab9	yes	33

Multipart Description/PDF files in .zip description

Document Description	Start	End
Drawings-only black and white line drawings	26	33
Abstract	25	25
Claims	21	24

	Specification		1	20	
Warnings:					
Information:					
6	Power of Attorney	2021-05-19-POA-4123-0850002.pdf	1420676 c9b63859da6c4d3d23071049a13efc7e358afe4e	no	2
Warnings:					
Information:					
7	Transmittal Letter	2021-05-19-IDS-Pleading-4123-0850002.pdf	173697 18e82c4cd456153a68f5f57b68f68c172dbd26c7	no	7
Warnings:					
Information:					
8	Information Disclosure Statement (IDS) Form (SB08)	2021-05-19-sIDS1-SB08a-4123-0850002.pdf	154749 0dbc8928589f4ae40b15ad2641ff71ddffa2f783	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
9	Information Disclosure Statement (IDS) Form (SB08)	2021-05-19-sIDS1-SB08b-4123-0850002.pdf	196952 1b3dcee31d1176b62c87004e73bd1fb8c9ac6dd0	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
10	Non Patent Literature	NPL1_ISRWO.PDF	119011 5e1b4f12a25317838cdb4f71ff3b20dfc2c910d1	no	6
Warnings:					
Information:					
11	Foreign Reference	FP4_CN109979515A.PDF	495239 4abd7872daa440ab5ff2b0001b1114c80d25fc5a	no	15
Warnings:					
Information:					

12	Fee Worksheet (SB06)	fee-info.pdf	34851 4353df7f4459bfc4cb5f131be986c5337b299e7c	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	5021086	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
202-772-8629
DONF@STERNEKESSLER.COM

May 19, 2021

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Patent Application under 37 C.F.R. § 1.53(b)
(*Continuation of Appl. No. 16/729,838; Filed: December 30, 2019*)
Appl. No. *To Be Assigned*; Filed: *Herewith*
For: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**
First Named Inventor: Zilong CHEN
Our Ref: 4123.0850002

Commissioner:

The following documents are transmitted herewith under 37 C.F.R. § 1.53(b) for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/AIA/15);

2. Payment made electronically for $1,820.00 to cover:

   $1,820.00 – Patent Application fee (including basic filing, search, and examination fees);

3. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);

4. U.S. Utility Patent Application entitled:

   METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

   and naming as Inventors: Zilong CHEN; Xiang FU

   the application consisting of:

   a. An Application Data Sheet (37 C.F.R. § 1.76);

Micron Ex. 1002, p. 85
Micron v. YMTC
IPR2024-00793

b. A copy of the signed Inventors Declaration, as originally filed in prior U.S. Appl. No. *16/729,838*;

c. A specification containing 25 total pages:

i. 20 pages of description prior to any claims;

ii. 4 pages (20 claims);

iii. a one page abstract;

d. 8 sheets of drawings: (Figures 1-8);

5. An executed Power of Attorney by Applicant (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A);

6. An Information Disclosure Statement (IDS);

7. Form PTO/SB/08a (1 sheet) listing 13 documents (US1-US9 and FP1-FP4);

8. Form PTO/SB/08b (1 sheet) listing 1 document (**NPL1**); and

9. Copies of cited documents (**FP4**) and (**NPL1**).

The above-listed documents are filed electronically.

Correspondence should be sent to Customer Number 26111.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/jcv
Enclosure(s)

Micron Ex. 1002, p. 86
Micron v. YMTC
IPR2024-00793

DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 17324877 Document Date: 05/19/2021

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

At the time of document entry (noted above):

- USPTO employees may access SCORE content via DAV or via the SCORE web page.
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Form Revision Date: March 1, 2019

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6727719

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ZILONG CHEN	03/09/2020
XIANG FU	03/09/2020

RECEIVING PARTY DATA

Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	NO. 88 WEILAI 3RD ROAD, EAST LAKE HIGH-TECH DEVELOPMENT ZONE
City:	WUHAN, HUBEI
State/Country:	CHINA

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	17324877

CORRESPONDENCE DATA

Fax Number: (202)371-2540

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 2023712600
Email: jvang@sternekessler.com
Correspondent Name: STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
Address Line 1: 1100 NEW YORK AVENUE, NW
Address Line 4: WASHINGTON, D.C. 20005

ATTORNEY DOCKET NUMBER:	4123.0850002
NAME OF SUBMITTER:	DONALD J. FEATHERSTONE REG.NO. 33,876
SIGNATURE:	/Donald J. Featherstone/
DATE SIGNED:	05/25/2021
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 4
source=Declaration-Assignment-4123-0850002#page1.tif
source=Declaration-Assignment-4123-0850002#page2.tif
source=Declaration-Assignment-4123-0850002#page3.tif
source=Declaration-Assignment-4123-0850002#page4.tif

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/729,838

filed on December 30, 2019

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is No. 88 Weilai 3rd Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**, for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

Micron Ex. 1002, p. 89
Micron v. YMTC
IPR2024-00793

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

2031285-011E549>-10. 218. 20. 65
32766-09/03/2020 10:28

Micron Ex. 1002, p. 90
Micron v. YMTC
IPR2024-00793

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Zilong CHEN** Date: 2020-03-09

Signature of Inventor: Zilong CHEN

LEGAL NAME OF INVENTOR

Inventor: **Xiang FU** Date: 2020-03-09

Signature of Inventor: Xiang Fu

2034285-011E549-10.218.20.65
32766-09/03/2020 10:28

Micron Ex. 1002, p. 91
Micron v. YMTC
IPR2024-00793

SCHEDULE A

UNITED STATES PATENTS, UNITED STATES PATENT APPLICATIONS AND INTERNATIONAL APPLICATIONS THAT DESIGNATE THE UNITED STATES

Application No.	Filing Date	Patent No.	Issue Date
PCT/CN2019/112728	October 23, 2019		

OTHER INTERNATIONAL APPLICATIONS AND PATENTS

Country	Application No.	Filing Date

2034285-011E5AA?-10.218.20.65
32766-09/03/2020 10:55

Micron Ex. 1002, p. 92
Micron v. YMTC
IPR2024-00793

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/324,877

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/324,877	05/19/2021	2827	1820	4123.0850002	20	2

CONFIRMATION NO. 8686

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT

OC000000125893680

Date Mailed: 05/27/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Zilong CHEN, Wuhan, CHINA;
Xiang FU, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA;

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of 16/729,838 12/30/2019
which is a CON of PCT/CN2019/112728 10/23/2019

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Micron Ex. 1002, p. 94
Micron v. YMTC
IPR2024-00793

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/26/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/324,877**

Projected Publication Date: 09/02/2021

Non-Publication Request: No

Early Publication Request: No

Title

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

Micron Ex. 1002, p. 95
Micron v. YMTC
IPR2024-00793

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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Micron Ex. 1002, p. 96
Micron v. YMTC
IPR2024-00793

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Micron Ex. 1002, p. 97
Micron v. YMTC
IPR2024-00793

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/324,877	05/19/2021	Zilong CHEN	4123.0850002

CONFIRMATION NO. 8686

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

PUBLICATION NOTICE

OC000000128161285

Title:METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Publication No.US-2021-0272637-A1
Publication Date:09/02/2021

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Micron Ex. 1002, p. 98
Micron v. YMTC
IPR2024-00793

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Sheet 1 of 1

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U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	FP5	CN 109584938 A	04-05-2019	YANGTZE MEMORY TECH CO LT		✓

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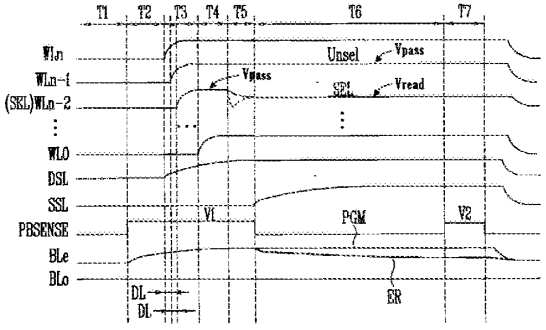
权利要求书 3 页 说明书 12 页 附图 4 页

(54)发明名称

用于对非易失性存储设备执行读取操作的方法

(57)摘要

在一种用于对非易失性存储设备执行读取操作的方法中，对选择的位线预充电。向所有字线顺序地施加通过电压。被施加到从所有字线中选择的字线的通过电压被改变为读取电压。读取电压被施加到所选择的字线。读取被耦合到所选字线的存储单元的数据。



CN 101866694 A

Micron Ex. 1002, p. 100
Micron v. YMTC
IPR2024-00793

1. 一种用于对非易失性存储设备执行读取操作的方法，所述方法包括：

对选择的位线预充电；

向所有字线顺序地施加通过电压；

把向在所有字线当中选择的字线施加的所述通过电压改变为读取电压；

向所选择的字线施加所述读取电压；以及

读取被耦合到所选择的字线的存储单元的数据。

2. 如权利要求 1 所述的方法，进一步包括：

在向所选择的字线施加所述读取电压之前把所选择的字线放电。

3. 如权利要求 1 所述的方法，其中向所有字线施加通过电压包括从邻近于漏选线的字线到邻近于源选线的字线向字线顺序地施加所述通过电压。

4. 如权利要求 3 所述的方法，其中以 10ns 到 10000ns 的延迟时间向所有字线顺序地施加所述通过电压。

5. 如权利要求 1 所述的方法，其中所有字线被分为均包括一条或更多条字线的各个组，并且所述通过电压被施加到每个组。

6. 如权利要求 1 所述的方法，其中读取存储单元的数据进一步包括：

估算所选择的存储单元的阈值电压的变动；以及

感测被耦合到所选择的存储单元的所选位线的电压的变化。

7. 如权利要求 1 所述的方法，进一步包括：

当向所有字线施加所述通过电压时导通漏选晶体管和源选晶体管；及

当把施加到所选择的字线的通过电压改变为所述读取电压并且向所选择的字线施加所述读取电压时，关断所述源选晶体管。

8. 如权利要求 7 所述的方法，进一步包括：

在读取所述存储单元的数据之前，当所选择的字线的电压电平达到读取电压电平时，再次导通所述源选晶体管。

9. 一种用于对非易失性存储设备执行读取操作的方法，所述方法包括：

对选择的位线预充电；

向所有字线顺序地施加通过电压并且同时向所选择的字线施加读取电压；以及

读取被耦合到所选择的字线的存储单元的数据。

10. 如权利要求 9 所述的方法，其中向所有字线施加通过电压包括从邻近于漏选线的字线到邻近于源选线的字线向字线顺序地施加所述通过电压。

11. 如权利要求 10 所述的方法，其中以 10ns 到 10000ns 的延迟时间向所有字线顺序地施加所述通过电压。

12. 如权利要求 9 所述的方法，其中所有字线被分为均包括一条或更多条字线的各个组，并且所述通过电压被施加到每个组。

13. 如权利要求 9 所述的方法，其中读取存储单元的数据进一步包括：

估算所选择的存储单元的阈值电压的变动；以及

感测被耦合到所选择的存储单元的所选位线的电压的变化。

14. 一种用于对非易失性存储设备执行读取操作的方法，所述方法包括：

形成多个字线组，每个字线组都包括一条或更多条字线；

Micron Ex. 1002, p. 101
Micron v. YMTC
IPR2024-00793

向所有字线组的所有字线顺序地施加通过电压；

把向在所有字线当中选择的字线施加的通过电压改变为读取电压；

向所选择的字线施加所述读取电压；以及

读取被耦合到所选择的字线的存储单元的数据。

15. 如权利要求 14 所述的方法，进一步包括：

在向所选择的字线施加所述读取电压之前把所选择的字线放电。

16. 如权利要求 14 所述的方法，其中向所有字线施加通过电压包括依照从漏选线到源选线的字线组的次序向所有字线施加所述通过电压。

17. 如权利要求 14 所述的方法，其中以 10ns 到 10000ns 的延迟时间向所有字线顺序地施加所述通过电压。

18. 如权利要求 14 所述的方法，其中读取存储单元的数据还包括：

估算所选择的存储单元的阈值电压的变动；以及

感测被耦合到所选择的存储单元的所选位线的电压的变化。

19. 一种用于对非易失性存储设备执行读取操作的方法，所述方法包括：

形成多个字线组，每个字线组都包括多条字线；

向所有字线组的所有字线顺序地施加通过电压并且同时向所选择的字线施加读取电压；以及

读取被耦合到所选择的字线的存储单元的数据。

20. 如权利要求 19 所述的方法，其中向所有字线施加通过电压包括依照从漏选线到源选线的字线组的次序向所有字线施加所述通过电压。

21. 如权利要求 19 所述的方法，其中以 10ns 到 10000ns 的延迟时间向所有字线顺序地施加所述通过电压。

22. 如权利要求 19 所述的方法，其中读取存储单元的数据还包括：

估算所选择的存储单元的阈值电压的变动；以及

感测被耦合到所选择的存储单元的所选位线的电压的变化。

23. 一种用于对非易失性存储设备执行读取操作的方法，所述方法包括：

同时向所有字线施加通过电压；

对选择的位线预充电；

把向在所有字线当中选择的字线施加的所述通过电压改变为读取电压；

向所选择的字线施加所述读取电压；以及

读取被耦合到所选择的字线的存储单元的数据。

24. 如权利要求 23 所述的方法，进一步包括：

当向所有字线施加所述通过电压时导通漏选晶体管和源选晶体管；及

当把向所选择的字线施加的所述通过电压改变为所述读取电压并且向所选择的字线施加所述读取电压时，关断所述源选晶体管。

25. 如权利要求 23 所述的方法，其中当施加所述通过电压时，所述漏选晶体管和所述源选晶体管均导通。

26. 如权利要求 23 所述的方法，进一步包括：

在读取所述存储单元的数据之前，当所选择的字线的电压电平达到读取电压电平时，

Micron Ex. 1002, p. 102
Micron v. YMTC
IPR2024-00793

再次导通所述源选晶体管。

27. 如权利要求 23 所述的方法，进一步包括：

在向所选择的字线施加所述读取电压之前把所选择的字线放电。

28. 如权利要求 23 所述的方法，其中读取所述存储单元的数据进一步包括：

估算所选择的存储单元的阈值电压的变动；以及

感测被耦合到所选择的存储单元的所选位线的电压的变化。

29. 一种用于对非易失性存储设备执行读取操作的方法，所述方法包括：

向所选择的字线施加读取电压并且同时向其余的字线施加通过电压；

对选择的位线预充电；以及

读取被耦合到所选择的字线的存储单元的数据。

30. 如权利要求 29 所述的方法，其中当施加所述读取电压或通过电压时，漏选晶体管和源选晶体管均导通。

31. 如权利要求 30 所述的方法，进一步包括通过向字线施加所述读取电压或通过电压来把选择的串的沟道电耦合到字线，然后关断所述源选晶体管。

32. 如权利要求 29 所述的方法，其中读取存储单元的数据还包括：

估算所选择的存储单元的阈值电压的变动；以及

感测被耦合到所选择的存储单元的所选位线的电压的变化。

Micron Ex. 1002, p. 103
Micron v. YMTC
IPR2024-00793

用于对非易失性存储设备执行读取操作的方法

[0001] 相关申请的交叉引用

[0002] 本申请要求 2009 年 4 月 14 日提交的韩国专利申请序列号 10-2009-0032250 的优先权，将其全部内容通过引用并入本文中。

技术领域

[0003] 本发明涉及一种用于对非易失性存储设备执行读取操作的方法，并且尤其涉及一种能够改进读取操作的可靠性的、用于对非易失性存储设备执行读取操作的方法。

背景技术

[0004] 在非易失性存储设备的读取操作中，可以通过向被电耦合到选择的串的位线施加预充电电压、向被电耦合到选择的存储单元的字线施加读取电压并且感测预充电位线的电压电平的变化，来读取数据。

[0005] 图 1 是用于图示已知的非易失性存储设备的问题的剖视图。

[0006] 参照图 1，非易失性存储设备包括在半导体衬底 10 上形成的多条字线 WL0 到 WLn（其中 n 是自然数）。多条字线 WL0 到 WLn 被形成在源选线 SSL 和漏选线 DSL 之间。多条字线 WL0 到 WLn、源选线 SSL 和漏选线 DSL 中的每条都具有这样的结构，在该结构中，在半导体衬底 10 上形成栅绝缘层 12、浮置栅 14、电介质层 16 和控制栅 18。在于源选线 SSL 和漏选线 DSL 中形成的电介质层 16 的每个的一部分中形成接触孔，由此把浮置栅 14 和控制栅 18 电耦合。此外，在源选线 SSL 与多条字线 WL0 到 WLn 之间、在多条字线 WL0 到 WLn 之间以及在多条字线 WL0 到 WLn 与漏选线 DSL 之间的半导体衬底 10 中形成结区 10a。

[0007] 作为一个例子，描述了关于被耦合到字线中的第三字线 WL2 的存储单元的读取操作。

[0008] 在非易失性存储设备的读取操作中，如上所述，向被电耦合到要读取的存储单元的位线施加预充电电压。向被电耦合到未选择的存储单元的字线 WL1 到 WLn 施加通过电压，并且向被电耦合到选择的存储单元的第三字线 WL2 施加读取电压。

[0009] 如果所选存储单元是编程的单元并且被施加到所选择的第三字线 WL2 的读取电压电平低于编程的单元的阈值电压，那么在所选存储单元下面没有形成沟道。在这种情况下，在向源选线 SSL 施加导通电压之前，被电耦合到源选线 SSL 的源选晶体管保持在关断状态。据此，在源选晶体管下面也没有形成沟道。如上所述，如果源选晶体管和所选存储单元都处于关断状态，那么可能出现在关断区域之间电压电平上升的沟道升压现象。参照图 1，在源选线 SSL 和第三字线 WL2 之间的半导体衬底 10 中可能出现沟道升压。然而，在朝着漏选线 DSL 的半导体衬底 10 中不出现沟道升压。这是因为向漏选线 DSL 施加导通电压，以便把位线 BL 的电压转送到有源区。

[0010] 如上所述，如果其中出现沟道升压的区域和其中没有出现沟道升压的区域存在于相同的串中，那么可能在其中出现沟道升压的区域和其中没有出现沟道升压的区域之间形成高电场，因此可能产生热电子‘e’。特别地是，由于热电子‘e’可能渗透到朝着源选线 SSL

Micron Ex. 1002, p. 104
Micron v. YMTC
IPR2024-00793

的方向靠近所选存储单元的存储单元中，因此存储单元的阈值电压分布可能会变动。即，由于热电子‘e’的渗入，所以可能对被耦合到第二字线 WL1 的存储单元执行不想要的软编程操作。

[0011] 如果如上所述阈值电压变动，那么不仅可能改变存储单元的数据，而且可能增加存储单元的阈值电压分布的宽度，这可能会降低特别是多级单元 (MLC) 的可靠性。

发明内容

[0012] 依照一个或多个实施例，在读取操作期间，可以抑制出现沟道升压。据此，可以防止出现热电子，并且可以防止源于所产生的热电子的存储单元的阈值电压分布的变动。

[0013] 在依照第一实施例的用于对非易失性存储设备执行读取操作的方法中，向所有字线顺序地施加通过电压。被施加到在所有字线当中选择的字线的通过电压被改变为读取电压。读取电压被施加到所选择的字线。读取被耦合到所选择字线的存储单元的数据。

[0014] 在依照第二实施例的用于对非易失性存储设备执行读取操作的方法中，对选择的位线预充电。通过电压被顺序施加到所有字线，并且同时，读取电压被施加到选择的字线。读取被耦合到所选字线的存储单元的数据。

[0015] 在包括存储单元的存储块中，在向所有字线顺序地施加通过电压之后，读取电压被施加到所选择的字线。

[0016] 把通过电压改变为读取电压并且向选择的字线施加读取电压包括对已经施加了通过电压的所选字线进行放电并且向所选字线施加读取电压。

[0017] 向所有字线施加通过电压包括从邻近于漏选线的字线到邻近于源选线向字线顺序地施加通过电压。

[0018] 以 10ns 到 10000ns 的延迟时间向所有字线顺序地施加通过电压。

[0019] 所有字线被分成各个组，每个组包括一条或更多条字线，并且通过电压被施加到每个组。

[0020] 在依照第三实施例的用于对非易失性存储设备执行读取操作的方法中，形成均包括一条或多条字线的多个字线组。通过电压被顺序地施加到所有字线组的所有字线。被施加到在所有字线当中选择的字线的通过电压被改变为读取电压，并且向选择的字线施加读取电压。读取被耦合到所选择字线的存储单元的数据。

[0021] 在依照第四实施例的用于对非易失性存储设备执行读取操作的方法中，形成均包括多条字线的多个字线组。通过电压被顺序施加到所有字线组的所有字线，并且同时，读取电压被施加到所选择的字线。读取被耦合到所选择字线的存储单元的数据。

[0022] 把通过电压改变为读取电压并且向选择的字线施加读取电压包括对已经施加了通过电压的所选字线进行放电并且向所选字线施加读取电压。

[0023] 向所有字线施加通过电压包括依照从漏选线到源选线的字线组的次序向所有字线施加通过电压。

[0024] 以 10ns 到 10000ns 的延迟时间向所有字线顺序地施加通过电压。

[0025] 在依照第五实施例的用于对非易失性存储设备执行读取操作的方法中，对选择的位线预充电。在对选择的位线预充电之后，同时向所有字线施加通过电压。被施加到从所有字线中选择的字线的通过电压被改变为读取电压，并且向选择的字线施加读取电压。读

Micron Ex. 1002, p. 105
Micron v. YMTC
IPR2024-00793

取被耦合到所选择字线的存储单元的数据。

[0026] 在依照第六实施例的用于对非易失性存储设备执行读取操作的方法中，向所有字线同时施加通过电压。对选择的位线预充电。被施加到在所有字线当中选择的字线的通过电压被改变为读取电压，并且向选择的字线施加读取电压。读取被耦合到所选择字线的存储单元的数据。

[0027] 当向所有字线施加通过电压时，漏选晶体管和源选晶体管均导通。当把施加到选择的字线的通过电压改变为读取电压并且向选择的字线施加读取电压时，关断源选晶体管。

[0028] 当施加通过电压时，漏选晶体管和源选晶体管均导通。

[0029] 把通过电压改变为读取电压并且向选择的字线施加读取电压包括：在读取存储单元的数据之前关断源选晶体管，当选择的字线的电压电平达到读取电压电平时再次导通源选晶体管。

[0030] 把通过电压改变为读取电压并且向选择的字线施加读取电压包括对已经施加了通过电压的所选字线进行放电继而向所选字线施加读取电压。

[0031] 在依照第七实施例的用于对非易失性存储设备执行读取操作的方法中，读取电压被施加到选择的字线，并且同时，通过电压被施加到其余字线。对选择的位线预充电。读取被耦合到所选择字线的存储单元的数据。

[0032] 当施加读取电压或通过电压时，漏选晶体管和源选晶体管均导通。

[0033] 在所述方法中，通过向字线施加读取电压或通过电压来把选择的串的沟道电耦合到字线，然后关断源选晶体管。

[0034] 读取存储单元的数据包括估算所选存储单元的阈值电压的变动并继而感测被耦合到所选存储单元的所选位线的电压变化。

附图说明

[0035] 图 1 是用于图示已知的非易失性存储设备的问题的剖视图；

[0036] 图 2 是非易失性存储设备的电路图；

[0037] 图 3 是用于图示依照第一实施例的用于对非易失性存储设备执行读取操作的方法的时序图；

[0038] 图 4 是用于图示依照第二实施例的用于对非易失性存储设备执行读取操作的方法的时序图；

[0039] 图 5 是用于图示依照第三实施例的用于对非易失性存储设备执行读取操作的方法的时序图；

[0040] 图 6 是用于图示依照第四实施例的用于对非易失性存储设备执行读取操作的方法的时序图；

[0041] 图 7 是用于图示依照第五实施例的用于对非易失性存储设备执行读取操作的方法的时序图；

[0042] 图 8 是用于图示依照第六实施例的用于对非易失性存储设备执行读取操作的方法的时序图；以及

[0043] 图 9 是用于图示依照第七实施例的用于对非易失性存储设备执行读取操作的方

Micron Ex. 1002, p. 106
Micron v. YMTC
IPR2024-00793

法的时序图。

具体实施方式

[0044] 以下，将参考附图详细描述本公开的一些实施例。提供了附图以便使那些本领域普通技术人员能够理解本公开的实施例的范围。

[0045] 图 2 是非易失性存储设备的电路图。

[0046] 非易失性存储设备包括存储单元阵列 200、位线选择部件 210 和页面缓冲器 220，在图 2 中只示出了页面缓冲器 220 的一部分。

[0047] 存储单元阵列 200 包括多个串对 STe 和 STo。可以依照串的位置把串分为偶数串 STe 或奇数串 STo。例如，编号为偶数的串可以成为偶数串 STe，并且编号为奇数的串可以成为奇数串 STo。从而，并行交替地布置偶数串 STe 和奇数串 STo。每个串具有相同的配置。作为一个例子下面将描述偶数串 STe。

[0048] 漏选晶体管 DST 被耦合到偶数串 STe 的漏端，并且源选晶体管 SST 被耦合到其源端。在漏选晶体管 DST 和源选晶体管 SST 之间串联耦合多个存储单元 F0 到 Fn（其中 n 是自然数）。耦合到不同串的各漏选晶体管 DST 的栅端被耦合在一起，由此形成漏选线 DSL。耦合到不同串的各源选晶体管 SST 的栅端被耦合在一起，由此形成源选线 SSL。此外，耦合到不同串的各存储单元 F0 到 Fn 的栅端被耦合在一起，由此分别形成多条字线 WL0 到 WLn（其中 n 是自然数）。漏选晶体管 DST 的漏端被耦合到位线。偶数串 STe 被电耦合到偶数位线 BLe，且奇数串 STo 被电耦合到奇数位线 BLo。

[0049] 位线选择部件 210 包括在偶数位线 BLe 和第一节点 D1 之间耦合的第三开关 N3、在偶数位线 BLe 和奇数位线 BLo 之间串联耦合的第一和第二开关 N1 和 N2 以及在奇数位线 BLo 和第一节点 D1 之间耦合的第四开关 N4。可以使用 NMOS 晶体管实现第一到第四开关 N1 到 N4 中的每个。在第一和第二开关 N1 和 N2 之间施加电压 VIRPWR。第一开关 N1 响应于偶数放电信号 DISe 来动作，并且第二开关 N2 响应于奇数放电信号 DISo 来动作。第三开关 N3 响应于偶数选择信号 SELBLe 来动作，并且第四开关 N4 响应于奇数选择信号 SELBLo 来动作。

[0050] 在图 2 中，只示出了页面缓冲器 220 的一部分，以便描述与此公开有关的部分。页面缓冲器 220 包括在第一节点 D1 和感测节点 SO 之间耦合的第五开关 N5 和在电源电压 (VDD) 和感测节点 SO 之间耦合的预充电开关 P1。可以使用 NMOS 晶体管实现第五开关 N5，并且可以使用 PMOS 晶体管实现预充电开关 P1。第五开关 N5 响应于感测信号 PBSENSE 来动作，并且预充电开关 P1 响应于预充电信号 PRECH_b 来动作。下面更详细地描述使用以上电路的读取操作。

[0051] 图 3 是用于图示依照第一实施例的用于对非易失性存储设备执行读取操作的方法的时序图。

[0052] 参照图 2 和 3，向所有字线顺序地施加通过电压 (Vpass)，其中向选择的字线施加通过电压，然后在通过电压被改变为读取电压 (Vread) 之后执行读取操作。例如，下面将描述要读取的存储单元被耦合到偶数位线 BLe 的情况。

[0053] 非易失性存储设备的读取操作包括感测节点 SO 被预充电的第一区段 T1、位线被预充电的第二区段 T2、通过电压被施加到字线的第三区段 T3、电压被施加到沟道的第四区

Micron Ex. 1002, p. 107
Micron v. YMTC
IPR2024-00793

段 T4、读取电压被施加到选择的字线的第五区段 T5、执行估算操作的第六区段 T6 和数据被感测的第七区段 T7。

[0054] 在第一区段 T1 中，感测节点 SO 被预充电。更详细地，通过向预充电开关 P1 施加逻辑低电平的预充电信号 PRECH_b 来导通预充电开关 P1。当导通预充电开关 P1 时，电源电压 (vdd) 被转送到感测节点 SO，由此对感测节点 SO 预充电。

[0055] 在第二区段 T2 中，位线被预充电。更详细地，施加第一电压 (V1) 电平的感测信号 PBSENSE，由此导通第五开关 N5。在选择偶数位线 BLe 的情况下，导通第三开关 N3，并且关断第四开关 N4。从而，感测节点 SO 和偶数位线 BLe 被电耦合在一起，因此偶数位线 BLe 被预充电。

[0056] 在第三区段 T3 中，施加字线电压。更详细地，逻辑高电平的电压被施加到漏选线 DSL，由此导通漏选晶体管 DST。此时，逻辑低电平的电压被施加到源选线 SSL，以使源选晶体管 SST 保持在关断状态。接下来，向所有字线 WLn 到 WL0（其中 n 是自然数）顺序地施加通过电压 (Vpass)。

[0057] 由于导通漏选晶体管 DST 并且从而经由位线向相应的串施加电压，所以通过电压 (Vpass) 优选从邻近漏选晶体管 DST 的字线 WLn 开始被顺序施加到字线。例如，通过电压 (Vpass) 可以施加到第 n 字线 WL，并且在特定的延迟时间 DL 过去之后，它可以被施加到第 (n-1) 字线 WLn-1。延迟时间 DL 可以被设置为 10ns 到 10000ns。这里，‘ns’指的是纳秒（即，时间单位）。当向所有字线 WLn 到 WL0 顺序地施加通过电压 (Vpass) 时，相应串的所有沟道可以被电耦合在一起。同时，所有字线可以被分为多个组 Gr0 到 GrJ（其中 J 是自然数），每组包括两条或更多条字线。在这种情况下，通过电压 (Vpass) 可以被施加到每组的所有字线。

[0058] 第四区段 T4 是沟道连接区段。通过电压 (Vpass) 被施加到所有字线 WL0 到 WLn 持续特定的时段。优选地是，每个存储单元导通，并且它保持在导通状态中持续特定时段，以致所有沟道被电耦合在一起。例如，在 1000ns 到 10000ns 时间期间，通过电压 (Vpass) 可以被施加到所有字线 WL0 到 WLn，以致可以统一地形成沟道。

[0059] 在第五区段 T5 中，施加读取电压 (Vread)。在向选择的存储块内的所有字线施加通过电压 (Vpass) 之后，已经被施加到所选字线（即，耦合到要读取的存储单元的字线）的通过电压 (Vpass) 被改变为读取电压 (Vread)。例如，在第 (n-1) 字线 WLn-2（假定第一字线为 WL0）是选择的字线的情况下，读取电压 (Vread) 被施加到已经施加了通过电压 (Vpass) 的第 (n-1) 字线 WLn-2。或者，在已经施加通过电压 (Vpass) 的所选字线被放电之后，可以向所选字线 SEL 施加读取电压 (Vread)。可以说第一到第四区段是其中统一地形成选择的串的沟道的区段，并且第五到第七区段是其中读取选择的存储单元的数据的区段。

[0060] 第六区段 T6 是估算区段。更详细地，当降低已经被施加到所选字线 WLn-2 的通过电压 (Vpass) 的电压电平时，因此通过电压 (Vpass) 被改变为读取电压 (Vread)，逻辑高电平的电压被施加到源选线 SSL。在因为选择的存储单元的阈值电压分布电平为高而关断单元的情况下，可以产生沟道升压。为了防止此问题，在执行估算操作的同时导通源选晶体管 SST。或者，当在第五区段 T5 中读取电压 (Vread) 被施加到所选字线时，逻辑高电平的电压可以被施加到源选线 SSL。感测信号 PBSENSE 从逻辑高电平被改变为逻辑低电平，且然后被施加到第五开关 N5。

Micron Ex. 1002, p. 108
Micron v. YMTC
IPR2024-00793

[0061] 在地电压（例如，0V）被施加到共用源线 CSL 的状态中，可以依照选择的存储单元的数据来改变被预充电的偶数位线 BLe 的电压电平。例如在选择的存储单元是擦除单元 ER 的情况下，偶数位线 BLe 的电压电平可被降低。同时在选择的存储单元是编程的单元 PGM 的情况下，偶数位线 BLe 的电压电平维持逻辑高电平。电压电平由于漏泄电流可能被略微降低。

[0062] 第七区段 T7 是感测区段。施加第二电压（V2）电平的感测信号 PBSENSE。即，页面缓冲器 220 与已经被估算的偶数位线 BLe 被电耦合在一起，并且页面缓冲器 220 通过感测偶数位线 BLe 的电压电平变化来读取所选存储单元的数据。

[0063] 图 4 是用于图示依照第二实施例的用于对非易失性存储设备执行读取操作的方法的时序图。

[0064] 参照图 2 和 4，所有字线被分为多个字线组 Gr0 到 Grk（其中 k 是自然数），每组包括一条或更多条字线。通过电压（Vpass）优选被施加到每个字线组的所有字线。特别地是，在通过电压（Vpass）被施加到选择的字线 SEL 继而被施加到所有字线之后，施加到所选字线 SEL 的通过电压（Vpass）被改变为读取电压（Vread），然后执行读取操作。例如，下面将描述要读取的存储单元被耦合到偶数位线 BLe 的情况。

[0065] 非易失性存储设备的读取操作包括感测节点 SO 被预充电的第一区段 T1、位线被预充电的第二区段 T2、通过电压被施加到字线的第三区段 T3、沟道相连接的第四区段 T4、施加读取电压的第五区段 T5、执行估算操作的第六区段 T6 和感测数据的第七区段 T7。

[0066] 在第一区段 T1 中，感测节点 SO 被预充电。更详细地，激活预充电信号 PRECH_b 以便导通预充电开关 P1。从而，感测节点 SO 被预充电。

[0067] 在第二区段 T2 中，位线被预充电。更详细地，感测信号 PBSENSE 被激活为第一电压（V1）电平。在选择偶数位线 BLe 的情况下，导通第三开关 N3，并且关断第四开关 N4。从而，感测节点 SO 和偶数位线 BLe 被电耦合在一起，因此偶数位线 BLe 被预充电。

[0068] 在第三区段 T3 中，施加字线电压。更详细地，逻辑高电平的电压被施加到漏选线 DSL，由此导通漏选晶体管 DST。此时，逻辑低电平的电压被施加到源选线 SSL。接下来，向字线组 Grk 到 Gro（其中 k 是自然数）顺序地施加通过电压（Vpass）。特别地是，由于导通漏选晶体管 DST，所以通过电压（Vpass）优选从邻近漏选晶体管 DST 的字线组开始被顺序地施加到各字线组。更详细地，通过电压（Vpass）被同时施加到在第 k 字线组 Grk 中包括的所有字线。在特定的延迟时间 DL 过去之后，通过电压（Vpass）被同时施加到在第（k-1）字线组 Grk-1 中包括的所有字线。如果通过电压（Vpass）如上所述被顺序地施加到所有字线组，那么沟道可以被容易地电耦合在一起。延迟时间 DL 可以被设置为 10ns 到 10000ns。这里，‘ns’指的是纳秒（即，时间单位）。当通过电压（Vpass）被顺序地施加到所有字线组 Grk 到 Gr0 时，偶数位线 BLe 的预充电电压被施加到选择的串的各沟道。

[0069] 在第四区段 T4 中，各沟道相互连接。尽管即便在第三区段中沟道被电耦合在一起，不过可以通过维持特定的时段把沟道更有效地耦合在一起。更详细地，在通过电压（Vpass）被施加到所有字线组 Gr0 到 Grk 的状态中，尽管逻辑低电平的电压被施加到源选线 SSL，不过没有出现沟道升压。更详细地，通过电压（Vpass）被施加到在所有字线组 Gr0 到 Grk 中包括的所有字线 WL0 到 WLn 持续特定时段。优选地是，在沟道可被充分地耦合在一起的时间期间，施加通过电压（Vpass）。例如，可以施加通过电压（Vpass）持续 1000ns 到

Micron Ex. 1002, p. 109
Micron v. YMTC
IPR2024-00793

10000ns。

[0070] 在第五区段 T5 中，施加读取电压。更详细地，向被电耦合到要读取的存储单元的所选字线 SEL 施加读取电压 (Vread)。例如在要读取的所选字线 SEL 被包括在第 (k-2) 字线组 Grk-2 中的情况下，读取电压 (Vread) 而不是已经被施加到所选字线 SEL 的通过电压 (Vpass) 被施加到所选字线 SEL。此时，通过电压 (Vpass) 继续被施加到在第 (k-2) 字线组 Grk-2 中所包括的、除所选字线 SEL 之外的未选择的字线 Unsel，并且通过电压 (Vpass) 也继续被施加到其它字线组的字线。或者，当读取电压 (Vread) 被施加到所选字线 SEL 时，在对所选字线 SEL 进行放电之后可以施加读取电压 (Vread)。

[0071] 如上所述，由于在把选择的串的所有沟道耦合在一起之后施加读取电压 (Vread)，所以可以防止在字线组 Gr0 到 Grk 下面出现沟道升压。据此，可以抑制出现热电子，这是因为在所选串的阱区内没有产生电场差异。此外，由于可抑制出现热电子，所以可防止存储单元的阈值电压分布的变动。

[0072] 第六区段 T6 是估算区段。更详细地，通过向第五开关 N5 施加其电压电平已经被改变为逻辑低电平的感测信号 PBSENSE，并且向源选线 SSL 施加逻辑高电平的电压，来导通源选晶体管 SST。此时，地电压 (例如，0V) 被施加到共用源线 CSL。在估算区段中，通过电压 (Vpass) 继续被施加到未选择的字线组 Grk、Grk-1 和 Grk-3 到 Gr0 的字线，并且读取电压 (Vread) 继续被施加到所选字线 SEL。在被耦合到所选字线 SEL 的存储单元是擦除的单元或者存储单元的阈值电压电平低于读取电压的情况下，所述存储单元导通。从而，偶数位线 BLe 的电压降低 (ER)。同时，在被耦合到所选字线 SEL 的存储单元的阈值电压电平高于读取电压的情况下，存储单元被关断。从而，偶数位线 BLe 的电压保持不变 (PGM)。

[0073] 第七区段 T7 是感测区段。向第五开关 N5 施加第二电压 (V2) 电平的感测信号 PBSENSE。从而，偶数位线 BLe 与页面缓冲器 220 的感测节点 SO 被电耦合在一起，并且页面缓冲器 220 通过对感测节点 SO 的电压电平的变化进行感测来读取所选存储单元的数据。

[0074] 图 5 是用于图示依照第三实施例的用于对非易失性存储设备执行读取操作的方法的时序图。

[0075] 参照图 2 和 5，非易失性存储设备的读取操作包括感测节点 SO 被预充电的第一区段 T1、位线被预充电的第二区段 T2、电压被施加到字线的第三区段 T3、电压被施加到沟道的第四区段 T4、执行估算操作的第五区段 T5 和感测数据的第六区段 T6。

[0076] 在第一区段 T1 中，感测节点 SO 被预充电。更详细地，通过向预充电开关 P1 施加逻辑低电平的预充电信号 PRECH_b 来导通预充电开关 P1。当导通预充电开关 P1 时，电源电压 (Vdd) 被转送到感测节点 SO，由此对感测节点 SO 预充电。

[0077] 在第二区段 T2 中，位线被预充电。更详细地，施加第一电压 (V1) 电平的感测信号 PBSENSE，由此导通第五开关 N5。在选择偶数位线 BLe 的情况下，导通第三开关 N3，并且关断第四开关 N4。从而，感测节点 SO 和偶数位线 BLe 被电耦合在一起，因此偶数位线 BLe 被预充电。

[0078] 在第三区段 T3 中，电压被施加到字线。更详细地，逻辑高电平的电压被施加到漏选线 DSL，由此导通漏选晶体管 DST。此时，逻辑低电平的电压被施加到源选线 SSL，以致源选晶体管 SST 保持关断状态。接下来，驱动电压顺序地施加到所有字线。这里，读取电压 (Vread) 被施加到选择的字线 SEL，并且通过电压 (Vpass) 被施加到其余未选择的字线

Micron Ex. 1002, p. 110
Micron v. YMTC
IPR2024-00793

Unsel。

[0079] 由于导通漏选晶体管 DST 并且从而经由位线向相应的串施加电压，所以通过电压 (Vpass) 优选从邻近漏选晶体管 DST 的字线 WLn 开始顺序地施加到字线。例如，通过电压 (Vpass) 可被施加到第 n 字线 WLn，并且在特定的延迟时间 DL 过去之后，它可以被施加到第 (n-1) 字线 WLn-1。延迟时间 DL 可以被设置为 10ns 到 10000ns。这里，'ns' 指的是纳秒 (即，时间单位)。当向所有字线 WLn 到 WL0 顺序地施加通过电压 (Vpass) 或读取电压 (Vread) 时，相应串的沟道可以被容易地耦合在一起。

[0080] 第四区段 T4 是沟道连接区段。通过电压 (Vpass) 被施加到所有字线 WL0 到 WLn 持续特定的时段。优选地是，每个存储单元导通，并且它保持导通状态持续特定时段，以致所有沟道被电耦合在一起。例如，在 1000ns 到 10000ns 时间期间，通过电压 (Vpass) 可以被施加到所有字线 WL0 到 WLn，以致可以统一地形成沟道。

[0081] 第五区段 T5 是估算区段。更详细地，逻辑高电平的电压被施加到源选线 SSL，以便由此导通源选晶体管 SST。同时，感测信号 PBSENSE 的电压电平被改变为逻辑低电平并且被施加到第五开关 N5。

[0082] 在地电压 (例如，0V) 被施加到共用源线 CSL 的状态中，可以依照选择的存储单元的数据来改变被预充电的偶数位线 BLe 的电压电平。例如在选择的存储单元是擦除的单元或者存储单元的阈值电压电平低于读取电压的情况下，偶数位线 BLe 的电压电平降低 (ER)。同时，在选择的存储单元的阈值电压电平高于读取电压的情况下，偶数位线 BLe 的电压电平保持逻辑高电平 (PGM)。

[0083] 第六区段 T6 是感测区段。向第五开关 N5 施加第二电压 (V2) 的感测信号 PBSENSE。即，页面缓冲器 220 与已经被估算的偶数位线 BLe 被电耦合在一起，并且页面缓冲器 220 通过感测偶数位线 BLe 的电压电平变化来读取所选存储单元的数据。

[0084] 图 6 是用于图示依照第四实施例的用于对非易失性存储设备执行读取操作的方法的时序图。

[0085] 参照图 2 和 6，所有字线被分为多个字线组 Gr0 到 Grk(k 是自然数)，每组包括一条或更多条字线，并且电压被顺序地施加到每个字线组的所有字线。这里，在包括选择的字线 SEL 的字线组中，读取电压 (Vread) 被施加到所选字线 SEL，并且通过电压 (Vpass) 同时被施加到该字线组中未选择的字线 Unsel。与此同时，通过电压 (Vpass) 被同时施加到不包括所选字线 SEL 的字线组的所有字线。例如，下面将描述要读取的存储单元被耦合到偶数位线 BLe 的情况。

[0086] 非易失性存储设备的读取操作包括感测节点 SO 被预充电的第一区段 T1、位线被预充电的第二区段 T2、电压被施加到字线的第三区段 T3、沟道被耦合在一起的第四区段 T4、执行估算操作的第五区段 T5 和感测数据的第六区段 T6。

[0087] 在第一区段 T1 中，感测节点 SO 被预充电。更详细地，通过向预充电开关 P1 施加逻辑低电平的预充电信号 PRECH_b 来导通预充电开关 P1。响应于此，电源电压 (Vdd) 被转送到感测节点 SO，由此对感测节点 SO 进行预充电。

[0088] 在第二区段 T2 中，位线被预充电。更详细地，施加第一电压 (V1) 电平的感测信号 PBSENSE，由此对偶数位线 BLe 预充电。例如，在选择偶数位线 BLe 的情况下，可以导通第三开关 N3，并且可以关断第四开关 N4。从而，感测节点 SO 和偶数位线 BLe 被电耦合在一起，

Micron Ex. 1002, p. 111
Micron v. YMTC
IPR2024-00793

因此偶数位线 BLe 被预充电。

[0089] 在第三区段 T3 中，电压被施加到字线。更详细地，逻辑高电平的电压被施加到漏选线 DSL，由此导通漏选晶体管 DST。此时，施加到源选线 SSL 的电压保持逻辑低电平。接下来，向字线组 Grk 到 Gr0（其中 k 是自然数）顺序地施加驱动电压（通过电压或读取电压）。优选地是，通过电压 (Vpass) 被施加到字线组 Grk 到 Gr0 中未选择的字线 Unsel，并且读取电压 (Vread) 被施加到所选字线 SEL。

[0090] 由于导通漏选晶体管 DST，所以驱动电压（通过电压或读取电压）优选从邻近漏选晶体管 DST 的字线组开始被顺序地施加到字线。更详细地，通过电压 (Vpass) 被同时施加到在第 k 字线组 Grk 中包括的所有字线。接下来，在特定的延迟时间 DL 过去之后，通过电压 (Vpass) 被同时施加到在第 (k-1) 字线组 Grk-1 中包括的所有字线。特别地是，在包括所选字线 SEL 的字线组 Grk-2 中，读取电压 (Vread) 被施加到所选字线 SEL，并且通过电压 (Vpass) 被同时施加到其余未选择的字线 Unsel。在字线组之间的延迟时间 DL 被设置为 10ns 到 10000ns。这里‘ns’（即，时间单位）指的是‘纳秒’。如果驱动电压（通过电压或读取电压）如上所述被顺序地施加到所有字线组 Grk 到 Gr0，那么选择的串的各沟道可以被容易地电耦合在一起，并且可以抑制出现沟道升压。

[0091] 在第四区段 T4 中，其中电压被施加到在所有字线组中包括的所有字线的状态保持不变。更详细地，通过电压 (Vpass) 或读取电压 (Vread) 被施加到在所有字线组 Gr0 到 Grk 中包括的所有字线 WL0 到 WLn 持续特定的时段。优选地是，在沟道可以被充分电耦合在一起的时段施加电压 (Vpass) 或 (Vread)。例如，优选地是，在 1000ns 到 10000ns 的时间期间施加电压 (Vpass) 或 (Vread)。

[0092] 第五区段 T5 是估算区段。更详细地，其电压电平已经被改变为逻辑低电平的感测信号 PBSENSE 被施加到第五开关 N5，并且逻辑高电平的电压被施加到源选线 SSL，由此导通源选晶体管 SST。此时，地电压（例如，0V）被施加到共用源线 CSL。在估算区段中，通过电压 (Vpass) 继续被施加到未选择的字线组 Grk、Grk-1 和 Grk-3 到 Gr0 的所有字线，并且读取电压 (Vread) 继续被施加到所选字线 SEL。在被耦合到所选字线 SEL 的存储单元的阈值电压电平高于读取电压 (Vread) 的情况下，沟道电压保持不变，这是因为所选择的存储单元被关断。即，偶数位线 BLe 的电压电平保持不变 (PGM)。同时，在被耦合到所选字线 SEL 的存储单元是擦除的单元 ER 或者存储单元的阈值电压低于读取电压 (Vread) 的情况下，因为所选的存储单元导通，所以沟道的电压电平降低。即，偶数位线 BLe 的电压电平降低 (ER)。

[0093] 第六区段 T6 是感测区段。第二电压 (V2) 的感测信号 PBSENSE 被施加到第五开关 N5，由此把页面缓冲器 220 的感测节点 SO 和偶数位线 BLe 电耦合。据此，页面缓冲器 220 可以通过感测页面缓冲器 220 的感测节点 SO 的电压电平变化来读取所选存储单元的数据。

[0094] 图 7 是用于图示依照第五实施例的用于对非易失性存储设备执行读取操作的方法的时序图。

[0095] 参照图 2 和 7，在对所选择的位线预充电之后，通过电压被同时施加到所有字线。接下来，已经被施加到选择的字线的通过电压被改变为读取电压，然后执行读取操作。例如，下面将描述要读取的存储单元被耦合到偶数位线 BLe 的情况。

[0096] 非易失性存储设备的读取操作包括感测节点 SO 被预充电的第一区段 T1、位线被预充电的第二区段 T2、通过电压被施加到字线的第三区段 T3、施加读取电压的第四区段

Micron Ex. 1002, p. 112
Micron v. YMTC
IPR2024-00793

T4、执行估算操作的第五区段 T5 和感测数据的第六区段 T6。

[0097] 在第一区段 T1 中，感测节点 SO 被预充电。更详细地，通过向预充电开关 P1 施加逻辑低电平的预充电信号 PRECH_b 来导通预充电开关 P1。响应于此，电源电压 (Vdd) 被转送到感测节点 SO，由此对感测节点 SO 进行预充电。

[0098] 在第二区段 T2 中，位线被预充电。更详细地，激活第一电压 (V1) 电平的感测信号 PBSENSE。例如，在选择偶数位线 BLe 的情况下，可以导通第三开关 N3，并且可以关断第四开关 N4。从而，感测节点 SO 和偶数位线 BLe 被电耦合在一起，因此偶数位线 BLe 被预充电。

[0099] 在第三区段 T3 中，电压被施加到字线。更详细地，通过电压 (Vpass) 被同时施加到所有字线 WL0 到 WLn，由此把沟道电耦合。此时，逻辑高电平的电压被施加到漏选线 DSL 和源选线 SSL，由此导通漏选晶体管 DST 和源选晶体管 SST。特别地是，由于导通源选晶体管 SST，所以尽管通过电压 (Vpass) 被同时施加到所有字线也可以防止出现沟道升压。这里，通过电压 (Vpass) 优选在 1000ns 到 10000ns 时间期间被施加到所有字线 WL0 到 WLn，以便保持沟道。如上所述，由于通过电压 (Vpass) 被施加到所有字线 WL0 到 WLn，所以可以把沟道电耦合在一起。此外，由于导通源选晶体管 SST，所以可以防止出现沟道升压。

[0100] 在第四区段 T4 中，施加读取电压。向被电耦合到要读取的存储单元的选择的字线 SEL 施加读取电压 (Vread)。更详细地，已施加到所选字线 SEL 的通过电压 (Vpass) 被改变为读取电压 (Vread)，然后向所选字线 SEL 施加读取电压 (Vread)。或者，在已施加了通过电压 (Vpass) 的所选字线 SEL 被放电之后，可以向所选字线 SEL 施加读取电压 (Vread)。此时，其电平已改变为逻辑低电平的电压被施加到源选线 SSL。即，由于在把沟道电耦合之后施加读取电压 (Vread)，所以可防止出现沟道升压。据此，因为还可以抑制出现热电子，所以可防止存储单元的阈值电压分布的变动。此时，通过电压 (Vpass) 继续被施加到其余未选择的字线 Unsel。

[0101] 第五区段 T5 是估算区段。更详细地，其电压电平已改变为逻辑低电平的感测信号 PBSENSE 被施加到第五开关 N5，并且逻辑高电平的电压被施加到源选线 SSL，由此导通源选晶体管 SST。此时，地电压 (例如，0V) 被施加到共用源线 CSL。在估算区段中，通过电压 (Vpass) 继续被施加到所有未选择的字线，并且读取电压 (Vread) 继续被施加到所选字线 SEL。在被耦合到所选字线 SEL 的存储单元的阈值电压电平高于读取电压 (Vread) 的情况下，偶数位线 BLe 的电压被维持 (PGM)，这是因为所选择的存储单元被关断。同时，在被耦合到所选字线 WLn-2 的存储单元是擦除的单元 ER 或者存储单元的阈值电压低于读取电压 (Vread) 的情况下，因为所选的存储单元导通，所以偶数位线 BLe 的电压电平降低 (ER)。

[0102] 第六区段 T6 是感测区段。第二电压 (V2) 的感测信号 PBSENSE 被施加到第五开关 N5，由此把页面缓冲器 220 的感测节点 SO 与偶数位线 BLe 电耦合。据此，页面缓冲器 220 可以通过感测页面缓冲器 220 的感测节点 SO 的电压电平变化来读取所选存储单元的数据。

[0103] 图 8 是用于图示依照第六实施例的用于对非易失性存储设备执行读取操作的方法的时序图。

[0104] 在用于操作读取操作的方法中，在通过向所有字线同时施加通过电压把沟道电耦合之后，读取电压被施加到选择的字线。下面将更详细地描述读取操作。

[0105] 参照图 2 和 8，非易失性存储设备的读取操作包括感测节点 SO 被预充电的第一区段 T1、沟道被耦合在一起的第二区段 T2、位线被预充电的第三区段 T3、施加读取电压的第

Micron Ex. 1002, p. 113
Micron v. YMTC
IPR2024-00793

四区段 T4、执行估算操作的第五区段 T5 和感测数据的第六区段 T6。

[0106] 在第一区段 T1 中，感测节点 SO 被预充电。更详细地，通过向预充电开关 P1 施加逻辑低电平的预充电信号 PRECH_b 来导通预充电开关 P1。当导通预充电开关 P1 时，电源电压 (Vdd) 被转送到感测节点 SO，由此对感测节点 SO 预充电。

[0107] 在第二区段 T2 中，通过电压 (Vpass) 被同时施加到所有字线 WL。当通过电压 (Vpass) 被施加到所有字线 WL 时，在被耦合到字线 WL 的存储单元下面，沟道被电耦合在一起。此时，通过向漏选线 DSL 和源选线 SSL 施加逻辑高电平电压来导通漏选晶体管 DST 和源选晶体管 SST。在地电压 (Vss) 已经被施加到共用源线 CSL 的情况下，位线被放电和复位。

[0108] 在第三区段 T3 中，偶数位线 BLe 被预充电。当第一电压 (V1) 的感测信号 PBSENSE 被施加到第五开关 N5 时，把已经被预充电的感测节点 SO 与偶数位线 BLe 电耦合在一起，因此偶数位线 BLe 被预充电。在这种情况下，由于导通源选晶体管 SST，所以偶数位线 BLe 被缓慢地预充电。

[0109] 在第四区段 T4 中，读取电压 (Vread) 被施加到选择的字线 SEL。优选地，当已被施加到源选线 SSL 的逻辑高电平的电压被改变为逻辑低电平继而被施加到源选线 SSL 时，读取电压 (Vread) 被施加到所选字线 SEL。更详细地，代替已被施加到所选字线 SEL 的通过电压 (Vpass)，读取电压 (Vread) 被施加到所选字线 SEL。或者，已施加了通过电压 (Vpass) 的所选字线 SEL 可以被放电，并且然后读取电压 (Vread) 可以被施加到所选字线 SEL。在这种情况下，由于在所有沟道被耦合到选择的串的状态中施加读取电压 (Vread)，所以可以抑制出现沟道升压。据此，由于可以阻止出现热电子，所以可防止存储单元的阈值电压分布的变动。在这种情况下，通过电压 (Vpass) 继续被施加到其余未选择的字线 Unsel。

[0110] 第五区段 T5 是估算区段。更详细地，其电压电平已经从逻辑高电平被改变为逻辑低电平的感测信号 PBSENSE 被施加到第五开关 N5，并且逻辑高电平的电压被施加到源选线 SSL，由此导通源选晶体管 SST。此时，地电压 (例如，0V) 被施加到共用源线 CSL。在估算区段中，通过电压 (Vpass) 继续被施加到未选择的字线 Unsel，并且读取电压 (Vread) 继续被施加到所选字线 SEL。当导通源选晶体管 SST 时，依照被耦合到所选字线 SEL 的存储单元的数据状态来改变偶数位线 BLe 的电压电平。例如，在被耦合到所选字线 SEL 的存储单元的阈值电压电平高于读取电压的情况下，因为所选择的存储单元被关断，所以沟道电压被维持 (PGM)。同时，在被耦合到所选字线 SEL 的存储单元是擦除的单元或者存储单元的阈值电压低于读取电压的情况下，因为所选的存储单元导通，所以沟道的电压电平降低 (ER)。

[0111] 在第六区段 T6 中，在完成对所选存储单元的估算后，第二电压 (V2) 的感测信号 PBSENSE 施加到第五开关 N5，由此把页面缓冲器 220 的感测节点 SO 与偶数位线 BLe 电耦合。据此，页面缓冲器 220 可以通过感测页面缓冲器 220 的感测节点 SO 的电压电平变化来读取所选存储单元的数据。

[0112] 图 9 是用于图示依照第七实施例的用于对非易失性存储设备执行读取操作的方法的时序图。

[0113] 在操作读取操作的方法中，在通过向所有字线同时施加通过电压或读取电压把沟道电耦合之后，执行读取操作。下面将更详细地描述该方法。

[0114] 参照图 2 和 9，非易失性存储设备的读取操作包括感测节点 SO 被预充电的第一区

Micron Ex. 1002, p. 114
Micron v. YMTC
IPR2024-00793

段 T1、沟道被耦合在一起的第二区段 T2、位线被预充电的第三区段 T3、施加读取电压的第四区段 T4、执行估算操作的第五区段 T5 和感测数据的第六区段 T6。

[0115] 在第一区段 T1 中，感测节点 SO 被预充电。更详细地，通过向预充电开关 P1 施加逻辑低电平的预充电信号 PRECH_b 来导通预充电开关 P1。当导通预充电开关 P1 时，电源电压 (Vdd) 被转送到感测节点 SO，由此对感测节点 SO 预充电。

[0116] 在第二区段 T2 中，通过电压 (Vpass) 被施加到未选择的字线 Unsel，并且读取电压 (Vread) 被同时施加到选择的字线 SEL。此时，逻辑高电平的电压被施加到漏选线 DSL 和源选线 SSL，由此导通漏选晶体管 DST 和源选晶体管 SST。尽管通过电压 (Vpass) 或读取电压 (Vread) 被施加到字线 WL，不过因为漏选和源选晶体管 DST 和 SST 均导通，所以不会出现沟道升压。

[0117] 在第三区段 T3 中，偶数位线 BLe 被预充电。更详细地，施加第一电压 (V1) 电平的感测信号 PBSENSE。从而，已经被预充电的感测节点 SO 和偶数位线 BLe 被电耦合在一起，因此偶数位线 BLe 被预充电。在这种情况下，由于导通源选晶体管 SST，所以偶数位线 BLe 被缓慢地预充电。

[0118] 在第四区段 T4 中，已被施加到源选线 SSL 的电压被改变为逻辑低电平继而被施加到源选线 SSL，由此关断源选晶体管 SST。在这种情况下，可以确保偶数位线 BLe 的预充电电平具有足够用于读取操作的电平。尽管源选晶体管 SST 已经被关断并且在所选存储单元下面的沟道通过施加到所选字线 SEL 的读取电压 (Vread) 被去激活，不过因为沟道已经被电耦合，所以可以阻止出现沟道升压。

[0119] 第五区段 T5 是估算区段。更详细地，其电压电平已经从逻辑高电平改变为逻辑低电平的感测信号 PBSENSE 被施加到第五开关 N5，并且逻辑高电平的电压被施加到源选线 SSL，由此导通源选晶体管 SST。此时，地电压 (例如，0V) 被施加到共用源线 CSL。在估算区段中，通过电压 (Vpass) 继续被施加到未选择的字线 Unsel，并且读取电压 (Vread) 继续被施加到所选字线 SEL。当导通源选晶体管 SST 时，依照被耦合到所选字线 SEL 的存储单元的数据状态来改变偶数位线 BLe 的电压电平。例如，在被耦合到所选字线 SEL 的存储单元的阈值电压电平高于读取电压的情况下，因为所选择的存储单元被关断，所以沟道电压被维持 (PGM)。同时，在被耦合到所选字线 SEL 的存储单元是擦除的单元或者存储单元的阈值电压低于读取电压的情况下，因为所选的存储单元导通，所以沟道的电压电平降低 (ER)。

[0120] 第六区段 T6 中，在完成对所选存储单元的估算后，第二电压 (V2) 的感测信号 PBSENSE 施加到第五开关 N5，由此把页面缓冲器 220 的感测节点 SO 和偶数位线 BLe 电耦合。据此，页面缓冲器 220 可以通过感测页面缓冲器 220 的感测节点 SO 的电压电平变化来读取所选存储单元的数据。

[0121] 如上所述，在把选择的串的沟道电耦合之后，执行读取操作。从而，可以防止在整个所选串内或在所选串的部分中出现沟道升压。由于可以抑制出现沟道升压，所以可以防止其中出现电场差异的区域，因此可以防止出现热电子。由于可以防止把热电子引入到存储单元中，所以可防止阈值电压分布的变动，因此可以改进非易失性存储设备的可靠性。

[0122] 依照本公开的实施例，可以通过阻止在读取操作中出现沟道升压来防止出现热电子。从而，可以防止存储单元的阈值电压分布的变动，并且可防止阈值电压分布宽度的增加。据此，可改进非易失性存储设备的可靠性。

Micron Ex. 1002, p. 115
Micron v. YMTC
IPR2024-00793

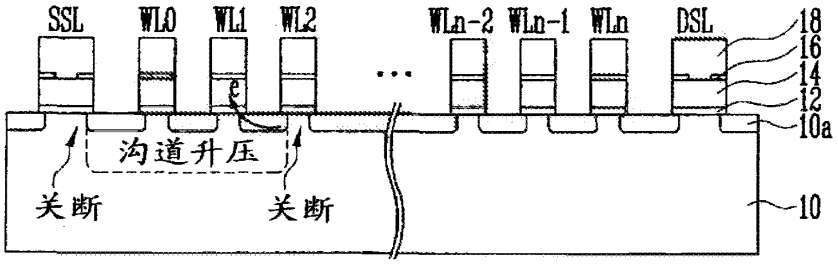


图 1

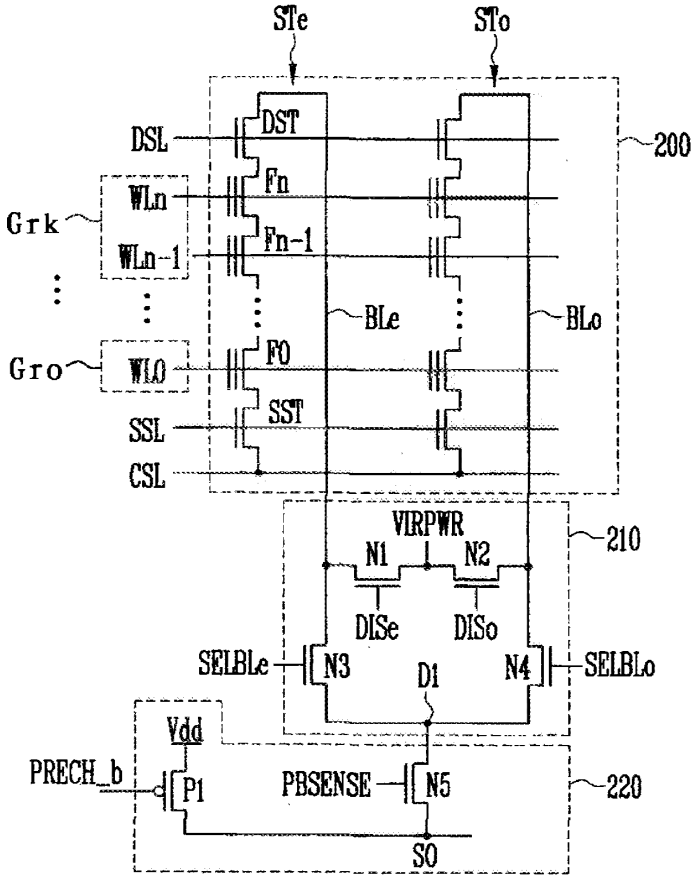


图 2

Micron Ex. 1002, p. 116
Micron v. YMTC
IPR2024-00793

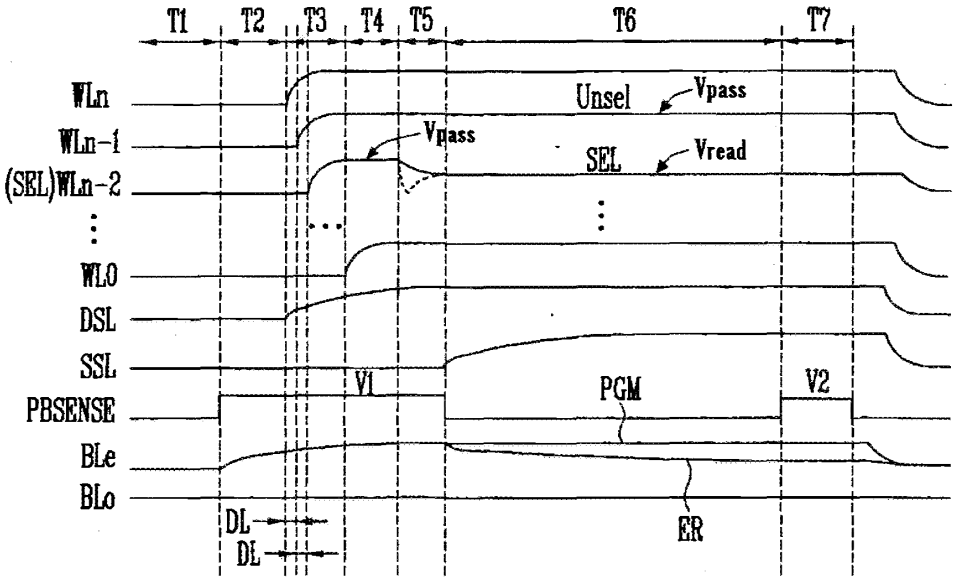


图 3

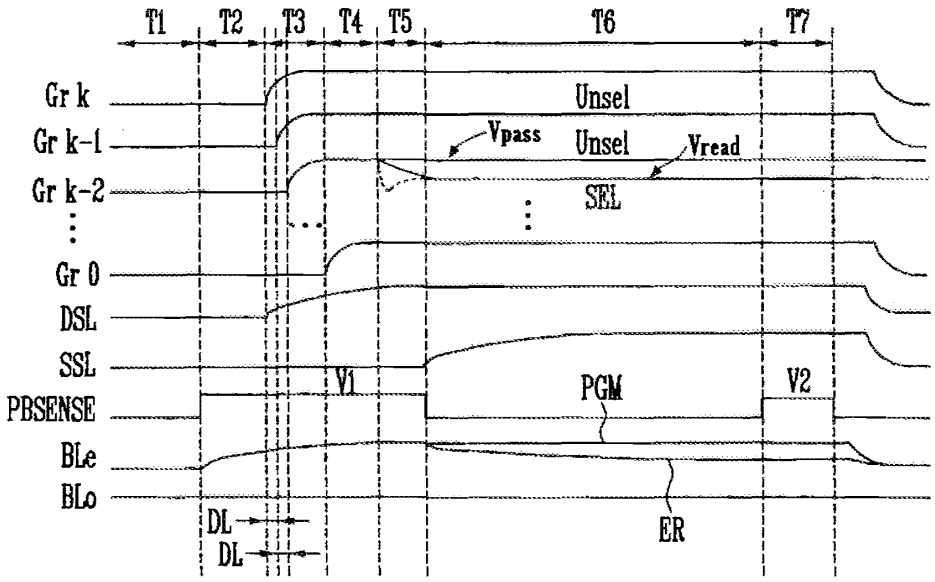


图 4

Micron Ex. 1002, p. 117
Micron v. YMTC
IPR2024-00793

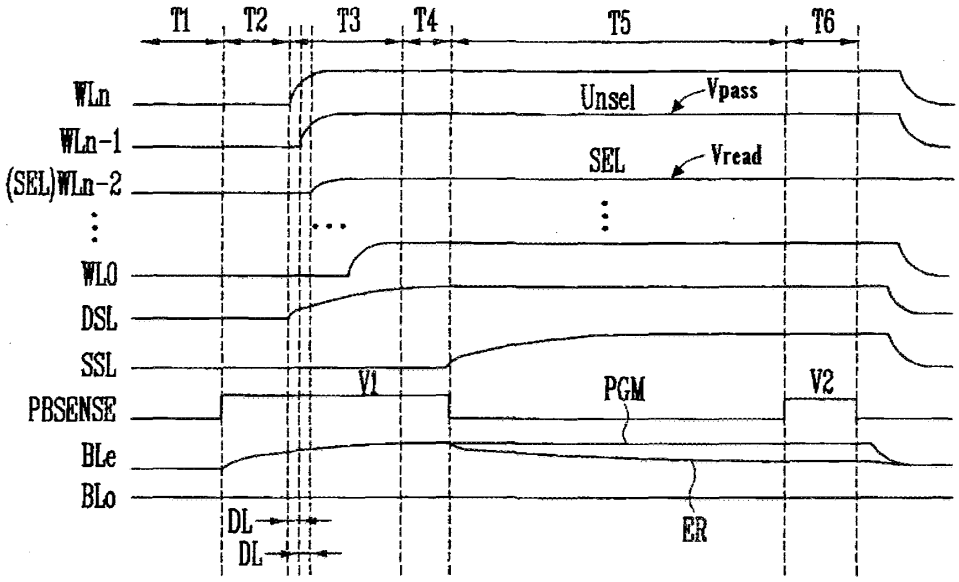


图 5

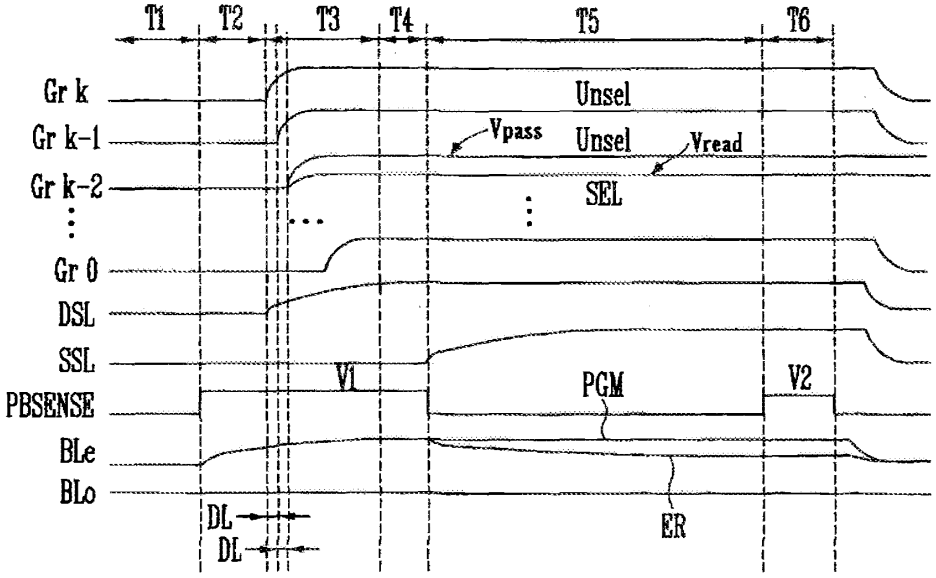


图 6

Micron Ex. 1002, p. 118
Micron v. YMTC
IPR2024-00793

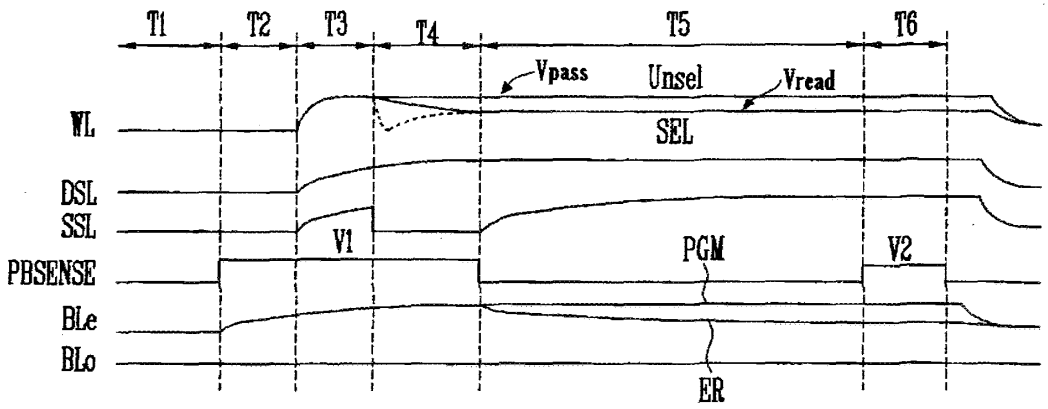


图 7

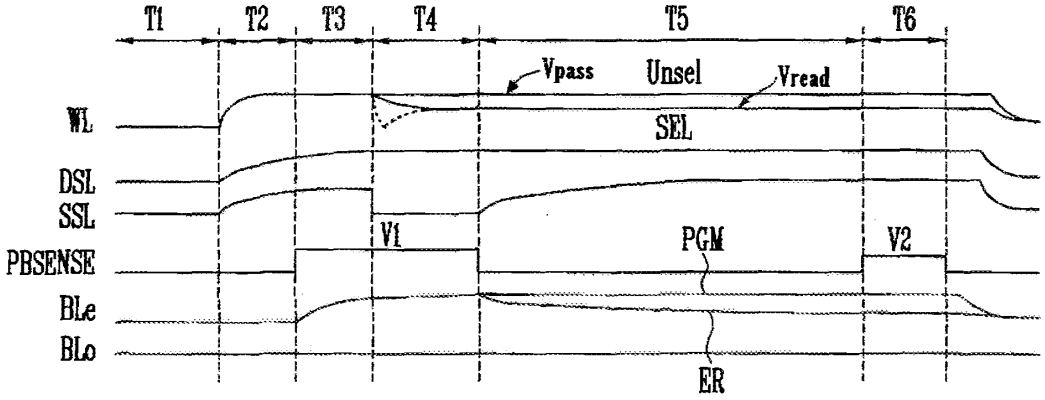


图 8

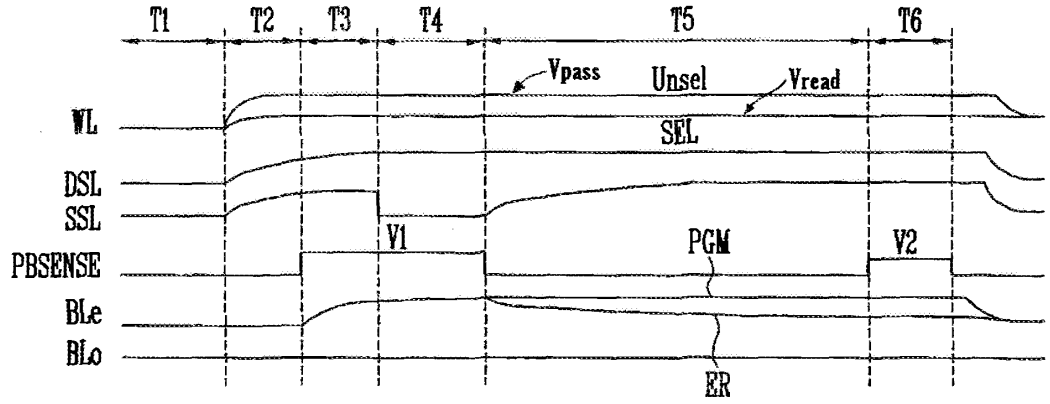


图 9

Micron Ex. 1002, p. 119
Micron v. YMTC
IPR2024-00793

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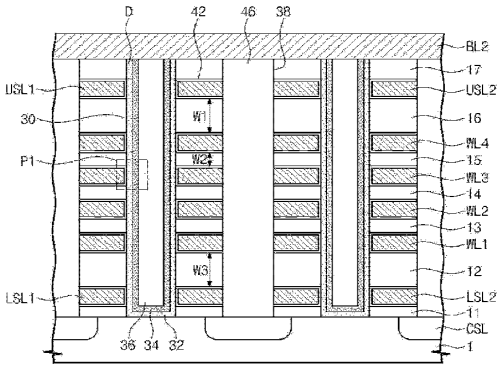
权利要求书9页 说明书25页 附图44页

(54)发明名称

三维电阻性随机存取存储器器件、其操作方法及其制造方法

(57)摘要

本发明涉及一种三维电阻性随机存取存储器器件、其操作方法及其制造方法。半导体器件包括在水平方向上延伸的衬底。在衬底上存在着在相对于衬底的水平延伸方向的垂直方向上延伸的有源柱。在衬底上存在沿着有源柱在垂直方向上延伸的可变电阻性图案，可变电阻性图案的电阻响应于其氧化或还原而改变。栅极存在于有源柱的侧壁处。



CN 103490008 A

Micron Ex. 1002, p. 120
Micron v. YMTC
IPR2024-00793

1. 一种半导体器件，包括：

在水平方向上延伸的衬底；

在所述衬底上在相对于所述衬底的水平延伸方向的垂直方向上延伸的有源柱；

在所述衬底上的可变电阻性图案，该可变电阻性图案沿着所述有源柱在所述垂直方向上延伸，所述可变电阻性图案的电阻响应于其氧化或还原而改变；以及

位于所述有源柱的侧壁处的栅极。

2. 根据权利要求 1 所述的半导体器件，其中所述有源柱是包括侧壁和基底的杯形结构。

3. 根据权利要求 2 所述的半导体器件，其中所述可变电阻性图案是包括侧壁和基底的杯形结构。

4. 根据权利要求 3 所述的半导体器件，其中所述可变电阻性图案位于所述有源柱的所述侧壁的内部区域处并位于所述有源柱的所述基底上。

5. 根据权利要求 2 所述的半导体器件，其中所述可变电阻性图案是中空结构，所述中空结构包括位于所述有源柱的所述侧壁的内部区域处的侧壁。

6. 根据权利要求 1 所述的半导体器件，其中所述有源柱是包括侧壁和基底的杯形结构，且其中所述有源柱的所述侧壁包括第一和第二有源层。

7. 根据权利要求 1 所述的半导体器件，还包括在所述有源柱和所述衬底之间的单晶材料的焊盘。

8. 根据权利要求 7 所述的半导体器件，其中所述单晶材料的焊盘具有与所述有源柱的外侧壁对齐的外侧壁。

9. 根据权利要求 1 所述的半导体器件，其中所述有源柱的底部接触所述衬底，且其中所述电阻性图案的底部在所述垂直方向上与所述有源柱的底部间隔开。

10. 根据权利要求 1 所述的半导体器件，其中所述电阻性图案在所述水平方向上具有小于 20nm 的厚度。

11. 根据权利要求 1 所述的半导体器件，其中所述可变电阻性图案是具有侧壁的中空结构，且其中所述有源柱位于所述可变电阻性图案的所述侧壁的内部区域处。

12. 根据权利要求 1 所述的半导体器件，还包括：

在所述衬底上的多个层间介电层；

多个栅极图案，每个栅极图案都位于邻近的下层间介电层和邻近的上层间介电层之间；

其中所述有源柱和所述可变电阻性图案在所述垂直方向上延伸穿过所述多个层间介电层和所述多个栅极图案；

其中：

所述多个栅极图案的最上栅极图案包括上选择晶体管的上选择栅极；

所述多个栅极图案的最下栅极图案包括下选择晶体管的下选择栅极；并且

在所述上选择栅极和所述下选择栅极之间的所述多个栅极图案的剩余栅极图案包括所述半导体器件的单元串的存储器单元晶体管的控制栅极；并且

其中所述半导体器件包括半导体存储器器件。

13. 根据权利要求 12 所述的半导体器件，其中：

Micron Ex. 1002, p. 121
Micron v. YMTC
IPR2024-00793

连接在所述半导体器件的第一水平方向上排列的共享所述半导体存储器器件的同一层的存储器单元晶体管的控制栅极，以提供所述半导体存储器器件的字线；

所述半导体器件的单元串的存储器单元晶体管通过垂直沟道串联耦合在一起；并且

连接在所述半导体器件的第二水平方向上排列的垂直沟道的上部，以提供所述半导体存储器器件的位线。

14. 根据权利要求 12 所述的半导体器件，其中：

所述最上栅极图案包括第一和第二最上栅极图案，所述第一和第二最上栅极图案用于所述半导体存储器器件的第一和第二上选择晶体管的第一和第二上选择栅极；并且

所述最下栅极图案包括第一和第二最下栅极图案，所述第一和第二最下栅极图案用于所述半导体存储器器件的第一和第二下选择晶体管的第一和第二下选择栅极。

15. 根据权利要求 12 所述的半导体器件，其中：

所述有源柱在所述水平方向上相邻于所述上选择晶体管的所述上选择栅极、所述下选择晶体管的所述下选择栅极以及所述存储器单元晶体管的所述控制栅极；并且

所述可变电阻性图案在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极，且在所述水平方向上不相邻于所述上选择晶体管的所述上选择栅极和所述下选择晶体管的所述下选择栅极。

16. 根据权利要求 15 所述的半导体器件，还包括位于所述有源柱和所述衬底之间的单晶材料的焊盘。

17. 根据权利要求 12 所述的半导体器件，其中：

所述有源柱在所述水平方向上相邻于所述上选择晶体管的所述上选择栅极、所述下选择晶体管的所述下选择栅极以及所述存储器单元晶体管的所述控制栅极；并且

所述可变电阻性图案在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述下选择晶体管的所述下选择栅极，且在所述水平方向上不相邻于所述上选择晶体管的所述上选择栅极。

18. 根据权利要求 12 所述的半导体器件，其中所述可变电阻性图案是具有侧壁的中空结构，且其中所述有源柱位于所述可变电阻性图案的所述侧壁的内部区域处。

19. 根据权利要求 18 所述的半导体器件，还包括在所述有源柱和所述衬底之间的单晶材料的焊盘，其中：

所述单晶材料的焊盘在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极；

所述有源柱在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性图案在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极，且在所述水平方向上不相邻于所述下选择晶体管的所述下选择栅极和所述上选择晶体管的所述上选择栅极。

20. 根据权利要求 18 所述的半导体器件，还包括在所述有源柱和所述衬底之间的单晶材料的焊盘，其中：

所述单晶材料的焊盘在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极；

Micron Ex. 1002, p. 122
Micron v. YMTC
IPR2024-00793

所述有源柱在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性图案在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极，且在所述水平方向上不相邻于所述下选择晶体管的所述下选择栅极。

21. 根据权利要求 18 所述的半导体器件，其中：

所述有源柱在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极、所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性图案在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极，且在所述水平方向上不相邻于所述下选择晶体管的所述下选择栅极和所述上选择晶体管的所述上选择栅极。

22. 根据权利要求 18 所述的半导体器件，其中：

所述有源柱在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极、所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性图案在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极，且在所述水平方向上不相邻于所述下选择晶体管的所述下选择栅极。

23. 根据权利要求 18 所述的半导体器件，其中：

所述有源柱在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极、所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性图案在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极以及所述存储器单元晶体管的所述控制栅极，且在所述水平方向不相邻于所述上选择晶体管的所述上选择栅极。

24. 一种半导体器件，包括：

在水平方向上延伸的半导体材料的衬底；

在所述衬底上的多个层间介电层；

多个栅极图案，每个栅极图案都在邻近的下层间介电层和邻近的上层间介电层之间；

在所述衬底上并在垂直方向上延伸穿过所述多个层间介电层和所述多个栅极图案的半导体材料的垂直沟道；以及

沿所述半导体材料的垂直沟道的可变电阻性材料的垂直沟道；其中所述可变电阻性材料的垂直沟道具有响应于其氧化和还原的可变电阻。

25. 根据权利要求 24 所述的半导体器件，其中在所述垂直沟道中的电流是双向的，在所述半导体器件的编程操作过程中的电流的第一方向，以及在所述半导体器件的擦除操作过程中相反于所述第一方向的电流的第二方向。

26. 根据权利要求 24 所述的半导体器件，其中：

所述多个栅极图案的最上栅极图案包括上选择晶体管的上选择栅极；

所述多个栅极图案的最下栅极图案包括下选择晶体管的下选择栅极；

在所述上选择栅极和所述下选择栅极之间的所述多个栅极图案的剩余栅极图案包括所述半导体器件的单元串的存储器单元晶体管的控制栅极；

Micron Ex. 1002, p. 123
Micron v. YMTC
IPR2024-00793

连接在所述半导体器件的第一水平方向上排列的共享所述半导体存储器器件的同一层的存储器单元晶体管的控制栅极，以提供所述半导体器件的字线；

所述半导体器件的单元串的存储器单元晶体管通过所述垂直沟道串联耦合在一起；

连接在所述半导体器件的第二水平方向上排列的半导体材料的垂直沟道的上部，以提供所述半导体器件的位线；并且

所述半导体器件包括半导体存储器器件。

27. 根据权利要求 26 所述的半导体器件，其中在所述衬底和所述半导体材料的垂直沟道的上部之间沿所述半导体材料的垂直沟道存在电流通路，且其中所述下选择晶体管和所述上选择晶体管控制所述电流通路的操作。

28. 根据权利要求 24 所述的半导体器件，其中所述半导体材料的垂直沟道具有内侧壁和外侧壁。

29. 根据权利要求 28 所述的半导体器件，其中所述可变电阻性材料的垂直沟道位于所述半导体材料的垂直沟道的所述内侧壁处。

30. 根据权利要求 28 所述的半导体器件，其中所述可变电阻性材料的垂直沟道位于所述半导体材料的垂直沟道的所述外侧壁处。

31. 根据权利要求 24 所述的半导体器件，其中所述半导体材料的垂直沟道是包括侧壁和基底的杯形结构。

32. 根据权利要求 31 所述的半导体器件，其中所述可变电阻性材料的垂直沟道是包括侧壁和基底的杯形结构。

33. 根据权利要求 32 所述的半导体器件，其中所述可变电阻性材料的垂直沟道位于所述半导体材料的垂直沟道的所述侧壁的内部区域处和所述半导体材料的垂直沟道的所述基底上。

34. 根据权利要求 31 所述的半导体器件，其中所述可变电阻性材料的垂直沟道是中空结构，所述中空结构包括位于所述半导体材料的垂直沟道的侧壁的内部区域处的侧壁。

35. 根据权利要求 24 所述的半导体器件，其中所述半导体材料的垂直沟道是包括侧壁和基底的杯形结构，且其中所述半导体材料的垂直沟道的所述侧壁包括第一和第二有源层。

36. 根据权利要求 24 所述的半导体器件，还包括在所述半导体材料的垂直沟道和所述衬底之间的单晶材料的焊盘。

37. 根据权利要求 36 所述的半导体器件，其中所述单晶材料的焊盘具有与所述半导体材料的垂直沟道的外侧壁对齐的外侧壁。

38. 根据权利要求 24 所述的半导体器件，其中所述半导体材料的垂直沟道的底部接触所述衬底，且其中所述可变电阻性材料的垂直沟道的底部在所述垂直方向上与所述半导体材料的垂直沟道的所述底部间隔开。

39. 根据权利要求 24 所述的半导体器件，其中所述可变电阻性材料的垂直沟道在所述水平方向上具有小于 20nm 的厚度。

40. 根据权利要求 39 所述的半导体器件，其中所述可变电阻性材料的垂直沟道是具有侧壁的中空结构，且其中所述半导体材料的垂直沟道位于所述可变电阻性材料的垂直沟道的所述侧壁的内部区域处。

Micron Ex. 1002, p. 124
Micron v. YMTC
IPR2024-00793

41. 根据权利要求 24 所述的半导体器件，其中：

所述多个栅极图案的最上栅极图案包括上选择晶体管的上选择栅极；

所述多个栅极图案的最下栅极图案包括下选择晶体管的下选择栅极；并且

在所述上选择栅极和所述下选择栅极之间的所述多个栅极图案的剩余栅极图案包括所述半导体器件的单元串的存储器单元晶体管的控制栅极；并且

其中所述半导体器件包括半导体存储器器件。

42. 根据权利要求 41 所述的半导体器件，其中：

连接在所述半导体器件的第一水平方向上排列的共享所述半导体存储器器件的同一层的存储器单元晶体管的控制栅极，以提供所述半导体存储器器件的字线；

所述半导体器件的单元串的存储器单元晶体管通过所述垂直沟道串联耦合在一起；并且

连接在所述半导体器件的第二水平方向上排列的半导体材料的垂直沟道的上部，以提供所述半导体存储器器件的位线。

43. 根据权利要求 41 所述的半导体器件，其中：

所述最上栅极图案包括第一和第二最上栅极图案，所述第一和第二最上栅极图案用于所述半导体存储器器件的第一和第二上选择晶体管的第一和第二上选择栅极；并且

所述最下栅极图案包括第一和第二最下栅极图案，所述第一和第二最下栅极图案用于所述半导体存储器器件的第一和第二下选择晶体管的第一和第二下选择栅极。

44. 根据权利要求 41 所述的半导体器件，其中：

所述半导体材料的垂直沟道在所述水平方向上相邻于所述上选择晶体管的所述上选择栅极、所述下选择晶体管的所述下选择栅极以及所述存储器单元晶体管的所述控制栅极；并且

所述可变电阻性材料的垂直沟道在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极，且在所述水平方向上不相邻于所述上选择晶体管的所述上选择栅极和所述下选择晶体管的所述下选择栅极。

45. 根据权利要求 44 所述的半导体器件，还包括在所述半导体材料的垂直沟道和所述衬底之间的单晶材料的焊盘。

46. 根据权利要求 41 所述的半导体器件，其中：

所述半导体材料的垂直沟道在所述水平方向上相邻于所述上选择晶体管的所述上选择栅极、所述下选择晶体管的所述下选择栅极以及所述存储器单元晶体管的所述控制栅极；并且

所述可变电阻性材料的垂直沟道在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述下选择晶体管的所述下选择栅极，且在所述水平方向上不相邻于所述上选择晶体管的所述上选择栅极。

47. 根据权利要求 41 所述的半导体器件，其中所述可变电阻性材料的垂直沟道是具有侧壁的中空结构，且其中所述半导体材料的垂直沟道位于所述可变电阻性材料的垂直沟道的所述侧壁的内部区域处。

48. 根据权利要求 47 所述的半导体器件，还包括在所述半导体材料的垂直沟道和所述衬底之间的单晶材料的焊盘，

Micron Ex. 1002, p. 125
Micron v. YMTC
IPR2024-00793

其中：

所述单晶材料的焊盘在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极；

所述半导体材料的垂直沟道在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性材料的垂直沟道在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极，且在所述水平方向上不相邻于所述下选择晶体管的所述下选择栅极和所述上选择晶体管的所述上选择栅极。

49. 根据权利要求 47 所述的半导体器件，还包括在所述半导体材料的垂直沟道和所述衬底之间的单晶材料的焊盘，

其中：

所述单晶材料的焊盘在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极；

所述半导体材料的垂直沟道在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性材料的垂直沟道在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极，且在所述水平方向上不相邻于所述下选择晶体管的所述下选择栅极。

50. 根据权利要求 47 所述的半导体器件，其中：

所述半导体材料的垂直沟道在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极、所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性材料的垂直沟道在所述水平方向上相邻于所述存储器单元晶体管的控制栅极，且在所述水平方向上不相邻于所述下选择晶体管的所述下选择栅极和所述上选择晶体管的所述上选择栅极。

51. 根据权利要求 47 所述的半导体器件，其中：

所述半导体材料的垂直沟道在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极、所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性材料的垂直沟道在所述水平方向上相邻于所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极，且在所述水平方向不相邻于所述下选择晶体管的所述下选择栅极。

52. 根据权利要求 47 所述的半导体器件，其中：

所述半导体材料的垂直沟道在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极、所述存储器单元晶体管的所述控制栅极以及所述上选择晶体管的所述上选择栅极；并且

所述可变电阻性材料的垂直沟道在所述水平方向上相邻于所述下选择晶体管的所述下选择栅极以及所述存储器单元晶体管的所述控制栅极，且在所述水平方向上不相邻于所述上选择晶体管的所述上选择栅极。

Micron Ex. 1002, p. 126
Micron v. YMTC
IPR2024-00793

53. 一种形成半导体器件的方法，包括：

在水平方向延伸的衬底上提供在垂直方向上交替的层间介电层和牺牲层的堆叠；

在所述层间介电层和所述牺牲层中形成开口；

在所述开口中形成半导体材料的垂直沟道，所述半导体材料的垂直沟道在所述垂直方向上延伸；

在所述开口中形成可变电阻性材料的垂直沟道，所述可变电阻性材料的垂直沟道在所述垂直方向上延伸，所述可变电阻性材料的垂直沟道具有响应于其氧化或还原而可变的电阻；以及

以导电图案替代所述牺牲层。

54. 根据权利要求 53 所述的方法，其中在所述开口中形成所述半导体材料的垂直沟道包括形成所述半导体材料的垂直沟道以具有位于所述开口的侧壁处的侧壁。

55. 根据权利要求 54 所述的方法，其中在所述开口中形成所述可变电阻性材料的垂直沟道包括在所述半导体材料的垂直沟道的所述侧壁的内部区域处形成所述可变电阻性材料的垂直沟道。

56. 根据权利要求 53 所述的方法，其中在所述开口中形成所述可变电阻性材料的垂直沟道包括形成所述可变电阻性材料的垂直沟道以具有位于所述开口的侧壁处的侧壁。

57. 根据权利要求 56 所述的方法，其中在所述开口中形成所述半导体材料的垂直沟道包括在所述可变电阻性材料的垂直沟道的侧壁的内部区域处形成所述半导体材料的垂直沟道。

58. 根据权利要求 56 所述的方法，其中所述半导体材料的垂直沟道在所述水平方向上具有小于 20nm 的厚度。

59. 根据权利要求 53 所述的方法，其中在所述开口中形成所述半导体材料的垂直沟道包括在所述开口中形成接触所述衬底的所述半导体材料的垂直沟道。

60. 根据权利要求 53 所述的方法，还包括，在所述开口中形成所述半导体材料的垂直沟道之前，在所述开口中在所述衬底上形成单晶材料的焊盘，并且在所述开口中在所述焊盘上形成所述半导体材料的垂直沟道。

61. 一种控制半导体存储器器件的方法，所述半导体存储器器件包括：

在水平方向上延伸的半导体材料的衬底；

在所述衬底上的多个层间介电层；

多个栅极图案，每个栅极图案都在邻近的下层间介电层和邻近的上层间介电层之间；

在所述衬底上并在垂直方向上延伸穿过所述多个层间介电层和所述多个栅极图案的半导体材料的垂直沟道，所述垂直沟道具有外侧壁和内侧壁；以及

位于所述半导体材料的垂直沟道的所述内侧壁处的可变电阻性材料的垂直沟道；

所述方法包括：

对所述多个存储器单元中选定的一个进行选择性编程；以及

对所述多个存储器单元中已编程的选定的一个进行选择性擦除；

其中对所述多个存储器单元中选定的一个进行选择性编程包括通过响应于所述可变电阻性材料的氧化和还原中的一种而改变所述可变电阻性材料的垂直沟道的电阻来进行编程，并且

Micron Ex. 1002, p. 127
Micron v. YMTC
IPR2024-00793

其中对所述多个存储器单元中选定的一个进行选择性擦除包括通过响应于所述可变电阻性材料的氧化和还原中的另一种而改变所述可变电阻性材料的垂直沟道的电阻来进行擦除。

62. 根据权利要求 61 所述的方法，其中所述半导体材料的垂直沟道中的电流是双向的，在半导体器件的选择性编程过程中的电流的第一方向，以及在所述半导体器件的选择性擦除过程中的相反于所述第一方向的电流的第二方向。

63. 根据权利要求 62 所述的方法，其中：

所述多个栅极图案的最上栅极图案包括上选择晶体管的上选择栅极；

所述多个栅极图案的最下栅极图案包括下选择晶体管的下选择栅极；

在所述上选择栅极和所述下选择栅极之间的所述多个栅极图案的剩余栅极图案包括所述半导体器件的单元串的存储器单元晶体管的控制栅极；

连接在所述半导体器件的第一水平方向上排列的共享所述半导体存储器器件的同一层的存储器单元晶体管的控制栅极，以提供所述半导体器件的字线；

所述半导体器件的单元串的存储器单元晶体管通过所述半导体材料的垂直沟道串联耦合在一起；

连接在所述半导体器件的第二水平方向上排列的所述半导体材料的垂直沟道的上部，以提供所述半导体器件的位线；并且

所述半导体器件包括半导体存储器器件。

64. 根据权利要求 63 所述的方法，其中所述存储器单元晶体管的页包括在同一控制栅极控制下的存储器单元晶体管，且其中选择性编程所述多个存储器单元中的至少一个包括小于所述存储器单元晶体管的页地进行选择性编程。

65. 根据权利要求 63 所述的方法，其中所述存储器单元晶体管的页包括在同一控制栅极控制下的存储器单元晶体管，且其中选择性擦除所述多个存储器单元中的至少一个包括小于所述存储器单元晶体管的页地进行选择性擦除。

66. 根据权利要求 63 所述的方法，其中所述选择性编程包括：

对所述衬底施加低电压；

对所述多个存储器单元中所选定的一个的所述半导体材料的垂直沟道所连接到的所述位线施加设定电压；

对与所述多个存储器单元中未被选定的存储器单元相关联的字线施加激活电压；以及

对与所述多个存储器单元中所选定的一个相关联的字线施加去活电压。

67. 根据权利要求 63 所述的方法，其中所述选择性擦除包括：

对所述衬底施加复位电压；

对所述多个存储器单元中所选定的一个的所述半导体材料的垂直沟道所连接到的所述位线施加低电压；

对与所述多个存储器单元中未被选定的存储器单元相关联的字线施加激活电压；以及

对与所述多个存储器单元中所选定的一个相关联的字线施加去活电压。

68. 根据权利要求 63 所述的方法，其中所述选择性擦除包括：

对所述衬底施加低电压；

对所述多个存储器单元中所选定的一个的所述半导体材料的垂直沟道所连接到的所

Micron Ex. 1002, p. 128
Micron v. YMTC
IPR2024-00793

述位线施加感测电压；

对与所述多个存储器单元中未被选定的存储器单元相关联的字线施加激活电压；以及

对与所述多个存储器单元中所选定的一个相关联的字线施加去活电压。

69. 一种存储器系统，包括：

产生命令和地址信号的存储器控制器；以及

包括多个存储器器件的存储器模块，所述存储器模块接收所述命令和地址信号并响应地将数据存储至至少一个存储器器件和从至少一个存储器器件调取数据，

其中每一个存储器器件都包括：

在水平方向上延伸的衬底；

在所述衬底上在相对于衬底的水平延伸方向的垂直方向上延伸的有源柱；

在所述衬底上沿所述有源柱在所述垂直方向上延伸的可变电阻性图案，所述可变电阻性图案的电阻响应于其氧化或还原而改变；以及

位于所述有源柱的侧壁处的栅极。

Micron Ex. 1002, p. 129
Micron v. YMTC
IPR2024-00793

三维电阻性随机存取存储器器件、其操作方法及其制造方法

[0001] 相关申请的交叉引用

[0002] 本美国非临时专利申请根据 35U.S.C. § 119 条款要求于 2012 年 9 月 5 日提交的韩国专利申请 No. 10-2012-0098463 的优先权，通过引用将该韩国专利申请全部内容并入本文。

技术领域

[0003] 本文的公开涉及一种半导体器件，且更具体涉及一种三维电阻性随机存取存储器（3D RRAM）器件、其操作方法及其制造方法。

背景技术

[0004] 已经提出三维集成电路（3D-IC）存储器技术以致力于增加半导体存储器器件的容量。在各种 3D-IC 存储器技术构造中，多个存储器单元以三维排列。虽然已经考虑采用精细图案技术或多级单元（MLC）技术来促进存储器器件的更高集成度，但是这种精细图案技术通常伴随着更高的制造成本，且 MLC 技术在增加单个存储器单元中可存储的数据位的数量方面存在一定局限。因此，作为用于实现增加的存储器容量的工艺设计技术的候选，3D-IC 存储器技术方案已经变得具有吸引力。

[0005] 近来，已经提出“冲孔 - 插塞”技术作为能大幅增加存储器容量的 3D-IC 存储器技术的示例。这种冲孔 - 插塞技术包括在衬底上顺序堆叠多个薄层并形成贯穿多个薄层的插塞。

发明内容

[0006] 发明概念的各个实施例都针对三维电阻性随机存取存储器（3D RRAM）器件、其操作方法及其制造方法。

[0007] 根据一些实施例，半导体器件包括：在水平方向上延伸的衬底；在衬底上在相对于衬底的水平延伸方向的垂直方向上延伸的有源柱；在衬底上沿着有源柱在垂直方向上延伸的可变电阻性图案，可变电阻性图案的电阻响应于其氧化或还原而改变；以及位于有源柱侧壁的栅极。

[0008] 在一些实施例中，有源柱是包括侧壁和基底的杯形结构。

[0009] 在一些实施例中，可变电阻性图案是包括侧壁和基底的杯形结构。

[0010] 在一些实施例中，可变电阻性图案位于有源柱的侧壁的内部区域处并位于有源柱的基底上。

[0011] 在一些实施例中，可变电阻性图案是中空结构，该中空结构包括位于有源柱的侧壁的内部区域处的侧壁。

[0012] 在一些实施例中，有源柱是包括侧壁和基底的杯形结构，且其中有源柱的侧壁包括第一和第二有源层。

Micron Ex. 1002, p. 130
Micron v. YMTC
IPR2024-00793

[0013] 在一些实施例中，半导体器件还包括在有源柱和衬底之间的单晶材料的焊盘。

[0014] 在一些实施例中，单晶材料的焊盘具有与有源柱的外侧壁对齐的外侧壁。

[0015] 在一些实施例中，有源柱的底部接触衬底且其中电阻性图案的底部在垂直方向上与有源柱的底部间隔开。

[0016] 在一些实施例中，电阻性图案在水平方向上具有小于 20nm 的厚度。

[0017] 在一些实施例中，可变电阻性图案是具有侧壁的中空结构，且其中有源柱位于可变电阻性图案的侧壁的内部区域处。

[0018] 在一些实施例中，半导体器件还包括：衬底上的多个层间介电层；多个栅极图案，每个栅极图案都位于邻近的下层间介电层和邻近的上层间介电层之间；其中有源柱和可变电阻性图案在垂直方向上延伸穿过多个层间介电层和多个栅极图案；其中：多个栅极图案的最上栅极图案包括上选择晶体管的上选择栅极；多个栅极图案的最下栅极图案包括下选择晶体管的下选择栅极；且上选择栅极和下选择栅极之间的多个栅极图案的剩余栅极图案包括半导体器件的单元串的存储器单元晶体管的控制栅极；且其中半导体器件包括半导体存储器器件。

[0019] 在一些实施例中：连接在半导体器件的第一水平方向上排列的共享所述半导体存储器器件的同一层的存储器单元晶体管的控制栅极，以提供半导体存储器器件的字线；半导体器件的单元串的存储器单元晶体管通过垂直沟道串联耦合在一起；且连接在半导体器件的第二水平方向上排列的垂直沟道的上部，以提供半导体存储器器件的位线。

[0020] 在一些实施例中：最上栅极图案包括第一和第二最上栅极图案，第一和第二最上栅极图案用于半导体存储器器件的第一和第二上选择晶体管的第一和第二上选择栅极；且最下栅极图案包括第一和第二最下栅极图案，第一和第二最下栅极图案用于半导体存储器器件的第一和第二下选择晶体管的第一和第二下选择栅极。

[0021] 在一些实施例中：有源柱在水平方向上相邻于上选择晶体管的上选择栅极、下选择晶体管的下选择栅极以及存储器单元晶体管的控制栅极；且可变电阻性图案在水平方向上相邻于存储器单元晶体管的控制栅极且在水平方向上不相邻于上选择晶体管的上选择栅极和下选择晶体管的下选择栅极。

[0022] 在一些实施例中，半导体器件还包括位于有源柱和衬底之间的单晶材料的焊盘。

[0023] 在一些实施例中：有源柱在水平方向上相邻于上选择晶体管的上选择栅极、下选择晶体管的下选择栅极以及存储器单元晶体管的控制栅极；且可变电阻性图案在水平方向上相邻于存储器单元晶体管的控制栅极以及下选择晶体管的下选择栅极，且在水平方向上不相邻于上选择晶体管的上选择栅极。

[0024] 在一些实施例中，可变电阻性图案是具有侧壁的中空结构，且其中有源柱位于可变电阻性图案的侧壁的内部区域处。

[0025] 在一些实施例中，半导体器件还包括在有源柱和衬底之间的单晶材料的焊盘，其中：单晶材料的焊盘在水平方向上相邻于下选择晶体管的下选择栅极；有源柱在水平方向上相邻于存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性图案在水平方向上相邻于存储器单元晶体管的控制栅极，且在水平方向上不相邻于下选择晶体管的下选择栅极和上选择晶体管的上选择栅极。

[0026] 在一些实施例中，半导体器件还包括在有源柱和衬底之间的单晶材料的焊盘，其

Micron Ex. 1002, p. 131
Micron v. YMTC
IPR2024-00793

中：单晶材料的焊盘在水平方向上相邻于下选择晶体管的下选择栅极；有源柱在水平方向上相邻于存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性图案在水平方向上相邻于存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极，且在水平方向上不相邻于下选择晶体管的下选择栅极。

[0027] 在一些实施例中：有源柱在水平方向上相邻于下选择晶体管的下选择栅极、存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性图案在水平方向上相邻于存储器单元晶体管的控制栅极，且在水平方向上不相邻于下选择晶体管的下选择栅极和上选择晶体管的上选择栅极。

[0028] 在一些实施例中：有源柱在水平方向上相邻于下选择晶体管的下选择栅极、存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性图案在水平方向上相邻于存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极，且在水平方向上不相邻于下选择晶体管的下选择栅极。

[0029] 在一些实施例中：有源柱在水平方向上相邻于下选择晶体管的下选择栅极、存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性图案在水平方向上相邻于下选择晶体管的下选择栅极以及存储器单元晶体管的控制栅极，且在水平方向不相邻于上选择晶体管的上选择栅极。

[0030] 根据一些实施例，半导体器件包括：在水平方向上延伸的半导体材料的衬底；衬底上的多个层间介电层；多个栅极图案，每个栅极图案都位于邻近的下层间介电层和邻近的上层间介电层之间；在衬底上并在垂直方向上延伸穿过多个层间介电层和多个栅极图案的半导体材料的垂直沟道；以及沿半导体材料的垂直沟道的可变电阻性材料的垂直沟道；其中可变电阻性材料的垂直沟道具有响应于其氧化和还原的可变电阻。

[0031] 在一些实施例中，垂直沟道中的电流是双向的，在半导体器件的编程操作过程中的电流的第一方向，以及在半导体器件的擦除操作过程中相反于第一方向的电流的第二方向。

[0032] 在一些实施例中：多个栅极图案的最上栅极图案包括上选择晶体管的上选择栅极；多个栅极图案的最下栅极图案包括下选择晶体管的下选择栅极；在上选择栅极和下选择栅极之间的多个栅极图案的剩余栅极图案包括半导体器件的单元串的存储器单元晶体管的控制栅极；连接在半导体器件的第一水平方向上排列的共享所述半导体存储器器件的同一层的存储器单元晶体管的控制栅极，以提供半导体器件的字线；半导体器件的单元串的存储器单元晶体管通过垂直沟道串联耦合在一起；连接在半导体器件的第二水平方向上排列的半导体材料的垂直沟道的上部，以提供半导体器件的位线；且半导体器件包括半导体存储器器件。

[0033] 在一些实施例中，在衬底和半导体材料的垂直沟道的上部之间，沿着半导体材料的垂直沟道存在电流通路，且其中下选择晶体管和上选择晶体管控制电流通路的操作。

[0034] 在一些实施例中，半导体材料的垂直沟道具有内侧壁和外侧壁。

[0035] 在一些实施例中，可变电阻性材料的垂直沟道位于半导体材料的垂直沟道的内侧壁处。

[0036] 在一些实施例中，可变电阻性材料的垂直沟道位于半导体材料的垂直沟道的外侧壁处。

Micron Ex. 1002, p. 132
Micron v. YMTC
IPR2024-00793

[0037] 在一些实施例中，半导体材料的垂直沟道是包括侧壁和基底的杯形结构。

[0038] 在一些实施例中，可变电阻性材料的垂直沟道是包括侧壁和基底的杯形结构。

[0039] 在一些实施例中，可变电阻性材料的垂直沟道位于半导体材料的垂直沟道的侧壁的内部区域处且位于半导体材料的垂直沟道的基底上。

[0040] 在一些实施例中，可变电阻性材料的垂直沟道是中空结构，该中空结构包括位于半导体材料的垂直沟道的侧壁的内部区域处的侧壁。

[0041] 在一些实施例中，半导体材料的垂直沟道是包括侧壁和基底的杯形结构，且其中半导体材料的垂直沟道的侧壁包括第一和第二有源层。

[0042] 在一些实施例中，半导体器件还包括在半导体材料的垂直沟道和衬底之间的单晶材料的焊盘。

[0043] 在一些实施例中，单晶材料的焊盘具有与半导体材料的垂直沟道的外侧壁对齐的外侧壁。

[0044] 在一些实施例中，半导体材料的垂直沟道的底部接触衬底，且其中可变电阻性材料的垂直沟道的底部在垂直方向上与半导体材料的垂直沟道的底部间隔开。

[0045] 在一些实施例中，可变电阻性材料的垂直沟道在水平方向上具有小于 20nm 的厚度。

[0046] 在一些实施例中，可变电阻性材料的垂直沟道是具有侧壁的中空结构，且其中半导体材料的垂直沟道位于可变电阻性材料的垂直沟道的侧壁处的内部区域。

[0047] 在一些实施例中：多个栅极图案的最上栅极图案包括上选择晶体管的上选择栅极；多个栅极图案的最下栅极图案包括下选择晶体管的下选择栅极；并且在上选择栅极和下选择栅极之间的多个栅极图案的剩余栅极图案包括半导体器件的单元串的存储器单元晶体管的控制栅极；且半导体器件包括半导体存储器器件。

[0048] 在一些实施例中：连接在半导体器件的第一水平方向上排列的共享所述半导体存储器器件的同一层的存储器单元晶体管的控制栅极，以提供半导体器件的字线；半导体器件的单元串的存储器单元晶体管通过垂直沟道串联耦合在一起；且连接在半导体器件的第二水平方向上排列的半导体材料的垂直沟道的上部，以提供半导体存储器器件的位线。

[0049] 在一些实施例中：最上栅极图案包括第一和第二最上栅极图案，第一和第二最上栅极图案用于半导体存储器器件的第一和第二上选择晶体管的第一和第二上选择栅极；且最下栅极图案包括第一和第二最下栅极图案，第一和第二最下栅极图案用于半导体存储器器件的第一和第二下选择晶体管的第一和第二下选择栅极。

[0050] 在一些实施例中：半导体材料的垂直沟道在水平方向上相邻于上选择晶体管的上选择栅极、下选择晶体管的下选择栅极以及存储器单元晶体管的控制栅极；且可变电阻性材料的垂直沟道在水平方向上相邻于存储器单元晶体管的控制栅极，且在水平方向上不相邻于上选择晶体管的上选择栅极和下选择晶体管的下选择栅极。

[0051] 在一些实施例中，半导体器件还包括在半导体材料的垂直沟道和衬底之间的单晶材料的焊盘。

[0052] 在一些实施例中：半导体材料的垂直沟道在水平方向上相邻于上选择晶体管的上选择栅极、下选择晶体管的下选择栅极以及存储器单元晶体管的控制栅极；且可变电阻性材料的垂直沟道在水平方向上相邻于存储器单元晶体管的控制栅极以及下选择晶体管的

Micron Ex. 1002, p. 133
Micron v. YMTC
IPR2024-00793

下选择栅极，且在水平方向上不相邻于上选择晶体管的上选择栅极。

[0053] 在一些实施例中，可变电阻性材料的垂直沟道是具有侧壁的中空结构，且其中半导体材料的垂直沟道位于可变电阻性材料的垂直沟道的侧壁的内部区域处。

[0054] 在一些实施例中，半导体器件还包括在半导体材料的垂直沟道和衬底之间的单晶材料的焊盘，其中：单晶材料的焊盘在水平方向上相邻于下选择晶体管的下选择栅极；半导体材料的垂直沟道在水平方向上相邻于存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性材料的垂直沟道在水平方向上相邻于存储器单元晶体管的控制栅极，且在水平方向上不相邻于下选择晶体管的下选择栅极和上选择晶体管的上选择栅极。

[0055] 在一些实施例中，半导体器件还包括：在半导体材料的垂直沟道和衬底之间的单晶材料的焊盘，其中：单晶材料的焊盘在水平方向上相邻于下选择晶体管的下选择栅极；半导体材料的垂直沟道在水平方向上相邻于存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性材料的垂直沟道在水平方向上相邻于存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极，且在水平方向上不相邻于下选择晶体管的下选择栅极。

[0056] 在一些实施例中：半导体材料的垂直沟道在水平方向上相邻于下选择晶体管的下选择栅极、存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性材料的垂直沟道在水平方向上相邻于存储器单元晶体管的控制栅极，且在水平方向上不相邻于下选择晶体管的下选择栅极和上选择晶体管的上选择栅极。

[0057] 在一些实施例中：半导体材料的垂直沟道在水平方向上相邻于下选择晶体管的下选择栅极、存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性材料的垂直沟道在水平方向上相邻于存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极，且在水平方向不相邻于下选择晶体管的下选择栅极。

[0058] 在一些实施例中：半导体材料的垂直沟道在水平方向上相邻于下选择晶体管的下选择栅极、存储器单元晶体管的控制栅极以及上选择晶体管的上选择栅极；且可变电阻性材料的垂直沟道在水平方向上相邻于下选择晶体管的下选择栅极以及存储器单元晶体管的控制栅极，且在水平方向上不相邻于上选择晶体管的上选择栅极。

[0059] 根据一些实施例，形成半导体器件的方法包括：在水平方向延伸的衬底上，提供在垂直方向上交替的层间介电层和牺牲层的堆叠；在层间介电层和牺牲层中形成开口；在开口中形成半导体材料的垂直沟道，半导体材料的垂直沟道在垂直方向上延伸；在开口中形成可变电阻性材料的垂直沟道，可变电阻性材料的垂直沟道在垂直方向上延伸，可变电阻性材料的垂直沟道具有响应于可变电阻性材料的氧化或还原的可变电阻；以及以导电图案替代牺牲层。

[0060] 在一些实施例中，在开口中形成半导体材料的垂直沟道包括形成半导体材料的垂直沟道以具有在开口的侧壁处的侧壁。

[0061] 在一些实施例中，在开口中形成可变电阻性材料的垂直沟道包括在半导体材料的垂直沟道的侧壁的内部区域处形成可变电阻性材料的垂直沟道。

[0062] 在一些实施例中，在开口中形成可变电阻性材料的垂直沟道包括形成可变电阻性材料的垂直沟道以具有位于开口的侧壁处的侧壁。

Micron Ex. 1002, p. 134
Micron v. YMTC
IPR2024-00793

[0063] 在一些实施例中，在开口中形成半导体材料的垂直沟道包括在所述可变电阻性材料的垂直沟道的侧壁的内部区域处形成半导体材料的垂直沟道。

[0064] 在一些实施例中，半导体材料的垂直沟道在水平方向上具有小于 20nm 的厚度。

[0065] 在一些实施例中，在开口中形成半导体材料的垂直沟道包括在开口中形成接触衬底的半导体材料的垂直沟道。

[0066] 在一些实施例中，该方法还包括，在开口中形成半导体材料的垂直沟道之前，在开口中在衬底上形成单晶材料的焊盘，以及在开口中在焊盘上形成半导体材料的垂直沟道。

[0067] 根据一些实施例，提供一种控制半导体存储器器件的方法。该半导体存储器器件包括：在水平方向上延伸的半导体材料的衬底；衬底上的多个层间介电层；多个栅极图案，每个栅极图案都位于邻近的下层间介电层和邻近的上层间介电层之间；在衬底上并在垂直方向上延伸穿过多个层间介电层和多个栅极图案的半导体材料的垂直沟道，垂直沟道具有外侧壁和内侧壁；以及位于半导体材料的垂直沟道的内侧壁处的可变电阻性材料的垂直沟道。该方法包括：对多个存储器单元中选定的一个进行选择性编程；以及对多个存储器单元中选定的一个进行选择性擦除；其中对多个存储器单元中选定的一个进行选择性编程包括通过响应于可变电阻性材料的氧化和还原中的一种而改变可变电阻性材料的垂直沟道的电阻来进行编程，且其中对多个存储器单元中选定的一个进行选择性擦除包括通过响应于可变电阻性材料的氧化和还原中的另一种而改变可变电阻性材料的垂直沟道的电阻来进行擦除。

[0068] 在一些实施例中，半导体材料的垂直沟道中的电流是双向的，在半导体器件的选择性编程过程中的电流的第一方向，以及在半导体器件的选择性擦除过程中的相反于第一方向的电流的第二方向。

[0069] 在一些实施例中：多个栅极图案的最上栅极图案包括上选择晶体管的上选择栅极；多个栅极图案的最下栅极图案包括下选择晶体管的下选择栅极；在上选择栅极和下选择栅极之间的多个栅极图案的剩余栅极图案包括半导体器件的单元串的存储器单元晶体管的控制栅极；连接在半导体器件的第一水平方向上排列的共享所述半导体存储器器件的同一层的存储器单元晶体管的控制栅极，以提供半导体器件的字线；半导体器件的单元串的存储器单元晶体管通过半导体材料的垂直沟道串联耦合在一起；连接在半导体器件的第二水平方向上排列的半导体材料的垂直沟道的上部，以提供半导体器件的位线；且半导体器件包括半导体存储器器件。

[0070] 在一些实施例中，存储器单元晶体管的页包括在同一控制栅极控制下的存储器单元晶体管，且其中选择性编程多个存储器单元中的至少一个包括小于存储器单元晶体管的页地进行择性编程。

[0071] 在一些实施例中，存储器单元晶体管的页包括在同一控制栅极控制下的存储器单元晶体管，且其中选择性擦除多个存储器单元中的至少一个包括小于存储器单元晶体管的页地进行选择性擦除。

[0072] 在一些实施例中，选择性编程包括：对衬底施加低电压；对多个存储器单元中选定的一个的半导体材料的垂直沟道所连接到的位线施加设定电压；对与多个存储器单元中未被选定的存储器单元相关联的字线施加激活电压；以及对与多个存储器单元中选定的一个相关联的字线施加去活电压。

Micron Ex. 1002, p. 135
Micron v. YMTC
IPR2024-00793

[0073] 在一些实施例中，选择性擦除包括：对衬底施加复位电压；对多个存储器单元中选定的一个的半导体材料的垂直沟道所连接到的位线施加低电压；对与多个存储器单元中未被选定的存储器单元相关联的字线施加激活电压；以及对与多个存储器单元中选定的一个相关联的字线施加去活电压。

[0074] 在一些实施例中，选择性擦除包括：对衬底施加低电压；对多个存储器单元中选定的一个的半导体材料的垂直沟道所连接到的位线施加感测电压；对与多个存储器单元中未被选定的存储器单元相关联的字线施加激活电压；以及对与多个存储器单元中选定的一个相关联的字线施加去活电压。

[0075] 根据一些实施例，一种存储器系统包括：产生命令和地址信号的存储器控制器；以及包括多个存储器器件的存储器模块，存储器模块接收命令和地址信号并响应地将数据存储到至少一个存储器器件和从至少一个存储器器件中调取数据。每个存储器器件都包括：在水平方向上延伸的衬底；在衬底上相对于衬底的水平延伸方向在垂直方向上延伸的有源柱；在衬底上沿有源柱在垂直方向上延伸的可变电阻性图案，可变电阻性图案的电阻响应于其氧化或还原而改变；以及位于有源柱的侧壁处的栅极。

[0076] 根据一些实施例，电阻性 RAM 器件包括衬底、布置在衬底上具有中空结构的有源柱、接触有源柱的可变电阻性图案以及布置为相邻于有源柱的侧壁的栅极。可变电阻性图案的电阻通过其氧化或还原而改变。

[0077] 在一些实施例中，电阻性 RAM 器件还可以包括填充有源柱的内部空间的掩埋绝缘图案。在这种情况下，可变电阻性图案可布置在有源柱和掩埋绝缘图案之间。

[0078] 在一些实施例中，有源柱可具有约 50 纳米以下的厚度。

[0079] 在一些实施例中，电阻性 RAM 器件还可以包括在有源柱和栅极之间的栅极绝缘层。在这种情况下，可变电阻性图案可布置在栅极绝缘层和有源柱之间。

[0080] 在一些实施例中，可变电阻性图案可具有 20 纳米以下的厚度。

[0081] 在一些实施例中，相邻于栅极的可变电阻性图案的电阻可以根据位于栅极两侧的有源柱中产生的第一和第二场效应源 / 漏区之间的电压差以及施加至相邻于栅极的可变电阻性图案的电场的方向而改变。

[0082] 在一些实施例中，可变电阻性图案可包括过渡金属氧化物层。

[0083] 在一些实施例中，可变电阻性图案可包括选自锆（Zr）、铪（Hf）、铝（Al）、镍（Ni）、铜（Cu）、钼（Mo）、钽（Ta）、钛（Ti）、钨（W）、铬（Cr）、锶（Sr）、镧（La）、锰（Mn）、钙（Ca）、镨（Pr）和硅（Si）构成的组中的至少一种元素的氧化物材料。

[0084] 在一些实施例中，电阻性 RAM 器件还可以包括在衬底和有源柱之间的有源焊盘。

[0085] 在一些实施例中，可变电阻性图案可包括具有可变电阻性质的开关层以及接触开关层以与开关层交换氧原子的氧交换层。

[0086] 在一些实施例中，开关层和氧交换层中的至少一个可以包括具有非化学计量组分的过渡金属氧化物层。

[0087] 在一些实施例中，可变电阻性图案还可以包括接触有源柱的隧道势垒层。

[0088] 在一些实施例中，隧道势垒层可包括具有化学计量组分的过渡金属氧化物层。

[0089] 在一些实施例中，开关层和氧交换层可包括同一过渡金属氧化物层，且隧道势垒层可包括不同于开关层和氧交换层的过渡金属氧化物层。

Micron Ex. 1002, p. 136
Micron v. YMTC
IPR2024-00793

[0090] 在一些实施例中，隧道势垒层可薄于开关层和氧交换层中的至少一个。

[0091] 根据另外的实施例，电阻性 RAM 器件包括衬底、从衬底突出并具有中空结构的有源柱、相邻于有源柱的下侧壁的下选择栅极、相邻于有源柱的上侧壁的上选择栅极、布置在下选择栅极和上选择栅极之间相邻于有源柱的中部侧壁的多个单元栅极，以及接触有源柱相邻于多个单元栅极的可变电阻性图案。可变电阻性图案的电阻通过其氧化或还原而改变。

[0092] 在一些实施例中，可变电阻性图案可延伸到相邻于下选择栅极和上选择栅极中的至少一个。

[0093] 在一些实施例中，在多个单元栅极之间的第一距离可以小于在上选择栅极和最上单元栅极之间的第二距离以及在下选择栅极和最下单元栅极之间的第三距离中的至少一个。

[0094] 在一些实施例中，下选择栅极和上选择栅极中的至少一个可包括多个子选择栅极。

[0095] 在一些实施例中，电阻性 RAM 器件还可以包括布置在衬底和有源柱之间的有源焊盘。下选择栅极可相邻于有源焊盘的侧壁。

[0096] 在一些实施例中，电阻性 RAM 器件还可以包括填充有源柱的内部空间的掩埋绝缘图案。在这种情况下，可变电阻性图案可布置在有源柱和掩埋绝缘图案之间。

[0097] 在一些实施例中，有源柱可具有约 50 纳米以下的厚度。

[0098] 在一些实施例中，电阻性 RAM 器件还可以包括在有源柱和单元栅极之间的栅极绝缘层。在这种情况下，可变电阻性图案可布置在栅极绝缘层和有源柱之间。

[0099] 在一些实施例中，可变电阻性图案可具有 20 纳米以下的厚度。

[0100] 在一些实施例中，相邻于从多个单元栅极中选定的一个的可变电阻性图案的电阻可以根据位于选定的单元栅极两侧的有源柱中产生的第一和第二场效应源 / 漏区之间的电压差以及施加至相邻于选定的栅极的可变电阻性图案的电场的方向而改变。

[0101] 在一些实施例中，电阻性 RAM 器件还可以包括布置在衬底中的公共源线以及电连接至公共源线的至少一个虚位线。

[0102] 在一些实施例中，电阻性 RAM 器件还可以包括在有源柱的基底部和可变电阻性图案的底面之间的第一空间中布置的至少一个下掩埋绝缘图案，以及在可变电阻性图案的顶面上的第二空间中布置的上掩埋绝缘图案。第一和第二空间可位于有源柱的内部空间中。

[0103] 根据另外的实施例，在操作电阻性 RAM 器件的方法中，电阻性 RAM 器件包括衬底、从衬底突出的有源柱以及包括有源柱的单元串。单元串包括相邻于有源柱的下侧壁的下选择元件、相邻于有源柱的上侧壁的上选择元件，以及相邻于有源柱在下选择元件和上选择元件之间布置的多个存储器单元。每个存储器单元都包括单元晶体管和可变电阻性层，且可变电阻性层接触有源柱。该方法包括选择性编程多个存储器单元中的一个，以及擦除所编程的存储器单元。通过还原或氧化可变电阻性层以改变可变电阻性层的电阻来执行选择性编程或擦除多个存储器单元中的一个。

[0104] 在一些实施例中，可通过在选定的存储器单元的单元晶体管的源和漏区之间产生电压差，以及通过改变施加至相邻于选定的存储器单元的可变电阻性图案的电场的方向，来执行选择性编程或擦除组成单元串的多个存储器单元中的一个。

Micron Ex. 1002, p. 137
Micron v. YMTC
IPR2024-00793

[0105] 在一些实施例中，选定的存储器单元的单元晶体管可在编程操作和擦除操作过程中截止。

[0106] 在一些实施例中，编程操作可在选定的存储器单元的单元晶体管的源区和漏区之间的可变电阻性层中形成电流通路。

[0107] 在一些实施例中，擦除操作可移除选定的存储器单元的单元晶体管的源区和漏区之间的可变电阻性层中形成的电流通路。

[0108] 在一些实施例中，单元串可以是第一单元串，且电阻性 RAM 器件还可以包括多个附加单元串、电连接至单元串的有源柱的上部的多个位线、电连接至单元串的有源柱的下部的公共源线以及电连接至公共源线的虚位线对。附加单元串的每一个都可以具有与第一单元串相同的构造。多个位线可布置在虚位线对之间。同时对其施加编程电压或擦除电压的位线的数量可小于在虚位线对之间布置的位线的总数量。

[0109] 在一些实施例中，选择性编程多个存储器单元中的一个包括在第一电流方向上迫使电流进入选定的存储器单元的可变电阻性层以降低可变电阻性层的电阻，且擦除所编程的存储器单元可包括在与第一电流方向相反的第二电流方向上迫使电流进入所编程的存储器单元的可变电阻性层以增大可变电阻性层的电阻。

[0110] 根据其他实施例，制造电阻性 RAM 器件的方法包括：在衬底上交替堆叠层间绝缘层和牺牲层、图案化层间绝缘层和牺牲层以形成暴露衬底的有源孔、在有源孔中形成具有中空结构的有源柱以及接触有源柱的可变电阻性图案，以及以导电图案替代牺牲层。通过可变电阻性图案的氧化或还原改变可变电阻性图案的电阻。

[0111] 在一些实施例中，形成有源柱和可变电阻性图案可包括在有源孔中共形地形成有源层，以部分填充有源孔，以及在有源孔中形成至少覆盖有源层的内侧壁的可变电阻性层。

[0112] 在一些实施例中，形成有源柱和可变电阻性图案可包括形成覆盖有源孔的侧壁的可变电阻性层，以及在有源孔中的可变电阻性层的内侧壁上和通过有源孔暴露的衬底上形成有源层。

[0113] 在一些实施例中，该方法还可以包括在形成有源柱之前形成填充有源孔的下部的有源焊盘。

附图说明

[0114] 参考附图和伴随的详细说明将使发明概念变得更加明显。

[0115] 图 1 是示出根据本发明概念的一些实施例的电阻性 RAM 器件的示意电路图。

[0116] 图 2 是示出根据本发明概念的第一实施例的电阻性 RAM 器件的平面图。

[0117] 图 3 是沿图 2 的 I-I’ 线截取的截面图。

[0118] 图 4A、4B 和 4C 是示出图 3 的“P1”部分的放大图。

[0119] 图 5A 是示出根据本发明概念，对根据第一实施例的电阻性 RAM 器件进行编程时的图 3 的“P1”部分的放大图。

[0120] 图 5B 是示出根据本发明概念，对根据第一实施例的电阻性 RAM 器件进行擦除时的图 3 的“P1”部分的放大图。

[0121] 图 6 示出根据本发明概念的一些实施例的电阻性 RAM 器件中的电流。

[0122] 图 7 是示出根据本发明概念的其他实施例的电阻性 RAM 器件的示意电路图。

Micron Ex. 1002, p. 138
Micron v. YMTC
IPR2024-00793

[0123] 图 8 至图 15 是示出根据本发明概念制造图 3 中所示的电阻性 RAM 器件的方法的截面图。

[0124] 图 16 是示出根据本发明概念的第二实施例的电阻性 RAM 器件的截面图。

[0125] 图 17 是示出根据本发明概念的第三实施例的电阻性 RAM 器件的截面图。

[0126] 图 18、19 和 20 是示出根据本发明概念制造图 17 中所示的电阻性 RAM 器件的方法的截面图。

[0127] 图 21 是示出根据本发明概念的第四实施例的电阻性 RAM 器件的截面图。

[0128] 图 22、23 和 24 是示出根据本发明概念制造图 21 中所示的电阻性 RAM 器件的方法的截面图。

[0129] 图 25 是示出根据本发明概念的第五实施例的电阻性 RAM 器件的截面图。

[0130] 图 26 是示出根据本发明概念制造图 25 中所示的电阻性 RAM 器件的方法的截面图。

[0131] 图 27 是示出根据本发明概念的第六实施例的电阻性 RAM 器件的截面图。

[0132] 图 28、29、30 和 31 是示出根据本发明概念制造图 27 中所示的电阻性 RAM 器件的方法的截面图。

[0133] 图 32 是示出根据本发明概念的第七实施例的电阻性 RAM 器件的截面图。

[0134] 图 33 是示出根据本发明概念的第八实施例的电阻性 RAM 器件的截面图。

[0135] 图 34 和 35 是示出根据本发明概念制造图 33 中所示的电阻性 RAM 器件的方法的截面图。

[0136] 图 36 是示出根据本发明概念的第九实施例的电阻性 RAM 器件的截面图。

[0137] 图 37 是示出根据本发明概念的第十实施例的电阻性 RAM 器件的截面图。

[0138] 图 38 是示出根据本发明概念的第十一实施例的电阻性 RAM 器件的截面图。

[0139] 图 39 是示出根据本发明概念，对根据第十一实施例的电阻性 RAM 器件进行编程时的图 38 的“P2”部分的放大图。

[0140] 图 40 是示出根据本发明概念，对根据第十一实施例的电阻性 RAM 器件进行擦除时的图 38 的“P2”部分的放大图。

[0141] 图 41、42、43、44 和 45 是示出根据第十一实施例的一些变型实施例的电阻性 RAM 器件的截面图。

[0142] 图 46 是示出包括根据本发明概念的一些实施例的电阻性 RAM 器件的存储器系统的示例的示意框图。

[0143] 图 47 是示出包括根据本发明概念的一些实施例的电阻性 RAM 器件的存储卡的示例的示意框图。

[0144] 图 48 是示出包括根据本发明概念的一些实施例的电阻性 RAM 器件的信息处理系统的示例的示意框图。

具体实施方式

[0145] 现在将参考附图更全面说明发明概念的示例性实施例，在附图中示出了示例性实施例的示例。但是发明概念的示例性实施例可以以多种不同方式实施且不应被理解为限于本文所阐述的实施例，而是提供这些实施例以便使本公开内容全面和完整，并将示例性实

Micron Ex. 1002, p. 139
Micron v. YMTC
IPR2024-00793

施例的概念全面传达给本领域技术人员。在附图中，出于清楚的目的，放大了层和区域的厚度。附图中相同的附图标记表示相同的要素且因此将省略其说明。

[0146] 本文所用术语仅用于说明特定实施例的目的且不旨在限制发明概念。如本文所用，单数术语“一”、“该”旨在也包括复数形式，除非上下文另外明示。还应理解的是，当本文中使用术语“包括”和 / 或“包含”时，规定存在所述的特征、整体、步骤、操作、元件和 / 或部件，但不排除存在或加入一个或更多的其他特征、整体、步骤、操作、元件、部件和 / 或其组合。类似地，还应理解的是，当诸如层、区域或衬底的元件被称为位于另一元件“上”时，其可直接位于其他元件上或可存在中间的元件。相反，术语“直接”是指不存在中间的元件。如本文所用，术语“和 / 或”包括一个或多个相关列出的条目的任意和全部的组合。

[0147] 此外，具体实施方式中的实施例将以截面图和 / 或平面图作为发明概念的理想示例性图示进行说明。在附图中，出于清楚说明的考虑，可放大层和区域的尺寸。因此，示例性图示的形状可根据制造技术和 / 或容许误差而改变。因此，发明概念的实施例不限于示例性图示中所示的特定形状，而是可包括根据制造工艺可以创建的其他形状。例如，示出为矩形的蚀刻区可具有圆形或曲线特征。因此，附图中所示的区域实质上是示意性的，且它们的形状不旨在说明器件的区域的实际形状，且不旨在限制示例性实施例的范围。

[0148] 以下将参考附图更全面说明示例性实施例。根据示例性实施例的非易失性存储器包括三维电阻性 RAM 器件。

[0149] < 第一实施例 >

[0150] 图 1 是示出根据本发明概念的一些实施例的电阻性 RAM 器件的示意电路图，且图 2 是示出根据第一实施例的电阻性 RAM 器件的平面图。而且，图 3 是沿图 2 的 I-I’ 线截取的截面图。

[0151] 参考图 1、2 和 3，根据示例性实施例的电阻性 RAM 器件包括公共源线 CSL、位线 BL1、BL2 和 BL3，以及布置在公共源线 CSL 和位线 BL1、BL2 和 BL3 之间的单元串 CSTR。

[0152] 在一些实施例中，公共源线 CSL 可布置在衬底 1 中或衬底 1 上。在各种实施例中，衬底 1 可包括半导体衬底或布置在半导体衬底上的外延层。公共源线 CSL 可包括布置在衬底 1 中的杂质区。公共源线 CSL 可具有与衬底 1 不同的导电类型。在一些实施例中，当衬底 1 掺杂 P 型杂质时，公共源线 CSL 可掺杂 N 型杂质。

[0153] 有源柱 32 可在第一方向 L1 上从衬底 1 突出。例如，有源柱可在相对于衬底 1 的水平延伸方向的垂直方向上延伸。在一些实施例中，诸如结合本实施例所描述的，有源柱 32 可具有中空结构，例如具有侧壁和基底的杯形。在一些实施例中，有源柱 32 可接触衬底 1。每个有源柱 32 都可以包括 P 型多晶硅材料或非掺杂多晶硅材料。在有源柱 32 具有中空结构的构造中，有源柱 32 的侧壁可形成得非常薄。例如，侧壁可形成为具有约 50 纳米以下的厚度。在有源柱 32 具有上述薄侧壁的这种布置中，电场可在电阻性 RAM 器件的操作过程中被有效和 / 或高效地施加至相邻于有源柱 32 的侧壁的可变电阻性层 34。

[0154] 漏区 D 可布置在有源柱 32 的相应的上部中。在一些实施例中，漏区 D 可具有与公共源线 CSL 相同的导电类型。

[0155] 在一些实施例中，位线 BL1、BL2 和 BL3 可布置在有源柱 32 上并电连接至漏区 D。位线 BL1、BL2 和 BL3 可在水平延伸方向，即在水平第二方向 L2 上延伸以定位为彼此平行，且可彼此间隔。

Micron Ex. 1002, p. 140
Micron v. YMTC
IPR2024-00793

[0156] 第一组单元串 CSTR 可并联连接到位线 BL1，且第二组单元串 CSTR 可并联连接到位线 BL2。此外，第三组单元串 CSTR 可并联连接到位线 BL3。单元串 CSTR 可并联电连接到具有基本上相同电势的公共源线 CSL 的至少一个。

[0157] 每个单元串 CSTR 都可配置为包括有源柱 32 中的一个。在一些实施例中，每个单元串 CSTR 都可包括：下选择晶体管 LST，下选择晶体管 LST 的栅极可被连接至一个公共源线 CSL；上选择晶体管 UST，被连接至位线 BL1、BL2 和 BL3 中的一个；以及多个存储器单元 MC，被布置在上选择晶体管 UST 和下选择晶体管 LST 之间。在每个单元串 CSTR 中，下选择晶体管 LST、多个存储器单元 MC 以及上选择晶体管 UST 都可以沿电流通路串联电连接。在每个单元串 CSTR 中，有源柱 32 可提供下选择晶体管 LST、多个存储器单元 MC 以及上选择晶体管 UST 的沟道区。

[0158] 上选择晶体管 UST 的栅电极可延伸以提供上选择线 USL1、USL2 和 USL3。上选择晶体管 UST 可位于距衬底 1 基本上相同的距离。上选择线 USL1、USL2 和 USL3 可在水平延伸方向，即第三方向 L3 上延伸，以便彼此平行。在一些实施例中，第一、第二和第三方向 L1、L2 和 L3 可彼此正交。

[0159] 下选择晶体管 LST 的栅电极可延伸以提供下选择线 LSL1、LSL2 和 LSL3。下选择晶体管 LST 可位于距衬底 1 基本上相同的距离。下选择线 LSL1、LSL2 和 LSL3 可在第三方向 L3 上延伸，以便彼此平行。

[0160] 每个存储器单元 MC 都可以包括单元晶体管 CT 和可变电阻性层 34。组成存储器单元 MC 的单元晶体管 CT 的栅极可延伸以提供字线 WL1、WL2、WL3 和 WL4。每个单元晶体管 CT 都可以包括形成在有源柱 32 的两部分中的电场效应源区和电场效应漏区，它们位于字线 WL1、WL2、WL3 和 WL4 中对应的一个的两侧。位于相对于衬底 1 相同的垂直高度，或者换言之，位于器件的相同层的不同单元串 CSTR 的单元晶体管 CT 的栅极可彼此电连接以组成字线 WL1、WL2、WL3 和 WL4 中的一个。包括相同字线且由此连接的栅极在被施加电压时具有相同的电势。在一些实施例中，字线 WL1、WL2、WL3 和 WL4 通常可为线性形状且可在第三方向 L3 上延伸。在一些实施例中，字线 WL1、WL2、WL3 和 WL4 通常可为平面形状且在第二方向 L2 和第三方向 L3 二者上延伸。

[0161] 在一些实施例中，所有下选择晶体管 LST、上选择晶体管 UST 和单元晶体管 CT 中的一些可被配置为采用有源柱 32 作为沟道区的金属氧化物半导体场效应晶体管（MOSFET）。

[0162] 在一些实施例中，可变电阻性层 34 可直接接触相应的有源柱 32 的内表面。由可变电阻性层 34 包围的内部空间或区域可包括掩埋绝缘图案 36。在一些实施例中，掩埋绝缘图案 36 可包括氧化硅型材料。可变电阻性层 34 可被布置在掩埋绝缘图案 36 和有源柱 32 之间。但是，在其他将在本文中说明的实施例中，可变电阻性层 34 的其他位置也是可能的。在本实施例中，每个可变电阻性层 34 都具有覆盖有源柱 32 中的一个的内底面和内侧壁的杯形。但是，在其他将在本文中说明的实施例中，可变电阻性层 34 的其他形状也是可能的。

[0163] 图 4A、4B 和 4C 是示出图 3 的部分“P1”的放大图。

[0164] 参考图 4A，在一些实施例中，可变电阻性层 34 可包括单一开关层。可变电阻性层 34 的电阻率可根据施加至可变电阻性层 34 的电场的方向和强度和 / 或施加在可变电阻性层 34 两端之间的电压差而改变。例如，可变电阻性层 34 的电阻可根据施加在包括了可变电阻性层 34 的单元晶体管 CT 的场效应源区和场效应漏区之间的电压差而改变。

Micron Ex. 1002, p. 141
Micron v. YMTC
IPR2024-00793

[0165] 在一些实施例中，可变电阻性层 34 可包括过渡金属氧化物层。可变电阻性层 34 可包括选自由锆（Zr）、铪（Hf）、铝（Al）、镍（Ni）、铜（Cu）、钼（Mo）、钽（Ta）、钛（Ti）、钨（W）、铬（Cr）、锶（Sr）、镧（La）、锰（Mn）、钙（Ca）、镨（Pr）和硅（Si）组成的组中的至少一种元素的氧化物材料。但是，可变电阻性层 34 可具有非化学计量组分。例如，当可变电阻性层 34 是过渡金属氧化物材料或氧化硅材料时，可变电阻性层 34 的氧含量可以约为其化学计量氧含量的 0.8 倍至 0.9 倍。

[0166] 参考图 4B，可变电阻性层 34 可选地还包括具有可变电阻性质的开关层 34a 以及与开关层 34a 交换氧原子的氧交换层 34b。在一些实施例中，开关层 34a 可被布置在有源柱 32 和氧交换层 34b 之间。开关层 34a 可包括与参考图 4A 说明的可变电阻性层 34 相同的材料层。即，可根据施加在包括了开关层 34a 的单元晶体管 CT 的场效应源区和场效应漏区之间的电压差（或根据所施加的电场的方向和强度）而在开关层 34a 中产生或从该层中移除采取导电细丝形式的电流通路。因此，开关层 34a 的电阻可在导电细丝产生在开关层 34a 中时减小，且开关层 34a 的电阻可在导电细丝从开关层 34a 中移除时增大。氧交换层 34b 可被布置为接触开关层 34a。当对包括了开关层 34a 的单元晶体管 CT 进行编程时（例如，当导电细丝产生或存在于开关层 34a 中时），开关层 34a 中的氧原子会移动或迁移进氧交换层 34b 以降低开关层 34a 的电阻。相反，当对包括了开关层 34a 的单元晶体管 CT 进行擦除时（例如，当导电细丝从开关层 34a 中移除或在开关层 34a 中不存在导电细丝时），氧交换层 34b 中的氧原子会移动或迁移进开关层 34a 以增大开关层 34a 的电阻。在一些实施例中，氧交换层 34b 还可以包括具有氧含量低于其化学计量氧含量的过渡金属氧化物层。但是，在其他实施例中，氧交换层 34b 的氧含量可大于开关层 34a 的氧含量。

[0167] 参考图 4C，可变电阻性层 34 可以可选地包括三层材料，该三层材料包括图 4B 中所示的开关层 34a、图 4B 中所示的氧交换层 34b 且还包括接触有源柱 32 的隧道势垒层 34c。在一些实施例中，隧道势垒层 34c 可被布置在有源柱 32 和开关层 34a 之间，且开关层 34a 可被布置在隧道势垒层 34c 和氧交换层 34b 之间。开关层 34a 可包括与参考图 4B 所述相同的材料层，且氧交换层 34b 可包括与参考图 4B 所述相同的材料层。隧道势垒层 34c 可包括氧材料层，该氧材料层包括不同于开关层 34a 中所包含的过渡金属的过渡金属。在一些实施例中，隧道势垒层 34c 在组成上可以比开关层 34a 和氧交换层 34b 更稳定。即，隧道势垒层 34c 中所包含的过渡金属和氧的组成可以具有其化学计量组分。隧道势垒层 34c 可用于防止开关层 34a 和氧交换层 34b 中的氧原子扩散和 / 或迁移进入与其邻近的有源柱 32。此外，隧道势垒层 34c 可抑制在有源柱 32 和开关层 34a（或氧交换层 34b）之间的物理反应。因此，隧道势垒层 34c 可用作隧穿势垒层。在一些实施例中，隧道势垒层 34c 在水平方向上可薄于开关层 34a 和氧交换层 34b 中的至少一层。

[0168] 在图 4B 和 4C 中所示的实施例的替换实施例中，开关层 34a 和氧交换层 34b 可相对彼此调换位置。此外，在其他实施例中，可变电阻性层 34 可包括交替或随机堆叠的多个开关层 34a、多个氧交换层 34b 以及多个隧道势垒层 34c。因此，在一些实施例中，可存在任意数目的开关层 34a、氧交换层 34b 以及隧道势垒层 34c。

[0169] 再次参考图 1、2 和 3，层间绝缘层 11 至 17 可被布置在位线 BL1、BL2 和 BL3，上选择线 USL1、USL2、USL3，字线 WL1、WL2、WL3 和 WL4，下选择线 LSL1、LSL2 和 LSL3 以及衬底 1 之间。在一些实施例中，层间绝缘层 11 至 17 可包括氧化硅型材料中的一种或其他合适的

Micron Ex. 1002, p. 142
Micron v. YMTC
IPR2024-00793

绝缘性材料。

[0170] 在本文中所述的各种实施例的一个中，栅绝缘层 42 可被布置在有源柱 32 和导电线 USL1-USL3，WL1-WL4 以及 LSL1-LSL3 之间。在一些实施例中，栅绝缘层 42 可包括氧化硅层，且用作栅绝缘层 42 的氧化硅层具有化学计量组分比。即，用作栅绝缘层 42 的氧化硅层的硅与氧的组分可以是 1:2。栅绝缘层 42 可延伸进入线 USL1-USL3、WL1-WL4 和 LSL1-LSL3 与层间绝缘层 11 至 17 之间的水平取向的界面，如图中所示。

[0171] 线 USL1-USL3，WL1-WL4 和 LSL1-LSL3 中的每一个都包括掺杂的多晶硅层和 / 或含金属层。含金属层可包括单一金属层、金属氮化物层和 / 或金属硅化物层。

[0172] 上选择线 USL1、USL2 和 USL3 可通过在第三方向 L3 上或垂直方向上延伸的隔离绝缘图案 46 而彼此分隔，如图 2 和 3 中所示。隔离绝缘图案 46 还可在垂直方向上从衬底 1 延伸。因此，处于相同层的字线 WL1 可通过隔离绝缘图案 46 而彼此分隔，且处于相同层的字线 WL2 可通过隔离绝缘图案 46 而彼此分隔。类似地，处于相同层的字线 WL3 可通过隔离绝缘图案 46 而彼此分隔，且处于相同层的字线 WL4 可通过隔离绝缘图案 46 而彼此分隔。而且，下选择线 LSL1、LSL2 和 LSL3 可通过隔离绝缘图案 46 而彼此分隔。每个隔离绝缘图案 46 例如都可以包括氧化硅层、氮化硅层和 / 或氮氧化硅层，或其他合适的绝缘性材料层。在一些实施例中，隔离绝缘图案 46 可延伸接触衬底 1。在字线 WL1、WL2、WL3 和 WL4 之间的垂直距离 W2 可以小于在上选择线 USL1、USL2 和 USL3 与最上字线 WL4 之间的垂直距离 W1 以及在下选择线 LSL1、LSL2 和 LSL3 与最下字线 WL1 之间的垂直距离 W3 中的至少一个。

[0173] 现在将说明根据一些实施例的电阻性 RAM 器件的编程操作、擦除操作以及读取操作。

[0174] 图 5A 是示出对根据第一实施例的电阻性 RAM 器件进行编程时的图 3 的部分“P1”的放大图，且图 5B 是示出对根据第一实施例的电阻性 RAM 器件进行擦除时的图 3 的部分“P1”的放大图。此外，图 6 示出根据一些实施例的电阻性 RAM 器件中的电流。

[0175] 首先说明编程操作。

[0176] 参考图 1、3 和 5A，在存储器单元 MC 的存储器单元 P1 被选择进行编程的情况下，可以将接地电压或单元晶体管 CT 的次阈值电压施加至连接到所选存储器单元 P1 的栅电极的第三字线 WL3 以截止所选存储器单元 P1 的单元晶体管 CT。此外，可以将电压值大于单元晶体管 CT 的阈值电压的高电压施加至未选择的字线，例如包括了所选存储器单元 P1 的单元串 CSTR（或串块）中的第一、第二和第四字线 WL1、WL2 和 WL4。此外，可以将电压值大于选择晶体管 UST 和 LST 的阈值电压的高电压施加至包括了所选存储器单元 P1 的串块（或单元串 CSTR）中的第一上选择线 USL1 和第一下选择线 LSL1。而且，可以将大于用于在所选存储器单元 P1 的可变电阻性层 34 中产生导电细丝的设定电压（或形成电压）的高电压施加至连接到包括了所选存储器单元 P1 的单元串 CSTR 的第二位线 BL2。而且，可将公共源线 CSL 接地。接地电压可施加至属于未选择串块（未示出）的所有字线、上选择线、下选择线和位线。

[0177] 在上述情况下，包括了所选存储器单元 P1 的单元串 CSTR（或串块）中的未选择的存储器单元 MC 的上选择晶体管 UST、下选择晶体管 LST 以及单元晶体管 CT 可在所选存储器单元 P1 的单元晶体管 CT 截止时导通。此外，由于边缘场效应的操作，场效应源 / 漏区 SD1 和 SD2 可以形成在线 USL1、WL1、WL2、WL3、WL4 和 LSL1 之间的有源柱 32 的部分中。因此，施加至第二位线 BL2 的超过设定电压（或形成电压）的高电压可以被传导至在连接到所选存

Micron Ex. 1002, p. 143
Micron v. YMTC
IPR2024-00793

储器单元P1的第三字线WL3和相邻于所选存储器单元P1的第四字线WL4之间的有源柱32的部分中形成的第一场效应源/漏区SD1，且施加至公共源线CSL的接地电压可以被传导至在连接到所选存储器单元P1的第三字线WL3和相邻于所选存储器单元P1的第二字线WL2之间的有源柱32的部分中形成的第二场效应源/漏区SD2（参见图5A）。因此，大于设定电压（或形成电压）的电压可以被施加在所选存储器单元P1的第一和第二场效应源/漏区SD1和SD2之间，且电流可以在第一电流方向上（例如从第二位线BL2朝向公共源线CSL的方向）流动。因此，可变电阻性层34中包含的过渡金属原子可以迁移进入在有源柱32和可变电阻性层34之间的界面，或者可变电阻性层34中包含的氧原子可以扩散出以减少可变电阻性层34的过渡金属氧化物材料。因此，诸如导电细丝PM的电路径可以形成在第一和第二场效应源/漏区SD1和SD2之间的可变电阻性层34中。导电细丝PM可以在相邻于有源柱32的侧面区域处形成可变电阻性层中，如图5A中所示。因此，包括了导电细丝PM的所选存储器单元MC可以被认为是具有逻辑数据“1”或“开启”状态的已编程单元。导电细丝PM可具有各种形状，且出于说明的容易和方便起见，图5A仅示出导电细丝PM的各种形状中的一种。

[0178] 以下说明擦除操作。

[0179] 参考图1、3和5B，在存储器单元MC的已编程存储器单元P1被选择擦除的情况下，接地电压或单元晶体管CT的次阈值电压可以被施加至连接到所选存储器单元P1的栅电极的第三字线WL3以截止所选存储器单元P1的单元晶体管CT。此外，电压值大于单元晶体管CT的阈值电压的高电压可以被施加至未选择的字线，例如包括了所选存储器单元P1的单元串CSTR（或串块）中的第一、第二和第四字线WL1、WL2和WL4。此外，电压值大于选择晶体管UST和LST的阈值电压的高电压可以被施加至包括了所选存储器单元P1的串块（或单元串CSTR）中的第一上选择线USL1和第一下选择线LSL1。而且，接地电压可以被施加至连接到包括了所选存储器单元P1的单元串CSTR的第二位线BL2，且其他位线可以被浮置，或者复位电压（或形成电压）可以被施加至其他位线。此外，大于所选存储器单元P1的可变电阻性层34的复位电压（或形成电压）的高电压可以被施加至公共源线CSL。接地电压可以被施加至属于未选择串块（未示出）的所有字线、上选择线、下选择线以及位线。

[0180] 在上述偏置情况下，在包括了所选存储器单元P1的单元串CSTR（或串块）中的未选择存储器单元MC的上选择晶体管UST、下选择晶体管LST以及单元晶体管CT可在所选存储器单元P1的单元晶体管CT截止时导通。此外，由于存在边缘场效应，场效应源/漏区SD1和SD2可以形成在线USL1、WL1、WL2、WL3、WL4和LSL1之间的有源柱32的部分中。因此，施加至第二位线BL2的接地电压可以被传导至在连接到所选存储器单元P1的第三字线WL3和相邻于所选存储器单元P1的第四字线WL4之间的有源柱32的部分中形成的第一场效应源/漏区SD1，且施加至公共源线CSL的超过设定电压（或形成电压）的高电压可以被传导至在连接到所选存储器单元P1的第三字线WL3和相邻于所选存储器单元P1的第二字线WL2之间的有源柱32的部分中形成的第二场效应源/漏区SD2（参见图5B）。因此，大于设定电压（或形成电压）的电压可以被施加在所选存储器单元P1的第一和第二场效应源/漏区SD1和SD2之间，且电流可以在相反于第一电流方向的第二电流方向（例如从公共源线CSL朝向第二位线BL2的方向）上流动。因此，导电细丝PM中包含的过渡金属原子可以迁移进入可变电阻性层34中的其他位置，或者可变电阻性层34中包含的氧原子可以在朝

Micron Ex. 1002, p. 144
Micron v. YMTC
IPR2024-00793

向导电细丝 PM 的方向上迁移以氧化导电细丝 PM。因此，可以移除导电细丝 PM，如图 5B 中所示。从中移除了导电细丝 PM 的所选存储器单元 MC 可被认为是具有逻辑数据“0”或“关闭”状态的已擦除单元。

[0181] 可按照存储器单元的页面执行上述编程操作和擦除操作，其中存储器单元的页面由处于同一控制栅极控制下的存储器单元晶体管表示。在一些实施例中，存储器单元的页面被确定为共享所述半导体存储器器件的同一字线的那些单元。在其他实施例中，可以对于少于存储器单元晶体管的页面执行编程和擦除操作。例如，存储器单元的页面可包括共享所述半导体存储器器件的同一层的所有存储器单元，在这种情况下，字线连接至被连接到同一字线的所有存储器单元。

[0182] 对于编程和擦除操作来说，期望仅对单元串的一部分执行上述操作。这是因为在这些操作执行过程中，所选串将吸引电流，且过量的电流将经过公共源线。这继而可以人为地升高公共源线上的电压。通过一次对串的子集进行编程，可减轻或消除这种现象的影响。

[0183] 现在将说明读取操作(或验证操作)。

[0184] 参考图 1、3 和 6，如果选择读取存储器单元 MC 的存储器单元 P1，则可以将接地电压或单元晶体管 CT 的次阈值电压施加至连接到所选存储器单元 P1 的栅电极的第三字线 WL3 以截止所选存储器单元 P1 的单元晶体管 CT。此外，可以将电压值大于单元晶体管 CT 的阈值电压的高电压施加至未选择的字线，例如在包括了所选存储器单元 P1 的单元串 CSTR(或串块)中的第一、第二和第四字线 WL1、WL2 和 WL4。此外，可以将大于选择晶体管 UST 和 LST 的阈值电压的高电压施加至在包括了所选存储器单元 P1 的串块(或单元串 CSTR)中的第一上选择线 USL1 和第一下选择线 LSL1。而且，可以将感测电压施加至连接到包括了所选存储器单元 P1 的单元串 CSTR 的第二位线 BL2，且将其他位线浮置或接地。而且，可将公共源线 CSL 接地。接地电压可施加至属于未选择的串块(未示出)的所有字线、上选择线、下选择线和位线。

[0185] 在上述偏置情况下，没有电流流过所选存储器单元 P1 的单元晶体管 CT。但是在所选存储器单元 P1 是已编程单元的情况下，电流可以流过在所选存储器单元 P1 的可变电阻性层 34 中形成的导电细丝 PM，如图 5A 和 6 的箭头 CF 所示。流过所选存储器单元 P1 的导电细丝 PM 的电流可由连接到第二位线 BL2 的感测放大器感测。因此，所选存储器单元 P1 可被认为是具有逻辑数据“1”的已编程单元。相反，当所选存储器单元 P1 是参考图 5B 所述的擦除单元时，没有电流流过所选存储器单元 P1，因为所选存储器单元 P1 中没有任何导电细丝。在这种情况下，所选存储器单元 P1 可被认为是具有逻辑数据“0”的已擦除单元。

[0186] 如上所述，所选存储器单元 P1 的单元晶体管 CT 在所有编程 / 擦除 / 读取操作过程中总是截止。

[0187] 图 7 是示出根据其他实施例的电阻性 RAM 器件的示意电路图。

[0188] 参考图 7，根据本实施例的电阻性 RAM 器件可以包括直接连接至公共源线 CSL 的虚位线 DBL。N 个位线 BL1、BL2…和 BLn 可被布置在虚位线 DBL 之间的每个块中。虚位线 DBL 可防止或抑制公共源线 CSL 的电压电平在编程 / 擦除操作过程中波动到规定范围之外。当执行编程操作或擦除操作时，编程电压(例如设定电压或形成电压)或擦除电压(例如负设定电压或负形成电压)可同时施加至在每个块中布置的 n 个位线 BL1、BL2…和 BLn 中的 m 个位线 BL1、BL2…BLm。即，在编程操作(或擦除操作)过程中同时对其施加编程电压(或擦除

Micron Ex. 1002, p. 145
Micron v. YMTC
IPR2024-00793

电压）的位线数目可以小于在每个块中布置的位线的总数目。如果编程操作（或擦除操作）过程中同时对其施加编程电压（或擦除电压）的位线数目增加，则流过公共源线 CSL 的电流量也可能在编程操作（或擦除操作）过程中增大。在这种情况下，公共源线 CSL 的电压电平可能严重波动，这继而导致编程错误（或擦除错误）。但是，根据本实施例，同时对其施加编程电压（或擦除电压）的位线数目可以小于在每个块中布置的位线的总数目，如上所述。这可以降低编程错误或擦除错误发生的概率。

[0189] 根据实施例的电阻性 RAM 器件可以包括连接至最上单元晶体管 CT 的上选择晶体管 UST 和连接至最下单元晶体管的下选择晶体管 LST。如果选择晶体管 UST 和 LST 截止，则可最小化流过单元晶体管 CT 的不期望存在的单元泄漏电流。

[0190] 根据实施例的电阻性 RAM 器件采用可变电阻性层 34 作为数据存储元件。鉴于采用电荷捕获层的非易失性存储器器件可能需要约 20 伏特的高编程电压以将电荷注入电荷捕获层，这种数据存储元件的形式与基于电荷捕获层的数据存储元件不同且更具优势。但是，为了对根据实施例的电阻性 RAM 器件进行编程或擦除，可将相对低的电压施加至字线和选择线以导通单元晶体管和选择晶体管，且可将约 5 伏特的相对低的形成电压施加至位线或公共源线。即，可利用专用的相对低的电压对根据实施例的电阻性 RAM 器件进行编程或擦除。因此，根据本文所述实施例的电阻性 RAM 器件无需包括高电压晶体管的高压电路。因此，可在不形成高压区的情况下实现根据实施例的电阻性 RAM 器件的单元阵列区。此外，因为利用相对低的电压操作根据实施例的电阻性 RAM 器件，因此可减小在字线 WL1、WL2、WL3 和 WL4 之间的间隔或距离。因此，也可降低根据实施例的三维电阻性 RAM 器件的高度。

[0191] 图 8 至 15 是示出根据本发明概念的实施例，制造图 3 中所示的电阻性 RAM 器件的方法的截面图。

[0192] 参考图 8，在衬底 1 上交替或重复堆叠多个层间绝缘层 11-17 以及多个牺牲层 21-26。在一些实施例中，层间绝缘层 11-17 可由氧化硅型材料或其他合适的绝缘性材料形成。牺牲层 21-26 可由相对于层间绝缘层 11-17 具有蚀刻选择性的材料形成。例如，牺牲层 21-26 可由氮化硅层或其他适用于牺牲层的材料形成。

[0193] 参考图 9，可以图案化层间绝缘层 11-17 和牺牲层 21-26 以形成暴露衬底 1 的有源孔 30。

[0194] 参考图 10，有源层 32 和可变电阻性层 34 可顺序并共形地形成在包括了有源孔 30 的衬底上。在各种实施例中，有源层 32 可由非掺杂多晶硅层或具有与衬底 1 相同导电类型的掺杂多晶硅层形成。可变电阻性层 34 可由选自由锆（Zr）、铪（Hf）、铝（Al）、镍（Ni）、铜（Cu）、钼（Mo）、钽（Ta）、钛（Ti）、钨（W）和硅（Si）组成的组中的至少一种的氧化物材料形成。在其他实施例中，可变电阻性层 34 可包括另一合适的可变电阻性材料。可以利用有源层 32 和可变电阻性层 34 来部分地填充每个有源孔 30。掩埋绝缘层 36 可形成在可变电阻性层 34 上以填充有源孔 30。掩埋绝缘层 36 可由氧化硅型材料形成。

[0195] 参考图 11，可平坦化掩埋绝缘层 36、可变电阻性层 34 以及有源层 32 以暴露第七层间绝缘层 17 的顶面。因此，可在每个有源孔 30 中形成有源柱 32、可变电阻性图案 34 以及掩埋绝缘图案 36。

[0196] 参考图 12，对有源孔 30 之间的层间绝缘层 11-17 以及牺牲层 21-26 图案化以形成暴露衬底 1 的沟槽 38。沟槽 38 可形成为在图 2 中所示的第三方向 L3 上延伸。随后可以将

Micron Ex. 1002, p. 146
Micron v. YMTC
IPR2024-00793

杂质离子注入到通过沟槽 38 暴露的衬底 1 中，由此在衬底 1 中形成公共源线 CSL。

[0197] 参考图 13，可以选择性移除牺牲层 21-26 以暴露层间绝缘层 11-17 的顶面和底面以及有源柱 32 的侧壁。

[0198] 参考图 14，栅绝缘层 42 可共形地形成在所得结构上移除了牺牲层 21-26 的位置。栅绝缘层 42 可至少形成在有源柱 32 的侧壁以及暴露的衬底 1 上。栅绝缘层 42 可由氧化硅层形成。在各种实施例中，可利用沉积工艺或热氧化工艺形成栅绝缘层 42。导电层 44 可形成在栅绝缘层 42 上以填充沟槽 38 和层间绝缘层 11-17 之间的空间。导电层 44 可形成为至少包括掺杂多晶硅层、金属层、金属氮化物层和金属硅化物层中的一个。

[0199] 参考图 15，可以选择性移除在沟槽 38 中形成的导电层 44 和栅绝缘层 42，以形成下选择线 LSL1-LSL3、字线 WL1-WL4 以及上选择线 USL1-USL3，且隔离绝缘图案 46 可以形成在相应的空沟槽 38 中。因此，下选择线 LSL1-LSL3、字线 WL1-WL4 以及上选择线 USL1-USL3 可以彼此分隔并隔离。

[0200] 再次参考图 3，可以利用离子注入工艺在有源柱 32 的相应的上部中形成漏区 D。导电层可形成在包括漏区 D 的衬底上，且可以图案化导电层以形成在图 2 中所示的第二方向 L2 上延伸的位线 BL1-BL3。

[0201] 根据上述实施例，可变电阻性层 34 形成为接触有源柱 32。因此，可更容易制造根据本实施例的电阻性 RAM 器件。

[0202] < 第二实施例 >

[0203] 图 16 是示出根据本发明概念的第二实施例的电阻性 RAM 器件的截面图。

[0204] 参考图 16，本实施例与图 3 中所示的前一实施例的不同之处在于可变电阻性图案 34 的形状。即，根据本实施例的电阻性 RAM 器件可以包括仅覆盖有源柱 32 的内侧壁而没有覆盖有源柱的底面的间隔体形状可变电阻性图案 34。以此方式，所得的可变电阻性图案 34 通常是柱形的，而不是图 15 的实施例中所示的杯形。

[0205] 通过形成如图 10 中所示的有源层 32 和可变电阻性层 34、通过各向异性蚀刻可变电阻性层 34 以形成间隔体形状可变电阻性图案 34 以及通过在相应的有源孔 30 中形成掩埋绝缘图案 36，可以制造根据本实施例的电阻性 RAM 器件。

[0206] < 第三实施例 >

[0207] 图 17 是示出根据本发明概念的第三实施例的电阻性 RAM 器件的截面图。

[0208] 参考图 17，根据本实施例的电阻性 RAM 器件可以包括有源柱 32 和栅绝缘层 42。每个有源柱 32 都可以包括第一有源层 32a 和第二有源层 32b，且栅绝缘层 42 可以包括第一栅绝缘层 42a 和第二栅绝缘层 42b。第一栅绝缘层 42a 可以覆盖有源孔 30 的侧壁并可以具有间隔体形状。此外，第一栅绝缘层 42a 可具有 L 形截面。第一栅绝缘层 42a 还可以覆盖有源孔 30 中的层间绝缘层 11-17 的侧壁。第二栅绝缘层 42b 可以在水平方向上延伸以在层间绝缘层 11-17 和线 LSL1-LSL2、WL1-WL4 以及 USL1-USL3 之间垂直定位。第一有源层 32a 可以具有侧壁间隔体形状并可以覆盖第一栅绝缘层 42a 与第二栅绝缘层 42b 相对的内侧壁。第二有源层 32b 可以覆盖第一有源层 32a 与第一栅绝缘层 42a 相对的内侧壁并可以延伸到通过有源孔 30 暴露的衬底 1 上。在一些实施例中，第一有源层 32a 和第二有源层 32b 可由相同材料层形成。第一栅绝缘层 42a 和第二栅绝缘层 42b 可由相同材料层形成。

[0209] 本实施例的其他元件可以具有与第一实施例中所述相同或相似的构造。

Micron Ex. 1002, p. 147
Micron v. YMTC
IPR2024-00793

[0210] 图 18、19 和 20 是示出根据本发明概念的制造如图 17 中所示的电阻性 RAM 器件的方法的截面图。

[0211] 参考图 18，如图 9 中所示，可以图案化层间绝缘层 11-17 和牺牲层 21-26 以形成暴露衬底 1 的有源孔 30。第一栅绝缘层 42a 和第一有源层 32a 可顺序并共形地形成在包括有源孔 30 的衬底上。第一栅绝缘层 42a 可由氧化硅层形成。第一有源层 32a 可由掺杂多晶硅层或非掺杂多晶硅层形成。

[0212] 参考图 19，可以各向异性蚀刻第一有源层 32a 和第一栅绝缘层 42a 以在每个有源孔 30 中形成间隔体形状的第一有源层 32a 和间隔体形状的第一栅绝缘层 42a。第二有源层 32b、可变电阻性层 34 以及掩埋绝缘层 36 可形成在包括了间隔体形状的第一有源层 32a 和间隔体形状的第一栅绝缘层 42a 的衬底上。在一些实施例中，可共形地形成第二有源层 32b 和可变电阻性层 34，且掩埋绝缘层 36 可形成为填充有源孔 30。

[0213] 参考图 20，可以平坦化掩埋绝缘层 36、可变电阻性层 34 以及第二有源层 32b 以暴露最上层间绝缘层（例如第七层间绝缘层 17）的顶面，由此在每个有源孔 30 中形成杯形的第二有源层 32b、杯形的可变电阻性层 34 以及掩埋绝缘图案 36。

[0214] 随后，如参考图 17 所述，可以图案化层间绝缘层 11-17 和牺牲层 21-26 以形成暴露衬底 1 的沟槽 38，并可以移除牺牲层 21-26。随后，第二栅绝缘层 42b 可以共形地形成在移除了牺牲层 21-26 的衬底上。随后，可以对包括了第二栅绝缘层 42b 的衬底应用与第一实施例中所述相同或相似的工艺。

[0215] < 第四实施例 >

[0216] 图 21 是示出根据本发明概念的第四实施例的电阻性 RAM 器件的截面图。

[0217] 参考图 21，根据本实施例的电阻性 RAM 器件可以包括在有源柱 32 和衬底 1 之间布置的有源焊盘 9。在一些实施例中，有源焊盘 9 可由与有源柱 32 相同的材料的形成。在各种实施例中，有源焊盘 9 的宽度可以大于有源柱 32 的宽度。相邻于有源焊盘 9 和有源柱 32 之间的界面的第二层间绝缘层 12 可以是包括第一子层间绝缘层 12a 和第二子层间绝缘层 12b 的双层材料。有源焊盘 9 的顶面可以与第一子层间绝缘层 12a 的顶面共面。下选择线 LSL1-LSL3 可布置为相邻于有源焊盘 9 的侧壁。每个可变电阻性层 34 的外侧壁可以由字线 WL1-WL4 和上选择线 USL1-USL3 中的一个围绕。本实施例的其他元件可以具有与第一实施例中所述相同或相似的构造。

[0218] 图 22、23 和 24 是示出制造图 21 中所示的电阻性 RAM 器件的方法的截面图。

[0219] 参考图 22，可以在衬底 1 上顺序形成第一层间绝缘层 11、第一牺牲层 21 以及第一子层间绝缘层 12a。可以图案化第一子层间绝缘层 12a、第一牺牲层 21 以及第一层间绝缘层 11 以形成暴露衬底 1 的下有源孔 7。随后可以在相应的下有源孔 7 中形成有源焊盘 9。可通过在第一子层间绝缘层 12a 上沉积多晶硅层以填充下有源孔 7 且通过平坦化多晶硅层来形成有源焊盘 9。在一些实施例中，多晶硅层或有源焊盘 9 可以经历热退火处理以形成单晶硅层或单晶有源焊盘。

[0220] 参考图 23，可以在包括了有源焊盘 9 的衬底上形成第二子层间绝缘层 12b，且可以在第二子层间绝缘层 12b 上交替形成第二至第六牺牲层 22-26 以及第三至第七层间绝缘层 13-17。可以图案化第三至第七层间绝缘层 13-17、第二至第六牺牲层 22-26 以及第二子层间绝缘层 12b 以形成暴露相应的有源焊盘 9 的有源孔 30。在形成有源孔 30 的过程中，有源

Micron Ex. 1002, p. 148
Micron v. YMTC
IPR2024-00793

焊盘 9 可作为蚀刻停止层。

[0221] 参考图 24，可以利用与第一实施例中所述相同的工艺在每个有源孔 30 中形成有源柱 32、可变电阻性图案 34 以及掩埋绝缘图案 36。随后，可以对包括了有源柱 32、可变电阻性图案 34 以及掩埋绝缘图案 36 的焊盘应用与第一实施例中所述相同或相似的工艺。

[0222] 在根据本实施例制造的电阻性 RAM 器件中，有源焊盘 9 可以用于改善有源柱 32 和衬底 1 之间的电流(例如图 21 的公共源线 CSL)。本文中会更全面说明这种效果。

[0223] 如图 18 中所示，当通过蚀刻层间绝缘层 11-17 和牺牲层 21-26 形成有源孔 30 时，衬底 1 可能被过度蚀刻以完全打开深有源孔 30。因此在有源孔 30 下方的衬底 1 可能凹陷。即，有源孔 30 的底面可能位于衬底 1 的初始顶面之下的位置。在这种情况下，如果第一栅绝缘层 42a 如第三实施例中所述形成在有源孔 30 中(参见图 17 和 18)，则有源孔 30 中的第一栅绝缘层 42a 的下部可能形成为从衬底 1 的初始顶面向下突出。第一栅绝缘层 42a 的这些突出物可能干扰在有源孔 30 中形成的有源柱 32 和衬底 1 中形成的公共源线 CSL 之间的电流。因此，在形成有源孔 30 和栅绝缘层 42 之前在衬底 1 上形成有源焊盘 9 的情况下，栅绝缘层不会干扰有源柱 32 和公共源线 CSL 之间的电流。

[0224] < 第五实施例 >

[0225] 图 25 是示出根据本发明概念的第五实施例的电阻性 RAM 器件的截面图。

[0226] 参考图 25，根据本实施例的电阻性 RAM 器件可以包括在有源柱 32 和衬底 1 之间布置的有源焊盘 9，且有源焊盘 9 和有源柱 32 可布置在暴露衬底 1 的有源孔 30 中。在每个有源孔 30 中，有源焊盘 9 的侧壁可以与有源柱 32 的外侧壁垂直对齐。下选择线 LSL1-LSL3 可以围绕有源焊盘 9 的侧壁。字线 WL1-WL4 和上选择线 USL1-USL3 可以围绕有源柱 32 的外侧壁，且可变电阻性图案 34 可以布置在相应的有源柱 32 中。本实施例的其他元件可以具有与第一实施例中所述或本文所述的一些其他实施例中相同或相似的构造。

[0227] 图 26 是示出制造图 25 中所示的电阻性 RAM 器件的方法的截面图。

[0228] 参考图 26，如图 9 中所示，可以图案化层间绝缘层 11-17 和牺牲层 21-26 以形成暴露衬底 1 的有源孔 30。可以利用选择外延生长(SEG)工艺在暴露的衬底 1 上生长半导体外延层，由此在相应的有源孔 30 中形成有源焊盘 9。随后可以利用与第一实施例中所述相同或相似的方式在有源孔 30 中形成有源柱和可变电阻性图案。后续工艺可以与第一实施例中所述工艺相同或相似。

[0229] < 第六实施例 >

[0230] 图 27 是示出根据本发明概念的第六实施例的电阻性 RAM 器件的截面图。

[0231] 参考图 27，根据本实施例的电阻性 RAM 器件可以包括在每个有源孔 30 中布置的有源柱 32 和可变电阻性图案 34。可变电阻性图案 34 可布置在有源柱 32 中以便具有杯形，且可变电阻性图案 34 也可具有杯形。此外，根据本实施例的电阻性 RAM 器件可以包括在有源柱 32 的基部和可变电阻性图案 34 的底面之间布置的下掩埋绝缘图案 8。可变电阻性图案 34 的底面可以位于下选择线 LSL1-LSL3 和第一字线 WL1 之间的高度。下掩埋绝缘图案 8 可由诸如氧化硅层、氮化硅层或氮氧化硅层或其他合适的绝缘材料层的绝缘材料形成。本实施例的其他元件可以具有与第一实施例中所述相同或相似的构造。以此方式，在本实施例，下选择晶体管不包括可变电阻性层图案 34。

[0232] 图 28、29、30 和 31 是示出制造图 27 中所示的电阻性 RAM 器件的方法的截面图。

Micron Ex. 1002, p. 149
Micron v. YMTC
IPR2024-00793

[0233] 参考图 28，如图 9 中所示，可以图案化层间绝缘层 11-17 和牺牲层 21-26 以形成暴露衬底 1 的有源孔 30。有源层 32 可共形地形成在包括了有源孔 30 的衬底上。下掩埋绝缘层 8 可以形成在有源层 32 上以填充有源孔 30。

[0234] 参考图 29，可以回蚀下掩埋绝缘图案 8 以在有源孔 30 的相应的下部形成下掩埋绝缘层 8。下掩埋绝缘图案 8 可形成为使下掩埋绝缘图案 8 的顶面位于下选择线 LSL1-LSL3 和第一字线 WL1 之间的高度。因此，可暴露位于比下掩埋绝缘图案 8 更高的高度的有源层 32 的部分。

[0235] 参考图 30，可变电阻性层 34 可共形地形成在暴露的有源层 32 和下掩埋绝缘图案 8 上，且掩埋绝缘层 36 可形成在可变电阻性层 34 上以填充有源孔 30。

[0236] 参考图 31，可以平坦化掩埋绝缘层 36、可变电阻性层 34 和有源层 32 以暴露最上层间绝缘层 17 的顶面。随后可以利用与第一实施例中所述相同或相似的方式执行后续工艺。

[0237] < 第七实施例 >

[0238] 图 32 是示出根据本发明概念的第七实施例的电阻性 RAM 器件的截面图。

[0239] 参考图 32，根据本实施例的电阻性 RAM 器件可以包括垂直间隔并堆叠的第一下选择线 LSL1 对以及垂直间隔并堆叠的第二下选择线 LSL2 对。类似地，根据本实施例的电阻性 RAM 器件还可以包括垂直间隔并堆叠的第一上选择线 USL1 对以及垂直间隔并堆叠的第二上选择线 USL2 对。本实施例的其他元件可以具有与第一实施例中所述相同或相似的构造。

[0240] < 第八实施例 >

[0241] 图 33 是示出根据本发明概念的第八实施例的电阻性 RAM 器件的截面图。

[0242] 本实施例类似于参考图 27 说明的第六实施例。因此为了避免赘述，将主要说明本实施例和图 27 中所示的第六实施例之间的不同。

[0243] 参考图 33，可变电阻性图案 34 和掩埋绝缘图案 36 的顶面可以位于最上字线（例如第四字线 WL4）和上选择线 USL1-USL3 之间的高度。此外，在位线 BL1-BL3 和掩埋绝缘图案 36 之间的有源孔 30 可由上掩埋绝缘图案 48 填充。以此方式，在本实施例中，下选择晶体管和上选择晶体管不包括可变电阻性层图案 34。本实施例的其他元件可以具有与第六实施例中所述相同或相似的构造。

[0244] 图 34 和 35 是示出制造图 33 中所示的电阻性 RAM 器件的方法的截面图。

[0245] 参考图 34，可以回蚀图 30 中所示的掩埋绝缘层 36 和可变电阻性层 34 并使其凹陷以在有源孔 30 中形成可变电阻性图案 34 和掩埋绝缘图案 36。可变电阻性图案 34 和掩埋绝缘图案 36 可形成为使可变电阻性图案 34 和掩埋绝缘图案 36 的顶面可以位于最上字线（例如第四字线 WL4）和上选择线 USL1-USL3 之间的高度。有源层 32 可以在掩埋绝缘层 36 和可变电阻性层 34 被回蚀并凹陷时用作蚀刻停止层。因此，即使在掩埋绝缘层 36 和可变电阻性层 34 被回蚀并凹陷之后，最上层间绝缘层（例如第七层间绝缘层 17）可以仍被有源层 32 覆盖。

[0246] 参考图 35，上掩埋绝缘层 48 可以沉积在有源层 32 上以填充掩埋绝缘图案 36 上的有源孔 30。可以平坦化上掩埋绝缘层 48 和有源层 32 以暴露最上层间绝缘层 17 的顶面并在相应的有源孔 30 中形成上掩埋绝缘图案 48。随后可以利用与第一实施例中所述相同或

Micron Ex. 1002, p. 150
Micron v. YMTC
IPR2024-00793

相似的方式执行后续工艺。

[0247] < 第九实施例 >

[0248] 图 36 是示出根据本发明概念的第九实施例的电阻性 RAM 器件的截面图。

[0249] 参考图 36，根据本实施例的电阻性 RAM 器件可以包括在有源柱 32 和衬底 1 之间布置的有源焊盘 9，且有源焊盘 9 和有源柱 32 可布置在暴露衬底 1 的有源孔 30 中。可变电阻性图案 34 可以覆盖有源柱 32 的内侧壁并具有间隔体形状。可变电阻性图案 34 的顶面可以位于上选择线 USL1-USL3 和最上字线 WL4 之间的高度，且可变电阻性图案 34 的底面可以位于下选择线 LSL1-LSL3 和最下字线 WL1 之间的高度。由可变电阻性图案 34 围绕的有源孔 30 可以被掩埋绝缘图案 36 填充，且位线 BL1-BL3 和掩埋绝缘图案 36 之间的有源孔 30 可以被上掩埋绝缘图案 48 填充。本实施例的其他元件可以具有与第五和第八实施例中所述相同或相似的构造。此外，可以利用与第五和第八实施例中所述相同或相似的方式形成本发明的其他元件。

[0250] < 第十实施例 >

[0251] 图 37 是示出根据本发明概念的第十实施例的电阻性 RAM 器件的截面图。

[0252] 参考图 37，根据本实施例的电阻性 RAM 器件可以包括在每个有源孔 30 中布置的可变电阻性图案 34 和掩埋绝缘图案 36，且每个有源孔 30 中的可变电阻性图案 34 和掩埋绝缘图案 36 可以由字线 WL1-WL4 以及下选择线 LSL1-LSL3 中的一个围绕。即，可变电阻性图案 34 和掩埋绝缘图案 36 的顶面可以位于上选择线 USL1-USL3 和最上字线（例如第四字线 WL4）之间的高度。掩埋绝缘图案 36 和可变电阻性图案 34 上的有源孔 30 可以由上掩埋绝缘图案 48 填充。本实施例的其他元件可以具有与第一实施例中所述相同或相似的构造。以此方式，在本实施例中，上选择晶体管不包括可变电阻性层图案 34。此外，可以利用与第一实施例中所述相同或相似的方式形成本实施例的其他元件。

[0253] < 第十一实施例 >

[0254] 图 38 是示出根据本发明概念，根据第十一实施例的电阻性 RAM 器件的截面图。图 39 是示出对根据第十一实施例的电阻性 RAM 器件进行编程时，图 38 的部分“P2”的放大图，且图 40 是示出对根据第十一实施例的电阻性 RAM 器件进行擦除时，图 38 的部分“P2”的放大图。

[0255] 参考图 38，根据本实施例的电阻性 RAM 器件可以包括覆盖有源孔 30 的相应的侧壁的间隔体形状的可变电阻性图案 34，以及覆盖可变电阻性图案 34 的相应的内侧壁的杯形有源柱 32。此外，栅绝缘层 42 可以覆盖每个可变电阻性图案 34 的部分外侧壁。即，可变电阻性图案 34 可以布置在栅绝缘层 42 和有源柱 32 之间。在本实施例中，可变电阻性图案 34 的每个侧壁可非常薄，例如具有约 20 纳米以下的厚度。如果可变电阻性图案 34 如上所述具有薄侧壁，则在电阻性 RAM 器件的操作过程中可将电场有效和 / 或高效地施加到相邻于可变电阻性图案 34 的有源柱 32。本实施例的其他元件可具有与第一实施例中所述相同或相似的构造。

[0256] 可以与第一实施例中所述类似的方式对图 38 中所示的电阻性 RAM 器件进行编程、擦除和读取。当对根据本实施例的电阻性 RAM 器件进行编程时，如图 39 中所示，导电细丝 PM 可以形成在可变电阻性图案 34 中。此外，当对根据本实施例的电阻性 RAM 器件进行擦除时，如图 40 中所示，可以移除形成在可变电阻性图案 34 中的导电细丝 PM。当选择图 39 中

Micron Ex. 1002, p. 151
Micron v. YMTC
IPR2024-00793

所示的已编程存储器单元以读出其中存储的数据时，即使所选存储器单元的单元晶体管截止，单元电流也可以流过导电细丝 PM，如图 39 的箭头“CF”所示。

[0257] 为了制造图 38 中所示的电阻性 RAM 器件，以与例如结合图 9 的实施例在本文中所述的相同的方式形成有源孔 30，且可变电阻性图案 34 可形成在有源孔 30 的侧壁上。在它们不覆盖孔的底部的意义上，可变电阻性图案 34 可形成为具有间隔体形状。因此，位于有源孔 30 下方的衬底 1 的部分可在形成可变电阻性图案 34 之后暴露。随后可以在相应的有源孔 30 中形成具有杯形的有源柱 32 并由可变电阻性图案 34 围绕。可以利用与第一实施例中所述相同或相似的方式形成本实施例的其他元件。

[0258] 图 41、42、43、44 和 45 是示出根据第十一实施例的其他变型实施例的电阻性 RAM 器件的截面图。

[0259] 参考图 41，根据本变型实施例的电阻性 RAM 器件可以包括在有源柱 32 和衬底 1 之间布置的有源焊盘 9，且有源焊盘 9 和有源柱 32 可以布置在暴露衬底 1 的有源孔 30 中。可变电阻性图案 34 可以布置在有源柱 32 和有源孔 30 的侧壁之间。可变电阻性图案 34 可延伸以覆盖围绕字线 WL1-WL4 的栅绝缘层 42。可变电阻性图案 34 的顶面可以位于最上字线(例如第四字线 WL4)和上选择线 USL1-USL3 之间的高度，且可变电阻性图案 34 的底面可以位于最下字线(例如第一字线 WL1)和下选择线 LSL1-LSL3 之间的高度。本变型实施例的其他元件可具有与图 38 中所示相同或相似的构造。

[0260] 参考图 42，根据本变型实施例的电阻性 RAM 器件可以类似于图 41 中所示的电阻性 RAM 器件。但是根据本实施例的电阻性 RAM 器件可以不包括图 41 中所示的电阻性 RAM 器件的有源焊盘 9。因此，有源柱 32 可以在垂直方向上延伸以接触衬底 1。本变型实施例的其他元件可以具有与图 41 中所示相同或相似的构造。

[0261] 参考图 43，根据本变型实施例的电阻性 RAM 器件可以类似于图 42 中所示的电阻性 RAM 器件。但是，本变型实施例的可变电阻性图案 34 可向上延伸进入上选择线 USL1-USL3 与有源柱 32 之间的界面。本变型实施例的其他元件可以具有与图 42 中所示相同或相似的构造。

[0262] 参考图 44，根据本变型实施例的电阻性 RAM 器件可以类似于图 43 中所示的电阻性 RAM 器件。但是，根据本变型实施例的电阻性 RAM 器件可以包括在可变电阻性图案 34 和衬底 1 之间布置的有源焊盘 9。本变型实施例的其他元件可以具有与图 43 中所示相同或相似的构造。

[0263] 参考图 45，根据本变型实施例的电阻性 RAM 器件可以类似于图 38 中所示的电阻性 RAM 器件。但是，本变型实施例的可变电阻性图案 34 可以不延伸为覆盖上选择线 USL1-USL3 的侧壁。即，可变电阻性图案 34 的顶面可以位于最上字线(例如第四字线 WL4)和上选择线 USL1-USL3 之间的高度。本变型实施例的其他元件可以具有与图 38 中所示相同或相似的构造。

[0264] 图 41、42、43、44 和 45 中所示的电阻性 RAM 器件可以与第一至第十一实施例中所述相同或相似的方式制造。

[0265] 图 46 是示出包括了根据一些实施例的电阻性 RAM 器件的存储器系统的示例的示意性框图。

[0266] 参考图 46，存储器系统 1100 可应用于个人数字助理(PDA)、便携计算机、网络平板

Micron Ex. 1002, p. 152
Micron v. YMTC
IPR2024-00793

电脑、无线电话、移动电话、数字音乐播放器或存储卡中。存储器系统 1100 还可以应用于通过无线接收或传输信息数据的其他电子产品中。

[0267] 存储器系统 1100 可以包括控制器 1110、输入 / 输出(I/O)单元 1120、存储器器件 1130、接口单元 1140 以及数据总线 1150。控制器 1110、I/O 单元 1120、存储器器件 1130 以及接口单元 1140 中的至少两个可以通过数据总线 1150 彼此通信。即,数据总线 1150 可以对应于电信号传输的路径。

[0268] 控制器 1110 可以包括微处理器、数字信号处理器(DSP)、微控制器等中的至少一个。存储器器件 1130 可以存储由控制器 1110 执行的命令。I/O 单元 1120 可以从外部装置接收数据或信号,或可以将数据或信号传输给外部装置。I/O 单元 1120 可以包括小键盘、键盘或显示单元。

[0269] 存储器器件 1130 可以包括至少一个根据上述示例性实施例的电阻性 RAM 器件。存储器器件 1130 还可以包括不同于上述实施例中说明的电阻性 RAM 器件的另一类型的半导体存储器器件。例如,存储器器件 1130 还可以包括另一类型的非易失性存储器器件或易失性存储器器件。

[0270] 接口单元 1140 可以将电数据传输至通信网络或可以从通信网络接收电数据。

[0271] 图 47 是示出包括了根据实施例的电阻性 RAM 器件的存储卡的示例的示意性框图。

[0272] 参考图 47,存储卡 1200 可以包括具有至少一个根据上述示例性实施例的电阻性 RAM 器件的存储器器件 1210。存储卡 1200 可用作存储大容量数据的数据存储介质。存储卡 1200 还可以包括控制主机和存储器器件 1210 之间的数据通信的存储器控制器 1220。

[0273] 存储器控制器 1220 可以包括静态随机存取存储器(SRAM)器件 1221、中央处理单元(CPU)1222、主机接口单元 1223、错误检查和纠正(ECC)块 1224 以及存储器接口单元 1225。SRAM 器件 1221 可以用作 CPU1222 的操作存储器。主机接口单元 1223 可被配置为包括存储卡 1200 和主机之间的数据通信协议。ECC 块 1224 可以检测并纠正从存储器器件 1210 读出的数据的错误。存储器接口单元 1225 可以将存储器控制器 1220 连接至存储器器件 1210。中央处理单元(CPU)1222 可以控制用于存储器控制器 1220 的数据通信的总体操作。即使未在附图中示出,存储卡 1200 还可以包括存储与主机交互的代码数据的只读存储器(ROM)器件。

[0274] 图 48 是示出包括了根据实施例的电阻性 RAM 器件的信息处理系统的示例的框图。

[0275] 参考图 48,信息处理系统 1300 可以是移动系统、台式计算机等。信息处理系统 1300 可以包括具有至少一个根据上述示例性实施例的电阻性 RAM 器件的存储器单元 1310。信息处理系统 1300 还可以包括调制解调器(MODEM)1320、中央处理单元(CPU)1330、随机存取存储器(RAM)器件 1340 以及用户接口单元 1350。存储器单元 1310、MODEM1320、CPU1330、RAM 器件 1340 以及用户接口单元 1350 中的至少两个可以通过数据总线 1360 彼此通信。存储器单元 1310 可以具有与图 47 中所示的存储卡 1200 基本上相同的构造。即,存储器单元 1310 可以包括存储器器件 1311 以及控制存储器器件 1311 的整体操作的存储控制器 1312。

[0276] 存储器单元 1310 可以存储由 CPU1330 处理的数据或从外部系统传输的数据。存储器单元 1310 可被配置为包括固态盘(SSD)。在这种情况下,组成信息处理系统 1300 的存储器单元 1310 可以稳定并可靠地存储大容量数据。如果存储器单元 1310 的可靠性提高,则信息处理系统 1300 可节省检查和纠正数据所需要的资源。因此,信息处理系统 1300 可

Micron Ex. 1002, p. 153
Micron v. YMTC
IPR2024-00793

提供快速数据通信。即使附图中未示出，信息处理系统 1300 还可以包括相机图像处理器、应用芯片组和 / 或输入 / 输出单元。

[0277] 可利用各种封装技术密封根据上述示例性实施例的三维电阻性 RAM 器件。例如，可利用封装上封装（PoP）技术、球栅阵列（BGA）技术、芯片级封装（CSP）技术、带引线的塑料芯片载体（PLCC）技术、塑料双列直插封装（PDIP）技术、华夫盘包装管芯技术、晶圆形式管芯技术、板上芯片（COB）技术、陶瓷双列直插封装（CERDIP）技术、塑料四方扁平封装（PQFP）技术、薄四方扁平封装（TQFP）技术、小外形封装（SOIC）技术、窄间距小外形封装（SSOP）技术、薄小外形封装（TSOP）技术、系统级封装（SIP）技术、多芯片封装（MCP）技术、晶圆级制造封装（WFP）技术以及晶圆级加工堆叠封装（WSP）技术密封根据上述示例性实施例的电阻性 RAM 器件。

[0278] 根据上述实施例，选择晶体管可串联电连接到包括了可变电阻性图案的存储器单元。因此，如果选择晶体管截止，则可最小化流过单元晶体管的不期望的单元泄漏电流。

[0279] 此外，替代电荷捕获层的过渡金属氧化物层可用作用于数据存储元件的可变电阻性层。因此，与采用电荷捕获层作为数据存储元件的非易失性存储器器件相比，可降低编程电压、擦除电压以及读取电压。

[0280] 而且，多个虚位线可以并联电连接到公共源线，且 n 个位线可以布置在虚位线之间的每个串块中。在这种设计构造中，在编程模式或擦除模式过程中，可同时将编程电压或擦除电压施加至在一个串块中布置的 n 个位线中的 m 个位线（数目“m”小于数目“n”）。因此，可降低编程错误或擦除错误发生的概率，这是因为即使在执行编程操作或擦除操作时，公共源线也保持稳定的电压电平。

[0281] 此外，可变电阻性层可形成为接触用作单元晶体管的沟道层的有源柱。因此，可以更容易地制造包括可变电阻性层的电阻性 RAM 器件。

[0282] 虽然已经参考示例性实施例说明了发明概念，但是对于本领域技术人员显而易见的是在不脱离发明概念的精神和范围的情况下可进行各种改变和改进。因此，应当理解上述实施例不是限制性的而是说明性的。因此，发明概念的范围由随附权利要求及其等价物的最广义可允许解释确定，且不应由上文束缚或限定。

Micron Ex. 1002, p. 154
Micron v. YMTC
IPR2024-00793

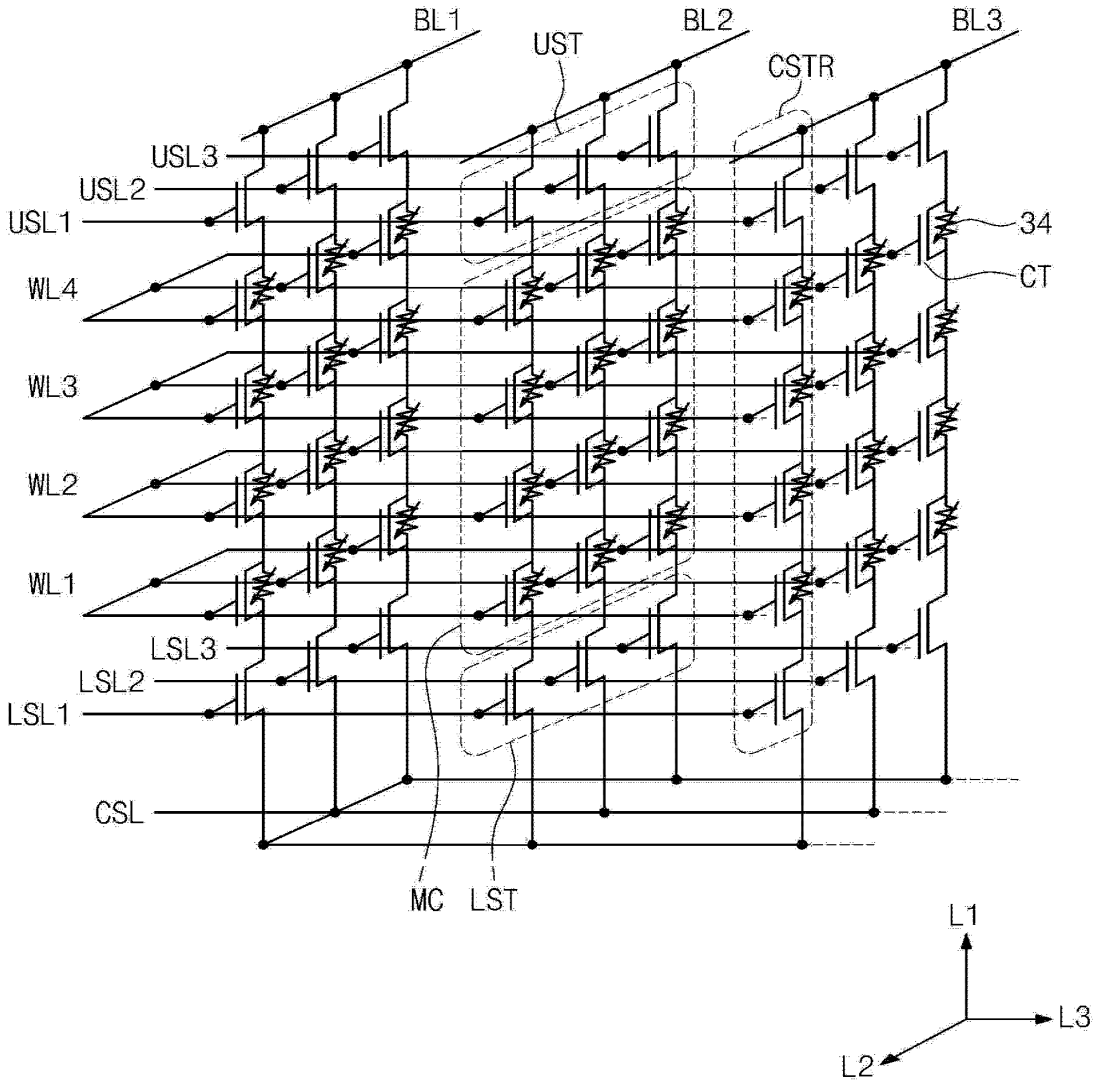


图 1

Micron Ex. 1002, p. 155
Micron v. YMTC
IPR2024-00793

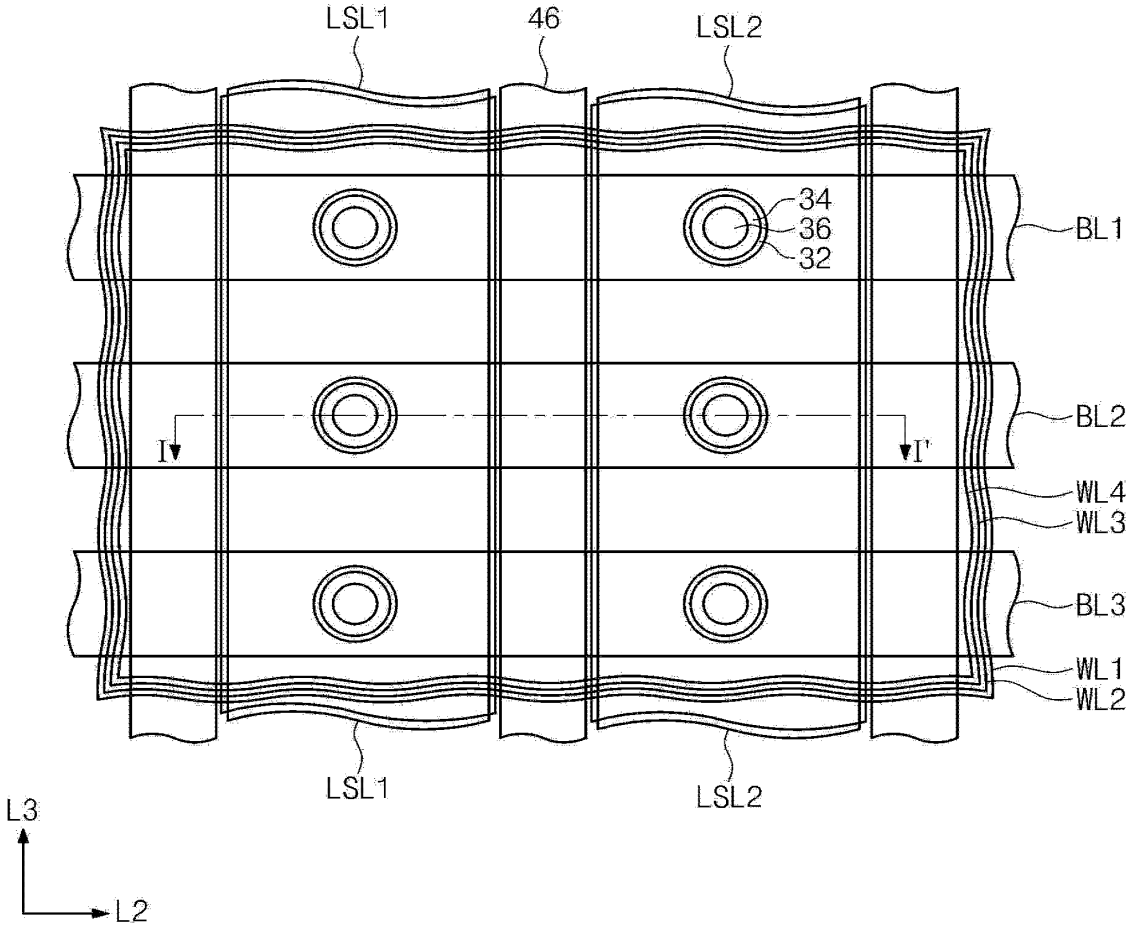


图 2

Micron Ex. 1002, p. 156
Micron v. YMTC
IPR2024-00793

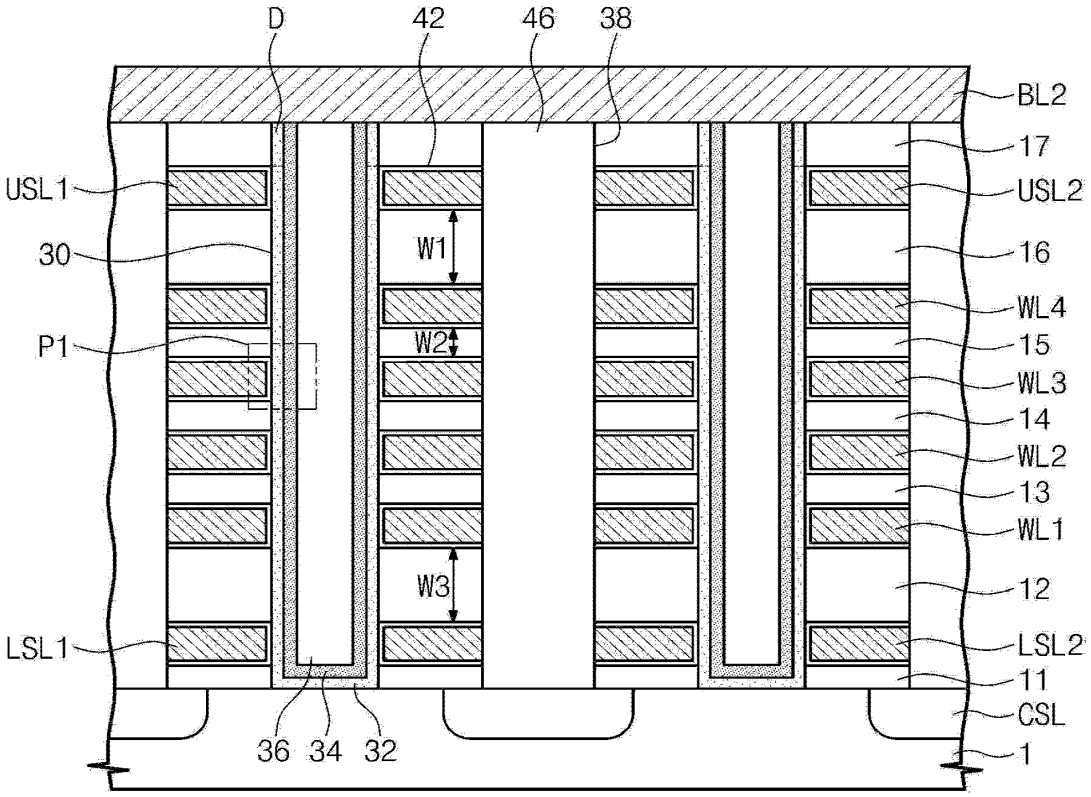


图 3

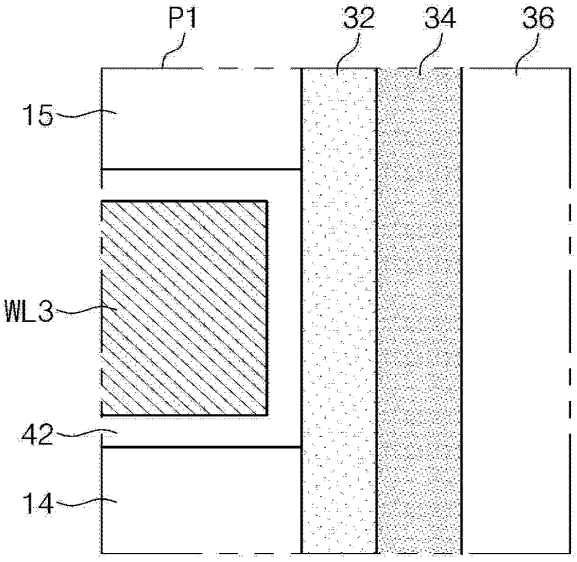


图 4A

38

Micron Ex. 1002, p. 157
Micron v. YMTC
IPR2024-00793

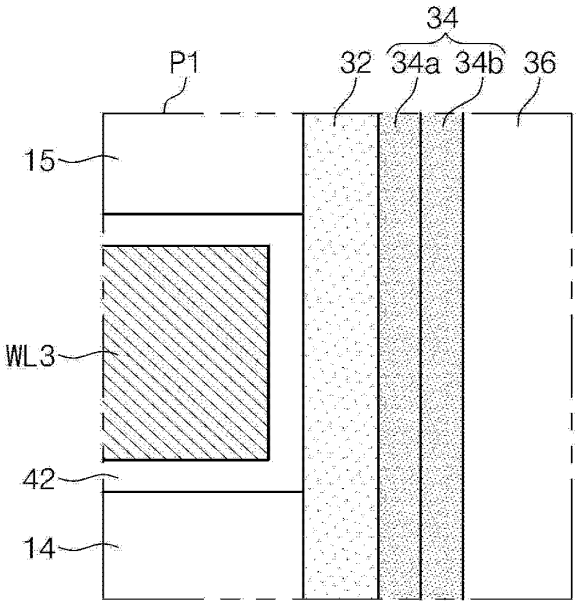


图 4B

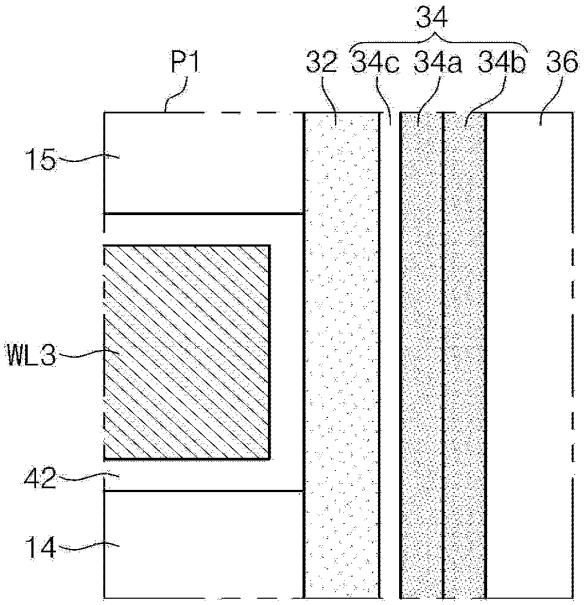


图 4C

Micron Ex. 1002, p. 158
Micron v. YMTC
IPR2024-00793

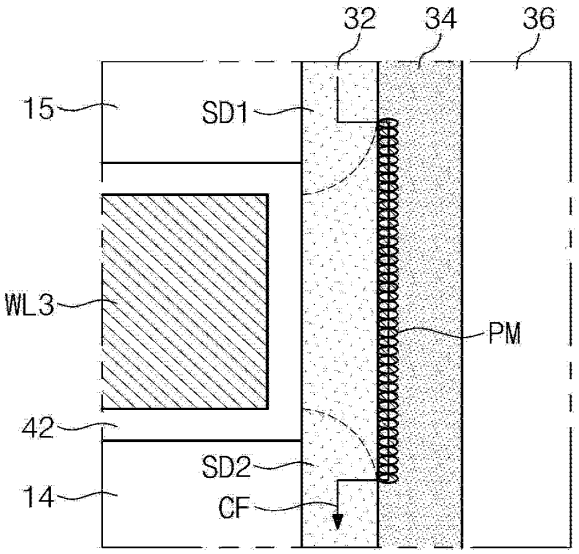


图 5A

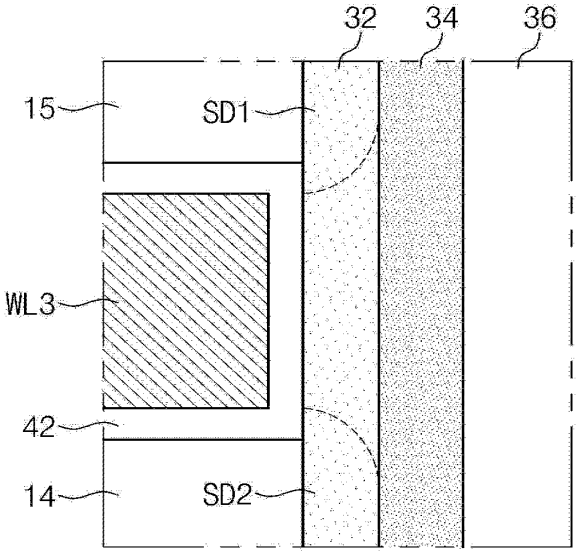


图 5B

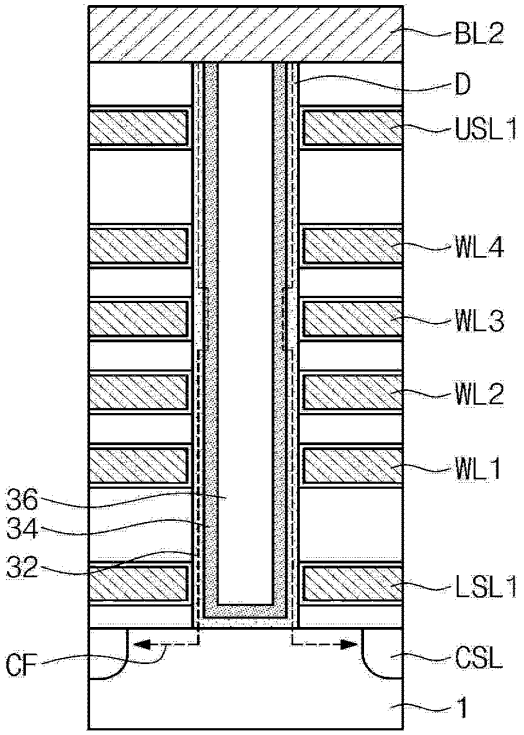


图 6

Micron Ex. 1002, p. 159
Micron v. YMTC
IPR2024-00793

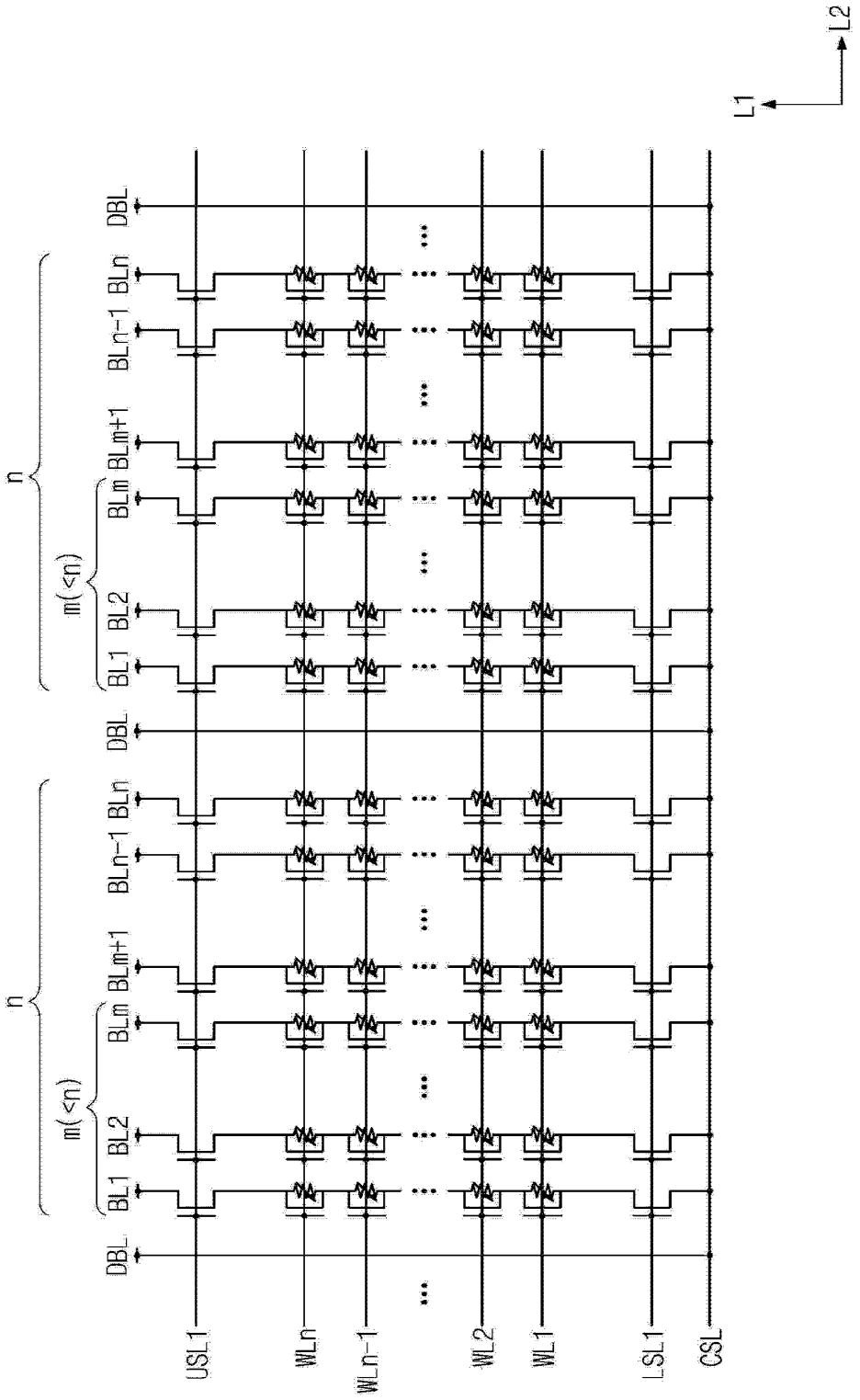


图 7

Micron Ex. 1002, p. 160
Micron v. YMTC
IPR2024-00793

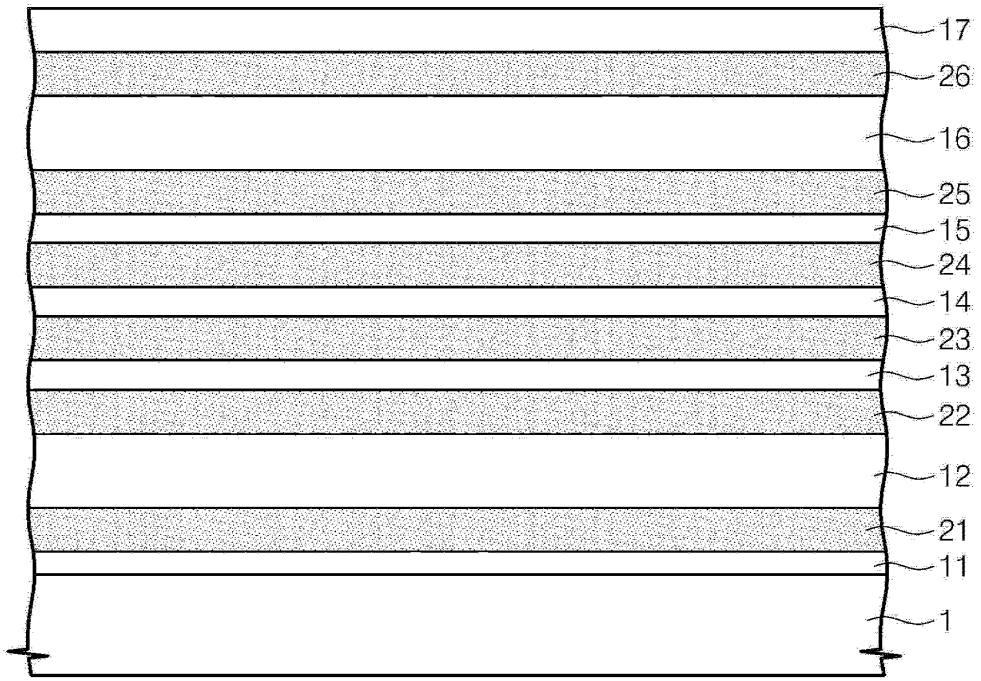


图 8

Micron Ex. 1002, p. 161
Micron v. YMTC
IPR2024-00793

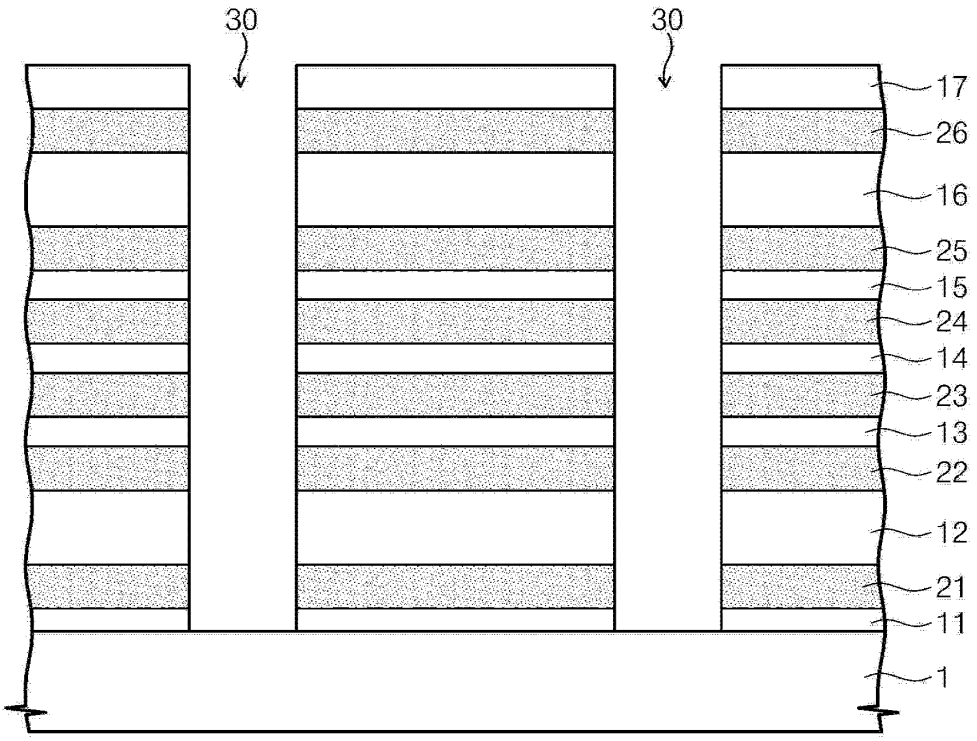


图 9

Micron Ex. 1002, p. 162
Micron v. YMTC
IPR2024-00793

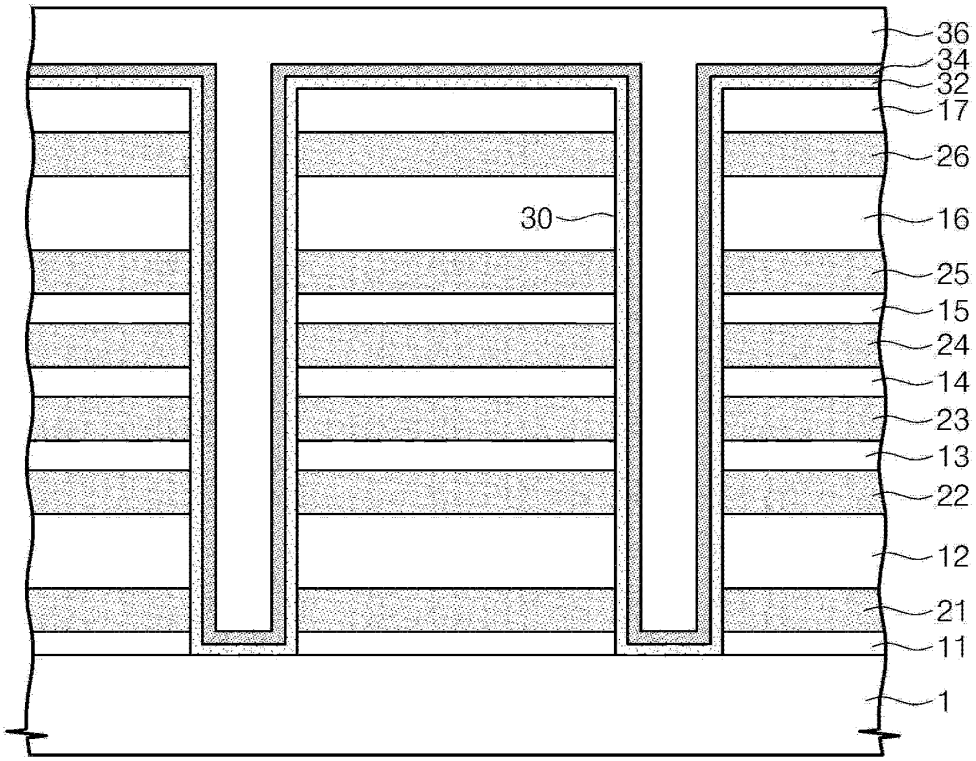


图 10

Micron Ex. 1002, p. 163
Micron v. YMTC
IPR2024-00793

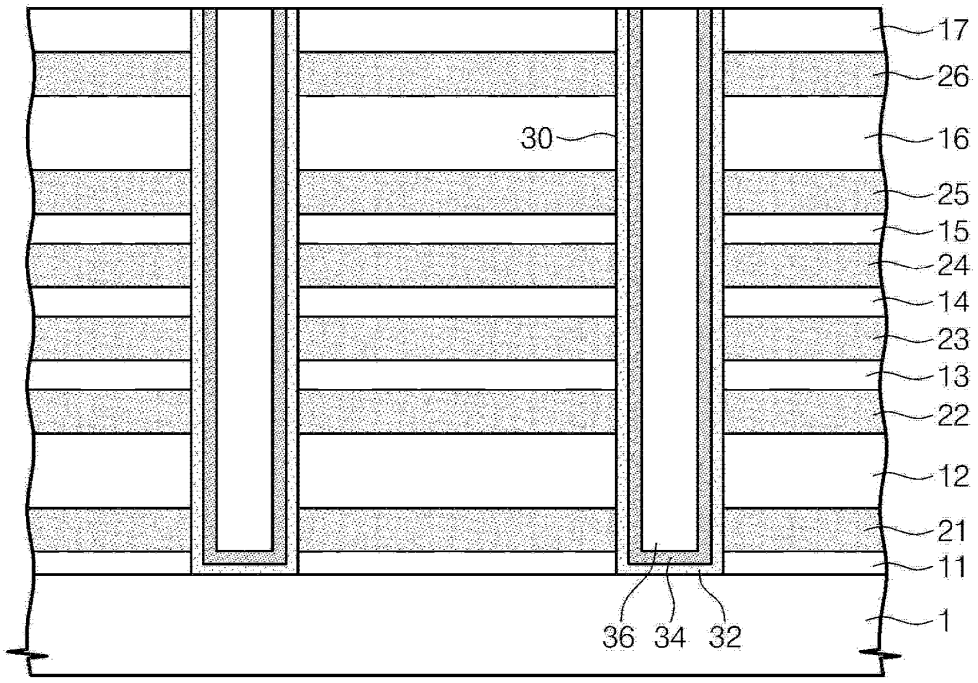


图 11

Micron Ex. 1002, p. 164
Micron v. YMTC
IPR2024-00793

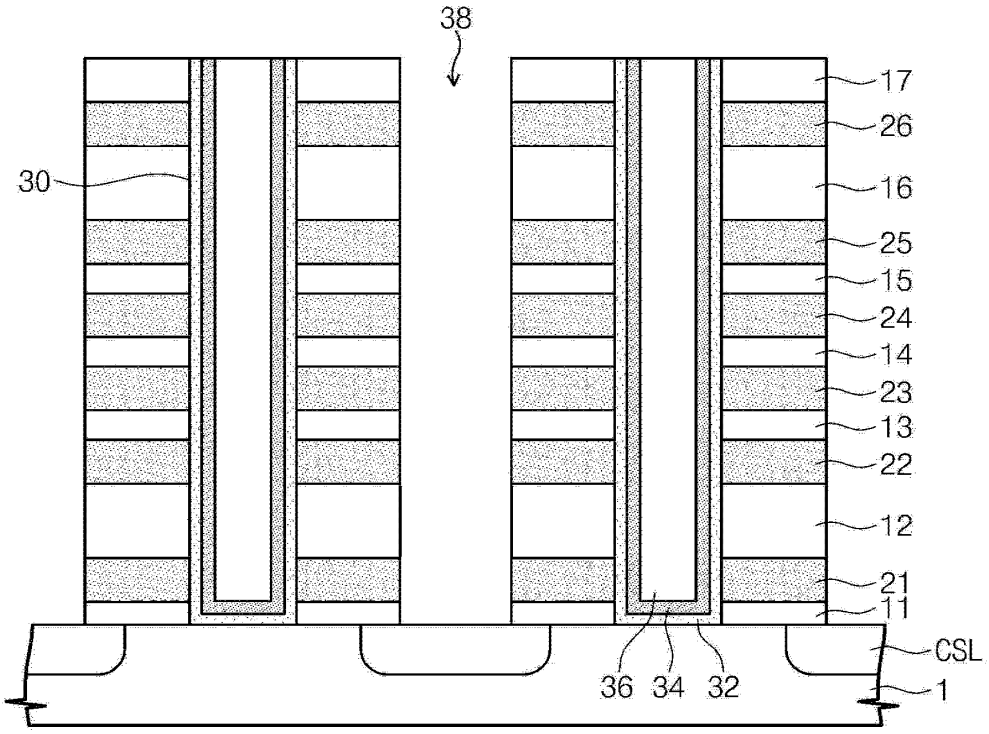


图 12

Micron Ex. 1002, p. 165
Micron v. YMTC
IPR2024-00793

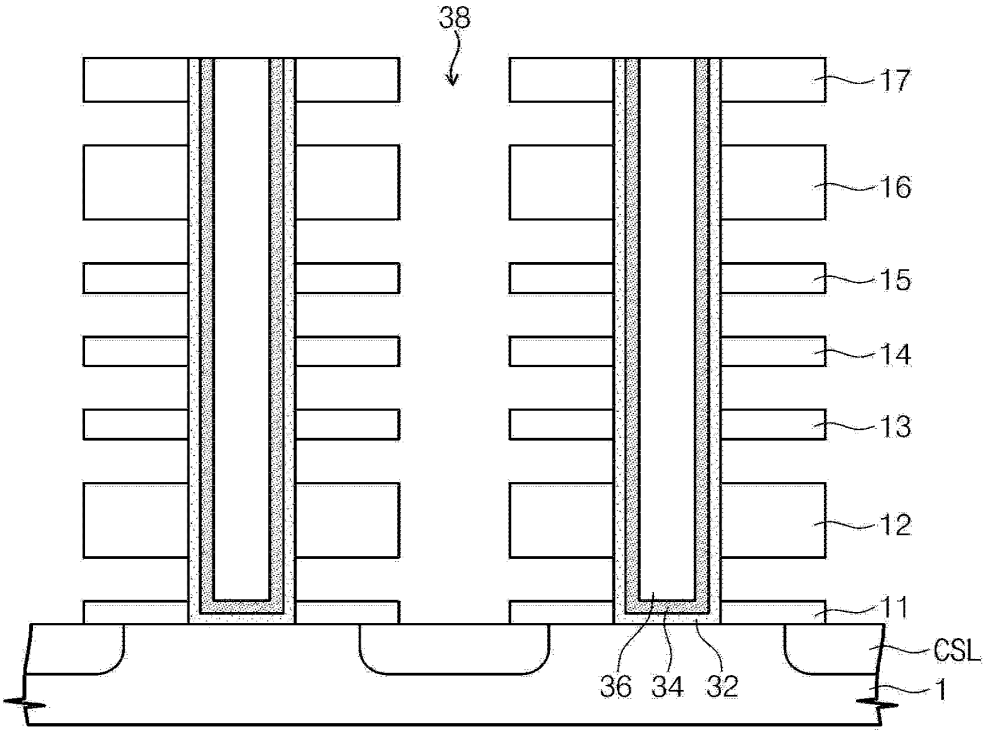


图 13

Micron Ex. 1002, p. 166
Micron v. YMTC
IPR2024-00793

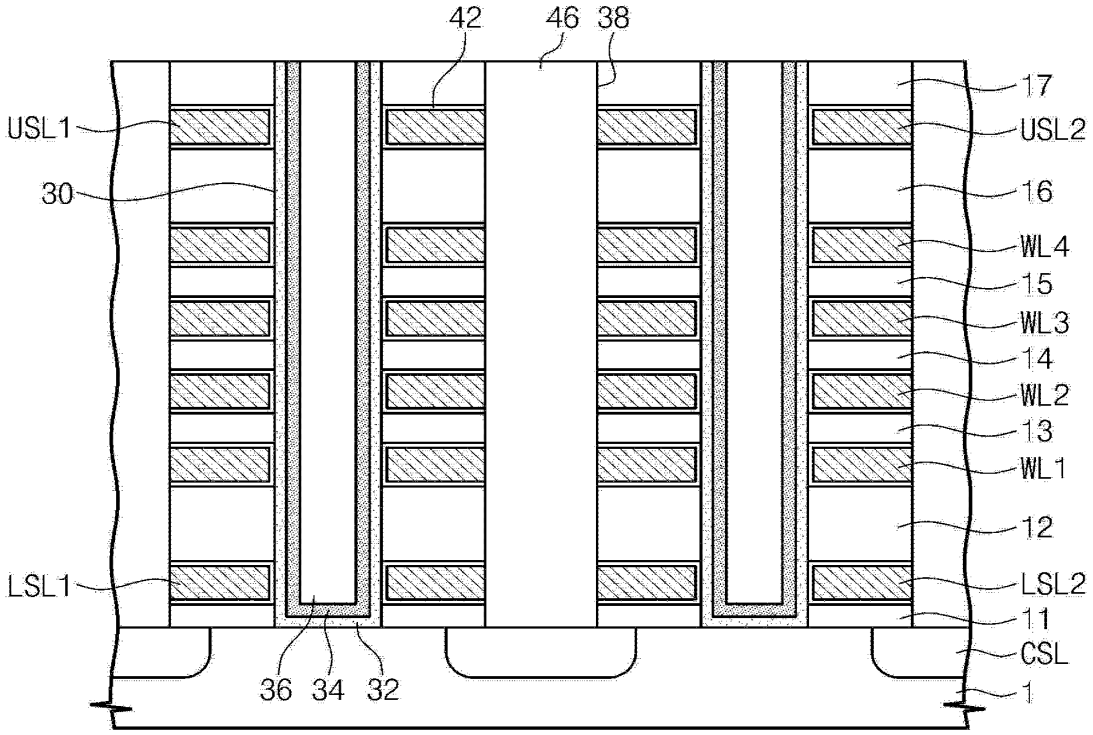


图 15

Micron Ex. 1002, p. 168
Micron v. YMTC
IPR2024-00793

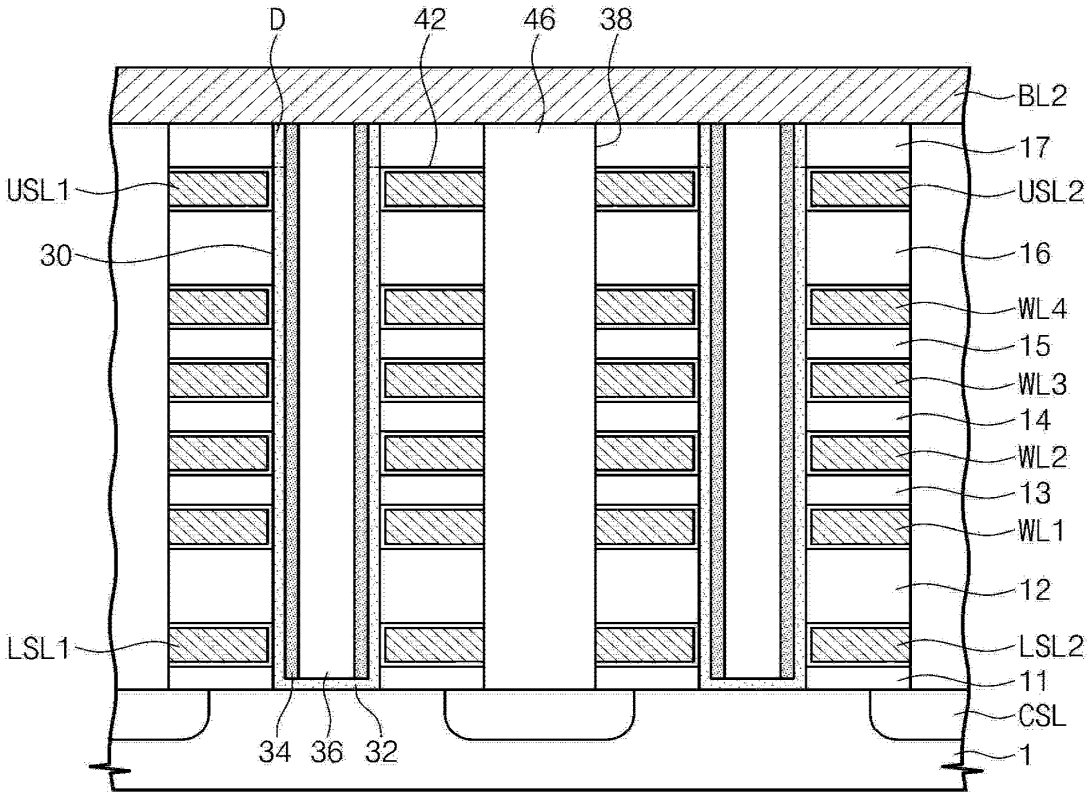


图 16

Micron Ex. 1002, p. 169
Micron v. YMTC
IPR2024-00793

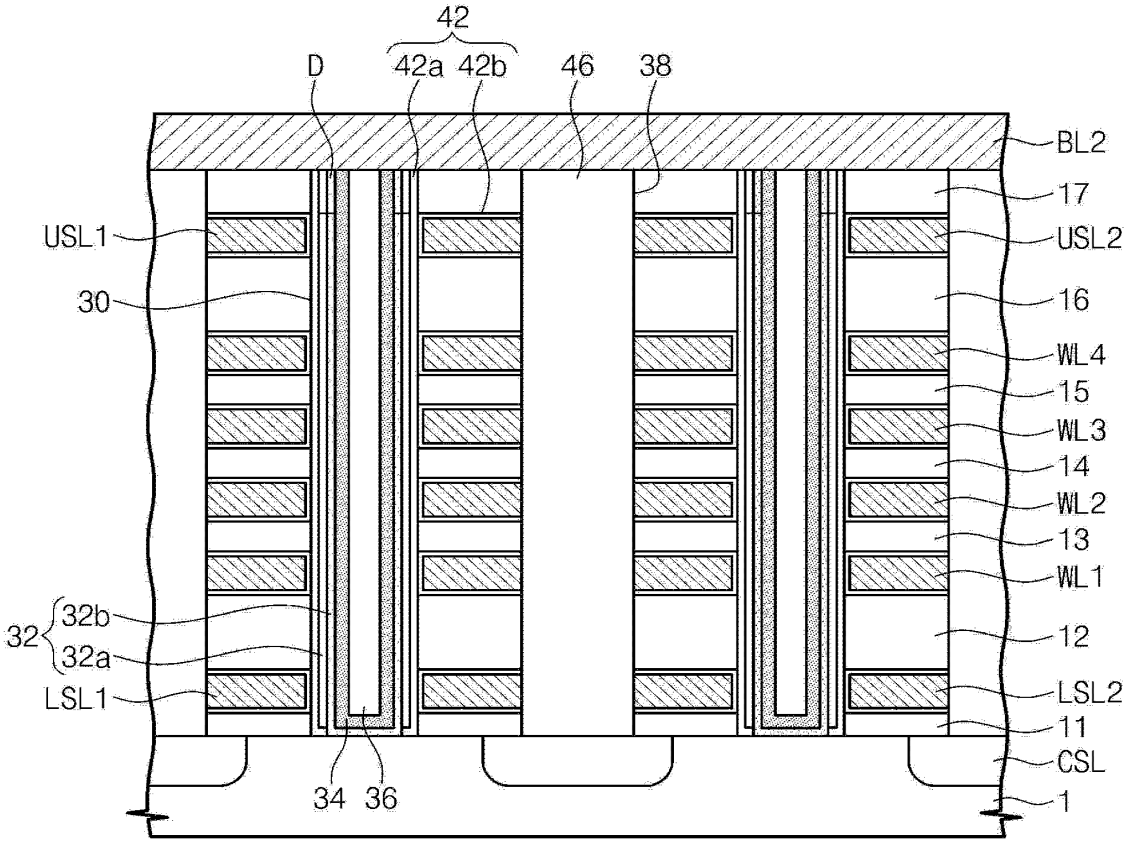


图 17

Micron Ex. 1002, p. 170
Micron v. YMTC
IPR2024-00793

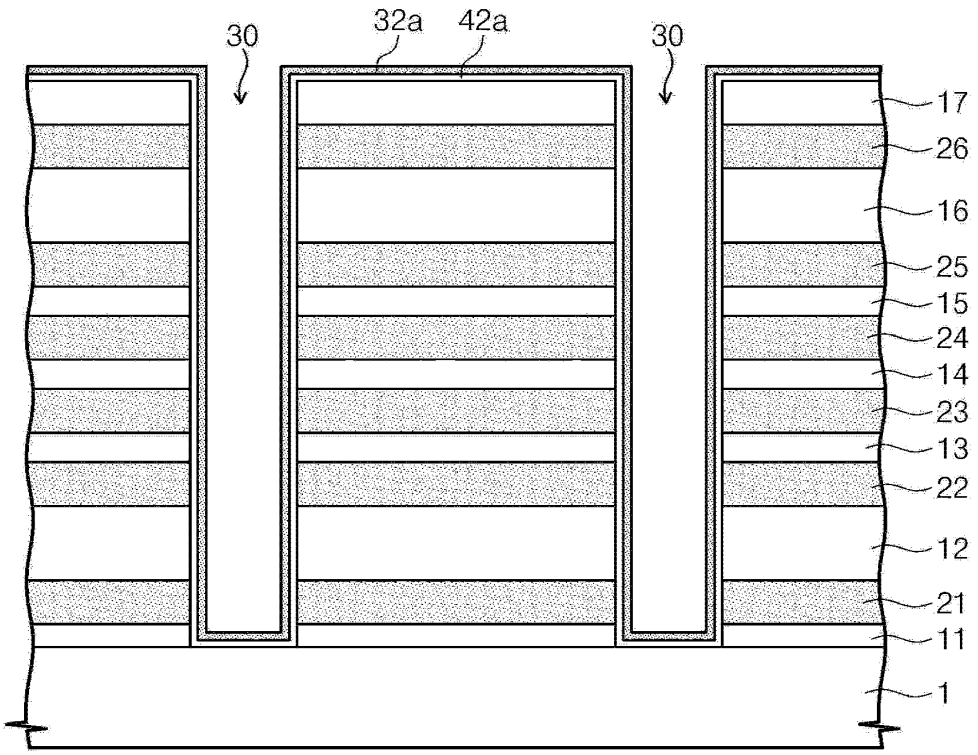


图 18

Micron Ex. 1002, p. 171
Micron v. YMTC
IPR2024-00793

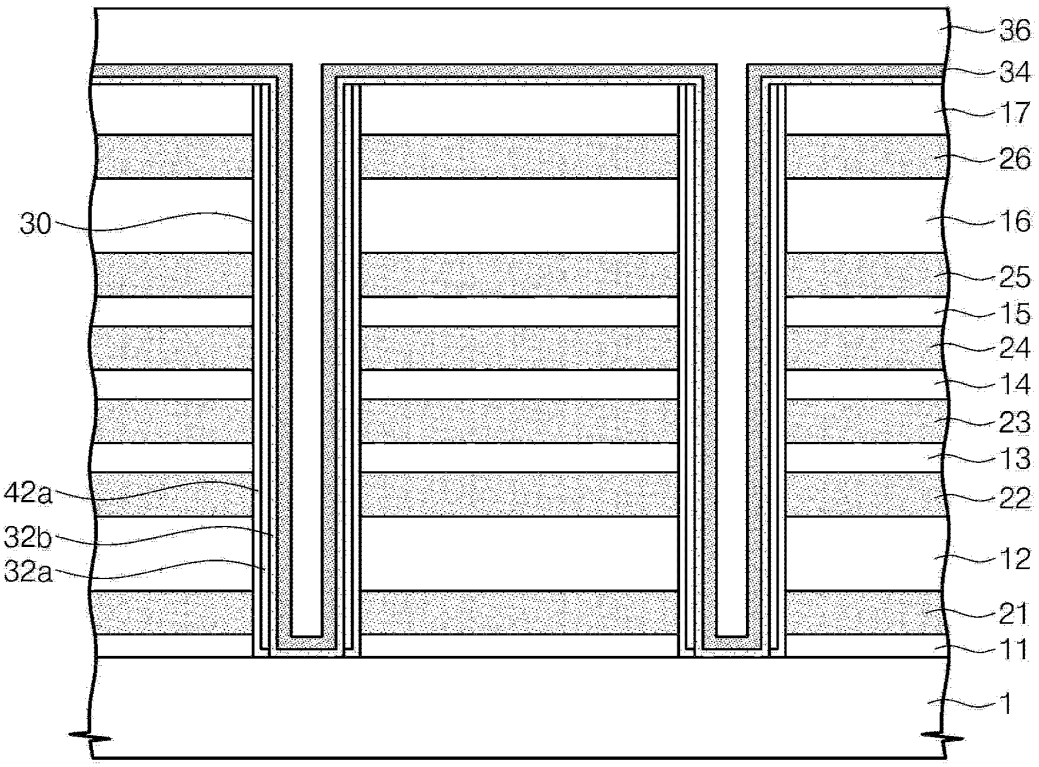


图 19

Micron Ex. 1002, p. 172
Micron v. YMTC
IPR2024-00793

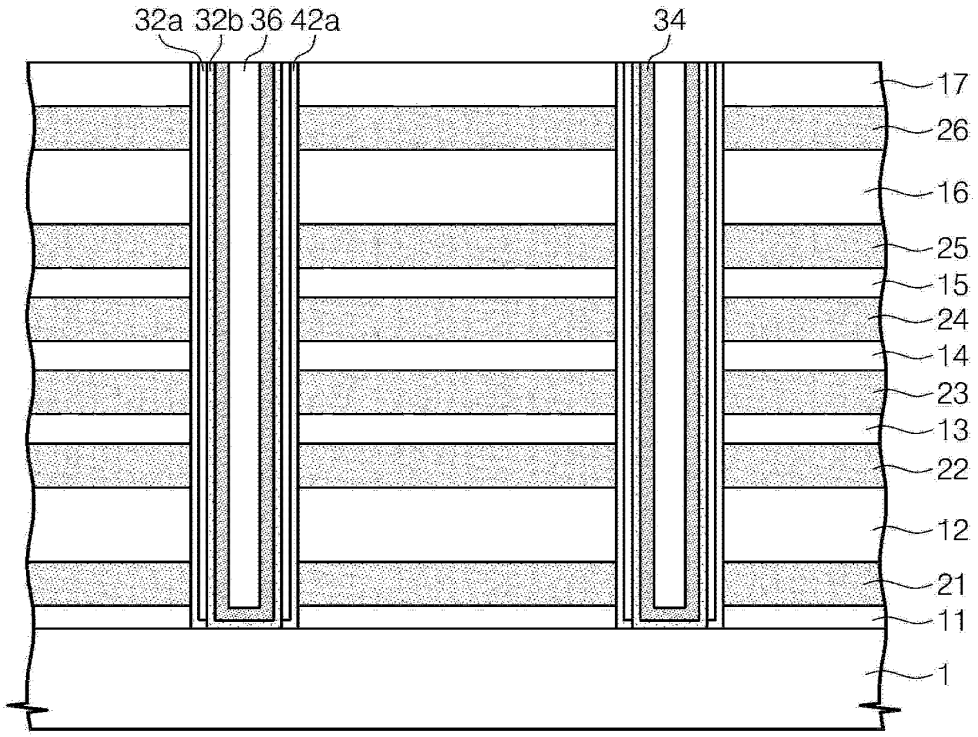


图 20

Micron Ex. 1002, p. 173
Micron v. YMTC
IPR2024-00793

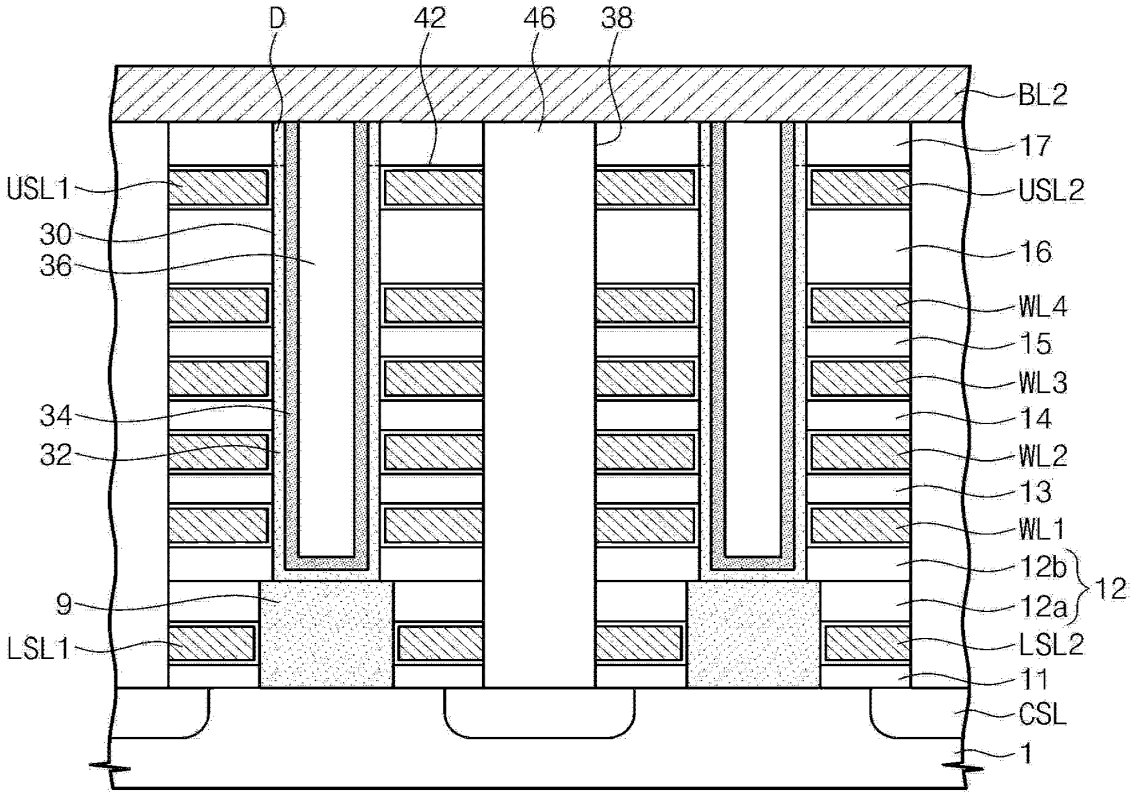


图 21

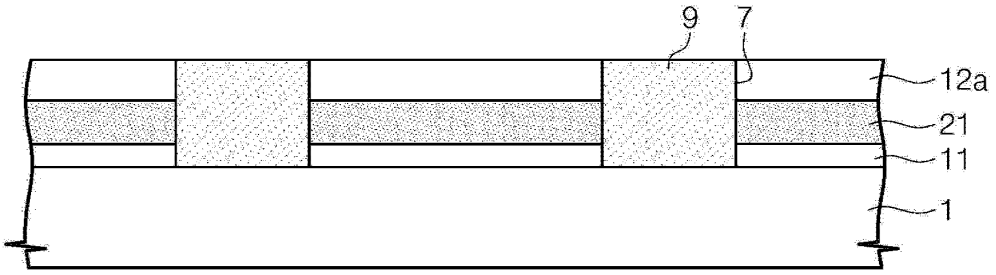


图 22

Micron Ex. 1002, p. 174
Micron v. YMTC
IPR2024-00793

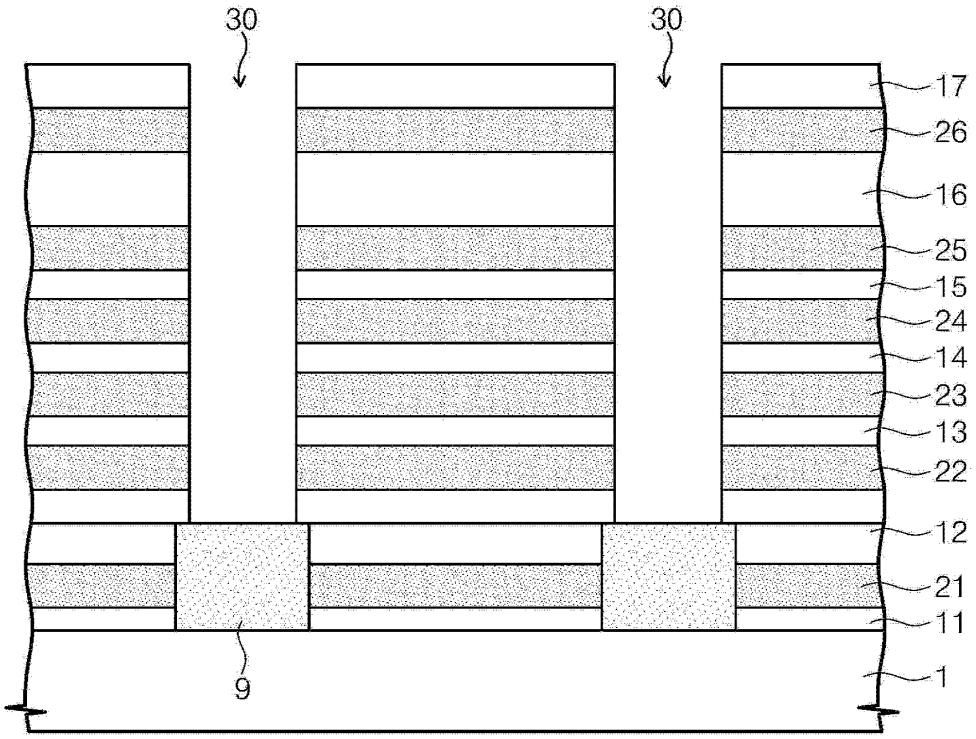


图 23

Micron Ex. 1002, p. 175
Micron v. YMTC
IPR2024-00793

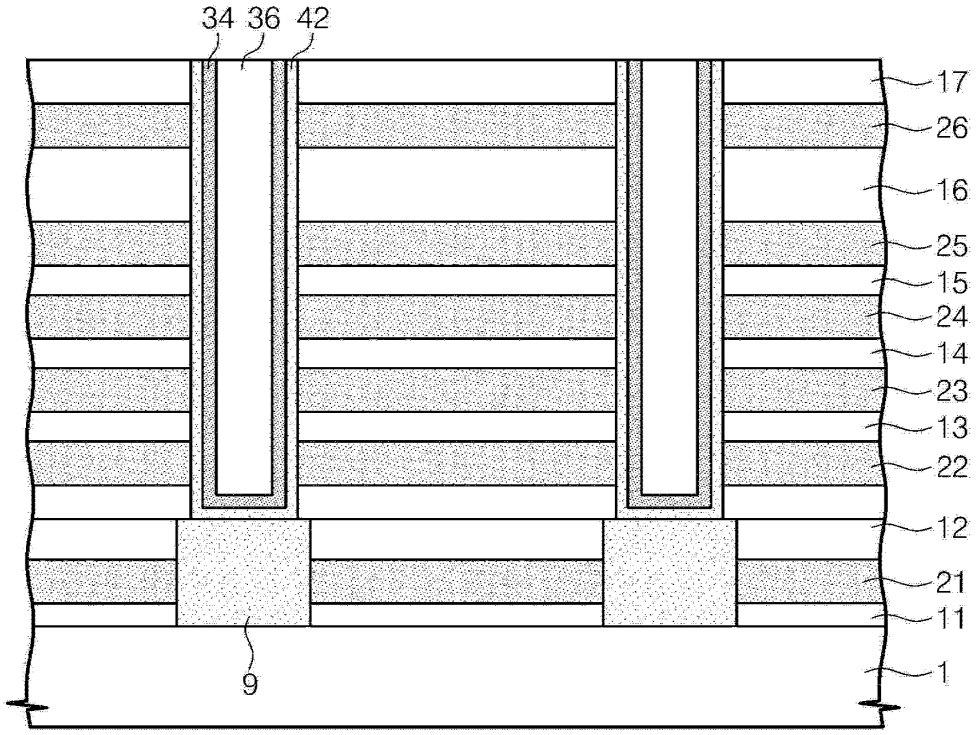


图 24

Micron Ex. 1002, p. 176
Micron v. YMTC
IPR2024-00793

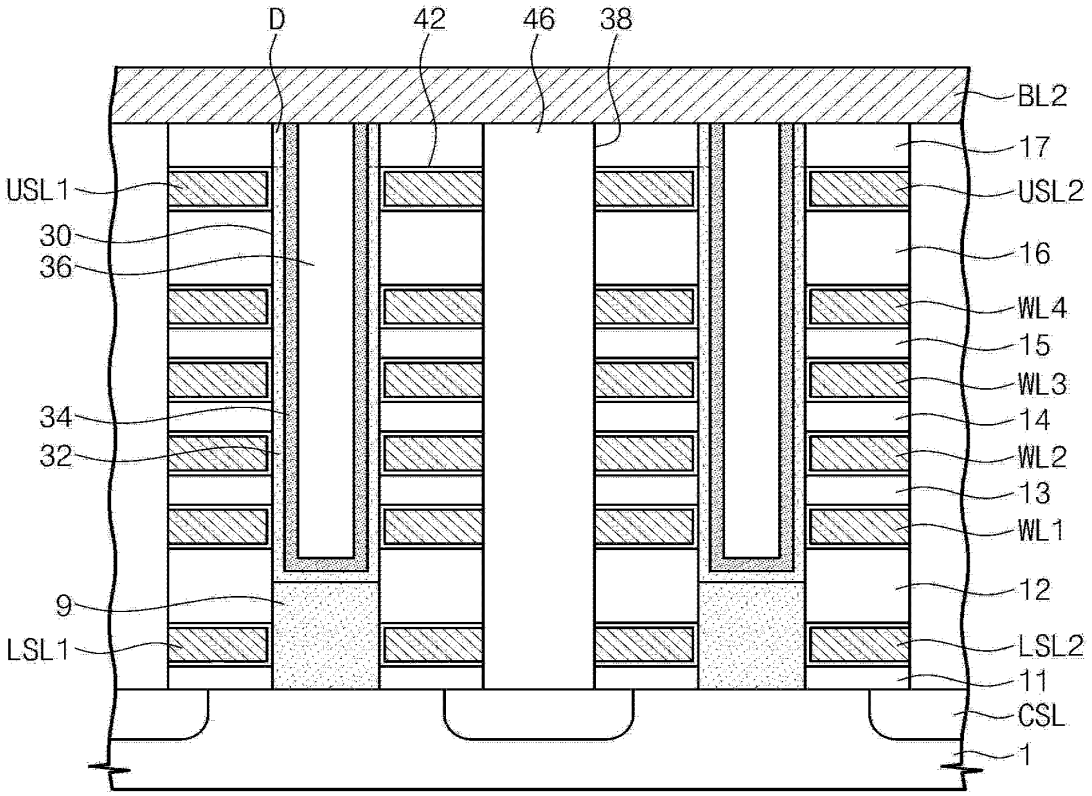


图 25

Micron Ex. 1002, p. 177
Micron v. YMTC
IPR2024-00793

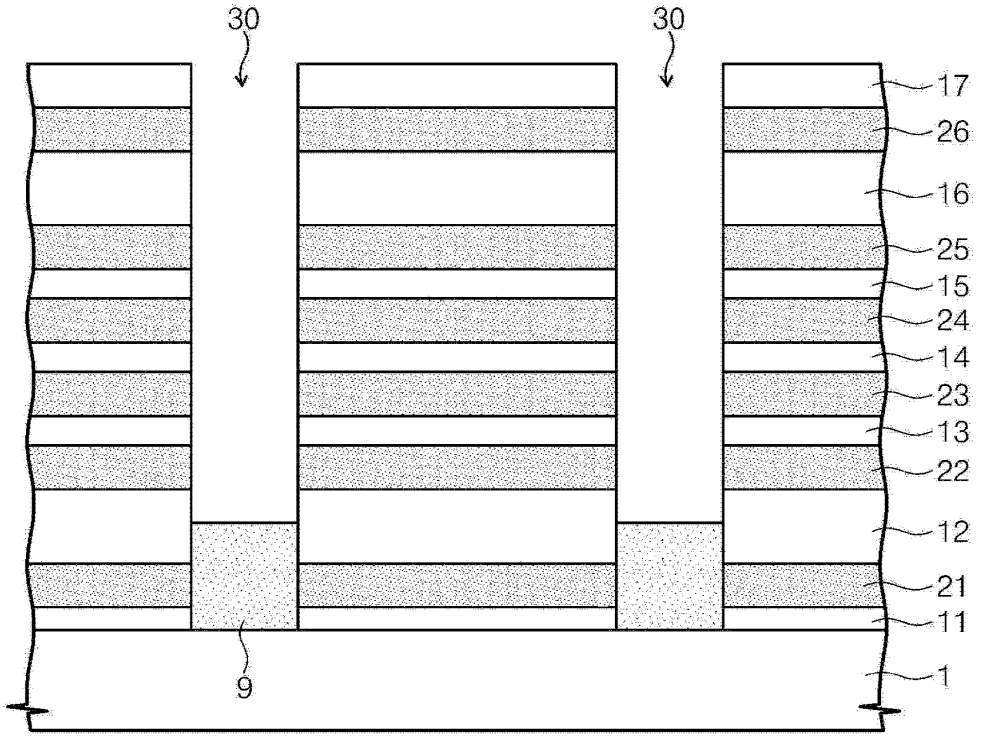


图 26

Micron Ex. 1002, p. 178
Micron v. YMTC
IPR2024-00793

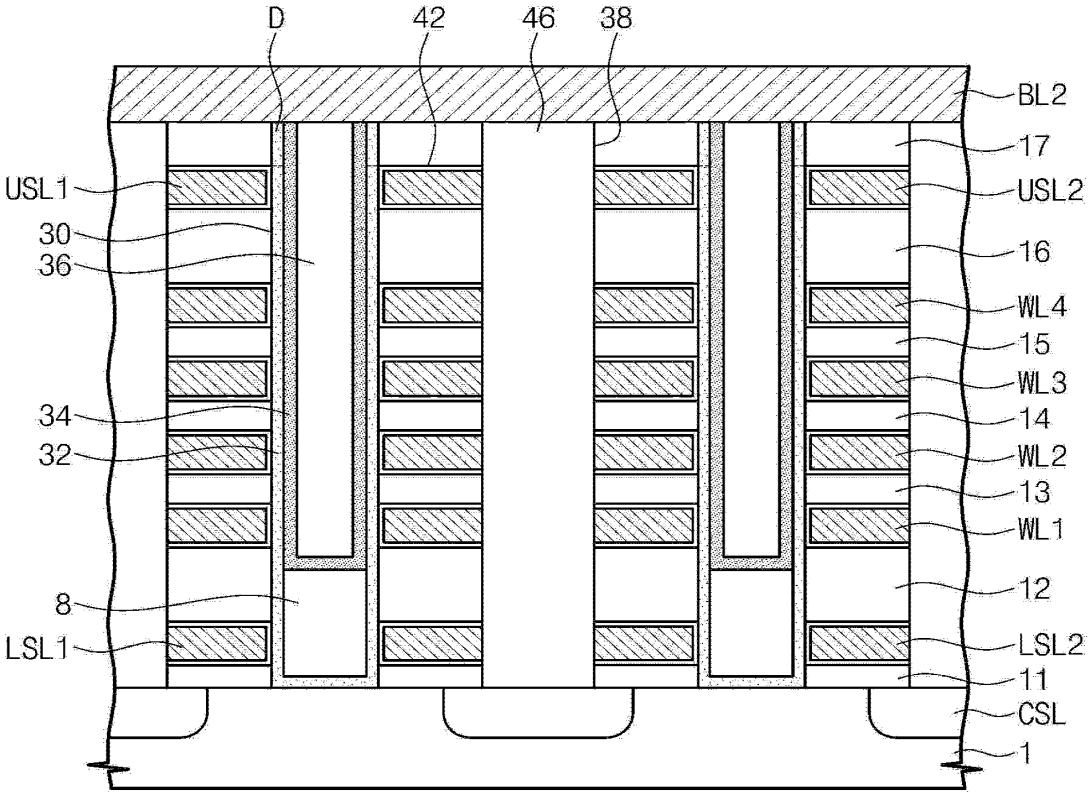


图 27

Micron Ex. 1002, p. 179
Micron v. YMTC
IPR2024-00793

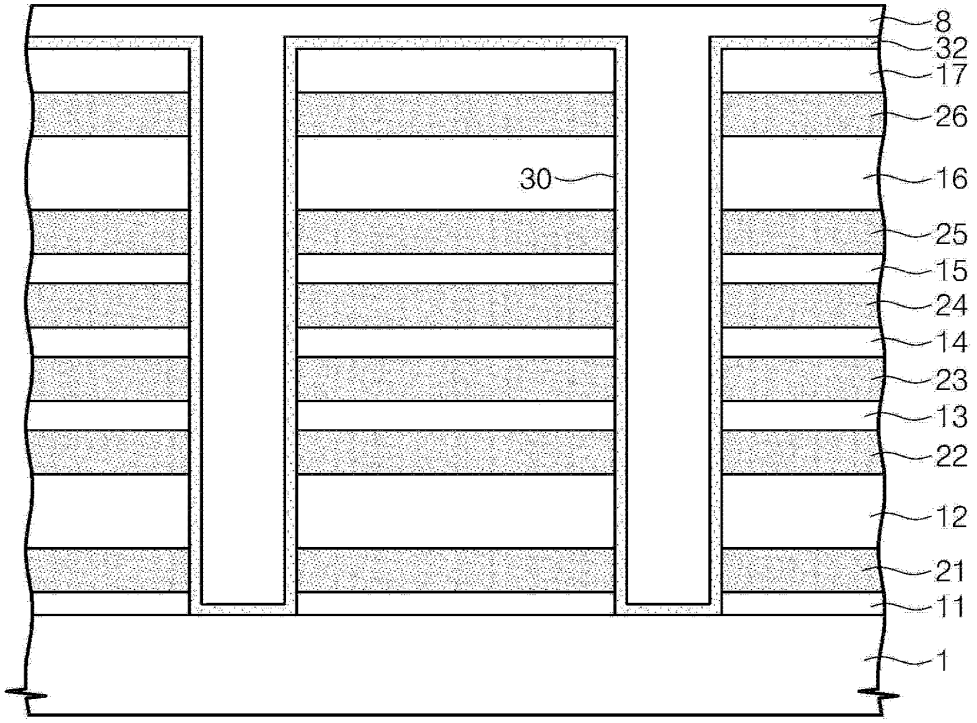


图 28

Micron Ex. 1002, p. 180
Micron v. YMTC
IPR2024-00793

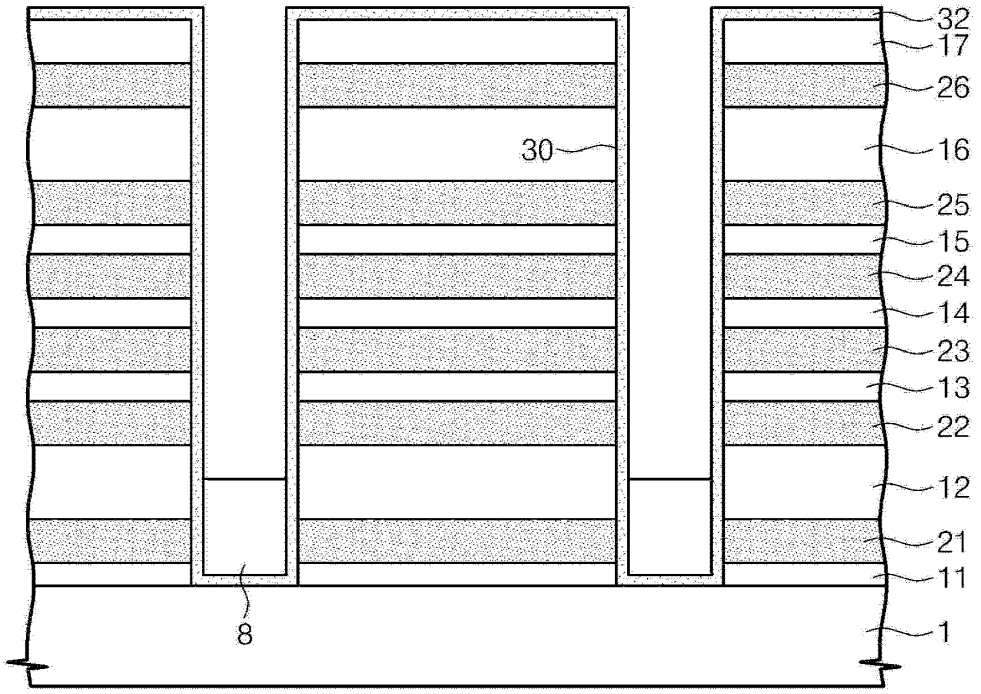


图 29

Micron Ex. 1002, p. 181
Micron v. YMTC
IPR2024-00793

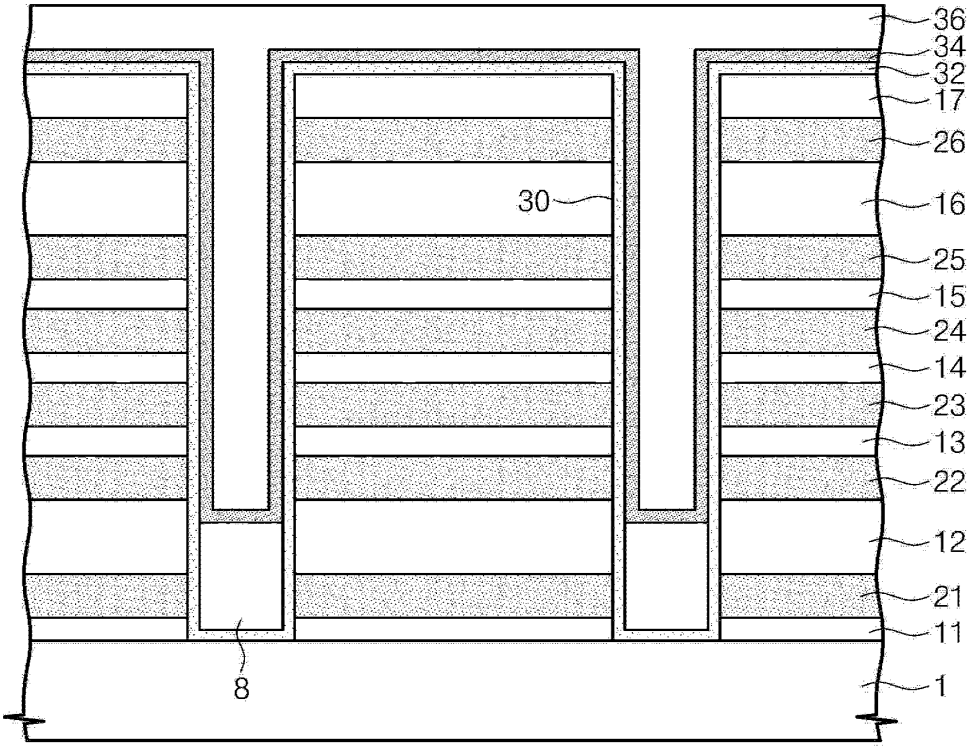


图 30

Micron Ex. 1002, p. 182
Micron v. YMTC
IPR2024-00793

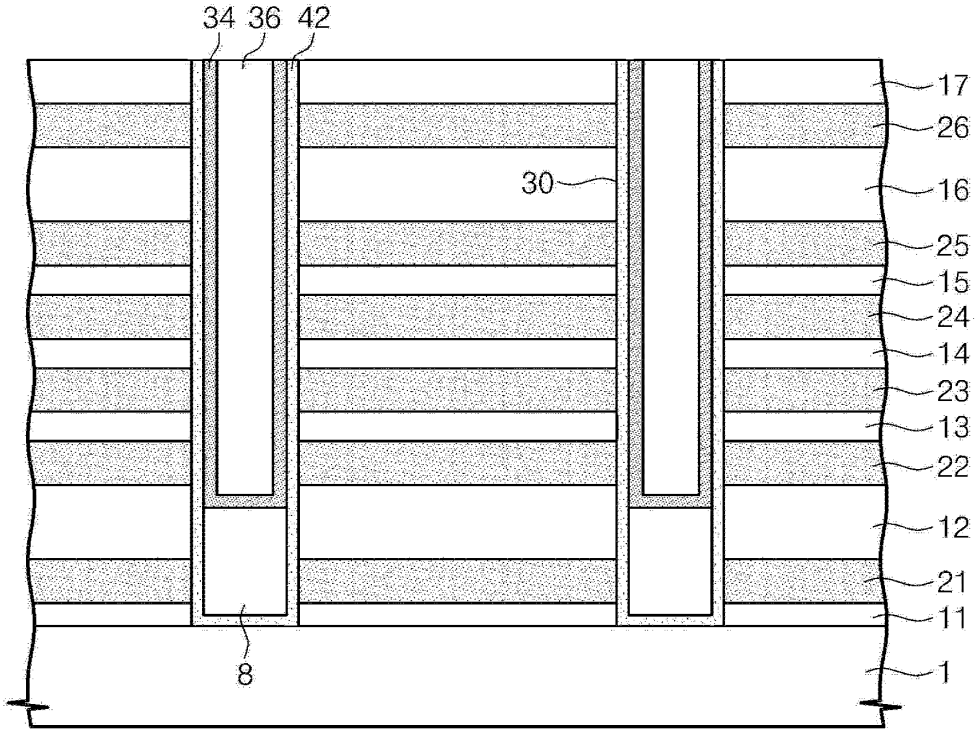


图 31

Micron Ex. 1002, p. 183
Micron v. YMTC
IPR2024-00793

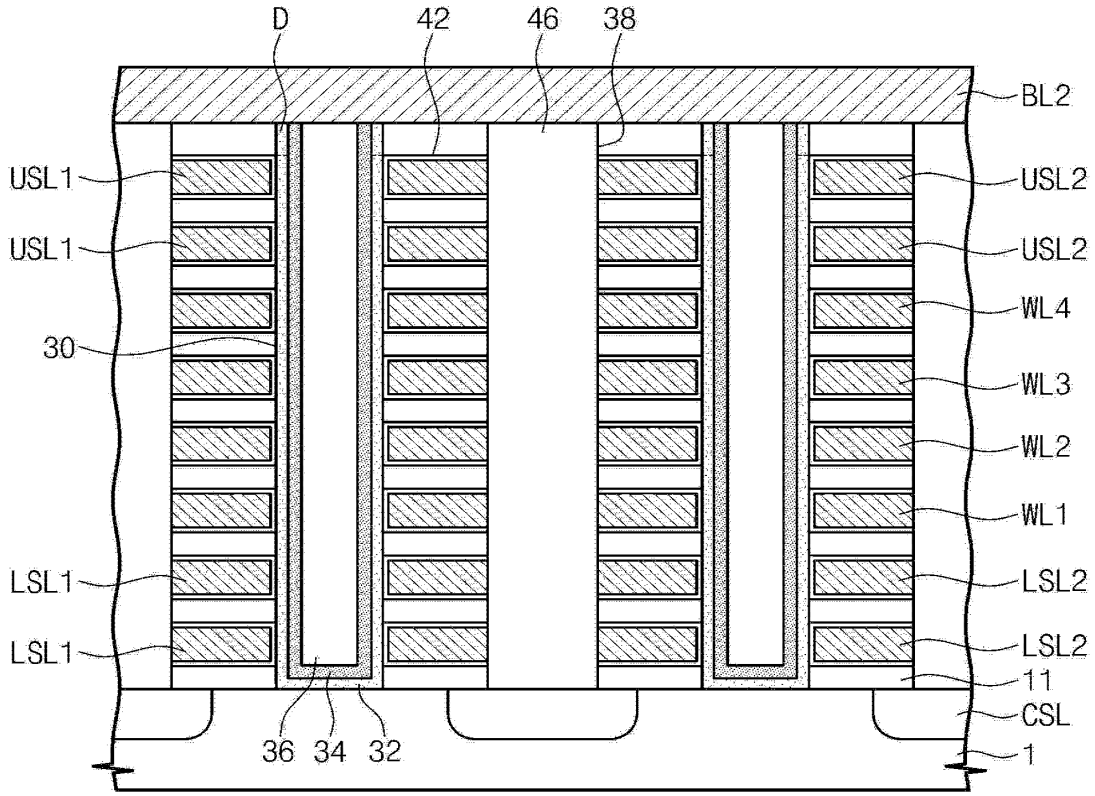


图 32

Micron Ex. 1002, p. 184
Micron v. YMTC
IPR2024-00793

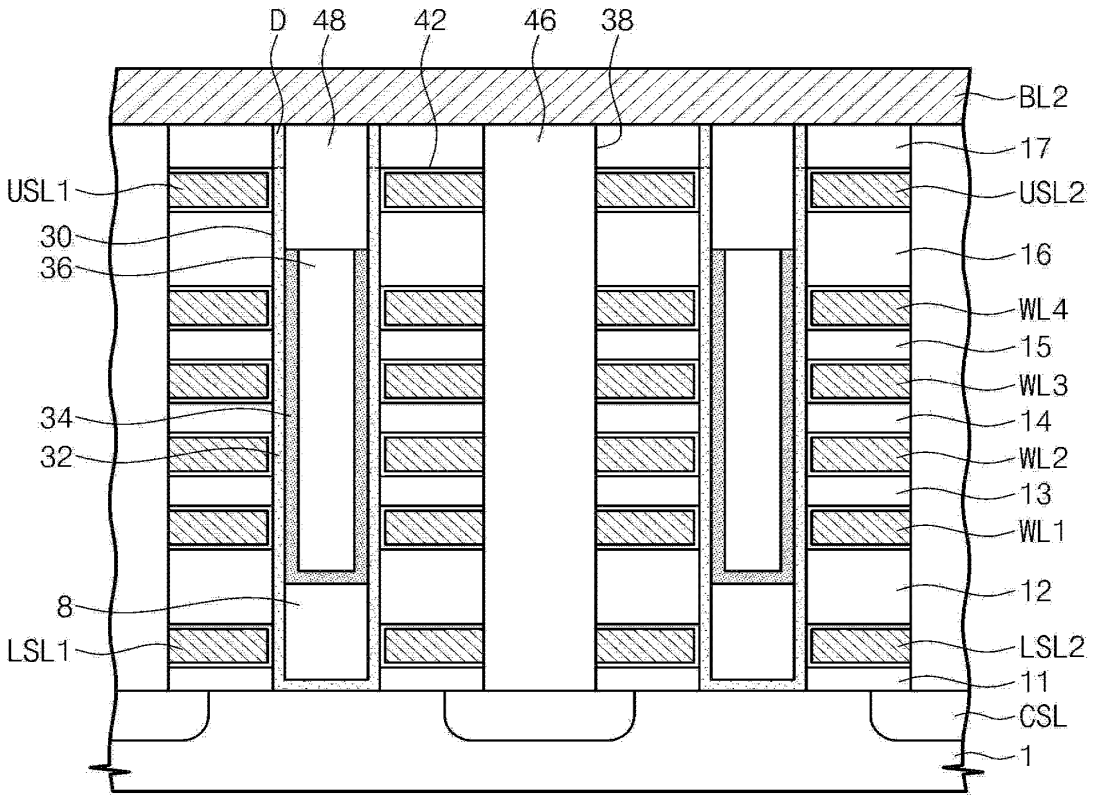


图 33

Micron Ex. 1002, p. 185
Micron v. YMTC
IPR2024-00793

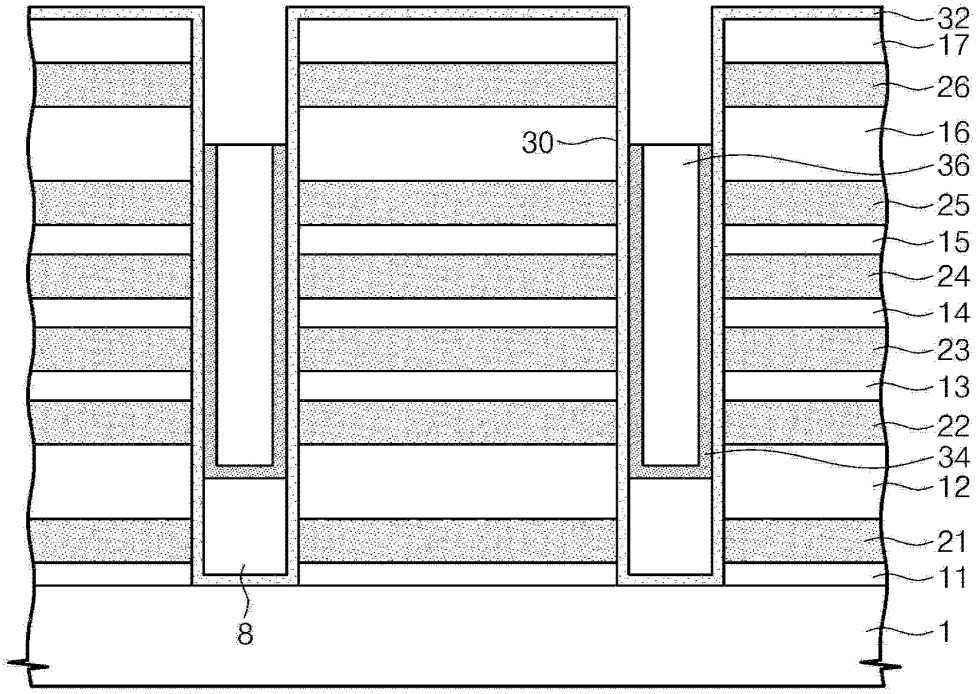


图 34

Micron Ex. 1002, p. 186
Micron v. YMTC
IPR2024-00793

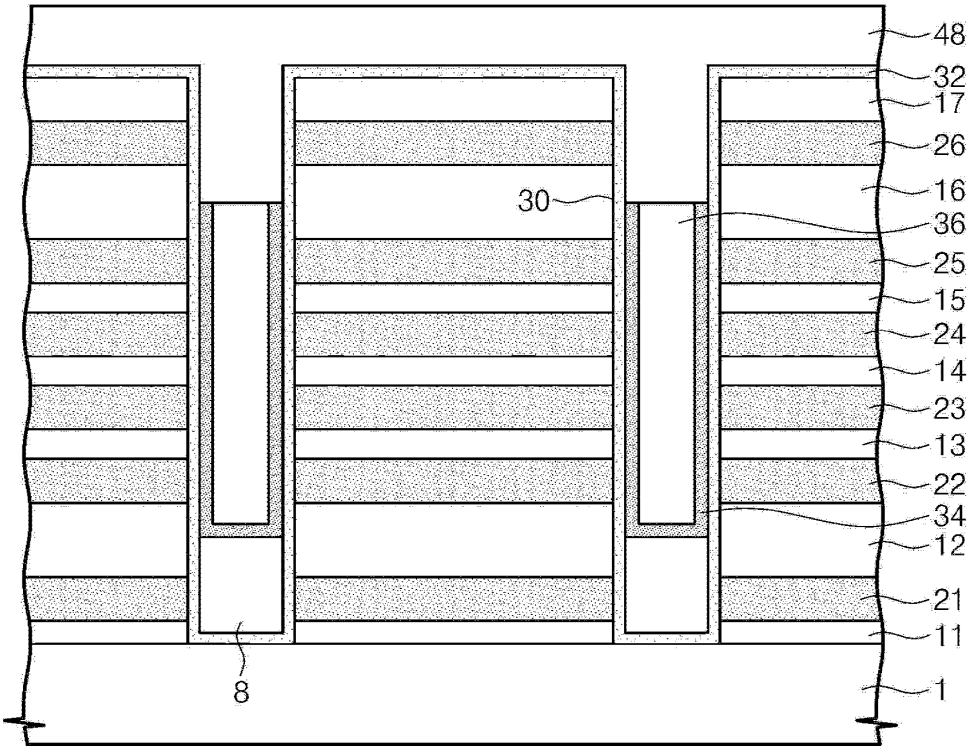


图 35

Micron Ex. 1002, p. 187
Micron v. YMTC
IPR2024-00793

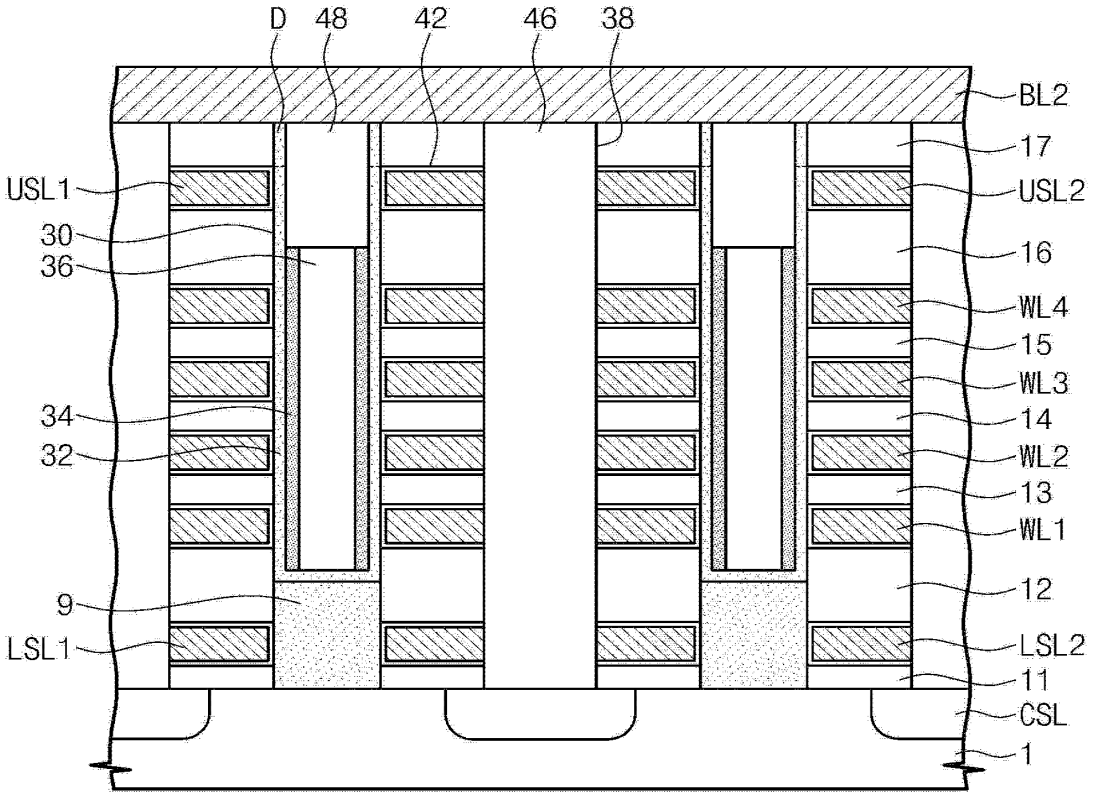


图 36

Micron Ex. 1002, p. 188
Micron v. YMTC
IPR2024-00793

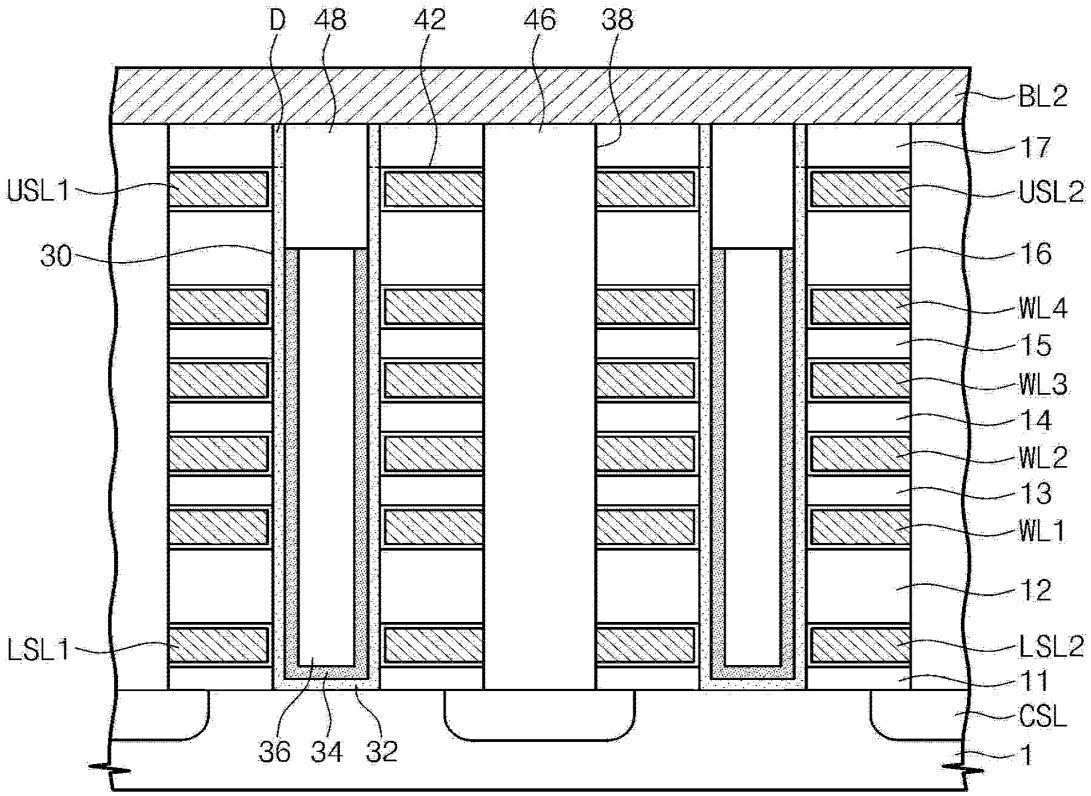


图 37

Micron Ex. 1002, p. 189
Micron v. YMTC
IPR2024-00793

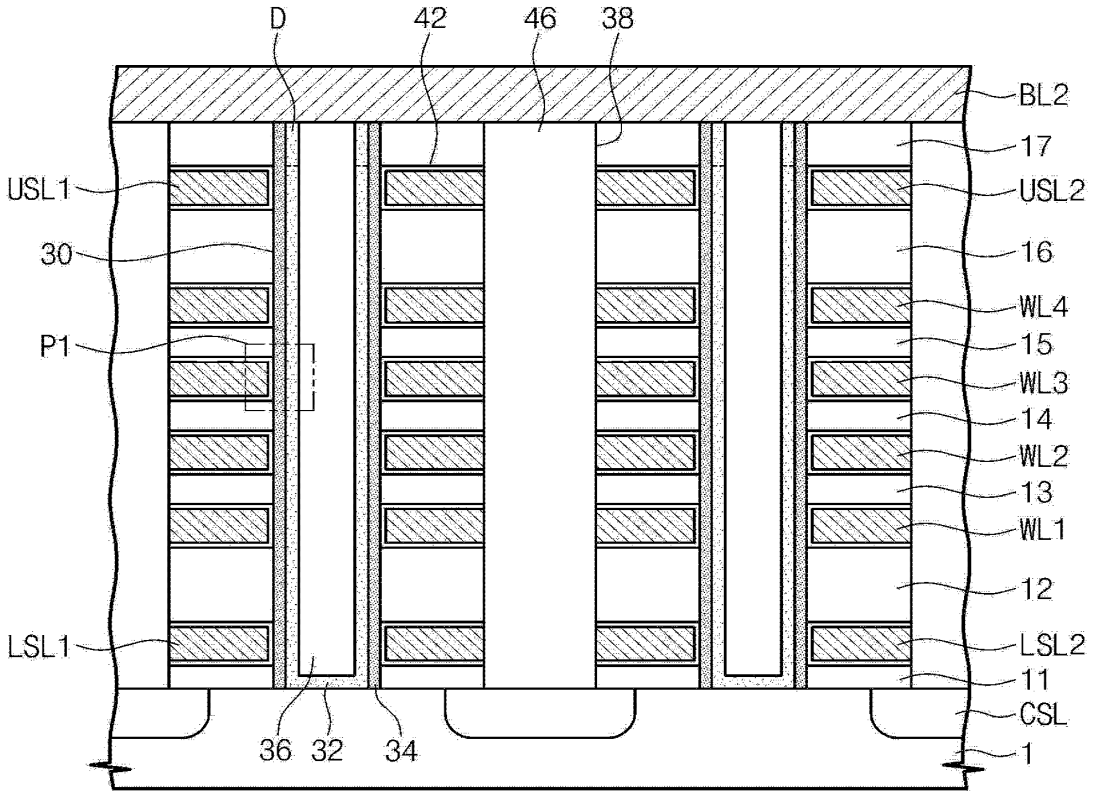


图 38

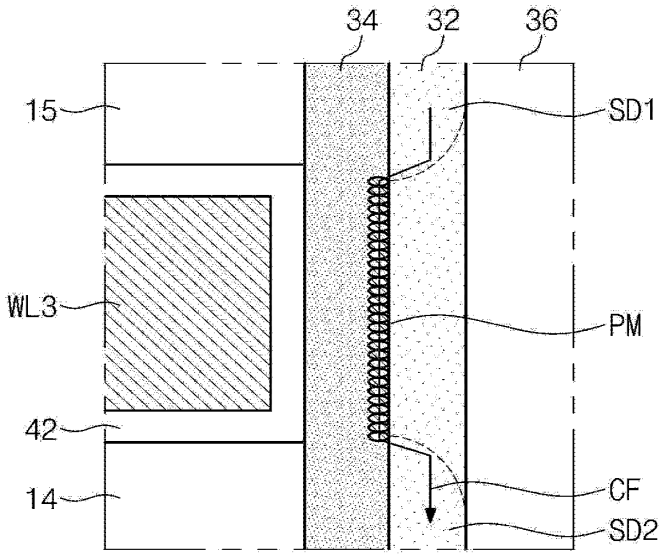


图 39

Micron Ex. 1002, p. 190
Micron v. YMTC
IPR2024-00793

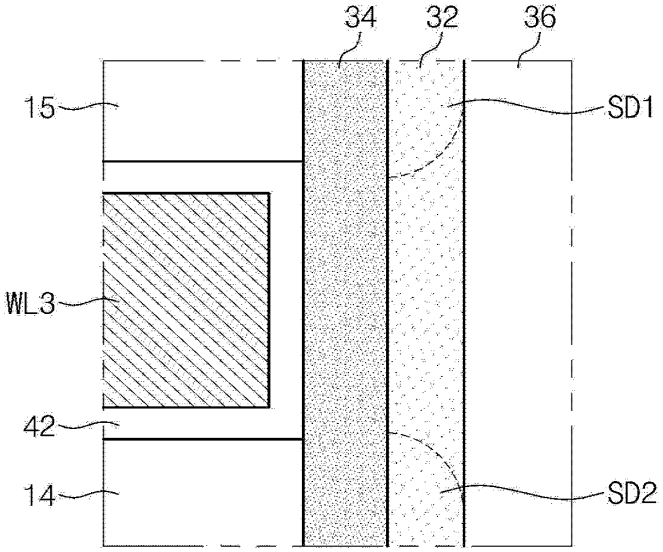


图 40

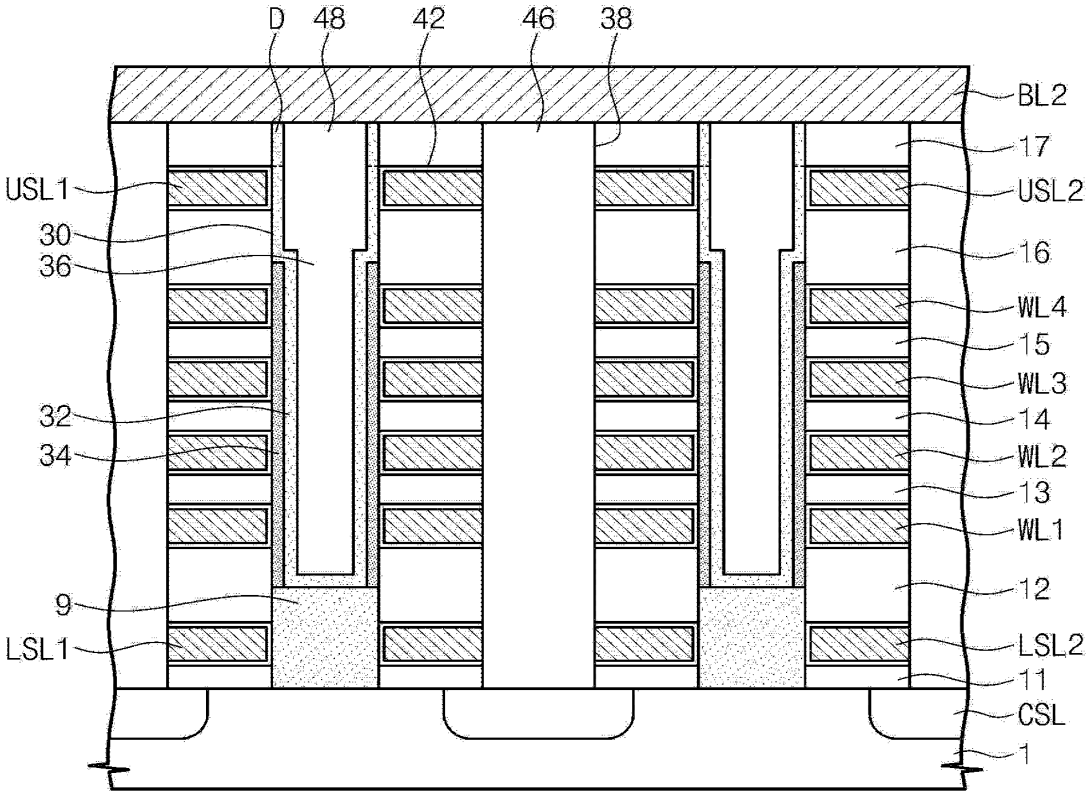


图 41

Micron Ex. 1002, p. 191
Micron v. YMTC
IPR2024-00793

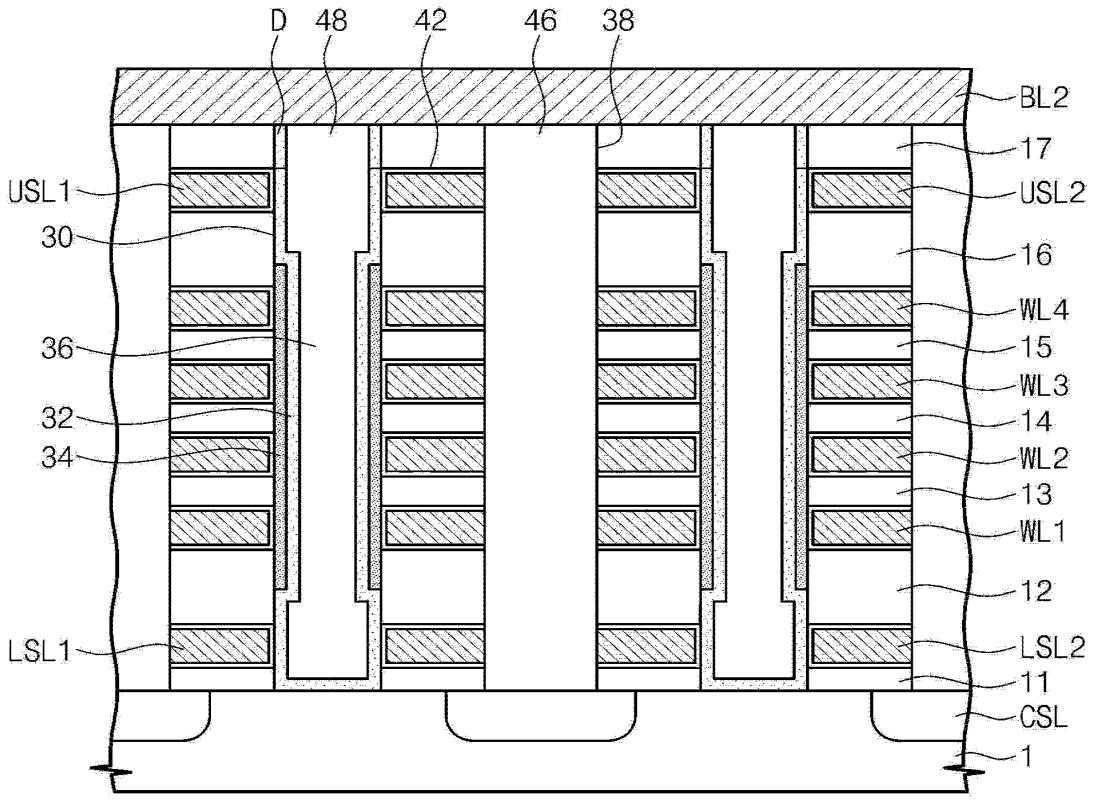


图 42

Micron Ex. 1002, p. 192
Micron v. YMTC
IPR2024-00793

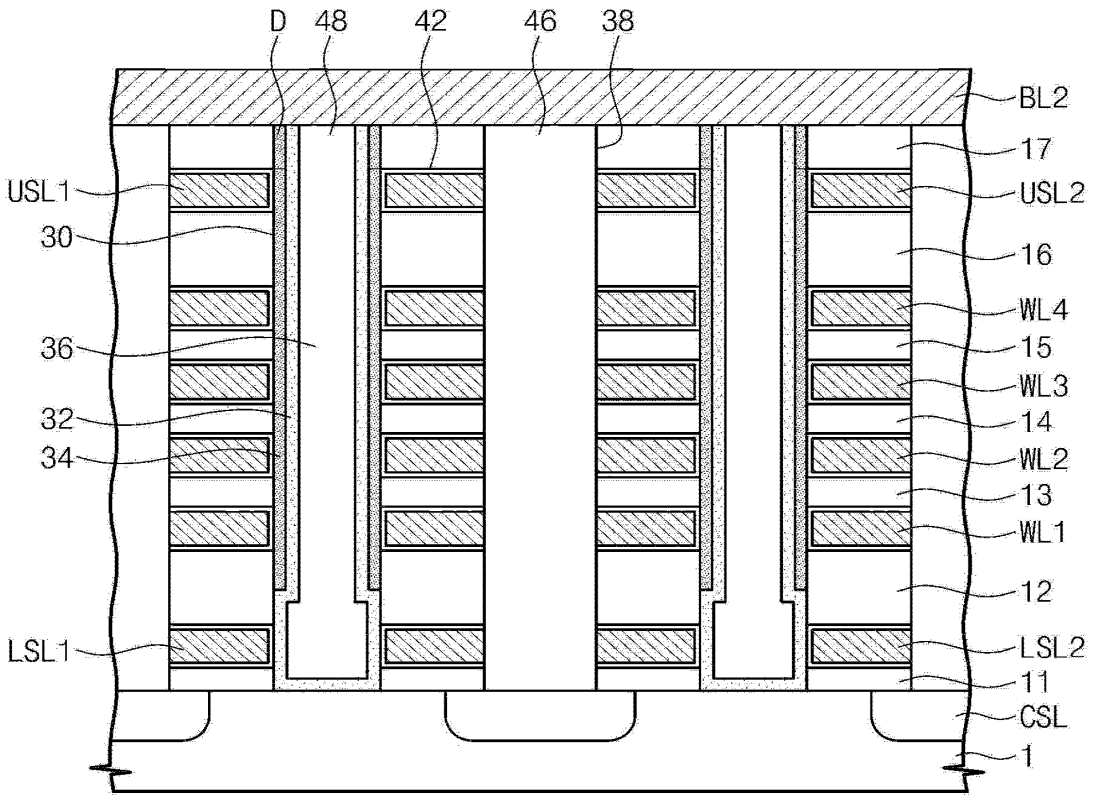


图 43

Micron Ex. 1002, p. 193
Micron v. YMTC
IPR2024-00793

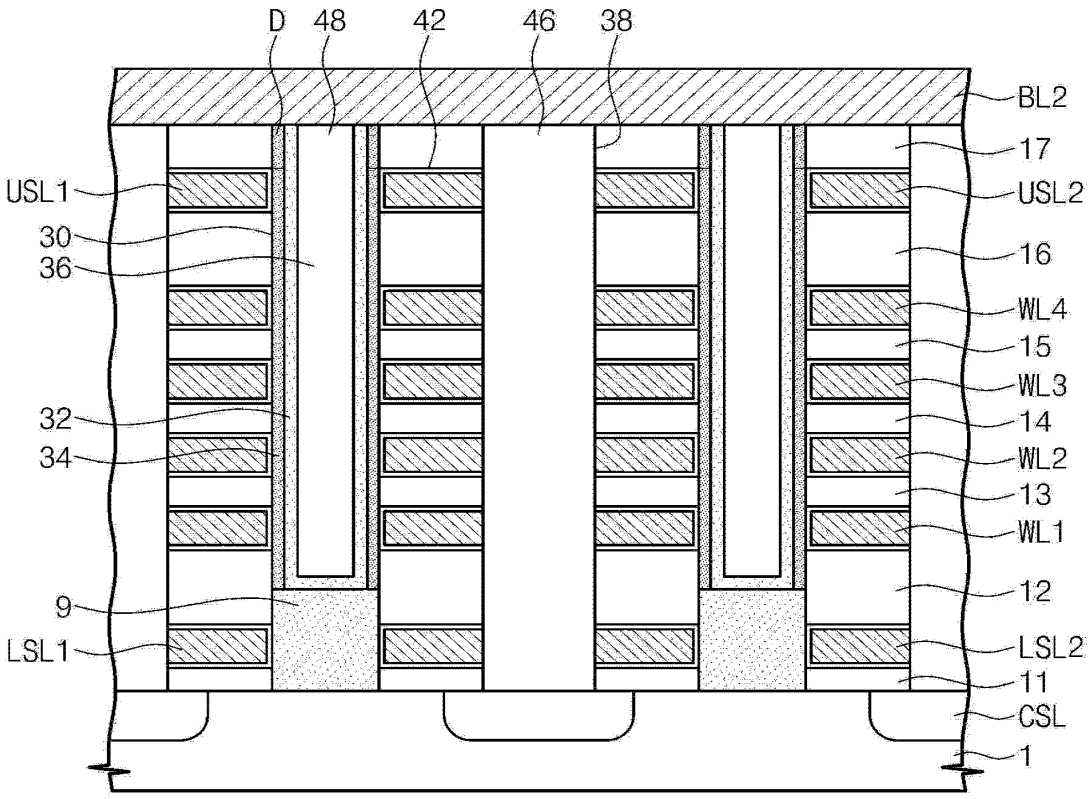


图 44

Micron Ex. 1002, p. 194
Micron v. YMTC
IPR2024-00793

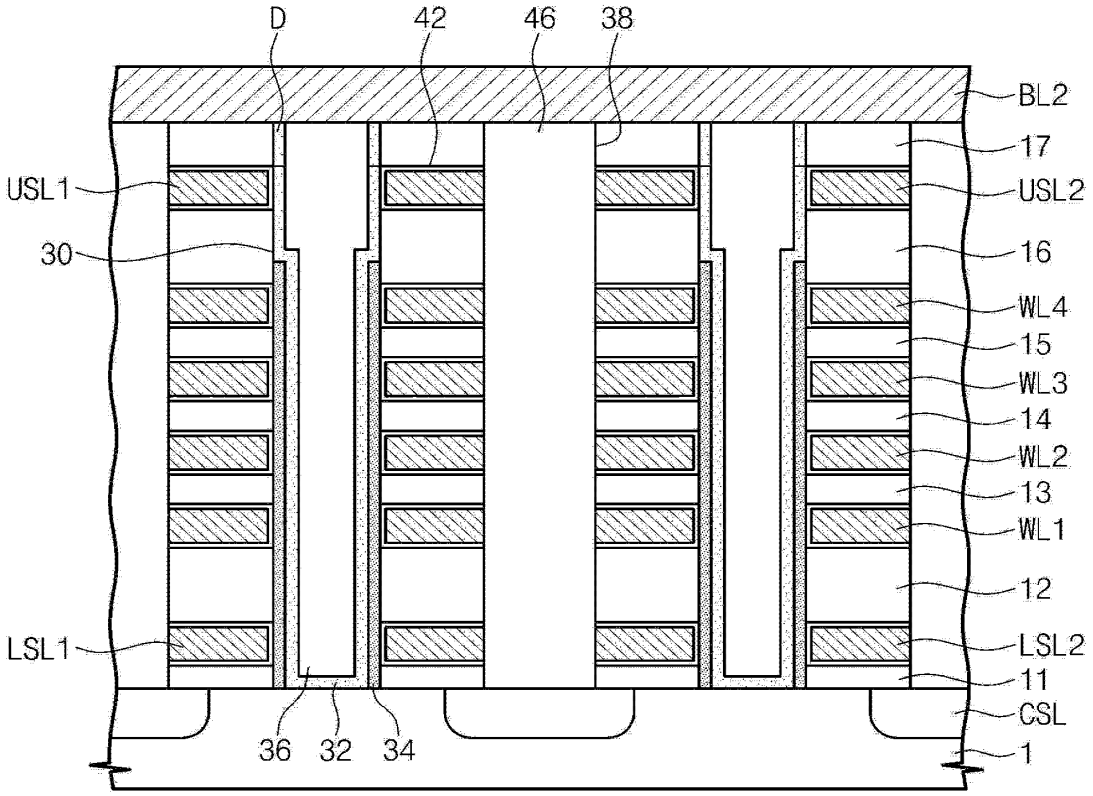


图 45

Micron Ex. 1002, p. 195
Micron v. YMTC
IPR2024-00793

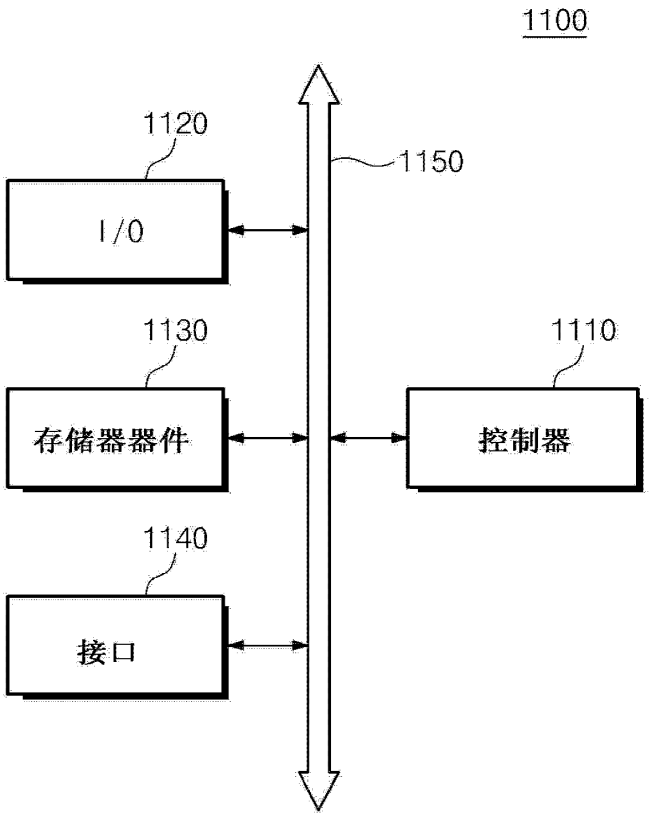


图 46

Micron Ex. 1002, p. 196
Micron v. YMTC
IPR2024-00793

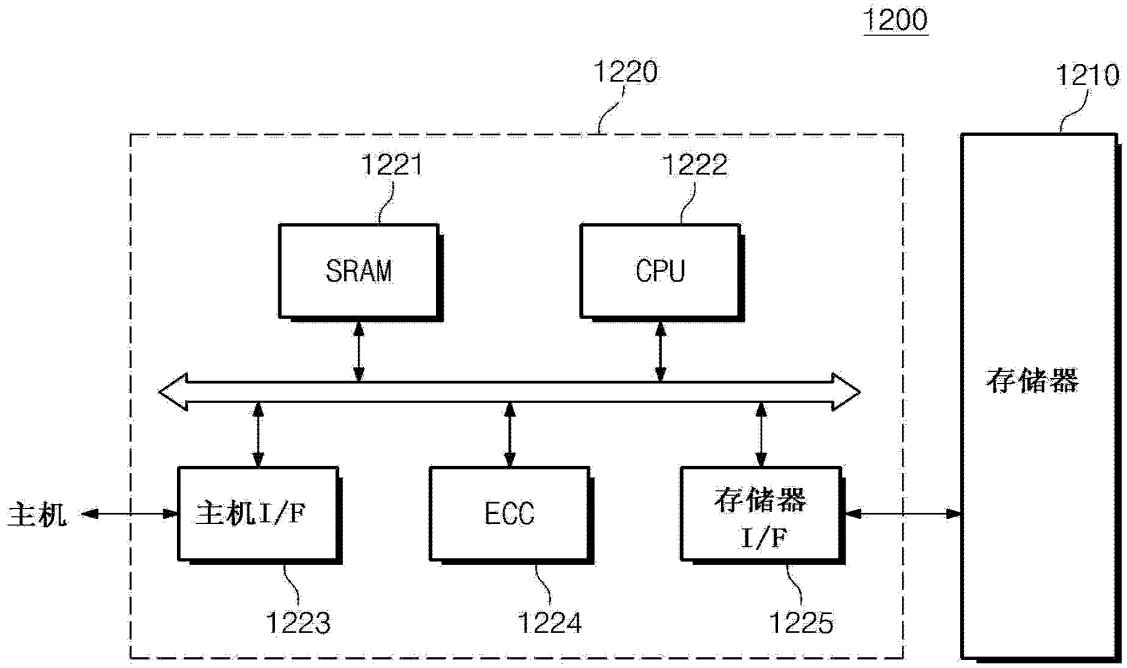


图 47

Micron Ex. 1002, p. 197
Micron v. YMTC
IPR2024-00793

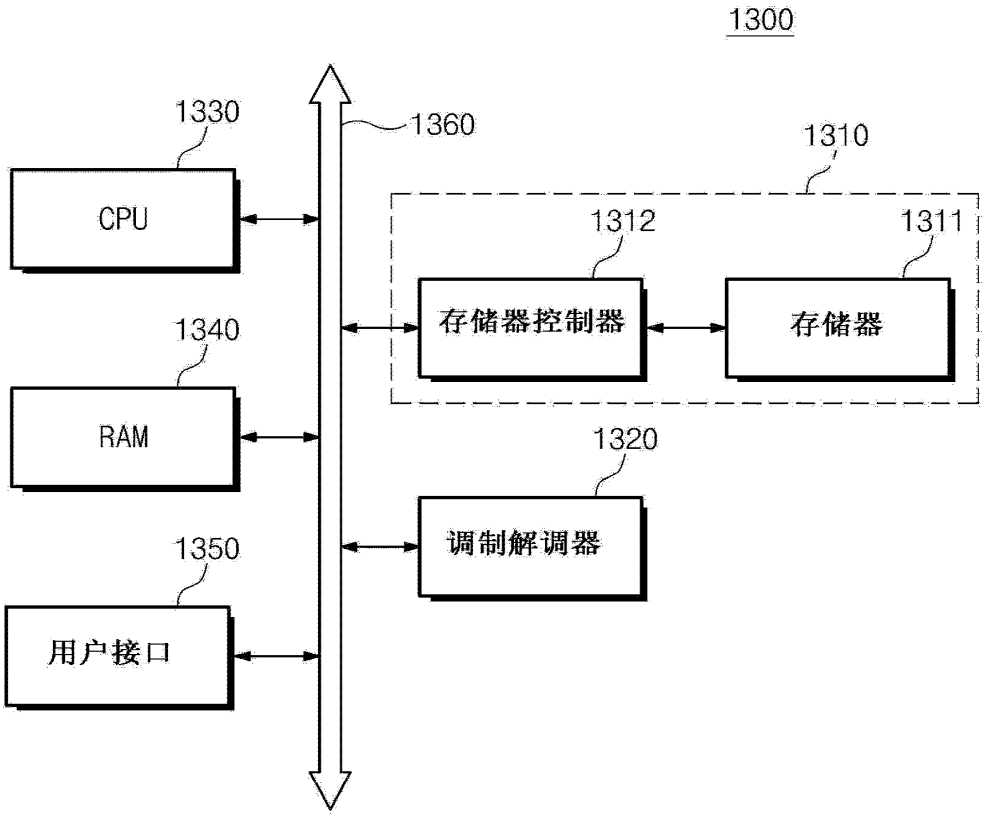


图 48

Micron Ex. 1002, p. 198
Micron v. YMTC
IPR2024-00793

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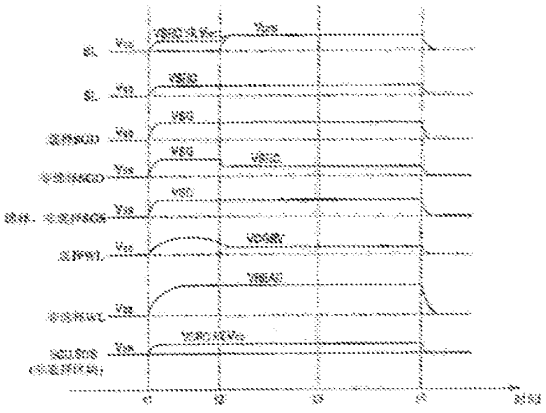
权利要求书1页 说明书12页 附图13页

(54)发明名称

半导体存储装置

(57)摘要

本发明的实施方式抑制非选择存储串的读取干扰。实施方式的半导体存储装置具备存储串，该存储串具有第1及第2选择晶体管以及多个存储单元。在读取动作中，对源极线施加高于接地电压的第1电压，对连接在所选择的存储串的第1及第2选择栅极线，施加将第1及第2选择晶体管设为接通状态的第2电压。在读取动作的第1期间，对连接在非选择的存储串的第1选择栅极线施加第2电压，在读取动作的继第1期间之后的第2期间，对连接在非选择的存储串的第1选择栅极线施加第3电压，该第3电压高于接地电压，并且为对第1电压加上第1选择晶体管的阈值之后的电压以下。



CN 107170746 A

Micron Ex. 1002, p. 199
Micron v. YMTC
IPR2024-00793

1.一种半导体存储装置，其特征在于，具备：

存储单元阵列，具备多个存储串，所述多个存储串分别具备第1及第2选择晶体管、以及在所述第1及第2选择晶体管之间串联连接并且积层的多个存储单元；

多条字线，分别连接在所述多个存储单元；

位线，共通连接在所述多个第1选择晶体管；

多个第1选择栅极线，分别连接在所述多个第1选择晶体管的栅极；

多个第2选择栅极线，分别连接在所述多个第2选择晶体管的栅极；以及

源极线，共通连接在所述多个第2选择晶体管；且

在读取动作中，对所述源极线施加高于接地电压的第1电压，

在所述读取动作中，对连接在所选择的存储串的第1及第2选择栅极线，施加将所述第1及第2选择晶体管设为接通状态的第2电压，

在所述读取动作的第1期间，对连接在非选择的存储串的第1选择栅极线施加所述第2电压，

在所述读取动作的继所述第1期间之后的第2期间，对连接在所述非选择的存储串的第1选择栅极线施加第3电压，该第3电压高于所述接地电压，并且为对所述第1电压加上所述第1选择晶体管的阈值所得的电压以下。

2.根据权利要求1所述的半导体存储装置，其特征在于：所述第3电压与所述第1电压相同。

3.根据权利要求1或2所述的半导体存储装置，其特征在于：在所述读取动作中，对连接在所述非选择的存储串的第2选择栅极线施加所述第2电压。

4.根据权利要求1或2所述的半导体存储装置，其特征在于：在所述第1期间，对连接在所述非选择的存储串的第2选择栅极线施加所述第2电压，

在所述第2期间，对连接在所述非选择的存储串的第2选择栅极线施加所述第3电压，且

在所述读取动作的继所述第2期间之后的第3期间，对连接在所述非选择的存储串的第2选择栅极线施加所述第2电压。

5.根据权利要求1或2所述的半导体存储装置，其特征在于：在所述第1期间，对非选择的字线施加将存储单元设为接通状态的第4电压。

6.根据权利要求1或2所述的半导体存储装置，其特征在于：在所述第1期间，对所述位线施加所述第1电压，或使所述位线为浮动状态。

7.根据权利要求1或2所述的半导体存储装置，其特征在于：所述多个第2选择栅极线作为1条第2选择栅极线而被共有。

Micron Ex. 1002, p. 200
Micron v. YMTC
IPR2024-00793

半导体存储装置

[0001] [相关申请]

[0002] 本申请享有以日本专利申请2016-40290号(申请日:2016年3月2日)为基础申请的优先权。本申请通过参照该基础申请而包含基础申请的全部内容。

技术领域

[0003] 实施方式涉及一种半导体存储装置。

背景技术

[0004] 作为非易失性半导体存储装置,已知有NAND(Not-AND,与非)型闪速存储器。

发明内容

[0005] 实施方式提供一种能够抑制非选择存储串的读取干扰的半导体存储装置。

[0006] 实施方式的半导体存储装置具备:存储单元阵列,具备多个存储串,所述多个存储串分别具备第1及第2选择晶体管、以及在所述第1及第2选择晶体管之间串联连接并且积层的多个存储单元;多条字线,分别连接在所述多个存储单元;位线,共通连接在所述多个第1选择晶体管;多个第1择栅极线,分别连接在所述多个第1选择晶体管的栅极;多个第2选择栅极线,分别连接在所述多个第2选择晶体管的栅极;以及源极线,共通连接在所述多个第2选择晶体管。在读取动作中,对所述源极线施加高于接地电压的第1电压,在所述读取动作中,对连接在所选择的存储串的第1及第2选择栅极线,施加将所述第1及第2选择晶体管设为接通状态的第2电压。在所述读取动作的第1期间,对连接在非选择的存储串的第1选择栅极线施加所述第2电压,在所述读取动作的继所述第1期间之后的第2期间,对连接在所述非选择的存储串的第1选择栅极线施加第3电压,该第3电压高于所述接地电压,并且为对所述第1电压加上所述第1择晶体管的阈值所得的电压以下。

附图说明

[0007] 图1是本实施方式的NAND型闪速存储器的框图。

[0008] 图2是存储单元阵列的框图。

[0009] 图3是存储单元阵列所含的1个区块的电路图。

[0010] 图4是区块的一部分区域的剖视图。

[0011] 图5是说明虚设单元晶体管的电路图。

[0012] 图6是读出放大器部及数据高速缓冲存储器的框图。

[0013] 图7是读出放大器部的电路图。

[0014] 图8是行解码器的电路图。

[0015] 图9是说明区块选择动作的示意图。

[0016] 图10是说明本实施方式的NAND型闪速存储器的读取动作的时序图。

[0017] 图11是说明比较例的读取动作的时序图。

Micron Ex. 1002, p. 201
Micron v. YMTC
IPR2024-00793

[0018] 图12(a)、(b)是用来说明读取干扰的示意性能带图。

[0019] 图13是说明本实施方式的NAND型闪速存储器的读取动作的时序图。

[0020] 图14是说明比较例的读取动作的时序图。

具体实施方式

[0021] 以下，参照附图，对实施方式进行说明。

[0022] 本实施方式的半导体存储装置是能够电改写数据的非易失性半导体存储器，在以下的实施方式中，作为半导体存储装置，列举NAND型闪速存储器为例进行说明。

[0023] [1]NAND型闪速存储器的构成

[0024] 图1是本实施方式的NAND型闪速存储器10的框图。NAND型闪速存储器10具备存储单元阵列11、行解码器12、列解码器13、读出放大器部14、数据高速缓冲存储器(数据锁存电路)15、核心驱动器16、电压产生电路17、输入输出电路18、地址寄存器19、控制器20及状态寄存器21。

[0025] 存储单元阵列11具备多个区块，多个区块分别具备多个存储单元晶体管(有时也简称为存储单元)。存储单元晶体管包含能够电改写的EEPROM(注册商标)单元。为了控制施加到存储单元晶体管的电压，而在存储单元阵列11配设着多条位线、多条字线及源极线。关于存储单元阵列11的详细情况，将在后文进行叙述。

[0026] 行解码器12从地址寄存器19接收区块地址信号及行地址信号，基于这些信号，选择对应的区块内的任一字线。列解码器13从地址寄存器19接收列地址信号，基于该列地址信号，选择任一位线。

[0027] 读出放大器部14在读取数据时，侦测及放大从存储单元读取到位线的数据。另外，读出放大器部14在写入数据时，将写入数据传送到位线。对存储单元阵列11读取数据及写入数据是以多个存储单元为单位而进行，该单位成为页。

[0028] 数据高速缓冲存储器15以页单位保存数据。数据高速缓冲存储器15在读取数据时，暂时保存从读出放大器部14以页单位传送的数据，并将其串行地向输入输出电路18传送。另外，数据高速缓冲存储器15在写入数据时，暂时保存从输入输出电路18串行地传送的数据，并将其以页单位向读出放大器部14传送。

[0029] 核心驱动器16将数据的写入、读取及删除所需的电压供给到行解码器12、读出放大器部14及未图示的源极线驱动器等。通过核心驱动器16供给的电压经由行解码器12、读出放大器部14及源极线驱动器施加到存储单元(具体来说，为字线、选择栅极线、位线及源极线)。

[0030] 电压产生电路17产生各动作所需的内部电压(例如将电源电压升压后所得的电压)，将这些内部电压供给到核心驱动器16。

[0031] 控制器20控制NAND型闪速存储器10的整体动作。控制器20从外部的主机装置(未图示)接收各种外部控制信号，例如芯片使能信号CEn、地址锁存使能信号ALE、指令锁存使能信号CLE、写入使能信号WEn及读取使能信号REn。信号名所附的“n”表示低态有效(active low)。

[0032] 控制器20基于这些外部控制信号，识别从输入输出端子I/O供给的地址Add及指令CMD。然后，控制器20将地址Add经由地址寄存器19传送到列解码器13及行解码器12。另外，

Micron Ex. 1002, p. 202
Micron v. YMTC
IPR2024-00793

控制器20对指令CMD进行解码。控制器20根据外部控制信号及指令CMD，进行数据的读取、写入、及删除的各序列控制。另外，控制器20为了将NAND型闪速存储器10的动作状态通知到主机装置，而输出待命/忙碌信号R/Bn。主机装置通过接收待命/忙碌信号R/Bn，能够获知NAND型闪速存储器10的状态。

[0033] 输入输出电路18在与主机装置之间，经由NAND总线进行数据(包含指令CMD、地址Add及数据)的收发。

[0034] 例如在电源接通时，状态寄存器21暂时保存从存储单元阵列11的ROM用户空间文件系统(Filesystem in Userspace，FUSE)读取的管理数据。另外，状态寄存器21暂时保存存储单元阵列11的动作所需的各种数据。状态寄存器21例如包含SRAM(Static Random Access Memory，静态随机存取存储器)。

[0035] [1-1]存储单元阵列11的构成

[0036] 图2是存储单元阵列11的框图。存储单元阵列11具备多个区块BLK(BLK0、BLK1、BLK2、……)。多个区块BLK分别具备多个串单元SU(SU0、SU1、SU2、……)。多个串单元SU分别具备多个NAND串22。存储单元阵列11内的区块数、1个区块BLK内的串单元数及1个串单元SU内的NAND串数可分别任意地设定。

[0037] 图3是存储单元阵列11所含的1个区块BLK的电路图。多个NAND串22分别具备多个存储单元晶体管MT及2个选择晶体管ST1、ST2。在本说明书中，有时也将存储单元晶体管称为存储单元或单元。图3表示NAND串22具备8个存储单元晶体管MT(MT0～MT7)的构成例，但NAND串22所具备的存储单元晶体管MT的数量可任意地设定。存储单元晶体管MT具备包含控制栅极及电荷储存层的积层栅极，将数据非易失地存储。存储单元晶体管MT能够以存储1比特数据(二进制)的方式构成，也能够以存储2比特以上的数据(或三进制以上)的方式构成。

[0038] 多个存储单元晶体管MT以它们的电流路径串联连接的方式配置在选择晶体管ST1、ST2之间。该串联连接的一端侧的存储单元晶体管MT的电流路径连接在选择晶体管ST1的电流路径的一端，另一端侧的存储单元晶体管MT的电流路径连接在选择晶体管ST2的电流路径的一端。

[0039] 串单元SU0所含的多个选择晶体管ST1的栅极共通连接在选择栅极线SGD0，同样地，在串单元SU1～SU3分别连接选择栅极线SGD1～SGD3。串单元SU0所含的多个选择晶体管ST2的栅极共通连接在选择栅极线SGS0，同样地，在串单元SU1～SU3分别连接选择栅极线SGS1～SGS3。此外，处于同一区块BLK内的多个选择晶体管ST2的栅极也可以共通连接在同一选择栅极线SGS。处于同一区块BLK内的存储单元晶体管MT0～MT7的控制栅极分别连接在字线WL0～WL7。

[0040] 在存储单元阵列11内呈矩阵状配置的NAND串22中处于同一列的多个NAND串22的选择晶体管ST1的电流路径的另一端共通连接在位线BL0～BL(m－1)中的任一条。“m”为1以上的整数。也就是说，1条位线BL在多个区块BLK间将处于同一列的NAND串22共通连接。同一区块BLK所含的多个选择晶体管ST2的电流路径的另一端共通连接在源极线SL。源极线SL例如在多个区块间将多个NAND串22共通连接。

[0041] 处于同一区块BLK内的多个存储单元晶体管MT的数据例如被统括地删除。数据的读取及写入是针对共通连接在配设于1个区块BLK的1条字线WL的多个存储单元晶体管MT而统括地进行。将该数据单位称为页。

Micron Ex. 1002, p. 203
Micron v. YMTC
IPR2024-00793

[0042] 图4是区块BLK的一部分区域的剖视图。在p型阱区域30上形成着多个NAND串22。也就是说，在阱区域30上，依次积层着作为选择栅极线SGS而发挥功能的例如4层配线层31、作为字线WL0～WL7而发挥功能的8层配线层32、及作为选择栅极线SGD而发挥功能的例如4层配线层33。在所积层的配线层间形成着未图示的绝缘膜。

[0043] 然后，形成贯通这些配线层31、32、33而到达阱区域30的存储孔34，在存储孔34内形成着柱状的半导体层35。在半导体层35的侧面，依次形成着栅极绝缘膜36、电荷储存层(绝缘膜)37及区块绝缘膜38。由此形成存储单元晶体管MT及选择晶体管ST1、ST2。半导体层35作为NAND串22的电流路径而发挥功能，成为供形成各晶体管的信道的区域。半导体层35的上端连接在作为位线BL而发挥功能的金属配线层39。

[0044] 在阱区域30的表面区域内形成着n^+型杂质扩散层40。在扩散层40上形成着接触插塞41，接触插塞41连接在作为源极线SL而发挥功能的金属配线层42。进而，在阱区域30的表面区域内形成着p^+型杂质扩散层43。在扩散层43上形成接触插塞44，接触插塞44连接在作为阱配线CPWELL而发挥功能的金属配线层45。阱配线CPWELL是用来经由阱区域30对半导体层35施加电位的配线。

[0045] 以上的构成在图4所记载的纸面的深度方向上排列多个，由在深度方向上排列的多个NAND串22的集合形成串单元SU。

[0046] 此外，NAND串22也可以具备虚设单元晶体管。图5是说明虚设单元晶体管的电路图。

[0047] 在选择晶体管ST2与存储单元晶体管MT0之间，例如串联连接着2个虚设单元晶体管DT0、DT1。在存储单元晶体管MT7与选择晶体管ST1之间，例如串联连接着2个虚设单元晶体管DT2、DT3。在虚设单元晶体管DT0～DT3的栅极分别连接着虚设字线DWL0～DWL3。虚设单元晶体管的构造与存储单元晶体管相同。虚设单元晶体管并非用来存储数据，而具有如下功能，即，在写入脉冲施加动作或删除脉冲施加动作中，缓和存储单元晶体管或选择晶体管所受到的干扰。

[0048] 关于存储单元阵列的构成，例如在2009年3月19日提出申请的名为“三维积层非易失性半导体存储器”的美国专利申请12/407,403号中有所记载。另外，2009年3月18日提出申请的名为“三维积层非易失性半导体存储器”的美国专利申请12/406,524号、2010年3月25日提出申请的名为“非易失性半导体存储装置及其制造方法”的美国专利申请12/679,991号、2009年3月23日提出申请的名为“半导体存储器及其制造方法”的美国专利申请12/532,030号中有所记载。这些专利申请整体通过参照而被引用在本申请的说明书中。

[0049] 另外，数据的删除能够以区块BLK单位或小于区块BLK的单位进行。关于删除方法，例如在2011年9月18日提出申请的名为“NONVOLATILE SEMICONDUCTOR MEMORY DEVICE”的美国专利申请13/235,389号中有所记载。另外，在2010年1月27日提出申请的名为“NONVOLATILE SEMICONDUCTOR STORAGE DEVICE”的美国专利申请12/694,690号中有所记载。进而，在2012年5月30日提出申请的名为“NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND DATAERASE METHOD THEREOF”的美国专利申请13/483,610号中有所记载。这些专利申请的整体通过参照而被引用在本申请的说明书中。

[0050] [1-2]读出放大器部14及数据高速缓冲存储器15的构成

[0051] 接下来，对读出放大器部14及数据高速缓冲存储器15的构成进行说明。图6是读出

Micron Ex. 1002, p. 204
Micron v. YMTC
IPR2024-00793

放大器部14及数据高速缓冲存储器15的框图。

[0052] 数据高速缓冲存储器15例如具备3个高速缓冲存储器ADL、BDL、XDL。数据高速缓冲存储器15所含的高速缓冲存储器的数量根据1个存储单元所存储的比特数而适当设定。

[0053] 高速缓冲存储器ADL、BDL、XDL能够暂时存储数据。高速缓冲存储器XDL配置在最靠近IO焊盘(IO pad)的位置，并且经由双向总线YIO而连接在输入输出电路18。高速缓冲存储器XDL经由内部总线LBUS连接在读出放大器部14及高速缓冲存储器ADL、BDL。存储在高速缓冲存储器XDL的写入数据等能够经由内部总线LBUS而复制及传送到高速缓冲存储器ADL、BDL。高速缓冲存储器ADL、BDL的物理位置并无限制，可适当配置。

[0054] 读出放大器部(S/A)14具备在读取时用来保存其结果的高速缓冲存储器(读出放大器高速缓冲存储器)SDL。存储在高速缓冲存储器SDL的读取数据等可经由内部总线LBUS而复制及传送到高速缓冲存储器ADL、BDL。

[0055] 读出放大器部14经由位线BL连接在存储单元，具有相当于能够统括地读取的单位(例如32千字节)的容量。具体来说，在统括地读取32千字节的情况下，位线BL被准备32768字节、也就是262144比特的量，高速缓冲存储器SDL、ADL、BDL、XDL的每一个也被配置相同数量。

[0056] [1-3]读出放大器部14的具体构成

[0057] 接下来，对读出放大器部14的构成进行说明。图7是读出放大器部14的电路图。

[0058] 读出放大器部14具备多个N信道MOS晶体管(以下称为NMOS)51～57、多个P信道MOS晶体管(以下称为PMOS)58、59、传送闸极60、61、高速缓冲存储器(数据锁存电路)SDL及电容器63。高速缓冲存储器SDL例如由时控反相器电路62a、62b构成。

[0059] NMOS51的电流路径的一端连接在被供给电源电压Vdd的节点。NMOS51的电流路径的另一端经由传送闸极60、NMOS54、传送闸极61而接地(连接在被供给接地电压Vss的节点)。在NMOS54与传送闸极61的连接节点连接NMOS55的电流路径的一端。该NMOS55的另一端连接在配置于存储单元阵列11的位线BL。在NMOS51并联连接NMOS52、53的串联电路。

[0060] PMOS58的电流路径的一端连接在被供给电源电压Vdd的节点。PMOS58的电流路径的另一端经由PMOS59连接在构成高速缓冲存储器SDL的反相器电路62a的输入端子，并且经由NMOS56而接地。与该反相器电路62a交叉耦合的时控反相器电路62b的输入端子经由NMOS57连接在内部总线LBUS。PMOS59的栅极经由读出节点SEN而连接在NMOS52与NMOS53的连接节点及电容器63的一端。对电容器63的另一端供给时钟信号CLK。

[0061] 如下所述，控制器20对读出放大器部14内供给各种控制信号(例如信号BLX、BLC、BLS、HLL、XXL、STB、RST、NCO)。

[0062] 对NMOS51的栅极供给信号BLX。对构成传送闸极60的NMOS的栅极，供给构成高速缓冲存储器SDL的反相器电路62a的输出端子的信号LAT。对构成传送闸极60的PMOS的栅极，供给反相器电路62a的输入端子的信号INV。对NMOS54的栅极供给信号BLC。对NMOS55的栅极供给信号BLS。

[0063] 对构成传送闸极61的NMOS的栅极供给信号INV。对构成传送闸极61的PMOS的栅极供给信号LAT。

[0064] 对NMOS52的栅极供给信号HLL。对NMOS53的栅极供给信号XXL。对PMOS58的栅极供给信号STB。对NMOS56的栅极供给重置信号RST。对NMOS57的栅极供给信号NCO。

Micron Ex. 1002, p. 205
Micron v. YMTC
IPR2024-00793

[0065] 接下来，对所述读出放大器部14中的写入动作、读取动作及写入验证动作进行概略性说明。

[0066] (写入动作)

[0067] 在对存储单元写入数据的情况下，控制器20产生如下控制信号。首先，控制器20将信号STB设为高电平(以下记作“H”电平)，将重置信号RST暂时设为“H”电平，重置高速缓冲存储器SDL。由此，高速缓冲存储器SDL的信号LAT成为“H”电平，信号INV成为低电平(以下记作“L”电平)。

[0068] 之后，控制器20将信号NCO设为“H”电平。由此，从内部总线LBUS将数据取入到高速缓冲存储器SDL。在该数据为表示写入的“L”电平(“0”)的情况下，信号LAT成为“L”电平，信号INV成为“H”电平。另外，在数据为表示非写入的“H”电平(“1”)的情况下，高速缓冲存储器SDL的数据不变，信号LAT保持“H”电平，信号INV保持“L”电平。

[0069] 接着，控制器20将信号BLX、BLC、BLS设为“H”电平。于是，在写入的情况下，也就是在高速缓冲存储器SDL的信号LAT为“L”电平，信号INV为“H”电平的情况下，传送闸极60断开，传送闸极61接通，位线BL成为接地电压Vss。在该状态下，如果字线成为编程电压Vpgm，那么对存储单元写入数据。

[0070] 另一方面，在非写入的情况下，也就是在高速缓冲存储器SDL的信号LAT为“H”电平，信号INV为“L”电平的情况下，传送闸极60接通，传送闸极61断开，所以位线BL被充电成为电源电压Vdd。此处，在字线成为编程电压Vpgm的情况下，存储单元的信道被升压为高电位，所以不对存储单元写入数据。

[0071] (读取动作及写入验证动作)

[0072] 在从存储单元读取数据的情况下，控制器20产生如下控制信号。首先，控制器20将重置信号RST暂时设为“H”电平，重置高速缓冲存储器SDL。由此，高速缓冲存储器SDL的信号LAT成为“H”电平，信号INV成为“L”电平。

[0073] 之后，控制器20将信号BLS、BLC、BLX、HLL、XXL设为特定的电压。由此，位线BL被充电，并且电容器63的节点SEN被充电成为电源电压Vdd。此处，在存储单元的阈值电压高于读取电平的情况下，存储单元为断开状态，位线BL保持为“H”电平。也就是说，节点SEN保持为“H”电平。另外，在存储单元的阈值电压低于读取电平的情况下，存储单元成为接通状态，位线BL的电荷被放电。因此，位线BL成为“L”电平。由此，节点SEN也成为“L”电平。

[0074] 接着，控制器20将信号STB设为“L”电平。于是，在存储单元接通的情况下，因为节点SEN为“L”电平，所以PMOS59接通。由此，高速缓冲存储器SDL的信号INV成为“H”电平，信号LAT成为“L”电平。另一方面，在存储单元断开的情况下，因为节点SEN为“H”电平，所以PMOS59断开。由此，高速缓冲存储器SDL的信号INV保持为“L”电平，信号LAT保持为“H”电平。

[0075] 之后，控制器20将信号NCO设为“H”电平。于是，NMOS57接通，高速缓冲存储器SDL的数据被向内部总线LBUS传送。

[0076] 另外，在写入动作后，进行验证存储单元的阈值电压的写入验证动作。该写入验证动作与所述读取动作相同。

[0077] [1-4]行解码器12的构成

[0078] 接下来，对行解码器12的构成进行说明。图8是行解码器12的电路图。行解码器12具备区块解码器70及多个传送栅极。

Micron Ex. 1002, p. 206
Micron v. YMTC
IPR2024-00793

[0079] 区块解码器70具备NAND栅极70A及反相器电路70B。对NAND栅极70A的第1输入端子(高态有效(active high))输入信号RDECAD,对NAND栅极70A的第2输入端子(低态有效)输入信号BADBLK。

[0080] 信号RDECAD是在对应的区块为选择区块的情况下成为"H"电平,在对应的区块为非选择区块的情况下成为"L"电平的信号。信号BADBKL是在对应的区块为不良区块(坏块)的情况下成为"H"电平的信号。

[0081] NAND栅极70A输出信号BLKSEL。NAND栅极70A的输出端子连接在反相器电路70B的输入端子。反相器电路70B输出信号BLKSELn。

[0082] 行解码器12具备传送栅极71(71-0～71-3)、72(72-0～72-3)、73、74(74-0～74-3)、75、76。这些传送栅极由高耐压用N信道MOS晶体管构成。

[0083] MOS晶体管71、72用来对选择栅极线SGD传送电压。MOS晶体管71-0～71-3的电流路径的一端分别连接在选择栅极线SGD0～SGD3,另一端分别连接在信号线SGDI0～SGDI3,对栅极共通地供给信号BLKSEL。

[0084] MOS晶体管72-0～72-3的电流路径的一端分别连接在选择栅极线SGD0～SGD3,另一端共通连接在信号线USGDI,对栅极共通地供给信号BLKSELn。

[0085] MOS晶体管73用来对字线WL传送电压。MOS晶体管72的电流路径的一端连接在对应的字线WL,另一端连接在对应的信号线CG,对栅极供给信号BLKSEL。此外,图8中只图示了1个MOS晶体管73,但要准备相当于字线WL的条数的量的MOS晶体管73。

[0086] MOS晶体管74用来对选择栅极线SGS传送电压。MOS晶体管74-0～74-3的电流路径的一端分别连接在选择栅极线SGS0～SGS3,另一端分别连接在信号线SGSI0～SGSI3,对栅极共通地供给信号BLKSEL。

[0087] MOS晶体管75、76用来对选择栅极线SGSB传送电压。虽然图3中省略图示,但选择栅极线SGSB(及与其连接的选择晶体管)配置在NAND串22的最下层,具有降低NAND串22的源极侧的电阻的功能,用来对非选择区块传送特定的电压。

[0088] MOS晶体管75的电流路径的一端连接在选择栅极线SGSB,另一端连接在信号线SGSBI,对栅极供给信号BLKSEL。MOS晶体管76的电流路径的一端连接在选择栅极线SGSB,另一端连接在信号线USGSI,对栅极供给信号BLKSELn。

[0089] 选择栅极线SGSB连接在源极侧的多个选择晶体管中的最下层的选择晶体管。选择栅极线SGSB(及与其连接的选择晶体管)具有降低NAND串22(具体来说,为柱状的半导体层35)的电阻的功能。在选择区块中,连接在选择栅极线SGSB的选择晶体管被接通。写入动作、读取动作及删除动作中的NAND串22的电压设定是使用选择栅极线SGS而进行。

[0090] 信号线SGDI0～SGDI3、USGDI、CG、SGSI0～SGSI3、SGSBI、USGSI连接在核心驱动器16。

[0091] [2]NAND型闪速存储器10的动作

[0092] 首先,对区块选择动作进行说明。图9是说明区块选择动作的示意图。

[0093] 在选择区块中,MOS晶体管71、73、74、75成为接通状态,MOS晶体管72、76成为断开状态。因此,在选择区块中,选择栅极线SGD连接在信号线SGDI,选择栅极线SGS连接在信号线SGSI,选择栅极线SGSB连接在信号线SGSBI,字线WL连接在信号线CG。

[0094] 进而,在三维积层NAND型闪速存储器10中能够选择选择区块内的1个串单元。如图

Micron Ex. 1002, p. 207
Micron v. YMTC
IPR2024-00793

9所示，作为一例，在只选择选择区块内的串单元SU0的情况下，核心驱动器16对选择栅极线SGD0施加使选择晶体管ST1为接通状态的电压SGD_SEL，对选择栅极线SGS0、SGSB施加使选择晶体管ST2为接通状态的电压SGS_SEL。另外，核心驱动器16对选择栅极线SGD1～SGD3施加使选择晶体管ST1为断开状态的电压SGD_USEL，对选择栅极线SGS1～SGS3施加使选择晶体管ST2为断开状态的电压SGS_USEL。对字线WL施加下述电压VREAD或电压VCGRV。

[0095] 另一方面，在非选择区块中，MOS晶体管71、73、74、75成为断开状态，MOS晶体管72、76成为接通状态。因此，在非选择区块中，选择栅极线SGD连接在信号线USGDI，选择栅极线SGSB连接在信号线USGSI。字线WL及选择栅极线SGS成为浮动状态。核心驱动器16对选择栅极线SGD0～SGD3施加使选择晶体管ST1为断开状态的电压USGD，对选择栅极线SGSB施加使选择晶体管ST2为断开状态的电压USGS。

[0096] 此外，像所述那样，连接在处于同一区块BLK内的多个选择晶体管ST2的选择栅极线SGS也可以为共通。该情况下，选择栅极线SGS＜3:0＞作为共通的选择栅极线SGS被配线。

[0097] 这样一来，在三维积层NAND型闪速存储器中，在选择区块内存在选择NAND串及非选择NAND串。因此，会发生二维(平面)NAND型闪速存储器中不存在的固有的读取干扰。在本实施方式中，主旨在于抑制在非选择NAND串中，SGD旁边的存储单元(或虚设单元)的热载流子注入引起的读取干扰。

[0098] 以下，分为ABL(all-bit-line，全位线)方式与位线屏蔽方式，对读取动作进行说明。ABL方式是从全部位线同时读取数据的方式。位线屏蔽方式是从偶数位线及奇数位线个别地读取数据的方式。非读取对象的位线设定为接地电压Vss，作为屏蔽线而发挥功能。

[0099] [2-1]ABL方式的动作

[0100] 图10是说明ABL方式中的NAND型闪速存储器10的读取动作的时序图。此外，在图10中，时刻t1～t2的期间是用来降低升压后的信道电压的读取准备期间，时刻t2～t3的期间是预充电期间，时刻t3～t4的期间是用来判定存储单元的数据的读取期间。

[0101] 在时刻t1，控制器20对位线BL施加接地电压Vss(＝0V)或电压VSRC，对源极线施加电压VSRC。电压VSRC满足“Vss＜VSRC＜Vdd”。控制器20对选择字线WL施加读取电压VCGRV，对非选择字线WL施加读取通过电压VREAD。读取电压VCGRV是用来判定读取对象的存储单元的阈值、也就是存储单元的数据的电压。读取通过电压VREAD是与存储单元的保存数据无关地将存储单元设为接通状态的电压。此外，在图10中，通过与非选择字线WL的耦合，使选择字线WL的电压暂时大于读取电压VCGRV。

[0102] 另外，控制器20对选择SGD(所选择的选择栅极线SGD)、非选择SGD(非选择的选择栅极线SGD)、选择SGS(所选择的选择栅极线SGS)、非选择SGS(非选择的选择栅极线SGS)施加电压VSG。电压VSG是使选择晶体管ST1、ST2为接通状态的电压，例如6V左右。也就是说，在本实施方式中，在非选择NAND串中，选择晶体管ST1被暂时接通。

[0103] 在选择区块的非选择NAND串中，如果在连接在选择字线WL的存储单元处于切断状态时，选择晶体管ST1保持断开的状态，那么在非选择字线WL上升到读取通过电压VREAD时，漏极侧信道被升压，选择字线WL旁边的存储单元会因热载流子注入引起的读取干扰而阈值上升。因此，为了降低升压后的信道的电压，通过在使非选择字线WL上升到读取通过电压VREAD时，使非选择NAND串的选择晶体管ST1暂时接通，而能够抑制选择字线WL旁边的存储单元中的热载流子注入引起的读取干扰。

Micron Ex. 1002, p. 208
Micron v. YMTC
IPR2024-00793

[0104] 在非选择区块中，对选择栅极线SGD、SGS施加接地电压Vss或电压VSRC。

[0105] 接着，在时刻t2，控制器20对位线BL施加预充电电压Vpre。预充电电压Vpre是用来在从存储单元读取数据之前对位线BL预充电的电压，例如为“VSRC+0.5V”左右。

[0106] 接着，控制器20对非选择SGD施加电压VSRC。由此，在非选择NAND串中，选择晶体管ST1断开。该情况下，非选择SGD设定为与源极线SL相同的电压VSRC，所以能够将选择晶体管ST1断开，并且减小与相邻字线的电压差。

[0107] 此外，在时刻t2施加到非选择SGD的电压并不限定于与源极线相同的电压VSRC，只要为使选择晶体管ST1断开的电压即可。也就是说，在时刻t2施加到非选择SGD的电压只要高于接地电压Vss，并且为“对源极线的电压VSRC加上选择晶体管ST1的阈值所得的电压”以下即可。

[0108] 接着，在时刻t3，读出放大器部14通过判定位线的电流，而读取存储单元的数据。之后，在时刻t4，将各种配线的电压重置。

[0109] 此外，也可以在时刻t1～t2的期间，使全部位线BL为浮动状态。该情况下，也能够实现所述相同的动作，并且与所述将位线BL设为电压VSRC的情况相比，能够降低消耗电力。

[0110] (比较例)

[0111] 图11是说明比较例的读取动作的时序图。在比较例中，在时刻t2，控制器20对非选择SGD施加接地电压Vss。由此，在非选择NAND串中，选择晶体管ST1断开。在比较例中，非选择SGD与和其相邻的字线的电压差变大。

[0112] 图12是用来说明读取干扰的示意性能带图。图12(a)表示比较例，图12(b)表示本实施方式。

[0113] 例如，存储单元的阈值Vt＝2V，选择晶体管ST1的阈值Vt＝3.5V，VREAD＝8V，VSRC＝1V，Vpre＝1.5V(或1V)。例如，因施加到非选择字线WL6、WL7的读取通过电压VREAD，而导致信道被升压到4V左右。

[0114] 在比较例中，对选择栅极线SGD施加0V，选择晶体管ST1的信道为-3.5V左右。相对于此，在本实施方式中，对选择栅极线SGD施加电压VSRC(＝1V)，选择晶体管ST1的信道为-2.5V左右。由此，在本实施方式中，在选择栅极线SGD与和其相邻的字线WL7之间，信道的电压差降低，读取干扰被缓和。

[0115] [2-2]位线屏蔽方式的动作

[0116] 图13是说明位线屏蔽方式中的NAND型闪速存储器10的读取动作的时序图。在位线屏蔽方式中，在从偶数位线读取数据的情况下，对奇数位线施加接地电压Vss，另一方面，在从奇数位线读取数据的情况下，对偶数位线施加接地电压Vss。以下，只对与ABL方式不同的动作进行说明。

[0117] 在时刻t2，控制器20对选择SGS及非选择SGS施加电压VSRC。于是，在选择NAND串及非选择NAND串中，选择晶体管ST2断开。由此，NAND串中不会流动电流，所以能够通过电压Vpre确实地对位线BL充电。

[0118] 此外，在时刻t2施加到SGS的电压并不限定于与源极线相同的电压VSRC，只要为将选择晶体管ST2切断的电压即可。也就是说，在时刻t2施加到SGS的电压只要高于接地电压Vss，并且为“对源极线的电压VSRC加上选择晶体管ST2的阈值所得的电压”以下即可。

[0119] 在时刻t3，控制器20对SGS施加电压VSG。之后，读出放大器部14通过判定位线的电

Micron Ex. 1002, p. 209
Micron v. YMTC
IPR2024-00793

压，而读取存储单元的数据。

[0120] (比较例)

[0121] 图14是说明比较例的读取动作的时序图。在比较例中，在时刻t2，控制器20对非选择SGD、选择SGS及非选择SGS施加接地电压Vss。由此，在非选择NAND串中，选择晶体管ST1断开。另外，在选择NAND串及非选择NAND串中，选择晶体管ST2断开。

[0122] 与ABL方式的情况同样地，在比较例中，非选择SGD与和其相邻的字线的电压差变大。另一方面，在本实施方式中，在选择栅极线SGD与和其相邻的字线WL之间，信道的电压差降低，读取干扰被缓和。

[0123] [3]实施方式的效果

[0124] 例如，在选择栅极线SGD旁边配置着虚设单元(存储单元也相同)。选择栅极线SGD旁边的虚设单元受到读取干扰的次数与通常的存储单元相比，多相当于字线WL数量的量，所以即便通常的存储单元的干扰处于允许范围内，虚设单元也会更受到干扰。如果虚设单元的阈值上升到影响单元电流(在读取时流过NAND串的电流)的级别，那么会对读取动作产生影响。

[0125] 在本实施方式中，在例如将源极线SL偏压到1V左右的正电压VSRC而非接地电压Vss那样的Negative Sense动作中，对非选择NAND串的选择栅极线SGD施加例如与施加到源极线SL的电压相同的电压VSRC。由此，在选择栅极线SGD与和其相邻的虚设字线WL之间，信道的电压差降低。其结果，能够抑制选择栅极线SGD旁边的虚设单元(或存储单元)中的热载流子注入引起的读取干扰。

[0126] (变化例)

[0127] 在1个存储单元晶体管MT保存2比特数据的情况下，其阈值电压根据保存数据而取用4种电平中的任一种。在将4种电平由低到高依次设为删除电平、A电平、B电平及C电平的情况下，在A电平的读取动作时施加到选择字线的电压例如为0V～0.55V之间。并不限定于此，也可以为0.1V～0.24V、0.21V～0.31V、0.31V～0.4V、0.4V～0.5V、0.5V～0.55V等任一个之间。在B电平的读取时施加到选择字线的电压例如为1.5V～2.3V之间。并不限定于此，也可以为1.65V～1.8V、1.8V～1.95V、1.95V～2.1V、2.1V～2.3V等任一个之间。在C电平的读取动作时施加到选择字线的电压例如为3.0V～4.0V之间。并不限定于此，也可以为3.0V～3.2V、3.2V～3.4V、3.4V～3.5V、3.5V～3.6V、3.6V～4.0V等任一个之间。作为读取动作的时间(tR)，例如也可以为25μs～38μs、38μs～70μs、70μs～80μs等任一个之间。

[0128] 写入动作包含编程及编程验证。在写入动作中，最初施加到在编程时选择的字线的电压例如为13.7V～14.3V之间。并不限定于此，例如也可以为13.7V～14.0V、14.0V～14.6V等任一个之间。也可以使大于第奇数条字线进行写入时最初施加到所选择的字线的电压、与对第偶数条字线进行写入时最初施加到所选择的字线的电压不同。在将编程动作设为ISPP方式(Incremental Step Pulse Program，增量步进脉冲编程)时，作为上升的电压，例如可列举0.5V左右。作为施加到非选择的字线的电压，例如可以为6.0V～7.3V之间。并不限定于此，例如也可以为7.3V～8.4V之间，也可以为6.0V以下。也可以根据非选择的字线是第奇数条字线还是第偶数条字线，而使所施加的通过电压不同。作为写入动作的时间(tProg)，例如可以为1700μs～1800μs、1800μs～1900μs、1900μs～2000μs之间。

[0129] 在删除动作中，最初施加到配置在半导体衬底上部并且在上方配置着存储单元的

Micron Ex. 1002, p. 210
Micron v. YMTC
IPR2024-00793

阱的电压例如为12V～13.6V之间。并不限定于此，例如也可以为13.6V～14.8V、14.8V～19.0V、19.0V～19.8V、19.8V～21V等任一个之间。作为删除动作的时间(tErase)，例如可以为3000μs～4000μs、4000μs～5000μs、4000μs～9000μs之间。

[0130] 另外，存储单元例如也可以为如下构造。存储单元在硅衬底等半导体衬底上具有介隔膜厚为4nm～10nm的隧道绝缘膜而配置的电荷储存膜。该电荷储存膜可设定为膜厚为2nm～3nm的氮化硅(SiN)膜或氮氧化硅(SiON)膜等绝缘膜与膜厚为3nm～8nm的多晶硅(Poly-Si)膜的积层构造。也可以在多晶硅膜中添加钌(Ru)等金属。存储单元在电荷储存膜之上具有绝缘膜。该绝缘膜具有例如被膜厚为3nm～10nm的下层High-k膜与膜厚为3nm～10nm的上层High-k膜夹着的膜厚为4nm～10nm的氧化硅(SiO)膜。作为High-k膜的材料，可列举氧化铪(HfO)等。另外，氧化硅膜的膜厚可以比High-k膜的膜厚厚。在绝缘膜上，隔着膜厚为3nm～10nm的功函数调整用膜而设置膜厚为30nm～70nm的控制电极。此处，功函数调整用膜例如为氧化钽(TaO)等金属氧化膜、氮化钽(TaN)等金属氮化膜等。控制电极可使用钨(W)等。可以在存储单元间配置气隙。

[0131] 虽已对本发明的若干实施方式进行了说明，但这些实施方式是作为示例而提出的，并非意在限定发明的范围。这些新颖的实施方式能够以其他各种方式来实施，且能够在不脱离发明的主旨的范围内进行各种省略、替换、变更。这些实施方式或其变化包含在发明的范围或主旨内，并且包含在权利要求书所记载的发明及其均等的范围内。

[0132] [符号的说明]

[0133]	10	NAND型闪速存储器
[0134]	11	存储单元阵列
[0135]	12	行解码器
[0136]	13	列解码器
[0137]	14	读出放大器部
[0138]	15	数据高速缓冲存储器
[0139]	16	核心驱动器
[0140]	17	电压产生电路
[0141]	18	输入输出电路
[0142]	19	地址寄存器
[0143]	20	控制器
[0144]	21	状态寄存器
[0145]	22	NAND串
[0146]	30	阱区域
[0147]	31～33	配线层
[0148]	35	半导体层
[0149]	36	栅极绝缘膜
[0150]	37	电荷储存层
[0151]	38	区块绝缘膜
[0152]	39、42、45	金属配线层
[0153]	40、43	扩散层

Micron Ex. 1002, p. 211
Micron v. YMTC
IPR2024-00793

[0154]	41、44	接触插塞

Micron Ex. 1002, p. 212
Micron v. YMTC
IPR2024-00793

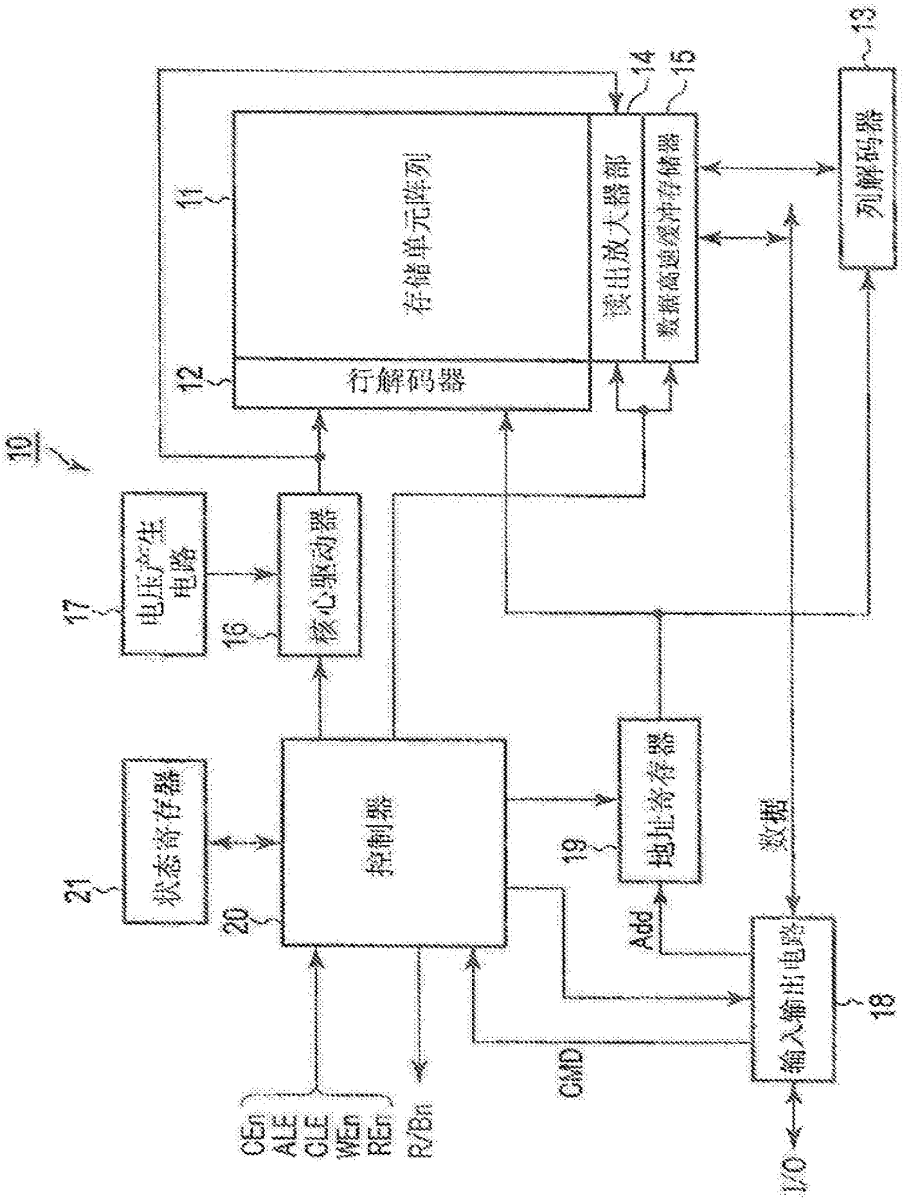


图1

Micron Ex. 1002, p. 213
Micron v. YMTC
IPR2024-00793

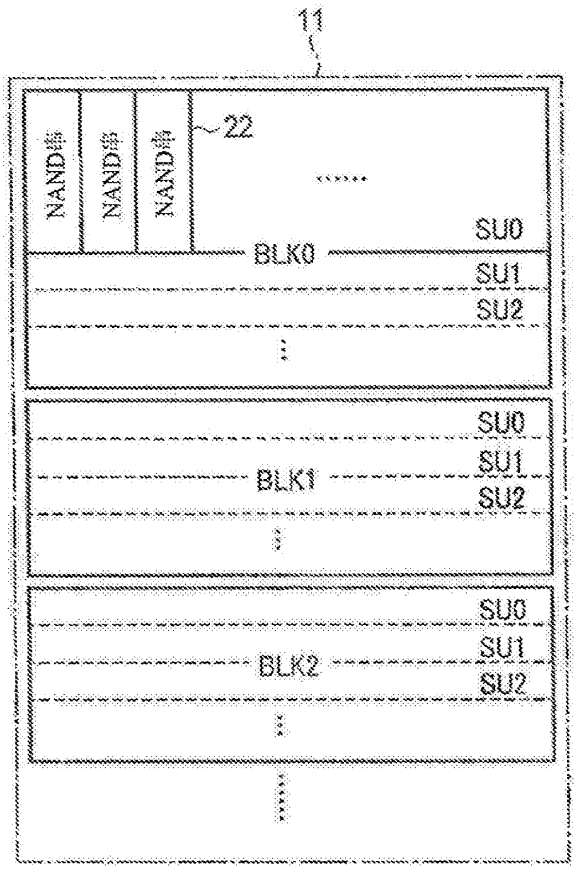


图2

Micron Ex. 1002, p. 214
Micron v. YMTC
IPR2024-00793

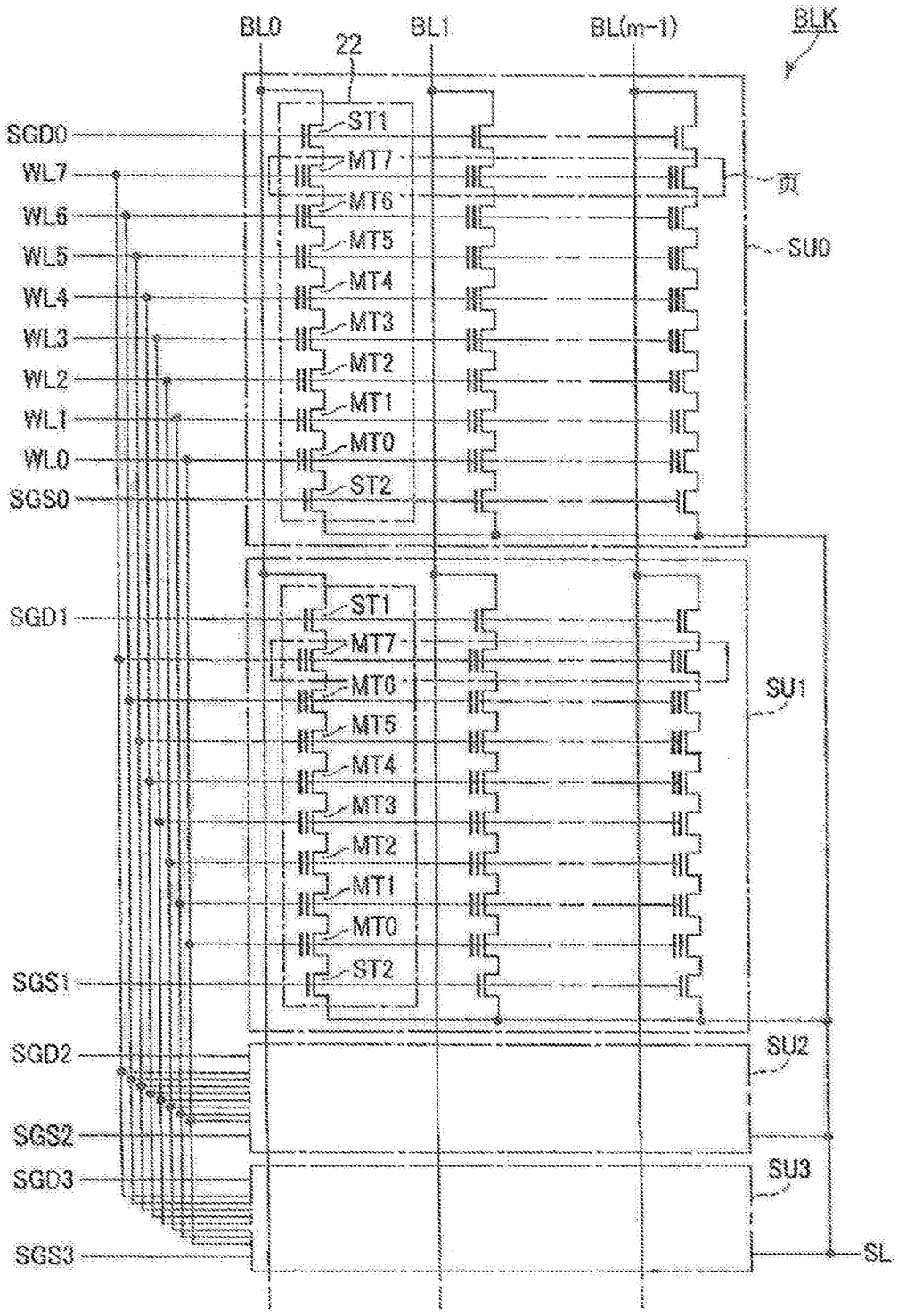


图3

Micron Ex. 1002, p. 215
Micron v. YMTC
IPR2024-00793

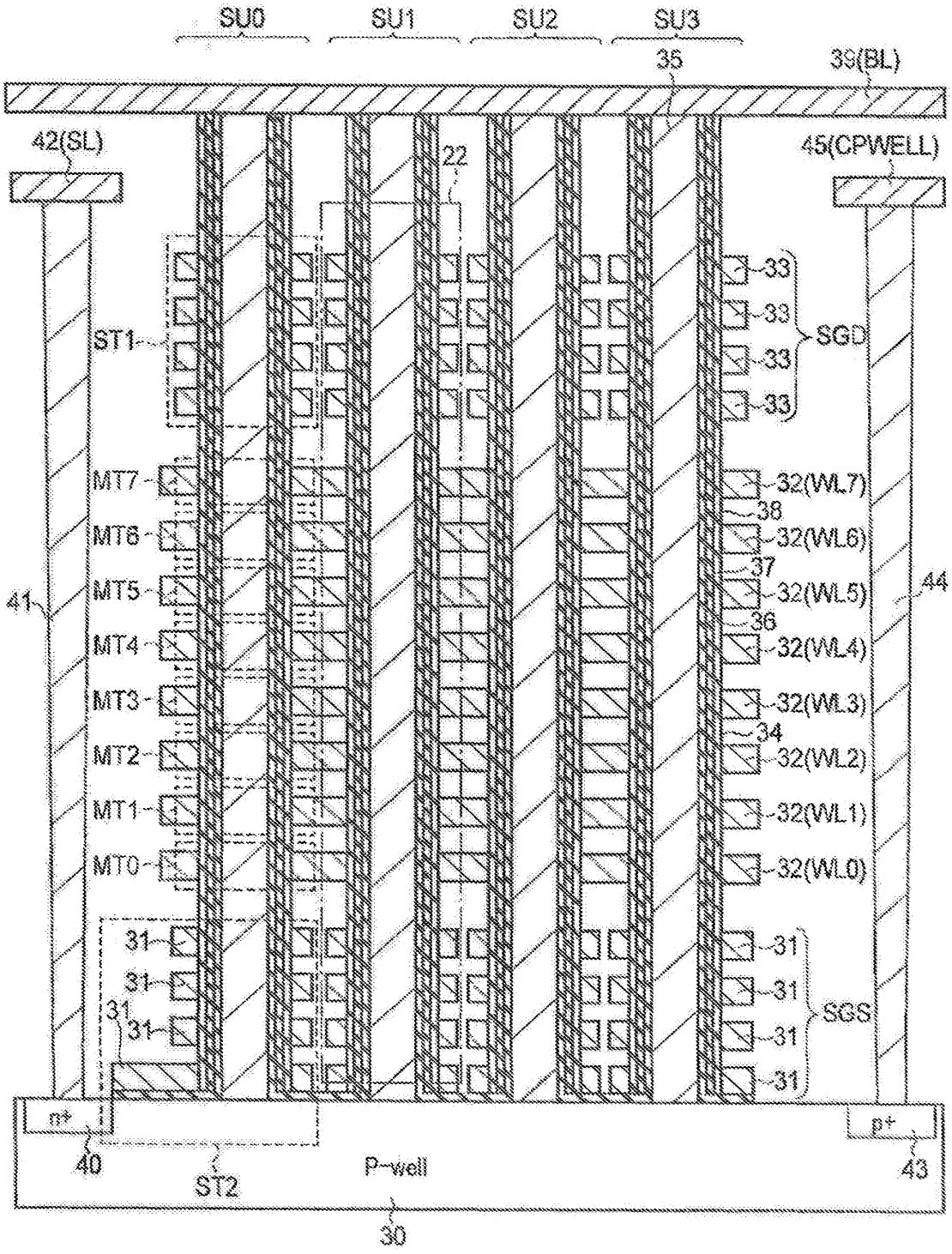


图4

Micron Ex. 1002, p. 216
Micron v. YMTC
IPR2024-00793

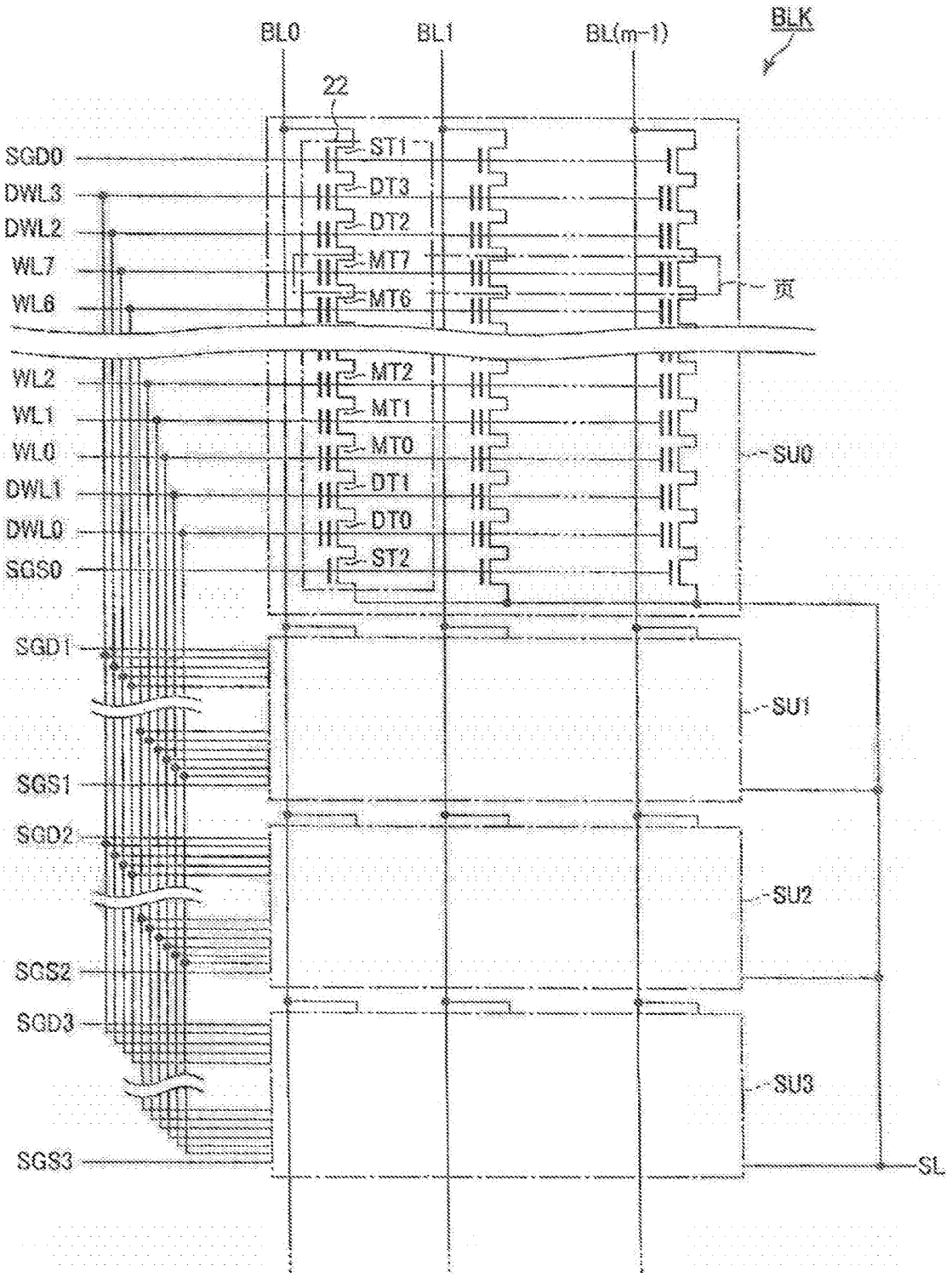


图5

Micron Ex. 1002, p. 217
Micron v. YMTC
IPR2024-00793

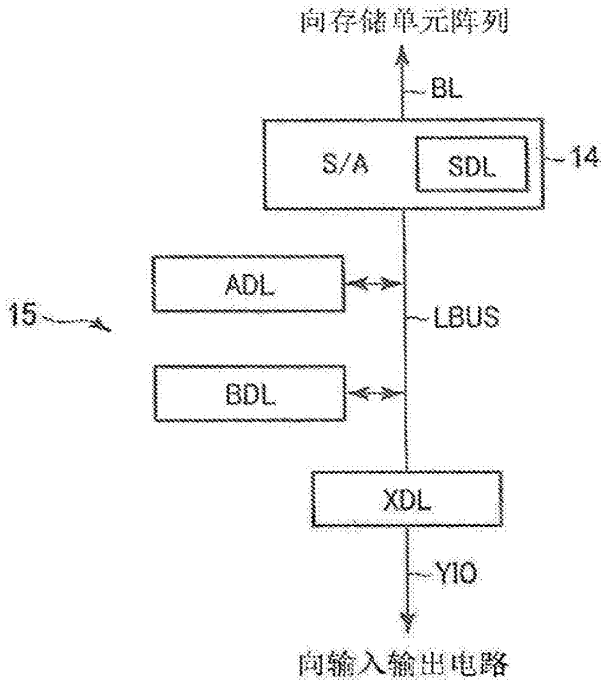


图6

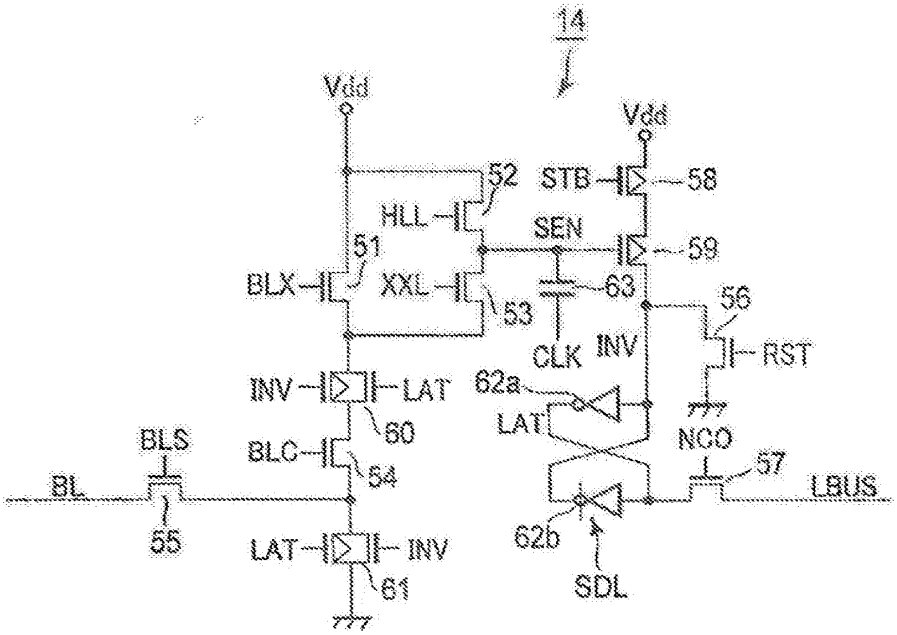


图7

Micron Ex. 1002, p. 218
Micron v. YMTC
IPR2024-00793

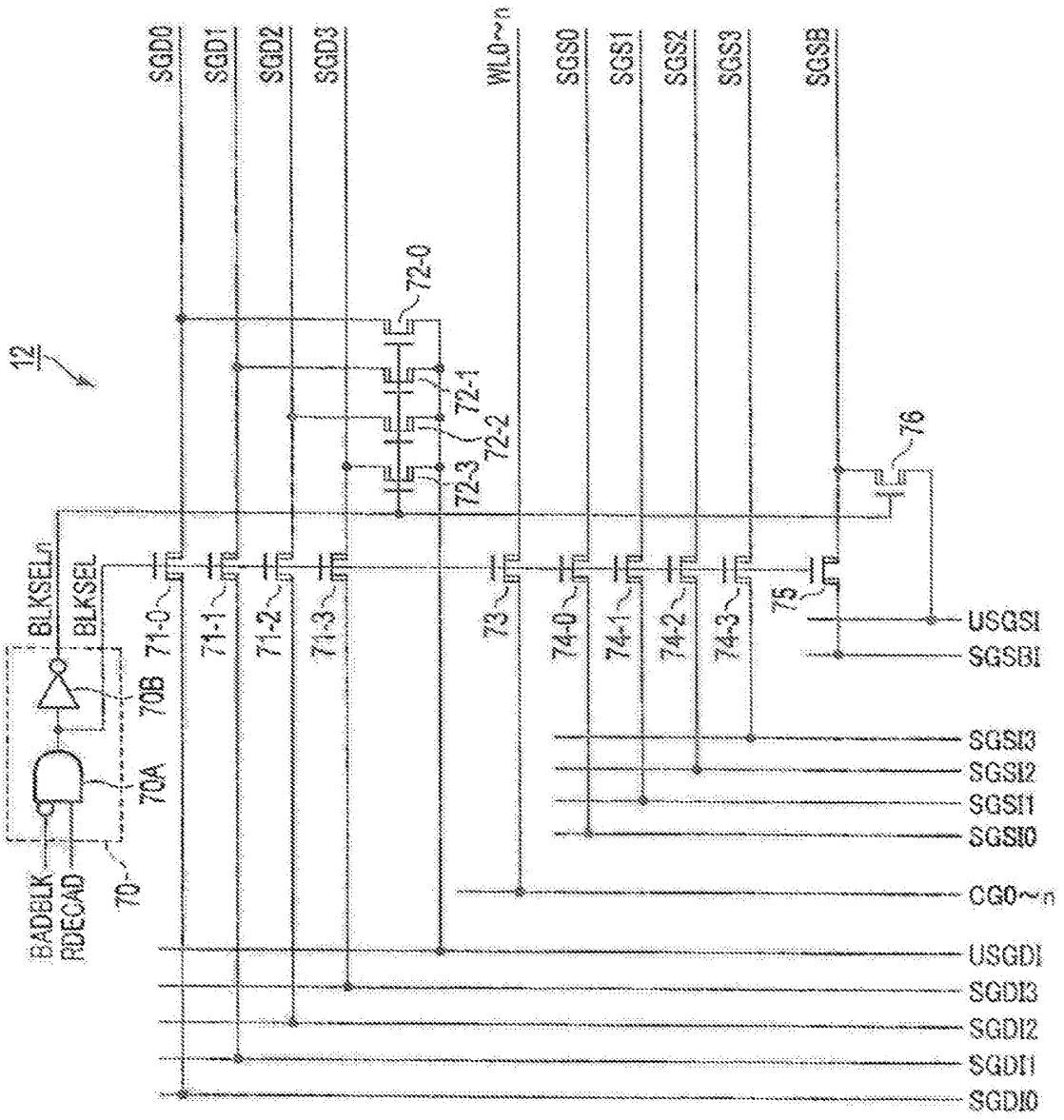


图8

Micron Ex. 1002, p. 219
Micron v. YMTC
IPR2024-00793

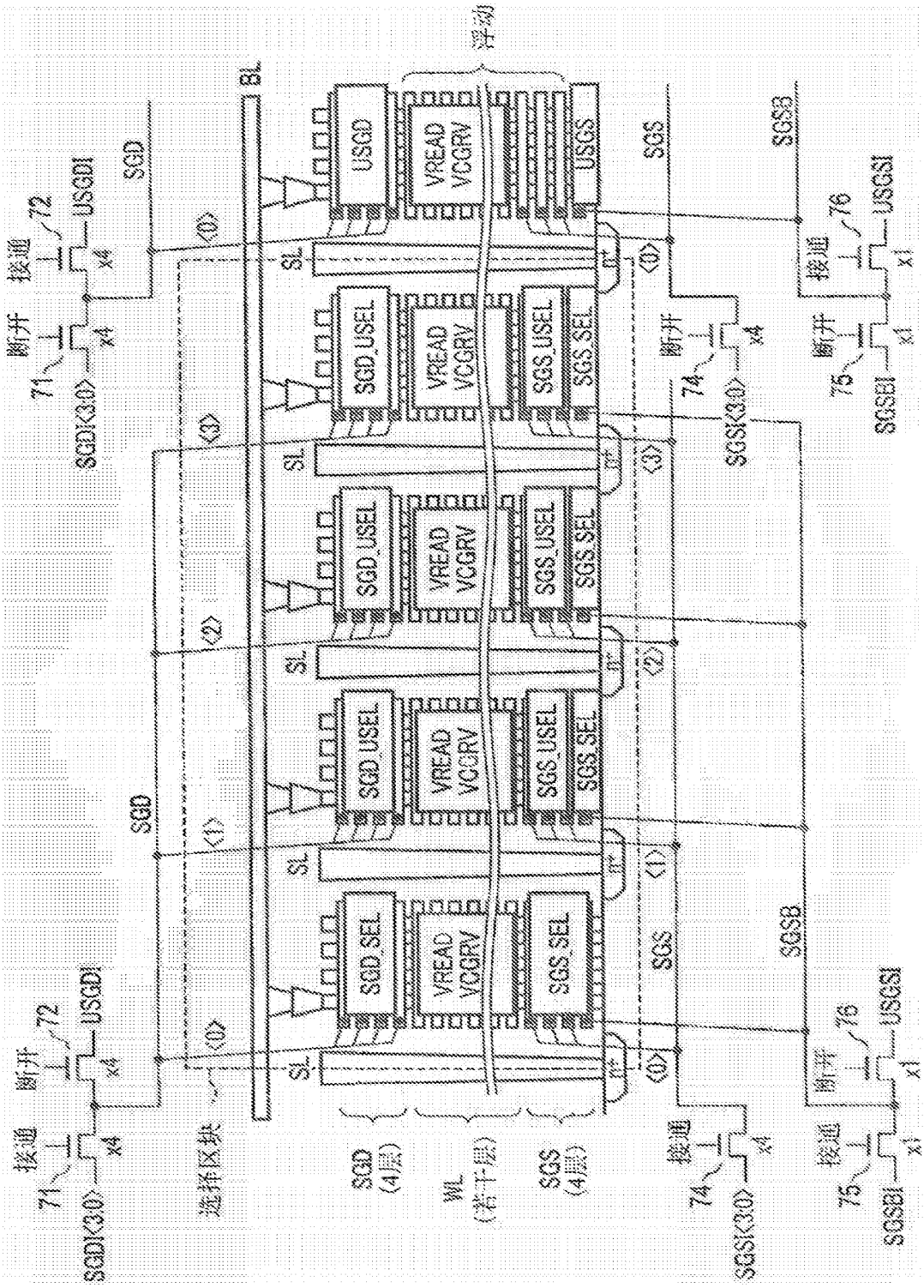


图9

Micron Ex. 1002, p. 220
Micron v. YMTC
IPR2024-00793

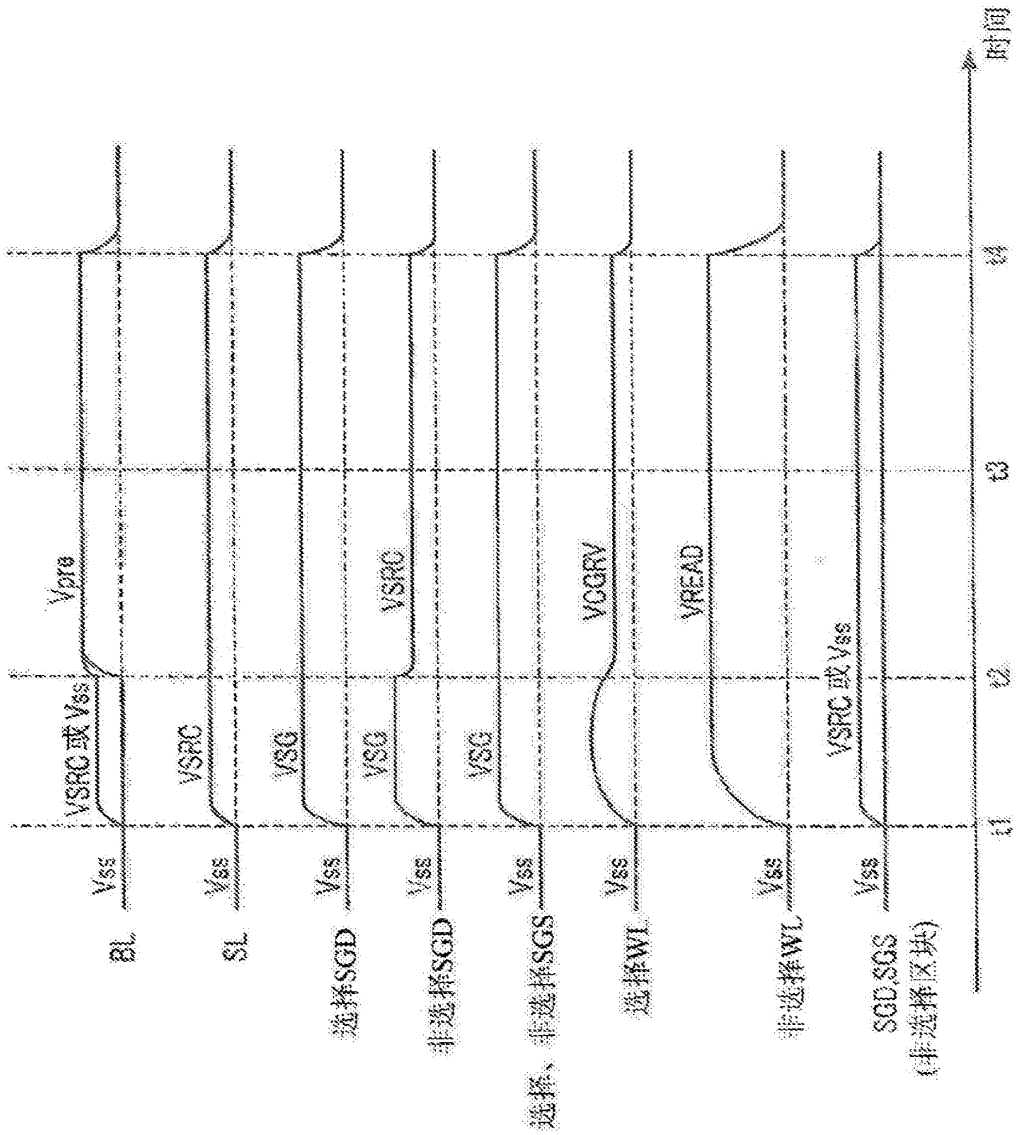


图10

Micron Ex. 1002, p. 221
Micron v. YMTC
IPR2024-00793

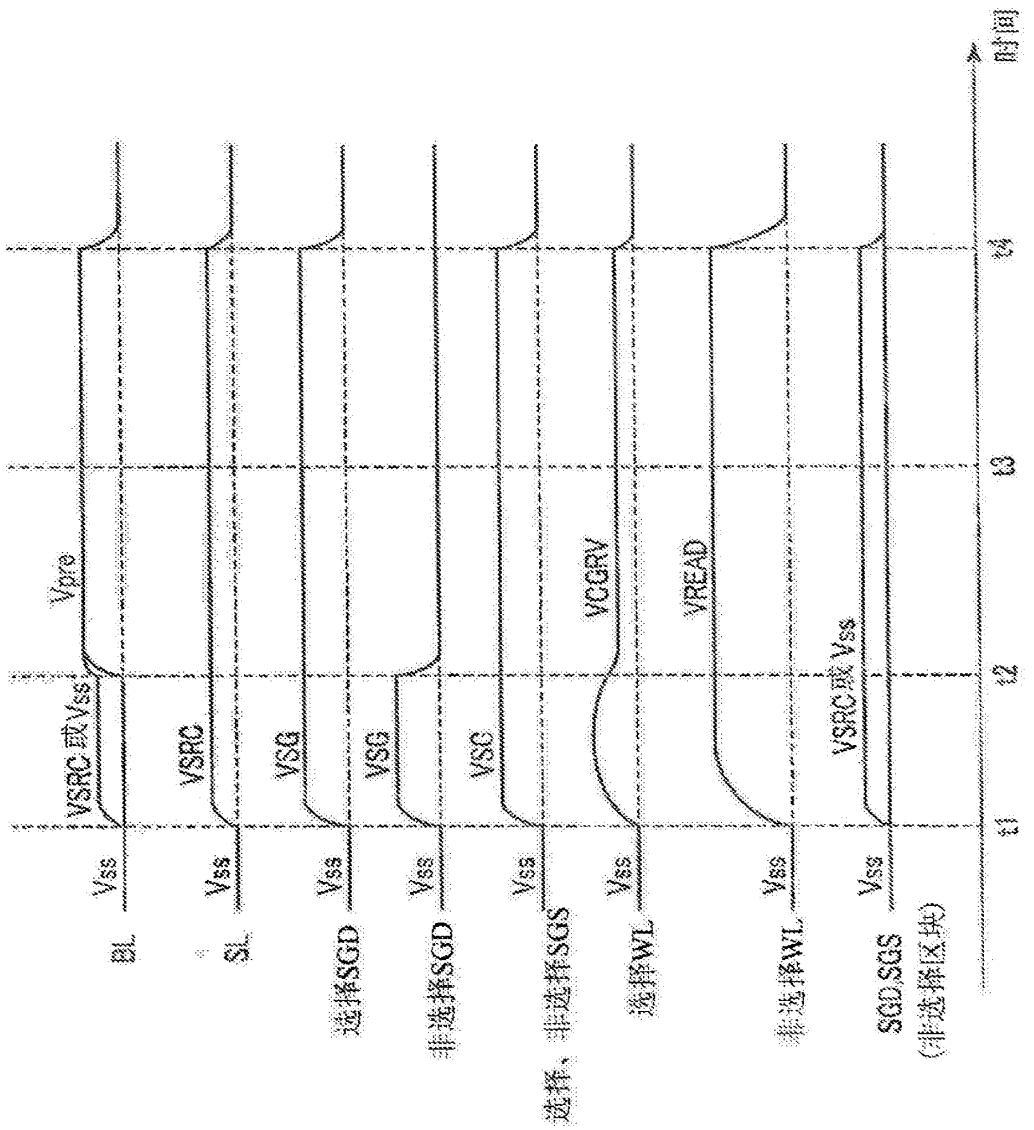


图11

Micron Ex. 1002, p. 222
Micron v. YMTC
IPR2024-00793

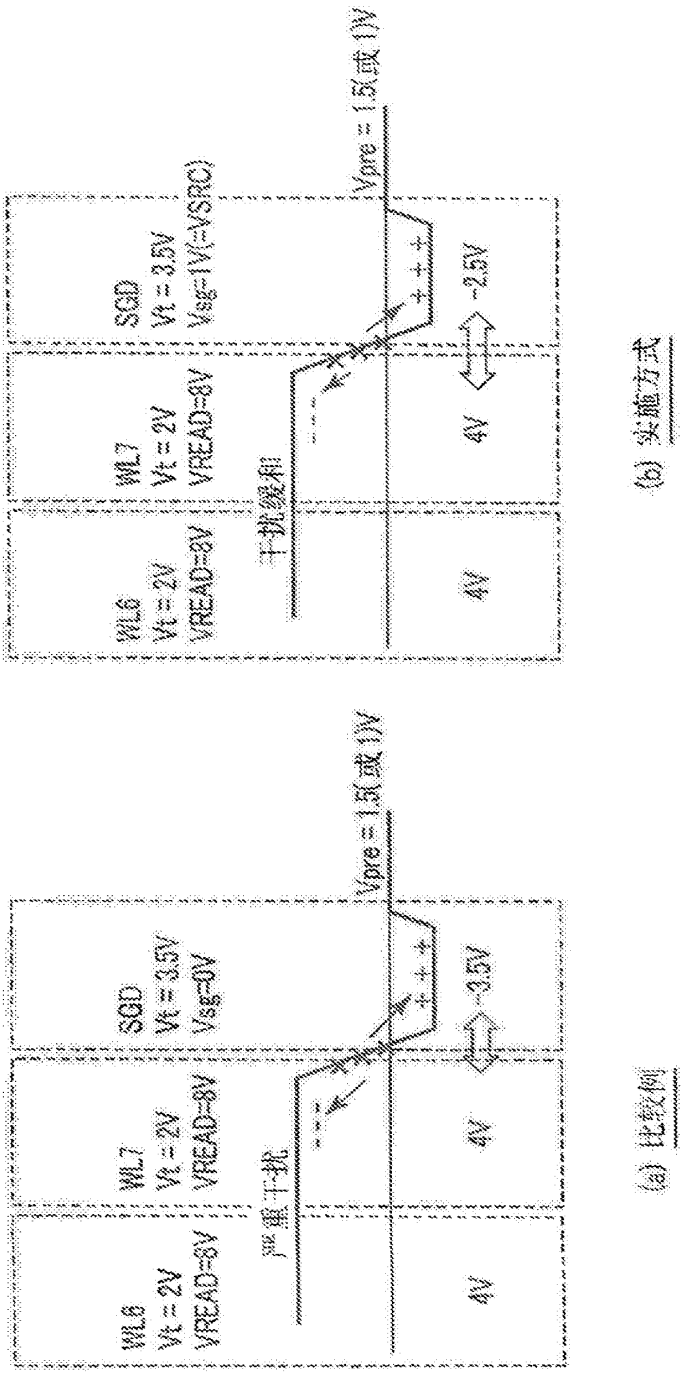


图12

Micron Ex. 1002, p. 223
Micron v. YMTC
IPR2024-00793

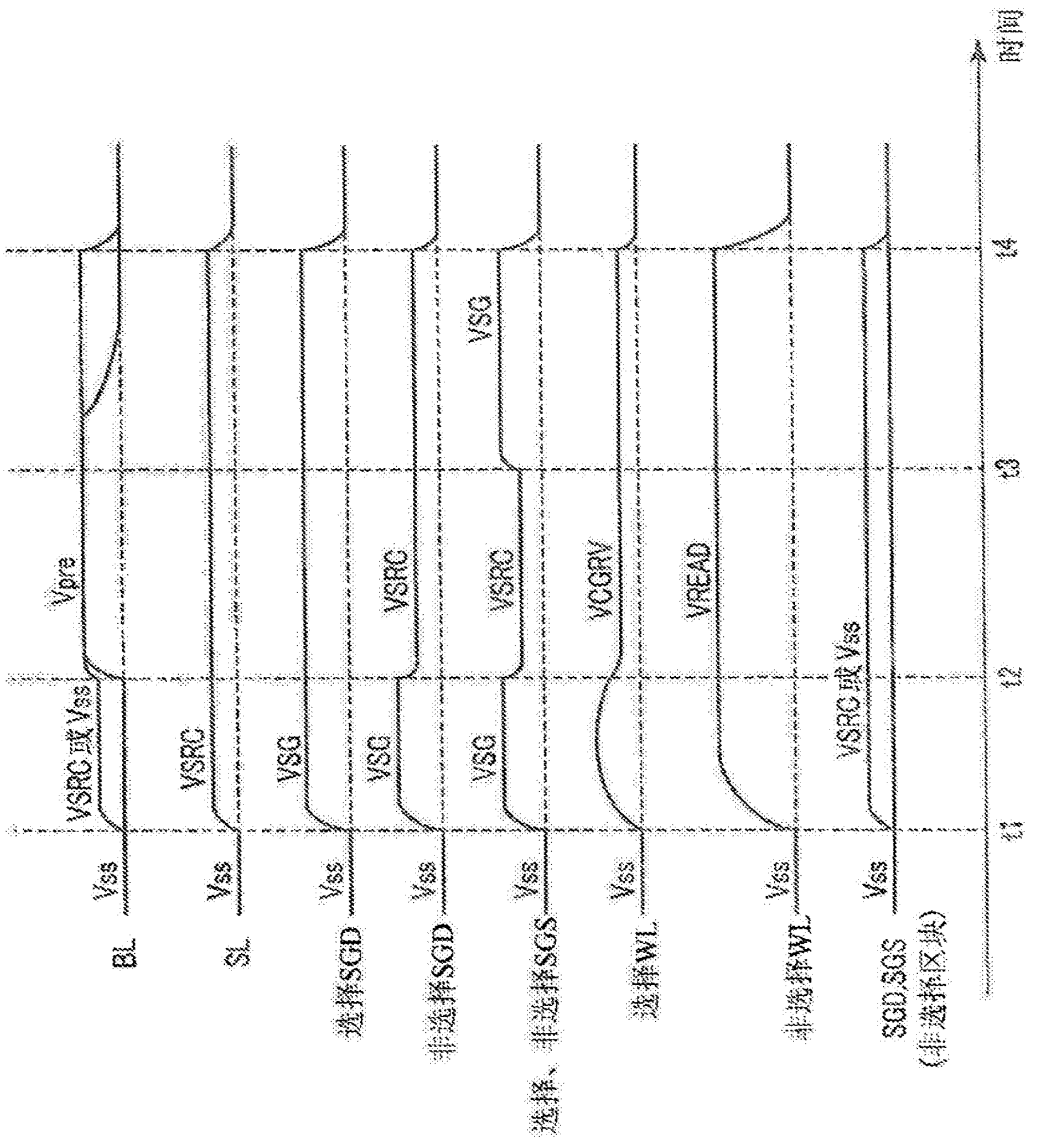


图13

Micron Ex. 1002, p. 224
Micron v. YMTC
IPR2024-00793

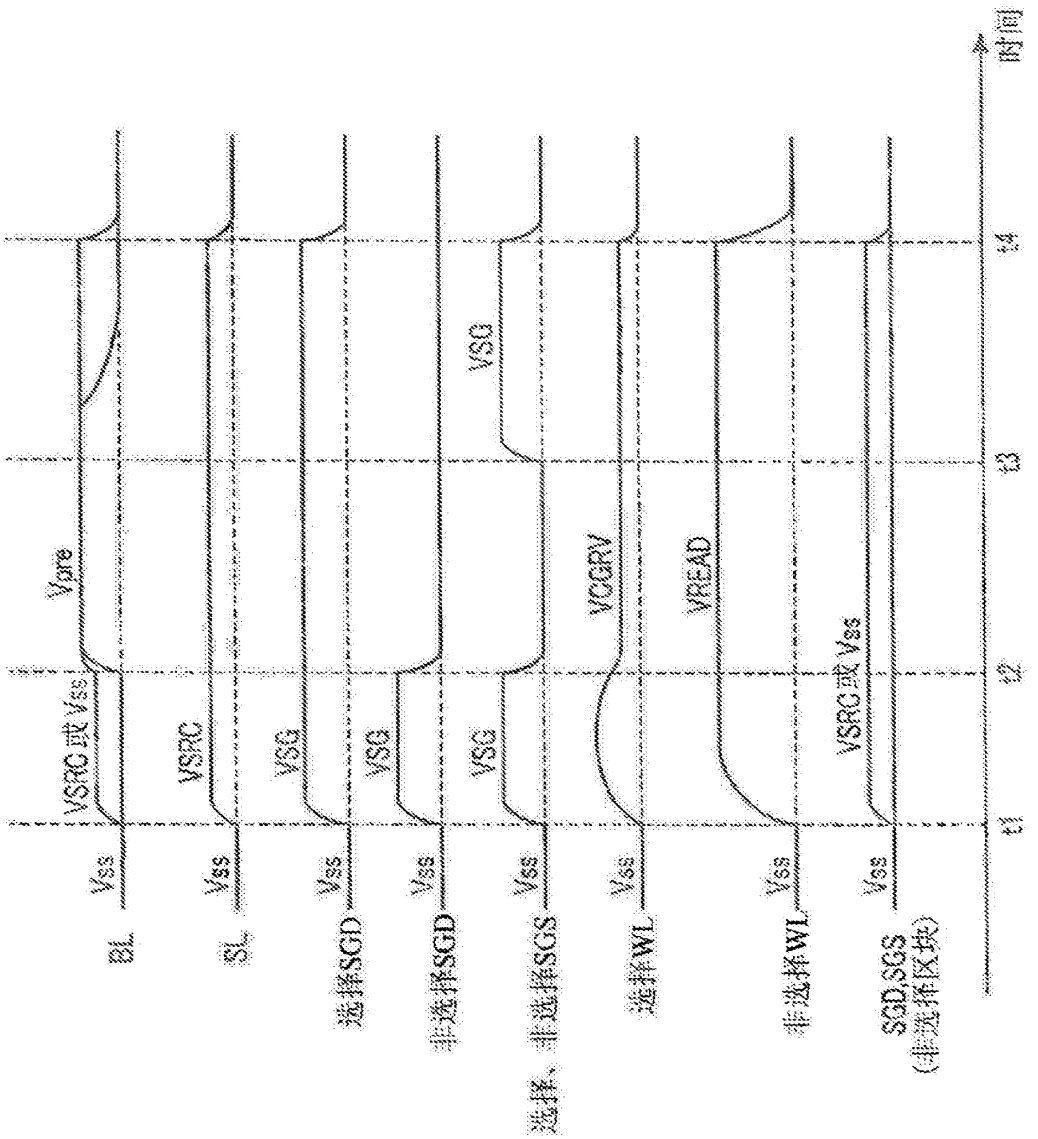


图14

Micron Ex. 1002, p. 225
Micron v. YMTC
IPR2024-00793

Espacenet

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Reading method of 3D NAND flash memory

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Classification: **- international:** ***G11C16/08; G11C16/26***
- cooperative: **G11C16/08 (CN); G11C16/26 (CN)**

Application number: CN201810864131 20180801 Global Dossier

Priority number(s): CN201810864131 20180801

Abstract of CN109065091 (A)

The invention relates to a method for reading 3D NAND flash memory, the 3D NAND flash memory includes a plurality of memory cells arranged in an array within a three-dimensional space, forming a plurality of memory strings, the transistor at the top of each memory string is an upper select transistor, the upper selection tube is connected to a bit line, the transistor at the bottom of the string is a lower select transistor, a plurality of memory cells located within the same layer form a memory row, the gates of the memory cells located in the same memory row are all connected to the same word line, and the memory string in which the memory cells are to be read is taken as a selected string. The reading method is characterized in that the reading method comprises the steps of a preconduction stage and a reading stage, wherein a continuous precharge voltage is applied to the bit line in the preconduction stage; at the same time, the upper selection tube of the selected string and the upper selection tube of the unselected string are turned on, and the lower selection tube of the selected string and the lower selection tube of the unselected string are turned off.

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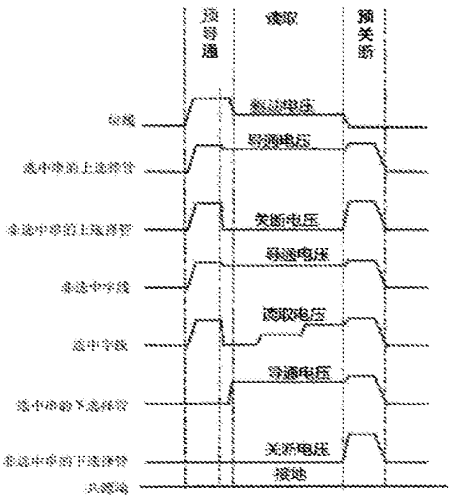
权利要求书1页 说明书4页 附图3页

(54)发明名称

3D NAND闪存的读取方法

(57)摘要

本发明涉及一种3D NAND闪存的读取方法，所述3D NAND闪存包括在三维空间内阵列排布的多个存储单元，构成多个存储串，每一个存储串的顶部的晶体管为上选择管，所述上选择管连接至位线，存储串底部的晶体管为下选择管，位于同一层内的多个存储单元组成存储行，位于同一存储行内的存储单元的栅极均连接至同一字线，待读取存储单元所在的存储串作为选中串，其特征在于，所述读取方法包括依次进行的预导通阶段和读取阶段步骤，其中，在所述预导通阶段中对位线施加持续的预充电压；同时，导通选中串的上选择管和非选中串的上选择管，关断选中串的下选择管和非选中串的下选择管。



CN 109065091 A

Micron Ex. 1002, p. 227
Micron v. YMTC
IPR2024-00793

1.一种3D NAND闪存的读取方法，所述3D NAND闪存包括在三维空间内阵列排布的多个存储单元，构成多个存储串，每一个存储串的顶部的晶体管为上选择管，所述上选择管连接至位线，存储串底部的晶体管为下选择管，位于同一层内的多个存储单元组成存储行，位于同一存储行内的存储单元的栅极均连接至同一字线，待读取存储单元所在的存储串作为选中串，其特征在于，所述读取方法包括依次进行的预导通阶段和读取阶段步骤，其中，在所述预导通阶段中对位线施加持续的预充电压；同时，导通选中串的上选择管和非选中串的上选择管，关断选中串的下选择管和非选中串的下选择管。

2.根据权利要求1所述的3D NAND闪存的读取方法，其特征在于，读取阶段中，对位线施加驱动电压；所述预充电压大于所述驱动电压。

3.根据权利要求1所述的3D NAND闪存的读取方法，其特征在于，在所述预导通阶段中还包括：在预导通阶段结束之前，关断所述非选中串的上选择管；对位线施加预充电压直至预导通阶段结束。

4.根据权利要求1所述的3D NAND闪存的读取方法，其特征在于，在所述预导通阶段中还包括：在对位线施加预充电压的同时，对选中字线和非选中字线施加预导通电压。

5.根据权利要求1所述的3D NAND闪存的读取方法，其特征在于，还包括位于所述读取阶段之后的预关断阶段；所述预关断阶段中，位线保持低电位。

6.根据权利要求5所述的3D NAND闪存的读取方法，其特征在于，所述预关断阶段中，导通选中串的上选择管、非选中串的上选择管、选择串的下选择管和非选中串的下选择管，以及对非选中字线和选中字线均施加预关断电压。

Micron Ex. 1002, p. 228
Micron v. YMTC
IPR2024-00793

3D NAND闪存的读取方法

技术领域

[0001] 本发明涉及半导体技术领域，尤其涉及一种3D NAND闪存的读取方法。

背景技术

[0002] 近年来，闪存(Flash Memory)存储器的发展尤为迅速。闪存存储器的主要特点是在不加电的情况下能长期保持存储的信息，且具有集成度高、存取速度快、易于擦除和重写等优点，因而在微机、自动化控制等多项领域得到了广泛的应用。为了进一步提高闪存存储器的位密度(Bit Density)，同时减少位成本(Bit Cost)，三维的闪存存储器(3D NAND)技术得到了迅速发展。

[0003] 在3D NAND闪存结构中，按照串和行进行三维排列，现有技术在对某一存储单元进行读取操作时，经常会对该存储单元相邻的其他存储单元造成读干扰的问题，造成数据漂移。

[0004] 如何在读取过程中，减少读干扰，提高读取数据的准确性，是目前亟待解决的问题。

发明内容

[0005] 本发明所要解决的技术问题是，提供一种3D NAND闪存的读取方法，在读取过程中减少读干扰。

[0006] 本发明提供一种3D NAND闪存的读取方法，所述3D NAND闪存包括在三维空间内阵列排布的多个存储单元，构成多个存储串，每一个存储串的顶部的晶体管为上选择管，所述上选择管连接至位线，存储串底部的晶体管为下选择管，位于同一层内的多个存储单元组成存储行，位于同一存储行内的存储单元的栅极均连接至同一字线，待读取存储单元所在的存储串作为选中串，所述读取方法包括依次进行的预导通阶段和读取阶段步骤，其中，在所述预导通阶段中对位线施加持续的预充电压；同时，导通选中串的上选择管和非选中串的上选择管，关断选中串的下选择管和非选中串的下选择管。

[0007] 可选的，读取阶段中，对位线施加驱动电压；所述预充电压大于所述驱动电压。

[0008] 可选的，在所述预导通阶段中还包括：在预导通阶段结束之前，关断所述非选中串的上选择管；对位线施加预充电压直至预导通阶段结束。

[0009] 可选的，在所述预导通阶段中还包括：在对位线施加预充电压的同时，对选中字线和非选中字线施加预导通电压。

[0010] 可选的，还包括位于所述读取阶段之后的预关断阶段；所述预关断阶段中，位线保持低电位。

[0011] 可选的，所述预关断阶段中，导通选中串的上选择管、非选中串的上选择管、选择串的下选择管和非选中串的下选择管，以及对非选中字线和选中字线均施加预关断电压。

[0012] 本发明的3D NAND闪存读取方法中，在正式读取之前具有预导通阶段，在预导通阶段，对位线施加预充电压，在读取阶段之前关断非选择串的上选择管和下选择管，使得在读

Micron Ex. 1002, p. 229
Micron v. YMTC
IPR2024-00793

取阶段非选中串的沟道电势等于预充电压，从而降低非选中串受到的读干扰，减少读取错误。

附图说明

[0013] 图1为本发明一具体实施方式的3D NAND的存储结构示意图；

[0014] 图2为本发明一具体实施方式的对3D NAND的存储单元进行读取的时序图；

[0015] 图3为本发明一具体实施方式的对3D NAND的存储单元进行读取的时序图。

具体实施方式

[0016] 下面结合附图对本发明提供的3D NAND闪存的读取方法的具体实施方式做详细说明。

[0017] 请参考图1，为本发明一具体实施方式的3D NAND的存储结构示意图。其中每个黑点代表一个存储单元。

[0018] 所述3D NAND的存储结构包括在三维空间内阵列排布的多个存储单元，构成多个存储串，位于同一个存储串内的存储单元的沟道在物理上连接。每一个存储串的顶部的晶体管为上选择管，上选择管连接至位线，存储串底部的晶体管为下选择管，不同存储串之间通过上选择管和下选择管区分。位于同一层内的多个存储单元组成存储行，位于不同存储串但位于同一存储行内的存储单元的栅极在物理上相连接，均连接至同一字线。

[0019] 在对所述存储结构中的某一存储单元进行读取操作时，需要确定选中的存储单元所在的存储串以及所在的行，所述选中的存储单元所在的存储串作为选中串，所在行作为选中行。例如，要读取图1中圈出的选中存储单元的信息，需要对位线1和位线2施加驱动电压，打开该选中存储单元所在选中串的上选择管1和下选择管1，将所述存储单元所在行以外的非选中行的字线1和字线3施加导通电压，从而将该选中串的沟道导通；并且关断非选中串的上选择管2和下选择管2，避免其他非选中串的沟道被导通；在选中行的字线2上加读取电压，对选中的存储单元内的信息进行读取。

[0020] 由于在所述非选中行的字线1和字线3上施加导通电压，这个导通电压在上升过程中会在连接至字线1和字线3上的所有存储单元的沟道内耦合出电势，造成热载流子注入串扰，从而导致其他非选中的存储单元内存储的电子发生漂移，从而发生非选中存储单元内存储的数据发生改变，以及读取的选中存储单元内的数据发生漂移等问题。

[0021] 请参考图2，为一个具体实施方式中的对3D NAND的存储单元进行读取的时序图。

[0022] 待读取的存储单元所在的存储串作为选中串，待读取的存储单元所在存储行作为选中行，连接至选中行的字线作为选中字线。该具体实施方式中，在对存储单元进行真正读取之前，会有一个预导通阶段，用来打开选中串和非选中串的沟道。

[0023] 具体的，在预导通阶段，对非选中字线和选中字线均施加预导通电压，以打开选中串和非选中串的沟道，在非选中字线和选中字线电压的上升时期，非选中串的上选择管和非选中串的下选择管施加的电压也跟随上升，这样使得所述非选中串的上选择管、非选中串的下选择管均打开；对所述选中串的上选择管、选中串的下选择管也施加预导通电压，使得所述选中串的上选择管、选中串的下选择管均打开；同时位线保持低电位。本发明的具体实施方式中，低电位均为0V，其他具体实施方式中低电位也可以为其他电压值。非选中串和

Micron Ex. 1002, p. 230
Micron v. YMTC
IPR2024-00793

选中串的沟道与位线导通，沟道电势会保持和位线同样的低电位，因此非选中串和选中串的沟道不会因为字线电压的变化而耦合出电压，从而避免对非选中存储单元的字线施加导通电压时造成的热载流子注入串扰的问题。

[0024] 到了读取阶段，对位线施加驱动电压，对非选中串的上选择管和非选中串的下选择管施加断开电压，使得非选中串的上选择管和下选择管均关断，使得非选中串的沟道与位线断开，非选中串的沟道电势被锁定为低电位0V。非选中串上加导通电压的非选中行的存储单元受到“导通电压-0V”引起的读干扰，而非选中串的选中行的存储单元则受到“读取电压-0V”引起的读干扰，读取电压与导通电压接近。

[0025] 而选中串的上选择管和下选择管则被施加导通电压，使得选中串的沟道与位线导通，选中串的沟道电势等于位线上的驱动电压。选中串上的非选中存储单元的栅极则通过非选中字线被施加导通电压，因此，选中串上的非选中存储单元会承受“导通电压-驱动电压”引起的读干扰。

[0026] 读干扰和引起读干扰的电压正相关，电压越大，读干扰越强。因此，导通电压越大，对存储单元的读干扰越大。因此，该具体实施方式中，选中串上的非选中存储单元承受“导通电压-驱动电压”引起的读干扰小于非选中串上的存储单元受到的读干扰。为了提高存储器读取的准确性，需要进一步降低非选中串上的存储单元受到的读干扰。

[0027] 为了进一步降低非选中串上的加导通电压的存储单元受到的读干扰，本发明的发明人提出了另一种3D NAND闪存的读取方法。

[0028] 请参考图3为本发明另一具体实施方式中采用另一读取方法对3D NAND的存储单元进行读取的时序图。

[0029] 该具体实施方式中，所述3D NAND闪存的读取方法，包括依次进行的预导通阶段和读取阶段步骤。

[0030] 在整个读取过程中，存储结构的共源端均接地。与上一具体实施方式中不同的是，在所述预导通阶段中：对位线施加持续的预充电压；同时，预导通选中串的上选择管和非选中串的上选择管，关断选中串的下选择管和非选中串的下选择管。

[0031] 在预导通阶段，还包括对选中行字线以及非选中行字线均施加预导通电压，使得各个存储单元的沟道打开。由于所述非选中串的上选择管导通，使得所述非选中串的沟道与位线导通，沟道电势等于位线上的预充电压。沟道电势与位线电压保持一致，使得在对字线施加电压时不会产生耦合电压，可以避免热载流子注入串扰的问题。

[0032] 由于对位线施加预充电压，若选中串的下选择管和非选中串的下选择管为打开状态，会导致较大的漏电，因此在预导通阶段需要关断选中串的下选择管和非选中串的下选择管。并且，关断选中串的下选择管和非选中串的下选择管使得各存储串的沟道和位线依然相通，不会产生热载流子注入干扰。

[0033] 该具体实施方式中，在预导通阶段结束之前，先关断所述非选中串的上选择管，而对位线施加预充电压直至预导通阶段结束。这样，在非选中串的上选择管关断之前，非选中串的沟道电势一直等于位线上的预充电压；当非选中串的上选择管关断，而同时所述非选中串的下选择管也处于关断状态，所述非选中串沟道中的电势会保持为预充电压。在其他具体实施方式中，也可以在预导通阶段结束时，将位线电压由预充电压调整为驱动电压的同时，关断所述非选中串的上选择管。

Micron Ex. 1002, p. 231
Micron v. YMTC
IPR2024-00793

[0034] 读取阶段中，对位线施加驱动电压，选中串的上选择管栅极和选中串的下选择管栅极均施加导通电压；非选中串的上选择管和下选择管的栅极均施加关断电压；非选中字线施加导通电压，而选中字线施加读取电压，对选中存储单元进行读取。在读取阶段中，非选择串的沟道电势为预充电压，非选中串上的非选中行的存储单元受到由“导通电压-预充电压”引起的读干扰，非选中串上的选中行上的非选中存储单元则受到“读取电压-预充电压”引起的读干扰。由于所述预充电压为高电压，因此该具体实施方式的读取方法能够有效减少非选择串上的存储单元的读干扰。

[0035] 而对于选中串，由于在读取阶段，选中串的上选择关和下选择管均打开，因此，选中串的沟道电势等于位线上的驱动电压，因此，选中串上的非选中存储单元受到由“导通电压-驱动电压”引起的读干扰。

[0036] 在一个具体实施方式中，所述预充电压大于所述驱动电压，使得非选择串上的存储单元受到的读干扰小于选中串上的存储单元受到的读干扰，进而更大程度上减少读取错误。

[0037] 本发明的具体实施方式中，所述读取方法包括位于所述读取阶段之后的预关断阶段。在所述预关断阶段中，停止对连接选中串的位线施加电压，使得所述位线电压保持低电位。而对所述选中串的上选择管和下选择管、非选中串的上选择管和下选择管施加导通电压，使它们均被打开，同时对选中字线和非选中字线均施加导通电压，使得选中串和非选中串的沟道均导通至位线，共源端接地，将选中串和非选中串沟道内的电子均导出，将各存储单元沟道电势都拉低为0，以便于进行后续的读取或擦写操作。

[0038] 本发明的具体实施方式在对3D NAND闪存进行读取的过程中，在正式读取之前具有预导通阶段，在预导通阶段，对位线施加预充电压，在读取阶段之前关断非选择串的上选择管和下选择管，使得在读取阶段非选中串的沟道电势等于预充电压，从而降低非选中串受到的读干扰，进而减少在对3D NAND闪存进行读取过程中的读取错误。

[0039] 以上所述仅是本发明的优选实施方式，应当指出，对于本技术领域的普通技术人员，在不脱离本发明原理的前提下，还可以做出若干改进和润饰，这些改进和润饰也应视为本发明的保护范围。

Micron Ex. 1002, p. 232
Micron v. YMTC
IPR2024-00793

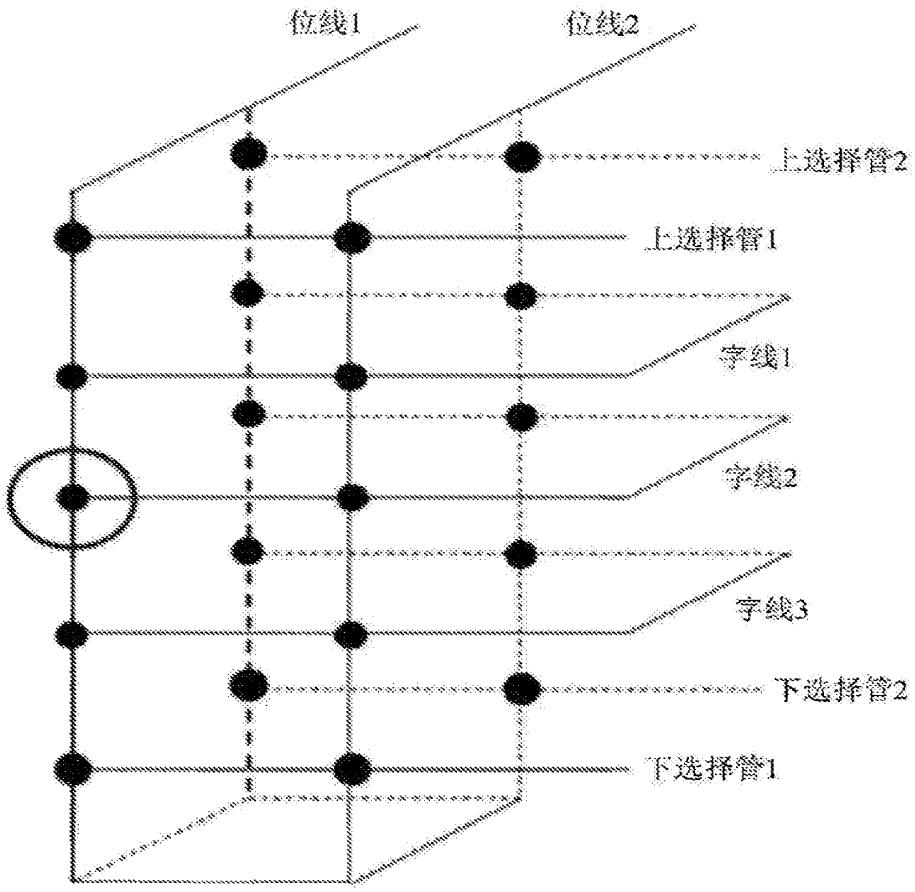


图1

Micron Ex. 1002, p. 233
Micron v. YMTC
IPR2024-00793

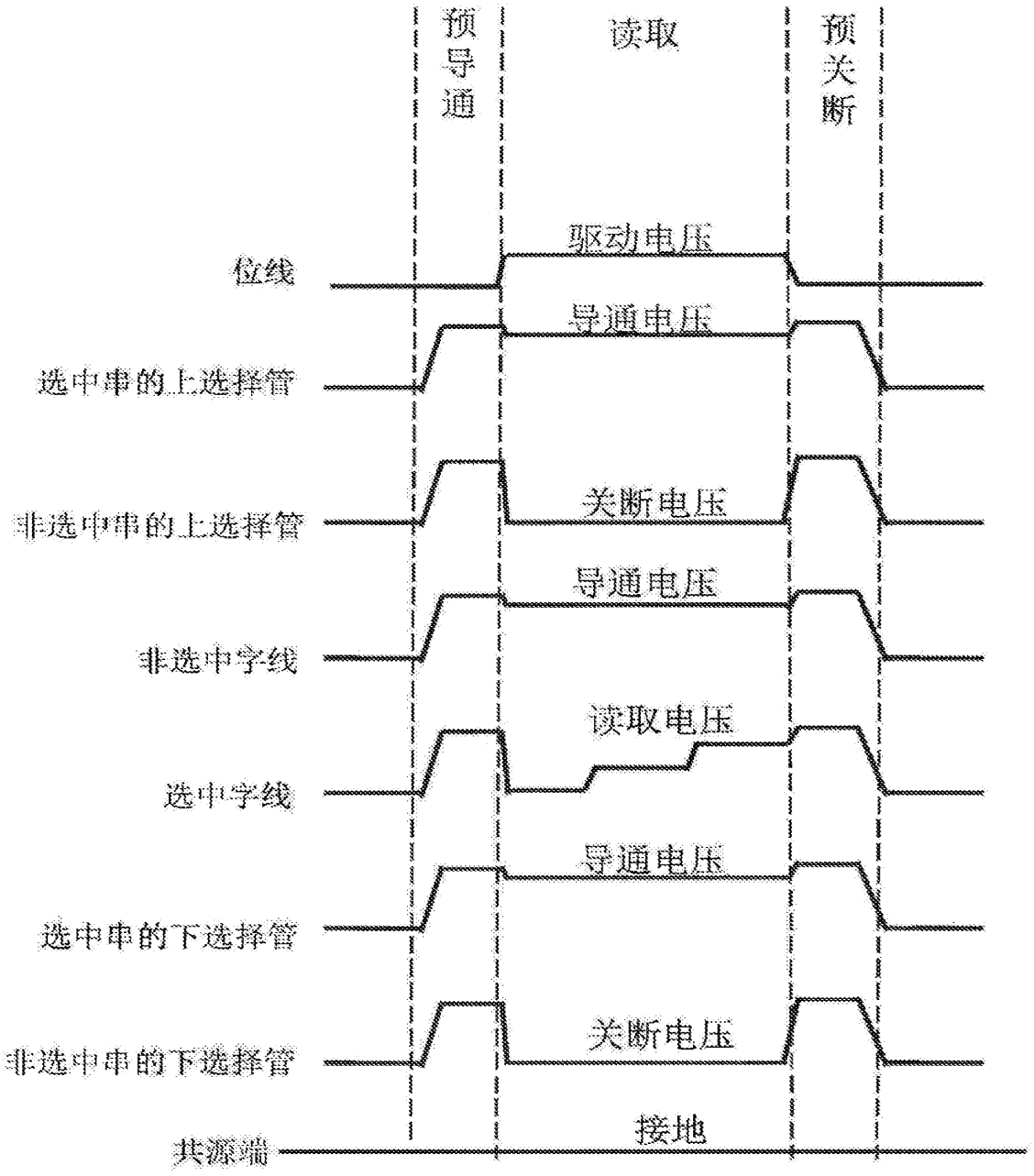


图2

Micron Ex. 1002, p. 234
Micron v. YMTC
IPR2024-00793

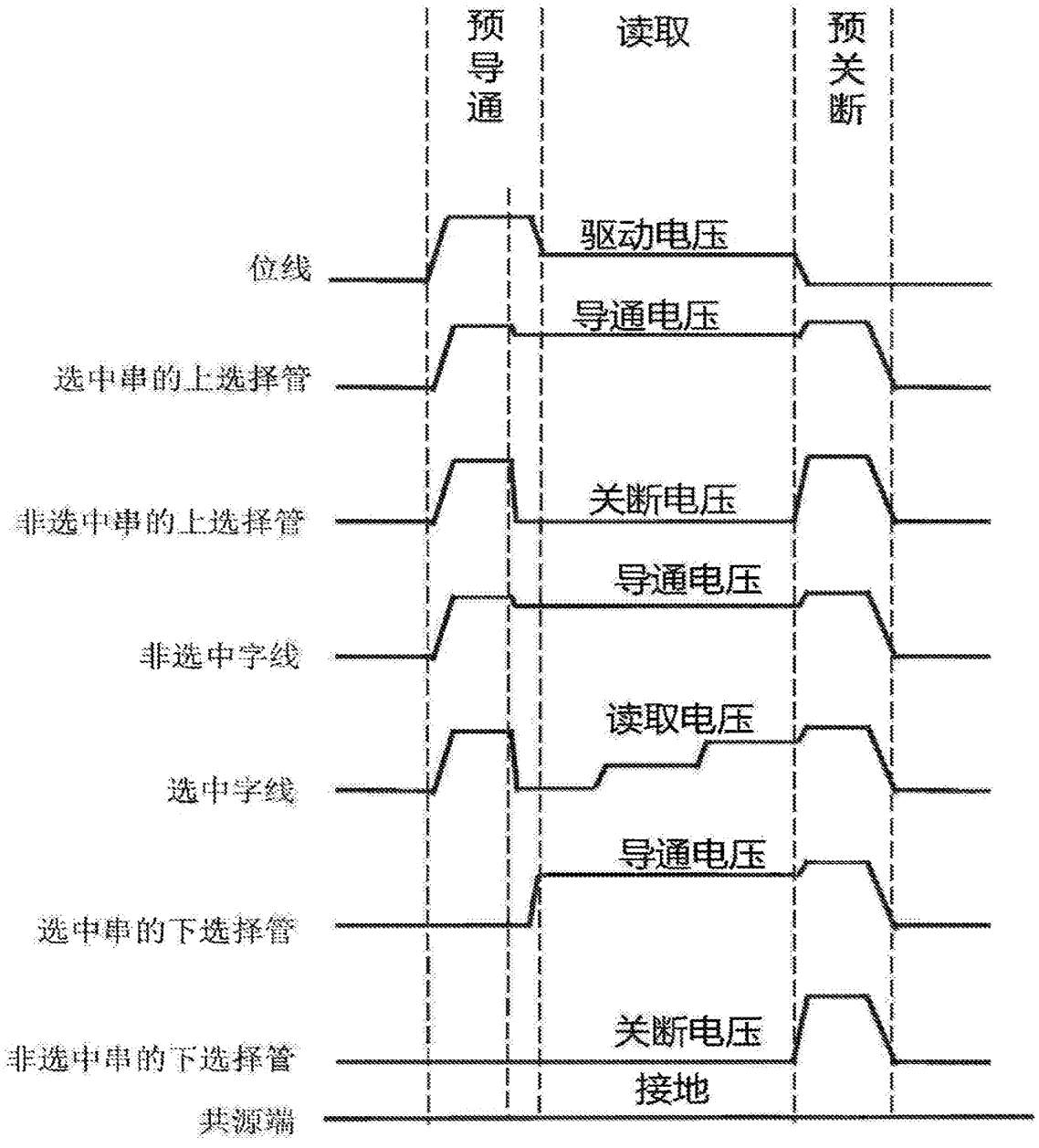


图3

Micron Ex. 1002, p. 235
Micron v. YMTC
IPR2024-00793

Espacenet

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Data reading method and device of flash memory, storage equipment and storage medium

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Abstract of CN109584938 (A)

The embodiment of the invention discloses a data reading method and device of a flash memory, storage equipment and a storage medium. The method comprises the following steps of: in an interference suppression stage of a reading period, applying a first voltage for reducing reading interference to a word line selected by a flash memory; In the reading phase of the reading period,applying a secondvoltage of reading data to the word line selected by the flash memory.

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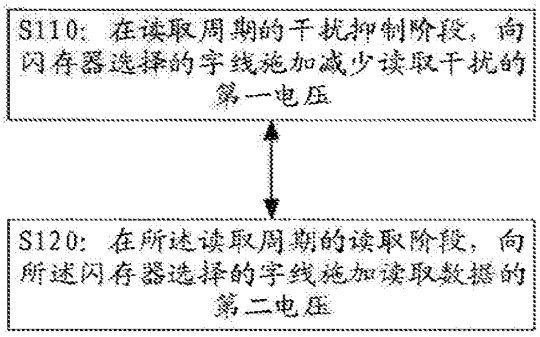
权利要求书3页 说明书11页 附图6页

(54)发明名称

闪存器的数据读取方法及装置、存储设备及存储介质

(57)摘要

本发明实施例公开了一种闪存器的数据读取方法及装置、存储设备及存储介质。所述方法包括：在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压；在所述读取周期的读取阶段，向所述闪存器选择的字线施加读取数据的第二电压。



CN 109584938 A

Micron Ex. 1002, p. 237
Micron v. YMTC
IPR2024-00793

1.一种闪存器的数据读取方法，其特征在于，包括：

在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压；

在所述读取周期的读取阶段，向所述闪存器选择的字线施加读取数据的第二电压。

2.根据权利要求1所述的方法，其特征在于，

所述在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压，包括以下至少之一：

在位于所述读取阶段的第一干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一子电压；

在位于所述读取阶段之后的第二干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第二子电压。

3.根据权利要求2所述的方法，其特征在于，

所述在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压，包括以下至少之一：

在所述第一干扰抑制阶段，通过升压使得施加在选择的字线上的电压达到所述第一子电压；在维持所述第一子电压的时长达到第一时长之后，通过降压使得施加在选择的字线上的电压下降到所述第二电压，以进入所述读取阶段；

通过升压使得施加在选择的字线上的所述第二电压上升到第二子电压，以从所述读取阶段进入所述第二干扰抑制阶段，并维持所述第二子电压达到第二时长后，通过降压进行电压恢复。

4.根据权利要求1所述的方法，其特征在于，

所述第二电压小于所述第一电压。

5.根据权利要求1所述的方法，其特征在于，

一个所述干扰抑制阶段的时长与一个所述读取阶段的时长比值为：1:N；N为大于1。

6.根据权利要求4所述的方法，其特征在于，

所述时长比值的取值区间为：1.5至6。

7.根据权利要求1所述的方法，其特征在于，所述方法还包括：

从第一模式和第二模式中选择目标读取模式；

所述在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压，包括：

若所述目标读取模式为所述第一模式，在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压。

8.根据权利要求7所述的方法，其特征在于，

所述从第一模式和第二模式中选择目标读取模式，包括：

根据所述存储器的状况参数，从所述第一模式和所述第二模式中选择目标读取模式。

9.根据权利要求8所述的方法，其特征在于，

所述根据所述存储器的状况参数，从所述第一模式和所述第二模式中选择目标读取模式，包括以下至少之一：

根据所述闪存器的当前读取负载状况，从所述第一模式和所述第二模式中选择目标读取模式；

Micron Ex. 1002, p. 238
Micron v. YMTC
IPR2024-00793

根据读取的存储页或存储块的读取次数，从所述第一模式和所述第二模式中选择目标读取模式；

根据读取数据的读取速率要求，从所述第一模式和所述第二模式中选择目标读取模式。

10.一种闪存器读取装置，其特征在于，包括：

第一施加模块，用于在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压；

第二施加模块，用于在所述读取周期的读取阶段，向所述闪存器选择的字线施加读取数据的第二电压。

11.根据权利要求10所述的装置，其特征在于，

所述第一施加模块，具体用于执行以下至少之一：

在位于所述读取阶段的第一干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一子电压；

在位于所述读取阶段之后的第二干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第二子电压。

12.根据权利要求11所述的装置，其特征在于，

所述第一施加模块，具体用于执行以下至少之一：

在所述第一干扰抑制阶段，通过升压使得施加在选择的字线上的电压达到所述第一子电压；在维持所述第一子电压的时长达到第一时长之后，通过降压使得施加在选择的字线上的电压下降到所述第二电压，以进入所述读取阶段；

通过升压使得施加在选择的字线上的所述第二电压上升到第二子电压，以从所述读取阶段进入所述第二干扰抑制阶段，并维持所述第二子电压达到第二时长后，通过降压进行电压恢复。

13.根据权利要求10所述的装置，其特征在于，

所述第二电压小于所述第一电压。

14.根据权利要求10所述的装置，其特征在于，

一个所述干扰抑制阶段的时长与一个所述读取阶段的时长比值为：1:N;N为大于1。

15.根据权利要求14所述的装置，其特征在于，

所述时长比值的取值区间为：1.5至6。

16.根据权利要求10所述的装置，其特征在于，所述装置还包括：

选择模块，用于从第一模式和第二模式中选择目标读取模式；

所述第一施加模块，具体用于若所述目标读取模式为所述第一模式，在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压。

17.根据权利要求16所述的装置，其特征在于，

所述选择模块，具体用于根据所述存储器的状况参数，从所述第一模式和所述第二模式中选择目标读取模式。

18.根据权利要求17所述的装置，其特征在于，

所述选择模块，具体用于执行以下至少之一：

根据所述闪存器的当前读取负载状况，从所述第一模式和所述第二模式中选择目标读

Micron Ex. 1002, p. 239
Micron v. YMTC
IPR2024-00793

取模式：

根据读取的存储页或存储块的读取次数，从所述第一模式和所述第二模式中选择目标读取模式；

根据读取数据的读取速率要求，从所述第一模式和所述第二模式中选择目标读取模式。

19.一种存储设备，其特征在于，包括：

闪存器，

控制器，与所述存储器连接，用于通过计算机可执行指令的执行，通过权利要求1至9任一项提供的方法从所述闪存器读取数据。

20.一种计算机存储介质，所述计算机存储介质存储有计算机可执行指令；所述计算机可执行指令被执行后，能够实现权利要求1至9任一项提供的方法。

Micron Ex. 1002, p. 240
Micron v. YMTC
IPR2024-00793

闪存器的数据读取方法及装置、存储设备及存储介质

技术领域

[0001] 本发明涉及存储技术领域，尤其涉及一种闪存器的数据读取方法及装置、存储设备及存储介质。

背景技术

[0002] 闪存器是一种具有数据记忆功能的非易失性存储器。闪存器的读写可以是以页为单位进行的。由于闪存器存储容量大的特点，大量的应用各种电子设备。所述闪存器按照其存储阵列的堆叠状况，可以分为二维的2D闪存器和三维的3D闪存器。

[0003] 在应用过程中发现一些数据写入存储单元之后，经过多次读写会比较快的数据记忆错误，且在一些情况下这种数据记忆错误是无法通过存储校正的方式校正的不可修复错误。故如何减缓这种数据记忆错误的出现和/或减少不可修复错误的出现，是亟待解决的问题之一。

发明内容

[0004] 有鉴于此，本发明实施例期望提供一种闪存器的数据读取方法及装置、存储设备及存储介质。

[0005] 本发明的技术方案是这样实现的：

[0006] 一种闪存器的数据读取方法，包括：

[0007] 在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压；

[0008] 在所述读取周期的读取阶段，向所述闪存器选择的字线施加读取数据的第二电压。

[0009] 基于上述方案，所述在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压，包括以下至少之一：

[0010] 在位于所述读取阶段的第一干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一子电压；

[0011] 在位于所述读取阶段之后的第二干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第二子电压。

[0012] 基于上述方案，所述在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压，包括以下至少之一：

[0013] 在所述第一干扰抑制阶段，通过升压使得施加在选择的字线上的电压达到所述第一子电压；在维持所述第一子电压的时长达到第一时长之后，通过降压使得施加在选择的字线上的电压下降到所述第二电压，以进入所述读取阶段；

[0014] 通过升压使得施加在选择的字线上的所述第二电压上升到第二子电压，以从所述读取阶段进入所述第二干扰抑制阶段，并维持所述第二子电压达到第二时长后，通过降压进行电压恢复。

Micron Ex. 1002, p. 241
Micron v. YMTC
IPR2024-00793

[0015] 基于上述方案，所述第二电压小于所述第一电压。

[0016] 基于上述方案，一个所述干扰抑制阶段的时长与一个所述读取阶段的时长比值为：1:N;N为大于1。

[0017] 基于上述方案，所述时长比值的取值区间为：1.5至6。

[0018] 基于上述方案，所述方法还包括：

[0019] 从第一模式和第二模式中选择目标读取模式；

[0020] 所述在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压，包括：

[0021] 若所述目标读取模式为所述第一模式，在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压。

[0022] 基于上述方案，所述从第一模式和第二模式中选择目标读取模式，包括：

[0023] 根据所述存储器的状况参数，从所述第一模式和所述第二模式中选择目标读取模式。

[0024] 基于上述方案，所述根据所述存储器的状况参数，从所述第一模式和所述第二模式中选择目标读取模式，包括以下至少之一：

[0025] 根据所述闪存器的当前读取负载状况，从所述第一模式和所述第二模式中选择目标读取模式；

[0026] 根据读取的存储页或存储块的读取次数，从所述第一模式和所述第二模式中选择目标读取模式；

[0027] 根据读取数据的读取速率要求，从所述第一模式和所述第二模式中选择目标读取模式。

[0028] 一种闪存器读取装置，包括：

[0029] 第一施加模块，用于在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压；

[0030] 第二施加模块，用于在所述读取周期的读取阶段，向所述闪存器选择的字线施加读取数据的第二电压。

[0031] 基于上述方案，所述第一施加模块110，具体用于执行以下至少之一：

[0032] 在位于所述读取阶段的第一干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一子电压；

[0033] 在位于所述读取阶段之后的第二干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第二子电压。

[0034] 基于上述方案，所述第一施加模块110，具体用于执行以下至少之一：

[0035] 在所述第一干扰抑制阶段，通过升压使得施加在选择的字线上的电压达到所述第一子电压；在维持所述第一子电压的时长达到第一时长之后，通过降压使得施加在选择的字线上的电压下降到所述第二电压，以进入所述读取阶段；

[0036] 通过升压使得施加在选择的字线上的所述第二电压上升到第二子电压，以从所述读取阶段进入所述第二干扰抑制阶段，并维持所述第二子电压达到第二时长后，通过降压进行电压恢复。

[0037] 基于上述方案，所述第二电压小于所述第一电压。

Micron Ex. 1002, p. 242
Micron v. YMTC
IPR2024-00793

[0038] 基于上述方案，一个所述干扰抑制阶段的时长与一个所述读取阶段的时长比值为：1：N；N为大于1。

[0039] 基于上述方案，所述时长比值的取值区间为：1.5至6。

[0040] 基于上述方案，所述装置还包括：

[0041] 选择模块，用于从第一模式和第二模式中选择目标读取模式；

[0042] 所述第一施加模块，具体用于若所述目标读取模式为所述第一模式，在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压。

[0043] 基于上述方案，所述选择模块，具体用于根据所述存储器的状况参数，从所述第一模式和所述第二模式中选择目标读取模式。

[0044] 基于上述方案，所述选择模块，具体用于执行以下至少之一：

[0045] 根据所述闪存器的当前读取负载状况，从所述第一模式和所述第二模式中选择目标读取模式；

[0046] 根据读取的存储页或存储块的读取次数，从所述第一模式和所述第二模式中选择目标读取模式；

[0047] 根据读取数据的读取速率要求，从所述第一模式和所述第二模式中选择目标读取模式。

[0048] 一种存储设备，其特征在于，包括：

[0049] 闪存器，

[0050] 控制器，与所述存储器连接，用于通过计算机可执行指令的执行，通过前述任意技术方案提供的闪存器的数据读取方法从所述闪存器读取数据。

[0051] 一种计算机存储介质，所述计算机存储介质存储有计算机可执行指令；所述计算机可执行指令被执行后，能够实现前述任意技术方案提供的闪存器的数据读取方法。

[0052] 本发明实施例提供的技术方案，在一个读取周期内会利用干扰抑制阶段向闪存器选择的字线施加第一电压，如此，与选择的字线连接的存储单元，就可以在干扰抑制阶段导通，释放掉自身沟道内影响其相邻存储单元的数据读取的干扰电荷，从而减少对其相邻的存储单元中读取的数据的干扰，提升存储器的数据存储准确率，并进一步减少，因为存储单元内数据反复读取导致电荷累积产生的记忆错误的现象、减少数据不可修复错误的出现概率、或延迟数据不可修复错误的出现时间。

附图说明

[0053] 图1为本发明实施例提供的第一种闪存器的数据读取方法的流程示意图；

[0054] 图2为本发明实施例提供的第二种闪存器的数据读取方法的流程示意图；

[0055] 图3A为本发明实施例提供的一种读取周期的示意图；

[0056] 图3B为本发明实施例提供的另一种读取周期的示意图；

[0057] 图3C为本发明实施例提供的又一种读取周期的示意图；

[0058] 图4为本发明实施例提供的第三种闪存器的数据读取方法的流程示意图；

[0059] 图5为本发明实施例提供的闪存器读取装置的结构示意图；

[0060] 图6A为本发明实施例提供的一种存储阵列的示意图；

[0061] 图6B为本发明实施例提供的另一种存储阵列的示意图；

Micron Ex. 1002, p. 243
Micron v. YMTC
IPR2024-00793

[0062] 图7A为本发明实施例提供的一种PHCI的形成示意图；

[0063] 图7B为本发明实施例提供的一种NHCI的形成示意图；

[0064] 图7C为本发明实施例提供的一种开启电压的变化示意图；

[0065] 图8为本发明实施例提供的一种闪存器的读取方法的读取电压的示意图。

具体实施方式

[0066] 以下结合说明书附图及具体实施例对本发明的技术方案做进一步的详细阐述。

[0067] 如图1所示，本实施例提供一种闪存器的数据读取方法，包括：

[0068] 步骤S110：在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压；

[0069] 步骤S120：在所述读取周期的读取阶段，向所述闪存器选择的字线施加读取数据的第二电压。

[0070] 本实施例提供的闪存器的数据读取方法可应用于包括闪存器的存储设备中。

[0071] 所述存储设备可包括：存储阵列；所述存储这列由多个存储单元排列形成。

[0072] 存储阵列内设置有与存储单元的栅极连接的字线，与存储单元的漏极连接的位线。若需要从存储单元上读取数据，需要通过在字线上施加高于接地点所对应的参考电压的读取电压(即为步骤S120中的第二电压)，若存储单元导通，则施加在位线上的电压就可以被检测到。若存储单元没有被导通，则当前施加在位线上的电压就不会被检测到。故此时，可在字线和位线上施加一定电压，根据存储单元的导通状况，确定对应的存储单元记忆的数据是“1”还是“0”。若存储单元写入的数据为“1”，则存储单元的沟通内保存有写入数据时所注入的载流子，可能需要在字线上施加更大的电压才能被导通。故在一些实施例中个，所述第二电压可等于或约等于写入数据“1”所对应的电压；如此，若存储单元导通则认为存储当前存储的数据为“0”，否则可为“1”。

[0073] 在本实施例中读取所述闪存器时，读取周期至少分为两种阶段，一种读取阶段，在该读取阶段用于从闪存器的存储单元上读取数据；另一种干扰抑制阶段，用于减少读取干扰。

[0074] 在一些实施例中，所述干扰抑制阶段可为一个或多个，所述干扰抑制阶段可位于所述读取阶段之前，也可以位于所述读取阶段之后。

[0075] 在另一些实施例中，所述读取阶段也可以为一个或多个；但是若所述读取阶段为多个，则所述读取阶段是连续分布的；多个读取阶段所对应的电压可能有轻微的变化；例如，在一个读取阶段结束之后时，微调所述第二电压进入下一个读取阶段，直到完成预定个数的读取阶段为止。

[0076] 根据读取地址确定出闪存器中存储阵列中当前被选择导通的字线，这种字线称之为选择的字线。在干扰抑制阶段，向闪存器的选择的字线施加第一电压，此处的第一电压相对于参考电压而言是高电压，是可以导通对应的存储单元的电压；如此，第一电压施加到选择的字线上之后，对应的存储单元被导通，如此，导通的存储单元被连接到接地点，如此，因为载流子注入效应导致的沟道内累计电荷可以被释放掉，从而减少读取干扰。

[0077] 在一些实施例中，为了尽可能消除沟道内累计的电荷对读取干扰，会所述第一电压可大于所述第二电压，所述第二电压可为所述读取阶段所使用的读取数据的电压；如此，

Micron Ex. 1002, p. 244
Micron v. YMTC
IPR2024-00793

即便沟道内累计的电荷高于读取阶段的第二电压，由于第一电压大于第二电压，相应的存储单元依然被导通了，沟通内的电压在存储单元导通的情况下，是可以被释放掉的；从而在本读取周期内或下一读取周期内减少电荷累计导致的读取错误。

[0078] 在一些实施例中，如图2所示，所述步骤S110可包括以下至少之一：

[0079] 步骤S111：在位于所述读取阶段的第一干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一子电压，其中，所述第一干扰抑制阶段位于所述读取阶段之前；

[0080] 步骤S112：在位于所述读取阶段之后的第二干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第二子电压，其中，所述第二干扰抑制阶段位于所述读取阶段之前。

[0081] 即所述干扰抑制阶段可包括位于读取阶段之前的第一干扰抑制阶段，或，仅包括位于读取阶段之后的第二干扰抑制阶段，或者，还可同时包括所述第一干扰抑制阶段和第二干扰抑制阶段。

[0082] 例如，位于所述读取阶段之前的第一干扰抑制阶段，用于降低正向电压造成的热载流子注入效应PHCI导致的读取干扰；

[0083] 位于所述读取阶段之后的第二干扰抑制阶段，用于降低负向电压造成的热载流子注入效应NHCI导致的读取干扰。

[0084] 在本实施例中，若所述干扰抑制阶段为第一干扰抑制阶段，则所述第一电压等于所述第一子电压；若所述干扰抑制阶段为第二干扰抑制阶段，则所述第一电压为所述第二子电压。在本实施例中，所述第一子电压和所述第二子电压可以相等，也可以不等。在一些实施例中，为了简化控制，所述第一子电压和所述第二子电压可以相等。

[0085] 图3A和图3B为本发明实施例提供的几种不同的读取周期示意图。

[0086] 在图3A中，读取周期包括：第一干扰抑制阶段和读取阶段；

[0087] 在图3B中，读取周期包括：读取阶段和第二干扰抑制阶段；

[0088] 在图3C中，读取周期包括：第一干扰抑制阶段、读取阶段及第二干扰抑制阶段。

[0089] 在一些实施例中，所述步骤S110可包括以下至少之一：

[0090] 在所述第一干扰抑制阶段，通过升压使得施加在选择的字线上的电压达到第一子电压；在维持所述第一子电压的时长达到第一时长之后，通过降压使得施加在选择的字线上的电压下降到所述第二电压，以进入所述读取阶段；

[0091] 通过升压使得施加在选择的字线上的所述第二电压上升到第二子电压，以从所述读取阶段进入所述第二干扰抑制阶段，并维持所述第二子电压达到第二时长后，通过降压进行电压恢复。

[0092] 如此，若所述读取周期同时包括第一干扰抑制阶段及所述第二干扰抑制阶段，则从所述存储器上读取数据可包括：

[0093] 在第一干扰抑制阶段，通过升压使得施加在选择的字线上的电压达到第一子电压，使得存储单元被导通以释放存储单元的至少部分沟道电势；释放的部分沟道电势可为热流子注入效应导致的；

[0094] 在维持所述第一子电压的时长达到第一时长之后，通过降压使得施加在选择的字线上的电压下降到所述第二电压，以进入所述读取阶段；此处的第一时长，可为预先确定释放掉热流子注入效应导致的沟道电势所需的时间；

[0095] 在读取阶段，根据存储单元是否被导通确定当前存储单元写入的数据，例如，通过

Micron Ex. 1002, p. 245
Micron v. YMTC
IPR2024-00793

在存储单元所连接的字线上施加对应于数据“1”的第二电压，若存储单元当前导通，则认为该存储单元写入的数据“0”，否则可认为该存储单元写入的数据为“1”；

[0096] 在维持所述第二电压值的时长达到第二时长之后，通过升压使得施加在选择的字线上的电压上升到第二子电压，以进入所述第二干扰抑制阶段。此处的第二时长，可为预先确定释放掉热流子注入效应导致的沟道电势所需的时间。

[0097] 为了实现沟道内累计的电荷对其他存储单元的读取的干扰，一方面需要保证干扰抑制阶段有足够长的时间来释放干扰电荷，另一方面，需要减少不必要的时间浪费，以确保一定的读取速率。故在本实施例中，一个所述干扰抑制阶段的时长将等于或小于所述读取阶段的时长。通常情况下，所述干扰抑制阶段，所述第一时长和所述第二时长，与一个读取阶段的时长具有一定的对应关系。例如，一个所述干扰抑制阶段的时长与一个所述读取阶段的时长之间的时长比值，可为1:N；其中，N为大于1的数。进一步地，所述时长比值的取值区间为：1.5至6。此时，所述第一时长和所述第二时长都会小于一个所述读取阶段的时长。

[0098] 在一些实施例中，所述第一时长和所述第二时长可以相等，也可以不等；为了简化控制，所述第一时长和所述第二时长可以相等。

[0099] 在一些实施例中，如图4所示，所述方法还包括：

[0100] 步骤S100：从第一模式和第二模式中选择目标读取模式；其中，所述第一模式的读取周期包括：干扰抑制阶段和读取阶段；所述第二模式的读取周期包括：读取阶段；

[0101] 所述步骤S110可包括：若所述目标读取模式为所述第一模式，在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压。

[0102] 所述第一模式又可以分为第一子模式、第二子模式及第三子模式；

[0103] 其中，所述第一子模式的读取周期包括：第一干扰抑制阶段和读取阶段；

[0104] 所述第二子模式的读取周期包括：读取阶段和第二干扰抑制阶段；

[0105] 所述第三子模式的读取周期包括：第一干扰抑制阶段、读取阶段及第三干扰抑制阶段。

[0106] 所述第二模式可为常规读取模式，第二模式的读取周期相对于第一模式的读取周期，少了所述干扰抑制阶段。例如，所述第二模式的读取周期仅包括：读取阶段。

[0107] 在本实施例中，存储设备在读取闪存器的数据之前，需要从第一模式和第二模式中选择一个当前用户数据读取的目标读取模式。

[0108] 若选择目标读取模式为所述第一模式，才会执行所述步骤S110，在读取周期内引入干扰抑制阶段，实现存储单元内热流子效应注入的载流子的释放，以减少读取干扰。

[0109] 在本实施例中，存储设备可以根据当前的状况参数，选择合适当前状态的目标读取模式。由于第一模式的读取周期比第二模式的读取周期多了干扰抑制阶段，则第一模式的读取周期比第二模式的读取周期长，若当前需要求较高速率的读取数据，则可以选择第二模式作为所述目标读取模式，否则可以选择所述第一模式作为目标读取模式。

[0110] 在一些实施例中，所述步骤S100可具体包括以下至少之一：

[0111] 根据所述闪存器的当前读取负载状况，从所述第一模式和所述第二模式中选择目标读取模式；

[0112] 根据读取的存储页或存储块的读取次数，从所述第一模式和所述第二模式中选择目标读取模式；

Micron Ex. 1002, p. 246
Micron v. YMTC
IPR2024-00793

[0113] 根据读取数据的读取速率要求，从所述第一模式和所述第二模式中选择目标读取模式。

[0114] 例如，当前该闪存器有大量的读取任务，则闪存器的当前读取负载就大或者读取负载比值就比较高，则此时可有优先选择第二模式作为目标读取模式，则在一个读取周期内就不用执行干扰抑制阶段所消耗的时间，加速读取速率，降低读取负载量或负载率。

[0115] 具体可如：根据所述闪存器的当前读取负载状况，从所述第一模式和所述第二模式中选择目标读取模式，包括：

[0116] 若所述闪存器的当前读取负载率大于第一负载率，或者，所述闪存器的当前读取负载量大于第一负载量，为了迅速降低负载率或负载量，可以优先考虑所述第二模式为目标读取模式，否则可以优先选择第一模式为目标读取模式。

[0117] 再例如，所述根据读取的存储页或存储块的读取次数，从所述第一模式和所述第二模式中选择目标读取模式，包括：

[0118] 闪存器的某一个存储页或存储块写入数据之后的次数低于第一次数，则选择第二模式作为所述目标读取模式，否则可以选择第一模式作为所述目标读取模式。

[0119] 若闪存器被读取数据的存储也或存储块写入数据之后被反复读取，则由于读取电压导致的沟道的热载流子注入效应，会导致沟道内堆积有电荷，则此时为了减少由于读取过程中的电压进一步造成沟道内电荷的堆积，可以优先选择第一模式作为目标读取模式，否则可以从读取速率等读取性能考虑，优先考虑选择第二模式作为目标读取模式。

[0120] 当前存储设备在向外设高速传输数据，或者，存储设备自身因为数据输出的需求（例如，高清视频输出），需要从闪存器上高速读取数据。在本实施例中，所述根据读取数据的读取速率要求，从所述第一模式和所述第二模式中选择目标读取模式，可包括：

[0121] 若读取数据的速率要求达到预定要求，则选择第二模式为目标读取模式，否则可以选择第一模式作为目标读取模式。

[0122] 具体如，如存储设备处于高速传输状态下或者高清视频显示状态下，则可认定所述速率要求达到所述预定要求。

[0123] 在一些实施例中，所述方法还包括：

[0124] 若确定选择第一模式作为目标读取模式，根据所述闪存器的当前状况参数从所述第一子模式、第二子模式及第三子模式中选择一种作为所述目标读取模式。

[0125] 例如，若所述闪存器的当前负载量低于第二负载量，或者，当前负载率低于第二负载量，则优先选择第三子模式作为所述目标读取模式，否则随机或交替选择所述第一子模式或第二子模式作为所述目标读取模式。所述第二负载率低于所述第一负载率；所述第二负载量低于所述第二负载量。

[0126] 再例如，若确定选择所述第一模式为目标读取模式，还会根据所述当前所需的读取速率从第一子模式、第二子模式及第三子模式中选择一种作为所述目标读取模式。若当前所需的读取速率对应于低速模式即可，则优先选择第三子模式，若当前所需的读取速率位于低速模式和高速模式之间，则优先选择第一子模式或第二子模式作为所述目标读取模式。

[0127] 在一些实施例中，若选择第一子模式或第二子模式作为目标读取模式时，则还根据历史时刻的目标读取模式，选择当前时刻的目标读取模式。例如，前一个读取周期的目标

Micron Ex. 1002, p. 247
Micron v. YMTC
IPR2024-00793

读取模式，或者，前一次选择的目标读取模式，选择与前一个读取周期的目标读取模式或者前一次选择的目标读取模式，所对应的目标读取模式不同的模式为当前的目标读取模式。例如，前一个读取周期或前一次选择的目标读取模式为第一子模式，则本次可以选择第二子模式为所述目标读取模式；则通过轮询或交替选择第一子模式和第二子模式，可以同时减少PHCI及NHCI导致的读取干扰。

[0128] 总之，在本实施例中，从第一模式和第二模式选择目标读取模式，可以根据闪存器的当前状况参数来确定，从而选择出符合存储设备当前状况的目标读取模式。

[0129] 如图5所示，本实施例提供一种闪存器读取装置，包括：

[0130] 第一施加模块110，用于在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压；

[0131] 第二施加模块120，用于在所述读取周期的读取阶段，向所述闪存器选择的字线施加读取数据的第二电压。

[0132] 在一些实施例中，所述第一施加模块110和所述第二施加模块120可为程序模块，所述程序模块被处理器执行后，能够实现向闪存器选择的字线施加读取数据的第一电压；该第一电压可以导通连接在该选择的字线上的存储单元，从而释放掉因为HCI等方式在存储单元内沟道内积累的干扰电荷；从而减少数据读取干扰。

[0133] 在还有一些实施例中观，所述第一施加模块110和第二施加模块120可为软硬结合模块，所述软硬结合模块可为各种可编程电路；所述可编程电路可为复杂可编程阵列或现场可编程阵列。

[0134] 在另外一些实施例中，所述第一施加模块110和所述第二施加模块120可为纯硬件模块，例如，专用集成电路。

[0135] 在一些实施例中，所述第一施加模块110，具体用于执行以下至少之一：

[0136] 在位于所述读取阶段的第一干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一子电压；

[0137] 在位于所述读取阶段之后的第二干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第二子电压。

[0138] 在一些实施例中所述第一施加模块110，具体用于执行以下至少之一：

[0139] 在所述第一干扰抑制阶段，通过升压使得施加在选择的字线上的电压达到所述第一子电压；在维持所述第一子电压的时长达到第一时长之后，通过降压使得施加在选择的字线上的电压下降到所述第二电压，以进入所述读取阶段；

[0140] 通过升压使得施加在选择的字线上的所述第二电压上升到第二子电压，以从所述读取阶段进入所述第二干扰抑制阶段，并维持所述第二子电压达到第二时长后，通过降压进行电压恢复。

[0141] 在一些实施例中所述第二电压小于所述第一电压。

[0142] 在一些实施例中一个所述干扰抑制阶段的时长与一个所述读取阶段的时长比值为：1：N；N为大于1。

[0143] 在一些实施例中，所述时长比值的取值区间为：1.5至6。

[0144] 在一些实施例中，所述装置还包括：

[0145] 选择模块，用于从第一模式和第二模式中选择目标读取模式；

Micron Ex. 1002, p. 248
Micron v. YMTC
IPR2024-00793

[0146] 所述第一施加模块110，具体用于若所述目标读取模式为所述第一模式，在读取周期的干扰抑制阶段，向闪存器选择的字线施加减少读取干扰的第一电压。

[0147] 在一些实施例中，所述选择模块，具体用于根据所述存储器的状况参数，从所述第一模式和所述第二模式中选择目标读取模式。

[0148] 在一些实施例中，所述选择模块，具体用于执行以下至少之一：

[0149] 根据所述闪存器的当前读取负载状况，从所述第一模式和所述第二模式中选择目标读取模式；

[0150] 根据读取的存储页或存储块的读取次数，从所述第一模式和所述第二模式中选择目标读取模式；

[0151] 根据读取数据的读取速率要求，从所述第一模式和所述第二模式中选择目标读取模式。

[0152] 本实施例还提供一种存储设备，包括：

[0153] 闪存器，

[0154] 控制器，与所述存储器连接，用于通过计算机可执行指令的执行，通过前述任意技术方案提供的闪存器的数据读取方法从所述闪存器上读取数据，例如，可执行图1、图2及图4所示方法的一种或多种。

[0155] 该闪存器可为2D闪存器，也可以为3D闪存器。

[0156] 在本实施例中，所述控制器可为各种类型的具有信息或信号处理功能的器件，例如，中央处理器、微处理器、数字信号处理器、可编程阵列、专用集成电路等。

[0157] 在一些实施例中，所述存储设备还包括：驱动模组，所述控制器通过所述驱动电路与所述闪存器连接。所述驱动模组，用于提供读取所述闪存器上数据的电压。所述驱动模组可包括：时钟电路，用于提供时钟信号；变压电路，将所述时钟信号提供的时钟信号的电压变压到所述第一电压或所述第二电压。

[0158] 本实施例还提供一种计算机存储介质，所述计算机存储介质存储有计算机可执行指令；所述计算机可执行指令被执行后，能够实现前述一个或多个技术方案提供的闪存器的数据读取方法，例如，可以执行如图1、图2及图4所示方法中的一种或多种。

[0159] 所述计算机存储介质可为各种类型的计算机存储介质，可选为非瞬间存储介质。

[0160] 以下结合上述任意实施例提供几个具体示例：

[0161] 闪存器的存储阵列的字线连接在存储单元的栅极；在编程阶段，存储单元字线上施加的电压不同，则注入到存储单元的载流子的数目是不同的，则存储单元进入到不同的存储状态，相当于写入了不同的数据。一般存储单元可具有二种存储状态，一种是写入了数据“0”的状态、一种是未写入数据的状态，未写入数据的状态，表示该存储单元记录的数据为“1”。

[0162] 在一些实施例中，所述存储器的数据写入是以页为单位为单位的。在数据写入或读取时，都是逐行逐列的处理的。

[0163] 在执行读操作时，根据访问地址，确定出访问地址所对应的字线，这些字线在本实施例中称之为：选择的字线；剩余的字线为未选择的字线。

[0164] 导通电压(Vpass)会施加到未选择的字线上，确保连接在同一个位线上的多个存储单元，能够允许位线电压传导到需要读取数据的存储单元上。

Micron Ex. 1002, p. 249
Micron v. YMTC
IPR2024-00793

[0165] 在3D闪存器中，存储阵列是3D的，存储阵列有多层堆叠形成的。由于读取过程中沟道升压效应，未被选中的字线所连接的存储单元(Unsel_TSG所连接的存储单元)上被选择的字线所连接的存储单元对其上方近未被选择字线连接的存储单元会产生热载流子注入效应；或者，由于读取过程结束后沟道降压效应，未被选中的字线所连接的存储单元(Unsel_TSG所连接的存储单元)上未被选择的字线连接的存储单元对被选择的字线所连接存储单元产生热载流子注入效应，而注入的热载流子会影响其相邻的存储单元记忆的数据的准确度和读取准确度。

[0166] 图7A所示为PHCI的形成示意图，在进行数据读取时，由于当前选择的存储单元在读取电压的作用下可能不会处于导通状态，进而可能使得当前选择的存储单元上一层存储单元的沟道产生正向电势，该正向电势，会造成对上一层存储单元的沟道内的热载流子注入效应即PHCI。图7B所示为NHCI的形成示意图；在读取电压下降的过程中，由于读取电压小于上方存储单元的导通电压(Vpass)使得当前选中的存储单元在降压过程中很快就处于关断状态，造成上方的存储单元的沟道处于浮空的状态，进而使得当前选择的存储单元上一层存储单元的沟通产生负向电势，该负向电势，会造成对上一层存储单元的沟道内的热载流子注入效应即NHCI。

[0167] 图7C所示为一个存储单元经过多次读取之后，其开启电压在电压轴上的浮动。此处的开启电压可为导通存储单元的电压。

[0168] 本示例提供过一种可抑制读取干扰的数据读取方法，包括：

[0169] 在读取周期内，在读取阶段之前设置读取准备阶段，在读取阶段之后设置读取完成阶段；具体可以根据应用环境，在读取周期包含所述读取阶段之外，单独增加读取准备阶段、单独增加读取完成阶段、同时增加读取准备阶段和读取完成阶段，或者，读取准备阶段和读取完成阶段都不增加。

[0170] 此处的读取准备阶段相当于前述实施例的第一干扰抑制阶段；所述读取完成阶段相当于实施例的第二干扰抑制阶段。

[0171] 图6A和图6B为同一个存储阵列，在读取周期未添加有读取预备阶段时，出现了未选择字线的电压升高的现象，不再是0V。在读取周期内添加了有读取预备阶段之后，可以将累积的沟道电势卸掉，从而可以如图6B所示，未选择的字线上的电压均为0V。

[0172] 如图8所示，在整个读取周期内，顶层栅极电压(TSG)施加导通电压Vtsg，从而TSG所对应的晶体管导通，允许位线电压通过。底层栅极电压(BSG)施加Vtsg，使得BSG对应的晶体管导通，该晶体管接地，如此可以形成导通回路。

[0173] 在读取准备阶段，在Sel_TSG(4)上施加的电压为Vtsg(9)，在未被选择字线Unsel_TSG(5)上施加的电压为0V；在未被选择字线Unsel_WL(7)上施加的电压为Vpass；其中，Unsel_WL表示未选择的字线。在选择的字线Sel_WL(6)上施加高电压Vprepare(10)，在BSG(8)上施加电压Vbsg；且BSG(8)连接到地；该Vprepare(10)的压值可大致等于Vpass；如此，Sel_WL(6)所作用的存储单元导通，可以将不稳定的载流子释放到地(GND)，同时还可以抑制读取电压升压阶段的PHCI。

[0174] 在读取阶段，施加在Sel_WL(6)上的电压从Vprepare(10)切换到Vread(13)，用于Sel_WL(6)所连接存储单元的数据读取。

[0175] 在读取完成阶段，在Sel_TSG(4)上施加Vtsg(9)，在未被选择字线Unsel_TSG(5)上

Micron Ex. 1002, p. 250
Micron v. YMTC
IPR2024-00793

施加的电压为0V；在未被选择字线Unsel_WL(7)上施加的电压为Vpass；在选择的字线Sel_WL(6)上施加高电压Vwrap-up(14)，在BSG(8)上施加电压Vbsg；且BSG(8)连接到地；Vwrap-up(14)高于Vread，导通Sel_WL(6)所连接的存储单元，从而使得存储单元通过BSG(8)，释放读取阶段产生的不稳定的载流子，并且抑制在读取电压下降阶段的NHCI。

[0176] 总之，通过读取预备阶段和读取完成阶段的引入，可以抑制Sel_WL(6)所连接存储单元内的沟道电势对unSel_WL(7)所连接的读取干扰就得到了抑制。

[0177] 在本申请所提供的几个实施例中，应该理解到，所揭露的设备和方法，可以通过其它的方式实现。以上所描述的设备实施例仅仅是示意性的，例如，所述单元的划分，仅仅为一种逻辑功能划分，实际实现时可以有另外的划分方式，如：多个单元或组件可以结合，或可以集成到另一个系统，或一些特征可以忽略，或不执行。另外，所显示或讨论的各组成部分相互之间的耦合、或直接耦合、或通信连接可以是通过一些接口，设备或单元的间接耦合或通信连接，可以是电性的、机械的或其它形式的。

[0178] 上述作为分离部件说明的单元可以是、或也可以不是物理上分开的，作为单元显示的部件可以是、或也可以不是物理单元，即可以位于一个地方，也可以分布到多个网络单元上；可以根据实际的需要选择其中的部分或全部单元来实现本实施例方案的目的。

[0179] 另外，在本发明各实施例中的各功能单元可以全部集成在一个处理模块中，也可以是各单元分别单独作为一个单元，也可以两个或两个以上单元集成在一个单元中；上述集成的单元既可以采用硬件的形式实现，也可以采用硬件加软件功能单元的形式实现。

[0180] 本领域普通技术人员可以理解：实现上述方法实施例的全部或部分步骤可以通过程序指令相关的硬件来完成，前述的程序可以存储于一计算机可读取存储介质中，该程序在执行时，执行包括上述方法实施例的步骤；而前述的存储介质包括：移动存储设备、只读存储器(Read-Only Memory，ROM)、随机存取存储器(Random Access Memory，RAM)、磁碟或者光盘等各种可以存储程序代码的介质。

[0181] 以上所述，仅为本发明的具体实施方式，但本发明的保护范围并不局限于此，任何熟悉本技术领域的技术人员在本发明揭露的技术范围内，可轻易想到变化或替换，都应涵盖在本发明的保护范围之内。因此，本发明的保护范围应以所述权利要求的保护范围为准。

Micron Ex. 1002, p. 251
Micron v. YMTC
IPR2024-00793

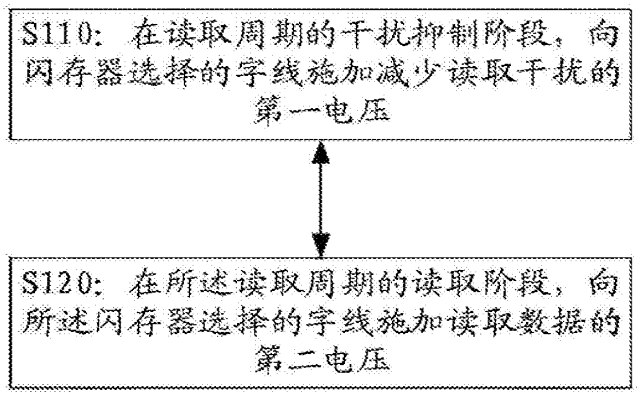


图1

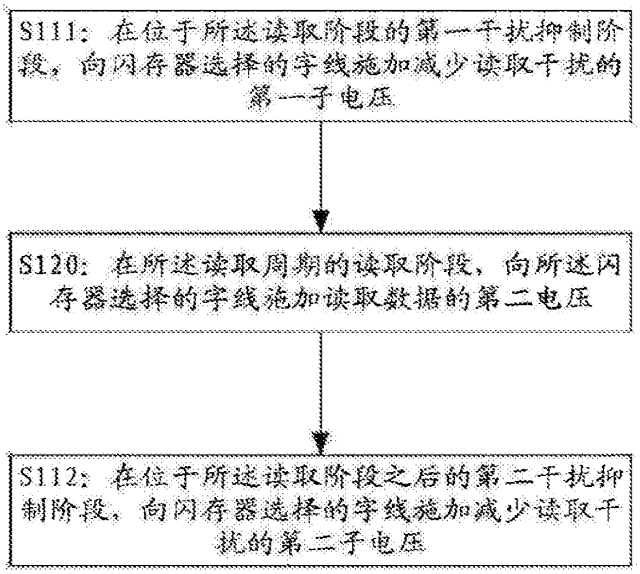


图2

Micron Ex. 1002, p. 252
Micron v. YMTC
IPR2024-00793

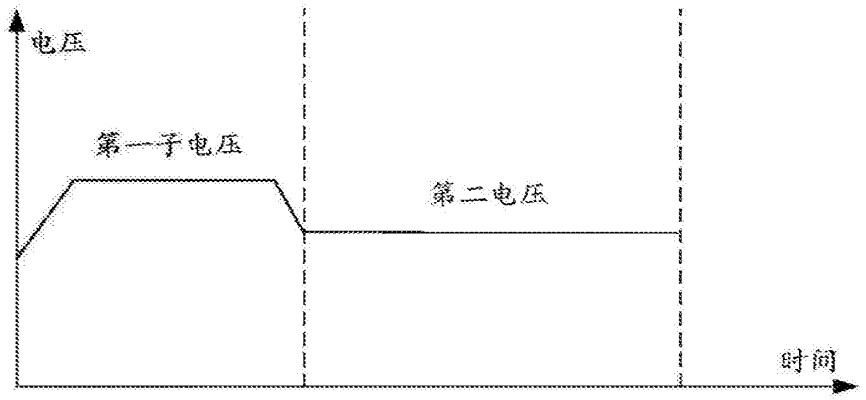


图3A

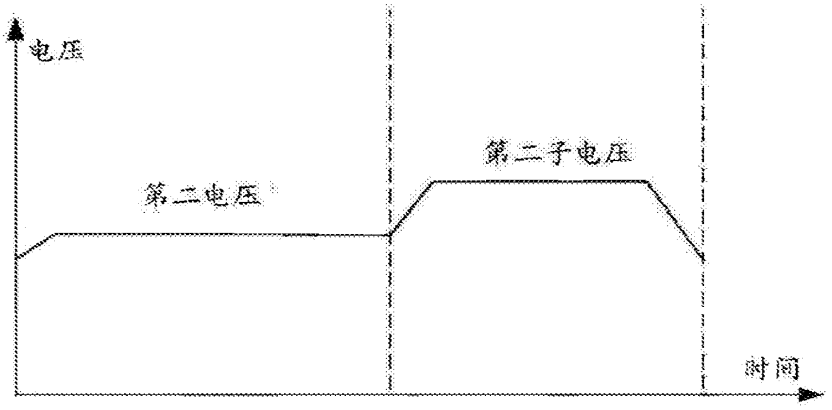


图3B

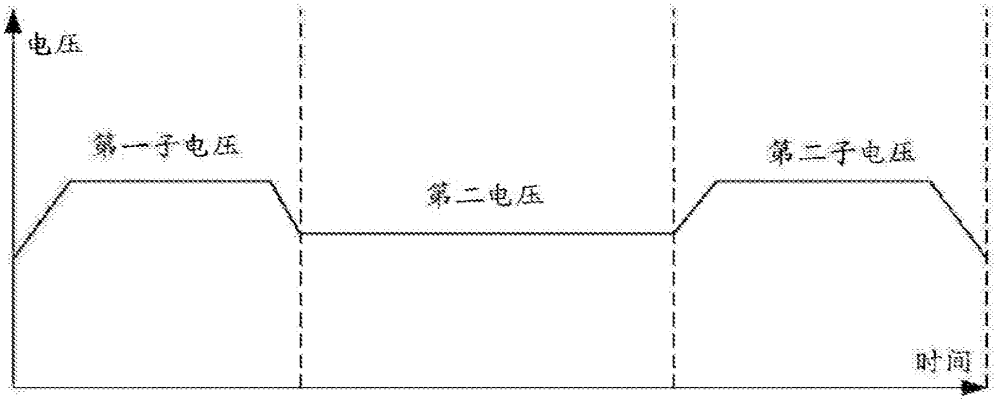


图3C

Micron Ex. 1002, p. 253
Micron v. YMTC
IPR2024-00793

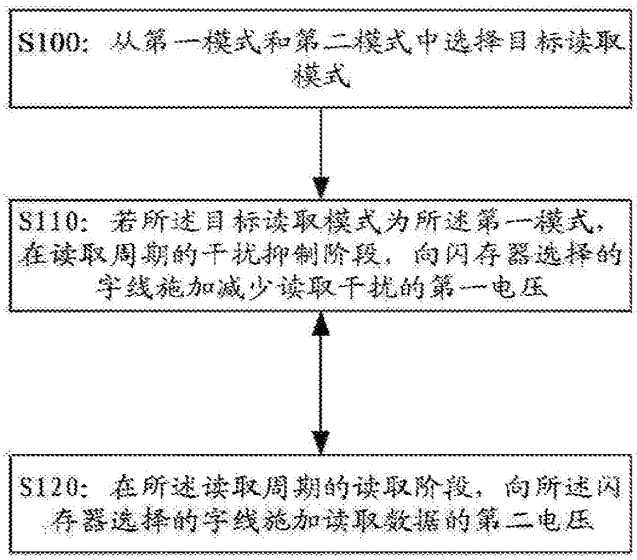


图4

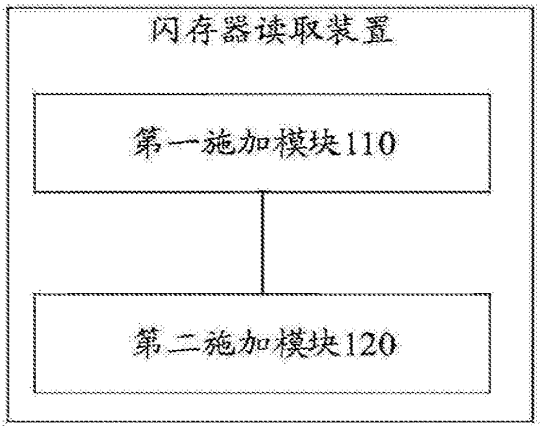


图5

Micron Ex. 1002, p. 254
Micron v. YMTC
IPR2024-00793

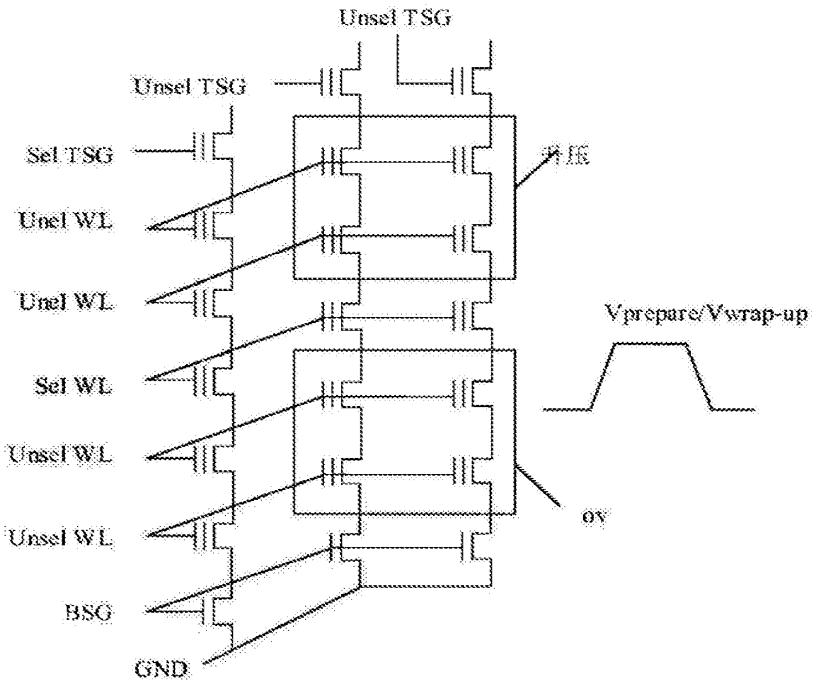


图6A

Micron Ex. 1002, p. 255
Micron v. YMTC
IPR2024-00793

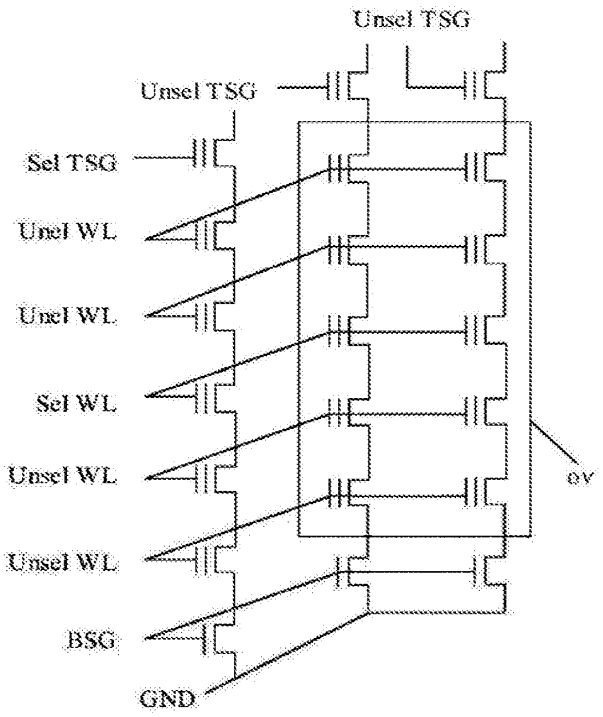


图6B

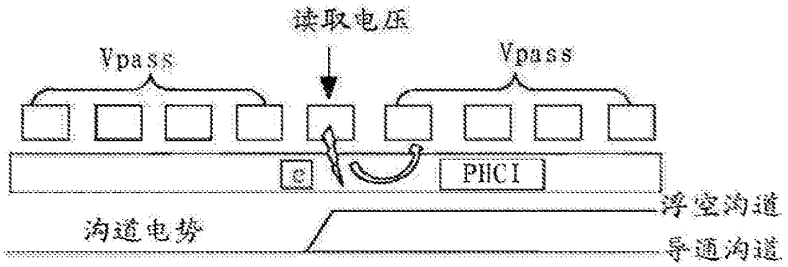


图7A

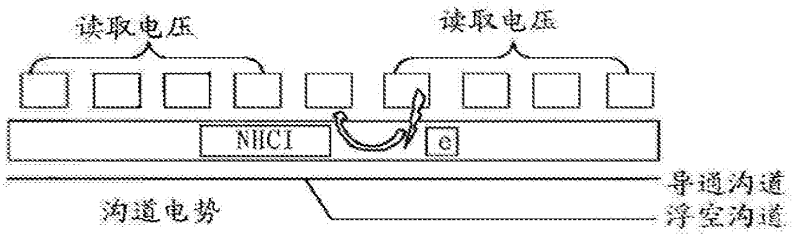


图7B

Micron Ex. 1002, p. 256
Micron v. YMTC
IPR2024-00793

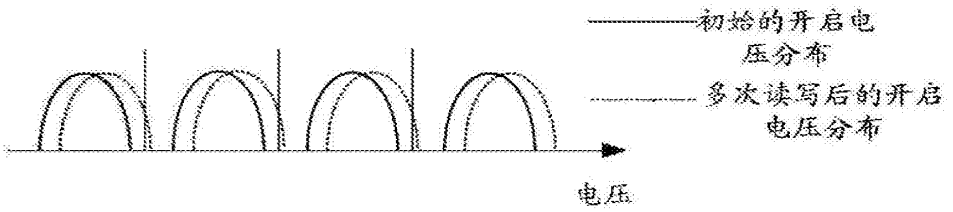


图7C

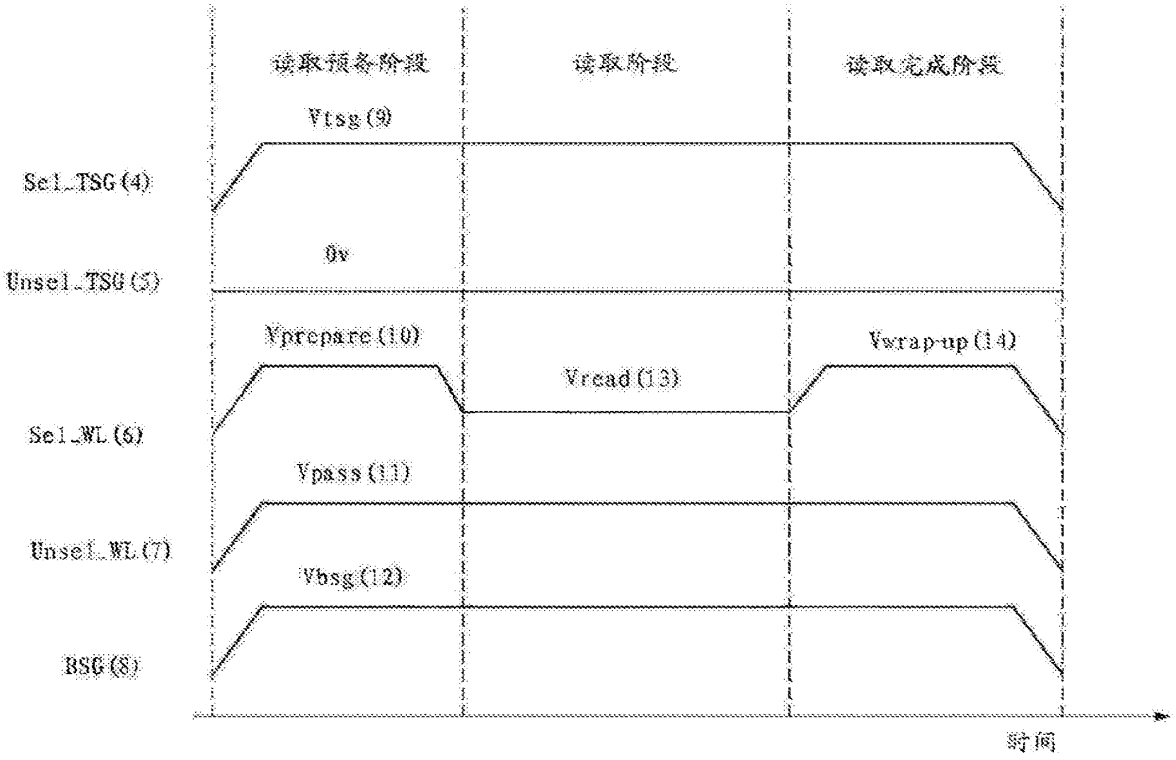


图8

Micron Ex. 1002, p. 257
Micron v. YMTC
IPR2024-00793

Electronic Acknowledgement Receipt

EFS ID:	45554453
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International Application Number:	
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Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Min Yang/Jon Baitlon
Filer Authorized By:	Min Yang
Attorney Docket Number:	4123.0850002
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Filing Date:	19-MAY-2021
Time Stamp:	16:33:34
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	sIDS1-Cover-Letter-IDS-4123-0850002.pdf	229209 9e54f95ba93e1d728211a1abd27e51d877a ddbe7	no	1

Warnings:

Information:					
2	Transmittal Letter	sIDS1-Pleading-4123-0850002.pdf	131793 33efe1e8476e2d1d5c061c7e3114b9408b161f8a	no	7
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	sIDS1-SB08a-4123-0850002.pdf	153917 58e1393c0b25e3ed12bf37acb87c14be4021860e	no	1
Warnings:					
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This is not an USPTO supplied IDS fillable form					
4	Foreign Reference	FP1_CN101866694A.pdf	484710 7e31f08bb0fddd26948d1b171fcc8ade15f174d7	no	20
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7	Foreign Reference	FP4_CN109065091A.pdf	352539 53d100325fabe9b47240f993a8f10469b635d380	no	10
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8	Foreign Reference	FP5_CN109584938A.pdf	677542 d20dbf43f3590e9242e86db047c3e4a81dd19dc4	no	22
Warnings:					
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Total Files Size (in bytes):	5335146

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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April 25, 2022

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8686
Art Unit: To Be Assigned
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 17/324,877; Filed: May 19, 2021
For: **Method For Reading Three-Dimensional Flash Memory**
First Named Inventor: Zilong CHEN
Our Ref: 4123.0850002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. First Supplemental Information Disclosure Statement;
2. Form PTO/SB/08a (1 sheet) listing 10 documents (**US1-US5**) and (**FP1-FP5**); and
3. Copies of cited documents (**FP1-FP5**).

The above-listed items are filed electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

M-Y/jcb
Enclosures

18352428_1.DOCX

Micron Ex. 1002, p. 261
Micron v. YMTC
IPR2024-00793

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Zilong CHEN	Confirmation No.: 8686
Applicant: YANGTZE MEMORY TECHNOLOGIES CO., LTD.	Art Unit: *To Be Assigned*
Application No.: 17/324,877	Examiner: *To Be Assigned*
Filing Date: May 19, 2021	Atty. Docket: 4123.0850002

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

First Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Form PTO/SB/08a or its equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Form based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart[1] foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office

[1] The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

Micron Ex. 1002, p. 263
Micron v. YMTC
IPR2024-00793

Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. The required fee is provided through online credit card payment authorization in the amount of $260.00 in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of $260.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

Micron Ex. 1002, p. 264
Micron v. YMTC
IPR2024-00793

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

Micron Ex. 1002, p. 265
Micron v. YMTC
IPR2024-00793

☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

☒ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **FP4** (CN 109065091 A) appears to describe a "reading method of 3D NAND flash memory," as noted in the attached English-language translation of the abstract.

Document **FP5** (CN 109584938 A) appears to describe a "data reading method and device of flash memory, storage equipment and storage medium," as noted in the attached English-language translation of the abstract.

Document **US2** (8,031,530 B2) is submitted herewith as the English-language counterpart of document **FP1** (CN 101866694 A).

Document **US3** (9,093,369 B2) is submitted herewith as the English-language counterpart of document **FP2** (CN 103490008 A).

Document **US5** (10,008,269 B2) is submitted herewith as the English-language counterpart of document **FP3** (CN 107170746 A).

☒ 8. Copies of documents **FP1-FP5** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patents and patent application publication cited as documents **US1-US5** on the attached IDS Form are submitted.

Micron Ex. 1002, p. 266
Micron v. YMTC
IPR2024-00793

☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____ in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

☐ 11. Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No._____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

Micron Ex. 1002, p. 267
Micron v. YMTC
IPR2024-00793

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Form, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

Date: April 25, 2022

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18352418.1

Micron Ex. 1002, p. 268
Micron v. YMTC
IPR2024-00793

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/324,877	05/19/2021	Zilong CHEN	4123.0850002	8686

26111 7590 07/26/2022

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER
LE, THONG QUOC

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
07/26/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

Micron Ex. 1002, p. 269
Micron v. YMTC
IPR2024-00793

Office Action Summary	Application No. 17/324,877	Applicant(s) CHEN et al.	
	Examiner THONG Q LE	Art Unit 2827	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 04/25/2022; 05/19/2021.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Micron Ex. 1002, p. 270
Micron v. YMTC
IPR2024-00793

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

1. Claims 1-20 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 04/25/2022.

Information Disclosure Statement (IDS) filed on 05/19/2021.

3. Information disclosed and list on PTO 1449 was considered.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.

Claim(s) 1-20 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Yang et al. (Pub. U.S. 2019/0371394).

Regarding claims 1,4,16, Yang et al. disclose a three-dimensional (3D) memory device (Figure 7), comprising:

a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers (Figure 8), wherein:

each memory string comprises a plurality of memory cells (Figure 12A, [0147])); and

each memory cell is addressable through a word line and a bit line (Figure 8, WL, BL); and

a circuit (Figure 1, 110) f the memory array configured to conduct, on a target memory cell, a read- verification operation (Figures 11C-11D) for removing fast charges during a first time period, wherein the circuit is configured to:

apply, on an unselected top select gate (Figure 15, Vsg) of an unselected memory string, a prepare voltage during the first time period and an off voltage during a second time period (Figure 15, 1531) ;

apply, on a selected word line (Figure 15, 1501) associated with the target memory cell, the off voltage (Figure 15, 0V) during the first time period and a read voltage during the second time period (Figure 11E, 1141); and

apply, on an unselected word line (Figure 15, 1511), a pass voltage (Figure 15, 1513) during the first time period and the second time period.

Regarding claims 2-3,17, Yang et al. disclose wherein the circuit is further configured to: electrically connect a selected memory string containing the target

memory cell to the bit line and an array common source by applying a top select gate voltage (Figure 3, SGD, 446) on a selected top select gate and applying a lower select gate voltage on a lower select gate (Figure 3, 445) during the first time period and the second time period ([0101-0102]).

Regarding claim 18, Yang et al. disclose wherein to remove the fast charges of the target memory cell, the circuit is further configured to: apply the top select gate voltage on the selected top select gate and the lower select gate voltage on the lower select gate before applying the pass voltage on the unselected word line ([0100-0102]).

Regarding claim 19, Yang et al. disclose wherein each memory string comprises: a channel hole ([0004]); a core filling film in a center of the channel hole; a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and a channel layer sandwiched between the memory film and the core filling film ([0116-0119]).

Regarding claims 12-13, 20, Yang et al. disclose wherein the circuit is further configured to remove the fast charges from a portion of the storage layer associated with the target memory cell ([0044],[0050]).

Regarding claim 5, Yang et al. disclose further comprising: measuring a threshold voltage of the target memory cell during the second time period ([0131]).

Regarding claim 6, Yang et al. disclose wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell ([0144]-0145]).

Regarding claim 7, Yang et al. disclose wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell ([0144]).

Regarding claim 8, Yang et al. disclose wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is lower than a threshold voltage of an unselected memory cell ([0144-0145]).

Regarding claim 9, Yang et al. disclose wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V [0137]).

Regarding claim 10, Yang et al. disclose wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V ([0144]).

Regarding claim 11, Yang et al. disclose wherein applying the off voltage comprises applying a voltage about 0V (Figure 16, 0V,[0192]).

Regarding claim 14, Yang et al. disclose wherein the removing the fast charges comprises: removing the fast charges from the target memory cell to a neighboring unselected memory cell ([0193]).

Regarding claim 15, Yang et al. disclose wherein conducting the read-verification operation comprises conducting a failed bit count in parallel ([0056],[0077]).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THONG QUOC LE whose telephone number is (571)272-1783. The examiner can normally be reached 7:30AM-5:30PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/THONG Q LE/

Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 17/324,877	Applicant(s)/Patent Under Reexamination CHEN et al.	
	Examiner THONG Q LE	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20190371394-A1	12-2019	Yang; Xiang	G06F11/1072	1/1
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Micron Ex. 1002, p. 276
Micron v. YMTC
IPR2024-00793

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	**Art Unit**
	THONG Q LE	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/19/2022								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								

Micron Ex. 1002, p. 277
Micron v. YMTC
IPR2024-00793

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	Art Unit
	THONG Q LE	2827

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483;G11C16/10;G11C16/08;G11C11/5628;G11C11/5671;G11C16/3427;G11C16/24;G11C16/26;G11C11/5642;G11C16/0408;G11C2211/5641;G11C16/3459;G11C2211/5621;G11C16/30;G11C16/3418;G11C16/14;G11C16/16;G11C16/32;G11C16/3436;G11C16/3445;G11C11/5635;G11C16/0466;G11C16/349;G11C2211/563;G11C7/12;G11C11/4063;G11C16/12;G11C16/28;G11C16/34;G11C16/3454;G11C16/3481;G11C2211/562;G11C2211/5625;G11C2211/5642;G11C2211/5648;G11C5/145;G11C7/14;G11C7/222;G11C8/08;H01L27/11582;H01L27/11556;H01L27/1157;H01L27/11548;H01L27/11595;H01L27/11524;H01L29/7884;H01L27/0255;H01L27/115;H01L27/11565 365/185.17;365/185.22;365/185.29;365/185.01;365/185.03;365/185.05;365/185.18;365/185.19	07/19/2022	TL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
	365/185.17;365/185.22;365/185.29;365/185.01;365/185.03;365/185.05;365/185.18;365/185.19	07/19/2022	TL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E searched	07/19/2022	TL
Inventor searched	07/19/2022	TL

Micron Ex. 1002, p. 278
Micron v. YMTC
IPR2024-00793

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	Art Unit
	THONG Q LE	2827

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	Interference searched	07/19/2022	TL

Micron Ex. 1002, p. 279
Micron v. YMTC
IPR2024-00793

Bibliographic Data

Application No: 17/324,877

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /THONG Q LE/ (Examiner's Signature) | (Initials)

Title: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
05/19/2021	365	2827	4123.0850002
RULE			

APPLICANTS

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

INVENTORS

Zilong CHEN, Wuhan, CHINA

Xiang FU, Wuhan, CHINA

CONTINUING DATA

This application is a CON of 16729838 12/30/2019 PAT 11043279

16729838 is a CON of PCT/CN2019/112728 10/23/2019

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

05/26/2021

STATE OR COUNTRY

CHINA

ADDRESS

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005
UNITED STATES

FILING FEE RECEIVED

$1,820

PTO/SB/08a (07-09)
Approved for use through 11/30/2020. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	17/324,877
Filing Date	May 19, 2021
First Named Inventor	Zilong CHEN
Art Unit	To Be Assigned
Examiner Name	~~To Be Assigned~~ Thong Le
Attorney Docket Number	4123.0850002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	US- 2010/0046300 A1	02-25-2010	Sarin et al.	
	US2	US- 8,031,530 B2	10-04-2011	Joo	
	US3	US- 9,093,369 B2	07-28-2015	Shin et al.	
	US4	US- 9,666,296 B1	05-30-2017	Maejima	
	US5	US- 10,008,269 B2	06-26-2018	Maejima	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	FP1	CN 101866694 A	10-20-2010	HYNIX SEMICONDUCTOR INC		
	FP2	CN 103490008 A	01-01-2014	SAMSUNG ELECTRONICS CO LT		
	FP3	CN 107170746 A	09-15-2017	TOSHIBA KK		
	FP4	CN 109065091 A	12-21-2018	YANGTZE MEMORY TECH CO LT		✓
	FP5	CN 109584938 A	04-05-2019	YANGTZE MEMORY TECH CO LT		✓

Examiner Signature	/THONG Q LE/	Date Considered	07/18/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/08a (07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Zilong CHEN
Art Unit	To Be Assigned
Examiner Name	~~To Be Assigned~~ Thong Le
Attorney Docket Number	4123.0850002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	US- 2012/0275223 A1	11-01-2012	Baek	
	US2	US- 2013/0128667 A1	05-23-2013	Lee et al.	
	US3	US- 2013/0339603 A1	12-19-2013	Zhu et al.	
	US4	US- 2015/0179269 A1	06-25-2015	Lee	
	US5	US- 2019/0333590 A1	10-31-2019	Lee	
	US6	US- 2021/0125674 A1	04-29-2021	Chen et al.	
	US7	US- 9,607,707 B1	03-28-2017	Pang et al.	
	US8	US- 9,704,587 B1	07-11-2017	Park	
	US9	US- 10,121,554 B2	11-06-2018	Harari	
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	FP1	CN 102760490 A	10-31-2012	SK HYNIX INC		
	FP2	CN 108140415 A	06-08-2018	SUNRISE MEMORY CORP		
	FP3	CN 109390012 A	02-26-2019	GIGADEVICE SEMICONDUCTOR		✓
	FP4	CN 109979515 A	07-05-2019	YANGTZE MEMORY TECH CO LT		✓

Examiner Signature	/THONG Q LE/	Date Considered	07/18/2022

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PTO/SB/08b (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Zilong CHEN
Art Unit	To Be Assigned
Examiner Name	~~To Be Assigned~~ Thong Le
Attorney Docket Number	4123.0850002

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2019/112728, mailed July 22, 2020; 6 pages.	

Examiner Signature	/THONG Q LE/	Date Considered	07/18/2022

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	1666056	memory AND three-dimensional	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 09:47 AM
L2	1080	L1 AND (unselect$3 OR deselect$3) WITH select$3 ADJ select$3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:11 AM
L3	229	L2 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:13 AM
L4	140	L2 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:14 AM
L5	75	L2 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1 AND select$3 ADJ word ADJ line$1 AND target	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:14 AM
L6	32	L2 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1 AND select$3 ADJ word ADJ line$1 AND target AND read ADJ voltage AND pass ADJ voltage	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:15 AM
L7	28	L6 AND period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD,	OR	ON	ON	2022/07/18 11:52 AM

Micron Ex. 1002, p. 284
Micron v. YMTC
IPR2024-00793

			DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L8	28	L6 AND period AND voltage	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 11:52 AM
L9	4	L8 AND first ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:49 AM
L10	3	L8 AND first ADJ period AND second ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:50 AM
L11	0	L8 AND first ADJ tiome ADJ period AND second ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:50 AM
L12	3	L10	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:50 AM
L13	2841561	L8 ans read AND verify	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:51 AM
L14	28	L8 AND read AND verify	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2022/07/19 10:52 AM

Micron Ex. 1002, p. 285
Micron v. YMTC
IPR2024-00793

			AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L15	0	L14 AND read-verifycation	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:52 AM
L16	0	L14 AND read-verification	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:52 AM
L17	9	L14 AND read WITH verification	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:53 AM
L18	28	L14	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:53 AM
L19	32	L6	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 11:31 AM
L20	36	(Artificial Intelligence) More Like: US-20190371394-A1 Text: (CN-111406289-A OR WO-2019236153-A1 OR US-10636487-B2 OR US-11081180-B2 OR US-20200243138-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO,	OR	ON	ON	2022/07/19 04:54 PM

Micron Ex. 1002, p. 286
Micron v. YMTC
IPR2024-00793

		A1 OR DE-112019000157-T5 OR US-10153051-B1 OR US-20190318792-A1 OR US-10482984-B2 OR CN-111406287-A OR WO-2019236152-A1 OR US-10438671-B1 OR US-10726922-B2 OR US-20190371406-A1 OR EP-3455857-B1 OR WO-2019199371-A1 OR US-20190311772-A1 OR US-10446244-B1 OR DE-112019000164-T5 OR US-10269435-B1).did.	MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L21	28	L18	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 04:54 PM
L22	485980	((G11C16/0483 OR G11C16/10 OR G11C16/08 OR G11C11/5628 OR G11C11/5671 OR G11C16/3427 OR G11C16/24 OR G11C16/26 OR G11C11/5642 OR G11C16/0408 OR G11C2211/5641 OR G11C16/3459 OR G11C2211/5621 OR G11C16/30 OR G11C16/3418 OR G11C16/14 OR G11C16/16 OR G11C16/32 OR G11C16/3436 OR G11C16/3445 OR G11C11/5635 OR G11C16/0466 OR G11C16/349 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 04:59 PM

Micron Ex. 1002, p. 287
Micron v. YMTC
IPR2024-00793

		G11C2211/563 OR G11C7/12 OR G11C11/4063 OR G11C16/12 OR G11C16/28 OR G11C16/34 OR G11C16/3454 OR G11C16/3481 OR G11C2211/562 OR G11C2211/5625 OR G11C2211/5642 OR G11C2211/5648 OR G11C5/145 OR G11C7/14 OR G11C7/222 OR G11C8/08 OR H01L27/11582 OR H01L27/11556 OR H01L27/1157 OR H01L27/11548 OR H01L27/11595 OR H01L27/11524 OR H01L29/7884 OR H01L27/0255 OR H01L27/115 OR H01L27/11565 OR H01L27/2454 OR H01L27/249 OR H01L45/04 OR H01L45/06 OR H01L45/10 OR H01L45/145 OR H01L45/146 OR H01L27/11529 OR G06F11/1012 OR G06F11/1072 OR G06F11/186 OR G06F12/0246 OR G06F12/0866).cpc. OR (365/185.17 OR 365/185.22 OR 365/185.29 OR 365/185.01 OR 365/185.03 OR 365/185.05 OR 365/185.18 OR 365/185.19).ccls.)					
L23	1120	L22 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1 AND select$3 ADJ word ADJ line$1 AND target AND read ADJ voltage AND pass ADJ voltage	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 04:59 PM
L24	0	L23 AND first ADJ tiome ADJ period AND	(US-PGPUB; USPAT; USOCR; FIT (AP, AT,	OR	ON	ON	2022/07/19 05:00 PM

Micron Ex. 1002, p. 288
Micron v. YMTC
IPR2024-00793

		second ADJ period	AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L25	11	L23 AND first ADJ time ADJ period AND second ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 05:00 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Micron Ex. 1002, p. 289
Micron v. YMTC
IPR2024-00793

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO				*Complete if Known*	
SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	17/324,877
				Filing Date or 371(c) Date	May 19, 2021
				First Named Inventor	Zilong CHEN
				Art Unit	2827
				Examiner Name	LE, THONG QUOC
Sheet	1	of	1	Attorney Docket Number	4123.0850002

U.S. PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Document Number Number-Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US 1	2019/0294367 A1	09-26-2019	Takada et al.	
	US 2	2017/0076813 A1	03-16-2017	Kato et al.	

FOREIGN PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

18962212.1

Examiner Signature		Date Considered	

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UNITED STATES
PATENT AND TRADEMARK OFFICE

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Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/324,877	**09/02/2022 12:26:43 PM ET**	**4123.0850002**

Title of Invention

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8686	FILED BY	Julia Vang
PATENT CENTER #	60934473	FILING DATE	05/19/2021
CUSTOMER #	26111	FIRST NAMED INVENTOR	Zilong CHEN
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Min Yang

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2022-09-02-Cover-Letter-IDS-4123-0850002.pdf	2	Miscellaneous Incoming Letter	308 KB
2022-09-02-sIDS2-Pleading-4123.0850002.pdf	6	Transmittal Letter	169 KB
2022-09-02-sIDS2-SB08a-4123-0850002.pdf	1	Information Disclosure Statement (IDS) Form (SB08)	138 KB

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Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2022-09-02-Cover-Letter-IDS-4123-0850002.pdf	7E10C13E3474E69AD2B49F0DE3C52B682E3063E2FC141B863683027365701 50B6C7AF2B4916558C7F7C00CAE798FAA7E965F7A5D905B4D46DFAEAC25E276F04F
2022-09-02-sIDS2-Pleading-4123.0850002.pdf	CEF1757D07CF2099841CD2F1B83CD187BB7359E210237F4F593ED7C1E754C5C91D4D2D8341A1585C18F41FB088C56A684EEB6900D4EEBC406F865FC63E8D8F9F
2022-09-02-sIDS2-SB08a-4123-0850002.pdf	77B34B467C2AA36740E3F79E6F40E0EC36452FF6392CCF6FC3655DE9260562D850A2EAF9F107BF69E37EEA5E87AD982A7751B4B6A4AAE4445FE8572B2779C246

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

MIN YANG
STUDENT ASSOCIATE
202-772-8702
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September 2, 2022

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8686
Art Unit 2827
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 17/324,877; Filed: May 19, 2021
For: **Method For Reading Three-Dimensional Flash Memory**
First Named Inventor: Zilong CHEN
Our Ref: 4123.0850002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of **$260** to cover the IDS fee;

2. Second Supplemental Information Disclosure Statement;

3. Form PTO/SB/08a (1 sheet) listing 2 documents (US1-US2);

The above-listed items are filed electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Micron Ex. 1002, p. 293
Micron v. YMTC
IPR2024-00793

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

M-Y/jcv
Enclosure(s)

Micron Ex. 1002, p. 294
Micron v. YMTC
IPR2024-00793

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Zilong CHEN	Confirmation No.: 8686
Applicant: YANGTZE MEMORY TECHNOLOGIES CO., LTD.	Art Unit: 2827
Application No.: 17/324,877	Examiner: LE, THONG QUOC
Filing Date: May 19, 2021	Atty. Docket: 4123.0850002

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

Second Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a or its equivalent and/or PTO/SB/08b or its equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98. The numbering on this Second Supplemental Information Disclosure Statement is a continuation of the numbering in Applicant's Information Disclosure Statement filed on April 25, 2022 in connection with the above-captioned application.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart[1] foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national

[1] The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

Micron Ex. 1002, p. 296
Micron v. YMTC
IPR2024-00793

stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☒ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ c. The required fee is provided through online credit card payment authorization in the amount of **$260** in payment of the fee under 37 C.F.R. § 1.17(p).

Micron Ex. 1002, p. 297
Micron v. YMTC
IPR2024-00793

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published

Micron Ex. 1002, p. 298
Micron v. YMTC
IPR2024-00793

application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

☐ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

☒ 8. In accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications cited as documents US1-US2 on the attached IDS Form are submitted.

☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____ in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

Micron Ex. 1002, p. 299
Micron v. YMTC
IPR2024-00793

☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No._____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

Date: September 2, 2022

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Micron Ex. 1002, p. 300
Micron v. YMTC
IPR2024-00793

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/324,877	09/02/2022 12:26:43 PM ET	4123.0850002

Title of Invention

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8686	FILED BY	Julia Vang
PATENT CENTER #	60934473	AUTHORIZED BY	Min Yang
CUSTOMER #	26111	FILING DATE	05/19/2021
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Zilong CHEN

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1008	E202292C29444551	Julia Vang

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
			TOTAL AMOUNT:	$260.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/324,877	05/19/2021	Zilong CHEN	4123.0850002	8686

26111 7590 10/20/2022

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER
LE, THONG QUOC

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
10/20/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

Micron Ex. 1002, p. 303
Micron v. YMTC
IPR2024-00793

Examiner-Initiated Interview Summary	Application No. 17/324,877	Applicant(s) CHEN et al.		
	Examiner THONG Q LE	Art Unit 2827	AIA (First Inventor to File) Status Yes	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
THONG Q LE	Primary Examiner	Telephonic
Min Yang	Attorney	

Date of Interview: 14 October 2022

Issues Discussed:

35 U.S.C. 102

Discussed claim 1, explaining the different between Figure 6 in application and Figure 15 in reference.

/THONG Q LE/ Primary Examiner, Art Unit 2827	

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Micron Ex. 1002, p. 304
Micron v. YMTC
IPR2024-00793

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/324,877	Filing Date 05/19/2021	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	10/20/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/RENEE D HAWKINS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor**:** Zilong CHEN	Confirmation No.: 8686
Applicant: YANGTZE MEMORY TECHNOLOGIES CO., LTD.	Art Unit: 2827
Application No.: 17/324,877	Examiner: LE, THONG QUOC
Filed: May 19, 2021	Atty. Docket: 4123.0850002

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated **July 26, 2022** ("Office Action"), Applicant submits the following Remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims, or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Status of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:

applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period;

applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and

applying, on an unselected word line, a pass voltage during the first time period and the second time period,

wherein the read-verification operation removes fast charges of the target memory cell during the first time period.

2. (Original) The method of claim 1, further comprising:

applying, on a selected top select gate of a selected memory string containing the target memory cell, a top select gate voltage during the first time period and the second time period; and

applying, on a lower select gate of the selected memory string containing the target memory cell, a lower select gate voltage during the first time period and the second time period.

3. (Original) The method of claim 2, wherein the applying the top select gate voltage comprises electrically connecting the selected memory string to a bit line; and the applying the lower select gate voltage comprises electrically connecting the selected memory string to an array common source.

4. (Original) The method of claim 2, wherein the applying the pass voltage comprises applying the pass voltage with a delay period after the selected top select gate and the lower select gate are at the top select gate voltage and the lower select gate voltage, respectively.

5. (Original) The method of claim 1, further comprising:

Micron Ex. 1002, p. 307
Micron v. YMTC
IPR2024-00793

measuring a threshold voltage of the target memory cell during the second time period.

6. (Original) The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell.

7. (Original) The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell.

8. (Original) The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is lower than a threshold voltage of an unselected memory cell.

9. (Original) The method of claim 1, wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V.

10. (Original) The method of claim 1, wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V.

11. (Original) The method of claim 1, wherein applying the off voltage comprises applying a voltage about 0V.

12. (Original) The method of claim 1, wherein the removing the fast charges comprises:
removing the fast charges from a storage layer of the target memory cell.

13. (Original) The method of claim 1, wherein the removing the fast charges comprises:
removing electrical charges from shallow traps in the storage layer of the target memory cell.

14. (Original) The method of claim 1, wherein the removing the fast charges comprises:
removing the fast charges from the target memory cell to a neighboring unselected memory cell.

Micron Ex. 1002, p. 308
Micron v. YMTC
IPR2024-00793

15. (Original) The method of claim 1, wherein conducting the read-verification operation comprises conducting a failed bit count in parallel.

16. (Original) A three-dimensional (3D) memory device, comprising:

a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein:

each memory string comprises a plurality of memory cells; and

each memory cell is addressable through a word line and a bit line; and

a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:

apply, on an unselected top select gate of an unselected memory string, a prepare voltage during the first time period and an off voltage during a second time period;

apply, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and

apply, on an unselected word line, a pass voltage during the first time period and the second time period.

17. (Original) The 3D memory device of claim 16, wherein the circuit is further configured to:

electrically connect a selected memory string containing the target memory cell to the bit line and an array common source by applying a top select gate voltage on a selected top select gate and applying a lower select gate voltage on a lower select gate during the first time period and the second time period.

18. (Original) The 3D memory device of claim 17, wherein to remove the fast charges of the target memory cell, the circuit is further configured to:

apply the top select gate voltage on the selected top select gate and the lower select gate voltage on the lower select gate before applying the pass voltage on the unselected word line.

Micron Ex. 1002, p. 309
Micron v. YMTC
IPR2024-00793

19. (Original) The 3D memory device of claim 16, wherein each memory string comprises:

a channel hole;

a core filling film in a center of the channel hole;

a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and

a channel layer sandwiched between the memory film and the core filling film.

20. (Original) The 3D memory device claim 19, wherein the circuit is further configured to remove the fast charges from a portion of the storage layer associated with the target memory cell.

Micron Ex. 1002, p. 310
Micron v. YMTC
IPR2024-00793

Remarks

Reconsideration of this Application is respectfully requested.

Claims 1-20 are pending in the application, with claims 1 and 16 being the independent claims. No amendment is made in this reply.

Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Statement of Substance of Telephonic Examiner Interview

Examiner Thong Le is thanked for his time during a phone interview held on October 14, 2022, between the Examiner and Applicant's representative Min Yang (Reg. #78,149). During the interview, the outstanding rejections and the applied references were discussed. No agreement was reached regarding allowability of the claims.

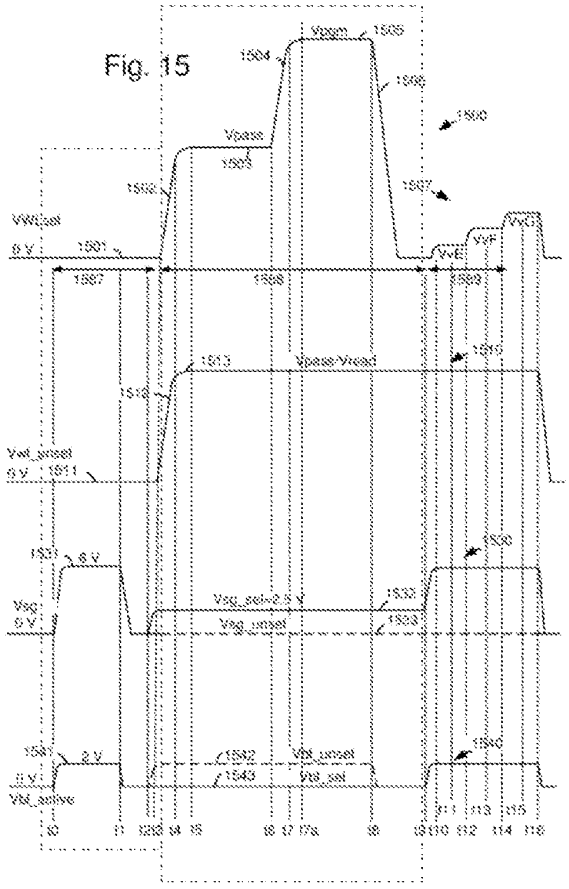
Rejections under 35 U.S.C. § 102

Claims 1-20 are rejected under 35 U.S.C. § 102(a)(1) as being allegedly anticipated by U.S. Publication No. 2019/0371394 to Yang *et al.* ("Yang"). (Office Action, pp. 35). Applicant respectfully traverses these rejections.

Independent claim 1 recites, *inter alia*: "*applying, on an unselected top select gate of an unselected memory string,* ***a prepare voltage*** *during a first time period*," "*applying, on a selected word line associated with the target memory cell,* ***the off voltage*** *during the first time period*," and "*applying, on an unselected word line,* ***a pass voltage*** *during the first time period.*" Independent claim 16 recites similar distinguishing features. The Office Action relies on Yang's Figures 11C-11E and 15 to allegedly disclose all the features of independent claim 1. (Office Action, p. 3). However, while Yang applies the 6V pre-charge voltage to SGD transistors and applies 0V to selected word lines during the pre-charge phase (t0-t3), the voltage signal 1511 applied to

Micron Ex. 1002, p. 311
Micron v. YMTC
IPR2024-00793

unselected word lines is 0V during this period. (Yang, ¶¶[0185]-[0191], FIG. 15, which is reproduced below for convenience). Yang only appears to apply the pass voltage to the unselected word lines during the program phase (t3-t9) and the verify phase (t9-t16). (*Id.*) Thus, Yang does not anticipate claims 1 and 16. Applicant respectfully requests the anticipation rejection of claims 1 and 16 be withdrawn and claims 1 and 16 be passed onto allowance.



Yang, FIG. 15 (annotated).

Dependent claims 2-20 are likewise not unpatentable in view of Yang for at least the same reasons as the independent claims 1 and 16 from which they respectively depend, and further in

Micron Ex. 1002, p. 312
Micron v. YMTC
IPR2024-00793

view of their own respective features. Applicant respectfully requests the rejections of claims 2-20 be withdrawn and these claims be passed onto allowance.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

Date: October 20, 2022

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

18827525.2

Micron Ex. 1002, p. 313
Micron v. YMTC
IPR2024-00793

Electronic Acknowledgement Receipt

EFS ID:	46857692
Application Number:	17324877
International Application Number:	
Confirmation Number:	8686
Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Min Yang/Julia Vang
Filer Authorized By:	Min Yang
Attorney Docket Number:	4123.0850002
Receipt Date:	20-OCT-2022
Filing Date:	19-MAY-2021
Time Stamp:	14:02:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2022-10-20-Cover-Letter-4123-0850002.pdf	198872 4cc08e76cda6f1352526061fe5e47dabae0169a5	no	1

Warnings:

Information:					
2		2022-10-20-Amendment-Reply-111-4123-0850002.pdf	503070 817466e209dc2c5c5704728d4cf2fd09ed9a0a3b	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	8

Warnings:	
Information:	
Total Files Size (in bytes):	701942

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

MIN YANG
STUDENT ASSOCIATE
202-772-8702
MYANG@STERNEKESSLER.COM

October 20, 2022

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8686
Art Unit: 2827

Re: U.S. Utility Patent Application
Appl. No. 17/324,877; Filing Date: May 19, 2021
For: **Method For Reading Three-Dimensional Flash Memory**
First Named Inventor: Zilong CHEN
Our Ref: 4123.0850002

Commissioner:

Transmitted herewith for appropriate action is a document entitled ***Reply Under 37 C.F.R. § 1.111***, which is submitted electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims, or forwarding to appeal), or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

M-Y/jcv
Enclosure(s)

Micron Ex. 1002, p. 316
Micron v. YMTC
IPR2024-00793

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 11/04/2022

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER
LE, THONG QUOC

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/04/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/324,877	05/19/2021	Zilong CHEN	4123.0850002	8686

TITLE OF INVENTION: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	02/06/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

Micron Ex. 1002, p. 317
Micron v. YMTC
IPR2024-00793

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 11/04/2022

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/324,877	05/19/2021	Zilong CHEN	4123.0850002	8686

TITLE OF INVENTION: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	02/06/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, THONG QUOC	2827	365-185020

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Micron Ex. 1002, p. 318
Micron v. YMTC
IPR2024-00793

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/324,877	05/19/2021	Zilong CHEN	4123.0850002	8686

26111 7590 11/04/2022

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/04/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Micron Ex. 1002, p. 319
Micron v. YMTC
IPR2024-00793

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/324,877	Applicant(s) CHEN et al.	
	Examiner THONG Q LE	Art Unit 2827	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 10/20/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/02/2022.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/THONG Q LE/
Primary Examiner, Art Unit 2827

Micron Ex. 1002, p. 321
Micron v. YMTC
IPR2024-00793

DETAILED ACTION

1. Amendment filed on 10/20/2022 has been entered.

2. Claims 1-20 are presented for examination.

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 09/02/2022.

4. Information disclosed and list on PTO 1449 was considered.

Reasons for Allowance

5. Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 1-20 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. The prior art does not teach the claimed invention having a wherein apply, on an unselected top select gate of an unselected memory string, a prepare voltage during the first time period and an off voltage during a second time period; apply, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period;

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THONG QUOC LE whose telephone number is (571)272-1783. The examiner can normally be reached 7:30AM-5:30PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/THONG Q LE/

Primary Examiner, Art Unit 2827

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	**Art Unit**
	THONG Q LE	2827

CPC						
Symbol					**Type**	**Version**
G11C	/	16	/	3427	F	2013-01-01
G11C	/	16	/	0483	I	2013-01-01
G11C	/	16	/	08	I	2013-01-01
G11C	/	16	/	26	I	2013-01-01
H01L	/	27	/	11582	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/THONG Q LE/ Primary Examiner, Art Unit 2827	28 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20221028

Micron Ex. 1002, p. 324
Micron v. YMTC
IPR2024-00793

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	**Art Unit**
	THONG Q LE	2827

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G11C	/	16	/	00	

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
365	185.02

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					
365	185.17	185.22	185.29	185.01	185.05	185.18

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/THONG Q LE/ Primary Examiner, Art Unit 2827	28 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20221028

Micron Ex. 1002, p. 325
Micron v. YMTC
IPR2024-00793

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	Art Unit
	THONG Q LE	2827

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19										
	2		11		20										
	3		12												
	4		13												
	5		14												
	6		15												
	7		16												
	8		17												
	9		18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/THONG Q LE/ Primary Examiner, Art Unit 2827	28 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20221028

Micron Ex. 1002, p. 326
Micron v. YMTC
IPR2024-00793

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	Art Unit
	THONG Q LE	2827

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483;G11C16/10;G11C16/08;G11C11/5628;G11C11/5671;G11C16/3427;G11C16/24;G11C16/26;G11C11/5642;G11C16/0408;G11C2211/5641;G11C16/3459;G11C2211/5621;G11C16/30;G11C16/3418;G11C16/14;G11C16/16;G11C16/32;G11C16/3436;G11C16/3445;G11C11/5635;G11C16/0466;G11C16/349;G11C2211/563;G11C7/12;G11C11/4063;G11C16/12;G11C16/28;G11C16/34;G11C16/3454;G11C16/3481;G11C2211/562;G11C2211/5625;G11C2211/5642;G11C2211/5648;G11C5/145;G11C7/14;G11C7/222;G11C8/08;H01L27/11582;H01L27/11556;H01L27/1157;H01L27/11548;H01L27/11595;H01L27/11524;H01L29/7884;H01L27/0255;H01L27/115;H01L27/11565 365/185.17;365/185.22;365/185.29;365/185.01;365/185.03;365/185.05;365/185.18;365/185.19	10/28/2022	TL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
	365/185.17;365/185.22;365/185.29;365/185.01;365/185.03;365/185.05;365/185.18;365/185.19	10/28/2022	TL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E searched	10/28/2022	TL
Inventor searched	10/28/2022	TL

Micron Ex. 1002, p. 327
Micron v. YMTC
IPR2024-00793

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	Art Unit
	THONG Q LE	2827

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	Interference searched	10/28/2022	TL

Micron Ex. 1002, p. 328
Micron v. YMTC
IPR2024-00793

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/324,877	CHEN et al.
	Examiner	**Art Unit**
	THONG Q LE	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☑ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47		
CLAIM		**DATE**								
Final	Original	07/19/2022	10/28/2022							
	1	✓	=							
	2	✓	=							
	3	✓	=							
	4	✓	=							
	5	✓	=							
	6	✓	=							
	7	✓	=							
	8	✓	=							
	9	✓	=							
	10	✓	=							
	11	✓	=							
	12	✓	=							
	13	✓	=							
	14	✓	=							
	15	✓	=							
	16	✓	=							
	17	✓	=							
	18	✓	=							
	19	✓	=							
	20	✓	=							

Micron Ex. 1002, p. 329
Micron v. YMTC
IPR2024-00793

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	1666056	memory AND three-dimensional	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 09:47 AM
L2	1080	L1 AND (unselect$3 OR deselect$3) WITH select$3 ADJ select$3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:11 AM
L3	229	L2 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:13 AM
L4	140	L2 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:14 AM
L5	75	L2 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1 AND select$3 ADJ word ADJ line$1 AND target	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:14 AM
L6	32	L2 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1 AND select$3 ADJ word ADJ line$1 AND target AND read ADJ voltage AND pass ADJ voltage	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 10:15 AM
L7	28	L6 AND period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD,	OR	ON	ON	2022/07/18 11:52 AM

Micron Ex. 1002, p. 330
Micron v. YMTC
IPR2024-00793

			DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L8	28	L6 AND period AND voltage	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/18 11:52 AM
L9	4	L8 AND first ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:49 AM
L10	3	L8 AND first ADJ period AND second ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:50 AM
L11	0	L8 AND first ADJ tiome ADJ period AND second ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:50 AM
L12	3	L10	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:50 AM
L13	2841561	L8 ans read AND verify	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:51 AM
L14	28	L8 AND read AND verify	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2022/07/19 10:52 AM

Micron Ex. 1002, p. 331
Micron v. YMTC
IPR2024-00793

			AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L15	0	L14 AND read-verifycation	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:52 AM
L16	0	L14 AND read-verification	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:52 AM
L17	9	L14 AND read WITH verification	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:53 AM
L18	28	L14	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 10:53 AM
L19	32	L6	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 11:31 AM
L20	36	(Artificial Intelligence) More like doc: US-20190371394-A1 Text: (CN-111406289-A OR WO-2019236153-A1 OR US-10636487-B2 OR US-11081180-B2 OR US-20200243138-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO,	OR	ON	ON	2022/07/19 04:54 PM

Micron Ex. 1002, p. 332
Micron v. YMTC
IPR2024-00793

		A1 OR DE-112019000157-T5 OR US-10153051-B1 OR US-20190318792-A1 OR US-10482984-B2 OR CN-111406287-A OR WO-2019236152-A1 OR US-10438671-B1 OR US-10726922-B2 OR US-20190371406-A1 OR EP-3455857-B1 OR WO-2019199371-A1 OR US-20190311772-A1 OR US-10446244-B1 OR DE-112019000164-T5 OR US-10269435-B1).did.	MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L21	28	L18	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 04:54 PM
L22	485980	((G11C16/0483 OR G11C16/10 OR G11C16/08 OR G11C11/5628 OR G11C11/5671 OR G11C16/3427 OR G11C16/24 OR G11C16/26 OR G11C11/5642 OR G11C16/0408 OR G11C2211/5641 OR G11C16/3459 OR G11C2211/5621 OR G11C16/30 OR G11C16/3418 OR G11C16/14 OR G11C16/16 OR G11C16/32 OR G11C16/3436 OR G11C16/3445 OR G11C11/5635 OR G11C16/0466 OR G11C16/349 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 04:59 PM

Micron Ex. 1002, p. 333
Micron v. YMTC
IPR2024-00793

		G11C2211/563 OR G11C7/12 OR G11C11/4063 OR G11C16/12 OR G11C16/28 OR G11C16/34 OR G11C16/3454 OR G11C16/3481 OR G11C2211/562 OR G11C2211/5625 OR G11C2211/5642 OR G11C2211/5648 OR G11C5/145 OR G11C7/14 OR G11C7/222 OR G11C8/08 OR H01L27/11582 OR H01L27/11556 OR H01L27/1157 OR H01L27/11548 OR H01L27/11595 OR H01L27/11524 OR H01L29/7884 OR H01L27/0255 OR H01L27/115 OR H01L27/11565 OR H01L27/2454 OR H01L27/249 OR H01L45/04 OR H01L45/06 OR H01L45/10 OR H01L45/145 OR H01L45/146 OR H01L27/11529 OR G06F11/1012 OR G06F11/1072 OR G06F11/186 OR G06F12/0246 OR G06F12/0866).cpc. OR (365/185.17 OR 365/185.22 OR 365/185.29 OR 365/185.01 OR 365/185.03 OR 365/185.05 OR 365/185.18 OR 365/185.19).ccls.)					
L23	1120	L22 AND (unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1 AND select$3 ADJ word ADJ line$1 AND target AND read ADJ voltage AND pass ADJ voltage	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 04:59 PM
L24	0	L23 AND first ADJ tiome ADJ period AND	(US-PGPUB; USPAT; USOCR; FIT (AP, AT,	OR	ON	ON	2022/07/19 05:00 PM

Micron Ex. 1002, p. 334
Micron v. YMTC
IPR2024-00793

		second ADJ period	AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L25	11	L23 AND first ADJ time ADJ period AND second ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/19 05:00 PM
L26	1174	(unselect$3 OR deselect$3) WITH select$3 ADJ gate AND string$1 AND select$3 ADJ word ADJ line$1 AND target AND read ADJ voltage AND pass ADJ voltage	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/28 10:15 AM
L27	150	L26 AND selected ADJ word ADJ line WITH target WITH cell	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/28 10:16 AM
L28	44	(Artificial Intelligence) Similar to: 17/324,877 with 0 CPC Selections and 0 Text Selections Text: (CN-111406288-A OR KR-20200062351-A OR US-10438671-B1 OR KR-102327113-B1 OR WO-2019245607-A1 OR EP-3685383-A1 OR US-20180233207-A1 OR US-10438674-B2 OR US-9972399-B2 OR US-20180033492-A1 OR WO-2019221791-A1 OR US-10269570-B2 OR US-20190355429-A1 OR US-10522232-B2 OR US-10937655-B2 OR TW-201946065-A OR US-20190206690-A1 OR KR-20220068541-A OR US-20190392894-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO))	OR	ON	ON	2022/10/28 10:18 AM

Micron Ex. 1002, p. 335
Micron v. YMTC
IPR2024-00793

		A1 OR CN-111149169-B OR US-9620232-B2 OR US-20160232981-A1 OR US-10825513-B2 OR CN-113066518-A OR US-20190066793-A1 OR US-10388381-B2 OR US-20210398593-A1 OR US-10553298-B1 OR US-20200035312-A1 OR TW-202123244-A OR WO-2021114011-A1 OR US-20210174852-A1 OR EP-3891747-A1 OR US-20190333592-A1 OR CN-111149169-A OR US-10510425-B2 OR US-20180277231-A1 OR JP-7132444-B2 OR US-9349478-B2 OR JP-2018156714-A OR US-11222674-B2 OR TW-I728674-B OR CN-110400588-A OR KR-20190123981-A OR KR-102414186-B1 OR KR-20170114349-A OR KR-20210120072-A OR US-9595345-B2 OR US-20190164609-A1 OR US-10373687-B2).did.					
L29	45	(Artificial Intelligence) Similar to: 17/324,877 with 3 CPC Selections and 2 Text Selections Text: (US-20180233207-A1 OR US-10438674-B2 OR US-9972399-B2 OR US-20180033492-A1 OR US-10937655-B2 OR US-10269570-B2 OR US-20190206690-A1 OR KR-20200062351-A OR CN-111406288-A OR WO-2019245607-A1 OR EP-3685383-A1 OR US-10438671-B1 OR KR-102327113-B1 OR US-20210398593-A1 OR US-20160232981-A1 OR US-9620232-B2	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO))	OR	ON	ON	2022/10/28 10:20 AM

Micron Ex. 1002, p. 336
Micron v. YMTC
IPR2024-00793

		OR KR-20170114349-A OR US-20190066793-A1 OR US-10388381-B2 OR KR-102414186-B1 OR WO-2021261744-A1 OR KR-0161413-B1 OR KR-20180013111-A OR US-20190164609-A1 OR US-10373687-B2 OR TW-I707346-B OR US-20220301628-A1 OR JP-WO2006059375-A1 OR TW-202215651-A OR CN-107393590-B OR US-9672917-B1 OR WO-2006059375-A1 OR TW-201804474-A OR JP-4698605-B2 OR CN-108320772-B OR WO-2019221791-A1 OR CN-111149169-B OR US-20060215477-A1 OR US-10971232-B2 OR CN-107665721-B OR US-7251161-B2 OR US-10236064-B2 OR US-20190051355-A1 OR CN-113066518-A OR TW-201946065-A OR US-20190355429-A1 OR US-20150221387-A1 OR US-10522232-B2 OR US-20190392894-A1 OR US-20190122734-A1).did.					
L30	2	L29 AND first ADJ time ADJ period	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO))	OR	ON	ON	2022/10/28 10:46 AM
L31	0	L29 AND first ADJ time ADJ period AND read-verification	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO))	OR	ON	ON	2022/10/28 10:48 AM
L32	45	L29	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO))	OR	ON	ON	2022/10/28 10:48 AM

L33	472094	((G11C16/0483 OR G11C16/0466 OR G11C16/08 OR G11C16/10 OR G11C16/3459 OR G11C11/5628 OR G11C16/30 OR G11C16/26 OR G11C16/3427 OR G11C16/24 OR G11C16/32 OR G11C16/3418 OR G11C11/5671 OR G11C16/12 OR G11C16/3404 OR G11C16/06 OR G11C16/34 OR G11C5/147 OR G11C16/0408 OR G11C16/14 OR G11C2211/5621 OR G11C16/16 OR G11C17/08 OR G11C11/4074 OR G11C11/4094 OR G11C11/5642 OR G11C16/04 OR G11C16/0425 OR G11C7/14 OR G11C8/08 OR G11C8/14 OR G11C11/5635 OR G11C16/0433 OR G11C16/0458 OR G11C16/20 OR G11C16/28 OR G11C7/065 OR G11C7/10 OR G11C7/1006 OR G11C7/1051 OR G11C7/1078 OR G11C7/12 OR G11C7/22 OR G11C8/10 OR H01L27/11582 OR H01L27/11573 OR H01L27/11524 OR H01L27/11568 OR H01L27/1157 OR H01L27/11556 OR H01L21/28141 OR H01L27/11519 OR H01L27/11565 OR H01L29/40114 OR H01L29/513 OR H01L29/7884 OR H01L29/7926 OR H01L23/528 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO))	OR	ON	ON	2022/10/28 10:50 AM

Micron Ex. 1002, p. 338
Micron v. YMTC
IPR2024-00793

		H01L27/11521 OR H01L27/11529 OR H01L29/40117 OR H01L29/42344 OR H01L29/7883 OR H01L29/7885 OR H01L21/28568 OR H01L21/31116 OR H01L21/76802 OR H01L21/76879 OR H01L27/0207 OR H01L27/115 OR H01L27/11517 OR H01L27/11526 OR H01L27/11551 OR H01L27/11558 OR H01L27/1156 OR H01L27/11578 OR H01L27/1203 OR H01L27/2454 OR H01L27/249 OR H01L29/0649 OR H01L29/0847 OR H01L29/1095 OR H01L29/42328 OR H01L29/7889 OR H01L45/04 OR H01L45/06 OR H01L45/085 OR H01L45/1226 OR H01L45/146).cpc. OR (365/185.17 OR 365/185.02 OR 365/185.18 OR 365/230.03).ccls. OR ("LEE; HEE YOUL".ine. OR "SEO; JI HYUN".ine. OR "CHEN; HONG-YAN".ine. OR "CHEN HONG-YAN".ine.))					
L34	1	L33 AND first ADJ time ADJ period AND read-verification	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO))	OR	ON	ON	2022/10/28 10:50 AM
L35	36	L20	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/28 11:37 AM
L36	2	L32 AND L35	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2022/10/28 11:38 AM

Micron Ex. 1002, p. 339
Micron v. YMTC
IPR2024-00793

			AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	1	L33 AND first ADJ time ADJ period AND read-verification	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/28 10:50 AM

Micron Ex. 1002, p. 340
Micron v. YMTC
IPR2024-00793

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO				Complete if Known	
SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	17/324,877
				Filing Date or 371(c) Date	May 19, 2021
				First Named Inventor	Zilong CHEN
				Art Unit	2827
				Examiner Name	LE, THONG QUOC
Sheet	1	of	1	Attorney Docket Number	4123.0850002

U.S. PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Document Number Number-Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US 1	2019/0294367 A1	09-26-2019	Takada et al.	
	US 2	2017/0076813 A1	03-16-2017	Kato et al.	

FOREIGN PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

18962212.1

Examiner Signature	/THONG Q LE/	Date Considered	10/28/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.Q.L/

MIN YANG
STUDENT ASSOCIATE
202-772-8702
MYANG@STERNEKESSLER.COM

Sterne Kessler
STERNE KESSLER GOLDSTEIN & FOX

February 1, 2023

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8686
Attn: Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 17/324,877; Filed: May 19, 2021
For: **Method For Reading Three-Dimensional Flash Memory**
First Named Inventor: Zilong CHEN
Our Ref: 4123.0850002

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated **November 4, 2022**, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Issue Fee Transmittal (Form PTOL-85);
2. Online Credit Card Payment Authorization for $1,200 to cover:

   $1,200 – Issue Fee; and
3. Comments on Statement of Reasons for Allowance.

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

M-Y/jcv
Enclosure(s)

Micron Ex. 1002, p. 342
Micron v. YMTC
IPR2024-00793

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 11/04/2022

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/324,877	05/19/2021	Zilong CHEN	4123.0850002	8686

TITLE OF INVENTION: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	02/06/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, THONG QUOC	2827	365-185020

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sterne, Kessler, Goldstein & Fox P.L.L.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Yangtze Memory Technologies Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Wuhan, Hubei, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 19-0036

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Min Yang/ Date February 1, 2023

Typed or printed name Min Yang Registration No. 78,149

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Micron Ex. 1002, p. 343
Micron v. YMTC
IPR2024-00793

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Zilong CHEN	Confirmation No.: 8686
Applicant: YANGTZE MEMORY TECHNOLOGIES CO., LTD.	Art Unit: 2827
Application No.: 17/324,877	Examiner: LE, THONG QUOC
Filing Date: May 19, 2021	Atty. Docket: 4123.0850002

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

Comments on Statement of Reasons for Allowance

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop: Issue Fee

Commissioner:

Applicant thanks the Examiner for indicating the allowability of claims 1-20 in the Notice of Allowance dated November 4, 2022.

Comments on Statement of Reasons for Allowance

Applicant notes the Examiner's Statement of Reasons for Allowance presented on page 2 of the Notice of Allowance. Applicant reserves the right to demonstrate claims 1-20 are allowable over the art made of record for further reasons related to any of their recited features. Applicant further contends that reservation of this right does not give rise to any implication regarding whether the Applicant agrees with or acquiesces in the reasoning provided by the Examiner.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

Date: February 1, 2023

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/324,877	02/01/2023 11:40:27 AM ET	4123.0850002

Title of Invention

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8686	FILED BY	Julia Vang
PATENT CENTER #	61525593	AUTHORIZED BY	Min Yang
CUSTOMER #	26111	FILING DATE	05/19/2021
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Zilong CHEN

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1008	E202321B42262125	Julia Vang

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1501	UTILITY ISSUE FEE	1200.00	1	1200.00
			TOTAL AMOUNT:	$1,200.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage

submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
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P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/324,877	**02/01/2023 11:40:27 AM ET**	**4123.0850002**

Title of Invention

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8686	FILED BY	Julia Vang
PATENT CENTER #	61525593	FILING DATE	05/19/2021
CUSTOMER #	26111	FIRST NAMED INVENTOR	Zilong CHEN
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Min Yang

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2023-02-01-Cover-Letter-4123.0850002.pdf	1	Miscellaneous Incoming Letter	217 KB
2023-02-01-Issue-Fee-4123-0850002.PDF	1	Issue Fee Payment (PTO-85B)	260 KB
2023-02-01-Comments-Statement-Reasons-for-Allowance-4123-0850002.pdf	1	Post Allowance Communication - Incoming	126 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)

2023-02-01-Cover-Letter-4123.0850002.pdf	9FADB87D211E0C2E3E758256AE2E9FF77F3C64A1B77FADECF57D638B423E1804D663374DB4165070079C7F6938773E59176E9EAC1A6EA98C926D5A2B0A78826C
2023-02-01-Issue-Fee-4123-0850002.PDF	5A06AA8A4D2359A9F6C33D13ABF25D552262E2256A188EBC3191843D000C9B18A094C1E6A66F2E4D27B349296EF6B0A92E2040DAF9276F139A69025CC0C3FFF0
2023-02-01-Comments-Statement-Reasons-for-Allowance-4123-0850002.pdf	BD00B1CC88DE583D4845EE574FD08E0AC8A0CCDAE5FAF1C8B3159AC19E8511AC56CFF767510163643E77A06B8CB5D8D4FE012885E9E0009AB41333F3351F247C

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/324,877	03/07/2023	11600342	4123.0850002	8686

26111 7590 02/15/2023

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 7 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Zilong CHEN, Wuhan, CHINA;
Xiang FU, Wuhan, CHINA;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Micron Ex. 1002, p. 349
Micron v. YMTC
IPR2024-00793