

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00793
U.S. Patent No. 11,600,342
Issue Date: May 19, 2020

Title: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

DECLARATION OF DAVID KUAN-YU LIU, PH.D.

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I, David Kuan-Yu Liu, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or of any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in the claims of U.S. Patent No. 11,600,342, which I refer to herein as the ’342 patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$550 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My curriculum vitae (“CV”) is included as Ex. 1004 and provides an accurate description of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

6. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

7. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

8. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating a novel source-side injection mechanism for flash EPROM channel hot-electron programming. A source-side injection mechanism is one particular form of a hot carrier injection (HCI) mechanism.

9. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing flash cell and periphery devices in AMD's CMOS-based 0.5 μm and 0.35 μm flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology to accommodate x-decoder transistors and high voltage transistors for negative gate

erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

10. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices. This included various different types of memory, including NAND flash memory and embedded flash memory.

11. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

12. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75 nm CMOS technology node, a half node version between 90 nm and 65 nm).

13. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing embedded non-volatile memory process technology for power management product applications.

14. Since 2007, I have served as a technical consultant where I have provided expert advice regarding flash memory technology, CMOS process

technology, and semiconductor device physics. As part of this, I have considered, assessed, and assisted with the design of various different memory devices, including NAND flash and monolithic 3D memory structures.

III. ASSIGNMENT AND MATERIALS CONSIDERED

15. I have been asked to provide analysis and explain the subject matter of the '342 patent, including the state of the art when the application underlying the '342 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '342 patent including how that art relates to the challenged claims of the '342 patent and to provide my opinions regarding whether that art invalidates the claimed subject matter.

16. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the claims of the '342 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any applicable rule.

17. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '342 patent.

18. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of

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scientific and engineering principles, and my experience. I have also reviewed and considered the '342 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials.

Exhibit	Description
1005	U.S. Patent Publ. No. 2021/0027848 A1 to Seo (“Seo”)
1006	U.S. Patent Publ. No. 2015/0003169 A1 to Nam et al. (“Nam”)
1007	Choi et al., “Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory,” 2016 Symposium on VLSI Technology, Digest of Technical Papers, 78-79 (“Choi”)
1008	U.S. Patent Publ. No. 2012/0151301A1 to Izumi et al. (“Izumi”)
1012	U.S. Patent No. 9,589,978 to Yip
1013	Aritome, “NAND Flash Memory Technologies” (2016)
1014	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1015	U.S. Patent Publ. No. 2020/0168276 A1 to Yang
1016	U.S. Patent No. 9,620,233 to Dong et al.
1017	Micheloni, “3D Flash Memories” (2016)
1018	U.S Patent No. 10,276,251 B1 to Lobana et al.
1019	U.S Patent No. 9,361,993 B1 to Chen et al.
1020	Affidavit of Nathaniel E. Frank-White (Internet Archive) re Choi Reference (Ex. 1007)
1021	Declaration of Gordon MacPherson (IEEE) re Choi Reference (Ex. 1007)

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Exhibit	Description
1022	Certified File History of U.S. Patent No. 10,403,637 to Lue
1023	Wu et al., “Multiscale simulation of lateral charge loss in Si3N4 3D NAND flash based on density functional theory,” Journal of Physics D: Applied Physics, vol. 52, no. 39, 395103, 2019
1024	U.S. Patent Publ. No. 2019/0198117 A1 to Yu et al.
1025	U.S. Patent No. 10,121,529 B2 to Lee
1026	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1027	U.S. Patent Publ. No. 2020/0395372 A1 to Seo et al.
1028	U.S. Patent Publ. No. 2019/0348122 A1 to Ko et al.
1029	U.S. Patent Publ. No. 2016/0293271 A1 to Won et al.

IV. UNDERSTANDING OF THE LAW

19. I am not an attorney, but have been instructed in and applied the law as described in this section.

20. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the claims of the alleged invention in Section V below.

21. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of

claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

22. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

23. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

24. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

25. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

26. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

27. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

28. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed

at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

29. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

30. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

31. I have been informed and I understand that factors referred to as “objective indicia of non-obviousness” or “secondary considerations” are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

32. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention.

33. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

34. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

35. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

36. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity.

37. In my opinion, a POSITA in the field of the '342 patent would have had a master's degree in electrical engineering or a similar discipline, along with 4-5 years of professional experience working with (e.g., researching, designing, or developing) NAND flash memory devices (including issues relating to the operation,

e.g., reading of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

38. In my opinion, this POSITA would have been aware of and generally knowledgeable about NAND memory's structure, its component parts, how it operates, and how it is controlled.

39. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile NAND flash memory—I was a person of more than the ordinary level of skill in the art as of October 23, 2019, which I have been asked to assume is the effective filing date of the '342 patent. In forming my opinions, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGY BACKGROUND

40. This section provides technology background to the '342 patent.

A. NAND Flash Structure

41. “Flash memory” represents an example of “non-volatile memory.” Ex. 1012, 1:24-26.

42. “Non-volatile memory is memory that can retain its data values for some extended period without the application of power.” Ex. 1012, 1:26-28.

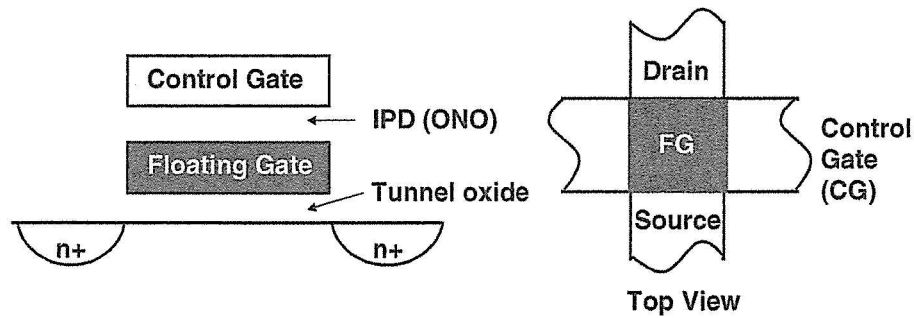
43. NAND flash has been known and in use for quite some time, having been first developed in 1987. *See* Ex. 1013, 22.

44. Like all semiconductor memory, NAND flash includes memory “cells.” In NAND flash, data is stored in a “cell” formed from a single transistor that is the logical equivalent of what a POSITA would have understood to be a “NOT AND” circuit. Ex. 1013, 38-39. This is why this type of memory is referred to as “NAND.”

45. A NAND memory cell can be formed from a “Nch MOS transistor with [a] poly-silicon floating gate (FG).” Ex. 1013, 38-39. “Charge is stored in [the] FG” and the “potential of [the] FG is controlled by a control gate (CG) voltage with capacitive coupling between [the] CG and FG.” *Id.*

46. The presence and the amount of the charge on the floating gate of this type of cell will determine how well the memory cell transistor conducts current under a given control gate voltage. For an Nch memory cell, the more electrons that are stored on the floating gate, the higher the control gate voltage will need to be to turn on the transistor. This control gate voltage that turns on the transistor is known as the threshold voltage.

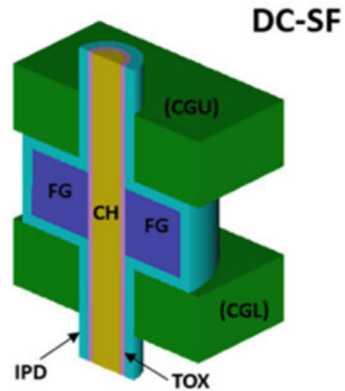
47. The below figure provides an example of one type of flash memory cell:



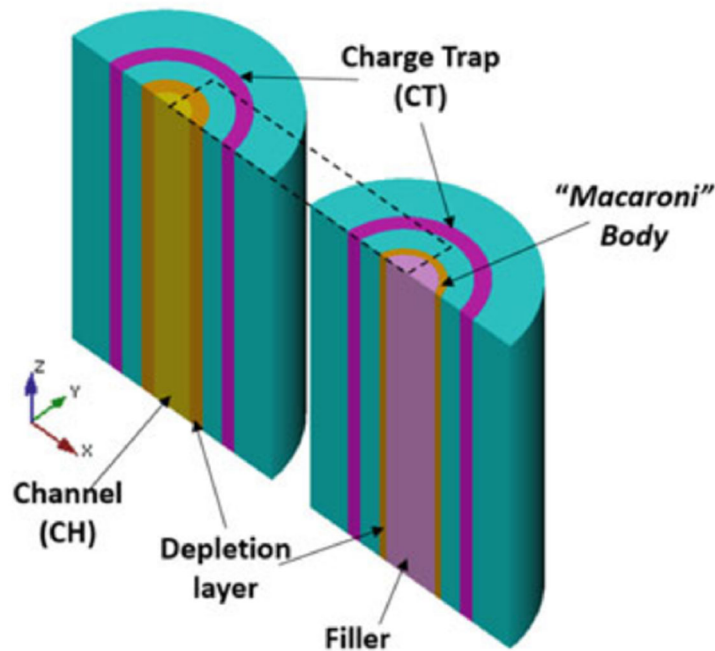
Ex. 1013, 39.

48. Other NAND flash employs a transistor with a “charge trap[.]” *See* Ex. 1026, 109. In this type of transistor, charge is stored in “non-conducting dielectric layer,” like silicon nitride, instead of a conductive floating gate. *See id.*

49. The two most common types of 3D Flash memory cells are conductive floating gate memory cells and charge-trap memory cells. Because of the conductive floating gates, the vertical memory string with conductive floating gates is made with separated floating gates. The conductive floating gates must be separated because, otherwise, the charge in respective memory cells would not remain in the respective memory cells. The below shows one level of such a string (I discuss these vertical memory strings below):



Ex. 1017, 145. Charge-trap technology, in contrast, employs a non-conductive data storage portion, e.g., silicon nitride, and thus the charge-trap layer is not separated and merely extends through the entire vertical string:



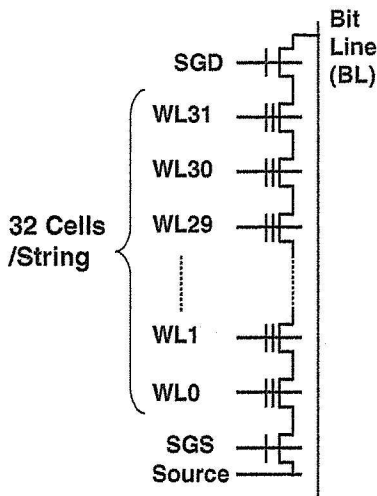
Id., 106.

50. NAND flash memory cells are arranged in “strings” with multiple cells “connected in series.” Ex. 1013, 38.

51. The cells are flanked by “two select transistors (SGD, SGS).” Ex. 1013, 38. The “SGD connects” at the string’s drain side “to isolate it from the bit line (BL),” and the “SGS connects at” the string’s source side “to isolate it from a source line (SL).” *Id.*

52. Word lines are connected to the control gate of each memory cell. Ex. 1013, 38-39.

53. An example of one NAND memory string with memory cells arranged in series along the string is shown below:

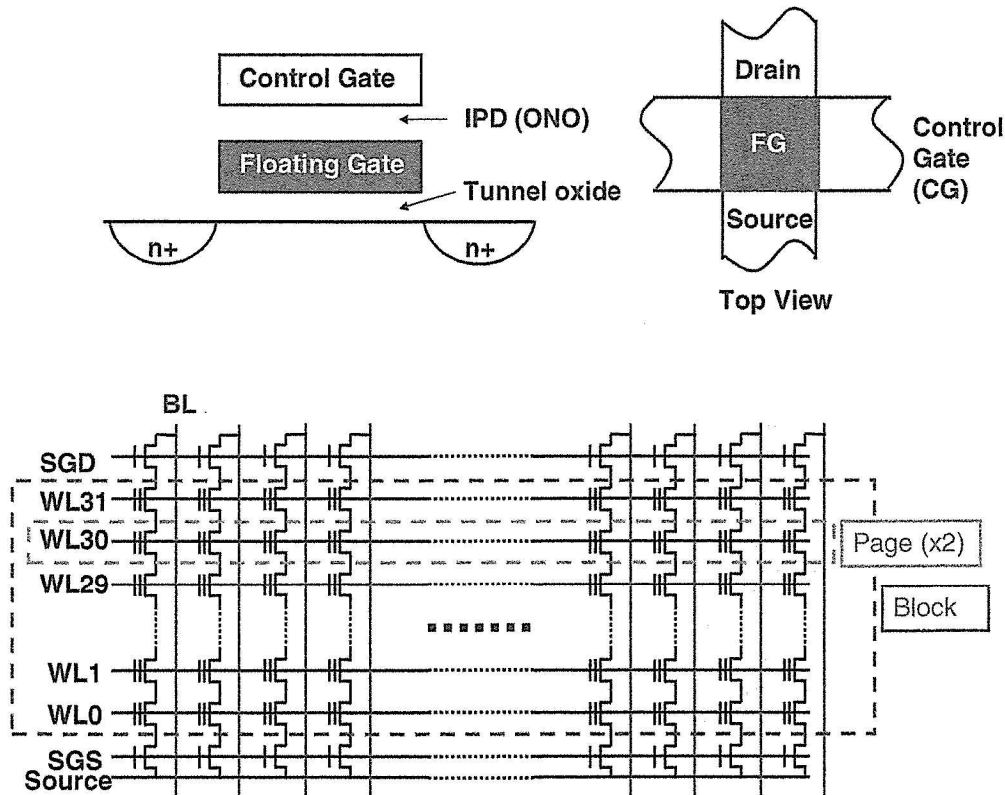


Ex. 1013, 39.

54. Early NAND flash devices were formed as two-dimensional arrays on a substrate surface.

55. Here, the “memory array is formed by straight active area lines ... and straight gate lines” located on a substrate surface. Ex. 1013, 38. Memory cells are located at the “intersection[s]” of the lines. *Id.*

56. An example of this is shown below, with an example memory cell again shown in the top figure, and a two-dimensional array of such cells shown in the figure below:



Ex. 1013, 39-40.

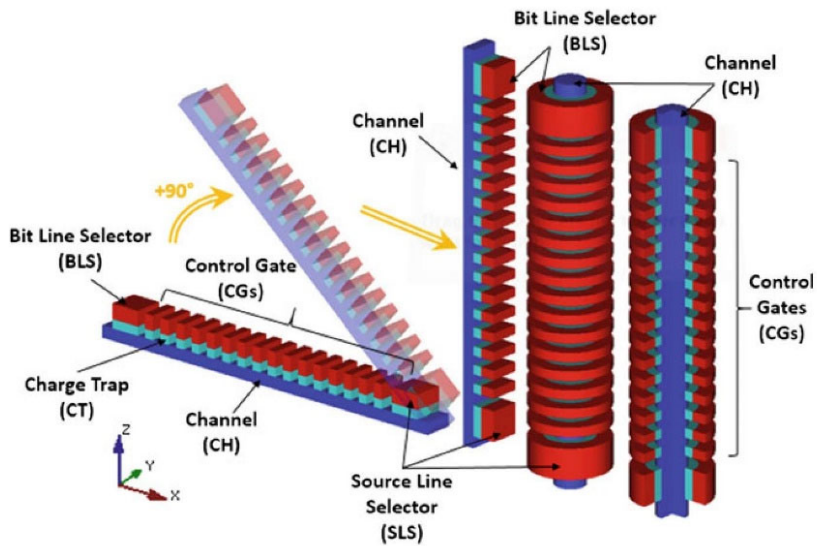
57. As also shown, the cells are grouped into “page[s]” extending along the word lines and “block[s].” Ex. 1013, 40. “[R]ead and program operations are performed per page” while “the erase operation is performed per block.” *Id.*, 39.

58. “In order to further scale down the memory cell size of NAND flash memory,” the art developed so-called “three-dimensional (3D) NAND flash cells” starting in about 2006. Ex. 1013, 292.

59. In 3D NAND, rather than arranging memory cells in a two-dimensional array, 3D NAND arranges cells in a three-dimensional array that is built up in layers.

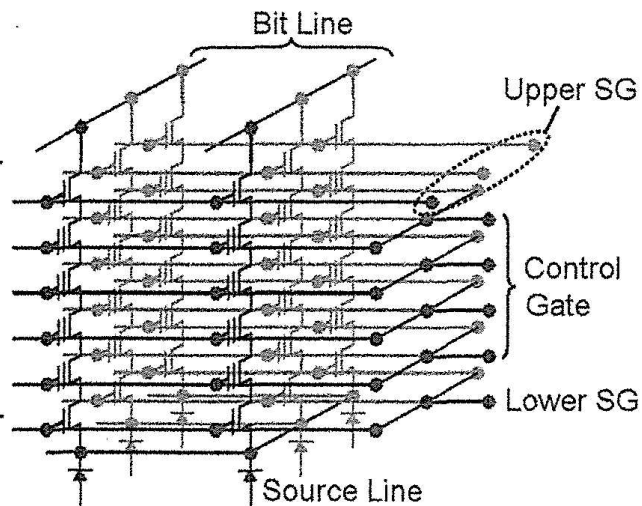
60. A POSITA would have known that “[c]onceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1014, 3.

61. The following image provides a demonstrative example of the relationship between the structure of a 2D NAND string and a 3D NAND string:



Ex. 1026, 122.

62. Multiple such vertical channels are then repeated in a three-dimensional array:



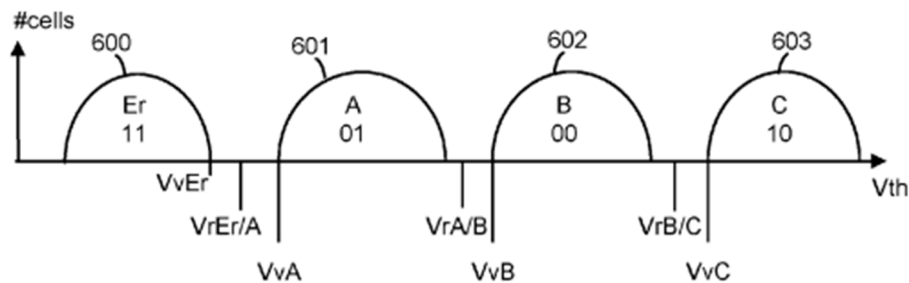
Ex. 1013, 296.

63. “Production of 3D NAND flash memory ... started in August 2013.”

Ex. 1013, 393.

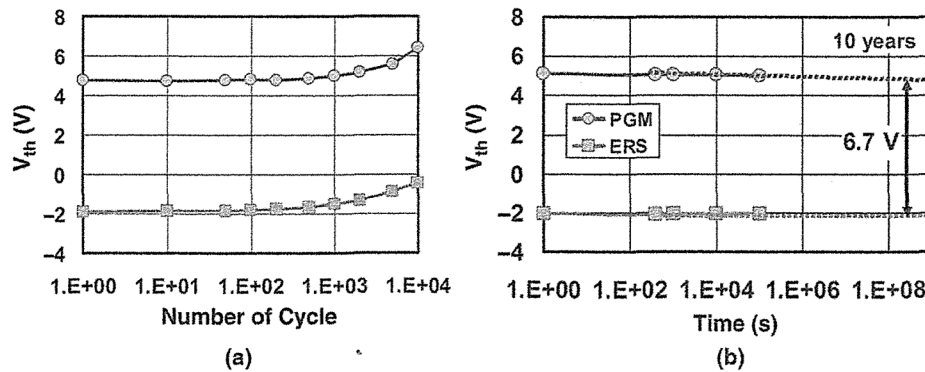
B. 3D NAND Flash Operation

64. A memory cell stores a data state (e.g., binary 00, 01, 10, or 11 for a cell designed to hold two bits) through a programming operation that injects and retains some amount of charge in its charge-storage material. The threshold voltage (V_{th}) at which the cell transistor turns on increases “in proportion to the amount of stored charge.” Ex. 1016, 13:43-49. The data state of the memory cell is represented by a given tight window of threshold voltage. A two-bit-per-cell NAND memory may have a V_{th} -versus-data-state distribution illustrated below:



Id., FIG. 6; *see also* Ex. 1013 at 342-44 (FIG. 7.77 showing same).

65. It is well known to a POSITA that in an MLC NAND flash memory cell, and an SLC memory cell as well, the V_{th} in the erase state, or the lowest V_{th} state, is usually negative. Ex. 1013, 312.



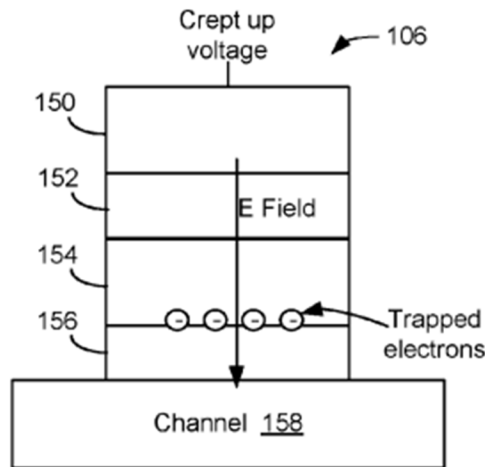
Id., FIG 7.33 (showing the retention characteristics for the highest programmed V_{th} and the erase V_{th} (lowest V_{th} state), with the erase V_{th} having negative value).

66. During read operations, all cell transistors on a selected memory string except the selected cell to be read are given a control gate voltage that is higher than the highest V_{th} of all possible data states to render the transistors conductive, also known as a pass voltage. *Ex.* 1016, 3:21-27, 3:33-37. A read voltage between two data states is applied to the control gate of the selected cell. *Id.*, 3:22-29, 14:31-34. If the read voltage is higher than the V_{th} of the selected cell, the cell transistor turns on and the memory string conducts current. Otherwise, the string does not conduct current. This process allows the threshold voltage of the target cell to be measured and its data state to be determined. *Id.*, 3:10-11, 9:66-10:15, 14:34-37.

67. NAND device programming involves a cycle of two steps: a programming operation and a read (also known as verify) operation. For 3D NAND flash devices, the programming operation is typically done via incremental step

pulse programming (“ISPP”). The ISPP process involves applying a voltage pulse to a control gate of the selected word line—while simultaneously applying a pass voltage to unselected word lines—to inject electrons into a charge-storing part of the transistor, e.g., a floating gate or charge-trapping layer. *See e.g.*, Ex. 1019, 11:47-50. Then, a read (verify) operation may be performed after the programming operation to verify correct programming of the memory cell, i.e., to determine whether the programming pulse was sufficient. Ex. 1018, 10:43-47; Ex. 1019, 11:50-52. This verify operation can be identical to the read operation described above (using a verify voltage). Ex. 1018, 16:18-21; Ex. 1019, 17:10-13. ISPP will stop if the verify operation confirms that the memory cell has been programmed to the correct threshold voltage (above the verify voltage). Ex. 1019, 11:27-31; Ex. 1015, [0104]. Otherwise, the ISPP process will continue until the proper threshold voltage has been reached.

68. Data storage using charge trap technology, e.g., storing charges in a charge-trap memory cell, has a drawback in that charges may escape (i.e., de-trap) over time, especially under high temperature. Ex. 1013, 327. Electric fields can cause de-trapping which, over time, can alter the intended data state. *Id.*, Ex. 1016, 3:52-59, 17:12-17. Charges at shallow interfaces of the charge-trapping layer, sometimes referred to as “fast charges,” are more susceptible to this phenomenon. *Id.*, 2:44-51, 3:54-63.



Id., FIG. 1A.

VII. THE '342 PATENT

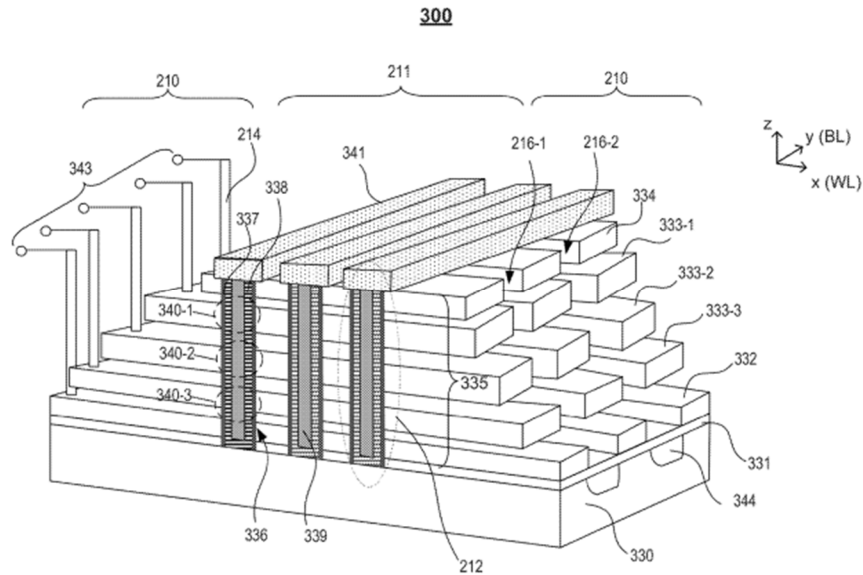
A. Effective Filing Date

69. I understand that the application leading to the '342 patent was filed on May 19, 2021. Based on my review of the '342 patent, I note that it also references a PCT application on its face, which was filed October 23, 2019. For purposes of this declaration, I have been instructed to assume that October 23, 2019 is the effective filing date of the '342 patent.

70. My opinions in this declaration were formed from the perspective of a POSITA as of October 23, 2019, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

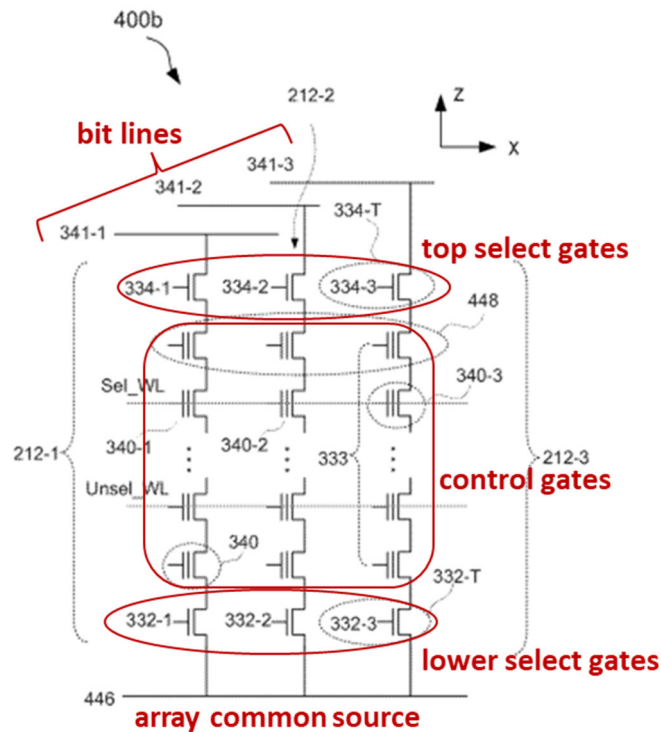
B. Overview

71. The '342 patent relates to “[a] method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device.” Ex. 1001, Abstract.



Id., FIG. 3.

72. The 3D memory device of the '342 patent is a NAND flash memory based on charge-trapping technology. Ex. 1001, 1:29-32, 7:15-22. I discuss charge-trapping technology in Section VI. The '342 patent's 3D memory has a conventional structure of vertical memory strings, control gate (word lines), and select gates:



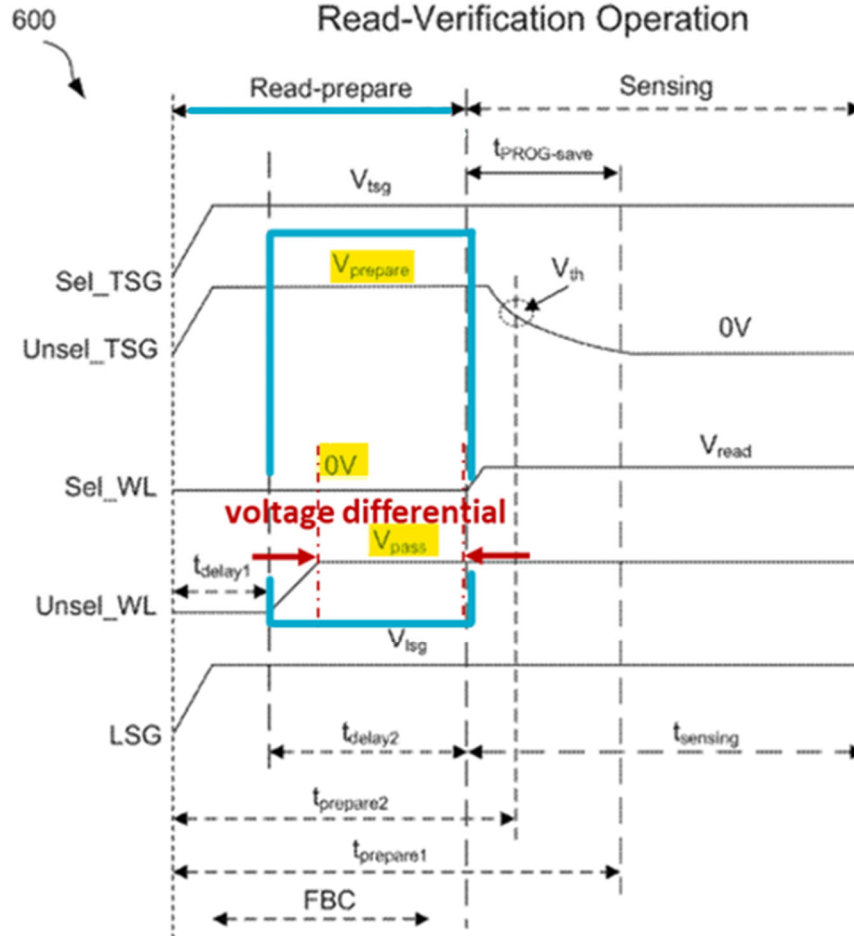
Id., FIG. 4B (annotated); 7:51-8:4.

73. The '342 patent recognizes the issue of de-trapping in charge-trap memories. Ex. 1001, 1:29-36. The patent refers to “charges trapped in shallow traps” as “fast charges.” *Id.*, 1:33. This is because this de-trapping occurs soon after programming.

74. The '342 patent discusses “removing fast charges of the target memory cell at a read-prepare step” before a read/sensing operation. Ex. 1001, Abstract, FIGs. 6-8. In short, the '342 patent seeks to remove the fast charges because, in effect, removing the fast charges would create a consistent amount of charge in the cell after programming, and these fast charges should not be accounted in

determining the threshold voltage, or the data state, of the memory cell. In other words, if one were not to remove the fast charges, the fast charges would de-trap over time and the amount of charge in the cell would decrease over that period of time, potentially changing the threshold voltage to the point of changing the data state.

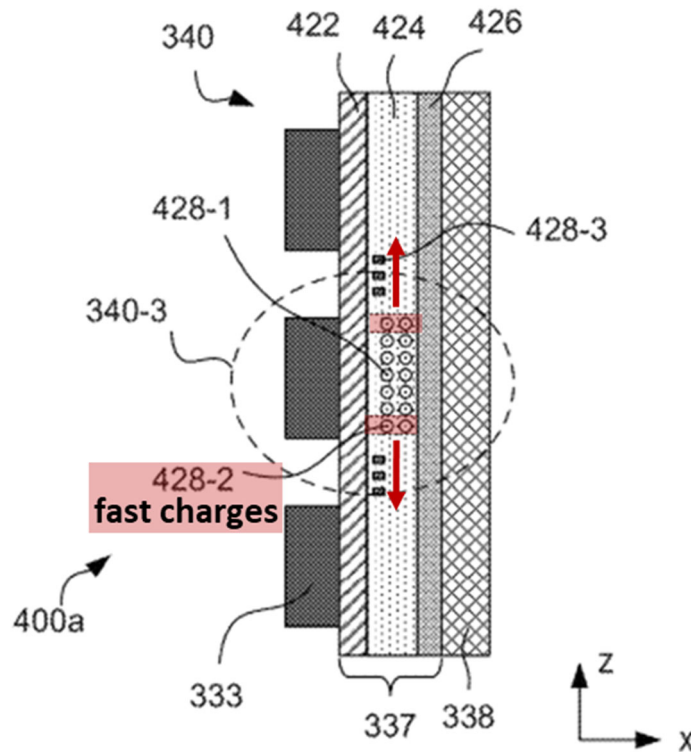
75. The '342 patent teaches “[r]emoving the fast charges of the target memory cell includes applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).” Ex. 1001, Abstract. This operation and the corresponding voltages can be seen below:



Ex. 1001, FIG. 6 (annotations added). The read-prepare period occurs before the sensing period, and the sensing period is the time in which the target memory cell is read. The prepare voltage, also called “pre-pulse,” turns on the unselected top select gate (Unsel_TSG), i.e., the unselected string. *Id.*, 8:67, 12:56-62. Unselected means that memory string is not the target of the sensing operation, and should not contribute to the current on the bitline during the sensing period. The pass voltage, which is applied to Unsel_WL during the read-prepare and sensing periods, is a term

of art and turns on the unselected word lines (Unsel_WL). “Turn on” means that the voltage on the control gate or select gate is sufficient to create a conductive channel in the respective portion of that memory string. In other words, like turning on a MOSFET, the voltage is above the threshold value to create a conductive channel.

76. The differential between V_{off} on a selected word line and V_{pass} on neighboring, unselected word lines (in particular, adjacent word lines) generates an electric field. This electric field is simply the result of the voltage difference between the selected word line and the adjacent unselected word lines. The field may be present not only at the surface of the memory film, but also can extend into the channel layer. 12:10-34. This electric field exerts a force to “de-trap the fast charges 428-2 from the shallow traps, pull[ing] them towards the neighboring unselected memory cells.” Ex. 1001, 12:24-34.



Id., FIG. 4A (annotated). After the fast charges are removed from the selected cell, they may be “recombined with charges of opposite sign or be removed through the conductive path established in the channel of the unselected memory cells.” *Id.*, 12:34-37. The charge-recombination mechanism does not require a conductive path through the memory string, due to the presence of holes that are already in the semiconductor film.

C. Prosecution History

77. As noted above, I have reviewed the '342 patent's prosecution history.

78. During prosecution of the application that resulted in the '342 patent, the claims were rejected under 35 U.S.C. §102(a)(1) over U.S. publication

2019/0371394 (to Yang). Ex. 1002, 271-274. In response, Applicant distinguished Yang by arguing that during the first time period, zero volts are “applied” to the “unselected word lines” in contravention of claim 1 of the ’342 patent, which requires that a pass voltage be applied during the first time period. *Id.*, 311-312. A notice of allowance followed. *Id.*, 321-323.

D. Claims

79. For reference, claims 1-6 and 8-20 of the ’342 patent are reproduced below:

1. A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:

applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period;

applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and

applying, on an unselected word line, a pass voltage during the first time period and the second time period,

wherein the read-verification operation removes fast charges of the target memory cell during the first time period.

2. The method of claim 1, further comprising:

applying, on a selected top select gate of a selected memory string containing the target memory cell, a top select gate voltage during the first time period and the second time period; and

applying, on a lower select gate of the selected memory string containing the target memory cell, a lower select gate voltage during the first time period and the second time period.

3. The method of claim 2, wherein the applying the top select gate voltage comprises electrically connecting the selected memory string to a bit line; and the applying the lower select gate voltage comprises electrically connecting the selected memory string to an array common source.

4. The method of claim 2, wherein the applying the pass voltage comprises applying the pass voltage with a delay period after the selected top select gate and the lower select

gate are at the top select gate voltage and the lower select gate voltage, respectively.

5. The method of claim 1, further comprising:

measuring a threshold voltage of the target memory cell during the second time period.

6. The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell.

8. The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is lower than a threshold voltage of an unselected memory cell.

9. The method of claim 1, wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V.

10. The method of claim 1, wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V.

11. The method of claim 1, wherein applying the off voltage comprises applying a voltage about 0V.

12. The method of claim 1, wherein the removing the fast charges comprises:

removing the fast charges from a storage layer of the target memory cell.

13. The method of claim 1, wherein the removing the fast charges comprises:

removing electrical charges from shallow traps in the storage layer of the target memory cell.

14. The method of claim 1, wherein the removing the fast charges comprises:

removing the fast charges from the target memory cell to a neighboring unselected memory cell.

15. The method of claim 1, wherein conducting the read-verification operation comprises conducting a failed bit count in parallel.

16. A three-dimensional (3D) memory device, comprising:

a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein:

each memory string comprises a plurality of memory cells; and

each memory cell is addressable through a word line and a bit line; and

a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:

apply, on an unselected top select gate of an unselected memory string, a prepare voltage during the first time period and an off voltage during a second time period;

apply, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and

apply, on an unselected word line, a pass voltage during the first time period and the second time period.

17. The 3D memory device of claim 16, wherein the circuit is further configured to:

electrically connect a selected memory string containing the target memory cell to the bit line and an array common source by applying a top select gate voltage on a selected top select gate and applying a lower select gate voltage on a lower select gate during the first time period and the second time period.

18. The 3D memory device of claim 17, wherein to remove the fast charges of the target memory cell, the circuit is further configured to:

apply the top select gate voltage on the selected top select gate and the lower select gate voltage on the lower select gate before applying the pass voltage on the unselected word line.

19. The 3D memory device of claim 16, wherein each memory string comprises:

a channel hole;
a core filling film in a center of the channel hole;
a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and
a channel layer sandwiched between the memory film and the core filling film.

20. The 3D memory device claim 19, wherein the circuit is further configured to remove the fast charges from a portion of the storage layer associated with the target memory cell.

VIII. CLAIM CONSTRUCTION

80. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

81. I have been informed that the words of a claim are generally given the ordinary and customary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification, and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

82. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

83. In my opinion, the terms of the '342 patent's claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

84. Nonetheless, I will address how the '342 patent describes “applying” voltages “during” particular “time period[s].” Consistent with the plain and ordinary meaning of such language, the '342 patent uses it to mean that sometime during a given period, a given voltage is applied. In other words, the '342 patent does not use this language to mean that the given voltage is applied throughout the given time period.

85. For example, claim 1 recites “applying, on an unselected word line, a pass voltage during the first time period....” Ex. 1001, Claim 1. As can be seen below, the pass voltage V_{pass} is not applied throughout the first (“Read-prepare”) time period:

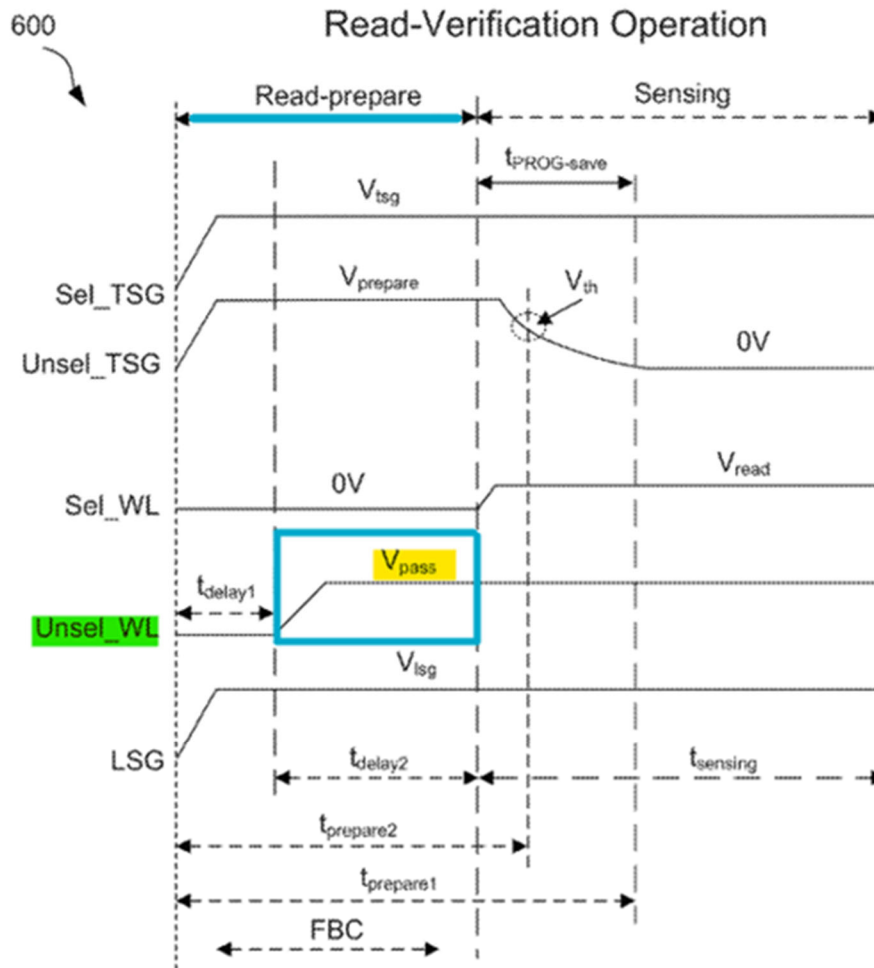


Fig. 6

Id., FIG. 6.

86. This understating of “applying” a voltage “during” is consistent with claim 4. Claim 4 recites: “The method of claim 2, wherein the applying the pass voltage comprises applying the pass voltage with a delay period after the selected top select gate and the lower select gate are at the top select gate voltage and the lower select gate voltage, respectively.” As can be seen from this language, there is

a delay period before applying the given voltage, and thus the voltage is not applied during the entire read-prepare stage. Because claim 1 is broader than claim 4, this means that the claimed voltages, e.g., the pass voltage, need not be applied during the entire claimed periods, e.g., “during the first time period.”

IX. UNPATENTABILITY ANALYSIS

87. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '342 patent, a POSITA would have considered claims 1-6 and 8-20 of the '342 patent to be unpatentable as obvious over the prior art discussed in this declaration.

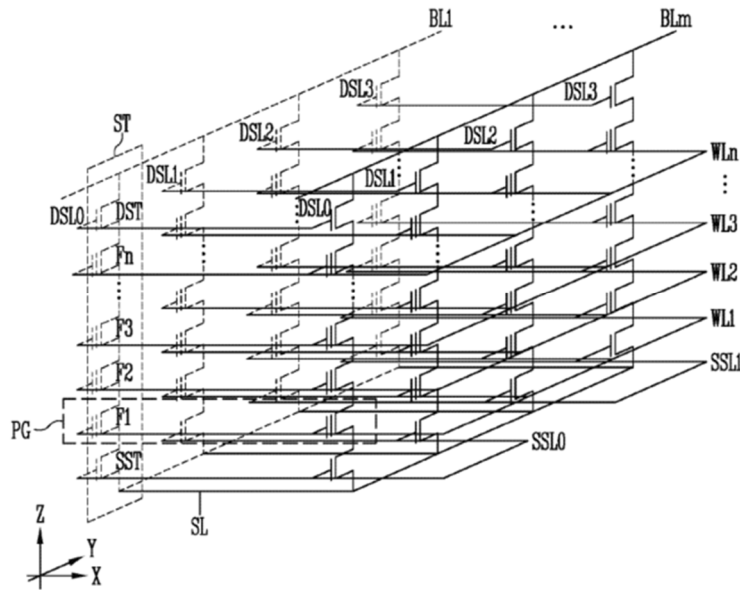
A. Overview of the Prior Art

88. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

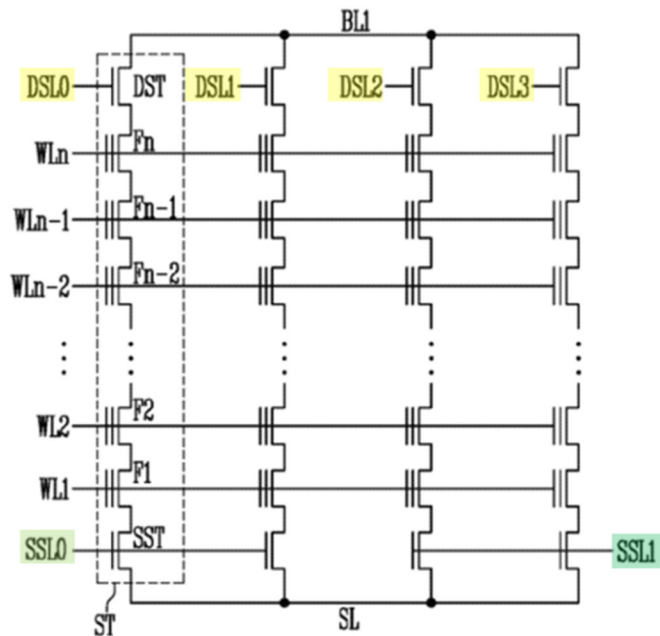
1. Seo

89. U.S. Patent Publ. No. 2021/0027848A1 (“Seo”) was filed on October 18, 2019, and was published on January 28, 2021. Ex. 1005, Cover. I understand that Seo is prior art to the '342 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

90. Seo generally relates to read operations of nonvolatile memory devices such as 3D NAND flash memory. Ex. 1005, Abstract, [0004]-[0007].



Id., FIG. 3. As shown above, Seo’s memory devices comprise memory strings with individual drain select lines (“DSL”) and partially shared source select lines (“SSL”). Individual drain select lines means that one line controls a single memory string for a given bitline, whereas shared source select lines means that one line controls more than one string. The drain is on the top, and the DSL are top select gates. The source is on the bottom, and the SSL are bottom select gates. More specifically, each of the four memory strings has a dedicated DSL (DSL0-DSL3). But the two strings on the left share SSL0, while the two strings on the right share the separate SSL1.

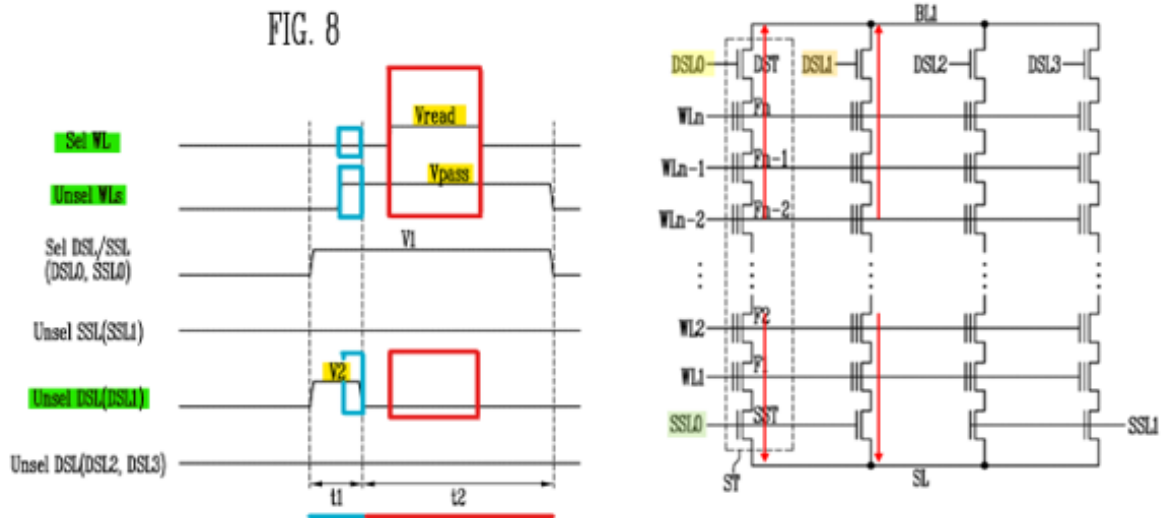


Id., FIG. 4 (annotated).

91. Seo is focused on reducing a disturbance known as hot carrier injection (“HCI”) occurring on an unselected memory string during read operations. Ex. 1005, [0008], [0048]. As I discuss in Section VI.B, during read operations, a high pass voltage is applied to all word lines coupled to unselected memory cells to make the cells conductive. *Supra* §VI.B; Ex. 1013, 254. Again, this is necessary so that it can be determined whether the read voltage applied to the target word line turns on, or does not turn on, the selected memory cell. The high gate voltage boosts the channel voltage of the unselected cells. *Id.* This voltage boost generates hot electrons at a selected cell if the voltage differential between its source and drain is large. *Id.* The hot electrons can be injected into an unselected cell sharing the same selected word line and disturb its data state. *Id.* Disturb means alter the state from

the expected or programmed state. This can inadvertently change the programmed state (or erased state) of the unselected memory cells. By applying DSL and SSL voltages *before* the read operation, Seo controls channel voltages of the relevant memory strings via coupling to bit lines and source lines, reducing voltage boost and HCI. Ex. 1005, [0048], [0088]-[0089]. This mitigates the disturb issue.

92. Seo refers to two time periods: t1 and t2. The first period (t1) comes before the actual sensing period of t2. As shown below, during t1, (1) a high pass voltage, a turn on voltage, is applied to the unselected word line (“Unsel WLs”), (2) an off voltage, ground, is applied to the selected word line (“Sel WL”), and (3) a high prepare voltage, V2, is applied to the unselected string (“Unsel DSL”). During t2, (1) a high pass voltage is applied to the unselected word line, (2) a read voltage, Vread, is applied to the selected word line, and (3) an off voltage, ground, is applied to the unselected string. These voltages are illustrated below:



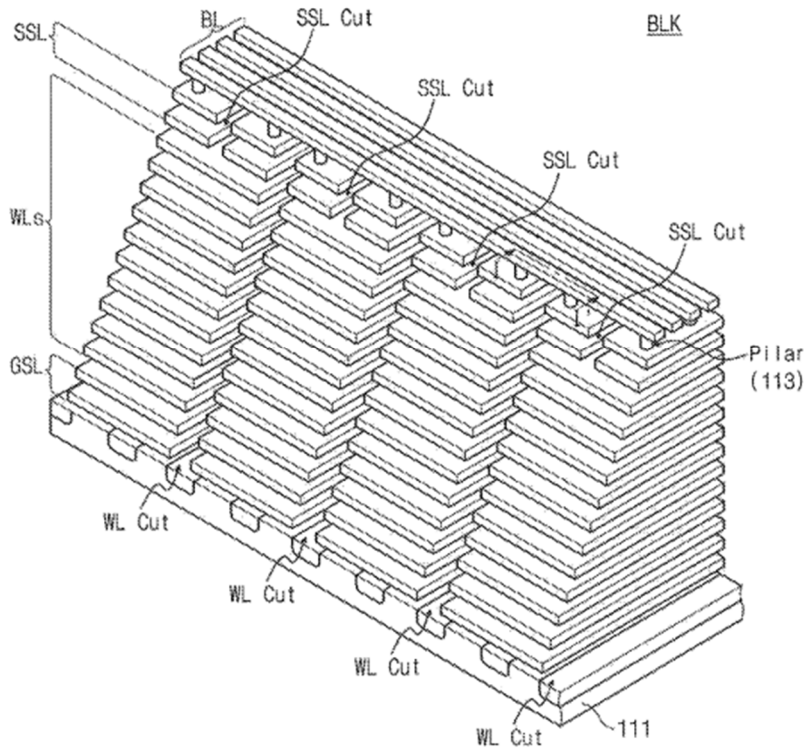
Id., FIGs. 8, 4 (annotated).

93. Seo's focus is on reducing HCI. But as I will describe in more detail in the claim mapping section, Seo's method also removes fast charges. The removal is a result of the electric field that Seo's read operation creates during t_1 . As shown above, it is the same field that the '342 patent states removes fast charges.

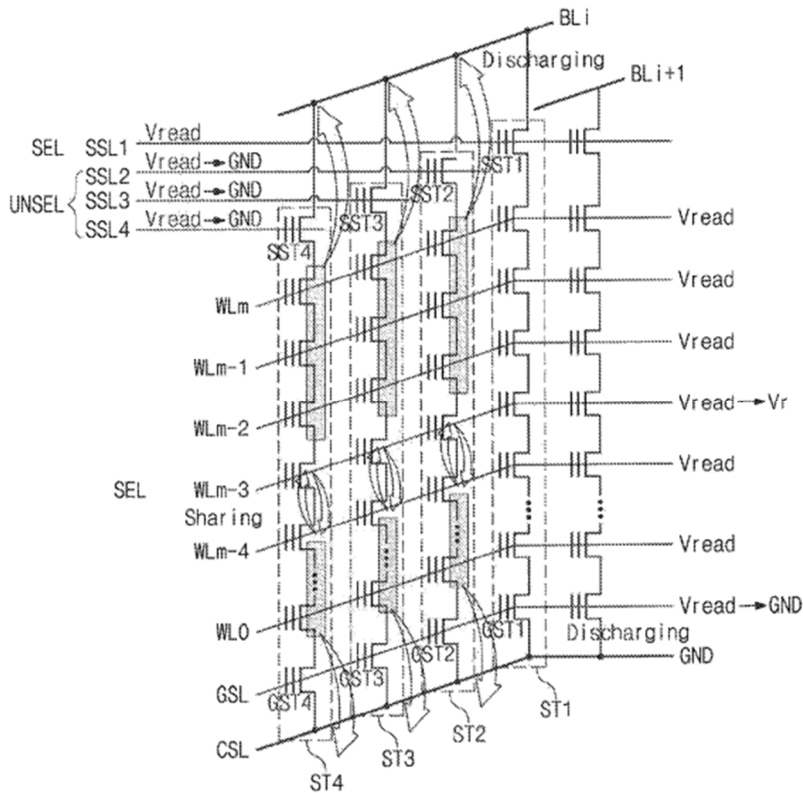
2. Nam

94. U.S. Patent Publ. No. 2015/0003169A1 ("Nam") was filed on April 1, 2014, and was published on January 1, 2015. Ex. 1006, Cover. I understand that Nam is prior art to the '342 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

95. Nam is also directed to read or verify operations of nonvolatile memory devices such as 3D NAND flash memory. Ex. 1006, Abstract, [0029], [0065], [0155].



Id., FIG. 2A. As shown above and below, Nam disclose a conventional 3D memory device.

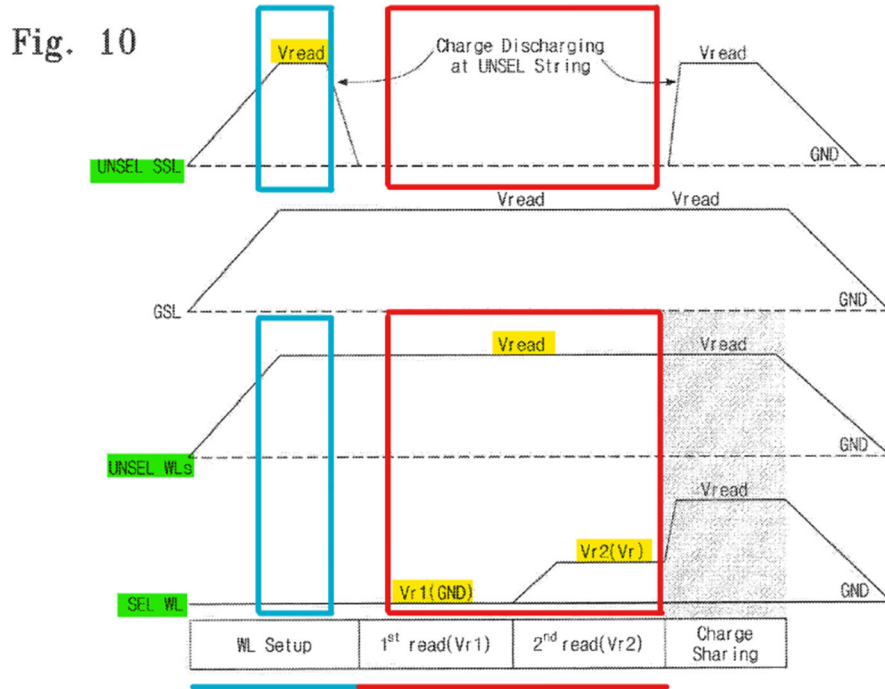


Id., FIG. 3.

96. Nam discloses immune disturbance read modes to control channel charges before and after read operations. Ex. 1006, [0070]. The need to control the channel charge before read operation is for discharging the excess charge stemming from channel boosting during the programming operation right before the read verify. The need to control the channel charge after the read operation is for discharging the negative charge, and the resultant negative potential, due to the effect of down coupling (when the voltage on the unselected word lines drop to GND from Vread after the read verify/sensing operation.)

97. Not controlling the channel charge before and after the read operation will result in the memory cell on an unselected string that shares the selected word line being subjected to HCI disturbance, due to the potential difference between the drain side and source side of such an unselected memory cell sharing the same selected word line but on an unselected string. Nam largely focuses on the charge-sharing phase after read operations to prevent disturbance.

98. There are two relevant time periods of Nam's operation. The first is WL Setup, which occurs before the sensing period. The sensing period is the 1st and 2nd read period. The sensing period consists of these two sub-periods because Nam's memory cells are multi-level cells and there are two sensing operations. As shown below, during WL Setup, (1) a high pass voltage, V_{read} , is applied to the unselected word line ("Unsel WLS"), (2) an off voltage, ground, is applied to the selected word line ("Sel WL"), and (3) a high prepare voltage, V_{read} , is applied to the unselected string ("Unsel SSL"). During the 1st and 2nd read period, (1) a high pass voltage, V_{read} , is applied to the unselected word line, (2) read voltages, V_{r1} and V_{r2} , are applied to the selected word line, and (3) an off voltage, ground, is applied to the unselected string.



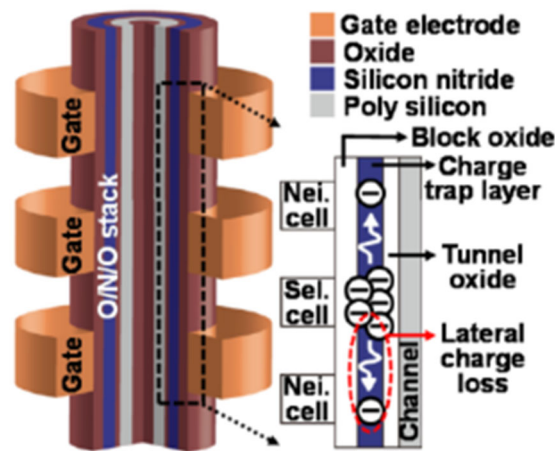
Ex. 1006, FIG. 10 (annotated). Nam's focus is post-reading activity. But as I will describe in more detail in the claim mapping section, Nam's method also removes fast charges. The removal is a result of the electric field that Nam's read operation creates during WL Setup. As shown above, it the same field that the '342 patent states removes fast charges.

3. Choi

99. Choi was presented at the IEEE 2016 Symposium on VLSI Technology Digest of Technical Papers. Ex. 1007; Ex. 1020, Ex. B. Choi was published online at IEEE Xplore on September 22, 2016. Ex. 1021. IEEE Xplore was well known by POSITAs in 2016. This Symposium is a prestigious annual event dating back decades and was also well known to POSITAs in 2016. This is evident from industry

discussion of the Symposium. Ex. 1020, Exs. A-B. Choi was publicly accessible and readily available to POSITAs well before 2019. Therefore, I understand that Choi is prior art to the '342 patent under 35 U.S.C. §102(a)(1) (AIA).

100. Choi presents an evaluation of fast-charge loss in 3D NAND Flash memory. Choi provides this discussion in the context of a charge trap memory structure. More specifically, the charge trap structure includes a cylindrical pillar (that is, the structure of a vertical memory string) wrapped in channel and ONO layers within an alternating metal-and-dielectric stack, as well as its graphical representation of fast-charge loss:



Ex. 1007, FIG. 1 (annotation in original). Note that the charge-trap material is the silicon nitride. The surrounding dielectric layers are the blocking and tunneling oxides.

101. Choi correlates “fast charge loss” with “early retention”: “fast charge loss within a few seconds, which is referred to as early retention.” Ex. 1007,

Abstract. Choi recognizes that fast-charge loss occurs within seconds of cell programming, and that reports indicate fast-charge loss causes undesirable drifts in threshold voltages of charge-trapping memory cells. *Id.*, 1:16-24. These drifts are undesirable because they can inadvertently alter the data state of memory cells.

102. Contrary to prior reports, Choi found that lateral fast-charge loss (i.e., in a direction parallel to the length of memory string through the shared charge trap layer) is the “primar[y]” mechanism of early retention (that is, fast-charge loss). Ex. 1007, 1:26-32, 2:48-52, 1:9-12. Choi explains that “a large lateral electric field is generated at the edge of the cell in which there is a greater chance for stored charges in a charge trap layer to spread laterally.” *Id.*, 2:16-18. “[T]he edge of the cell” refers to an interface with an adjacent cell, as Figure 1 above illustrates. Shallow traps exist at the edge of the cell, and the charge trap (storage) layers are shared between adjacent cells. Importantly, as mentioned earlier, the electric field between neighboring selected and unselected word line can extend into the charge storage layer, and Choi teaches that a large lateral electric field can de-trap fast charges in the charge trap layer.

103. Choi found that early retention, i.e., fast-charge loss, with its accompanying threshold-voltage shift, can occur “immediately after programming.” Ex. 1007, 1:20-24. Accordingly, Choi’s evaluation of fast-charge loss begins within a few seconds of the program operation. *Id.*, 1:50-55. Note that Choi’s observation

regarding the timing of fast-charge loss raises the issue of what normally happens right after a program operation, namely, a read operation. *See* §VI.B. Thus, the fast-charge loss would occur during and after this read operation, and the read operation should account for this fast-charge loss issue.

104. Choi's evaluation is illustrated in Figure 2 of Ex. 1007. The target V_t right after programming is significantly shifted within just a few seconds, due to the observed fast charge loss in a lateral direction. This shift in V_t would result in convolution of the stored data state and result in data error. As is evident from the discussion below, were the verify operation to occur before the shift, the verify will be successful (e.g., as shown below, PV3). But then after the fast charge loss (the shift), the data state will shift to an incorrect state (PV2). In sum, this fast charge loss creates a problem when verifying the data state, because the threshold value that is being verified might change.

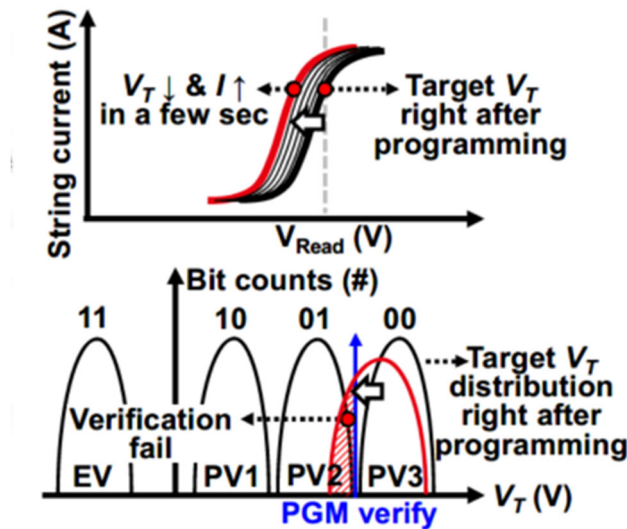
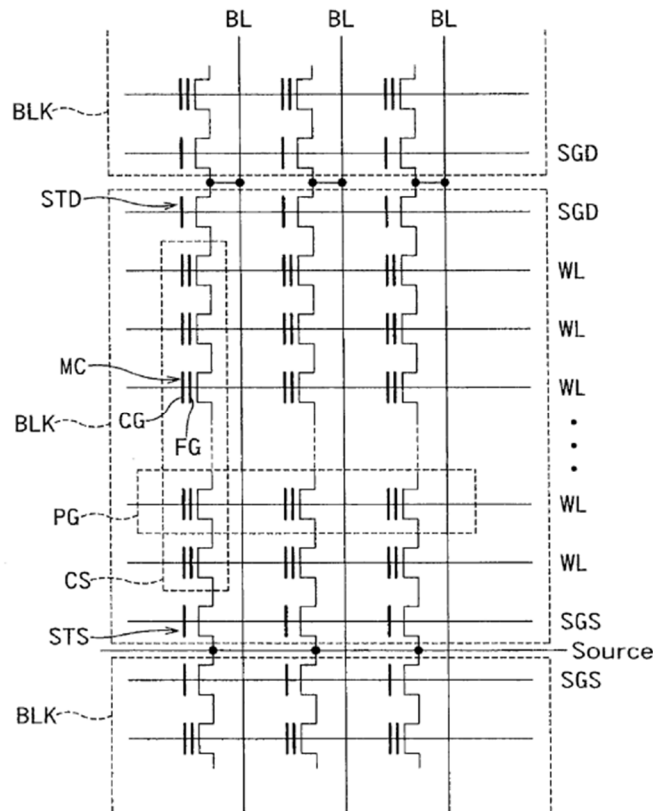


Fig. 2. Schematic of the early retention and its effect on V_T and I . The early retention threatens the MLC capability and the tight V_T distribution.

4. Izumi

105. U.S. Patent Publ. No. 2012/0151301A1 (“Izumi”) was filed on July 5, 2011, and was published on June 14, 2012. Ex. 1008, Cover. I understand that Izumi is prior art to the ’342 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

106. Izumi relates to read operations of nonvolatile charge-storage memory devices such as NAND flash memory. Ex. 1008, Abstract, [0003], [0018], [0041].



Id., FIG. 2. Note that practically speaking, all non-volatile memories require error-correcting-code circuitry to correct bits, because such memories include memory cells that will fail. A non-volatile memory cell is known to have an endurance level that represents an average number of accesses before the cell fails. Izumi recognizes the excessive power consumption of the conventional error-correcting-code (“ECC”) approach. *Id.*, [0003]-[0004]. Izumi reduces power consumption by selectively activating one or two ECC circuits having different error-correcting capabilities. *Id.*, Abstract, [0082]-[0083]. During read-verification operations, Izumi’s method counts the number of failed bits, which determines the ECC circuitry that it must activate. *Id.*, [0077], [0081], [0084].

B. Ground 1: Claims 1-6, 8-14, and 16-20 Are Obvious Over Seo in View of Choi

107. In my opinion, a POSITA would have considered Seo and Choi to be within the scope of the prior art and highly relevant to the patentability of the '342 patent's claims.

108. In my opinion, Seo in view of Choi and the knowledge of a POSITA renders claims 1-6, 8-14, and 16-20 obvious.

1. Claim 1

[1.Pre] “A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:”

109. In my opinion, to the extent the preamble is limiting, Seo discloses, or at least renders obvious, the preamble.

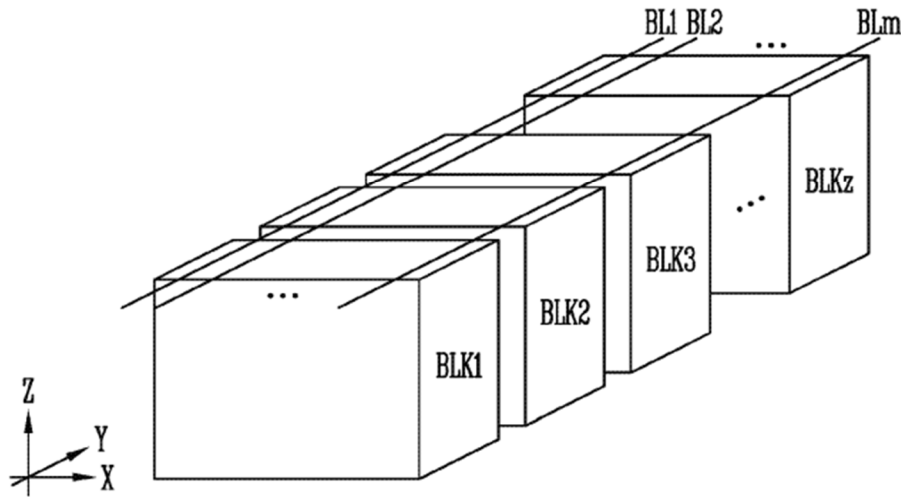
110. Seo teaches a method of reading a “[*m*]emory device” that “includes a *memory cell* array” (Ex. 1005, Abstract),¹ which is “*three-dimensionally* structured.” *Id.*, [0050].

111. Seo discloses: “Flash memory may be classified into NOR-type memory and NAND-type memory.” Ex. 1005, [0004]. And Seo further discloses: “Flash memory devices may be classified into two-dimensional semiconductor devices, in which memory strings are horizontally formed on a semiconductor substrate, and *three-dimensional semiconductor devices*, in which memory strings

¹ Emphasis added unless otherwise noted.

are vertically formed on a semiconductor substrate.” *Id.*, [0006]. As shown below, Seo depicts its embodiments as three-dimensional semiconductor devices. Thus, Seo discloses 3D Flash memories.

FIG. 2



Id., FIG. 2.

112. As with virtually any memory, these “memory cells” are “**read**” by a “**read operation.**” Ex. 1005, Abstract; [0072]. Seo’s read operation involves “appl[ying]” a “read voltage V_{read} ” “to a selected word line” labeled “Sel WL.” *Id.*, [0090]. This read voltage is used to determine the threshold voltage of the memory cell. The target memory cell (also known as the selected memory cell) is located at the intersection of the selected word line and the selected memory string. *Id.*, FIG. 5; §VI.A-B. Note that bit lines connect to the memory strings. *Id.* Thus, as with

conventional memories, a memory cell is selected using a word line and bit line. Thus, Seo discloses *[a] method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device.*²

113. Seo would have been understood to disclose its read operation for verification for two reasons.

114. First, Seo discloses its read operation in the abstract. Ex. 1005, [0086]-[0090]. A fundamental use of a read operation was for verification after a program. *See* §§VI.B, IX.B.19. In fact, every program operation involves at least one read operation (a program operation may involve multiple read operations if the program operation uses incremental pulses). *Id.*

115. Second, Seo discloses devices that would implement its read operation, and Seo specifically refers to “program operations” in those devices. Ex. 1005, [0108]. A POSITA would have understood that these program operations involve read operations to verify. *See* §VI.B.. As I discuss, ISPP involves cycles of pulse and read (verify). *Id.* Thus, by Seo disclosing a program operation, Seo would have been understood to disclose using its read to verify. A verify simply sets the read voltage (see limitation [1.B]) to the programming target voltage to ensure the programming pulse(s) successfully programmed the memory cell.

² For clarity, I use red italics for claim language.

116. In sum, a POSITA would have understood Seo's read operations are applicable to a verify operation from the discussion of a read operation in the abstract (as Seo describes the read operation) and certainly would have understood the read operation applicable to a verify operation from Seo's express mention of program operations in the context of describing its read operation.

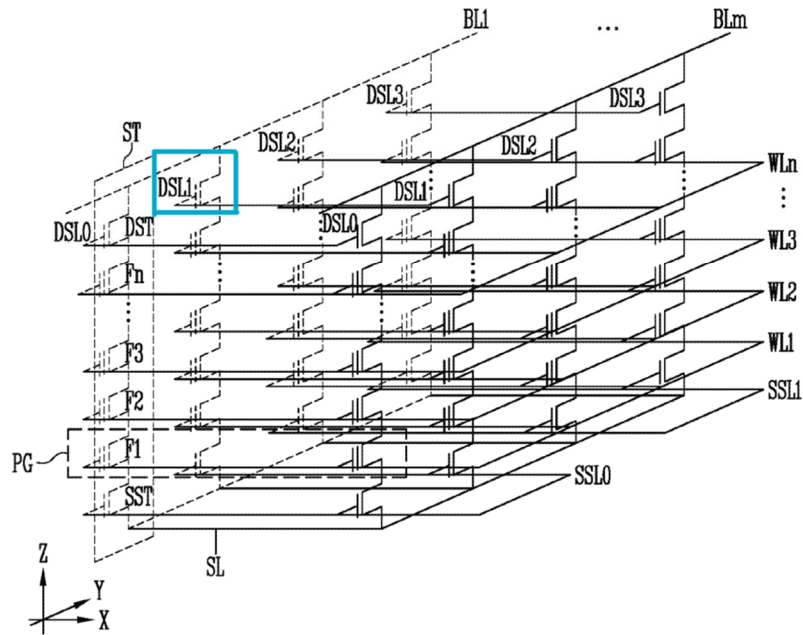
117. In addition, it is my opinion that employing Seo's read to verify would have at least been obvious in view of Choi for several reasons. *See* Ex. 1007, FIG. 2 (verification), §IX.B.19.

[1.A] “applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period”

118. Seo discloses this limitation.

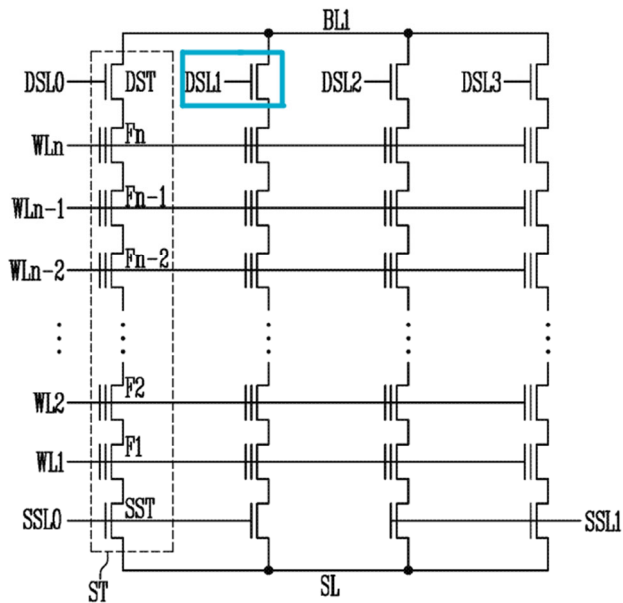
119. Seo discloses “drain select transistor” (“DST”), to which a “drain select line[]” (“DSL”) connects, and each of the DST is a *top select gate of a ... memory string*. Ex. 1005, [0048], [0055]. This is a conventional component of a 3D memory string. *See* §VI.A.

FIG. 3



Id., FIG. 3 (annotated).

FIG. 4

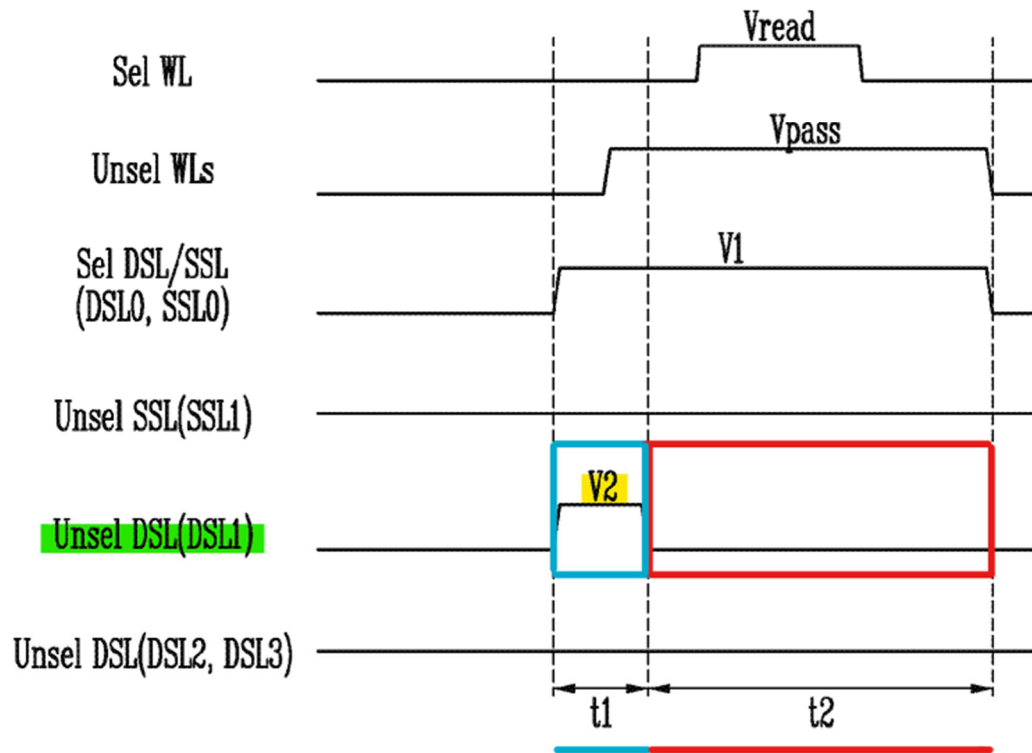


Id., FIG. 4 (annotated).

120. Figure 8, shown below, illustrates a read operation. Ex. 1005, [0086]. t1 corresponds to *a first time period* and t2 corresponds to *a second time period*. The t2 period is the actual sensing phase of the read operation (the period that senses the threshold value of the target memory cell), and t1 is, in effect, a period that prepares for the sensing operation. I describe in limitation [1.D] that t1 accomplishes the fast charge removal.

121. As part of the read operation, during t1, a “voltage V2”—the *prepare voltage*—is *applied* to “DSL1” that “correspond[s] to the unselected memory string.” Ex. 1005, [0088]. This voltage turns on DSL1 (meaning the voltage is above the threshold level of the cell or transistor at that level of the memory string). *Id.* Seo’s voltage V2 performs the function of the *prepare voltage*: turning on a corresponding transistor. Ex. 1001, 12:56-62. The voltage application on an unselected DSL occurs *during the first time period* (“t1”). *During*, according to the plain language, means at a point in the course of (here, t1). Next, a low voltage, e.g., ground (Vss) is applied—*an off voltage*—*during a second time period* (“t2”). Ex. 1005, [0075], [0088]-[0089]. An *off voltage* turns off a transistor and is typically 0 volts. This is consistent with the ’342 patent. Ex. 1001, 2:25-27.

FIG. 8



Ex. 1005, FIG. 8 (annotated).

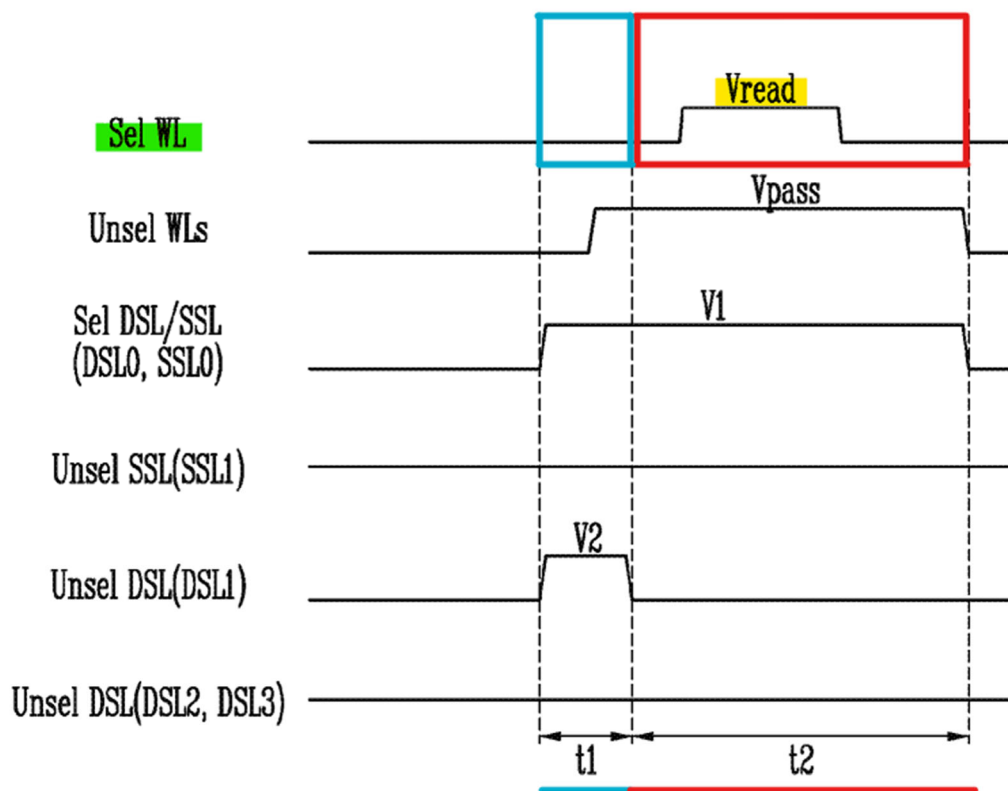
122. Thus, Seo discloses *applying, on an unselected top select gate of an unselected memory string* (e.g., Unsel DSL (DSL1)), *a prepare voltage during a first time period* (e.g., $V2$ during $t1$) *and an off voltage during a second time period* (e.g., off voltage during $t2$).

[1.B] “*applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period;*”

123. Seo discloses this limitation.

124. As shown below, a zero voltage—an *off voltage*—is applied to a *selected word line* (“Sel WL”) during “t1” (the *first time period*). Ex. 1005, [0088]-[0090]. Again, an *off voltage* turns off the memory cell. Then, the “*read voltage* *V_{read}* may be *applied*” during “t2” (the *second time period*). Ex. 1005, [0090]. The *read voltage* is used in Seo to measure the *target cell’s* threshold voltage.

FIG. 8



Id., FIG. 8 (annotated).

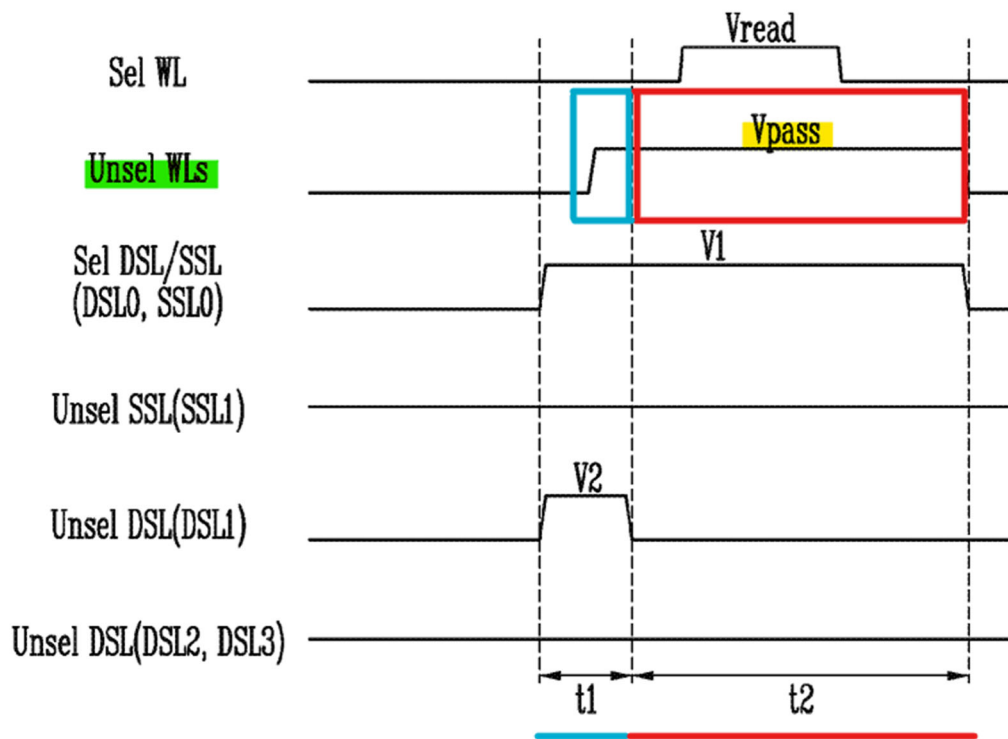
125. Thus, Seo discloses *applying, on a selected word line associated with the target memory cell* (e.g., Sel WL), *the off voltage during the first time period* (0 volts during t1) *and a read voltage during the second time period* (V_{read} during t2).

[1.C] “applying, on an unselected word line, a pass voltage during the first time period and the second time period,”

126. Seo discloses this limitation.

127. Seo discloses that a “**pass voltage** V_{pass} ” is applied to “**unselected word lines**” (“Unsel WLS”) during the **first** and **second time periods**, t_1 - t_2 . Ex. 1005, [0082], [0083], [0089]. **Unselected word lines** are word lines that do not include the target memory cell to read. V_{pass} means a pass voltage, and that voltage turns on the memory cells.

FIG. 8



Id., FIG. 8 (annotated); *see also id.*, [0089].

128. Thus, Seo discloses *applying, on an unselected word line* (e.g., Unsel WLs), *a pass voltage during the first time period and the second time period* (e.g., V_{pass} during t_1 and t_2).

[1.D] “wherein the read-verification operation removes fast charges of the target memory cell during the first time period”

129. Seo discloses this limitation or, at a minimum, renders it obvious in view of Choi.

130. The '342 patent discloses its *read-verification operation* in the context of charge-trap memories. Charge-trap memories include a continuous charge-trap material that runs vertically through a memory string. *See* §VI.A. Charge-trap memories experience the fast-charge loss issue because of this continuous layer. Choi discusses this. Ex. 1007.

131. In this context, the '342 patent discloses that “[r]emoving the fast charges of the target memory cell includes applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).” Ex. 1001, Abstract. In other words, the '342 patent states that applying these voltages removes fast charge. As §§IX.B.1[1.A]-[1.C] demonstrate, Seo discloses these voltages. Specifically, Seo teaches having a higher voltage on

unselected WLs (including WLs adjacent to the selected WL) relative to the selected WL *during the first time period*. §§IX.B.1[1.A]-[1.C]. This set of bias conditions conforms precisely to the specification in the ‘342 patent, which states that the electric field between the neighboring selected and unselected word line can extend into the charge storage layer film. Ex 1001, 12:24-34. The electric field can generate an electric force on the fast charges captured in the storage layer. The electric force can de-trap the fast charges from the shallow traps, pulling them towards the neighboring unselected memory cell. The fast charges can then be recombined with charges of opposite sign or be removed through the conductive path in the channel. In short, this voltage differential creates a lateral electric field and results in the lateral movement of the fast charges from a selected cell to the neighboring cells. *See* §IX.A.3.

132. Seo would have been understood to disclose charge-trap memories.

133. First, Seo discloses that its read operation is for a 3D Flash memory device. *See* §IX.B.1[1.Pre]. Charge-trap memory is a type of 3D memory device. Ex. 1017, 101. As to 3D Flash memory, the two basic types were conductive floating gate and charge-trap. *Id.*, 101, 144. Indeed, charge-trap memories were incredibly popular at the time of the alleged invention, and the basics of a charge-trap memory were textbook-level material. Charge-trap memories improve “power and reliability.” *Id.*, 101.

134. Second, Seo discloses that it is “directed to a memory device capable of improving a disturb phenomenon of an unselected memory string during a read operation.” Ex. 1005, [0008]. Charge trap memories suffer from the “disturb phenomenon” that Seo specifically addresses. Ex. 1017, 101, 108. Thus, a POSITA would have viewed Seo’s disclosures as applicable to charge-trap memories, because Seo is addressing a problem of charge-trap memories.

135. Third, a POSITA in leveraging the teaching of Seo would look to other teachings of Seo at around the time of Seo’s patent publication for possible guidance in applying Seo’s teaching. Indeed, there is another patent publication from Seo, filed before the Effective Filing Date of the ’342 patent, with a foreign filing date of July 23, 2019. Ex. 1027 (U.S. Patent Publ. No 2010/0395372A1). This Seo reference expressly references “charge trap film.” *Id.*, [0053]. This publication gives credence in framing Seo within the context of charge trap memories.

136. Thus, a POSITA would have understood that Seo discloses performing its read operation on charge-trap memories. More specifically, a POSITA would have immediately understood from reading Seo that Seo is disclosing its read operation as applicable to Flash memories, including Flash charge-trap memories. And as the ’342 states, Seo’s operation would remove fast charges in a charge-trap memory. Ex. 1001, Abstract.

137. To the extent that one were to argue that Seo does not disclose a “charge-trap” memory or removal of “fast charges,” I disagree for the reasons above. Regardless, Seo in view of Choi renders obvious claim [1.D]. Specifically, in view of Choi, a POSITA would have found employing Seo’s read operation in a 3D charge-trap memory obvious and would have known Seo’s read operation removes fast charges.

138. Choi specifically discloses a “3-D NAND flash memory with a charge trap layer.” Ex. 1007, 1:16-17. Choi observes the issue of “early retention (fast charge loss within a few seconds)” “originates from the lateral charge loss through the shared charge trap layers.” *Id.*, Title, 1:10-11. Choi discloses that an electric field parallel to the memory-string pillar induces charge loss from shallow traps after cell programming. *Id.*, 1:2-12, 2:13-38. “[S]hallowly trapped electrons” are more likely to be lost due to lateral movement when “a large lateral electric field is generated at the edge of the [memory] cell,” i.e., near the interfaces with adjacent cells. *Id.*, 1:28-29, 2:4-25, FIG. 1. The lateral electron movement from the selected memory cell to its neighboring memory cells (labeled “[l]ateral charge loss” though appearing vertically in the figure due to the orientation of the memory string) is shown below:

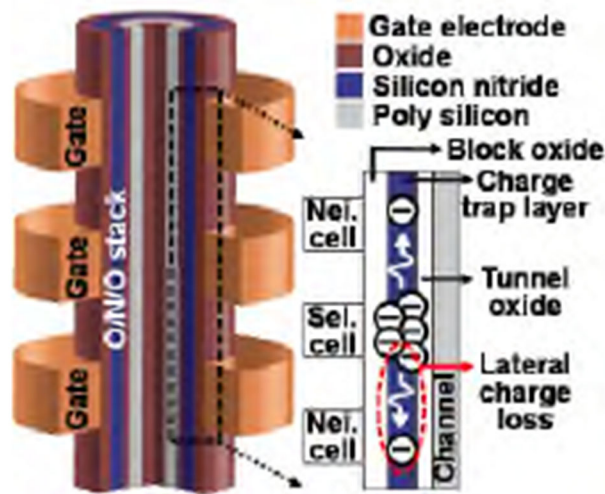


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Id., FIG. 1 (annotation in original). Seo creates such “a large lateral electric field” during the first time period t1 of the read operation (as I describe above, and as the ’342 recognizes, the voltage differential between the adjacent, unselected WL and selected WL during t1 creates the electric field that de-traps the fast charges). Accordingly, it would have been obvious to employ Seo’s read operation in Choi’s charge-trap memory with Choi’s express disclosure of removing fast charges. *See* §IX.B.19.

139. Accordingly, Seo discloses, or at least in view of Choi renders obvious, *wherein the read-verification operation removes fast charges of the target memory cell during the first time period* (e.g., voltage differential on the WLs during t1

creates an electric field that removes charges from charge-trap memory cells). As I explain above, Seo's read operation creates an electric field that removes fast charges, and fast-charge loss happens within a few seconds of programming. Choi, 1:2-5. Verification follows immediately after a program. Thus, Seo's read operation, when used for verification, removes fast charges.

2. Claim 2

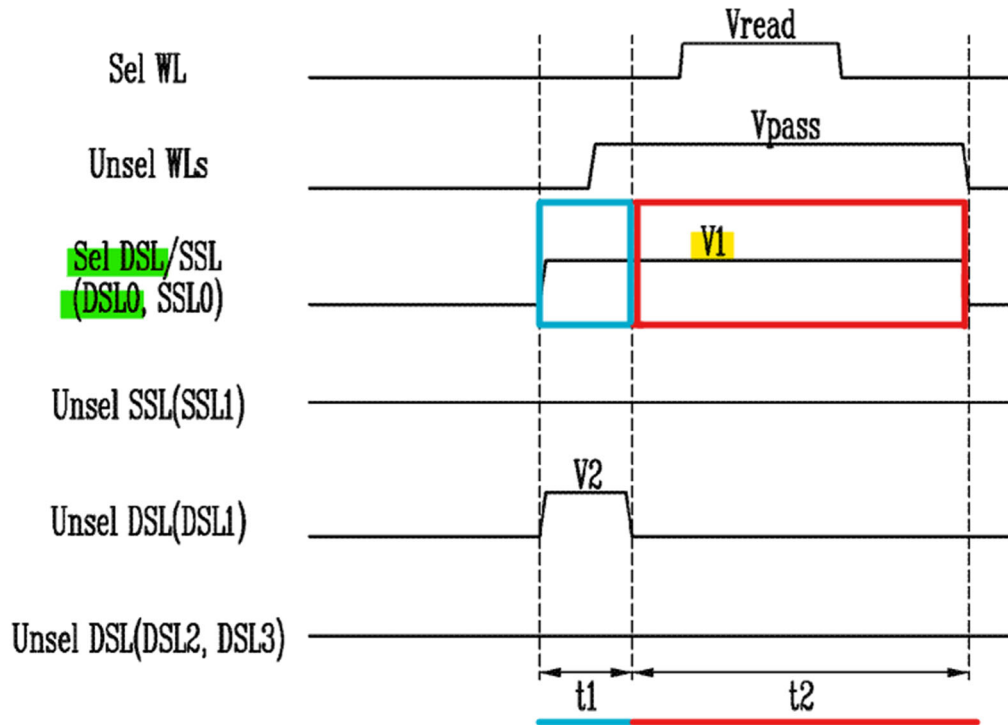
140. Claim 2 depends from claim 1 and further requires:

[2.A] “applying, on a selected top select gate of a selected memory string containing the target memory cell, a top select gate voltage during the first time period and the second time period;”

141. Seo discloses this limitation.

142. Seo's DSLs connect to the *top select gate[s]* (DSTs). See Limitation [1.A]; Ex. 1005, [0074]. *During the first time period and the second time period*, a “voltage V1 may be applied” to “DSL0” that “correspond[s] to [the] selected memory string ST.” *Id.*, [0088].

FIG. 8



Id., FIG. 8 (annotated). $V1$ turns on the transistor. *Id.*, [0088]. This means that the $V1$ voltage is above the transistor's threshold voltage. This is consistent with the '342 patent. Ex. 1001, 2:9-12, 11:11-27.

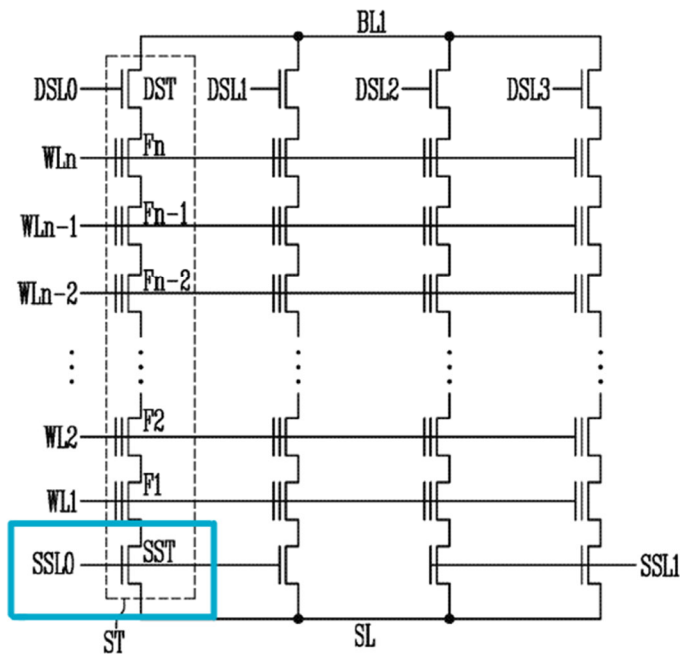
[2.B] “applying, on a lower select gate of the selected memory string containing the target memory cell, a lower select gate voltage during the first time period and the second time period.”

143. Seo discloses this limitation.

144. Seo discloses “source select transistor[s]” (each a “SST”), i.e., *lower select gate[s]*, to which “source select line[s]” (“SSL”) connect. Ex. 1005, [0055].

Note that in Seo, the drain side is the top of the memory string, and the source side is the bottom of the memory string.

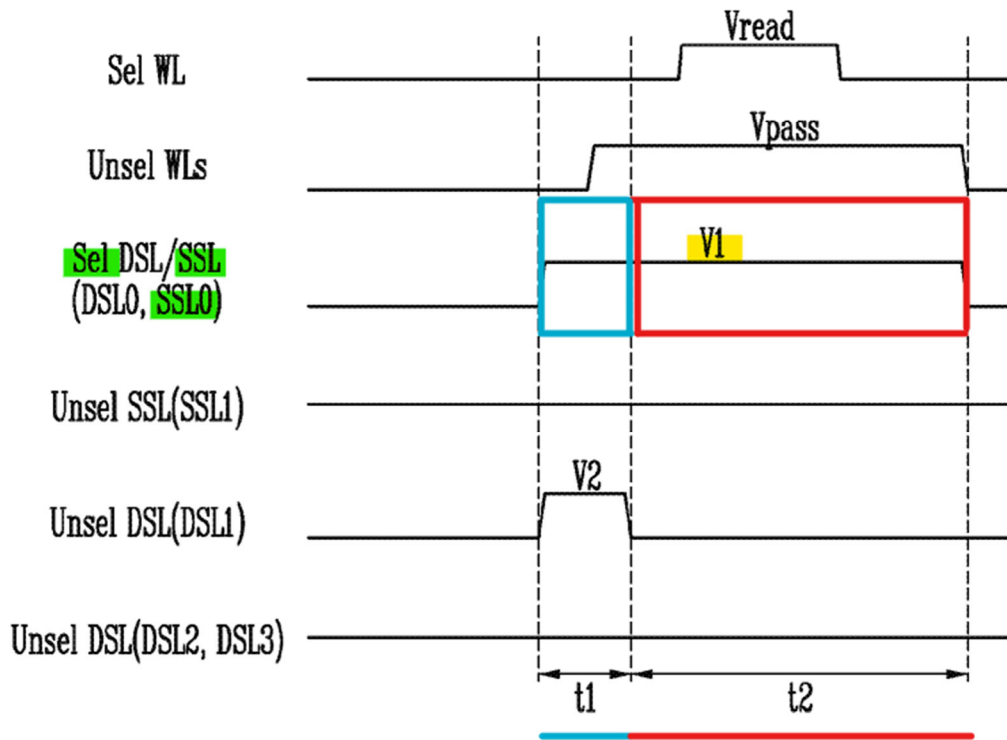
FIG. 4



Id., FIG. 4 (annotated).

145. *During the first time period and the second time period*, a “voltage V1” is applied to “the first source select line SSL0” that “correspond[s] to [the] *selected memory string* ST” (“Sel SSL”). Ex. 1005, [0088]; *see also id.*, [0079].

FIG. 8



Id., FIG. 8 (annotated).

3. Claim 3

146. Claim 3 depends from claim 2 and further requires:

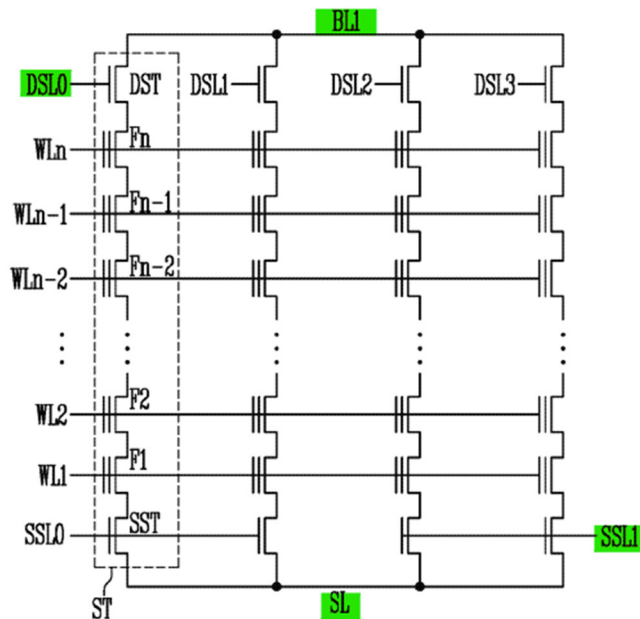
[3] “wherein the applying the top select gate voltage comprises electrically connecting the selected memory string to a bit line; and the applying the lower select gate voltage comprises electrically connecting the selected memory string to an array common source.”

147. Seo discloses this limitation.

148. Seo’s *top select gate* is DST, which is coupled to DSL. Limitation [1.A]. And the *lower select gate* corresponds to Seo’s SST, which is coupled to SSL.

Limitation [2.B]. The DSL turns on the top select gate transistor and couples the memory string to a “bit line,” and the SSL turns on the lower select gate transistor and couples the memory string to a common “source line.” Ex. 1005, [0038], [0055]. Recall that the bottom of the memory string is the source side, and thus connects to a source region (typically in the substrate).

FIG. 4



Id., FIG. 4 (annotated).

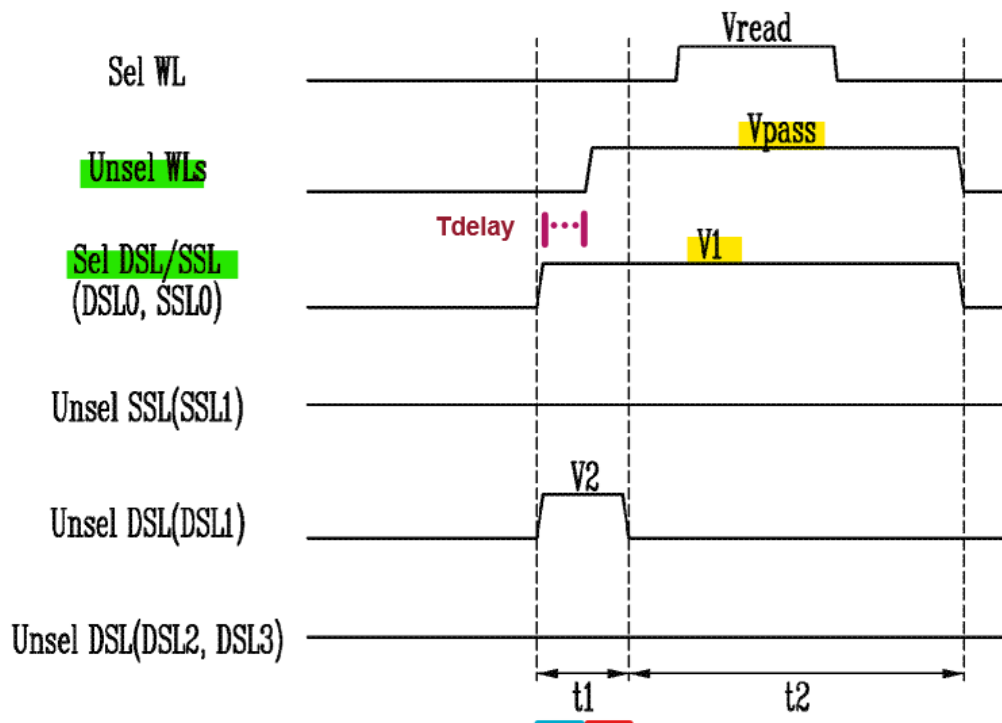
149. *[A]pplying the top select gate voltage (V1) electrically connect[s] the selected memory string (selected memory string ST) to a bit line (BL1); and the applying the lower select gate voltage (V1) comprises electrically connecting the selected memory string (selected memory string ST) to an array common source (SL).* Ex. 1005, [0088] (“The first voltage V1 may be a voltage to turn on the drain

select transistor DST and the source select transistor SST.”); Limitation [2.A, B], Ex. 1005, FIG. 8. As can be seen in the above figure, when the transistors turn on, the respective connections are made (*electrically connecting*).

150. As shown above, the “source line” is an *array common source* because the source is common to the array. Ex. 1005, FIG. 4, *see also id.*, FIG. 3. In practice, there is a common source region in the substrate. Seo’s common source is just like the *array common source* (446) of the ’342 patent.

153. Seo discloses *applying the pass voltage* on an unselected word line (V_{pass}) (which turns on the corresponding memory cells), and V₁ on both the *selected TSG* and selected *LSG* (which turns on the respective transistors DST and SST). Limitations [1.C], [2.A], [2.B]. This “V_{pass}” is “applied” “[s]ubsequently” to voltage V₁. As can be seen below, there is a *delay period* before V_{pass} is applied. Ex. 1005, [0089].

FIG. 8



Id., FIG. 8 (annotated).

5. Claim 5

154. Claim 5 depends from claim 1 and further requires:

[5] “measuring a threshold voltage of the target memory cell during the second time period.”

155. Seo discloses this limitation.

156. The '342 patent uses *measuring a threshold voltage of a target memory cell* to refer to a read operation. Ex. 1001, 10:60-11:3. A read operation measures a threshold voltage by determining whether the transistor will turn on at a particular voltage. Technically, this measurement determines whether the memory cell's threshold voltage is above or below a particular level (because the memory cell will “turn on,” i.e., form a conductive channel). *See id.* (describing how “[a]fter the read prepare step, the voltage bias on the ... (Sel_WL) can be reduced from ... $V_{prepare}$ to ... V_{read} to sense (i.e., read or measure) the threshold voltage V_{th} of the target memory cell.”) (emphasis added).

157. Seo discloses, or in view of Choi renders obvious, a *read-verification operation*. *See supra* limitation [1.Pre]. During this operation, Seo discloses measuring *a threshold voltage* by applying “Vread” “during a second time period t2” to “Sel WL,” which is connected to the target memory cell (*see* limitation [1.B]). Ex. 1005, [0090]. The period t2 is the sensing period in which the target cell is read. *Id.* This sensing operation determines whether the memory cell's threshold voltage is above or below Vread. *Id.*

6. Claim 6

158. Claim 6 depends from claim 1 and further requires:

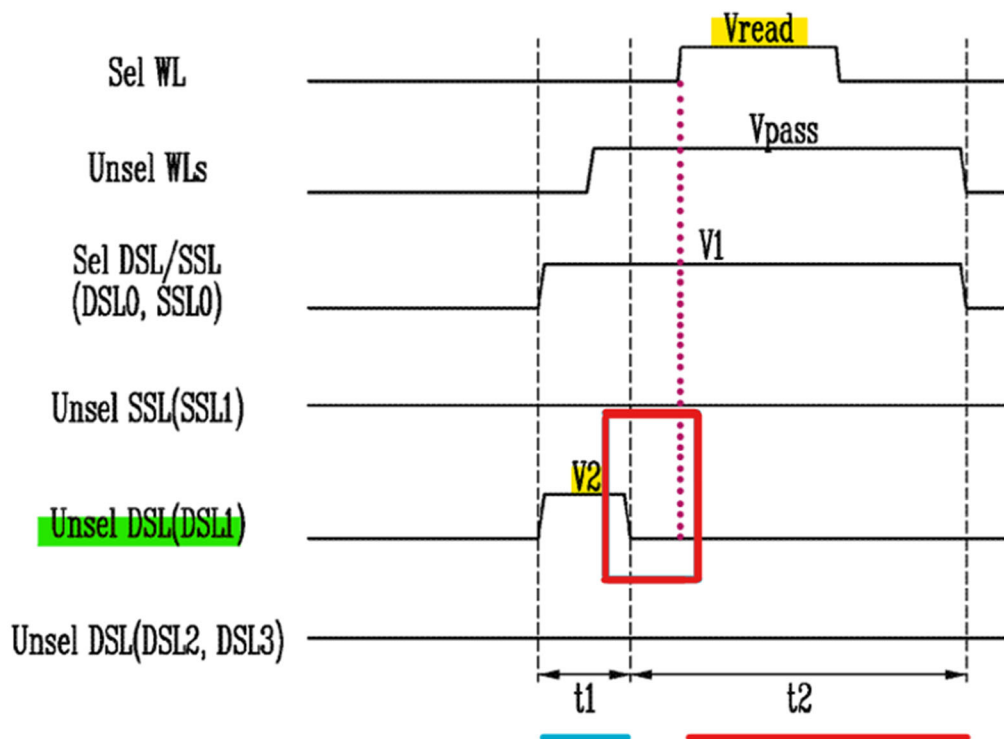
[6] “wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell”

159. Seo discloses, or at least renders obvious, this limitation.

160. Seo’s *read voltage* is V_{read} on Sel WL, and the voltage of the unselected top select gate is that of Seo’s Unsel DSL. *Supra* limitations [1.A]-[1.B].

Accordingly, this additional claim limitation refers to a point in time shown below:

FIG. 8



Ex. 1005, FIG. 8 (annotated).

161. As shown, when *applying the read voltage* occurs, the voltage on *the unselected top select gate* (Unsel DSL1) is 0V. Thus, Unsel DSL1 is *higher* (0V) than the *threshold voltage*—the voltage at which a transistor turns on—*of an unselected memory cell*. This is because *unselected memory cell[s]* may be erased. While programmed memory cells may have a positive threshold voltage, erased memory cells definitely have a negative threshold voltage. *See* §VI.B.

162. That other memory cells may be erased or programmed is clear, and certainly obvious, from Seo. As was well known, non-volatile memory cells may be in the erase state.

163. 3D flash memories include an erase operation that erases an entire block, i.e., an array that includes a plurality of memory strings. Ex. 1017, 91-93; *see also* Ex 1006, [0108] (recognizing “erase”). Thus, as the programming starts and fills up a block, there will necessarily be both erased and programmed unselected cells in the block.

164. In addition, typical programming in 3D memories involves programming from top to bottom or from bottom to top. Ex. 1024, [0115], [0130]. In other words, with a bottom to top approach, after erasing the block, the first row programmed is the lowest row of memory cells. The subsequent programs (until the last row is programmed) will involve a program operation in which there exists both unselected programmed and erased cells.

165. Each approach, bottom to top or top to bottom, was an obvious implementation of Seo. Again, such techniques were standard and well known. Ex. 1024, [0115], [0130]. They were beneficial, because with these approaches, one knows that either the rows above or below are programmed (and the other rows are erased). Thus, that known state is taken into account when attempting to mitigate issues relating to, for example, programming. In fact, a more advanced programming scheme can take advantage of the knowledge of the state of the neighboring cells to compensate for the parasitic effects and achieve a more uniform programming distribution. Ex. 1025, 8:18-53. Further, sequential program order simplifies controller decoding operation, since the address of the next page to be programmed in the sequence would not need to be fetched again from the controller once the programming operation commences. Finally, it would be necessary to implement a programming scheme for Seo's device, and these sequential programming schemes were well understood. Each approach was easily implementable, and simply involves using a pointer that increments either up or down. That each approach simply uses an incrementing pointer is another benefit, because this obviates the needs to track all the unprogrammed rows. In other words, that one pointer indicates all rows above or below are unprogrammed.

166. Thus, with either of these approaches, when performing the read on any but the top-most or bottom-most row, there would be unselected memory cells that

are erased and programmed. For example, programming from bottom to top, the memory cells of the rows below the selected word line will be programmed and the rows above the selected word line will be erased.

167. Thus, *an unselected memory cell*, e.g., an erased cell, will have a negative threshold voltage, and *a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell*.

7. Claim 8

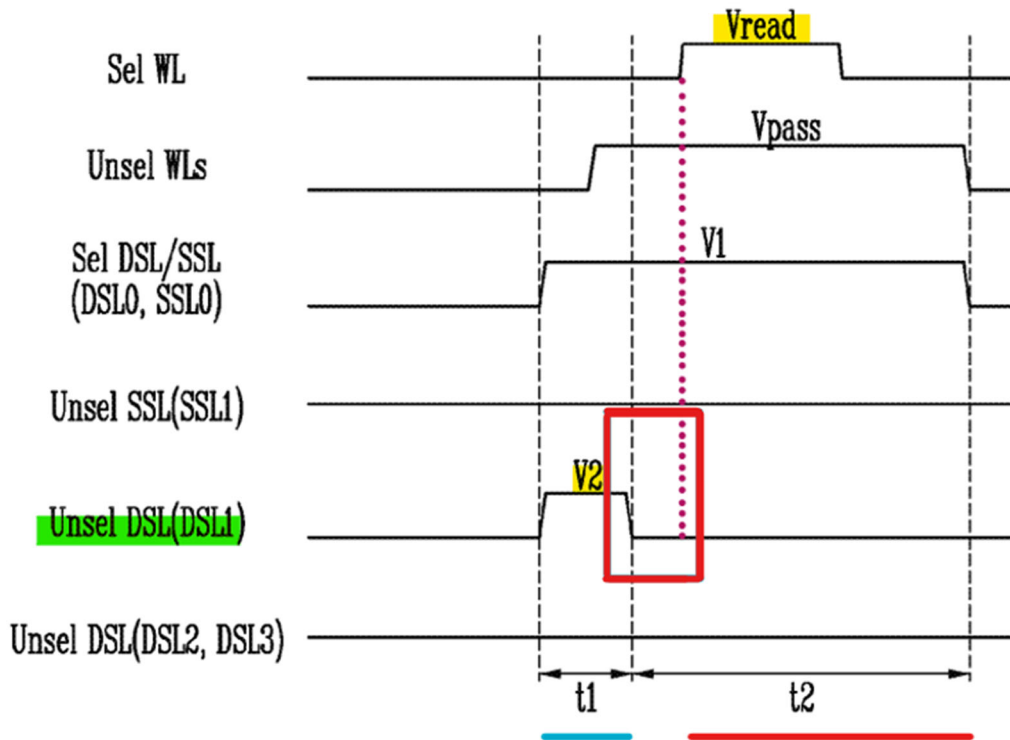
168. Claim 8 depends from claim 1 and further requires:

[8] “wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is lower than a threshold voltage of an unselected memory cell”

169. Seo discloses, or at least renders obvious, this limitation.

170. As described above, Seo’s *read voltage* is V_{read} on Sel WL, and the voltage of the unselected top select gate is that of Seo’s Unsel DSL. *Supra* limitations [1.A]-[1.B]. Accordingly, this additional claim limitation refers to the time period below:

FIG. 8



Ex. 1005, FIG. 8 (annotated).

171. As shown above, when *applying the read voltage* occurs, the voltage on *the unselected top select gate* (Unsel DSL1) is 0V. Thus, Unsel DSL1 is *lower* (0V) than the *threshold voltage*—the voltage at which a transistor turns on—*of an unselected memory cell* that is programmed to a high V_t data state. I explain why unselected memory cells will be either erased or programmed to a high V_t state in my analysis of claim 6 above.

8. Claim 9

172. Claim 9 depends from claim 1 and further requires that:

[9] “wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V”

173. A POSITA would have known that the purpose of Seo’s prepare voltage is to connect the unselected string to the bitline, so that the potential of the channel of the unselected string can be maintained.

174. Furthermore, a POSITA would have known the typical operation voltage on Seo’s select gate line is 4.5V during a read operation in order to ensure that the select gate transistor turns on to conduct current from the memory string. *See e.g.*, Ex. 1013, 333. This prepare voltage needs to be higher than a typical supply voltage, Vcc (3.3V), in order to account for the series resistance from the memory cell string. Thus, it would have been understood, and at least obvious, that Seo’s voltage, which turns on the transistor (see limitation [1.A]), is within the range of 4V to 7V.

TABLE 7.2 Operation conditions for the DC-SF NAND cells^a

Bias	Erase (V)	Program (V)	Read (V)
BL	0	0/V _{cc}	1
SGD	4.5	4.5	4.5
CG4	V _{erase} : -11	V _{pass2} : 2	V _{read} : 4
CG3	V _{erase} : -11	V _{pgm} : 15	0
CG2	V _{erase} : -11	V _{pgm} : 15	0
CG1	V _{erase} : -11	V _{pass2} : 2	V _{read} : 4
CG0	V _{erase} : -11	V _{pass1} : 4	V _{read} : 4
SGS	4.5	0	4.5
SL	0	V _{cc}	0

Id., Table 7.2.

9. Claim 10

175. Claim 10 depends from claim 1 and further requires that:

[10] “wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V.”

176. Seo’s pass voltage in this 3D memory context was ordinarily around 7V. By way of example, Nam uses such a conventional pass voltage. *See* §IX.D.9. Thus, it would have been understood, and at least obvious, that Seo’s voltage, which is a pass voltage (see limitation [1.D]), is within the range of 5V to 9V.

10. Claim 11

177. Claim 11 depends from claim 1 and further requires:

[11] “wherein applying the off voltage comprises applying a voltage about 0V.”

178. Seo discloses this limitation.

179. Seo discloses an *off voltage* of ground. Limitations [1.A, B]. Seo discloses: “The drain select line voltages (for example, V_{DSL2} and V_{DSL3}) of the

remaining unselected memory strings may be set to a ground voltage V_{ss} or a voltage lower than a threshold voltage of the drain select transistor DST.” Ex. 1005, [0075]. Ground (V_{ss}) is usually 0 volts. By stating that the turn off voltage could be less than the threshold, this implies that Seo is using 0 volts as ground (or it would at least have been obvious). It would have at least been obvious because ground is usually 0 volts, which is the industry standard. Indeed, unless there is a negative charge pump in the address decoder circuit, the lowest voltage, or the off voltage, that is supplied from the decoder circuit would be V_{ss} or ground, or a voltage of 0V. An example of ground as 0 volts is shown in Nam. *See* §IX.D.10.

11. Claim 12

180. Claim 12 depends from claim 1 and further requires:

[12] “wherein the removing the fast charges comprises: removing the fast charges from a storage layer of the target memory cell.”

181. Seo discloses this limitation, or in view of Choi, renders it obvious.

182. As my analysis under Limitation [1.D] demonstrates, Seo discloses, or in view of Choi renders obvious, a charge-trap memory device and the removal of fast charges. Such removal occurs in the storage layer, e.g., silicon nitride, of such a memory. Limitation [1.D]; Ex. 1007, Introduction. The silicon nitride stores the charges that change the memory cell’s threshold voltage. The shallowly-trapped charges are in this layer.

12. Claim 13

183. Claim 13 depends from claim 1 and further requires:

[13] “wherein the removing the fast charges comprises: removing electrical charges from shallow traps in the storage layer of the target memory cell.”

184. Seo discloses this limitation, or in view of Choi, renders it obvious.

185. As my analysis under Limitation [1.D] demonstrates, Seo discloses, or in view of Choi renders obvious, a charge-trap memory device and the removal of fast charges. Such removal occurs in shallow traps in the storage layer, e.g., silicon nitride, of such a memory. Limitation [1.D]; Ex. 1007, Introduction.

13. Claim 14

186. Claim 14 depends from claim 1 and further requires:

[14] “wherein the removing the fast charges comprises: removing the fast charges from the target memory cell to a neighboring unselected memory cell.”

187. Seo discloses, or at least renders obvious in view of Choi, this limitation.

188. As my analysis under Limitation [1.D] demonstrates, Seo discloses, or in view of Choi renders obvious, a charge-trap memory device and the removal of fast charges. Such removal involves the direction *from the target memory cell to a neighboring unselected memory cell*. Limitation [1.D]; Ex. 1007, 2:16-18 (“spread laterally”). Specifically, as shown below, the voltage differential in Seo’s read operation (between the adjacent and selected wordline) creates an electrical field,

driving the charges from target cell to a neighboring cell (which Choi refers to as “lateral charge loss”). Choi found this directional movement to be the dominant form of fast-charge loss. *See* §IX.A.3. The continuous layer of silicon nitride enables the directional movement.

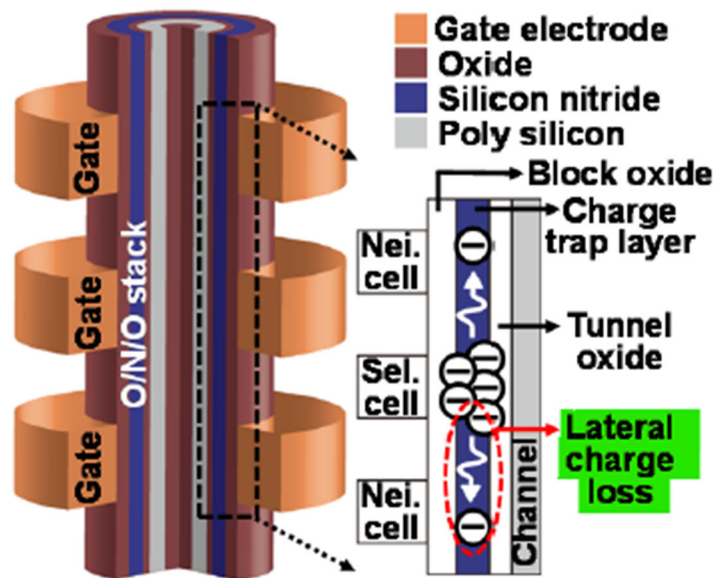


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Ex. 1007, FIG. 1 (green highlight added, other annotation in original).

14. Claim 16

189. Claim 16 is an independent claim and requires:

[16.Pre] “A three-dimensional (3D) memory device, comprising:”

190. In my opinion, to the extent this preamble is limiting, Seo discloses it.

Note that the preamble of claim 1 also recites *a three-dimensional (3D) memory device*. Ex. 1005, FIG. 2; [0050], §IX.B.1[Pre].

[16.A] “a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein:”

191. Seo discloses, or at least renders obvious in view of Choi, this limitation.

192. Seo’s memory device includes a *memory array, comprising a plurality of memory strings extending vertically*. Seo teaches that its “three-dimensional semiconductor devices” includes “memory strings” that “are vertically formed on a semiconductor substrate.” Ex. 1005, [0006], [0007], [0051]. Vertical memory strings refers to a 3D memory. See §VI.A.

193. Seo would have been understood to disclose a *film stack of alternating conductive and dielectric layers*. The alternating “stack” of gate and dielectric layers was a basic building block of 3D memory. Ex. 1013, 294-95. This stack provides the word lines (which are conductive) to select the rows of memory cells. The dielectric layers (which are typically an oxide) are necessary to insulate the gate layers from each other. A POSITA would have understood Seo’s 3D memory to

include such. This can also be seen in Seo Figure's 2 and Seo's reference to "stacked" "memory cells." Ex. 1005, [0051], FIG. 2. Implementing such a stack was routine and textbook-level knowledge.

194. Alternatively, Seo in view of Choi renders the *film stack* obvious. Choi shows a "device structure" of a "WL stacked tube-type" three-dimensional "NAND flash memory." Ex. 1007, FIG. 5, 1:41-43. The film stack comprises alternating SiO₂ and MG (metal gate) layers. *Id.*, FIG. 5. Metal is obviously conductive. And SiO₂ is a dielectric material.

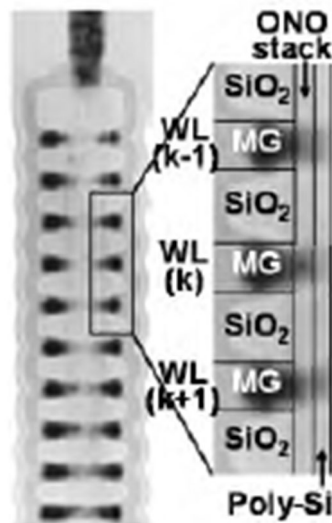


Fig. 5. TEM image of the tube-type 2y WL stacked 3-D NAND flash memory used in this work.

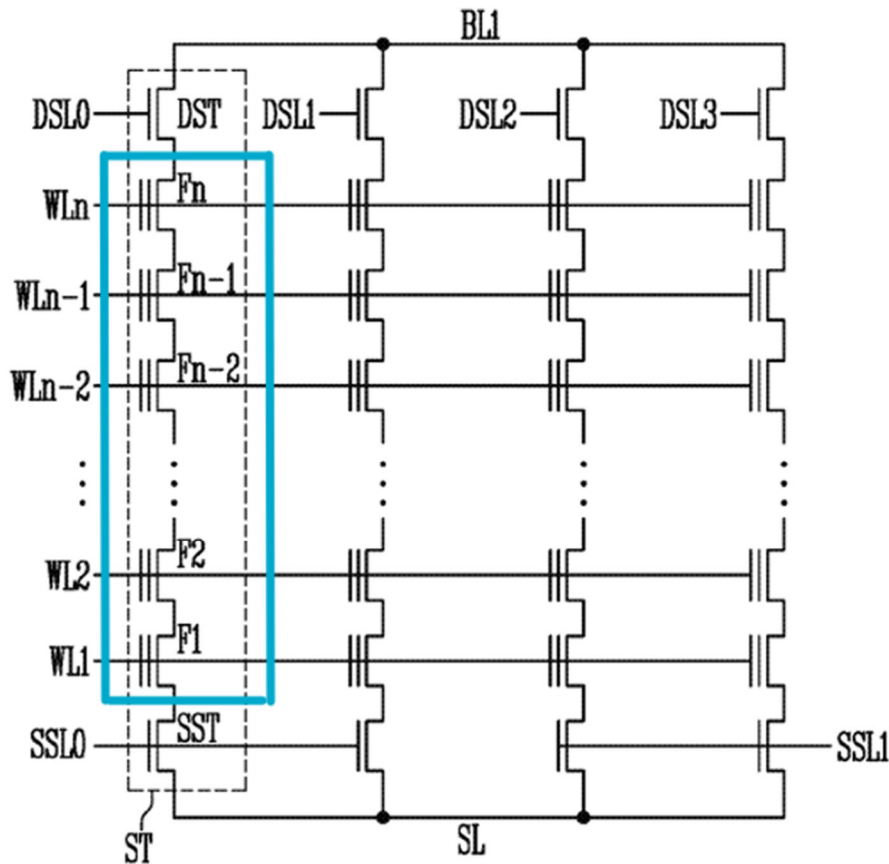
Id., FIG. 5; see IX.B.18 (motivation).

[16.A.i] “each memory string comprises a plurality of memory cells; and”

195. Seo discloses this limitation.

196. “Each of the plurality of **memory strings**” “may include...first to nth **memory cells** F1 to Fn[.]” Ex. 1005, [0062], [0007], [0055].

FIG. 4

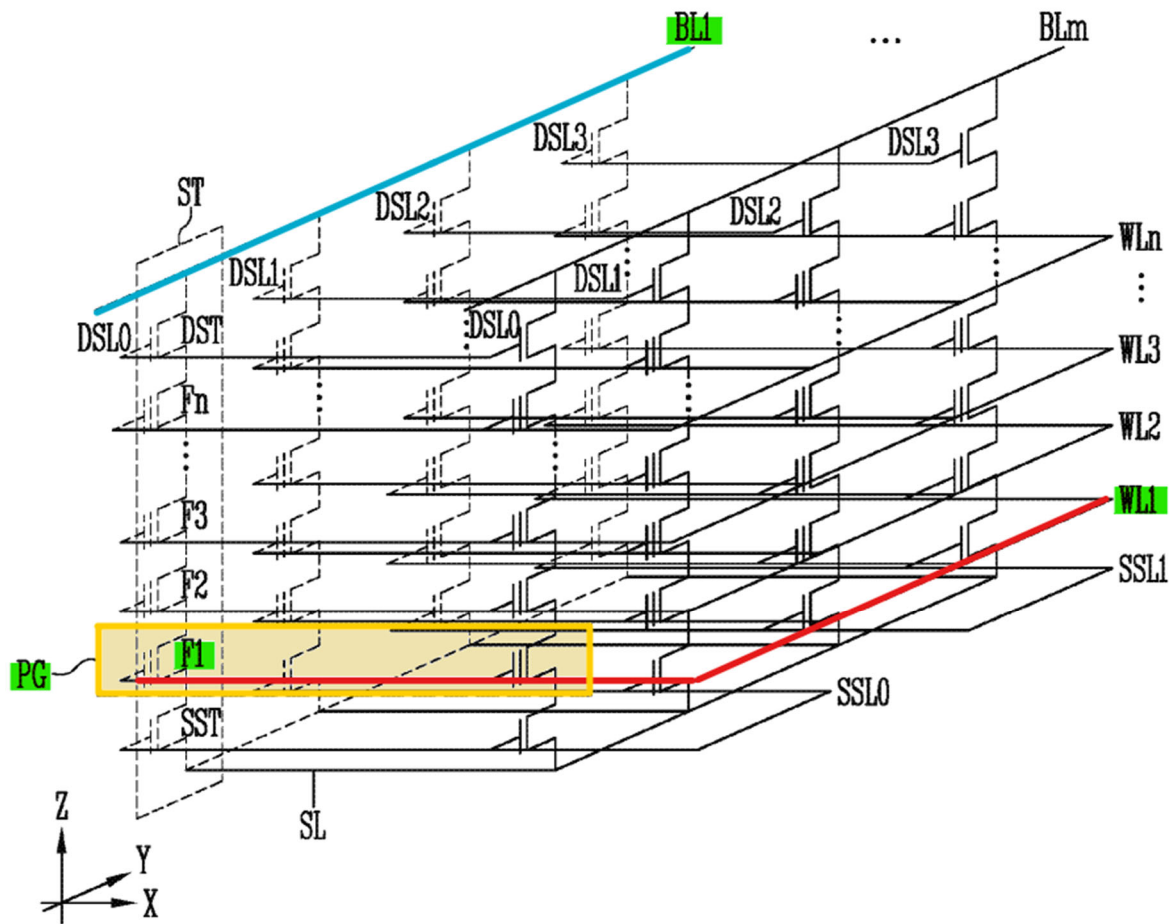


Id., FIG. 4 (annotated).

[16.A.ii] “each memory cell is addressable through a word line and a bit line; and”

197. Seo discloses this limitation.

198. Note that this limitation refers to the conventional addressing of a 3D memory. Seo equates word lines with pages (an addressable unit in an addressing scheme). Seo discloses selecting “a page and memory strings to perform the read operation.” Ex. 1005, [0073]. A page constitutes “memory cells coupled to the same word line in the first direction X among the strings ST coupled to the first bit line BL1 to the mth bit line BLm.” *Id.*, [0058]. Thus, selecting a page (*id.* [0073]) is selecting its corresponding *word line*. Within this page, a *bit line* is used to select the memory string (BL1 to BLm). *Id.*, [0044] (explaining that page buffers are coupled to the memory cell array through bit lines); [0074].

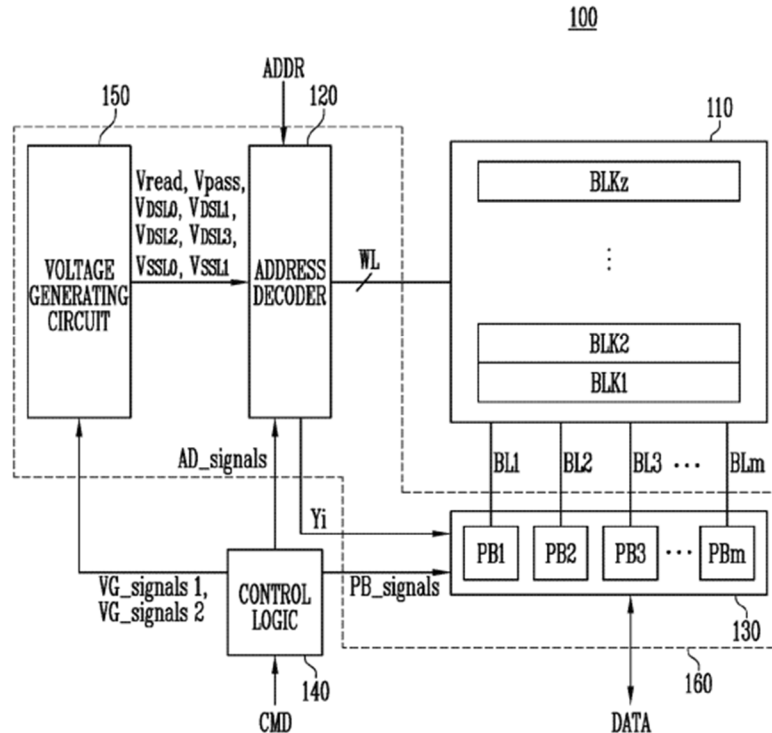


Id., FIG. 3 (annotated).

[16.B] “a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:”

199. The portion of the limitation that recites *a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation*, refers to the control circuitry that implements application of the various voltages of the claim. Seo discloses this circuitry in various functional blocks:

FIG. 1



Ex. 1005, FIG 1. The “control logic 140” sits at the highest functional level and controls other functional blocks, including the control of the voltages applied to the various array elements, and effectuates the read operation. *Id.*, [0047]. The voltage generating circuit would include voltage pumps or similar circuitry to generate the necessary voltages.

200. In Section IX.B.1[1.D], I demonstrate that Seo’s read operation is *for removing fast charges during a first time period in the first time period* (Seo’s t1).

[16.B.i] “apply, on an unselected top select gate of an unselected memory string, a prepare voltage during the first time period and an off voltage during a second time period”

201. This limitation is identical to Limitation [1.A] except for using “apply” instead of “applying,” and is met for the same reasons set forth therein.

[16.B.ii] “apply, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and”

202. This limitation is identical to Limitation [1.B] except for using “apply” instead of “applying,” and is met for the same reasons set forth therein.

[16.B.iii] “apply, on an unselected word line, a pass voltage during the first time period and the second time period”

203. This limitation is identical to Limitation [1.C] except for using “apply” instead of “applying,” and is met for the same reasons set forth therein.

15. Claim 17

204. Claim 17 depends from claim 16 and further requires:

[17] “wherein the circuit is further configured to: electrically connect a selected memory string containing the target memory cell to the bit line and an array common source by applying a top select gate voltage on a selected top select gate and applying a lower select gate voltage on a lower select gate during the first time period and the second time period.”

205. This limitation is substantively the same as claims 2 and 3. Here, the claim recites a *circuit* that performs the steps. As I discuss under limitation [16.B], Seo’s circuitry preforms these steps.

16. Claim 18

206. Claim 18 depends from claim 17 and further requires:

[18] “wherein to remove the fast charges of the target memory cell, the circuit is further configured to: apply the top select gate voltage on the selected top select gate and the lower select gate voltage on the lower select gate before applying the pass voltage on the unselected word line.”

207. This additional limitation is substantively identical to that of claim 4 and met for the same reason in my analysis under claim 4.

17. Claim 19

208. Claim 19 depends from claim 16 and further requires:

[19.A] “a channel hole”

209. Seo in view of Choi renders this limitation obvious.

210. Choi’s “tube-type” three-dimensional “NAND flash memory” has the *channel hole*. The ’342 patent uses channel hole to refer to the cavity through the stack in which the string is formed. Ex. 1001, 6:46-64.

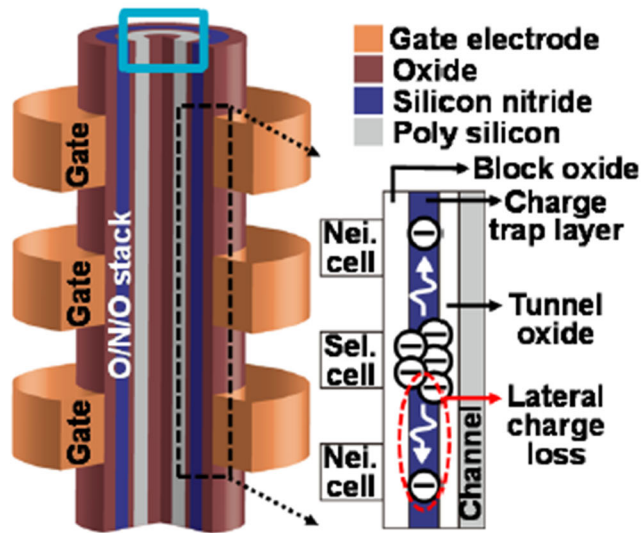


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Ex. 1007, FIG. 1 (annotated).

[19.B] “a core filling film in a center of the channel hole;”

211. Seo in view of Choi renders this limitation obvious.

212. There is a *core filling film* in Choi’s *channel hole* (i.e., oxide, with polysilicon surrounding it) in the center below. This is known as a core filler.

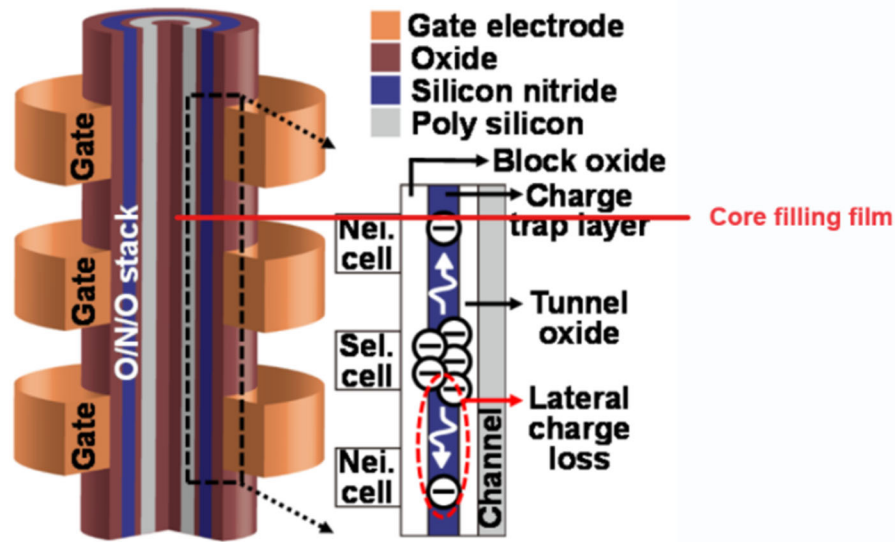


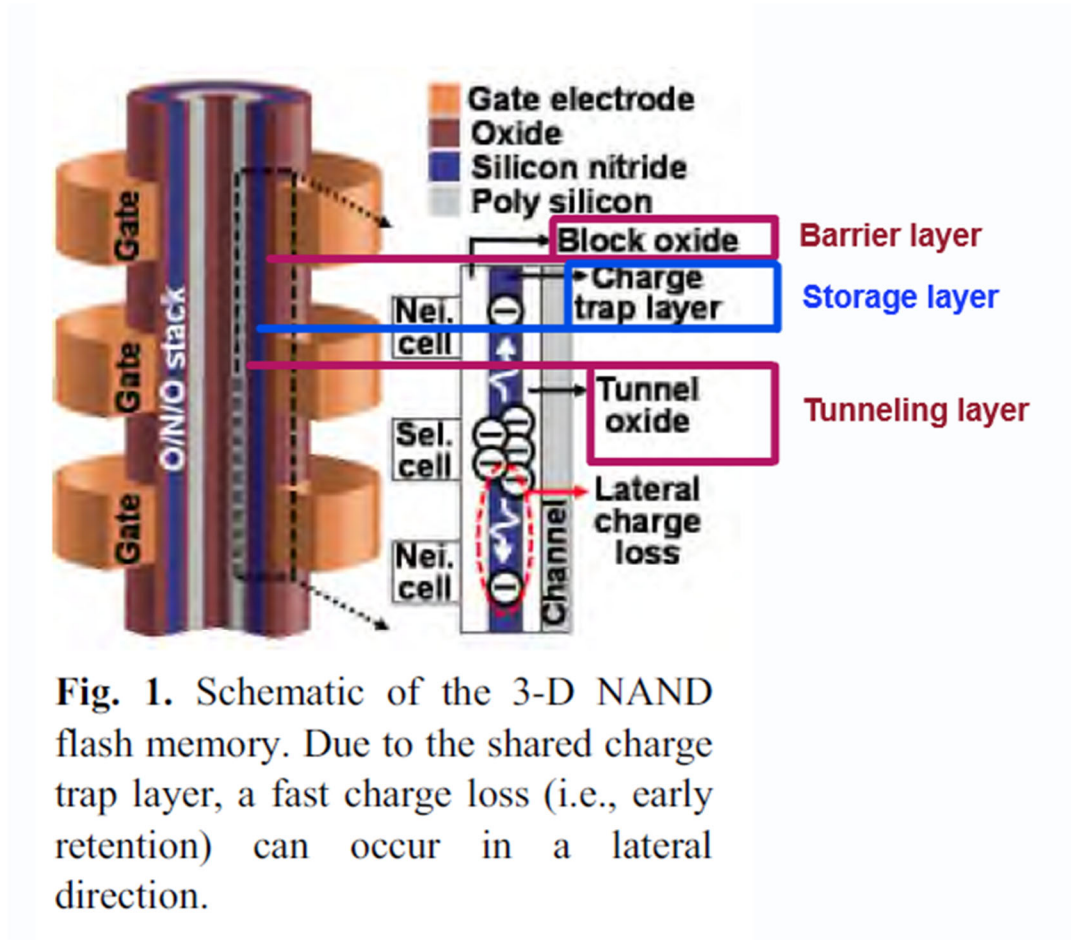
Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Ex. 1007, FIG. 1 (annotated).

[19.C] “a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and”

213. Seo in view of Choi renders this limitation obvious.

214. This limitation cites basic layers of a charge-trap memory cell. Choi’s “3-D NAND flash memory” includes each layer. The inner maroon-colored “Tunnel Oxide” is a *tunneling layer*; the blue-colored “Silicon nitride” is the *storage layer* (“charge trap layer”); and the outer maroon-colored “Block Oxide” is a *barrier layer*.



Ex. 1007, FIG. 1 (annotated).

[19.D] “a channel layer sandwiched between the memory film and the core filling film.”

215. Seo in view of Choi renders this limitation obvious.

216. Choi’s *channel layer* (polysilicon) in gray-coloring (and green annotation) below, is *sandwiched between* the *memory film* (see *supra* limitation [19.C] (the ONO film marked with light blue annotation)) *and the core filling film* (see *supra* limitation [19.B] (the maroon oxide marked with the red annotation)).

The *channel layer* is referred to as a channel layer because the conductive channel is formed in this layer.

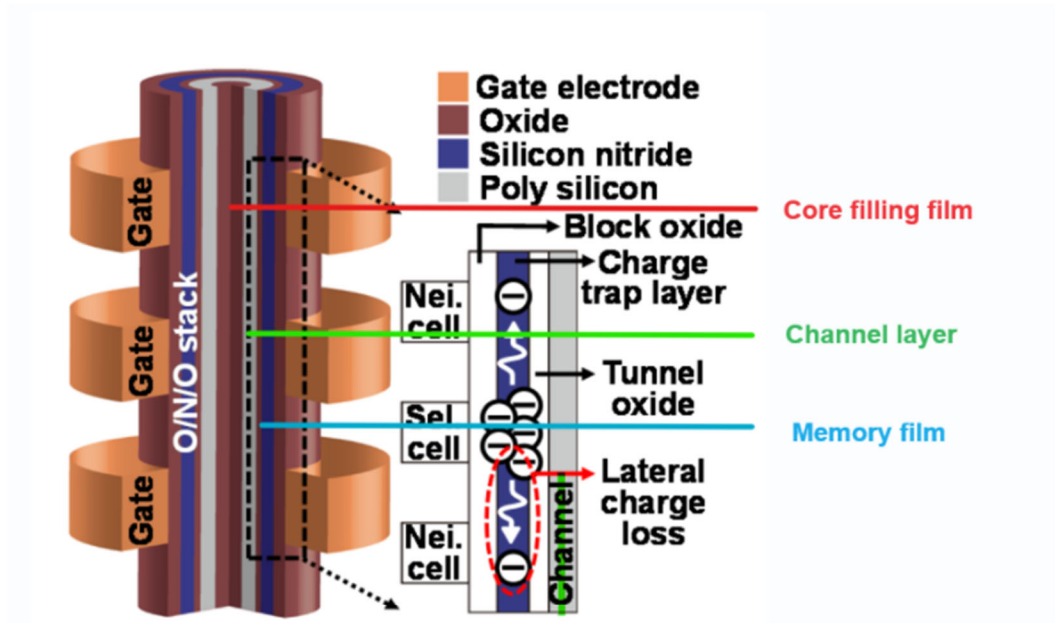


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Ex. 1007, FIG.1 (annotated).

18. Claim 20

217. Claim 20 depends from claim 19 and further requires:

[20] “wherein the circuit is further configured to remove the fast charges from a portion of the storage layer associated with the target memory cell.”

218. This limitation is substantively the same as claim 12. The difference is the that this claim requires a *circuit* to effectuate removing fast charges from a

portion of the storage layer. I discuss that a *circuit* performs the relevant operations in limitation [16.B].

19. Motivation to Combine

219. It would have been obvious, and a POSITA would have been motivated with a reasonable expectation of success, to apply Choi's teachings to Seo regarding: (1) charge trap memory and stack teachings (alternating gate/dielectric layers), and (2) read-verification step and fast charge removal for several reasons.

220. As general matter, a POSITA would have found Choi's teaching highly relevant to Seo. Both Seo and Choi address issues in the field of 3D NAND flash memory, and more specifically, issues relating to read operations in these devices. Ex. 1005, Abstract; Ex. 1007, 1:14-26. Seo is a patent application assigned to SK Hynix Inc., and many of Choi's authors are from SK Hynix's research center. *See* Ex. 1005, Cover; Ex. 1007, Cover. This would indicate that Choi's teachings are applicable to Seo. Choi describes the physics underlying certain of these issues (fast charges). Ex. 1007, p. 1. A POSITA would have been motivated to consider Choi to understand and improve on Seo's memory device. Specifically, Choi teaches how an electric field can impact fast-charge loss. Ex. 1007, p. 1. A POSITA would have considered Seo's read operation in view of Choi's description of the device physics in devices such as Seo.

221. **Choi's charge trap memory and stack teachings:** First, Seo does not describe in detail its 3D NAND memory cells. This is not unusual, as 3D NAND memory cells were well known at the time, and Seo's invention focuses on a read operation, not the device structure of a charge-trap memory cell. Choi, on the other hand, addresses issues relating to charge-trap memory cells, recognizing the promise of charge-trap technology. A POSITA would have considered Choi to implement the underlying 3D NAND memory of Seo, particularly because Choi addresses the issue of fast-charge loss in such memories. Ex. 1007, 1:16-20 ("Although 3-D NAND flash memory with a charge trap layer (SiN) has many merits, the retention characteristics stemming from lateral charge loss are expected to cause problems because the charge trap layers are shared between word-lines (WLs) (FIG, 1)."). Put another way, a POSITA would have been motivated to consider references such as Choi that detail how to implement the underlying structural formation of Seo's base 3D memory and how to overcome issues in implementing that structure.

222. Second, and more generally, charge-trap memory became the norm for 3D Flash memory before 2019. And for 3D Flash memory, the two basic types were conductive floating gate and charge-trap. Ex. 1017, 101, 144. It was textbook-level knowledge that "most of 3D memories [were] based on 'charge trap' cells." *Id.*, 15. POSITAs knew that charge-trap technology was more "scalable than floating gate." *Id.* Charge-trap memories improve "power and reliability." *Id.*, 101. Note that in

charge-trap memories, a continuous thin film, e.g., silicon nitride, serves as the storage layer. This is an improvement over conductive floating gate technology that requires separating each gate. Thus, a POSITA would have been motivated to consider implementing Seo in a charge-trap memory given its advantages (as is evident from its popularity).

223. Third, Seo's read operation creates a voltage differential that removes fast charges before a read, and Choi teaches a practical use of this electric field to overcome an issue in charge-trap memories. *See* §§IX.A.3, IX.B.1[1.D]. Specifically, Choi teaches that this voltage differential, which creates an electrical field, de-traps charges. *Id.* Choi further teaches that without such de-trapping, verification may be inaccurate. *See* §IX.A.3.

224. Fourth, Seo's disclosure of reducing read disturbance is also directly applicable to a charge-trap device. Due to the nature of having a polysilicon channel that is not directly biased when the top and bottom select transistors are not turned on for an unselected string, the read disturbance issue is more prominent due to the potential of the channel being capacitively coupled to the various voltages applied on the word lines of the memory strings. Thus, a POSITA would have recognized that Seo's read operation was specifically advantageous to Choi's charge-trap memory with respect to reducing HCI.

225. A POSITA would have had a reasonable expectation of success in applying Choi's structural teachings to Seo.

226. First, by 2019, charge-trap memory was the norm for 3D memory. Ex. 1017, 15. Again, 3D charge trap memories were textbook material. *Id.* In particular, the charge-trap memory string and 3D stack architecture were basic building blocks at the time. *Id.*, 105-106.

227. Second, Seo's 3D memory architecture would have been understood to include gate layers and memory pillars given its graphical depiction, and thus a POSITA would have understood that Seo was compatible with such a memory. Ex. 1005, FIG. 3.

228. Third, not only were 3D charge-trap memories known, but the device physics relating to their operational characteristics and programming issues were known. Ex. 1007. This enables a POSITA to account for those issues, such as fast-charge loss. *Id.*

229. **As to Choi's read-verification step and fast charge removal teachings:** First, both Seo and Choi address issues relating to the reliability of read operations. Ex. 1005, [0008]; Ex. 1007, 1:16-26. Typically, a POSITA concerned with a particular function, such as a read, would have been motivated to consider all issues pertaining to that function. Thus, a POSITA implementing Seo's read method

would have been motivated to consider other issues relating to read operations, and Choi expressly addresses how fast-charge loss can impact reads.

230. Second, Seo focuses on hot-charge injection (“HCI”), and Choi focuses on fast-charge loss. *See* §§IX.A.1, 3. A POSITA was well aware of these issues. Ex. 1013, Ex. 1016; Ex. 1001, 1:29-36 (acknowledging fast-charge-loss issue in the background section). Thus, a POSITA implementing Seo would have been aware of the issues that Choi addresses and would have been motivated to consider Seo’s read operation in view of Choi’s teachings to further improve Seo’s device.

231. Third, Seo’s read operation creates a voltage differential by applying a higher voltage on unselected word lines than on the selected word line during the first time period t_1 . *See* §IX.B.1[1.D]. In particular, this voltage differential will create an electric field near the selected memory cell when considering the voltage differential of the adjacent word line and the selected word line. A POSITA would have been motivated to consider the effect of this electrical field created by the voltage differential. Choi addresses how this electrical field will impact de-trapping. And Choi expressly teaches this in the context of program-verify operations, because the fast-charge loss occurs immediately after a program. Ex. 1007, FIG. 2. Thus, Choi not only teaches the effect of Seo’s voltage differential, but focuses in on the important time period in which the voltage differential may be advantageous.

232. Fourth, Choi, in effect, lays out an advantageous use case for Seo's read operation, namely, as a verify that also removes fast charges. Recall that Choi found that lateral fast-charge loss was more dominant than vertical loss in charge trap memories. *See* §IX.A.3. Choi further teaches that an electric field will de-trap the charges. Ex. 1007, p. 1. A POSITA would have recognized that the lateral-electric-field-inducing voltage differential, as Seo discloses, is what Choi describes as driving the lateral fast-charge loss. Next, Choi describes that because of fast charge loss, a typical read-verify may be unsuccessful because the verification will occur before the fast-charge loss. This is because the verification may occur before fast charges de-trap and may not accurately sense what the threshold voltage and associated data state will be after the fast-charge loss. As shown below, a verification might verify that a cell is in state PV3, but after the fast-charge loss, the cell would drift to PV2. Thus, a POSITA would have recognized the benefit of using Seo's read operation to verify. Specifically, Seo's operation would remove the fast charges. A verification would then indicate the cell was in PV2 and require another programming pulse.

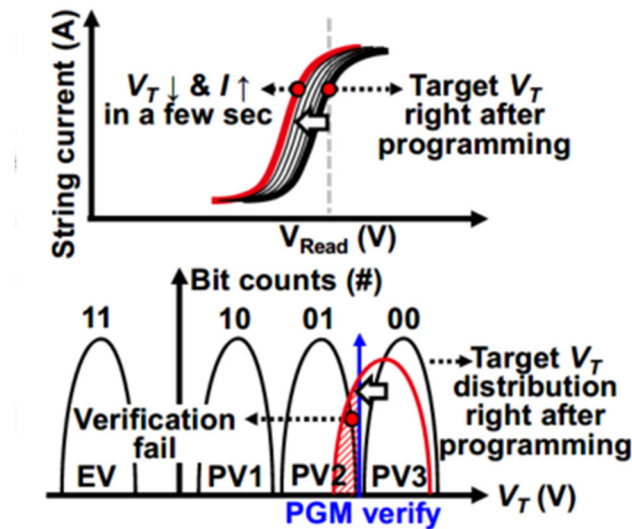


Fig. 2. Schematic of the early retention and its effect on V_T and I . The early retention threatens the MLC capability and the tight V_T distribution.

Id., FIG. 2.

233. I will also comment on the general knowledge of a POSITA. First, it was well known that read operations and verify operations are virtually identical. A POSITA understood that “the read operation may include the verification read operation for verifying the success of the program operation or the normal read operation for determining the data stored in the memory cells.” Ex. 1028, [0103]. By “normal read operation,” this refers to a read that does not immediately follow a program operation and that does not verify the program operation. Imagine taking a picture. When this occurs, the data is programmed into the memory and the read operation will verify that the program was successful. Later on, when viewing that picture, “normal read operations” retrieve the data to display the picture. Thus, a

read operation for both verifying and normal reads are the fundamental uses of the read algorithm in Flash memories.

234. Second, the details of this read algorithm is incredibly important to reduce issues relating to the various disturb mechanisms. In short, a read operation can inadvertently alter the data state of the target and other memory cells. In simple terms, this means a read operation can actually corrupt the data in the memory. These concerns are no less when verifying a program operation, because the verification operation can cause the exact same problems. Thus, Seo's read operation that mitigates these issues would have been equally applicable to mitigate these issues for either a normal read or for a read that verifies a programming operation.

235. Third, as I discuss above, the read operation is very important to mitigate the various disturb issues. As a result, a read operation is not something that designers simply select and implement. Rather, there is significant testing to arrive at the ideal read operation that balances the various disturb issues with performance. Once arriving at a suitable read operation that strikes the right balance, a POSITA would have been highly motivated to employ that same operation, rather than creating an entirely different operation. I describe below the slight tweak to the read voltage for verification. This only slightly changes the voltage on the selected word line during the sensing stage.

236. A POSITA would have had a reasonable expectation of success in applying Choi's read-verification and fast-charge-removal teachings to Seo.

237. First, as I discuss above, both Seo and Choi employ a conventional 3D architecture. Thus, one would understand Choi's teachings to be applicable to Seo.

238. Second, Choi teaches the device physics of Seo's read operation. This would have given a POSITA an understanding of how Seo's read operation would be suitable, and implementable, to verify. And verification was a standard use of a read operation. *See* §VI.B.

239. Third, Choi teaches the timing of fast-charge loss (see above). This would enable a POSITA to determine the impact of Seo's read operation, which removes fast charges, on fast-charge loss. Specifically, a POSITA would have understood that Seo's read operation, when verifying, would remediate fast-charge loss because the verification occurs during the fast-loss period.

240. Fourth, how to use a read operation for verification was well understood. In a normal read operation, the read voltage (the voltage applied on the selected word line during sensing) is set between data states (for a multi-level cells). In a verify operation, instead of a read voltage, a verify voltage is used. *See* Ex. 1029, [0181]. Setting different voltage levels for read and verify operations was a routine practice. *See* Ex. 1019, 25:2-8; Ex. 1028, [0054]-[0055]. There is just a slight difference in these voltages, because, for example, the verify voltage may be

set at the low end of the threshold distribution (for multi-level cells). *Id.* The voltages on other memory elements are kept the same, because those voltages relate to mitigating issues relating to inadvertently altering data states.

C. Ground 2: Claim 15 Is Obvious Over Seo in View of Choi and Izumi

1. Claim 15

241. Claim 15 depends from claim 1 and further requires:

[15] “wherein conducting the read-verification operation comprises conducting a failed bit count in parallel.”

242. In my opinion, a POSITA would have considered Izumi to be within the scope of the prior art and highly relevant to the patentability of the ’342 patent’s claim 15.

243. In my opinion, Seo in view of Choi and Izumi renders this additional limitation obvious.

244. Izumi discloses this limitation.

245. Izumi defines a *fail bit* as a data bit whose write value differs from its read value. Ex. 1008, [0076]. Bit failure in non-volatile memory has been a standard issue since the creation of non-volatile memories. A read operation can occur “[a]t the same time” as *fail-bit counts* are acquired during a write operation to determine whether to activate one or both ECC circuits. *Id.*, [0077]-[0079]. ECC circuitry corrects the inaccurate data from failed bits. Additionally circuitry is necessary

depending on the bits that must be corrected. And “*fail-bit counts* . . . are updated during a read operation.” *Id.*, [0076]. More specifically, “[w]hen a data read operation starts, the operation controller 506 acquires previous *fail-bit counts* . . . *simultaneously* with reading of data...,” and the counts are then updated. *Id.*, [0081], [0084] (emphasis added); *see also id.*, FIG. 8 (steps S310, S370). Thus, *failed-bit counts* are acquired and updated during a read operation following a write operation, *i.e.*, *conduct[ed] in parallel* to a *read-verification operation*. And similar to the ’342 patent, additional write operations may occur after failed bits are counted. *Compare* Ex. 1001, 14:5-6 *with* Ex. 1008, [0079].

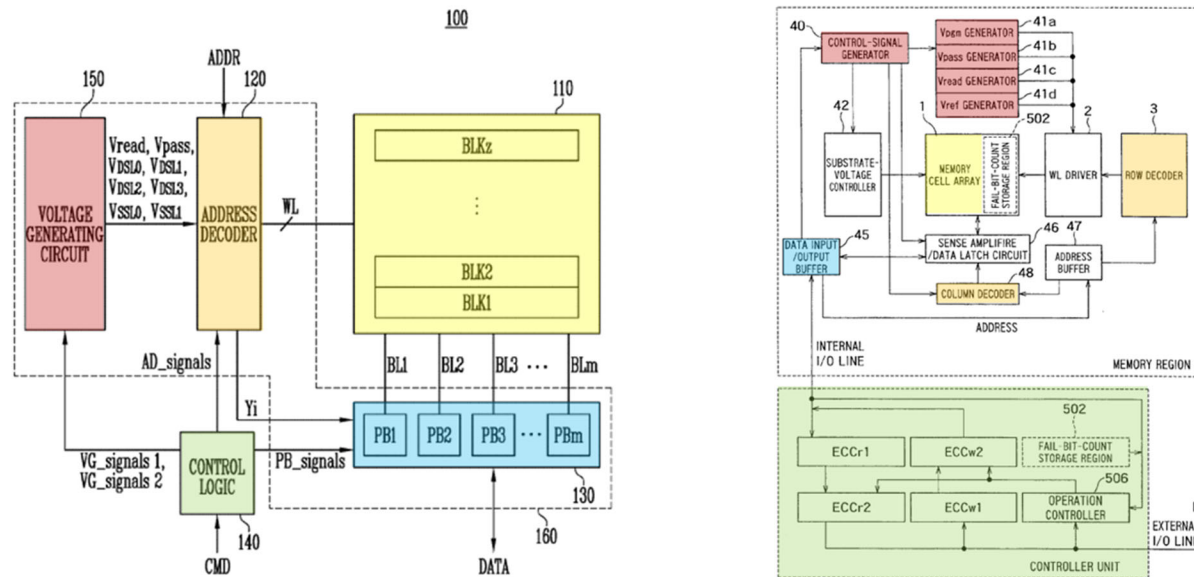
246. A POSITA would have been motivated to combine Seo with Izumi’s failed-bit count for several reasons.

247. First, the failure of bits is an issue in 3D memories like Seo (as with conventional non-volatile memories). Ex. 1017, 47-50. Seo attempts to mitigate read-disturb effects. But this does not solve the problem of memory cells that will ultimately fail. *Id.*, 47. This is because, for example, such memory cells have a standard endurance level and will ultimately fail (some sooner than others). One manifestation of such a failure is that the cell would not be able to verify to the desired programmed voltage after repeating the program and read-verify operation cycles. Izumi’s ECC approach to correct such bits was a well-known mechanism

for detecting and correcting failed bits and would have been advantageous to Seo's device, providing the same corrective function. Ex. 1008, [0003]-[0004].

248. Second, Izumi's specific approach reduces power consumption by selectively activating one or two ECC circuits to tailor ECC capability to the device condition. Ex. 1008, [0078], [0082]. In other words, it activates only the necessary circuitry in view of the number of failed bits. Izumi's low-power ECC techniques are thus specifically suitable for correcting failed bits, because it does so while minimizing power consumption.

249. Third, Seo and Izumi are in the same field and Seo includes the same high-level functional blocks (e.g., address decoders, control logic, and buffer) to implement Izumi's ECC techniques. And both aim to improve read-operation accuracy, and thus a POSITA would have looked to Izumi to further Seo's goals. Ex. 1005, [0008], [0089]; Ex. 1008, [0003]-[0004]. Izumi applies its failed-bit-count method to a memory like Seo's: a NAND flash using charge-trapping technology, and a memory array comprising bit lines and word lines and partitioned into pages. Ex. 1008, Abstract, [0003], [0018], [0041].



Ex. 1005, FIG. 1; Ex. 1008, FIG. 6 (both annotated). Izumi discloses a 2D NAND flash, but as I explain above, failed bits are a concern regardless of the dimensionality of the flash memory, and Izumi's failed-bit-count and ECC techniques also apply to 3D NAND flash. The ECC circuitry operates to correct bits of data, regardless of whether those bits come from 2D or 3D NAND.

250. A POSITA would have had a reasonable expectation of success in applying Izumi's teachings to Seo.

251. First, using ECC to correct failed bits, as Izumi does, was textbook material. Ex. 1017, 50. ECC is undergraduate-level material.

252. Second, the components Izumi uses for ECC such as the ECC circuits and failed-bit-count storage can reside in the control logic and a partition of the memory array, components common to Seo's and Izumi's memory devices. *See*

supra Ex. 1005, FIG. 1; Ex. 1008, FIG. 6. For example, one would simply implement Izumi's additional circuitry in Seo's circuit blocks.

253. I note that Choi confirms that Seo's read-verification operations remove fast charges. Therefore, Choi has no impact on combining Izumi's failed-bit count into Seo's device.

D. Ground 3: Claims 1-3, 5-6, 8-14, 16-17, and 19-20 Are Obvious Over Nam in View of Choi

254. In my opinion, a POSITA would have considered Nam and Choi to be within the scope of the prior art and highly relevant to the patentability of the '342 patent's claims.

255. In my opinion, Nam in view of Choi and the knowledge of a POSITA renders claims 1-3, 5-6, 8-14, 16-17, and 19-20 obvious.

1. Explanation of Figures

256. Because I cite to various figures of Nam, I will first provide a description of how these figures relate.

257. Nam discloses that its "inventive concept [is] more fully described with reference to FIGS. 1 to 10." Ex. 1006, [0147]. The focus is on Nam's "immune disturbance read operation." Other figures in Nam, e.g., Figure 19, also describe use cases of Nam's "immune disturbance read operation," such as the verification use. *Id.*, [0155]-[0156].

258. Figures 1-3 and 5 depict exemplary structural aspects of Nam's memory array. Ex. 1006, [0033]-[0036], [0038]. For example, Figure 5 illustrates a charge-trap memory string. *Id.*, Figure 5.

259. Figure 3 also illustrates a prior art pre-sensing and sensing scheme. Ex. 1006, [0094]-[0096]. The sensing phase measures the threshold value of the target memory cell. *Id.*, [0096]. This is the heart of any read operation. The specification often refers back to Figure 3, because Nam's immune disturbance read employs this prior art sensing scheme. Nam's focus is on the phases before and after sensing that remediate issues relating to the sensing phase, such as disturb. *Id.*, [0122]. I note that Figure 3 includes an obvious error. Figure 3 indicates that the bottom select gate would be at ground during sensing. This is an obvious error, because the top and bottom select gates must be on to be able to sense whether the respective memory cell is conductive. Other figures correctly illustrate that the bottom select gate is at a pass voltage, which turns on the select transistor, during sensing.

260. Figure 5 illustrates the physics of charge sharing among memory cells in a charge-trap memory string. Ex. 1006, [0099]-[0100].

261. Figure 4 depicts exemplary threshold and erase voltage values. Ex. 1006, [0098]. These threshold values correspond to the erase and data states.

262. Nam uses Figures 6-10 to describe the immune disturbance read and illustrate different signals over four time periods: (1) WL Setup (pre-sensing), (2) 1st

and 2nd reads (sensing), (3) Charge Share, and (4) Recovery. Ex. 1006, FIGs. 6-10. These figures build upon each other as I discuss below.

263. As an initial matter, in my analysis, I focus on the first two periods: (1) WL Setup (pre-sensing), and (2) 1st and 2nd reads (sensing). Ex. 1006, FIGs. 6-10. As I will explain, the WL Setup period removes fast charges.

264. Nam uses Figure 6 to first describe the basic signaling of the immune disturbance read operation, namely, the voltages on “UNSEL WLs” (unselected word lines) and “SEL WL” (selected word line). These signals are identical for Figures 6-10 with respect to the first two periods. Ex. 1006, FIG. 6.

265. Nam uses Figures 7-9 to illustrate options of using different signals on different UNSEL WLs during the Charge Sharing and Recovery periods. Ex. 1006, FIGs. 7-9.

266. Figure 9 illustrates the voltages on “SEL SSL” (selected top select gate) and “GSL” (bottom select gate) voltages. Ex. 1006, FIG. 9.

267. Figure 10 adds the voltage on “UNSEL SSL” (unselected top gate). Ex. 1006, FIG. 10, [0122] (“Referring to FIG. 10, an immune disturbance read operation on unselected string selection lines UNSEL SSL *may further include* applying ... to ... UNSEL SSL”). Note that Figure 10 omits the “SEL SSL” (selected top select gate) waveform from Figure 9, as its focus is on the additional of UNSEL SSL. *Id.*,

FIGs. 9, 10. This line must be high during the read phase, because the select gates must be on.

2. Claim 1

[1.Pre] “A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:”

268. In my opinion, to the extent the preamble is limiting, Nam discloses it.

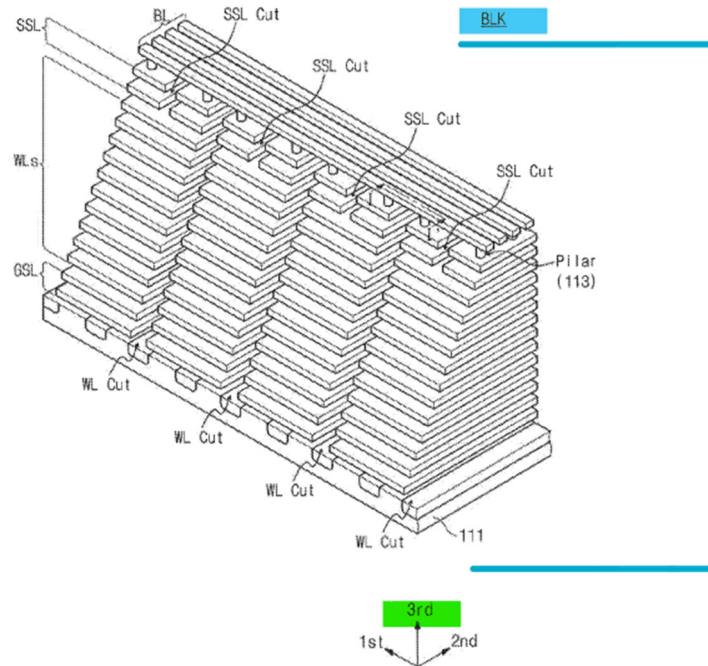
269. Nam discloses a read operation: “[a] method of reading a nonvolatile memory device” that includes the step of “sensing a state of a memory cell.” Ex. 1006, Abstract.

270. And Nam discloses that its read operation (“immune disturbance read operation”) is for verification, i.e., for use *after* a program operation, e.g., a *read-verification operation*. Ex. 1006, [0026] (“a verification read operation”), [0155] (“immune disturbance read operation may be selectively performed at a program verification operation”), FIG. 19.

271. Nam’s read operation occurs on “memory cells corresponding to the selected word line WLm-3 and the selected string selection line SSL1,” i.e., a *target memory cell*. Ex. 1006, [0096].

272. Nam discloses that its operations are applicable to a *three-dimensional* memory device (Ex. 1006, [0029] (“vertical NAND flash memory”), [0065] (“[e]ach of the memory blocks” may “have a *three-dimensional* structure”). Nam depicts a conventional 3D NAND memory below:

Fig. 2A



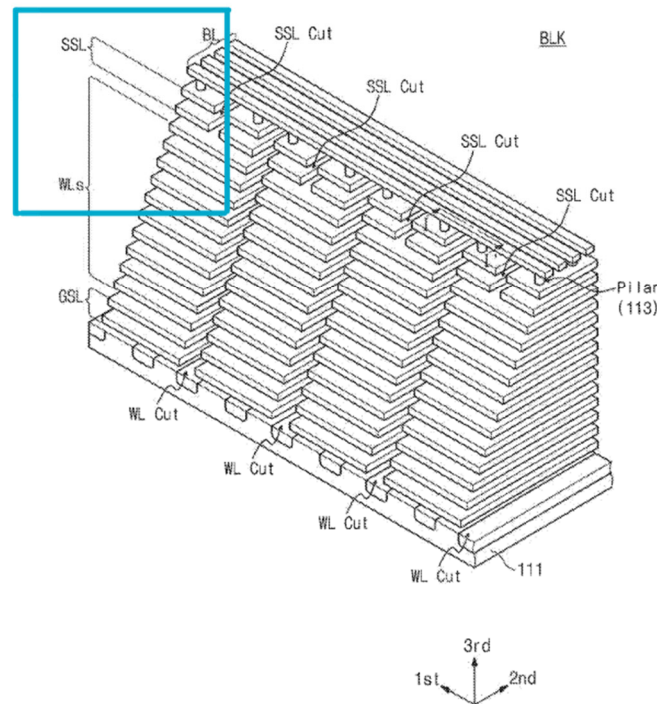
Id., FIG. 2A (annotated). Thus, Nam discloses *a method for conducting a read-verification operation* (e.g., an immune disturbance read operation) *on the memory cells connected with the selected word line may be performed on a target memory cell* (e.g., memory cell connected to a selected word line/string) *in a three-dimensional (3D) memory device* (e.g., three-dimensional memory).

[1.A] “*applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period:*”

273. Nam discloses this limitation.

274. Nam refers to the *top select gate* as a “string selection line SSL.” Ex. 1006, [0064].³ As shown below, the SSL layers reside at the top of the memory stack and select string(s).

Fig. 2A



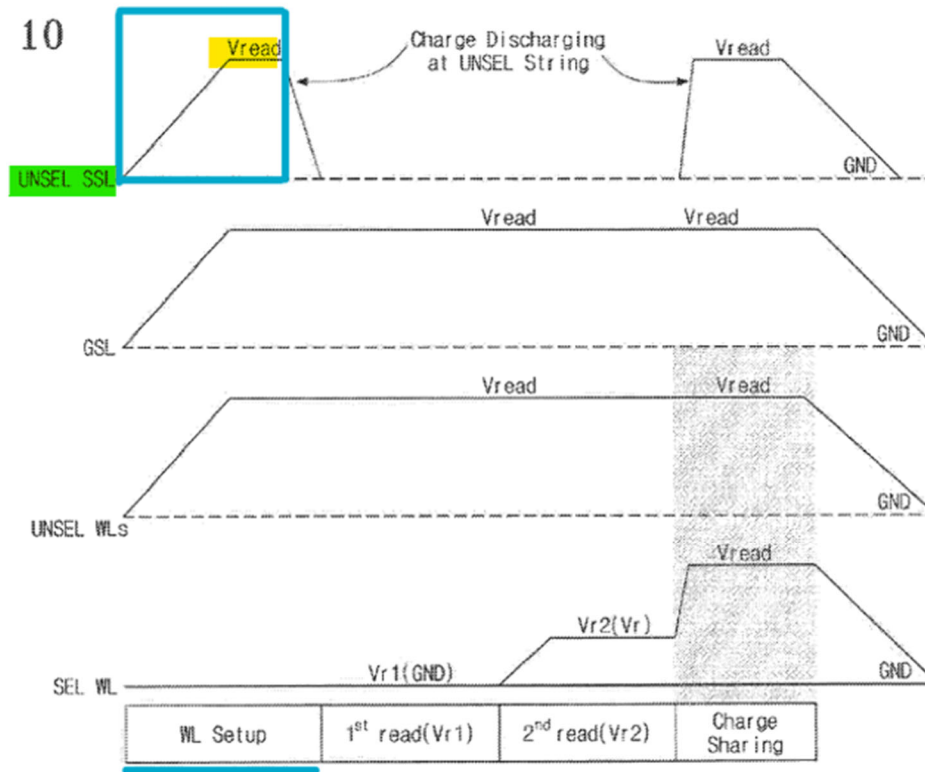
Id., FIG. 2A (annotated), [0076].

³ At times, Nam refers to “string selection transistors,” which are the individual transistors of the SSL layers. Ex. 1006, [0133]. The SSL layers connect to these transistors and thus applying a voltage to an SSL layer applies a voltage to the string selection transistors that connect to that layer.

275. Nam discloses that “FIG. 10 is a timing diagram illustrating an immune disturbance read operation according to an exemplary embodiment of the inventive concept.” Ex. 1006, [0122]. Figure 10 includes *a first time period*, i.e., “WL Setup,” and *a second time period*, i.e., “1st read[V_{r1}]” and “2nd read[V_{r2}].” *Id.*, [0104]. The setup period, as the name suggests, effectively prepares for the sensing stage. There are 1st and 2nd reads because Nam employs multi-level cells.

276. During *a first time period*, “the read pass voltage V_{read} may be applied to unselected string selection lines UNSEL SSL before a sensing operation (e.g., before the 1st read and 2nd read).” Ex. 1006, [0122]. Pass refers to a voltage sufficiently high to turn on the relevant transistors.

Fig. 10

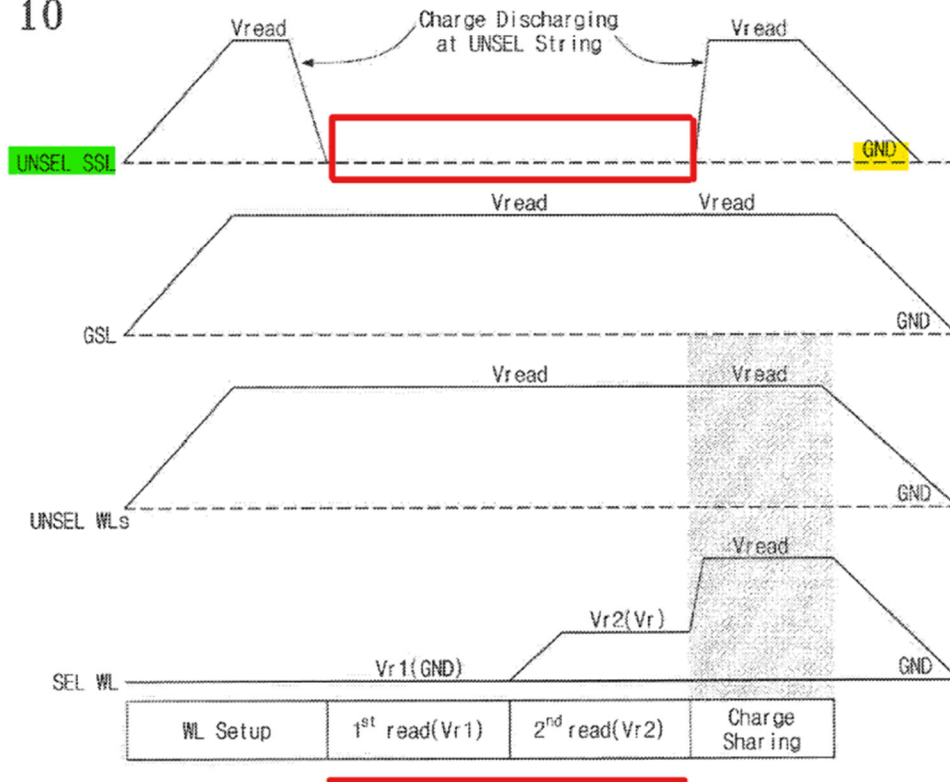


Id., FIG. 10 (annotated.).

277. The '342 patent provides a non-limiting embodiment in which the prepare voltage is between 4-7 volts. Ex. 1001, 2:40-44. While it is not my opinion that the claim requires this specific voltage range, Nam's Vread pass voltage is within this range. Ex. 1006, [0098] ("Vread may be about 7V"). Like Figure 6 of the '342 patent, Nam's Vread pass voltage is greater than the voltage applied to the selected word line during the reading phase. *Compare* Ex. 1001, FIG. 6 (Vprepare versus Vread), *with* Ex. 1006, FIG. 10 (Vread versus Vr2(Vr)).

278. Further, during *a second time period*, Nam discloses applying an *off voltage*—namely, GND (ground)—to unselected string selection lines UNSEL SSL.

Fig. 10



Ex. 1006, FIG. 10 (annotated). Ground is an *off voltage* because it does not turn on the transistor. *Id.*, [0098] (compare with voltage that turns on transistor).

279. The description of Figure 10 states: “[a]n operation of applying the read pass voltage Vread to unselected string selection lines UNSEL SSL at a sensing operation *may be substantially the same as that described with reference to FIG. 3, and a description thereof is thus omitted.*” Ex. 1006, [0122]. In the full context of the ’342 patent, “applying the read pass voltage Vread to unselected string

selection lines UNSEL SSL at a sensing operation” would have been understood to refer to ramping the applied voltage from Vread to GND as sensing starts. Ex. 1006, [0096], [0122]. This is clear from Figures 3 and 10.

280. With respect to Figure 3, Nam discloses that application of Vread on UNSEL SSL terminates when the sensing operation begins: “after boosting charges of the unselected strings ST2 to ST4 are discharged or shared, bit lines BLi and BLi+1 may be pre-charged, ***a ground voltage GND may be applied to the unselected string selection lines*** SSL2, SSL3 and SSL4, a read voltage Vr may be applied to the selected word line WLM-3, and the read pass voltage Vread may be applied to the remaining word lines WL0 to WLM-4 and WLM-2 to WLM. ***Under this bias condition, a sensing operation may be performed***” Ex. 1006, [0096].

281. A POSITA would have understood that the ramping down of the unselected string selection lines to a ground voltage GND is necessary in order to turn off the unselected strings, since otherwise any current conduction on the unselected strings would be sensed by the BLi and cause erroneous sensing of the current on the selected string.

282. With respect to Figure 10, on UNSEL SSL, the applied voltage ramps down from ***Vread to ground*** at the start of the sensing period (1st and 2nd reads) and then after sensing, ramps up from ***ground to Vread***. Consistent with Figure 3, this

demonstrates that during the sensing, “a ground voltage GND may be applied to the unselected string selection lines.” Ex. 1006, [0096], FIG. 10.

283. Thus, Nam discloses *applying, on an unselected top select gate of an unselected memory string* (e.g., UNSEL SSL), *a prepare voltage during a first time period* (e.g., Vread during WL Setup) *and an off voltage during a second time period* (e.g., GND during 1st and 2nd read periods).

[1.B] “applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period;”

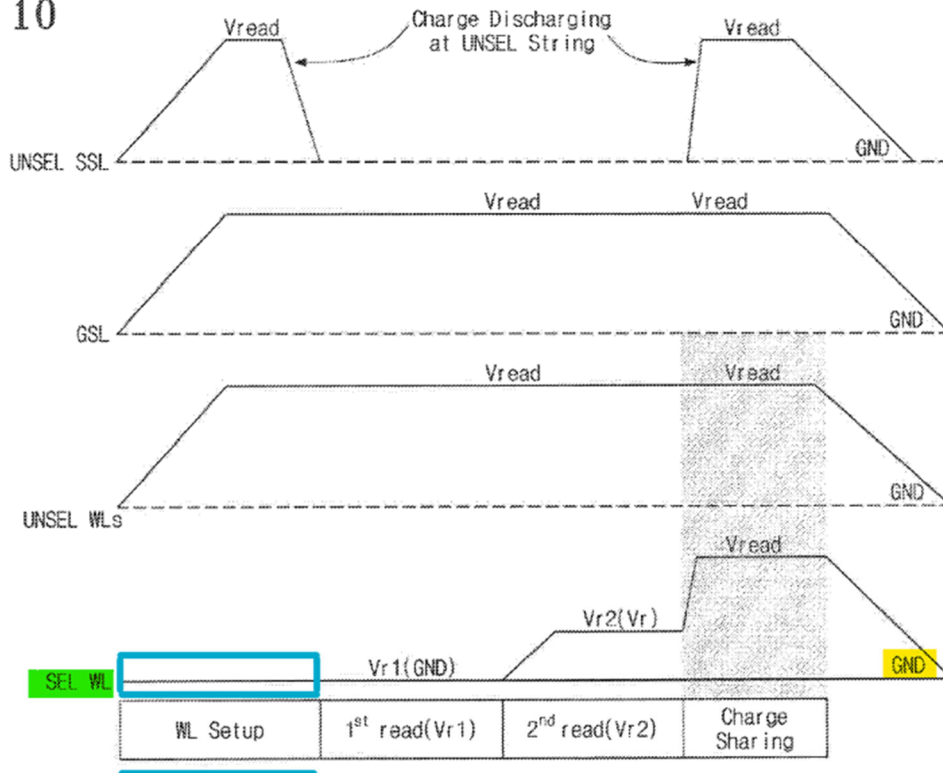
284. Nam discloses this limitation.

285. Nam discloses “read operations” on a *memory cell*. Ex. 1006, [0104]. This “read operation” occurs on “memory cells” that correspond to “the selected wordline” (i.e., *selected word line associated with the target memory cell*), *id.*, [0094]-[0096] (“a sensing operation may be performed to detect on or off states of memory cells corresponding to the selected word line”). In other words, the *target memory cell* is read by using a selected word line (and bit line).

286. Nam discloses how “[i]n the word line setup section WL Setup [*the first time period*], a ground voltage GND may be applied to a selected word line SEL WL.”⁴ Ex. 1006, [0105].

⁴ GND may be 0 volts. Ex. 1006, [0100].

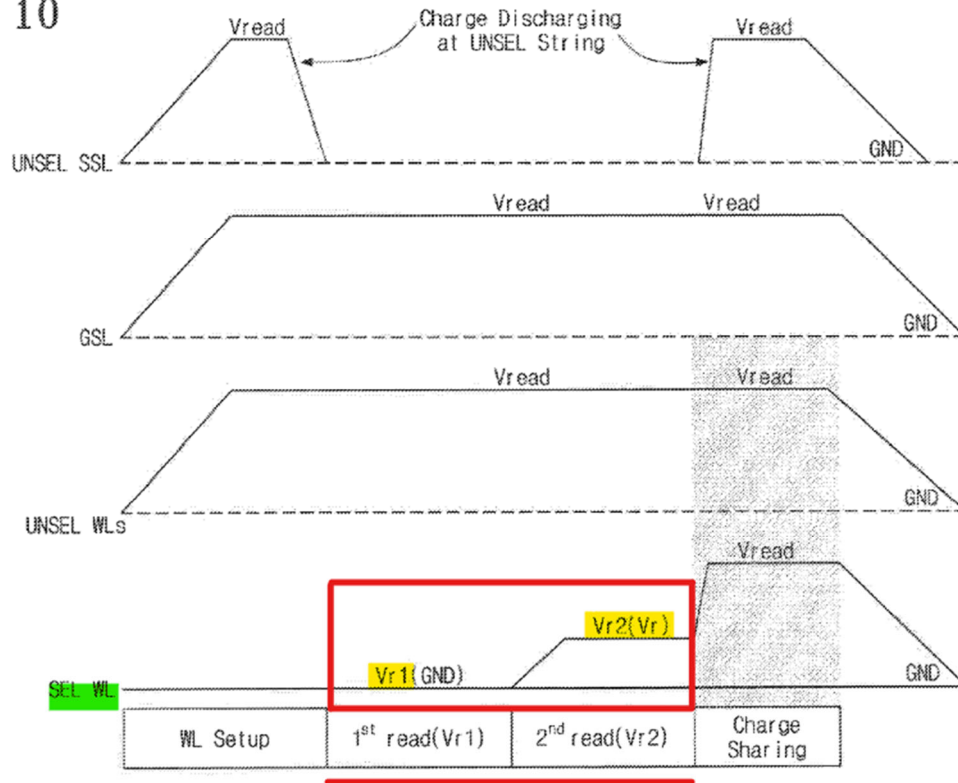
Fig. 10



Id., FIG. 10 (annotated).

287. Next, in the “first read section read” and “second read section” (*the second time period*), a “sensing operation may be performed.” Ex. 1006, [0106]. This involves applying a “read voltage V_r ,” such as “a first read voltage $Vr1$ ” and “a second read voltage $Vr2$ ” to the selected wordline. *Id.*, [0096], [0104], [0106]. Again, Nam employs multi-level cells, thus there are two read voltages. Each read voltages determines whether the memory cell’s threshold is above or below a particular value.

Fig. 10



Id., FIG. 10 (annotated).

288. Thus, Nam discloses *applying, on a selected word line associated with the target memory cell* (e.g., SEL WL), *the off voltage during the first time period* (e.g., Ground during WL Setup) *and a read voltage during the second time period* (e.g., Vr1(GND) during 1st read period and Vr2(Vr) during 2nd read period).

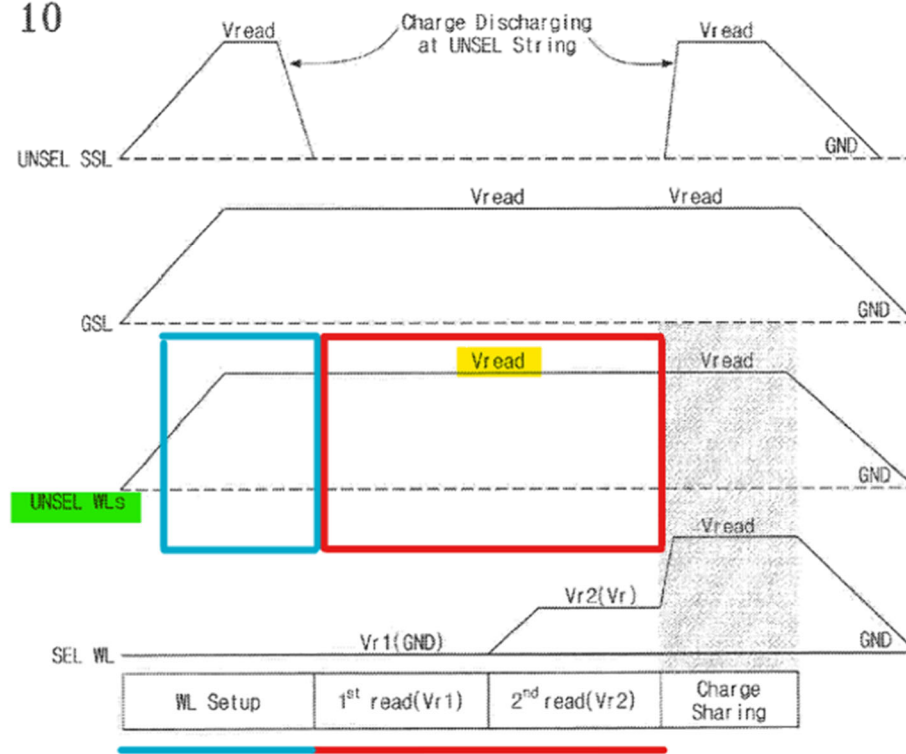
[1.C] “*applying, on an unselected word line, a pass voltage during the first time period and the second time period,*”

289. Nam discloses this limitation.

290. During both the WL Setup (*the first time period*) and the 1st and 2nd reads (*the second time period*), Nam discloses that a “read pass voltage Vread may

be applied to the remaining word lines,” i.e., *unselected word lines*. Ex. 1006, [0096], [0105] (“[i]n the word line setup section WL Setup [*the first time period*], . . . a read pass Vread voltage may be applied to unselected word lines UNSEL WLs”). These voltages turn on the memory cells above and below the target memory cell. This is necessary in a sensing stage.

Fig. 10



Id., FIG. 10 (annotated).

291. Thus, Nam discloses *applying, on an unselected word line* (e.g., UNSEL WLs), *a pass voltage during the first time period and the second time period* (e.g., read pass Vread during WL Setup, and 1st and 2nd reads).

[1.D] “wherein the read-verification operation removes fast charges of the target memory cell during the first time period”

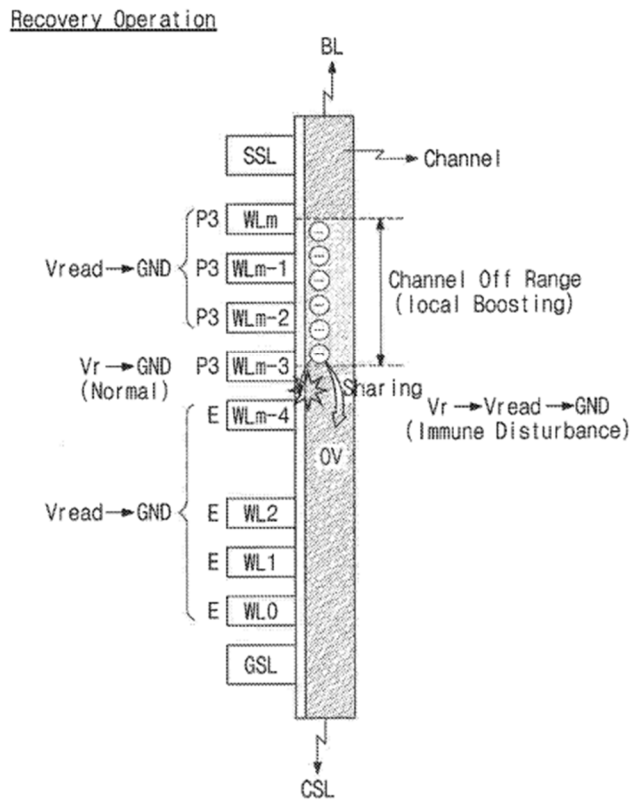
292. Nam discloses this limitation or, at a minimum, renders it obvious in view of Choi.

293. Nam discloses charge-trap memory cells in several places.

294. First, Nam broadly describes its memory as applicable to “NAND flash memory.” Ex. 1006, [0164], Claim 24. NAND flash memory includes charge-trap memory cells. Ex. 1017, 101. Indeed, charge-trap was one of two basic 3D flash memories. *Id.*, 101, 144.

295. Second, Nam depicts a charge-trap device:

Fig. 5



Ex. 1006, FIG. 5, [0099]. As shown above, the 3D vertical channel includes a solid, continuous memory channel, e.g., silicon nitride. The word line immediately abuts these materials. There are no segmented floating gates.

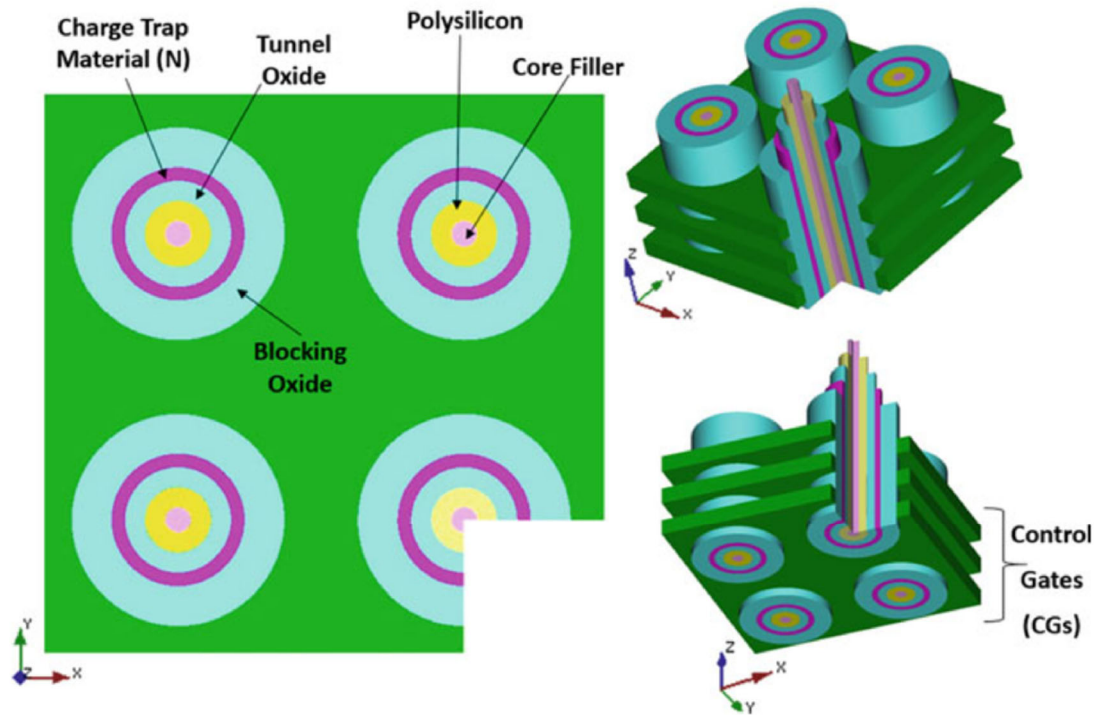


Fig. 4.6 BiCS memory cells

Ex. 1017, 105. As can be seen above, the charge-trap material and surrounding oxide layers are continuous layers of material that run vertically through the string. And the gate layers immediately abut these materials.

296. In contrast, conductive, floating gate 3D vertical channels include segmented floating gates. Ex. 1017, 145-48. This is because the floating gates are conductive. They must be separated or the charge within respective gates would escape.

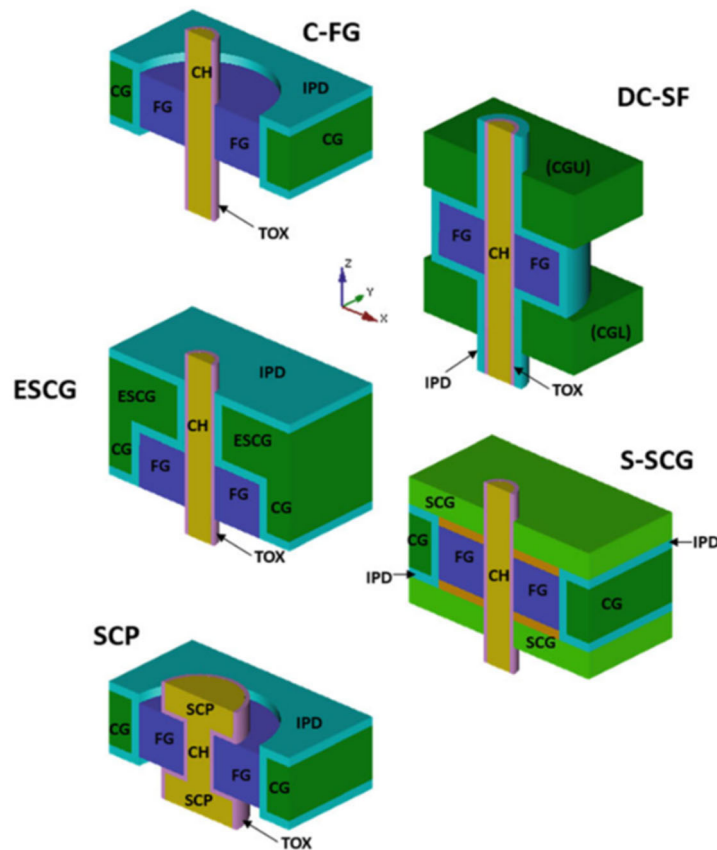


Fig. 5.1 Different types of 3D floating gate memory cells

Ex. 1017, 145. No such floating, segmented gates are in Nam's Figure 5.

297. Given these multiple disclosures, a POSITA would have understood immediately that Nam's teachings are provided in the context of charge-trap devices. At a minimum, these teachings at least render obvious charge-trap memories. I discuss how disclosures of 3D Flash memory renders obvious charge-trap memory in Ground 1, under limitation [1.D].

298. As I describe above, Nam teaches the requisite waveforms for the claimed *read-verification operation*. See *supra* limitations [1.A]-[1.C]. Of note, Nam teaches having a higher voltage on unselected WLs (including WLs adjacent

to the selected WL) relative to the selected WL during the *first time period*, WL Setup. Ex. 1006, Fig. 7. In charge trap devices, this voltage differential creates a lateral electric field and results in the lateral movement of the fast charges from the selected cell to either of the neighboring cells, as required by claim [1.D]. See IX.A.3.

299. To the extent that Patent Owner argues that Nam does not disclose removing fast charges, I disagree for the reasons above. Regardless, Nam in view of Choi render this limitation obvious as well. Choi expressly teaches that a voltage differential (e.g., a higher voltage on unselected WLs (including WLs adjacent to the selected WL) relative to the selected WL) removes fast charges. See §§IX.A.3, IX.B.1[1.D]. This creates the lateral fast-charge loss (due to de-trapping). The electric field causes the de-trapping. Thus, in view of Choi, a POSITA would have understood that Nam's read-verification operation removes fast charges. See §IX.D.18.

300. Accordingly, Nam discloses, or at least in view of Choi renders obvious, *wherein the read-verification operation removes fast charges of the target memory cell during the first time period* (e.g., voltage differential from the read-verification operation removes charge from Nam's charge trap memory cells).

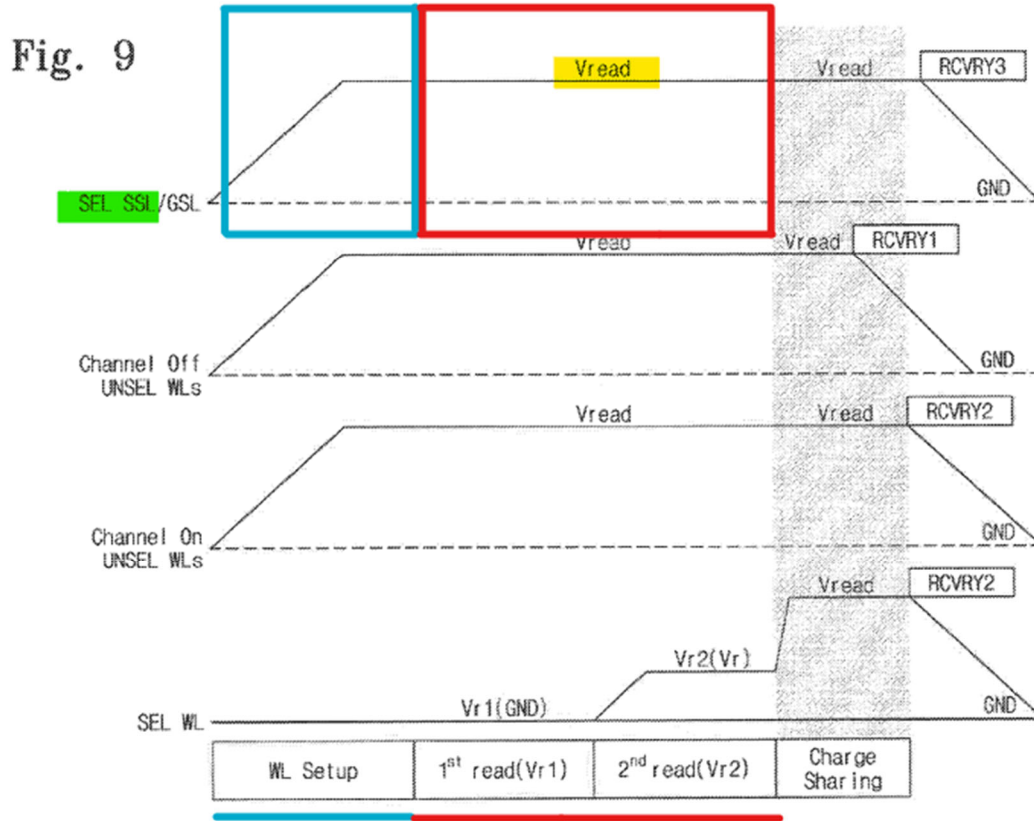
3. Claim 2

301. Claim 2 depends from claim 1 and further requires:

[2.A] “applying, on a selected top select gate of a selected memory string containing the target memory cell, a top select gate voltage during the first time period and the second time period;”

302. Nam discloses this limitation.

303. Recall that an SSL (which includes SSTs as respective gate transistors) is the *top select gate* of Nam. See §IX.D.2[1.A]; Ex. 1006, [0090]. Further, recall that Figure 9 shows aspects of Nam’s read operation beyond those depicted in Figure 10, including the *selected top gate of the selected memory string containing the target cell* (SEL SSL). See §§IX.D.1, IX.D.2[1.C]. As shown below, as part of the same read-verification operation as Figure 10, Figure 9 shows that during *the first time period and the second time period* (e.g., WL Setup, and 1st and 2nd read), Vread (*a top select gate voltage*) is applied to SEL SSL:



Ex. 1006, FIG. 9 (annotated). Vread turns on the transistor. Ex. 1005, [0098].

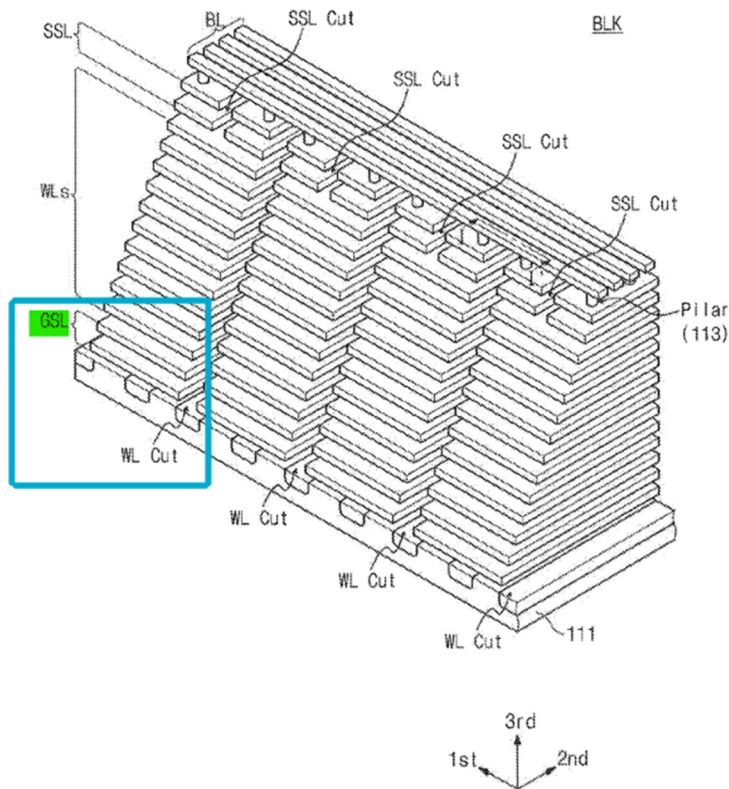
[2.B] “applying, on a lower select gate of the selected memory string containing the target memory cell, a lower select gate voltage⁵ during the first time period and the second time period.”

304. Nam discloses this limitation.

⁵ For both the top select gate voltage and lower select gate voltages, the '342 patent provides examples of 4-7 voltages, which turn on the respective transistors. Ex. 1001, 2:9-12, 11:11-27. The V1 voltage of Seo does the same. Ex. 1005, [0088].

305. As shown below, the *lower select gate of the selected memory string containing the target memory cells* is Nam's GSL:

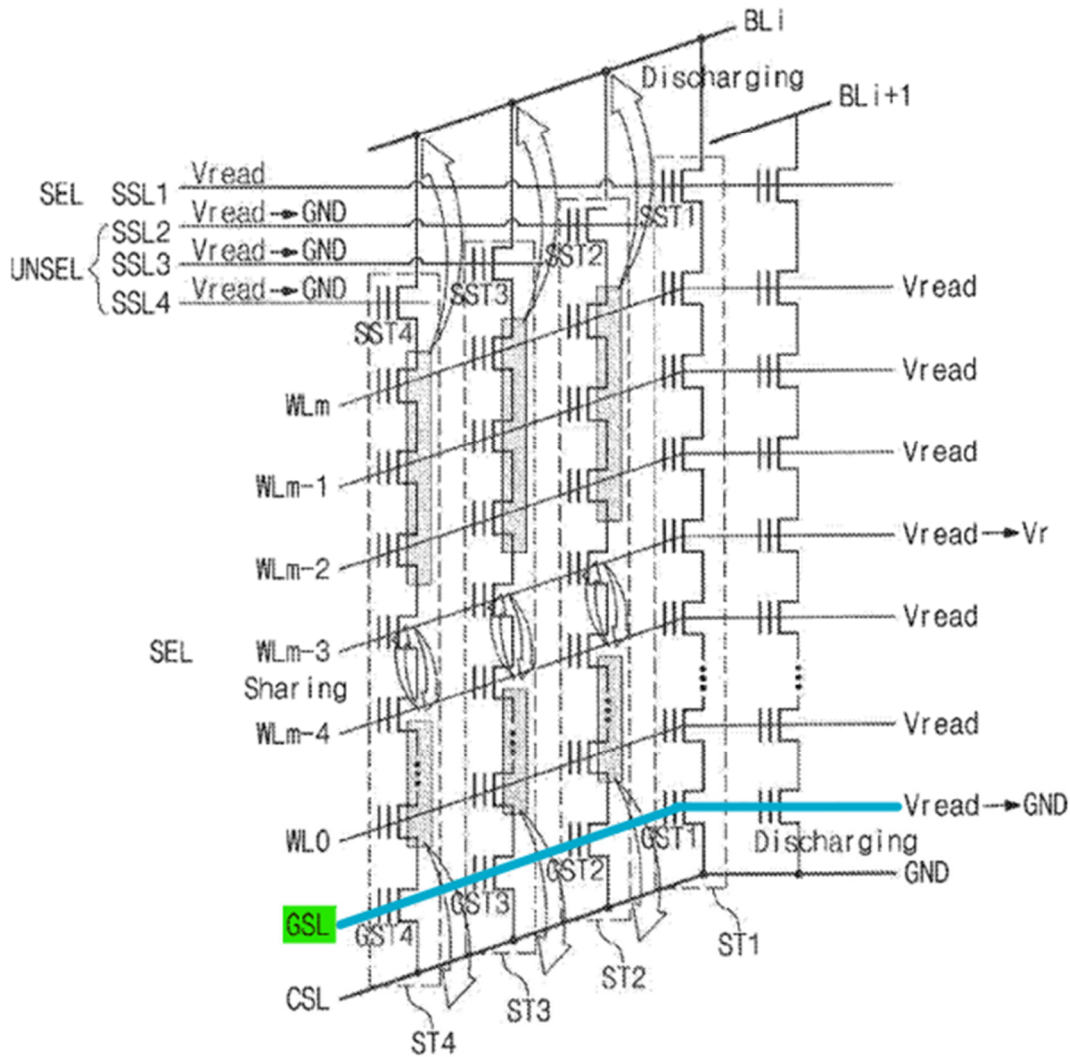
Fig. 2A



Ex. 1006, FIG. 2A (annotated), [0065], [0076]. As shown above and below, Nam does not refer to “selected” GSL or “unselected” GSL, because the GSL (unlike the SSL) is *shared* among what Nam refers to as the selected and unselected strings:

Fig. 3

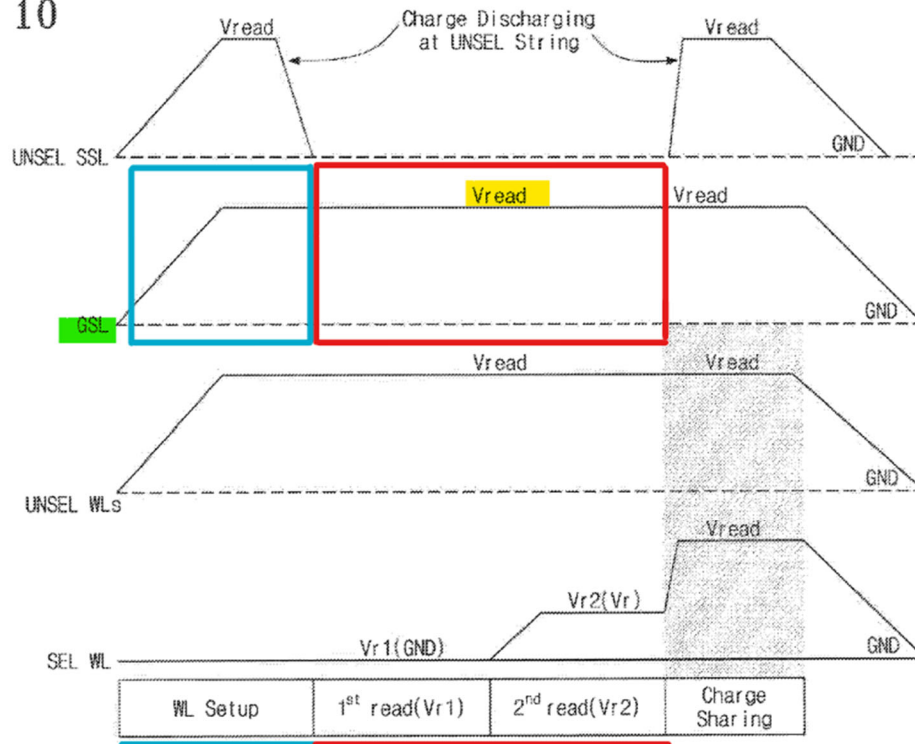
(Prior Art)



Id., FIG. 3 (annotated).

306. And, as further shown below, during *the first time period and the second time period*, Vread (*a lower select gate voltage*) is applied to the GSL:

Fig. 10



Ex. 1006, FIG. 10 (annotated). Vread turns on the transistor. Ex. 1005, [0098].

4. Claim 3

307. Claim 3 depends from claim 2 and further requires:

[3] “wherein the applying the top select gate voltage comprises electrically connecting the selected memory string to a bit line; and the applying the lower select gate voltage comprises electrically connecting the selected memory string to an array common source.”

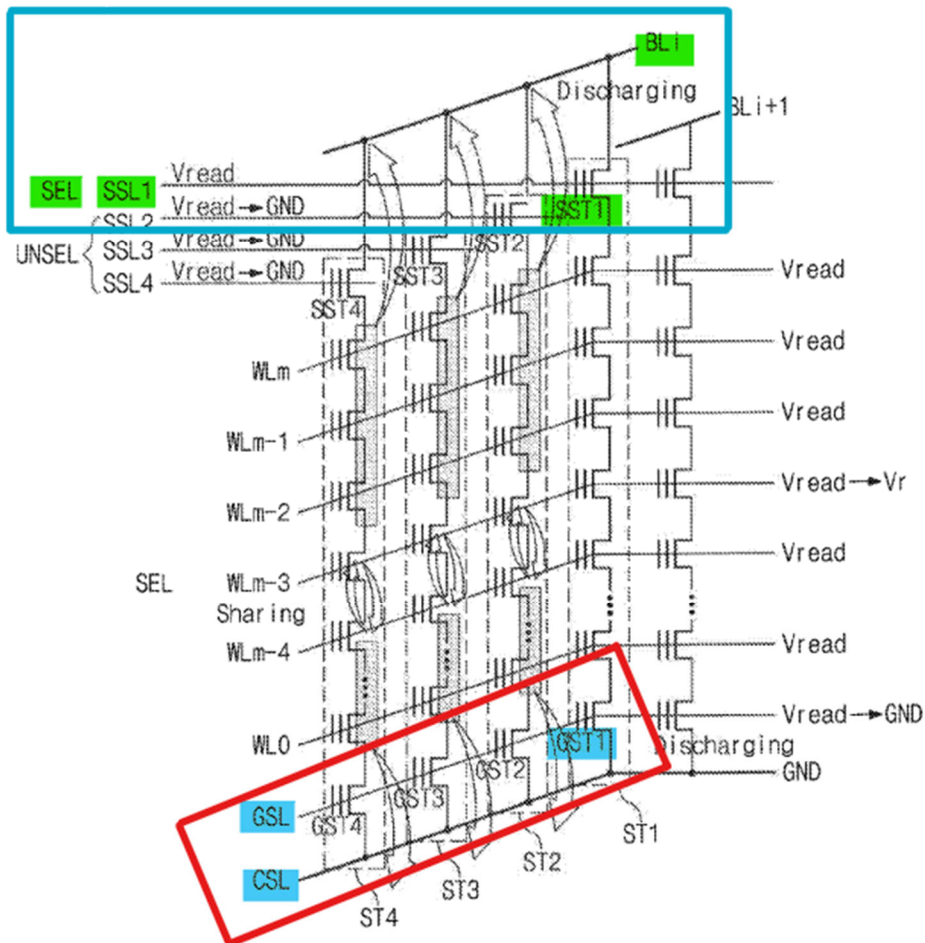
308. Nam discloses this limitation.

309. First, *applying the top select gate voltage* and *applying the lower select gate voltage* in Nam entails applying Vread (see limitation [2.A, 2.B]), which turns on the transistors. Ex. 1006, [0098]. As shown below, turning on *the top select gate*

connects the memory string to the *bit line* and turning on *the lower select gate* connects the memory string to an *array common source* (“CSL”).

Fig. 3

(Prior Art)



Id., FIG. 3 (annotated); [0094] (“For ease of description, it is assumed that a bit line BLi is connected with four strings ST1 to ST4.”); [0100] (“the channel corresponding to memory cells connected with the lower word lines WLm-4 to WL0 is connected with a common source line CSL”). Note that Nam uses a scheme that divides the memory into multiple arrays, and while each array includes a common

source line, those common source lines connect together to form a *single* common source for the device. *Id.*, [0076] (“Each word line cut WL Cut may include a common source line CSL. In exemplary embodiments of the inventive concept, the common source lines CSL included in the word line cuts WL Cuts may be interconnected.”).

5. Claim 5

310. Claim 5 depends from claim 1 and further requires:

[5] “*measuring a threshold voltage of the target memory cell during the second time period.*”

311. Nam discloses this limitation.

312. As Section IX.B.5 demonstrates, this limitation refers to a read operation that compares the memory cell’s threshold voltage to a read voltage to determine its data state (and corresponding threshold voltage). Nam discloses a read operation that *measure[s] a threshold voltage of the target memory cell*, e.g., measuring whether the *threshold voltage* in Nam’s *target memory cell* is P1 or P3. Ex. 1006, [0096] (“a read voltage V_r may be applied to the selected word line W_{Lm-3} ”), [0098] (“Referring to FIG. 4, a ground voltage GND may be used to distinguish an erase state E and a first program state P1. A read voltage V_r may be used to determine the uppermost state P3.”). Nam’s *second time period* is the sensing phase, which is marked by the 1st read and 2nd read period. *See* §IX.D.2[1.B].

6. Claim 6

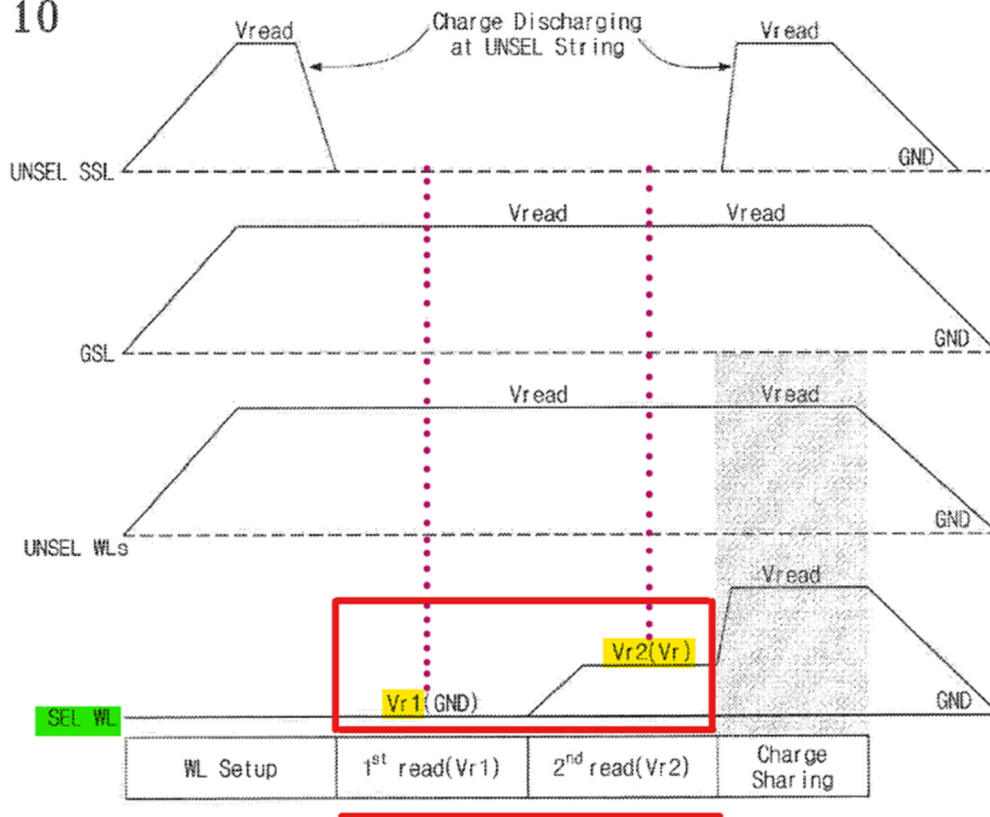
313. Claim 6 depends from claim 1 and further requires:

[6] “wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is higher than a threshold voltage of an unselected memory cell”

314. Nam discloses, or at least renders obvious, this limitation.

315. Recall that *applying the read voltage during the second time*, and more specifically, *applying the read voltage*, refers to when Vr1 and Vr2 are applied.

Fig. 10



Ex. 1006, FIG. 10 (annotated); limitation [1.B].

316. *When* this occurs, the *voltage of the unselected top select gate* is 0 volts.

Limitation [1.A]. The threshold voltage of an unselected memory cell may be any

of its threshold voltages corresponding to E, P1, P2, and P3. Ex. 1006, [0098]. 0 volts is higher than the E state. I explain that this will occur after a block erase and programming progresses past the first row, and the obvious bottom to top and top to bottom programming approaches in §IX.B.6.

7. Claim 8

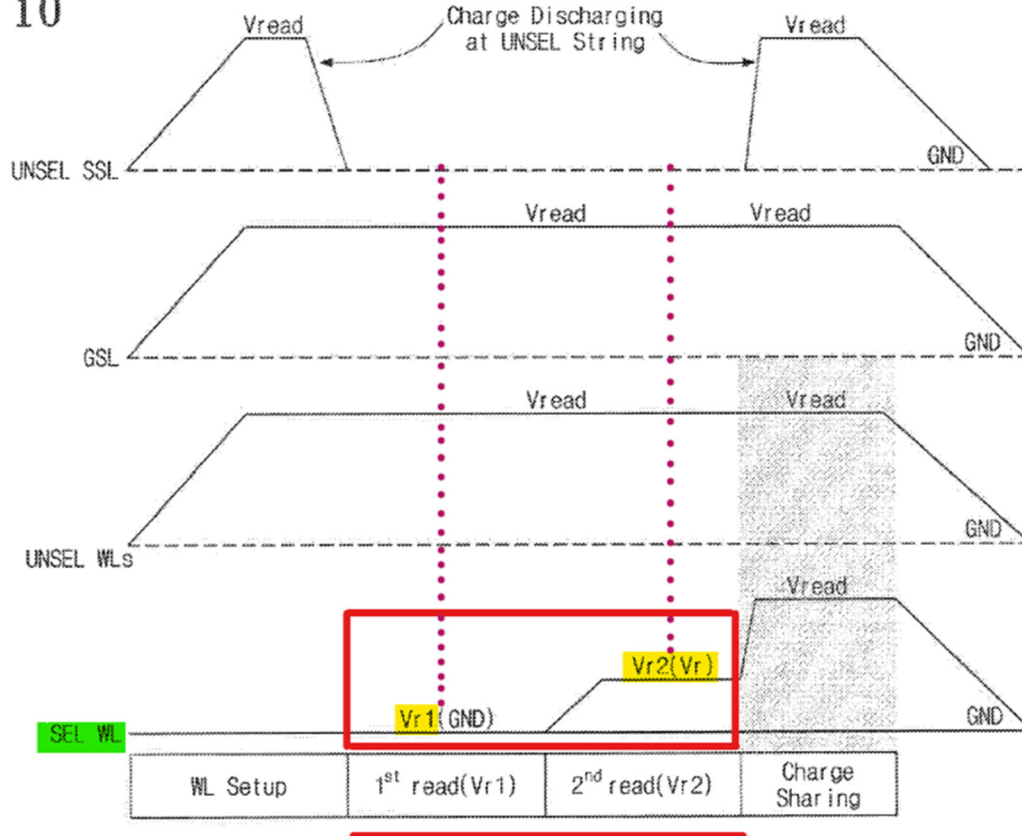
317. Claim 8 depends from claim 1 and further requires:

[8] “wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate is lower than a threshold voltage of an unselected memory cell”

318. Nam discloses this limitation.

319. Recall that *applying the read voltage during the second time*, and more specifically, *applying the read voltage*, refers to when Vr1 and Vr2 are applied.

Fig. 10



Ex. 1006, FIG. 10 (annotated); limitation [1.B].

320. *When* this occurs, the *voltage of the unselected top select gate* is 0 volts.

§IX.D.6. The threshold voltage of an unselected memory cell may be any of its threshold voltages corresponding to E, P1, P2, and P3. Ex. 1006, [0098]. Zero volts is lower than each of the positive voltage levels P1, P2, and P3. *Id.*, [0098], FIG. 4. Nam further discloses that *unselected memory cell[s]* may be programmed. *Id.*, [0095] (“To share boosting charges of the unselected strings ST2 to ST4 before a sensing operation, a read pass voltage V_{read} may be applied to the selected word line WL_m-3 .”).

321. Again, as I have explained, the voltage of an unselected top select gate will be lower than a threshold voltage of an unselected memory cell after a block erase and programming progresses past the first row in the obvious bottom to top and top to bottom programming approaches in §IX.B.6.

322. Accordingly, when Vr1 and Vr2 are applied, Nam discloses that *a voltage of the unselected top select gate* (e.g., 0 volts) *is lower than a threshold voltage of an unselected memory cell* (e.g., positive values P1, P2, and P3).

8. Claim 9

323. Claim 9 depends from claim 1 and further requires that:

[9] “wherein applying the prepare voltage comprises applying a voltage in a range between 4V to 7V”

324. Nam discloses this limitation.

325. Nam discloses that the “read pass voltage,” i.e., *the prepare voltage*, “may be about 7V.” Ex. 1006, [0098].

9. Claim 10

326. Claim 10 depends from claim 1 and further requires:

[10] “wherein applying the pass voltage comprises applying a voltage in a range between 5V to 9V”

327. Nam discloses this limitation.

328. Nam discloses that the “read pass voltage,” i.e., *the pass voltage*, “may be about 7V.” Ex. 1006, [0098].

10. Claim 11

329. Claim 11 depends from claim 1 and further requires:

[11] “wherein applying the off voltage comprises applying a voltage about 0V.”

330. Nam discloses this limitation.

331. Nam discloses that its “ground voltage GND,” i.e., *off voltage*, is, “e.g., 0V.” Ex. 1006, [0100].

11. Claim 12

332. Claim 12 depends from claim 1 and further requires:

[12] “wherein the removing the fast charges comprises: removing the fast charges from a storage layer of the target memory cell.”

333. Nam discloses this limitation, or at least in view of Choi renders it obvious.

334. For the reasons described above, claim 12 involves removing charges trapped in shallow traps of a storage layer of the target memory cell. *See* §§IX.A.3, XI.B.11. This is also known as de-trapping the charges. Nam’s discloses, or at least renders obvious, a charge-trap memory device and creating an electric field that removes fast charges (*see* limitation [1.D]). Thus, Nam discloses, and certainly renders obvious, removing fast charges from the charge-trap layer.

335. Choi likewise teaches a charge-trapping device and discloses that an “electric field” parallel to the memory string pillar creates charge loss from shallow traps after cell programming. Ex. 1007, 1:2-12, 1:13-39. As described above,

Nam's voltage application creates such an electric field to remove charges from "shallow[] trap[s] ... in a charge trap layer." *Id.*, 1:13-39; *supra* limitation [1.D].

12. Claim 13

336. Claim 13 depends from claim 1 and further requires:

[12] "wherein the removing the fast charges comprises: removing electrical charges from shallow traps in the storage layer of the target memory cell."

337. Nam discloses this limitation, or at least renders it obvious in view of Choi.

338. Claims 13 and 12 are substantively identical because the '342 patent refers to "charges trapped in shallow traps" as "fast charges." Ex. 1001, 1:33. The fast charges are trapped in shallow traps in a charge-trap memory. *See* §IX.D.11.

13. Claim 14

339. Claim 14 depends from claim 1 and further requires:

[14] "wherein the removing the fast charges comprises: removing the fast charges from the target memory cell to a neighboring unselected memory cell."

340. Nam discloses this limitation, or at least renders it obvious in view of Choi.

341. As my analysis of claim [1.D] establishes, Nam's read operation involves a voltage differential that creates an electric field that removes fast charges laterally, i.e., to neighboring unselected memory cells. *See* §IX.D.2[1.D]. Further,

as I discuss there, Choi confirms this effect of Nam's read operation. I discuss this lateral movement to neighboring cells in §IX.A.3.

14. Claim 16

342. Claim 16 is an independent claim and requires:

[16.Pre] "A three-dimensional (3D) memory device, comprising:"

343. To the extent this preamble is limiting, Nam's device is *a three-dimensional (3D) memory device*. See §IX.D.2[1.Pre].

[16.A] "a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein:"

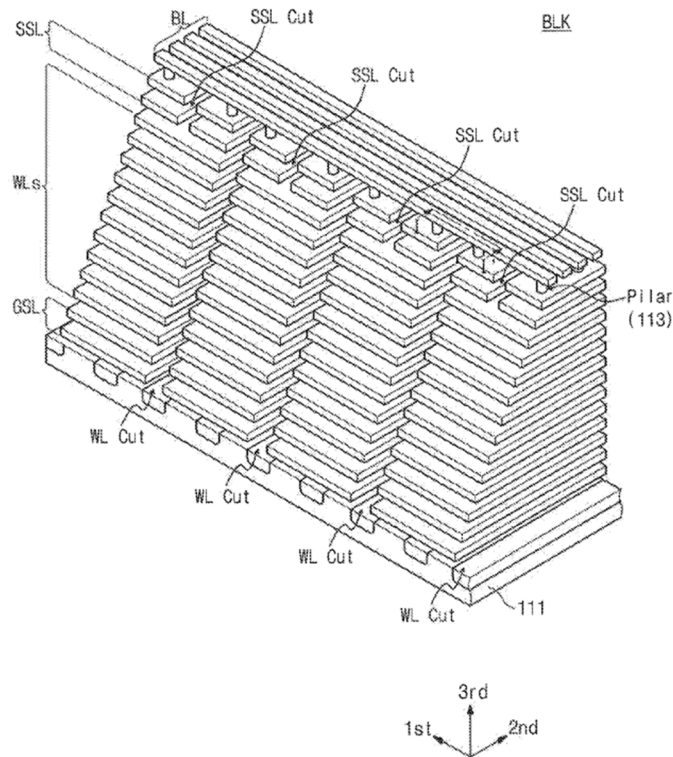
344. Nam discloses this limitation.

345. First, Nam discloses "a memory cell array" that includes "plurality of memory blocks." Ex. 1006, [0063]-[0064], FIG. 1.

346. Second, the memory blocks "include a plurality of strings," each of which include "a plurality of memory cells." Ex. 1006, [0065]. These are vertical memory strings. *Id.*

347. Third, as shown below, Nam discloses a conventional 3D memory stack:

Fig. 2A

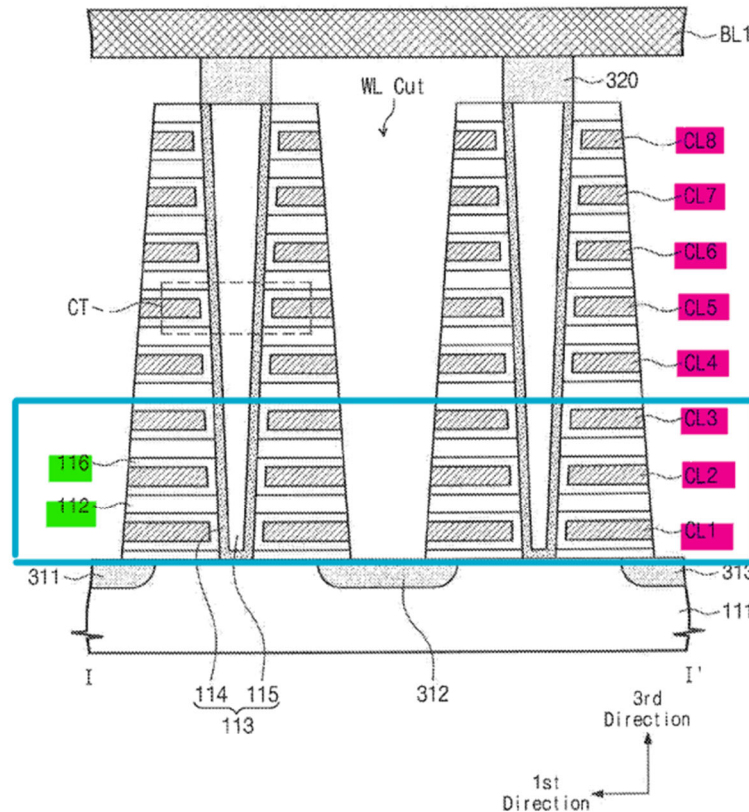


Ex. 1006, FIG. 2A.

348. The above figure depicts the basic alternating stack of dielectric (to isolate the gate layers) and conductive layers (the gate layers) of a 3D NAND flash memory. Ex. 1006, [0164]. With reference to FIG. 2B below, Nam further discloses that “a plurality of insulation materials 112 may be provided sequentially along a third direction.” *Id.*, [0082]. This may be an oxide. *Id.* Additionally, “[i]nsulation films 116 may be provided on exposed surfaces of the insulation materials 112” *Id.*, [0086]. And, in spaces “between” these insulation film layers, “conductive materials CL1 to CL8” are “placed[.]” *Id.*, [0088], [0092]. This refers to the

conventional memory stack of a 3D memory. The conductive gate layers must have insulating layers between them to electrically isolate the gate layers.

Fig. 2B



Id., FIG. 2B (annotated).

349. Finally, Nam discloses that “[a] string may be formed by making a pillar 113 connected with a bit line BL penetrating the at least one string selection line SSL, the word lines WLs, and the at least one ground selection line GSL.” Ex. 1006, [0076]. That is, these *memory strings extend vertically* through the *film stack*. I discuss this conventional 3D memory structure in §VI.A.

[16.A.i] “each memory string comprises a plurality of memory cells; and”

350. Nam discloses this limitation.

351. Nam discloses a “a plurality of *strings*,” each of which include “a *plurality of memory cells*.” Ex. 1006, [0065]. The gate layers intersect with the strings at the location of the memory cells.

[16.A.ii] “each memory cell is addressable through a word line and a bit line; and”

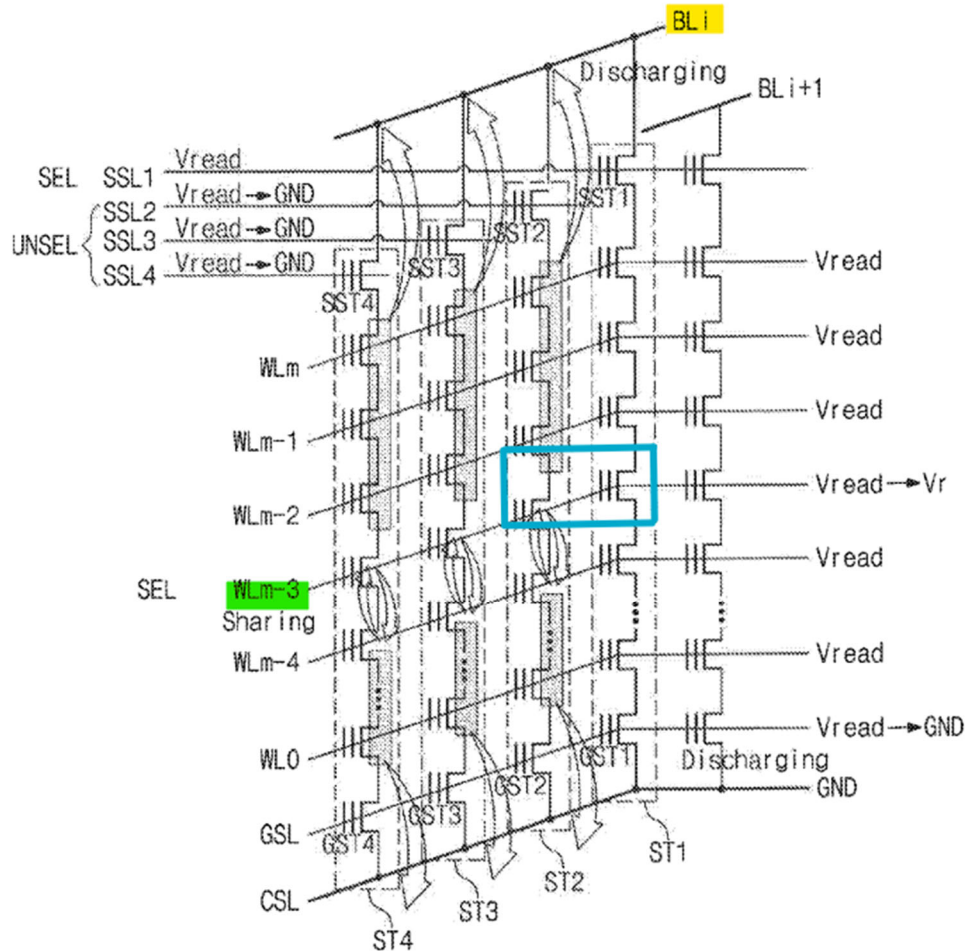
352. Nam discloses this limitation.

353. Nam’s memory device contains an “address decoder 120.” Ex. 1006, [0063]. A decoder in a memory translates memory addresses to identify the target physical location in memory, e.g., a row (word line) and column (bit line). Nam’s memory array can be “connected to the address decoder” via “word lines WLs.” *Id.*, [0064], [0094], [0096]. Similarly, the “memory cell array” can be “connected to the input/output circuit 130” via “bit lines BLs.” *Id.*, [0064]. The bit line and a respective word line intersect at a respective memory cell. The address decoder receives an external address (e.g., from a host system or controller) and uses the word lines and bit lines to access the array. *Id.*, [0066]-[0067].

354. Further, *each memory cell is addressable through a word line and a bit line* as shown below:

Fig. 3

(Prior Art)



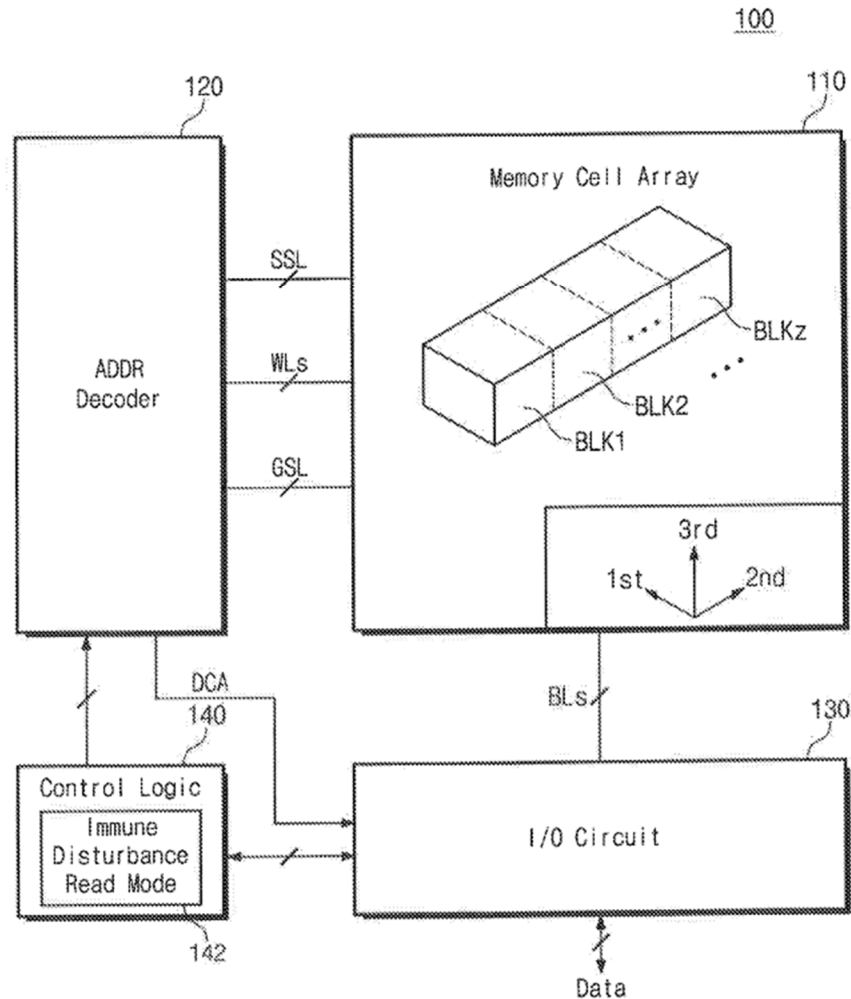
Ex. 1006, FIG. 3 (annotated).

[16.B] “a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:”

355. Nam discloses, or at least renders obvious, this limitation.

356. As to *a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation*, the high-level components of Nam are shown below:

Fig. 1



Ex. 1006, FIG 1. Nam discloses that “[t]he control logic 140 may control an overall operation of the nonvolatile memory device 100 including ... a read operation....” *Id.*, [0069]. Thus, the control logic controls the applications of the voltages in

limitations [1.A]-[1.C]. Thus, Nam discloses *a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation.*

357. As to *for removing fast charges during a first time period*, I describe how Nam's read operation does this under limitation [1.D]. Note that this occurs via Nam's voltage differential during WL Setup, i.e., *the first time period*. See §IX.D.2[1.D].

[16.B.i] “apply, on an unselected top select gate of an unselected memory string, a prepare voltage during the first time period and an off voltage during a second time period”

358. This limitation is identical to Limitation [1.A] except for using “apply” instead of “applying,” and is met for the same reasons set forth therein.

[16.B.ii] “apply, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and”

359. This limitation is identical to Limitation [1.B] except for using “apply” instead of “applying,” and is met for the same reasons set forth therein.

[16.B.iii] “apply, on an unselected word line, a pass voltage during the first time period and the second time period”

360. This limitation is identical to Limitation [1.C] except for using “apply” instead of “applying,” and is met for the same reasons set forth therein.

15. Claim 17

361. Claim 17 depends from claim 16 and further requires:

[17] “wherein the circuit is further configured to: electrically connect a selected memory string containing the target memory cell to the bit line and an array common source by applying a top select gate voltage on a selected top select gate and applying a lower select gate voltage on a lower select gate during the first time period and the second time period.”

362. This limitation is substantively the same as claims 2 and 3, namely, requiring (here by the *circuit*) that top and lower select gate voltages create connections, respectively, to the bit line and array common source, and is met for the same reasons set forth therein (as to *circuit*, see *supra* §IX.D.14[16.B]).

16. Claim 19

363. Claim 19 depends from claim 16 and further requires:

[19.A] “a channel hole”

[19.B] “a core filling film in a center of the channel hole;”

[19.C] “a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, a storage layer and a tunneling layer; and”

[19.D] “a channel layer sandwiched between the memory film and the core filling film.”

364. Nam in view of Choi renders these additional limitations obvious for the same reasons that Seo in view of Choi renders them obvious; namely, Choi discloses these additional limitations. See §IX.B.17.

17. Claim 20

365. Claim 20 depends from claim 19 and further requires:

[20] “wherein the circuit is further configured to remove the fast charges from a portion of the storage layer associated with the target memory cell.”

366. This limitation is substantively the same as claim 12, namely, requiring (here by the *circuit*) removing fast charges from a portion of the storage layer, and is met for the same reasons set forth therein (as to *circuit*, see §IX.D.14[16.B]).

18. Motivation to Combine

367. A POSITA would have found it obvious and would have been motivated to apply Choi’s teachings to Nam regarding fast charge removal and charge-trap memory cells for several reasons.

368. First, both Nam and Choi address issues in the field of 3D NAND flash memory relating to read operations. Ex. 1006, [0013]-[0017], [0030]; Ex. 1007, 1:14-26. And Choi describes the device physics underlying fast-charge loss. Thus, a POSITA would have been motivated to consider Choi to understand and improve on Nam’s memory device. In particular, Choi discusses a driving force of fast-charge loss and how it can affect a read-verification. As Nam relates to read-verification (see [1.Pre], [1.D]), a POSITA would have been motivated to consider Choi in implementing Nam’s read operation to determine how the fast-charge loss may impact Nam’s read operation.

369. Second, Nam focuses on post-read disturbance (after the sensing stage) while Choi focuses on fast-charge loss (which occurs immediately after a program). §§IX.A.2-3. Thus, Choi's teachings are particularly instructive to Nam's WL Setup, which Nam does not detail. Thus, a POSITA would have been motivated to consider Choi's teachings to improve and understand issues relating to the WL Setup period. And again, because Nam expressly contemplates using its read operation for verification, Choi's teachings about the time in which verification occurs would have been understood to be particularly instructive.

370. Third, as I explain in limitation [1.D], Nam creates a voltage differential by applying a higher voltage on unselected word lines than on the selected word lines during the first time period (WL Setup) and, as I explain in limitation [1.D], Nam discloses the use of the read operation on a charge-trap memory. A POSITA knew of the fast-charge loss issue in these memories and would have thus been motivated to consider Choi, because Choi expressly evaluates the fast-charge loss issue and the impact of Nam's voltage differential (by considering the corresponding electric field).

371. Fourth, while Nam does not detail its charge-trap memory cell disclosures, Choi details the various components and the fast-charge loss issue within the specific structural context of the charge-trap components. I discuss how

Choi recognizes the benefits of charge-trap memories, which is one of two basic types of Flash memory in §IX.B.19.

372. A POSITA would have had a reasonable expectation of success in applying Choi's fast-charge-removal teachings to Nam for several reasons.

373. First, as explained above, Nam's memory is structurally similar to Choi's from a high-level perspective. *Compare* Ex. 1006, FIGs. 2A, 2B, 5 with Ex. 1007, FIGs. 1, 5. Specifically, both are conventional 3D memories. Thus, one would expect Choi's teachings to be applicable to Nam.

374. Second, Choi teaches the effect of the voltage differential (and corresponding electric field) of Nam's read operation. Put another way, Choi effectively explains Nam's operational characteristics. A POSITA would have thus understood Nam's device more precisely in view of Choi, including the timing of the effect of the voltage differential relative to a verification.

375. Third, Choi makes it clear that Nam's read operation would remediate fast charge issues in a verification that occurs close in time to a program operation. This would have been confirmation to a POSITA that Nam's read operation was advantageous for verification.

376. Fourth, charge-trap memory was textbook material in 2019. *See* §§VI.B, IX.B.19.

E. Ground 4: Claim 15 Is Obvious Over Nam in View of Choi and Izumi

1. Claim 15

377. Claim 15 depends from claim 1 and further requires:

[15] “wherein conducting the read-verification operation comprises conducting a failed bit count in parallel.”

378. Nam in view of Choi and Izumi renders this additional limitation obvious for the same reason that Seo in view of Choi and Izumi renders it obvious. *See* §IX.C.1.

379. A POSITA would have found it obvious to combine Nam with Izumi. First, a POSITA would have been motivated to incorporate Izumi’s failed-bit count into Nam because Izumi teaches an improvement over Nam’s existing ECC embodiment. Read operations of nonvolatile NAND memory devices were subject to various factors affecting their accuracy, e.g., read disturb and failure to due to endurance limitations. *See, e.g.*, Ex. 1006, [0159]; Ex. 1007, 1:16-20. Nam’s disclosure regarding both read-disturb-effect improvement and ECC shows that Nam sought to address multiple read issues. The basic use of ECC in both Nam and Izumi was a well-known mechanism for detecting and correcting failed bits. Ex. 1008, [0003]-[0004]. But Izumi teaches an approach of selectively activating one or two ECC circuits to tailor ECC capability to the device condition, thereby reducing power consumption. *Id.*, [0078], [0082]. Put simply, Izumi teaches only

discloses a 2D NAND flash, failed bits are a concern regardless of the dimensionality of the flash, and that Izumi's failed-bit-count and ECC techniques also apply to 3D NAND flash. The failure of bits is a result of endurance limitations, and this limitation is present on both 2D and 3D devices. Nam demonstrates this by including an ECC circuit in its memory devices. Ex. 1006, FIG. 22, [0171]-[0173].

381. Thus, a POSITA would have found it obvious that Izumi's disclosure of failed-bit counting and ECC can be incorporated with Nam's ECC circuit. And a POSITA would have had a reasonable expectation of success combining them because they disclose analogous and compatible components, and both disclose using ECC for failed-bit correction. Thus, combining their known techniques on a conventional NAND device would have had a predictable result.

382. As explained above, Choi simply renders explicit a POSITA's understanding that Nam's read-verification operations remove fast charges. *See* §IX.D.2[1.D]. Therefore, Choi has no impact on combining Izumi's failed-bit count into Nam's device.

F. Secondary Considerations of Non-Obviousness

383. Based on my review of the '342 patent's prosecution history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims.

Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342
Declaration of David Kuan-Yu Liu, Ph.D.

384. I am not separately aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, copying, or the like. Instead, as discussed above, it is my opinion that the subject matter embraced by the '342 patent's claims was known in and obvious over the prior art. Moreover, it is also my opinion that the teachings of the prior art would have been expected to successfully function as, or be usable with, working 3D NAND memory devices.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: April 26, 2024

Location: Fremont, California

Signature: 

DR. DAVID KUAN-YU LIU