Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory

Bongsik Choi[1], Sang Hyun Jang[2], Jinsu Yoon[1], Juhee Lee[1], Minsu Jeon[1], Yongwoo Lee[1], Jungmin Han[1], Jieun Lee[1], Dong Myong Kim[1], Dae Hwan Kim[1], Chan Lim[2], Sungkye Park[2], and Sung-Jin Choi[1]*

[1]School of Electrical Engineering, Kookmin University, Seoul 02707, Korea, [2]R&D Division, SK hynix Inc., Icheon, Gyeongki 17336, Korea

Phone: +82-2-910-5543, Fax: +82-2-910-4449, E-mail: sjchoiee@kookmin.ac.kr

Abstract

A fast charge loss within a few seconds, which is referred to as early retention, was observed in tube-type 2y word-line stacked 3-D NAND flash memory for the first time, and the origin of the early retention was comprehensively evaluated. Using a fast-response pulse *I-V* system, the early retention characteristics from microseconds to seconds were thoroughly investigated, and the correlations with various program and erase levels were examined using solid and checkerboard patterns. Our findings indicate that the early retention mainly originates from the lateral charge loss through the shared charge trap layers and suggest that the program and erase levels should be balanced and optimized to reduce the early retention.

Introduction

Due to scaling down limits, increasing process cost, and reliability issues in planar NAND flash memory, 3-D NAND flash memory has been considered to be a very promising candidate [1-3]. Although 3-D NAND flash memory with a charge trap layer (SiN) has many merits, the retention characteristics stemming from lateral charge loss are expected to cause problems because the charge trap layers are shared between word-lines (WLs) (Fig. 1). Therefore, a fast charge loss within a few seconds, which we refer to as 'early retention,' can be observed and can cause unwanted results in a negative shift of the threshold voltage (V_T) and a positive shift of the string read current immediately after programming. This early retention threatens multi-level cell (MLC) capability (Fig. 2) and product-level reliability requirements. It has been reported that early retention can take place predominately through vertical charge loss via the tunnel or block oxide immediately after programming resulting from the shallowly trapped electrons in a charge trap layer [2]. However, we observed that severe early retention can occur through a lateral charge loss as well in the WL stacked 3-D NAND structure because of the inevitably shared charge trap layer between WLs (Fig. 3). Therefore, in this work, for the first time, we comprehensively evaluate the early retention behaviors from the lateral charge loss point of view using diverse test situations, such as various program and erase levels, and a fast-response pulse *I-V* system in tube-type 3-D NAND flash memory. Moreover, early retention on the cell states, i.e., solid and checkerboard pattern (S/P and C/P), has been thoroughly characterized (Fig. 4).

Measurement Result and Discussion

Fig. 5 shows a TEM cross-section image and the core device structure of the 2y WL stacked tube-type 3-D NAND flash memory, which is referred to as 'SMArt', used in this work [3]. Fig. 6(a) shows the conventional DC *I-V* measurement sequences for characterizing the early retention. The initialization step was performed to assure all cells were erased before programming. The early retention under various program levels (PV1, PV2, and PV3) was measured at 90 ºC (Fig. 6(b)). Note that the early retention rapidly occurred within 1 min, which necessitates the measurement of the early retention within a few seconds for precise analysis. Therefore, we performed fast response pulse *I-V* measurements using incremental step pulse programming (ISPP) followed by immediate retention measurements (Fig. 7(a)). The reading phase is enabled (delay < 100 μsec) immediately after programming so that accurate early retention characteristics were obtained. The string read current was first measured (Figs. 7(b) and 7(c)) and then transformed into early retention defined as $V_{T,loss}$ (Fig. 8). First, we measured the early retention characteristics in the states of the cells, i.e., S/P and C/P, under various PV levels, as shown in Fig. 8. It should be noted that the early retention is obviously aggravated by increasing PV levels in both states. Importantly, these results showed a clear opposite trend to a previous report in which a greater PV level showed a greater $V_{T,loss}$, i.e., worsened early retention due to increased vertical charge loss [2].

To further evaluate the origin of the observed trends, we performed a TCAD simulation by considering the erasing operation in the initialization step. Thus the cell was first erased prior to programming to describe real measurement sequences. Fig. 9 shows the simulated profiles of trapped electrons and holes in a charge trap layer for different PV levels for the S/P. At the lower PV level, it is clearly observed that there were a large number of residual holes that are not fully compensated by the trapped electrons during programming. During erasing, the holes injected into the charge trap layer can spread outside of cells due to the relatively longer erasing time and the high diffusivity of the holes [4]. Therefore, the trapped electrons from the lower PV level cannot completely compensate the injected holes resulting in residual holes. As a result, a large lateral electric field is generated at the edge of the cell in which there is a greater chance for stored charges in a charge trap layer to spread laterally. To confirm the influence of the non-compensated residual holes on the early retention, additional measurement were performed by varying the erasing levels (EV1, EV2, and EV3) in the initialization step (Fig. 10). As expected, a greater EV level as well as a lower PV level resulted in worsened early retention due to residual holes. This observation indicates that the early retention mainly occurs through lateral charge loss in the shared charge trap layers rather than vertical charge loss.

Figs. 11 and 12 also show the simulation and measurement results of early retention in a C/P. It is clearly observed that the trends of the early retention for various PV and EV levels were similar in the S/P and the C/P, but the dependence of the early retention on the PV levels for the C/P was less than for the S/P (Fig. 13). That is, the early retention was easily relaxed with increasing PV levels in the S/P but not in the C/P. Moreover, it is worthwhile to note that the overall early retention was more severe in the C/P than in the S/P. Fig. 14 shows the simulated conduction band edge profile (E_C) of the SiN and the corresponding lateral electric field in the S/P and the C/P. We confirm that for the C/P, the lateral electric field was mostly governed by the erased state of neighboring cells. However, for the S/P, the lateral electric field was specifically determined from the non-compensated residual holes. In addition, more electrons could be trapped between the WLs at a greater PV level in the S/P due to the strong fringing electric field, which effectively compensated for the injected holes during erasing (Fig. 15). Therefore, the dependence of the early retention on the PV levels was more noticeable in the S/P. Note that our findings suggest that both PV and EV levels should be optimized and balanced in the S/P and the C/P to minimize the early retention (Fig. 16).

Conclusion

We comprehensively evaluated the early retention in WL stacked tube-type 3-D NAND flash memory for the first time. We found that the early retention rapidly occurs within a few seconds and primarily originates from the lateral charge loss through the shared charge trap layer. The early retention was shown to be much worse for the C/P than for the S/P. Moreover, by measuring the early retention under various PV and EV levels, we concluded that the non-compensated residual holes at the edge of the cells play a significant role in early retention and, thus, should be optimized and balanced.

References

[1] J. Jang et al., VLSI Tech. Dig., p. 192, 2009. [2] C.-P. Chen et al., IEEE IEDM, p 118, 5, 2010. [3] E.-S. Choi et al., IEEE IEDM, p 211, 2012. [4] C. Kang et al., IRPS, pp. 167-169, 2007.

Micron Ex. 1007, p. 1
Micron v. YMTC
IPR2024-00793

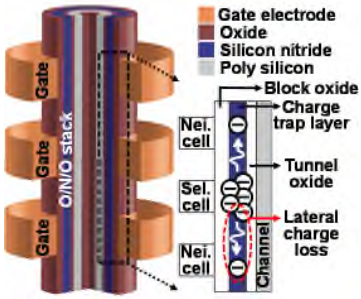

Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

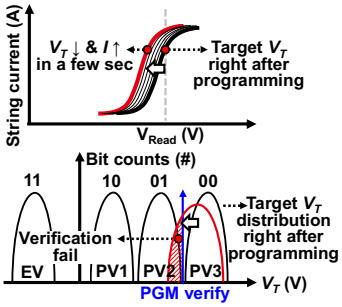

Fig. 2. Schematic of the early retention and its effect on V_T and I. The early retention threatens the MLC capability and the tight V_T distribution.

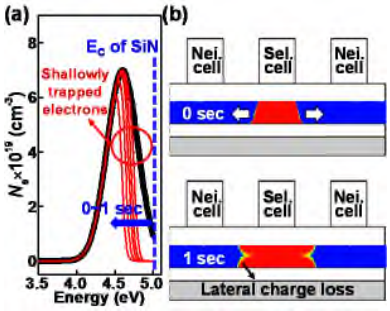

Fig. 3. (a) Simulated energy distribution of trapped electrons during the retention time (1 sec): input trap level (black line) and extracted trap levels (red line). (b) Simulated contours of the redistribution of the trapped electrons during the retention time (1 sec).

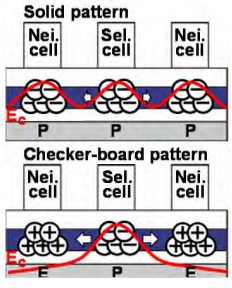

Fig. 4. (a) Schematic of the trapped electrons and holes at two different cell states, such as a S/P and a C/P. The E_C of SiN is also shown for the comparison.

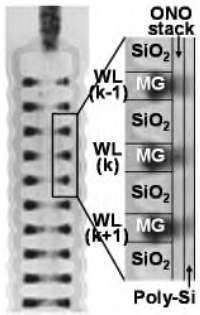

Fig. 5. TEM image of the tube-type 2y WL stacked 3-D NAND flash memory used in this work.

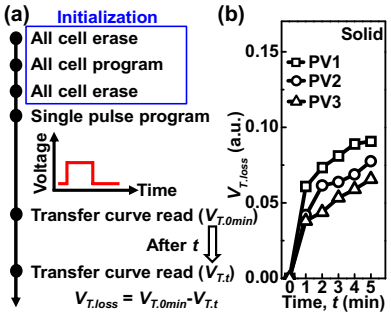

Fig. 6. (a) Sequences of the conventional DC *I-V* measurements. The early retention ($V_{T,loss}$) was measured by reading the transfer curves. (b) $V_{T.loss}$ vs. retention time. The fast charge loss occurred within 1 min.

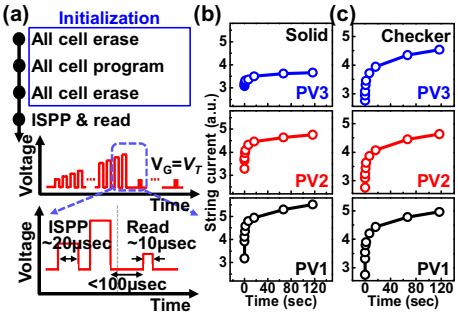

Fig. 7. (a) Sequences of the pulse *I-V* measurements. The ISPP was used for programming. String current vs. retention time from μsec to 120 sec as a parameter of the PV levels for the (b) S/P and (c) C/P.

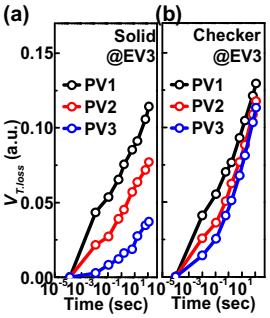

Fig. 8. Transformed early retention ($V_{T.loss}$) vs. retention time as a parameter of the PV levels for the (a) S/P and (b) C/P.

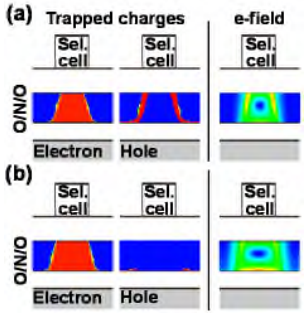

Fig. 9. Simulated contours of the trapped electrons and holes and corresponding electric field for (a) a small PV level and (b) a large PV level for the S/P.

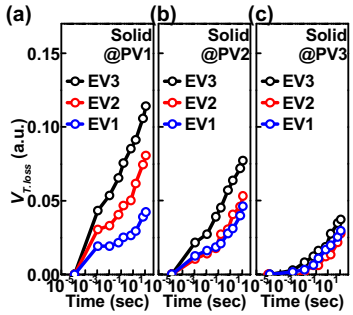

Fig. 10. $V_{T.loss}$ vs. retention time as a parameter of EV levels for different PV levels: (a) PV1, (b) PV2, and (c) PV3 for the S/P.

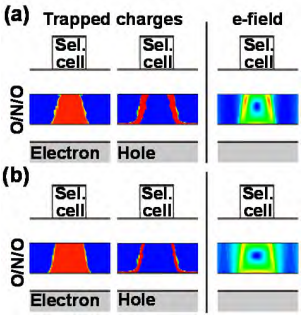

Fig. 11. Simulated contours of the trapped electrons and holes and the corresponding electric field for (a) a small PV level and (b) a large PV level for the C/P.

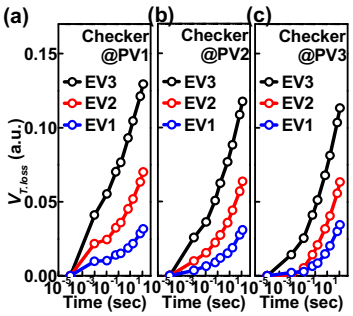

Fig. 12. $V_{T.loss}$ vs. retention time as a parameter of the EV levels for different PV levels: (a) PV1, (b) PV2, and (c) PV3 for the C/P.

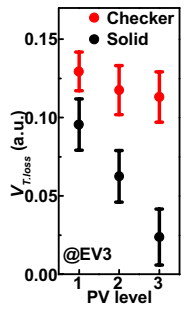

Fig. 13. Comparison of the early retention between the S/P and the C/P at a large EV level.

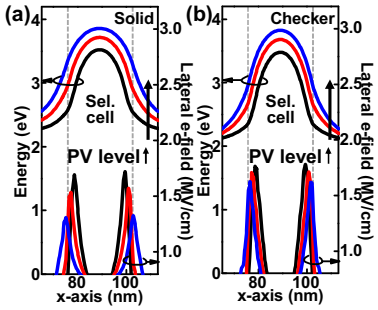

Fig. 14. Simulation of the E_C of SiN and the lateral electric field for (a) the S/P and (b) the C/P. The lateral electric field was more influenced by increasing the PV levels in the S/P than in the C/P.

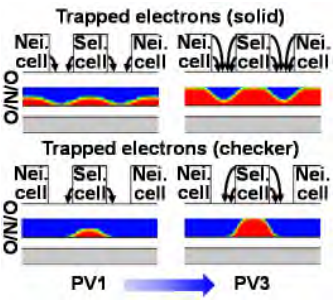

Fig. 15. Simulation of the trapped electrons in the S/P and the C/P. The trapped electrons between WLs in the S/P can easily compensate for the injected hole during erasing.

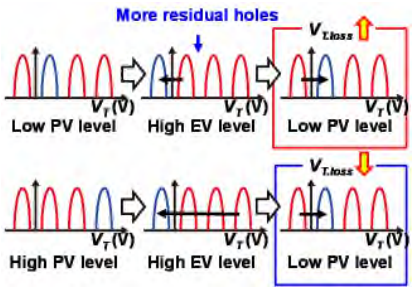

Fig. 16. Historical dependences of the early retention. The specific sequence, which was low PV level → high EV level → low PV level, may result in aggravated early retention due to residual holes at the edge of the selected cell. Therefore, balanced PV/EV levels are necessary.

Acknowledgement: This work was supported by SK Hynix Inc. and NRF (2013R1A1A1057870).

Micron Ex. 1007, p. 2
Micron v. YMTC
IPR2024-00793