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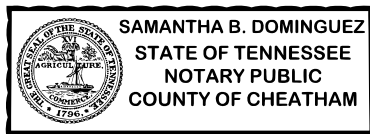
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EXHIBIT A

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2016 VLSI TECHNOLOGY SYMPOSIUM

2016 VLSI CIRCUITS SYMPOSIUM

2016 VLSI Technology and Circuits

ABOUTPROGRAMPLENARY, PANELS and LUNCHEONCOURSES & WORKSHOPSAUTHORSATTENDEESMEDIA

PROGRAM

Home → PROGRAM

VLSI Program

Schedule of Events:

Tuesday, June 14

Joint Reception – Palace Lounge, 7:15 p.m. – 8:00 p.m.
Joint Technology/Circuits Panel Session – Tapa II, 8:00 p.m. – 10:00 p.m.
Technology Panel Session – Tapa I, 8:00 p.m. – 10:00 p.m.

Wednesday, June 15

Executive Panel – Coral Ballrooms 4 & 5, 5:20 p.m. – 6:50 p.m.
Joint Luau Banquet – Great Lawn, 7:00 p.m. – 9:00 p.m.

Thursday, June 16

Luncheon Talk – Nautilus Suite, 12:15 p.m. – 1:30 p.m.
Solid State Circuits Society Young Professionals, Honolulu Lanai, 6:00 p.m. – 8:00 p.m.
Circuits Evening Panel Sessions, Tapa I and II, 8:00 p.m. – 10:00 p.m.

Friday, June 17

Solid State Circuits Society 30th Symposium on VLSI Circuits Luncheon for SSCS Members, Honolulu Suite, 12:15 p.m. – 1:30 p.m.

For full program information, click on the buttons below.

Technology Program

Circuits Program

Program at a Glance - PDF

Program Glance - Excel (download)

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Conference Schedule

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2016 Symposia on VLSI Technology and Circuits announces call for papers

The official Call for Papers has been issued for the 2016 Symposia on VLSI Technology and Circuits, to be held at the Hilton Hawaiian Village June 13-16, 2016 (Technology) and June 15-17, 2016 (Circuits). The deadline for paper submissions to both conferences is January 25, 2016. The late-news paper submissions deadline for the Symposia on VLSI Technology is March 24, 2016; there is no late-news submission for the Symposium on VLSI Circuits. Complete details for paper submission can be found online at: <http://www.vlissymposium.org/authors/>

For the past 28 years, the combined annual Symposia on VLSI Technology and Circuits has provided an opportunity for the world's top device technologists, circuit and system designers to engage in an open exchange of leading edge ideas at the world's premier mid-year conference for microelectronics technology. Held together since 1987, the Symposia on VLSI Technology and Circuits have alternated each year between sites in the US and Japan, enabling attendees to learn about new directions in the development of VLSI technology & circuit design through the industry's leading research and development presentations.

The comprehensive technical programs at the two Symposia are augmented with short courses, invited speakers and several evening panel sessions. Since 2012, the Symposia have presented joint focus sessions that include invited and contributed papers on topics of mutual interest to both technology and circuit attendees.

The Symposium on VLSI Technology seeks technical innovation and advances in all aspects of IC technology, as well as the emerging IoT (Internet of Things) field, including:

- **IoT systems & technologies**, including ultra-low power, heterogeneous integration, sensors, connectivity, power management, digital/analog, microcontrollers and application processors
- **Stand-alone & embedded memories**, including DRAM, SRAM, non-volatile and emerging memory technologies
- **CMOS Technology, microprocessors & SoCs**, including scaling, VLSI manufacturing concepts and yield optimization
- **RF / analog / digital technologies** for mixed-signal SoC, RF front end; analog, mixed-signal I/O, high voltage, imaging, MEMS, integrated sensors
- **Process & material technologies**, including advanced transistor process and architecture, modeling and reliability; alternate channel; advanced lithography, high-density patterning; SOI and III-V technologies, photonics, local interconnects and Cu/optical interconnect scaling
- **Packaging technologies & System-in-Package (SiP)**
- **Photonics Technology & "Beyond CMOS" devices**

The Symposium on VLSI Circuits seeks original papers showcasing technical innovations and advances in the following areas:

- **Digital circuits and processor techniques** for standalone and embedded processors
- **Memory circuits, architectures & interfaces** for volatile and non-volatile memories, including emerging memory technologies
- **Clock generation and distribution** for high-frequency digital and mixed-signal applications
- **Analog and mixed-signal circuits**, including amplifiers, filters and data converters
- **Wireline receivers & transmitters**, including circuits for inter-chip and long-reach applications
- **Wireless receivers & transmitters**, including circuits for WAN, LAN, PAN, BAN, inter-chip and mm-wave applications
- **Power management circuits**, including battery management circuits, voltage regulators, energy harvesting circuits
- **Application-oriented circuits & VLSI systems**, imagers, displays, and sensors for biomedical and

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• **Application-oriented circuits & PCB systems:** imagers, displays, and sensors for biomedical and healthcare applications

Joint technology and circuits focus sessions feature invited and contributed papers highlighting innovations and advances in materials, processes, devices, integration, reliability and modeling in the areas of advanced memories, 3D integration, and the impact of technology scaling on advanced circuit design. Submissions are strongly encouraged in the following areas of joint interest:

- **Design in scaled technologies:** scaling of digital, memory, analog and mixed-signal circuits in advanced CMOS processes
- **Design enablement:** design for manufacturing, process/design co-optimization, on-die monitoring of variability and reliability
- **Embedded memory technology & design:** SRAM, DRAM, Flash, PCRAM, RRAM, MRAM and NVRAM memory technologies
- **3D & heterogeneous integration:** power and thermal management; inter-chip communications, SIP architectures and systems

Papers sought for “big integration”

Authors are encouraged to submit papers that showcase innovations that extend beyond single ICs and into the module, including focus areas in the Internet of Things (IoT), industrial electronics, “big data” management, biomedical applications, robotics and smart cars. These topics will be featured in focus sessions as part of the program.

Best Student Paper Award

Awards for best student paper at each Symposia will be chosen, based on the quality of the papers and presentations. The recipients will receive a financial award, travel cost support and a certificate at the opening session of the 2017 Symposium. For a paper to be reviewed for this award, the author must be enrolled as a full-time student at the time of submission, must be the lead author and presenter of the paper, and must indicate on the web submission form that the paper is a student paper.

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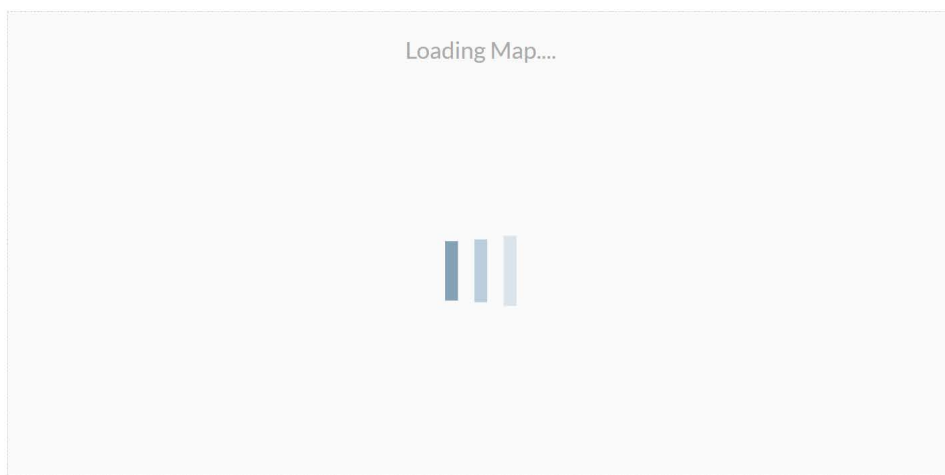
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2016 Symposia on VLSI Technology & Circuits

06/13/2016 - 06/16/2016 - All Day

Location: Hilton Hawaiian Village



The annual Symposium on VLSI Technology and Circuits will be held at the Hilton Hawaiian Village, Honolulu, Hawaii from June 13-16, 2016 (Technology) and June 14-17, 2016 (Circuits). The theme of this year's program is "Inflections for a Smart Society." The program includes focus sessions, panel discussions and short courses, including focus sessions on "Systems & Embedded Memory" and "Interconnect & 3D Integration," and panel discussions, "How Moore's Law, Industry Consolidation and System Trends Are Shaping the Memory Roadmap," "More Moore, More than Moore or Mo(o)re Slowly?"

This year marks the 36th anniversary for the Symposium on VLSI Technology, and the 30th anniversary for the Symposium on VLSI Circuits. The two conferences have been held together since 1987, providing an opportunity for the world's top device technologists, circuit and system designers to exchange leading edge research on microelectronics technology, with alternating venues between Hawaii and Japan.

Sponsoring Organizations

The Symposium on VLSI Technology is sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics, in cooperation with the IEEE Solid State Circuits Society.

The Symposium on VLSI Circuits is sponsored by the IEEE Solid State Circuits Society and the Japan Society of Applied Physics, in cooperation with the Institute of Electronics, Information and Communication Engineers.

Find further information, registration and a complete program at: <http://www.vlssymposium.org>.



UPCOMING EVENTS

2023 Symposium on VLSI Technology & Circuits: Call for Papers Closes Feb. 1
Feb 1, 2023

2022 Phil Kaufman Award Ceremony and Banquet Honoring Dr. Giovanni De Micheli
Feb 23, 2023

TestConX 2023 - Call for Presentations
Mar 5, 2023

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PAST EVENTS

Inaugural Chiplet Summit Set for January 24-26
Jan 24, 2023

SEMICON Japan 2022 to Spotlight
Innovations Driving Semiconductor
Industry Growth

Dec 14, 2022

68th Annual IEEE International
Electron Devices Meeting

Dec 3, 2022

Sitemap

3D In-Depth

What is 3D Integration?
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scaling impact microelectronics business and future industry drivers.

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Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND flash memory

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[▽ Bongsik Choi ; ▽ Sang Hyun Jang ; ▽ Jinsu Yoon ; ▽ Juhee Lee ; ▽ Minsu Jeon ; ▽ Yongwoo Lee ; ▽ Jungmin Han ; ▽ Jieun Lee ; ▽ Dong...](#) [View All Authors](#)

Abstract

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Abstract:
A fast charge loss within a few seconds, which is referred to as early retention, was observed in tube-type 2y word-line stacked 3-D NAND flash memory for the first time, and the origin of the early retention was comprehensively evaluated. Using a fast-response pulse I-V system, the early retention characteristics from microseconds to seconds were thoroughly investigated, and the correlations with various program and erase levels were examined using solid and checkerboard patterns. Our findings indicate that the early retention mainly originates from the lateral charge loss through the shared charge trap layers and suggest that the program and erase levels should be balanced and optimized to reduce the early retention.

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Electron traps, Flash memories, Solids, Programming, Electric fields, Current measurement

INSPEC: Controlled Indexing

logic gates, circuit optimisation, flash memories

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Figures

References

charge trap layers, tube-type 3D NAND flash memory, fast charge loss, early retention, 2y word-line stacked 3D NAND flash memory, fast-response pulse I-V system, erase levels, solid patterns, checkerboard patterns, lateral charge loss

Citations

Keywords

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EXHIBIT B

2016 IEEE Symposium on VLSI Technology (VLSI Technology 2016)

**Honolulu, Hawaii, USA
14-16 June 2016**



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