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YU et al.

(54) **NONVOLATILE MEMORY DEVICE AND METHOD OF PROGRAMMING IN THE SAME**

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G11C 16/04	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 16/16*** (2013.01); ***G11C 16/08*** (2013.01); *H01L 27/11556* (2013.01); ***G11C 16/26*** (2013.01); ***G11C 16/0483*** (2013.01); ***G11C 16/24*** (2013.01)

(57) **ABSTRACT**

To program in a nonvolatile memory device, a memory block is provided with a plurality of sub blocks disposed in a vertical direction where the memory block includes a plurality of cell strings each including a plurality of memory cells connected in series and disposed in the vertical direction. A plurality of intermediate switching transistors are disposed in a boundary portion between two adjacent sub blocks in the vertical direction. Each of the plurality of intermediate switching transistors is selectively activated based on a program address during a program operation. The selectively activating each of the plurality of intermediate switching transistors includes selectively turning on one or more intermediate switching transistors in a selected cell string based on the program address.

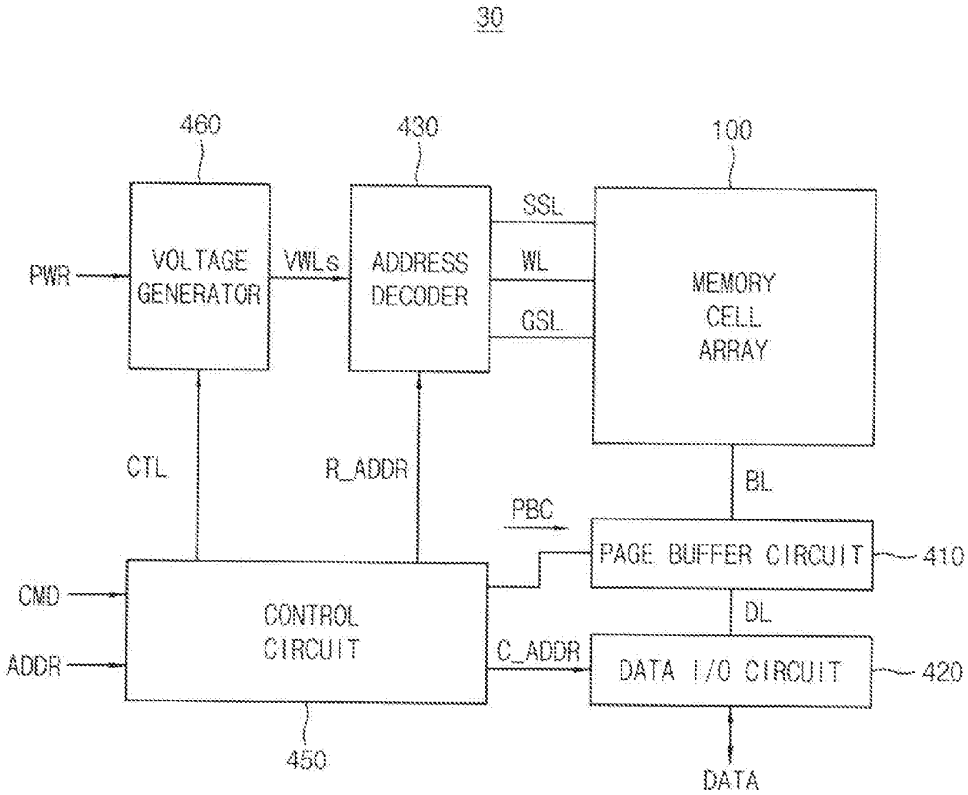


FIG. 1

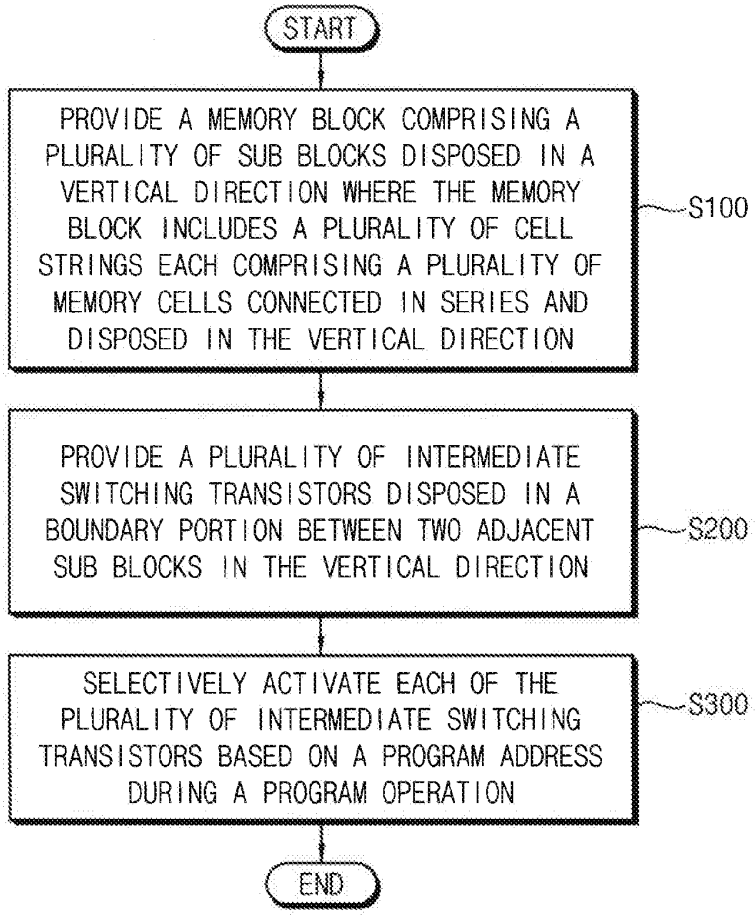

START
PROVIDE A MEMORY BLOCK COMPRISING A PLURALITY OF SUB BLOCKS DISPOSED IN A VERTICAL DIRECTION WHERE THE MEMORY BLOCK INCLUDES A PLURALITY OF CELL STRINGS EACH COMPRISING A PLURALITY OF MEMORY CELLS CONNECTED IN SERIES AND DISPOSED IN THE VERTICAL DIRECTION
S100
PROVIDE A PLURALITY OF INTERMEDIATE SWITCHING TRANSISTORS DISPOSED IN A BOUNDARY PORTION BETWEEN TWO ADJACENT SUB BLOCKS IN THE VERTICAL DIRECTION
S200
SELECTIVELY ACTIVATE EACH OF THE PLURALITY OF INTERMEDIATE SWITCHING TRANSISTORS BASED ON A PROGRAM ADDRESS DURING A PROGRAM OPERATION
S300
END

FIG. 2

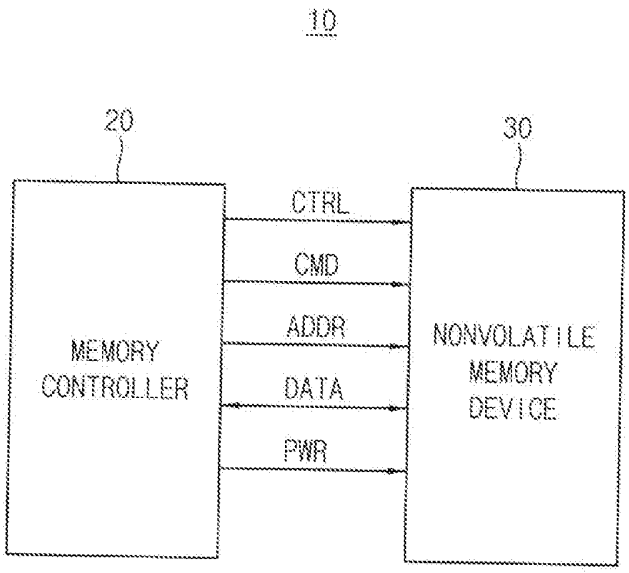

10
20
30
MEMORY CONTROLLER
CTRL
CMD
ADDR
DATA
PWR
NONVOLATILE MEMORY DEVICE

FIG. 3

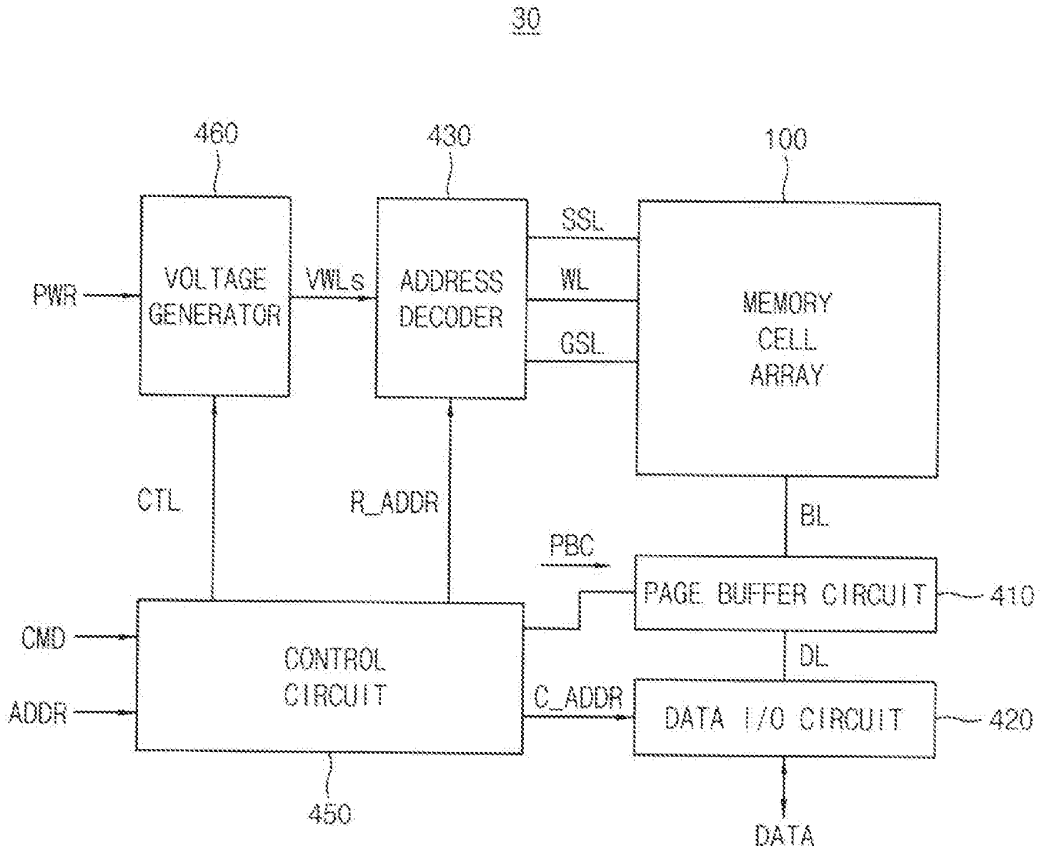

30
460
430
100
PWR
VOLTAGE GENERATOR
VWLs
ADDRESS DECODER
SSL
WL
GSL
MEMORY CELL ARRAY
CTL
R_ADDR
BL
PBC
PAGE BUFFER CIRCUIT
410
CMD
ADDR
CONTROL CIRCUIT
DL
C_ADDR
DATA I/O CIRCUIT
420
450
DATA

FIG. 4

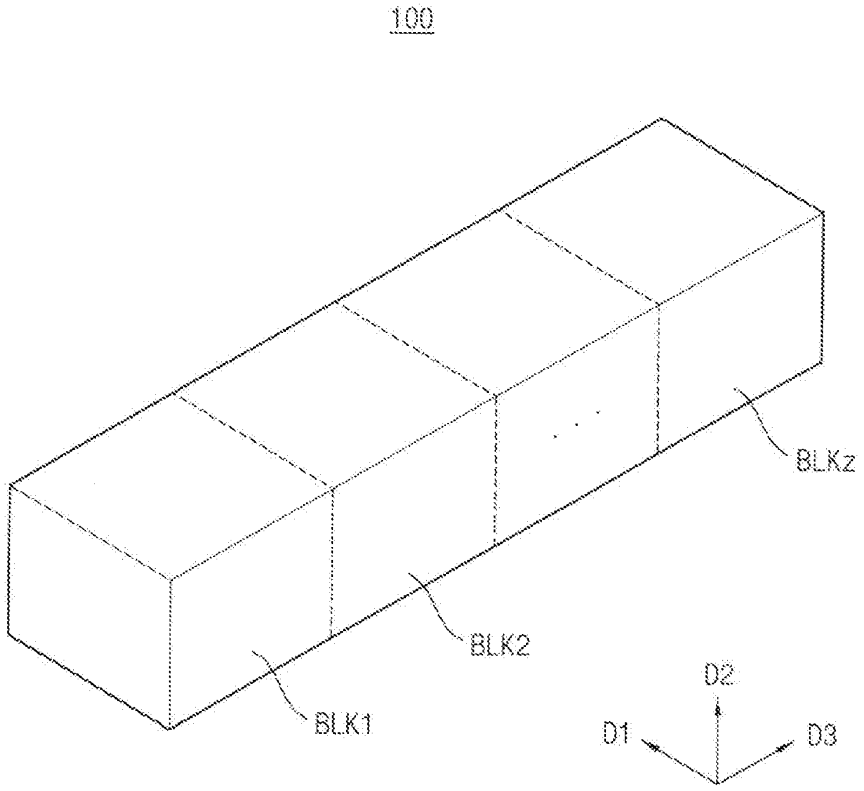


FIG. 5

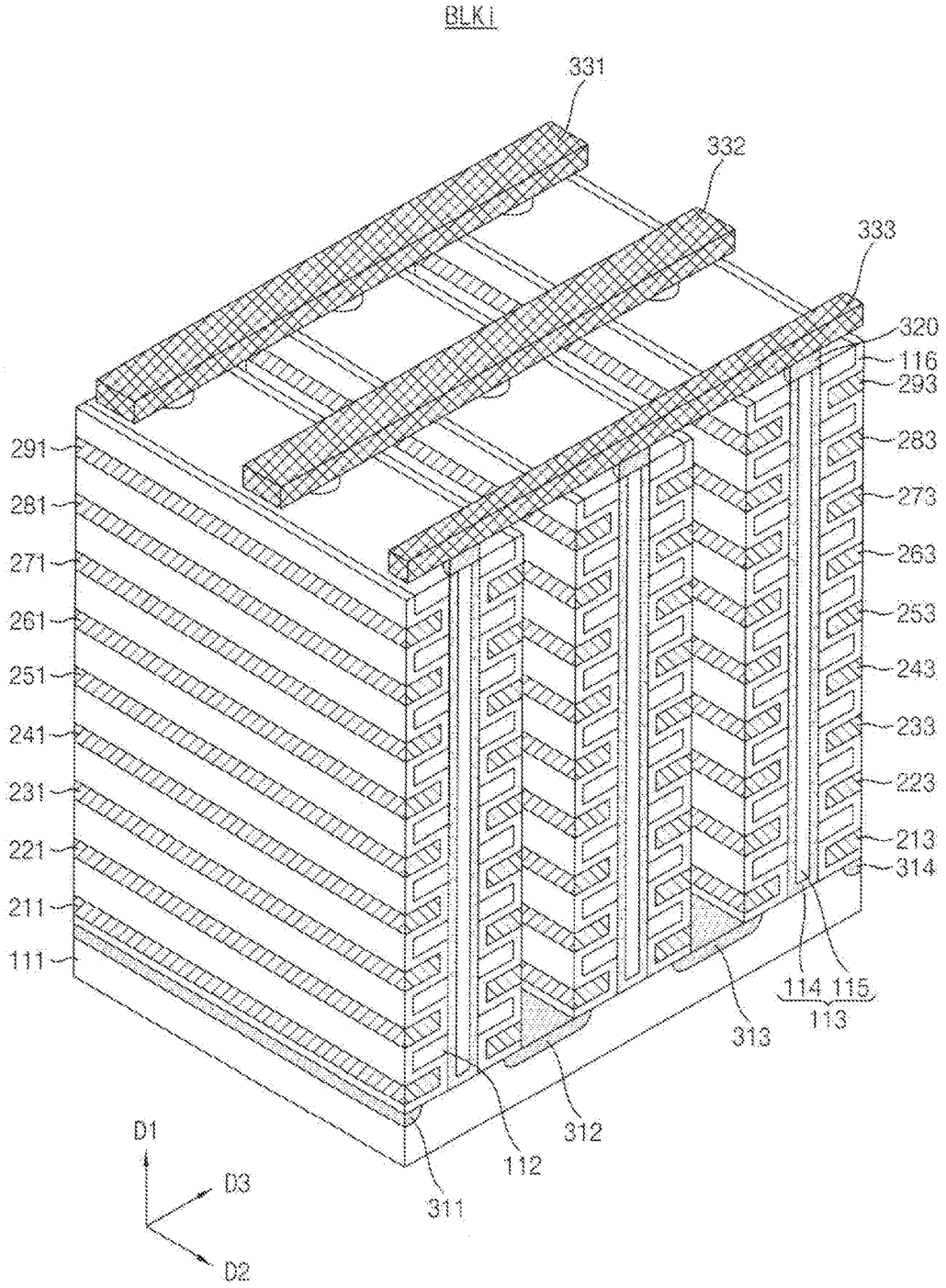

BLK1
331
332
333
320
116
293
283
273
263
253
243
233
223
213
314
291
281
271
261
251
241
231
221
211
111
114 115
113
313
312
112
311
D1
D3
D2

FIG. 6

BLKi

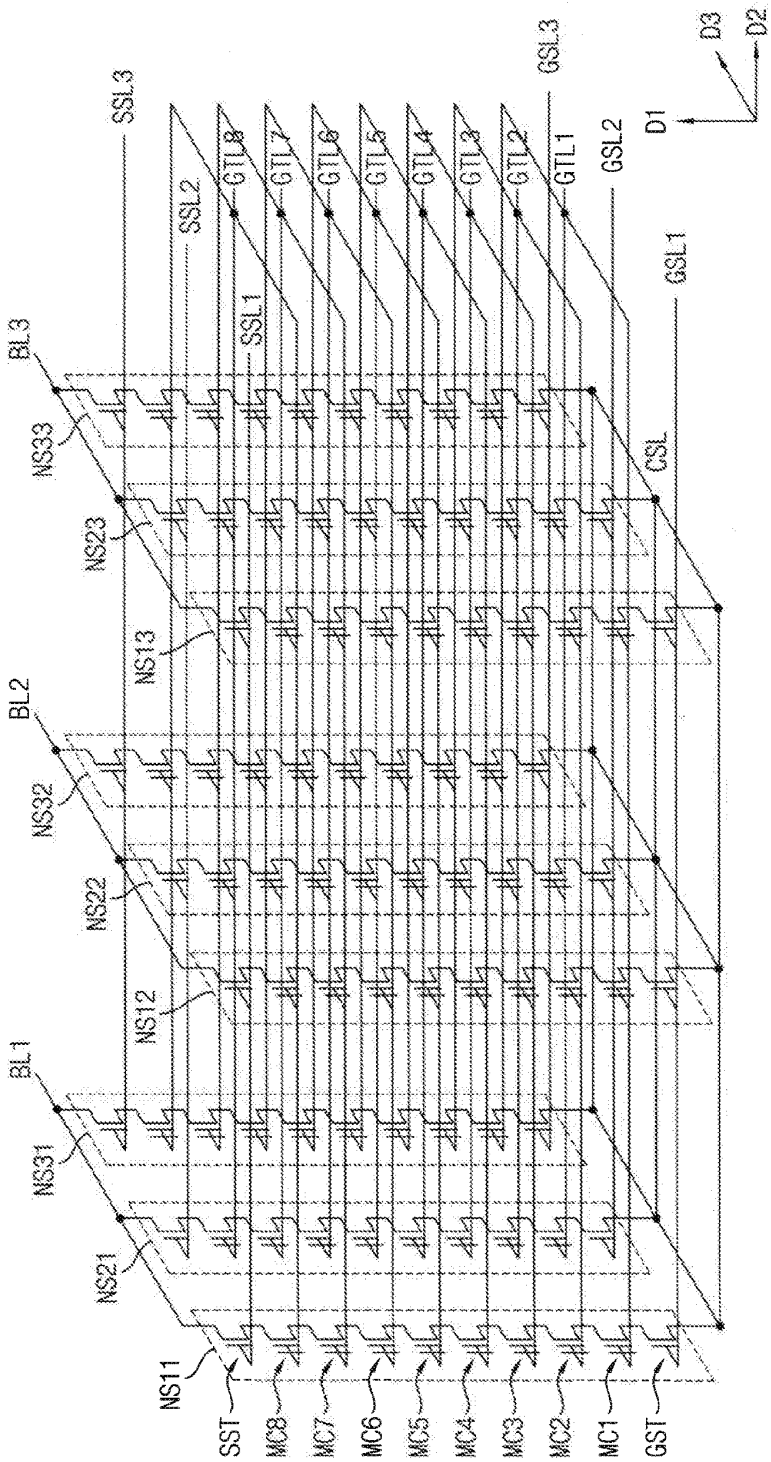

SSL3
SSL2
SSL1
GTL8
GTL7
GTL6
GTL5
GTL4
GTL3
GTL2
GTL1
GSL3
GSL2
GSL1
CSL
D1
D2
D3
BL3
BL2
BL1
NS33
NS23
NS13
NS32
NS22
NS12
NS31
NS21
NS11
SST
MC8
MC7
MC6
MC5
MC4
MC3
MC2
MC1
GST

FIG. 7

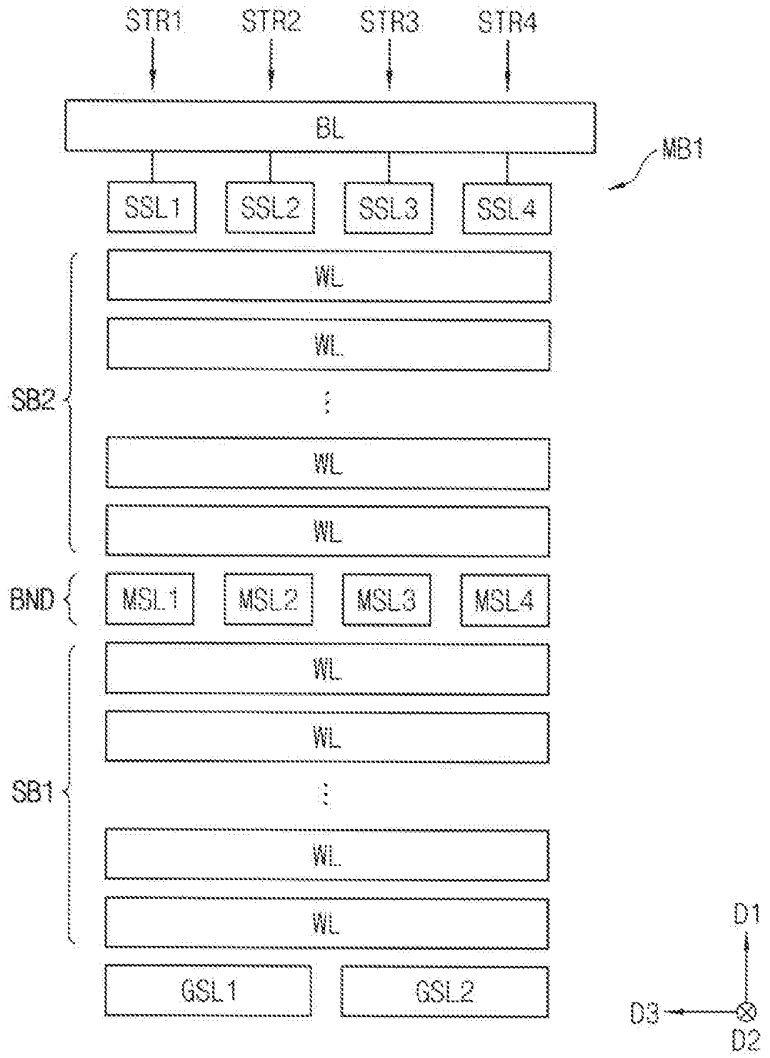

STR1
STR2
STR3
STR4
BL
MB1
SSL1
SSL2
SSL3
SSL4
WL
WL
SB2
WL
WL
BND
MSL1
MSL2
MSL3
MSL4
WL
WL
SB1
WL
WL
GSL1
GSL2
D1
D3
D2

FIG. 8A

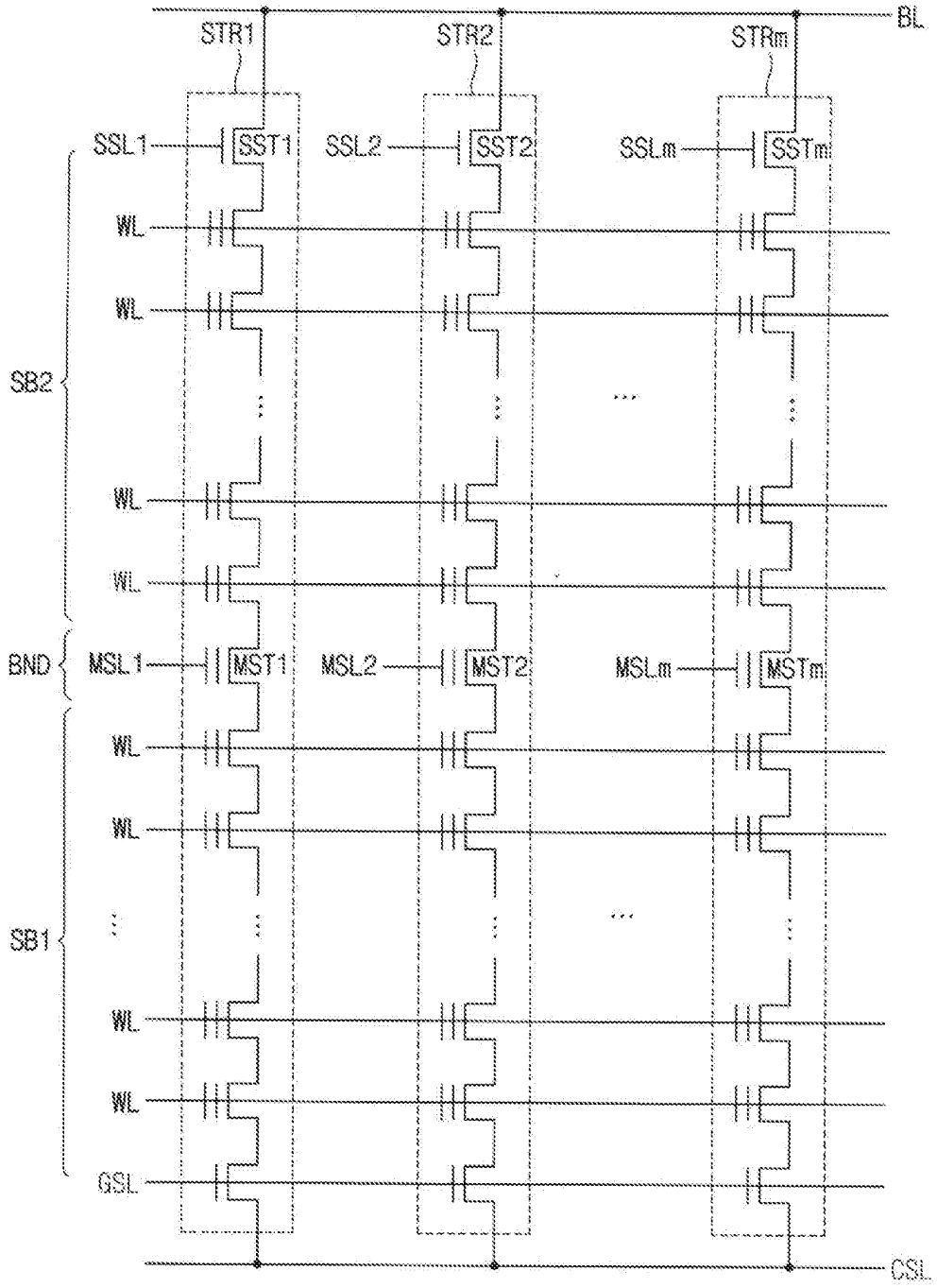

BL
STR1
STR2
STRm
SSL1
SST1
SSL2
SST2
SSLm
SSTm
WL
SB2
BND
MSL1
MST1
MSL2
MST2
MSLm
MSTm
SB1
GSL
CSL

FIG. 8B

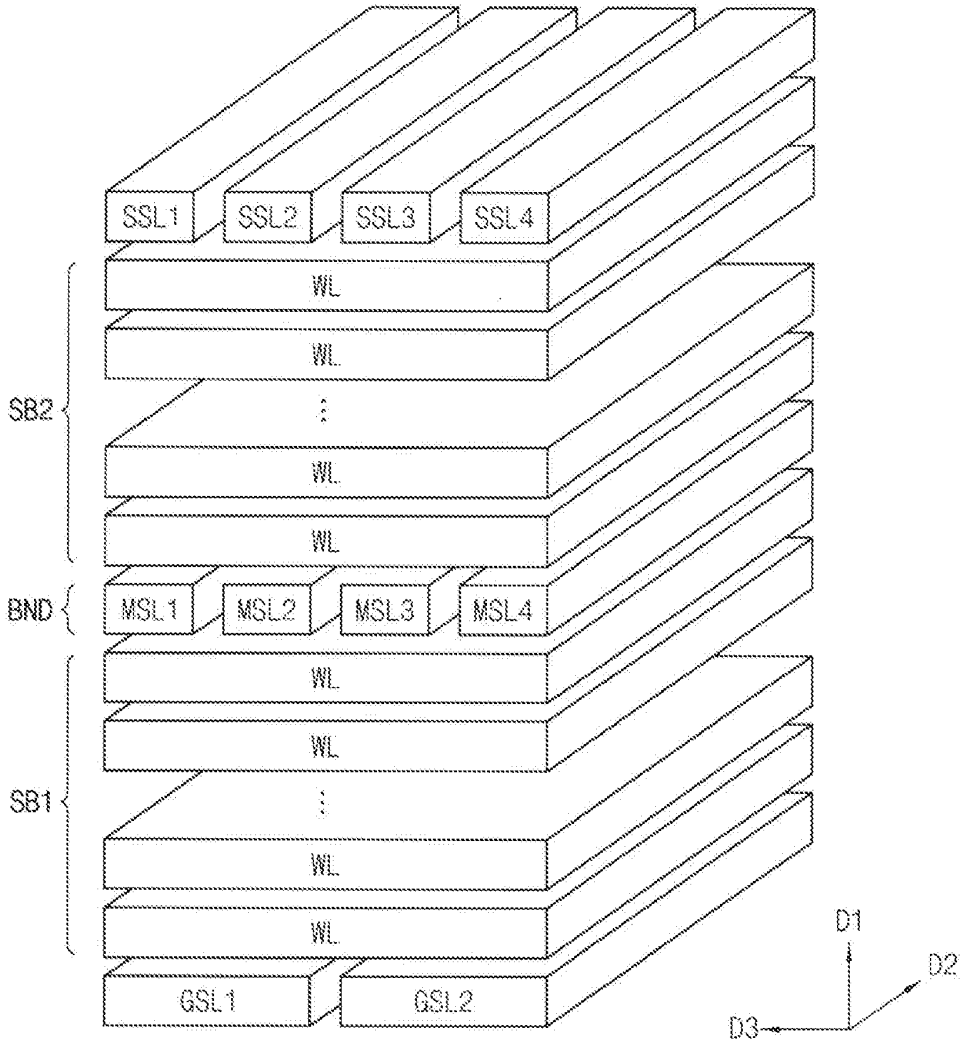

SSL1
SSL2
SSL3
SSL4
WL
WL
SB2
WL
WL
BND
MSL1
MSL2
MSL3
MSL4
WL
WL
SB1
WL
WL
GSL1
GSL2
D1
D2
D3

FIG. 9A

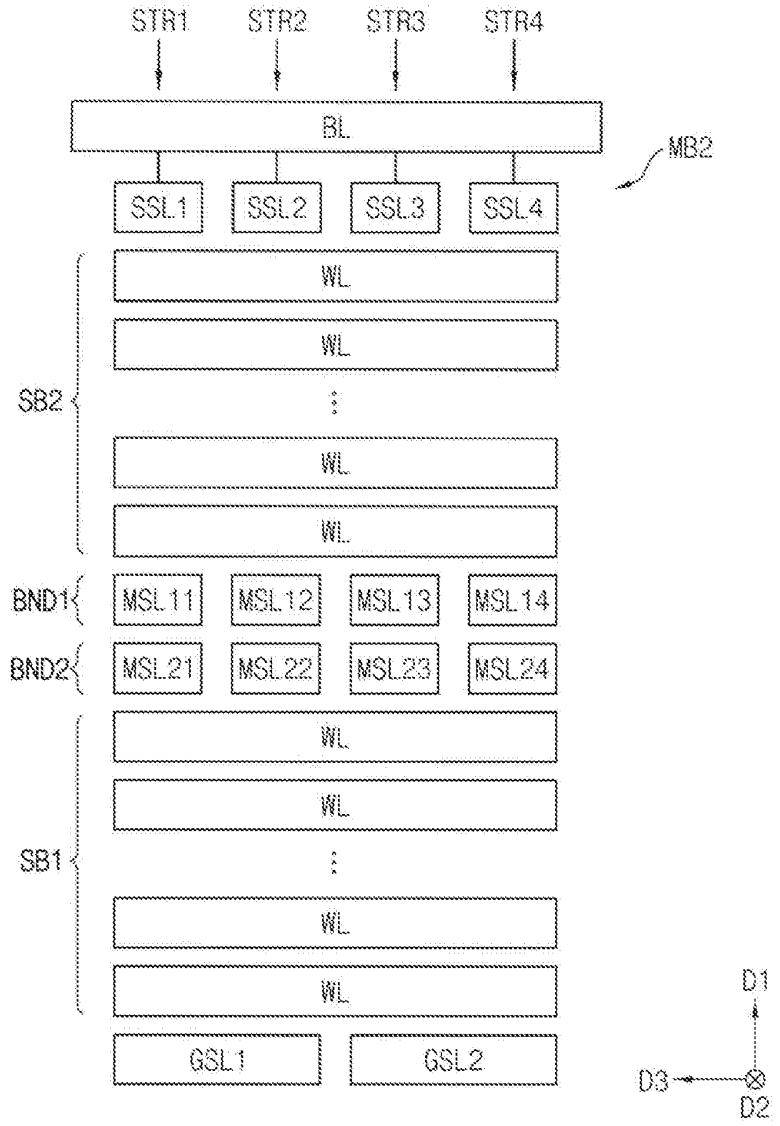

STR1
STR2
STR3
STR4
BL
MB2
SSL1
SSL2
SSL3
SSL4
WL
WL
SB2
WL
WL
BND1
MSL11
MSL12
MSL13
MSL14
BND2
MSL21
MSL22
MSL23
MSL24
WL
WL
SB1
WL
WL
GSL1
GSL2
D1
D3
D2

FIG. 9B

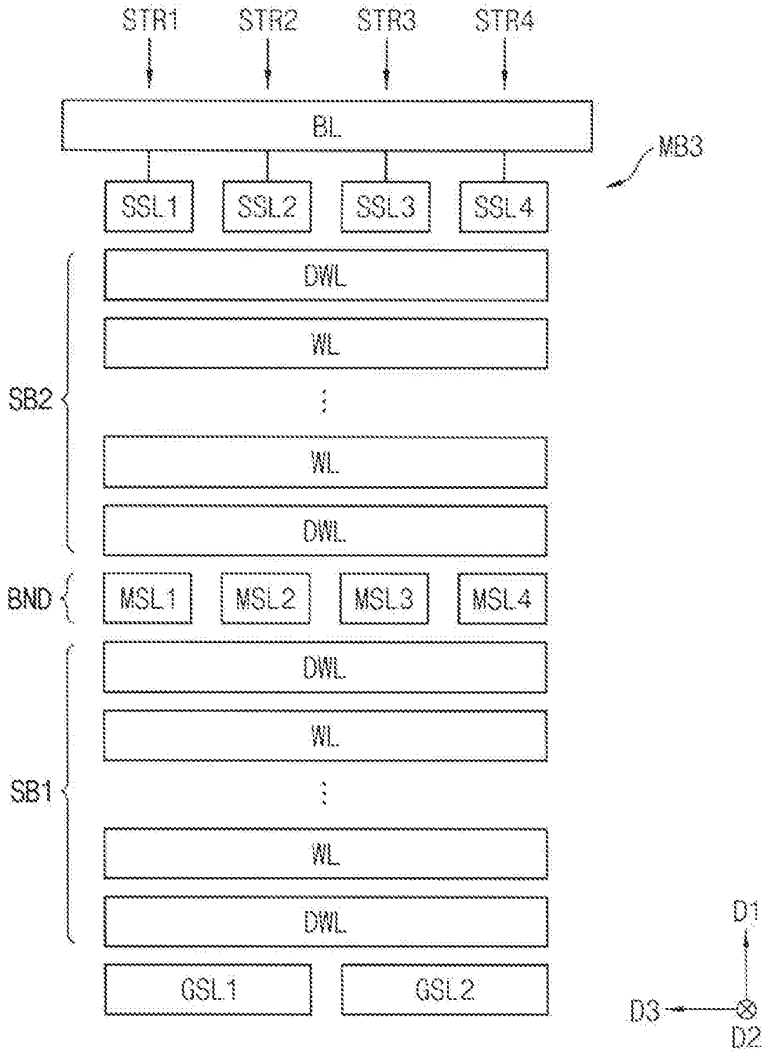

STR1
STR2
STR3
STR4
BL
MB3
SSL1
SSL2
SSL3
SSL4
DWL
WL
SB2
WL
DWL
BND
MSL1
MSL2
MSL3
MSL4
DWL
WL
SB1
WL
DWL
GSL1
GSL2
D1
D3
D2

FIG. 9C

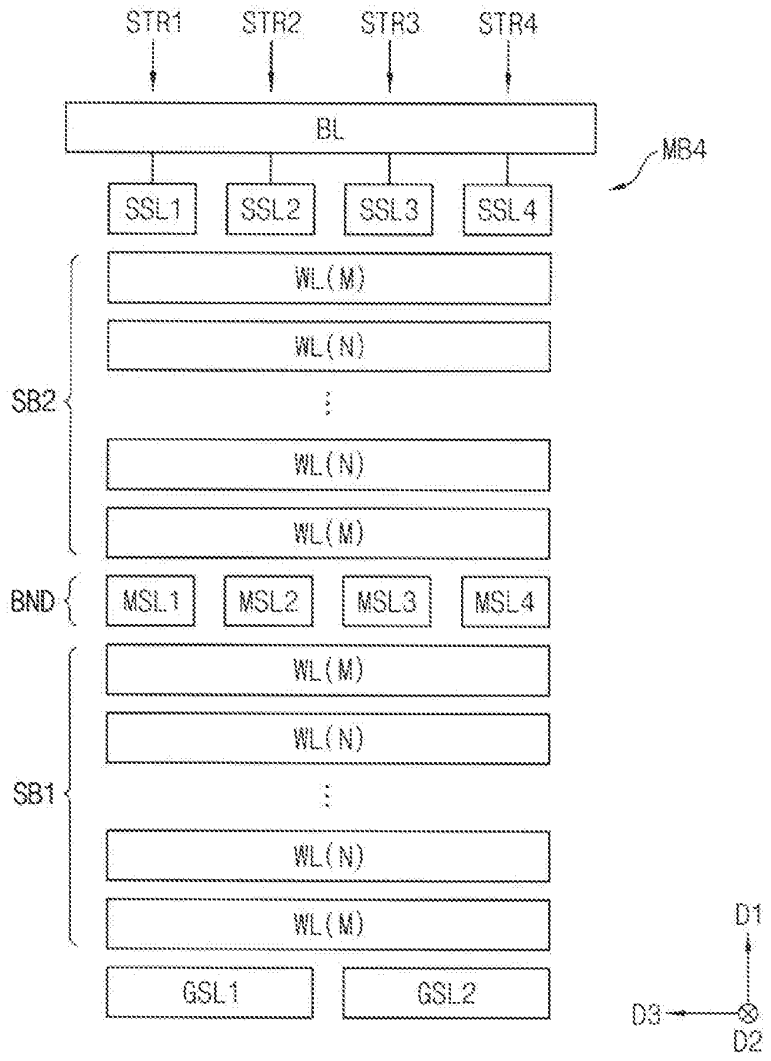

STR1
STR2
STR3
STR4
BL
MB4
SSL1
SSL2
SSL3
SSL4
WL(M)
WL(N)
SB2
WL(N)
WL(M)
BND
MSL1
MSL2
MSL3
MSL4
WL(M)
WL(N)
SB1
WL(N)
WL(M)
GSL1
GSL2
D1
D3
D2

FIG. 9D

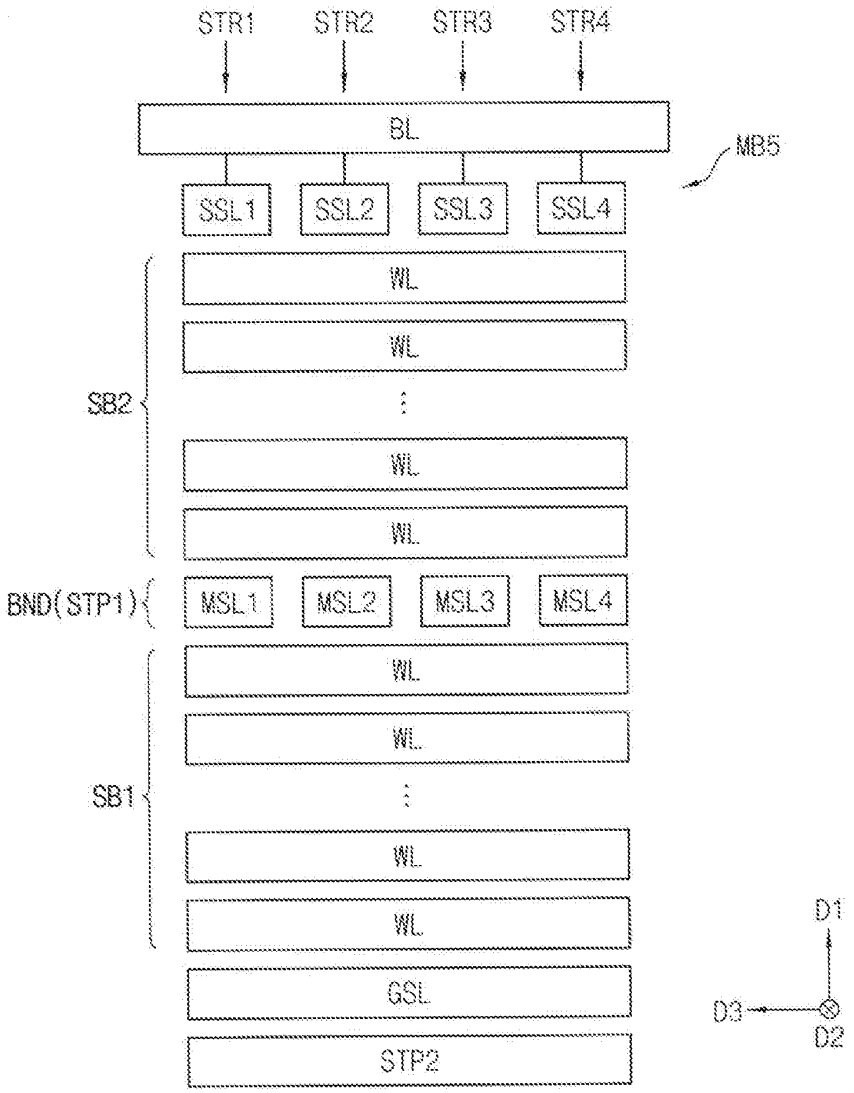

STR1
STR2
STR3
STR4
BL
MB5
SSL1
SSL2
SSL3
SSL4
WL
WL
SB2
WL
WL
BND(STP1)
MSL1
MSL2
MSL3
MSL4
WL
WL
SB1
WL
WL
GSL
STP2
D1
D3
D2

FIG. 10

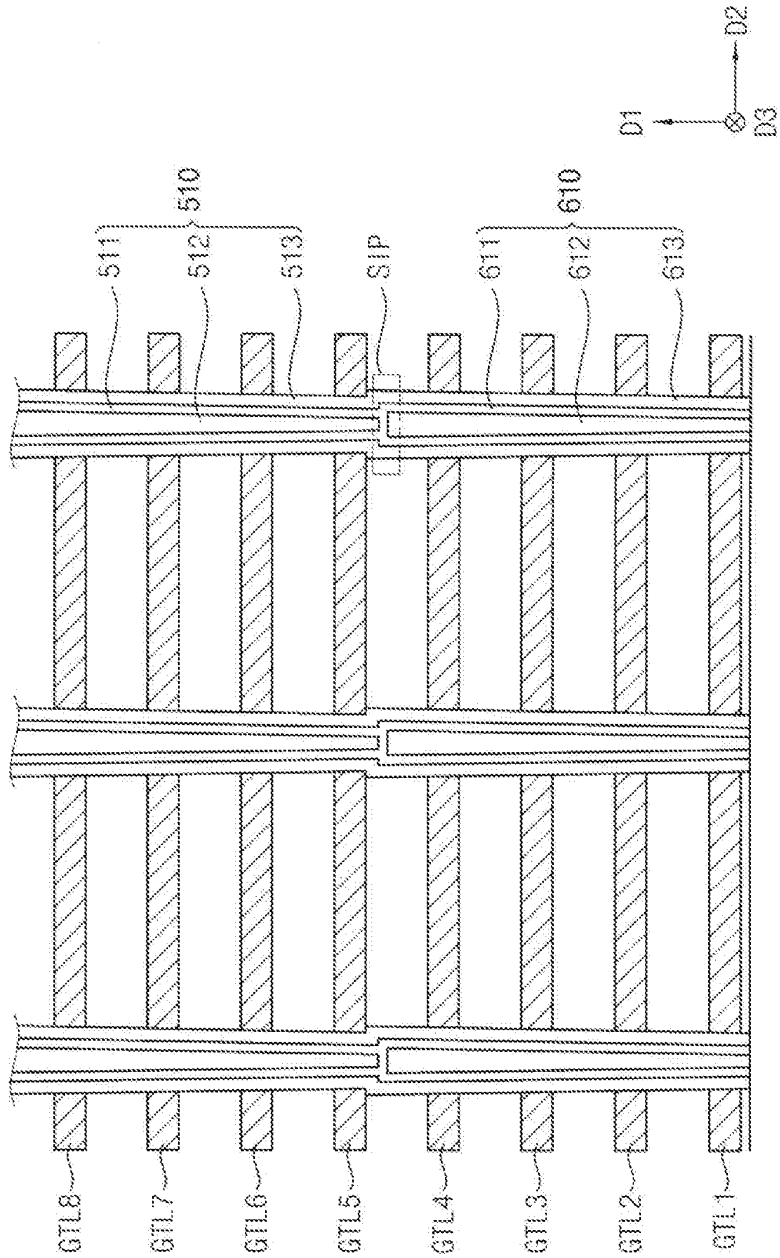

D1
D2
D3
510
511
512
513
SIP
610
611
612
613
GTL8
GTL7
GTL6
GTL5
GTL4
GTL3
GTL2
GTL1

FIG. 11

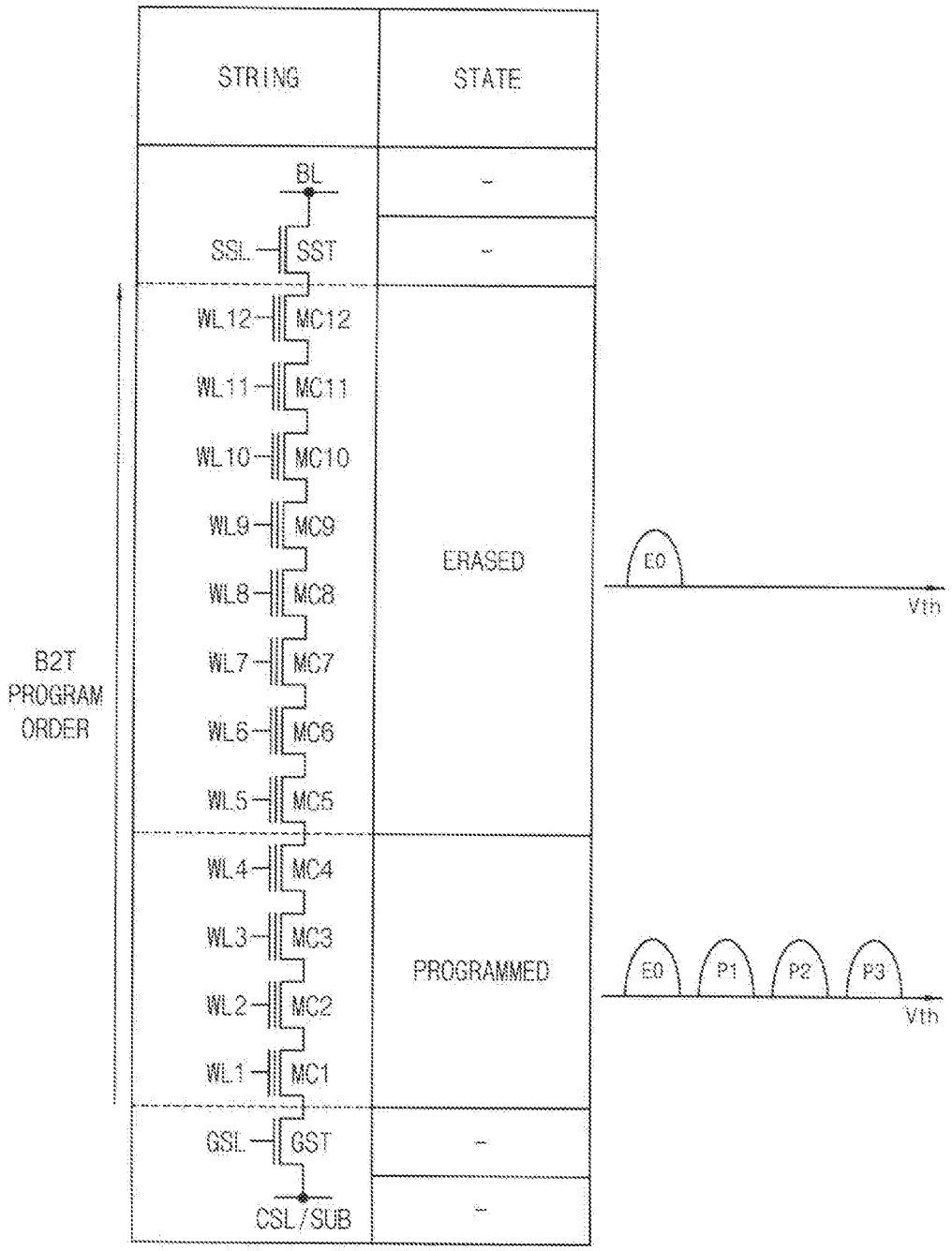

STRING
STATE
BL
SSL
SST
WL12
MC12
WL11
MC11
WL10
MC10
WL9
MC9
WL8
MC8
WL7
MC7
WL6
MC6
WL5
MC5
WL4
MC4
WL3
MC3
WL2
MC2
WL1
MC1
GSL
GST
CSL/SUB
ERASED
PROGRAMMED
B2T
PROGRAM
ORDER
E0
Vth
E0
P1
P2
P3
Vth

FIG. 12

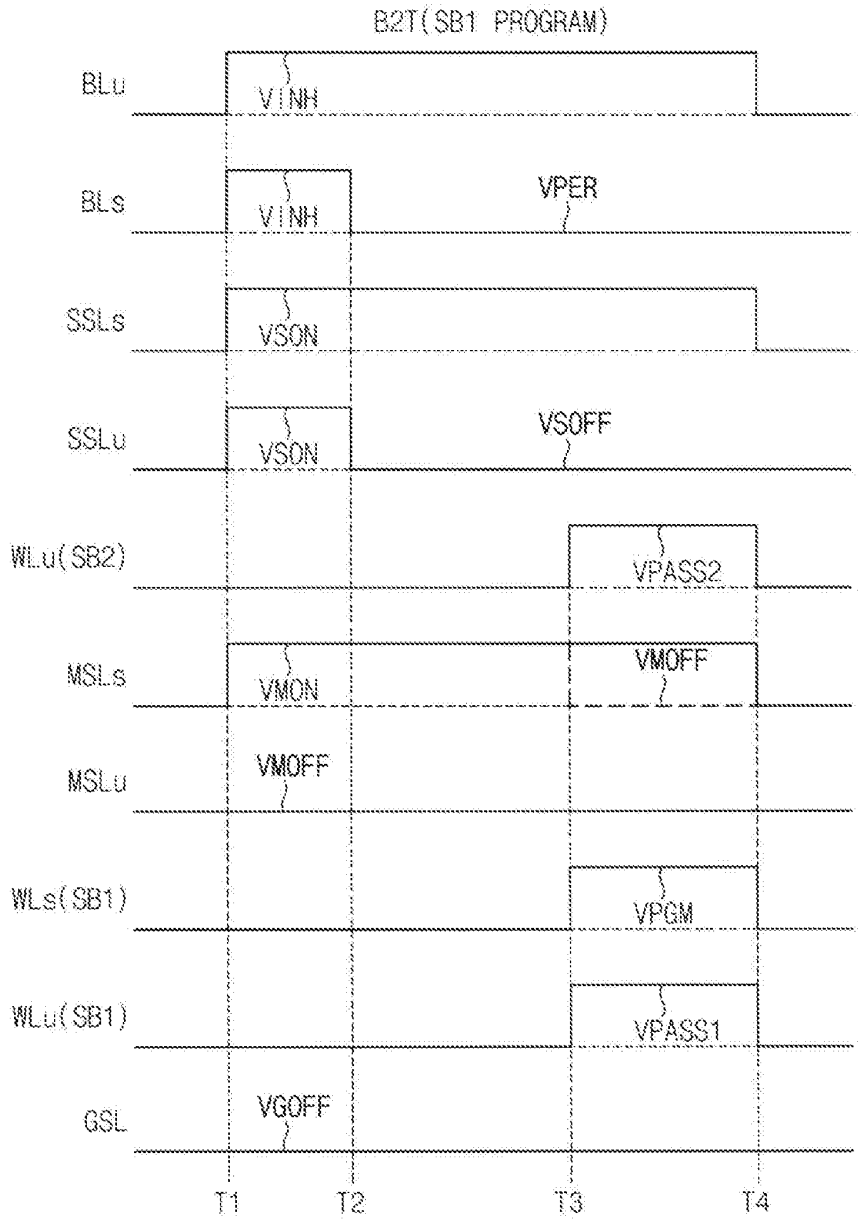

B2T(SB1 PROGRAM)
BLu
VINH
BLs
VINH
VPER
SSLs
VSON
SSLu
VSON
VSOFF
WLu(SB2)
VPASS2
MSLs
VMON
VMOFF
MSLu
VMOFF
WLs(SB1)
VPGM
WLu(SB1)
VPASS1
GSL
VGOFF
T1
T2
T3
T4

FIG. 13

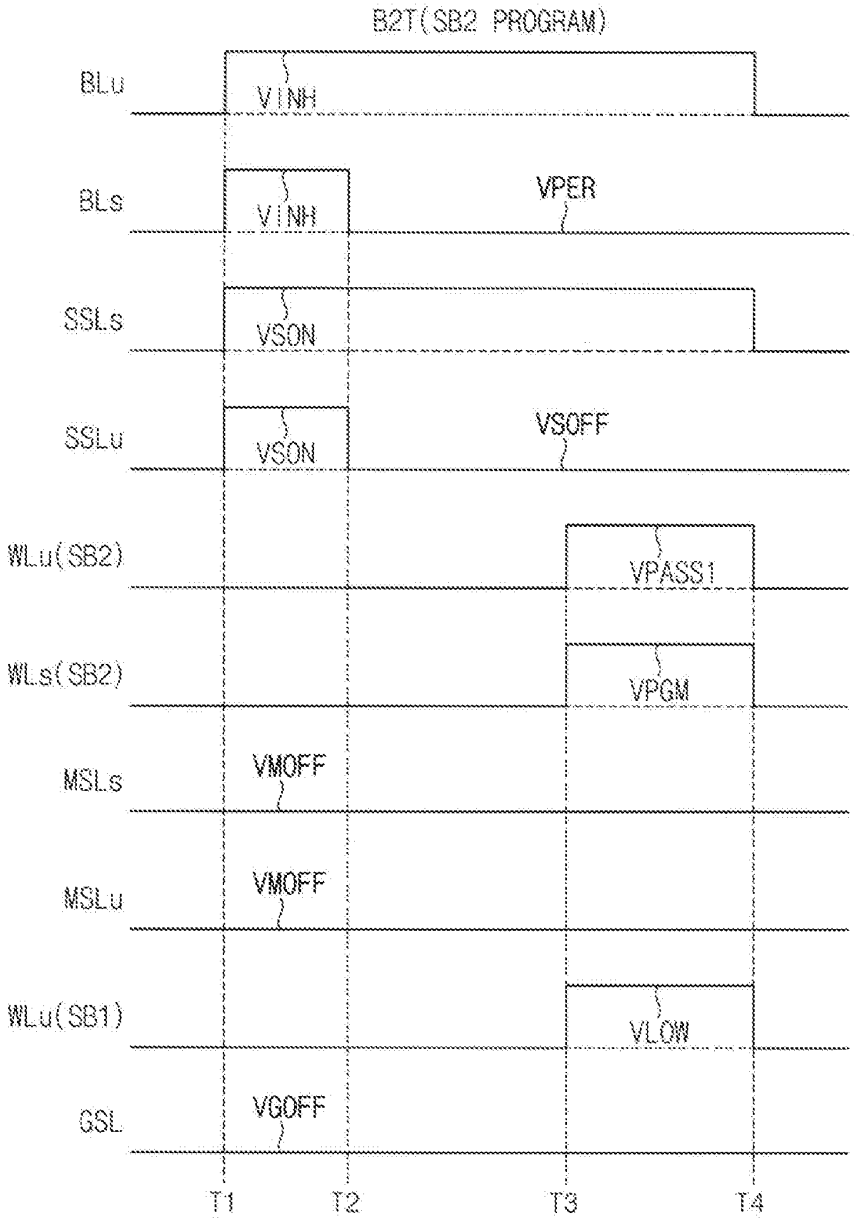

B2T(SB2 PROGRAM)
BLu
VINH
BLs
VINH
VPER
SSLs
VSON
SSLu
VSON
VSOFF
WLu(SB2)
VPASS1
WLs(SB2)
VPGM
MSLs
VMOFF
MSLu
VMOFF
WLu(SB1)
VLOW
GSL
VGOFF
T1
T2
T3
T4

FIG. 14

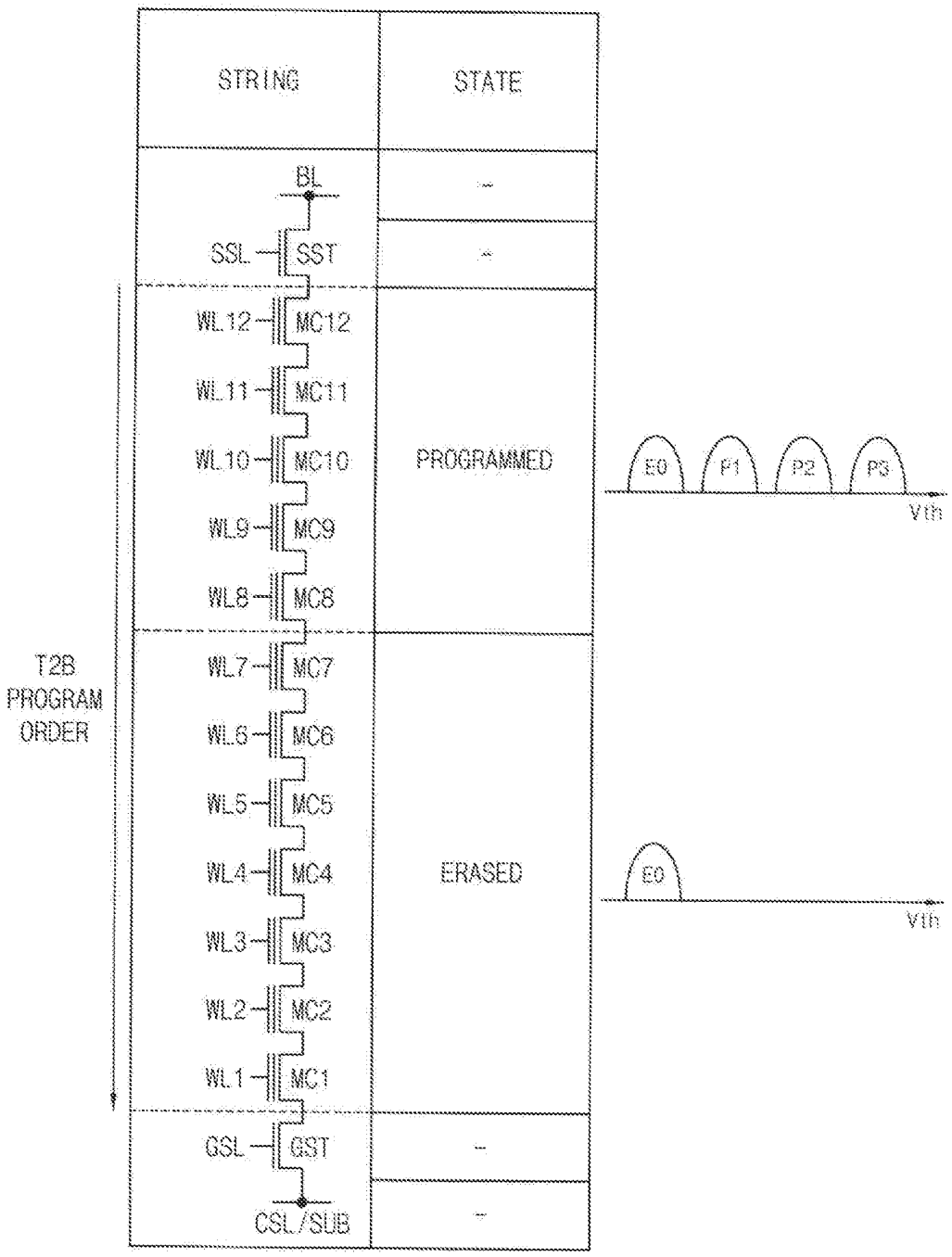

STRING
STATE
BL
SSL
SST
WL12
MC12
WL11
MC11
WL10
MC10
WL9
MC9
WL8
MC8
PROGRAMMED
E0
P1
P2
P3
Vth
T2B
PROGRAM
ORDER
WL7
MC7
WL6
MC6
WL5
MC5
WL4
MC4
WL3
MC3
WL2
MC2
WL1
MC1
ERASED
E0
Vth
GSL
GST
CSL/SUB

FIG. 15

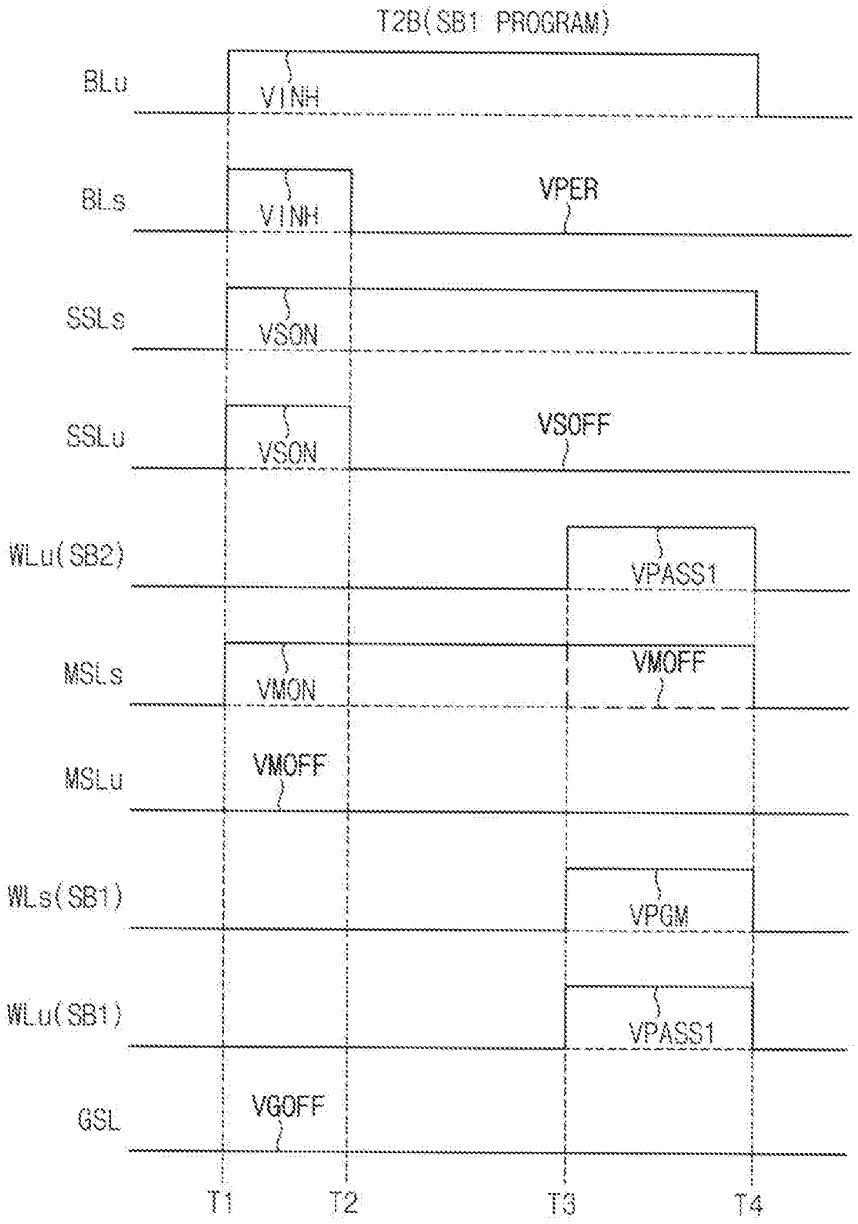

T2B(SB1 PROGRAM)
BLu
VINH
BLs
VINH
VPER
SSLs
VSON
SSLu
VSON
VSOFF
WLu(SB2)
VPASS1
MSLs
VMON
VMOFF
MSLu
VMOFF
WLs(SB1)
VPGM
WLu(SB1)
VPASS1
GSL
VGOFF
T1
T2
T3
T4

FIG. 16

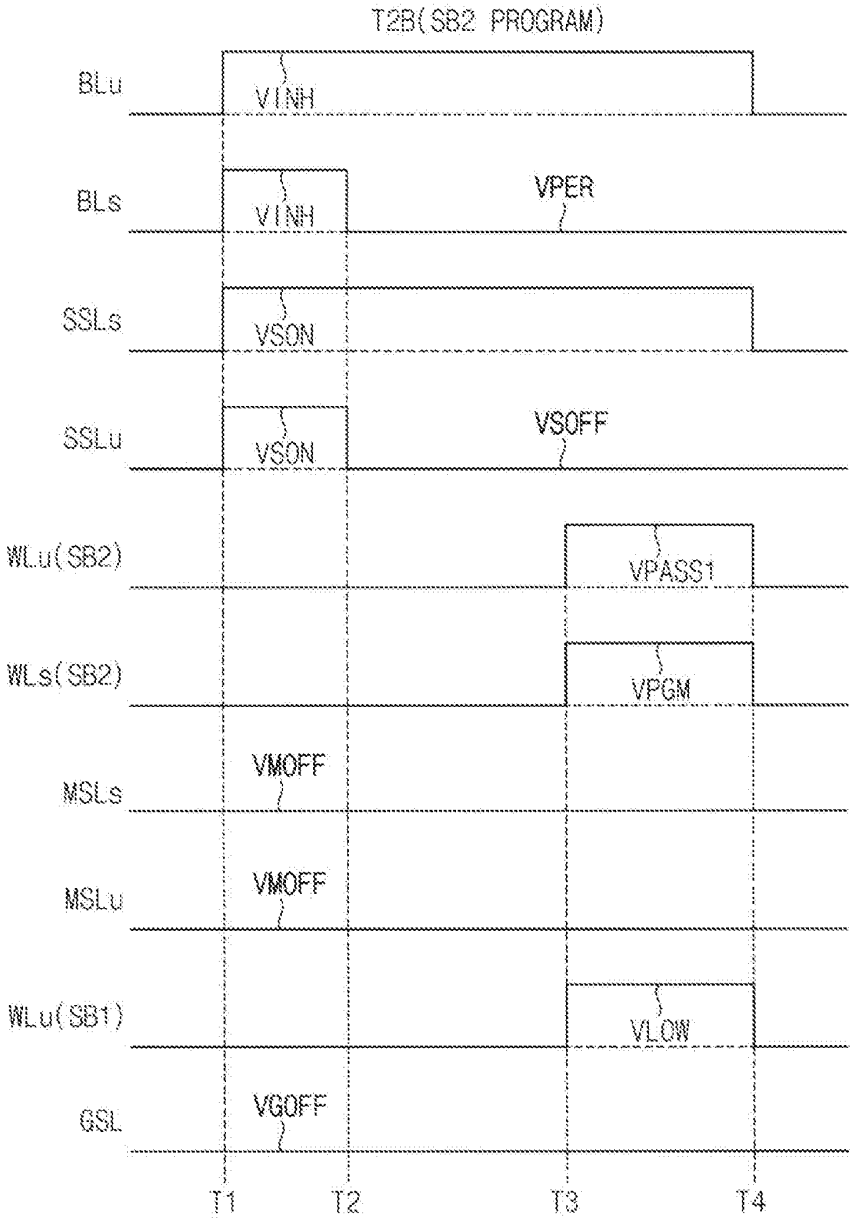

T2B(SB2 PROGRAM)
BLu
VINH
BLs
VINH
VPER
SSLs
VSON
SSLu
VSON
VSOFF
WLu(SB2)
VPASS1
WLs(SB2)
VPGM
MSLs
VMOFF
MSLu
VMOFF
WLu(SB1)
VLOW
GSL
VGOFF
T1
T2
T3
T4

FIG. 17

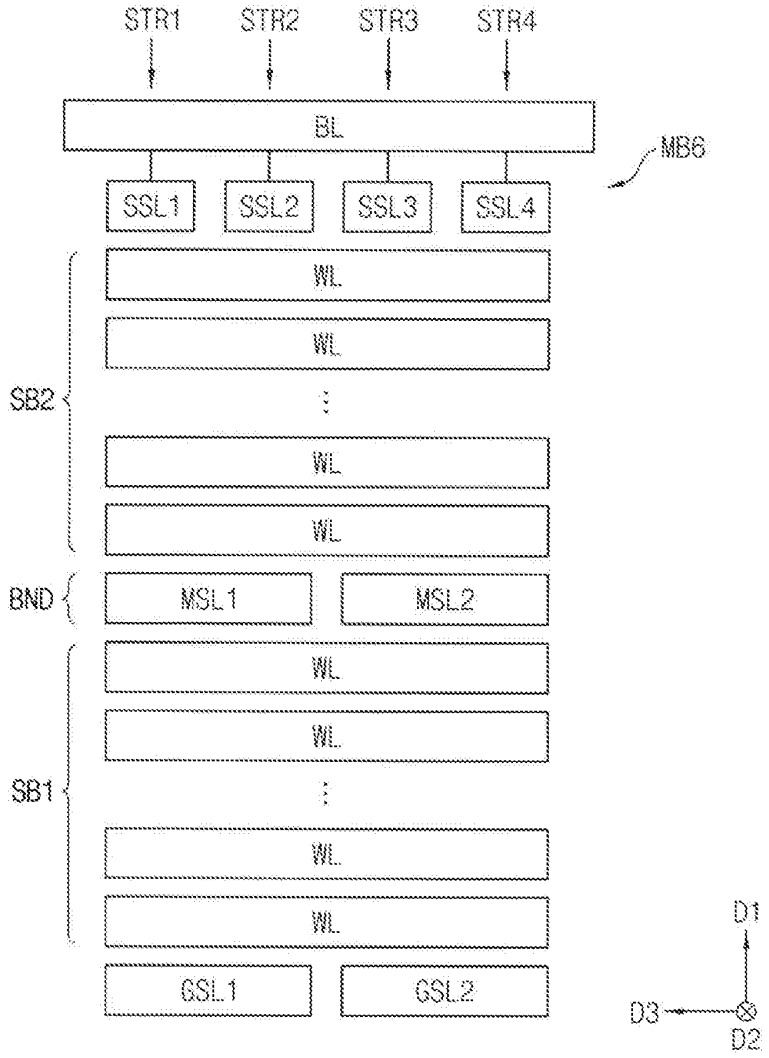

STR1
STR2
STR3
STR4
BL
MB6
SSL1
SSL2
SSL3
SSL4
WL
WL
SB2
WL
WL
BND
MSL1
MSL2
WL
WL
SB1
WL
WL
GSL1
GSL2
D1
D3
D2

FIG. 18

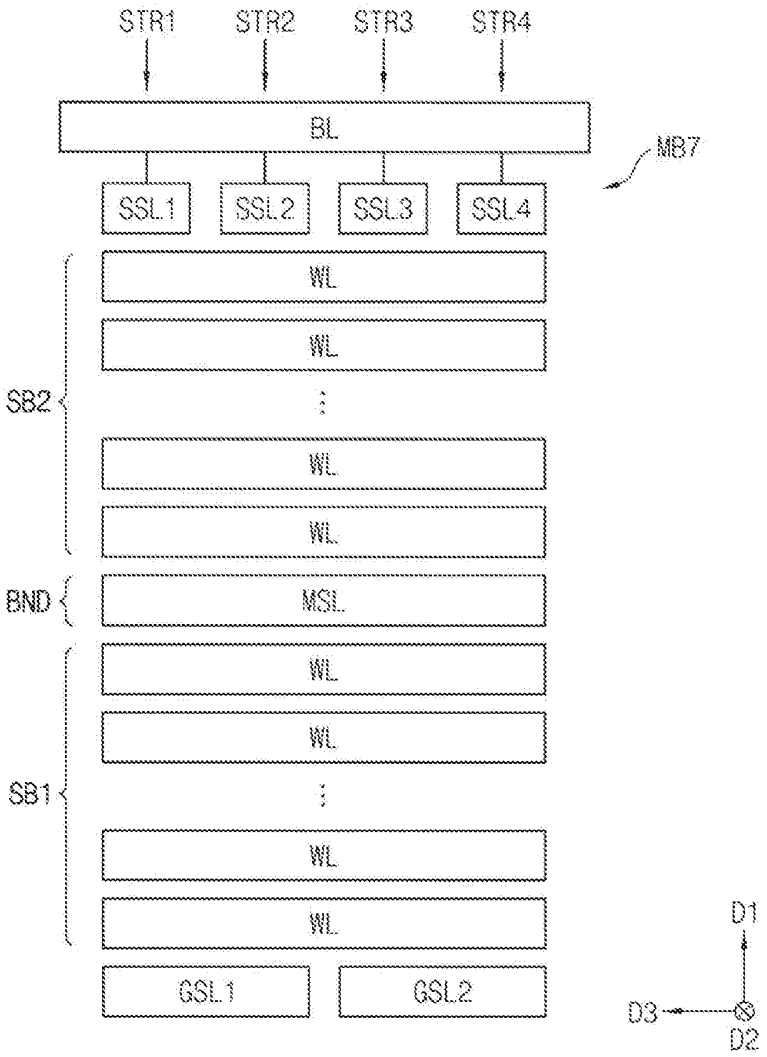

STR1
STR2
STR3
STR4
BL
MB7
SSL1
SSL2
SSL3
SSL4
WL
WL
SB2
WL
WL
BND
MSL
WL
WL
SB1
WL
WL
GSL1
GSL2
D1
D3
D2

FIG. 19

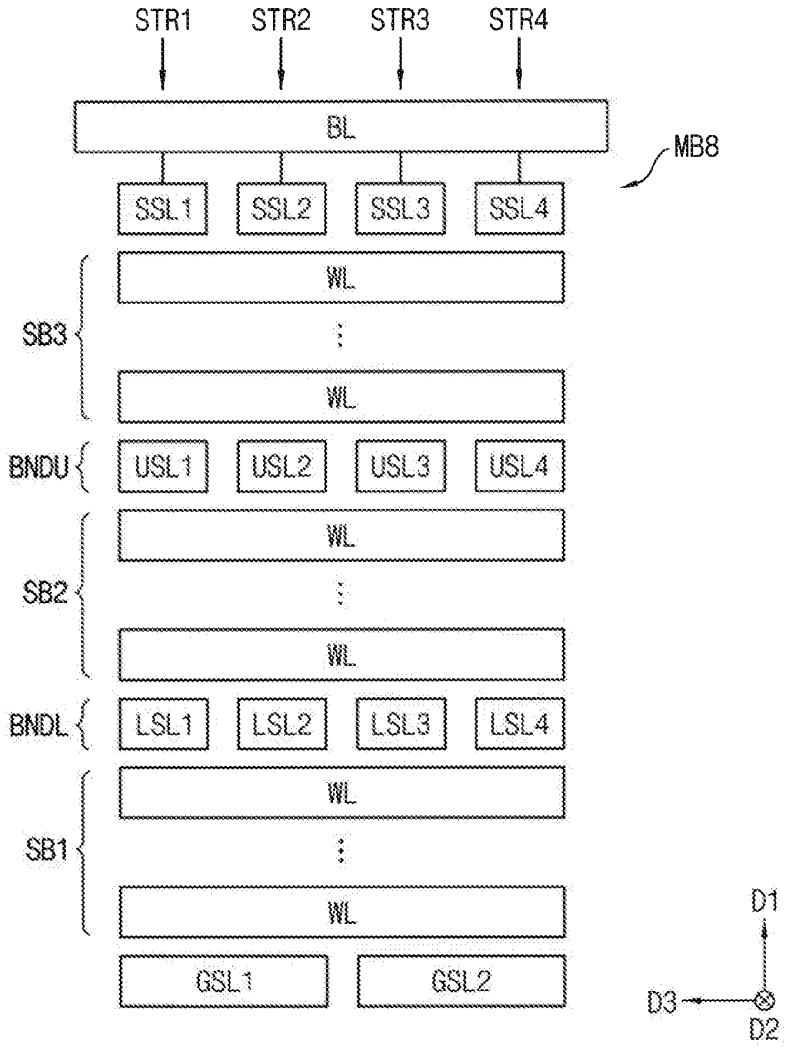

STR1
STR2
STR3
STR4
BL
MB8
SSL1
SSL2
SSL3
SSL4
SB3
WL
WL
BNDU
USL1
USL2
USL3
USL4
SB2
WL
WL
BNDL
LSL1
LSL2
LSL3
LSL4
SB1
WL
WL
GSL1
GSL2
D1
D3
D2

FIG. 20

B2T(SB1 PROGRAM)

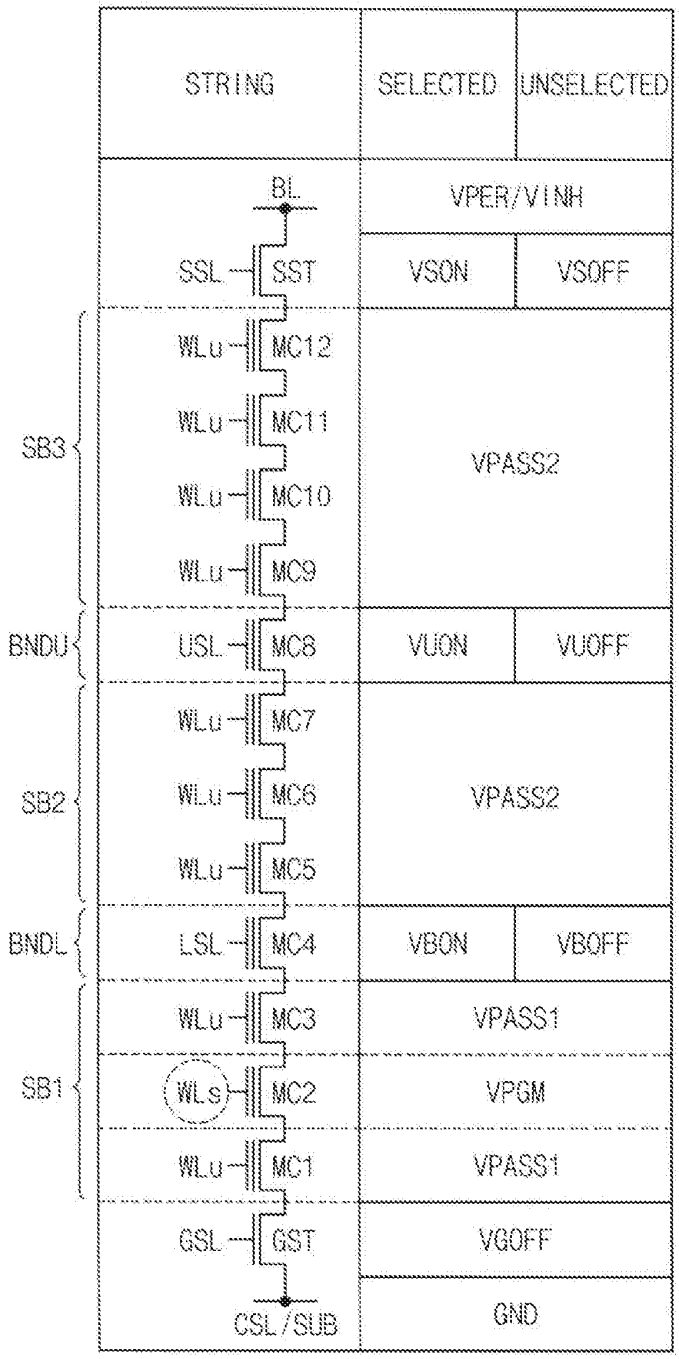


FIG. 21

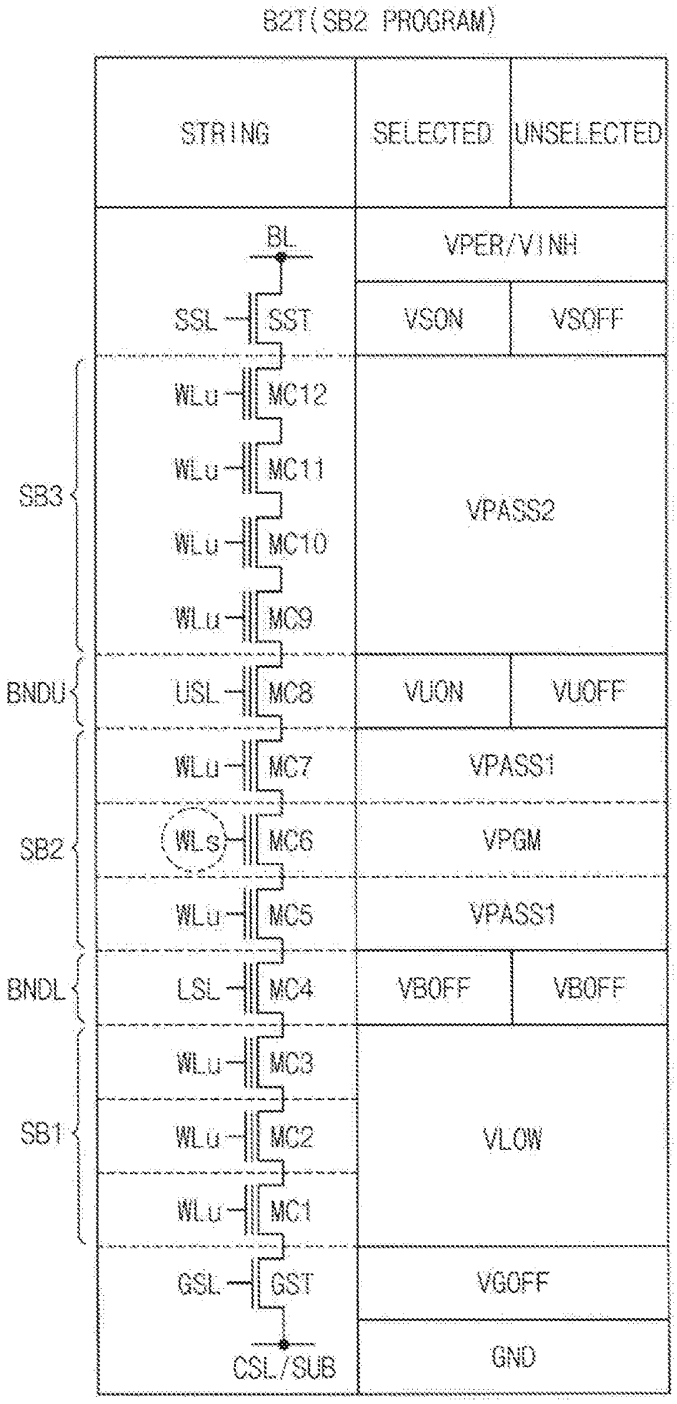

B2T(SB2 PROGRAM)
STRING
SELECTED
UNSELECTED
BL
VPER/VINH
SSL
SST
VSON
VSOFF
WLu
MC12
MC11
MC10
MC9
VPASS2
SB3
BNDU
USL
MC8
VUON
VUOFF
MC7
VPASS1
SB2
WLs
MC6
VPGM
MC5
VPASS1
BNDL
LSL
MC4
VBOFF
VBOFF
MC3
MC2
MC1
VLOW
SB1
GSL
GST
VGOFF
CSL/SUB
GND

FIG. 22

B2T(SB3 PROGRAM)

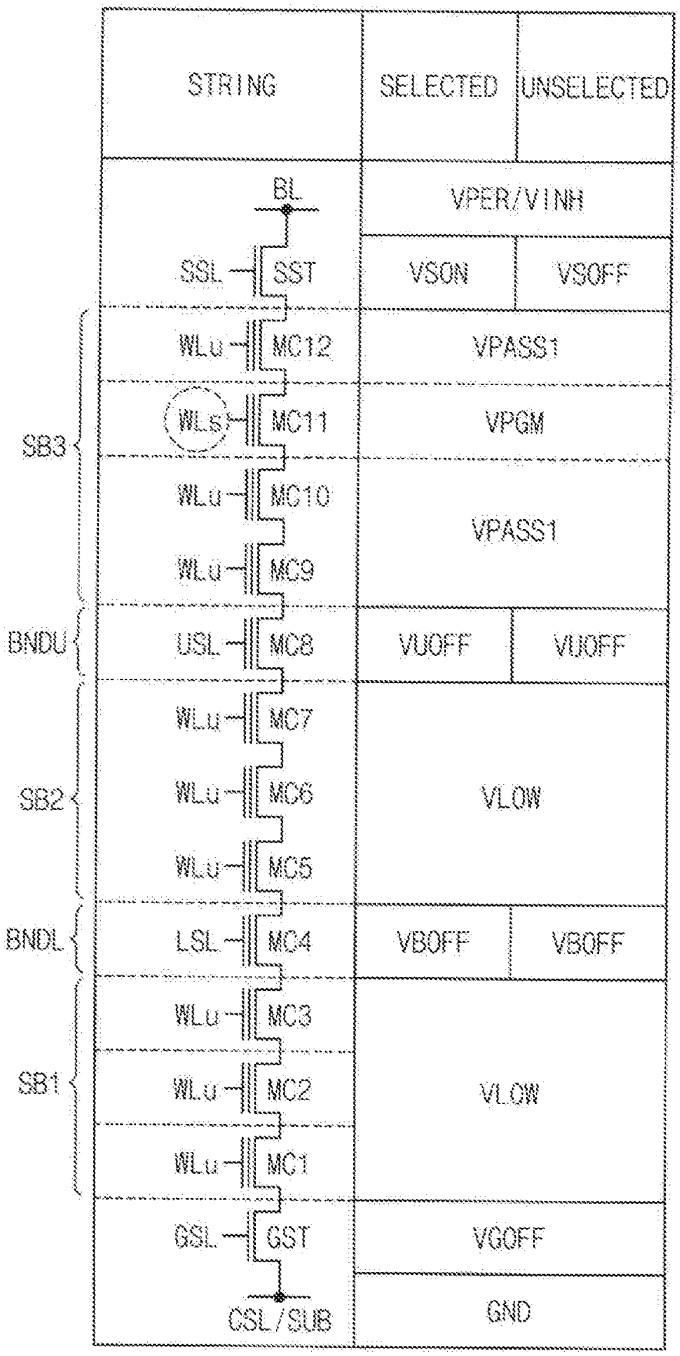


FIG. 23

T2B(SB1 PROGRAM)

	STRING	SELECTED	UNSELECTED
	BL	VPER/VINH	
	SSL — SST	VSON	VSOFF
SB3	WLu — MC12	VPASS1	
	WLu — MC11		
	WLu — MC10		
	WLu — MC9		
BNDU	USL — MC8	VUON	VUOFF
SB2	WLu — MC7	VPASS1	
	WLu — MC6		
	WLu — MC5		
BNDL	LSL — MC4	VBON	VBOFF
SB1	WLu — MC3	VPASS1	
	WLe — MC2	VPGM	
	WLu — MC1	VPASS1	
	GSL — GST	VGOFF	
	CSL/SUB	GND	

FIG. 24

T2B(SB2 PROGRAM)

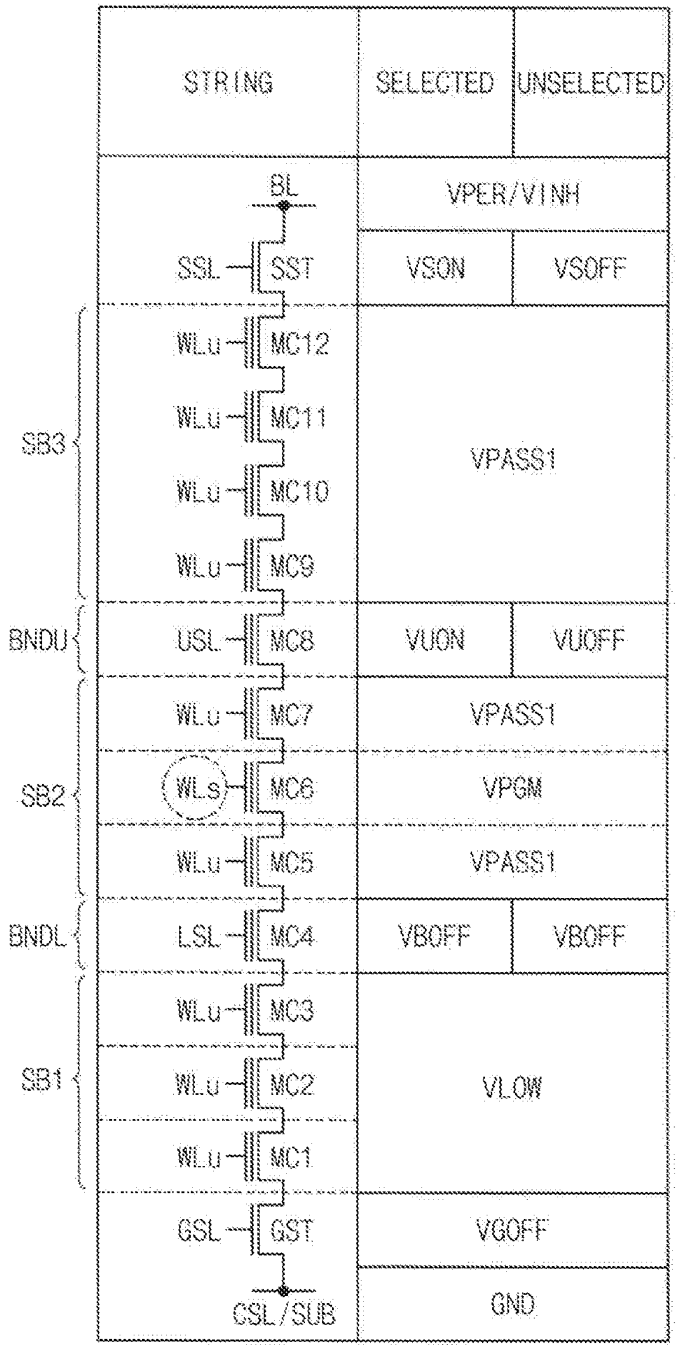


FIG. 25

T2B(SB3 PROGRAM)

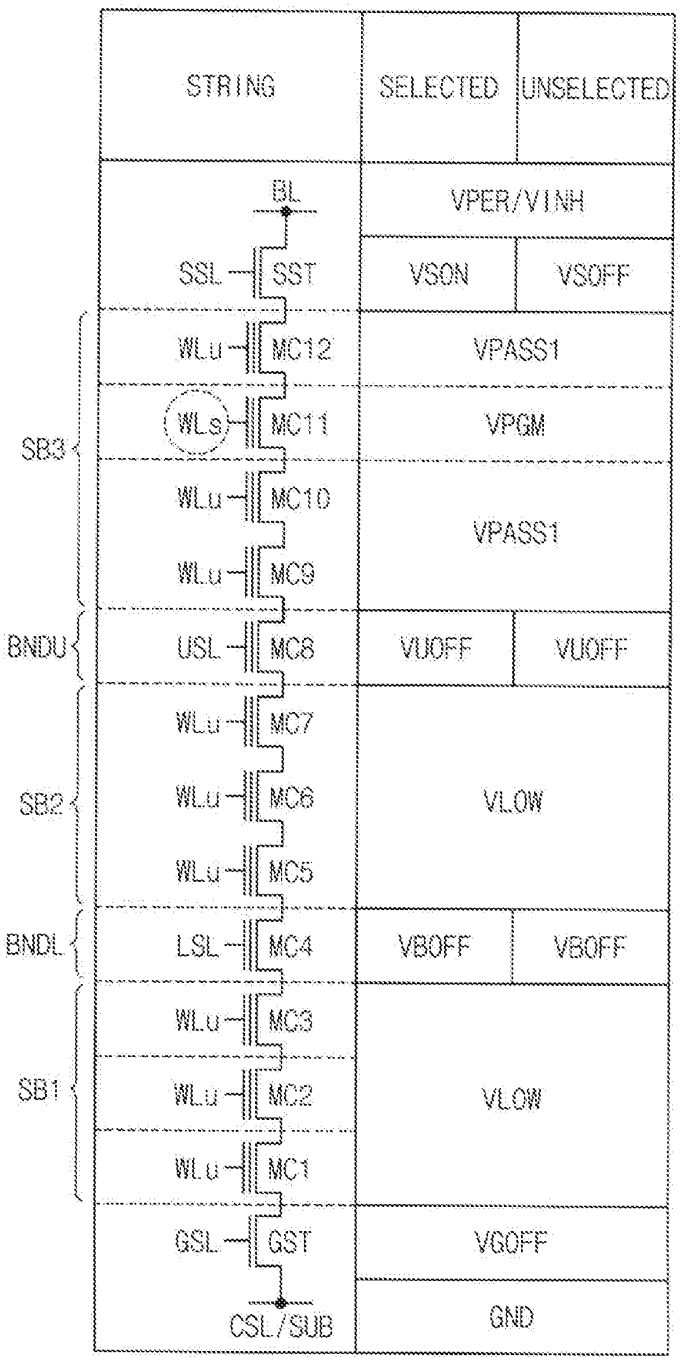
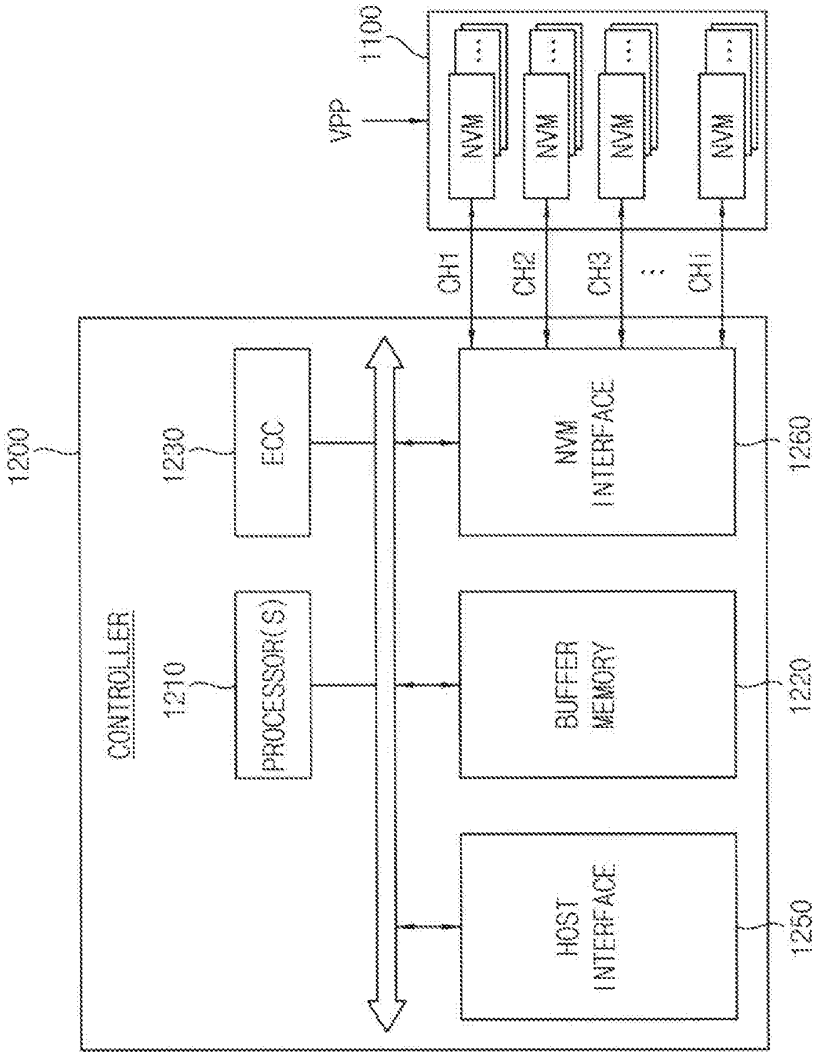


FIG. 26


1000
1200
CONTROLLER
1210
PROCESSOR(S)
1230
ECC
HOST INTERFACE
1250
BUFFER MEMORY
1220
NVM INTERFACE
1260
CH1
CH2
CH3
CH1
VPP
1100
NVM
NVM
NVM
NVM

NONVOLATILE MEMORY DEVICE AND METHOD OF PROGRAMMING IN THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This U.S. Non-provisional application claims priority under 35 USC § 119 to Korean Patent Application No. 10-2017-0178312, filed on Dec. 22, 2017, in the Korean Intellectual Property Office (KIPO), the disclosure of which is incorporated by reference in its entirety herein.

BACKGROUND

1. Technical Field

[0002] Example embodiments relate generally to semiconductor integrated circuits, and more particularly to a nonvolatile memory device and a method of programming in a nonvolatile memory device.

2. Discussion of the Related Art

[0003] Nonvolatile memory devices may maintain stored data even though power is off. While volatile memory devices are widely used as main memories of various apparatuses, nonvolatile memory devices are widely used for storing program codes and/or data in various electronic devices, such as computers, mobile devices, etc.

[0004] Recently, nonvolatile memory devices of three-dimensional structure such as a vertical NAND memory devices have been developed to increase integration degree and memory capacity of the nonvolatile memory devices. Along with increases in the integration degree and memory capacity, disturbance on unselected memory cells increases while selected memory cells are programmed.

SUMMARY

[0005] Some example embodiments may provide a method of programming in a nonvolatile memory device capable of reducing disturbance on unselected memory cells during a program operation.

[0006] Some example embodiments may provide a nonvolatile memory device capable of reducing disturbance on unselected memory cells during a program operation.

[0007] According to example embodiments, to program in a nonvolatile memory device, a memory block is provided with a plurality of sub blocks disposed in a vertical direction where the memory block includes a plurality of cell strings each including a plurality of memory cells connected in series and disposed in the vertical direction. A plurality of intermediate switching transistors are disposed in a boundary portion between two adjacent sub blocks in the vertical direction. Each of the plurality of intermediate switching transistors is selectively activated based on a program address during a program operation. The selectively activating each of the plurality of intermediate switching transistors includes selectively turning on one or more intermediate switching transistors in a selected cell string based on the program address.

[0008] According to example embodiments, a method of programming in a nonvolatile memory device, includes, providing a memory block including a first sub block below a stopper layer and a second sub block above the stopper layer where the memory block includes a plurality of cell strings each including a plurality of memory cells connected in series and disposed in a vertical direction, providing a plurality of intermediate switching transistors disposed in the stopper layer, a program address is included in the first sub block during a program operation, turning on one or more intermediate switching transistors in a selected cell string when a selected word line corresponding to a program address is included in the first sub block during a program operation, and turning off the one or more intermediate switching transistors in the selected cell string when the selected word line is included in the second sub block during the program operation.

[0009] According to example embodiments, a nonvolatile memory device includes a memory block, a plurality of intermediate switching transistors, and a control circuit. The memory block is divided into a plurality of sub blocks and includes a plurality of cell strings each including a plurality of memory cells connected in series and disposed in a vertical direction. The plurality of intermediate switching transistors are disposed in a boundary portion between two adjacent sub blocks in the vertical direction. The control circuit selectively turns on one or more intermediate switching transistors in a selected cell string independently of intermediate switching transistors in unselected cell strings based on a program address during a program operation.

[0010] The nonvolatile memory device and the method of programming in the nonvolatile memory device according to example embodiments may reduce program voltage disturbances and pass voltage disturbances and thus may increase performance and lifetime of the nonvolatile memory device through independent activating of each of the intermediate switching transistors to implement local boosting of string segments irrelevant to programming.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Example embodiments of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

[0012] FIG. **1** is a flow chart illustrating a method of programming in a nonvolatile memory device according to example embodiments.

[0013] FIG. **2** is a block diagram illustrating a memory system according to example embodiments.

[0014] FIG. **3** is a block diagram illustrating an example embodiment of a nonvolatile memory device included in the memory system of FIG. **2**.

[0015] FIG. **4** is a block diagram illustrating a memory cell array included in the nonvolatile memory device of FIG. **3**.

[0016] FIG. **5** is a perspective view illustrating one of memory blocks of FIG. **4**.

[0017] FIG. **6** is a circuit diagram illustrating an equivalent circuit of the memory block described with reference to FIG. **5**.

[0018] FIG. **7** is a cross-sectional view illustrating a memory block according to example embodiments.

[0019] FIG. **8**A is a circuit diagram illustrating an equivalent circuit corresponding to a structure of FIG. **7**.

[0020] FIG. **8**B is a perspective view illustrating a memory block corresponding to a structure of FIG. **7**.

[0021] FIGS. **9**A through **9**D are cross-sectional views illustrating a memory block according to example embodiments.

[0022] FIG. **10** is a cross-sectional view for describing an example embodiment of a boundary portion included in a memory block according to example embodiments.

[0023] FIG. **11** is a diagram illustrating a first program scenario according to example embodiments.

[0024] FIG. **12** is a timing diagram illustrating a program operation of a first sub block according to the first program scenario of FIG. **11**.

[0025] FIG. **13** is a timing diagram illustrating a program operation of a second sub block according to the first program scenario of FIG. **11**.

[0026] FIG. **14** is a diagram illustrating a second program scenario according to example embodiments.

[0027] FIG. **15** is a timing diagram illustrating a program operation of a first sub block according to the second program scenario of FIG. **14**.

[0028] FIG. **16** is a timing diagram illustrating a program operation of a second sub block according to the second program scenario of FIG. **15**.

[0029] FIGS. **17** and **18** are cross-sectional views illustrating a memory block according to example embodiments.

[0030] FIG. **19** is a cross-sectional view illustrating a memory block divided into three sub blocks according to example embodiments.

[0031] FIGS. **20** through **22** are timing diagrams illustrating program operations of sub blocks in FIG. **19** according to the first program scenario of FIG. **11**.

[0032] FIGS. **23** through **25** are timing diagrams illustrating program operations of sub blocks in FIG. **19** according to the second program scenario of FIG. **14**.

[0033] FIG. **26** is a block diagram illustrating a solid state disk or solid state drive (SSD) according to example embodiments.

DETAILED DESCRIPTION

[0034] Various example embodiments will be described more fully hereinafter with reference to the accompanying drawings, in which some example embodiments are shown. In the drawings, like numerals refer to like elements throughout. The repeated descriptions may be omitted.

[0035] FIG. **1** is a flow chart illustrating a method of programming in a nonvolatile memory device according to example embodiments.

[0036] Referring to FIG. **1**, a memory block includes a plurality of sub blocks disposed in a vertical direction where the memory block includes a plurality of cell strings each comprising a plurality of memory cells connected in series and disposed in the vertical direction (S**100**). The memory block may be divided into two sub blocks as will be described below with reference to FIG. **7**, three sub blocks as will be described below with reference to FIG. **19**, and in the same way four or more sub blocks.

[0037] A plurality of intermediate switching transistors are disposed in a boundary portion between two adjacent sub blocks of the plurality of sub blocks in the vertical direction (S**200**). In some example embodiments, as will be described below with reference to FIGS. **7**, **8**A and **8**B, the boundary portion may correspond to one gate layer. In other example embodiments, as will be described below with reference to FIG. **9**A, the boundary portion may correspond to two or more gate layers that are adjacent in the vertical direction. In still other example embodiments, as will be described below with reference to FIG. **19**, the boundary portion may correspond to two or more gate layers that are spaced apart in the vertical direction. Here, the gate layers indicate the conductive materials **213** to **293** in FIG. **5**, that is, gate layers in which gate lines GTL**1**~GTL**8** in FIG. **6** are formed. In example embodiments, the boundary portion (or, a stopper layer) may be referred to as an area including one or more transistors not connected to word lines, string selection lines, and ground selection lines in each cell string. The boundary portion may also be referred to as a separate portion between an upper channel hole and a lower channel hole of a channel hole in each cell string.

[0038] Each of the plurality of intermediate switching transistors is selectively activated based on a program address during a program operation (S**300**). For example, each of the plurality of intermediate switching transistors may be individually and independently selectively activated based on a program address. The selective activating based on the program address will be described below with reference to FIGS. **11** through **25**.

[0039] As the number of the word lines formed in the gate layers stacked in the vertical direction is increased to increase the density of each memory block, the pass voltage disturbance on the memory cells connected to the unselected word lines during the program operation is increased. Also the program voltage disturbance on the memory cells connected to the selected word line but included in the unselected cell strings is increased as the number of the cell strings in each memory block is increased.

[0040] The nonvolatile memory device and the method of programming in the nonvolatile memory device according to example embodiments may reduce a program voltage disturbance and a pass voltage disturbance and thus increase performance and lifetime of the nonvolatile memory device through independent switching of the intermediate switching transistors to implement local boosting of string segments irrelevant to programming. Here the local boosting indicates that an entire channel is not boosted but a portion of a channel, that is, a boosted channel segment is boosted by a pass voltage and/or a program voltage.

[0041] FIG. **2** is a block diagram illustrating a memory system according to example embodiments.

[0042] Referring to FIG. **2**, a memory system **10** may include a memory controller **20** and at least one memory device **30**.

[0043] The memory device **30** may be a nonvolatile memory device as described herein. The memory system **10** may include data storage media based on flash memory such as a memory card, a universal serial bus (USB) memory and solid state drive (SSD).

[0044] The nonvolatile memory device **30** may perform a read operation, an erase operation, and a program operation or a write operation under control of the memory controller **20**. The nonvolatile memory device **30** receives a command CMD, an address ADDR and data DATA through input/output lines from the memory controller **20** for performing such operations. In addition, the nonvolatile memory device **30** receives a control signal CTRL through a control line from the memory controller **20**. In addition, the nonvolatile memory device **30** receives a power PWR through a power line from the memory controller **20**.

[0045] FIG. **3** is a block diagram illustrating an example embodiment of a nonvolatile memory device included in the memory system of FIG. **2**.

[0046] Referring to FIG. **3**, the nonvolatile memory device **30** includes a memory cell array **100**, a page buffer circuit

410, a data input/output circuit **420**, an address decoder **430**, a control circuit **450** and a voltage generator **460**.

[0047] The memory cell array **100** may be coupled to the address decoder **430** through a plurality of string selection lines SSL, a plurality of word lines WL, and a plurality of ground selection lines GSL. In addition, the memory cell array **100** may be coupled to the page buffer circuit **410** through a plurality of bit lines BL.

[0048] The memory cell array **100** may include a plurality of memory cells coupled to the plurality of word lines WL and the plurality of bit lines BL. In some example embodiments, the memory cell array **100** may be a three-dimensional memory cell array, which is formed on a substrate in a three-dimensional structure (or a vertical structure). In this case, the memory cell array **100** may include a plurality of NAND strings that are vertically oriented such that at least one memory cell is located over another memory cell.

[0049] The control circuit **450** may receive a command (signal) CMD and an address (signal) ADDR from the memory controller **20** and control erasure, programming and read operations of the nonvolatile memory device **30** based on the command signal CMD and the address signal ADDR. An erasure operation may comprise performing a sequence of erase loops, and a program operation may include performing a sequence of program loops. Each program loop may include a program operation and a program verification operation. Each erase loop may include an erase operation and an erase verification operation. The read operation may include a normal read operation and data recover read operation.

[0050] For example, the control circuit **450** may generate the control signals CTL, which are used for controlling the voltage generator **460**, and may generate the page buffer control signal PBC for controlling the page buffer circuit **410**, based on the command signal CMD, and generate the row address R_ADDR and the column address C_ADDR based on the address signal ADDR. The control circuit **450** may provide the row address R_ADDR to the address decoder **430** and provide the column address C_ADDR to the data input/output circuit **420**.

[0051] The address decoder **430** may be coupled to the memory cell array **100** through the plurality of string selection lines SSL, the plurality of word lines WL, and the plurality of ground selection lines GSL. During the program operation or the read operation, the address decoder **430** may determine one of the plurality of word lines WL as a selected word line and determine rest of the plurality of word lines WL except for the selected word line as unselected word lines based on the row address R_ADDR.

[0052] In addition, during the program operation or the read operation, the address decoder **430** may determine one of the plurality of string selection lines SSL as a selected string selection line and determine rest of the plurality of string selection lines SSL except for the selected string selection line as unselected string selection lines based on the row address R_ADDR.

[0053] The voltage generator **460** may generate word line voltages VWL, which are required for the operation of the memory cell array **100** of the nonvolatile memory device **30**, based on the control signals CTL. The voltage generator **460** may receive the power PWR from the memory controller **20**. The word line voltages VWL may be applied to the plurality of word lines WL through the address decoder **430**.

[0054] For example, during the program operation, the voltage generator **460** may apply a program voltage to the selected word line and may apply a program pass voltage to the unselected word lines. In addition, during the program verification operation, the voltage generator **460** may apply a program verification voltage to the first word line and may apply a verification pass voltage to the unselected word lines.

[0055] In addition, during the normal read operation, the voltage generator **460** may apply a read voltage to the selected word line and may apply a read pass voltage to the unselected word lines. During the data recover read operation, the voltage generator **460** may apply the read voltage to a word line adjacent to the selected word line and may apply a recover read voltage to the selected word line.

[0056] The page buffer circuit **410** may be coupled to the memory cell array **100** through the plurality of bit lines BL. The page buffer circuit **410** may include a plurality of buffers. In some example embodiments, each buffer may be connected to only one bit line. In other example embodiments, each buffer may be connected to two or more bit lines.

[0057] The page buffer circuit **410** may temporarily store data to be programmed in a selected page or data read out from the selected page of the memory cell array **100**.

[0058] The data input/output circuit **420** may be coupled to the page buffer circuit **410** through data lines DL. During the program operation, the data input/output circuit **410** may receive program data DATA received from the memory controller **20** and provide the program data DATA to the page buffer circuit **410** based on the column address C ADDR received from the control circuit **450**. During the read operation, the data input/output circuit **420** may provide read data DATA, having been read from the memory cell array **100** and stored in the page buffer circuit **410**, to the memory controller **20** based on the column address C_ADDR received from the control circuit **450**.

[0059] In addition, the page buffer circuit **410** and the data input/output circuit **420** may read data from a first area of the memory cell array **100** and write this read data to a second area of the memory cell array **100** (e.g., without transmitting the data to a source external to the nonvolatile memory device **30**, such as to the memory controller **20**). That is, the page buffer circuit **410** and the data input/output circuit **420** may perform a copy-back operation.

[0060] Hereinafter, a first direction D**1** indicates a direction perpendicular to an upper surface of a semiconductor substrate, and a second direction D**2** and a third direction D**3** indicate two directions parallel to the upper surface of the semiconductor substrate. For example, the second direction and the third direction D**3** may be perpendicular to each other. The first direction D**1** may be referred to as a vertical direction, the second direction D**2** may be referred to as a row direction and the third direction D**3** may be referred to as a column direction. The direction indicated by an arrow in figures and the opposite direction may be considered as the same direction.

[0061] FIG. **4** is a block diagram illustrating a memory cell array included in the nonvolatile memory device of FIG. **3**, and FIG. **5** is a perspective view illustrating one of memory blocks of FIG. **4**.

[0062] Referring to FIG. **4**, the memory cell array **100** may include a plurality of memory blocks BLK**1** to BLKz. In an embodiment, the memory blocks BLK**1** to BLKz are

selected by the address decoder **430** in FIG. **3**. For example, the address decoder **430** may select a particular memory block BLK corresponding to a block address among the memory blocks BLK**1** to BLKz.

[0063] Referring to FIG. **5**, a memory block BLKi includes NAND strings which are formed on a substrate in a three-dimensional structure (or a vertical structure). The memory block BLKi includes structures extending along the first, second and third directions D**1**, D**2** and D**3**.

[0064] A substrate **111** is provided. For example, the substrate **111** may have a well of a first type (e.g., a first conductive type). For example, the substrate **111** may have a p-well formed by implanting a group 3 element such as boron (B). For example, the substrate **111** may have a pocket p-well provided in an n-well. In an embodiment, the substrate **111** has a p-type well (or a p-type pocket well). However, the conductive type of the substrate **111** is not limited to the p-type.

[0065] A plurality of doping regions **311** to **314** extending along the first direction D**1** are provided in/on the substrate **111**. For example, the plurality of doping regions **311** to **314** may have a second type (e.g., a second conductive type) different from the first type of the substrate **111**. In an embodiment, the first to fourth doping regions **311** to **314** have an n-type. However, the conductive type of the first to fourth doping regions **311** to **314** is not limited to the n-type.

[0066] A plurality of insulation materials **112** extending along the first direction D**1** are sequentially provided along the second direction D**2** on a region of the substrate **111** between the first and second doping regions **311** and **312**. For example, the plurality of insulation materials **112** are provided along the second direction D**2**, being spaced by a specific distance. For example, the insulation materials **112** may include an insulation material such as an oxide layer.

[0067] A plurality of pillars **113** penetrating the insulation materials along the second direction D**2** are sequentially disposed along the first direction D**1** on a region of the substrate **111** between the first and second doping regions **311** and **312**. For example, the plurality of pillars **113** penetrate the insulation materials **112** to contact the substrate **111**.

[0068] For example, each pillar **113** may include a plurality of materials. For example, a channel layer **114** of each pillar **113** may include a silicon material having a first type. For example, the channel layer **114** of each pillar **113** may include a silicon material having the same type as the substrate **111**. In an embodiment, the channel layer **114** of each pillar **113** includes a p-type silicon. However, the channel layer **114** of each pillar **113** is not limited to the p-type silicon.

[0069] An internal material **115** of each pillar **113** includes an insulation material. For example, the internal material **115** of each pillar **113** may include an insulation material such as a silicon oxide. In some examples, the inner material **115** of each pillar **113** may include an air gap.

[0070] An insulation layer **116** is provided along the exposed surfaces of the insulation materials **112**, the pillars **113**, and the substrate **111**, on a region between the first and second doping regions **311** and **312**.

[0071] A plurality of first conductive materials **211** to **291** are provided on surfaces of the insulation layer **116**, in a region between the first and second doping regions **311** and **312**. For example, the first conductive material **211** extending along the second direction D**2** is provided between the insulation material **112** adjacent to the substrate **111** and the substrate **111**. In more detail, the first conductive material **211** extending along the second direction D**2** is provided between the insulation layer **116** at the bottom of the insulation material **112** adjacent to the substrate **111** and the substrate **111**.

[0072] A first conductive material extending along the second direction D**2** is provided between the insulation layer **116** at the top of the specific insulation material among the insulation materials **112** and the insulation layer **116** at the bottom of a specific insulation material among the insulation materials **112**. For example, a plurality of first conductive materials **221** to **281** extending along the second direction D**2** are provided between the insulation materials **112** and it may be understood that the insulation layer **116** is provided between the insulation materials **112** and the first conductive materials **221** to **281**. The first conductive materials **211** to **291** may be formed of a conductive metal. In some examples, the first conductive materials **211** to **291** may include a conductive material such as a polysilicon.

[0073] The same structures as those on the first and second doping regions **311** and **312** may be provided in a region between the second and third doping regions **312** and **313**. In the region between the second and third doping regions **312** and **313**, provided are a plurality of insulation materials **112** extending along the second direction D**2**, a plurality of pillars **113** disposed sequentially along the second direction D**2** and penetrating the plurality of insulation materials **112** along the first direction D**1**, an insulation layer **116** provided on the exposed surfaces of the plurality of insulation materials **112** and the plurality of pillars **113**, and a plurality of conductive materials **213** to **293** extending along the second direction D**2**.

[0074] Drains **320** are provided on the plurality of pillars **113**, respectively. On the drains, the second conductive materials **331** to **333** extending along the third direction D**3** are provided. The second conductive materials **331** to **333** are disposed along the second direction D**2**, being spaced by a specific distance. The second conductive materials **331** to **333** are respectively connected to the drains **320** in a corresponding region. The drains **320** and the second conductive material **333** extending along the third direction D**3** may be connected through each contact plug. The second conductive materials **331** to **333** may include metal materials. The second conductive materials **331** to **333** may include conductive materials such as a polysilicon.

[0075] The layers in which the first conductive materials are formed correspond to gate layers and the first conductive materials may form gate lines such as a string selection line SSL, a word line WL, intermediate switching lines MSL, USL and LSL, a ground selection line GSL, etc. The second conductive materials may form a bit line BL.

[0076] FIG. **6** is a circuit diagram illustrating an equivalent circuit of the memory block described with reference to FIG. **5**.

[0077] The memory block BLKi of FIG. **6** may be formed on a substrate in a three-dimensional structure (or a vertical structure). For example, a plurality of NAND strings or cell strings included in the memory block BLKi may be formed in the first direction D**1** perpendicular to the upper surface of the substrate.

[0078] Referring to FIG. **6**, the memory block BLKi may include NAND strings NS**11** to NS**33** coupled between bit lines BL**1**, BL**2** and BL**3** and a common source line CSL.

Each of the NAND strings NS**11** to NS**33** may include a string selection transistor SST, a plurality of memory cells MC**1** to MC**8**, and a ground selection transistor GST. In FIG. **6**, each of the NAND strings NS**11** to NS**33** is illustrated to include eight memory cells MC**1** to MC**8**. However, example embodiments are not limited thereto. In some example embodiments, each of the NAND strings NS**11** to NS**33** may include any number of memory cells.

[0079] Each string selection transistor SST may be connected to a corresponding string selection line (one of SSL**1** to SSL**3**). The plurality of memory cells MC**1** to MC**8** may be connected to corresponding gate lines GTL**1** to GTL**8**, respectively. The gate lines GTL**1** to GTL**8** may be word lines and some of the gate lines GTL**1** to GTL**8** may be dummy word lines. In addition, some of the gate lines GTL**1** to GTL**8** may be intermediate switching lines and the memory cells connected to the intermediate switching lines may be referred to as intermediate switching transistors. Each ground selection transistor GST may be connected to a corresponding ground selection line (one of GSL**1** to GSL**3**). Each string selection transistor SST may be connected to a corresponding bit line (e.g., one of BL**1**, BL**2** and BL**3**), and each ground selection transistor GST may be connected to the common source line CSL.

[0080] Word lines (e.g., WL**1**) having the same height may be commonly connected, and the ground selection lines GSL**1** to GSL**3** and the string selection lines SSL**1** to SSL**3** may be separated. Even though not illustrated, the gate lines corresponding to the intermediate switching lines may be separated as will be described below. In FIG. **6**, the memory block BLKi is illustrated to be coupled to eight gate lines GTL**1** to GTL**8** and three bit lines BL**1** to BL**3**. However, example embodiments are not limited thereto. Each memory block in the memory cell array **100** may be coupled to any number of word lines and any number of bit lines.

[0081] Hereinafter, the memory cells may be omitted and only the gate lines stacked in the vertical direction may be illustrated in figures of a memory block for convenience of illustration. The gate lines may include a string selection line SSL, a word line WL, a dummy word line DWL, intermediate switching lines MSL, USL and LSL and a ground selection line GSL. The transistors driven by the intermediate switching lines MSL, USL and LSL may be referred to as intermediate switching transistors. For convenience of illustration and description, only four cell strings STR**1**~STR**4** are connected to a same bit line BL in following figures. However, example embodiments are not limited thereto, and the number of cell strings may be determined variously.

[0082] FIG. **7** is a cross-sectional view illustrating a memory block according to example embodiments.

[0083] Referring to FIG. **7**, a memory block MB**1** may include a first sub block SB**1** disposed below a boundary portion BND and a second sub block SB**2** disposed above the boundary portion BND. For example, memory cells connected to a selected word line corresponding to a program address in the first sub block SB**1** are disposed vertically between the common source line CSL and the boundary portion BND. For example, memory cells connected to a selected word line corresponding to a program address in the second sub block SB**2** are disposed vertically between a corresponding bit line and the boundary portion BND. As described with reference to FIGS. **5** and **6**, the memory block MB**1** may include a plurality of cell strings STR**1**~STR**4** (e.g., NAND strings NS**11** to NS**41**), and each of the cell strings STR**1**~STR**4** may include a plurality of memory cells disposed in the vertical direction D**1**. The memory cells are connected to the word lines WL.

[0084] A plurality of string selection lines SSL**1**~SSL**4** may be formed in an uppermost gate layer of the memory block MB**1** (e.g., in each cell string), and a plurality of string selection transistors may be connected to the plurality of the string selection lines SSL**1**~SSL**4**, respectively, to control electric connections between the plurality of cell strings STR**1**~STR**4** and a bit line BL.

[0085] A plurality of ground selection lines GSL**1** and GSL**2** may be formed in a lowest gate layer of the memory block MB**1** (e.g., in each cell string), and a plurality of ground selection transistors may be connected to the plurality of the ground selection lines GSL**1** and GSL**2**, respectively, to control electric connections between the plurality of cell strings STR**1**~STR**4** and a source line CSL. Even though FIG. **7** illustrates that each ground selection line is assigned to two cell strings, example embodiments are not limited thereto.

[0086] A plurality of intermediate switching transistors MST**1**~MST**4** may be disposed in the boundary portion BND between the sub blocks SB**1** and SB**2** to control electrical connections with memory cells of the plurality of cell strings STR**1**~STR**4**, as will be described below with reference to FIGS. **8**A and **8**B. The plurality of intermediate switching transistors MST**1**~MST**4** are respectively connected to a plurality of intermediate switching lines MSL**1**~MSL**4**.

[0087] In some example embodiments, the cell strings STR**1**~STR**4** connected to the same bit line BL may be divided into a plurality of cell string groups where each group of the cell string groups is electrically connected to the same bit line through each of string selection transistors. Each of the plurality of intermediate switching transistors may be independently activated by units of the cell string groups based on the program address during the program operation.

[0088] In some example embodiments, as illustrated in FIG. **7**, the cell strings STR**1**~STR**4** connected to the same bit line BL may be grouped one by one, and the intermediate switching transistors may be independently activated one by one. Such independent switching may be implemented by separating the gate line in the boundary portion BND into the intermediate switching lines MSL**1**~MSL**4**.

[0089] In some example embodiments, as will be described below with reference to FIGS. **17** and **18**, each string group may include N cell strings connected to the same bit line where N is a natural number greater than 1, and the intermediate switching transistors corresponding to the same bit line may be independently activated N by N.

[0090] As described with reference to FIG. **3**, the address decoder **430** may select one of the string selection lines SSL as a selected string selection line based on the row address R_ADDR provided from the control circuit **450**. In the same way, the address decoder **430** may determine one of the plurality of intermediate switching lines MSL**1**~MSL**4** as a selected intermediate switching line. The selected intermediate switching transistors connected to the selected intermediate switching line may be turned on independently or selectively by applying a turn-on voltage to the selected intermediate switching line and applying a turn-off voltage to the other unselected intermediate switching lines.

[0091] FIG. **8**A is a circuit diagram illustrating an equivalent circuit corresponding to a structure of FIG. **7**, and FIG. **8**B is a perspective view illustrating a memory block corresponding to a structure of FIG. **7**.

[0092] FIG. **8**A illustrates two-dimensional version of a memory block including cell strings connected to one bit line BL and one source line CSL for convenience of illustration, but it will be understood that the memory block may have a three-dimensional structure of a plurality of bit lines as described with reference to FIGS. **5** and **6**.

[0093] Referring to FIGS. **8**A and **8**B, a memory block may include a plurality of cell strings STR**1**~STRm connected between a bit line BL and a source line CSL. The cell strings STR**1**~STRm may include string selection transistors SST**1**~SSTm controlled by string selection lines SSL**1**~SSLm, memory cells controlled by word lines WL, intermediate switching transistors MST**1**~MSTm controlled by intermediate switching lines MSL**1**~MSLm and a ground selection transistors controlled by a ground selection line, respectively. Here, m is a natural number grater than 1. The memory cells connected to word lines disposed in edge portions of the sub blocks SB**1** and SB**2** may be dummy cells. Data may not be stored in the dummy cells or smaller data bits may be stored in each of the dummy cells different from the normal cells.

[0094] In example embodiments, each of the dummy cells may be implemented as a cell-type such as a flash memory cell including a floating gate, or a transistor-type (e.g., a normal transistor) without the floating gate. For example, if each of the dummy cells is a normal transistor, the dummy cell may not have stored data, and if each of the dummy cells is a cell-type transistor, some data may be stored in each of the dummy cells.

[0095] FIG. **8**A illustrates an example embodiment that the ground selection transistors are connected to the same ground selection line GSL and FIG. **8**B illustrates another example embodiment that the ground selection transistors are connected to the respective ground selection lines GSL**1** and GSL**2**. However, example embodiments are not limited thereto.

[0096] As illustrated in FIGS. **8**A and **8**B, the intermediate switching transistors MST**1**~MSTm connected to the same bit line BL may be activated independently one by one by separating the gate line of the boundary portion BND into the intermediate switching lines MSL**1**~MSLm respectively corresponding to the cell strings STR**1**~STRm. The separated intermediate switching lines MSL**1**~MSLm may be extended along the second direction D**2** and arranged along the third direction D**3** as the string selection lines SSL~SSLm, as illustrated in FIG. **8**B.

[0097] In example embodiments, each of the intermediate switching transistors MST**1**~MSTm may be implemented as a cell-type such as a flash memory cell including a floating gate, or a transistor-type (e.g., a normal transistor) without the floating gate. If the intermediate switching transistor is a cell-type transistor, a threshold voltage of the intermediate switching transistor may be changed by a program operation.

[0098] FIGS. **9**A through **9**D are cross-sectional views illustrating a memory block according to example embodiments.

[0099] Memory blocks in FIGS. **9**A through **9**D are similar to the memory block as described with reference to FIGS. **7**, **8**A and **8**B, and the repeated descriptions may be omitted.

[0100] Referring to FIG. **9**A, a boundary portion of a memory block MB**2** may include two or more gate layers that are adjacent to each other in the vertical direction D**1**. FIG. **9**A illustrates two gate layers adjacent in the vertical direction D**1**, a first boundary portion BND**1** and a second boundary portion BND**2**, but example embodiments are not limited thereto. The boundary portion dividing the sub blocks may include three or more gate layers adjacent in the vertical direction D**1**.

[0101] The first boundary portion BND**1** may include a plurality of intermediate switching lines MSL**11**~MSL**14** controlling the respective electric connections of the cell strings STR**1**~STR**4** and the second boundary portion BND**2** may include a plurality of intermediate switching lines MSL**21**~MSL**24** controlling the respective electric connections of the cell strings STR**1**~STR**4**. The same driving voltage may be applied to the two intermediate switching lines MSL**1***i* and MSL**2***i* corresponding to the same cell string STRi.

[0102] As such, using the adjacent two or more gate lines as the boundary portion, with respect to each cell string, a lower string segment included in the first sub block SB**1** may be electrically disconnected from an upper string segment included in the second sub block SB**2**, and thus the effect of the local boosting may be enhanced.

[0103] Referring to FIG. **9**B, in a memory block MB**3**, at least one word line disposed in edge portions of the first sub block SB**1** and the second sub block SB**2** may be determined as a dummy word line DWL. The memory cells connected to the dummy word line DWL may be dummy cells in which data are not stored.

[0104] Dummy word lines DWL may be conductive lines formed adjacent to the plurality of word lines WL (e.g., normal gate lines). The dummy word lines DWL are patterned from the same conductive layers forming such normal gate lines. For example, dummy word lines DWL may be simultaneously formed with normal gate lines with the same processes that deposit and pattern the conductive layers forming normal gate lines.

[0105] Referring to FIG. **9**C, in a memory block MB**4**, M data bits may be stored in the memory cells connected to the word lines of edge portions and N data bits may be stored in the memory cells connected to the word lines of center portions of the sub blocks SB**1** and SB**2**, where M is smaller than N. For example, the memory cells of the edge portions may be operated as a single level cell (SLC) and the memory cells of the center portions may be operated as a multiple level cell (MLC).

[0106] As described with reference to FIGS. **9**B and **9**C, the characteristic degradation of the memory cells according to the manufacturing process may be compensated by operating the memory cells as the dummy cells in which data are not stored or data of smaller bits are stored.

[0107] Referring to FIG. **9**D, a memory block MB**5** may include a first stopper layer STP**1** disposed in a center portion and a second stopper layer STP**2** disposed in a lowest portion in each cell string. For example, intermediate switching transistors in the second stopper layer STP**2** may be simultaneously controlled by the same switching line. As will be described below with reference to FIG. **10**, the first stopper layer STP**1** may be used as the above-described boundary portion BND. With respect to the cell strings connected to the same bit line, the number of cell strings

connected to the same ground selection line may be two as illustrated in FIG. **9**A, four as illustrated in FIG. **9**D, and so on.

[0108] As the number of the word lines increases, that is, as the number of the gate lines stacked in the vertical direction increases, a multiple stack structure may be adopted due to problems of manufacturing process. As an example, FIG. **10** illustrates a double stack structure.

[0109] FIG. **10** is a cross-sectional view for describing an example embodiment of a boundary portion included in a memory block according to example embodiments.

[0110] Referring to FIG. **10**, a channel hole of each cell string STR may include a first sub channel hole **610** and a second sub channel hole **510**. A channel hole may be referred to as a pillar. The first sub channel hole **610** may include a channel layer **611**, an inner material **612** and an insulation layer **613**. The second sub channel hole **510** may include a channel layer **511**, an inner material **512** and an insulation layer **513**. The channel layer **611** of the first channel hole **610** may be connected to the channel layer **511** of the second sub channel hole **510** through a

[0111] P-type silicon pad SIP. The sub channel holes **610** and **510** may be formed using a stopper line GTL**5** having an appropriate etch rate. For example, the stopper line GTL**5** may be formed of polysilicon and the other gate lines GTL**1**~GTL**4** and the GTL**6**~GTL**8** may be formed of metal such as tungsten to implement the appropriate etch rate.

[0112] The above-described boundary portion BND may correspond to the stopper layer GTL**5** that is used to form the plurality of sub channel holes. The cells in the stopper layer GTL**5** may be improper for storing data, and the stopper layer may be used as the boundary portion BND to from the intermediate switching transistors. Example embodiments are not limited to a boundary portion of one stopper layer, and the boundary portion may include two or more gate layers.

[0113] FIG. **11** is a diagram illustrating a first program scenario according to example embodiments.

[0114] FIG. **11** illustrates one cell string STR including a string selection transistor SST connected to a string selection line SSL, a ground selection transistor GST connected to a ground selection line GSL and memory cells MC**1**~MC**12** connected to word lines WL**1**~WL**12** and states of memory cells. The cell string is connected between a bit line BL, a source line CSL and a substrate voltage SUB. FIG. **11** illustrates a non-limiting example of twelve memory cells and an MLC storing two bits.

[0115] Referring to FIG. **11**, according to a first program scenario, the program operation may be performed in an upward direction from a lowest word line. In other words, as the data stored in the memory block increase, the data may be filled in erased cells in the upward direction from bottom to top (B2T program order). The not-programmed memory cells MC**5**~MC**12** are in an erased state E**0**, and each of the programmed memory cells MC**1**~MC**4** may be in one of the erased state E**0** and programmed states P**1**, P**2** and P**3**. For example, at least one of the memory cells MC**2**~MC**11** may be an intermediate switching transistor.

[0116] FIG. **12** is a timing diagram illustrating a program operation of a first sub block according to the first program scenario of FIG. **11**.

[0117] FIG. **12** illustrates a selective activating of intermediate switching transistors when a selected word line WLs corresponding to a program address is included in a first sub block SB**1**. Time interval T**1**~T**2** is an initialization period and time interval T**3**~T**4** is a program period while a program voltage VPGM is applied to the selected word line WLs. Hereinafter, a turn-on voltage and a turn-off voltage represent voltage of levels to turn on and off a corresponding transistor. During the program operation, a turn-off voltage VGOFF may be applied to a ground selection line GSL and the cell string may be electrically disconnected from the source line CSL.

[0118] A program inhibition voltage VINH may be applied to an unselected bit line BLu. The program inhibition voltage VINH may be applied during the initialization period T**1**~T**2** and then a program permission voltage VPER may be applied to a selected bit line BLs.

[0119] A turn-on voltage VSON may be applied to a selected string selection line SSLs. The turn-on voltage VSON may be applied during the initialization period T**1**~T**2** and then a turn-off voltage VSOFF may be applied to an unselected string selection line SSLu. According to the turn-on voltage VSON or the turn-off voltage VSOFF, each string selection transistor may be activated selectively and the electrical connection between the bit line and the cell string STR may be controlled.

[0120] Accordingly the cell string may be electrically connected to the bit line BL during the program interval T**3**~T**4**, and the channel of the cell string may receive the program inhibition voltage VINH or the program permission voltage VPER depending on a data bit to be programmed. The unselected cell string STR may be electrically disconnected from the bit line BL and the source line CSL and thus floated.

[0121] During the program interval T**3**~T**4**, a program voltage VPGM may be applied to a selected word line WLs of the first sub block SB**1** and a first pass voltage VPASS**1** may be applied to an unselected word line WLu of the first sub block SB**1**. The first pass voltage VPASS**1** has a level capable of turning on a memory cell that has a highest threshold voltage distribution.

[0122] During the program interval T**3**~T**4**, a second pass voltage VPASS**2** lower than the first pass voltage VPASS**1** may be applied to an unselected word line of the second sub block SB**2**. According to the first program scenario, all of the memory cells of the second sub block SB**2** are in the erased state E**0**. Accordingly it is sufficient for the second pass voltage VPASS**2** to have a level capable of turning on the memory cell of the erased state E**0**. As such, using the second pass voltage VPASS**2** lower than the first pass voltage VPASS**1**, the pass voltage disturbance on the memory cells of the second sub block SB**2** may be reduced.

[0123] A turn-on voltage VMON may be applied to a selected intermediate switching line MSLs corresponding to the program address and a turn-off voltage VMOFF may be applied to the unselected intermediate switching lines MSLu except the selected intermediate switching line. As a result, during the program operation of the first sub block SB**1**, the selected intermediate switching transistor connected to the selected intermediate switching line MSLs may be turned on and the unselected intermediate switching transistor connected to the unselected intermediate switching line MSLu may be turned off.

[0124] As such, the local boosting may be implemented through the selective switching of the intermediate switching transistors based on the program address. In case of programming the word line of the first sub block SB**1**, at

time point T3 when the program voltage VPGM and the first pass voltage VPASS1 are applied to the word lines of the first sub block SB1, the channel of the unselected cell string may be boosted together and thus the stress on the memory cells irrelevant to programming may be reduced. The lower string segment of the unselected cell string may be electrically disconnected from the upper string segment of the unselected cell string by turning off the unselected intermediate switching transistor, and thus the local boosting of the lower string segment may be implemented. Through the local boosting, the program voltage disturbance and the pass voltage disturbance of the unselected cell string may be reduced.

[0125] FIG. **13** is a timing diagram illustrating a program operation of a second sub block according to the first program scenario of FIG. **11**. The descriptions repeated with FIG. **12** may be omitted.

[0126] Referring to FIG. **13**, when the selected word line WLs corresponding to the program address is included in the second sub block SB**2**, the first pass voltage VPASS**1** may be applied to the unselected word lines WLu of the second sub block SB**2** during the program interval T**3**~T**4**. The unselected word lines WLu included in the first sub block SB**1** may be floated or a low voltage VLOW lower than the first pass voltage VPASS**1** may be applied to the unselected word lines WLu included in the first sub block SB**1** during the program period T**3**~T**4**. The low voltage VLOW is for removing uncertainty when the unselected word lines WLu in the first sub block SB**1** are floated, and the low voltage VLOW may be lower than the second pass voltage VPASS**2** in FIG. **12**. For example, when the low voltage VLOW is applied to the unselected word lines WLu included in the first sub block SB**1**, the memory cells connected to the unselected word lines WLu included in the first sub block SB**1** may be in a turned off state. In some examples, the first pass voltage VPASS**1** may be applied to the unselected word lines WLu in the first sub block SB**1** during the program interval T**3**~T**4**.

[0127] When the selected word line WLs corresponding to the program address is included in the second sub block SB**2**, the turn-off voltage VMOFF may be applied to the selected intermediate switching line MSLs and the unselected intermediate switching line MSLu regardless of the program address. Accordingly all of the intermediate switching transistors may be turned off during the program operation regardless of the program address.

[0128] As such, the local boosting may be implemented through the selective switching of the intermediate switching transistors based on the program address. In case of programming the word line of the second sub block SB**2**, at time point T**3** when the program voltage VPGM and the first pass voltage VPASS**1** are applied to the word lines of the second sub block SB**2**, the channel of the unselected cell string may be boosted together and thus the stress on the memory cells irrelevant to programming may be reduced. With respect to the selected cell string and the unselected cell string, the upper string segment may be electrically disconnected from the lower string segment by turning off the selected and unselected intermediate switching transistors, and thus the local boosting of the upper string segment may be implemented. Through the local boosting, the program voltage disturbance and the pass voltage disturbance may be reduced.

[0129] FIG. **14** is a diagram illustrating a second program scenario according to example embodiments. The descriptions repeated with FIG. **11** may be omitted.

[0130] Referring to FIG. **14**, according to a second program scenario, the program operation may be performed in a downward direction from an uppermost word line. In other words, as the data stored in the memory block increase, the data may be filled in erased cells in the downward direction from top to bottom (T2B program order). The not-programmed memory cells MC**1**~MC**7** are in an erased state E**0**, and each of the programmed memory cells MC**8**~MC**12** may be in one of the erased state E**0** and programmed states P**1**, P**2** and P**3**. For example, at least one of the memory cells MC**2**~MC**11** may be an intermediate switching transistor.

[0131] FIG. **15** is a timing diagram illustrating a program operation of a first sub block according to the second program scenario of FIG. **14**, and FIG. **16** is a timing diagram illustrating a program operation of a second sub block according to the second program scenario of FIG. **15**.

[0132] The selective switching by the selected intermediate switching line MSLs and the unselected intermediate switching line MSLu of FIGS. **15** and **16** according to the second program scenario is the same as that of FIGS. **12** and **13** according to the first program scenario.

[0133] The descriptions repeated with FIGS. **12** and **13** may be omitted.

[0134] Referring to FIG. **15**, when the selected word line WLs corresponding to the program address is included in the first sub block SB**1**,

[0135] The same pass voltage VPASS**1** may be applied to the unselected word lines WLu included in the first sub block SB**1** and the unselected word lines WLu in the second sub block

[0136] SB during the program period T**3**~T**4**.

[0137] Referring to FIG. **16**, when the selected word line WLs corresponding to the program address is included in the second sub block SB**2**, the first pass voltage VPASS**1** may be applied to the unselected word lines WLu included in the second sub block SB**2** during the program period T**3**~T**4**. In contrast, the unselected word lines included in the first sub block SB**1** may be floated or the low voltage VLOW lower than the first pass voltage VPASS**1** may be applied to the unselected word lines included in the first sub block SB**1** during the program period T**3**~T**4**. For example, when the low voltage VLOW is applied to the unselected word lines WLu included in the first sub block SB**1**, the memory cells connected to the unselected word lines WLu included in the first sub block SB**1** may be in a turned off state.

[0138] FIGS. **17** and **18** are cross-sectional views illustrating a memory block according to example embodiments.

[0139] As described with reference to FIG. **7**, the cell strings STR**1**~STR**4** connected to the same bit line BL may be grouped into a plurality of cell string groups, where each of the cell strings is electrically connected to the same bit line through each of string selection transistors. The intermediate switching transistors may be independently activated by units of string groups. The descriptions repeated with FIG. **7** may be omitted.

[0140] In a memory block MB**6** of FIG. **17**, the cell strings STR**1**~STR**4** connected to the same bit line BL may be grouped two by two, and the intermediate switching transistors connected to the intermediate switching lines MSL**1** and MSL**2** may be independently activated two by two based on the program address. In contrast, a memory block

MB7 of FIG. 18, the cell strings STR1~STR4 connected to the same bit line BL may be grouped four by four, and the intermediate switching transistors connected to the intermediate switching lines MSL may be independently activated four by four based on the program address.

[0141] Hereinafter, example embodiments of a memory block including three sub blocks will be described with reference to FIGS. 19 through 25. The descriptions repeated with the example embodiment of the memory block including the two sub blocks may be omitted.

[0142] FIG. 19 is a cross-sectional view illustrating a memory block divided into three sub blocks according to example embodiments.

[0143] Referring to FIG. 19, the above-described boundary portion BND may include a lower boundary portion BNDL and an upper boundary portion BNDU. A memory block MB8 may include a first sub block SB1 below the lower boundary portion BNDL, a second sub block SB2 between the lower boundary portion BNDL and the upper boundary portion BNDU and a third sub block SB3 above the upper boundary portion BNDU.

[0144] The above-described intermediate switching transistors may include a plurality of lower switching transistors disposed in the lower boundary portion BNDL and connected to the lower switching lines LSL1~LSL4 and a plurality of upper switching transistors disposed in the upper boundary portion BNDU and connected to the upper switching lines USL1~USL4.

[0145] FIGS. 20 through 22 are diagrams illustrating program operations of sub blocks in FIG. 19 according to the first program scenario of FIG. 11. FIGS. 23 through 25 are diagrams illustrating program operations of sub blocks in FIG. 19 according to the second program scenario of FIG. 14.

[0146] FIGS. 20 through 25 illustrate driving voltages of gate lines SSL, WLu, WLs, USL, LSL and GSL with respect to a case of a selected cell string and a case of an unselected cell string. Hereinafter, the descriptions repeated with the first program order B2T of FIGS. 11, 12 and 13 and the second program order T2B of FIGS. 14, 15 and 16 may be omitted. The voltages VPGM, VPASS1, VPASS2 and VLOW applied to the selected word line WLs and the unselected word line WLu and the voltages VSON, VSOFF, VGON and VGOFF applied to the selection lines SSL and GSL are the same as the descriptions of FIGS. 11 through 16.

[0147] During the program operation, the program inhibition voltage VINH or the program permission voltage VPER may be applied to the bit line BL depending on the data bit to be programmed. For example, a ground voltage GND may be applied to the source line CSL.

[0148] FIGS. 20 through 25 illustrate a non-limiting example that the lower switch transistor corresponds to the fourth memory cell MC4 and the upper switch transistor corresponds to the eighth memory cell MC8 for convenience of illustration, and example embodiments are not limited thereto. The switching operation of the lower switching transistor MC4 may be controlled by the lower switching line LSL and switching operation of the upper switching transistor MC8 may be controlled by the upper switching line USL.

[0149] Referring to FIGS. 20 and 23, when the selected word line WLs corresponding to the program address is included in the first sub block SB1, the selected lower switching transistors and the selected upper switching transistors corresponding to the program address may be turned on. In contrast, the unselected lower switching transistors except the selected lower switching transistors and unselected upper switching transistors except the selected upper switching transistors may be turned off.

[0150] Referring to FIGS. 21 and 24, when the selected word line WLs corresponding to the program address is included in the second sub block SB2, the selected upper switching transistors corresponding to the program address may be turned on. In contrast, the selected lower switching transistors corresponding to the program address, the unselected lower switching transistors except the selected lower switching transistors and unselected upper switching transistors except the selected upper switching transistors may be turned off.

[0151] Referring to FIGS. 22 and 25, when the selected word line WLs corresponding to the program address is included in the third sub block SB3, the plurality of lower switching transistors and the plurality of upper switching transistors may be turned off regardless of the program address.

[0152] As such, the nonvolatile memory device and the method of programming in the nonvolatile memory device according to example embodiments may reduce program voltage disturbance and pass voltage disturbance and thus increase performance and lifetime of the nonvolatile memory device through independent switching of the intermediate switching transistors to implement local boosting of string segments irrelevant to programming.

[0153] FIG. 26 is a block diagram illustrating a solid state disk or solid state drive (SSD) according to example embodiments.

[0154] Referring to FIG. 26, an SSD 1000 includes multiple nonvolatile memory devices 1100 and an SSD controller 1200.

[0155] The nonvolatile memory devices 1100 may be configured optionally to receive a high voltage VPP. The nonvolatile memory devices 1100 may be the above-described memory devices disclosed above. The nonvolatile memory devices 1100 may include the intermediate switching transistors to implementing the local boosting of the string segment by selectively activating each of the intermediate switching transistors based on the program address.

[0156] The SSD controller 1200 is connected to the nonvolatile memory devices 1100 through multiple channels CH1 to CHi. The SSD controller 1200 includes one or more processors 1210, a buffer memory 1220, an error correction code (ECC) circuit 1230, a host interface 1250, and a nonvolatile memory interface 1260. The buffer memory 1220 stores data used to drive the SSD controller 1200. The buffer memory 1220 comprises multiple memory lines each storing data or a command. The ECC circuit 1230 calculates error correction code values of data to be programmed at a writing operation and corrects an error of read data using an error correction code value at a read operation. In a data recovery operation, The ECC circuit 1230 corrects an error of data recovered from the nonvolatile memory devices 1100.

[0157] As described above, the nonvolatile memory device and the method of programming in the nonvolatile memory device according to example embodiments may reduce program voltage disturbance and pass voltage disturbance and thus increase performance and lifetime of the nonvolatile memory device through independent switching

of the intermediate switching transistors to implement local boosting of string segments irrelevant to programming.

[0158] The present inventive concept may be applied to any electronic devices and systems requiring the PIM of the encrypted data. For example, the present inventive concept may be applied to systems such as be a memory card, a solid state drive (SSD), an embedded multimedia card (eMMC), a mobile phone, a smart phone, a personal digital assistant (PDA), a portable multimedia player (PMP), a digital camera, a camcorder, personal computer (PC), a server computer, a workstation, a laptop computer, a digital TV, a set-top box, a portable game console, a navigation system, a wearable device, an internet of things (IoT) device, an internet of everything (IoE) device, an e-book, a virtual reality (VR) device, an augmented reality (AR) device, etc.

[0159] The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the spirit and scope of the following claims.

What is claimed is:

1. A method of programming in a nonvolatile memory device, the method comprising:

providing a memory block comprising a plurality of sub blocks disposed in a vertical direction where the memory block includes a plurality of cell strings each comprising a plurality of memory cells connected in series and disposed in the vertical direction;

providing a plurality of intermediate switching transistors disposed in a boundary portion between two adjacent sub blocks in the vertical direction; and

selectively activating each of the plurality of intermediate switching transistors based on a program address during a program operation,

wherein selectively activating each of the plurality of intermediate switching transistors includes selectively turning on one or more intermediate switching transistors in a selected cell string based on the program address.

2. The method of claim **1**, wherein selectively activating each of the plurality of intermediate switching transistors includes:

when a selected word line corresponding to the program address is included in a sub block below the boundary portion,

turning on one or more intermediate switching transistors in a selected cell string; and

turning off intermediate switching transistors in unselected cell strings.

3. The method of claim **1**, wherein selectively activating each of the plurality of intermediate switching transistors includes:

when a selected word line corresponding to the program address is included in a sub block above the boundary portion, turning off the plurality of intermediate switching transistors regardless of the program address.

4. The method of claim **1**, wherein the plurality of cell strings includes a plurality of string groups each connected to the same bit line, wherein each of the cell strings is electrically connected to the same bit line through a respective string selection transistor, the method further comprising:

independently activating the plurality of intermediate switching transistors by units of the string groups based on the program address during the program operation.

5. The method of claim **1**, further comprising:

when a selected word line corresponding to the program address is included in a first sub block below the boundary portion, applying a first pass voltage to unselected word lines included in the first sub block and applying a second pass voltage lower than the first pass voltage to unselected word lines included in a second sub block above the boundary portion while applying a program voltage to the selected word line.

6. The method of claim **1**, further comprising:

when a selected word line corresponding to the program address is included in a second sub block above the boundary portion, applying a pass voltage to unselected word lines included in the second sub block and floating or applying a low voltage lower than the pass voltage to unselected word lines included in a first sub block below the boundary portion while applying a program voltage to the selected word line.

7. The method of claim **1**, further comprising:

when a selected word line corresponding to the program address is included in a first sub block below the boundary portion, applying the same pass voltage to unselected word lines included in the first sub block and a second sub block above the boundary portion while applying a program voltage to the selected word line.

8. The method of claim **7**, further comprising:

when a selected word line corresponding to the program address is included in the second sub block, applying the same pass voltage to unselected word lines included in the first and second sub blocks while applying the program voltage to the selected word line.

9. The method of claim **1**, wherein the boundary portion includes a lower boundary portion and an upper boundary portion in each cell string,

wherein the plurality of sub blocks includes a first sub block below the lower boundary portion, a second sub block between the lower boundary portion and the upper boundary portion and a third sub block above the upper boundary portion,

wherein the plurality of intermediate switching transistors include a plurality of lower switching transistors disposed in the lower boundary portion and a plurality of upper switching transistors disposed in the upper boundary portion, and

wherein selectively activating each of the plurality of intermediate switching transistors includes:

when a selected word line corresponding to the program address is included in the first sub block,

turning on one or more lower switching transistors and one or more upper switching transistors in a selected cell string, and

turning off lower and upper switching transistors in unselected cell strings.

10. The method of claim **9**, wherein selectively activating each of the plurality of intermediate switching transistors further includes:

when a selected word line corresponding to the program address is included in the second sub block:

in the selected cell string, turning on one or more upper switching transistors and turning off one or more lower switching transistors, and

turning off lower and upper switching transistors in unselected cell strings.

11. The method of claim **9**, wherein selectively activating each of the plurality of intermediate switching transistors further includes:

when a selected word line corresponding to the program address is included in the third sub block, turning off the plurality of lower and upper switching transistors regardless of the program address.

12. A method of programming in a nonvolatile memory device, comprising:

providing a memory block comprising a first sub block below a stopper layer and a second sub block above the stopper layer where the memory block includes a plurality of cell strings each comprising a plurality of memory cells connected in series and disposed in a vertical direction;

providing a plurality of intermediate switching transistors disposed in the stopper layer;

turning on one or more intermediate switching transistors in a selected cell string when a selected word line corresponding to a program address is included in the first sub block during a program operation; and

turning off the one or more intermediate switching transistors in the selected cell string when the selected word line is included in the second sub block during the program operation.

13. The method of claim **12**, further comprising:

when the selected word line is included in the first sub block, applying a first pass voltage to unselected word lines in the first sub block and applying a second pass voltage equal to or less than the first pass voltage to unselected word lines in the second sub block while applying a program voltage to the selected word line, and

when the selected word line is included in the second sub block, floating or applying a low pass voltage less than the second pass voltage to the unselected word lines in the first sub block and applying the first pass voltage to the unselected word lines in the second sub block, while applying the program voltage to the selected word line.

14. The method of claim **12**, further comprising:

when the selected word line is included in the first sub block, applying a first pass voltage to unselected word lines in the first sub block and applying a second pass voltage equal to or less than the first pass voltage to unselected word lines in the second sub block, while applying a program voltage to the selected word line, and

when the selected word line is included in the second sub block, applying the first pass voltage to the unselected word lines in the first and second sub blocks, while applying the program voltage to the selected word line.

15. A nonvolatile memory device comprising:

a memory block divided into a plurality of sub blocks and including a plurality of cell strings each comprising a plurality of memory cells connected in series and disposed in a vertical direction;

a plurality of intermediate switching transistors disposed in a boundary portion between two adjacent sub blocks in the vertical direction; and

a control circuit configured to selectively turn on one or more intermediate switching transistors in a selected cell string independently of intermediate switching transistors in unselected cell strings based on a program address during a program operation.

16. The nonvolatile memory device of claim **15**, wherein when a selected word line corresponding to the program address is included in a first sub block below the boundary portion, the control circuit turns on the one or more intermediate switching transistors in the selected cell string and turns off intermediate switching transistors in unselected cell strings.

17. The nonvolatile memory device of claim **16**, wherein when a selected word line corresponding to the program address is included in a second sub block above the boundary portion, the control circuit turns off the plurality of intermediate switching transistors.

18. The nonvolatile memory device of claim **16**, further comprising:

an address decoder configured to provide a plurality of voltages to word lines based on the program address,

wherein when a selected word line corresponding to the program address is included in a first sub block above the boundary portion, the address decoder provides a program voltage to the selected word line, a first pass voltage to unselected word lines included in the first sub block, and a second pass voltage lower than the first pass voltage to or floating unselected word lines included in a second sub block below the boundary portion.

19. The nonvolatile memory device of claim **15**, wherein the plurality of intermediate switching transistors disposed in the boundary portion includes a first set of intermediate switching transistors and a second set of intermediate switching transistors, wherein each intermediate switching transistor of the first set of intermediate switching transistors is disposed adjacent to and is connected to a respective intermediate switching transistor of the second set of intermediate switching transistors in the vertical direction.

20. The nonvolatile memory device of claim **15**, wherein each of the plurality of cell strings includes:

a first memory cell connected to a first word line formed adjacent to the boundary portion, and configured to store a number of bits smaller than a number of bits stored in each memory cell other than the first memory cell.

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