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Application Number: 16729838

Document Date: 12/30/2019

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- Drawing

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UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	Attorney Docket No.	4123.0850001
	First Named Inventor	Zilong CHEN
	Title	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
	Priority Mail Express® Label No.	

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>	Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
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1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent) 2. ☐ Applicant asserts small entity status. See 37 CFR 1.27 3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent. 4. ☒ Specification [Total Pages <u>24</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement) 5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>8</u>] 6. Inventor's Oath or Declaration [Total Pages _____] (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e)) a. ☐ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) 7. ☒ Application Data Sheet * See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent) 8. CD-ROM or CD-R in duplicate, large table, or Computer Program (Appendix) ☐ Landscape Table on CD 9. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. – c. are required) a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PAPERS 10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee <u>Yangtze Memory Technologies Co., Ltd.</u> 11. ☐ 37 CFR 3.73(c) Statement ☒ Power of Attorney (when there is an assignee) 12. ☐ English Translation Document (if applicable) 13. ☐ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached 14. ☐ Preliminary Amendment 15. ☐ Return Receipt Postcard (MPEP § 503) (Should be specifically itemized) 16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 18. ☒ Other: <u>EOT Authorization Under 37 C.F.R. 1.136(a)(3)</u> <u>Filing Fees: \$1720.00</u> <u>Surcharge Fee: \$160.00</u> _____ _____
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***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS				
☒ The address associated with Customer Number: <u>26111</u> OR ☐ Correspondence address below				
Name				
Address				
City	State	Zip Code		
Country	Telephone	Email		

Signature	/Donald J. Featherstone/	Date	12/30/19
Name (Print/Type)	Donald J. Featherstone	Registration No. (Attorney/Agent)	33,876

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0850001
		Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
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Inventor Information:

Inventor	1				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Zilong		CHEN		
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service					
City	Wuhan, Hubei		Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.				
Address 2	No. 88 Weilai 3rd Rd, East Lake High-Tech Dev Zone				
City	Wuhan, Hubei	State/Province			
Postal Code	430000	Country ⁱ	CN		

Inventor	2				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Xiang		FU		
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service					
City	Wuhan, Hubei		Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.				
Address 2	No. 88 Weilai 3rd Rd, East Lake High-Tech Dev Zone				
City	Wuhan, Hubei	State/Province			
Postal Code	430000	Country ⁱ	CN		

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Add

Correspondence Information:

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0850001
		Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence information of this application.

Customer Number	26111		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		
Attorney Docket Number	4123.0850001	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	26111		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0850001
		Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2019/112728	2019-10-23
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)	Remove
Additional Foreign Priority Data may be generated within this form by selecting the Add button.				Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0850001
		Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0850001
		Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.					
Applicant	1	<button>Remove</button>			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.					
<button>Clear</button>					
Assignee	Legal Representative under 35 U.S.C. 117		Joint Inventor		
● Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest			
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:					
Name of the Deceased or Legally Incapacitated Inventor:					
If the Applicant is an Organization check here. ☒					
Organization Name	Yangtze Memory Technologies Co., Ltd.				
Mailing Address Information For Applicant:					
Address 1	No. 88 Weilai 3rd Road				
Address 2	East Lake High-Tech Development Zone				
City	Wuhan, Hubei	State/Province			
Country	CN	Postal Code	430000		
Phone Number		Fax Number			
Email Address					
Additional Applicant Data may be generated within this form by selecting the Add button. <button>Add</button>					

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0850001
		Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		

Assignee	1		
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.			
Remove			
If the Assignee or Non-Applicant Assignee is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1	No. 88 Weilai 3rd Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	State/Province	
Country i	CN	Postal Code	430000
Phone Number		Fax Number	
Email Address			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add			

Signature:[Remove](#)

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the **INITIAL** filing of the application and either box A or B is **not** checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Donald J. Featherstone/		Date (YYYY-MM-DD)	2019-12-30	
First Name	Donald J.	Last Name	Featherstone	Registration Number	33,876
Additional Signature may be generated within this form by selecting the Add button. Add					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0850001
		Application Number	
Title of Invention	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: CHEN *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: To Be Assigned

(*Continuation of Appl. No.*
PCT/CN2019/112728; Filed October 23,
2019)

Filed: Herewith

Confirmation No.: To Be Assigned

Art Unit: To Be Assigned

Examiner: To Be Assigned

Atty. Docket: 4123.0850001

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

**Authorization to Treat a Reply as Incorporating an
Extension of Time Under 37 C.F.R. § 1.136(a)(3)**

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 12/30/19

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

SKGF_DC1:14339211.1

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Zilong CHEN
Title	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0850001

SIGNATURE of Applicant or Patent Practitioner

Signature	/Donald J. Featherstone/	Date (Optional)	12/30/19
Name	Donald J. Featherstone	Registration Number	33,876
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

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METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS AND INCORPORATION BY REFERENCE

[0001] This application claims priority to PCT/CN2019/112728 filed on October 23, 2019, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a method for reading a three-dimensional (3D) memory.

BACKGROUND

[0003] As memory devices are shrinking to smaller die size to reduce manufacturing cost and increase storage density, scaling of planar memory cells faces challenges due to process technology limitations and reliability issues. A three-dimensional (3D) memory architecture can address the density and performance limitation in planar memory cells.

[0004] In a 3D NAND flash memory, memory cells can be programmed for data storage based on charge-trapping technology. The storage information of a memory cell depends on the amount of charge trapped in a storage layer. However, fast charges, *i.e.*, charges trapped in shallow traps, can be easily lost. Therefore, the threshold voltage determining the stored information can be different between write and read operations. Accordingly, a read-prepare step is included in a read-verification operation after programming to remove the fast charges and verify the threshold voltage of the memory cell. Fast charge loss depending on the intrinsic de-trapping process in the storage layer can be long, making the read-verification operation inefficient. Therefore, a need exists for a method to accelerate fast charge loss so that threshold voltage or storage information of the memory cell can be verified or read more accurately and efficiently.

BRIEF SUMMARY

- [0005]** Embodiments of a method for conducting read-verification operation of a memory cell in a three-dimensional (3D) memory device is described in the present disclosure.
- [0006]** One aspect of the present disclosure provides a method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device. The method includes removing fast charges of the target memory cell at a read-prepare step, which includes applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL). The method also includes measuring a threshold voltage of the target memory cell at a sensing step.
- [0007]** In some embodiments, the method further includes applying a top select gate voltage (V_{tsg}) on a selected top select gate (Sel_TSG) of a selected memory string containing the target memory cell, and applying a lower select gate voltage (V_{lsg}) on a lower select gate (LSG) of the selected memory string containing the target memory cell.
- [0008]** In some embodiments, applying the top select gate voltage (V_{tsg}) includes electrically connecting the selected memory string to a bit line. In some embodiments, applying the lower select gate voltage (V_{lsg}) includes electrically connecting the selected memory string to an array common source.
- [0009]** In some embodiments, applying the top select gate voltage (V_{tsg}) includes applying a voltage between 4V to 7V. In some embodiments, applying the lower select gate voltage (V_{lsg}) includes applying a voltage between 4V to 7V.
- [0010]** In some embodiments, applying the pass voltage (V_{pass}) includes applying the pass voltage with a delay period after the selected top select gate (Sel_TSG) and the lower select gate (LSG) are at the top select gate voltage (V_{tsg}) and the lower select gate voltage (V_{lsg}), respectively.
- [0011]** In some embodiments, measuring the threshold voltage includes applying a read voltage (V_{read}) on the selected word line (Sel_WL). In some embodiments, applying the read voltage (V_{read}) includes applying a voltage between 0 to 2V. In some embodiments, applying the read voltage (V_{read}) includes applying a second off voltage on the unselected word line

(Unsel_WL). In some embodiments, applying the second off voltage on the unselected word line (Unsel_WL) includes applying a 0V.

[0012] In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is higher than a threshold voltage of an unselected memory cell. In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) equals to a threshold voltage of an unselected memory cell. In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is lower than a threshold voltage of an unselected memory cell.

[0013] In some embodiments, applying the prepare voltage (V_{prepare}) includes applying a voltage between 4V to 7V. In some embodiments, applying the first off voltage (V_{off}) includes applying a 0V. In some embodiments, applying the pass voltage (V_{pass}) includes applying a voltage between 5V to 9V.

In some embodiments, removing the fast charges includes removing the fast charges from a storage layer of the target memory cell of a selected memory string, wherein the selected memory string includes a channel hole penetrating vertically through a film stack of alternating conductive and dielectric layers, a core filling film in a center of the channel hole, and a memory film covering a sidewall of the channel hole. The selected memory string also includes a channel layer sandwiched between the memory film and the core filling film. In some embodiments, the memory film includes a barrier layer, the storage layer and a tunneling layer.

[0014] In some embodiments, removing the fast charges includes removing electrical charges from shallow traps in the storage layer of the target memory cell.

[0015] In some embodiments, removing the fast charges includes removing the fast charges from the target memory cell to a neighboring unselected memory cell.

[0016] In some embodiments, conducting the read-verification operation comprises conducting the read-prepare step and conducting a failed bit count in parallel.

[0017] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0018]** The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.
- [0019]** Fig. 1 illustrates a schematic top-down view of an exemplary three-dimensional (3D) memory die, according to some embodiments of the present disclosure.
- [0020]** Fig. 2 illustrates a schematic top-down view of a region of 3D memory die, according to some embodiments of the present disclosure.
- [0021]** Fig. 3 illustrates a perspective view of a portion of an exemplary 3D memory array structure, in accordance with some embodiments of the present disclosure.
- [0022]** Fig. 4(a) illustrates a cross-sectional view of 3D memory cells, according to some embodiments of the present disclosure.
- [0023]** Fig. 4(b) illustrates a schematic diagram of a 3D memory array, according to some embodiments of the present disclosure.
- [0024]** Fig. 5 illustrates a timing diagram of a read-verification operation with a prepare voltage (pre-pulse) applied on a selected word line, according to some embodiments of the present disclosure.
- [0025]** Figs. 6-8 illustrate timing diagrams of read-verification operations with accelerated fast charge loss, according to some embodiments of the present disclosure.
- [0026]** The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.
- [0027]** Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0028] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0029] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0030] In general, terminology can be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0031] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something, but also includes the meaning of “on” something with an intermediate feature or a layer there between. Moreover, “above” or “over” not only means

“above” or “over” something, but can also include the meaning it is “above” or “over” something with no intermediate feature or layer there between (i.e., directly on something).

[0032] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, can be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or process step in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0033] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate includes a “top” surface and a “bottom” surface. The top surface of the substrate is typically where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate unless stated otherwise. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0034] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, there above, and/or there below. A layer can include multiple layers. For

example, an interconnect layer can include one or more conductive and contact layers (in which contacts, interconnect lines, and/or vertical interconnect accesses (VIAs) are formed) and one or more dielectric layers.

[0035] In the present disclosure, for ease of description, “tier” is used to refer to elements of substantially the same height along the vertical direction. For example, a word line and the underlying gate dielectric layer can be referred to as “a tier,” a word line and the underlying insulating layer can together be referred to as “a tier,” word lines of substantially the same height can be referred to as “a tier of word lines” or similar, and so on.

[0036] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process step, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0037] In the present disclosure, the term “horizontal/horizontally/lateral/laterally” means nominally parallel to a lateral surface of a substrate, and the term “vertical” or “vertically” means nominally perpendicular to the lateral surface of a substrate.

[0038] As used herein, the term “3D memory” refers to a three-dimensional (3D) semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate.

[0039] Fig. 1 illustrates a top-down view of an exemplary three-dimensional (3D) memory device 100, according to some embodiments of the present disclosure. The 3D memory device 100 can be a memory chip (package), a memory die or any portion of a memory die, and can include one or more memory planes 101, each of which can include a plurality of memory blocks 103. Identical and concurrent operations can take place at each memory plane 101. The memory block 103, which can be megabytes (MB) in size, is the smallest size to carry out erase operations. Shown in Fig. 1, the exemplary 3D memory device 100 includes four memory planes 101 and each memory plane 101 includes six memory blocks

103. Each memory block 103 can include a plurality of memory cells, where each memory cell can be addressed through interconnections such as bit lines and word lines. The bit lines and word lines can be laid out perpendicularly (e.g., in rows and columns, respectively), forming an array of metal lines. The direction of bit lines and word lines are labeled as “BL” and “WL” in Fig. 1. In this disclosure, memory block 103 is also referred to as a “memory array” or “array.” The memory array is the core area in a memory device, performing storage functions.

[0040] The 3D memory device 100 also includes a periphery region 105, an area surrounding memory planes 101. The periphery region 105 contains many digital, analog, and/or mixed-signal circuits to support functions of the memory array, for example, page buffers, row and column decoders and sense amplifiers. Peripheral circuits use active and/or passive semiconductor devices, such as transistors, diodes, capacitors, resistors, etc., as would be apparent to a person of ordinary skill in the art.

[0041] It is noted that, the arrangement of the memory planes 101 in the 3D memory device 100 and the arrangement of the memory blocks 103 in each memory plane 101 illustrated in Fig. 1 are only used as an example, which does not limit the scope of the present disclosure.

[0042] Referring to Fig. 2, an enlarged top-down view of a region 108 in Fig. 1 is illustrated, according to some embodiments of the present disclosure. The region 108 of the 3D memory device 100 can include a staircase region 210 and a channel structure region 211. The channel structure region 211 can include an array of memory strings 212, each including a plurality of stacked memory cells. The staircase region 210 can include a staircase structure and an array of contact structures 214 formed on the staircase structure. In some embodiments, a plurality of slit structures 216, extending in WL direction across the channel structure region 211 and the staircase region 210, can divide a memory block into multiple memory fingers 218. At least some slit structures 216 can function as the common source contact (e.g., array common source) for an array of memory strings 212 in channel structure regions 211. A top select gate cut 220 can be disposed, for example, in the middle of each memory finger 218 to divide a top select gate (TSG) of the memory finger 218 into two portions, and thereby can divide a memory finger into two memory slices 224, where memory cells in a memory slice 224 that share the same word line form a programmable (read/write) memory page. While erase operation of a 3D NAND memory can be carried out

at memory block level, read and write operations can be carried out at memory page level. A memory page can be kilobytes (KB) in size. In some embodiments, region 108 also includes dummy memory strings 222 for process variation control during fabrication and/or for additional mechanical support.

[0043] Fig. 3 illustrates a perspective view of a portion of an exemplary three-dimensional (3D) memory array structure 300, according to some embodiments of the present disclosure. The memory array structure 300 includes a substrate 330, an insulating film 331 over the substrate 330, a tier of lower select gates (LSGs) 332 over the insulating film 331, and a plurality of tiers of control gates 333, also referred to as “word lines (WLs),” stacking on top of the LSGs 332 to form a film stack 335 of alternating conductive and dielectric layers. The dielectric layers adjacent to the tiers of control gates are not shown in Fig. 3 for clarity.

[0044] The control gates of each tier are separated by slit structures 216-1 and 216-2 through the film stack 335. The memory array structure 300 also includes a tier of top select gates (TSGs) 334 over the stack of control gates 333. The stack of TSG 334, control gates 333 and LSG 332 is also referred to as “gate electrodes.” The memory array structure 300 further includes memory strings 212 and doped source line regions 344 in portions of substrate 330 between adjacent LSGs 332. Each memory strings 212 includes a channel hole 336 extending through the insulating film 331 and the film stack 335 of alternating conductive and dielectric layers. Memory strings 212 also includes a memory film 337 on a sidewall of the channel hole 336, a channel layer 338 over the memory film 337, and a core filling film 339 surrounded by the channel layer 338. A memory cell 340 can be formed at the intersection of the control gate 333 and the memory string 212. The memory array structure 300 further includes a plurality of bit lines (BLs) 341 connected with the memory strings 212 over the TSGs 334. The memory array structure 300 also includes a plurality of metal interconnect lines 343 connected with the gate electrodes through a plurality of contact structures 214. The edge of the film stack 335 is configured in a shape of staircase to allow an electrical connection to each tier of the gate electrodes.

[0045] In Fig. 3, for illustrative purposes, three tiers of control gates 333-1, 333-2, and 333-3 are shown together with one tier of TSG 334 and one tier of LSG 332. In this example, each memory string 212 can include three memory cells 340-1, 340-2 and 340-3, corresponding to the control gates 333-1, 333-2 and 333-3, respectively. In some embodiments, the number of

control gates and the number of memory cells can be more than three to increase storage capacity. The memory array structure 300 can also include other structures, for example, TSG cut, common source contact (i.e., array common source) and dummy memory string. These structures are not shown in Fig. 3 for simplicity.

[0046] While floating gate memory cells has been traditionally utilized in flash memories, technology based on charge trapping has demonstrated more scaling ability and higher intrinsic reliability. Three-dimensional NAND using charge trapping technology has been developed for high density storage, where the storage information (*e.g.*, threshold voltage V_{th} of the memory cell) depends on the amount of charge trapped in a storage layer.

[0047] Fig. 4(a) illustrates a schematic cross-section of a 3D NAND memory 400a, which includes memory cells similar to the memory cell 340 in Fig. 3. The memory cell 340-3 includes a control gate (*e.g.*, the control gate 333), a memory film (*e.g.*, the memory film 337) and a channel layer (*e.g.*, the channel layer 338, also referred to as the channel).

[0048] In a 3D NAND memory, the memory film 337 can be disposed on a sidewall of each channel hole 336 (illustrated in Fig. 3). In some embodiments, the memory film 337 can include a barrier layer 422, a storage layer 424, and a tunneling layer 426. The barrier layer 422 can be used to block the movement of electronic charges 428 between the control gate 333 and the storage layer 424. The barrier layer 422 can include silicon oxide and high dielectric constant (high-k) dielectrics, for example, aluminum oxide. The storage layer 424 can be used to store electronic charges 428 and can include silicon nitride. The storage and/or removal of charges in the storage layer 424 can impact the on/off state and/or a conductance of the channel layer 338. The tunneling layer 426 can be used to control the tunneling of electronic charges 428 (electrons or holes) between the channel layer 338 and the storage layer 424. The tunneling layer 426 can be silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In a 3D NAND memory, the channel layer 338 can be disposed on a sidewall of the memory film 337 in the channel hole 336 (in Fig. 3.) The channel layer 338 can include amorphous silicon, polycrystalline silicon, and/or monocrystalline silicon.

[0049] Fig. 4(b) shows a schematic circuit diagram of a 3D memory array 400b. As described previously, the 3D memory array 400b includes a plurality of memory strings 212, each memory string 212 having a plurality of stacked memory cells 340. The memory string 212 also includes at least one field effect transistor (*e.g.*, MOSFET) at each end, which is

controlled by the lower select gate (LSG) 332 and the top select gate (TSG) 334, respectively. And the two respective transistors are referred to as lower and top select transistors 332-T and 334-T. The stacked memory cells 340 can be controlled by the control gates 333, where the control gates 333 are connected to word lines (not shown) of the 3D memory array 400b. The drain terminal of the top select transistor 334-T can be connected to the bit lines (*e.g.*, the bit line 341-1, 341-2, 341-3, etc.), and the source terminal of the lower select transistor 332-T can be connected to the doped source line region 344 (*see* Fig. 3), from where an array common source (ACS) 446 can be formed. The array common source 446 can be shared by the memory strings 212 in an entire memory block, and is also referred to as the common source line.

[0050] Referring to Figs. 4(a) and 4(b), in a NAND memory, read and write operations can be performed in a memory page, for example memory page 448, which includes memory cells sharing the same word line. In a NAND memory, each memory cell can be in an erased state or a programmed state. Initially, all memory cells in a block can be reset to the erased state as logic “1” by applying, for example, a negative voltage between the control gates 333 and source terminals of the memory cells (*e.g.*, the array common source 446) such that all the electronic charges 428 in the storage layers 424 of the memory cells can be removed. At the erased state, the threshold voltage V_{th} of the memory cells 340 can be reset to the lowest value, and the corresponding current flowing through the memory cells 340 between the source terminal (*e.g.*, the array common source 446) and the drain terminal (*e.g.*, the bit lines 341) can be at the highest level for a given bias on the word lines.

[0051] During programming (*i.e.*, writing), a high positive voltage pulse (*e.g.*, 12V to 18V) can be applied on the control gate 333 such that electronic charges 428 (*e.g.*, electrons) can be injected into the storage layer 424 of the memory cell 340, where the electronic charges 428-1 and 428-2 can be randomly captured by deep and shallow traps, respectively. After programming, the threshold voltage V_{th} of the memory cell 340 can be raised to a higher value than that of the erased state. At a higher threshold voltage V_{th} , the current flowing through the source and drain terminals of the memory cell can be at a reduced level for a given bias on the word lines. By measuring (*i.e.*, reading) the memory cell current, the threshold voltage V_{th} and thereby the state of the memory cell 340 can be determined accordingly.

- [0052] With multi-level-cell or triple-level-cell technology, each memory cell 340 can have multiple programmed states, *i.e.*, multiple values of threshold voltages V_{th} . After every programming pulse, a read-verification operation can be performed to check the state of the memory cell. As such, each memory cell 340 can store multiple bits, leading to significant increase of storage capacity.
- [0053] For memory cell 340 in a programmed state, electronic charges 428-1 and 428-2 located within the proximity of control gate 333 can affect threshold voltage V_{th} of the memory cell 340. The electronic charges 428-3 located beyond the electric field from control gate 333, and therefore have little impact on the threshold voltage V_{th} of the memory cell. In addition, electronic charges 428-2 captured by shallow traps in the storage layer 424 can be easily de-trapped, and can thereby cause initial threshold-voltage (V_{th}) shift (IVS) during storage period. This process is also referred to as fast charge loss. For programmed state at higher threshold voltage V_{th} , IVS can be larger due to larger amount of electronic charges injected to the storage layer, which results in larger number of electronic charges 428-2 captured by shallow traps (also referred to as fast charges).
- [0054] Due to IVS, the programmed state immediately after writing cannot reflect the target threshold voltage V_{th} of the memory cell 340 in real applications. Applying the fake high threshold voltage V_{th} can cause high bit-error-rate in the memory. Therefore, it is necessary to de-trap and remove fast charges prior to read operation such that the V_{th} distribution profile of each programmed state can be more accurately determined.
- [0055] Fig. 5 illustrates a timing diagram of a read-verification operation 500 with a prepare voltage (pre-pulse) applied on a selected word line, according to some embodiments of the present disclosure. The read-verification operation 500 can reduce read disturb for unselected memory strings in a 3D NAND memory. Read disturb can occur when the threshold voltage V_{th} (*i.e.*, the programmed state) of an unselected memory cell is changed or disturbed during read or read-verification of a selected memory cell. In some embodiments, the read-verification operation 500 includes two steps, *i.e.*, a read-prepare step and a sensing step, having duration of $t_{prepare}$ and $t_{sensing}$, respectively. The timing diagram of a selected top select gate (Sel_TSG), unselected top select gates (Unsel_TSG), a selected word line (Sel_WL), unselected word lines (Unsel_WL) and the lower select gate (LSG) are shown in Fig. 5.

[0056] The read-verification operation 500 starts with the read-prepare step. The TSG 334 and the LSG 332 of a selected memory string, for example TSG 334-3 and LSG 332-3 of a selected memory string 212-3 in Fig. 4(b), can be applied with a top select gate voltage V_{tsg} and a lower select gate voltage V_{lsg} . A corresponding top select transistor 334-T and a lower select transistor 332-T of the selected memory string 212-3 can be switched on. The top and lower select gate voltages V_{tsg} and V_{lsg} can be in a range between 4V to 7V. Accordingly, a current path through the stacked memory cells 340 can be established for the selected memory string 212-3. For example, the current flowing through the selected memory string 212-3 can be detected from the bit line 341-3 and the array common source 446 that are electrically connected with the selected memory string 212-3.

[0057] For the read-verification operation 500, the TSG of unselected memory strings (Unsel-TSG), for example TSG 334-1 of memory string 212-1 in Fig. 4(b), can be applied with a first off voltage (V_{off}), for example 0V, to switch off a corresponding top select transistor 334-T. Current path between the unselected memory strings 212-1 and bit lines 341-1 can be disconnected. Therefore, the channel of selected memory string 212-3 and unselected memory strings 212-1 can be electrically isolated.

[0058] It is noted that there is a delay for the voltages to ramp up during the read-prepare step. This delay can be caused by parasitic capacitors and resistors, and is well-known for a person skilled in the art. Although a memory string is selected and used as an example to describe read-verification operation herein, it is noted that a plurality of memory strings, for example, a memory finger can be selected and operated in a similar way.

[0059] Referring again to Figs. 4(a)-(b) and 5, to verify a target memory cell 340-3 in the selected memory string 212-3, a selected word line (*e.g.*, Sel_WL in Fig. 4(b)) can be applied with a prepare voltage $V_{prepare}$ (also referred to as pre-pulse), while other word lines not selected (*e.g.*, Unsel_WL in Fig. 4(b)) can be applied with a pass voltage V_{pass} . The selected word line are electrically connected to the control gate 333 of the target memory cell 340-3. The prepare voltage $V_{prepare}$ can be in a range between 4V to 7V, and the pass voltage V_{pass} can be in a range between 5V to 9V. The pass voltage V_{pass} can be higher than the highest threshold voltage of the programmed states such that the memory cells on the selected memory string 212-3 can be fully switched on. When the prepare voltage $V_{prepare}$ is applied on the selected word line Sel_WL, the target memory cell 340-3 can also be switched on.

Therefore, at time t_1 , the top and lower select transistors 334-T and 332-T, and all memory cells 340 of the selected memory string 212-3 are switched on. Current flows between the bit line 341-3 and the array common source 446 via the channel layer of the selected memory string 212-3. As current flowing through the channel layer 338 forming a conductive path, de-trapped fast charges 428-2 from the storage layer 424 can be removed through the conductive path. However, fast charge loss can be a slow process, which is shown in the timing diagram of the selected word line (Sel_WL) in Fig. 5.

[0060] In some embodiments, fast charges 428-2 can also be removed by thermal annealing or by implementing soft erase with a low negative voltage on the control gate. However, the read-prepare step generally can take a long time and thus impact the efficiency of the read-verification operation. Therefore, a need exists for a read-verification operation to provide accelerated fast charge loss and shorten read-prepare step.

[0061] In some embodiments, the read-prepare step can reduce read disturb for the unselected memory strings, for example, memory strings 212-1 and 212-2 in Fig. 4(b). As described above, the unselected top select gates (Unsel_TSG) for unselected memory strings (e.g., TSG 334-1 of memory string 212-1) can be applied with the first off voltage (V_{off}), e.g., 0V, to switch off the corresponding top select transistors 334-T and disconnect from the bit lines (e.g., bit line 341-1) as depicted in Fig. 4(b). In some embodiments, the lower select gates (LSG) of the unselected memory strings (e.g., LSG 332-1) are applied with the lower select gate voltage V_{lsg} such that the lower select transistors 332-T are switched on. By applying the prepare voltage V_{prepare} on the selected word line (Sel_WL), corresponding memory cells (e.g., memory cells 340-1, 340-2, 340-3, etc.) can be switched on if the prepare voltage V_{prepare} is selected to be higher than the threshold voltages of the programmed states of the memory cells. In this example, the channel of the memory cells of the unselected memory strings (e.g., memory cells 340-1) can be electrically connected to the array common source 446 to maintain at a predetermined potential, e.g., ground.

[0062] In an example that the prepare voltage V_{prepare} is not applied on the selected word line (Sel_WL), the memory cells corresponding to the selected word line (e.g., the memory cell 340-1 of memory string 212-1) may not be fully switched on (e.g., a voltage applied on the selected word line is lower than the threshold voltage V_{th} of the memory cell 340-1). Upper memory cells, i.e., memory cells located between the bit line (e.g., bit line 341-1) and the

selected word line (Sel_WL) of the unselected memory string (e.g., memory string 212-1), can have floating channels, where the channel layer is not electrically connected to the bit lines 341 or the common array source 446. Channel potential of the upper memory cells of the unselected memory string (e.g., memory string 212-1) can vary randomly. Memory cells with floating channel can suffer charge loss due to an unknown electrical field between the control gate 333 and the channel layer 338 (see FIG. 4(a)). The trapped charges 428 and thereby the threshold voltages V_{th} (i.e., programmed states) of the memory cells can be changed or disturbed, where the change can be significant with the increased number of reading operation. By introducing the read_prepare step prior to the sensing step, as described previously, read disturb on the unselected memory strings can be reduced.

[0063] After the read_prepare step, the voltage bias on the selected word line (Sel_WL) can be reduced from the prepare voltage $V_{prepare}$ to a read voltage V_{read} to sense (i.e., read or measure) the threshold voltage V_{th} of the target memory cell. The read voltage V_{read} can be in a range between 0V to 2V. For the target memory cell programmed with threshold voltage V_{th} lower than the read voltage V_{read} , the target memory cell can be switch on and form a conductive path in the channel layer 338. If the threshold voltage V_{th} is higher than the read voltage V_{read} , the channel of the target memory cell is switched off. The programmed state of the target memory cell can be determined accordingly. It is noted that the transition period from the prepare voltage $V_{prepare}$ to the read voltage V_{read} is a slow process due to parasitic capacitance and resistance as well as slow de-trapping process of fast trap loss. The sensing step can start after the Sel_WL reach the read voltage V_{read} , which increases the overall duration $t_{prepare}$ of read-prepare step.

[0064] Fig. 6 illustrates a read-verification operation 600 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 600 also includes the read-prepare step and the sensing step. During the read-prepare step of the read-verification operation 600, the Sel_TSG and the LSG can be applied with the top and lower select gate voltages V_{tsg} and V_{lsg} , respectively, to switch on the top and lower select transistors 334-T and 332-T (in Fig. 4(b)), similar to those used in the read-verification operation 500 in Fig. 5. However, unlike the read-verification operation 500, the Unsel_TSG of the read-verification operation 600 is applied with the prepare voltage $V_{prepare}$ during the read-prepare step. Accordingly, the

selected and unselected memory strings can all be electrically accessed from the bit line 341 and the array common source 446.

[0065] In some embodiments, during the read-prepare step of the read-verification operation 600, the selected memory cell can be switched off by applying a second off voltage, *e.g.*, 0V on the selected WL (*i.e.*, Sel_WL). The unselected memory cells (*i.e.*, Unsel_WL) can be switched on with the pass voltage V_{pass} after a delay period t_{delay1} . During the delay period t_{delay1} , all select transistors controlled by Sel_TSG, Unsel_TSG and LSG are turned on with applied voltages V_{tsg} , V_{prepare} and V_{lsg} and thus the channel of the memory string 212 can be electrically connected to the bit line 341 and the array common source 446 (shown in Fig. 4(b)), and can be maintained at a potential adjustable by a voltage of the bit line 341. When the Unsel_WL is applied with the pass voltage V_{pass} , all the unselected memory cells of the selected memory string are switched on. Therefore, the channel of the selected memory cell can be electrically connected to the bit line 341 through upper memory cells and to the array common source 446 through the lower memory cells. The channel of the selected memory cell can thereby be held at a potential adjustable by the voltage of the bit line 341 and the array common source 446.

[0066] In some embodiments, the delay period t_{delay1} is implemented such that the channel of the memory string 212 is not electrically isolated from the bit line 341 or the array common source 446 before Unsel_WL can be ramped up from 0V to the pass voltage V_{pass} . Referring to Fig. 4(b) and Fig. 6, if the Unsel_WL is applied with the pass voltage V_{pass} before the Sel_TSG reach the top select gate voltage V_{tsg} or Unsel_TSG reach the prepare voltage V_{prepare} , the top select transistors are off and upper portion of the channel layer 338 that is located close to the bit line 341 becomes a floating node. More specifically upper memory cells located between the bit line and the selected memory cell can have a floating channel potential. Similarly, if the Unsel_WL is applied with the pass voltage V_{pass} before the LSG ramps up to the lower select gate voltage V_{lsg} to switch on the lower select transistor, lower portion of the channel layer 338 that is located close to the array common source 446 becomes a floating node. More specifically lower memory cells located between the bit line and the selected memory cell can have a floating channel potential. When floating, channel potential of the memory cells can be boosted by the pass voltage V_{pass} of the Unsel_WL through coupled capacitance. The boosted channel potential of the unselected memory cells

can influence the channel potential of the neighboring selected memory cell and influence fast charge removing process. By introducing the delay period t_{delay1} , the aforementioned self-boosting effect or read disturb on the selected or unselected memory cell can be avoided.

[0067] In some embodiments, the read-prepare step also includes a delay period t_{delay2} , a duration between ramping up the pass voltage V_{pass} of Unsel_WL and the read voltage V_{read} of the Sel_WL. During the delay period t_{delay2} , the voltage of Sel_WL is kept at 0V while the voltage of Unsel_WL is raised from 0V to the pass voltage V_{pass} . As discussed previously, the pass voltage V_{pass} is applied on the Unsel_WL after the top and lower select transistors are switched on with applied voltages V_{tsg} , V_{prepare} and V_{lsg} on Sel_TSG, Unsel-TSG and LSG, respectively. As such, the selected memory cell is switched off while unselected memory cells are switched on. Referring back to Fig. 4(a), while the selected memory cell 340-3 is switched off, the neighboring unselected memory cells 340 are switched on. Between the selected memory cell 340-3 with a 0V gate bias and the neighboring unselected memory cells 340 with a gate bias of the pass voltage V_{pass} , an electric field parallel to the channel can be established accordingly. The electric field between the neighboring selected and unselected word line can also extend into the charge storage layer 424, the tunneling layer 426 and the channel layer 338. The electric field can generate an electric force on the fast charges 428-2 captured in the storage layer 424. The electric force can de-trap the fast charges 428-2 from the shallow traps, pull them towards the neighboring unselected memory cells. The fast charges can then be recombined with charges of opposite sign or be removed through the conductive path established in the channel of the unselected memory cells. As a result, fast charges 428-2 in the storage layer 424 of the selected memory cell 340-3 can be removed through electric field from neighboring unselected memory cells.

[0068] Referring again to Fig. 6, the duration of the read-prepare step of the read-verification operation 600 includes the sum of the delay period t_{delay1} and t_{delay2} . Both t_{delay1} and t_{delay2} can be pre-determined values.

[0069] In some embodiments, after the read-prepare step, the read voltage V_{read} is applied on the Sel_WL to start the sensing step and BL pre-charge. The sensing step has a duration of t_{sensing} , which can also be a predetermined value. During the sensing step, a voltage of 0V is applied on the Unsel_TSG, which switches off the unselected top select gates and electrically isolates the channel of selected memory string from the channel of unselected memory

strings. Similar to the read-verification operation 500 (in Fig. 5), the ramping-down process from the prepare voltage V_{prepare} to 0V has a delay time, resulting from parasitic resistance and capacitance of the 3D memory structure. To switch on the memory cells, the prepare voltage V_{prepare} can be set higher than the threshold voltage V_{th} of the memory cell. When the voltage of Unsel_TSG ramping down from the prepare voltage V_{prepare} to below V_{th} , the top select transistors of the unselected memory strings are switched off accordingly. The read-verification operation 600 has a duration t_{prepare2} from the beginning of the read-prepare step to the moment that the Unsel_TSG drops to below V_{th} . In the other words, the duration t_{prepare2} is the minimum time requirement for turning off the Unsel_TSG in the read-verification operation 600. The read-verification operation 600 has a duration t_{prepare1} from the beginning of the read-prepare step to the moment that the Unsel_TSG reaches 0V. For read-verification operation 600, duration of the read-prepare step, *i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$ is less than t_{prepare2} . The sensing step and BL pre-charge start when Unsel_TSG is above V_{th} and the unselected top select transistor is still on. This operation can provide a minimum time used for the read-prepare step, although more power is consumed. The time saved $t_{\text{PROG-save}}$ is a difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$.

[0070] Fig. 7 illustrates a read-verification operation 700 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 700 is similar to the read-verification operation 600, except having a duration of the read-prepare step (*i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$) equals t_{prepare2} , the minimum time requirement for turning off the Unsel_TSG. In the read-verification operation 700, the sensing step and BL pre-charge start when the unselected top select transistors are just turned off. Still, the time saved $t_{\text{PROG-save}}$ can be expressed as the difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$, as shown in Fig. 7. This operation can be sped-up, and thus improved, without consuming more power.

[0071] Fig. 8 illustrates a read-verification operation 800 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 800 is similar to the read-verification operation 600, except having a duration of the read-prepare step (*i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$) more than t_{prepare2} , the minimum time requirement for turning off the Unsel_TSG. In the read-verification operation 800, the sensing step and BL pre-charge start after the unselected top select

transistors are turned off. The time saved $t_{\text{PROG-save}}$ can also be expressed as the difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$, as shown in Fig. 8. This operation can allow more time for removing fast charges.

[0072] As described above, accelerating fast charge loss in a 3D NAND flash memory can be achieved by applying the prepare voltage V_{prepare} on Unsel_TSG, the pass voltage V_{pass} on the Unsel_WL, and 0V on the Sel-WL at the read-prepare step. The threshold voltage V_{th} of the target memory cell, associated with the Sel_WL, can be stabilized before the sensing step such that the verified storage data can be more reliable.

[0073] In addition, the read-verification operation described above can greatly reduce the time required at the read-prepare step. The fast charges can be removed by electric field generated between Sel_WL and neighboring Unsel_TSG. After fast charge removal, the sensing step starts when the voltage on Sel_WL is switched from 0V to the read voltage V_{read} , without the need to wait for the Unsel-TSG to ramp down from the prepare voltage V_{prepare} to 0V. Therefore, the duration of read-prepare step can be shortened, *i.e.*, $t_{\text{delay1}} + t_{\text{delay2}} < t_{\text{prepare1}}$, where $t_{\text{PROG-save}} = t_{\text{prepare1}} - t_{\text{delay1}} - t_{\text{delay2}}$ is the time saved.

[0074] 3D NAND flash memory with multi-level-cells typically uses an algorithm with incremental step pulses to program the memory cells. After every program pulse, a read-verification operation is performed to check the state of the memory cells. When the memory cell reaches the target state (*i.e.*, target threshold voltage), the program will be stopped. In the meantime, the memory cells not programed to the target state are calculated towards failed bit count (FBC), where the FBC can be executed in parallel to the read-verification operation to save the time of the entire programming cycle. As shown in Figs. 6-8, FBC operation can be performed in parallel with the read-prepare step. In some embodiments, duration of the FBC operation can be shorter than the duration of the read-prepare step, and the FBC operation can be incorporated within the read-prepare step starting at any suitable time. The failed memory cells can be programmed again to the target memory state accordingly.

[0075] In summary, the present disclosure provides a method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, where the method includes removing fast charges of the target memory cell at a read-prepare step and measuring a threshold voltage of the target memory cell at a sensing step. Removing the fast charges of the target memory cell includes applying a prepare voltage (V_{prepare}) on an

unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).

[0076] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt, for various applications, such specific embodiments, without undue experimentation, and without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0077] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0078] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0079] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:
 - removing fast charges of the target memory cell at a read-prepare step, comprising:
 - applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string;
 - applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell; and
 - applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL); and
 - measuring a threshold voltage of the target memory cell at a sensing step.
2. The method of claim 1, further comprising:
 - applying a top select gate voltage (V_{tsg}) on a selected top select gate (Sel_TSG) of a selected memory string containing the target memory cell; and
 - applying a lower select gate voltage (V_{lsg}) on a lower select gate (LSG) of the selected memory string containing the target memory cell.
3. The method of claim 2, wherein applying the top select gate voltage (V_{tsg}) comprises electrically connecting the selected memory string to a bit line; and applying the lower select gate voltage (V_{lsg}) comprises electrically connecting the selected memory string to an array common source.
4. The method of claim 2, wherein applying the top select gate voltage (V_{tsg}) comprises applying a voltage between 4V to 7V.
5. The method of claim 2, wherein applying the lower select gate voltage (V_{lsg}) comprises applying a voltage between 4V to 7V.
6. The method of claim 2, wherein applying the pass voltage (V_{pass}) comprises applying the pass voltage with a delay period after the selected top select gate (Sel_TSG) and the lower select gate (LSG) are at the top select gate voltage (V_{tsg}) and the lower select gate voltage (V_{lsg}), respectively.

7. The method of claim 1, wherein measuring the threshold voltage comprises applying a read voltage (V_{read}) on the selected word line (Sel_WL).
8. The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying a voltage between 0 to 2V.
9. The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying a second off voltage on the unselected word line (Unsel_WL).
10. The method of claim 9, wherein applying the second off voltage on the unselected word line (Unsel_WL) comprises applying a 0V.
11. The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is higher than a threshold voltage of an unselected memory cell.
12. The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) equals to a threshold voltage of an unselected memory cell.
13. The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is lower than a threshold voltage of an unselected memory cell.
14. The method of claim 1, wherein applying the prepare voltage (V_{prepare}) comprises applying a voltage between 4V to 7V.
15. The method of claim 1, wherein applying the first off voltage (V_{off}) comprises applying a 0V.
16. The method of claim 1, wherein applying the pass voltage (V_{pass}) comprises applying a voltage between 5V to 9V.
17. The method of claim 1, wherein removing the fast charges comprises removing the fast charges from a storage layer of the target memory cell of a selected memory string, wherein the selected memory string comprises:

a channel hole penetrating vertically through a film stack of alternating conductive and dielectric layers;

a core filling film in a center of the channel hole;

a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, the storage layer and a tunneling layer; and

a channel layer sandwiched between the memory film and the core filling film.

18. The method of claim 17, wherein removing the fast charges comprises removing electrical charges from shallow traps in the storage layer of the target memory cell.
19. The method of claim 17, wherein removing the fast charges comprises removing the fast charges from the target memory cell to a neighboring unselected memory cell.
20. The method of claim 1, wherein conducting the read-verification operation comprises conducting the read-prepare step and conducting a failed bit count in parallel.

ABSTRACT

A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device includes removing fast charges of the target memory cell at a read-prepare step and measuring a threshold voltage of the target memory cell at a sensing step. Removing the fast charges of the target memory cell includes applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).

100

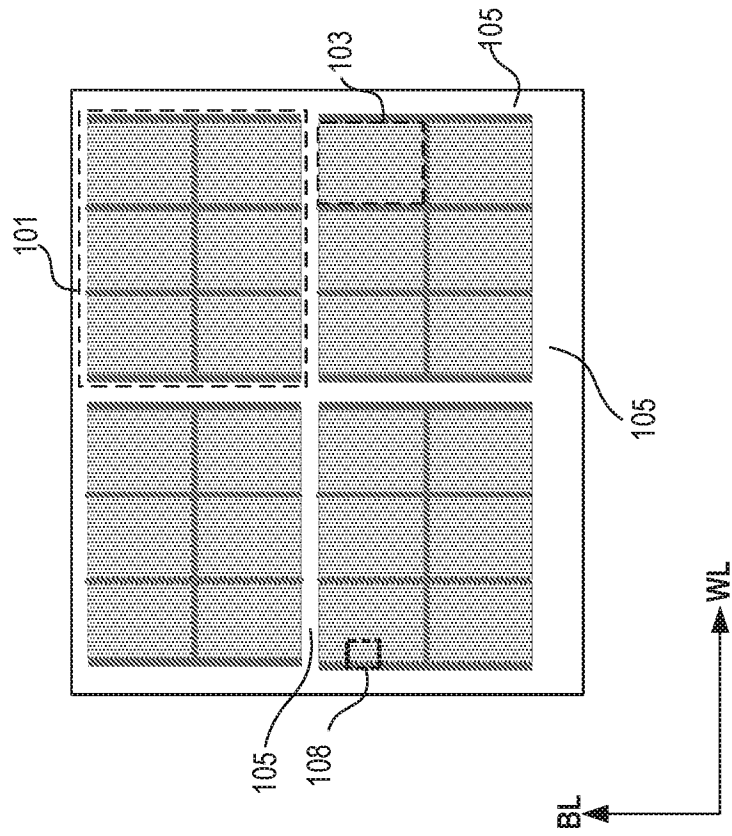
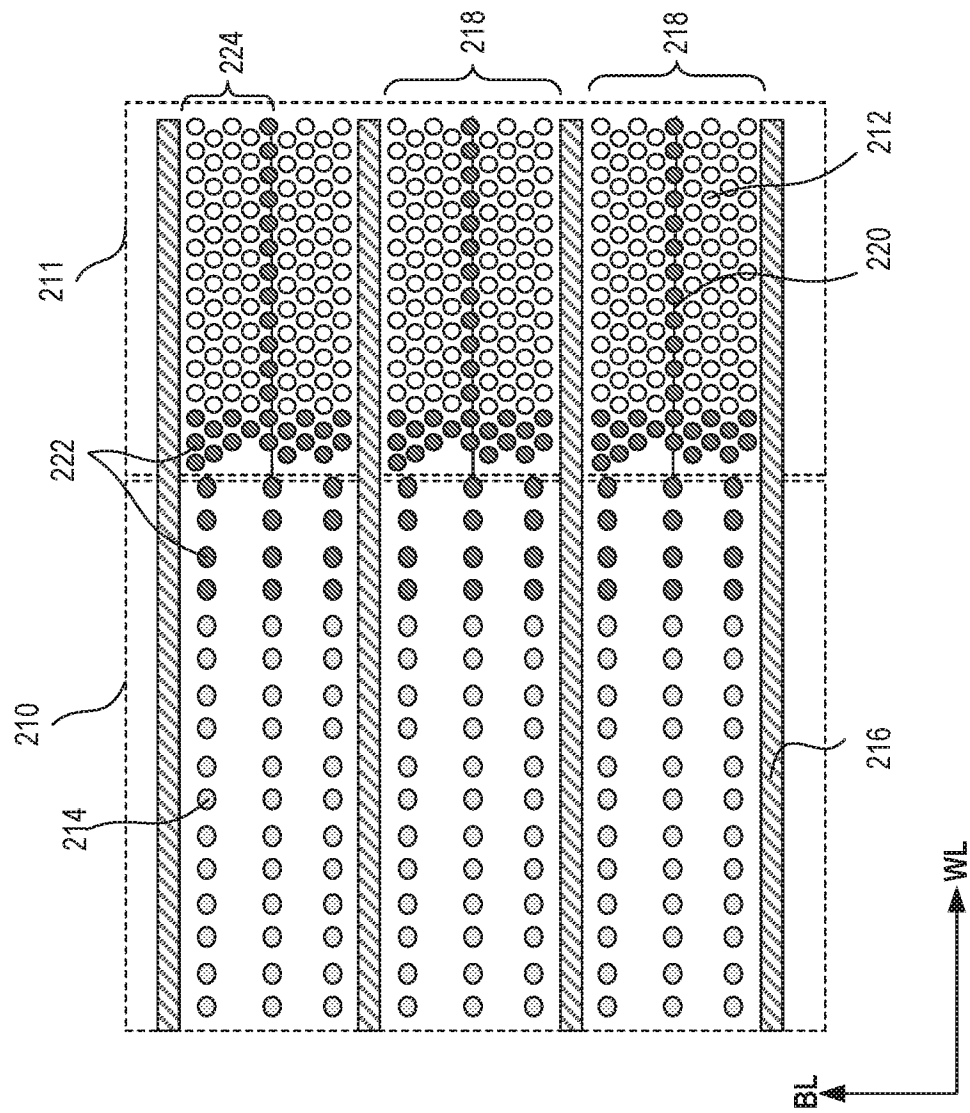
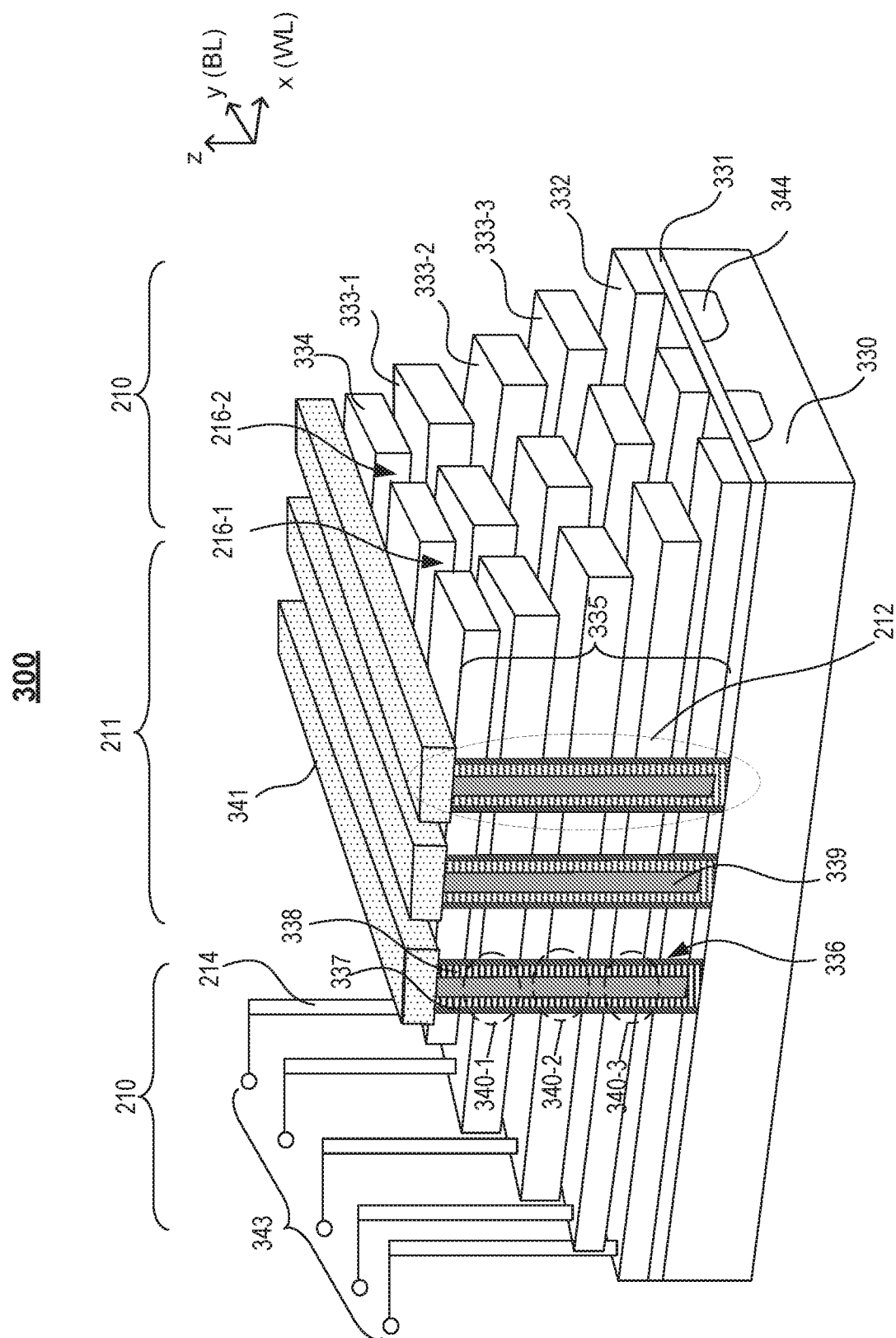


Fig. 1



2
0
1
1



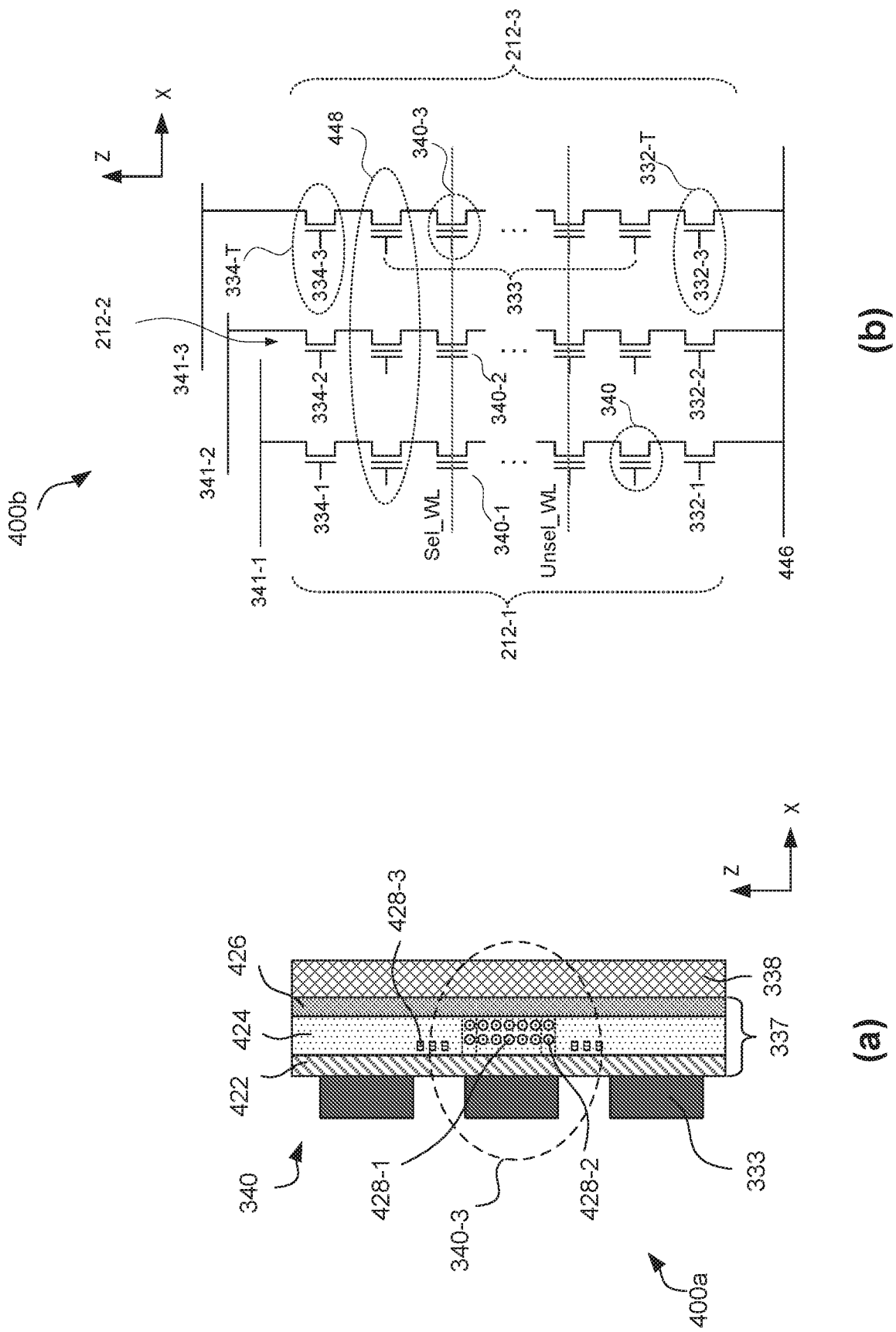


Fig. 4

Read-Verification Operation

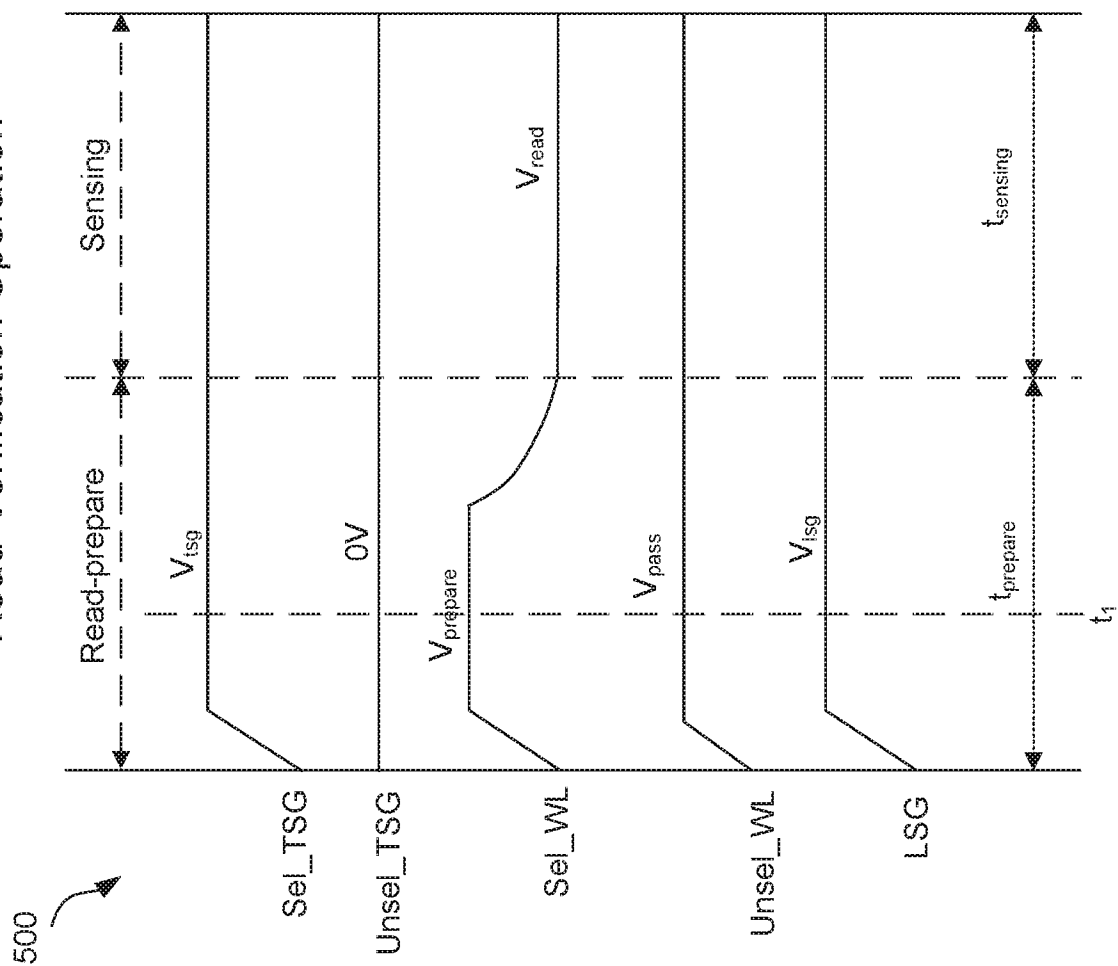


Fig. 5

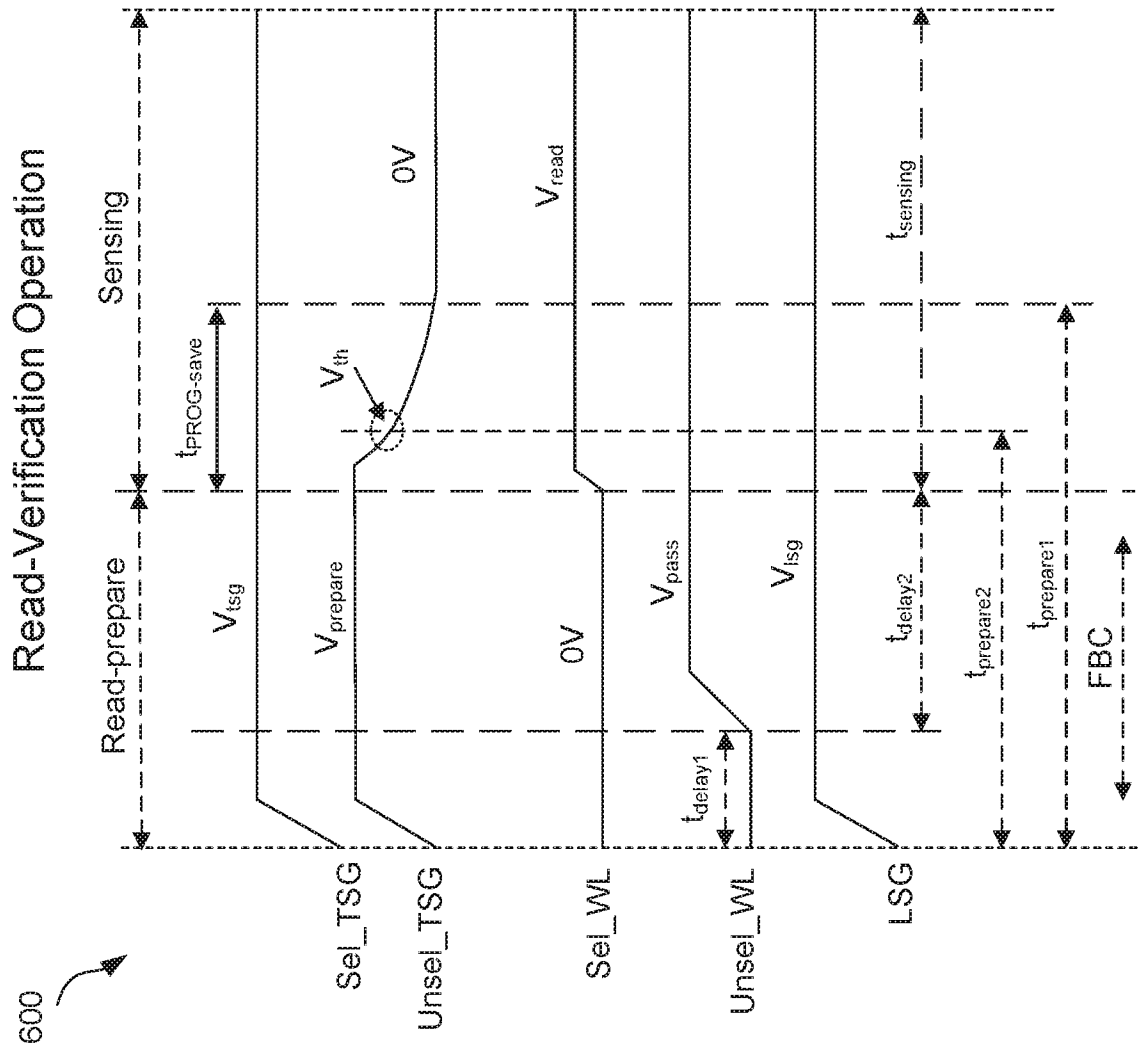


Fig. 6

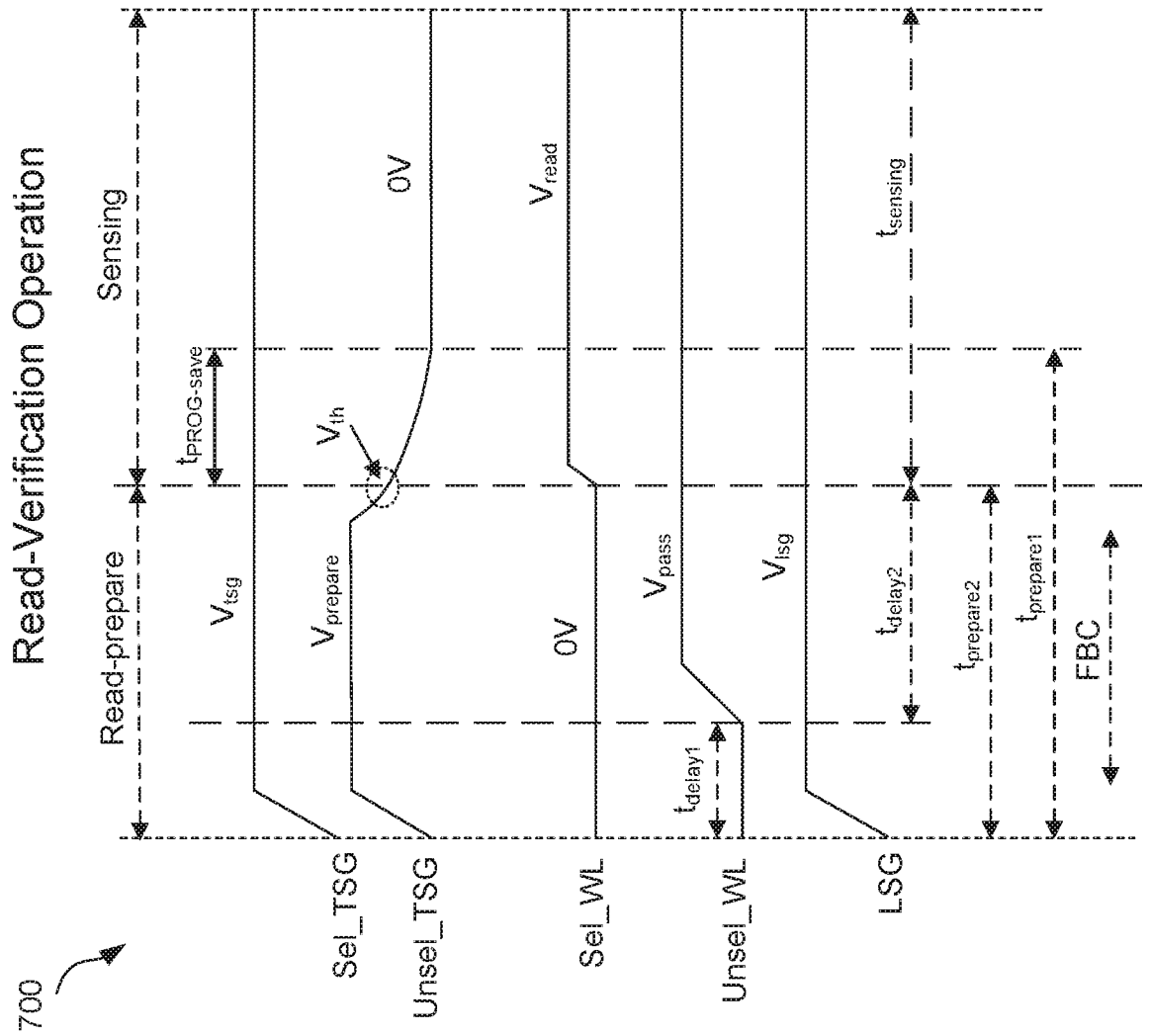


Fig. 7

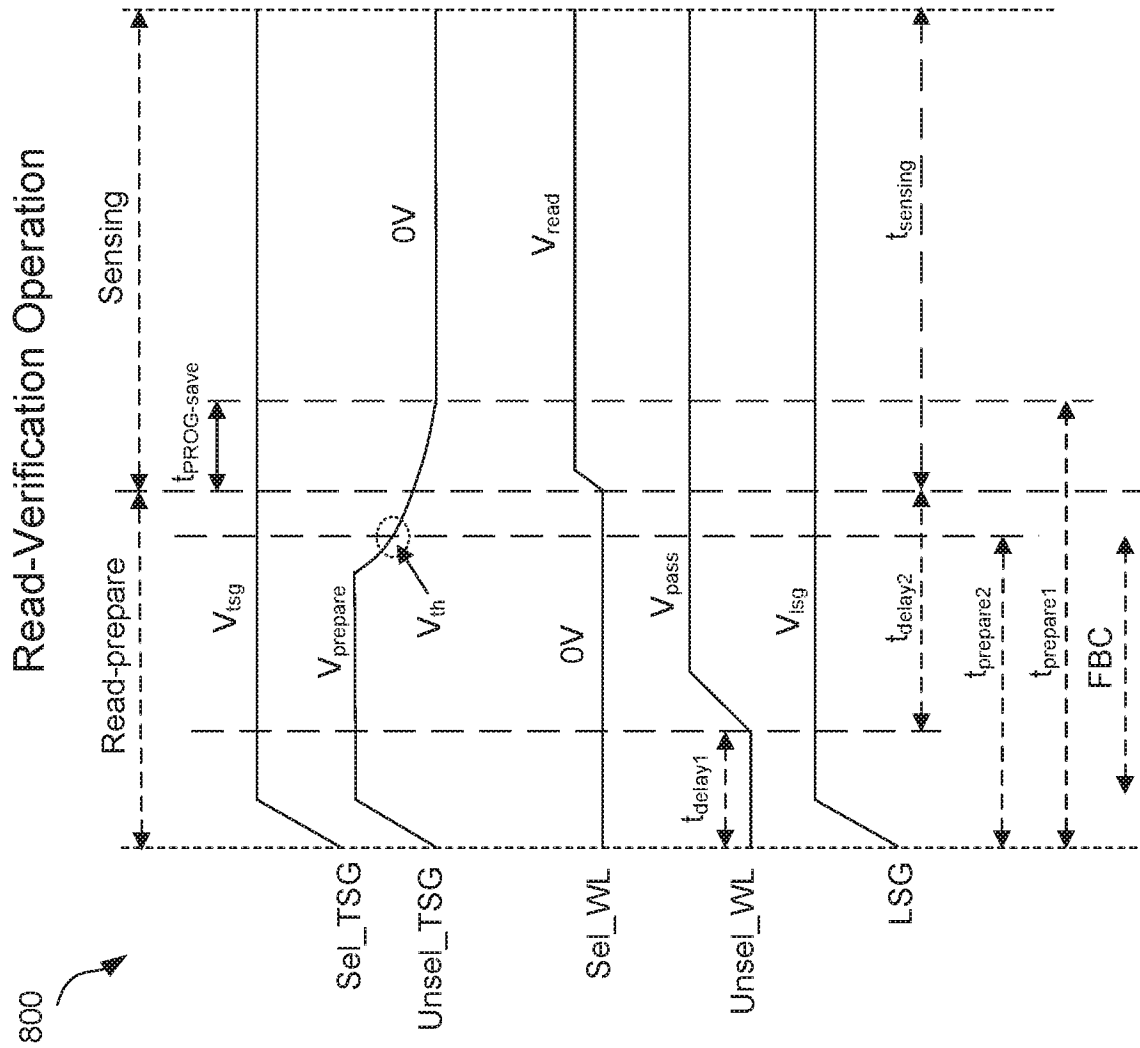


Fig. 8

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		
First Named Inventor/Applicant Name:		Zilong CHEN		
Filer:		Donald J. Featherstone/Patrick Duffy		
Attorney Docket Number:		4123.0850001		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1880

Electronic Acknowledgement Receipt

EFS ID:	38160367
Application Number:	16729838
International Application Number:	
Confirmation Number:	5773
Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Donald J. Featherstone/Patrick Duffy
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0850001
Receipt Date:	30-DEC-2019
Filing Date:	
Time Stamp:	13:10:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1880
RAM confirmation Number	E2019BTD10168637
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2019-12-30-SKGF-Cover-Letter-4123-0850001.pdf	269706	no	2
			d473c98e9b5572f79ed93d849416cacf31a9cee3		
Warnings:					
Information:					
2	Transmittal of New Application	Utility-Transmittal-4123-0850001.PDF	372988	no	2
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3	Application Data Sheet	ADS-4123-0850001.PDF	1256132	no	8
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Information:					
4	Authorization for Extension of Time all replies	2019-12-30-EOT-Authorization-4123-0850001.pdf	108597	no	1
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Warnings:					
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5	Power of Attorney	-POA-82A-4123-0850001.PDF	258462	no	1
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Warnings:					
Information:					
6	Power of Attorney	POA-82B-4123-0850001.PDF	547697	no	1
			f3a73d81f578f1a9b6360a1557d5e22f7a79e02e		
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					

Information:					
7		2019-12-30- Specification-4123-0850001. pdf	182957 6e1ca60aa163289d423e6bc6db022a9ed0c76d8f	yes	24
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	20	
	Claims		21	23	
	Abstract		24	24	
Warnings:					
Information:					
8	Drawings-only black and white line drawings	2019-12-30- Drawings-4123-0850001.pdf	156564 a5170a77a9d44f60bb0af23a8defd79b766e3314	no	8
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	36715 ffec95a97716d39ddbcb6e5998a66a6636ab7fa55	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			3189818		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

December 30, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Patent Application under 37 C.F.R. § 1.53(b)
(*Continuation of Appl. No. PCT/CN2019/112728; Filed October 23, 2019*)
Appl. No. To Be Assigned; Filed: Herewith
For: **METHOD FOR READING THREE-DIMENSIONAL FLASH
MEMORY**
Inventors: CHEN *et al.*
Our Ref: 4123.0850001

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S.
Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/AIA/15);
2. Payment made electronically for **\$1,880.00** to cover:
 - \$1,720.00** - Patent Application fees (including basic filing, search, and examination fees);
 - \$160.00** - Surcharge for late filing of Oath or Declaration;
3. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);
4. U.S. Utility Patent Application entitled:
METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
and naming as inventors:
Zilong CHEN and Xiang FU
the application consisting of:
 - a. An Application Data Sheet (37 C.F.R. § 1.76);

- b. A specification containing:
 - i. **20** pages of description prior to the claims;
 - ii. **3** pages of claims (**20** claims);
 - iii. a one (**1**) page abstract;
 - c. **8** sheets of drawings: (Figures **1-3, 4A, 4B, 5-8**);
5. The Transmittal for Power of Attorney form (PTO/AIA/82A) and an executed Power of Attorney by Applicant (PTO/AIA/82B).

The above-listed documents are filed electronically.

Correspondence should be sent to Customer Number 26111.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration.

Fee payment is provided via electronic filing. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/d-o
Enclosures

14339195.1



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/729,838	12/30/2019	Zilong CHEN	4123.0850001

CONFIRMATION NO. 5773

FORMALITIES LETTER



OC000000114131337

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Date Mailed: 01/24/2020

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given **TWO MONTHS** from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
 - More than one figure is present and one or more figure appears to be unnumbered or misnumbered in comparison to the brief description of the figures. See Figure(s) 4. The figures must be labeled "Fig." with a consecutive Arabic numeral (1, 2, etc.) or an Arabic numeral and capital letter in the English alphabet (A, B, etc.) and correspond with a brief description having the same figure number. See 37 CFR 1.84(u)(1).
 - (1) To correct the figure numbering, replacement figures must be submitted.
 - (2) To add a brief description of an unnumbered figure, or correct the reference in the specification to the figures, a proper substitute specification in compliance with 37 CFR 1.121(b)(3) and 1.125, providing a brief description of each drawing figure presented, added or amended to correspond to the corrected numbering of the figures, must be submitted. See also 37 CFR 1.77(b)(9).

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
Zilong CHEN
Xiang FU

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
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Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/llvuong/

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/729,838				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760			
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *			OR	x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 460 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/729,838	12/30/2019	2827	1880	4123.0850001	20	1

CONFIRMATION NO. 5773

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT



0000000114131336

Date Mailed: 01/24/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Zilong CHEN, Wuhan, CHINA;
Xiang FU, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2019/112728 10/23/2019

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/22/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/729,838**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No
Title

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

SCORE Placeholder Sheet for IFW Content

Application Number: 16729838

Document Date: 01/31/2020

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

At the time of document entry (noted above):

- USPTO employees may access SCORE content via DAV or via the SCORE web page.
- External customers may access SCORE content via PAIR using the Supplemental Content tab.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: CHEN *et al.*

Applicant: Yangtze Memory Technologies Co., Ltd.

Application No.: 16/729,838

Filing Date: December 30, 2019

Confirmation No.: 5773

Art Unit: 2827

Examiner: To Be Assigned

Atty. Docket: 4123.0850001

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

**Reply to Notice to File Corrected Application Papers and Preliminary
Amendment Under 37 C.F.R. § 1.115**

Mail Stop Missing Parts

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In response to the Notice to File Corrected Application Papers dated January 24, 2020, and in advance of prosecution, Applicant submits the following amendments and remarks.

Amendments to the Specification begin on page 2 of this paper. Marked-up and clean versions of a substitute specification are included.

Amendments to the Drawings begin on page 3 of this paper. A replacement sheet is included.

Remarks begin on page 4 of this paper.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Specification

Please replace the originally filed specification with the attached substitute specification. In compliance with 37 C.F.R. § 1.125, a marked up version and a clean version of the substitute specification are included. The substitute specification includes no new matter.

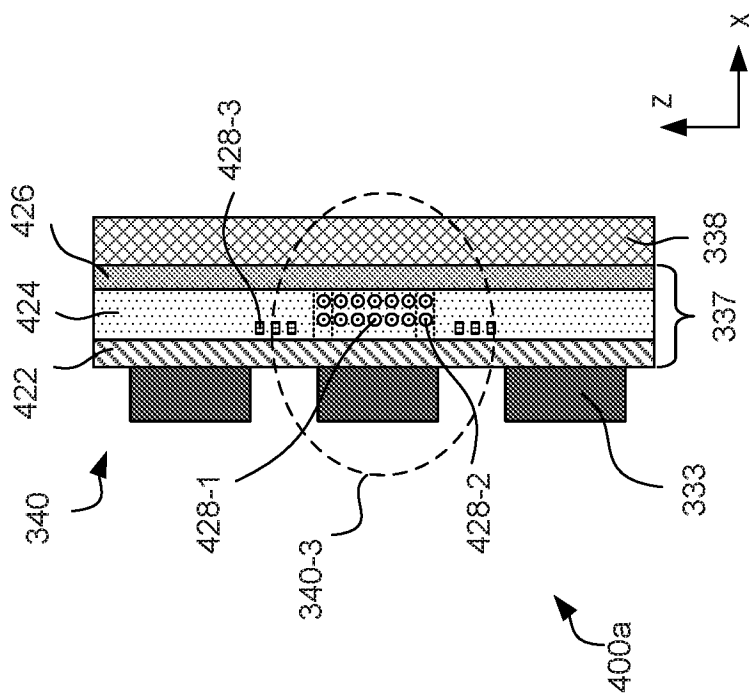


Fig. 4A

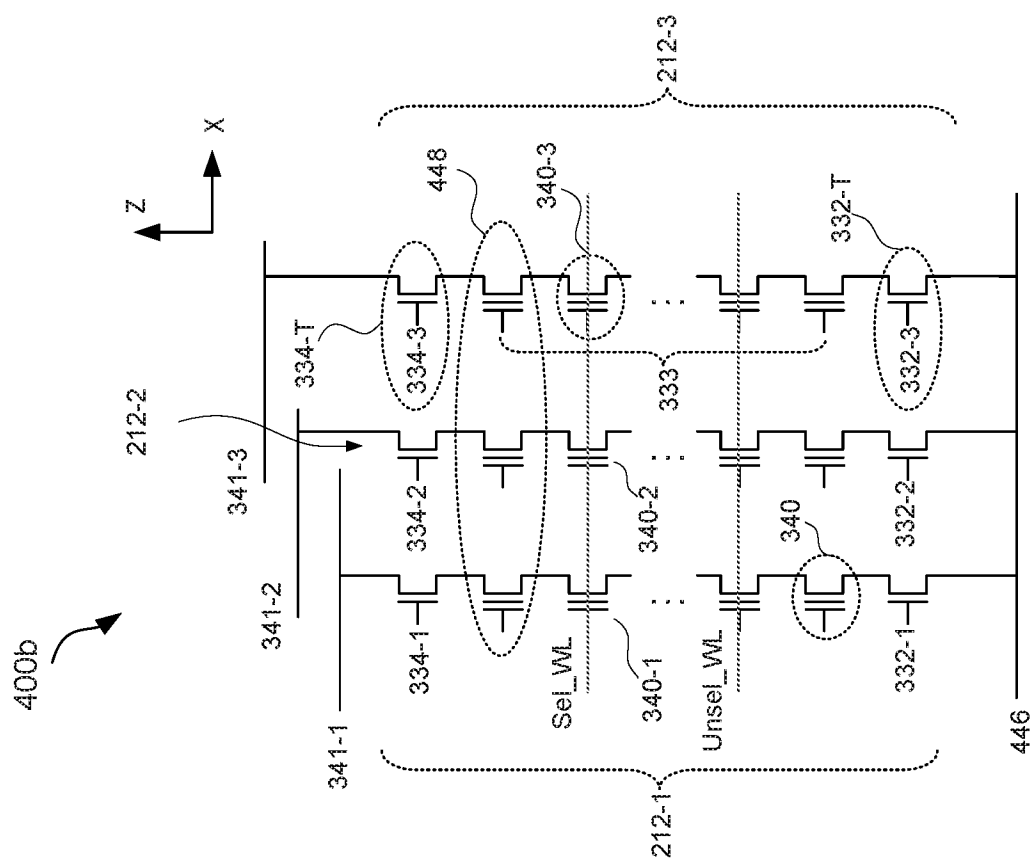


Fig. 4B



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/729,838	12/30/2019	Zilong CHEN	4123.0850001

CONFIRMATION NO. 5773

FORMALITIES LETTER

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



0000000114131337

Date Mailed: 01/24/2020

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given **TWO MONTHS** from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
 - More than one figure is present and one or more figure appears to be unnumbered or misnumbered in comparison to the brief description of the figures. See Figure(s) 4. The figures must be labeled "Fig." with a consecutive Arabic numeral (1, 2, etc.) or an Arabic numeral and capital letter in the English alphabet (A, B, etc.) and correspond with a brief description having the same figure number. See 37 CFR 1.84(u)(1).
 - (1) To correct the figure numbering, replacement figures must be submitted.
 - (2) To add a brief description of an unnumbered figure, or correct the reference in the specification to the figures, a proper substitute specification in compliance with 37 CFR 1.121(b)(3) and 1.125, providing a brief description of each drawing figure presented, added or amended to correspond to the corrected numbering of the figures, must be submitted. See also 37 CFR 1.77(b)(9).

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
Zilong CHEN
Xiang FU

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

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Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/llvuong/

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS AND INCORPORATION BY REFERENCE

[0001] This application claims priority to PCT/CN2019/112728 filed on October 23, 2019, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a method for reading a three-dimensional (3D) memory.

BACKGROUND

[0003] As memory devices are shrinking to smaller die size to reduce manufacturing cost and increase storage density, scaling of planar memory cells faces challenges due to process technology limitations and reliability issues. A three-dimensional (3D) memory architecture can address the density and performance limitation in planar memory cells.

[0004] In a 3D NAND flash memory, memory cells can be programmed for data storage based on charge-trapping technology. The storage information of a memory cell depends on the amount of charge trapped in a storage layer. However, fast charges, *i.e.*, charges trapped in shallow traps, can be easily lost. Therefore, the threshold voltage determining the stored information can be different between write and read operations. Accordingly, a read-prepare step is included in a read-verification operation after programming to remove the fast charges and verify the threshold voltage of the memory cell. Fast charge loss depending on the intrinsic de-trapping process in the storage layer can be long, making the read-verification operation inefficient. Therefore, a need exists for a method to accelerate fast charge loss so that threshold voltage or storage information of the memory cell can be verified or read more accurately and efficiently.

BRIEF SUMMARY

- [0005]** Embodiments of a method for conducting read-verification operation of a memory cell in a three-dimensional (3D) memory device is described in the present disclosure.
- [0006]** One aspect of the present disclosure provides a method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device. The method includes removing fast charges of the target memory cell at a read-prepare step, which includes applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL). The method also includes measuring a threshold voltage of the target memory cell at a sensing step.
- [0007]** In some embodiments, the method further includes applying a top select gate voltage (V_{tsg}) on a selected top select gate (Sel_TSG) of a selected memory string containing the target memory cell, and applying a lower select gate voltage (V_{lsg}) on a lower select gate (LSG) of the selected memory string containing the target memory cell.
- [0008]** In some embodiments, applying the top select gate voltage (V_{tsg}) includes electrically connecting the selected memory string to a bit line. In some embodiments, applying the lower select gate voltage (V_{lsg}) includes electrically connecting the selected memory string to an array common source.
- [0009]** In some embodiments, applying the top select gate voltage (V_{tsg}) includes applying a voltage between 4V to 7V. In some embodiments, applying the lower select gate voltage (V_{lsg}) includes applying a voltage between 4V to 7V.
- [0010]** In some embodiments, applying the pass voltage (V_{pass}) includes applying the pass voltage with a delay period after the selected top select gate (Sel_TSG) and the lower select gate (LSG) are at the top select gate voltage (V_{tsg}) and the lower select gate voltage (V_{lsg}), respectively.
- [0011]** In some embodiments, measuring the threshold voltage includes applying a read voltage (V_{read}) on the selected word line (Sel_WL). In some embodiments, applying the read voltage (V_{read}) includes applying a voltage between 0 to 2V. In some embodiments, applying the read voltage (V_{read}) includes applying a second off voltage on the unselected word line

(Unsel_WL). In some embodiments, applying the second off voltage on the unselected word line (Unsel_WL) includes applying a 0V.

[0012] In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is higher than a threshold voltage of an unselected memory cell. In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) equals to a threshold voltage of an unselected memory cell. In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is lower than a threshold voltage of an unselected memory cell.

[0013] In some embodiments, applying the prepare voltage (V_{prepare}) includes applying a voltage between 4V to 7V. In some embodiments, applying the first off voltage (V_{off}) includes applying a 0V. In some embodiments, applying the pass voltage (V_{pass}) includes applying a voltage between 5V to 9V.

In some embodiments, removing the fast charges includes removing the fast charges from a storage layer of the target memory cell of a selected memory string, wherein the selected memory string includes a channel hole penetrating vertically through a film stack of alternating conductive and dielectric layers, a core filling film in a center of the channel hole, and a memory film covering a sidewall of the channel hole. The selected memory string also includes a channel layer sandwiched between the memory film and the core filling film. In some embodiments, the memory film includes a barrier layer, the storage layer and a tunneling layer.

[0014] In some embodiments, removing the fast charges includes removing electrical charges from shallow traps in the storage layer of the target memory cell.

[0015] In some embodiments, removing the fast charges includes removing the fast charges from the target memory cell to a neighboring unselected memory cell.

[0016] In some embodiments, conducting the read-verification operation comprises conducting the read-prepare step and conducting a failed bit count in parallel.

[0017] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0018]** The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.
- [0019]** Fig. 1 illustrates a schematic top-down view of an exemplary three-dimensional (3D) memory die, according to some embodiments of the present disclosure.
- [0020]** Fig. 2 illustrates a schematic top-down view of a region of 3D memory die, according to some embodiments of the present disclosure.
- [0021]** Fig. 3 illustrates a perspective view of a portion of an exemplary 3D memory array structure, in accordance with some embodiments of the present disclosure.
- [0022]** ~~Fig. 4(a)~~ Fig. 4A illustrates a cross-sectional view of 3D memory cells, according to some embodiments of the present disclosure.
- [0023]** ~~Fig. 4(b)~~ Fig. 4B illustrates a schematic diagram of a 3D memory array, according to some embodiments of the present disclosure.
- [0024]** Fig. 5 illustrates a timing diagram of a read-verification operation with a prepare voltage (pre-pulse) applied on a selected word line, according to some embodiments of the present disclosure.
- [0025]** Figs. 6-8 illustrate timing diagrams of read-verification operations with accelerated fast charge loss, according to some embodiments of the present disclosure.
- [0026]** The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.
- [0027]** Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0028] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0029] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0030] In general, terminology can be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0031] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something, but also includes the meaning of “on” something with an intermediate feature or a layer there between. Moreover, “above” or “over” not only means

“above” or “over” something, but can also include the meaning it is “above” or “over” something with no intermediate feature or layer there between (i.e., directly on something).

[0032] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, can be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or process step in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0033] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate includes a “top” surface and a “bottom” surface. The top surface of the substrate is typically where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate unless stated otherwise. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0034] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, there above, and/or there below. A layer can include multiple layers. For

example, an interconnect layer can include one or more conductive and contact layers (in which contacts, interconnect lines, and/or vertical interconnect accesses (VIAs) are formed) and one or more dielectric layers.

[0035] In the present disclosure, for ease of description, “tier” is used to refer to elements of substantially the same height along the vertical direction. For example, a word line and the underlying gate dielectric layer can be referred to as “a tier,” a word line and the underlying insulating layer can together be referred to as “a tier,” word lines of substantially the same height can be referred to as “a tier of word lines” or similar, and so on.

[0036] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process step, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0037] In the present disclosure, the term “horizontal/horizontally/lateral/laterally” means nominally parallel to a lateral surface of a substrate, and the term “vertical” or “vertically” means nominally perpendicular to the lateral surface of a substrate.

[0038] As used herein, the term “3D memory” refers to a three-dimensional (3D) semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate.

[0039] Fig. 1 illustrates a top-down view of an exemplary three-dimensional (3D) memory device 100, according to some embodiments of the present disclosure. The 3D memory device 100 can be a memory chip (package), a memory die or any portion of a memory die, and can include one or more memory planes 101, each of which can include a plurality of memory blocks 103. Identical and concurrent operations can take place at each memory plane 101. The memory block 103, which can be megabytes (MB) in size, is the smallest size to carry out erase operations. Shown in Fig. 1, the exemplary 3D memory device 100 includes four memory planes 101 and each memory plane 101 includes six memory blocks

103. Each memory block 103 can include a plurality of memory cells, where each memory cell can be addressed through interconnections such as bit lines and word lines. The bit lines and word lines can be laid out perpendicularly (e.g., in rows and columns, respectively), forming an array of metal lines. The direction of bit lines and word lines are labeled as “BL” and “WL” in Fig. 1. In this disclosure, memory block 103 is also referred to as a “memory array” or “array.” The memory array is the core area in a memory device, performing storage functions.

[0040] The 3D memory device 100 also includes a periphery region 105, an area surrounding memory planes 101. The periphery region 105 contains many digital, analog, and/or mixed-signal circuits to support functions of the memory array, for example, page buffers, row and column decoders and sense amplifiers. Peripheral circuits use active and/or passive semiconductor devices, such as transistors, diodes, capacitors, resistors, etc., as would be apparent to a person of ordinary skill in the art.

[0041] It is noted that, the arrangement of the memory planes 101 in the 3D memory device 100 and the arrangement of the memory blocks 103 in each memory plane 101 illustrated in Fig. 1 are only used as an example, which does not limit the scope of the present disclosure.

[0042] Referring to Fig. 2, an enlarged top-down view of a region 108 in Fig. 1 is illustrated, according to some embodiments of the present disclosure. The region 108 of the 3D memory device 100 can include a staircase region 210 and a channel structure region 211. The channel structure region 211 can include an array of memory strings 212, each including a plurality of stacked memory cells. The staircase region 210 can include a staircase structure and an array of contact structures 214 formed on the staircase structure. In some embodiments, a plurality of slit structures 216, extending in WL direction across the channel structure region 211 and the staircase region 210, can divide a memory block into multiple memory fingers 218. At least some slit structures 216 can function as the common source contact (e.g., array common source) for an array of memory strings 212 in channel structure regions 211. A top select gate cut 220 can be disposed, for example, in the middle of each memory finger 218 to divide a top select gate (TSG) of the memory finger 218 into two portions, and thereby can divide a memory finger into two memory slices 224, where memory cells in a memory slice 224 that share the same word line form a programmable (read/write) memory page. While erase operation of a 3D NAND memory can be carried out

at memory block level, read and write operations can be carried out at memory page level. A memory page can be kilobytes (KB) in size. In some embodiments, region 108 also includes dummy memory strings 222 for process variation control during fabrication and/or for additional mechanical support.

[0043] Fig. 3 illustrates a perspective view of a portion of an exemplary three-dimensional (3D) memory array structure 300, according to some embodiments of the present disclosure. The memory array structure 300 includes a substrate 330, an insulating film 331 over the substrate 330, a tier of lower select gates (LSGs) 332 over the insulating film 331, and a plurality of tiers of control gates 333, also referred to as “word lines (WLs),” stacking on top of the LSGs 332 to form a film stack 335 of alternating conductive and dielectric layers. The dielectric layers adjacent to the tiers of control gates are not shown in Fig. 3 for clarity.

[0044] The control gates of each tier are separated by slit structures 216-1 and 216-2 through the film stack 335. The memory array structure 300 also includes a tier of top select gates (TSGs) 334 over the stack of control gates 333. The stack of TSG 334, control gates 333 and LSG 332 is also referred to as “gate electrodes.” The memory array structure 300 further includes memory strings 212 and doped source line regions 344 in portions of substrate 330 between adjacent LSGs 332. Each memory strings 212 includes a channel hole 336 extending through the insulating film 331 and the film stack 335 of alternating conductive and dielectric layers. Memory strings 212 also includes a memory film 337 on a sidewall of the channel hole 336, a channel layer 338 over the memory film 337, and a core filling film 339 surrounded by the channel layer 338. A memory cell 340 can be formed at the intersection of the control gate 333 and the memory string 212. The memory array structure 300 further includes a plurality of bit lines (BLs) 341 connected with the memory strings 212 over the TSGs 334. The memory array structure 300 also includes a plurality of metal interconnect lines 343 connected with the gate electrodes through a plurality of contact structures 214. The edge of the film stack 335 is configured in a shape of staircase to allow an electrical connection to each tier of the gate electrodes.

[0045] In Fig. 3, for illustrative purposes, three tiers of control gates 333-1, 333-2, and 333-3 are shown together with one tier of TSG 334 and one tier of LSG 332. In this example, each memory string 212 can include three memory cells 340-1, 340-2 and 340-3, corresponding to the control gates 333-1, 333-2 and 333-3, respectively. In some embodiments, the number of

control gates and the number of memory cells can be more than three to increase storage capacity. The memory array structure 300 can also include other structures, for example, TSG cut, common source contact (i.e., array common source) and dummy memory string. These structures are not shown in Fig. 3 for simplicity.

[0046] While floating gate memory cells has been traditionally utilized in flash memories, technology based on charge trapping has demonstrated more scaling ability and higher intrinsic reliability. Three-dimensional NAND using charge trapping technology has been developed for high density storage, where the storage information (*e.g.*, threshold voltage V_{th} of the memory cell) depends on the amount of charge trapped in a storage layer.

[0047] ~~Fig. 4(a)~~ Fig. 4A illustrates a schematic cross-section of a 3D NAND memory 400a, which includes memory cells similar to the memory cell 340 in Fig. 3. The memory cell 340-3 includes a control gate (*e.g.*, the control gate 333), a memory film (*e.g.*, the memory film 337) and a channel layer (*e.g.*, the channel layer 338, also referred to as the channel).

[0048] In a 3D NAND memory, the memory film 337 can be disposed on a sidewall of each channel hole 336 (illustrated in Fig. 3). In some embodiments, the memory film 337 can include a barrier layer 422, a storage layer 424, and a tunneling layer 426. The barrier layer 422 can be used to block the movement of electronic charges 428 between the control gate 333 and the storage layer 424. The barrier layer 422 can include silicon oxide and high dielectric constant (high-k) dielectrics, for example, aluminum oxide. The storage layer 424 can be used to store electronic charges 428 and can include silicon nitride. The storage and/or removal of charges in the storage layer 424 can impact the on/off state and/or a conductance of the channel layer 338. The tunneling layer 426 can be used to control the tunneling of electronic charges 428 (electrons or holes) between the channel layer 338 and the storage layer 424. The tunneling layer 426 can be silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In a 3D NAND memory, the channel layer 338 can be disposed on a sidewall of the memory film 337 in the channel hole 336 (in Fig. 3.) The channel layer 338 can include amorphous silicon, polycrystalline silicon, and/or monocrystalline silicon.

[0049] ~~Fig. 4(b)~~ Fig. 4B shows a schematic circuit diagram of a 3D memory array 400b. As described previously, the 3D memory array 400b includes a plurality of memory strings 212, each memory string 212 having a plurality of stacked memory cells 340. The memory string 212 also includes at least one field effect transistor (*e.g.*, MOSFET) at each end, which is

controlled by the lower select gate (LSG) 332 and the top select gate (TSG) 334, respectively. And the two respective transistors are referred to as lower and top select transistors 332-T and 334-T. The stacked memory cells 340 can be controlled by the control gates 333, where the control gates 333 are connected to word lines (not shown) of the 3D memory array 400b. The drain terminal of the top select transistor 334-T can be connected to the bit lines (*e.g.*, the bit line 341-1, 341-2, 341-3, etc.), and the source terminal of the lower select transistor 332-T can be connected to the doped source line region 344 (*see* Fig. 3), from where an array common source (ACS) 446 can be formed. The array common source 446 can be shared by the memory strings 212 in an entire memory block, and is also referred to as the common source line.

[0050] Referring to ~~Figs. 4(a) and 4(b)~~ Figs. 4A and 4B, in a NAND memory, read and write operations can be performed in a memory page, for example memory page 448, which includes memory cells sharing the same word line. In a NAND memory, each memory cell can be in an erased state or a programmed state. Initially, all memory cells in a block can be reset to the erased state as logic “1” by applying, for example, a negative voltage between the control gates 333 and source terminals of the memory cells (*e.g.*, the array common source 446) such that all the electronic charges 428 in the storage layers 424 of the memory cells can be removed. At the erased state, the threshold voltage V_{th} of the memory cells 340 can be reset to the lowest value, and the corresponding current flowing through the memory cells 340 between the source terminal (*e.g.*, the array common source 446) and the drain terminal (*e.g.*, the bit lines 341) can be at the highest level for a given bias on the word lines.

[0051] During programming (*i.e.*, writing), a high positive voltage pulse (*e.g.*, 12V to 18V) can be applied on the control gate 333 such that electronic charges 428 (*e.g.*, electrons) can be injected into the storage layer 424 of the memory cell 340, where the electronic charges 428-1 and 428-2 can be randomly captured by deep and shallow traps, respectively. After programming, the threshold voltage V_{th} of the memory cell 340 can be raised to a higher value than that of the erased state. At a higher threshold voltage V_{th} , the current flowing through the source and drain terminals of the memory cell can be at a reduced level for a given bias on the word lines. By measuring (*i.e.*, reading) the memory cell current, the threshold voltage V_{th} and thereby the state of the memory cell 340 can be determined accordingly.

- [0052] With multi-level-cell or triple-level-cell technology, each memory cell 340 can have multiple programmed states, *i.e.*, multiple values of threshold voltages V_{th} . After every programming pulse, a read-verification operation can be performed to check the state of the memory cell. As such, each memory cell 340 can store multiple bits, leading to significant increase of storage capacity.
- [0053] For memory cell 340 in a programmed state, electronic charges 428-1 and 428-2 located within the proximity of control gate 333 can affect threshold voltage V_{th} of the memory cell 340. The electronic charges 428-3 located beyond the electric field from control gate 333, and therefore have little impact on the threshold voltage V_{th} of the memory cell. In addition, electronic charges 428-2 captured by shallow traps in the storage layer 424 can be easily de-trapped, and can thereby cause initial threshold-voltage (V_{th}) shift (IVS) during storage period. This process is also referred to as fast charge loss. For programmed state at higher threshold voltage V_{th} , IVS can be larger due to larger amount of electronic charges injected to the storage layer, which results in larger number of electronic charges 428-2 captured by shallow traps (also referred to as fast charges).
- [0054] Due to IVS, the programmed state immediately after writing cannot reflect the target threshold voltage V_{th} of the memory cell 340 in real applications. Applying the fake high threshold voltage V_{th} can cause high bit-error-rate in the memory. Therefore, it is necessary to de-trap and remove fast charges prior to read operation such that the V_{th} distribution profile of each programmed state can be more accurately determined.
- [0055] Fig. 5 illustrates a timing diagram of a read-verification operation 500 with a prepare voltage (pre-pulse) applied on a selected word line, according to some embodiments of the present disclosure. The read-verification operation 500 can reduce read disturb for unselected memory strings in a 3D NAND memory. Read disturb can occur when the threshold voltage V_{th} (*i.e.*, the programmed state) of an unselected memory cell is changed or disturbed during read or read-verification of a selected memory cell. In some embodiments, the read-verification operation 500 includes two steps, *i.e.*, a read-prepare step and a sensing step, having duration of $t_{prepare}$ and $t_{sensing}$, respectively. The timing diagram of a selected top select gate (Sel_TSG), unselected top select gates (Unsel_TSG), a selected word line (Sel_WL), unselected word lines (Unsel_WL) and the lower select gate (LSG) are shown in Fig. 5.

- [0056]** The read-verification operation 500 starts with the read-prepare step. The TSG 334 and the LSG 332 of a selected memory string, for example TSG 334-3 and LSG 332-3 of a selected memory string 212-3 in ~~Fig. 4(a)~~ Fig. 4B, can be applied with a top select gate voltage V_{tsg} and a lower select gate voltage V_{lsg} . A corresponding top select transistor 334-T and a lower select transistor 332-T of the selected memory string 212-3 can be switched on. The top and lower select gate voltages V_{tsg} and V_{lsg} can be in a range between 4V to 7V. Accordingly, a current path through the stacked memory cells 340 can be established for the selected memory string 212-3. For example, the current flowing through the selected memory string 212-3 can be detected from the bit line 341-3 and the array common source 446 that are electrically connected with the selected memory string 212-3.
- [0057]** For the read-verification operation 500, the TSG of unselected memory strings (Unsel-TSG), for example TSG 334-1 of memory string 212-1 in ~~Fig. 4(a)~~ Fig. 4B, can be applied with a first off voltage (V_{off}), for example 0V, to switch off a corresponding top select transistor 334-T. Current path between the unselected memory strings 212-1 and bit lines 341-1 can be disconnected. Therefore, the channel of selected memory string 212-3 and unselected memory strings 212-1 can be electrically isolated.
- [0058]** It is noted that there is a delay for the voltages to ramp up during the read-prepare step. This delay can be caused by parasitic capacitors and resistors, and is well-known for a person skilled in the art. Although a memory string is selected and used as an example to describe read-verification operation herein, it is noted that a plurality of memory strings, for example, a memory finger can be selected and operated in a similar way.
- [0059]** Referring again to ~~Figs. 4(a) (b) and 5~~ Figs. 4A, 4B and 5, to verify a target memory cell 340-3 in the selected memory string 212-3, a selected word line (*e.g.*, Sel_WL in ~~Fig. 4(a)~~ Fig. 4B) can be applied with a prepare voltage V_{prepare} (also referred to as pre-pulse), while other word lines not selected (*e.g.*, Unsel_WL in ~~Fig. 4(a)~~ Fig. 4B) can be applied with a pass voltage V_{pass} . The selected word line are electrically connected to the control gate 333 of the target memory cell 340-3. The prepare voltage V_{prepare} can be in a range between 4V to 7V, and the pass voltage V_{pass} can be in a range between 5V to 9V. The pass voltage V_{pass} can be higher than the highest threshold voltage of the programmed states such that the memory cells on the selected memory string 212-3 can be fully switched on. When the prepare voltage V_{prepare} is applied on the selected word line Sel_WL, the target memory cell 340-3

can also be switched on. Therefore, at time t_1 , the top and lower select transistors 334-T and 332-T, and all memory cells 340 of the selected memory string 212-3 are switched on. Current flows between the bit line 341-3 and the array common source 446 via the channel layer of the selected memory string 212-3. As current flowing through the channel layer 338 forming a conductive path, de-trapped fast charges 428-2 from the storage layer 424 can be removed through the conductive path. However, fast charge loss can be a slow process, which is shown in the timing diagram of the selected word line (Sel_WL) in Fig. 5.

[0060] In some embodiments, fast charges 428-2 can also be removed by thermal annealing or by implementing soft erase with a low negative voltage on the control gate. However, the read-prepare step generally can take a long time and thus impact the efficiency of the read-verification operation. Therefore, a need exists for a read-verification operation to provide accelerated fast charge loss and shorten read-prepare step.

[0061] In some embodiments, the read-prepare step can reduce read disturb for the unselected memory strings, for example, memory strings 212-1 and 212-2 in ~~Fig. 4(b)~~ Fig. 4B. As described above, the unselected top select gates (Unsel_TSG) for unselected memory strings (e.g., TSG 334-1 of memory string 212-1) can be applied with the first off voltage (V_{off}), e.g., 0V, to switch off the corresponding top select transistors 334-T and disconnect from the bit lines (e.g., bit line 341-1) as depicted in ~~Fig. 4(b)~~ Fig. 4B. In some embodiments, the lower select gates (LSG) of the unselected memory strings (e.g., LSG 332-1) are applied with the lower select gate voltage V_{lsg} such that the lower select transistors 332-T are switched on. By applying the prepare voltage V_{prepare} on the selected word line (Sel_WL), corresponding memory cells (e.g., memory cells 340-1, 340-2, 340-3, etc.) can be switched on if the prepare voltage V_{prepare} is selected to be higher than the threshold voltages of the programmed states of the memory cells. In this example, the channel of the memory cells of the unselected memory strings (e.g., memory cells 340-1) can be electrically connected to the array common source 446 to maintain at a predetermined potential, e.g., ground.

[0062] In an example that the prepare voltage V_{prepare} is not applied on the selected word line (Sel_WL), the memory cells corresponding to the selected word line (e.g., the memory cell 340-1 of memory string 212-1) may not be fully switched on (e.g., a voltage applied on the selected word line is lower than the threshold voltage V_{th} of the memory cell 340-1). Upper memory cells, i.e., memory cells located between the bit line (e.g., bit line 341-1) and the

selected word line (Sel_WL) of the unselected memory string (*e.g.*, memory string 212-1), can have floating channels, where the channel layer is not electrically connected to the bit lines 341 or the common array source 446. Channel potential of the upper memory cells of the unselected memory string (*e.g.*, memory string 212-1) can vary randomly. Memory cells with floating channel can suffer charge loss due to an unknown electrical field between the control gate 333 and the channel layer 338 (*see* FIG. 4(a) Fig. 4A). The trapped charges 428 and thereby the threshold voltages V_{th} (*i.e.*, programmed states) of the memory cells can be changed or disturbed, where the change can be significant with the increased number of reading operation. By introducing the read_prepare step prior to the sensing step, as described previously, read disturb on the unselected memory strings can be reduced.

[0063] After the read_prepare step, the voltage bias on the selected word line (Sel_WL) can be reduced from the prepare voltage $V_{prepare}$ to a read voltage V_{read} to sense (*i.e.*, read or measure) the threshold voltage V_{th} of the target memory cell. The read voltage V_{read} can be in a range between 0V to 2V. For the target memory cell programmed with threshold voltage V_{th} lower than the read voltage V_{read} , the target memory cell can be switch on and form a conductive path in the channel layer 338. If the threshold voltage V_{th} is higher than the read voltage V_{read} , the channel of the target memory cell is switched off. The programmed state of the target memory cell can be determined accordingly. It is noted that the transition period from the prepare voltage $V_{prepare}$ to the read voltage V_{read} is a slow process due to parasitic capacitance and resistance as well as slow de-trapping process of fast trap loss. The sensing step can start after the Sel_WL reach the read voltage V_{read} , which increases the overall duration $t_{prepare}$ of read-prepare step.

[0064] Fig. 6 illustrates a read-verification operation 600 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 600 also includes the read-prepare step and the sensing step. During the read-prepare step of the read-verification operation 600, the Sel_TSG and the LSG can be applied with the top and lower select gate voltages V_{tsg} and V_{lsg} , respectively, to switch on the top and lower select transistors 334-T and 332-T (in Fig. 4(b) Fig. 4B), similar to those used in the read-verification operation 500 in Fig. 5. However, unlike the read-verification operation 500, the Unsel_TSG of the read-verification operation 600 is applied with the prepare voltage $V_{prepare}$ during the read-prepare step. Accordingly, the

selected and unselected memory strings can all be electrically accessed from the bit line 341 and the array common source 446.

[0065] In some embodiments, during the read-prepare step of the read-verification operation 600, the selected memory cell can be switched off by applying a second off voltage, *e.g.*, 0V on the selected WL (*i.e.*, Sel_WL). The unselected memory cells (*i.e.*, Unsel_WL) can be switched on with the pass voltage V_{pass} after a delay period t_{delay1} . During the delay period t_{delay1} , all select transistors controlled by Sel_TSG, Unsel_TSG and LSG are turned on with applied voltages V_{tsg} , V_{prepare} and V_{lsg} and thus the channel of the memory string 212 can be electrically connected to the bit line 341 and the array common source 446 (shown in ~~Fig. 4(b)~~ Fig. 4B), and can be maintained at a potential adjustable by a voltage of the bit line 341. When the Unsel_WL is applied with the pass voltage V_{pass} , all the unselected memory cells of the selected memory string are switched on. Therefore, the channel of the selected memory cell can be electrically connected to the bit line 341 through upper memory cells and to the array common source 446 through the lower memory cells. The channel of the selected memory cell can thereby be held at a potential adjustable by the voltage of the bit line 341 and the array common source 446.

[0066] In some embodiments, the delay period t_{delay1} is implemented such that the channel of the memory string 212 is not electrically isolated from the bit line 341 or the array common source 446 before Unsel_WL can be ramped up from 0V to the pass voltage V_{pass} . Referring to ~~Fig. 4(b)~~ Fig. 4B and Fig. 6, if the Unsel_WL is applied with the pass voltage V_{pass} before the Sel_TSG reach the top select gate voltage V_{tsg} or Unsel_TSG reach the prepare voltage V_{prepare} , the top select transistors are off and upper portion of the channel layer 338 that is located close to the bit line 341 becomes a floating node. More specifically upper memory cells located between the bit line and the selected memory cell can have a floating channel potential. Similarly, if the Unsel_WL is applied with the pass voltage V_{pass} before the LSG ramps up to the lower select gate voltage V_{lsg} to switch on the lower select transistor, lower portion of the channel layer 338 that is located close to the array common source 446 becomes a floating node. More specifically lower memory cells located between the bit line and the selected memory cell can have a floating channel potential. When floating, channel potential of the memory cells can be boosted by the pass voltage V_{pass} of the Unsel_WL through coupled capacitance. The boosted channel potential of the unselected memory cells

can influence the channel potential of the neighboring selected memory cell and influence fast charge removing process. By introducing the delay period t_{delay1} , the aforementioned self-boosting effect or read disturb on the selected or unselected memory cell can be avoided.

[0067] In some embodiments, the read-prepare step also includes a delay period t_{delay2} , a duration between ramping up the pass voltage V_{pass} of Unsel_WL and the read voltage V_{read} of the Sel_WL. During the delay period t_{delay2} , the voltage of Sel_WL is kept at 0V while the voltage of Unsel_WL is raised from 0V to the pass voltage V_{pass} . As discussed previously, the pass voltage V_{pass} is applied on the Unsel_WL after the top and lower select transistors are switched on with applied voltages V_{tsg} , V_{prepare} and V_{lsg} on Sel_TSG, Unsel-TSG and LSG, respectively. As such, the selected memory cell is switched off while unselected memory cells are switched on. Referring back to ~~Fig. 4(a)~~ Fig. 4A, while the selected memory cell 340-3 is switched off, the neighboring unselected memory cells 340 are switched on. Between the selected memory cell 340-3 with a 0V gate bias and the neighboring unselected memory cells 340 with a gate bias of the pass voltage V_{pass} , an electric field parallel to the channel can be established accordingly. The electric field between the neighboring selected and unselected word line can also extend into the charge storage layer 424, the tunneling layer 426 and the channel layer 338. The electric field can generate an electric force on the fast charges 428-2 captured in the storage layer 424. The electric force can de-trap the fast charges 428-2 from the shallow traps, pull them towards the neighboring unselected memory cells. The fast charges can then be recombined with charges of opposite sign or be removed through the conductive path established in the channel of the unselected memory cells. As a result, fast charges 428-2 in the storage layer 424 of the selected memory cell 340-3 can be removed through electric field from neighboring unselected memory cells.

[0068] Referring again to Fig. 6, the duration of the read-prepare step of the read-verification operation 600 includes the sum of the delay period t_{delay1} and t_{delay2} . Both t_{delay1} and t_{delay2} can be pre-determined values.

[0069] In some embodiments, after the read-prepare step, the read voltage V_{read} is applied on the Sel_WL to start the sensing step and BL pre-charge. The sensing step has a duration of t_{sensing} , which can also be a predetermined value. During the sensing step, a voltage of 0V is applied on the Unsel_TSG, which switches off the unselected top select gates and electrically

isolates the channel of selected memory string from the channel of unselected memory strings. Similar to the read-verification operation 500 (in Fig. 5), the ramping-down process from the prepare voltage V_{prepare} to 0V has a delay time, resulting from parasitic resistance and capacitance of the 3D memory structure. To switch on the memory cells, the prepare voltage V_{prepare} can be set higher than the threshold voltage V_{th} of the memory cell. When the voltage of Unsel_TSG ramping down from the prepare voltage V_{prepare} to below V_{th} , the top select transistors of the unselected memory strings are switched off accordingly. The read-verification operation 600 has a duration t_{prepare2} from the beginning of the read-prepare step to the moment that the Unsel_TSG drops to below V_{th} . In the other words, the duration t_{prepare2} is the minimum time requirement for turning off the Unsel_TSG in the read-verification operation 600. The read-verification operation 600 has a duration t_{prepare1} from the beginning of the read-prepare step to the moment that the Unsel_TSG reaches 0V. For read-verification operation 600, duration of the read-prepare step, *i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$ is less than t_{prepare2} . The sensing step and BL pre-charge start when Unsel_TSG is above V_{th} and the unselected top select transistor is still on. This operation can provide a minimum time used for the read-prepare step, although more power is consumed. The time saved $t_{\text{PROG-save}}$ is a difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$.

[0070] Fig. 7 illustrates a read-verification operation 700 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 700 is similar to the read-verification operation 600, except having a duration of the read-prepare step (*i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$) equals t_{prepare2} , the minimum time requirement for turning off the Unsel_TSG. In the read-verification operation 700, the sensing step and BL pre-charge start when the unselected top select transistors are just turned off. Still, the time saved $t_{\text{PROG-save}}$ can be expressed as the difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$, as shown in Fig. 7. This operation can be sped-up, and thus improved, without consuming more power.

[0071] Fig. 8 illustrates a read-verification operation 800 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 800 is similar to the read-verification operation 600, except having a duration of the read-prepare step (*i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$) more than t_{prepare2} , the minimum time requirement for turning off the Unsel_TSG. In the read-verification

operation 800, the sensing step and BL pre-charge start after the unselected top select transistors are turned off. The time saved $t_{\text{PROG-save}}$ can also be expressed as the difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$, as shown in Fig. 8. This operation can allow more time for removing fast charges.

[0072] As described above, accelerating fast charge loss in a 3D NAND flash memory can be achieved by applying the prepare voltage V_{prepare} on Unsel_TSG, the pass voltage V_{pass} on the Unsel_WL, and 0V on the Sel-WL at the read-prepare step. The threshold voltage V_{th} of the target memory cell, associated with the Sel_WL, can be stabilized before the sensing step such that the verified storage data can be more reliable.

[0073] In addition, the read-verification operation described above can greatly reduce the time required at the read-prepare step. The fast charges can be removed by electric field generated between Sel_WL and neighboring Unsel_TSG. After fast charge removal, the sensing step starts when the voltage on Sel_WL is switched from 0V to the read voltage V_{read} , without the need to wait for the Unsel-TSG to ramp down from the prepare voltage V_{prepare} to 0V. Therefore, the duration of read-prepare step can be shortened, *i.e.*, $t_{\text{delay1}} + t_{\text{delay2}} < t_{\text{prepare1}}$, where $t_{\text{PROG-save}} = t_{\text{prepare1}} - t_{\text{delay1}} - t_{\text{delay2}}$ is the time saved.

[0074] 3D NAND flash memory with multi-level-cells typically uses an algorithm with incremental step pulses to program the memory cells. After every program pulse, a read-verification operation is performed to check the state of the memory cells. When the memory cell reaches the target state (*i.e.*, target threshold voltage), the program will be stopped. In the meantime, the memory cells not programmed to the target state are calculated towards failed bit count (FBC), where the FBC can be executed in parallel to the read-verification operation to save the time of the entire programming cycle. As shown in Figs. 6-8, FBC operation can be performed in parallel with the read-prepare step. In some embodiments, duration of the FBC operation can be shorter than the duration of the read-prepare step, and the FBC operation can be incorporated within the read-prepare step starting at any suitable time. The failed memory cells can be programmed again to the target memory state accordingly.

[0075] In summary, the present disclosure provides a method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, where the method includes removing fast charges of the target memory cell at a read-prepare step and measuring a threshold voltage of the target memory cell at a sensing step. Removing

the fast charges of the target memory cell includes applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).

[0076] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt, for various applications, such specific embodiments, without undue experimentation, and without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0077] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0078] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0079] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS AND INCORPORATION BY REFERENCE

[0001] This application claims priority to PCT/CN2019/112728 filed on October 23, 2019, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a method for reading a three-dimensional (3D) memory.

BACKGROUND

[0003] As memory devices are shrinking to smaller die size to reduce manufacturing cost and increase storage density, scaling of planar memory cells faces challenges due to process technology limitations and reliability issues. A three-dimensional (3D) memory architecture can address the density and performance limitation in planar memory cells.

[0004] In a 3D NAND flash memory, memory cells can be programmed for data storage based on charge-trapping technology. The storage information of a memory cell depends on the amount of charge trapped in a storage layer. However, fast charges, *i.e.*, charges trapped in shallow traps, can be easily lost. Therefore, the threshold voltage determining the stored information can be different between write and read operations. Accordingly, a read-prepare step is included in a read-verification operation after programming to remove the fast charges and verify the threshold voltage of the memory cell. Fast charge loss depending on the intrinsic de-trapping process in the storage layer can be long, making the read-verification operation inefficient. Therefore, a need exists for a method to accelerate fast charge loss so that threshold voltage or storage information of the memory cell can be verified or read more accurately and efficiently.

BRIEF SUMMARY

- [0005]** Embodiments of a method for conducting read-verification operation of a memory cell in a three-dimensional (3D) memory device is described in the present disclosure.
- [0006]** One aspect of the present disclosure provides a method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device. The method includes removing fast charges of the target memory cell at a read-prepare step, which includes applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL). The method also includes measuring a threshold voltage of the target memory cell at a sensing step.
- [0007]** In some embodiments, the method further includes applying a top select gate voltage (V_{tsg}) on a selected top select gate (Sel_TSG) of a selected memory string containing the target memory cell, and applying a lower select gate voltage (V_{lsg}) on a lower select gate (LSG) of the selected memory string containing the target memory cell.
- [0008]** In some embodiments, applying the top select gate voltage (V_{tsg}) includes electrically connecting the selected memory string to a bit line. In some embodiments, applying the lower select gate voltage (V_{lsg}) includes electrically connecting the selected memory string to an array common source.
- [0009]** In some embodiments, applying the top select gate voltage (V_{tsg}) includes applying a voltage between 4V to 7V. In some embodiments, applying the lower select gate voltage (V_{lsg}) includes applying a voltage between 4V to 7V.
- [0010]** In some embodiments, applying the pass voltage (V_{pass}) includes applying the pass voltage with a delay period after the selected top select gate (Sel_TSG) and the lower select gate (LSG) are at the top select gate voltage (V_{tsg}) and the lower select gate voltage (V_{lsg}), respectively.
- [0011]** In some embodiments, measuring the threshold voltage includes applying a read voltage (V_{read}) on the selected word line (Sel_WL). In some embodiments, applying the read voltage (V_{read}) includes applying a voltage between 0 to 2V. In some embodiments, applying the read voltage (V_{read}) includes applying a second off voltage on the unselected word line

(Unsel_WL). In some embodiments, applying the second off voltage on the unselected word line (Unsel_WL) includes applying a 0V.

[0012] In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is higher than a threshold voltage of an unselected memory cell. In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) equals to a threshold voltage of an unselected memory cell. In some embodiments, applying the read voltage (V_{read}) includes applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is lower than a threshold voltage of an unselected memory cell.

[0013] In some embodiments, applying the prepare voltage (V_{prepare}) includes applying a voltage between 4V to 7V. In some embodiments, applying the first off voltage (V_{off}) includes applying a 0V. In some embodiments, applying the pass voltage (V_{pass}) includes applying a voltage between 5V to 9V.

In some embodiments, removing the fast charges includes removing the fast charges from a storage layer of the target memory cell of a selected memory string, wherein the selected memory string includes a channel hole penetrating vertically through a film stack of alternating conductive and dielectric layers, a core filling film in a center of the channel hole, and a memory film covering a sidewall of the channel hole. The selected memory string also includes a channel layer sandwiched between the memory film and the core filling film. In some embodiments, the memory film includes a barrier layer, the storage layer and a tunneling layer.

[0014] In some embodiments, removing the fast charges includes removing electrical charges from shallow traps in the storage layer of the target memory cell.

[0015] In some embodiments, removing the fast charges includes removing the fast charges from the target memory cell to a neighboring unselected memory cell.

[0016] In some embodiments, conducting the read-verification operation comprises conducting the read-prepare step and conducting a failed bit count in parallel.

[0017] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0018]** The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.
- [0019]** Fig. 1 illustrates a schematic top-down view of an exemplary three-dimensional (3D) memory die, according to some embodiments of the present disclosure.
- [0020]** Fig. 2 illustrates a schematic top-down view of a region of 3D memory die, according to some embodiments of the present disclosure.
- [0021]** Fig. 3 illustrates a perspective view of a portion of an exemplary 3D memory array structure, in accordance with some embodiments of the present disclosure.
- [0022]** Fig. 4A illustrates a cross-sectional view of 3D memory cells, according to some embodiments of the present disclosure.
- [0023]** Fig. 4B illustrates a schematic diagram of a 3D memory array, according to some embodiments of the present disclosure.
- [0024]** Fig. 5 illustrates a timing diagram of a read-verification operation with a prepare voltage (pre-pulse) applied on a selected word line, according to some embodiments of the present disclosure.
- [0025]** Figs. 6-8 illustrate timing diagrams of read-verification operations with accelerated fast charge loss, according to some embodiments of the present disclosure.
- [0026]** The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.
- [0027]** Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0028] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0029] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0030] In general, terminology can be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0031] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something, but also includes the meaning of “on” something with an intermediate feature or a layer there between. Moreover, “above” or “over” not only means

“above” or “over” something, but can also include the meaning it is “above” or “over” something with no intermediate feature or layer there between (i.e., directly on something).

[0032] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, can be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or process step in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0033] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate includes a “top” surface and a “bottom” surface. The top surface of the substrate is typically where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate unless stated otherwise. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0034] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, there above, and/or there below. A layer can include multiple layers. For

example, an interconnect layer can include one or more conductive and contact layers (in which contacts, interconnect lines, and/or vertical interconnect accesses (VIAs) are formed) and one or more dielectric layers.

[0035] In the present disclosure, for ease of description, “tier” is used to refer to elements of substantially the same height along the vertical direction. For example, a word line and the underlying gate dielectric layer can be referred to as “a tier,” a word line and the underlying insulating layer can together be referred to as “a tier,” word lines of substantially the same height can be referred to as “a tier of word lines” or similar, and so on.

[0036] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process step, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0037] In the present disclosure, the term “horizontal/horizontally/lateral/laterally” means nominally parallel to a lateral surface of a substrate, and the term “vertical” or “vertically” means nominally perpendicular to the lateral surface of a substrate.

[0038] As used herein, the term “3D memory” refers to a three-dimensional (3D) semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate.

[0039] Fig. 1 illustrates a top-down view of an exemplary three-dimensional (3D) memory device 100, according to some embodiments of the present disclosure. The 3D memory device 100 can be a memory chip (package), a memory die or any portion of a memory die, and can include one or more memory planes 101, each of which can include a plurality of memory blocks 103. Identical and concurrent operations can take place at each memory plane 101. The memory block 103, which can be megabytes (MB) in size, is the smallest size to carry out erase operations. Shown in Fig. 1, the exemplary 3D memory device 100 includes four memory planes 101 and each memory plane 101 includes six memory blocks

103. Each memory block 103 can include a plurality of memory cells, where each memory cell can be addressed through interconnections such as bit lines and word lines. The bit lines and word lines can be laid out perpendicularly (e.g., in rows and columns, respectively), forming an array of metal lines. The direction of bit lines and word lines are labeled as “BL” and “WL” in Fig. 1. In this disclosure, memory block 103 is also referred to as a “memory array” or “array.” The memory array is the core area in a memory device, performing storage functions.

[0040] The 3D memory device 100 also includes a periphery region 105, an area surrounding memory planes 101. The periphery region 105 contains many digital, analog, and/or mixed-signal circuits to support functions of the memory array, for example, page buffers, row and column decoders and sense amplifiers. Peripheral circuits use active and/or passive semiconductor devices, such as transistors, diodes, capacitors, resistors, etc., as would be apparent to a person of ordinary skill in the art.

[0041] It is noted that, the arrangement of the memory planes 101 in the 3D memory device 100 and the arrangement of the memory blocks 103 in each memory plane 101 illustrated in Fig. 1 are only used as an example, which does not limit the scope of the present disclosure.

[0042] Referring to Fig. 2, an enlarged top-down view of a region 108 in Fig. 1 is illustrated, according to some embodiments of the present disclosure. The region 108 of the 3D memory device 100 can include a staircase region 210 and a channel structure region 211. The channel structure region 211 can include an array of memory strings 212, each including a plurality of stacked memory cells. The staircase region 210 can include a staircase structure and an array of contact structures 214 formed on the staircase structure. In some embodiments, a plurality of slit structures 216, extending in WL direction across the channel structure region 211 and the staircase region 210, can divide a memory block into multiple memory fingers 218. At least some slit structures 216 can function as the common source contact (e.g., array common source) for an array of memory strings 212 in channel structure regions 211. A top select gate cut 220 can be disposed, for example, in the middle of each memory finger 218 to divide a top select gate (TSG) of the memory finger 218 into two portions, and thereby can divide a memory finger into two memory slices 224, where memory cells in a memory slice 224 that share the same word line form a programmable (read/write) memory page. While erase operation of a 3D NAND memory can be carried out

at memory block level, read and write operations can be carried out at memory page level. A memory page can be kilobytes (KB) in size. In some embodiments, region 108 also includes dummy memory strings 222 for process variation control during fabrication and/or for additional mechanical support.

[0043] Fig. 3 illustrates a perspective view of a portion of an exemplary three-dimensional (3D) memory array structure 300, according to some embodiments of the present disclosure. The memory array structure 300 includes a substrate 330, an insulating film 331 over the substrate 330, a tier of lower select gates (LSGs) 332 over the insulating film 331, and a plurality of tiers of control gates 333, also referred to as “word lines (WLs),” stacking on top of the LSGs 332 to form a film stack 335 of alternating conductive and dielectric layers. The dielectric layers adjacent to the tiers of control gates are not shown in Fig. 3 for clarity.

[0044] The control gates of each tier are separated by slit structures 216-1 and 216-2 through the film stack 335. The memory array structure 300 also includes a tier of top select gates (TSGs) 334 over the stack of control gates 333. The stack of TSG 334, control gates 333 and LSG 332 is also referred to as “gate electrodes.” The memory array structure 300 further includes memory strings 212 and doped source line regions 344 in portions of substrate 330 between adjacent LSGs 332. Each memory strings 212 includes a channel hole 336 extending through the insulating film 331 and the film stack 335 of alternating conductive and dielectric layers. Memory strings 212 also includes a memory film 337 on a sidewall of the channel hole 336, a channel layer 338 over the memory film 337, and a core filling film 339 surrounded by the channel layer 338. A memory cell 340 can be formed at the intersection of the control gate 333 and the memory string 212. The memory array structure 300 further includes a plurality of bit lines (BLs) 341 connected with the memory strings 212 over the TSGs 334. The memory array structure 300 also includes a plurality of metal interconnect lines 343 connected with the gate electrodes through a plurality of contact structures 214. The edge of the film stack 335 is configured in a shape of staircase to allow an electrical connection to each tier of the gate electrodes.

[0045] In Fig. 3, for illustrative purposes, three tiers of control gates 333-1, 333-2, and 333-3 are shown together with one tier of TSG 334 and one tier of LSG 332. In this example, each memory string 212 can include three memory cells 340-1, 340-2 and 340-3, corresponding to the control gates 333-1, 333-2 and 333-3, respectively. In some embodiments, the number of

control gates and the number of memory cells can be more than three to increase storage capacity. The memory array structure 300 can also include other structures, for example, TSG cut, common source contact (i.e., array common source) and dummy memory string. These structures are not shown in Fig. 3 for simplicity.

[0046] While floating gate memory cells has been traditionally utilized in flash memories, technology based on charge trapping has demonstrated more scaling ability and higher intrinsic reliability. Three-dimensional NAND using charge trapping technology has been developed for high density storage, where the storage information (*e.g.*, threshold voltage V_{th} of the memory cell) depends on the amount of charge trapped in a storage layer.

[0047] Fig. 4A illustrates a schematic cross-section of a 3D NAND memory 400a, which includes memory cells similar to the memory cell 340 in Fig. 3. The memory cell 340-3 includes a control gate (*e.g.*, the control gate 333), a memory film (*e.g.*, the memory film 337) and a channel layer (*e.g.*, the channel layer 338, also referred to as the channel).

[0048] In a 3D NAND memory, the memory film 337 can be disposed on a sidewall of each channel hole 336 (illustrated in Fig. 3). In some embodiments, the memory film 337 can include a barrier layer 422, a storage layer 424, and a tunneling layer 426. The barrier layer 422 can be used to block the movement of electronic charges 428 between the control gate 333 and the storage layer 424. The barrier layer 422 can include silicon oxide and high dielectric constant (high-k) dielectrics, for example, aluminum oxide. The storage layer 424 can be used to store electronic charges 428 and can include silicon nitride. The storage and/or removal of charges in the storage layer 424 can impact the on/off state and/or a conductance of the channel layer 338. The tunneling layer 426 can be used to control the tunneling of electronic charges 428 (electrons or holes) between the channel layer 338 and the storage layer 424. The tunneling layer 426 can be silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In a 3D NAND memory, the channel layer 338 can be disposed on a sidewall of the memory film 337 in the channel hole 336 (in Fig. 3.) The channel layer 338 can include amorphous silicon, polycrystalline silicon, and/or monocrystalline silicon.

[0049] Fig. 4B shows a schematic circuit diagram of a 3D memory array 400b. As described previously, the 3D memory array 400b includes a plurality of memory strings 212, each memory string 212 having a plurality of stacked memory cells 340. The memory string 212 also includes at least one field effect transistor (*e.g.*, MOSFET) at each end, which is

controlled by the lower select gate (LSG) 332 and the top select gate (TSG) 334, respectively. And the two respective transistors are referred to as lower and top select transistors 332-T and 334-T. The stacked memory cells 340 can be controlled by the control gates 333, where the control gates 333 are connected to word lines (not shown) of the 3D memory array 400b. The drain terminal of the top select transistor 334-T can be connected to the bit lines (*e.g.*, the bit line 341-1, 341-2, 341-3, etc.), and the source terminal of the lower select transistor 332-T can be connected to the doped source line region 344 (*see* Fig. 3), from where an array common source (ACS) 446 can be formed. The array common source 446 can be shared by the memory strings 212 in an entire memory block, and is also referred to as the common source line.

[0050] Referring to Figs. 4A and 4B, in a NAND memory, read and write operations can be performed in a memory page, for example memory page 448, which includes memory cells sharing the same word line. In a NAND memory, each memory cell can be in an erased state or a programmed state. Initially, all memory cells in a block can be reset to the erased state as logic “1” by applying, for example, a negative voltage between the control gates 333 and source terminals of the memory cells (*e.g.*, the array common source 446) such that all the electronic charges 428 in the storage layers 424 of the memory cells can be removed. At the erased state, the threshold voltage V_{th} of the memory cells 340 can be reset to the lowest value, and the corresponding current flowing through the memory cells 340 between the source terminal (*e.g.*, the array common source 446) and the drain terminal (*e.g.*, the bit lines 341) can be at the highest level for a given bias on the word lines.

[0051] During programming (*i.e.*, writing), a high positive voltage pulse (*e.g.*, 12V to 18V) can be applied on the control gate 333 such that electronic charges 428 (*e.g.*, electrons) can be injected into the storage layer 424 of the memory cell 340, where the electronic charges 428-1 and 428-2 can be randomly captured by deep and shallow traps, respectively. After programming, the threshold voltage V_{th} of the memory cell 340 can be raised to a higher value than that of the erased state. At a higher threshold voltage V_{th} , the current flowing through the source and drain terminals of the memory cell can be at a reduced level for a given bias on the word lines. By measuring (*i.e.*, reading) the memory cell current, the threshold voltage V_{th} and thereby the state of the memory cell 340 can be determined accordingly.

- [0052]** With multi-level-cell or triple-level-cell technology, each memory cell 340 can have multiple programmed states, *i.e.*, multiple values of threshold voltages V_{th} . After every programming pulse, a read-verification operation can be performed to check the state of the memory cell. As such, each memory cell 340 can store multiple bits, leading to significant increase of storage capacity.
- [0053]** For memory cell 340 in a programmed state, electronic charges 428-1 and 428-2 located within the proximity of control gate 333 can affect threshold voltage V_{th} of the memory cell 340. The electronic charges 428-3 located beyond the electric field from control gate 333, and therefore have little impact on the threshold voltage V_{th} of the memory cell. In addition, electronic charges 428-2 captured by shallow traps in the storage layer 424 can be easily de-trapped, and can thereby cause initial threshold-voltage (V_{th}) shift (IVS) during storage period. This process is also referred to as fast charge loss. For programmed state at higher threshold voltage V_{th} , IVS can be larger due to larger amount of electronic charges injected to the storage layer, which results in larger number of electronic charges 428-2 captured by shallow traps (also referred to as fast charges).
- [0054]** Due to IVS, the programmed state immediately after writing cannot reflect the target threshold voltage V_{th} of the memory cell 340 in real applications. Applying the fake high threshold voltage V_{th} can cause high bit-error-rate in the memory. Therefore, it is necessary to de-trap and remove fast charges prior to read operation such that the V_{th} distribution profile of each programmed state can be more accurately determined.
- [0055]** Fig. 5 illustrates a timing diagram of a read-verification operation 500 with a prepare voltage (pre-pulse) applied on a selected word line, according to some embodiments of the present disclosure. The read-verification operation 500 can reduce read disturb for unselected memory strings in a 3D NAND memory. Read disturb can occur when the threshold voltage V_{th} (*i.e.*, the programmed state) of an unselected memory cell is changed or disturbed during read or read-verification of a selected memory cell. In some embodiments, the read-verification operation 500 includes two steps, *i.e.*, a read-prepare step and a sensing step, having duration of $t_{prepare}$ and $t_{sensing}$, respectively. The timing diagram of a selected top select gate (Sel_TSG), unselected top select gates (Unsel_TSG), a selected word line (Sel_WL), unselected word lines (Unsel_WL) and the lower select gate (LSG) are shown in Fig. 5.

[0056] The read-verification operation 500 starts with the read-prepare step. The TSG 334 and the LSG 332 of a selected memory string, for example TSG 334-3 and LSG 332-3 of a selected memory string 212-3 in Fig. 4B, can be applied with a top select gate voltage V_{tsg} and a lower select gate voltage V_{lsg} . A corresponding top select transistor 334-T and a lower select transistor 332-T of the selected memory string 212-3 can be switched on. The top and lower select gate voltages V_{tsg} and V_{lsg} can be in a range between 4V to 7V. Accordingly, a current path through the stacked memory cells 340 can be established for the selected memory string 212-3. For example, the current flowing through the selected memory string 212-3 can be detected from the bit line 341-3 and the array common source 446 that are electrically connected with the selected memory string 212-3.

[0057] For the read-verification operation 500, the TSG of unselected memory strings (Unsel-TSG), for example TSG 334-1 of memory string 212-1 in Fig. 4B, can be applied with a first off voltage (V_{off}), for example 0V, to switch off a corresponding top select transistor 334-T. Current path between the unselected memory strings 212-1 and bit lines 341-1 can be disconnected. Therefore, the channel of selected memory string 212-3 and unselected memory strings 212-1 can be electrically isolated.

[0058] It is noted that there is a delay for the voltages to ramp up during the read-prepare step. This delay can be caused by parasitic capacitors and resistors, and is well-known for a person skilled in the art. Although a memory string is selected and used as an example to describe read-verification operation herein, it is noted that a plurality of memory strings, for example, a memory finger can be selected and operated in a similar way.

[0059] Referring again to Figs. 4A, 4B and 5, to verify a target memory cell 340-3 in the selected memory string 212-3, a selected word line (*e.g.*, Sel_WL in Fig. 4B) can be applied with a prepare voltage $V_{prepare}$ (also referred to as pre-pulse), while other word lines not selected (*e.g.*, Unsel_WL in Fig. 4B) can be applied with a pass voltage V_{pass} . The selected word line are electrically connected to the control gate 333 of the target memory cell 340-3. The prepare voltage $V_{prepare}$ can be in a range between 4V to 7V, and the pass voltage V_{pass} can be in a range between 5V to 9V. The pass voltage V_{pass} can be higher than the highest threshold voltage of the programmed states such that the memory cells on the selected memory string 212-3 can be fully switched on. When the prepare voltage $V_{prepare}$ is applied on the selected word line Sel_WL, the target memory cell 340-3 can also be switched on.

Therefore, at time t_1 , the top and lower select transistors 334-T and 332-T, and all memory cells 340 of the selected memory string 212-3 are switched on. Current flows between the bit line 341-3 and the array common source 446 via the channel layer of the selected memory string 212-3. As current flowing through the channel layer 338 forming a conductive path, de-trapped fast charges 428-2 from the storage layer 424 can be removed through the conductive path. However, fast charge loss can be a slow process, which is shown in the timing diagram of the selected word line (Sel_WL) in Fig. 5.

[0060] In some embodiments, fast charges 428-2 can also be removed by thermal annealing or by implementing soft erase with a low negative voltage on the control gate. However, the read-prepare step generally can take a long time and thus impact the efficiency of the read-verification operation. Therefore, a need exists for a read-verification operation to provide accelerated fast charge loss and shorten read-prepare step.

[0061] In some embodiments, the read-prepare step can reduce read disturb for the unselected memory strings, for example, memory strings 212-1 and 212-2 in Fig. 4B. As described above, the unselected top select gates (Unsel_TSG) for unselected memory strings (e.g., TSG 334-1 of memory string 212-1) can be applied with the first off voltage (V_{off}), e.g., 0V, to switch off the corresponding top select transistors 334-T and disconnect from the bit lines (e.g., bit line 341-1) as depicted in Fig. 4B. In some embodiments, the lower select gates (LSG) of the unselected memory strings (e.g., LSG 332-1) are applied with the lower select gate voltage V_{lsg} such that the lower select transistors 332-T are switched on. By applying the prepare voltage V_{prepare} on the selected word line (Sel_WL), corresponding memory cells (e.g., memory cells 340-1, 340-2, 340-3, etc.) can be switched on if the prepare voltage V_{prepare} is selected to be higher than the threshold voltages of the programmed states of the memory cells. In this example, the channel of the memory cells of the unselected memory strings (e.g., memory cells 340-1) can be electrically connected to the array common source 446 to maintain at a predetermined potential, e.g., ground.

[0062] In an example that the prepare voltage V_{prepare} is not applied on the selected word line (Sel_WL), the memory cells corresponding to the selected word line (e.g., the memory cell 340-1 of memory string 212-1) may not be fully switched on (e.g., a voltage applied on the selected word line is lower than the threshold voltage V_{th} of the memory cell 340-1). Upper memory cells, i.e., memory cells located between the bit line (e.g., bit line 341-1) and the

selected word line (Sel_WL) of the unselected memory string (e.g., memory string 212-1), can have floating channels, where the channel layer is not electrically connected to the bit lines 341 or the common array source 446. Channel potential of the upper memory cells of the unselected memory string (e.g., memory string 212-1) can vary randomly. Memory cells with floating channel can suffer charge loss due to an unknown electrical field between the control gate 333 and the channel layer 338 (see Fig. 4A). The trapped charges 428 and thereby the threshold voltages V_{th} (i.e., programmed states) of the memory cells can be changed or disturbed, where the change can be significant with the increased number of reading operation. By introducing the read_prepare step prior to the sensing step, as described previously, read disturb on the unselected memory strings can be reduced.

[0063] After the read_prepare step, the voltage bias on the selected word line (Sel_WL) can be reduced from the prepare voltage $V_{prepare}$ to a read voltage V_{read} to sense (i.e., read or measure) the threshold voltage V_{th} of the target memory cell. The read voltage V_{read} can be in a range between 0V to 2V. For the target memory cell programmed with threshold voltage V_{th} lower than the read voltage V_{read} , the target memory cell can be switch on and form a conductive path in the channel layer 338. If the threshold voltage V_{th} is higher than the read voltage V_{read} , the channel of the target memory cell is switched off. The programmed state of the target memory cell can be determined accordingly. It is noted that the transition period from the prepare voltage $V_{prepare}$ to the read voltage V_{read} is a slow process due to parasitic capacitance and resistance as well as slow de-trapping process of fast trap loss. The sensing step can start after the Sel_WL reach the read voltage V_{read} , which increases the overall duration $t_{prepare}$ of read-prepare step.

[0064] Fig. 6 illustrates a read-verification operation 600 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 600 also includes the read-prepare step and the sensing step. During the read-prepare step of the read-verification operation 600, the Sel_TSG and the LSG can be applied with the top and lower select gate voltages V_{tsg} and V_{lsg} , respectively, to switch on the top and lower select transistors 334-T and 332-T (in Fig. 4B), similar to those used in the read-verification operation 500 in Fig. 5. However, unlike the read-verification operation 500, the Unsel_TSG of the read-verification operation 600 is applied with the prepare voltage $V_{prepare}$ during the read-prepare step. Accordingly, the

selected and unselected memory strings can all be electrically accessed from the bit line 341 and the array common source 446.

[0065] In some embodiments, during the read-prepare step of the read-verification operation 600, the selected memory cell can be switched off by applying a second off voltage, *e.g.*, 0V on the selected WL (*i.e.*, Sel_WL). The unselected memory cells (*i.e.*, Unsel_WL) can be switched on with the pass voltage V_{pass} after a delay period t_{delay1} . During the delay period t_{delay1} , all select transistors controlled by Sel_TSG, Unsel_TSG and LSG are turned on with applied voltages V_{tsg} , V_{prepare} and V_{lsg} and thus the channel of the memory string 212 can be electrically connected to the bit line 341 and the array common source 446 (shown in Fig. 4B), and can be maintained at a potential adjustable by a voltage of the bit line 341. When the Unsel_WL is applied with the pass voltage V_{pass} , all the unselected memory cells of the selected memory string are switched on. Therefore, the channel of the selected memory cell can be electrically connected to the bit line 341 through upper memory cells and to the array common source 446 through the lower memory cells. The channel of the selected memory cell can thereby be held at a potential adjustable by the voltage of the bit line 341 and the array common source 446.

[0066] In some embodiments, the delay period t_{delay1} is implemented such that the channel of the memory string 212 is not electrically isolated from the bit line 341 or the array common source 446 before Unsel_WL can be ramped up from 0V to the pass voltage V_{pass} . Referring to Fig. 4B and Fig. 6, if the Unsel_WL is applied with the pass voltage V_{pass} before the Sel_TSG reach the top select gate voltage V_{tsg} or Unsel_TSG reach the prepare voltage V_{prepare} , the top select transistors are off and upper portion of the channel layer 338 that is located close to the bit line 341 becomes a floating node. More specifically upper memory cells located between the bit line and the selected memory cell can have a floating channel potential. Similarly, if the Unsel_WL is applied with the pass voltage V_{pass} before the LSG ramps up to the lower select gate voltage V_{lsg} to switch on the lower select transistor, lower portion of the channel layer 338 that is located close to the array common source 446 becomes a floating node. More specifically lower memory cells located between the bit line and the selected memory cell can have a floating channel potential. When floating, channel potential of the memory cells can be boosted by the pass voltage V_{pass} of the Unsel_WL through coupled capacitance. The boosted channel potential of the unselected memory cells

can influence the channel potential of the neighboring selected memory cell and influence fast charge removing process. By introducing the delay period t_{delay1} , the aforementioned self-boosting effect or read disturb on the selected or unselected memory cell can be avoided.

[0067] In some embodiments, the read-prepare step also includes a delay period t_{delay2} , a duration between ramping up the pass voltage V_{pass} of Unsel_WL and the read voltage V_{read} of the Sel_WL. During the delay period t_{delay2} , the voltage of Sel_WL is kept at 0V while the voltage of Unsel_WL is raised from 0V to the pass voltage V_{pass} . As discussed previously, the pass voltage V_{pass} is applied on the Unsel_WL after the top and lower select transistors are switched on with applied voltages V_{tsg} , V_{prepare} and V_{lsg} on Sel_TSG, Unsel-TSG and LSG, respectively. As such, the selected memory cell is switched off while unselected memory cells are switched on. Referring back to Fig. 4A, while the selected memory cell 340-3 is switched off, the neighboring unselected memory cells 340 are switched on. Between the selected memory cell 340-3 with a 0V gate bias and the neighboring unselected memory cells 340 with a gate bias of the pass voltage V_{pass} , an electric field parallel to the channel can be established accordingly. The electric field between the neighboring selected and unselected word line can also extend into the charge storage layer 424, the tunneling layer 426 and the channel layer 338. The electric field can generate an electric force on the fast charges 428-2 captured in the storage layer 424. The electric force can de-trap the fast charges 428-2 from the shallow traps, pull them towards the neighboring unselected memory cells. The fast charges can then be recombined with charges of opposite sign or be removed through the conductive path established in the channel of the unselected memory cells. As a result, fast charges 428-2 in the storage layer 424 of the selected memory cell 340-3 can be removed through electric field from neighboring unselected memory cells.

[0068] Referring again to Fig. 6, the duration of the read-prepare step of the read-verification operation 600 includes the sum of the delay period t_{delay1} and t_{delay2} . Both t_{delay1} and t_{delay2} can be pre-determined values.

[0069] In some embodiments, after the read-prepare step, the read voltage V_{read} is applied on the Sel_WL to start the sensing step and BL pre-charge. The sensing step has a duration of t_{sensing} , which can also be a predetermined value. During the sensing step, a voltage of 0V is applied on the Unsel_TSG, which switches off the unselected top select gates and electrically isolates the channel of selected memory string from the channel of unselected memory

strings. Similar to the read-verification operation 500 (in Fig. 5), the ramping-down process from the prepare voltage V_{prepare} to 0V has a delay time, resulting from parasitic resistance and capacitance of the 3D memory structure. To switch on the memory cells, the prepare voltage V_{prepare} can be set higher than the threshold voltage V_{th} of the memory cell. When the voltage of Unsel_TSG ramping down from the prepare voltage V_{prepare} to below V_{th} , the top select transistors of the unselected memory strings are switched off accordingly. The read-verification operation 600 has a duration t_{prepare2} from the beginning of the read-prepare step to the moment that the Unsel_TSG drops to below V_{th} . In the other words, the duration t_{prepare2} is the minimum time requirement for turning off the Unsel_TSG in the read-verification operation 600. The read-verification operation 600 has a duration t_{prepare1} from the beginning of the read-prepare step to the moment that the Unsel_TSG reaches 0V. For read-verification operation 600, duration of the read-prepare step, *i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$ is less than t_{prepare2} . The sensing step and BL pre-charge start when Unsel_TSG is above V_{th} and the unselected top select transistor is still on. This operation can provide a minimum time used for the read-prepare step, although more power is consumed. The time saved $t_{\text{PROG-save}}$ is a difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$.

[0070] Fig. 7 illustrates a read-verification operation 700 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 700 is similar to the read-verification operation 600, except having a duration of the read-prepare step (*i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$) equals t_{prepare2} , the minimum time requirement for turning off the Unsel_TSG. In the read-verification operation 700, the sensing step and BL pre-charge start when the unselected top select transistors are just turned off. Still, the time saved $t_{\text{PROG-save}}$ can be expressed as the difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$, as shown in Fig. 7. This operation can be sped-up, and thus improved, without consuming more power.

[0071] Fig. 8 illustrates a read-verification operation 800 designed to accelerate fast charge loss in a three-dimensional flash memory, according to some embodiments of the present disclosure. The read-verification operation 800 is similar to the read-verification operation 600, except having a duration of the read-prepare step (*i.e.*, $t_{\text{delay1}} + t_{\text{delay2}}$) more than t_{prepare2} , the minimum time requirement for turning off the Unsel_TSG. In the read-verification operation 800, the sensing step and BL pre-charge start after the unselected top select

transistors are turned off. The time saved $t_{\text{PROG-save}}$ can also be expressed as the difference between t_{prepare1} and $t_{\text{delay1}} + t_{\text{delay2}}$, as shown in Fig. 8. This operation can allow more time for removing fast charges.

[0072] As described above, accelerating fast charge loss in a 3D NAND flash memory can be achieved by applying the prepare voltage V_{prepare} on Unsel_TSG, the pass voltage V_{pass} on the Unsel_WL, and 0V on the Sel-WL at the read-prepare step. The threshold voltage V_{th} of the target memory cell, associated with the Sel_WL, can be stabilized before the sensing step such that the verified storage data can be more reliable.

[0073] In addition, the read-verification operation described above can greatly reduce the time required at the read-prepare step. The fast charges can be removed by electric field generated between Sel_WL and neighboring Unsel_TSG. After fast charge removal, the sensing step starts when the voltage on Sel_WL is switched from 0V to the read voltage V_{read} , without the need to wait for the Unsel-TSG to ramp down from the prepare voltage V_{prepare} to 0V. Therefore, the duration of read-prepare step can be shortened, *i.e.*, $t_{\text{delay1}} + t_{\text{delay2}} < t_{\text{prepare1}}$, where $t_{\text{PROG-save}} = t_{\text{prepare1}} - t_{\text{delay1}} - t_{\text{delay2}}$ is the time saved.

[0074] 3D NAND flash memory with multi-level-cells typically uses an algorithm with incremental step pulses to program the memory cells. After every program pulse, a read-verification operation is performed to check the state of the memory cells. When the memory cell reaches the target state (*i.e.*, target threshold voltage), the program will be stopped. In the meantime, the memory cells not programed to the target state are calculated towards failed bit count (FBC), where the FBC can be executed in parallel to the read-verification operation to save the time of the entire programming cycle. As shown in Figs. 6-8, FBC operation can be performed in parallel with the read-prepare step. In some embodiments, duration of the FBC operation can be shorter than the duration of the read-prepare step, and the FBC operation can be incorporated within the read-prepare step starting at any suitable time. The failed memory cells can be programmed again to the target memory state accordingly.

[0075] In summary, the present disclosure provides a method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, where the method includes removing fast charges of the target memory cell at a read-prepare step and measuring a threshold voltage of the target memory cell at a sensing step. Removing the fast charges of the target memory cell includes applying a prepare voltage (V_{prepare}) on an

unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).

[0076] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt, for various applications, such specific embodiments, without undue experimentation, and without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0077] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0078] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0079] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

Electronic Acknowledgement Receipt

EFS ID:	38456363
Application Number:	16729838
International Application Number:	
Confirmation Number:	5773
Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Donald J. Featherstone/David Ofori Amanfo
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0850001
Receipt Date:	31-JAN-2020
Filing Date:	30-DEC-2019
Time Stamp:	14:12:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2020-01-31-Miscellaneous-Letter-4123-0850001.pdf	226082	no	2
			18912b3094ea43b5412c41e46d1693662447cc88		

Warnings:

Information:					
2		2020-01-31-Preliminary-Amendment-4123-0850001.pdf	109395	yes	4
			2d029a8305925428d16b20aaff14c80a2a73db24		
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Preliminary Amendment	1	1		
	Specification	2	2		
	Drawings-only black and white line drawings	3	3		
	Applicant Arguments/Remarks Made in an Amendment	4	4		
Warnings:					
Information:					
3	Drawings-only black and white line drawings	2020-01-31-Replacement-Sheet-4123-0850001.pdf	132700	no	1
			441c6989a2f0f83899f16942b7aef87d2873b770		
Warnings:					
Information:					
4	Applicant Response to Pre-Exam Formalities Notice	2020-01-31-Notice-Corrected-Application-Papers-4123-0850001.pdf	1979398	no	2
			2a7c466c8ca7641e42f74c173ba58daf83bcc2e10		
Warnings:					
Information:					
5	Specification	2020-01-31-Substitute-Specification-Marked-Up-4123-0850001.pdf	138160	no	20
			ab02570c58cae87636922ed6b85d3991302c3f5f		
Warnings:					
Information:					
6	Specification	2020-01-31-Substitute-Specification-Clean-4123-0850001.pdf	137482	no	20
			810f8fa6b9952e872d4fa6a276f6ab6b4877413e		
Warnings:					
Information:					
Total Files Size (in bytes):			2723217		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

January 31, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 5773
Mail Stop Missing Parts

Re: U.S. Patent Application
Appl. No. 16/729,838; Filed: December 30, 2019
For: **METHOD FOR READING THREE-DIMENSIONAL FLASH
MEMORY**
Inventors: CHEN *et al.*
Our Ref: 4123.0850001

Commissioner:

In reply to the "Notice to File Corrected Application Papers," dated January 24, 2020, Applicant transmit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. Reply to Notice to File Corrected Application Papers and Preliminary Amendment Under 37 C.F.R. § 1.115;
2. 1 Sheet of Replacement Drawings: (Figures 4A and 4B);
3. A Copy of the Notice to File Corrected Application Papers, dated January 24, 2020;
4. Marked-Up Copy of Substitute Statement; and
5. Clean Copy of Substitute Statement.

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Commissioner for Patents
January 31, 2020
Page 2

If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/d-o
Enclosures

Amendments to the Drawings

Figures 4(a) and 4(b) are renumbered as “Fig. 4A” and “Fig. 4B,” respectively. A replacement drawing sheet with the amended Figures 4A and 4B is attached to this response. No new matter has been added based on this amendment. Identification of the replacement drawing sheet submitted herewith is provided in accordance with 37 C.F.R. §§ 1.84 and 1.121(d). Acknowledgement of the receipt, approval and entry of this drawing sheet into this application is respectfully requested.

Remarks

In reply to the Notice to File Corrected Application Papers dated January 24, 2020, Applicant submits herewith a marked-up version and a clean version of the substitute specification, and replacement Figures 4A and 4B. These changes are believed to introduce no new matter, and their entry thereof is respectfully requested.

Conclusion

Prompt and favorable consideration of these amendments is respectfully requested. Applicant believes the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 1/31/2020

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

14492270.1



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/729,838	12/30/2019	2827	1880	4123.0850001	20	1

CONFIRMATION NO. 5773

UPDATED FILING RECEIPT

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



Date Mailed: 02/05/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Zilong CHEN, Wuhan, CHINA;
Xiang FU, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2019/112728 10/23/2019

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/22/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/729,838**

Projected Publication Date: 04/29/2021

Non-Publication Request: No

Early Publication Request: No
Title

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/729,838				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760			
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *				x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 460 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1720			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/729,838	12/30/2019	Zilong CHEN	4123.0850001

CONFIRMATION NO. 5773

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

INFORMAL NOTICE



Date Mailed: 02/05/2020

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
Zilong CHEN
Xiang FU

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/ebekele/

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

April 2, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 5773
Art Unit 2827

Re: U.S. Utility Patent Application
Appl. No. 16/729,838; Filing Date: December 30, 2019
For: **METHOD FOR READING THREE-DIMENSIONAL FLASH
MEMORY**
Inventors: CHEN *et al.*
Our Ref: 4123.0850001

Commissioner:

Transmitted herewith for appropriate action is a document entitled ***Combined Declaration and Assignment***, which is submitted electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/jcv
Enclosure

14805073_1.docx

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 16/729,838
filed on December 30, 2019

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is No. 88 Weilai 3rd Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**, for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Zilong CHEN Date: 2020-03-09

Signature of Inventor: Zilong CHEN

LEGAL NAME OF INVENTOR

Inventor: Xiang FU Date: 2020-03-09

Signature of Inventor: Xiang Fu

SCHEDULE A

**UNITED STATES PATENTS, UNITED STATES PATENT APPLICATIONS AND
INTERNATIONAL APPLICATIONS THAT DESIGNATE THE UNITED STATES**

<u>Application No.</u>	<u>Filing Date</u>	<u>Patent No.</u>	<u>Issue Date</u>
PCT/CN2019/112728	October 23, 2019		

OTHER INTERNATIONAL APPLICATIONS AND PATENTS

<u>Country</u>	<u>Application No.</u>	<u>Filing Date</u>
----------------	------------------------	--------------------

Electronic Acknowledgement Receipt	
EFS ID:	39045400
Application Number:	16729838
International Application Number:	
Confirmation Number:	5773
Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Donald J. Featherstone/Julia Vang
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0850001
Receipt Date:	02-APR-2020
Filing Date:	30-DEC-2019
Time Stamp:	16:23:44
Application Type:	Utility under 35 USC 111(a)

Payment information:					
Submitted with Payment			no		
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2020-04-02-Cover-Letter-4123-0850001.pdf	323243	no	1
			0c00173d488785d169e81469eea23329522d6552		
Warnings:					

Information:					
2	Oath or Declaration filed	2020-04-02-Declaration-Assignment-4123-0850001.PDF	124384	no	4
			21efce808c5b235197ba2fa1bf0ac08e5a4a8805		
Warnings:					
Information:					
Total Files Size (in bytes):			447627		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6044552

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	ZILONG CHEN	03/09/2020
	XIANG FU	03/09/2020
RECEIVING PARTY DATA		
Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.	
Street Address:	NO. 88 WEILAI 3RD ROAD, EAST LAKE HIGH-TECH DEVELOPMENT ZONE, WUHAN	
City:	HUBEI	
State/Country:	CHINA	
PROPERTY NUMBERS Total: 1		
	Property Type	Number
	Application Number:	16729838
CORRESPONDENCE DATA		
Fax Number:	(202)371-2540	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
Phone:	2023712600	
Email:	jvang@sternekessler.com, myang@sternekessler.com	
Correspondent Name:	STERNE, KESSLER, GOLDSTEIN & FOX, P.L.L.C.	
Address Line 1:	1100 NEW YORK AVENUE, NW	
Address Line 4:	WASHINGTON, D.C. 20005	
ATTORNEY DOCKET NUMBER:	4123.0850001	
NAME OF SUBMITTER:	DONALD J. FEATHERSTONE	
SIGNATURE:	/Donald J. Featherstone/	
DATE SIGNED:	04/02/2020	
	This document serves as an Oath/Declaration (37 CFR 1.63).	
Total Attachments: 4		
source=2020-03-31-Assignment-4123-0850001#page1.tif		
source=2020-03-31-Assignment-4123-0850001#page2.tif		
source=2020-03-31-Assignment-4123-0850001#page3.tif		
source=2020-03-31-Assignment-4123-0850001#page4.tif		

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 16/729,838
filed on December 30, 2019

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is No. 88 Weilai 3rd Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**, for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Zilong CHEN Date: 2020-03-09

Signature of Inventor: Zilong CHEN

LEGAL NAME OF INVENTOR

Inventor: Xiang FU Date: 2020-03-09

Signature of Inventor: Xiang Fu

SCHEDULE A

**UNITED STATES PATENTS, UNITED STATES PATENT APPLICATIONS AND
INTERNATIONAL APPLICATIONS THAT DESIGNATE THE UNITED STATES**

Application No.	Filing Date	Patent No.	Issue Date
PCT/CN2019/112728	October 23, 2019		

OTHER INTERNATIONAL APPLICATIONS AND PATENTS

Country	Application No.	Filing Date
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Sheet

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3

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Complete if Known

Application Number	16/729,838
Filing Date	December 30, 2019
First Named Inventor	Zilong CHEN
Art Unit	2827
Examiner Name	LE, THONG QUOC
Attorney Docket Number	4123.0850001

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	MM-DD-YYYY			
	FP1	CN 102760490 A	10-31-2012	SK HYNIX INC		
	FP2	CN 108140415 A	06-08-2018	SUNRISE MEMORY CORP		
	FP3	CN 109390012 A	02-26-2019	GIGADEVICE SEMICONDUCTOR		✓

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(12) 发明专利申请

(10) 申请公布号 CN 102760490 A

(43) 申请公布日 2012. 10. 31

(21) 申请号 201210125262. 1

(22) 申请日 2012. 04. 25

(30) 优先权数据

10-2011-0038987 2011. 04. 26 KR

(71) 申请人 爱思开海力士有限公司

地址 韩国京畿道

(72) 发明人 白容默

(74) 专利代理机构 北京弘权知识产权代理事务
所(普通合伙) 11363

代理人 俞波 郭放

(51) Int. Cl.

G11C 16/02(2006. 01)

G11C 16/34(2006. 01)

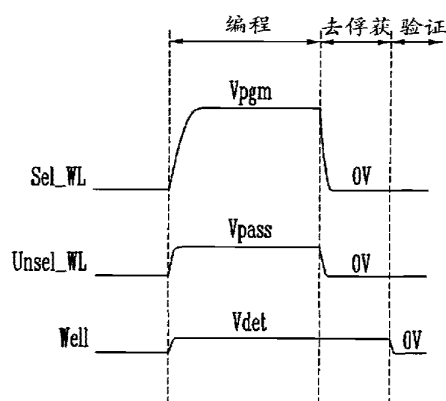
权利要求书 2 页 说明书 6 页 附图 4 页

(54) 发明名称

半导体器件及其操作方法

(57) 摘要

本发明公开了一种半导体器件及其操作方法。所述半导体器件的操作方法包括:通过将编程电压供给到存储器单元的控制栅极和将去俘获电压供给到在半导体衬底内形成的阱来对所述存储器单元进行编程;以及,随后在对编程的存储器单元进行验证之前通过将低于所述去俘获电压的电压供给到所述控制栅极并且还将所述去俘获电压供给到所述阱,来去除在所述存储器单元的隧道绝缘层中俘获的电子。



1. 一种半导体器件的操作方法,包括以下步骤:

通过将编程电压供给到存储器单元的控制栅极和将去俘获电压供给到在半导体衬底内形成的阱来对所述存储器单元进行编程;以及

随后在对编程的存储器单元进行验证之前,通过将低于所述去俘获电压的电压供给到所述控制栅极并且还将所述去俘获电压供给到所述阱,来去除在所述存储器单元的隧道绝缘层中俘获的电子。

2. 如权利要求 1 所述的操作方法,其中,所述去俘获电压具有低于所述编程电压的正电压。

3. 如权利要求 2 所述的操作方法,其中,所述去俘获电压为 0.1V 至 0.5V。

4. 如权利要求 1 所述的操作方法,其中,所述编程电压增加了所述去俘获电压。

5. 如权利要求 1 所述的操作方法,其中,将低于所述去俘获电压的电压供给到所述控制栅极的步骤包括:在所述去俘获电压被供给到所述阱的状态下将接地电压供给到所述控制栅极。

6. 如权利要求 1 所述的操作方法,还包括以下步骤:在去除在所述隧道绝缘层中俘获的电子之后通过降低施加给所述阱的电压来验证所述存储器单元。

7. 如权利要求 6 所述的操作方法,其中,降低施加给所述阱的电压的步骤包括将接地电压供给到所述阱。

8. 一种半导体器件的操作方法,包括以下步骤:

通过将编程电压供给到选中的字线、将通过电压供给到未选中的字线和将去俘获电压供给到阱来对选中的存储器单元进行编程,其中所述编程电压高于所述通过电压且所述通过电压高于所述去俘获电压;以及

随后在执行所述存储器单元的验证操作之前,将低于所述去俘获电压的电压供给到所述选中的字线和所述未选中的字线并且还将所述去俘获电压供给到所述阱。

9. 如权利要求 8 所述的操作方法,其中,所述去俘获电压具有低于通过电压的正电压。

10. 如权利要求 8 所述的操作方法,其中,所述去俘获电压为 0.1V 至 0.5V。

11. 如权利要求 8 所述的操作方法,其中,所述编程电压和所述通过电压中的每个都增加了所述去俘获电压。

12. 如权利要求 8 所述的操作方法,还包括:通过在所述去俘获电压被供给到所述阱的状态下,在将低于所述去俘获电压的电压供给到所述选中的字线和所述未选中的字线之后将接地电压供给所述阱来执行验证操作。

13. 如权利要求 8 所述的操作方法,还包括以下步骤:

将编程允许电压供给到与所述选中的存储器单元耦接的选中的位线,其中所述编程允许电压是为了在所述选中的存储器单元上执行编程、擦除或读取操作而施加的电压;以及

将编程禁止电压供给到剩余的未选中位线,其中所述编程禁止电压是为了防止在所述未选中的存储器单元上执行编程、擦除或读取操作而供给的电压。

14. 如权利要求 13 所述的操作方法,其中,

所述编程允许电压是接地电压,以及

所述编程禁止电压是电源电压。

15. 一种半导体器件,包括:

包括多个存储块的存储器单元阵列；

电压供给电路,被配置成将编程电压供给到选中的字线、将通过电压供给到未选中的字线以及将去俘获电压供给到阱,其中所述编程电压高于所述通过电压,所述通过电压高于所述去俘获电压;以及

控制电路,被配置成控制所述电压供给电路使得所述编程电压、所述通过电压和所述去俘获电压在编程操作中被分别供给到选中的字线、未选中的字线和阱,以及随后在编程验证操作之前,将低于所述去俘获电压的电压供给到所述选中的字线和所述未选中的字线并且还将所述去俘获电压供给到所述阱。

16. 如权利要求 15 所述的半导体器件,其中,所述电压供给电路包括:

电压生成器,被配置成响应于所述控制电路的控制信号而生成所述编程电压、所述通过电压和所述去俘获电压;以及

行译码器,被配置成将所述电压发生器的电压供给到所述选中的字线、所述未选中的字线和所述阱。

17. 如权利要求 16 所述的半导体器件,还包括:

页缓冲器组,包括多个页缓冲器,且被配置成在所述控制电路的控制下将编程许可电压或编程禁止电压供给到从所述存储块中选出的存储块,其中所述编程许可电压是为了在所述选中的存储器单元上执行编程操作、擦除操作或读取操作而供给的电压,所述编程禁止电压是为了防止在未选中的存储器单元上执行编程操作、擦除操作或读取操作而供给的电压;

列选择器,被配置成选择所述页缓冲器;以及

输入/输出电路,被配置成将数据传送到所述列选择器。

半导体器件及其操作方法

[0001] 相关申请的交叉引用

[0002] 本申请要求 2011 年 4 月 26 日提交的申请号为 10-2011-0038987 的韩国专利申请的优先权,本申请通过引用包括该申请的全部内容。

技术领域

[0003] 示例性实施例涉及一种半导体器件及其操作方法,更具体而言,涉及编程操作中的去俘获 (detrap) 方法。

背景技术

[0004] 半导体器件包括用于存储数据的多个存储器单元。为了在存储器单元中存储数据,执行编程操作。在编程操作中,一些电子被俘获在特定的层中,且被俘获的电子能够恶化存储器单元的电特性。以下参考图 1 来描述这种电子俘获现象。

[0005] 图 1 是示出常规编程操作的特征的存储器单元的截面图。

[0006] 如图 1 所示,存储器单元包括顺序层叠在半导体衬底 11 之上的隧道绝缘层 13、电荷俘获层 14、电介质层 15 以及控制栅极 16。结 12 形成在存储器单元两侧上的半导体衬底 11 中。结 12 形成在半导体衬底 11 内所形成的阱内,且隧道绝缘层 13 和阱彼此部分地重叠。电荷俘获层 14 也被称作浮置栅极。控制栅极 16 与字线 WL 耦接。隧道绝缘层 13 由氧化物层形成。电荷俘获层 14 和控制栅极 16 由导电层 (例如多晶硅层) 形成。电介质层 15 具有包括高电介质层 (或氧化物层)、氮化物层以及氧化物层的层叠结构。

[0007] 当编程许可电压 (例如 0V) 被供给到阱和位线时,通过向字线 WL 供给编程电压来执行存储器单元的编程操作。当高编程电压被供给到字线 WL 时,阱中的一些电子通过 Fowler-Nordheim(FN) 隧穿经由隧道绝缘层 13 向电荷俘获层 14 移动。被编程的存储器单元根据电荷俘获层 14 中俘获的电子的量而具有不同的阈值电压。当特定的存储器单元的阈值电压达到目标电平时,所述存储器单元对应于被编程的单元。当存储器单元的阈值电压低于目标电平时,所述存储器单元对应于未编程的 (或擦除的) 单元。

[0008] 通过向与存储器单元耦接的字线 WL 供给读取电压来执行存储器单元的读取操作。可以根据存储器单元的阈值电压高于还是低于读取电压来确定存储器单元的状态。

[0009] 如上所述,通过存储器单元的阈值电压来确定存储器单元的数据,且通过在电荷俘获层 14 中俘获的电子数目 (更具体来说,被编程的电子的数目) 来确定存储器单元的阈值电压。

[0010] 然而,在编程操作中,一些电子可能被俘获在隧道绝缘层 13 中而没有进入电荷俘获层 14。存储器单元的阈值电压可以通过俘获在隧道绝缘层 13 中的电子而改变。具体而言,随着编程、擦除和读取操作被重复执行,隧道绝缘层 13 的电特性逐步恶化。因而,隧道绝缘层 13 中俘获的电子数目可以根据半导体器件的操作次数的增加而增加。

发明内容

[0011] 根据示例性实施例,在编程操作中,编程电压和去俘获电压分别同时被供给到字线和阱,但是去俘获电压比编程电压供给更长的时间。因而,在隧道绝缘层中俘获的电子可以在编程操作中被去除。

[0012] 根据本发明一个方面,提供一种半导体器件的操作方法,包括:通过将编程电压供给到存储器单元的控制栅极和将去俘获电压供给到在半导体衬底内形成的阱来对所述存储器单元进行编程;以及随后在对编程的存储器单元进行验证之前,通过将低于所述去俘获电压的电压供给到所述控制栅极并且还将所述去俘获电压供给到所述阱,来去除俘获在所述存储器单元的隧道绝缘层中的电子。

[0013] 根据本发明另一方面的半导体器件的操作方法包括:通过将编程电压供给到选中的字线、将通过电压(pass voltage)供给到未选中的字线和将去俘获电压供给到阱来对选中的存储器单元进行编程,其中所述编程电压高于所述通过电压且所述通过电压高于所述去俘获电压;以及,随后在执行所述存储器单元的验证操作之前,将低于所述去俘获电压的电压供给到所述选中的字线和所述未选中的字线并且还将所述去俘获电压供给到所述阱。

[0014] 根据本发明又一方面的半导体器件包括:包括多个存储块的存储器单元阵列;电压供给电路,被配置成将编程电压供给到选中的字线、将通过电压供给到未选中的字线以及将去俘获电压供给到阱,其中所述编程电压高于所述通过电压,所述通过电压高于所述去俘获电压;以及控制电路,被配置成控制所述电压供给电路使得所述编程电压、所述通过电压和所述去俘获电压在编程操作中被分别供给到选中的字线、未选中的字线和阱,以及随后在编程验证操作之前,将低于所述去俘获电压的电压供给到所述选中的字线和所述未选中的字线,并且还将所述去俘获电压供给到阱。

附图说明

[0015] 图 1 是示出常规编程操作的特征的存储器单元的截面图;

[0016] 图 2 是示出根据本发明的一种编程方法的半导体器件的框图;

[0017] 图 3 是示出根据本发明的一种编程方法的时序图;以及

[0018] 图 4A 和 4B 是示出根据本发明的一种编程方法的特征的存储器单元的截面图。

具体实施方式

[0019] 下面将参照附图详细描述本发明的某些示例性实施例。提供附图是为了使本领域普通技术人员理解本发明实施例的范围。

[0020] 图 2 是示出根据本发明的编程方法的半导体器件的框图。

[0021] 参见图 2,半导体器件包括:存储器单元阵列 110;电路组(130、140、150、160、170 和 180),用于在存储器单元阵列 110 所包括的存储器单元上执行编程、读取或擦除操作;以及控制电路 120,用于控制电路组(130、140、150、160、170 和 180)以根据输入数据来设置存储器单元的阈值电压。

[0022] 例如,在 NAND 快闪存储器件中,电路组可以包括电压生成器 130、行译码器 140、页缓冲器组 150、列选择器 160、I/O(输入/输出)电路 170 和通过/失败(pass/fail)检查电路 180。

[0023] 存储器单元阵列 110 包括多个存储块。在图 2 中示出了存储块中的一个。存储块

包括共同耦接到阱 Well 的多个串 ST。一些串 ST 被指定为正常串,一些串 ST 被指定为标志串。串 ST 具有相同的结构。

[0024] 每个串 ST 包括:耦接到公共源级线 CSL 的源极选择晶体管 SST;多个存储器单元 F0 至 Fn;以及耦接到位线 BLe 和 BLo 的漏极选择晶体管 DST。标志串中所包括的存储器单元被称作标志单元,但是标志单元具有与包括在串 ST 中的其他存储器单元相同的结构。源极选择晶体管 SST 的栅极耦接到源极选择线 SSL,存储器单元 F0 至 Fn 的栅极耦接到各个字线 WL0 至 WLn,漏极选择晶体管 DST 的栅极耦接到漏极选择线 DSL。串 ST 耦接到相关的位线 BLe 和 BLo 并且耦接到公共源极线 CSL。

[0025] 控制电路 120 响应于命令信号 CMD 而在内部生成编程操作信号 PGM、读取操作信号 READ 或擦除操作信号 ERASE,并且还根据操作类型生成用于控制页缓冲器组 150 的页缓冲器的页缓冲器信号 PB SIGNALS。具体来说,在编程操作中,控制电路 120 分别同时向字线和阱供给编程电压和去俘获电压,但是去俘获电压比编程电压供给更长的时间。这里,向阱供给去俘获电压以朝着半导体衬底提取在存储器单元的隧道绝缘层中俘获的电子。

[0026] 此外,控制电路 120 响应于地址信号 ADD 产生行地址信号 RADD 和列地址信号 CADD。在编程或操作验证操作时,控制电路 120 还响应于由通过/失败检查电路 180 产生的检查信号 CS 来检查存储器单元的阈值电压是否升高到目标电平,并判断是否要再执行编程操作或擦除操作以及根据检查结果来判断编程操作或擦除操作是完成还是失败。

[0027] 电压供给电路 (130、140) 响应于控制电路 120 的信号 PGM、ERASE、READ 和 RADD 来将存储器单元的编程操作、读取操作或擦除操作所需的电压供给至存储块的漏极选择线 DSL、字线 WL0 至 WLn、源极选择线 SSL 以及阱。电压供给电路包括电压生成器 130 和行译码器 140。

[0028] 电压生成器 130 响应于控制电路 120 的操作信号 PGM、READ 和 ERASE (更具体来说,内部命令信号) 来将用于编程、读取或擦除存储器单元的操作电压输出至全局线。当对存储器单元进行编程时,电压生成器 130 向全局线供给用于编程的操作电压 (例如 Vpgm、Vpass、Vread 或 Vdet)。Vpgm 指编程电压、Vpass 指通过电压、Vread 指读取电压而 Vdet 指去俘获电压。

[0029] 行译码器 140 响应于控制电路 120 的行地址信号 RADD 将电压生成器 130 的操作电压传送至阱和存储块的局部线 DSL、SSL 以及 WL[n:0]。

[0030] 页缓冲器组 150 检测存储器单元的编程状态或擦除状态。页缓冲器组 150 包括耦接到位线 BLe 和 BLo 的页缓冲器,并响应于控制电路 120 的页缓冲器信号 PB SIGNALS 来向位线 BLe 和 BLo 供给在存储器单元 F0 至 Fn 中存储数据所需的电压。

[0031] 更具体而言,在存储器单元 F0 至 Fn 的编程操作、擦除操作或读取操作中,页缓冲器组 150 预充电位线 BLe 和 BLo 或者锁存对应于根据位线 BLe 和 BLo 的电压移动而检测到的存储器单元 F0 至 Fn 的阈值电压的数据。更具体而言,在编程操作中,页缓冲器组 150 根据锁存的数据将编程允许电压 (例如,接地电压) 或编程禁止电压 (例如,Vcc) 供给到位线 BLe 或 BLo。在读取操作中,页缓冲器组 150 根据存储在存储器单元 F0 至 Fn 的数据来控制位线 BLe 至 BLo 的电压,并检测存储器单元 F0 至 Fn 中存储的数据。此外,页缓冲器组 150 在擦除操作的早期阶段将擦除允许电压 (例如,Vcc) 供给到位线 BLe 和 BLo,并将编程允许电压 (例如,接地电压) 供给到与在编程操作中根据擦除验证结果而被擦除的串 ST 耦接的

位线 BLe 和 BLo。

[0032] 列选择器 160 响应于控制电路 120 的列地址信号 CADD 来选择页缓冲器组 150 的页缓冲器。在通过列选择器 160 选择的页缓冲器中锁存的数据被输出。此外,列选择器 160 经由列线 CL 接收从页缓冲器组 150 输出的数据并将所述数据传送到通过 / 失败检查电路 180。

[0033] 在编程操作中,I/O 电路 170 在控制电路 120 的控制之下将外部数据 DATA 传送到列选择器 160,以将数据 DATA 输入到页缓冲器组 150 的页缓冲器。当列选择器 160 将数据 DATA 顺序地传送至页缓冲器组 150 的页缓冲器时,页缓冲器将数据 DATA 存储在锁存器中。此外,在读取操作中,I/O 电路 170 经由列选择器 160 将从页缓冲器组 150 的页缓冲器接收的数据 DATA 输出到外部。

[0034] 在编程操作或擦除操作之后执行的验证操作期间,通过 / 失败检查电路 180 检查是否出现错误单元,并以检查信号 PFC 的形式输出验证操作的结果。通过 / 失败检查电路 180 还对错误单元的数目进行计数,并以计数信号 CS 的形式输出对错误单元进行计数的结果。

[0035] 在编程验证操作中,控制电路 120 控制在存储器单元的编程操作中供给到字线的编程电压的电平并控制电压发生器 130 使得可以选择性地将验证电压供给到字线。在一些实施例中,控制电路 120 可以根据通过 / 失败检查电路 180 的检查信号 CS 来控制电压生成器 130。

[0036] 以下描述使用上述半导体器件的存储器单元的编程方法。

[0037] 图 3 是示出根据本发明的一种编程方法的时序图。

[0038] 以下参考图 3 和图 2 来描述编程方法。

[0039] 1.编程时段

[0040] 当编程时段开始时,在编程允许电压(例如,接地电压)已经供给到选中的位线且编程禁止电压(例如,Vcc)已经供给到未选中位线的状态下,编程电压 Vpgm、通过电压 Vpass 以及去俘获电压 Vdet 分别同时供给到选中的字线 Sel_WL(更具体而言,字线 WL0 至 WLn 中的任意一个)、未选中的字线 Unsel_WL(更具体而言,除了选中字线以外的剩余字线)以及阱(图 4A 的阱)。

[0041] 编程电压 Vpgm 是用于对选中的存储器单元进行编程的电压,通过电压 Vpass 是用于在串 ST 中形成沟道的电压,而去俘获电压 Vdet 是用于去除在选中的存储器单元的除了电荷俘获层(例如,浮置栅极)以外的区域中俘获的电子的电压。在编程时段中,去俘获电压 Vdet 与对选中字线 Sel_WL 供给的编程电压 Vpgm 同时地供给到阱 Well,使得在随后的去俘获时段内被俘获的电子可以被容易地去除,而不是在编程时段内去除俘获的电子。作为一个防止编程效率被在编程时段内供给到阱 Well 的去俘获电压 Vdet 恶化的例子,编程电压 Vpgm 和通过电压 Vpass 可以升高去俘获电压 Vdet。

[0042] 具体来说,为了维持俘获在存储器单元的电荷俘获层中的电子,而不是选择性地去去除在编程操作中在除了电荷俘获层以外的区域(更具体而言,隧道绝缘层)中俘获的电子,去俘获电压 Vdet 具有低于通过电压 Vpass 的正电压。例如,去俘获电压 Vdet 可以是 0.1V 至 0.5V。在这个例子中,与没有施加去俘获电压时的编程电压 Vpgm 和通过电压 Vpass 相比,编程电压 Vpgm 和通过电压 Vpass 的每个可以升高 0.1V 至 0.5V。因而,在编程时段

中,存储器单元被编程而没有编程效率的减少。更具体而言,电子被俘获在存储器单元的电荷俘获层(图 1A 的 104)中,因此存储器单元被编程。通过施加编程电压 V_{pgm} 和通过电压 V_{pass} 至存储器单元,一些电子也被俘获在存储器单元的隧道绝缘层(图 4A 的 103)中。

[0043] 此外,在图 3 的编程时段内,当将去俘获电压 V_{det} 供给到阱 $We11$ 时,编程电压 V_{pgm} 和通过电压 V_{pass} 分别同时被供给到选中的字线 $Se1_WL$ 和未选中的字线 $Unsel_WL$ 。然而,在去俘获电压 V_{det} 已经供给到阱 $We11$ 的状态中,分别供给编程电压 V_{pgm} 和通过电压 V_{pass} 到选中的字线 $Se1_WL$ 和未选中的字线 $Unsel_WL$ 的方法可以根据编程方法而以各种方式来改变。例如,当去俘获电压 V_{det} 被供给到阱 $We11$ 时,通过电压 V_{pass} 可以同时供给到选中的字线 $Se1_WL$ 和未选中的字线 $Unsel_WL$,随后选中的字线 $Se1_WL$ 的电压可以增加到编程电压 V_{pgm} 。

[0044] 2. 去俘获时段

[0045] 当去俘获时段在编程时段之后开始时,编程电压 V_{pgm} 和通过电压 V_{pass} 不再分别被施加到字线 $Se1_WL$ 和字线 $Unsel_WL$,但是去俘获电压 V_{det} 仍然施加到阱 $We11$ 。更具体而言,如果去俘获电压 V_{det} 在字线 $Se1_WL$ 和字线 $Unsel_WL$ 的所有电压变为低于去俘获电压 V_{det} 的状态下继续施加到阱,在存储器单元的隧道绝缘层 103 中俘获的电子离开并进入阱 $We11$ (更具体而言,半导体衬底 101)中。因而,在引入到存储器单元中的电子中的被俘获在隧道绝缘层 103 中的电子可以被选择性地去除。然而,被俘获在存储器单元的电荷俘获层 104 中的电子可以保持不变,因为去俘获电压 V_{det} 具有例如 0.1V 至 0.5V 的低电压。

[0046] 在去俘获时段结束后,阱的电压降低到接地电压,且执行选中的存储器单元的验证操作(更具体而言,验证时段)。

[0047] 与本实施例的编程方法不同,在提供编程电压 V_{pgm} 时,可以不供给去俘获电压 V_{det} 至阱 $We11$,而是可以在编程电压 V_{pgm} 停止供给时供给。在这个例子中,执行编程操作所花费的时间增加。为此,如图 3 所示,去俘获电压 V_{det} 与编程电压 V_{pgm} 同时供给,但是去俘获电压 V_{det} 比编程电压 V_{pgm} 供给更长的时间。在这个实施例中,可以在较短的时间内执行去俘获操作。

[0048] 图 4A 和 4B 是用于说明根据本发明的所述编程方法的效果的存储器单元的横截面图。

[0049] 在图 4A 中示出了 NAND 存储器单元的基本结构。NAND 存储器单元包括顺序层叠在形成阱 $We11$ 中的半导体衬底 101 之上的隧道绝缘层 103、电荷俘获层 104、电介质层 105 以及控制栅极 106。结 102(更具体来说,源极和漏极)形成在存储器单元两侧上的半导体衬底 101 中。

[0050] 隧道绝缘层 103 可以由氧化物层形成。电荷俘获层 104 和控制栅极 106 可以由导电层形成(例如,多晶硅层)。电介质层 105 可以由高电介质层形成,或者由包括氧化物层、氮化物层和氧化物层的层叠结构形成。电荷俘获层 104 也被称作浮置栅极。控制栅极 106 耦接到字线 WL ,且隧道绝缘层 103 的一部分与阱 $We11$ 相邻。在图 3 的编程时段中,当将编程电压 V_{pgm} 供给到选中的字线 $Se1_WL$ 时,阱 $We11$ 中包括的电子中的一些通过 FN 隧穿而隧穿过隧道绝缘层 103,然后隧穿电子被俘获在电荷俘获层 104 中。在这个例子中,一些电子没有从隧道绝缘层 103 移动到电荷俘获层 104,而被俘获在隧穿绝缘层 103 中。

[0051] 参见图 4B 和图 3,在去俘获时段中,所有的字线 $Se1_WL$ 和 $Unsel_WL$ 的电压都小

于去俘获电压 V_{det} , 且俘获电压 V_{det} 继续供给到阱 Well。因此, 在隧道绝缘层 103 中俘获的电子可以选择性地离开而进入半导体衬底 101。更具体来说, 在去俘获阶段, 在浮置栅极 104 中俘获的电子保持不变, 在隧道绝缘层 103 中俘获的电子可以选择性地离开而进入半导体衬底 101。

[0052] 在本发明中, 将 NAND 存储器单元作为示例进行描述。然而, 上述的供给去俘获电压 V_{det} 的编程操作也可以应用于其他存储器单元结构, 例如 SONOS 结构。因而, 在编程操作之后的编程验证操作或读取操作中, 可以基于例如俘获在电荷俘获层 104 中的电子来确定存储器单元是否被编程。因而, 半导体器件可以更为可靠。

[0053] 如上所述, 在编程操作中, 将编程电压和去俘获电压分别同时供给到选中的字线和阱, 而去俘获电压比编程电压供给更长的时间。因而, 可以在较短时间内去除隧道绝缘层中俘获的电子。此外, 由于去除了在隧道绝缘层中俘获的电子, 编程、读取和擦除操作可以更为可靠。

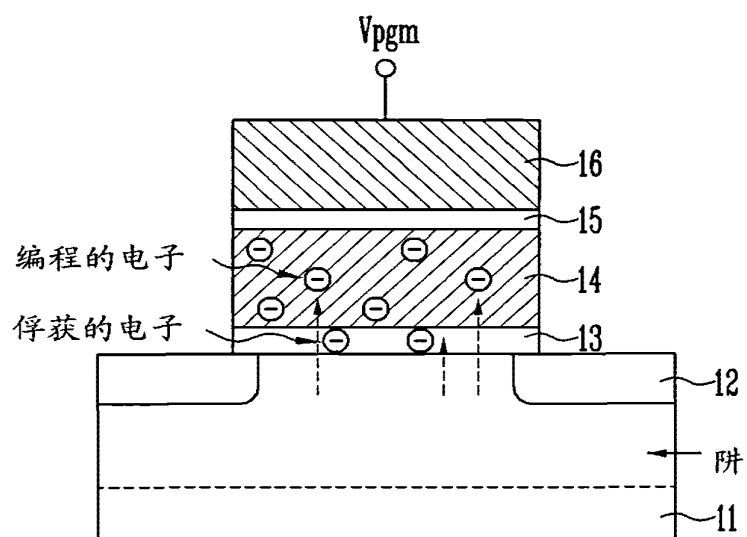


图 1

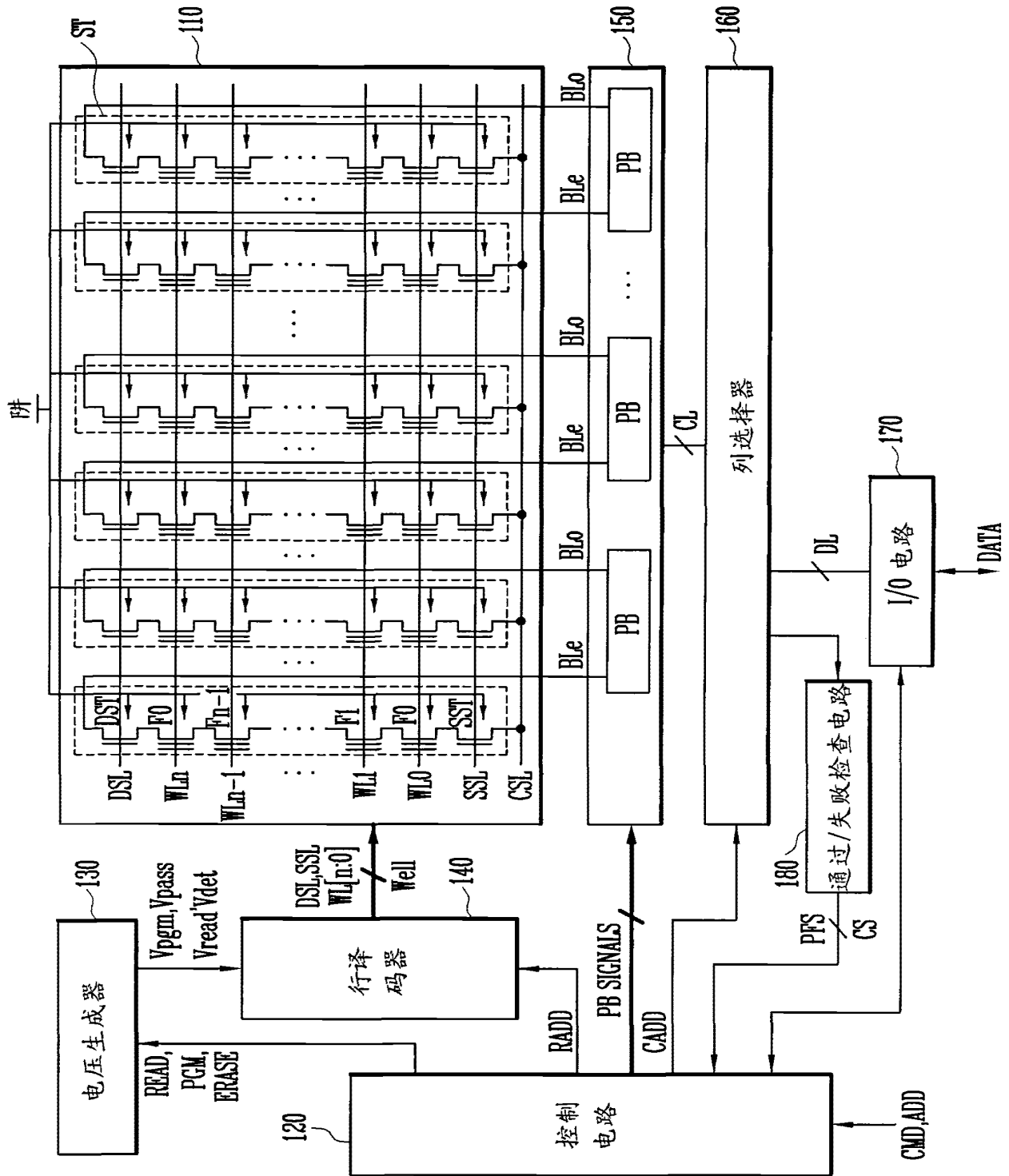


图 2

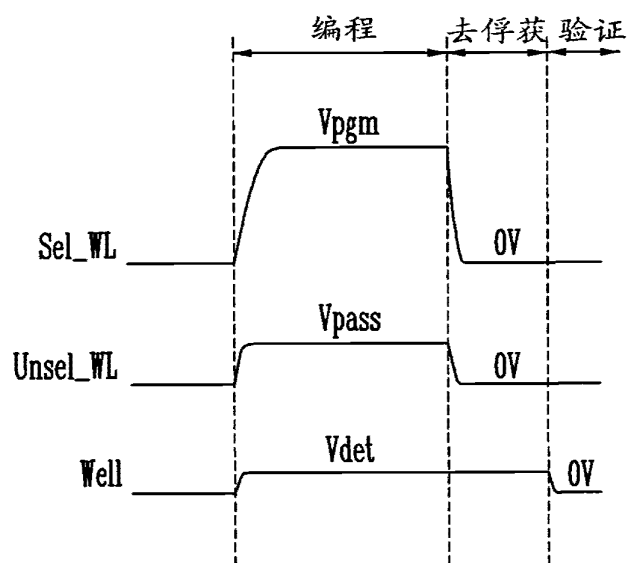


图 3

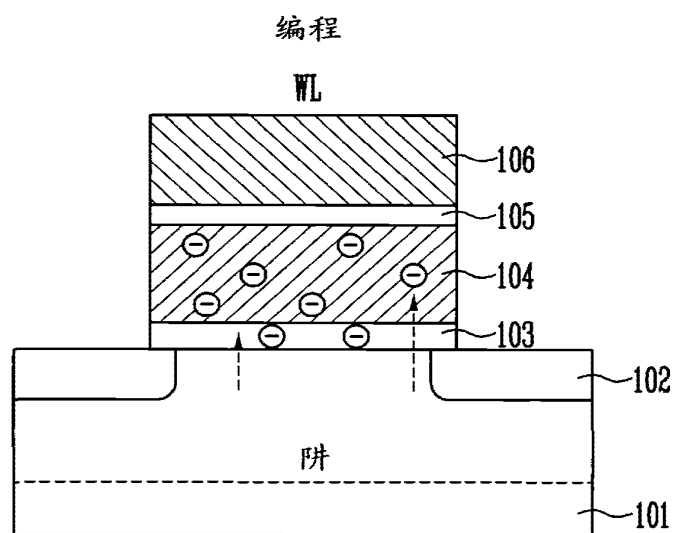


图 4A

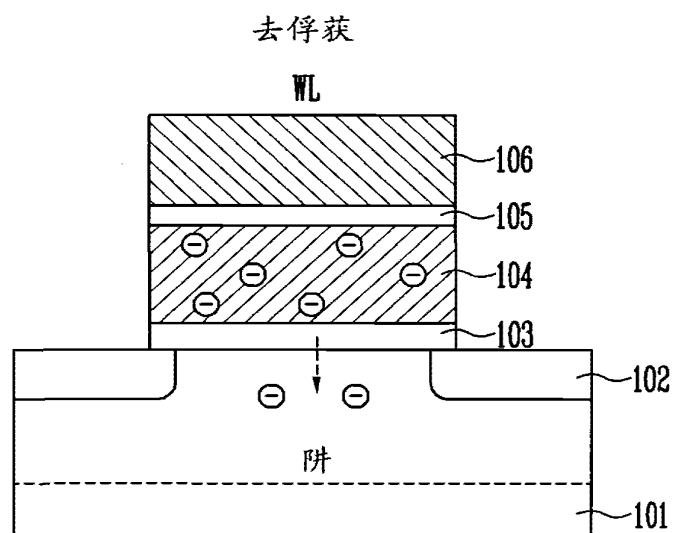


图 4B



(21)申请号 201680057342.4

(74)专利代理机构 北京市柳沈律师事务所
11105

(22)申请日 2016.07.27

代理人 孙瑞

(30)优先权数据

62/235,322 2015.09.30 US

15/220,375 2016.07.26 US

(85)PCT国际申请进入国家阶段日

2018.03.30

(51)Int.Cl.

G11C 16/04(2006.01)

G11C 11/34(2006.01)

G11C 16/06(2006.01)

H01L 29/792(2006.01)

(86)PCT国际申请的申请数据

PCT/US2016/044336 2016.07.27

(87)PCT国际申请的公布数据

W02017/058347 EN 2017.04.06

(71)申请人 日升存储公司

地址 美国加利福尼亚州

(72)发明人 E.哈拉里

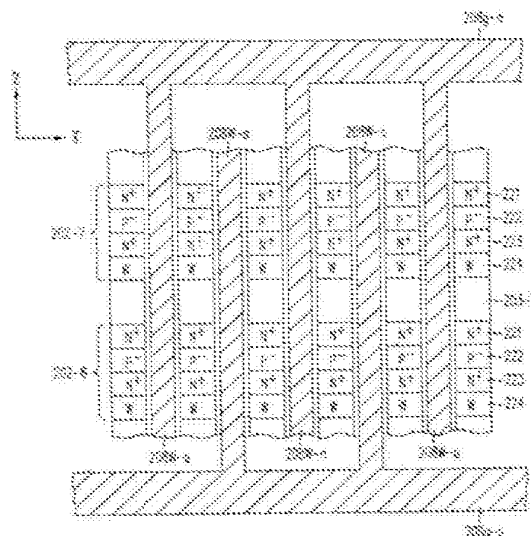
权利要求书5页 说明书15页 附图17页

(54)发明名称

布置在具有垂直控制栅极的堆叠的水平有源带中的多栅极NOR闪存薄膜晶体管串

(57)摘要

多栅极NOR闪存薄膜晶体管(TFT)串阵列(“多栅极NOR串阵列”)被组织为与硅衬底的表面平行延伸的水平有源带堆,其中每堆中的TFT由沿着有源带堆的一个或两个侧壁设置的垂直局部字线控制。每个有源带至少包括在两个共享源极或漏极层之间形成的沟道层。有源带的TFT中的数据存储器由设置在有源带和由相邻局部字线提供的控制栅极之间的电荷存储元件提供。取决于是否使用有源带的一侧或两侧,每个有源带可以提供属于一个或两个NOR串的TFT。



1. 一种存储器结构,包括:

具有基本平坦表面的半导体衬底;

在所述半导体衬底的表面上形成并且分开预定距离的第一堆有源带和第二堆有源带,其中,每堆有源带包括在两个或更多个隔离平面上一个设置在另一个的顶部之上并且沿着基本上平行于所述平坦表面的第一方向基本上彼此纵向对齐的两个或更多个有源带,并且其中,每个有源带包括设置在各具有第二导电类型的第二和第三半导体层之间的具有第一导电类型的第一半导体层;

电荷俘获材料;以及

多个导体,每个设置在所述第一堆有源带和所述第二堆有源带之间,其中,每个导体通过所述电荷俘获材料与每堆有源带分开,并且在基本上垂直于所述平坦表面的第二方向上纵向延伸。

2. 根据权利要求1所述的存储器结构,其中,所述第一、第二和第三半导体层每个包括多晶硅。

3. 根据权利要求1所述的存储器结构,其中,所述第一半导体层是P-掺杂多晶硅,并且所述第二和第三半导体层是N⁺掺杂多晶硅。

4. 根据权利要求1所述的存储器结构,其中,所述导体包含多晶硅。

5. 根据权利要求1所述的存储器结构,其中,所述导体包括N⁺掺杂多晶硅、P⁺掺杂多晶硅、和相对于二氧化硅具有高功函数的难熔金属之一。

6. 根据权利要求1所述的存储器结构,其中,每个有源带还包括与所述第二半导体层接触并且与所述第二半导体层基本上纵向对齐的金属层。

7. 根据权利要求1所述的存储器结构,其中,所述电荷俘获材料包括一层或多层氮化硅。

8. 根据权利要求7所述的存储器结构,其中,每层氮化硅设置在氧化硅层之间。

9. 根据权利要求1所述的存储器结构,其中,对于每个导体,当相对于所述第二和第三半导体层之一向所述导体施加超过预定值的电压时,与所述导体相邻的电荷俘获材料积聚电荷。

10. 根据权利要求1所述的存储器结构,其中,每个导体、邻近所述导体的电荷俘获材料、以及所述第一、第二和第三半导体层形成存储元件。

11. 根据权利要求10所述的存储器结构,其中,所述存储元件包括存储晶体管,其中所述导体用作所述存储晶体管的栅极端子,并且所述第一、第二和第三半导体层分别形成所述存储晶体管的沟道、源极和漏极端子。

12. 根据权利要求11所述的存储器结构,其中,所述存储晶体管中的两个或更多个沿所述第一方向并排定位。

13. 根据权利要求12所述的存储器结构,其中,所述存储晶体管中的两个或更多个沿着所述第一方向沿着每个所述有源带的两个侧边缘形成。

14. 根据权利要求11所述的存储器结构,其中,每个有源带的存储晶体管共享公共源极和漏极端子,但是每个存储晶体管存储所述沟道和导体之间的电荷。

15. 根据权利要求11所述的存储器结构,其中,每个存储晶体管具有原生增强阈值电压。

16. 根据权利要求11所述的存储器结构,其中,每个导体用作所述第一堆有源带中的存储晶体管之一的栅极端子和所述第二堆有源带中的存储晶体管之一的栅极端子。

17. 根据权利要求10所述的存储器结构,还包括:

形成在所述半导体衬底的平坦表面中和其上的电路;以及

一组或多组导电布线,每个导电布线沿平行于所述平坦表面的第三方向延伸,每个导电布线将所述电路连接到一个或多个存储元件的导体。

18. 根据权利要求17所述的存储器结构,其中,所述第三方向基本垂直于所述第一方向。

19. 根据权利要求17所述的存储器结构,其中,第一组导电布线设置在所述第一和第二堆有源带两者上方与平坦表面基本平行的层中。

20. 根据权利要求17所述的存储器结构,其中,第二组导电布线设置在与所述半导体衬底和所述第一和第二堆有源带的每个之间的平坦表面基本平行的层中。

21. 根据权利要求17所述的存储器结构,其中,所述存储元件每个被分配数字地址,其中,分配有偶数地址的存储元件通过所述第一组导电布线连接,并且其中,分配有奇数地址的存储元件通过所述第二组导电布线连接。

22. 根据权利要求17所述的存储器结构,其中,所述电路应用电压配置之一以使选定的一个或多个存储元件在预定时间段提供与每个存储元件相关的第二和第三半导体层之间的电流路径,从而将所述第三半导体层的寄生电容预充电至若干预定电压中选定的一个,选定的预定电压被选择用于以下之一:编程、编程抑制、读取和擦除所述存储元件的数据。

23. 根据权利要求17所述的存储器结构,其中,提供电触点以将所述电路分别连接到所述导体以及每个有源带的第一、第二和第三半导体层中的一个或多个。

24. 根据权利要求23所述的存储器结构,其中,存储在每个存储元件中的电荷俘获材料中的电荷表示存储在所述存储元件中的数据,其中,所述电路包括用于提供将被施加在每个存储元件上的多个电压配置的电压源,从而实现对编程充电、编程抑制充电、读取或擦除存储在所述存储元件中的数据。

25. 根据权利要求24所述的存储器结构,其中,所述数据表示存储在每个存储元件上的多于一位的二进制信息。

26. 根据权利要求24所述的存储器结构,其中,所述数据表示模拟存储器中的连续的存储状态。

27. 根据权利要求24所述的存储器结构,其中,所述电路进一步包括用于感测存储在所述存储元件中的数据的一个或多个感测放大器。

28. 根据权利要求24所述的存储器结构,其中,与每个有源带相关的存储元件被组织成一个或多个NOR串。

29. 根据权利要求24所述的存储器结构,其中,沿着所述第一方向与所述有源带的一侧相关的存储元件被组织成第一NOR串,并且其中,沿着所述第一方向与所述有源带的另一侧相关的存储元件被组织成第二NOR串。

30. 根据权利要求29所述的存储器结构,其中,在读取或编程操作期间,仅将与NOR串的寻址的存储元件相关的导体瞬时升高至读取或编程操作所需的预定电压,与所述NOR串的所有其它存储元件相关的导体保持在低于擦除的存储元件的阈值电压的电压。

31. 根据权利要求30所述的存储器结构,其中,在与寻址的存储元件相关的平面以外的一个或多个平面上的有源带使其第二或第三半导体层浮置或预充电到抑制电压。

32. 根据权利要求30所述的存储器结构,其中,与在多于一个平面上的有源带相关的存储元件在单个同时编程操作中被编程。

33. 根据权利要求32所述的存储器结构,其中,在所述同时编程操作期间,在每个平面中的每个有源带的第二或第三半导体层被适当地预充电到与编程或编程抑制操作相关的预定电压,编程电压然后施加到一个或多个寻址的导体,并且其中,所述并行编程操作在与寻址的导体相关的所有存储元件被验证为已经达到它们各自的预期状态之后终止。

34. 根据权利要求33所述的存储器结构,其中,所述编程电压为编程序列中的若干编程电压之一,每个编程电压表示不同的数据值。

35. 根据权利要求30所述的存储器结构,其中,在执行在一个或多个平面中的寻址的存储元件的一个或多个读取操作之前,将一个或多个平面中的每个有源带的第二或第三半导体层适当地同时预充电到与读取操作相关的预定电压,而所述第二或第三半导体层借助沿着其相关有源带的电容保持所述预定电压。

36. 根据权利要求35所述的存储器结构,其中,一个或多个平面上的有源带的预定电压用作彼此隔离的虚拟接地电压源,从而当寻址的存储元件被同时读取时避免接地反弹。

37. 根据权利要求10所述的存储器结构,其中,所述存储元件在以分钟、小时或天数测量的时间之后丢失所述电荷的预定部分,并且其中,在时间间隔之间对于每个存储元件读取和刷新电荷,所述时间间隔具有比对于存储的存储器状态被损坏的时间更短的持续时间。

38. 根据权利要求9所述的存储器结构,其中,所述电荷通过福勒-诺德海姆隧穿机制从所述第一、第二和第三半导体层之一提供。

39. 根据权利要求9所述的存储器结构,其中,所述电荷通过沟道热电子机制从所述第一、第二和第三半导体层之一提供。

40. 一种半导体制造方法,包括:

提供半导体衬底并在其中和其上形成电路;

在所述半导体衬底上提供多个有源层和埋设触点,每个有源层包括在具有第二电导率的第二和第三半导体层之间的具有第一电导率的第一半导体层,其中,每个有源层与下部有源层或所述半导体衬底通过电介质层电隔离,除了在所述埋设触点处之外,其中,所述埋设触点将每个有源层的第二或第三半导体层中的一个或多个连接到所述半导体衬底的电路;

图案化并各向异性地蚀刻多个有源层,以提供具有在第一方向上纵向延伸的侧壁的第一组沟槽,所述第一方向沿着第一方向基本平行于所述半导体衬底的表面;

在所述沟槽的侧壁上共形地提供电荷俘获材料;

用导电材料填充所述沟槽;并且

图案化并蚀刻所述导电材料的一部分,使得剩余的导电材料形成多个导体,所述多个导体沿基本上垂直于所述半导体衬底的表面的第二方向纵向延伸;并且

除了在所述导体处和暴露的并且连接到所述半导体衬底中的电路的多个触点处之外,在所述有源层上提供电介质材料层;以及

提供连接所述导体和暴露的触点的导电布线。

41. 根据权利要求40所述的方法, 其中, 所述第一、第二和第三半导体层每个包括多晶硅。

42. 根据权利要求41所述的方法, 其中, 每个有源层的第二和第三半导体层中的一个或两者被原位掺杂以具有所述第二电导率。

43. 根据权利要求40所述的方法, 其中, 每个有源层的第一半导体层被离子注入以具有所述第一电导率。

44. 根据权利要求43所述的方法, 其中, 提供单个热激活步骤以激活所有有源层中的注入物质。

45. 根据权利要求43所述的方法, 其中, 所述热激活步骤包括快速热退火。

46. 根据权利要求40所述的方法, 其中, 所述导体包括原位掺杂的 N^+ 多晶硅或 P^+ 掺杂多晶硅。

47. 根据权利要求40所述的方法, 其中, 提供所述有源层还包括提供与所述第二半导体层接触的金属层。

48. 根据权利要求40所述的方法, 其中, 所述电荷俘获材料包括一层或多层氮化硅。

49. 根据权利要求48所述的方法, 其中, 每层氮化硅设置在包括氧化硅、氧化铝或氧化钪的其他电介质层之间。

50. 根据权利要求40所述的方法, 还包括提供第二组导电布线, 所述第二组导电布线包括与所述导体重合的触点, 其中, 所述图案化和蚀刻所述沟槽的步骤暴露所述触点, 使得当所述导体形成时实现到导体的电连接。

51. 根据权利要求40所述的方法, 其中, 所述电荷俘获材料被提供为具有一厚度, 使得当对所述导体和第一、第二和第三半导体层施加超过预定值的电压时来自所述第一、第二和第三半导体层的电子通过福勒-诺德海姆隧穿机制隧穿到所述电荷俘获材料中。

52. 根据权利要求40所述的方法, 其中, 所述电荷俘获材料被提供为具有一厚度, 使得当对所述导体和第二和第三半导体层之一施加超过预定值的电压时来自所述第二和第三半导体层之一的电子通过沟道热电子注入机制隧穿到所述沟道上的电荷俘获材料中。

53. 一种在半导体衬底的平坦表面上形成的NOR串阵列, 包括第一NOR串和第二NOR串, 每个NOR串包括薄膜存储晶体管, 薄膜存储晶体管沿着平行于所述平坦表面的第一方向沿着纵向延伸的有源带形成, 其中, 每个NOR串中的薄膜存储晶体管共享公共漏极端子和公共源极端子, 并且其中, 所述第一NOR串的每个存储晶体管通过沿着垂直于所述平坦表面的第二方向纵向延伸的导体电连接到所述第二NOR串的对应的存储晶体管。

54. 根据权利要求53所述的NOR串阵列, 其中, 所述第一NOR串的有源带和所述第二NOR串的有源带均形成在平行于所述平坦表面的平面上。

55. 根据权利要求53所述的NOR串阵列, 还包括第三NOR串, 其中, 所述第一NOR串和所述第三NOR串形成在平行于所述平坦表面的平面上, 其中, 所述第三NOR串上的一个或多个存储晶体管被编程以具有参考阈值电压, 所述参考阈值电压在编程或读取操作期间与所述第一NOR串中的存储晶体管的阈值电压进行比较。

56. 根据权利要求53所述的NOR串阵列, 其中, 所述第一NOR串和所述第二NOR串分别形成在平行于所述平坦表面的第一和第二平面上, 所述NOR串阵列在所述第一和第二平面中

的每个上还包括一个或多个参考NOR串,其中,对于每个参考NOR串,每个参考NOR串上的一个或多个存储晶体管被编程以具有参考阈值电压,所述参考阈值电压在编程或读取操作期间在与所述参考NOR串相同的平面上的第一和第二NOR串之一中的存储晶体管的阈值电压进行比较。

57. 根据权利要求55所述的NOR串阵列,其中,在读取所述第一NOR串中的存储晶体管期间,所述第三NOR串提供参考串泄漏电流源,其中所述第三NOR串的所有存储晶体管处于断开状态。

58. 根据权利要求56所述的NOR串阵列,其中,当所述第一NOR串的存储晶体管用作多位层级单元时,所述多位层级的每个状态存储在单独的参考NOR串中。

布置在具有垂直控制栅极的堆叠的水平有源带中的多栅极 NOR闪存薄膜晶体管串

[0001] 相关申请的交叉引用

[0002] 本申请涉及并要求2015年9月30日提交的标题为“布置在具有垂直控制栅极的堆叠的水平有源带中的多栅极NOR闪存薄膜晶体管串”的美国临时专利申请(临时专利申请案)序列号62/235322的优先权。该临时专利申请通过引用整体并入本文。

技术领域

[0003] 本发明涉及高密度存储器结构。特别地,本发明涉及由互连的薄膜存储元件(比如薄膜存储晶体管)形成的高密度存储器结构。

背景技术

[0004] 在本公开中,描述了存储器电路结构。可以使用常规制造方法在平面半导体衬底(例如硅晶片)上制造这些结构。为了在本说明书中清晰起见,术语“垂直”是指垂直于半导体衬底表面的方向,术语“水平”是指平行于该半导体衬底表面的任何方向。

[0005] 现有技术中已知许多高密度非易失性存储器结构,有时称为“三维垂直NAND串”。这些高密度存储器结构中的许多是使用由沉积的薄膜(例如多晶硅薄膜)形成的薄膜存储晶体管形成的,并且被组织为“存储器串”的阵列。一种类型的存储器串被称为NAND存储器串或简称为“NAND串”。NAND串由多个串联连接的存储晶体管(“TFT”)组成。读取或编程任何串联连接的TFT需要激活NAND串中的所有串联连接的TFT。在这种NAND布置下,未被读取或编程的激活的TFT可能会遇到不希望的编程干扰或读取干扰条件。此外,由多晶硅薄膜形成的TFT具有比在单晶硅衬底中形成的常规晶体管低得多的沟道迁移率—因此具有更高的电阻率。NAND串中较高的串联电阻将串中的TFT的数量实际上限制为不超过64或128个TFT。需要通过长NAND串而被传导的低读取电流会导致较长的延迟。

[0006] 另一种类型的高密度存储器结构被称为NOR存储器串或“NOR串”。NOR串包括多个存储晶体管,每个连接到共享源极区域和共享漏极区域。因此,NOR串中的晶体管并联连接,使得NOR串中的读取电流在比通过NAND串的读取电流小得多的电阻上传导。目前,本发明人并不知道现有技术中由TFT形成的任何NOR串。为了读取或编程NOR串中的存储晶体管,仅需要激活该存储晶体管(即“开通”或导通),NOR串中的所有其他存储晶体管保持休眠(即“关断”或不导通)。因此,NOR串允许更快地感测要被读取的激活的存储晶体管,并避免未被读取或编程的NOR串的其他存储晶体管中的编程干扰或读取干扰条件。

[0007] 例如,在2013年1月30日提交并于2014年11月4日发布的Alsmeier等人(“Alsmeier”)的标题为“紧凑型三维垂直NAND及其制造方法”的美国专利8878278中公开了三维存储器结构。Alsmeier公开了各种类型的高密度NAND存储器结构,比如“兆兆位单晶片阵列晶体管”(TCAT) NAND阵列(图1A)、“管形位成本可扩展”(P-BiCS) 闪存(图1B)和“垂直NAND”存储器串结构。同样,2002年12月31日提交并且于2006年2月28日发布的标题为“制造包含串联连接的晶体管串的可编程存储器阵列结构的方法”的Walker等人(“Walker I”)的

美国专利7005350也公开了许多三维高密度NAND存储器结构。

[0008] 2005年8月3日提交并且于2009年11月3日发布的标题为“双栅极器件及方法”的Walker (“Walker II”)的美国专利7612411公开了一种“双栅极”存储器结构,其中公共有源区在形成于公共有源区的相对侧上的两个NAND串中提供独立控制的存储元件。

[0009] 2001年8月24日提交并且于2004年6月1日发布的标题为“具有靠近垂直体的水平栅极层的浮置栅晶体管”的Forbes (“Forbes”)的美国专利6744094公开了具有带有相邻平行水平栅极层的垂直体晶体管的存储器结构。

[0010] 2000年8月14日提交并于2003年6月17日发布的标题为“具有垂直沟道电流的多栅极半导体器件及制造方法”的Cleaves等人的美国专利6580124公开了一种具有沿着晶体管的垂直表面形成的两个或四个电荷存储介质的多位存储器晶体管。

[0011] 包括由垂直多晶硅栅极控制的水平NAND串的三维存储器结构在由W.Kim等人发表在2009超大规模集成电路技术会议,技术论文文摘,第188-189页上的文章“对于兆兆位密度存储的克服堆叠限制的多层垂直栅极NAND闪存”(“Kim”)中披露。也包括具有垂直多晶硅栅极的水平NAND串的另一种三维存储器结构在由HT Lue等人发表在2010超大规模集成电路技术会议,技术论文文摘,第131-132页上的文章“使用自由接点埋设沟道BF SONOS装置的高度可扩展8层三维垂直栅极(VG)TFT NAND闪存”中披露。

[0012] 在这里讨论的存储器结构中,存储的信息由存储的电荷表示,其可以通过使用各种技术中的任何一种而被引入。例如,1996年7月23日提交并于1998年6月16日发布的标题为“利用不对称电荷俘获的非易失性半导体存储器单元”的Eitan的美国专利5768192公开了基于“热电子沟道注入”技术的NR0M型存储晶体管操作。其他技术包括在TFT NAND串中使用的福勒-诺德海姆(Fowler-Nordheim)隧穿、以及直接隧穿,这两者对于本领域普通技术人员来说都是已知的。

发明内容

[0013] 根据本发明的一实施例,多栅极NOR闪存薄膜晶体管(TFT)串阵列(“多栅极NOR串阵列”)被组织为与硅衬底的表面平行延伸的水平有源带堆,其中每堆中的TFT由沿着有源带堆的一个或两个侧壁设置的垂直局部字线控制。每个有源带至少包括在两个共享源极或漏极层之间形成的沟道层。有源带的TFT中的数据存储由设置在有源带和由相邻局部字线提供的控制栅极之间的电荷存储元件提供。取决于是否使用有源带的一侧或两侧,每个有源带可以提供属于一个或两个NOR串的TFT。

[0014] 在一实施例中,有源带中的共享源极层或漏极层中的仅一个连接到电源电压,而另一源极或漏极层保持在由沉积在源极或漏极层中的电荷量确定的电压。在读取、写入或擦除操作之前,不被激活的TFT起到带电容器的作用,其中一个板是源极或漏极层本身,而另一个板是NOR串中的控制栅电极,其被参考到地面参考。带电容器上的电荷由一个或多个预充电TFT提供,所述TFT被瞬时激活以将电荷从连接到所接触的源极或漏极层的电源电压转移到带电容器。

[0015] 在一实施例中,TFT形成在每个有源带的两个垂直侧边缘上,使得垂直局部字线可以沿有源带的两个垂直侧边缘提供。在该实施例中,双密度通过使得沿着有源带的垂直边缘之一的局部字线与设置在有源带之上的水平全局字线接触而实现,而沿着有源带的另一

垂直边缘的局部字线通过设置在有源带下方的水平全局字线接触。所有全局字线可以在垂直于相应源带的方向的方向上延伸。通过在每个TFT中存储多于一位的数据可以实现甚至更大的存储密度。

[0016] 将TFT组织成NOR串而不是现有技术的NAND串—导致(i)接近动态随机存取存储器(DRAM)阵列的降低的读取延迟,(ii)降低对与长NAND串相关的读取干扰和程序干扰条件的敏感度,以及(iii)相对于平坦NAND或3D NAND阵列的降低的功耗和更低的成本。

[0017] 根据本发明的一个实施例,可以通过在块内提供电可编程参考串来补偿NOR串的块内的阈值电压的变化。通过比较正被读取的TFT的感测结果和参考NOR串上的同时读取的TFT的感测结果,可以基本上消除由于多栅极NOR串固有的后台泄漏电流引起的对读取操作的影响。在其他实施例中,每个TFT的电荷存储元件可以使其结构被修改以提供高写入/擦除周期耐久性,尽管需要更新的保留时间较短。然而,由于需要比常规动态随机存取存储器(DRAM)电路显著更少频率的刷新,所以本发明的NOR串阵列可以在一些DRAM应用中操作。与常规DRAM相比,NOR串的这种使用允许显著更低的位成本(cost-per-bit)品质因数,以及常规NAND串阵列相比显著更低的读取延迟。

[0018] 结合附图考虑下面的详细描述,可以更好地理解本发明。

附图说明

[0019] 图1a示出了概念化存储器结构100,其说明了根据本发明一个实施例的存储器单元的组织。

[0020] 图1b示出了根据本发明一个实施例的共享公共垂直字线的两堆NOR串的基本电路表示。

[0021] 图1c示出了在概念化存储器结构100的YZ平面横截面中的四个NOR串的堆的基本电路表示。

[0022] 图2a示出了根据本发明一个实施例的在半导体衬底201上形成有源层202-0至202-7之后但在形成各个有源带之前的在存储器结构200的YZ平面中的横截面。

[0023] 图2b-1示出了根据本发明一个实施例的结构220a,其可以用于实现图2a的有源层202-0至202-7中的任何一个。

[0024] 图2b-2示出了根据本发明一个实施例的结构220b,其包括与结构220a的层221和223中的一个相邻的附加金属子层224。

[0025] 图2b-3示出了根据本发明一个实施例的结构220c,其包括与结构220a的每个层221和223相邻的附加金属子层224。

[0026] 图2c示出了通过埋设触点205-0和205-1的YZ平面中的横截面,其将每个有源层202-0和202-1中的 N^+ 子层223连接到半导体衬底201中的触点206-0和206-1。

[0027] 图2d示出了在穿过图2a的存储器结构200的一部分中的有源层202-7的XY平面中的横截面中形成图2a的存储器结构200中的沟槽230。

[0028] 图2e示出了在穿过图2a的存储器结构200的一部分中的有源层202-7的XY平面中的横截面中沿着沟槽230在有源带的相对侧壁上沉积电荷俘获层231L和231R。

[0029] 图2f示出了沉积多晶硅或金属208以填充沟槽230。

[0030] 图2g示出了在图2f的存储器结构上的光刻图案化和蚀刻步骤之后,通过去除沉积

的多晶硅208的暴露部分来实现局部字线208w和预充电字线208-chg,并且采用绝缘材料209或气隙隔离填充产生的轴。

[0031] 图2h示出了穿过图2g的一行局部字线208w的XZ平面中的横截面,示出了有源层202-7和202-6中的有源带。

[0032] 图2i示出了图2h的局部字线208w中的每一个都连接到全局字线208g-a中的任何一个,在设置在有源层202-0到202-7之上的一个或多个层中布线,或者至全局字线208g-s之一,在设置在有源层202-0和衬底201之间的有源层下方的一层或多层中布线(参见图4a)。

[0033] 图2j示出了根据本发明一个实施例的图2i的实施例的替代实施例,其中仅提供了顶部全局字线—即没有任何底部全局字线,在该实施例中,沿有源带的一个边缘的局部字线相对于有源带的另一边缘上的局部字线交错(参见图4b)。

[0034] 图2k示出了根据本发明一个实施例的控制局部字线的相对侧上由有源带形成的TFT的每个局部字线208w(参见图4c)。

[0035] 图3示出了用于设置 N^+ 子层221中的源极线上的源极电压(V_{ss})的方法和电路元件;具体地,可以通过硬线解码的源极线连接280或者使用预充电TFT 303和位线连接270来设置源极线电压。

[0036] 图4a示出了对于图2i所示的本发明的实施例的XY平面中的横截面,示出了将局部字线208w连接到全局字线208g-a的触点291。

[0037] 图4b示出了对于图2j所示的本发明的实施例的XY平面中的横截面,示出了以交错配置将局部字线208w连接到顶部全局字线208g-a(或底部全局字线208g-s)的触点291。

[0038] 图4c示出了对于图2k所示的本发明的实施例的XY平面中的横截面,示出了将局部字线208w连接到全局字线208g-a以及相邻的有源带对之间的隔离209的触点291。

具体实施方式

[0039] 图1a示出了根据本发明一个实施例的便于在对存储器单元的组织的该详细描述中进行说明的概念化存储器结构100。如图1a所示,存储器结构100代表在衬底层101的表面上沉积的薄膜中形成的存储器单元的三维块。例如,衬底层101可以是用于制造集成电路的常规硅晶片,这对于本领域的普通技术人员来说是熟悉的。在该详细描述中,笛卡尔坐标系(比如图1a所示)仅用于便于讨论的目的。在该坐标系下,衬底层101的表面被认为是平行于XY平面的平面。因此,如本说明书中所用,术语“水平”是指平行于XY平面的任何方向,而“垂直”则是指Z方向。

[0040] 在图1a中,每个垂直列表示在水平NOR串的堆中共享垂直公共控制栅极或字线的存储元件(即薄膜存储晶体管或TFT),其中每个NOR串沿着Y方向延伸。每个NOR串沿着“有源带”由TFT形成,下面进一步详细描述。与NAND串不同,在NOR串中,写入、读取或擦除其中一个TFT不涉及激活NOR串中的其他TFT。如图1a所示,存储器结构100表示由4堆NOR串组成的阵列,每堆具有4个NOR串,并且每个NOR串具有4个TFT。注意,作为概念化结构,存储器结构100仅是本发明的存储器结构的某些显著特征的抽象。尽管在图1a中示出为 4×4 NOR串的阵列,每个串具有四个TFT,但本发明的存储器结构可以具有沿着X、Y和Z方向中的任何一个的任何数量的TFT。例如,沿着X和Z方向中的每个可能有2、4、8、16、32、64...NOR型串,每个NOR

串可能有2、4、8、16...8192或更多个TFT。使用2的整数次幂(即 2^n ,其中n是整数)的数字遵循常规存储器设计中的惯例。通常通过解码二进制地址来访问存储器的每个可寻址单元。因此例如,本发明范围内的存储器结构可以沿着X和Z方向中的每个具有M个NOR串,其中M是不一定为 2^n 的数字(对于任何整数n)。如果存储器块100每个具有8192堆的8个NOR串,每个NOR串具有8192个存储元件,则存储器块100将具有NOR型非易失性TFT形式的超过五亿个存储元件。由于现在使用多层级单元(MLC)技术将多于一个位存储在存储元件中并不少见,因此存储器块100可以存储超过十亿位的信息。一兆兆位的存储器芯片会有1000个或更多个这种模块,加上备用模块来代替有缺陷的或损坏的模块。

[0041] 作为概念化结构,存储器结构100在X、Y、Z方向中的任何一个方向上都没有按比例绘制。

[0042] 图1c示出了在概念化存储器结构100的YZ平面横截面中的4个NOR串的堆的基本电路表示。如图1c所示,每个NOR串沿Y方向延伸,存储元件连接在源极线153-m和位线154-m之间,其中m是相应源带的1至4之间的索引。4个NOR串中的相应存储元件连接相应的垂直字线151-n,其中n是沿着有源带的字线的索引。

[0043] 图1b示出了根据本发明一个实施例的共享公共垂直字线的两堆NOR串的基本电路表示。下面结合图2k讨论并说明这种配置的详细结构。如图1b所示,该基本电路配置包括设置在共享公共字线的存储器结构100的相邻列中的NOR串(例如NOR串150L和150R)。

[0044] 如图1b所示,NOR串150L和150R是位于公共字线151a的相对侧上的两个有源带中的NOR串。存储晶体管152R-1至152R-4和152L-1至152L-4分别是其公共垂直字线151a右侧的四个有源带中的存储元件和左侧的四个有源带中的存储元件。在该实施例中,如下面结合图2k和图4c更详细地示出,通过具有公共局部字线来控制相邻有源带的TFT,可以实现更大的存储密度。例如,字线151n控制位线153R-1、153R-2、153R-3和153R-4的NOR串中的TFT以及位线153L-1、153L-2、153L-3和153L-4的NOR串中的TFT。如下面更详细地讨论,在一个实施例中,可以在一些操作条件下使用每个NOR串固有的寄生电容C(例如串的N+扩散与其多个相关的局部字线之间的寄生电容),以提供虚拟电压源。

[0045] 可以使用常规的编程、抑制、擦除和读取电压对本发明的NOR串中的TFT进行编程、编程抑制、擦除或读取。在本发明的一个或多个实施例中,TFT由薄膜存储晶体管实现,薄膜存储晶体管使用福勒-诺德海姆隧穿或直接隧穿机制被编程或擦除。在另一实施例中,沟道热电子注入可用于编程。

[0046] 图2a示出了根据本发明一个实施例的在半导体衬底201上形成有源层202-0至202-7之后的存储器结构200的YZ平面中的横截面。如图2a所示,存储器结构200包括有源层202-0至202-7。半导体衬底201表示例如在形成有源层之前可以在其上形成用于存储器结构200的支持电路的P掺杂体硅晶片。这种支持电路可以包括模拟和数字电路。这些支持电路的一些示例可以包括移位寄存器、锁存器、感测放大器、参考单元、电源线、偏置和参考电压发生器、反相器、与非、或非、异或和其他逻辑门、输入/输出驱动器、地址解码器(包括位线和字线解码器)、其他存储器元件、定序器和状态机。这些支持电路可以由常规器件的构建块形成,例如N阱、P阱、三阱、N⁺、P⁺扩散、隔离区、低压和高压晶体管、电容器、电阻器和互连,如对于本领域技术人员来说是已知的。

[0047] 在半导体衬底201中和其上形成支持电路之后,提供绝缘层203-0,其例如可以是

沉积或生长的厚氧化硅。

[0048] 接下来,在一些实施例中,可以形成包括“全局字线”的一层或多层互连,这将在下面讨论。可以提供这样的金属互连线(例如图2c的全局字线接合垫264,下面讨论)作为沿垂直于将在稍后步骤形成的有源NOR串的预定方向延伸的水平长窄带。为了便于在该详细描述中进行讨论,假设全局字线沿X方向延伸。金属互连线可以通过在一个或多个沉积的金属层上施加光刻图案化和蚀刻步骤来形成。(可替代地,这些金属互连线可以使用常规的镶嵌工艺形成比如铜镶嵌工艺形成)。然后沉积厚氧化层203-0,之后使用常规的化学机械抛光(CMP)进行平坦化步骤。

[0049] 然后依次形成有源层202-0至202-7,每个有源层通过绝缘层203-1至203-7中相应的一个而与之之前的有源层绝缘。在图2a中,尽管示出了八个有源层,但可以提供任何数量的有源层。实际上,要提供的有源层的数量可取决于工艺技术,比如允许切穿有源层以到达半导体衬底201的良好控制的各向异性蚀刻工艺的可用性。每个有源层在下面讨论的蚀刻步骤中蚀刻,以形成各自沿Y方向延伸的大量平行有源带。

[0050] 图2b-1示出了根据本发明一个实施例的结构220a,其可以用于实现图2a的有源层202-0至202-7中的任何一个。如图2b-1所示,有源层220a包括沉积的多晶硅子层221-223。子层221-223可以连续地沉积在相同的处理室中而不会在其之间移除。可以通过沉积5-50nm的原位掺杂(doped in-situ)的 N^+ 多晶硅来形成子层223。然后通过沉积厚度在40-100nm范围内的未掺杂或轻掺杂多晶硅来形成子层222和221。然后子层221(即沉积的多晶硅的顶部)被 N^+ 掺杂。这种 N^+ 掺杂可以通过以下实现:(i) 砷或锑的低能量浅离子注入,形成20-50nm N^+ 掺杂顶部子层221,或(ii) 原位掺杂沉积的多晶硅,形成20-50nm N^+ 顶部子层221。(不应使用热扩散,因为它会使较早形成的较低有源层比较高有源层的扩散更大)。硼(P^-)或磷(N^-)离子的低剂量注入也可以足以穿透注入的或原位 N^+ 掺杂的子层221的能量进行,以便调整到增强模式阈值电压用于位于顶部 N^+ 掺杂子层221和底部 N^+ 掺杂子层223之间的子层222。

[0051] 在所有有源层202-0至202-7已经形成之后,优选地使用常规快速热退火技术(例如在700°C或更高温度下)发生子层221和222中的 N^+ 和 P^- 注入物质的热活化,从而确保所有有源层以大致相同的量经历高温处理。必须注意限制总热预算,以避免将 N^+ 子层223与 N^+ 子层221合并,从而不消除 P^- 子层222。需要 P^- 子层222保持足够厚以避免 $N^+P^-N^+$ 晶体管在 N^+ 子层221和223上施加低电压时击穿。

[0052] 子层222的最终厚度代表TFT沟道长度,其在长有源带上可以少至10nm或更少。在一实施例中,可以通过在沉积 N^+ 多晶硅子层221之前,沉积氮化硅(例如 SiN 或 Si_3N_4)的超薄(约1nm)膜,或在形成 N^+ 子层223之后的另一合适的扩散阻挡膜,然后再次沉积厚度范围在5-30nm的子层222的多晶硅之后,控制TFT沟道长度小于10nm。超薄氮化硅层可以通过化学气相沉积、原子层沉积或任何其他手段(例如低温下的高压氮化)而沉积。每层超薄氮化硅用作防止 N^+ 子层221和223中的掺杂剂扩散到 P^- 子层222中的扩散阻挡层,但是其足够薄以仅略微阻碍 N^+ 子层221(充当源极)和 N^+ 子层223(充当漏极)之间的区域中的MOS晶体管作用。(子层222的表面反转层中的电子容易直接隧穿1nm的氮化硅)。这些额外的超薄氮化硅层增加了制造成本,但是可以显著降低沿着处于“关闭”状态的有源带中的众多TFT中的漏电流,同时为处于“接通”状态的所访问的TFT提供高读取电流。

[0053] 可选地,为了沿着 N^+ 子层223和221的位线和源极线提供较低的电阻率,可以在 N^+ 子层221和223中相应的一个(例如图2b-2中的w)或者两者(例如图2b-3)附近提供附加的导电子层224。子层224可以由一个或多个沉积的金属层提供。例如,可以通过首先沉积1-2nm厚的TiN层,然后沉积10-40nm厚的钨层或类似的难熔金属或其硅化物或硅化金属来提供子层224。为了降低穿过长导电带的信号的“RC延迟”(即由于线电阻R和线电容C的乘积产生的时间延迟),并且为了最小化穿过长而窄的有源带的“IR降”(即由于电流I和线电阻R的乘积产生的电压降),期望降低的线电阻。然而,在每个有源层202-0至202-7中包含金属子层224可能增加制造过程的成本和复杂性,包括的复杂在于一些金属材料比其他子层中的材料比如多晶硅或氧化硅相对更加难以各向异性蚀刻。然而,使用金属子层224使得能够使用明显更长的有源带,这导致优良的阵列效率。另一方面,较短的有源带对 N^+ 子层223和 N^+ 子层221之间的泄漏具有优越的抗扰性,并且比较长的带具有更低的固有电容。集成电路设计人员可能会在低延迟最重要时选择较短的有源带(有或没有有一个或两个金属层)。可替代地,可以通过在每个有源带的两端处而不是仅在一端处提供埋设触点来减小带电阻。

[0054] 块形成图案化和蚀刻步骤在形成的有源层中定义单独的块。如下面讨论,每个块限定其中可以形成沿着Y方向平行延伸的大量(例如数千个)有源带的区域,其中每个有源带最终形成大量(例如数千个)TFT。

[0055] 依次形成有源层202-0至202-7中的每一个,每个有源层通过重复上述步骤而形成。另外,在限定每个有源层的块的块形成图案化中,每个下一个更高的有源层稍微延伸超过先前的有源层(例如,参见如下面讨论的图2c所示,层202-1延伸超过层202-0),以允许较高的有源层通过指定的埋设触点访问半导体衬底201中的其特定解码器和其他电路。

[0056] 图2c示出了通过埋设触点205-0和205-1的YZ平面中的横截面,其将有源层202-0和202-1的每个中的NT子层223连接到半导体衬底中的触点206-0和206-1。如图2c所示,例如,埋设触点205-0和205-1将半导体衬底201中的触点206-0和206-1连接到由有源层202-0和202-1的每个中的 N^+ 子层223形成的局部位线或源极线。可以类似地提供用于有源层202-2至202-7(未示出)的埋设触点以将有源层202-2至202-7连接到半导体衬底201中的触点206-2至206-7(未示出)。通过开关电路,触点206-0至206-7中的每一个可以将预充电电压 V_{b1} 施加到相应的位线或源极线,或者在读取操作期间可以连接到感测放大器或锁存器的输入端。开关电路可以将触点206-0至206-7中的每一个选择性地连接到多个特定电压源中的任何一个,比如编程电压(V_{program})、抑制电压(V_{inhibit})、擦除电压(V_{erase})或任何其他合适的预定或预充电参考电压 V_{b1} 或 V_{ss} 。在下面讨论的一实施例中,使用沿着位线或源极线的相对较大的寄生电容C,虚拟接地可以在每个有源层的子层221中产生。在该实施例中,不需要将埋设触点和分离互连提供给由有源层202-0至202-7的每个中的子层221形成的位线或源极线。

[0057] 图2c还示出了用于将要沿着X方向形成的全局字线连接到半导体衬底201中的触点262-0至262-n的埋设触点261-0至261-n。这些全局字线被提供以连接待形成的相应的局部字线208w(例如参见下面描述的图2g)。提供接合垫264以允许连接到尚未在全局字线261-0和261-n之上垂直形成的局部字线208w。通过开关电路和全局字线解码器,全局字线262-0至262-n中的每一个可被单独地选择性地连接,或者在几个全局字线之间被共享至多个参考电压源中的任何一个,比如阶梯式编程电压(V_{program})、读取电压(V_{read})和擦除电压

(V_{erase})。

[0058] 这些埋设触点、全局字线和接合垫可以使用常规光刻图案化和蚀刻步骤随后沉积一个或多个导体或通过合金化(例如钨金属或硅化钨)来形成。

[0059] 在形成顶部有源层(例如有源层202-7)之后,通过蚀刻穿过有源层以使用带形成掩模到达底部全局字线(或半导体衬底201)来形成沟槽。带形成掩模由沿Y方向(即垂直于沿X方向延伸的全局字线带的方向)延伸的长窄带的光刻胶层中的图案组成。顺序各向异性蚀刻通过有源层202-7向下蚀刻到202-0,并且通过介电隔离层203-7向下蚀刻到203-0。由于图2c的示例中八个要被蚀刻的有源层的数量(更一般地可以是16个或更多个有源层),光刻胶掩模本身可能不足够坚固以通过蚀刻穿过最低有源层所需的多次蚀刻保持带图案。因此,如本领域普通技术人员已知的,可能需要通过硬掩模材料比如碳进行加固。蚀刻终止于全局字线的接合垫上方的介电隔离。提供蚀刻停止阻挡膜比如氧化铝以在沟槽蚀刻序列期间保护接合垫可能是有利的。

[0060] 图2d示出了在穿过图2a的存储器结构200的一部分中的有源层202-7的XY平面中的横截面中形成图2a的存储器结构200中的沟槽230。在相邻的沟槽230之间是高纵横比、长而窄的有源带堆。为了获得最佳的蚀刻结果,当蚀刻通过不同子层的材料时,尤其是当存在金属子层224时,蚀刻化学品可能不得被改变。多步骤蚀刻的各向异性是重要的,因为应该尽可能地避免任何子层的底切,并且使得底部有源层中的有源带(例如有源层202-0中的有源带)具有大致与相邻有源带相同的宽度和间隙间隔,作为顶部有源层的有源带(即有源层202-7的有源带)中的对应宽度和间隙间隔。自然地,要被蚀刻的堆中的有源层的数量越多,则连续蚀刻的设计越具有挑战性。为了减轻与蚀刻通过例如32个有源层有关的困难,可以在每个8层的区域进行蚀刻,如上面提到的在第188-189页Kim所讨论的。如图2d所示,沟槽230沿着Y方向延伸。

[0061] 此后,在沟槽230中的有源带的侧壁上共形地沉积一层或多层电荷俘获材料。电荷俘获层通过以下方式形成:首先沉积或生长厚度为2-10nm的薄隧穿介电膜,通常是二氧化硅层或氧化硅-氮化硅-硅氧化物(“ONO”)三层,然后沉积4-10nm厚的电荷俘获材料层,通常为氮化硅或富硅的氮化物或氧化物或者嵌入薄介电膜中的纳米晶体或纳米点,然后用阻挡电介质将其覆盖。阻挡电介质可以是例如由ONO层或高介电常数膜(比如氧化铝、氧化铪或它们的某种组合)组成的5-15nm厚的层。存储元件可以是SONOS、TANOS、纳米点存储器、隔离的浮置栅极或本领域普通技术人员已知的任何合适的电荷俘获夹层结构。沟槽230必须足够宽以容纳邻接有源带的两个相对侧壁上的存储元件,以及由这些相对侧壁上的TFT共享的垂直局部字线。图2e示出了在穿过图2a的存储器结构200的一部分中的有源层202-7的XY平面中的横截面中沿着沟槽230在有源带的相对侧壁上沉积的电荷俘获层231L和231R。

[0062] 底部全局字线处的接触开口在层202-7的顶部被光刻图案化并且通过各向异性蚀刻穿过沟槽230底部处的电荷俘获材料而暴露,停止在底部全局字线接合垫(例如图2c的全局字线接合垫264)。在下面将结合图2i描述的一实施例中,应仅将交替行的沟槽230(例如其中形成的字线被分配奇数地址的行)向下蚀刻到底部全局字线。在一些实施例中,蚀刻之前是在各向异性蚀刻沟槽230底部的电荷俘获材料的期间沉积多晶硅的超薄膜(例如2-5nm厚),以保护沟槽230的侧壁上的阻挡电介质的垂直表面。

[0063] 此后,可以在电荷俘获层上沉积掺杂多晶硅(例如,P⁺多晶硅)以形成控制栅极或

垂直局部字线。由于 P^+ 掺杂多晶硅具有比 N^+ 掺杂多晶硅更高的功函数,因此其是优选的。可替代地,还可以使用相对于 SiO_2 具有高功函数的金属(例如钨、钼、铬或镍)来形成垂直局部字线。现在可以用 P^+ 掺杂多晶硅或金属填充沟槽230。在下面讨论的图2i的实施例中,在交替行的沟槽230中的掺杂多晶硅或金属(即托管分配有奇数地址的局部字线的行)与底部全局字线欧姆接触。在其他行的沟槽230中的多晶硅(即托管分配有偶数地址的局部字线的行)与底部全局字线隔离。(这些局部字线将被布线在顶部有源层之上的顶部全局字线接触)。现在可以去除光刻胶和硬掩模。然后可以使用CMP步骤来从每个块的顶部表面去除掺杂多晶硅。图2f示出了沉积多晶硅208以填充沟槽230。

[0064] 图2g示出了在图2f的存储器结构上的光刻图案化和蚀刻步骤之后,通过去除沉积的多晶硅208的暴露部分来实现局部字线208w,并且采用绝缘材料209填充产生的轴。在这种情况下掺杂多晶硅的去除是在相当有限的空间中的高纵横比蚀刻,可能需要使用上述技术的硬掩模。产生的轴可以填充有绝缘材料209或留下作为气隙。暴露用于挖掘的掺杂多晶硅的掩模图案是沿X方向延伸的平行带,从而它们与在一实施例中需要形成的全局字线重合以接触局部字线208w。

[0065] 在图2g中,在去除沉积多晶硅208的相应部分之后,电荷俘获层231L和231R的与绝缘材料209相邻的部分保留。在一些实施例中,电荷俘获层231L和231R的那些部分可以通过在用绝缘材料209填充轴之前的常规蚀刻工艺被去除。可以在除去掺杂多晶硅的同时或者在其之后执行在轴中的电荷俘获材料的蚀刻。随后的蚀刻也将除去各向异性蚀刻留下的任何精细多晶硅桁条;这种多晶硅桁条可能会引起不希望电荷泄漏,用作相邻垂直局部字线之间的电阻泄漏路径。去除这种电荷俘获材料还消除了一个TFT与TFT之间的俘获电荷沿着同一串立即至其左右的横向扩散。

[0066] 图2h示出了穿过一行局部垂直字线208w(也在图2g中在XY平面中示出)的XZ平面中的横截面,示出了有源层202-7和202-6中的有源带。如图2h所示,每个有源层包括 N^+ 子层221、 P^- 子层222和 N^+ 子层223。在一实施例中, N^+ 子层221(例如源极线)连接到接地参考电压 V_{ss} (未示出),且 N^+ 子层223(例如位线)根据图2c所示的方法连接到衬底201中的触点。因此,局部字线208w、有源层202-7或202-6的面向字线208w的部分和字线208w与有源层202-7或202-6的那部分之间的电荷俘获层231L形成存储元件或存储TFT,如图2h中的附图标记281和282所示。在208w的相对侧上面对的TFT281和282分别是TFT283和284,其中包含电荷俘获层231R。在提供TFT283和284的有源带202-6和202-7的另一侧上是TFT285和286。因此,图2h中所示的配置表示TFT的最高封装密度配置,其中每个垂直字线被沿着其两侧的两个有源带共享,每个有源带被沿着其两侧的两个字线共享, N 子层223可被充电至手持存储晶体管的操作所需的合适电压(例如编程电压 V_{prog} 、抑制电压 $V_{inhibit}$ 、擦除电压 V_{erase} 或读取参考电压 V_{bl})。如图2h所示,附加的金属子层224增加了位线的电导率,以便于存储器件的操作。在另一实施例中,任何有源层202-0至202-7中的 N^+ 子层221可以保持浮置。在每个有源层中,一个或多个局部垂直字线(被称为“预充电字线”:例如图2g中的预充电字线208-chg)可以用作非存储TFT。当施加合适的电压(即使预充电TFT呈现“导通”状态)时,每个预充电字线立即反转子层222,使得 N^+ 子层221可被预充电至 N^+ 子层223上的电压 V_{ss} 。当预充电字线上的电压撤回,(即返回到其“断开”状态)并且带两侧上的所有其他字线也“断开”时,器件操作可以随在预充电电压 V_{ss} 下保持充电作为虚拟参考的 N^+ 子层221继续,因为 N^+ 子层221的带电

容器中的寄生电容足够大以使其电荷保持足够长以支持编程和读取操作(参见下文)。

[0067] 当施加合适的电压时,每个局部字线208w可用于读取、写入或擦除存储在位于电荷俘获部分231L或231R上的每个有源层202-0至202-7中形成的TFT中指定的一个中的电荷。可替代地,在下面将结合图2k描述的一个实施例中,当施加合适的电压时,每个局部字线208w可用于读取、写入或擦除存储在位于电荷俘获部分231L或231R上的每个有源层202-0至202-7中形成的TFT的任何中的电荷。然而,如图2k所示,有源层202-0至202-7的两侧中仅有一侧形成为存储TFT,因此在本实施例中不需要底部和顶部全局字线。

[0068] 然后可以沉积隔离电介质或氧化物并将其表面平坦化。然后可以对半导体衬底201和局部字线208w的接触进行光刻图案化和蚀刻。在结合图2i和对应的图4a描述的一实施例中,仅为分配了偶数地址的那些提供对局部字线208w的接触(分配有奇数地址的局部字线从阵列的底部由底部全局字线接触)。对于图2j所示的实施例,为每个局部字线提供触点,但是局部字线相对于相反的字线交错,如图4b所示。沉积的金属层提供顶部金属层和触点。可以首先通过形成薄TiN层,接着形成低电阻金属层(例如钨)来提供这种金属层。然后对金属层进行光刻图案化以形成顶部全局字线。(可替代地,这些全局字线可以由铜镶嵌工艺来提供)。在一实施例中,这些全局字线是水平的,沿X方向延伸,与形成在隔离氧化物中的触点电连接(即由此接触局部字线208w)以及与半导体衬底201(未示出)的接触。当然,本领域技术人员已知的其他掩模和蚀刻工艺流程可以形成偶数和奇数寻址的局部字线并将它们适当地连接到它们的全局字线,或从阵列顶部通过顶部全局字或从阵列底部通过底部全局字线以及在一些实施例中两者兼有。

[0069] 图2i示出了图2h的局部字线208w中的每一个都连接到全局字线208g-a中的任何一个,在设置在有源层202-0到202-7之上的一个或多个层中布线,或者至全局字线208g-s之一,在设置在有源层202-0和衬底201之间的有源层下方的一层或多层中布线。耦合到底部全局字线的局部字线208w可被分配奇数地址,而耦合到顶部全局字线的局部字线208w可被分配偶数地址。图4a示出了XY平面中的对应横截面,示出了将局部字线208w连接到全局字线208g-a的触点291。(相反,在图2k和对应的图4c的实施例中,局部字线208w仅在有源带的一侧上控制每个有源带)。

[0070] 图2j示出了根据本发明一个实施例的图2i的实施例的替代实施例,其中仅提供了顶部全局字线(或者可替代地,仅提供底部全局字线)。在该实施例中,沿着有源带的一个边缘的局部字线相对于在有源带的另一边缘上的局部字线交错。这在图4b中示出,其示出了XY平面中的对应横截面,示出了将局部字线208w以交错配置连接到顶部全局字线208g-a(或底部全局字线208g-s)的触点291。该实施例通过避免形成底部全局字线(或顶部全局字线,视情况而定)所需的工艺步骤来简化工艺流程。在图2i和对应的图4a的实施例中,其中提供了顶部和底部全局字线,可以在全局字线的一个间距内的每个有源带的每个有源层中提供两个TFT(即在每个有源带中,使用有源带的一个侧壁形成一个TFT,并且从底部全局字线进行控制,使用有源带的另一侧壁形成另一TFT,并且从顶部全局字线进行控制)。(间距是一个最小线宽加上相邻线之间所需的最小间隔)。相反,如图2j和对应的图4b所示,可以在每个有源层中的一个全局字线间距内提供仅一个TFT。在每个带的两侧的两个局部字线208w可以相对于彼此交错,从而需要两个全局字线间距来接触它们两者。交错实施例的损失是双密度TFT的损失,其固有地使每个有源带的两个边缘在每个全局字线的一个间距内

提供TFT。

[0071] 图2k示出了根据本发明一个实施例的控制局部字线的相对侧上由有源带形成的TFT的每个局部字线208w。图4c示出了XY平面中的相应横截面,示出了将局部字线208w连接到全局字线208g-a以及相邻的有源带对之间的隔离209的触点291。如图2k所示,每个TFT由位于公共局部字线相对侧上的双对有源带中的任一个形成,每个双对有源带由填充有氧化物或介电材料或气隙209的沟槽与类似形成的相邻双对有源带隔离。相邻双对有源带之间的隔离沟槽容纳电荷俘获材料231或多晶硅208。在通过蚀刻限定局部字线208w之后,然后可以用氧化物或介电材料209填充被保护的隔离沟槽,或留作气隙。

[0072] 图3示意性地示出了每个有源带(例如参见图2b-1)的子层221通过硬线280(虚线)由金属或N⁺掺杂多晶硅导体连接到源极参考电压V_{ss}的实施例。每个硬线280可以独立连接,使得不同层的源极电压不必相同。由于仅在形成子层223之后才形成子层221,因此将子层221连接至参考电压V_{ss}的金属或N⁺掺杂多晶硅导体需要对每个有源层202-0至202-7进行一个或两个附加的图案化和蚀刻步骤,因此增加了处理成本。为了避免这种额外的成本,使用每个有源NOR串的大的固有寄生电容C。利用固有寄生电容C,不需要硬线280,并且每个有源带的子层221在暂时预充电到通过由预充电字线208-chg控制的局部垂直预充电TFT的作用从位线子层223转移到其的电压V_{ss}之后保持浮置。在长水平的NOR串(例如具有1024个或更多个存储TFT)中,可以在有源带的任一侧上提供几个预充电TFT(例如每512个TFT一个)。假定每个局部字线之间的局部电容作为一个板且N⁺/P⁻/N⁺有源层作为另一板,则每个这样的TFT提供通常约 3×10^{-18} 法拉的电容器。由于从带两侧有稍微多于2000个贡献电容的TFT,该串的总电容C接近0.01微微法拉,这足以将预充电电压维持在其上,远远超过在预充电操作之后立即进行的写入、擦除或读取操作所需的毫秒。可以通过延长NOR串以容纳沿串的每一侧数千个更多的TFT来增加电容C,从而相应地增加N⁺子层221上的预充电电压V_{ss}的保持时间。然而,较长的NOR串遭受N⁺子层221与N⁺子层223之间泄漏电流的增加,当读取被寻址的一个TFT时,这种泄漏电流可能干扰所感测的电流。此外,在读取操作期间预充电较大电容器所花费的时间可能与对低读取延迟(即快速读取访问时间)的要求相冲突。为了加速对长NOR串的电容C的预充电,通常需要提供多于一个的预充电TFT;这种预充电TFT可以分布在NOR串的整个长度上。

[0073] 在图3中还示出了到P⁻子层222的可选连接290,以从衬底201访问反偏置电压V_{bb}。可以使用负V_{bb}电压来调制沿着每个有源带的TFT的阈值电压,从而减少N⁺源极子层221和N⁺漏极子层223之间的亚阈值泄漏电流。在一些实施例中,可以在擦除操作期间向其控制栅极保持在接地电势的隧穿擦除TFT施加高正V_{bb}电压。

[0074] 因为NOR串中的TFT并联连接,所以本发明的NOR串的读取操作条件应当优选地确保沿着有源带的两个边缘的所有TFT以增强模式操作(即它们各自具有其控制栅极151n与其源极电压V_{ss}之间的正阈值电压),以便当带两侧的所有控制栅极都保持在V_{ss}或低于V_{ss}时,抑制有源带的N⁺子层221和223之间的泄漏电流。该增强阈值电压可以通过用P-掺杂剂浓度(通过硼,浓度通常在 1×10^{16} 和 1×10^{17} 每cm³之间)对子层222进行掺杂来实现,以便产生约1伏的原生TFT阈值电压,并通过将所有未被寻址的局部字线保持在0伏的有源带的两侧上。可替代地,如果沿着有源串的一些TFT具有负阈值电压(即在耗尽模式阈值电压中),则可以通过将N⁺子层221上的V_{ss}电压升高到约1.5伏并且将N⁺子层223上的电压V_{b1}升高到约

1.5伏以上约半伏到一伏的电压同时将所有局部字线保持在0伏来实现泄漏电流抑制。这提供了与将字线电压相对于源极保持在-1.5伏相同的效果,由此抑制了由处于轻微耗尽阈值电压的TFT引起的任何泄漏。此外,在擦除NOR串之后,擦除操作应优选地包括软编程操作,该操作将已被过度擦除的任何TFT转换为耗尽模式阈值电压回到增强模式阈值电压。

[0075] 上述电荷俘获材料(例如ONO堆)具有离子数据保留时间(通常在多年内测量),但耐久性低。在一定数量的写入-擦除周期之后,耐久性存储晶体管的性能降低的量度,如果小于一万个周期,其通常被认为是低的。然而,可以改变电荷俘获材料以减少保留时间,但显著增加耐久性(例如将保留时间减少到几小时,同时将耐久性增加到数千万次的写入/擦除周期)。例如,在ONO膜或电荷俘获层的类似组合中,隧道电介质通常6-8nm的氧化硅可被减少到2nm或更少的氧化硅,或者被另一电介质(例如氮化硅或SiN)完全替换。在适度的正控制栅极电压下,电子将通过直接隧穿(与福勒-诺德海姆隧穿不同)被吸引到氮化硅电荷俘获层中,这里电子将被暂时截留几分钟到几小时或几天。电荷俘获氮化硅层和氧化硅或氧化铝阻挡层将阻止这些电子逸出到控制栅字线,但它们最终会泄漏回到有源子层(电子带负电并且彼此排斥)。即使2nm或更小的隧道电介质在延长的周期之后局部破裂,被俘获的电子也将缓慢离开它们在氮化硅层中的阱。电荷储存材料的其他组合也可导致高耐久性但低保留(“半挥发性”)TFT。这种TFT可能需要周期性的写入刷新来补充丢失的电荷。因为这种TFT向相对较快的读取访问时间提供低延迟,所以具有这种TFT的本发明的NOR串阵列可以用于当前可以通过相对较慢的DRAM获得的应用。这种NOR串阵列在DRAM上的优势包括:位成本低得多,因为DRAM不能建立在三维块中,并且功耗要低得多,因为与目前DRAM技术所需的每几毫秒相比,刷新周期只需要每隔几分钟运行一次或每隔数小时一次。通过改变电荷俘获材料(例如图2e中的电荷俘获层231L和231R)的构造以及通过适当地调整编程/读取/擦除条件以并入周期性数据刷新来实现本发明的NOR串阵列。

[0076] 根据本发明的另一实施例,也可以使用沟道热电子注入方法对NOR串阵列进行编程,类似于本领域普通技术人员已知的在NROM/镜像位晶体管中使用的方法。在NROM/镜像位晶体管中,代表一位的电荷存储在沟道区域的与漏极区域的接合处旁边的一端,并且通过反转源极和漏极的极性,代表第二位的电荷被编程并存储在沟道区域的源极接点旁边的另一端。典型的编程电压是漏极5伏特,源极0伏特和控制栅极8伏特。如本领域技术人员所熟知的,读取两个位需要反向读取源极和漏极。然而,沟道热电子编程比隧道编程效率低得多,因此该方法不适用于通过隧穿可能的大规模并行编程。沟道热电子注入方法虽然提供了两倍的位密度,使其对档案记忆等应用具有吸引力。

[0077] 接下来描述本发明的NOR串的示例性操作。

[0078] 读取操作

[0079] 为了在有源带上的许多TFT中读取TFT,有源带两侧上的TFT最初被设置为“关闭”状态,使得所选块中的所有全局和局部字线最初保持为0伏特。在图3中,寻址的NOR串可以通过解码电路共享几个NOR串之间的感测电路,或者每个NOR串可以直接连接到专用感测电路,并且共享相同平面的许多其他寻址的NOR串可被并行地感测。每个寻址的NOR串具有的源极(N^+ 子层221)被设置为 $V_{ss} \sim 0V$,或者通过硬线280或者通过位线连接270连同预充电字线208-chg(在此情况下,在预充电阶段期间, V_{b1} 被初始保持在0伏特)。在预充电阶段之后,通过位线连接270将位线(即 N^+ 子层223)设置为约 $V_{b1} \sim 2$ 伏特。 V_{b1} 电压是寻址的NOR串的感

测放大器处的感测电压。一个寻址的全局字线及其所有相关的垂直局部字线从0伏提升到2伏左右,而块中的所有其他全局字线都处于其关闭状态。如果寻址的TFT处于擦除状态(即 $V_{th} \sim 1$ 伏特),则位线电压 V_{bl} 将开始朝向源极电压 V_{ss} 放电。该电压骤降由相应的感测放大器检测。然而,如果寻址的TFT处于编程状态(例如 $V_{th} \sim 3$ 伏),则不会检测到骤降。

[0080] 当使用MLC时(即在每个TFT中存储多于一位的信息),寻址的TFT可被编程为几个阈值电压中的任一个(例如用于表示两位数据的四个状态的1伏(对于擦除状态)、2.5伏、4伏或5.5伏)。寻址的全局字线及其局部字线可以以递增的电压步长上升,直到由相应的感测放大器在寻址的TFT中检测到导通为止。可替代地,可以施加单个字线电压 V_{bl} (例如 $V_{bl} = 6$ 伏),并且电压 V_{bl} 的放电速率可以与表示代表存储在TFT中的位的四个电压状态的几个可编程参考电压中的每一个的放电速率进行比较。这种方法可以扩展到存储8个状态(用于3位MLC TFT)或连续的状态,从而有效地提供模拟存储。可编程参考电压存储在同一块中的作为参考NOR串的NOR串中,优选位于与寻址的NOR串相同的平面中。当使用MLC时,可以提供多于一个可编程参考NOR串来检测每个编程状态。例如,如果使用3位MLC,则应至少有7个参考NOR串;优选地,应该为每个有源层和每个块提供整组参考NOR串。可编程参考NOR串通过读取、编程和后台泄漏紧密跟踪同一块中的操作NOR串的特性。只有有源带两侧之一上的TFT才能参与读取操作:有源带另一侧上的每个TFT必须设置为“关闭”状态。如本领域技术人员已知的,读取多状态TFT的正确状态的其他方式。

[0081] 读取速度快,因为与AN串相比,在NOR串中只有要读取的TFT需要“接通”,其中与正被读取的一个TFT串联的TFT必须也“接通”。在有源层中未设置金属子层224的实施例中(例如参见图2b-1的220a),对于每侧上具有1024个TFT的串,典型的电阻 R 为 ~ 100000 欧姆,并且典型的电容 $C \sim 10-14$ 法拉,以提供1纳秒量级的RC时间延迟。即使在有源带两侧上的每个NOR串中有4098个TFT,RC时间延迟仍将小于20纳秒。如果提供金属子层224以减小有源带的电阻 R ,则时间延迟可以大大减小。为了进一步减少读取延迟,所选择的有源块中的一些或所有平面可以始终被预充电到它们的读取电压 V_{ss} 和 V_{bl} ,由此使它们准备立即感测寻址的TFT(即立即在读取操作之前消除预充电阶段)。这种准备待机需要非常小的待机功率,因为周期性地重新充电电容器 C 以补偿电荷泄漏所需的电流非常小。在每个模块中,所有八个或更多个平面上的所有串都可以预充电以便快速读取;例如,在读取平面207-0(图2a)中的所有串之后,由于其 V_{ss} 和 V_{bl} 先前已经被设置用于读取,因此可以以短的顺序读取平面207-1。

[0082] 在存储块100中,在单个操作中只能读取每个NOR串的一个TFT。在具有八千个NOR串的平面中,共享公共全局字线的八千个TFT可以全部被同时读取,只要每个NOR串连接到其自己的感测放大器。如果每个感测放大器在例如使用串解码电路的同一平面内的四个NOR串中共享,则需要在四个连续步骤中进行四个读取操作,每个读取操作涉及两千个TFT。每个平面可以提供其自己的一组专用感测放大器,或者可替代地可以通过平面解码选择器在八个或更多个平面中的NOR串之间共享一组感测放大器。为每个平面提供独立的感测放大器允许所有平面的NOR串的同时读取操作,这相应地提高了读取吞吐量。然而,这种吞吐量是以额外的感测放大器所需的额外芯片面积为代价的,并且当太多TFT一次被读取时也可能产生接地电压反弹。在这方面,依靠预充电电容器 C 设置虚拟 V_{ss} 电压的实施例是特别有利的,因为它消除了这种接地电压反弹,因为所有NOR串的源电压 V_{ss} 没有连接到芯片的 V_{ss} 地线。

[0083] 编程(写入)和编程抑制操作

[0084] 有几种方法可以将寻址的TFT编程到其预定的阈值电压。最常见的方法是提供隧穿,即直接隧穿或福勒-诺德海姆隧穿。这些隧穿和电荷俘获机制中的任何一种都是高效的,所以需要非常小的电流来编程TFT,允许以最小的功耗并行编程数以万计的TFT。为了说明的目的,让我们假设通过隧穿编程需要施加100微秒(μs)持续时间的20伏脉冲到寻址的字线(控制栅极),0伏施加到有源带(例如图2a中的202-0)。在这些条件下,TFT的N+源极和漏极(图2b-1中的子层221、223)和P-沟道(子层222)在表面反转并且电子隧穿到电荷俘获层中。可以通过施加半选择电压(例如在本例中为10伏)来抑制TFT编程。例如,可以通过将字线电压降低到10伏同时保持带电压为0伏或者通过将有源带电压升高到10伏同时将字线电压保持在20伏或两者的某种组合来实现编程抑制。一次只能对一个寻址的有源带上的一个TFT进行编程,但其他带上的TFT可以在相同的编程周期内并行编程。当对在寻址的有源带的一侧上的多个TFT中的一个(例如偶数寻址的NOR串中的一个TFT)进行编程时,NOR串中的所有其他TFT被编程抑制,如有源带的另一侧上的所有TFT(例如奇数寻址的NOR串中的所有TFT)。一旦寻址的TFT被编程到其指定状态的目标阈值电压,就需要该TFT的编程抑制,因为超调该目标电压将对TFT施加不必要的应力。当使用MLC时,超调目标电压可能导致超越或与下一个较高目标阈值电压状态的阈值电压合并。应该注意的是,在共享相同全局字线及其相关局部字线的同一平面上的相邻有源带中的所有TFT因此暴露于20伏编程电压,并且一旦它们被编程到它们的目标阈值电压就需要被编程抑制。类似地,同一块内并且共享相同全局字线及其相关局部字线的其他平面上的所有TFT也因此暴露于20伏编程电压—也需要编程—抑制。这些程序和编程抑制条件都可以在本发明中得到满足,因为每个有源带的偶数和奇数侧由不同的全局字线及其相关的局部字线控制,并且因为每个有源带上的电压无关其平面都可以独立于所有其他有源带或其他平面进行设置。

[0085] 在一个示例中,块中的所有TFT首先被擦除到约1伏的阈值电压。然后将每个寻址的TFT的有源带上的电压设置为0伏(例如通过连接270结合预充电字线208-chg,或者通过连接280,如图3所示),如果寻址的TFT将被编程;否则如果寻址TFT将保持在其擦除状态(即编程抑制),则寻址的TFT的有源带上的电压被设置为10伏。与寻址的TFT相关的全局字线然后升高到20伏,无论是在一个步骤中,还是在从约14伏开始递增地增加电压的短暂步骤中。这种增量电压阶跃降低了TFT上的电应力,并避免超出目标阈值电压。块中的所有其他全局字线设置为半选10伏。所有平面上未在块中寻址的所有有源带以及寻址平面内未被单独寻址的所有有源带也被设置为10伏或可能浮置。这些有源带与局部字线强力耦合,这些字线的电压为10伏,因此浮置在接近10伏的电压下。递增的较高电压编程脉冲中的每个之后是读取周期以确定寻址的TFT是否已经达到其目标阈值电压。当达到目标阈值电压时,有源带电压升高到10伏(可替代地带浮置,并且当除了块中的一个寻址的全局字线之外的全部字线都升高到10伏时升高接近10伏)以抑制进一步编程,而全局字线保持编程在同一平面上尚未达到其目标阈值电压的其他寻址带。当所有寻址的TFT已被读取验证以正确编程时,该编程序列终止。当使用MLC时,可以通过首先对所有寻址的有源带的电容器C进行预充电(例如参见通过图3的连接270和预充电字线208-chg)至几个电压之一(例如当两位信息要存储在每个TFT中时为0、1.5、3.0或4.5伏)来加速编程多个阈值电压状态中的正确一个。然后将20伏脉冲施加到寻址的全局字线,其将TFT暴露于不同的有效隧穿电压(即分别为20、18.5、

17或15.5伏),导致四个阈值电压中的正确一个是在单个课程编程步骤中进行编程。之后,可以在各个TFT层级上施加精细的编程脉冲。

[0086] 由于块中每个有源带的固有电容C,所以在对寻址的全局字线施加高电压脉冲之前,块中所有平面上的所有有源带可以将其预充电电压状态设置在适当位置。因此,可以实现大量TFT的并行编程。此后,可以执行单独的读取验证,并且在必要时将正确编程的有源带重新设置为编程抑制模式。预充电是有利的,因为编程时间相对较长(例如约100微秒),同时对所有电容器C进行预充电或对寻址的TFT进行读取验证可在大于1000倍的时间段内执行。因此,在单个全局字线编程序列中编程尽可能多的TFT是有利的。

[0087] 擦除操作

[0088] 对于一些电荷俘获层,擦除是通过俘获电荷的反向隧穿来实现的,这可能相当慢(例如可能需要几十毫秒的擦除脉冲)。因此,擦除操作通常在块级执行,通常在后台执行。典型的块可以是八个平面高,每个平面具有8000个有源带,每个带在其任一侧上有4000个TFT,在一个块中总共五亿个TFT,使得一个兆兆位芯片包括约1000个这样的块,如果两位信息存储在每个TFT上。理想地,块擦除是通过在保持块中的所有全局字线在0伏的同时通过连接290(例如参见图3)向每个有源带的P⁻子层222(例如参见图2b-1)施加约20伏来执行的。擦除脉冲的持续时间应该使得大多数TFT被擦除到零和1伏之间的略微增强模式阈值电压。一些TFT可能会超调并被擦除为耗尽模式(即具有稍微负的阈值电压)。作为擦除命令的一部分,这些TFT需要在擦除脉冲结束之后被编程到轻微增强模式阈值电压。

[0089] 可替代地,代替施加到P⁻子层的V_{bb},在所有有源带上的子层221和223升高到约20伏,同时在擦除脉冲的持续时间内将所有全局字线保持在零伏。该方案要求带选择解码器(图2c中的206-0、206-1)采用能够在其接点处承受20伏的晶体管。可替代地,除了寻址的全局字线以外的所有全局字线都保持在零伏,同时将寻址的全局字线脉冲为-20伏,并将平面202-0至202-7中的所有有源带保持在零伏。该方法仅擦除被一个寻址的全局位线触及的所有TFT的XZ切片。

[0090] NROM TFT实施例的擦除可以使用带间隧穿引起的热空穴注入的常规NROM擦除机制来实现。为了中和俘获电子的电荷:在字线上施加-5伏,在源极子层221上施加零伏,且在漏极子层223上施加5伏。

[0091] 提供以上详细描述是为了说明本发明的具体实施例,而不是限制性的。在本发明的范围内的许多变化和修改是可能的。在所附权利要求中阐述了本发明。

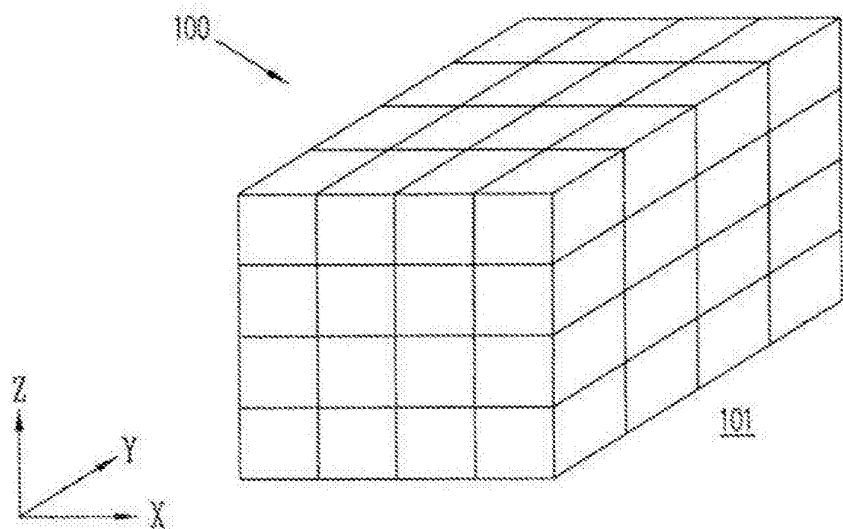


图1a

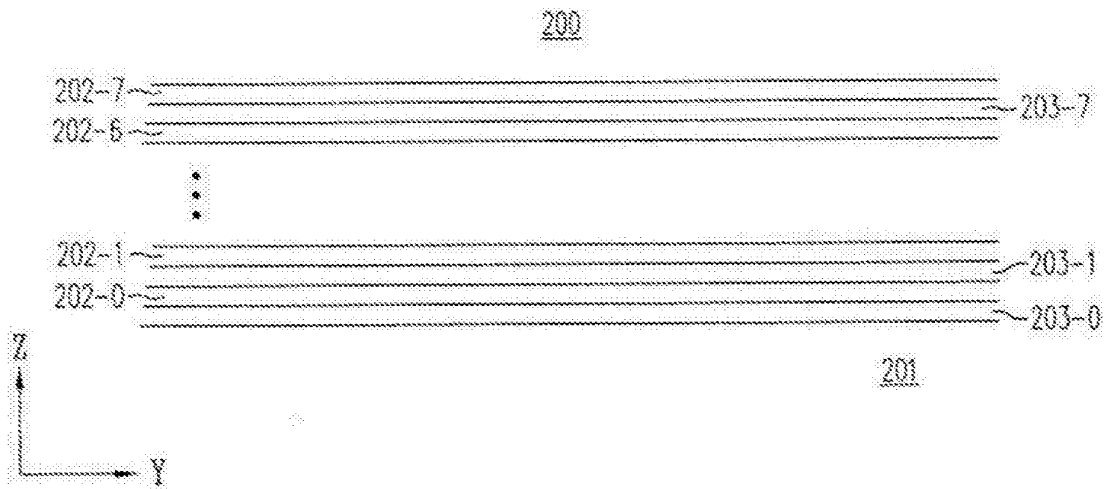


图2a

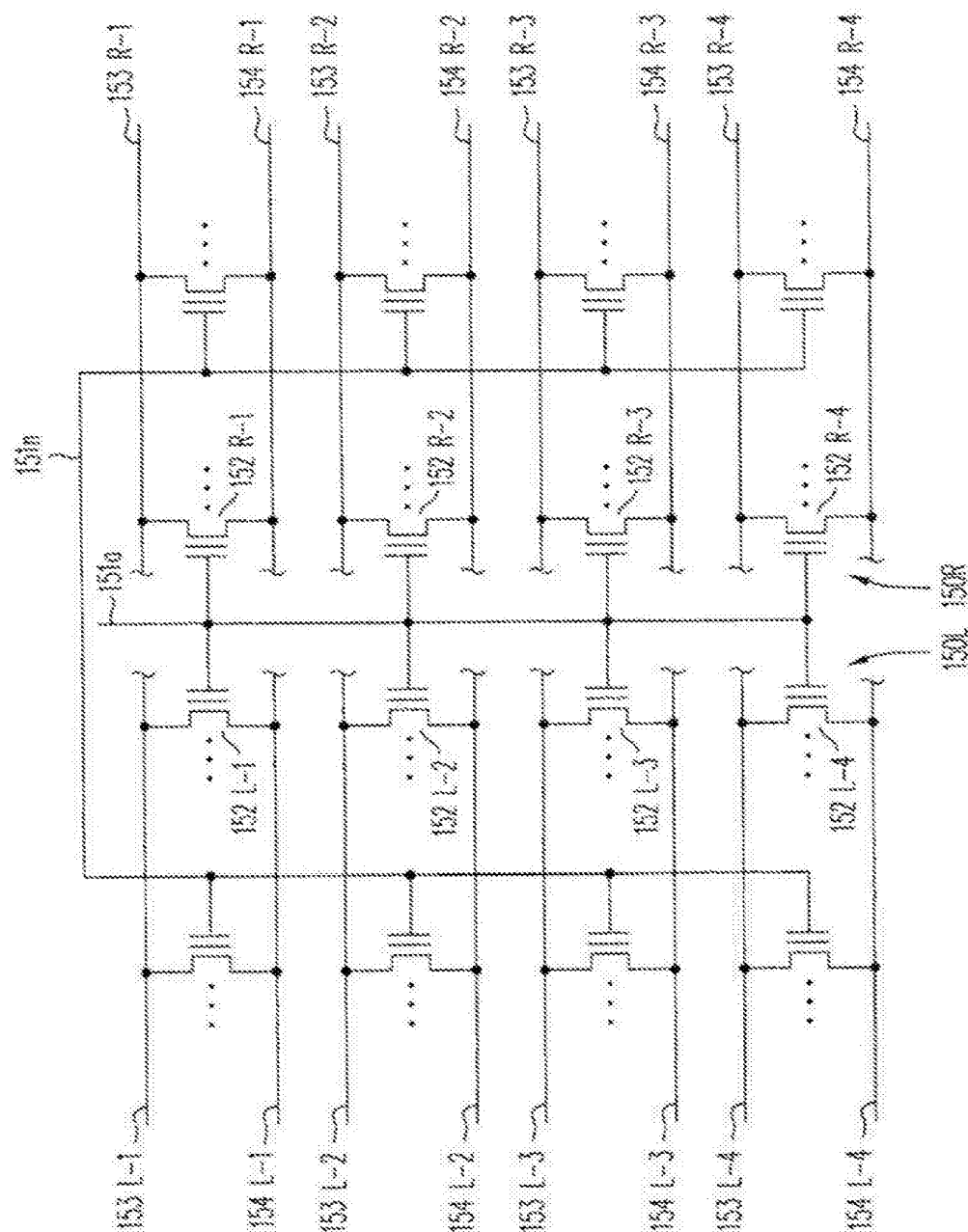


图1b

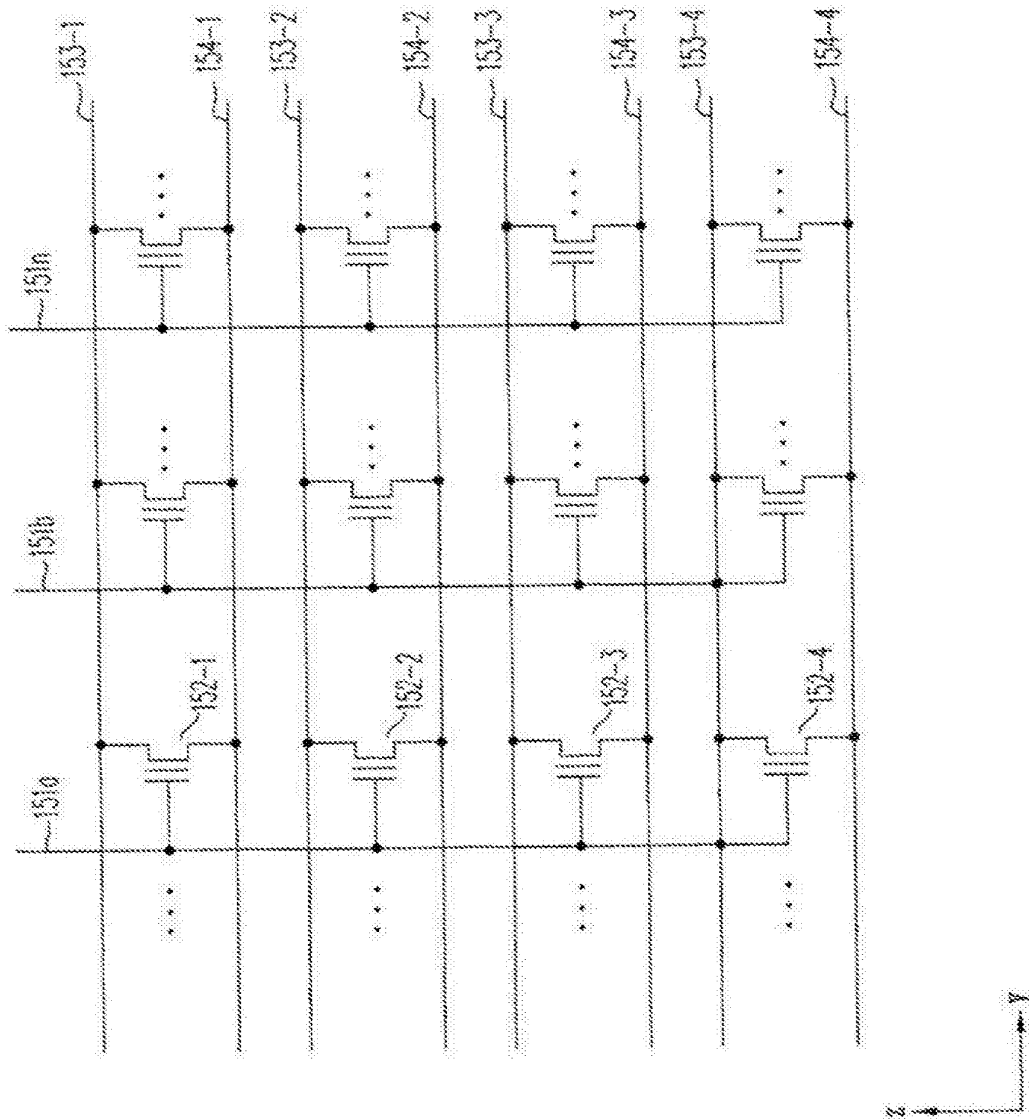


图1c

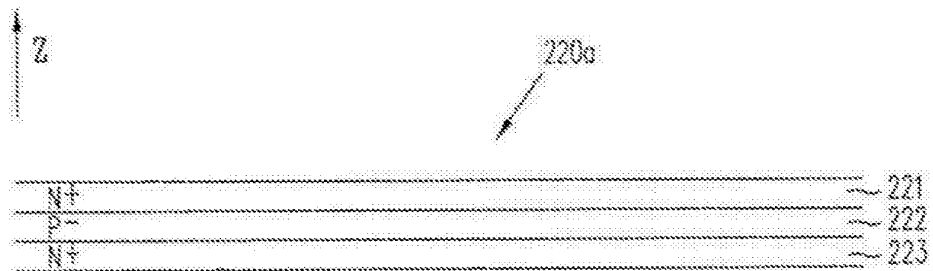


图2b-1

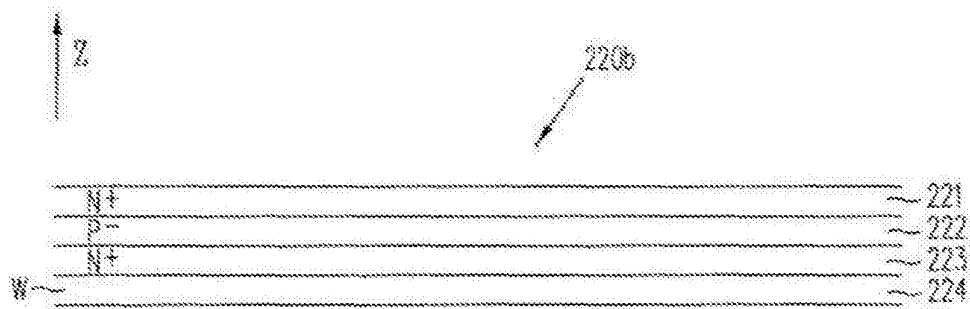


图2b-2

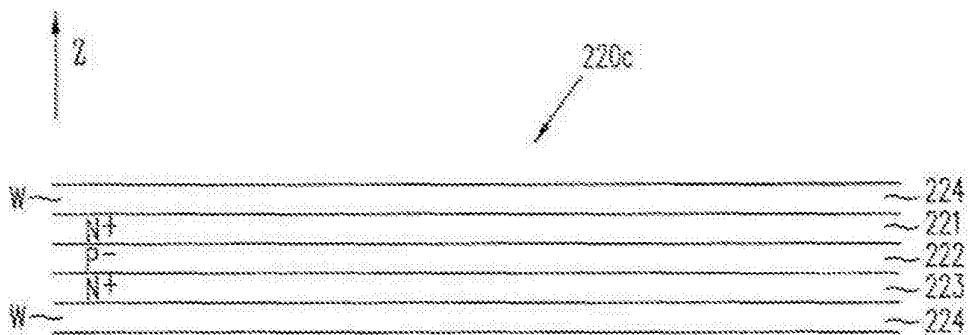


图2b-3

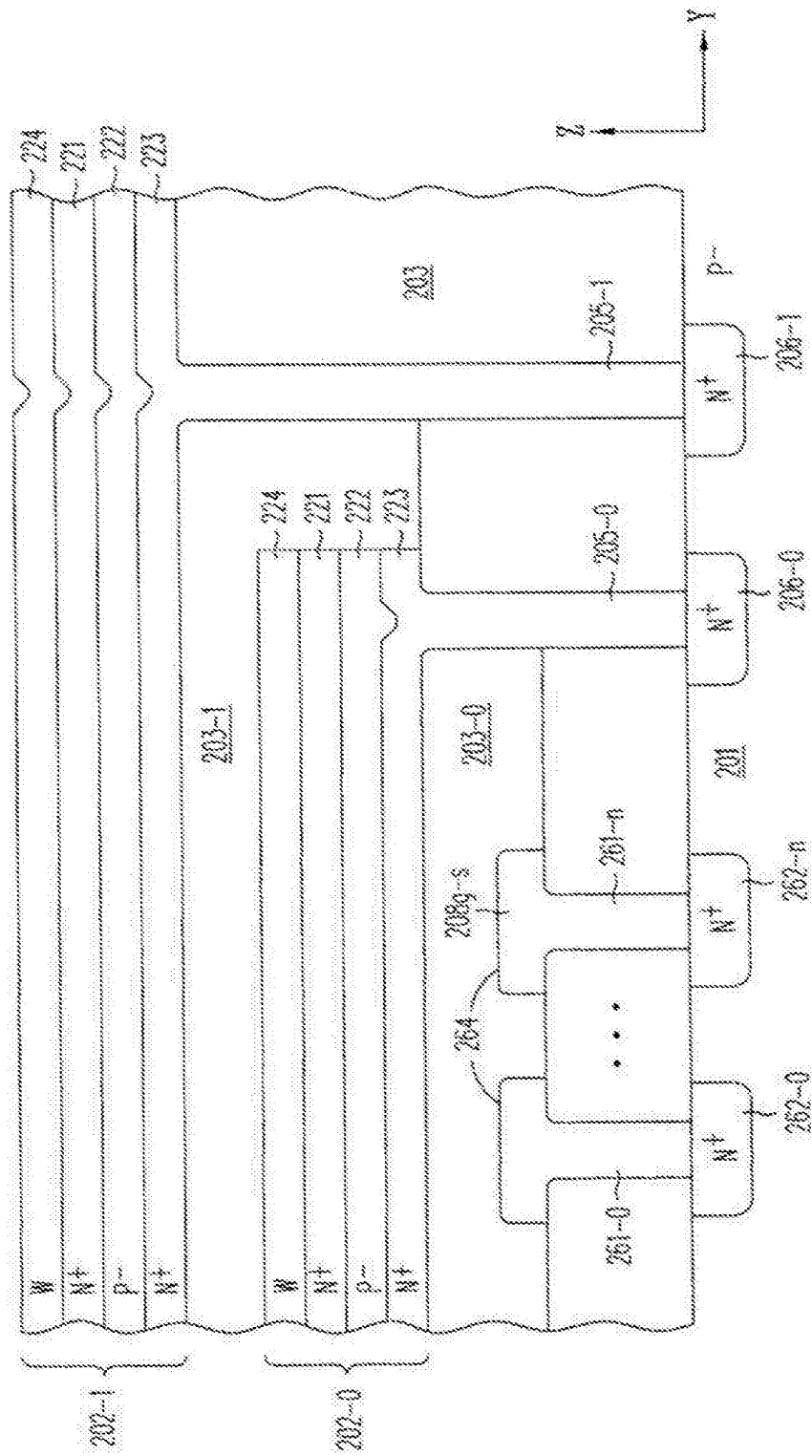


图2c

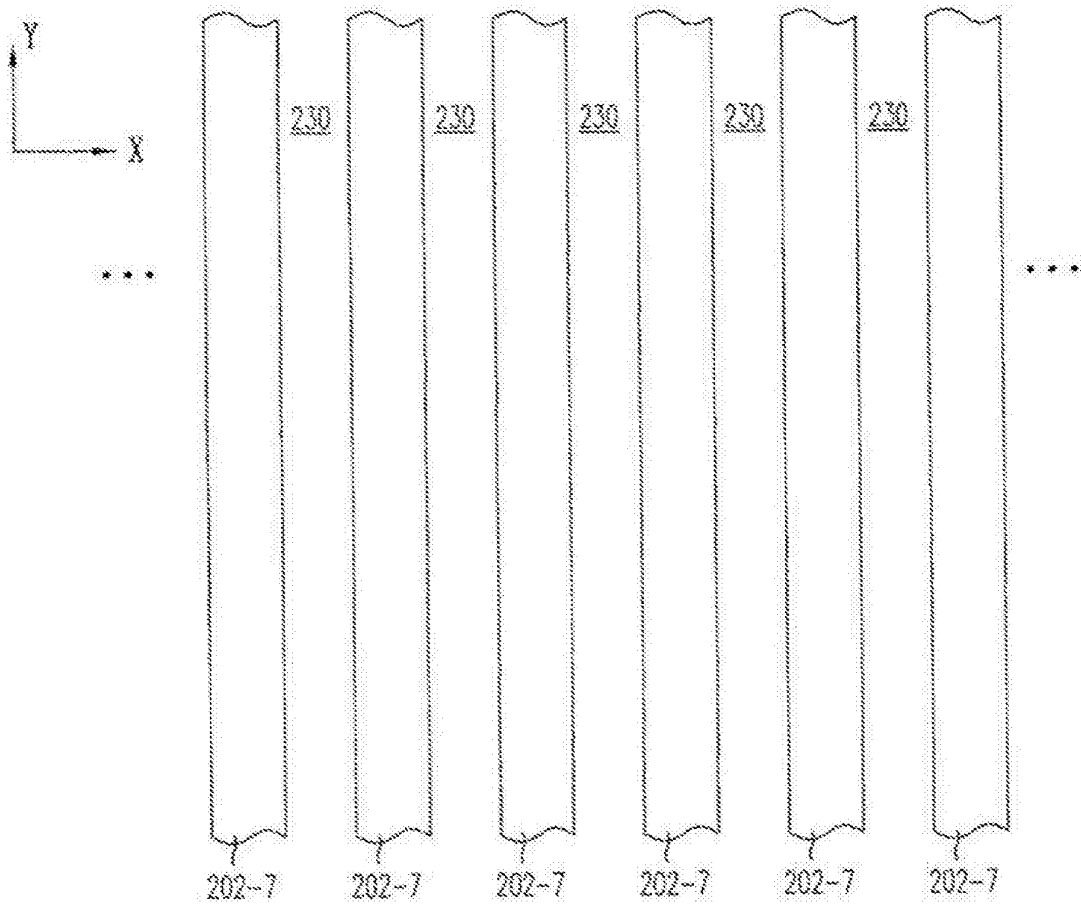


图2d

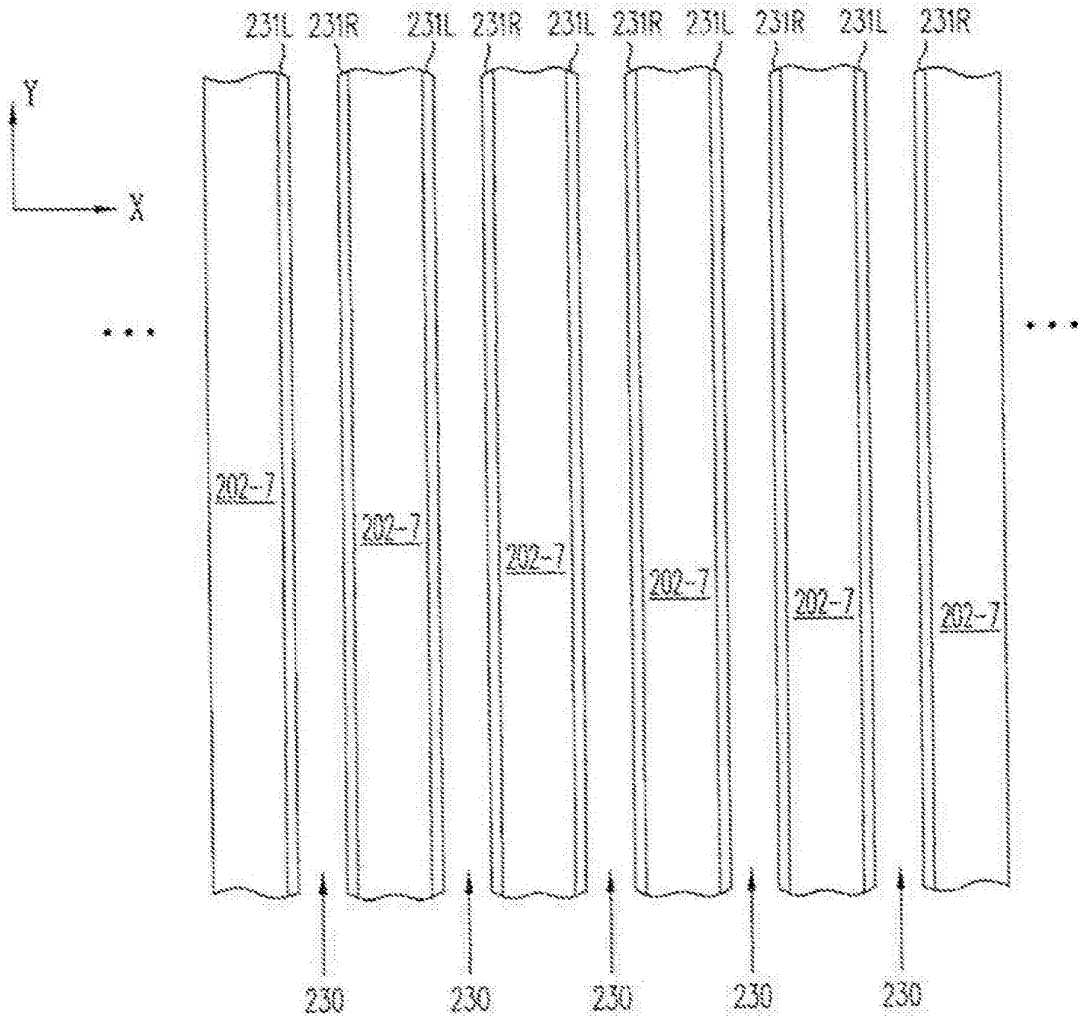


图2e

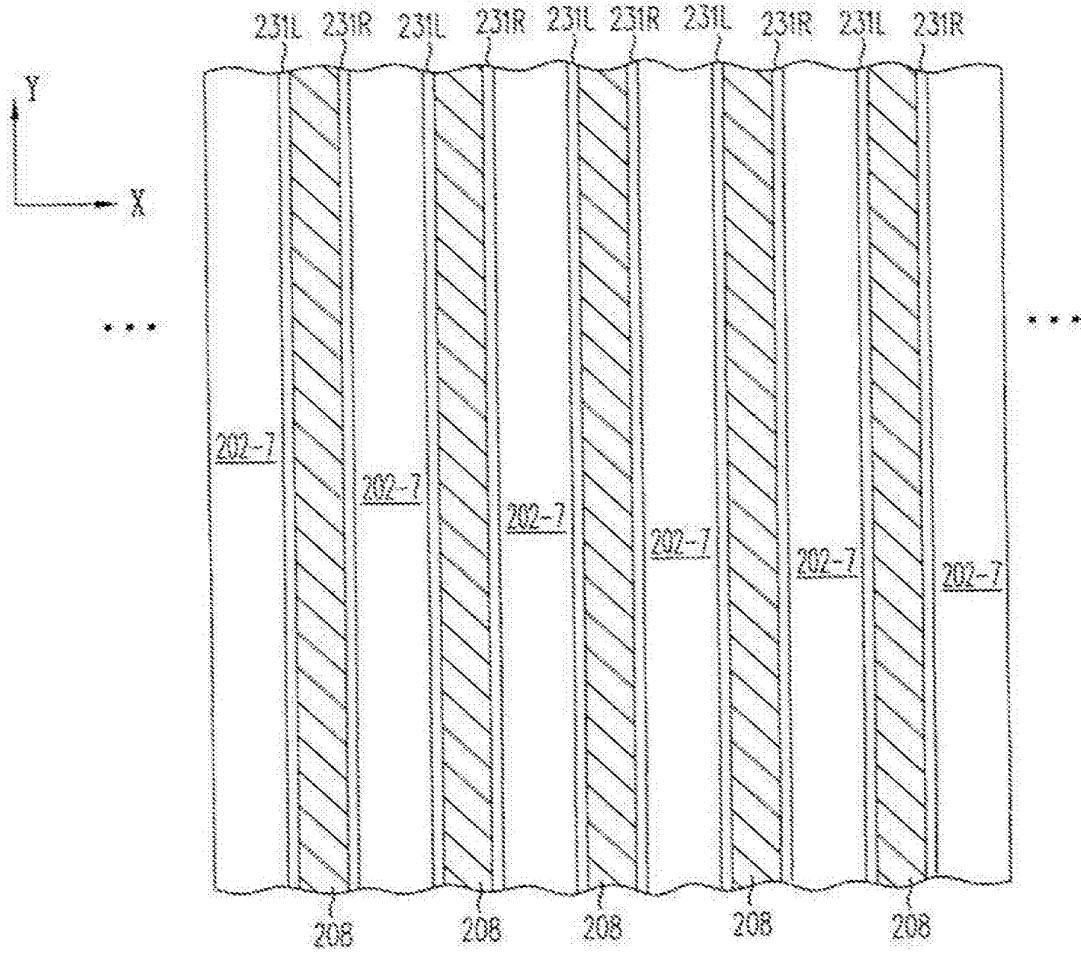


图2f

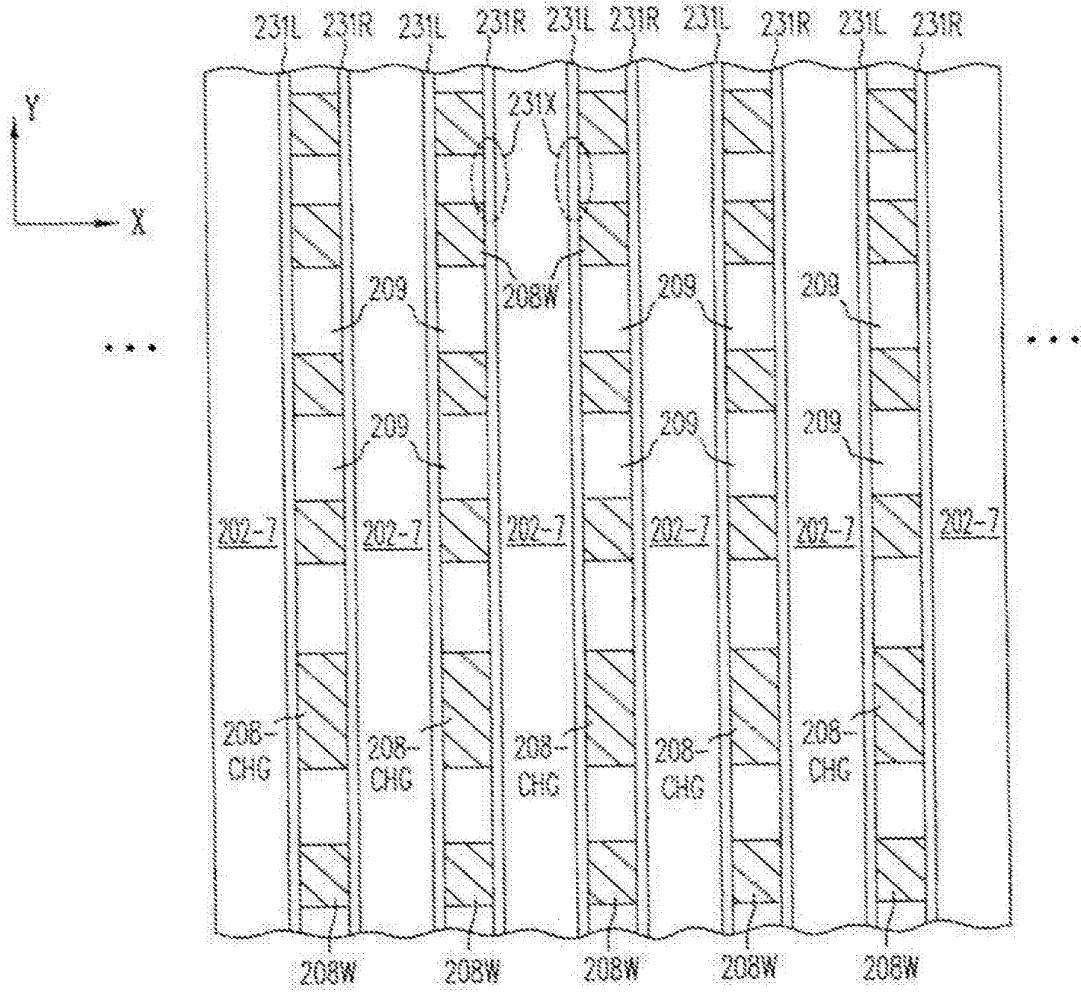


图2g

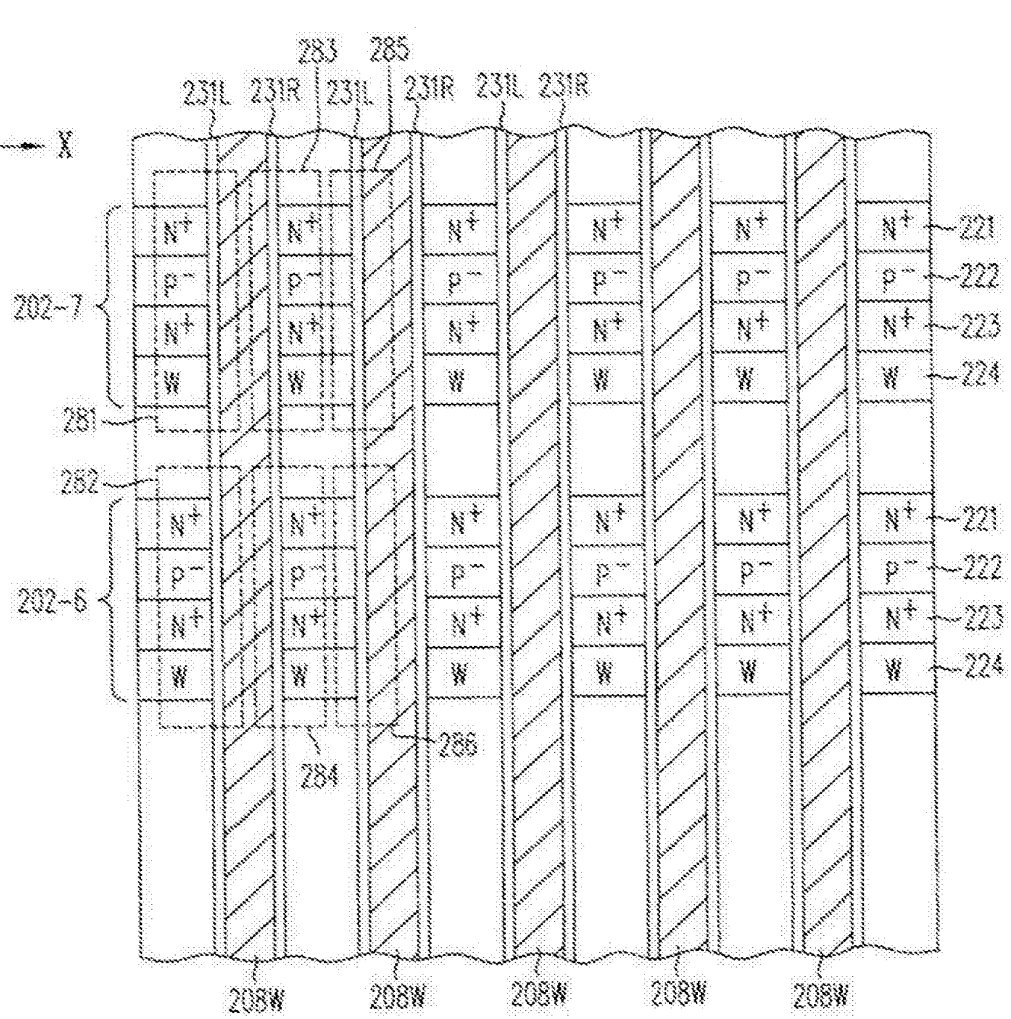


图2h

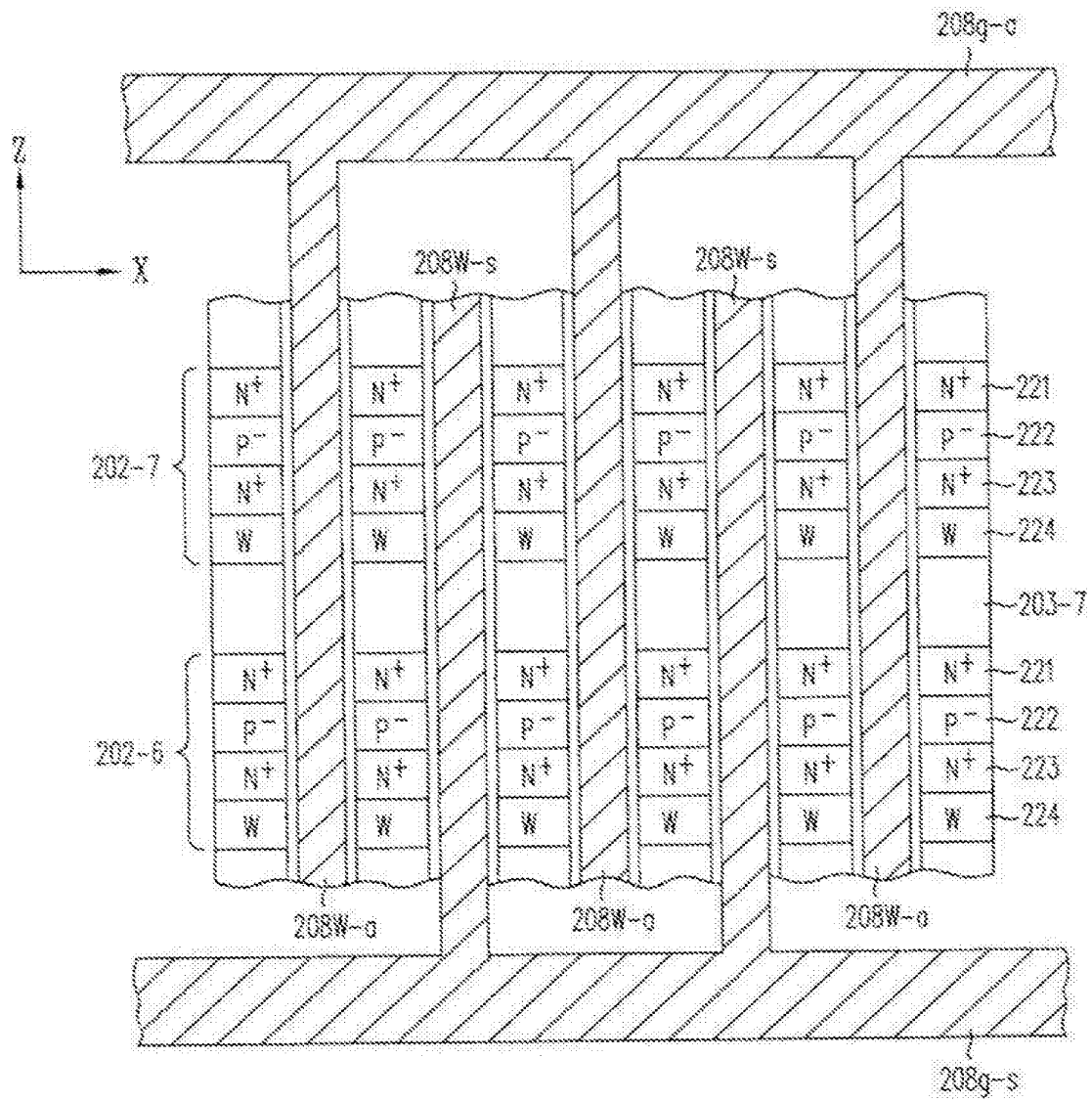


图2i

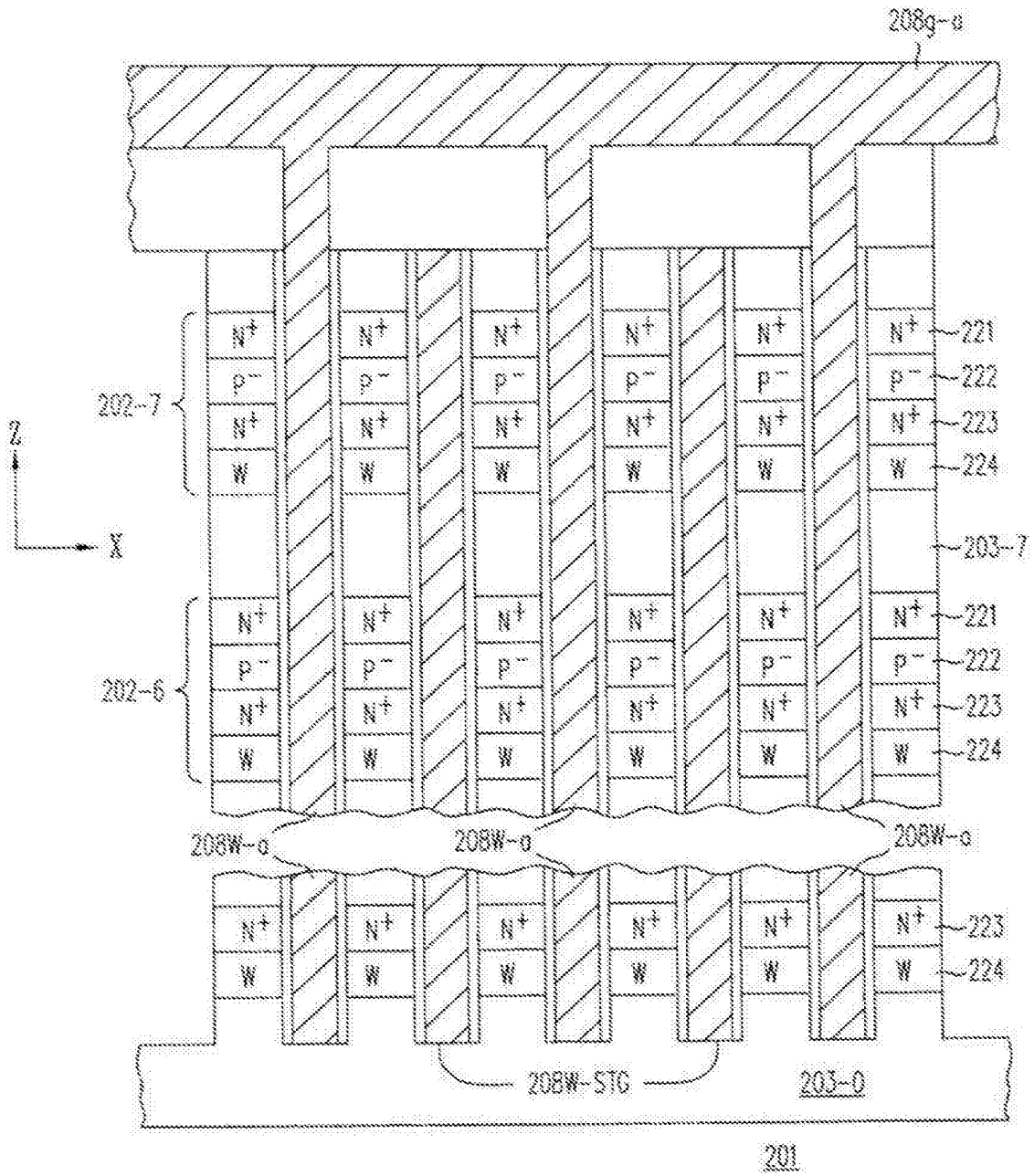


图2j

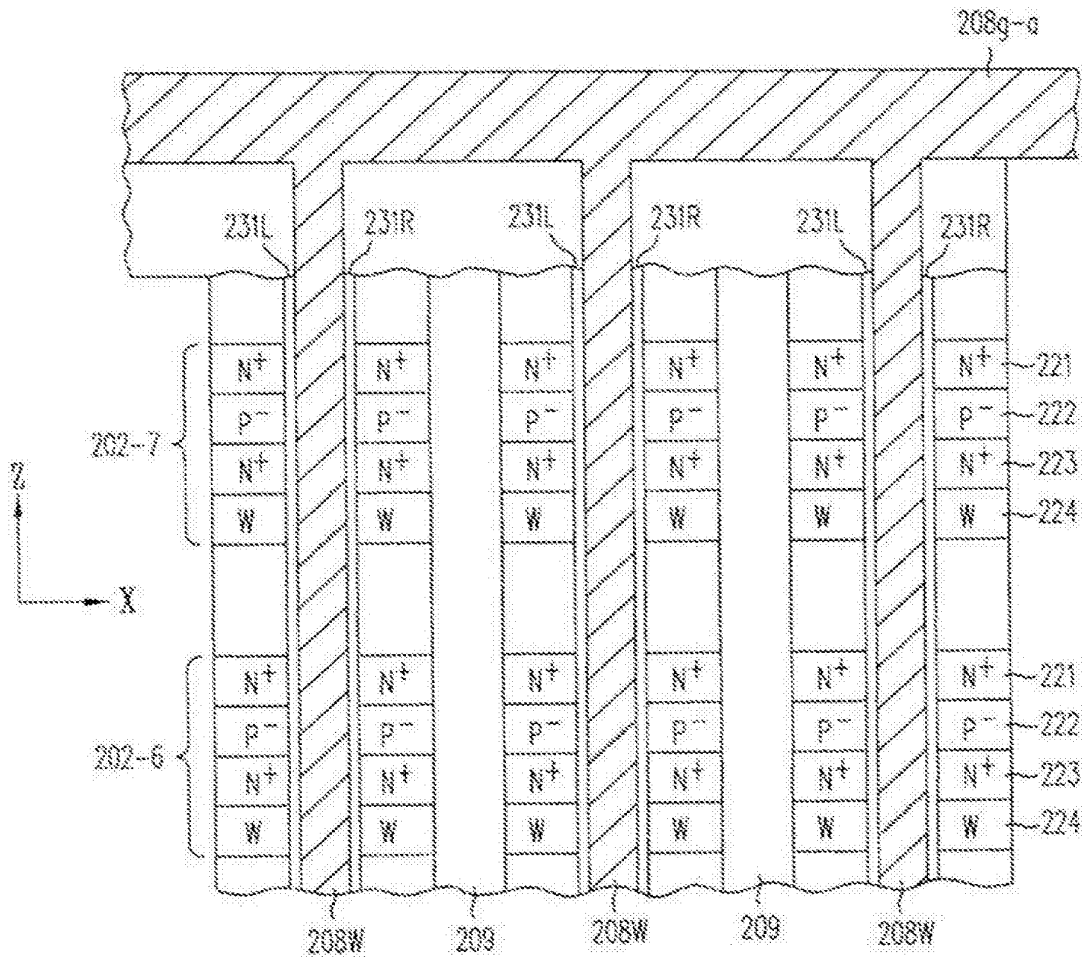


图2k

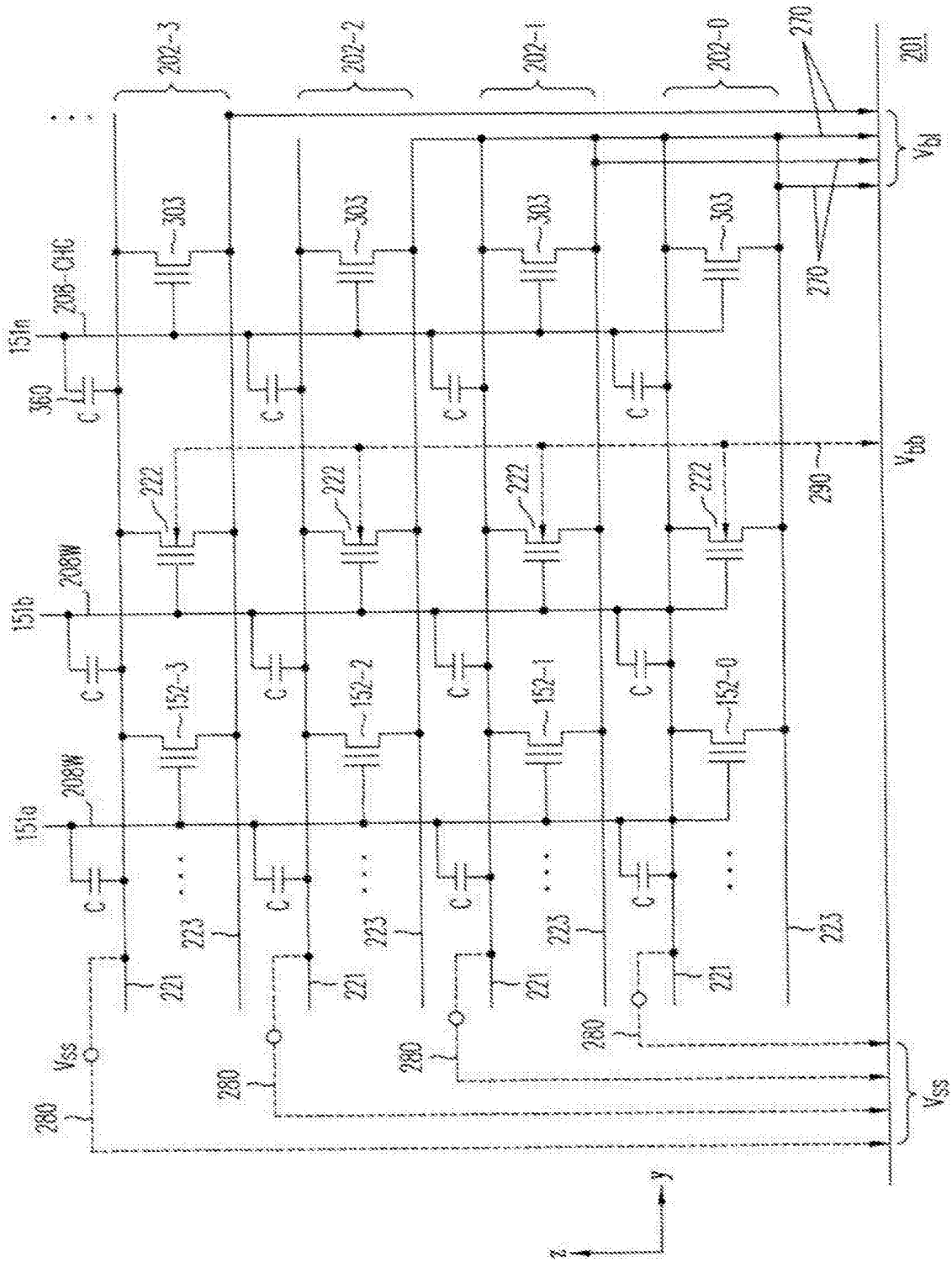


图3

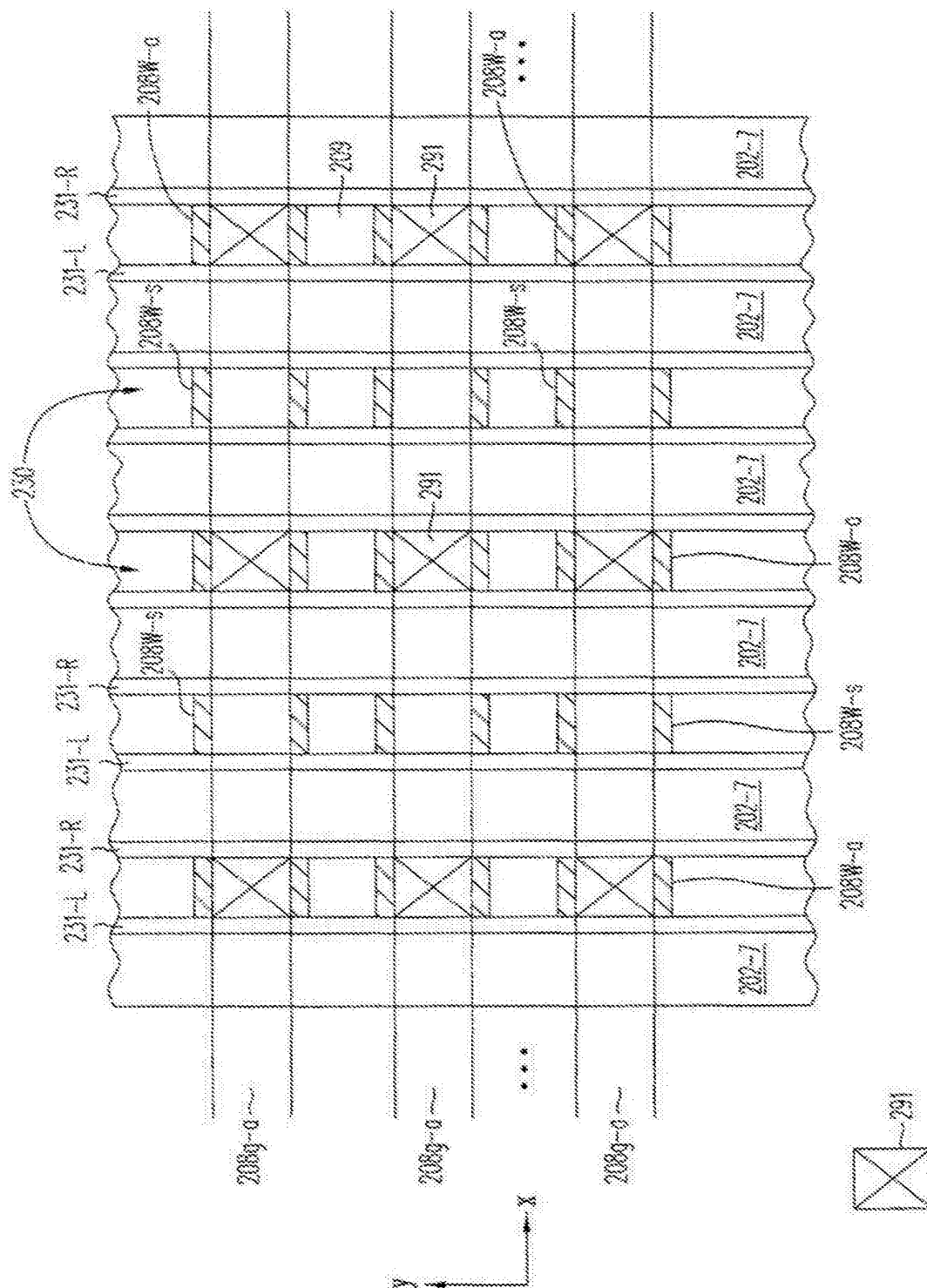


图4a

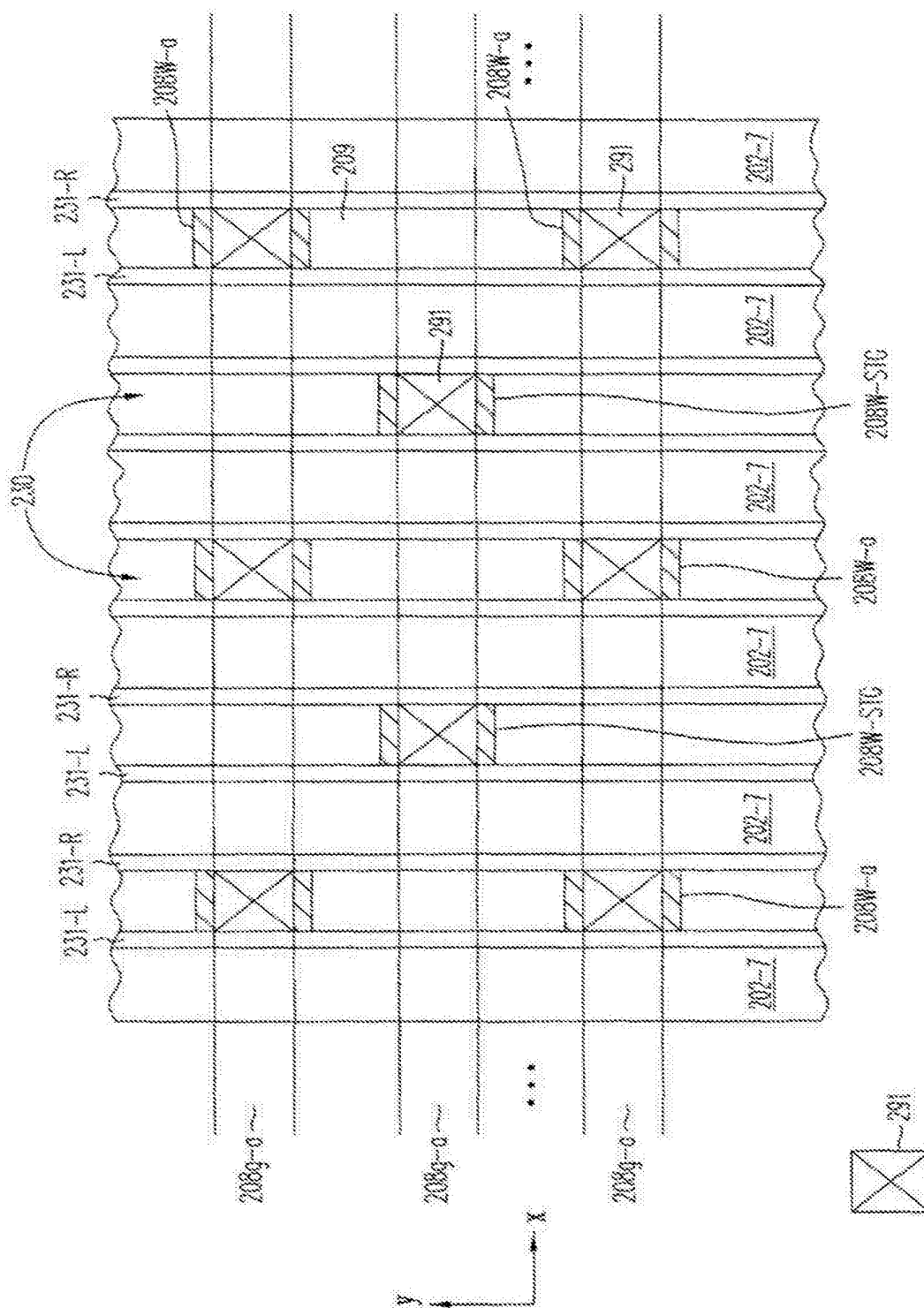


图4b

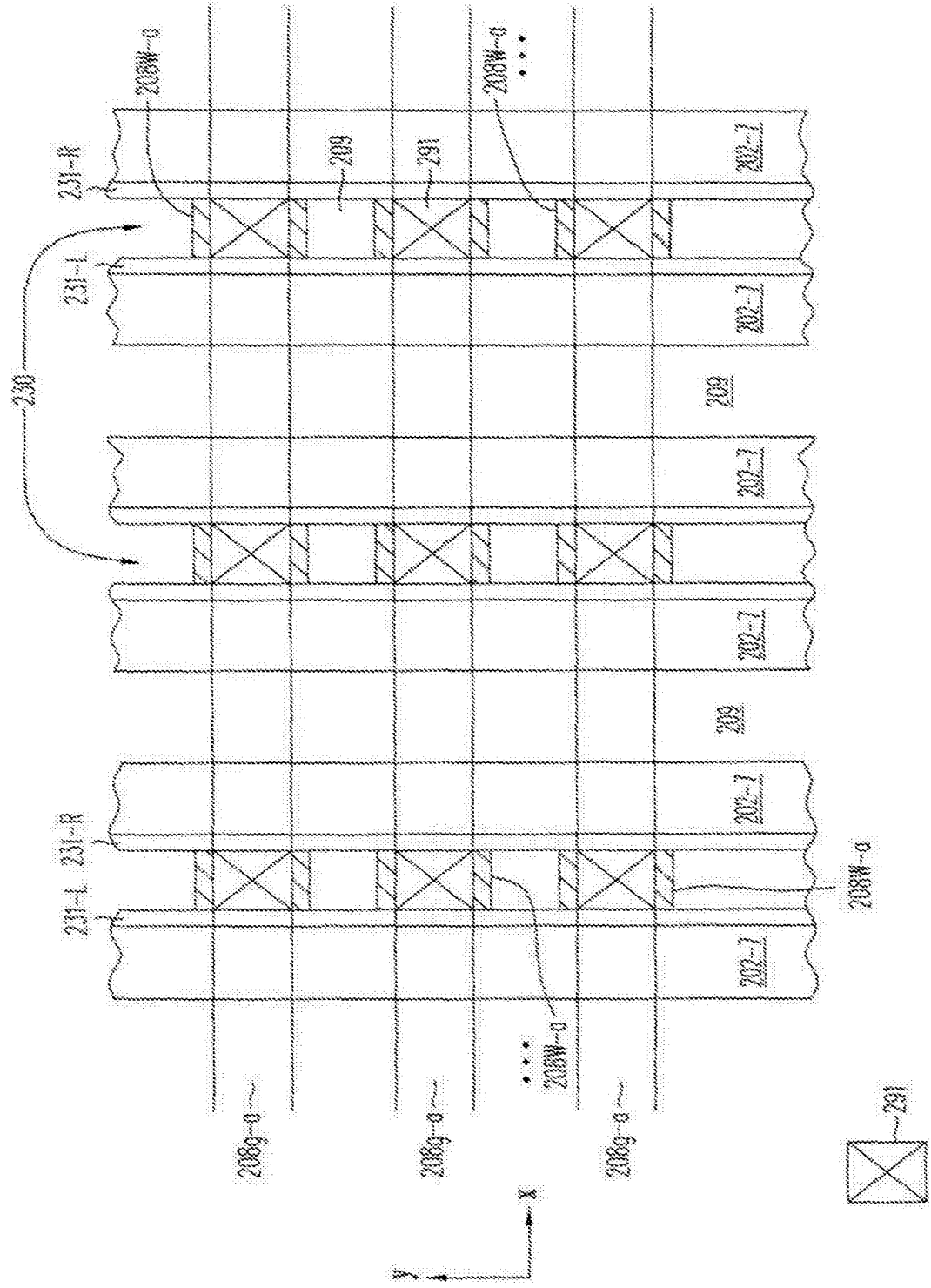


图4c



Espacenet

Bibliographic data: CN109390012 (A) — 2019-02-26
Method and apparatus for removing electrons from oxide layer surface of floating gate memory
Inventor(s): ZHANG SAI; LIU XIAOQING ± (张赛; 刘晓庆)

Applicant(s): GIGADEVICE SEMICONDUCTOR BEIJING INC; HEFEI GEYI INTEGRATED CIRCUIT CO LTD ± (北京兆易创新科技股份有限公司; 合肥格易集成电路有限公司)

Classification: - **international:** **G11C16/04; G11C16/14**
 - **cooperative:** **G11C16/0408 (CN); G11C16/14 (CN)**
Application number: CN201710681531 20170810 Global Dossier
Priority number (s): CN201710681531 20170810

Abstract of CN109390012 (A)

A method and apparatus for removing electrons from a surface of a floating gate memory oxide layer are provided, comprises performing a negative pressure weak erase operation on a storage unit of at least one data stack or at least one data block of all data stacks. A negative pressure weak erase operation includes applying a first voltage to a gate of a memory cell of at least one data stack or at least one data block, A second voltage is applied to the substrate of the memory cells in the at least one data stack or at least one data block, the value of the first voltage being smaller than the value of the second voltage, and the source and drain of the memory cells in the at least one data stack or at least one data block are suspended. The embodiment of the invention provides a method and a device for removing electrons on the oxide layer surface of a floating gate memory. The negative pressure weak erasing operation is carried out on a memory cell to remove electrons captured on the oxide layer surface, thereby solving the problem of degradation of the floating gate memory performance after long-term use and prolonging the service life of the floating gate memory.



(12)发明专利申请

(10)申请公布号 CN 109390012 A

(43)申请公布日 2019.02.26

(21)申请号 201710681531.5

(22)申请日 2017.08.10

(71)申请人 北京兆易创新科技股份有限公司
地址 100083 北京市海淀区学院路30号科大天工大厦A座12层
申请人 合肥格易集成电路有限公司

(72)发明人 张赛 刘晓庆

(74)专利代理机构 北京品源专利代理有限公司
11332
代理人 孟金喆

(51)Int.Cl.
G11C 16/04(2006.01)
G11C 16/14(2006.01)

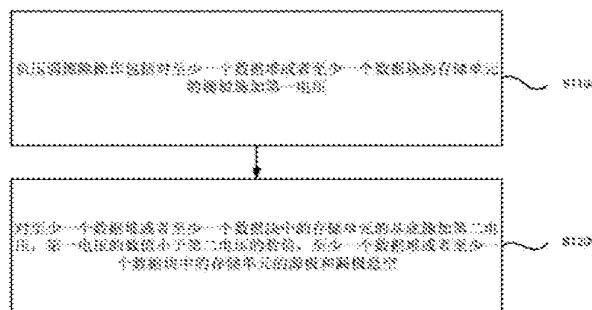
权利要求书2页 说明书6页 附图3页

(54)发明名称

去除浮栅存储器氧化层表面电子的方法及装置

(57)摘要

本发明实施例提供了一种去除浮栅存储器氧化层表面电子的方法及装置,包括:对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,负压弱擦除操作包括对至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,第一电压的数值小于第二电压的数值,至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空。本发明实施例提供了一种去除浮栅存储器氧化层表面电子的方法及装置,对存储单元进行负压弱擦除操作,去除氧化层表面俘获的电子,从而解决长期使用后浮栅存储器性能的衰退问题,延长浮栅存储器的使用寿命。



1. 一种去除浮栅存储器氧化层表面电子的方法,其特征在于,包括:

对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,所述负压弱擦除操作包括对所述至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对所述至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,所述第一电压的数值小于所述第二电压的数值,所述至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空。

2. 根据权利要求1所述的方法,其特征在于,

所述第一电压的数值范围为大于或等于-1V,小于或等于0V;

所述第二电压的数值范围为大于或等于9V,小于或等于10V。

3. 根据权利要求1所述的方法,其特征在于,

所述负压弱擦除操作与上电操作或者擦除操作在同一时间段进行。

4. 根据权利要求3所述的方法,其特征在于,

对所述浮栅存储器进行上电操作和负压弱擦除操作时,还包括记录所述至少一个数据堆或者至少一个数据块的存储单元的地址。

5. 根据权利要求3所述的方法,其特征在于,

对选中数据堆中的选中数据块的存储单元进行擦除操作,所述选中数据堆的个数为1个,所述选中数据块的个数为1个。

6. 根据权利要求3所述的方法,其特征在于,

在所述擦除操作过程中,对所述选中数据堆中的非选中数据块的存储单元进行所述负压弱擦除操作;

对所述选中数据堆中的选中数据块的存储单元的栅极施加第三电压,对所述选中数据堆中的选中数据块中的存储单元的基底施加第四电压,所述第三电压的数值范围小于所述第四电压的数值范围,所述选中数据堆中的选中数据块的存储单元的源极和漏极悬空;

所述第一电压与所述第二电压的差值的绝对值小于所述第三电压与所述第四电压的差值的绝对值。

7. 根据权利要求6所述的方法,其特征在于,

所述第三电压的数值范围为大于或等于-10V,小于或等于-9V;

所述第四电压的数值范围为大于或等于9V,小于或等于10V。

8. 一种去除浮栅存储器氧化层表面电子的装置,其特征在于,包括:

负压弱擦除模块,所述负压弱擦除模块用于对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,所述负压弱擦除操作包括对所述至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对所述至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,所述第一电压的数值小于所述第二电压的数值。

9. 根据权利要求8所述的装置,其特征在于,

所述第一电压的数值范围为大于或等于-1V,小于或等于0V;

所述第二电压的数值范围为大于或等于9V,小于或等于10V。

10. 根据权利要求8所述的装置,其特征在于,

还包括上电模块和擦除模块;

所述上电模块和所述擦除模块分别与所述负压弱擦除模块相连,用于所述负压弱擦除操作与上电操作或者擦除操作在同一时间段进行。

11. 根据权利要求10所述的装置,其特征在于,

还包括记录模块,所述记录模块分别与所述上电模块和所述负压弱擦除模块相连,用于对所述浮栅存储器进行上电操作和负压弱擦除操作时,还包括记录所述至少一个数据堆或者至少一个数据块的存储单元的地址。

12. 根据权利要求10所述的装置,其特征在于,

所述擦除模块对选中数据堆中的选中数据块的存储单元进行擦除操作,所述选中数据堆的个数为1个,所述选中数据块的个数为1个。

13. 根据权利要求10所述的装置,其特征在于,

所述擦除模块在所述擦除操作过程中,所述负压弱擦除模对所述选中数据堆中的非选中数据块的存储单元进行所述负压弱擦除操作;

所述擦除模块对所述选中数据堆中的选中数据块的存储单元的栅极施加第三电压,对所述选中数据堆中的选中数据块中的存储单元的基底施加第四电压,所述第三电压的数值范围小于所述第四电压的数值范围,所述选中数据堆中的选中数据块的存储单元的源极和漏极悬空;

所述第一电压与所述第二电压的差值的绝对值小于所述第三电压与所述第四电压的差值的绝对值。

14. 根据权利要求13所述的装置,其特征在于,

所述第三电压的数值范围为大于或等于-10V,小于或等于-9V;

所述第四电压的数值范围为大于或等于9V,小于或等于10V。

去除浮栅存储器氧化层表面电子的方法及装置

技术领域

[0001] 本发明实施例涉及非易失性存储器技术领域,尤其涉及一种去除浮栅存储器氧化层表面电子的方法及装置。

背景技术

[0002] 浮栅存储器采用浮栅场效应管作为基本的存储单元,浮栅和沟道之间用氧化层隔离。写数据的过程是栅极加正压将电子拉入浮栅中。电子即使在浮栅存储器掉电后,仍然会存留在浮栅中。擦除数据过程则在栅极施压反向电压,通过隧穿效应将电子拉出浮栅。由于浮栅中电子的漏电流,以及多次的写或擦除操作会使得氧化层表面俘获电子,形成电子层。这个电子层会干扰正常的写或擦除操作,从而影响浮栅存储器的性能。但是目前并没有很好的办法来解决这个问题。

发明内容

[0003] 有鉴于此,本发明实施例提供了一种去除浮栅存储器氧化层表面电子的方法及装置,去除氧化层表面俘获的电子,从而解决长期使用后浮栅存储器性能的衰退问题,延长浮栅存储器的使用寿命。

[0004] 第一方面,本发明实施例提供了一种去除浮栅存储器氧化层表面电子的方法,包括:

[0005] 对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,所述负压弱擦除操作包括对所述至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对所述至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,所述第一电压的数值小于所述第二电压的数值,所述至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空。

[0006] 可选的,所述第一电压的数值范围为大于或等于-1V,小于或等于0V;

[0007] 所述第二电压的数值范围为大于或等于9V,小于或等于10V。

[0008] 可选的,所述负压弱擦除操作与上电操作或者擦除操作在同一时间段进行。

[0009] 可选的,对所述浮栅存储器进行上电操作和负压弱擦除操作时,还包括记录所述至少一个数据堆或者至少一个数据块的存储单元的地址。

[0010] 可选的,对选中数据堆中的选中数据块的存储单元进行擦除操作,所述选中数据堆的个数为1个,所述选中数据块的个数为1个。

[0011] 可选的,在所述擦除操作过程中,对所述选中数据堆中的非选中数据块的存储单元进行所述负压弱擦除操作;

[0012] 对所述选中数据堆中的选中数据块的存储单元的栅极施加第三电压,对所述选中数据堆中的选中数据块中的存储单元的基底施加第四电压,所述第三电压的数值范围小于所述第四电压的数值范围,所述选中数据堆中的选中数据块的存储单元的源极和漏极悬空;

[0013] 所述第一电压与所述第二电压的差值的绝对值小于所述第三电压与所述第四电压的差值的绝对值。

[0014] 可选的,所述第三电压的数值范围为大于或等于-10V,小于或等于-9V;

[0015] 所述第四电压的数值范围为大于或等于9V,小于或等于10V。

[0016] 第二方面,本发明实施例提供了一种去除浮栅存储器氧化层表面电子的装置,包括:

[0017] 负压弱擦除模块,所述负压弱擦除模块用于对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,所述负压弱擦除操作包括对所述至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对所述至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,所述第一电压的数值小于所述第二电压的数值。

[0018] 可选的,所述第一电压的数值范围为大于或等于-1V,小于或等于0V;

[0019] 所述第二电压的数值范围为大于或等于9V,小于或等于10V。

[0020] 可选的,还包括上电模块和擦除模块;

[0021] 所述上电模块和所述擦除模块分别与所述负压弱擦除模块相连,用于所述负压弱擦除操作与上电操作或者擦除操作在同一时间段进行。

[0022] 可选的,还包括记录模块,所述记录模块分别与所述上电模块和所述负压弱擦除模块相连,用于对所述浮栅存储器进行上电操作和压弱擦除操作时,还包括记录所述至少一个数据堆或者至少一个数据块的存储单元的地址。

[0023] 可选的,所述擦除模块对选中数据堆中的选中数据块的存储单元进行擦除操作,所述选中数据堆的个数为1个,所述选中数据块的个数为1个。

[0024] 可选的,所述擦除模块在所述擦除操作过程中,所述负压弱擦除模对所述选中数据堆中的非选中数据块的存储单元进行所述负压弱擦除操作;

[0025] 所述擦除模块对所述选中数据堆中的选中数据块的存储单元的栅极施加第三电压,对所述选中数据堆中的选中数据块中的存储单元的基底施加第四电压,所述第三电压的数值范围小于所述第四电压的数值范围,所述选中数据堆中的选中数据块的存储单元的源极和漏极悬空;

[0026] 所述第一电压与所述第二电压的差值的绝对值小于所述第三电压与所述第四电压的差值的绝对值。

[0027] 可选的,所述第三电压的数值范围为大于或等于-10V,小于或等于-9V;

[0028] 所述第四电压的数值范围为大于或等于9V,小于或等于10V。

[0029] 本发明实施例提供的去除浮栅存储器氧化层表面电子的方法及装置,对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,即对至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,第一电压的数值小于第二电压的数值,至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空,总的来说,是在基底和栅极之间形成了一个电场,该电场方向是从基底指向栅极的,因此电子便会在电场力的作用下,从隧穿氧化层中被拉出来,脱离隧穿氧化层中缺陷的捕获,从而解决长期使用后浮栅存储器性能的衰退问题,延长浮栅存储器的使用寿命。

附图说明

[0030] 图1为本发明实施例一提供的一种去除浮栅存储器氧化层表面电子的方法的流程示意图；

[0031] 图2为本发明实施例一提供的一种浮栅存储器的结构示意图；

[0032] 图3为本发明实施例二提供的一种去除浮栅存储器氧化层表面电子的方法的流程示意图；

[0033] 图4为本发明实施例三提供的一种去除浮栅存储器氧化层表面电子的方法的流程示意图；

[0034] 图5所示为本发明实施例四提供的一种去除浮栅存储器氧化层表面电子的装置的结构示意图。

具体实施方式

[0035] 下面结合附图和实施例对本发明作进一步的详细说明。可以理解的是，此处所描述的具体实施例仅仅用于解释本发明，而非对本发明的限定。另外还需要说明的是，为了便于描述，附图中仅示出了与本发明相关的部分而非全部结构。

[0036] 实施例一

[0037] 图1为本发明实施例提供的一种去除浮栅存储器氧化层表面电子的方法的流程示意图，该装置可以由去除浮栅存储器氧化层表面电子的装置来执行，其中该装置可由硬件和/或软件来实现，具体包括如下步骤：

[0038] 对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作。

[0039] 步骤110、负压弱擦除操作包括对至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压。

[0040] 步骤120、对至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压，第一电压的数值小于第二电压的数值，至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空。

[0041] 在本实施例中，浮栅存储器包括多个存储单元，可以分为划分为多个数据堆，每一个数据堆可以划分为多个数据块，每一个数据块可以划分为多个数据页，每一个数据页可以划分为多个存储单元。

[0042] 在本实施中，参见图2，浮栅存储器包括半导体基底1、源极2、漏极3、隧穿氧化层4、浮栅5、层间绝缘层6、控制栅7以及控制栅7表面的金属层栅极8。隧穿氧化层的材料选取可以是氧化硅、氮化硅或者氧化硅和氮化硅的叠层。在浮栅存储器的使用过程，在编程操作的过程中，电子从隧穿氧化层进入到浮栅中，用于存储数据。在擦除操作的过程中，电子从浮栅经过隧穿氧化层被拉离到基底所在的区域。在多次的编程操作和擦除操作后，隧穿氧化层中会出现一些缺陷，这些缺陷在电子进出隧穿氧化层的时候会被缺陷所捕获，从而形成电子层。由于浮栅存储器主要是依据浮栅中的电子来决定其阈值电压，那么隧穿氧化层中的电子层势必会对存储器的电学性能造成影响。本发明实施例提供的去除浮栅存储器氧化层表面电子的方法，对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进

行负压弱擦除操作,即对至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,第一电压的数值小于第二电压的数值,至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空,总的来说,是在基底和栅极之间形成了一个电场,该电场方向是从基底指向栅极的,因此电子便会在电场力的作用下,从隧穿氧化层中被拉出来,脱离隧穿氧化层中缺陷的捕获,从而解决长期使用后浮栅存储器性能的衰退问题,延长浮栅存储器的使用寿命。

[0043] 实施例二

[0044] 图3为本发明实施例提供的一种去除浮栅存储器氧化层表面电子的方法的流程示意图。本实施例在上述实施例的基础上,限定了负压弱擦除操作与上电操作在同一时间段进行,如图3所示,该方法具体包括如下步骤:

[0045] 步骤210、对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,负压弱擦除操作包括对至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,第一电压的数值小于第二电压的数值,至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空,负压弱擦除操作与上电操作在同一时间段进行。

[0046] 可选的,第一电压的数值范围为大于或等于-1V,小于或等于0V;第二电压的数值范围为大于或等于9V,小于或等于10V。

[0047] 在本实施例中,上电操作是指给浮栅存储器接上外接电源的过程。浮栅存储器的控制器一般会选取微控制单元(Microcontroller Unit,MCU),MCU需要接的电压的数值大约为1.8V。上电的过程是指外接电源供给MCU电源,MCU将电压信号接到浮栅存储器的过程。上电过程持续的时间可以选择对浮栅存储器进行负压弱擦除操作,节省时间,还使得电子在负压弱擦除操作形成的电场力的作用下,从隧穿氧化层中被拉出来,脱离隧穿氧化层中缺陷的捕获,从而解决长期使用后浮栅存储器性能的衰退问题,延长浮栅存储器的使用寿命。

[0048] 步骤220、对浮栅存储器进行上电操作和负压弱擦除操作时,记录至少一个数据堆或者至少一个数据块的存储单元的地址。

[0049] 在本实施例中,客户一般会对浮栅存储器的存储性能例如运行速度提出要求。那么浮栅存储器的运行速度越快的话,负压若擦除的操作的单位就要越小。比如说,上电过程中,只针对一个数据块进行负压弱擦除操作,那么运行速度大于对于多个数据块或者数据堆进行负压弱擦除操作。具体的,可以根据对于存储器的性能需求进行自行选择。而记录下地址,则是方便下一次上电的时候对于其他存储单元继续进行负压弱擦除操作。

[0050] 本发明实施例上电过程持续的时间可以选择对浮栅存储器进行负压弱擦除操作,节省时间,还使得电子在负压弱擦除操作形成的电场力的作用下,从隧穿氧化层中被拉出来,脱离隧穿氧化层中缺陷的捕获,从而解决长期使用后浮栅存储器性能的衰退问题,延长浮栅存储器的使用寿命。

[0051] 实施例三

[0052] 图4为本发明实施例提供的一种去除浮栅存储器氧化层表面电子的方法的流程示意图。本实施例在上述实施例的基础上,限定了负压弱擦除操作与上电操作在同一时间段进行,如图4所示,该方法具体包括如下步骤:

[0053] 步骤310、负压弱擦除操作与擦除操作在同一时间段进行。

[0054] 步骤320、对选中数据堆中的选中数据块的存储单元进行擦除操作,选中数据堆的个数为1个,选中数据块的个数为1个。

[0055] 其中,在擦除操作过程中,对选中数据堆中的非选中数据块的存储单元进行负压弱擦除操作;对选中数据堆中的选中数据块的存储单元的栅极施加第三电压,对选中数据堆中的选中数据块中的存储单元的基底施加第四电压,第三电压的数值范围小于第四电压的数值范围,选中数据堆中的选中数据块的存储单元的源极和漏极悬空;第一电压与第二电压的差值的绝对值小于第三电压与第四电压的差值的绝对值。

[0056] 其中,对选中数据堆中的非选中数据块的存储单元进行负压弱擦除操作,负压弱擦除操作包括对选中数据堆中的非选中数据块的存储单元的栅极施加第一电压,对选中数据堆中的非选中数据块的存储单元的基底施加第二电压,第一电压的数值小于第二电压的数值,至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空。

[0057] 可选的,第一电压的数值范围为大于或等于-1V,小于或等于0V;第二电压的数值范围为大于或等于9V,小于或等于10V。

[0058] 可选的,第三电压的数值范围为大于或等于-10V,小于或等于-9V;

[0059] 第四电压的数值范围为大于或等于9V,小于或等于10V。

[0060] 本发明实施例提供的去除浮栅存储器氧化层表面电子的方法,对于选中数据块的存储单元,在第三电压和第四电压形成的电场下,可以被执行擦除操作。与此同时,对于非选中数据块的存储单元,在第一电压和第二电压形成的电场下,电子在电场力的作用下,从隧穿氧化层中被拉出来,脱离隧穿氧化层中缺陷的捕获,从而解决长期使用后浮栅存储器性能的衰退问题,延长浮栅存储器的使用寿命。

[0061] 需要说明的是,本发明实施例提供的去除浮栅存储器氧化层表面电子的方法,可以是上电过程负压弱擦除操作同时进行,在后续的擦除操作过程中,可以同时进行负压弱擦除操作。

[0062] 实施例四

[0063] 图5所示为本发明实施例四提供的一种去除浮栅存储器氧化层表面电子的装置的结构示意图,该装置可由硬件实现,如图5所示,该装置包括:

[0064] 负压弱擦除模块410,负压弱擦除模块410用于对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,负压弱擦除操作包括对至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,第一电压的数值小于第二电压的数值。

[0065] 本发明实施例提供的去除浮栅存储器氧化层表面电子的装置,通过负压弱擦除模块410,对所有数据堆中的至少一个数据堆或者至少一个数据块的存储单元进行负压弱擦除操作,即对至少一个数据堆或者至少一个数据块的存储单元的栅极施加第一电压,对至少一个数据堆或者至少一个数据块中的存储单元的基底施加第二电压,第一电压的数值小于第二电压的数值,至少一个数据堆或者至少一个数据块中的存储单元的源极和漏极悬空,总的来说,是在基底和栅极之间形成了一个电场,该电场方向是从基底指向栅极的,因此电子便会在电场力的作用下,从隧穿氧化层中被拉出来,脱离隧穿氧化层中缺陷的捕获,从而解决长期使用后浮栅存储器性能的衰退问题,延长浮栅存储器的使用寿命。

[0066] 可选的,第一电压的数值范围为大于或等于-1V,小于或等于0V;

[0067] 第二电压的数值范围为大于或等于9V,小于或等于10V。

[0068] 在上述技术方案的基础上,可选的,该装置还包括上电模块420和擦除模块430;上电模块420和擦除模块430分别与负压弱擦除模块410相连,用于负压弱擦除操作与上电操作或者擦除操作在同一时间段进行。

[0069] 可选的,在上述技术方案的基础上,该装置还包括记录模块440,记录模块440分别与上电模块420和负压弱擦除模块410相连,用于对浮栅存储器进行上电操作和负压弱擦除操作时,还包括记录至少一个数据堆或者至少一个数据块的存储单元的地址。

[0070] 可选的,在上述技术方案的基础上,擦除模块430对选中数据堆中的选中数据块的存储单元进行擦除操作,选中数据堆的个数为1个,选中数据块的个数为1个。

[0071] 可选的,在上述技术方案的基础上,擦除模块430在擦除操作过程中,负压弱擦除模块对选中数据堆中的非选中数据块的存储单元进行负压弱擦除操作;

[0072] 擦除模块430对选中数据堆中的选中数据块的存储单元的栅极施加第三电压,对选中数据堆中的选中数据块中的存储单元的基底施加第四电压,第三电压的数值范围小于第四电压的数值范围,选中数据堆中的选中数据块的存储单元的源极和漏极悬空;

[0073] 第一电压与第二电压的差值的绝对值小于第三电压与第四电压的差值的绝对值。

[0074] 可选的,在上述技术方案的基础上,第三电压的数值范围为大于或等于-10V,小于或等于-9V;第四电压的数值范围为大于或等于9V,小于或等于10V。

[0075] 上述实施例中提供的去除浮栅存储器氧化层表面电子的装置可执行本发明任意实施例所提供的去除浮栅存储器氧化层表面电子的方法,具备执行该方法相应的功能模块和有益效果。未在上述实施例中详尽描述的技术细节,可参见本发明任意实施例所提供的去除浮栅存储器氧化层表面电子的方法。

[0076] 注意,上述仅为本发明的较佳实施例及所运用技术原理。本领域技术人员会理解,本发明不限于这里所述的特定实施例,对本领域技术人员来说能够进行各种明显的变化、重新调整、相互结合和替代而不会脱离本发明的保护范围。因此,虽然通过以上实施例对本发明进行了较为详细的说明,但是本发明不仅仅限于以上实施例,在不脱离本发明构思的情况下,还可以包括更多其他等效实施例,而本发明的范围由所附的权利要求范围决定。

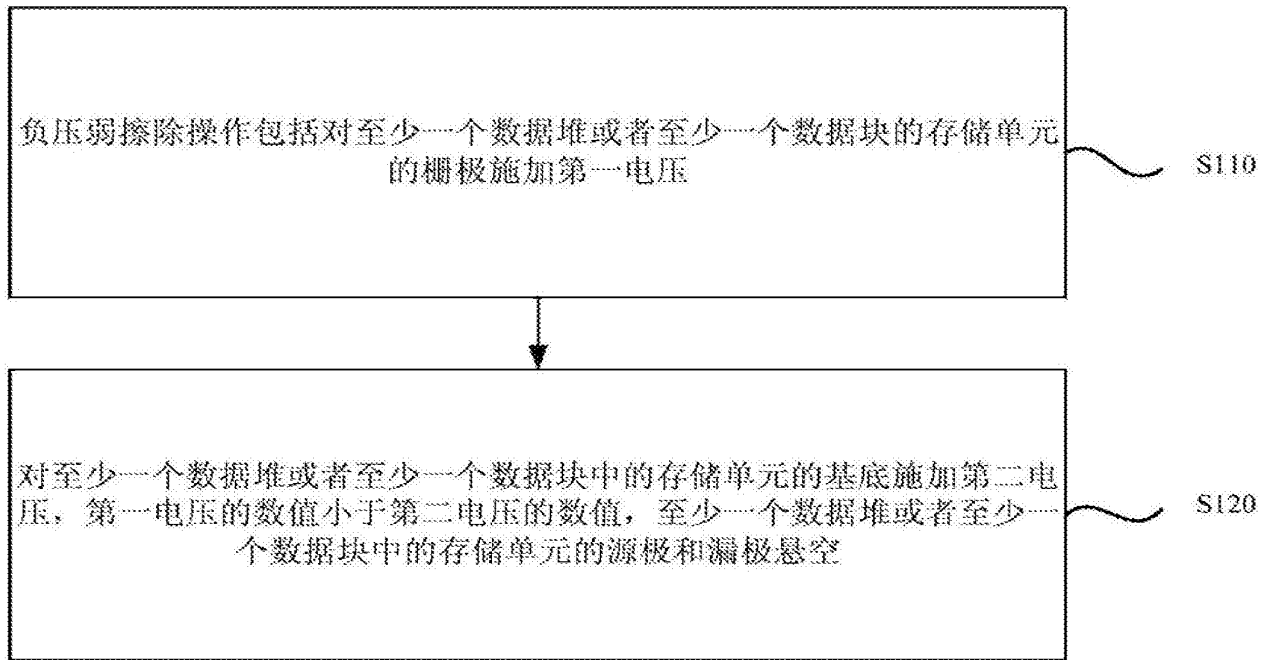


图1

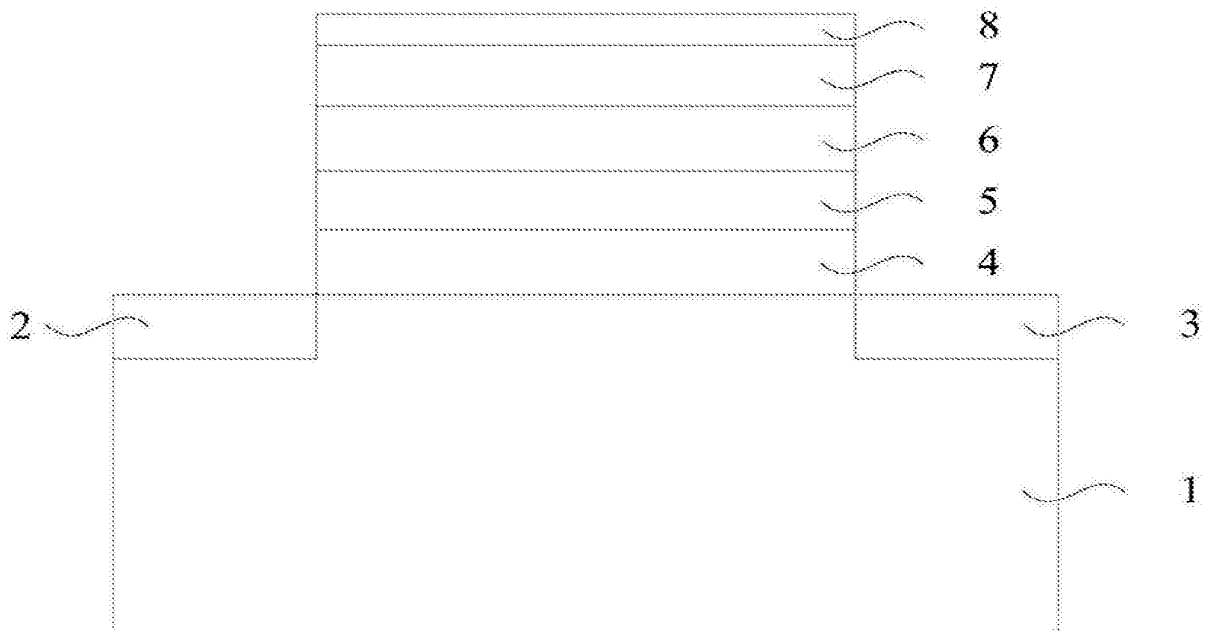


图2

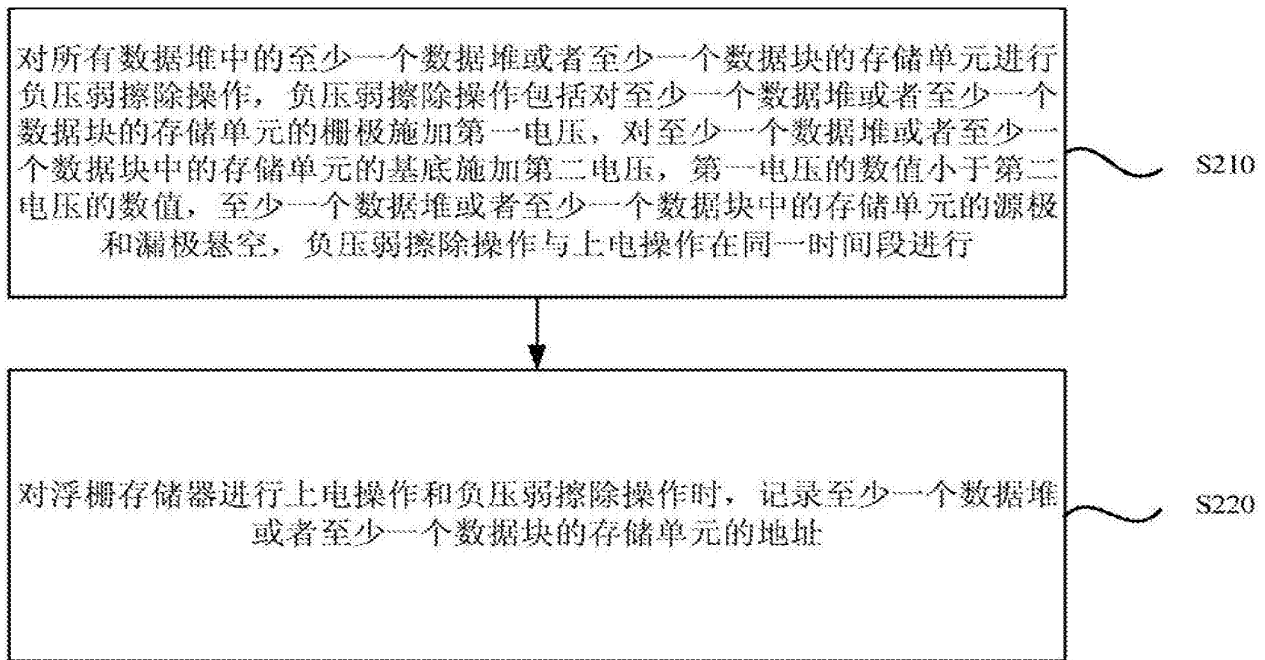


图3

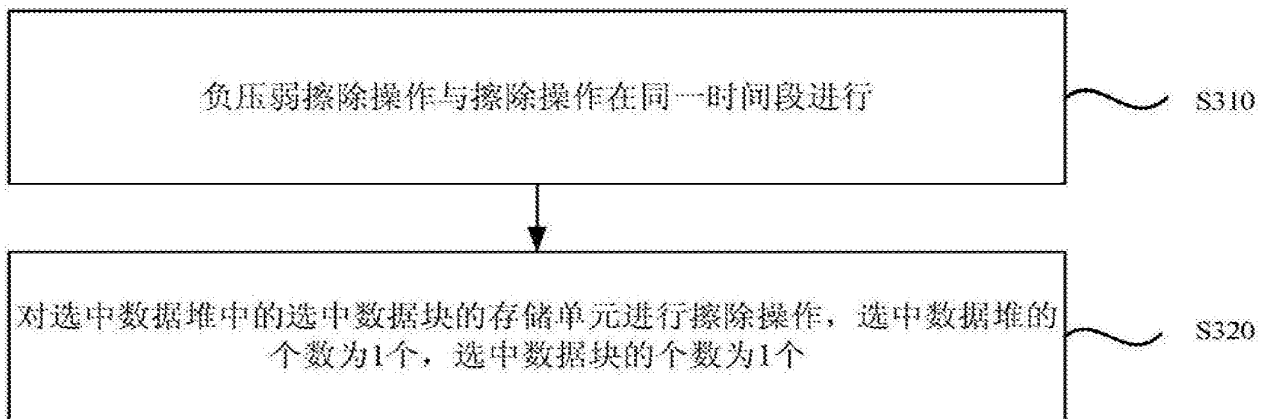


图4

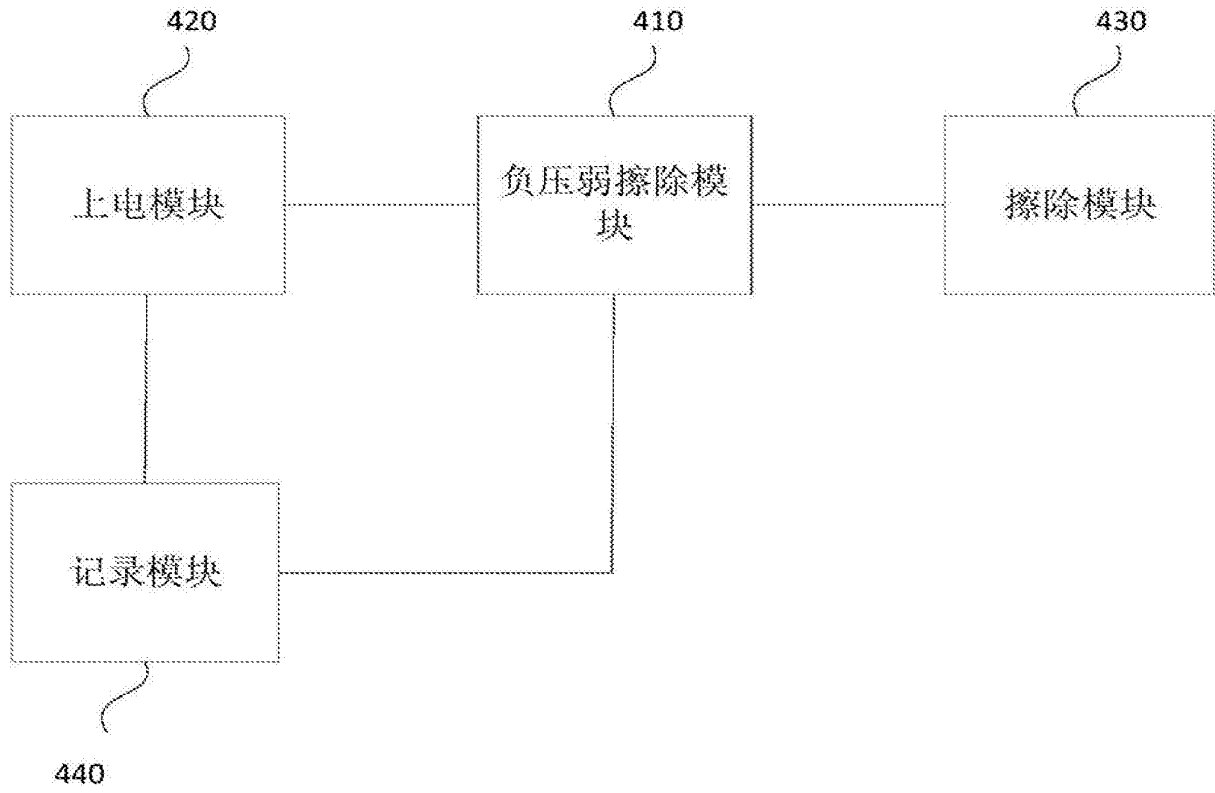


图5

Electronic Acknowledgement Receipt	
EFS ID:	40861418
Application Number:	16729838
International Application Number:	
Confirmation Number:	5773
Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Min Yang/Jon Baitlon
Filer Authorized By:	Min Yang
Attorney Docket Number:	4123.0850001
Receipt Date:	16-OCT-2020
Filing Date:	30-DEC-2019
Time Stamp:	12:19:02
Application Type:	Utility under 35 USC 111(a)

Payment information:					
Submitted with Payment			no		
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	IDS-Cover-Letter-4123-0850001.pdf	271511	no	1
			1326ad6026c25e6162f208ab3b06848d20dae120		
Warnings:					

Information:					
2	Transmittal Letter	IDS-Pleading-4123-0850001.pdf	129068	no	7
			a3ab0f47f79424bec8b114c4eaa9523ac7344941		
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	IDS-SB08A-4123-0850001.pdf	154084	no	1
			e509e7e427fed65b77a01b99211fdedd215bc7d0		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Foreign Reference	FP1_CN102760490A.pdf	101523	no	13
			cac54aba818794c1f33351beb3e3f330f26665fd		
Warnings:					
Information:					
5	Foreign Reference	FP2_CN108140415A.pdf	794905	no	38
			f1293303c7b038cda22db86ec52053f6aa432f53		
Warnings:					
Information:					
6	Foreign Reference	FP3_CN109390012A.pdf	225571	no	13
			66ebe95f6d106356f7b28d68b863418fe67ceb33		
Warnings:					
Information:					
Total Files Size (in bytes):			1676662		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

MIN YANG, PH.D.
PATENT AGENT
(202) 772-8702
MYANG@STERNEKESSLER.COM

October 16, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 5773
Art Unit 2827
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 16/729,838; Filing Date: December 30, 2019
For: **METHOD FOR READING THREE-DIMENSIONAL FLASH
MEMORY**
Inventors: CHEN *et al.*
Our Ref: 4123.0850001

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;
2. Form PTO/SB/08a (1 sheet) listing 8 documents (**US1-US5** and **FP1-FP3**); and
3. Copies of cited documents (**FP1-FP3**).

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

M-Y/jcb
Enclosures

15719192_1.docx

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: CHEN *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: 16/729,838

Filing Date: December 30, 2019

Confirmation No.: 5773

Art Unit: 2827

Examiner: LE, THONG QUOC

Atty. Docket: 4123.0850001

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Form PTO/SB/08a are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Form based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.
- ☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- ☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ c. The required fee is provided through online credit card payment authorization in the amount of \$260.00 in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of \$260.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

☒ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **FP3** (CN 109390012 A) appears to describe a “method and apparatus for removing electrons from oxide layer surface of floating gate memory,” as noted in the attached English-language translation of the abstract.

Document **US1** (2012/0275223 A1) is submitted herewith as the English-language counterpart of document **FP1** (CN 102760490 A).

Document **US5** (10,121,554 B2) is submitted herewith as the English-language counterpart of document **FP2** (CN 108140415 A).

☒ 8. Copies of documents **FP1-FP3** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patents and patent application publications cited as documents **US1-US5** on the attached IDS Form are submitted.

☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent

Application No(s). _____ in accordance with MPEP 2001.06(b), and
indicate in the next communication from the office that the art cited in the earlier
prosecution history has been reviewed in connection with the present application.

☐ 11. Applicants submit herewith Office Actions from the co-pending U.S. Patent Application

No. _____, filed _____, as documents _____ to _____.

The identification of these Office Actions is not to be construed as a waiver of secrecy as to
those applications now or upon issuance of the present application as a patent. The Examiner
is respectfully requested to consider the cited applications and the art cited therein during
examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Form, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang, Ph.D.
Agent for Applicant
Registration No. 78,149

Date: October 16, 2020

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/729,838	12/30/2019	Zilong CHEN	4123.0850001	5773
26111	7590	10/20/2020		
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER LE, THONG QUOC	
			ART UNIT	PAPER NUMBER
			2827	
			NOTIFICATION DATE	DELIVERY MODE
			10/20/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

1. Pre-amendment filed on 01/31/2020 has been entered.
2. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.

Claim 1-3, 7, 9 are rejected under 35 U.S.C. 102(a)(1) based upon a public use or sale or other public availability of the invention by Lee (Pub. U.S. 2019/0333590).

Regarding claim 1, Lee discloses a method for conducting a read-verification operation on a target memory cell ([0061-0062], target cell in fig.6) in a three-dimensional (3D) memory device (Figure 6), comprising:

removing fast charges of the target memory cell at a read-prepare step ([0064-0071], comprising:

applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string ([0066], Figure 8, (Unsel) DSL,SSL);

applying a first off voltage (V_{off}) on a selected word line (Sel WL) associated with the target memory cell (Figure 8, GWL, LWL,[0067]); and

applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL) (Figure 8, 81,[0067-0068]; and measuring a threshold voltage of the target memory cell at a sensing step ([0038],[0046],[0049-0050]).

Regarding claim 2, Lee discloses further comprising: applying a top select gate voltage (V_{tsg}) on a selected top select gate (Sel_TSG) of a selected memory string containing the target memory cell ; and applying a lower select gate voltage (V_{tsg}) on a lower select gate (LSG) of the selected memory string containing the target memory cell (Figure 8, (Sel) DSL, SSL).

Regarding claim 3, Lee discloses wherein applying the top select gate voltage (V_{tsg}) comprises electrically connecting the selected memory string to a bit line (Figure 7, BL); and applying the lower select gate voltage (V_{tsg}) comprises electrically connecting the selected memory string to an array common source (Figure 7, [0061-0062], example a selected cell).

Regarding claim 7, Lee discloses wherein measuring the threshold voltage comprises applying a read voltage (V_{read}) on the selected word line (SelWL) ([0040]).

Regarding claim 9, Lee discloses wherein applying the read voltage (V_{read})

comprises applying a second off voltage (V_{pass}) on the unselected word line (Unsel_WL) ([0040]).

Allowable Subject Matter

3. Claims 4-6, 8 -10-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4-6, 8, 10-20 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. The prior art does not teach the claimed invention having wherein applying the top select gate voltage (V_{tsg}) comprises applying a voltage between 4V to 7V, and wherein applying the lower select gate voltage (V_{tsg}) comprises applying a voltage between 4V to 7V, and wherein applying the pass voltage (V_{pass}) comprises applying the pass voltage with a delay period after the selected top select gate (Sel_TSG) and the lower select gate (LSG) are at the top select gate voltage (V_{tsg}) and the lower select gate voltage (V_{tsg}), respectively. and wherein applying the read voltage (V_{read}) comprises applying a voltage between 0 to 2V.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THONG QUOC LE whose telephone number is (571)272-1783. The examiner can normally be reached on 7:30AM-5:30PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

Art Unit: 2827

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/THONG Q LE/

Primary Examiner, Art Unit 2827

<i>Notice of References Cited</i>	Application/Control No. 16/729,838		Applicant(s)/Patent Under Reexamination CHEN et al.	
	Examiner THONG Q LE		Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS						
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20190333590-A1	10-2019	LEE; Hee Youl	G11C16/26	1/1
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS						
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS		
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/729,838	Applicant(s)/Patent Under Reexamination CHEN et al.
	Examiner THONG Q LE	Art Unit 2827

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483; G11C16/24; G11C16/26; G11C16/30; G11C16/12; G11C16/3454; G11C11/5628; G11C16/10; G11C16/3459; G11C11/5642; G11C11/5671; G11C16/08; G11C16/32; G11C2029/0411; G11C2211/5621; G11C2211/5646; G11C29/42; G11C29/52; G11C5/143; G06F3/0619	10/15/2020	TL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
1	1		

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
see search history printout	10/15/2020	TL
Google searched	10/15/2020	TL
Google Images searched	10/15/2020	TL
Google Patents searched	10/15/2020	TL

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	170,590	"3" adj dimension\$3 or three-dimension\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 09:07
L2	4,344	L1 and memory and method and target and verify\$3 and cell and select\$3 and \$3select\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 09:07
L3	236	L2 and pass adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 09:07
L4	57	L3 and threshold adj voltage with target with cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 09:07
L5	6	L4 and threshold adj voltage and target adj memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 09:07
L6	6	L4 and threshold adj voltage and target adj memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 09:14

L7	4,582,327	((G11C16/0483 OR G11C16/24 OR G11C16/26 OR G11C16/30 OR G11C16/12 OR G11C16/3454 OR G11C11/5628 OR G11C16/10 OR G11C16/3459 OR G11C11/5642 OR G11C11/5671 OR G11C16/08 OR G11C16/32 OR G11C2029/0411 OR G11C2211/5621 OR G11C2211/5646 OR G11C29/42 OR G11C29/52 OR G11C5/143 OR G06F3/0619 OR G06F3/065 OR G06F3/0653 OR G06F3/0659 OR G06F3/0679).CPC. OR (1/1).CCLS. OR (G11C16/34 OR G11C16/24 OR G11C16/26 OR G11C16/12 OR G11C16/30 OR G11C16/04 OR G11C16/10 OR G11C16/08 OR G11C29/42 OR G06F3/06).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 10:18
L8	170,590	"3" adj dimension\$3 or three-dimension\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 10:23
L9	821	prepar\$3 adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 10:23
L10	2	L8 and L9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 10:23
L11	236	L2 and pass adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 10:23
L12	4,344	L8 and memory and method and target and verify\$3 and cell and select\$3 and \$3select\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2020/10/15 10:23

			DERWENT; IBM_TDB			
L13	0	L12 and L9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/15 10:23
S1	170,494	"3" adj dimension\$3 or three- dimention\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:15
S2	1,045,062	1c amd memory and method and target and verify\$3 and cell and select\$3 and \$3select\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:18
S3	4,343	S1 and memory and method and target and verify\$3 and cell and select\$3 and \$3select\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:20
S4	235	S3 and pass adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:22
S5	57	S4 and threshold adj voltage with target with cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:23
S6	0	S5 and read-prepar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2020/10/13 10:25

			DERWENT; IBM_TDB			
S8	821	prepar\$3 adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:27
S9	0	S5 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:28
S10	0	S4 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:28
S11	0	S3 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:28
S12	65	S2 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:28
S13	0	S3 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 10:29
S14	2	S1 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2020/10/13 10:29

			DERWENT; IBM_TDB			
S15	4	read-prepar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:38
S16	170,494	"3" adj dimension\$3 or three- dimention\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:38
S17	4,343	S16 and memory and method and target and verify\$3 and cell and select\$3 and \$3select\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:38
S18	235	S17 and pass adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:38
S19	57	S18 and threshold adj voltage with target with cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:38
S20	6	S19 and threshold adj voltage and target adj memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:42
S21	0	S19 and S15 and S16 and 6reshold adj voltage and target adj memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2020/10/13 11:59

			DERWENT; IBM_TDB			
S22	0	S19 and S15 and S16 and S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:59
S23	0	S15 and S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:59
S24	4,343	S16 and memory and method and target and verify\$3 and cell and select\$3 and \$3select\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 11:59
S25	235	S24 and pass adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 12:00
S26	57	S25 and threshold adj voltage with target with cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 12:00
S27	5	S26 and time with sens\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/13 12:01
S28	170,494	"3" adj dimension\$3 or three-dimension\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2020/10/14 10:34

			DERWENT; IBM_TDB			
S29	4,343	S28 and memory and method and target and verify\$3 and cell and select\$3 and \$3select\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/14 10:34
S30	235	S29 and pass adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/14 10:34
S31	57	S30 and threshold adj voltage with target with cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/14 10:34
S32	5	S31 and time with sens\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/14 10:34
S33	4	read-prepar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/14 10:37
S34	4,343	S28 and memory and method and target and verify\$3 and cell and select\$3 and \$3select\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/14 10:38
S35	235	S34 and pass adj voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2020/10/14 10:38

			DERWENT; IBM_TDB			
S36	57	S35 and threshold adj voltage with target with cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/14 10:38
S37	6	S36 and threshold adj voltage and target adj memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/10/14 10:38

10/15/2020 10:27:02 AM

C:\Users\tle3\Documents\EAST\Workspaces\searchhistory\searchedhistory\16729838.wsp

Web Search History

date, time	web site	search string
10/13/2020 11:18:09 AM	Google	A method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Vprepare) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (Sel WL) associated with the target memory cell; and applying a pass voltage (Vpass) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.
10/13/2020 11:30:26 AM	Google Images	A method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Prepare) on an unselected top select gate (UnselecTED) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (Sel WL) associated with the target memory cell; and applying a pass voltage (Vpass) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.
10/13/2020 11:30:26 AM	Google	A method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Prepare) on an unselected top select gate (UnselecTED) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (Sel WL) associated with the target memory cell; and applying a pass voltage (Vpass) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.
10/13/2020 11:32:54 AM	Google Patents	Keyword Group 1 [remov\$3 fast charge]

date, time	web site	search string
10/13/2020 11:33:15 AM	Google Patents	Keyword Group 1 [remov\$3 fast charge] Keyword Group 2 [A method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Vprepare) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (Sel WL) associated with the target memory cell; and applying a pass voltage (Vpass) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.]
10/13/2020 11:33:16 AM	Google Patents	Keyword Group 1 [(remov\$3 fast charge) (A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Vprepare) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (Sel WL) associated with the target memory cell; and applying a pass voltage (Vpass) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.))
10/13/2020 11:33:44 AM	Google Patents	Keyword Group 1 [(A method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Vprepare) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (Sel WL) associated with the target memory cell; and applying a pass voltage (Vpass) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.)]

date, time	web site	search string
10/13/2020 11:33:44 AM	Google Patents	Keyword Group 1 [((A method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Vprepare) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (Sel WL) associated with the target memory cell; and applying a pass voltage (Vpass) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.))]
10/13/2020 11:34:14 AM	Google Patents	Keyword Group 1 [((A method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising:]
10/13/2020 11:34:14 AM	Google Patents	Keyword Group 1 [(((A method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising:))]
10/13/2020 11:34:51 AM	Google Patents	Keyword Group 1 [applying a top select gate voltage (Vtsg) on a selected top select gate (SelTSG) of a selected memory string containing the target memory cell; and applying a lower select gate voltage (Visg) on a lower select gate (LSG) of the selected memory string containing the target memory cell]
10/13/2020 11:34:52 AM	Google Patents	Keyword Group 1 [(applying a top select gate voltage (Vtsg) on a selected top select gate (SelTSG) of a selected memory string containing the target memory cell; and applying a lower select gate voltage (Visg) on a lower select gate (LSG) of the selected memory string containing the target memory cell)]
10/13/2020 11:36:57 AM	Google Patents	Keyword Group 1 [method for conducting a read-verification operation on a target memory cell in a three- dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step]

Bibliographic Data

Application No: 16/729,838

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged: /THONG Q LE/

Examiner's Signature

Initials

Title:

METHOD FOR READING THREE-DIMENSIONAL FLASH
MEMORY

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/30/2019	365	2827	4123.0850001
RULE			

APPLICANTS

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

INVENTORS

Zilong CHEN, Wuhan, CHINA

Xiang FU, Wuhan, CHINA

CONTINUING DATA

This application is a CON of PCT/CN2019/112728 10/23/2019

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

01/22/2020

STATE OR COUNTRY

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WASHINGTON, DC 20005

UNITED STATES

FILING FEE RECEIVED

\$1,880

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/729,838	Filing Date 12/30/2019	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		x \$100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		x \$460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED - PART II

	(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	01/19/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x \$480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE	
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/VICTORIA JOHNSON/	
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".							
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: CHEN *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: 16/729,838

Filing Date: December 30, 2019

Confirmation No.: 5773

Art Unit: 2827

Examiner: LE, THONG QUOC

Atty. Docket: 4123.0850001

Title: **METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY**

Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated **October 20, 2020** (“Office Action”), Applicant submits the following Amendment and Remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Electronic Acknowledgement Receipt

EFS ID:	41683042
Application Number:	16729838
International Application Number:	
Confirmation Number:	5773
Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Donald J. Featherstone/Julia Vang
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0850001
Receipt Date:	19-JAN-2021
Filing Date:	30-DEC-2019
Time Stamp:	16:36:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2021-01-19-Cover-Letter-4123-0850001.pdf	324540	no	1
			d0287ac064f4126adaab2d362cf7ba3dc8a fc13		

Warnings:

Information:					
2		2021-01-19- Reply-111-4123-0850001.pdf	316546	yes	8
			b58ca07e91f4d64b4034fd703fff40f95f41c929		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Arguments/Remarks Made in an Amendment		5	8	
	Claims		2	4	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
Warnings:					
Information:					
Total Files Size (in bytes):			641086		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

January 19, 2021

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 5773
Art Unit 2827
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 16/729,838; Filing Date: December 30, 2019
For: **METHOD FOR READING THREE-DIMENSIONAL FLASH
MEMORY**
Inventors: CHEN *et al.*
Our Ref: 4123.0850001

Commissioner:

Transmitted herewith for appropriate action is a document entitled ***Reply Under 37 C.F.R. § 1.111***, which is submitted electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/jcv
Enclosure(s)

Remarks

Reconsideration of this Application is respectfully requested.

Claims 1-20 are pending in the application, with claim 1 being the sole independent claim.

No amendment is made herein.

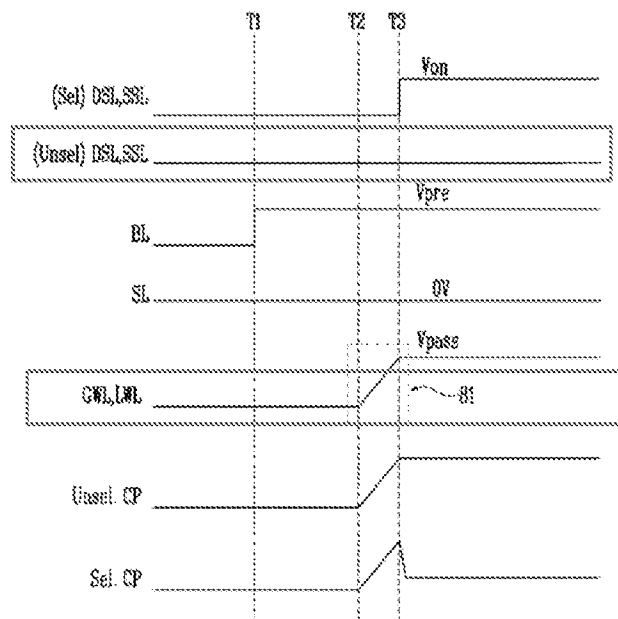
Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 1-3, 7 and 9 are rejected under 35 U.S.C. § 102(a)(1) based upon a public use or sale or other public availability of the invention by U.S. Publication No. 2019/0333590 to Lee (“Lee”). Applicant respectfully traverses these rejections.

Independent claim 1 recites, *inter alia*, “*applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string.*” The Office Action relies on Lee’s Figure 8 to allegedly disclose the above distinguishing features of claim 1. However, at time T1, Lee makes “all of the drain and [source] select lines DSL and SSL coupled to the memory blocks **float**.” (Lee, ¶[0067], FIG. 8.¹) Lee’s “drain and source select lines (Unsel) DSL and SSL included in the unselected memory blocks are **left floating**, so that the drain and source select transistors included in the unselected memory blocks remain turned off.” (Lee, ¶[0071], FIG. 8.) Lee only applies “a positive precharge voltage V_{pre} ” to the **bit lines BL**. (Lee, ¶[0066], FIG. 8.) Thus, Lee does not disclose or suggest “*applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string.*”

¹ Emphasis added unless noted otherwise.



Lee, FIG. 8 (annotated).

In addition, claim 1 recites, *inter alia*, “applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell; and applying a pass voltage (V_{pass}) on an unselected word line ($Unsel_WL$).” However, Lee applies the pass voltage V_{pass} of a positive voltage “to the global word lines GWL ,” and “[b]ecause all of the pass switch circuits are left enabled, when the pass voltage V_{pass} is applied to the global word lines GWL , the pass voltage V_{pass} is transmitted to **all of the local word lines LWL** .” (Lee, ¶[0067], FIG. 8.) Therefore, Lee does not apply different voltages to the selected and unselected word lines during the channel boosting operation between time T1 and T3.

Accordingly, Lee does not disclose or teach the distinguishing features of claim 1. Appellant respectfully request the rejection to be reversed and independent claim 1 be passed onto allowance.

Dependent claims 2-3, 7 and 9 should also be found allowable because they recite all of the features of claim 1, from which they respectively depend, as well as for their additional distinguishing features.

Allowable Subject Matter

Claims 4-6, 8 and 10-20 are objected to as being dependent on a rejected base claim, but would be allowed if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant thanks the Examiner for indicating the allowable subject matter, but declines to make these claims independent at this time based on the arguments above.

Applicant agrees that the claimed subject matter is patentable. However, Applicant takes no position regarding the reasons for allowance presented in the Office Action other than the positions Applicant may have previously taken during prosecution. Therefore, the Examiner's Reasons for Allowance should not be attributed to Applicant as an indication of the basis for Applicant's belief that the claims are patentable. Furthermore, Applicant respectfully asserts that there may also be additional reasons for patentability of the claimed subject matter not explicitly stated in this record, and Applicant does not waive the rights to such arguments by not further addressing such reasons herein.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such,

the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 1/19/21

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
15828914.4

Status of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:
 - removing fast charges of the target memory cell at a read-prepare step, comprising:
 - applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string;
 - applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell; and
 - applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL); and
 - measuring a threshold voltage of the target memory cell at a sensing step.
2. (Original) The method of claim 1, further comprising:
 - applying a top select gate voltage (V_{tsg}) on a selected top select gate (Sel_TSG) of a selected memory string containing the target memory cell; and
 - applying a lower select gate voltage (V_{lsg}) on a lower select gate (LSG) of the selected memory string containing the target memory cell.
3. (Original) The method of claim 2, wherein applying the top select gate voltage (V_{tsg}) comprises electrically connecting the selected memory string to a bit line; and applying the lower select gate voltage (V_{lsg}) comprises electrically connecting the selected memory string to an array common source.
4. (Original) The method of claim 2, wherein applying the top select gate voltage (V_{tsg}) comprises applying a voltage between 4V to 7V.
5. (Original) The method of claim 2, wherein applying the lower select gate voltage (V_{lsg}) comprises applying a voltage between 4V to 7V.

6. (Original) The method of claim 2, wherein applying the pass voltage (V_{pass}) comprises applying the pass voltage with a delay period after the selected top select gate (Sel_TSG) and the lower select gate (LSG) are at the top select gate voltage (V_{tsg}) and the lower select gate voltage (V_{lsg}), respectively.
7. (Original) The method of claim 1, wherein measuring the threshold voltage comprises applying a read voltage (V_{read}) on the selected word line (Sel_WL).
8. (Original) The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying a voltage between 0 to 2V.
9. (Original) The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying a second off voltage on the unselected word line (Unsel_WL).
10. (Original) The method of claim 9, wherein applying the second off voltage on the unselected word line (Unsel_WL) comprises applying a 0V.
11. (Original) The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is higher than a threshold voltage of an unselected memory cell.
12. (Original) The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) equals to a threshold voltage of an unselected memory cell.
13. (Original) The method of claim 7, wherein applying the read voltage (V_{read}) comprises applying the read voltage (V_{read}) when a voltage of the unselected top select gate (Unsel_TSG) is lower than a threshold voltage of an unselected memory cell.
14. (Original) The method of claim 1, wherein applying the prepare voltage (V_{prepare}) comprises applying a voltage between 4V to 7V.

15. (Original) The method of claim 1, wherein applying the first off voltage (V_{off}) comprises applying a 0V.
16. (Original) The method of claim 1, wherein applying the pass voltage (V_{pass}) comprises applying a voltage between 5V to 9V.
17. (Original) The method of claim 1, wherein removing the fast charges comprises removing the fast charges from a storage layer of the target memory cell of a selected memory string, wherein the selected memory string comprises:
 - a channel hole penetrating vertically through a film stack of alternating conductive and dielectric layers;
 - a core filling film in a center of the channel hole;
 - a memory film covering a sidewall of the channel hole, wherein the memory film comprises a barrier layer, the storage layer and a tunneling layer; and
 - a channel layer sandwiched between the memory film and the core filling film.
18. (Original) The method of claim 17, wherein removing the fast charges comprises removing electrical charges from shallow traps in the storage layer of the target memory cell.
19. (Original) The method of claim 17, wherein removing the fast charges comprises removing the fast charges from the target memory cell to a neighboring unselected memory cell.
20. (Original) The method of claim 1, wherein conducting the read-verification operation comprises conducting the read-prepare step and conducting a failed bit count in parallel.



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NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 02/24/2021
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

LE, THONG QUOC

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 02/24/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/729,838	12/30/2019	Zilong CHEN	4123.0850001	5773

TITLE OF INVENTION: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	05/24/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
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Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

26111 7590 02/24/2021
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/729,838	12/30/2019	Zilong CHEN	4123.0850001	5773

TITLE OF INVENTION: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	05/24/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, THONG QUOC	2827	365-185020

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/729,838	12/30/2019	Zilong CHEN	4123.0850001	5773
26111	7590	02/24/2021	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			LE, THONG QUOC	
			ART UNIT	PAPER NUMBER
			2827	
DATE MAILED: 02/24/2021				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/729,838	Applicant(s) CHEN et al.	
	Examiner THONG Q LE	Art Unit 2827	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 01/29/2021.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>10/16/2020</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	---

/THONG Q LE/
Primary Examiner, Art Unit 2827

Search Notes 	Application/Control No. 16/729,838	Applicant(s)/Patent Under Reexamination CHEN et al.
	Examiner THONG Q LE	Art Unit 2827

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483; G11C16/24; G11C16/26; G11C16/30; G11C16/12; G11C16/3454; G11C11/5628; G11C16/10; G11C16/3459; G11C11/5642; G11C11/5671; G11C16/08; G11C16/32; G11C2029/0411; G11C2211/5621; G11C2211/5646; G11C29/42; G11C29/52; G11C5/143; G06F3/0619	10/15/2020	TL
G11C11/5642; G11C16/08; G11C16/32; G11C2029/0411; G11C2211/5646; G11C29/42; G11C29/52; G11C5/143	02/18/2021	TL
G06F3/0619; G06F3/065; G06F3/0653; G06F3/0659; G06F3/0679	02/18/2021	TL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
1	1	02/18/2021	TL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
see search history printout	02/18/2021	TL
Google searched	02/18/2021	TL
Google Images searched	02/18/2021	TL
Google Patents searched	02/18/2021	TL
Inventor searched	02/18/2021	TL

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<i>Search Notes</i> 	Application/Control No. 16/729,838	Applicant(s)/Patent Under Reexamination CHEN et al.
	Examiner THONG Q LE	Art Unit 2827

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	Interference searched	02/18/2021	TL

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Issue Classification 	Application/Control No. 16/729,838	Applicant(s)/Patent Under Reexamination CHEN et al.
	Examiner THONG Q LE	Art Unit 2827

CPC						
Symbol					Type	Version
G11C	/	16	/	3427	F	2013-01-01
G11C	/	16	/	0483	I	2013-01-01
H01L	/	27	/	11582	I	2013-01-01
G11C	/	16	/	08	I	2013-01-01
G11C	/	16	/	26	I	2013-01-01

CPC Combination Sets					
Symbol				Type	Set

NONE	Total Claims Allowed:	
(Assistant Examiner)	(Date)	20
/THONG Q LE/	18 February 2021	O.G. Print Claim(s)
Primary Examiner, Art Unit 2827	(Date)	O.G. Print Figure
(Primary Examiner)		1
		5

Issue Classification 	Application/Control No. 16/729,838	Applicant(s)/Patent Under Reexamination CHEN et al.
	Examiner THONG Q LE	Art Unit 2827

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G11C	/	16	/ 04
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
365	185.02

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
1	1					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/THONG Q LE/ Primary Examiner, Art Unit 2827 (Primary Examiner)	18 February 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 5

Issue Classification 	Application/Control No. 16/729,838	Applicant(s)/Patent Under Reexamination CHEN et al.
	Examiner THONG Q LE	Art Unit 2827

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19										
	2		11		20										
	3		12												
	4		13												
	5		14												
	6		15												
	7		16												
	8		17												
	9		18												

NONE	Total Claims Allowed:	
(Assistant Examiner)	(Date)	20
/THONG Q LE/ Primary Examiner, Art Unit 2827	18 February 2021	O.G. Print Claim(s)
(Primary Examiner)	(Date)	1
		O.G. Print Figure
		5

PTO/SB/08a (07-09)

Approved for use through 11/30/2020. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet

1

of

1

Application Number

16/729,838

Filing Date

December 30, 2019

First Named Inventor

Zilong CHEN

Art Unit

2827

Examiner Name

LE, THONG QUOC

Attorney Docket Number

4123.0850001

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
	FP1	CN 102760490 A	10-31-2012	SK HYNIX INC		
	FP2	CN 108140415 A	06-08-2018	SUNRISE MEMORY CORP		
	FP3	CN 109390012 A	02-26-2019	GIGADEVICE SEMICONDUCTOR		✓

Examiner
Signature

/THONG Q LE/

Date
Cons

02/18/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Web Search History

date, time	web site	search string
2/17/2021 3:50:58 PM	Google	an array of memory cells each comprising a capacitive storage element; a controller coupled with the array of memory cells and configured to demodulate or decode data signals or command signals, or both, for the array of memory cells; a first circuit coupled with the controller and comprising a first inverting input configured to amplify a reference signal and a first input configured to amplify a first data signal; a second circuit coupled with the controller and comprising a second inverting input configured to amplify the reference signal and a second input configured to amplify a second data signal; and a capacitor or inductor coupled with the first inverting input and the second input and configured to block a frequency subset of the second data signal that is lower than a threshold frequency.
2/17/2021 3:53:26 PM	Google Patents	Keyword Group 1 [an array of memory cells each comprising a capacitive storage element; a controller coupled with the array of memory cells and configured to demodulate or decode data signals or command signals, or both, for the array of memory cells; a first circuit coupled with the controller and comprising a first inverting input configured to amplify a reference signal and a first input configured to amplify a first data signal; a second circuit coupled with the controller and comprising a second inverting input configured to amplify the reference signal and a second input configured to amplify a second data signal; and a capacitor or inductor coupled with the first inverting input and the second input and configured to block a frequency subset of the second data signal that is lower than a threshold frequency.]
2/18/2021 1:17:00 PM	Google	A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (V_{prepare}) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (V_{off}) on a selected word line (SelWL) associated with the target memory cell; and applying a pass voltage (V_{pas}) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.
2/18/2021 1:18:09 PM	Google Patents	Keyword Group 1 [memory]

date, time	web site	search string
2/18/2021 1:18:16 PM	Google Patents	Keyword Group 1 [A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Vprepare) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (SelWL) associated with the target memory cell; and applying a pass voltage (Vpas) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.]
2/18/2021 1:19:24 PM	Google Patents	Keyword Group 1 [(A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Vprepare) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (SelWL) associated with the target memory cell; and applying a pass voltage (Vpas) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step.)]
2/18/2021 1:20:06 PM	Google Patents	Keyword Group 1 [conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising: removing fast charges of the target memory cell at a read-prepare step, comprising: applying a prepare voltage (Vprepare) on an unselected top select gate (UnselTSG) of an unselected memory string; applying a first off voltage (Voff) on a selected word line (SelWL) associated with the target memory cell; and applying a pass voltage (Vpas) on an unselected word line (Unsel WL); and measuring a threshold voltage of the target memory cell at a sensing step]



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/729,838	12/30/2019	Zilong CHEN	4123.0850001

CONFIRMATION NO. 5773

PUBLICATION NOTICE



OC000000125251889

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Title:METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Publication No.US-2021-0125674-A1

Publication Date:04/29/2021

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

DONALD J. FEATHERSTONE
DIRECTOR
202-772-8629
DONF@STERNEKESSLER.COM



May 19, 2021

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 5773
Attn: Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 16/729,838; Filed: December 30, 2019
For: **METHOD FOR READING THREE-DIMENSIONAL FLASH
MEMORY**
First Named Inventor: Zilong CHEN
Our Ref: 4123.0850001

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated **February 24, 2021**, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark office:

1. Issue Fee Transmittal (Form PTOL-85); and
2. Online Credit Card Payment Authorization for \$1,200.00 to cover:

\$1,200.00 – Issue Fee.

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/jcv
Enclosure(s)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

26111 7590 02/24/2021
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/729,838	12/30/2019	Zilong CHEN	4123.0850001	5773

TITLE OF INVENTION: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	05/24/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, THONG QUOC	2827	365-185020

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Sterne, Kessler, Goldstein
& Fox P.L.L.C.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Yangtze Memory Technologies Co., Ltd.

Wuhan, Hubei, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

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5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29☐ Applicant asserting small entity status. See 37 CFR 1.27☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Donald J. Featherstone/ Date 5/19/21
Typed or printed name Donald J. Featherstone Registration No. 33,876

Electronic Patent Application Fee Transmittal				
Application Number:		16729838		
Filing Date:		30-Dec-2019		
Title of Invention:		METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY		
First Named Inventor/Applicant Name:		Zilong CHEN		
Filer:		Donald J. Featherstone/Julia Vang		
Attorney Docket Number:		4123.0850001		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	42766122
Application Number:	16729838
International Application Number:	
Confirmation Number:	5773
Title of Invention:	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
First Named Inventor/Applicant Name:	Zilong CHEN
Customer Number:	26111
Filer:	Donald J. Featherstone/Julia Vang
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0850001
Receipt Date:	19-MAY-2021
Filing Date:	30-DEC-2019
Time Stamp:	17:07:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E20215IH07464763
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2021-05-19-Cover-Letter-4123-0850001.pdf	222310	no	1
			9c37721c19dc78b247bf59bbe8227132b6d62b9f		
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	2021-05-19-Issue-Fee-4123-0850001.PDF	188720	no	1
			86ae2fd80a31601910ed2932aa7c268ec5b97456		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30389	no	2
			d7e9ec7141825cddd61033ca04c6577901fbd131		
Warnings:					
Information:					
Total Files Size (in bytes):			441419		
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/729,838	06/22/2021	11043279	4123.0850001	5773

26111 7590 06/02/2021

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Zilong CHEN, Wuhan, CHINA;
Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA
Xiang FU, Wuhan, CHINA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

**TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE
REGISTERED PRACTITIONERS**

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16729838
Filing Date	December 30, 2019
First Named Inventor	Zilong CHEN
Title	METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY
Art Unit	2827
Examiner Name	THONG LE
Attorney Docket Number	2018-00538-YMTC-PCT-US

SIGNATURE of Applicant or Patent Practitioner

Signature	/Mark C. Zimmerman /	Date (Optional)	July 3, 2024
Name	Mark C. Zimmerman	Registration Number	44006
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐

*Total of _____ forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0035. Public burden for this form is estimated to average 3 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.** If filing this completed form by mail, send to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

OR

34431

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Tuenlai Daniel Chan

Title

Deputy General Counsel, Head of Intellectual Property Department

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0035. Public burden for this form is estimated to average 3 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.** If filing this completed form by mail, send to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a Federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 9) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Additional Uses

Additional USPTO uses of the information in this record may include disclosure to: 1) the International Bureau of the World Intellectual Property Organization, if the record is related to an international application filed under the Patent Cooperation Treaty; 2) the public i) after publication of the application pursuant to 35 U.S.C. 122(b), ii) after issuance of a patent pursuant to 35 U.S.C. 151, iii) if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections, or an issued patent, or iv) without publication of the application or patent under the specific circumstances provided for by 37 CFR 1.14(a)(1)(v)-(vii); and/or 3) the National Archives and Records Administration, for inspection of records.



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
16/729,838

RECEIPT DATE / TIME
07/03/2024 03:34:24 PM Z ET

ATTORNEY DOCKET #
4123.0850001

Title of Invention

METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 11043279

CONFIRMATION # 5773

FILED BY Kaoru Julian

PATENT CENTER # 66233895

FILING DATE 12/30/2019

CUSTOMER # 26111

FIRST NAMED
INVENTOR Zilong CHEN

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Mark Zimmerman

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2018-00538-YMTC-PCT-US_POA.pdf	3	Power of Attorney	402 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2018-00538-YMTC-PCT-US_POA.pdf	FFD363E4DFE927AE76C7E49E790E5AFAB0B4267AFB1D80 35DE1937E310899265A62B756676D92B4971A9B8A562643B10 A531E4902A76834801058551695566

by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/729,838	12/30/2019	Zilong CHEN	2018-00538-YMTC-PCT-US

CONFIRMATION NO. 5773

34431
HANLEY, FLIGHT & ZIMMERMAN, LLC
10 S. WACKER DRIVE
SUITE 3500
CHICAGO, IL 60606

POA ACCEPTANCE LETTER



OC000000075356312

Date Mailed: 07/17/2024

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/03/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/tnguyen/



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/729,838	12/30/2019	Zilong CHEN	4123.0850001

CONFIRMATION NO. 5773

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1101 K Street, NW
10th Floor
WASHINGTON, DC 20005

POWER OF ATTORNEY NOTICE



OC000000075356202

Date Mailed: 07/17/2024

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/03/2024.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/tnguyen/