

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00793
Patent 11,600,342 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–6 and 8–20 of U.S. Patent No. 11,600,342 B2 (“the ’342 patent,” Ex. 1001). Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 11 (“Prelim. Resp.”).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2023). For the reasons discussed below, we deny the Petition and do not institute an *inter partes* review.

A. *Real Parties in Interest*

Petitioner identifies “Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 4. Patent Owner identifies itself as the real party in interest. Paper 3 (Mandatory Notice), 2.

B. *Related Matters*

The parties indicate that the ’342 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 4; Paper 3, 2.

C. *The ’342 Patent*

The ’342 patent, titled “Method for Reading Three-Dimensional Flash Memory,” relates to “a method for conducting read-verification operation of a memory cell in a three-dimensional (3D) memory device.” Ex. 1001, code [54], 1:49–51. “The method includes removing fast charges of the target memory cell at a read-prepare step” by applying “a prepare voltage

($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string,” “a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell,” and “a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).” *Id.* at 1:55–61.

Figure 6 is reproduced below.

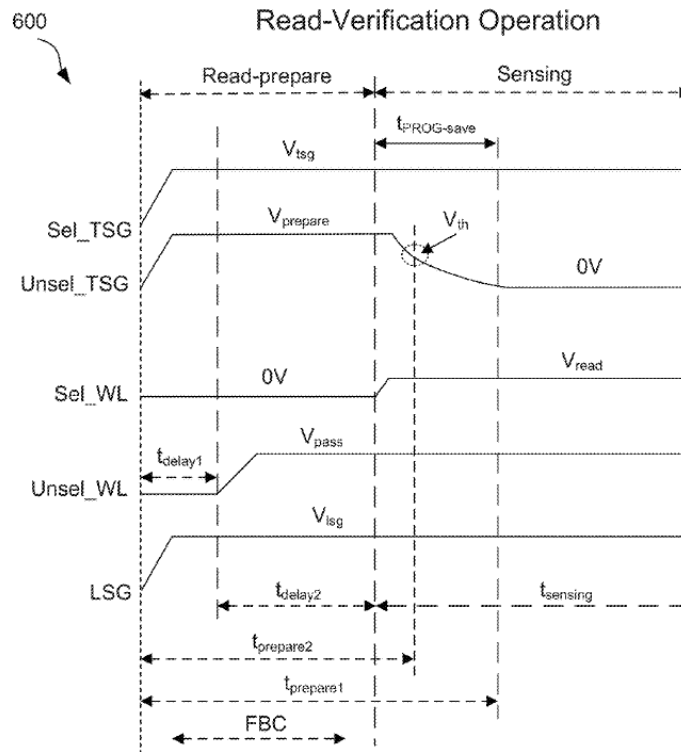


Fig. 6

Ex. 1001, Fig. 6. Figure 6 illustrates a timing diagram of a read-verification operation with accelerated fast charge loss. *Id.* at 3:28–30. Read-verification operation 600 includes the read-prepare step and the sensing step. *Id.* at 11:14–15. During the read-prepare step, top and lower select voltages V_{tsg} and V_{lsg} are applied to Sel_TSG and LSG, respectively, to switch on the top and lower select transistors, and prepare voltage $V_{prepare}$ is applied to Unsel_TSG. *Id.* at 11:15–24. The selected memory cell can be switched off by applying a second off voltage (e.g., 0V) on selected word

line Sel_WL, and the unselected memory cells Unsel_WL can be switched on with pass voltage V_{pass} after a delay period t_{delay1} . *Id.* at 11:29–33.

The read-prepare step also includes a delay period t_{delay2} , which is the time between ramping up pass voltage V_{pass} of Unsel_WL and the read voltage V_{read} of the Sel_WL. Ex. 1001, 12:10–13. During t_{delay2} , the voltage of Sel_WL is kept at 0V and the voltage of Unsel_WL increases from 0V to V_{pass} . *Id.* at 12:13–15. Because V_{pass} is applied on Unsel_WL after the top and lower select transistors are switched on with applied voltages V_{tsg} , $V_{prepare}$, and V_{lsg} on Sel_TSG, Unsel_TSG, and LSG, respectively, the selected memory cell is switched off while unselected memory cells are switched on. *Id.* at 12:15–23. The '342 patent explains that, between the selected memory cell with 0V gate bias and the neighboring unselected memory cells with a gate bias of the pass voltage V_{pass} , an electric field parallel to the channel is established. *Id.* at 12:24–27. The electric field between the neighboring selected and unselected word line can also extend into the charge storage layer, the tunneling layer, and the channel layer, and can generate an electric force on the fast charges captured in the storage layer. *Id.* at 12:27–32.

The '342 patent further explains that the electric force can de-trap the fast charges from the shallow traps and pull them towards the neighboring unselected memory cells. Ex. 1001, 12:32–34. The fast charges are then recombined with charges of opposite sign or removed through the conductive path established in the channel of the unselected memory cells, and the fast charges in the storage layer of the selected memory cell are removed through the electric field from neighboring unselected memory cells. *Id.* at 12:34–40.

D. Illustrative Claim

Petitioner challenges claims 1–6 and 8–20 of the '342 patent. Claims 1 and 16 are independent, illustrative of the claimed subject matter, and reproduced below.

1. [1.PRE] A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:

- [1.A] applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a second time period;
- [1.B] applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and
- [1.C] applying, on an unselected word line, a pass voltage during the first time period and the second time period;
- [1.D] wherein the read-verification operation removes fast charges of the target memory cell during the first time period.

Ex. 1001, 14:53–68 (bracketed material added).

16. [PRE] A three-dimensional memory device, comprising:

- [16.A] a memory array, comprising a plurality of memory strings extending vertically through a film stack of alternating conductive and dielectric layers, wherein;
 - [16.A.i] each memory string comprising a plurality of memory cells; and
 - [16.A.ii] each memory string is addressable through a word line and a bit line; and
- [16.B] a circuit of the memory array configured to conduct, on a target memory cell, a read-verification operation for removing fast charges during a first time period, wherein the circuit is configured to:

[16.B.i] apply, on an unselected top select gate of an unselected memory string, a prepare voltage during the first time period and an off voltage during the second time period;

[16.B.ii] apply, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and

[16.B.iii] apply, on an unselected word line, a pass voltage during the first time period and the second time period.

Id. at 16:4–27 (bracketed material added).

E. Asserted Grounds

Petitioner asserts that claims 1–6 and 8–20 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6, 8–14, 16–20	103 ¹	Seo, ² Choi ³
15	103	Seo, Choi, Izumi ⁴
1–3, 5, 6, 8–14, 16, 17, 19, 20	103	Nam, ⁵ Choi
15	103	Nam, Choi, Izumi

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’342 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

² Seo, US 2021/0027848 A1, published Jan. 28, 2021 (Ex. 1005).

³ Bongsik Choi, *Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory*, SYMPOSIUM ON VLSI TECHNOLOGY DIGEST OF TECHNICAL PAPERS, 78–79 (2016) (Ex. 1007).

⁴ Izumi, US 2012/0151301 A1, published June 14, 2012 (Ex. 1008).

⁵ Nam, US 2015/0003169 A1, published Jan. 1, 2015 (Ex. 1006).

Pet. 8. Petitioner relies on the Declaration of David Kuan-Yu Liu (Ex. 1003) in support of its contentions.

II. ANALYSIS

A. *Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “a master’s degree in electrical engineering or a similar discipline” with “4–5 years of professional experience working with (e.g., researching, designing, or developing) NAND flash memory devices (including issues relating to the operation, e.g., reading of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).”

Pet. 21–22 (citing Ex. 1003 ¶¶ 35–39). At this stage of the proceeding, Patent Owner neither responds to Petitioner’s proposed definition, nor provides a definition of its own. *See generally*, Prelim. Resp. Petitioner’s undisputed proposed definition appears to be consistent with the cited prior art and the disclosure of the ’342 patent, and we adopt it for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

B. *Claim Construction*

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of

ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Based on the record before us, we determine that no claim term requires express construction for purposes of this Decision.

C. Asserted Obviousness over Seo and Choi

Petitioner contends that claims 1–6, 8–14, and 16–20 would have been obvious over Seo and Choi. Pet. 29–66.

1. Overview of Seo

Seo is “directed to a memory device capable of improving a disturb phenomenon of an unselected memory string during a read operation.” Ex. 1005 ¶ 8. The memory device includes a memory cell array having a plurality of memory strings, a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation. *Id.* ¶ 9. “The memory device also includes control logic configured to control the voltage generating circuit to generate” first and second drain select line voltage applied to first and second unselected memory strings “among the unselected memory strings during the read operation, wherein the second drain select line voltage is different from the first drain select line voltage.” *Id.* Seo teaches that the “second drain select line voltage [is] applied to second unselected memory strings among the unselected memory strings at a second potential level lower than the first potential level.” *Id.* ¶ 10.

Seo describes a read operation where a first voltage V1 is applied to first drain select line DSL0 and first source select line SSL0 corresponding to a selected memory string ST, and a second voltage V2 is applied to second drain select line DSL1 corresponding to the unselected memory string that shares first select source line SSL0, during a first time period t1. *Id.* ¶ 88. Seo teaches that “second voltage V2 may have the same potential level as the first voltage V1.” *Id.* Seo further teaches that “[s]ubsequently, the pass voltage Vpass may be applied to unselected word lines Unsel WLs,” then “the read voltage Vread may be applied to a selected word line Sel WL during a second time period t2.” *Id.* ¶¶ 89–90.

2. Overview of Choi

Choi teaches that fast charge loss (which it refers to as “early retention”) “mainly originates from the lateral charge loss through the shared charge trap layers.” Ex. 1007, 1:9–11;⁶ *see also id.* at 2:23–25 (“This observation indicates that the early retention mainly occurs through lateral charge loss in the shared charge trap layers rather than vertical charge loss.”). Choi reports that during the erasing operation prior to programming, “the holes injected into the charge trap layer can spread outside of cells” and trapped electrons “cannot completely compensate the injected holes resulting in residual holes.” *Id.* at 2:12–16. Choi explains that “[a]s a result, a large lateral electric field is generated at the edge of the cell in which there is a greater chance for stored charges in a charge trap layer to spread laterally.” *Id.* at 2:16–18. Choi concludes that “the non-compensated

⁶ We refer to the left column on page 1 of Choi as column 1 and the right column on page 2 as column 2. *See* Ex. 1007, 1.

residual holes at the edge of the cells play a significant role in early retention and, thus, should be optimized and balanced.” *Id.* at 2:54–56.

3. *Claims 1–6 and 8–14*

Petitioner contends that the combination of Seo and Choi teaches all of the limitations of independent claim 1. Pet. 29–39. For example, with respect to limitations [1.A]–[1.C], Petitioner contends that Seo teaches “applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period” (applying, on Unsel DSL (DSL1), V2 during t1 and off voltage during t2), “applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period” (applying, on Sel WL, 0 volts during t1 and Vread during t2), and “applying, on an unselected word line, a pass voltage during the first time period and the second time period” (applying Vpass on Unsel WL during t1 and t2). *Id.* at 30–35.

Limitation [1.D] recites “wherein the read-verification operation removes fast charges of the target memory cell during the first time period.” Ex. 1001, 14:65–67. Petitioner contends that “the ’342 patent discloses that ‘[r]emoving the fast charges of the target memory cell includes’ applying the voltages of limitations [1.A]–[1.C]” and “Seo discloses these voltages.” Pet. 36 (citing Ex. 1001, code (57)) (emphases omitted; alteration in original). In particular, Petitioner contends that “Seo teaches having a higher voltage on unselected WLs (e.g., adjacent WLs to the selected WL) *during the first time period.*” *Id.* Petitioner contends that the ’342 patent recognizes that “this voltage differential removes fast charges.” *Id.* (citing Ex. 1001, 12:24–34; Ex. 1003 ¶¶ 129–131).

Petitioner further contends that “Seo discloses, or would have been understood to disclose, charge-trap 3D memories,” because “Seo discloses that its read operation is for a 3D Flash memory device,” and “[c]harge-trap memory is a type of 3D memory device” that “suffers from the ‘disturb phenomenon’ that Seo specifically addresses.” Pet. 36 (citing Ex. 1005 ¶ 8; Ex. 1017, 101, 108). According to Petitioner, “a charge-trap memory was one of two basic types of 3D Flash memory devices” and “were incredibly popular, textbook material in 2019.” *Id.* (citing Ex. 1017, 101, 144).

Patent Owner responds that Seo “does not discuss any techniques for removing fast charges during a read-verify operation,” and instead “is concerned with trying to mitigate unrelated sources of read disturb stemming from ‘Hot Carrier Injection,’ which occurs in a different location entirely.” Prelim. Resp. 25 (citing Ex. 1005 ¶¶ 89, 127). In particular, Patent Owner explains that “‘fast charges’ relate to shallowly trapped electrons in the memory cell storage layer, while ‘hot carrier injection’ is a distinct phenomenon that takes place in the channel of the memory cell string.” *Id.* (citing Ex. 1005 ¶ 104; Ex. 1001, 2:45–47).

Patent Owner argues that Petitioner incorrectly asserts that the ’342 patent recognizes that having a higher voltage on unselected word lines as compared to selected word lines inherently removes fast charges, because the ’342 patent “does not state or even suggest that a mere difference between unselected and selected word line voltages will necessarily remove fast charges.” *Id.* at 26. Instead, Patent Owner argues that the ’342 patent’s statements with respect to the memory cell structure in Figure 4A and the voltages and timing diagram in Figure 6 that an electric field parallel to the channel that extends into the charge storage layer, the tunneling layer, and the channel layer is sufficient to de-trap fast charges so that they can be

recombined and removed “do not suggest that Seo’s voltage amounts applied during Seo’s time period operate the same way on Seo’s memory device to generate fields with sufficient magnitude and duration to remove fast charges.” *Id.* at 26–27 (citing Ex. 1001, 12:24–34). Patent Owner further argues that “Seo says nothing about the actual voltages used during the first time period, how long the voltages are applied, or how those relate to removing fast charges in the context of Seo’s particular device.” *Id.* at 26–27 (alterations in original).

We understand Petitioner to be arguing that Seo inherently discloses a read-verification operation that “removes fast charges of the target memory cell during the first time period.” As Patent Owner notes, “Seo does not acknowledge the existence of fast charges, and does not discuss any techniques for removing fast charges during a read-verification operation.” Prelim. Resp. 25. In order to rely on inherency to establish the existence of a missing claim limitation in an obviousness analysis, “the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art.” *PAR Pharma, Inc. v. TWi Pharms., Inc.*, 773 F.3d 1186, 1195–96 (Fed. Cir. 2014). Petitioner, therefore, must show that fast charges of the target memory cell necessarily are removed during the first time period of Seo’s read-verification operation. On this record, neither Petitioner nor Dr. Liu sufficiently demonstrates that Seo’s read-verification operation would necessarily remove fast charges of the target memory cell during the first time period.

Petitioner and Dr. Liu assert that the ’342 patent recognizes that the voltage differential between the unselected WLs and the selected WL removes fast charges because the Abstract states that removing fast charges includes applying certain voltages to an unselected top select gate, a selected

word line, and an unselected word line. Pet. 36; Ex. 1003 ¶ 131. Petitioner and Dr. Liu also point to the '342 patent's description of an embodiment in which an electric field between the selected and unselected word line generates an electric force on fast charges captured in the storage layer that de-traps and removes the fast charges. Ex. 1001, 12:24–34. Petitioner and Dr. Liu, however, do not adequately explain why it follows from these disclosures in the '342 patent that the application of voltages described in Seo necessarily results in the removal of fast charges. In particular, we agree with Patent Owner that Petitioner and Dr. Liu do not provide any objective evidence or explanation as to how or why a POSITA would have understood that Seo's voltage amounts applied during Seo's time periods operate the same way on Seo's memory device to generate fields with sufficient magnitude and duration to remove fast charges. *See* Prelim. Resp. 26–27. That there is a possibility that Seo's applied voltages would remove fast charges is insufficient to establish inherency. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (Inherency “may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” (quotation omitted)).

Petitioner also contends that “it would have been obvious to employ Seo's read operation in a 3D charge-trap memory with the knowledge that it removes fast charges in view of Choi.” Pet. 37. Petitioner contends that “Choi specifically discloses a ‘3-D NAND flash memory with a charge trap layer,’” and “addresses the issue of ‘early retention (fast charge loss within a few seconds).”” *Id.* (citing Ex. 1007, 1:16–17). Petitioner contends that Choi teaches shallowly trapped electrons “are more likely to be lost due to lateral movement when ‘a large lateral electric field is generated at the edge

of the [memory] cell,’ i.e., near the interfaces with adjacent cells.” *Id.* (citing Ex. 1007, 1:28–29, 2:4–25, Fig. 1). Petitioner contends that, because “Seo creates such ‘a large lateral electric field,’” “it would have been obvious to employ Seo’s read operation in Choi’s charge-trap memory with Choi’s express disclosure of removing fast charges.” *Id.* at 38 (citing Ex. 1003 ¶¶ 137–138).

As we understand it, Petitioner is arguing that Choi teaches that in a large lateral electric field generated at the edge of the cell, there is a greater likelihood of fast charge loss, and because Seo also creates a large lateral electric field, it would have been obvious to apply Seo’s voltages to Choi’s charge-trap memory to remove the fast charges. We explain above, however, that Petitioner does not sufficiently establish that Seo’s applied voltages necessarily remove fast charges as required by claim 1.

We also note that Petitioner admits that Seo focuses on Hot Carrier Injection (“HCI”), but nevertheless would have been motivated to consider Choi’s teachings regarding fast-charge loss because “[b]oth issues were well known to a POSITA” and “knowing that Seo only expressly addressed HCI, a POSITA would have been motivated to consider Choi’s teachings regarding an additional reliability issue.” Pet. 64 (citing Ex. 1003 § 230). But Choi does not teach the claimed parameters for fast-charge loss, and Petitioner does not adequately support its statement that “a POSITA would have recognized that using Seo’s read operation to verify, which removes the fast charges, would result in a more accurate verification, because any threshold shifting would occur before verification.” *Id.* at 65 (citing Ex. 1003 § 232). In particular, Dr. Liu’s statement that “[a] POSITA would have recognized that the lateral-electrical-field-inducing voltage differential, as Seo discloses, is what Choi describes as driving the lateral fast-charge

loss” is not supported by objective evidence or sufficient explanation as to why a POSITA would have come to that understanding.

To the extent that Petitioner is arguing that Choi teaches that a large lateral electric field removes fast charges, we disagree. Choi teaches “a large lateral electric field is generated at the edge of the cell in which there is a greater chance for stored charges in a charge trap to spread laterally.” Ex. 1007, 2:16–18. Choi also teaches that the large lateral electric field is generated when, during the erasing operation prior to programming, “the holes injected into the charge trap layer can spread outside of cells” and trapped electrons “cannot completely compensate the injected holes resulting in residual holes.” *Id.* at 2:12–18. Choi concludes that fast charge loss can be reduced by optimizing and balancing the non-compensated residual holes. *Id.* at 2:54–56; *see also id.* at 1:9–12 (“Our findings indicate that the [fast charge loss] mainly originates from the lateral charge loss through the shared charge trap layers and suggest that the program and erase levels should be balanced and optimized to reduce the [fast charge loss].”). Moreover, Choi points to these non-compensated holes as causing the “large lateral electric field,” not some applied voltage as taught by Seo. *Id.* at 2:12–18. At best, Choi attributes the spread to the erasing step, and Petitioner does not explain why parameters of Choi’s erasing are pertinent to Seo’s read-verification step. *See id.* at 2:4–18; Prelim. Resp. 28.

We are also not persuaded, on this record, that Petitioner sufficiently establishes that Seo creates a large lateral electric field like the one described in Choi. In that regard, Petitioner and Dr. Liu simply state that “Seo creates such ‘a large lateral electric field,’” without providing sufficient and credible explanations as to why that would be the case. *See* Pet. 38; Ex. 1003 ¶ 138.

For these reasons, we determine that Petitioner does not establish a reasonable likelihood that it would prevail in showing that claim 1, and claims 2–6 and 8–14 that depend, directly or indirectly therefrom, would have been obvious over the combined teachings of Seo and Choi.

4. *Claims 16–20*

Petitioner contends that the combination of Seo and Choi teaches all of the limitation of independent claim 16, and claims 17–20 that depend, directly or indirectly, therefrom. Pet. 52–62. Petitioner relies on the same arguments with respect to the “on a target memory cell, a read-verification operation for removing fast charges during a first time period” element of limitation [16.B], and limitations [16.B.i]–[16.B.iii], as it did with respect to limitations [1.A]–[1.D] discussed above. *Id.* at 56–58. For the same reasons set forth with respect to claim 1, we determine that Petitioner does not establish a reasonable likelihood of prevailing in showing that claim 16, and claims 17–20 that depend therefrom, would have been obvious over the combined teachings of Seo and Choi.

D. *Asserted Obviousness over Nam and Choi*

Petitioner contends that claims 1–3, 5, 6, 8–14, 16, 17, 19, and 20. Pet. 69–103.

1. *Overview of Nam*

Nam describes a method of reading a nonvolatile memory device that includes applying a read voltage to a selected wordline, applying a read pass voltage to unselected wordlines, sensing a state of a memory cell connected to the selected wordline, and applying the read pass voltage to the selected wordline after sensing. Ex. 1006 ¶ 6.

Figure 10 is reproduced below.

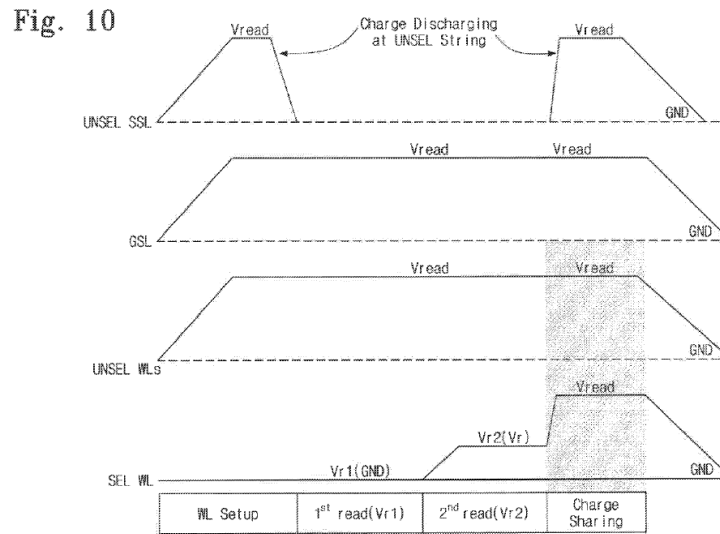


Figure 10 is a timing diagram illustrating an immune disturbance read operation described in Nam. Ex. 1006 ¶ 43. In the word line setup section WL Setup, a ground voltage GND is applied to a selected word line SEL WL, and a read pass voltage Vread is applied to unselected word lines UNSEL WL. *Id.* ¶ 105. In the first read section, a first sensing operation may be performed to sense an on/off state of a memory cell using ground voltage GND or a first read voltage Vr1, and a second sensing operation may be performed in the second read section to sense an on/off state of the memory cell using the read voltage Vr or a second read voltage Vr2. *Id.* ¶ 106. The read pass voltage Vread is applied to unselected string selection lines UNSEL SSL before the sensing operation (i.e., before the first read and the second read). *Id.* ¶ 122. In the Charge Sharing section, read pass voltage Vread is applied to unselected string selection lines UNSEL SSL. *Id.*

2. Claims 1–3, 5, 6, and 8–14

Petitioner contends that the combination of Nam and Choi teaches all of the limitations of claim 1. Pet. 71–83. For example, with respect to

limitations [1.A]–[1.C], Petitioner contends that Nam teaches “applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period” (applying, on UNSEL SSL, Vread during WL setup and GND during first and second read periods), “applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period” (applying, on SEL WL, Ground during WL Setup and Vr1(GND) during first read period and Vr2(Vr) during second read period), and “applying, on an unselected word line, a pass voltage during the first time period and the second time period” (applying read pass Vread on UNSEL WLs during WL Setup, and first and second reads). *Id.* at 73–81.

With respect to limitation [1.D] (“wherein the read-verification operation removes fast charges of the target memory cell during the first time period”), Petitioner contends that Nam states that its memory is applicable to NAND flash memory, and specifically depicts a charge-trap device. Pet. 81–82 (citing Ex. 1006 ¶¶ 99, 164, claim 24, Fig. 5; Ex. 1003 ¶¶ 293–297). Petitioner contends that “Nam teaches having a higher voltage on unselected WLs (including WLs adjacent to the selected WL) relative to the selected WL during the *first time period*, WL Setup,” which “creates a lateral electric field that removes fast charges.” *Id.* at 82–83 (citing Ex. 1001, 12:24–34). Petitioner also contends that “Choi expressly teaches that voltage differential removes fast charges,” and “[t]hus, in view of Choi, a POSITA would have understood that Nam’s read-verification operation removes fast charges in a charge-trap memory.” *Id.* at 83 (citing Ex. 1003 ¶ 299).

Patent Owner responds, as it did with respect to Petitioner's contentions based on Seo and Choi, that "Petitioner again is mistakenly arguing that having a higher voltage on unselected WLs inherently removes fast charges." Prelim. Resp. 31. Patent Owner also argues that "Petitioner mischaracterizes Choi as teaching that a 'voltage differential removes fast charges'" and "is once again mistakenly arguing that having a higher voltage on unselected WLs inherently removes fast charges or renders doing so obvious." *Id.* at 31–32.

We understand Petitioner to be arguing that Nam inherently discloses a read-verification operation that "removes fast charges of the target memory cell during the first time period." Pet. 83. Petitioner, therefore, must show that fast charges of the target memory cell necessarily are removed during the first time period of Nam's read-verification operation. *See PAR Pharma*, 773 F.3d at 1195–96. On this record, neither Petitioner nor Dr. Liu sufficiently demonstrates that Nam's read-verification operation would necessarily remove fast charges of the target memory cell during the first time period.

Petitioner and Dr. Liu point to the '342 patent's description of an embodiment in which an electric field between the selected and unselected word line generates an electric force on fast charges captured in the storage layer that de-traps and removes the fast charges to support the contention that the voltage differential between Nam's unselected and selected WLs during WL Setup "creates a lateral electric field that removes fast charges." Pet. 83 (citing Ex. 1001, 12:24–34); Ex. 1003 ¶ 298. Petitioner and Dr. Liu, however, do not adequately explain why it follows from these disclosures in the '342 patent that the application of voltages described in Nam necessarily results in the removal of fast charges. In particular, Petitioner and Dr. Liu

do not provide any objective evidence or explanation as to how or why a POSITA would have understood that Nam's voltage amounts applied during Nam's time periods operate the same way on Nam's memory device to generate fields with sufficient magnitude and duration to remove fast charges. *See* Prelim. Resp. 32. Furthermore, we are not persuaded, on this record, that Petitioner sufficiently establishes that Nam creates a lateral electric field. Petitioner and Dr. Liu simply state that voltage differentials in charge trap devices create a lateral electric field that removes fast charges without providing sufficient and credible explanations as to why that would be the case. *See* Pet. 83; Ex. 1003 ¶ 298. That there is a possibility that Nam's applied voltages would remove fast charges is insufficient to establish inherency. *See In re Robertson*, 169 F.3d at 745.

We are also not persuaded that "Choi expressly teaches that voltage differential removes fast charges." Pet. 83. Petitioner refers to the arguments it made with respect to Choi and limitation [1.D] in its ground based on Seo and Choi in support of this contention. *See id.* (citing Pet. 36–38 (§ IX.A.1[1.D])). We are not persuaded by those arguments for the reasons set forth above. *See* § II.C.3, *supra*. Notably, Patent Owner does not direct us to, nor do we discern, any disclosures in Choi regarding voltage differentials. In that regard, we agree with Patent Owner that "Choi does not disclose applying voltages to different word lines, or under what specific circumstances those voltages would remove fast charges following a programming operation." Prelim. Resp. 33–34.

For these reasons, we determine that Petitioner does not establish a reasonable likelihood that it would prevail in showing that claim 1, and claims 2, 4, 5, 6, and 8–14 that depend, directly or indirectly therefrom, would have been obvious over the combined teachings of Nam and Choi.

3. *Claims 16, 17, 19, and 20*

Petitioner contends that the combination of Nam and Choi teaches all of the limitation of independent claim 16, and claims 17, 19, and 20 that depend, directly or indirectly, therefrom. Pet. 94–101. Petitioner relies on the same arguments with respect to the “on a target memory cell, a read-verification operation for removing fast charges during a first time period” element of limitation [16.B], and limitations [16.B.i]–[16.B.iii], as it did with respect to limitations [1.A]–[1.D] discussed above. *Id.* at 98–100. For the same reasons set forth with respect to claim 1, we determine that Petitioner does not establish a reasonable likelihood of prevailing in showing that claim 16, and claims 17, 19, and 20 that depend therefrom, would have been obvious over the combined teachings of Nam and Choi.

E. *Remaining Grounds*

Petitioner contends that claim 15, which directly depends from claim 1, would have been obvious over the combination of Seo, Choi, and Izumi, or Nam, Choi, and Izumi. Pet. 66–69, 103–105. Petitioner does not rely on Izumi to remedy the deficiencies identified above with respect to Petitioner’s contentions regarding independent claim 1. *See id.* Accordingly, for the reasons set forth above with respect claim 1, we determine that Petitioner does not establish a reasonable likelihood of prevailing on its assertion that claim 15 would have been obvious over the combined teachings of Seo, Choi, and Izumi, or Nam, Choi, and Izumi. *See* §§ II.C.3, II.D.2, *supra*.

III. CONCLUSION

Based on the arguments in the Petition and the Preliminary Response, and the evidence of record, we determine that Petitioner does not establish a

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reasonable likelihood of prevailing on its challenge that claims 1–6 and 8–20 of the '342 patent are unpatentable.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied*, and no trial is instituted.

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