UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00793
U.S. Patent No. 11,600,342
Issue Date: March 7, 2023

Title: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

MOTION FOR REHEARING PURSUANT TO 37 C.F.R. § 42.71

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,600,342 to Chen et al.
1002	File History of U.S. Patent No. 11,600,342 to Chen et al.
1003	Declaration of David Kuan-Yu Liu, Ph.D. ("Liu")
1004	*Curriculum Vitae* of David Kuan-Yu Liu, Ph.D.
1005	U.S. Patent Publ. No. 2021/0027848 A1 to Seo ("Seo")
1006	U.S. Patent Publ. No. 2015/0003169 A1 to Nam et al. ("Nam")
1007	Choi et al., "Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory," 2016 Symposium on VLSI Technology, Digest of Technical Papers, 78-79 ("Choi")
1008	*Intentionally Omitted*
1009	Minute Order, Dkt. No. 42, dated February 22, 2024 in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1010	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1011	Docket from *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1012	U.S. Patent No. 9,589,978 to Yip
1013	Aritome, "NAND Flash Memory Technologies" (2016)
1014	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017

Exhibit	Description
1015	U.S. Patent Publ. No. 2020/0168276 A1 to Yang
1016	U.S. Patent No. 9,620,233 to Dong et al.
1017	Micheloni, “3D Flash Memories” (2016)
1018	U.S Patent No. 10,276,251 B1 to Lobana et al.
1019	U.S Patent No. 9,361,993 B1 to Chen et al.
1020	Affidavit of Nathaniel E. Frank-White (Internet Archive) re Choi Reference (Ex. 1007)
1021	Declaration of Gordon MacPherson (IEEE) re Choi Reference (Ex. 1007)
1022	Certified File History of U.S. Patent No. 10,403,637 to Lue
1023	Wu et al., “Multiscale simulation of lateral charge loss in Si3N4 3D NAND flash based on density functional theory,” Journal of Physics D: Applied Physics, vol. 52, no. 39, 395103, 2019
1024	U.S. Patent Publ. No. 2019/0198117 A1 to Yu et al.
1025	U.S. Patent No. 10,121,529 B2 to Lee
1026	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1027	U.S. Patent Publ. No. 2020/0395372 A1 to Seo et al.
1028	U.S. Patent Publ. No. 2019/0348122 A1 to Ko et al.
1029	U.S. Patent Publ. No. 2016/0293271 A1 to Won et al.
1030	*Intentionally Omitted*
1031	*Intentionally Omitted*
1032	*Intentionally Omitted*
1033	*Intentionally Omitted*

Exhibit	Description
1034	*Intentionally Omitted*
1035	Complaint for Patent Infringement, Dkt. No. 1, filed Nov. 9, 2023, in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1036	First Amended Complaint for Patent Infringement, Dkt. No. 29, filed Feb. 2, 2024, in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1037	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1038	Declaration of Jared Bobrow in Support of Petitioner's Motion for Admission *Pro Hac Vice*

I. INTRODUCTION

On December 2, 2024, the Patent Trial and Appeal Board ("Board") declined to institute *inter partes* review of claims 1-6 and 8-20 of U.S. Patent No. 11,600,342 B2 ("the '342 patent," Ex. 1001). *See* Paper 12 ("ID"). Petitioner Micron Technology, Inc. ("Petitioner" or "Micron") respectfully requests rehearing of that decision pursuant to 37 C.F.R. § 42.71(d) on the grounds that the Board (1) misapprehended Petitioner's obviousness argument to be an inherency argument, (2) overlooked the Petition's showing that the prior art discloses or renders obvious ***the specific voltage magnitudes*** that the '342 patent ***admits*** remove fast charges, and (3) overlooked the Petition's showing that the prior art renders obvious applying the voltages for a ***sufficiently long duration*** to remove fast charges in order to address the problem of fast-charge loss over time.

The '342 patent is directed to addressing the problem of fast-charge loss in a charge-trap 3D NAND memory device. Fast-charge loss involves the escape of shallowly trapped particles from the charge-trap layer of a memory cell over time, which can result in inaccurate threshold voltage determinations (namely, during a read-verification operation). To avoid inaccuracies caused by fast-charge loss over time, representative independent claim 1 of the '342 patent recites a method for "removing fast charges of the target memory cell at a read-prepare step" that takes place before a sensing operation. Ex. 1001, Abstract. Elements [1.A] through [1.C]

recite a two-step "read-verification" operation, wherein during a first time period, three voltages create "an electric field" that removes fast charges. ID, 3-4. Hence element [1.D] of the claim recites: "wherein the read-verification operation removes fast charges of the target memory cell during the first time period." Ex. 1001, 14:65-67. The three voltages that remove these fast charges are: (1) a prepare voltage, (2) an off voltage, and (3) a pass voltage. ID, 3-4; *see* Pet., 17-18.

The Petition demonstrates that every element of the '342 patent's method would have been obvious to a person of ordinary skill. *See generally* Paper 1 ("Pet."). The Petition establishes that the Seo and Nam prior art references each discloses or renders obvious a two-step read-verification operation for a 3D NAND memory device, just like the '342 patent. Pet., 22-24, 24-25, 29-35, 71-81. The Petition further explains that this two-step read-verification operation creates an electric field of sufficient magnitude to actually remove fast charges. Pet., 36, 82-83. The Petition cites Choi, which describes the unwanted effect of fast-charge loss over time (e.g., in Figure 2) and the primary cause of fast-charge loss, i.e., a lateral electric field, which can cause verification to fail. Pet., 27-28. Finally, the Petition demonstrates that in view of the impact of fast-charge loss on verification (as Choi teaches), a POSITA would have been motivated to apply the operations of Seo and Nam, including the three key voltages of claim 1, to accelerate fast-charge loss and improve the read-verification operation. Pet., 36-38, 83, 62-66, 101-103.

In Patent Owner's preliminary response (Paper 11, "POPR"), Patent Owner did not dispute that Seo and Nam both teach elements [1.A]-[1.C] of the claim—the two-step read-verification operation recited by the '342 patent. Nor did Patent Owner dispute that the methods of Seo and Nam apply a voltage differential during the first time period, which results in the creation of an electric field. Instead, Patent Owner argued that Seo and Nam did not disclose the "magnitude or duration of the applied voltages" (the three key voltages, which in turn create the corresponding electric field) in their respective read-prepare steps and that, as a result, Petitioner had not established that either reference "necessarily or inherently" removes fast charges. POPR, 14, 17, 22, 30. Patent Owner's entire response centered on this "flawed inherency" argument that supposedly is at the center of Petitioner's challenge. POPR, 2. And lack of inherency became the Board's entire reason for rejecting the Petition: The Board agreed with Patent Owner that Petitioner had not established that either Seo or Nam "inherently" or "necessarily remove[s] fast charges," dooming all of Petitioner's proposed combinations. ID, 12-15, 19-20.

Respectfully, Petitioner did not advance an inherency argument. Rather, Petitioner presented obviousness arguments. Specifically, the Petition establishes that Seo and Nam disclose each of the three key voltages in precisely the magnitude range that the '342 patent itself says—and claims in dependent claims—removes fast charges. Moreover, the Petition demonstrates that it would have been obvious

to apply these voltages (which admittedly remove fast charges) for a sufficient duration to improve the verification operation, because Choi teaches (and illustrates in its Figure 2) that not removing fast charges may result in the verification operation sensing the wrong data state. Indeed, the methods of Seo and Nam are for verification operations, and Choi simply demonstrates the benefits of these operations on the verification process.

The Board's failure to analyze Petitioner's arguments under the standard of obviousness led it to overlook key evidence and erroneously deny institution of review. A rehearing is warranted.

II. STANDARD OF REVIEW

Under 37 C.F.R. § 42.71(d), a party "may file a single request for rehearing[,] specifically identif[ying] all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed." On rehearing, the Board reviews a previous decision "for an abuse of discretion." 37 C.F.R. § 42.71(c). That standard is met where the Board "made a clear error of judgment in weighing relevant factors or exercised its discretion based upon an error of law or clearly erroneous factual findings." *Novo Nordisk of N. Am., Inc. v. Genentech, Inc.*, 77 F.3d 1364, 1367 (Fed. Cir. 1996). It includes instances where the Board overlooks relevant disclosures in a prior art reference. *See Merial Ltd. v. Virbac*, IPR2014-01279, Paper 18 at 7-8 (PTAB Apr. 15, 2015).

III. ARGUMENT

A. The Board, at Patent Owner's urging, incorrectly treated Micron's obviousness argument as an inherency argument.

Patent Owner's preliminary response—and the Board's decision—is premised on the notion that Petitioner relies purely on an "inherency" argument to show that its proposed combinations "necessarily" remove fast charges. ID, 12 (quoting *PAR Pharma, Inc. v. TWi Pharmas., Inc.*, 773 F.3d 1186, 1195-96 (Fed. Cir. 2014)); *see* POPR, 3-4; ID 11-14, 19-20. But Petitioner did not argue inherency. Instead, the Petition clearly presented an ***obviousness*** challenge, pointing not only to what Seo, Nam, and Choi "expressly teach[]," but also what they would "fairly suggest[]" to a person of ordinary skill. *Bradium Techs. LLC v. Iancu*, 923 F.3d 1032, 1049 (Fed. Cir. 2019); *see* Pet., 29 (obvious over "Seo in view of Choi and the knowledge of a POSITA"), 69 (obvious over "Nam in view of Choi and the knowledge of a POSITA"); *see also* Pet. 36-38, 62-66, 81-83, 101-02. Petitioner did not use the word "inherent" or "inherency" once. To the contrary, the Petition expressly identifies four obviousness grounds, each of which is based on two or more references. *See SAS Inst., Inc. v. Iancu*, 584 U.S. 357, 366 (2018) ("[T]he petitioner's petition … is supposed to guide the life of the litigation.").

That the Petition relies on obviousness is critical to this motion because the Institution Decision concludes that Seo and Nam do not inherently disclose "generat[ing] fields with sufficient magnitude and duration to remove fast charges."

ID, 13, 20. But Petitioner met its burden to show that Seo and Nam, in light of Choi, render both the necessary magnitude and duration ***obvious***, regardless of whether the methods they disclose necessarily have that effect.

To start, as discussed in more detail below (*see* § II.B), the Petition establishes that Seo and Nam disclose and/or render obvious the ***exact magnitudes*** of voltages that the ***claims of the '342 patent recite*** as removing fast charges—a showing that the Patent Owner also misled the Board into overlooking. In view of this, there can be no reasonable dispute that Seo and Nam "generate fields with sufficient magnitude" to remove fast charges. *Contra* ID, 13, 20 (finding that Petition did not provide such a showing).

Next, as discussed in greater detail below (*see* § II.C), Petitioner also established that the Grounds in the Petition would render obvious the application of these voltages for a sufficient ***duration*** to remove fast charges. Specifically, the Petition argues that it would have been ***obvious***, and a POSITA would have been motivated, to apply the voltages of Seo and Nam to remove fast charges to improve the verification operation. Pet., 64-65 ("Choi describes a use case for Seo's read operation and teaches that Seo's read operation would be beneficial to verify after programming."). To achieve that effect, a POSITA would have applied the voltages disclosed by Seo and Nam for a sufficient duration to remove fast charges.

At bottom, the proper question is whether it would have been obvious to apply the voltage waveforms of Seo or Nam—which Section II.B below demonstrates have sufficient magnitudes to remove fast charges—for an adequate time to achieve the known benefit of removing fast charges, e.g., before verification. Pet., 65 (citing Ex. 1003, ¶ 232 and explaining that applying this waveform removes fast charges to bring the program state into a steady state). As Section II.C below demonstrates, Petitioner made that showing. By focusing solely on inherency, the Board "fundamentally misconstrued" and "failed to adequately evaluate" Petitioner's obviousness argument. *Power Integrations, Inc. v. Lee*, 797 F.3d 1318, 1323-25 (Fed. Cir. 2015). It was not Petitioner's burden to establish—in a vacuum—that in Seo and Nam, "fast charges of the target memory cell necessarily are removed."[1]

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[1] Indeed, Petitioner does not contest that Seo and Nam do not explicitly "discuss any techniques for removing fast charges during a read-verification operation." ID, 11 (quoting POPR, 25); *see also* POPR, 17 ("Nam does not contemplate the existence of fast charges"). It was for that reason that the Petition expressly combines these primary references with Choi. Choi explains the primary mechanism and unwanted impact of fast-charge loss on verification. This provides a motivation for a POSITA to use Seo's and Nam's methods to achieve fast charge removal to improve verification. *See* §II.C.

ID, 12; *see* ID 19. That in and of itself constitutes legal error. *See Netflix, Inc. v. DivX, LLC*, No. 22-1083, 2023 WL 2298768, at *4 (Fed. Cir. Mar. 1, 2023) (explaining how a "redefinition" of the petitioner's argument constitutes "fundamental legal error").

B. The Board, at Patent Owner's urging, overlooked that Seo and Nam disclose or at least render obvious the exact voltage magnitudes that the claims of the '342 patent recite as removing fast charges.

Citing the POPR, the Institution Decision concludes that the electric field resulting from the voltages of Seo and Nam may not be of "sufficient magnitude and duration to remove fast charges."[2] ID, 13, 20. Critically, because Patent Owner did not address the Petitioner's full showing or the '342 patent's dependent claims at all, the Board overlooked that the Petition establishes that the voltages of Seo and Nam have the very same ***magnitudes*** that the '342 patent asserts remove fast charges.

As an initial matter, Patent Owner does not dispute that both Seo and Nam teach every element of the claimed "two-step read-verification operation" of the

[2] The Board also limited its analysis of the methods of Seo and Nam to the particular "memory device" expressly disclosed by each, again as a result of its inherency framing. *E.g.*, ID, 13. The Petition, however, advances an obviousness theory, combining the read operations of Seo and Nam with a conventional charge trap device. *E.g.*, Pet., 63.

’342 patent “that applies different voltages during different time periods.” *Compare* POPR, 5 (describing two-step read-verification operation) *with* Pet., 30-35 (explaining that Seo discloses claim elements [1.A]-[1.C]); Pet., 73-81 (explaining that Nam discloses claim elements [1.A]-[1.C]). Patent Owner further acknowledges that the two-step operation creates an “electric field” during “the first time period,” and further that this electric field exerts a force causing the removal of fast charges. *Compare* POPR, 6-7 *with* Pet., 17-18; *see also* Ex. 1001, 12:24-34. What’s more, Patent Owner does not dispute that the voltage differential created via Seo’s and Nam’s applied voltages “result[s] … [in an] electric field.” POPR 20, 21 (linking Seo’s and Nam’s “voltage difference” with the “resulting electric field”); *see id.* 14, 17 (similar). Instead, Patent Owner merely disputes that Petitioner established that Seo and Nam’s “prepare,” “off,” and “pass” voltages are of sufficient “magnitude and duration” to create an electric field to remove fast charges. POPR, 27, 32; *see* ID, 13, 20. In agreeing with Patent Owner, the Board clearly erred.

As to Nam, the Petition establishes that Nam discloses a 7V prepare voltage that is “within the exemplary ’342 range” of 4V to 7V. Pet., 75; *compare* Ex. 1001, 2:40-44, *with* Nam, [0098]; *see also* Pet., 92 (claim 9). The Petition establishes that Nam also uses 7V for the pass voltage, Pet., 80, 92 (claim 10), which again is within the exemplary ’342 range of 5V to 9V, Ex. 1001, 2:40-44. And the Petition

establishes that Nam's off voltage is a ground voltage—or 0V, Pet., 78 & n.13 (citing Nam, [0105], [0100]), again matching the off voltage of the '342 patent's exemplary embodiment. Ex. 1001, 2:40-44; *see also* Pet., 92 (claim 11). Indeed, Nam's voltages directly correspond to the exemplary voltages disclosed by the '342 patent, which, by virtue of dependent claims 9-11, satisfy claim 1, including the fast-charge removal limitation.

As to Seo, the Petition establishes that Seo discloses a prepare voltage capable of turning on the top select transistor, so a person of ordinary skill would have understood it to be within the exemplary range of 4V to 7V. Pet., 32, 48-49 (claim 9); *see* Ex. 1003, ¶¶ 119-121, 173-174. A person of ordinary skill also would have understood Seo's pass voltage to be within the '342 patent's exemplary 5V to 9V range, given the typical pass voltage of a 3D NAND Flash device. Pet., 35 (citing Ex. 1003, ¶ 127); Pet. 49 (claim 10, citing Ex. 1003, ¶ 176). And Seo discloses an off voltage of ground, which a person of ordinary skill would have understood to be 0V. Pet., 33-34 (citing Ex. 1003, ¶ 124); *see also id.* 49-50 (claim 11). Therefore, Seo discloses, or at least renders obvious, voltages in the '342 patent's exemplary range as well. Ex. 1001, 2:40-44.

There can be no reasonable dispute that Seo and Nam generate an electric field of a sufficient magnitude to remove fast charges.

C. The Board, at Patent Owner's urging, overlooked that Seo and Nam in view of Choi render obvious application of voltage magnitudes long enough to remove fast charges.

The Board also overlooked, at the Patent Owner's urging, Petitioner's showing that the prior art references render obvious application of the three key voltages for a sufficient ***duration*** to remove fast charges. *E.g.*, ID, 13.

The Petition establishes (and Patent Owner does not dispute) that unintentional fast-charge loss was well known. Pet., 16 ("de-trap" discussion), 64-65 (Choi's discussion of fast-charge loss); Ex. 1003, ¶¶ 68, 232 (supporting Petition). Next, the Petition explains how fast-charge loss can render a program verification "unsuccessful," citing Choi. Pet., 65 (e.g., Figure 2 of Choi). In his declaration, Dr. Liu explains how Choi demonstrates that fast-charge loss inadvertently can cause a program state to shift. Ex. 1003, ¶ 232; *see also* Pet., 65. The Petition then establishes that it would have been obvious to apply the voltages of Seo and Nam to remove these fast charges for a "more accurate verification." Pet., 65. Specifically, if the verification occurs before fast-charge removal, then the verification will sense and verify the data state in the wrong state (below, PV3), because subsequent fast-charge removal will cause the data state to drift (below, from PV3 to PV2):

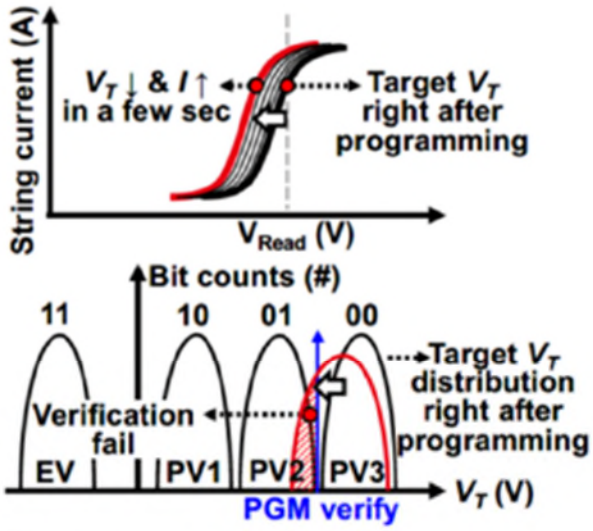

Fig. 2. Schematic of the early retention and its effect on V_T and I. The early retention threatens the MLC capability and the tight V_T distribution.

Ex. 1003, ¶ 232 (citing Choi's Figure 2); *see also* Pet., 65 (citing the same). If fast-charge removal occurs before the verification, however, there will be no such shift. That creates a more accurate read-verification. Pet. 65.

Respectfully, the Petition did not need to make any additional showing or identify a specific "duration" for two independent reasons, and Patent Owner's misleading arguments led the Board to overlook both of these reasons.

First, as demonstrated above, the Petition need not recite a specific duration that the voltages are applied, because the Grounds advance an argument that it would have been ***obvious*** to apply the methods of Seo and Nam in a manner that actually removes fast charges. Specifically, in order to improve the verification operation, a POSITA would have understood that Seo's and Nam's voltages must be applied long

enough to effectuate fast-charge removal. *See supra* § II.A. The Petition argues that it would have been obvious to use, for example, Seo's voltages such that "any threshold shifting [due to fast-charge loss or removal] would occur before verification." Pet., 65. Dr. Liu explains, in more detail, at Ex. 1003, ¶ 232: "A verification would then indicate the cell was in PV2 and require another programming pulse." In sum, the obviousness theory applies Seo's voltages—which admittedly have sufficient magnitude to remove fast charges (*see* §II.B)—long enough to remove fast charges, i.e., from a PV3 to PV2 state. Pet., 65; Ex. 1003, ¶ 232. The Petition also made this same showing as to Nam, demonstrating that a POSITA would have viewed application of Nam's sufficiently large voltage differential long enough to remove fast charges as obvious. Pet., 101 ("[A] POSITA would have been motivated to consider Choi … and improve on Nam's memory device."), 102 ("Choi makes clear that Nam's read operation would remediate fast charge issues in a verification that occurs close in time to a program operation.").

Second, the Board overlooked that the '342 patent asserts that fast charges "can be easily lost"—even without any intentional application of voltages to accelerate the loss—suggesting that an electric field need not be present for a lengthy period to de-trap fast charges. Ex. 1001, 1:29-36; Pet., 17 (citing same); *see also* Ex. 1001, 8:49-53. And the claims do not recite any particular amount of charge that must be removed. This is why the '342 patent does not recite a duration

requirement in discussing its method for fast-charge removal: "Removing the fast charges of the target memory cell includes applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL)." Ex. 1001, Abstract; *see also* Pet., 17 (citing the same). Put simply, the '342 patent's claims and specification describe no minimum length of time that voltages must be applied during the first time period to remove fast charges.

That the '342 patent does not discuss any "duration" requirement and, instead, states that fast charges are "easily lost" during any read-verification is critical. Nam expressly discloses that its read operation—which the '342 patent admits includes the voltages that remove fast charges (*see* §II.B)—is for read-verification, i.e., the period during which fast charges are particularly susceptible to removal according to the teachings of Choi. Pet., 71-72, 102-103. And similarly, the Petition demonstrates that using Seo's read operation for verification would have been obvious to a POSITA. Pet., 30. Therefore, a POSITA would have understood that even a brief application of the voltages disclosed by Seo and Nam would remove fast charges.

At bottom, when viewed through the correct legal lens of obviousness (not inherency), the Petition establishes that it would have been obvious to apply the three

voltages of Seo and Nam—voltages that admittedly have sufficient magnitudes to remove fast charges—long enough to successfully remove fast charges during a verification operation.

IV. CONCLUSION

For the foregoing reasons, Micron respectfully requests that the Board reconsider its decision denying review and institute a trial.

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing paper was caused to be served on December 31, 2024 via electronic mail, upon the following counsel of record for Patent Owner:

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