

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC.,  
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,  
Patent Owner

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Case No.: IPR2024-00794  
U.S. Patent No. 10,950,623  
Issue Date: March 16, 2021

Title: 3D NAND MEMORY DEVICE AND METHOD  
OF FORMING THE SAME

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**PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 10,950,623  
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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**LISTING OF EXHIBITS**

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                                                                                                                        |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1001           | U.S. Patent No. 10,950,623 B2 to Song et al.                                                                                                                                                                                                                                                              |
| 1002           | File History of U.S. Patent No. 10,950,623 to Song et al.                                                                                                                                                                                                                                                 |
| 1003           | Declaration of Dr. Jack C. Lee (“Lee”)                                                                                                                                                                                                                                                                    |
| 1004           | U.S. Patent No. 10,559,583 B2 to Park et al. (“Park”)                                                                                                                                                                                                                                                     |
| 1005           | U.S. Patent Publ. No. 2019/0122734 A1 to Shibata et al. (“Shibata”)                                                                                                                                                                                                                                       |
| 1006           | Aritome, “NAND Flash Memory Technologies” (2016)                                                                                                                                                                                                                                                          |
| 1007           | Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017                                                                                                                                                                                                                                           |
| 1008           | U.S. Patent Publ. No. 2015/0162084 A1 to Morooka et al.                                                                                                                                                                                                                                                   |
| 1009           | U.S. Patent Publ. No. 2015/0255478 A1 to Tanzawa                                                                                                                                                                                                                                                          |
| 1010           | U.S. Patent No. 9,589,978 to Yip                                                                                                                                                                                                                                                                          |
| 1011           | U.S. Patent Publ. No. 2017/0062337 A1 to Park et al.                                                                                                                                                                                                                                                      |
| 1012           | Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)                                                                                                                                                                                                                                       |
| 1013           | Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL                                                                                                                                              |
| 1014           | Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at <a href="https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf">https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf</a> |
| 1015           | File History of U.S. Patent No. 11,430,811 (Appl. No. 17/154,054) to Song et al.                                                                                                                                                                                                                          |
| 1016           | U.S. Patent No. 10,355,010 B2 to You et al.                                                                                                                                                                                                                                                               |

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| Exhibit | Description                                                                                                                                                                                                      |
|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1017    | U.S. Patent No. 9,299,718 B2 to Park et al.                                                                                                                                                                      |
| 1018    | U.S. Patent Publ. No. 2019/0035798 A1 to Hwang et al.                                                                                                                                                            |
| 1019    | U.S. Patent Publ. No. 2015/0137216 A1 to Lee et al.                                                                                                                                                              |
| 1020    | <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL, Zoom Civil Minute Order, dated February 22, 2024 (Dkt. No. 42) |
| 1021    | U.S. Patent Pub. 2019/0214404 A1 to Ahn et al.                                                                                                                                                                   |
| 1022    | <i>Curriculum Vitae</i> of Dr. Jack C. Lee                                                                                                                                                                       |
| 1023    | U.S. Patent No. 8,945,996 to Tang et al.                                                                                                                                                                         |

**I. Introduction**

Petitioner requests IPR of claims 1-11 of U.S. Patent 10,950,623 (“the ’623 patent”), assigned to Yangtze Memory Technologies Co., Ltd. (“Patent Owner”).

The ’623 patent relates to 3D NAND memory devices. Typical, prior art 3D NAND devices are formed from alternating layers of conductive and insulating material stacked on a substrate. The conductive layers include a lower “bottom select gate” (or “BSG”), intermediate word lines, and an upper “top select gate” (or “TSG”). Conductive columns pass through the layers to form vertical strings of memory cells. There are many such vertical strings in a 3D NAND device resulting in a three-dimensional array of memory cells. Conductive interconnects to a lower common source can also pass through the layers.

Typical prior art 3D NAND devices arrange the strings of memory cells into “blocks” that can be independently controlled. To allow for this control, each block includes its own BSG and TSG. According to the ’623 patent, as the blocks become larger their operation slows. Thus, the patent attempts to differentiate itself from prior art 3D NAND devices by dividing its memory blocks into “sub-blocks.” It does this by including “dielectric trenches” in at least the BSG layer. This divides the BSG into individually controllable “sub-BSGs” associated with the “sub-blocks.” Similarly, separate trenches optionally can be included in the TSG layer to divide it into “sub-TSGs.”

Claim 1—the '623 patent's only independent claim—requires one set of “dielectric trenches” in the BSG layer. Dependent claim 2 requires another set of “dielectric trenches” in the TSG layer. Dependent claims 3-11 reference a collection of standard 3D NAND features—like memory “channels” or “dummy” structures—and a few other basic “dielectric trench” structural requirements.

There was nothing new about this. This Petition focuses on two exemplary references: (1) U.S. Patent 10,559,583 (Ex. 1004, “Park”), and (2) U.S. Pub. 2019/0122734 A1 (Ex. 1005, “Shibata”). Both Park and Shibata—like the '623 patent—teach 3D NAND devices with blocks of memory divided into smaller sub-blocks. Both references also achieve this in the same way as the '623 patent: their select gate layers are divided into individually controllable portions by trenches of dielectric material.

More particularly, Park explains that its memory blocks can be divided into multiple independently controllable “unit areas.” To do so, Park's BSG—referred to as a “ground select line” or “GSL”—is separated into portions by “isolation insulating layers 111.” Each GSL portion is associated with and controls one of the “unit areas.”

Shibata similarly divides its blocks of memory into independently controllable “string units.” To effectuate this, Shibata employs dielectric “separation portions 62a” to divide its TSG—referred to as a “drain-side select

gate” or SGD—into portions that are associated with and control the “string units.”

In view of this, Park and Shibata render the ’623 patent’s claims unpatentable in multiple different ways.

**Ground 1** details how Park itself renders claims 1-11 obvious. Park employs a “dielectric trench” (isolation insulating layers 111) dividing its “BSG” (GSL) into individually controllable portions associated with memory unit areas. This ground is expressed in terms of obviousness—and not anticipation—because Park uses somewhat different language than the ’623 patent. For instance, it does not refer to its isolation insulating layers 111 as “trenches.” This, however, is exactly what a person having ordinary skill in the art (“POSITA”) would have understood Park’s insulating layer 111 to be: trenches of insulating material that divide Park’s BSG into sub-BSGs. Next, while Park teaches that its “TSG” (a string select line) also is divided into portions corresponding to the unit areas, it does not provide an example where isolation insulating layers 111 do so. Regardless, given Park’s discussion of these layers’ purpose, a POSITA would have considered it obvious to employ them to divide both Park’s BSG and TSG. *See, e.g., Game and Tech. Co. v. Activision Blizzard Inc.*, 926 F.3d 1370, 1381 (Fed. Cir. 2019) (single reference can support obviousness); *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (similar).

**Ground 2** details how Park—when modified by Shibata—also renders the claims obvious. It is possible that Patent Owner may argue that Park’s layers 111 are not the claimed “dielectric trenches” because they only separate Park’s BSG in cooperation with other structure (a collection of common source lines 105). Even if this were pertinent to the claims—it is not—the claims would still be obvious. Shibata explains that the use of narrower dielectric separation portions instead of wider common source lines to divide select gates allows memory devices to be made smaller and denser. It also provides a specific example that uses such a trench to divide a device’s TSG.

**Ground 3** explains how Shibata—modified in view of Park—also renders claims 1-11 obvious. Shibata teaches a memory device that employs a “dielectric trench” (like separation portions 62a) to divide its “TSG” (drain-side select gate) into individually controllable portions associated with memory string units. Shibata’s BSG also can be controlled on a string unit basis. But Shibata accomplishes this in its examples by employing multiple BSG layers. Park teaches that the same type of control can be achieved by dividing a single BSG layer into portions. As explained in this ground, a POSITA would have been motivated to apply this teaching to Shibata because doing so would allow it either to employ fewer layers (resulting in smaller size) or include more word lines (increasing memory density).

## **II. Mandatory Notices**

### **A. Real Party-in-Interest**

Petitioner Micron Technology, Inc. (“MTI”) and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

### **B. Related Matters**

Patent Owner YMTC has asserted the ’623 patent and U.S. Patents 10,658,378, 10,861,872, 10,868,031, 10,937,806, 11,468,957, 11,501,822 and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each of these asserted patents: IPR2024-00788 (’378 patent), IPR2024-00789 (’872 patent), IPR2024-00790 (’031 patent), IPR2024-00791 (’806 patent), IPR2024-00792 (’957 patent), IPR2024-00795 (’822 patent), and IPR2024-00793 (’342 patent).

**C. Counsel, Service, and Fee Information**

Petitioner designates the following counsel:

| <b>Lead Counsel</b>                                                                                                                                                                                                                                     | <b>Back-Up Counsel</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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Petitioner consents to service by electronic mail at the following addresses:

P52PTABDocket@orrick.com, PTABDocketJJL2@orrick.com, PTABDocketJ3B3@orrick.com, and micron-ymtc\_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

### **III. Requirements for IPR**

#### **A. Grounds for Standing**

Petitioner certifies that the '623 patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '623 patent on November 14, 2023. This petition was filed within 1 year of this date.

#### **B. Identification of Challenge and Statement of Precise Relief Requested**

Petitioner requests IPR of claims 1-11. This petition discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and is supported by the accompanying Declaration of Dr. Jack C. Lee (Ex. 1003, "Lee"), a leading expert in the 3D NAND field.

The application underlying the '623 patent—U.S. App. 16/365,725—was filed March 27, 2019 and facially identifies itself as a continuation of a December 7, 2018 PCT filing. Ex. 1001, Cover.

Petitioner relies on the following references: (1) Park (Ex. 1004) and (2) Shibata (Ex. 1005). These references are all prior art. *See* Section VIII.

Petitioner challenges the claims on the following grounds:

**Ground 1:** Claims 1-11 are obvious over Park;

**Ground 2:** Claims 1-11 are obvious over Park in view of Shibata; and

**Ground 3:** Claims 1-11 are obvious over Shibata in view of Park.

**IV. Institution Should Be Granted**

Petitioner has established a reasonable likelihood of success on the merits.

All other requirements for IPR have been met. The Board should institute IPR.

**A. There Are No Grounds for a § 314 Discretionary Denial in this Case**

There is a pending district court action involving the '623 patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '623 patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“*Fintiv*”). In particular: the district court may stay the case, any potential trial will occur years from now, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

**1. Possibility of a Stay**

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 12 (similar).

**2. Proximity of the Court’s Trial Date**

On February 22, 2024, the district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1020. If IPR is instituted, it should be completed before this date. *See also* Ex. 1014 (indicating an average of 48.9 months to trial). This weighs strongly in favor of institution.

**3. Investment in the Parallel Proceeding**

To date, the parties and Court have invested very little in the parallel proceeding. Beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are months away from the exchange of infringement and invalidity contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where “the

petitioner filed the petition expeditiously....” *Fintiv* at 11. Here, Patent Owner asserted eight different patents against Petitioner. *See* Ex. 1013. Yet, Petitioner proceeded with diligence filing a mere five months after being served with the original complaint and a little over two months after the filing of an amended complaint. *See id.* This also weighs strongly in favor of institution.

#### **4. Issue Overlap**

Given the early stage of the parallel proceeding, it is not yet possible to determine the amount of overlap. Patent Owner has not yet served infringement contentions or identified the asserted claims. Moreover, should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

#### **5. Party Overlap**

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

#### **6. Other Circumstances**

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not

previously consider. Thus, this factor also weighs in favor of institution.

**B. Denial Under § 325(d) Would Be Inappropriate**

Neither Park nor Shibata was cited by Patent Owner or considered by the Examiner during prosecution of the '623 patent. *See generally* Ex. 1002. Indeed, as explained in Section V.C, the Examiner did not specifically address or assess any prior art references or issue any prior art-based rejections in connection with the '623 patent. While the Examiner later used Shibata to reject the claims in an application claiming priority to the '623 patent, this did not occur until almost a year after the '623 patent had already issued. *See* Ex. 1015, 123-132. Moreover, the Examiner did not consider the features of Shibata that are the focus of this petition: separation portions 62a and interconnects LI in slits 60. *See id.* The Examiner's rejection of the claims over Shibata also forced applicant to amend the claims to include further limitations that are not part of the '623 patent's claims. *See id.*, 141-147. Thus, the later consideration of Shibata has no bearing on whether institution is appropriate here. Moreover, while other, different references naming an inventor with the last name "Park" were cited in certain applications related to the '623 patent, the Park reference discussed in this petition was not.

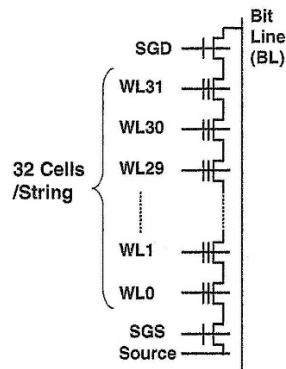
**V. The '623 Patent**

**A. Technological Background**

The '623 patent and the prior art discussed in this petition relate to NAND flash memory. "Flash memory" is a form of "non-volatile memory." Ex. 1010,

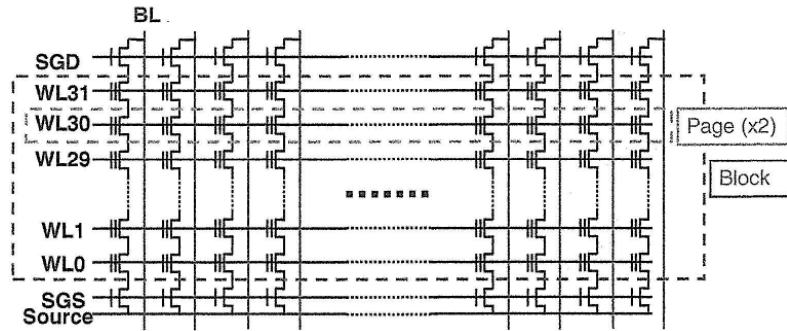
1:24-26. “Non-volatile memory ... can retain its data values ... without the application of power.” *Id.*, 1:26-28. NAND flash stores data in a “cell” formed from a transistor. Ex. 1006, 38-39; Ex. 1012, 109; Lee, ¶¶ 39-46.

NAND cells are arranged in “strings” with multiple cells “connected in series.” Ex. 1006, 38. The cells are surrounded by “select transistors (SGD, SGS).” *Id.* The “SGD connects” at the string’s drain side “to isolate it from the bit line (BL),” and the “SGS connects” at the string’s source side “to isolate it from a source line (SL).” *Id.* Word lines connect to each memory cell’s control gate. *Id.*, 38-39. One such string is shown below:

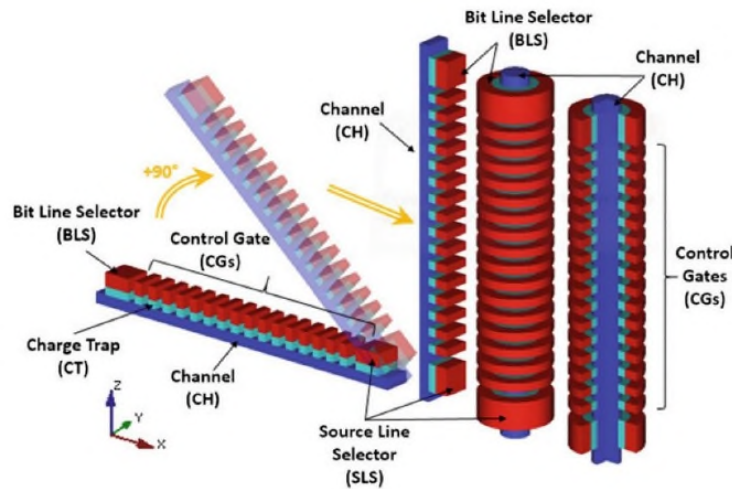


*Id.*, 39.

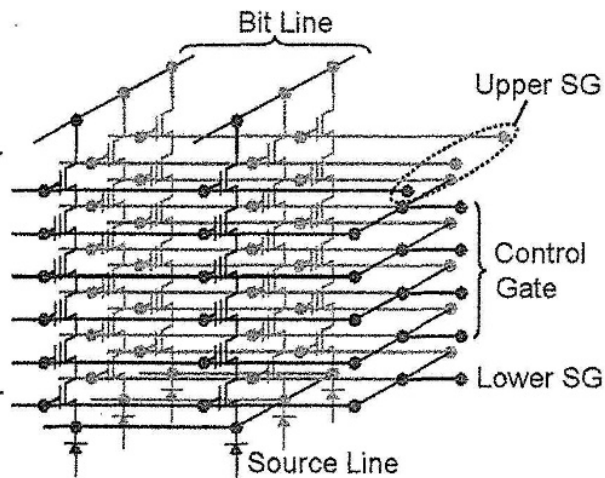
Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. Ex. 1006, 38.



*Id.*, 40. The cells are grouped into “page[s]” extending along the word lines and “block[s].” *Id.* “[R]ead and program operations are performed per page” while “the erase operation is performed per block.” *Id.*, 39. “[T]o further scale down the memory cell size,” 3D NAND was developed in 2006. *Id.*, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1007, 3.

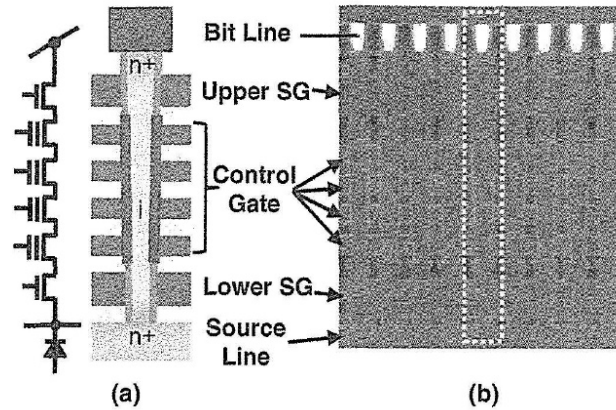


Ex. 1012, 122. Multiple such vertical channels are then repeated in a three-dimensional array:

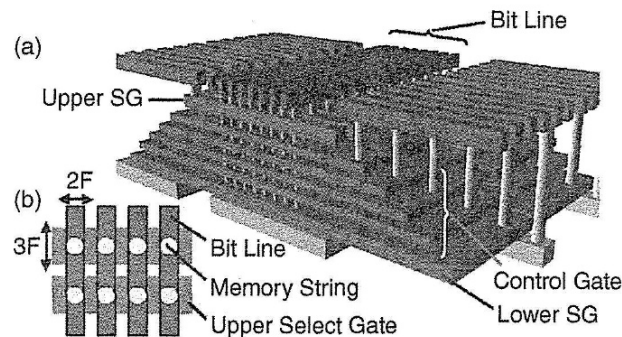


Ex. 1006, 296; Lee, ¶¶ 47-57.

3D NAND includes “multi-stacked layers of gate (plate)” material alternated with “dielectric” in a “[s]tack.” Ex. 1006, 294. A “through-hole” channel “filled by memory film ... and channel poly-Si” passes through the layers to form the string of vertically arranged memory cells. *Id.*, 295. “Each” layer of “electrode plate acts as a control gate.” *Id.* A particular vertical memory cell “string is selected by a bit line and an upper select gate (upper SG).” *Id.*, 296. A memory cell “is located in the intersection of a control gate plate” and the memory film/poly-Si channel. *Id.* The lowest layer is a “select gate (lower SG)” allowing the strings to connect to a lower “common source.” *Id.*, 295, 297. An example 3D NAND vertical memory cell string follows:



*Id.*, 296. In some 3D NAND, “[t]he control gates and lower SG are commonly connected in each layer in [a] block.” *Id.*, 295. “[T]he control gates and upper/lower SG are connected” to the memory’s “metal layers at [a] stair-like gate structure” located outside the memory array. *Id.*, 295, 297.



*Id.* at 296; Lee, ¶¶ 58-64 .

## B. Overview

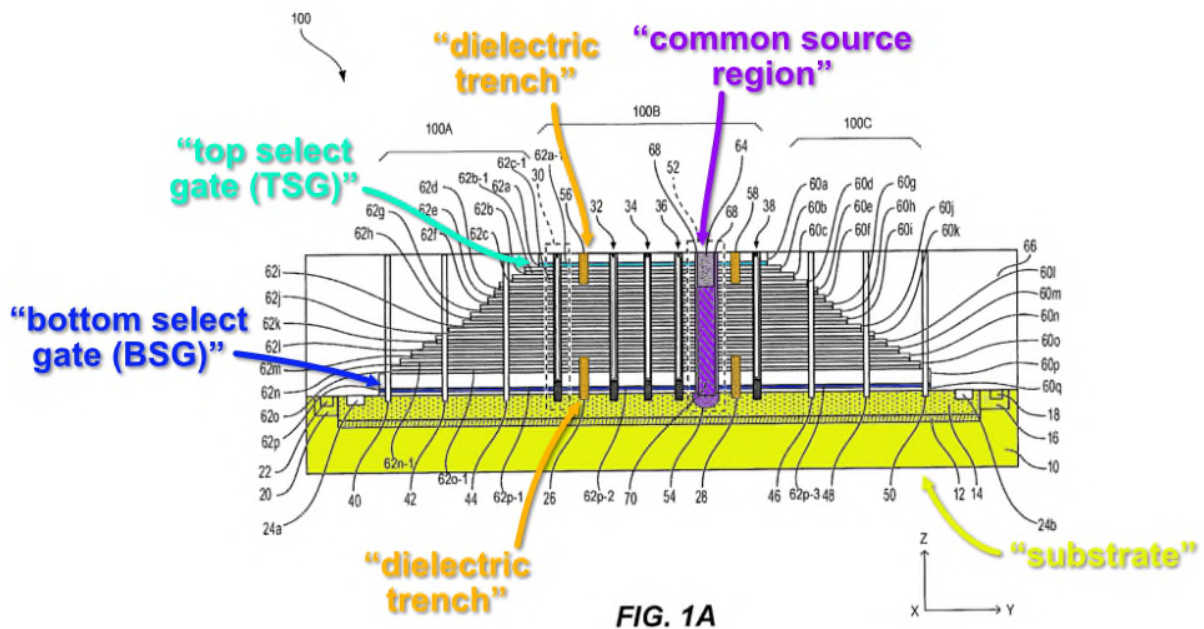
The '623 patent relates to a “3D NAND memory device.” Ex. 1001, 1:33-36. According to the patent, in existing devices, “memory cell strings of the same block can share a bottom select gate (BSG).” *Id.*, 1:51-52. “The shared BSG accordingly controls” all the “bottom select transistors (BSTs)” “of the vertical

NAND memory cell strings in that block simultaneously during” operation. *Id.*, 1:40-41, 1:53-58. This is a problem, according to the patent, because “the shared BSG can induce longer erasing time, longer data transfer time, and lower storage efficiency.” *Id.*, 1:58-60.

The patent purports to address this by employing a “divided block structure.” *Id.*, 1:33-36. “[E]ach of the blocks can be separated into a plurality of sub-blocks by dividing the shared BSG into a plurality of sub-BSGs” using “one or more first dielectric trenches.” *Id.*, 1:61-64. This in turn allows the “sub-blocks” to be “operated individually through controlling the respective sub-BSG.” *Id.*, 1:64-67. The patent similarly explains that “a shared/common TSG” can also be “divid[ed]” by “second dielectric trenches” into “sub-TSGs” that can also be independently controlled. *Id.*, 2:8-13.

Figure 1A provides an example. Here, the depicted “memory device 100”—like all 3D NAND devices—includes a BSG 62p (dark blue), a TSG 62a (light blue), and multiple “word lines” separated by “insulating layers” stacked over a “substrate 10.” *Id.*, 6:44-54. Electrical connection to these layers is made via the same type of “staircase region[.]” present in prior art 3D NAND. *Id.*, 8:44-60; Fig. 2. A “common source region 52” (purple) passes through all the layers and “is electrically coupled with the substrate 10...” *Id.*, 7:59-67. The memory strings are formed around “channel structures” 30/32/34/36/38. *Id.*, 8:23-26. As shown,

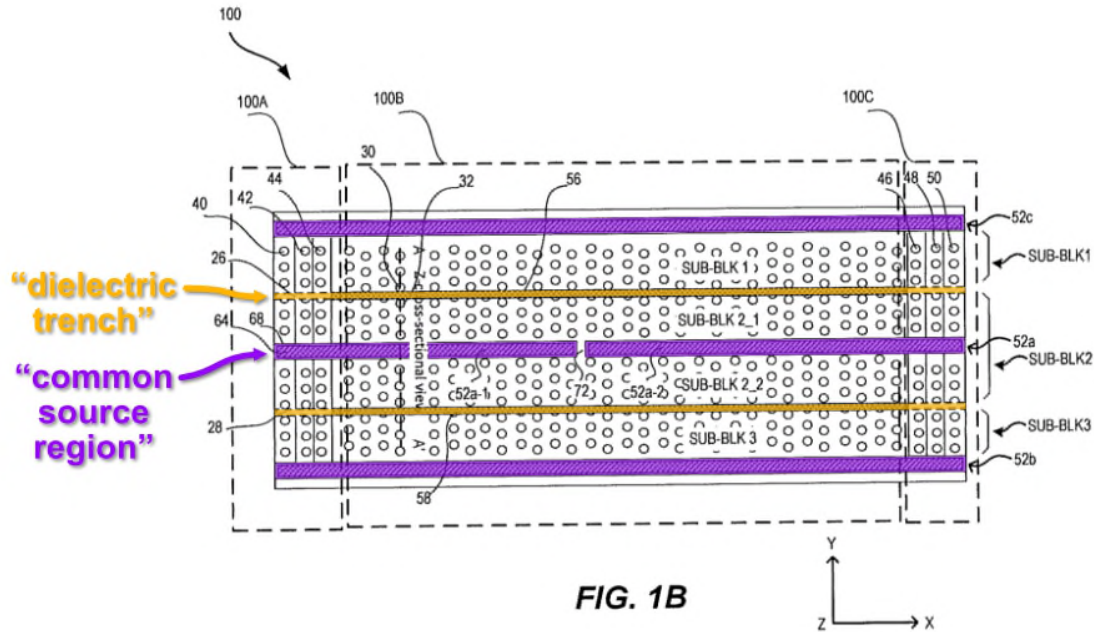
“first dielectric trenches” 26 and 28 (orange) are formed in the lower BSG, while “second trenches” 56 and 58 (also orange) are formed in the upper TSG. *Id.*, 7:17-35. The trenches divide the BSG and TSG into “sub-BSGs” and “sub-TSGs” associated with memory “sub-blocks” that “can be operated individually[.]” *Id.*, 7:45-53.



*Id.*, Fig. 1A.<sup>1</sup>

Figure 1B provides a top view. Trenches 26/56 and 28/58 (orange) run parallel to common source regions 52a-c (purple) along the “X-direction ... of the substrate.” *Id.*, 7:20-62.

<sup>1</sup> Petitioner has added all color to the figures.



*Id.*, Fig. 1B.

### C. Prosecution History

The '623 patent's claims were not rejected over the prior art during prosecution. *See generally* Ex. 1002. When allowing the claims, the Examiner did not discuss any prior art. *See id.*, 611-613.

## VI. Claim Construction

The Board applies the same *Phillips* claim construction standard used by district courts. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). For purposes of this petition, Petitioner submits that the terms of the '623 patent's claims do not require further construction and can be afforded their plain and ordinary meaning. *See Lee*, ¶¶ 88-91.

## **VII. Level of Ordinary Skill in the Art**

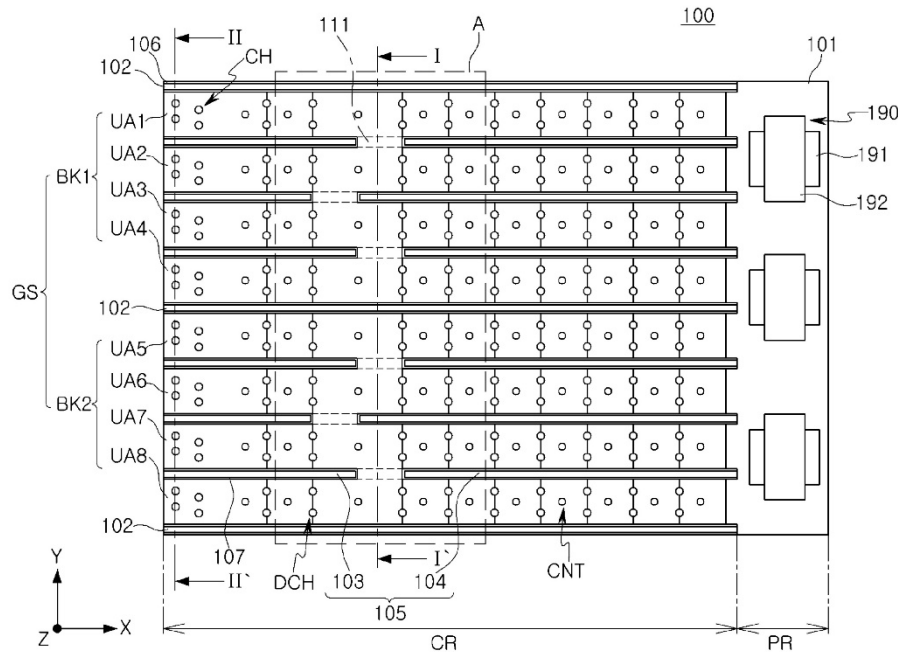
A POSITA in the field of the '623 patent would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may substitute for professional experience). Lee, ¶¶ 36-37. This POSITA would also have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled. *Id.*

## **VIII. Prior Art Overview**

### **A. Park**

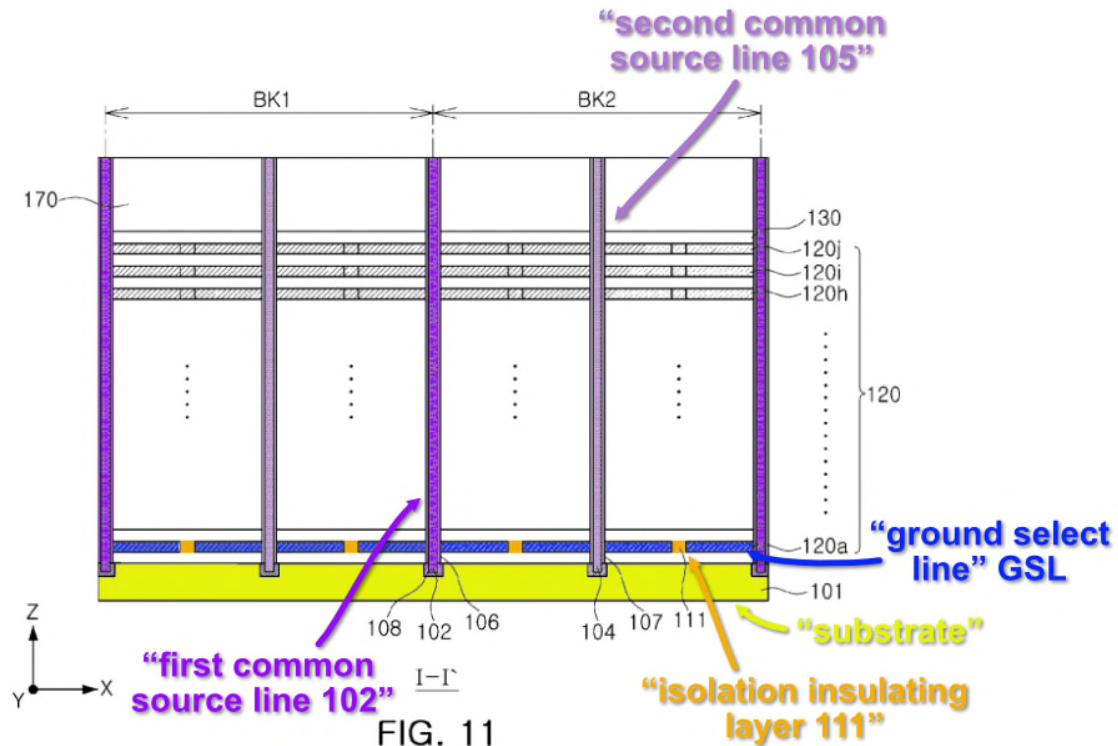
Park was filed January 25, 2017. Park, Cover. It is prior art under AIA § 102(a)(2).

Park teaches a "3D-NAND memory device." Park, 1:37-46. This device includes the standard 3D NAND layers: a lower "ground select line" GSL, an intermediate "plurality of word lines" WL, and an upper "string select line" SSL. *Id.*, 1:63-2:1. Multiple "common source line[s] 102" pass through these layers. *Id.*, 7:40-43. Electrical connection to the layers is made via "a stepped structure." *Id.*, 6:56-60. The device's memory cells are formed along "a plurality of channel structures extending vertically through" the GSL, WL, and SSL layers. *Id.*, 1:49-52. Like the '623 patent, Park sub-divides its memory "blocks" into smaller "unit

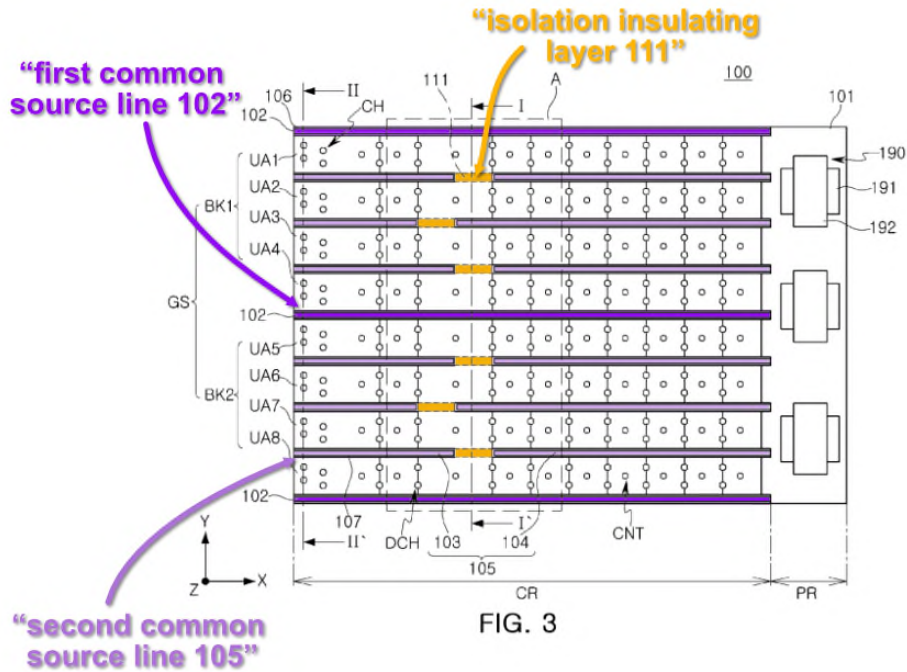


*Id.*, Fig. 3.

view along line I-I' in Figure 3. *Id.*, 2:60-61. Four “isolation insulating layers 111” are shown. Other such layers are located behind portions 104 of the “second common source lines 105”:



*Id.*, Fig. 11. The “common source lines 102” and “105” (both purple) and these “isolation insulating layers 111” (orange) extend in the same “first direction, e.g., the X-axis direction” of the device. *Id.*, 10:46-49.



*Id.*, Fig. 3.

## B. Shibata

Shibata was filed in the US on July 30, 2018 and claims priority to an October 23, 2017 foreign filing. *See* Shibata, Cover. It is prior art under AIA § 102(a)(2).

Shibata relates to a “memory device” with a “three-dimensional structure.” Shibata, [0003]. The device includes “multiple ... conductive layers stacked with ... insulator interposed...” *Id.* The layers include lower “source-side select gate” layers SGS, intermediate “word lines” WL, and an upper “drain-side select gate layer” SGD. *Id.*, [0003], [0048], [0074], [0166]. A conductive “interconnect portion LI ... is provided in [a] separation portion 60 (a slit ST)” passing through all the layers. *Id.*, [0065].

Shibata also divides its memory “block[s]” into smaller “string unit[s].” Shibata, [0162]-[0163]. In Figure 16 below, the memory block includes “two sub-blocks 200a and 200b subdivided by three separation portions 60 (slits ST)....” *Id.*, [0162]. One such slit is annotated in Figure 16; the other two are not shown and would be located at the figure bounds. *See id.* Sub-block 200a and 200b are divided into “string unit[s]” SU0-SU1 and SU2-SU3. The select gate portions in each string unit can be “controlled electrically independently.” *Id.*, [0083]. To allow for this, “separation portion[s] 62a” (orange) are formed from slits filled with “insulating films” in its drain-side select gate (light blue) to divide that gate into four “independently” controllable pieces SGD0-SGD3. *Id.*, [0088]-[0090], [0166]-[0167].

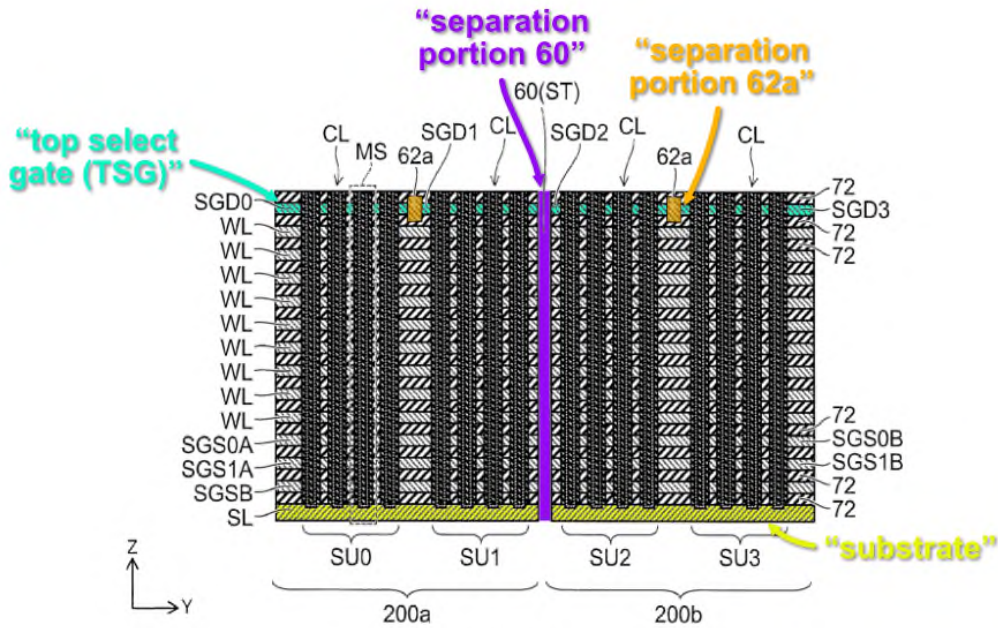


FIG. 16

*Id.*, Fig. 16. As shown in a top-down view below, these “separation portions” (orange) “extend in the same direction as the separation portion 60 (the slit ST)” (purple). *Id.*, [0088].

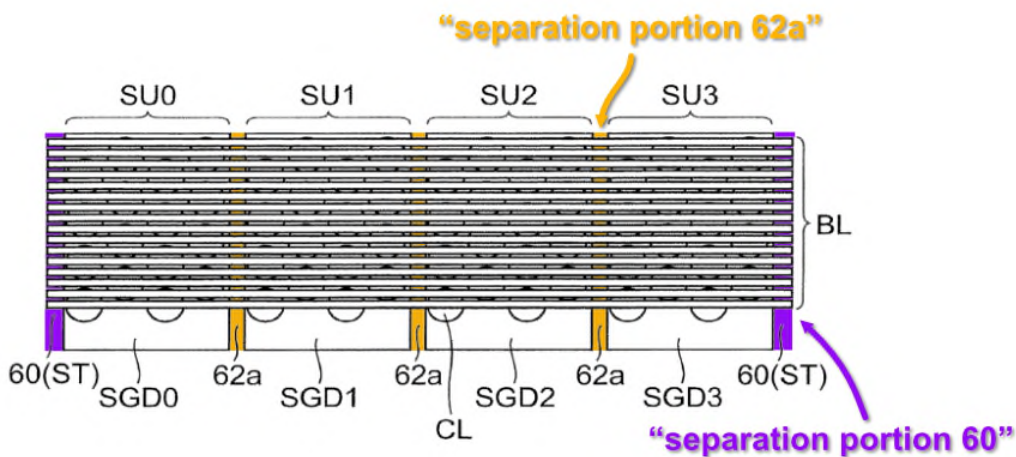


FIG. 47A

*Id.*, Fig. 47A. This is the case in all of Shibata’s embodiments. *See id.*, Figs. 7A-7B, 14A-14B.

## IX. The '623 Patent's Claims Are Obvious

**A. *Ground 1: Claims 1-11 Are Obvious Over Park***

Park, when considered in view of the knowledge of a POSITA, renders claims 1-11 obvious.

### 1. Claim 1

**[1.Pre] “A memory device, comprising:”**

To the extent limiting, Park teaches a “3D memory device.” Park, 1:14-17; 1:31-32; 3:24-27; Lee, ¶¶ 122-123.

**[1.A] “a substrate;”**

Park includes the claimed “**substrate**”: its “memory device 100 ... include[s]” a “substrate 101.” Park, 10:34-35; *id.*, 1:31-32. This substrate is annotated yellow below:

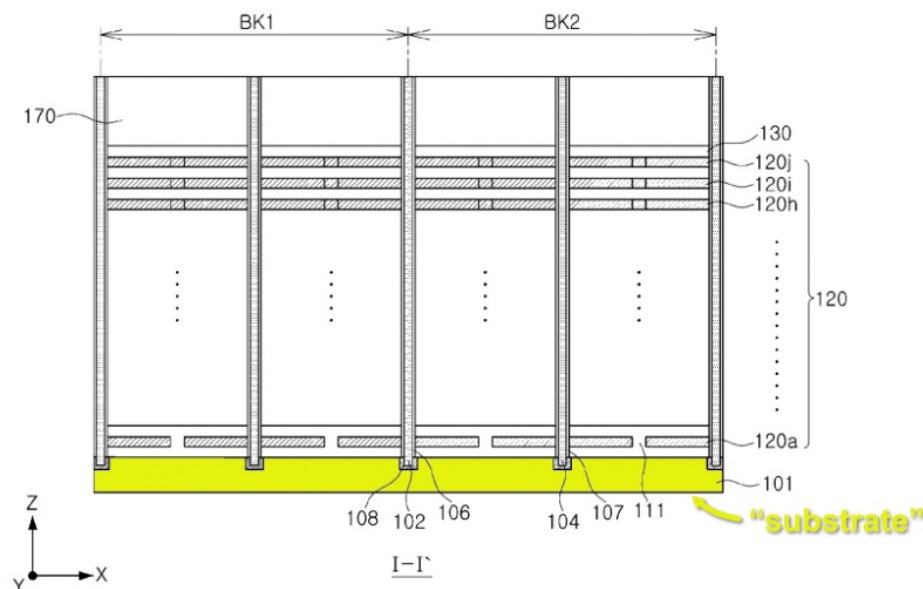


FIG. 11

*Id.*, Fig. 11; Lee, ¶¶ 124-126.

**[1.B] “a bottom select gate (BSG) disposed over the substrate;”**

Park’s “memory cell array” is formed from a “plurality of memory cell strings S.” Park, 4:17-18. “[E]ach” string “include[s]” a lower “ground select transistor GST,” “memory cells MC1 to MCn[,]” and an upper “string select transistor SST” “connected ... in series[.]” *Id.*, 4:18-28. The GST gates are “connected to a ground select line GSL.” *Id.*, 4:29-30. Each GST operates to connect an associated memory cell string to “common source line CSL.” *Id.*, 4:30-32. Thus, while Park employs a different acronym than the ’623 patent, it nonetheless teaches the claimed “*bottom select gate (BSG)*”: its GSL controls connection of the memory cell strings to a common source line. *Id.*, 4:18-32; Ex. 1001, 1:37-46 (similarly discussing BSG operation). The GLS is annotated blue in Figure 2 below:

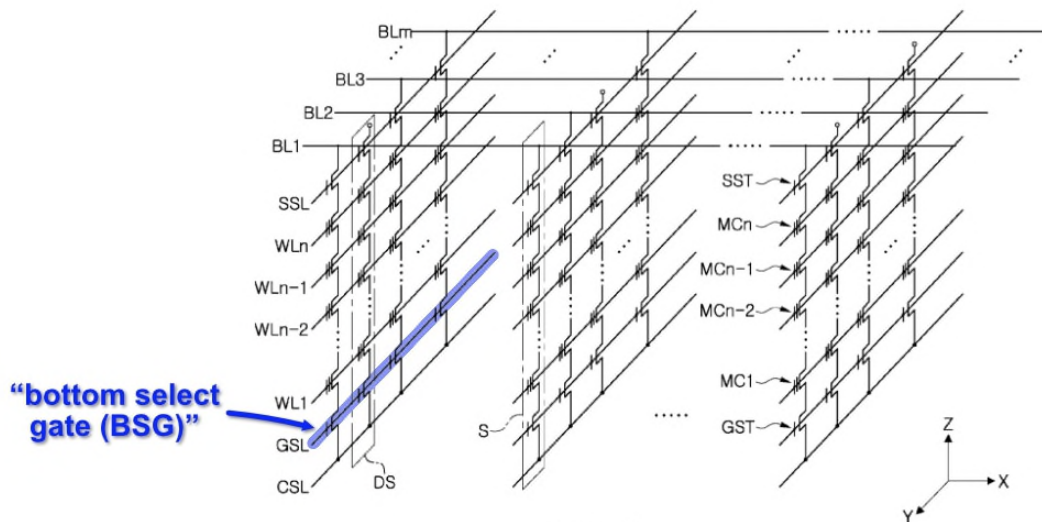


FIG. 2

Park, Fig. 2; Lee, ¶¶ 127-132.

Park also details where its GSL is located with respect to its substrate. Park's device is formed from multiple "gate electrode layers 120" separated by "interlayer insulating layer[s] 170" and "stacked on" "substrate 101." Park, 10:35-41. The lowest of these—closest to the substrate—is the GSL. *Id.*, 10:55-56. Thus, Park's "*bottom select gate*" (its GSL, blue below) is "*disposed over the substrate*" (yellow):

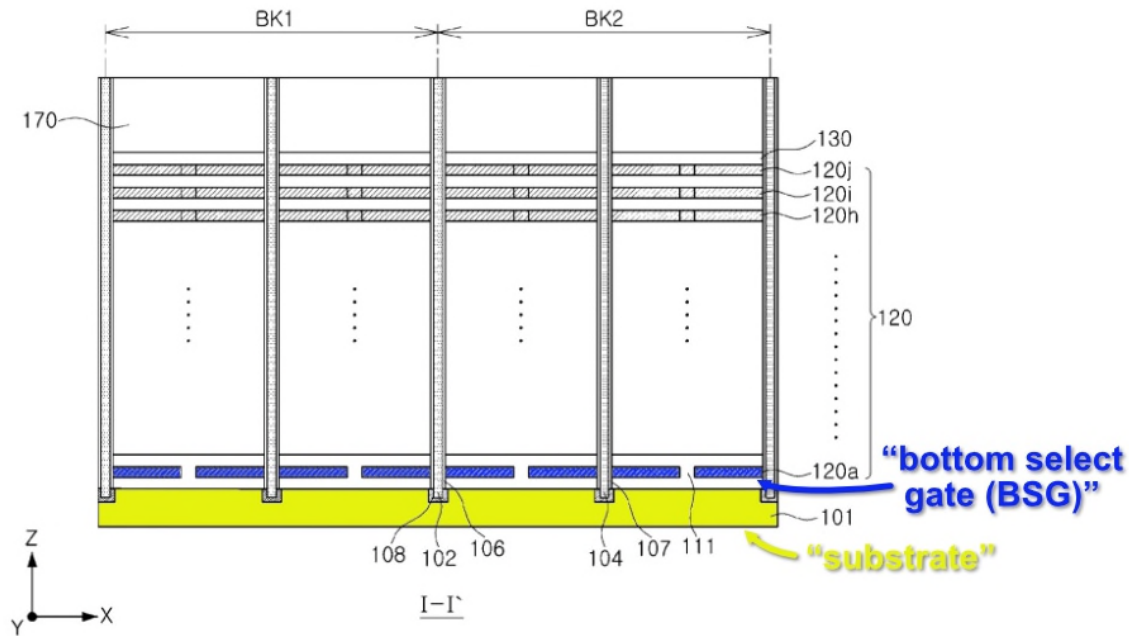


FIG. 11

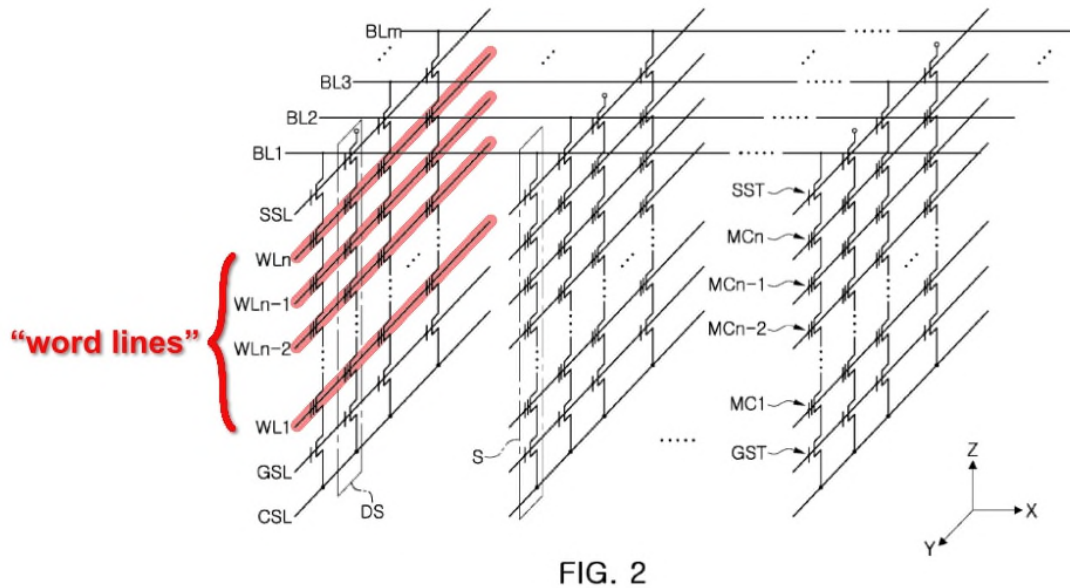
*Id.*, Fig. 11; Lee, ¶¶ 133-137.

**[1.C] “a plurality of word lines positioned over the BSG with a staircase configuration;”**

Park's memory device includes "*a plurality of word lines.*" Park's "memory cell array 2" includes "a plurality of memory cells arranged in a plurality of rows and a plurality of columns." Park, 3:28-30. Each row of "memory cell[s]"

is connected to a “single word line WL.” *Id.*, 3:28-36; 1:62-2:8; 3:39-44; 4:22-24.

These word lines are shown in Figure 2:



*Id.*, Fig. 2; Lee, ¶¶ 138-143.

Park’s word lines are also “*positioned over the BSG.*” Figure 4 provides an example: Park’s “*word lines*” (word lines 120*b-i*, red) are all “sequentially stacked” over the substrate and Park’s “*BSG*” (ground select line 120*a*, blue). Park, 6:65-7:2.

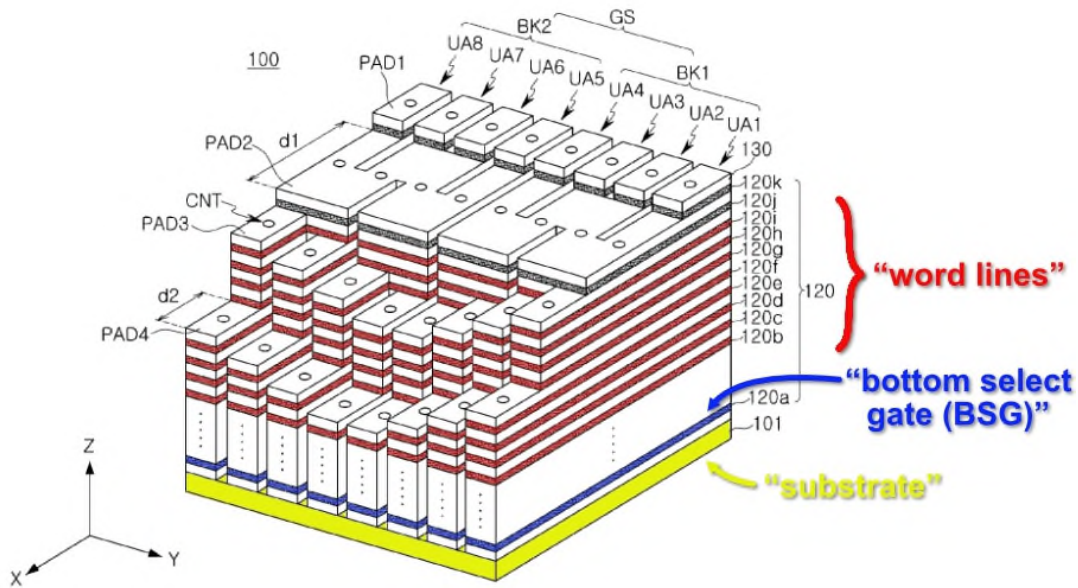


FIG. 4

*Id.*, Fig. 4; Lee, ¶¶ 144-147.

Park’s word lines also have “*a staircase configuration*”: Park’s various “gate electrode layers ... may extend by different lengths” such that they have “a stepped structure.” Park, 6:56-60; 7:8-11; 8:18-50; 11:62-65; Figs. 15, 25, 32; Lee, ¶¶ 148-150.

[1.D] “a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;”

Park includes the claimed “*plurality of insulating layers*”: “insulating layers” “electrically separate” Park’s gate electrode layers “from each other.” Park, 5:17-23; 6:49-52; 10:35-37; 10:40-45.

Next, Park’s “*insulating layers*” are located everywhere this limitation requires. As shown in Figure 11, there are insulation layers 130 (green) between “*the substrate*” (substrate 101, yellow) and “*the BSG*” (ground select line 120a,

blue), *“the BSG”* and *“the plurality of word lines”* (word lines 120b-120i, red), and the *“word lines”* themselves:

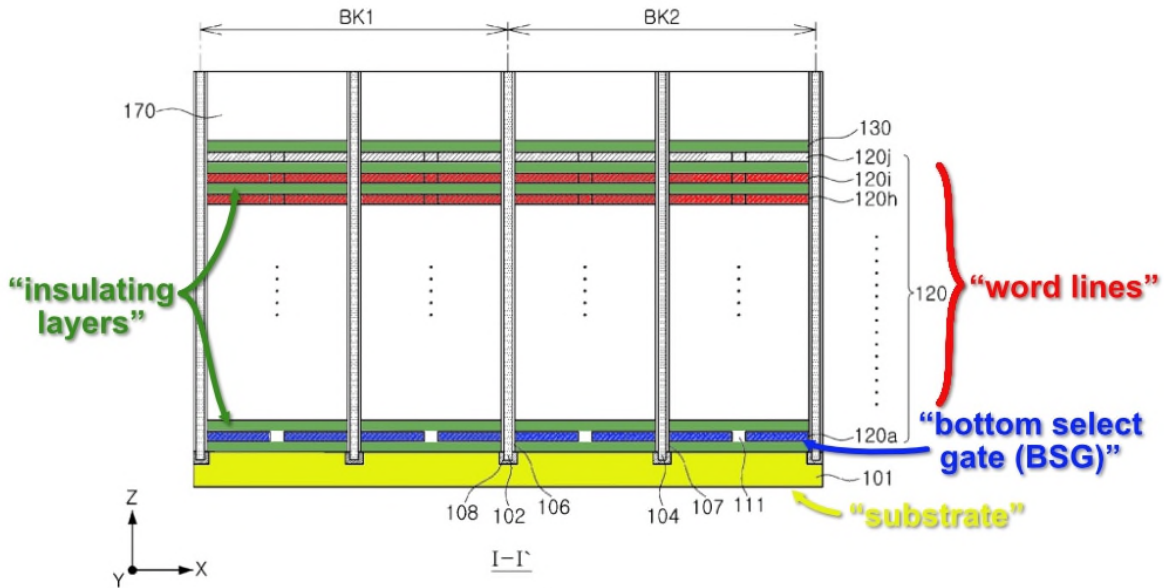


FIG. 11

Park, Fig. 11; Lee, ¶¶ 151-160.

[1.E] **“one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and”**

A POSITA would have understood Park’s *“BSG”* (its GSL) to be *“separate[d] ... into a plurality of sub-BSGs”* (GSL portions specific to unit areas UA1-UA8) by *“one or more first dielectric trenches”* (isolation insulating layers 111).

Park’s “memory device 100” can be “divided into a plurality of blocks BK1 and BK2.” Park, 4:61-5:8. These blocks are further sub-divided into “unit areas.” *Id.* In Figure 3, blocks BK1-BK2 are divided into unit area UA1-UA8. *Id.*, 5:8-10.

The “word lines” in each block are electrically connected and continuous across the unit areas.<sup>2</sup> *Id.*, 5:54-60; 7:44-50. But “[i]n order to independently control the memory cell devices” on a unit area basis, the SSL and GSL “may be separated from each other between ... unit areas UA1 to UA8.” *Id.*, 5:67-6:4. Per Park, different “portions of the ground select line” are “separated” at the unit area “boundaries” “by ... first common source lines 102, the second common source lines 105, and isolation insulating layers 111.” *Id.*, 6:8-12; 10:55-56.

Figure 3 provides an example top-down view. Isolation insulating layers 111 (orange) are located between common source lines 102, and extend lengthwise in the X-axis direction to close the gaps in common source lines 105 and separate the GSL in blocks BK1 and BK2 into unit areas UA1-UA8:

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<sup>2</sup> This is because the isolation insulating layers only separate the GSL and not the word lines above. Lee, ¶¶ 164-165.

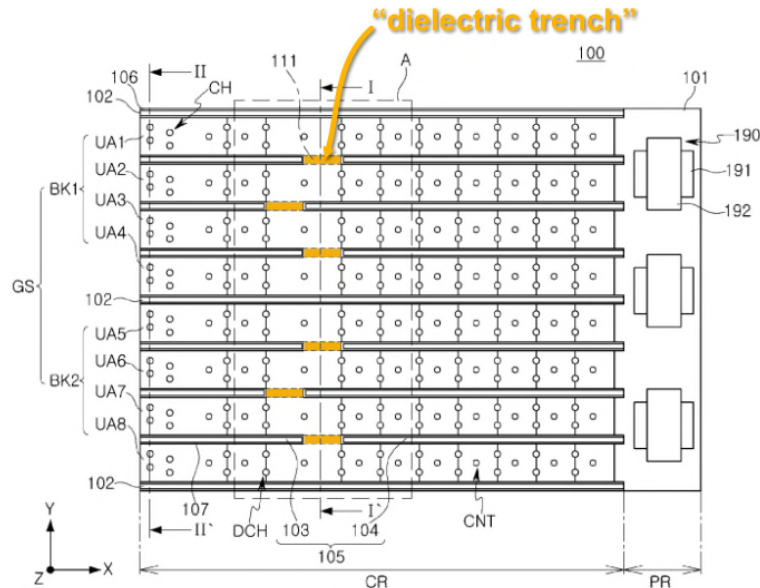


FIG. 3

Park, Fig. 3. Figure 11 provides a cross-sectional view along line I-I' from Figure 3. Isolation insulating layers 111 (orange) are located within and divide GSL layer 120a (blue) into portions corresponding to unit areas UA1-UA8:

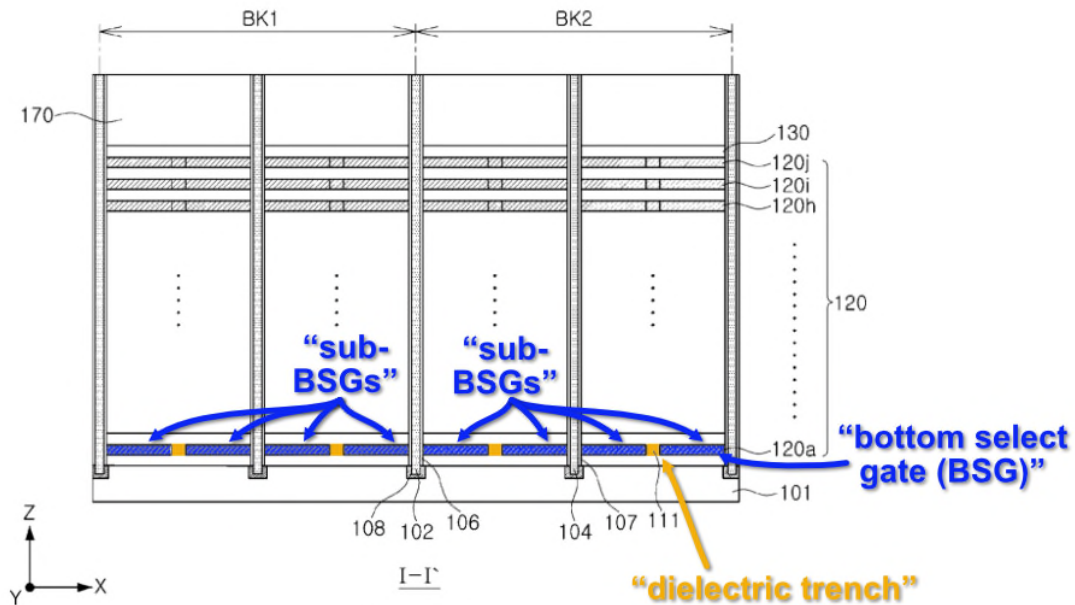


FIG. 11

*Id.*, Fig. 11. The isolation insulating layers are made from dielectric material like a

silicon oxide. *See id.*, 15:45-49, 12:59-64.

This is exactly what this claim limitation requires. Park includes ***“one or more first dielectric trenches formed in the BSG”*** (isolation insulating layers 111 formed within its GSL). These ***“dielectric trenches”*** ***“extend[] in a length direction of the substrate”*** (layers 111 extend lengthwise in the X-axis direction). Further, the ***“dielectric trenches”*** ***“separate the BSG into a plurality of sub-BSGs”*** (layers 111 cause Park’s GSL to be divided into portions corresponding to unit areas UA1-UA8). *See Lee*, ¶¶ 161-171.

While Park does not call its isolation insulating layer 111 a ***“trench,”*** a POSITA would nonetheless have understood that this is what it teaches. To form the layers 111, “opening regions OP” are “formed in the first sacrificial layer SL1” to “expose[]” the underlying “[p]ortions of the first insulating layer IL1.” Park, 12:65-13:1. This is shown in Figure 20 (top view) and 21 (cross-sectional view):

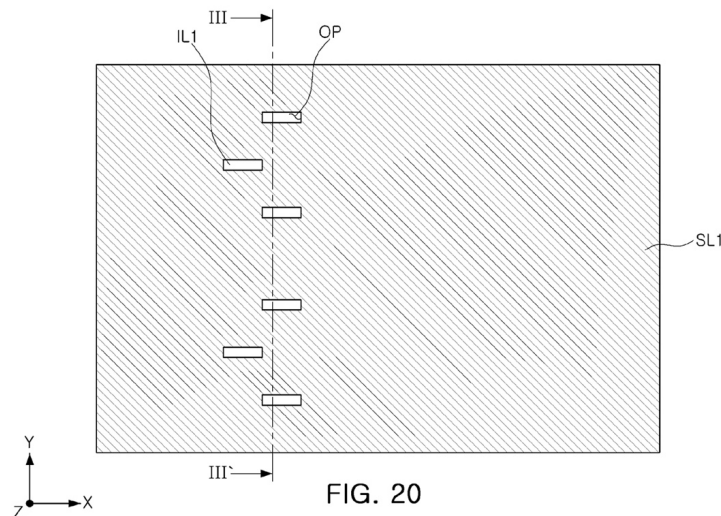
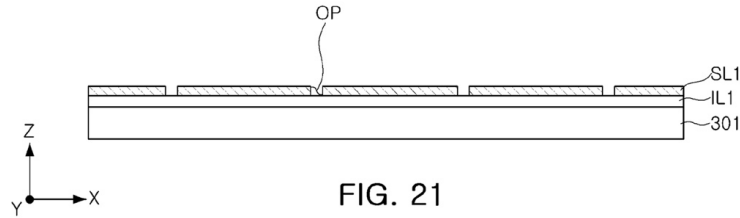


FIG. 20



*Id.*, Figs. 20-21. Opening OP is structured as a trench extending in Figure 20’s X-axis direction. *See id.* This opening is then “filled with an insulating material” forming “isolation regions[.]” *Id.*, 13:15-17. Thus, the isolation insulating layers are insulation filled trenches proceeding through one of Park’s conductive layers. *See id.*, 12:65-13:1; 13:15-17; Figs. 11, 20-21. Subsequently, the GSL is formed and these trenches remain in place, resulting in the GSL (the claimed “**bottom select gate**”) having insulation trenches formed within it. *See id.*, 15:35-43, 16:3-37.

The ’623 patent employs an analogous process to form its “dielectric trenches”: the patent’s trenches “can be formed by” forming “trench openings” through the desired layers and then “fill[ing]” these “trench openings” with “dielectric material.” Ex. 1001, 16:1-18; 17:43-55. Moreover, “[i]n some embodiments (i.e., Gate-last Formation Technology),” the BSG, word lines, and other layers can be “formed firstly using sacrificial layers” that are only replaced with conductive material after all other processing steps—including the trench formation—are completed. *Id.*, 7:1-16; 15:45-46 (noting that trench openings through a “BSG” are formed can be “sacrificial layers”); Lee, ¶¶ 172-176.

While there are some minor structural differences between Park's isolation insulating layer 111 and the example "dielectric trenches" shown in certain of the '623 patent's figures, this does not distinguish Park from the claims.

For instance, in Figures 1A and 1B of the '623 patent, dielectric trench 26 traverses nearly the entire length of depicted memory device 100. *See* Ex. 1001, Figs. 1A-1B. In Park, isolation insulating layer 111 does not extend across the full length of the memory device. Instead, it cooperates with common source lines 105 to divide Park's GSL into portions. *See, e.g.,* Park, 6:8-12; Fig. 3. Claim 1 requires only that the "dielectric trenches ... separate the BSG into a plurality of sub-BSGs." Nothing about the claim requires that the "dielectric trenches" perform this "separat[ion]" function completely by themselves without the help of any other structure. In fact, such an interpretation would be inconsistent with the '623 patent: common source regions 52c and 52b are located at the sub-block boundaries and thus also play a role in separating the memory into blocks and sub-blocks. *See* Ex. 1001, Fig. 1B; 9:3-8 ("common source regions 52b and 52c" are "disposed at two boundaries of the memory device 100" and "isolate" the memory device from surrounding structure). Moreover, the '623 patent repeatedly explains that its figures are "merely examples and are not intended to be limiting." *Id.*, 5:13-16; 5:33-36; 23:41-46. While not identical to trenches in the '623 patent's figures, Park's isolation insulating layers 111 do exactly what the claim requires: if

these layers were not present, the portions of Park's GSL in unit areas UA1-UA4 (or UA5-UA8) would be electrically connected to each other through the gaps in common source lines 105. *See* Lee, ¶¶ 177-182. The layers 111 function to divide the GSL into electrically separated (and independently controllable) portions. *See id.*, ¶ 182. If, however, it is for some reason determined that the claimed "dielectric trenches" must themselves "separate" the "BSG" into "sub-BSG" completely on their own, the claims would still be obvious over the combination of Park and Shibata as discussed in Ground 2.

Next, Figure 1A of the '623 patent also depicts dielectric trench 26 extending through multiple conductive layers (62n, 62o, and 62p), the intervening insulation, and into substrate 10. *See* Ex. 1001, Fig. 1A. Claim 1, however, requires only that the "dielectric trenches" be "formed in the BSG." *Id.*, claim 1. Neither the claim nor the specification requires that the "dielectric trench" enter the substrate. *See, e.g., id.*, Fig. 8A (trenches 26/28 do not extend into substrate 10); Lee, ¶¶ 184-187.

In sum, Park's isolation insulating trenches 111 perform the same function in the same way as the '623 patent's dielectric trenches. They are located within Park's "BSG." *E.g.*, Park, 10:55-56. And they divide that BSG layer into separate "sub-BSG" allowing for memory control on a sub-block basis. *E.g., id.*, 5:67-6:4; Lee, ¶ 187.

[1.F] “one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.”

Park teaches “*common source regions*.” Park’s memory device includes multiple “common source line[s] 102.” Park, 7:40-43. These lines “extend[] in the first direction, e.g., the X-axis direction” to “divide[]” the memory device into “first and second blocks BK1 and BK2....” *Id.*, 10:46-50; *see also* 1:53-54; 1:63-2:3. As shown in Figure 3, Park’s “*common source regions*” (common source lines 102, purple) “extend[]” in the same “*length direction of the substrate*” (the X-axis direction) as Park’s “*dielectric trenches*” (the isolation insulating layers 111, orange):

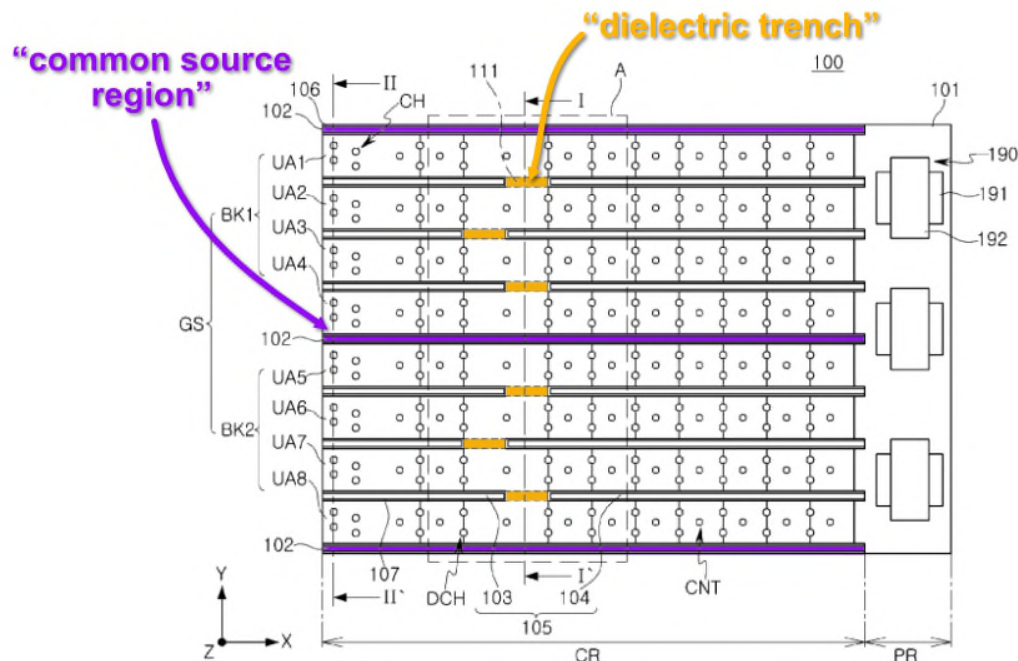


FIG. 3

*Id.*, Fig. 3.

Park's "common source lines 102" also pass through and "divide[]" its various "gate electrode layers 120 and the interlayer insulating layer[s] 170" to connect to the substrate Park, 10:46-11:6. Thus, Park's "*common source region*" (common source line 102, purple) "*extend[s] through the BSG*" (GSL 120a, blue), "*the plurality of word lines*" (word lines 120b-120i, red), and "*the plurality of insulating layers*" (green):

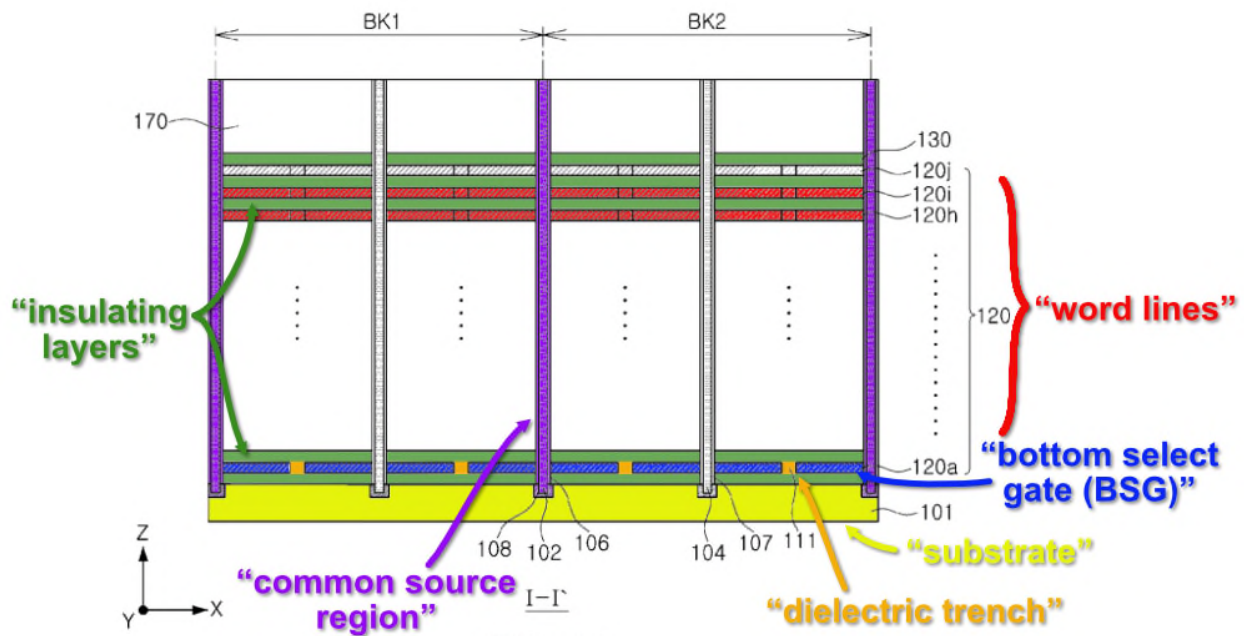


FIG. 11

*Id.*, Fig. 11; Lee, ¶¶ 188-194.

## 2. Claim 2

Claim 2 depends on claim 1 and further requires:

**[2.A] “a top select gate (TSG) positioned over the plurality of word lines, the TSG and the plurality of word lines being spaced apart by the plurality of insulating layers; and”**

The “stack of gate electrode layers” forming Park’s memory device includes an upper “string select line” SSL. Park, 1:63-2:1; *id.*, 7:20-29. This SSL (light blue below) allows each memory cell string to be “connected to ... a bit line BL.” *Id.*, 3:30-34.

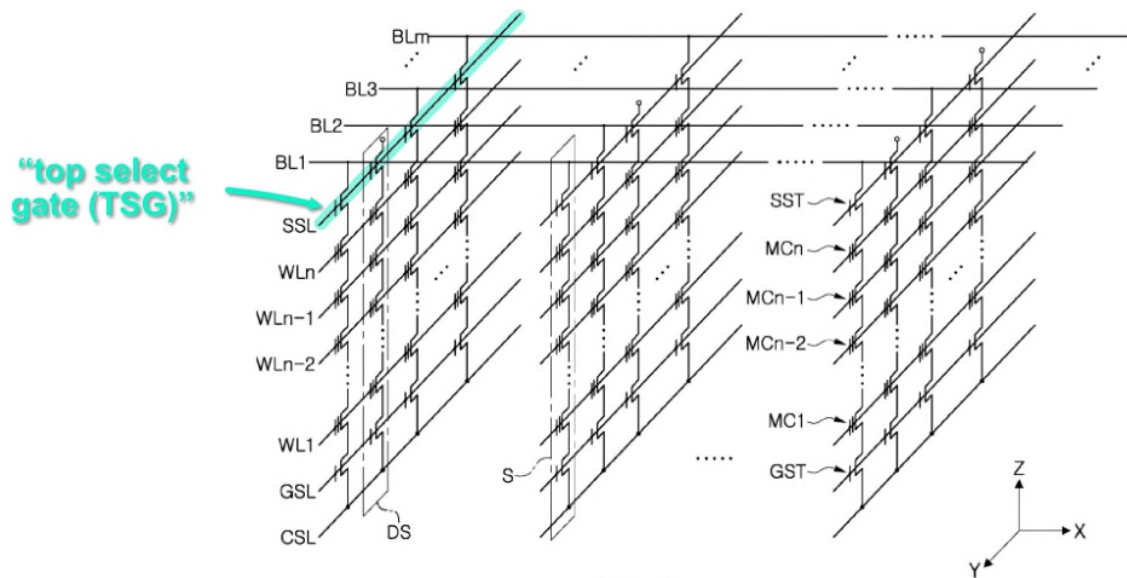


FIG. 2

*Id.*, Fig. 2.

Further, “insulating layers” are “disposed between” all Park’s “gate electrode layers[,]” including the SSL and adjacent layers. Park, 5:17-22. Figure 36 provides an example: “layer GL1 ... form[s] the” GSL. *Id.*, 16:9-11. “[L]ayers

GL5 to GL12 ... form the word lines....” *Id.*, 16:13-14. And “layers GL14 and GL15 may form the” SSL. *Id.*, 16:14-16. There are a “*plurality of insulating layers*” (green) between the “*plurality of word lines*” (layers GL5-GL12, red) and the “*top select gate (TSG)*” (layers GL14-G15, light blue):

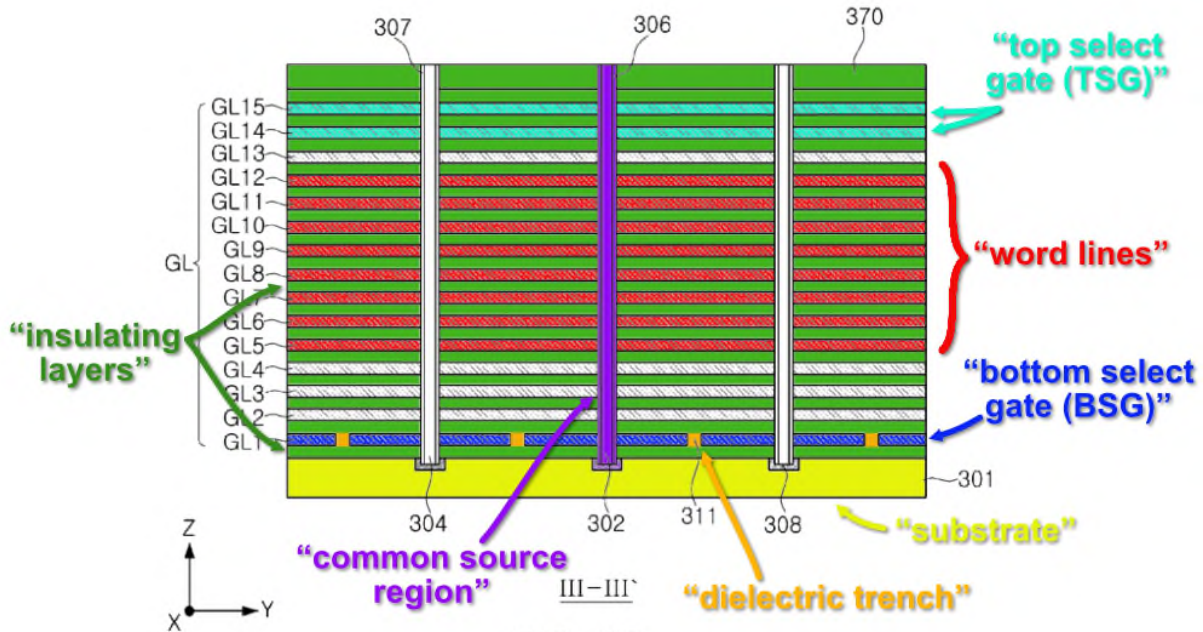


FIG. 36

*Id.*, Fig. 36; Lee, ¶¶ 196-201.

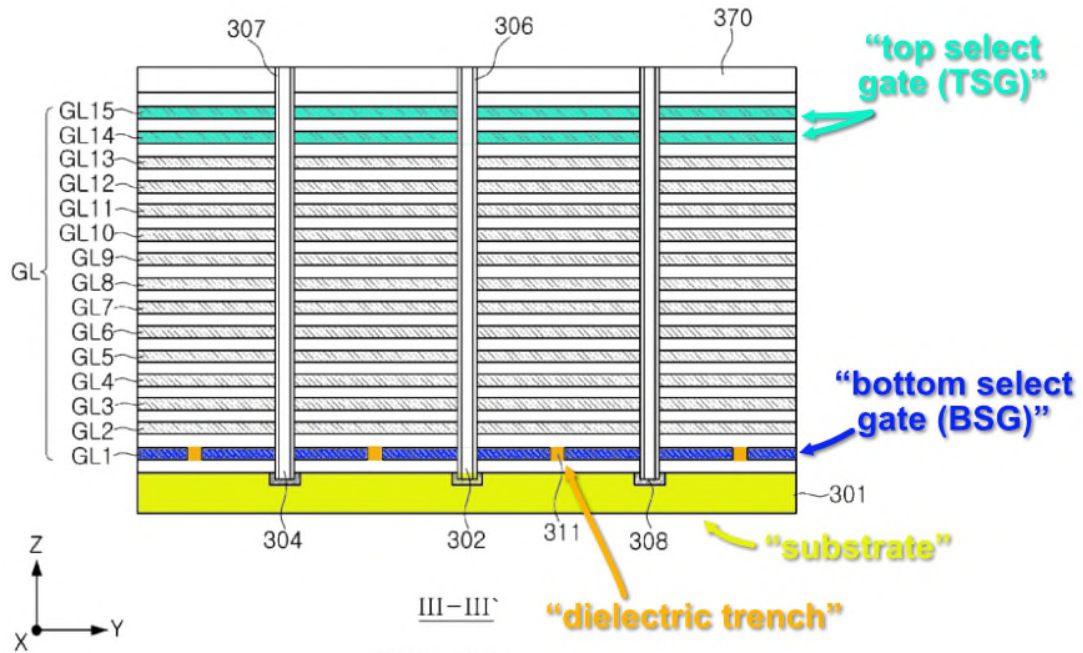
[2.B] “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.”

Both Park’s upper SSL and lower GSL are “separated” into parts “between ... unit areas UA1 to UA8” so that the unit areas can be “independently control[led].” Park, 5:65-6:12; *see also* 7:19-29 (discussing “separat[ion]” of SSL into portions); 16:22-37 (the GSL and SSL “may be divided into unit electrodes” associated with the same “unit areas”). Thus, as this claim requires, Park

“*separate[s]*” its “*TSG*” (the upper SSL) into “*sub-TSGs*” (the portions of the SSL corresponding to unit areas UA1-UA8). Lee, ¶¶ 202-204.

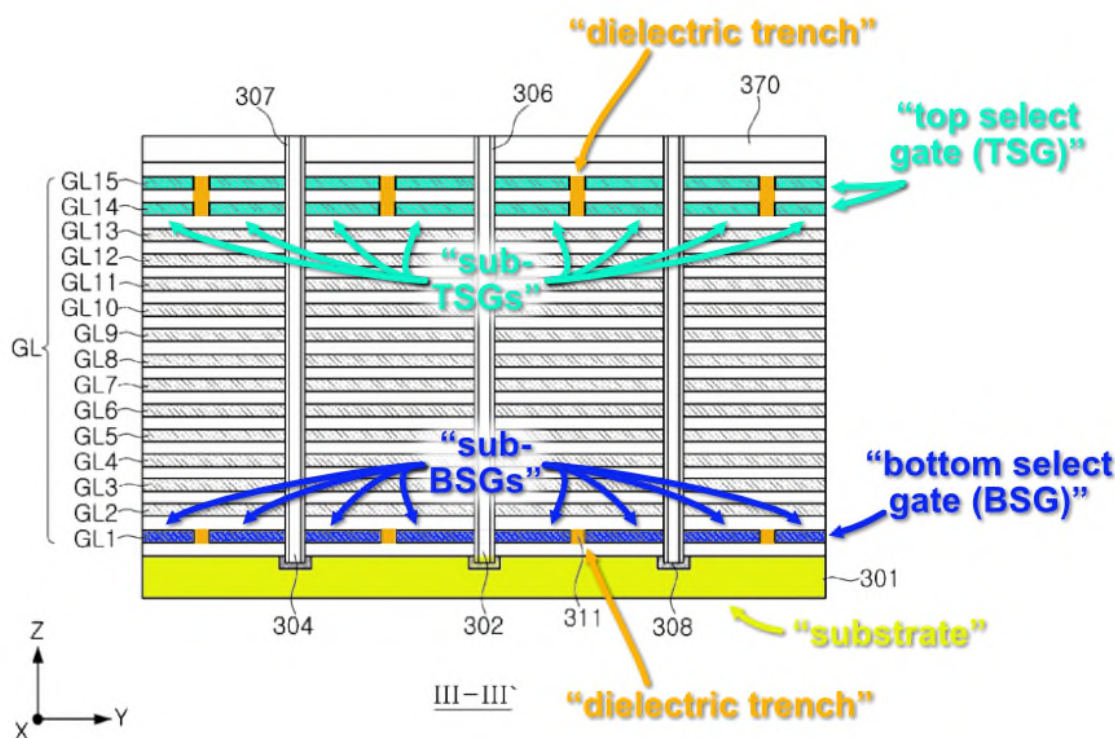
While Park does not provide an example of a device that effects this separation with “*one or more second dielectric trenches formed in the TSG*” that “*extend[] in the length direction of the substrate[,]*” a POSITA would nonetheless have considered this obvious in view of Park’s disclosure, in particular of the 111 isolation insulating layers, and the knowledge of a POSITA. Again, “isolation insulating layers 111” are employed to separate Park’s lower GSL into independently controllable portions. *See* Park, 5:67-6:4; 10:55-57; *supra* discussion of limitation [1.E]. In some of Park’s embodiments—including that shown in Figures 3, 4, and 11—the upper SSL does not have the same physical extent as the lower GSL. *See, e.g., id.*, Figs. 3, 4, and 11. As a result, it is not present over the portion of the GSL divided by “isolation insulating layers 111.” *See id.* So, here Park effects separation of the SSL using only “lines 102 and ... 103 of the second common source lines 105.” *Id.*, 6:4-8.

This, however, is only an “example.” Park, 6:4-8. In other embodiments—like Figure 36—the upper SSL is located over the portion of the GSL divided by isolation insulating layers 111 (the layers 111 are labeled 311 in this embodiment):



*Id.*, Fig. 36. Here, “GL1 . . . form[s] the” GSL. *Id.*, 16:9-11. And “GL14 and GL15 . . . form the” SSL. *Id.*, 16:14-16. As shown, the GSL is “divided into separate unit electrodes . . . by the isolation regions 311.” *Id.*, 16:22-26. Park also explains that SSL layers “GL14 and GL15” are also “separated from each other” into portions associated with “unit areas UA1 to UA8.” *Id.*, 16:30-36. But unlike in Park’s other embodiments, the SSL is present where it cannot be completely divided by the common source lines. *See id.*, Fig. 36. Doing so would also divide Park’s word lines, which are meant to be electrically connected and shared across its memory blocks. *See id.*, 7:44-56. Given this, a POSITA would have understood that another method to separate the SSL is required. Lee, ¶¶ 205-214.

The only other method for separating electrodes into portions set forth in Park is the use of “isolation insulating layers 111.” Thus, a POSITA would have recognized that one obvious way to achieve the missing but required separation of Park’s SSL would be to simply include another “isolation insulating region 111” in the upper SSL layers. An example of this is shown in the demonstrative below:



Lee, ¶¶ 215-216. Now, as adapted, “*one or more second dielectric trenches*” (a separate set of upper isolation insulating regions shown in orange) divides Park’s “*TSG*” (upper SSL layers GL14-GL15) into “*sub-TSGs*” (separate portions corresponding to unit areas UA1-UA8). *Id.*, ¶ 217. The same process used when forming the lower isolation insulating layers 111—forming an opening or trench and then filling it with dielectric material—would be used to form the new upper

isolation layers. *Id.*, ¶ 218.

A POSITA would have been motivated to use Park’s “isolation insulating layers 111” to divide its SSL layers and would have expected to succeed when doing so. Lee, ¶ 219. “Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.” *Boston Sci. Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009). Similarly, “predictable variation[s]” of the prior art’s teachings are also obvious. *See id.* (quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007)). This is all the application of Park’s “isolation insulating layers 111” to its upper SSL layers is here: Park already teaches that isolation insulating layers 111 can be used to divide select gates into individually controllable portions. A POSITA would have considered use of the same type of layers 111 in other places—including to divide the SSL—for the same purpose they already serve to be nothing more than a routine, obvious extension of Park’s existing teachings. *See* Lee, ¶¶ 220-223. Indeed, numerous prior art references teach this very approach. *See, e.g.*, Ex. 1017, 7:40-44, Fig. 3 (“string selection gate electrodes 202a and 202c” “separated” by “a cutting insulation pattern 118”); Ex. 1016, 6:5-15, Fig. 4A (“string select transistor SST” is “divided into a plurality of regions electrically separated” by “insulating layer 173”); Ex. 1018, [0058], Fig. 4B (“upper electrodes ELb ... may be spaced apart ... by an insulating separation pattern 50”).

Further, as discussed in Ground 2 below, this claim is also rendered obvious for additional reasons when Park is modified following Shibata's teachings.

### 3. Claim 3

Claim 3 depends on claim 2 and further requires that:

**[3] “the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate.”**

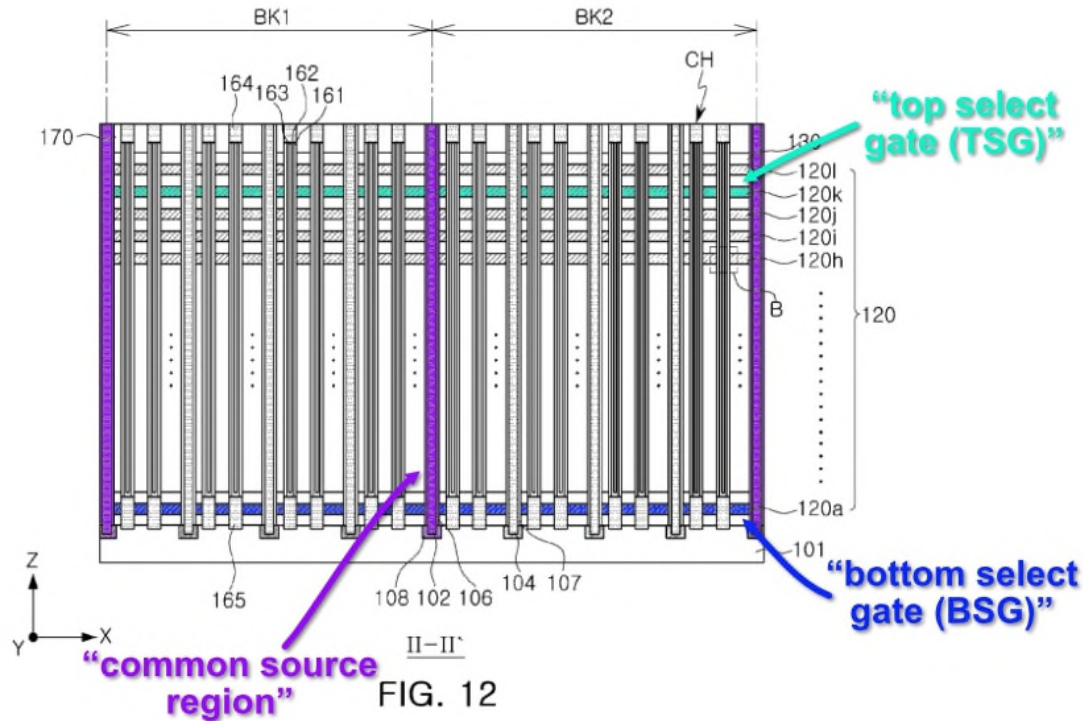
Park's SSL and GSL are “separated from each other” in the same location: “between ... areas UA1 to UA8.” Park, 6:1-4; 7:20-29 (similarly explaining that the lines are “separated” “at the boundaries between” “unit areas UA1 to UA8”); 16:26-37 (similar). This allows the that “memory cells of the respective ...unit areas UA1 to UA8 may be independently controlled.” *Id.*, 10:65-67. Again, as discussed in connection with claim 2, in certain of Park's embodiments, the SSL is located over the GSL. *See supra* discussion of claim 2. Because both the SSL and the GSL are stacked this way and separated at the same location (the boundaries of unit areas UA1-UA8), a POSITA would have considered it obvious and understood that when dielectric trenches are used to effect this division, they will be “*aligned*.” *See* Lee, ¶¶ 226-230.

#### 4. Claim 4

Claim 4 depends on claim 2 and further requires that:

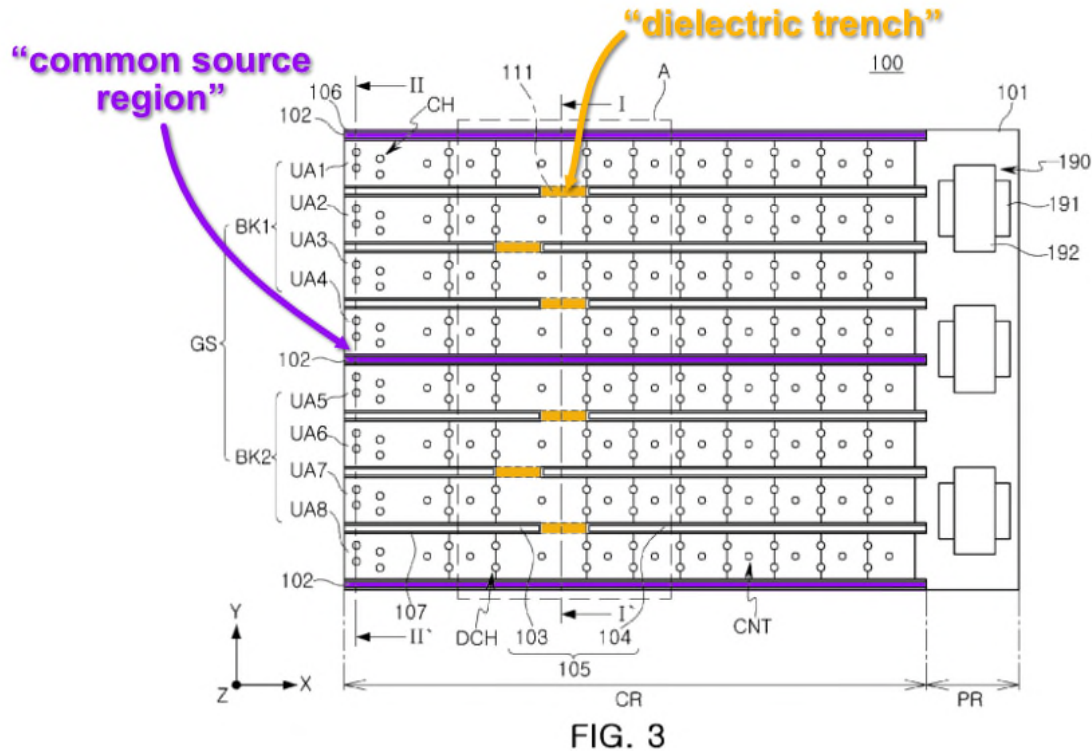
[4] “the one or more common source regions further pass through the TSG, and the one or more common source regions, the first dielectric trenches, and the second dielectric trenches extend parallel to each other in the length direction of the substrate.”

Again, Park’s memory device includes “*one or more common source regions*” (the common source lines 102). *See supra* discussion of limitation [1.F]. According to Park, these common source lines 102 pass through all its “gate electrode layers 120.” Park, 10:46-67. This includes Park’s “*TSG*” (its SSL). *See id.*, 2:1-3 (“first common source lines .... divid[e] the gate structure”); *see also* 7:20-29, 40-42. This is shown in Figure 12. “[C]ommon source regions” (common source lines 102, purple) pass through all the gate electrode layers 120, including Park’s “*TSG*” (SSL line 120*k*, light blue):



*Id.*, Fig. 12.

Park’s “*common source regions*” also “*extend parallel to*” the “*first dielectric trenches, and the second dielectric trenches*” “*in the length direction of the substrate.*” Per Park, common source lines 102 “*extend[] in the first direction, e.g., the X-axis direction...*” Park, 10:46-49; *see also* 1:53-54; 1:63-2:3. Park’s “*dielectric trenches*” (isolation insulating regions 111 and the equivalent regions that would be present in the SSL over the GSL, orange) extend in the same direction:



*Id.*, Fig. 3; *supra* discussion of claim 2; Lee, ¶¶ 232-238.

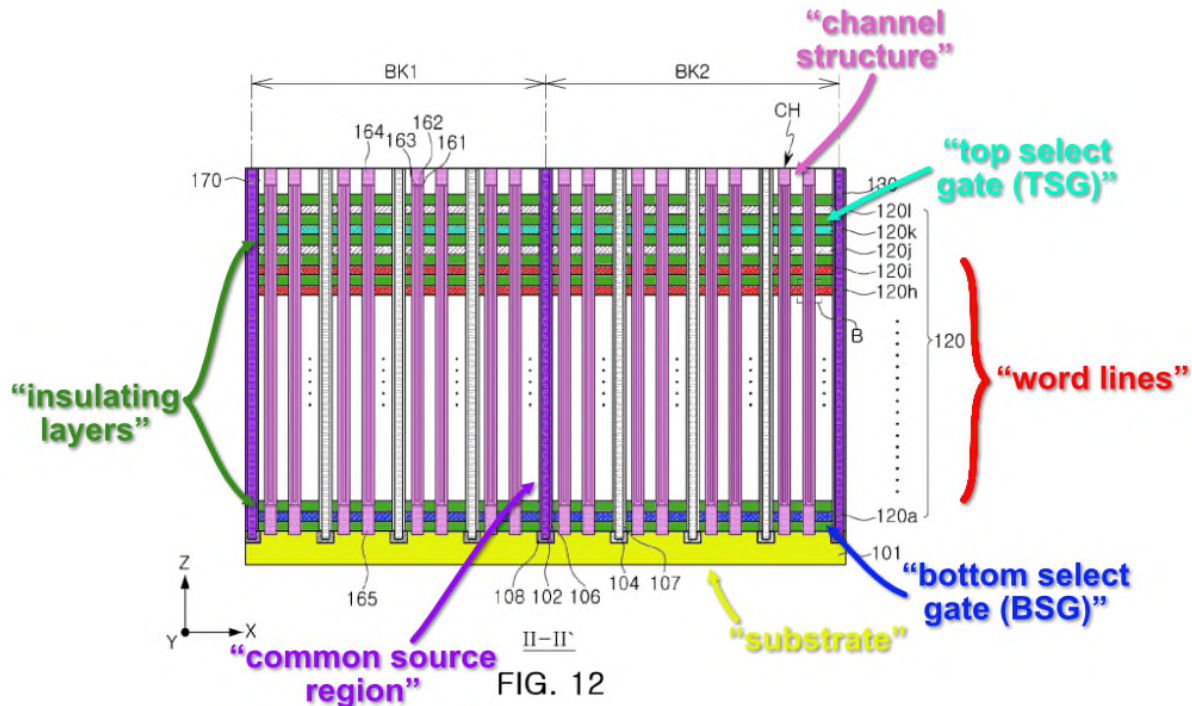
## 5. Claim 5

Claim 5 depends on claim 2 and further requires:

**[5] “a plurality of channel structures formed over the substrate along a height direction of the substrate that is perpendicular to the substrate, wherein each of the plurality of channel structure passes through the BSG, the plurality of word lines, the TSG, and the plurality of insulating layers.”**

Park’s memory device “includes a plurality of channel structures extending vertically through ... the gate electrode layers....” Park, 1:49-52; 5:34-41 (“cell channel structures CH” “penetrate” the gate/insulating layers); 11:11-14 (similar). Figure 12—annotated below—shows this. A “*plurality of channel structures*” (channel structures CH, pink) are “*over the substrate along a height direction of*

*the substrate that is perpendicular to the substrate*” (the CH extend vertically in the Z-axis direction from substrate 101, yellow). Further, these “*channel structures*” “*pass[] through the BSG*” (GSL layer 120a, blue), “*the plurality of word lines*” (the intermediate conductive layers, red), “*the TSG*” (SSL layer 120k, light blue), “*and the plurality of insulating layers*” (green):



*Id.*, Fig. 12; Lee, ¶¶ 239-243.

## 6. Claim 6

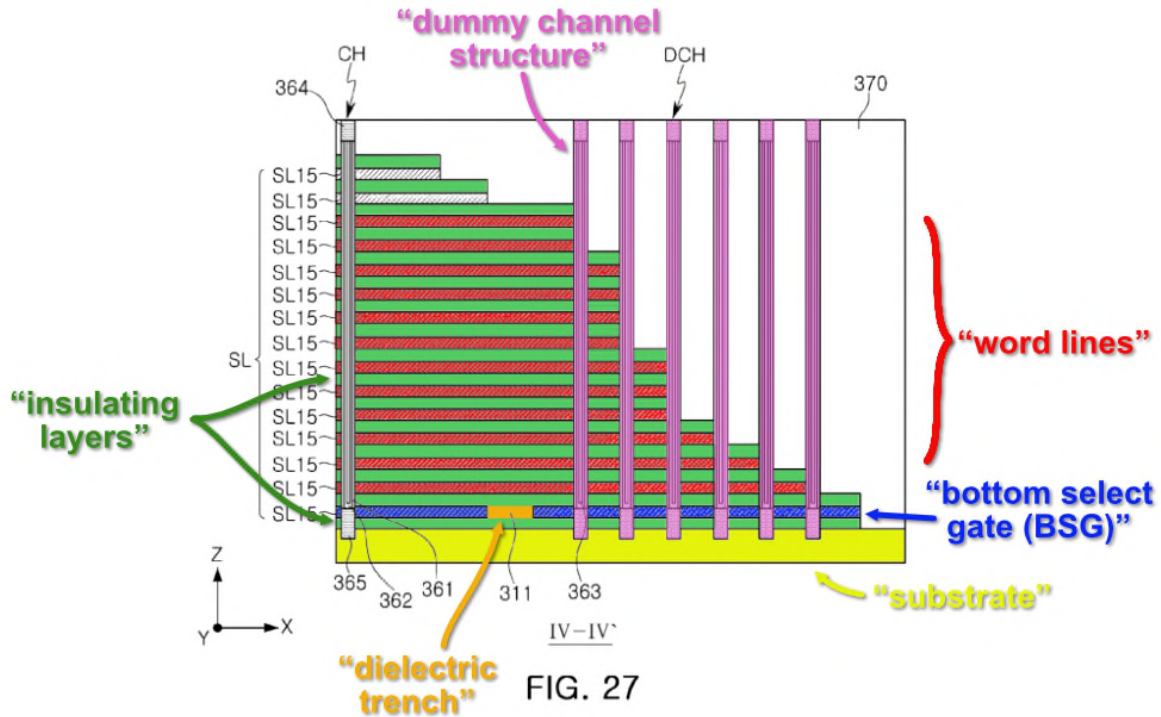
Claim 6 depends on claim 1 and further requires:

[6] “a plurality of dummy channel structures formed along the a height direction of the substrate that is perpendicular to the substrate, the plurality of dummy channel structures passing through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate.”

Park’s “memory device” also includes “at least one dummy string DS” with

“a dummy channel” “DCH[.]” Park, 4:55-65; 5:30-32. The “dummy channel structures DCH ... have a structure similar to that of the cell channel structures CH.” *Id.*, 11:19-21; *see also* 5:34-41.

As exemplified by Figure 27 below, Park teaches what this claim requires. A “*plurality of dummy channel structures*” (the DCH, pink) are “*formed along ... a height direction of the substrate that is perpendicular to the substrate*” (the DCH extend vertically in the Z-axis direction). Further, these “*dummy channel structures*” “*pass[] through the BSG*” (the lowest sacrificial layer that will later be replace with conductive GSL, blue), “*the plurality of word lines*” (the intermediate sacrificial layers that will also be later replaced with conductive WL, red), “*and the plurality of insulating layers*” (green), “*to extend into the substrate*” (yellow):



Park, Fig. 27; Lee, ¶¶ 244-252.

## 7. Claim 7

Claim 7 depends on claim 5 and further requires:

**[7] “a plurality of memory cell sub-blocks, each of the memory cell sub-blocks including a plurality of respective channel structures that are connected to a same sub-BSG and to a same sub-TSG, each of the memory cell sub-blocks being operated individually.”**

As explained above, Park’s “memory device 100” includes a “cell region CR” with a “gate structure GS” that can be “divided into a plurality of blocks BK1 and BK2.” Park, 4:61-5:7. “[A] plurality of cell channel structures CH” pass through the blocks’ “gate structure.” *Id.* Each block includes a portion of Park’s “memory cell array” (and thus a portion of its cell channel structures CH). *Id.*, 3:39-40; Fig. 3 (showing multiple channel structures CH in each block). The

blocks are further sub-divided into “unit areas.” *Id.* For example, “first block BK1” includes “unit areas UA1 to UA4” while “second block BK2” includes “unit areas UA5 to UA8.” *Id.*, 5:8-10. And according to Park, its SSL and GSL “may be separated from each other between ... unit areas UA1 to UA8.” *Id.*, 6:2-4. This allows the unit areas to be “independently controlled.” *Id.*, 7:17-29, 10:55-67. Park’s unit areas UA1-UA8 correspond to the claimed “*memory cell sub-blocks.*” Each unit area includes “*a plurality of respective channel structures*” (CH) that are “*connected to a same sub-BSG*” (the portion of the GSL in the unit area) and “*to a same sub-TSG*” (the portion of the SSL in the unit area) such that they can be “*operated individually.*” Lee, ¶¶ 253-259.

## 8. Claim 8

Claim 8 depends on claim 5 and further requires that:

**[8] “the one or more first dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate.”**

As shown in Figure 3, Park’s “*dielectric trenches*” (isolation insulating regions 111, orange) are “*alternatively disposed in the width direction*” (the Y-axis direction) with the “*common source regions*” (common source lines 102, purple) along the line I-I’:

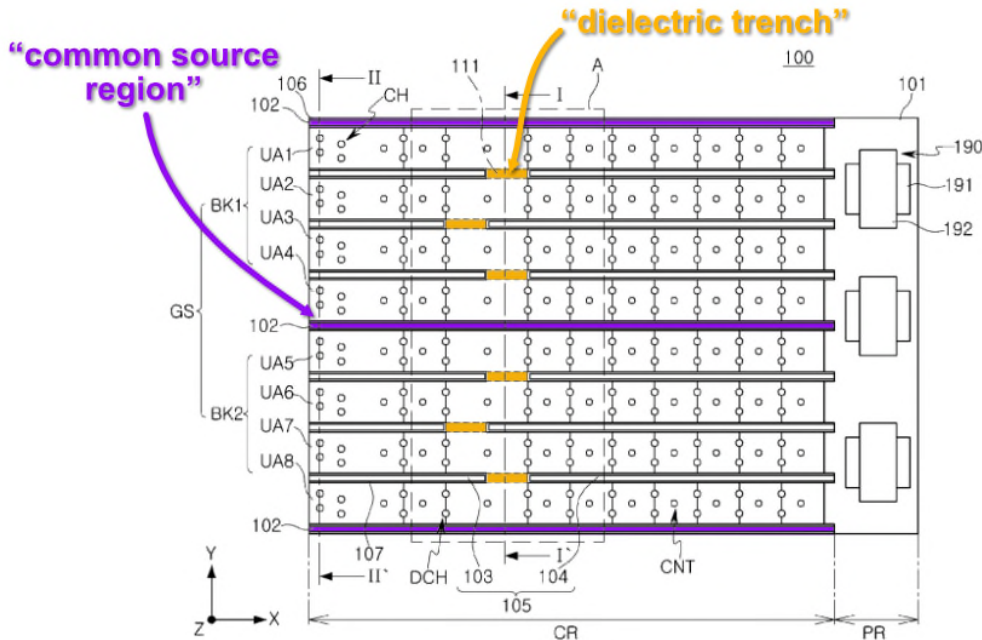


FIG. 3

Park, Fig. 3; Lee, ¶¶ 260-262.

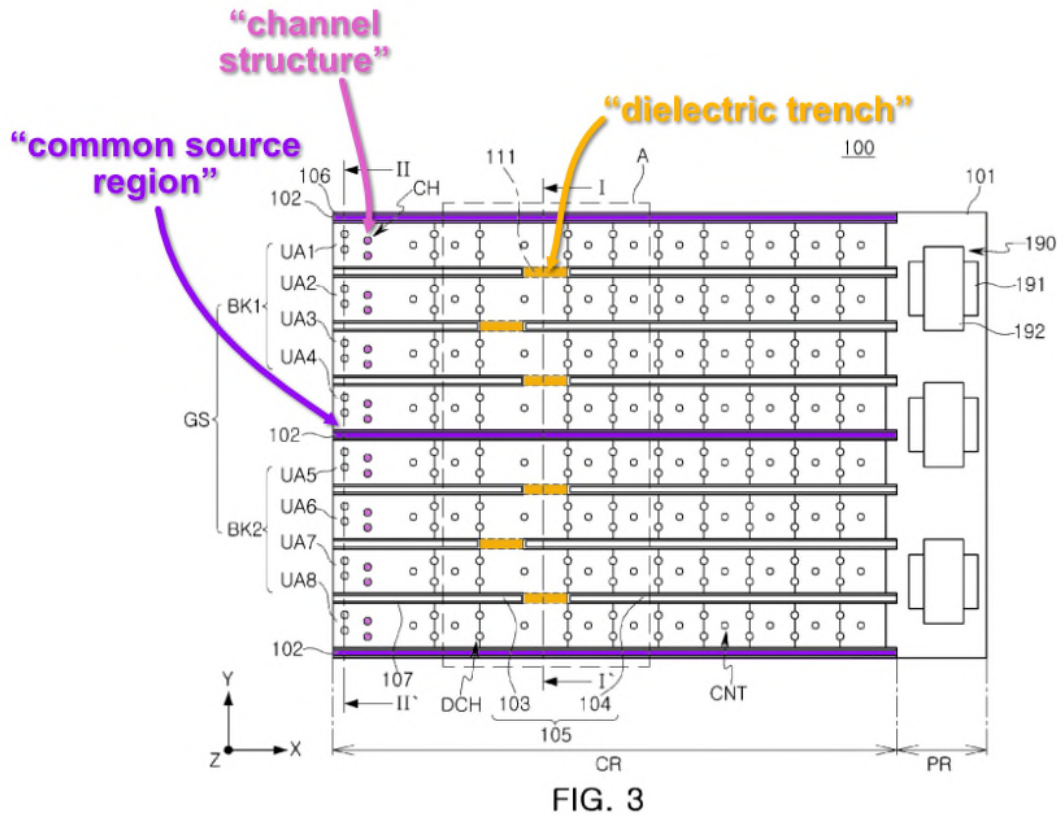
## 9. Claim 9

Claim 9 depends on claim 5 and further requires that:

[9] “the one or more second dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate so that a plurality of channel structures are disposed therebetween.”

As explained above when discussing claim 3, a POSITA would have considered it obvious to locate Park’s “first dielectric trenches” and “second dielectric trenches” over each other. *See supra* discussion of claim 3. This results in what this claim requires. The “*second dielectric trenches*” (orange below) are “*alternatively disposed in the width direction of the substrate*” (the Y-axis direction) with the “*common source regions*” (common source lines 102, purple). And there are a “*plurality of channel structures*” (channel structures CH, pink)

located between the trenches and common source regions:



Park, Fig. 3; Lee, ¶¶ 263-267.

## 10. Claim 10

Claim 10 depends on claim 1 and further requires:

[10] “one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.”

Park teaches the claimed “dummy BSGs” that are “between the plurality of word lines and the BSG” and are “spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.” Park includes “at least one dummy line between the string select line and the word lines or between the

ground select line and the word lines.” Park, 5:26-29; 16:9-17 (“dummy line[s]” may be located between the GSL and “word lines,” and SSL and “word lines”); 4:25-28 (similar); 7:2-7 (similar). All of Park’s gate electrode layers—including the dummy layers—are separated from adjacent layers by “insulating layers.” *Id.*, 5:17-26; 6:49-52; 10:34-45.

Next, a POSITA would have considered it obvious that Park’s “*first dielectric trenches*” (isolation insulating layers 111) would pass through not only its “*BSG*” (the GSL) but also its “*dummy BSG*” (the dummy lines adjacent to the GSL). According to Park, its “dummy lines” may also be “separated,” e.g., by the common source. *E.g.*, Park, 7:39-43. And because Park associates these dummies with its select lines (*see id.*, 5:26-29, 7:2-7), a POSITA would have understood that they would be—or at the very least obviously could be—structured and divided in the same way as the select lines themselves. *See* Lee, ¶¶ 269-275.

While Park does include embodiments where only its select lines—and not the dummy lines—are separated into portions corresponding to unit areas UA1-UA8, a POSITA would have recognized that these are only non-limiting examples. *See* Lee, ¶ 276. When the ’623 patent was filed, a range of different separation structures were known and used in the prior art. This includes structures separating only a single select gate layer (*see, e.g.*, Park, Fig. 11 (layer 111 separating line 120a)) or all the conductive layers (Shibata, Fig. 3 (element 60

separating a stack of conductive layers 70)). It was also known that a single dielectric trench could be structured to pass through and similarly divide multiple adjacent electrode layers. *E.g.*, Ex. 1018, [0058], Fig. 4B (trench 50 dividing two adjacent layers ELb). In view of these various known options, a POSITA would have considered it highly obvious that both Park's GSL and the adjacent dummy layer would be divided by the same dielectric trench. *See* Lee, ¶¶ 277-282. Doing so would also improve electrical performance. *Id.*, ¶ 281.

## 11. Claim 11

Claim 11 depends on claim 2 and further requires:

**[11] “one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs, and spaced apart from the plurality of the word lines and the TSG by the plurality of insulating layers.”**

As explained above when discussing claim 10, Park teaches that its memory device can include “dummy line[s]” between its “string select line” and the adjacent “word lines.” Park, 5:26-29. These dummy lines are the claimed “*dummy TSGs*.” Lee, ¶¶ 283-286. Moreover, a POSITA would have considered it obvious for Park's “second dielectric trenches” to pass through not only its “*TSG*” (the SSL) but also its “*dummy TSGs*” (the dummy lines) for the same reasons explained for claim 10. *Id.*, ¶ 287. Additionally, Park forms “dielectric trenches” by etching through already applied layers. *See* Park, 12:65-13:1. A POSITA would have recognized that when there is no surface to stop etch

progression, it is often difficult to etch through only a single layer when performing a timed etch. *See* Lee, ¶¶ 288-289. There is no such etch stop surface below Park’s SSL. *Id.*, ¶ 290. Because of this, a POSITA would have recognized that Park’s etching process could potentially form a trench not only in the SSL but also in at least some of the adjoining dummy layers. *Id.* A POSITA would have recognized that one of the functions of the dummy layers would have been to provide a buffer ensuring that—while the trench enters some of the dummy layers—it does not reach the word lines. *Id.*, ¶ 291.

**B. Ground 2: Claims 1-11 Are Obvious Over Park in View of Shibata**

As explained above in Ground 1, Park teaches (or renders obvious) everything claims 1-11 require, including the use of “*dielectric trenches*” to divide select gate layers into independently controllable portions.

Despite this, it is possible that Patent Owner may argue that Park’s isolation insulating layers 111 do not qualify as the “dielectric trenches” of claim 1 because they separate Park’s “BSG” into portions only in cooperation with Park’s common source line 105. Patent Owner might also argue that a POSITA would not have found it obvious to employ Park’s layers 111 to separate both its lower “BSG” and its upper “TSG” into portions as claim 2 requires. While both arguments would be wrong, all the claims would still be obvious when Shibata’s teachings are applied to Park.

Shibata—like Park—teaches a “semiconductor memory device” with memory cells arranged in a “three-dimensional structure.” Shibata, [0002]-[0003]. Shibata divides its memory into independently controllable “unit[s].” *E.g., id.*, [0083], [0129], [0167], [0227], [0270]. Also like Park, Shibata achieves this independent control by dividing one of its select gate layers into portions with trenches of dielectric material. In particular, as exemplified in Figure 16 below, multiple “separation portion[s] 62a” “pierce[] ... the drain-side select gate layer of the uppermost layer of the multiple conductive layers 70[.]” *Id.*, [0090]. This divides Shibata’s upper “**TSG**” (the drain-side select gate layers) into “**sub-TSGs**” (portions SDG0-SGD3):

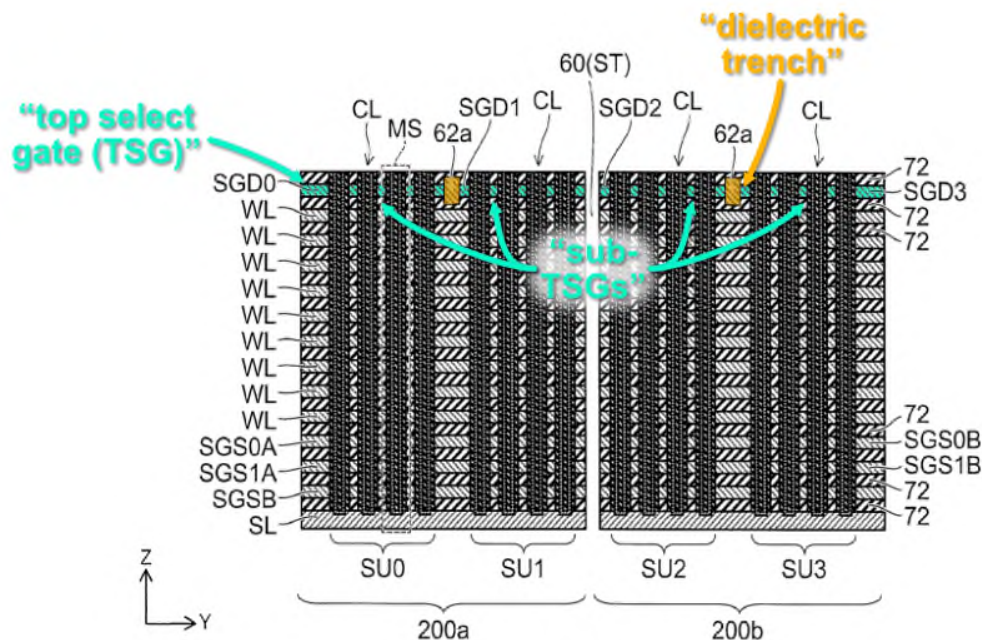
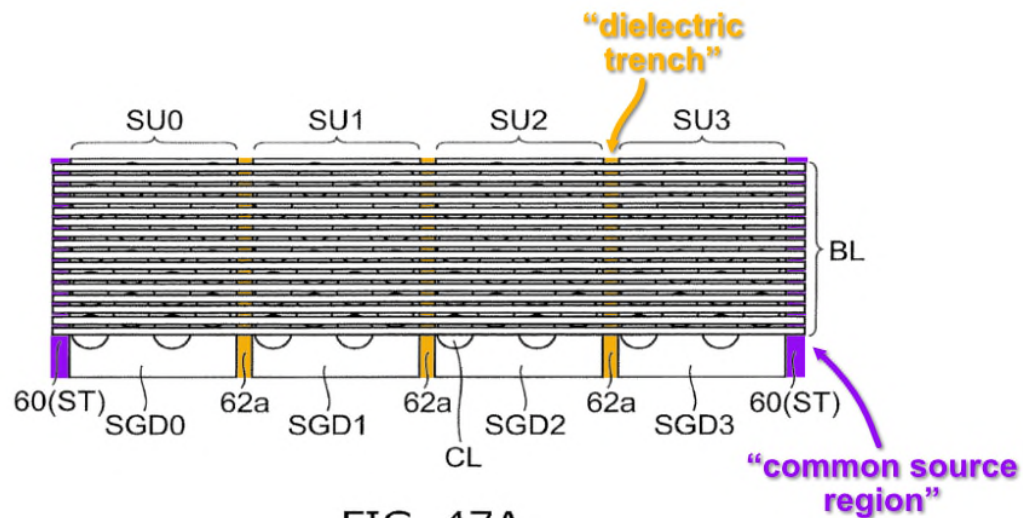


FIG. 16

*Id.*, Fig. 16; [0166]. The “separation portion 62a is an insulating film extending in

the same direction as the separation portions 60 (the slits ST) piercing the entire stacked body 100.” *Id.* These portions 60 / slits ST can include an “interconnect portion LI” electrically connected to a lower common source “active region 10a of the substrate 10.” *Id.*, [0065]. As shown below, Shibata’s “separation portion[s] 62a” traverse the entire length of its memory device for purposes of dividing the select gates:



*Id.*, Fig. 47A.

Applying this to Park, a POSITA would have eliminated Park’s second common source lines 105 and replace them with longer isolation insulating regions 111 with dimensions analogous to Shibata’s separation portions 62a. *See Lee*, ¶¶ 294-303. The below demonstrative provides one example of how this would be achieved:

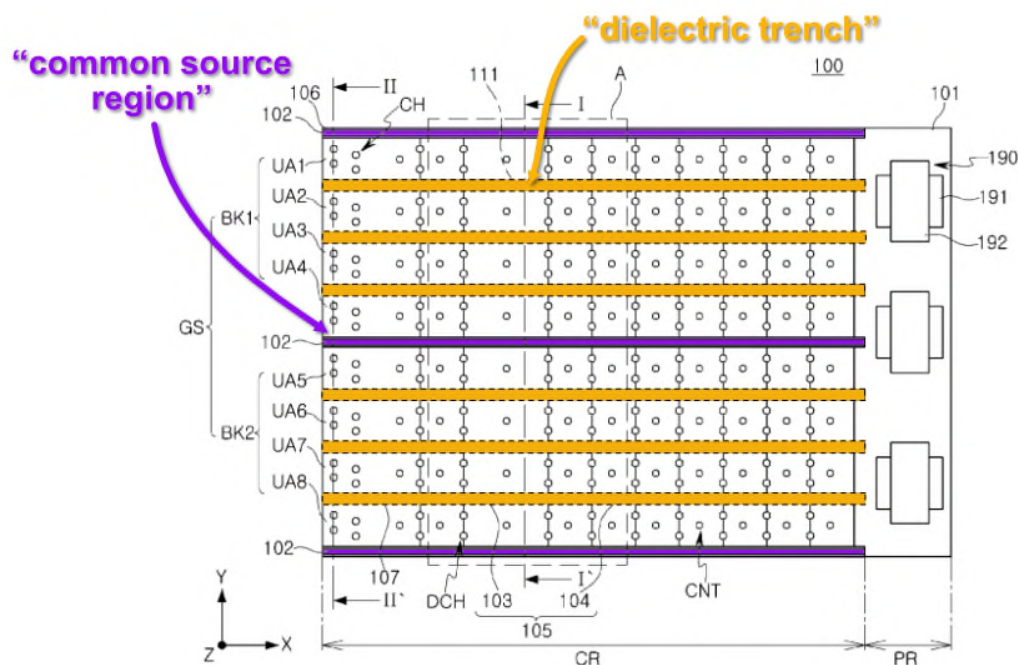


FIG. 3

*Id.*, ¶ 304.

Now, as adapted, Park includes longer “*dielectric trench[es]*” (the lengthened isolation insulation regions 111 shown in orange) that span the length of its device to completely and by themselves separate its “*BSG*” (the lower GSL) into “*sub-BSGs*” (portions associated with unit areas UA1-UA8). Lee, ¶ 305. Moreover, because the second common source regions 105 that previously separated Park’s “*TSG*” (the upper SSL layers) into portions are no longer present, a POSITA also would have included “*second dielectric trenches*”—in the form of Shibata’s “separation portion[s] 62a”—in Park’s “*TSG*.” *Id.*, ¶¶ 306-307. This would allow Park’s upper SSL to continue to be divided into individually controllable portions. *See* Park, 5:65-6:12; 7:19-29, 16:22-37.

Shibata explains that using dielectric “separation portions” to effect division—instead of more common source regions—results in an improved device: dielectric “separation portions” “are narrower than the widths of the separation portions 60.” Shibata, [0116]. So, by using the narrower dielectric separation portions instead of wider common source regions to divide the memory, “it is possible to ... reduce the planar size of the memory cell array.” *Id.*, [0118]; [0154]. Other prior art includes similar teachings. *E.g.*, Ex. 1009, [0001] (“a large number of source contacts in a memory array ... degrade the efficiency of the memory array and result in a large die size and a high fabrication cost”).

This would have motivated a POSITA to replace Park’s wider second common source lines 105 with additional, narrower dielectric trenches like Shibata’s separation portions 62a. Lee, ¶¶ 308-312. A POSITA would have recognized that doing so would allow Park’s memory device to be made smaller. *Id.* Alternatively, the device would be the same size, but there would be additional space for memory cell channels beneficially increasing the device’s memory density. *Id.*, ¶ 313. While it would be improved, the device would continue to function as intended: the lower GSL and upper SSL would still be divided into portions allowing for independent control of unit areas UA1-UA8. *Id.*, ¶ 314.

A POSITA also would have considered application of Shibata to Park to amount to nothing more than a routine, obvious design choice. Lee, ¶ 315. As

shown by both Park and Shibata, it was known that select gates can be divided into individually controllable portions by either trenches of insulation or common source regions. *Id.*, ¶ 316. A POSITA would have considered both design approaches when implementing Park. *Id.*

A POSITA also would have had a reasonable expectation of success. Park already employs trenches of dielectric material to separate its select gates into independently controllable portions. Lee, ¶ 317. Lengthening these trenches, or including similar trenches in other gate layers, would have been considered nothing more than an extension of an approach that Park already utilizes. *Id.*, ¶ 318. Park does imply that allowing “isolation regions” to face each other in a layer can present issues. *See, e.g.*, Park, 15:35-16:2. But Shibata proposes a solution to this. *See* Shibata, [0324]-[0325]. In particular, if facing trenches of isolation like Shibata’s “separation portions 62a” inhibit the removal of sacrificial layers—resulting in “narrower” select gates with increased resistance—separate “drive circuits” can be employed in each individually controllable memory unit to maintain proper device operation. *See id.*, [0446]-[0449]. A POSITA also would have recognized that any manufacturing issues could be minimized by replacing some—but not all—of Park’s common source lines 105 with isolation insulating layers 111:

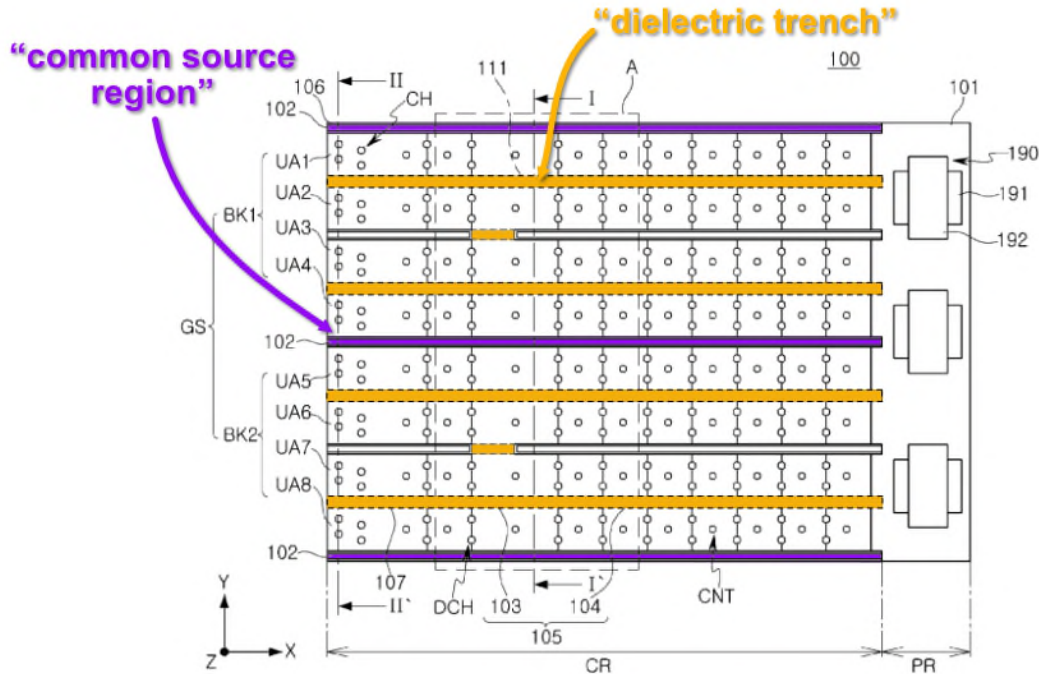


FIG. 3

Lee, ¶¶ 319-323. In such a design, the vast majority of the layered structure has a lengthwise cut—that will eventually contain common source regions 102 and 105—on at least one side. *See id.* This would ensure that the majority of the sacrificial layers are removed and replaced with conductive material, thereby improving device performance without the need for separate drivers. *Id.*, ¶ 324.

**C. Ground 3: Claims 1-11 Are Obvious Over Shibata in View of Park**

Shibata—when modified in view of Park and the knowledge of a POSITA—also renders claims 1-11 obvious.

**1. Claim 1**

**[1.Pre] “A memory device, comprising:”**

To the extent limiting, Shibata teaches a “semiconductor memory device.” Shibata, [0002]; Lee, ¶¶ 327-328.

**[1.A] “a substrate;”**

Shibata’s memory device includes a “memory cell array 1” supported on “the substrate 10” with a “source layer ... SL” on its surface. Shibata, [0055]-[0056]. “The source layer SL” can be “a semiconductor layer doped with an impurity....” *Id.* Shibata also teaches that the source layer SL (and an associated insulating layer 41) can be replaced in any of its embodiments with a “active region (e.g., a P-type well) 10a” on the upper surface of “substrate 10.” *Id.*, [0065]. This is shown in Figure 23. The “***substrate***” in this figure (the combination of substrate 10 and active region 10a) is annotated yellow:

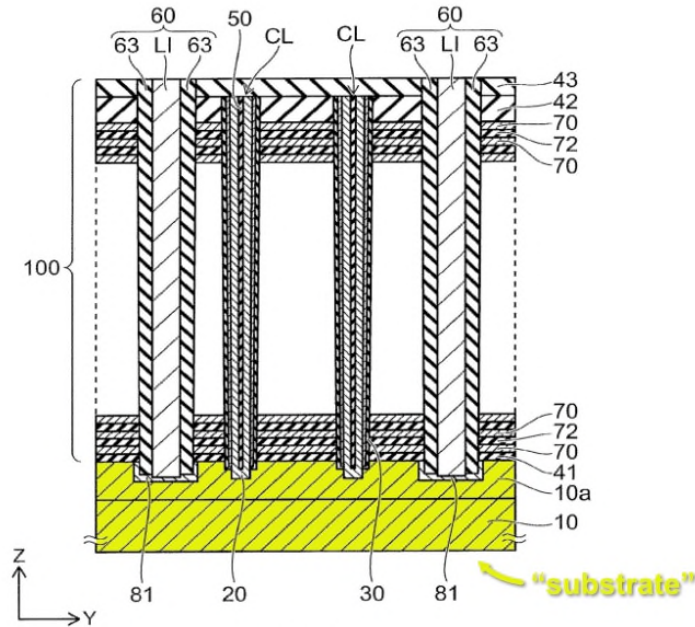


FIG. 23

*Id.*, Fig. 23; Lee, ¶¶ 329-336.

**[1.B] “a bottom select gate (BSG) disposed over the substrate;”**

Shibata’s memory device includes a “stacked body 100” that is located over its substrate and source layer. Shibata, [0055]. The “stacked body” is formed from “multiple ... conductive layers” with “insulator interposed....” *Id.*, [0003]. Among the conductive layers are “select gates functioning as control gates of select transistors.” *Id.* The “lowermost” “conductive layer 70 ... functions as a control gate (a source-side select gate) of the source-side select transistor[s] STS.” *Id.*, [0074]; [0048]. For example, in Figure 15 there is “one ... drain-side select gate layer[]” (labeled SGD) and “three ... source-side select gate layers” (labeled SGS0, SGS1, and SGSB). *Id.*, [0166]. Shibata’s “**bottom select gate (BSG)**” (the lower source-side select gate or SGS layers) are annotated blue below:

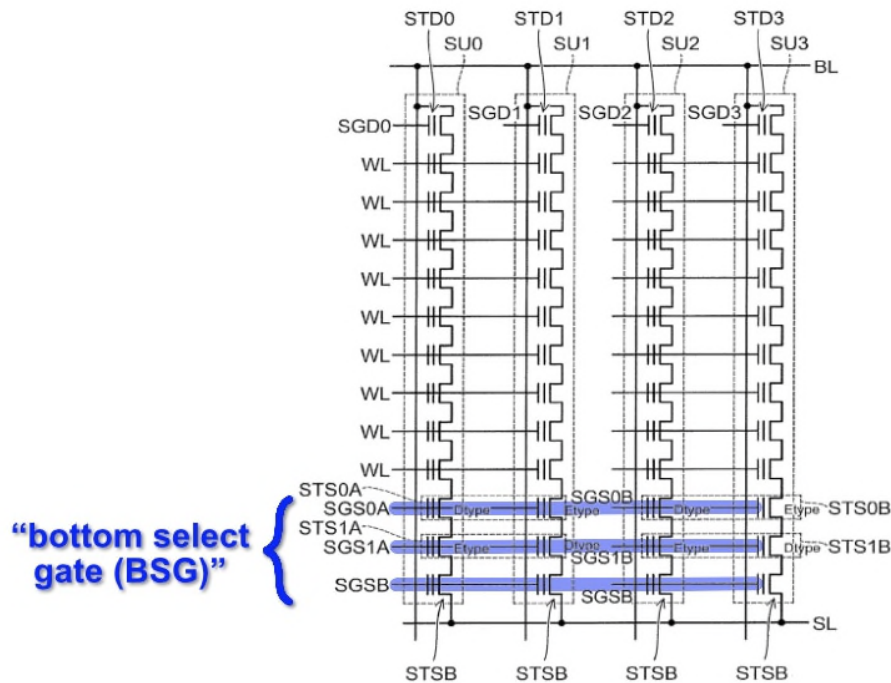


FIG. 15

*Id.*, Fig. 15. The same-source side select gate layers are also depicted in Figure 16. As shown, they are stacked and “*disposed over*” Shibata’s substrate (the yellow source layer SL, which again can be replaced with an active region 10a at the top of a substrate 10):

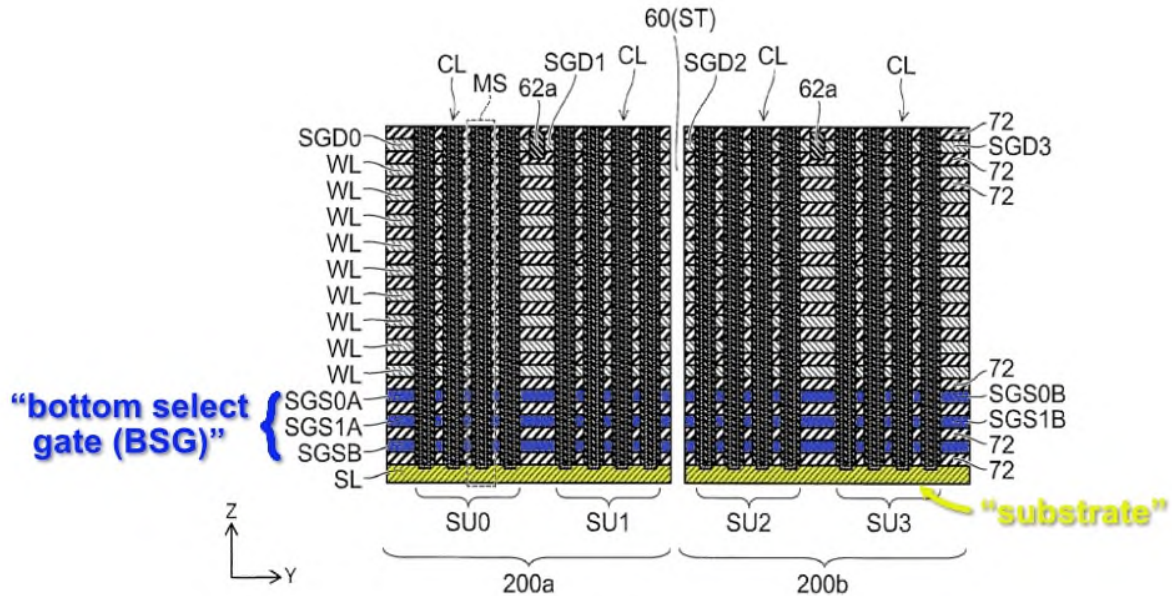


FIG. 16

*Id.*, Fig. 16; Lee, ¶¶ 337-343.

[1.C] “a plurality of word lines positioned over the BSG with a staircase configuration;”

The “multiple ... conductive layers” that make up Shibata’s device include layers of “word lines.” Shibata, [0003]; [0048]. Per Shibata, these “word lines WL are stacked between the drain-side select gate layer and the source-side select gate layers.” *Id.*, [0166]. Figure 15 shows a memory device including this “*plurality of word lines*” (WL, red):



This limitation also requires that the “*word lines*” have a “*staircase configuration*.” Shibata does not reference a staircase, or discuss how electrical connection is made to its various word lines. Park, however, does. According to Park, a memory device’s “gate electrode layers”—including the word lines—“may extend by different lengths” such that they have “a stepped structure” to allow electrical connection. Park, 6:56-60; 7:8-11; 8:18-50; 11:62-65; Figs. 15, 25, 32.

A POSITA would have considered it obvious to employ this type of “step” structure with Shibata. A POSITA would have recognized that for Shibata’s memory device to function, its word lines must be electrically connected to other circuitry that supplies the word lines with signals at appropriate times during the device’s operation (e.g., to select a target word line and associated memory cells for access). *See* Lee, ¶¶ 350-354. Shibata explains that its memory device has a “three-dimensional structure.” Shibata, [0003]. When the ’623 patent was filed, one of the most common and routinely used methods to connect to the word lines of such a structure was via a staircase outside of the memory cell array. *See, e.g.*, Ex. 1006, 295-297 (in typical 3D NAND, “the control gates and upper/lower SG are connected to the metal layers [via a] stair-like gate structure”); Ex. 1007, 7 (it is “common in 3D NAND” to employ a “staircase structure” to “build the connection to the wordlines and ... select gates”); Ex. 1011, [0003] (“[o]ne method of forming” required “electrical connection” to the “word lines” of a “conventional

vertical memory array” “includes forming a so-called ‘stair step’ structure”); Lee, ¶¶ 355-356. Such structures were highly routine and predictable to implement, as these were conventional structures in 3D NAND devices. *Id.*

**[1.D] “a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;”**

Shibata also teaches a device including a “*plurality of insulating layers.*” In particular, Shibata explains that there are “insulating layers 72 interposed” between each of its device’s “multiple conductive layers 70.” Shibata, [0061]. There is also an “insulating layer 72” between the “source layer SL” (or substrate active region 10a) “and the conductive layer 70 on the lowermost layer.” *Id.* Figure 16 provides an example. As shown, there are “*insulating layers*” (insulating layers 72, green) between the “*substrate*” (the SL / active region 10a, yellow) and “*BSG*” (the SGS layers, blue), between the “*BSG*” and “*plurality of word lines*” (the WL layers, red), and between the “*word lines*” themselves:

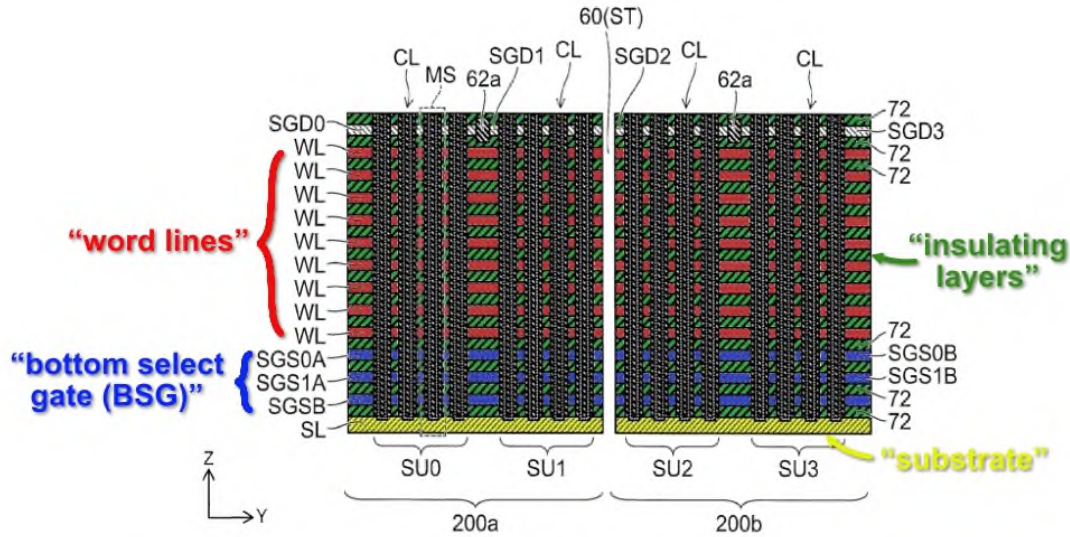


FIG. 16

*Id.*, Fig. 16; Lee, ¶¶ 357-360.

**[1.E] “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and”**

A POSITA would have considered this limitation obvious in view of Shibata and Park. Shibata explains that its memory can be divided into “block[s],” “sub-blocks” and “string unit[s].” Shibata, [0162]-[0163]. In Figure 16, the memory includes “two sub-blocks 200a and 200b subdivided by three separation portions 60 (slits ST)...” (one of these is labeled in the figure, while the others will be at the sub-block boundaries). *Id.*, [0162]. Each “sub-block” is then further divided into “string unit[s].” *Id.*, [0163]. “[S]tring unit SU0 and ... string unit SU1” are in “sub-block 200a” while “string unit SU2 and ... string unit SU3” are in “the other sub-block 200b....” *Id.* Per Shibata, the portions of its select gates in each string unit can be “controlled electrically independently.” *Id.*, [0083].

The sub-blocks are surrounded by a “[s]eparation portion 60” that “extends in the X-direction” and passes through all the device’s layers. Shibata, [0057]. “[S]eparation portion[s] 62a” are located between the string units. *Id.*, [0088]-[0090]. In Figure 16, these “separation portions” are “insulating films that extend in the same direction as the separation portion 60 (the slit ST).” *Id.*, [0088]. The separation portions are formed from an “insulating film” such as “a silicon oxide film[.]” *Id.*, [0107], [0110]. “The separation portion 62a is disposed between” string units “adjacent to each other” and “pierces only the drain-side select gate layer of the uppermost layer of the multiple conductive layers 70....” *Id.*, [0090]. The “separation portion[s]” operate to divide the select gate into four pieces SGD0-SGD3. *Id.*, [0166]. Again, this allows SGD0-SGD3 to be “controlled electrically independently.” *Id.*, ¶ [0167]. In sum, and as this limitation requires, a POSITA would have understood Shibata to employ a “*dielectric trench*” (its separation portions 62a) for purposes of separating one of its “*select gate[s]*” (the upper drain-side select gate layer) into “*sub*” gates (portions SGD0-3):

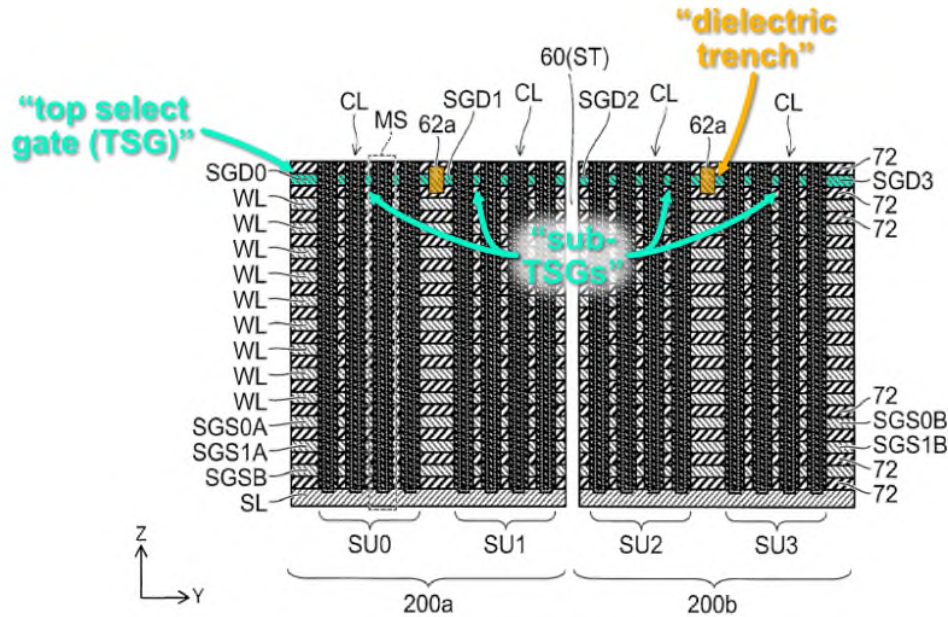


FIG. 16

*Id.*, Fig. 16; Lee, ¶¶ 361-372.

While Shibata does not refer to its “separation portion 62a” as a “trench,” this is what a POSITA would understand it to be. To form the separation portion, a “mask” is “formed on the stacked body 100” and “a slit ... is formed by RIE (reactive ion etching).” Shibata, [0106]. “The slit ... pierces the mask 75, the insulating layer 72” and the “sacrificial layer 71” that will later be replaced with conductive material to form the select gate. *Id.* The “slit” is then “fill[ed]” with “an insulating film ... 62” to form the “separation portion.” *Id.*, [0107]; [0108]-[0109]. This process is shown, for instance, in Figures 8B and 8C below:



FIG. 8B



FIG. 8C

*Id.*, Figs. 8B-C; Lee, ¶¶ 373-376.

While Shibata only employs its separation portion to divide its upper drain-side select gate and not its “*BSG*,” a POSITA would have considered it obvious to employ a similar approach in connection with its lower source-side select gate. To allow for control of its memory strings on a unit basis, Shibata employs both (1) separation portions 62a that divide its upper drain-side select gate into units (*see* Shibata, [0167]) and (2) multiple layers of bottom source-side select gates to connect/disconnect the various string units to either a lower source layer or the substrate (*see id.*, [0172], [0192]-[0200]). While the multiple bottom select gates can facilitate control on a string unit basis, a POSITA would have recognized that they require additional manufacturing steps and make Shibata’s memory array taller. *See* Lee, ¶¶ 377-379. Given this, a POSITA would have been motivated to consider other design alternatives that also allow for the same type of control

Shibata already provides. *See id.*, ¶ 380.

Park provides one such alternative. Rather than employing multiple bottom select gates, Park instead divides a single lower gate layer into multiple portions with isolation insulating layers 111. *See* Park, 5:67-6:12; 10:55-57. Fig. 11 provides an example:

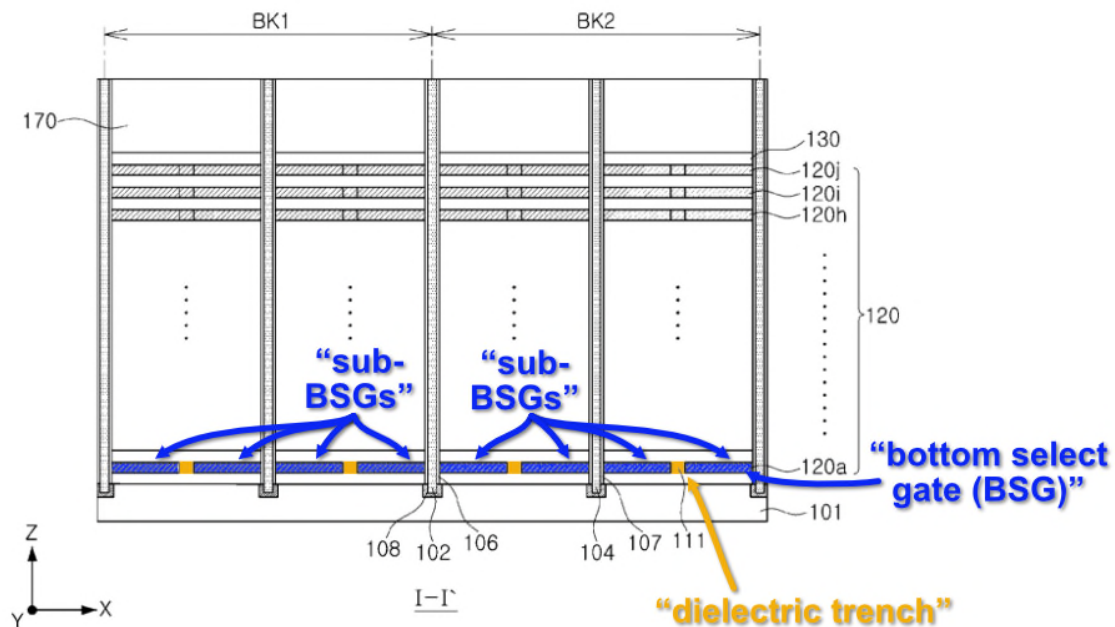
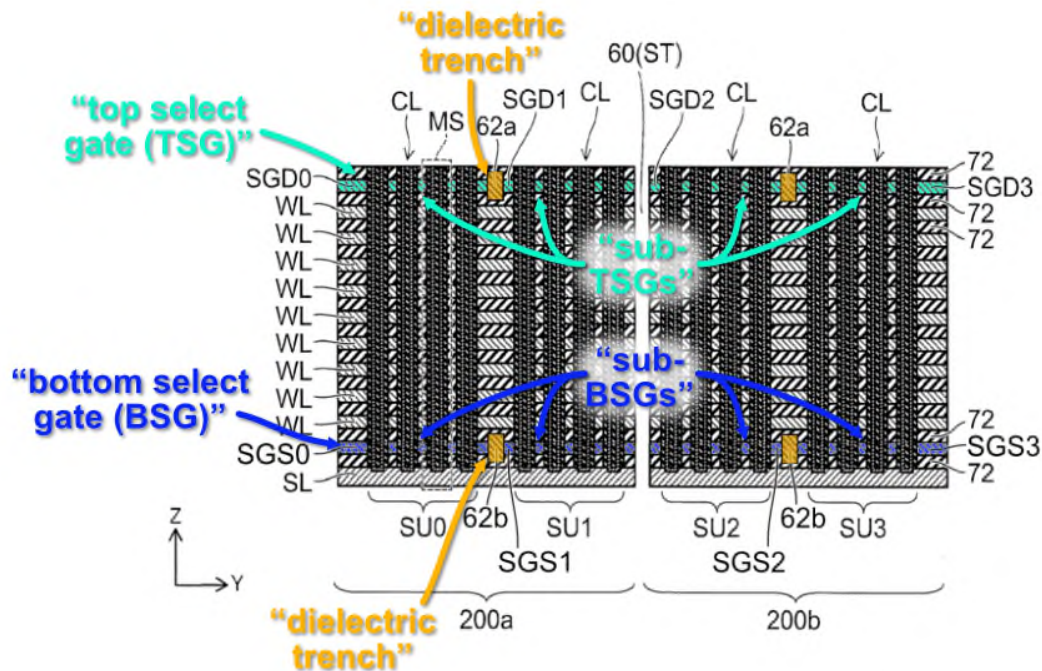


FIG. 11

Park, Fig. 11. Following these teachings when implementing Shibata results in what this limitation requires. Rather than multiple lower source-side select gate layers, Shibata would employ a single “*bottom select gate (BSG)*” (lower source-side select gate or SGS layer) with “*dielectric trenches*” (new additional separation portions 62b) “*separate[ing] the BSG*” into “*sub-BSGs*” (new layer portions SGS0-SGS3). As shown in the demonstrative figure below, these new

portions 62b would match the existing portions 62a in position and dimension to ensure that the select gates continue to allow for the independent control of the memory on the same unit-basis taught in Shibata:



See Lee, ¶¶ 381-384.

When the '623 patent was filed, a POSITA would have recognized that “[i]n order to reduce bit cost in 3D NAND cell, it is very important to increase the number of stacked cells.” Ex. 1006, 355. Relatedly, “increasing [the] number of stacked cells is the only reasonable way to reduce the effective memory cell size in 3D cells.” *Id.*, 357; see also Ex. 1007, 2 (“The basic idea behind 3D NAND is to ‘grow’ cells in the vertical dimension, thus reaching a higher density per area.”); Ex. 1012, 139 (“[t]o reduce the bit size, the number of stacked cells needs to go up”). But, when additional layers are added to a 3D NAND device, it becomes

more difficult to etch the hole in which the memory string channel structure will be formed. Ex. 1006, 387. Further, the increased channel length resulting from added layers results in reduced cell current and worse performance. *Id.*

This would have motivated application of Park's teachings to Shibata. Lee, ¶¶ 385-388. Because Shibata's multiple bottom select gate layers would be replaced with a single divided gate layer, the number of word lines could be increased without impacting the overall height of Shibata's stack. This would increase memory density without making it more difficult to etch the channel holes or impacting channel current. *Id.*, ¶¶ 389-390; *see also* Ex. 1008, [0002], [0066] (explaining that there is "continuous pressure to reduce component dimensions and fit more components in a given amount of chip area" and that one of the ways to meet this goal is to "reduce an amount of memory cell string selection circuitry").

A POSITA also would have been motivated to apply Park's teachings to Shibata because doing so would reduce the number of needed manufacturing steps. The embodiment shown in Figure 16 of Shibata employs three bottom select gates, separated by three layers of insulation. Following Park's teachings, these six layers would be replaced by just two: a single bottom select gate (separated by dielectric trenches) and a single layer of insulation. Lee, ¶¶ 391-392. Elimination of the other four layers would remove some steps from the manufacturing process, reducing manufacturing time and cost. *Id.* Moreover, controlling isolation for the

string units individually would have the added benefit of reducing the load on the drivers. *Id.*, ¶ 393.

Further, as shown by both Shibata and Park, it was well known that trenches of dielectric material could be used to divide select gates. Lee, ¶¶ 394-396. Numerous other references use trenches for the same purpose. *See, e.g.*, Ex. 1017, 7:40-42, Fig. 3 (employing a “cutting insulation pattern 118”); Ex. 1016, 6:5-15, Fig. 4A (employing a “insulating layer 173”); Ex. 1018, [0058], Fig. 4B (employing “insulating separation pattern 50”); Ex. 1019, [0158], Fig. 22 (employing “separation layer pattern 109”). Using this—as opposed to some other method—to separate Shibata’s bottom select gate into multiple portions would have been considered nothing more than routine design choice. Lee, ¶ 396. Indeed, Shibata already forms trenches in the top select gate. *Id.*

A POSITA would have had a reasonable expectation of success in applying Park’s teachings to Shibata. Shibata already employs and is open to use of dielectric trenches to separate select gate layers. A POSITA would have considered use of this same approach to separate its bottom select gate to be nothing more than an obvious extension of an approach Shibata already employs. Lee, ¶¶ 397-398. Moreover, Park would have confirmed to a POSITA that this approach could be successfully used to divide not only a memory device’s top select gate, but also its bottom select gate. *Id.*, ¶ 399.

[1.F] “one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.”

Shibata teaches that its memory device includes “an interconnect portion LI of a conductive material” within “separation portion 60 (a slit ST)” that contacts an “active region 10a of the substrate 10.” Shibata, [0065]. This “interconnect portion LI” in the “separation portion 60”—the claimed “*common source regions formed over the substrate*”—is annotated purple in Figure 23 below. As shown, it passes through Shibata’s “*BSG*” (blue), the “*word lines*” (red), the intervening “*insulating layers*” (green), and the “*TSG*” (light blue):

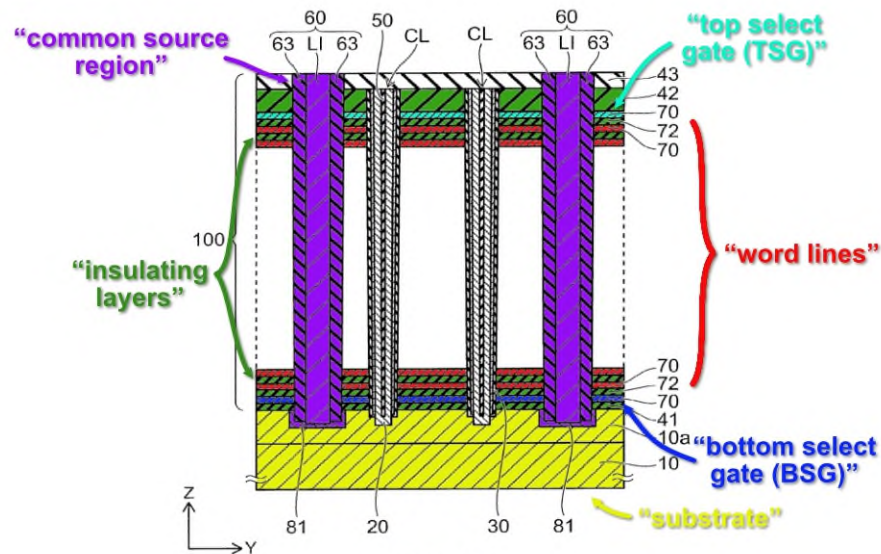


FIG. 23

*Id.*, Fig. 23. Figure 16 similarly shows the common source region in slit 60 passing through the device’s layers:

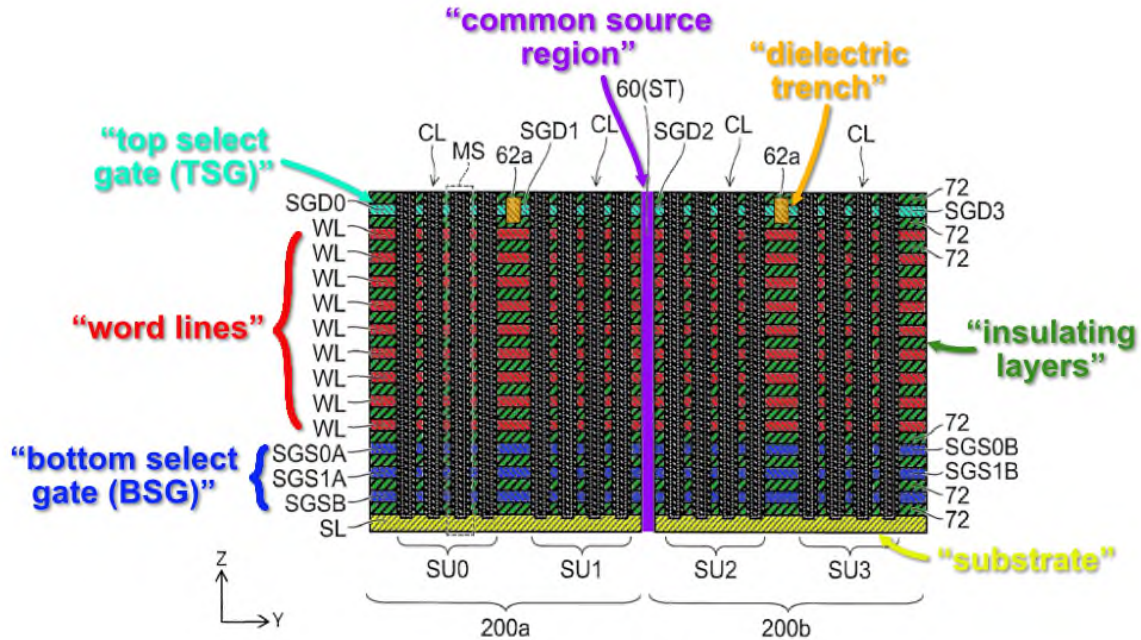


FIG. 16

*Id.*, Fig. 16.

Shibata also teaches that its “separation portion 62a ... extend[s] in the same direction as the separation portions 60 (the slits ST)....” Shibata, [0166]. Thus, as shown in Figure 47A, the “*common source region*” (purple) “*extend[s]*” in the same “*length direction*” as the “*dielectric trench[es]*” (orange):

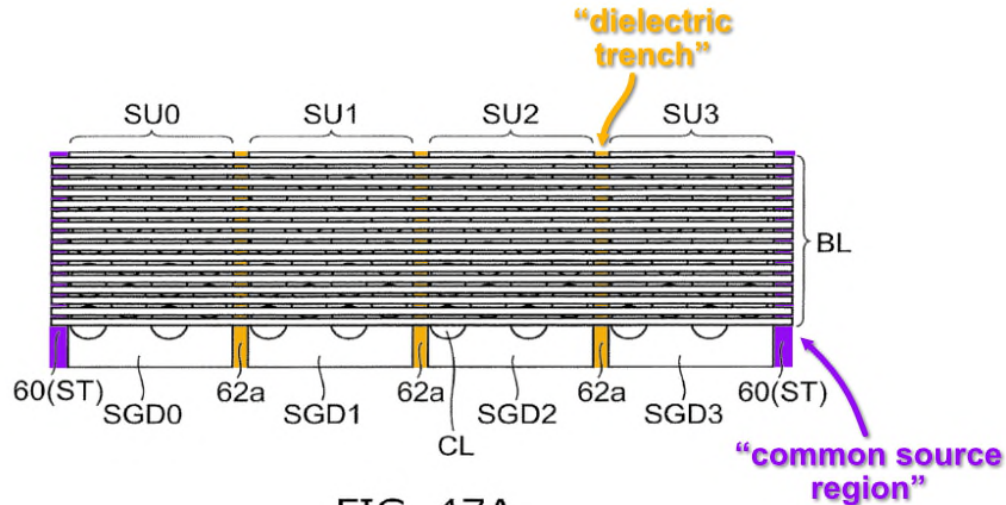


FIG. 47A

*Id.*, Fig. 47A; Lee, ¶¶ 400-406.

## 2. Claim 2

Claim 2 depends on claim 1 and further requires:

[2.A] “a top select gate (TSG) positioned over the plurality of word lines, the TSG and the plurality of word lines being spaced apart by the plurality of insulating layers; and”

The “uppermost layer” of Shibata’s “multiple conductive layers 70 functions as ... a drain-side select gate....” Shibata, [0074]. This is the claimed “*top select gate (TSG)*.” Lee, ¶¶ 407-409. Further, in Shibata, “insulating layers 72” are “interposed” between all conductive layers. Shibata, [0061]. Thus, Shibata’s “*TSG*” (the drain-side select gate, light blue) is “*spaced apart*” from its “*word lines*” (red) by a “*plurality of insulating layers*” (green):

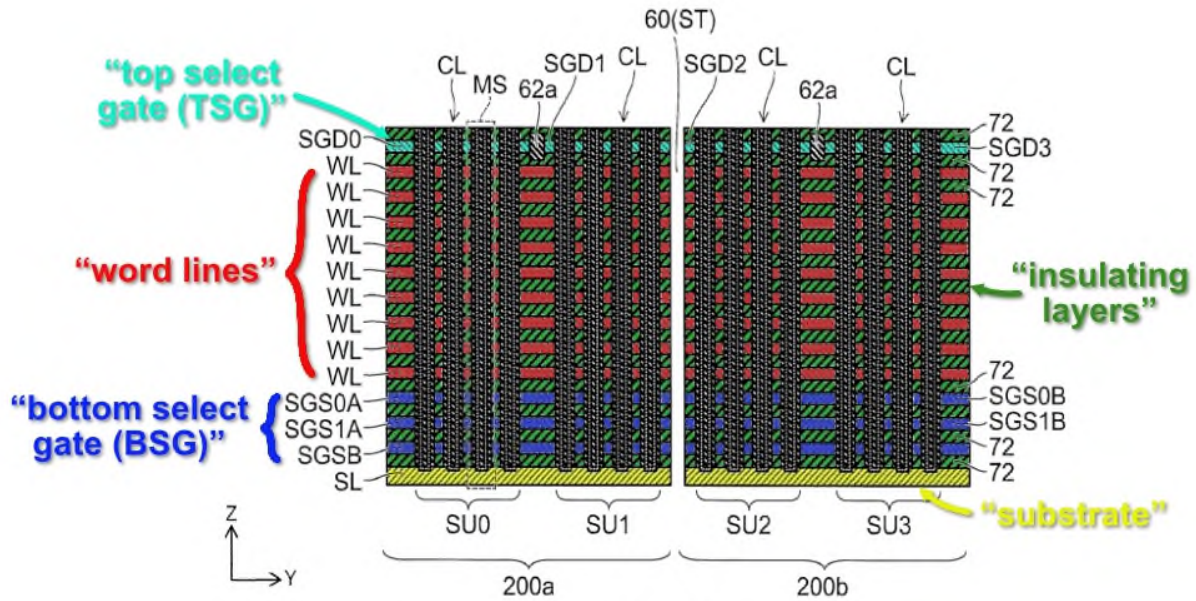


FIG. 16

*Id.*, Fig. 16; Lee, ¶¶ 410-411.

[2.B] “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.”

As explained, Shibata includes “*one or more second dielectric trenches*” (separation portions 62a) that separate its “*TSG*” (the upper drain-side select gate) into “*sub-TSGs*” (portions SGD0-SDG3):

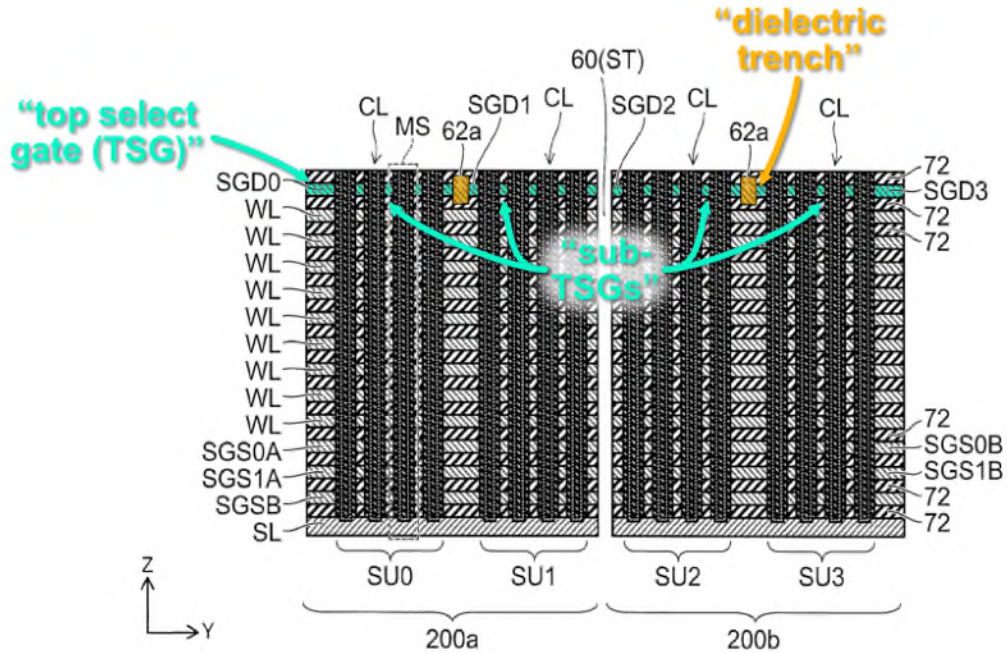


FIG. 16

Shibata, Fig. 16; *supra* discussion of limitation [1.E]; Lee, ¶¶ 412-413.

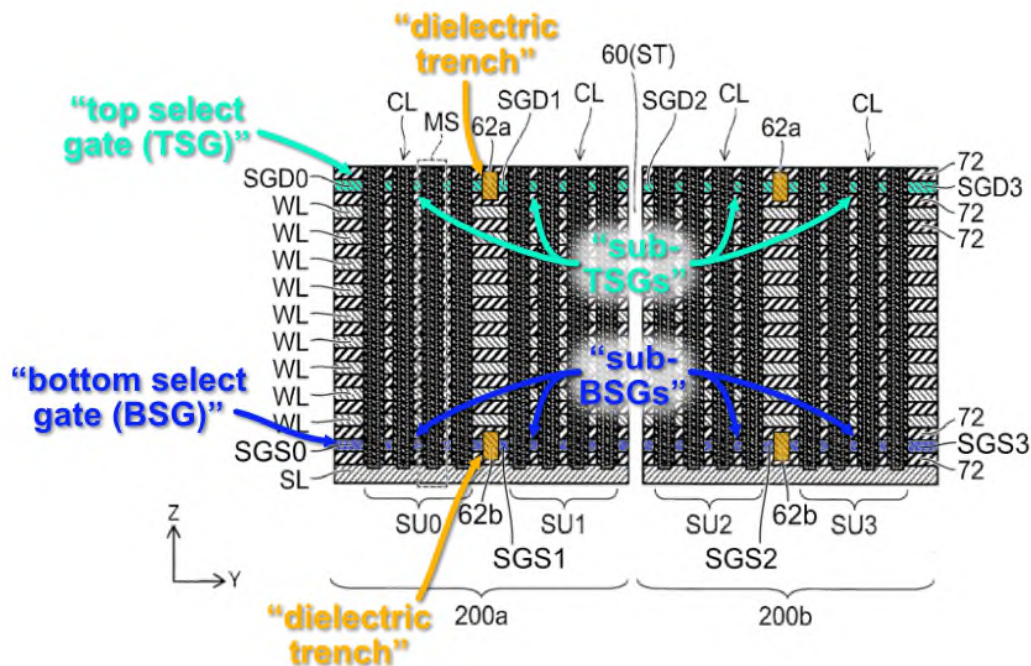
### 3. Claim 3

Claim 3 depends on claim 2 and further requires that:

**[3] “the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate.”**

This is taught by Shibata and Park. Shibata divides its memory blocks into “string units.” Shibata, [0145]; [0194]. To allow for this, Shibata’s top and bottom select gates are structured such that they can be “controlled electrically independently” on a string unit basis. *See id.*, [0167], [0192]-[0200], [0227]. In Figure 16, “separation portion[s] 62a”—located between string units SU0-SU3—divide Shibata’s top select gate. *Id.*, [0166], [0168]-[0171]; Fig. 16. Park similarly positions “isolation insulating layers 111” dividing its lower GSL layer between its

individually controllable “unit areas.” Park, 5:67-6:15. As discussed in connection with claim 1, the device of Shibata and Park would include upper and lower trenches with the same physical extent to allow Shibata’s memory string units to continue to be independently controlled. *See supra* discussion of claim 1. Given this, a POSITA would have understood that the “*first*” and “*second dielectric trench[es]*” (Shibata’s existing separation portions and additional separation portions applied following Park) respectively dividing Shibata’s top and bottom select gates would be located between the individually controllable string units SU0-SU3 such that they are “*aligned*.” *See* Lee, ¶¶ 414-420. As shown in the demonstrative below, locating the trenches in this way would allow Shibata’s memory to continue to be controlled on a string unit basis:



*Id.*, ¶ 421.

#### 4. Claim 4

Claim 4 depends on claim 2 and further requires that:

[4] “the one or more common source regions further pass through the TSG, and the one or more common source regions, the first dielectric trenches, and the second dielectric trenches extend parallel to each other in the length direction of the substrate.”

Shibata includes “*one or more common source regions*” (an interconnect portion LI within separation portion 60 / slit ST). *See supra* discussion of limitation [1.F]. This “*common source region*” (purple) passes through Shibata’s “*TSG*” (light blue):

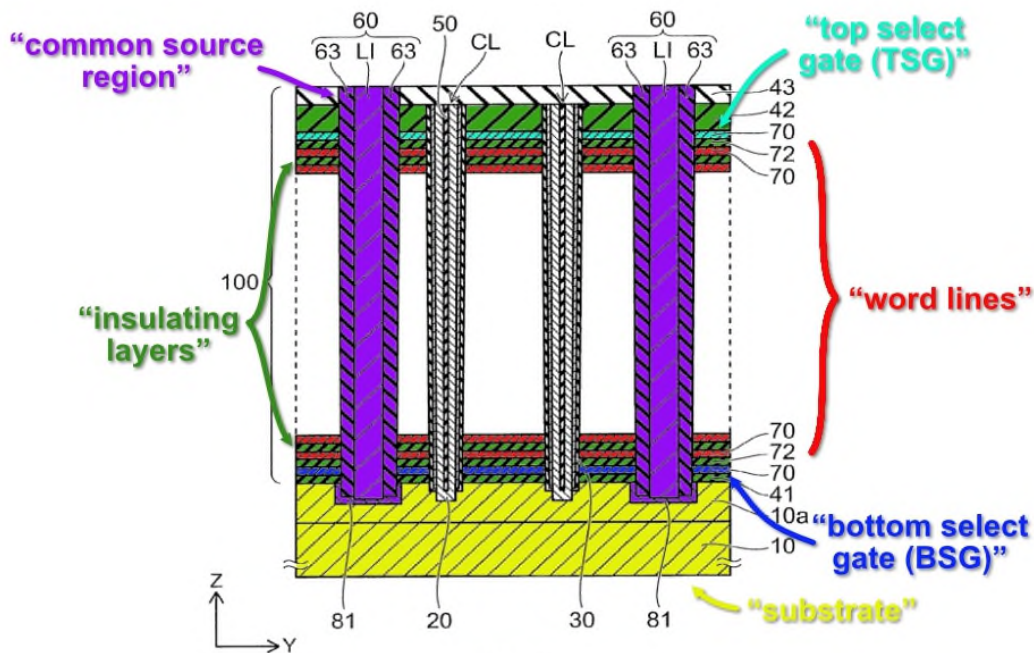


FIG. 23

Shibata, Fig. 23.

Shibata’s “*common source regions*” also “*extend parallel to*” the “*first dielectric trenches, and the second dielectric trenches*” “*in the length direction*

*of the substrate.*” Per Shibata, the “separation portion[s] ... extend[] in the same direction as the separation portions 60 (the slits ST)...” Shibata, [0166]. This is shown in Figure 47A: the “*common source region*” (purple) “*extend[s]*” in the same “*length direction*” as the “*dielectric trench*” (orange). Because both the “*first*” and “*second*” “*dielectric trenches*” are obviously located between the same string units, a POSITA would have understood that they both extend in the same direction:

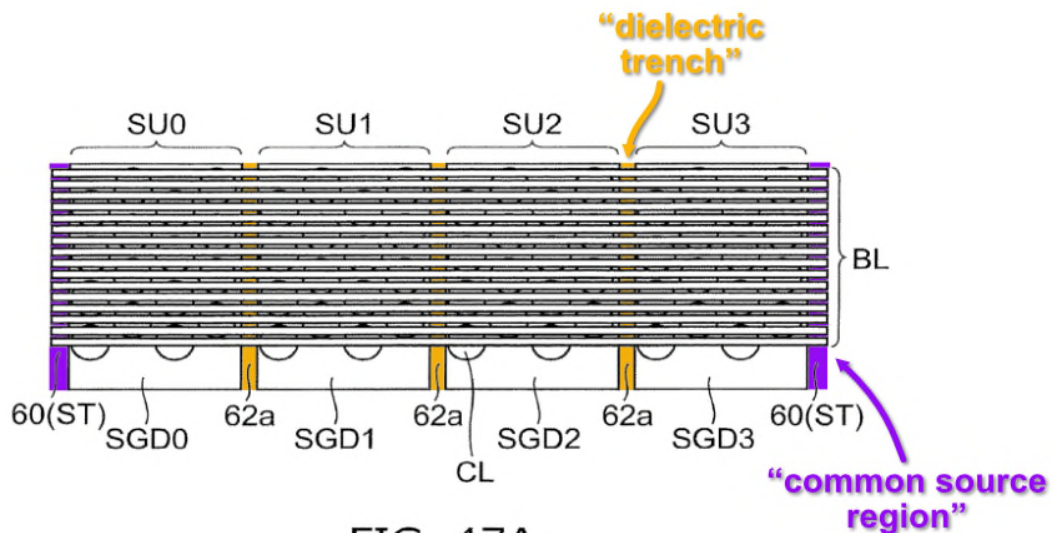


FIG. 47A

*Id.*, Fig. 47A; Lee, ¶¶ 422-429.

## 5. Claim 5

Claim 5 depends on claim 2 and further requires:

**[5] “a plurality of channel structures formed over the substrate along a height direction of the substrate that is perpendicular to the substrate, wherein each of the plurality of channel structure passes through the BSG, the plurality of word lines, the TSG, and the plurality of insulating layers.”**

Shibata’s “memory device” includes “memory strings” with “memory cells” arranged in “series in a first direction.” Shibata, [0048]. Each memory string includes an associated “columnar portion[] CL.” *Id.*, [0055]. “The columnar portions CL pierce the stacked body 100 and reach the source layer SL” on the substrate. *Id.* [0059]; [0075].

Figure 16—annotated below—shows this. A “*plurality of channel structures*” (channel structures CL, with one pink) are “*over the substrate along a*” “*perpendicular*” “*height direction of the substrate*” (the CL extend vertically in the Z-axis direction from substrate, yellow). These “*channel structures*” “*pass[] through the BSG*” (the lower SGS layers, blue), “*the plurality of word lines*” (the WL layers, red), “*the TSG*” (the upper SDG layer, light blue), “*and the plurality of insulating layers*” (green):

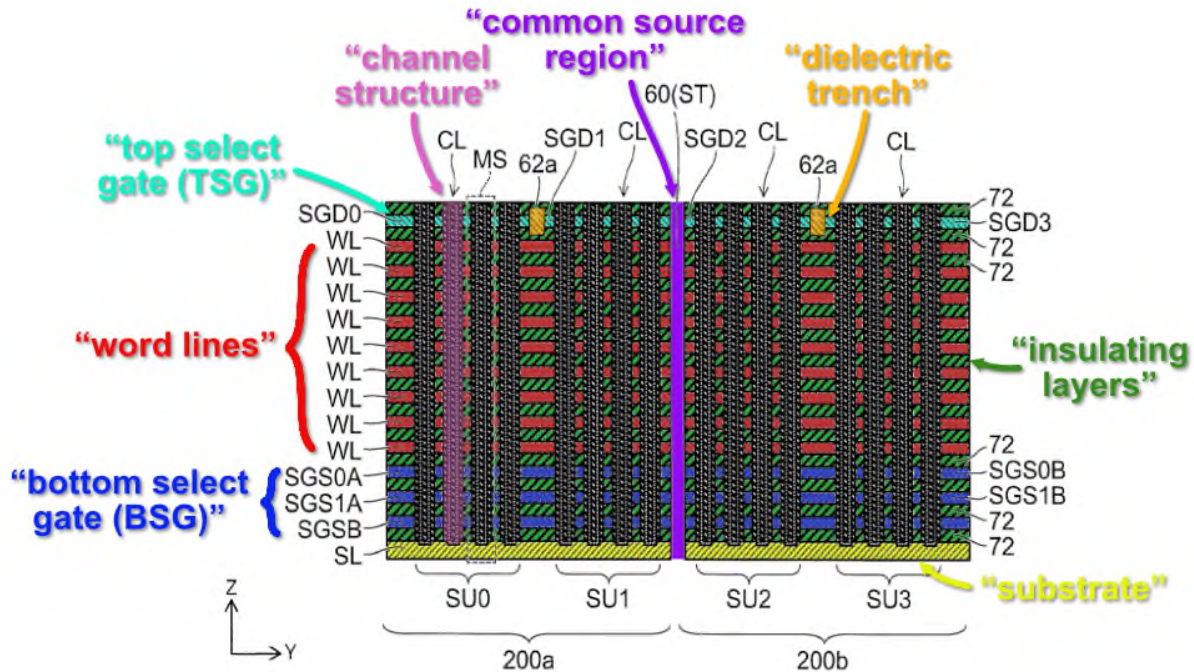


FIG. 16

Shibata, Fig. 16; Lee, ¶¶ 430-436.

## 6. Claim 6

Claim 6 depends on claim 1 and further requires:

[6] “a plurality of dummy channel structures formed along the a height direction of the substrate that is perpendicular to the substrate, the plurality of dummy channel structures passing through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate.”

Shibata’s memory device includes “memory strings” with “memory cells” arranged along “columnar portions CL.” Shibata, [0048], [0055]. While Shibata’s focus is not on its memory’s staircase and the dummy columns typically present here, a POSITA would nonetheless have considered it obvious that these would be present. *See* Lee, ¶¶ 437-443. Park explains that 3D NAND routinely includes a multitude of “dummy channel structures” to “secure stability” of the

memory device when sacrificial layers are removed, and that both dummy and cell channels can have “similar” “structure[s].” Park, 5:30-45, 11:19-21. Further, this type of dummy support structure was routinely present. Ex. 1023, 5:64-6:2. A POSITA would have understood that Shibata’s memory also requires support in its staircase region when its sacrificial layers are removed (*see* Shibata, [0103]-[0105], [0113]), and thus also obviously includes the claimed “*dummy channel structures*”—like those in Park—passing through its layers. *See* Lee, ¶ 443.

## 7. Claim 7

Claim 7 depends on claim 5 and further requires:

**[7] “a plurality of memory cell sub-blocks, each of the memory cell sub-blocks including a plurality of respective channel structures that are connected to a same sub-BSG and to a same sub-TSG, each of the memory cell sub-blocks being operated individually.”**

The “block[s]” of Shibata’s memory can be further divided into multiple separate “string units” such as “SU0, SU1, and SU2.” Shibata, [0079]. And each “string unit includes multiple memory strings MS” with associated “columnar portions CL.” *Id.* Further, as explained, Shibata divides its select gates with “separation portions” to allow the string units to be “controlled electrically independently.” *Id.*, [0083], [0129], [0167], [0227], [0270]; *supra* discussion of limitations [1.B], [1.E].

Shibata’s string units are the claimed “*memory cell sub-blocks.*” Each string unit includes “*a plurality of respective channel structures*” (structures CL)

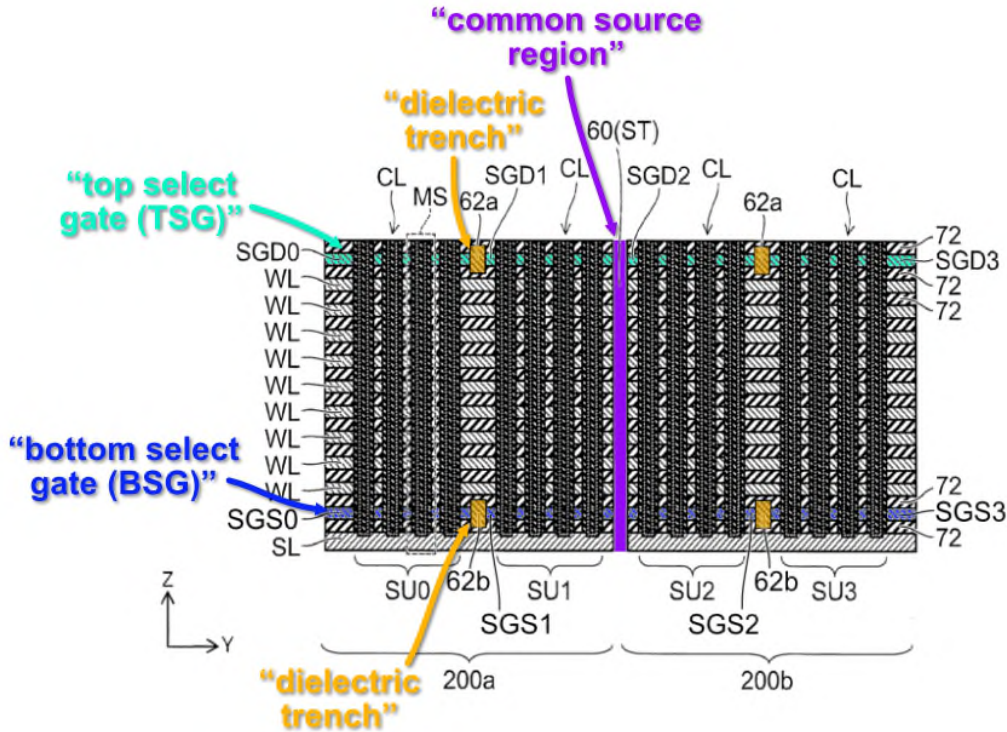
that are “*connected to a same sub-BSG*” (portions of the lower select gate) and “*to a same sub-TSG*” (portions of the upper select gate) such that they can be “*operated individually.*” Lee, ¶¶ 444-450.

## 8. Claim 8

Claim 8 depends on claim 5 and further requires that:

[8] “the one or more first dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate.”

Shibata’s upper “*dielectric trenches*” (separation portions 62a, orange) are “*alternatively disposed in the width direction*” (the Y-axis direction) with the “*common source regions*” (purple). Again, as explained when discussing claim 3, a POSITA would have understood that the “*first dielectric trenches*” added to Shibata when following Park’s teachings would be located below the upper trenches and such that they are also “*alternatively disposed*” with the common source regions. This is shown in the below demonstrative:



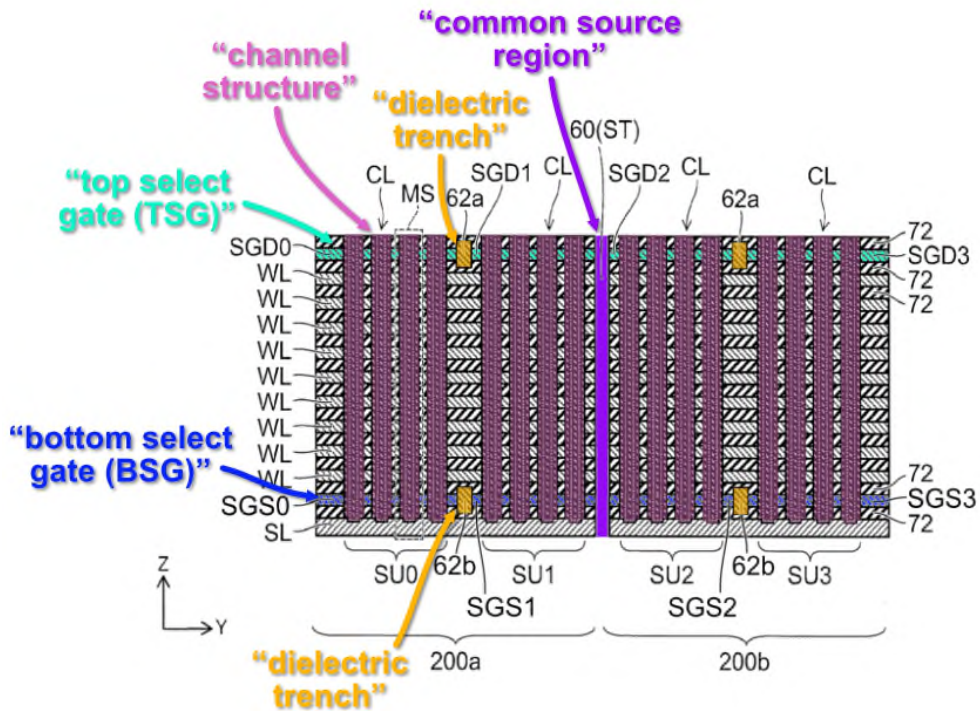
See Lee, ¶¶ 451-453.

## 9. Claim 9

Claim 9 depends on claim 5 and further requires that:

[9] “the one or more second dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate so that a plurality of channel structures are disposed therebetween.”

As shown in the demonstrative below applying Park’s lower trenches to Shibata, Shibata’s “*dielectric trenches*” (the separation portions, orange) are “*alternatively disposed in the width direction*” with the “*common source regions*” (purple). (See *supra* discussion of claim 8). Further, each of Shibata’s string units SU0-SU3 includes multiple “*channel structures*” (structure CL, pink) located between the “*dielectric trenches*” and “*common source regions*”:



Lee, ¶¶ 454-457.

## 10. Claim 10

Claim 10 depends on claim 1 and further requires:

[10] “one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.”

According to Shibata, “a dummy word line may be provided between the drain-side select gate and the word lines and/or between the source-side select gate and the word lines.” Shibata, [0457]. In the ’623 patent, “bottom dummy word lines” are the same as “dummy BSGs.” Ex. 1001, 6:44-48. Thus, Shibata includes “one or more dummy BSGs” that are “formed between the plurality of word lines

*and the BSG*”: “dummy word lines” are located between Shibata’s select gate layer and word lines. *See* Lee, ¶¶ 458-462.

A POSITA also would have considered it obvious that when Park’s teachings are applied to Shibata, Shibata’s lower “*dielectric trench*” (the separation portions 62b) would “*separate*” not only its “*BSG*” (the lower select gate layer), but also its “*dummy BSG*” (the dummy line adjacent to the select gate layer). While Shibata explains that its word lines are “provided commonly” across the string units (Shibata, [0165]), it divides the select gate layers on a string unit basis (*see id.*, [0083], [0129], [0167], [0227], [0270]). Shibata places its dummies adjacent to and associates them with its select gates. *Id.*, [0457]. Given this, a POSITA would have understood that they would be—or at the very least obviously could be—structured and divided in the same way as the select gates themselves. *See* Lee, ¶¶ 463-466.

Next, Shibata teaches a range of different separation portion structures. For instance, “separation portion 62a” in Figure 16 passes through a single gate layer. *See* Shibata, Fig. 16. Figure 3 employs two separation portions 62a and 62b separating adjacent select gate layers. *See id.*, Fig. 3. Another “separation portion 60” in Figure 3 is structured such that it passes through all of the conductive layers. *See id.* A POSITA would have considered use of all these known design alternatives when implementing Shibata. Lee, ¶¶ 467-469; *supra* Section IX.A.10.

In view of these various known options, a POSITA would have considered it highly obvious that both Shibata's bottom select gate layer and the adjacent dummy layer would be divided by the same dielectric trench. *See* Lee, ¶ 470.

## 11. Claim 11

Claim 11 depends on claim 2 and further requires:

**[11] “one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs, and spaced apart from the plurality of the word lines and the TSG by the plurality of insulating layers.”**

As explained when discussing claim 10, Shibata teaches that its memory device can include “dummy ... line[s]” between its “drain-side select gate and the word lines.” Shibata, [0457]. These dummy lines are the claimed “*dummy TSGs*.” *See* Lee, ¶¶ 471-474. Moreover, a POSITA would have considered it obvious for Shibata's “second dielectric trenches” to pass through not only its “*TSG*” (the select gate) but also its “*dummy TSGs*” (the dummy lines) for the same reasons explained in connection with claim 10. *See id.*, ¶¶ 475-477; *supra* Section IX.A.11.

## D. Secondary Considerations

There is no evidence in the '623 patent's prosecution history of any pertinent secondary considerations of nonobviousness.

**X. Conclusion**

For the foregoing reasons, Petitioner respectfully requests institution of IPR and cancellation of claims 1-11.

Respectfully submitted,

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Dated: April 12, 2024

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**CERTIFICATE OF COMPLIANCE**

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,970 words.

Dated: April 12, 2024

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**CERTIFICATE OF SERVICE**

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on April 11, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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