

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00794
U.S. Patent No. 10,950,623
Issue Date: March 16, 2021

Title: 3D NAND MEMORY DEVICE AND METHOD
OF FORMING THE SAME

DECLARATION OF DR. JACK C. LEE

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in the claims of U.S. Patent No. 10,950,623, which I refer to herein as the ’623 patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My curriculum vitae (“CV”) is attached hereto as Ex. 1022 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other things, 3D NAND technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the

Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

11. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and 3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

12. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

13. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

14. I have been asked to provide analysis and explain the subject matter of the '623 patent, including the state of the art when the application underlying the '623 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '623 patent including how that art relates to the challenged claims of the '623 patent and to provide my opinions regarding whether that art invalidates the claimed subject matter.

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15. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the claims of the '623 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

16. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '623 patent.

17. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the '623 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1004	U.S. Patent No. 10,559,583 B2 to Park et al. ("Park")
1005	U.S. Patent Publ. No. 2019/0122734 A1 to Shibata et al. ("Shibata")
1006	Aritome, "NAND Flash Memory Technologies" (2016)
1007	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1008	U.S. Patent Publ. No. 2015/0162084 A1 to Morooka et al.

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Exhibit	Description
1009	U.S. Patent Publ. No. 2015/0255478 A1 to Tanzawa
1010	U.S. Patent No. 9,589,978 to Yip
1011	U.S. Patent Publ. No. 2017/0062337 A1 to Park et al.
1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1015	File History of U.S. Patent No. 11,430,811 (Appl. No. 17/154,054) to Song et al.
1016	U.S. Patent No. 10,355,010 B2 to You et al.
1017	U.S. Patent No. 9,299,718 B2 to Park et al.
1018	U.S. Patent Publ. No. 2019/0035798 A1 to Hwang et al.
1019	U.S. Patent Publ. No. 2015/0137216 A1 to Lee et al.
1021	U.S. Patent Pub. 2019/0214404 A1 to Ahn et al.
1023	U.S. Patent No. 8,945,996 to Tang et al.

IV. UNDERSTANDING OF THE LAW

18. I am not an attorney, but have been instructed in and applied the law as described in this section.

19. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the claims of the alleged invention in Section V below.

20. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

21. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

22. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

23. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

24. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

25. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

26. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield

predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

27. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

28. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

29. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

30. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial

expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

31. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention.

32. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

33. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

34. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

35. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have

been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

36. In my opinion, a POSITA in the field of the '623 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

37. In my opinion, this POSITA would also have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled.

38. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of December 2018. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGICAL BACKGROUND

39. Before addressing the '623 patent in detail, some background on the technology of the '623 patent should be considered.

40. The '623 patent and the prior art discussed in this petition relate generally to NAND flash memory.

41. “Flash memory” is a form of “non-volatile memory.” Ex. 1010, 1:24-26. “Non-volatile memory is memory that can retain its data values for some extended period without the application of power.” *Id.*, 1:26-28. Two common types of flash memory array architectures are the NAND and NOR architectures. NAND offers a higher integration density and occupies a larger market than NOR flash.

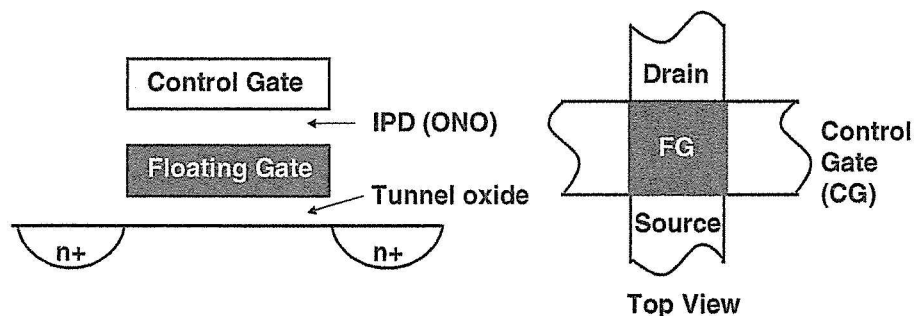
42. NAND flash was first developed in 1987. *See* Ex. 1006, 22.

43. NAND flash stores data in a memory “cell” formed from a single transistor that is the logical equivalent of a NOT AND circuit. Ex. 1006, 38-39.

44. In one known type of NAND flash, the memory cell is formed from a “Nch MOS transistor with [a] poly-silicon floating gate (FG).” Ex. 1006, 38-39. The FG is electrically isolated by the surrounding insulating layer, hence the name, “floating” gate and electrons placed on the floating gate are trapped. In other words, “charge is stored in [the] FG” and the “potential of [the] FG is controlled by [a] control gate (CG) voltage with capacitive coupling between [the] CG and FG.” *Id.* When negative-charge electrons are stored in the FG, these trapped charges push electrons away from the surface of the substrate (the channel) due to coulombic force. The CG would have to be applied a higher voltage to attract electrons back to the channel in order to turn on the transistor. This means that a negative-charged FG

causes an increase in the threshold voltage (e.g., to V_{T0}), in comparison to the threshold voltage of an uncharged FG (V_{T1}). Therefore, by sensing the transistor current by applying a voltage (V_{READ}) on the CG where $V_{T1} < V_{\text{READ}} < V_{T0}$, one can determine whether the FG is charged (i.e., the cell is of bit “0”) or uncharged (bit “1”). This is essentially the *reading* operation of a NAND flash cell. To *program* (or *write*) a NAND flash memory cell, a high voltage (V_{pgm}) is applied to the CG while keeping substrate/source/drain at 0V. “Electrons are injected to the floating gate (FG)” by “a tunneling mechanism through the tunnel oxide” *Id.* at 44. The threshold voltage of the memory cell would increase from V_{T1} to V_{T0} . “An erase operation is performed by applying high-voltage (V_{era}) to substrate...while keeping CG at 0V” *Id.* Electrons in the FG are ejected to the substrate through the tunnel oxide.

45. The below figure provides an example of a flash memory cell:



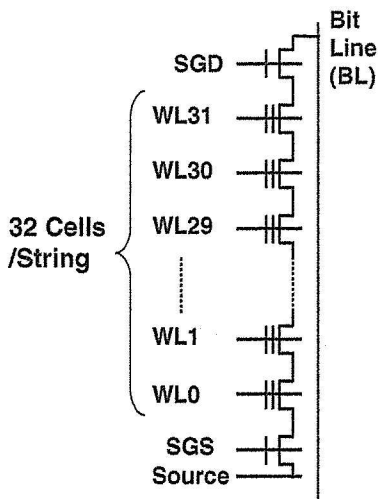
Ex. 1006, 39.

46. Other NAND flash employ a transistor with a “charge trap” layer. *See* Ex. 1012, 109. In this type of transistor, charge is stored in “non-conducting dielectric layer”—like silicon nitride—instead of a floating gate. *See id.*

47. NAND flash memory cells are arranged in so-called “strings” with multiple cells “connected in series.” Ex. 1006, 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a string consists of 32 to 128 NAND cells.

48. Each end of a string is terminated with a “select transistor.” One is often called the “SGD” (drain-end select gate transistor) and the other one is often called “SGS” (source-end select gate transistor). The “SGD connects” at the string’s drain side “to isolate it from the bit line (BL).” Ex. 1006, 38. Hence, the SGD is also known as the “bit line select transistor” or the “upper select gate.” The “SGS connects at” the string’s source side “to isolate it from a source line (SL).” *Id.* Since the source line is commonly connected to the ground terminal, SGS is also known as the “ground select transistor” or the “lower select gate.” Word lines are connected to each memory cell control gate. *Id.*, 38-39.

49. An example of one such string is shown below:



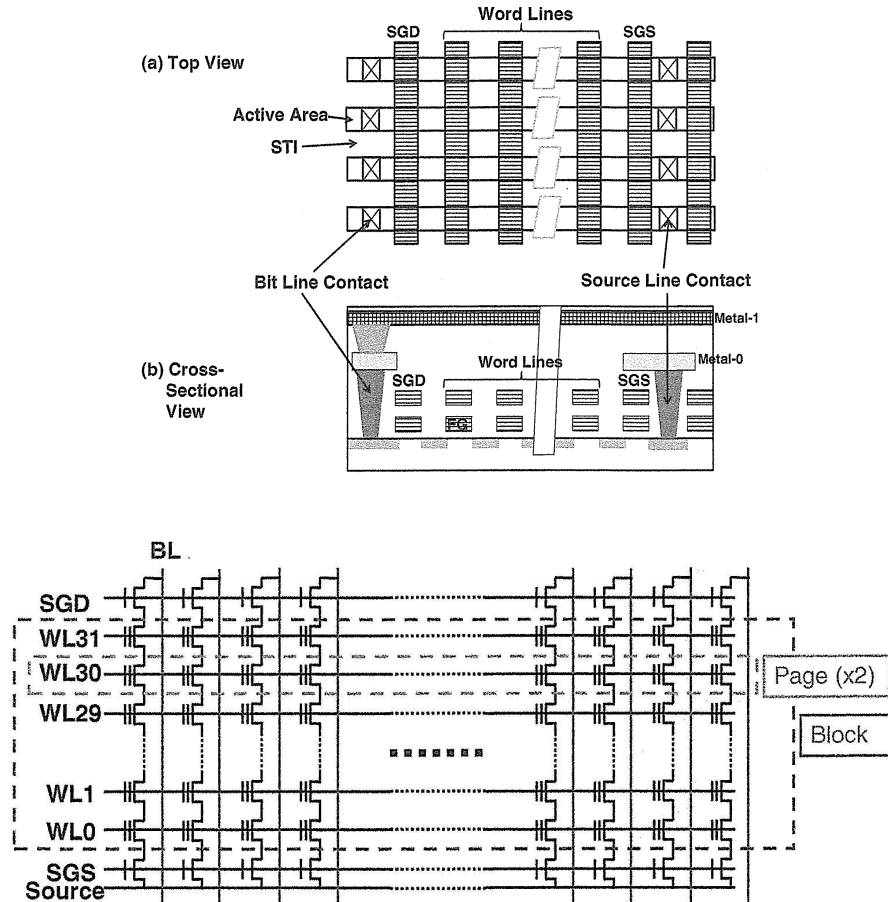
Ex. 1006, 39.

50. Early NAND flash devices were formed as two-dimensional arrays on a substrate surface.

51. Here, the “memory array is formed by straight active area lines ... and straight gate lines” located on a substrate surface. Ex. 1006, 38. Memory cells are located at the “intersection[s]” of the lines. *Id.*

52. An example of a two-dimensional NAND flash memory array is shown below. Figures (a) and (b) illustrate the top view and the cross-sectional view of the memory array, respectively. The third figure shows the circuit schematic drawing of the memory array.

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Ex. 1006, 40.

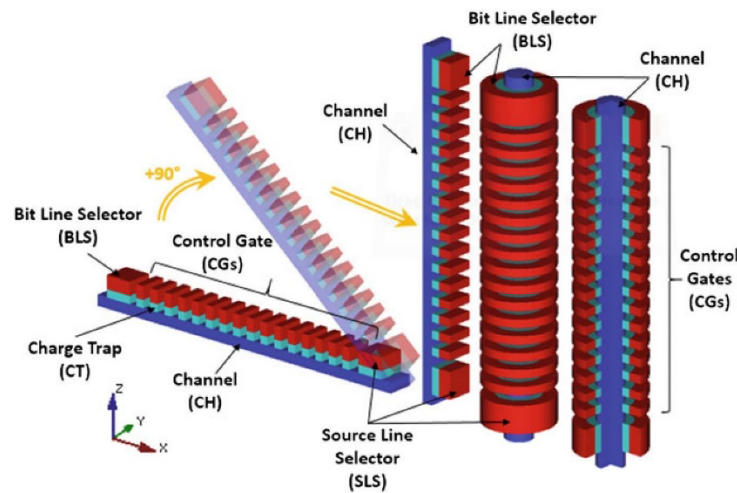
53. As also shown, the cells are grouped into “page[s]” extending along the word lines and “block[s]” which include all the pages along the bit lines, excluding the SGD and the SGS select transistors *Id.* “[R]ead and program operations are performed per page” while “the erase operation is performed per block.” Ex. 1006, 39. For example, to *read* a selected group of cells, e.g., all the memory cells on the page along WL30 in the circuit schematic above, the voltage on the CG (WL30) is pulled up to V_{READ} while all other word lines (unselected cells) are pulled up above V_{T0} . This way all “the unselected cells act as pass transistors.” *Id.*, 45. A string is

selected by a bit line and the drain-end select gate transistor (SGD). The string of memory cells along a bit line would conduct if the selected cell is programmed to bit “1”, i.e. uncharged FG. The *program* operation of the NAND flash is similar to the read operation, except a higher voltage (V_{pgm}) is used on the selected page. The *erase* operation is performed in the entire block consisting of multiple pages. “The word[]lines of the selected blocks are grounded” (*id.*, 48) while high erase voltage (V_{era}) is applied to the p-well (i.e., the “substrate” in the memory cell area). This causes extraction of electrons from the FG into the p-well via tunneling mechanism. All the memory cells in the block are then set to bit “1.” Since the block size is the minimum granularity of erase operation, reducing the block size could reduce the system burden of the data management and thereby improve system performance.

54. To boost data storage densities and reduce cost per gigabit, the art developed so-called “three-dimensional (3D) NAND flash cells” starting in about 2006. Ex. 1006, 292.

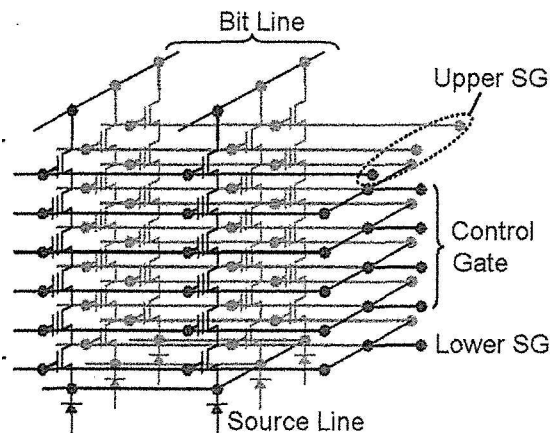
55. In 3D NAND, rather than arranging memory cells in a two-dimensional array, 3D NAND arranges cells in a three-dimensional array that is built up in layers. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1007, 3.

56. The following image provides an example:



Ex. 1012, 122.

57. Multiple of such vertical channels are then repeated in a three-dimensional array:



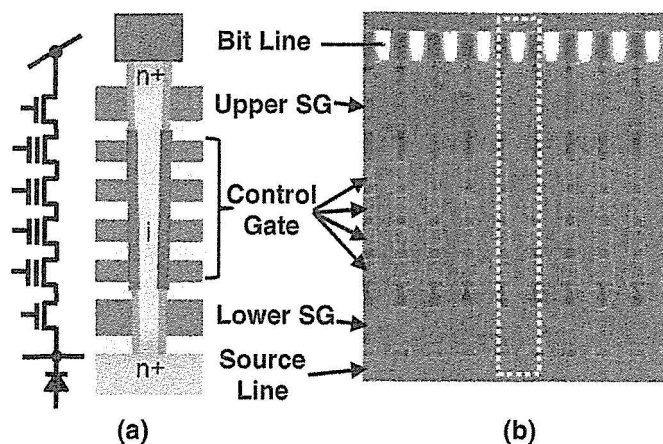
Ex. 1006, 296.

58. 3D NAND includes “multi-stacked layers of gate (plate)” material alternated with “dielectric” “deposited” in a “[s]tack.” Ex. 1006, 294. The flash memory device offers the industry’s highest layer count and the highest areal density

(bits per unit area). A “through-hole is fabricated through” the layers and is “filled by memory film ... and channel poly-Si” to form a string of vertically arranged memory cells. *Id.*, 295. “Each” layer of “electrode plate acts as a control gate except the lowest plate,” which “function[s] as the lower select gate (lower SG)”, i.e., SGS, the source-end select gate transistor. *Id.*

59. “A single bit” of memory cell “is located” at “the intersection of a control gate plate” and the memory film/poly-Si channel. Ex. 1006, 295.

60. An example 3D NAND vertical memory cell string is shown below:

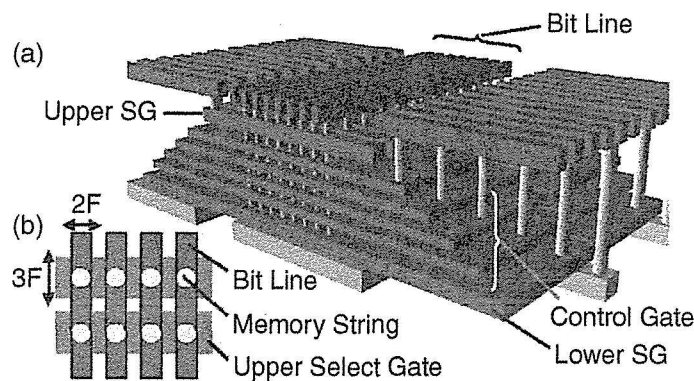


Ex. 1006, 296.

61. For purposes of programming the cells in a memory string, the “string is selected by a bit line and an upper select gate (SG).” Ex. 1006, 295.

62. “[T]he control gates and upper/lower SG are connected” to the memory’s conductive “layers at [a] stair-like gate structure” located outside the memory array. Ex. 1006, 297. The stair-like (terrace) structure is created to expose

and allow connection to each conductive layer via vertical word line contacts. The conductive layers are insulated from each other by insulating materials, also known as “dielectrics.” The dielectric layers serve the purposes of preventing interference of electrical signals from one conductive layer to other layers and providing structural support so that the conductive structures do not collapse. An example of this is shown below:



Id. at 296.

63. “The bottom of” each “memory string is connected to the common source diffusion formed on the silicon substrate.” Ex. 1006, 297.

64. “Production of 3D NAND flash memory ... started in August 2013.”
Ex. 1006, 393.

VII. THE '623 PATENT

A. Effective Filing Date

65. I understand that the application leading to the '623 patent was filed on March 27, 2019.

66. Based on my review of the '623 patent, I note that it also references a PCT application on its face, which was filed December 7, 2018.

67. For purposes of this declaration, I have been instructed to use December 7, 2018 as the effective filing date of the '623 patent. My opinions in this declaration were formed from the perspective of a POSITA as of December 7, 2018, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

B. Overview

68. The '623 patent relates to a “3D NAND memory device.” Ex. 1001, 1:33-36.

69. According to the patent, in existing devices, “memory cell strings of the same block can share a bottom select gate (BSG).” Ex. 1001, 1:51-52. “The shared BSG accordingly controls” all the “bottom select transistors (BSTs)” “of the vertical NAND memory cell strings in that block simultaneously during” operation. *Id.*, 1:40-41, 1:53-58.

70. This is a problem, according to the patent, because “the shared BSG can induce longer erasing time, longer data transfer time, and lower storage efficiency.” Ex. 1001, 1:58-60.

71. The patent purports to address this by employing a “divided block structure.” Ex. 1001, 1:33-36.

72. “[E]ach of the blocks can be separated into a plurality of sub-blocks by dividing the shared BSG into a plurality of sub-BSGs” using “one or more first dielectric trenches.” Ex. 1001, 1:61-64.

73. This in turn allows the “sub-blocks” to be “operated individually through controlling the respective sub-BSG.” Ex. 1001, 1:64-67.

74. The patent similarly explains that “a shared/common TSG” (TSG stands for top select gate) can also be “divid[ed]” by “second dielectric trenches” into “sub-TSGs” that can also be independently controlled. Ex. 1001, 2:8-13.

75. Figure 1A, which is reproduced in annotated form below, provides an example. All color has been added to this figure (and the other patent figures reproduced throughout this declaration).

76. Here, the depicted “memory device 100”—like all 3D NAND devices—includes a BSG 62p (dark blue), a TSG 62a (light blue), and multiple “word lines” separated by “insulating layers” stacked over a “substrate 10.” Ex. 1001, 6:44-54.

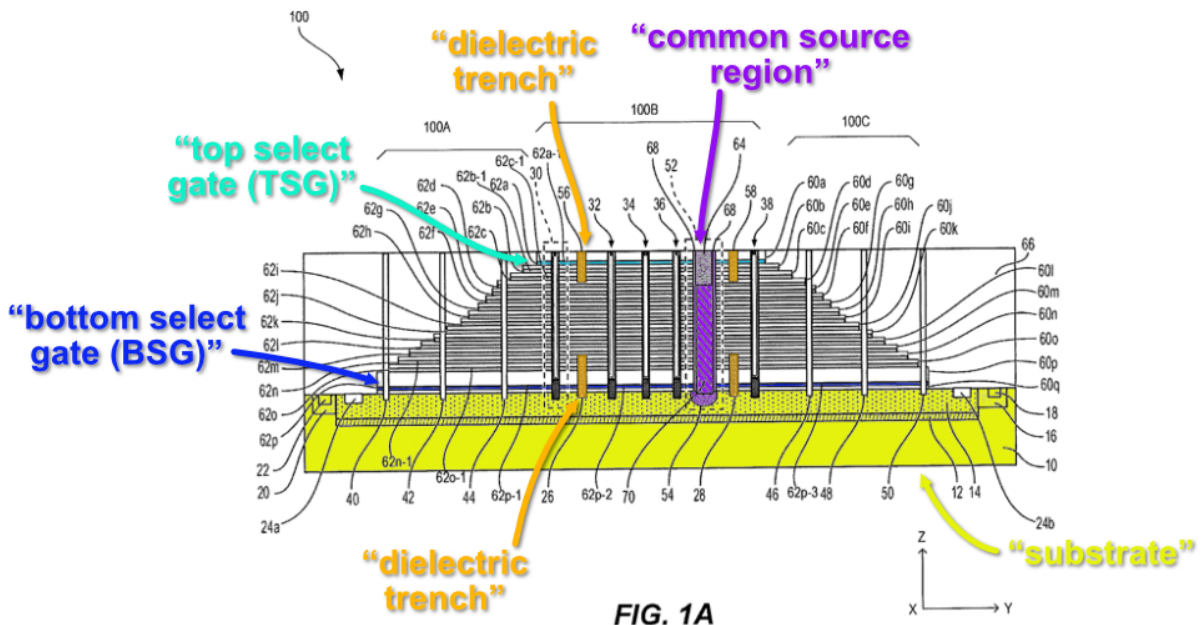
77. Electrical connection to these layers is made via the same type of “staircase region[]” present in prior art 3D NAND. Ex. 1001, 8:44-60; Fig. 2.

78. A “common source region 52” (annotated purple) passes through all the layers and “is electrically coupled with the substrate 10...” Ex. 1001, 7:59-67.

79. The memory strings are formed around “channel structures” 30/32/34/36/38. Ex. 1001, 8:23-26.

80. As shown, “first dielectric trenches” 26 and 28 (annotated brown/orange) are formed in the lower BSG, while “second trenches” 56 and 58 (also annotated orange) are formed in the upper TSG. Ex. 1001, 7:17-35.

81. The trenches divide the BSG and TSG into “sub-BSGs” and “sub-TSGs” associated with memory “sub-blocks” that “can be operated individually[.]” Ex. 1001, 7:45-53.

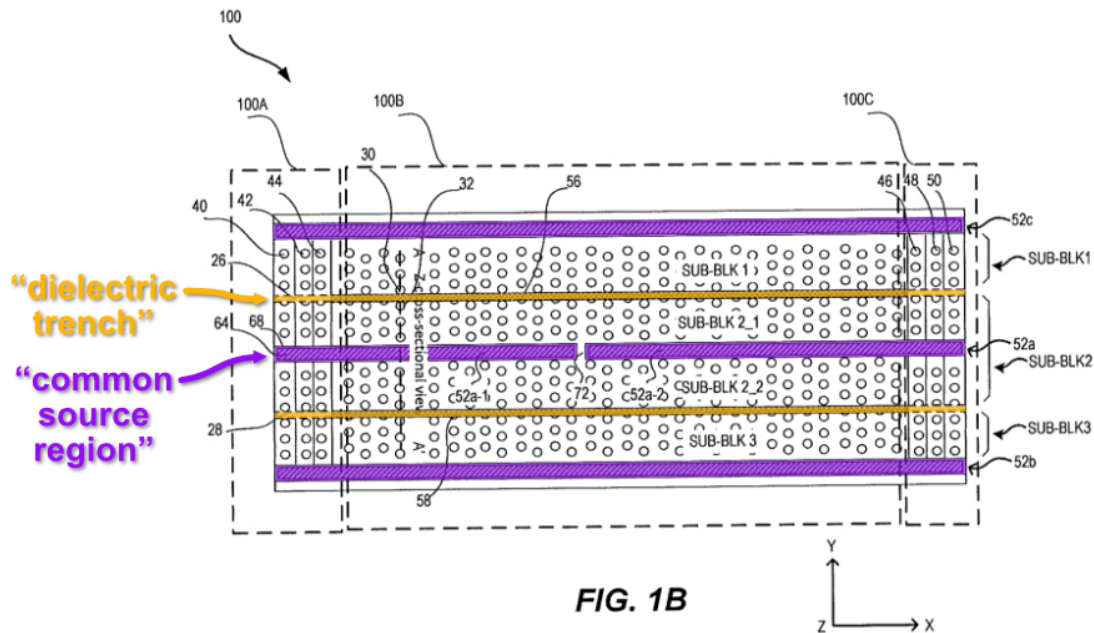


Id., Fig. 1A.

82. Figure 1B provides a top view of the structure shown in Figure 1A.

83. Trenches 26/56 and 28/58 (annotated orange) run parallel to common source regions 52a-c (annotated purple) along the “X-direction ... of the substrate.”

Ex. 1001, 7:20-62.



Id., Fig. 1B (annotated).

C. Prosecution History

84. As noted above, I have reviewed the '623 patent's prosecution history.

85. The '623 patent's claims were not rejected over the prior art during prosecution. *See generally* Ex. 1002, 611.

86. Further, when allowing the claims, the Examiner did not discuss any prior art. *See* Ex. 1002, 612-613.

D. Claims

87. For reference, claims 1-11 of the '623 patent are reproduced below:

1. A memory device, comprising:

a substrate;

a bottom select gate (BSG) disposed over the substrate;

a plurality of word lines positioned over the BSG with
a staircase configuration;

a plurality of insulating layers disposed between the
substrate, the BSG, and the plurality of word lines;

one or more first dielectric trenches formed in the BSG
and extending in a length direction of the substrate
to separate the BSG into a plurality of sub-BSGs;
and

one or more common source regions formed over the
substrate and extending in the length direction of the
substrate, wherein the one or more common source
regions extend through the BSG, the plurality of
word lines, and the plurality of insulating layers.

2. The memory device of claim 1, further comprising:

a top select gate (TSG) positioned over the plurality of
word lines, the TSG and the plurality of word lines
being spaced apart by the plurality of insulating
layers; and

one or more second dielectric trenches formed in the
TSG and extending in the length direction of the
substrate to separate the TSG into a plurality of sub-
TSGs.

3. The memory device of claim 2, wherein the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate.

4. The memory device of claim 2, wherein the one or more common source regions further pass through the TSG, and the one or more common source regions, the first dielectric trenches, and the second dielectric trenches extend parallel to each other in the length direction of the substrate.

5. The memory device of claim 2, further comprising:
a plurality of channel structures formed over the substrate along a height direction of the substrate that is perpendicular to the substrate, wherein each of the plurality of channel structure passes through the BSG, the plurality of word lines, the TSG, and the plurality of insulating layers.

6. The memory device of claim 1, further comprising:
a plurality of dummy channel structures formed along the a height direction of the substrate that is perpendicular to the substrate, the plurality of dummy channel structures passing through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate.

7. The memory device of claim 5, further comprising a plurality of memory cell sub-blocks, each of the memory cell sub-blocks including a plurality of respective channel structures that are connected to a same sub-BSG and to a same sub-TSG, each of the memory cell sub-blocks being operated individually.

8. The memory device of claim 5, wherein the one or more first dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate.

9. The memory device of claim 5, wherein the one or more second dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate so that a plurality of channel structures are disposed therebetween.

10. The memory device of claim 1, further comprising one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.

11. The memory device of claim 2, further comprising one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one

or more second dielectric trenches into a plurality of dummy sub-TSGs, and spaced apart from the plurality of the word lines and the TSG by the plurality of insulating layers.

VIII. CLAIM CONSTRUCTION

88. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

89. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

90. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

91. In my opinion, the terms of the '623 patent's claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

IX. UNPATENTABILITY ANALYSIS

92. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '623 patent, a POSITA would have considered claims 1-11 of the '623 patent to be unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art

93. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

1. Park

94. Park indicates on its face that it was filed January 25, 2017. *See* Ex. 1004, Cover. In view of this date filing, which is before the '623 patent's own December 2018 effective filing date, I understand that Park is prior art under 35 U.S.C. § 102(a)(2)

95. Park teaches a "3D-NAND memory device." Ex. 1004, 1:37-46.

96. This device includes the standard 3D NAND layers: a lower "ground select line" GSL, an intermediate "plurality of word lines" WL, and an upper "string select line" SSL. Ex. 1004, 1:63-2:1.

97. Multiple “common source line[s] 102” pass through these layers. Ex. 1004, 7:40-43.

98. Electrical connection to the layers is made via “a stepped structure.” Ex. 1004, 6:56-60.

99. The device’s memory cells are formed along “a plurality of channel structures extending vertically through” the GSL, WL, and SSL layers. Ex. 1004, 1:49-52.

100. Like the ’623 patent, Park sub-divides its memory “blocks” into smaller “unit areas.” Ex. 1004, 4:61-5:7.

101. For instance, as shown in Figure 3, a top view of the memory device from Park below, the memory device can include a “first block BK1” with “unit areas UA1 to UA4” and a “second block BK2” with “unit areas UA5 to UA8.” Ex. 1004, 5:8-10.

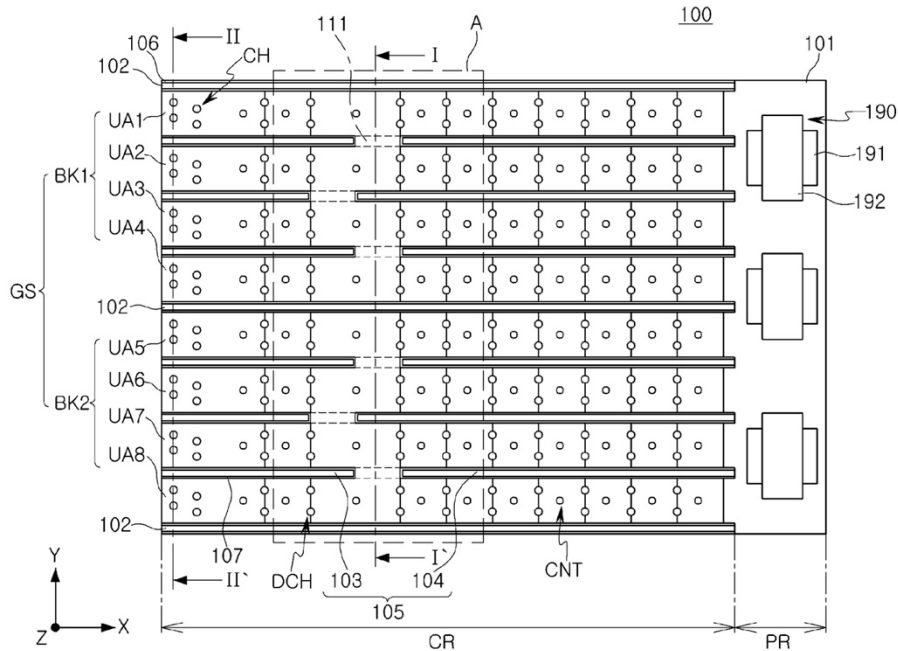


FIG. 3

Id., Fig. 3.

102. “[T]he memory cell devices” can be “independently control[led]” on a unit-by-unit basis. Ex. 1004, 5:67-6:4.

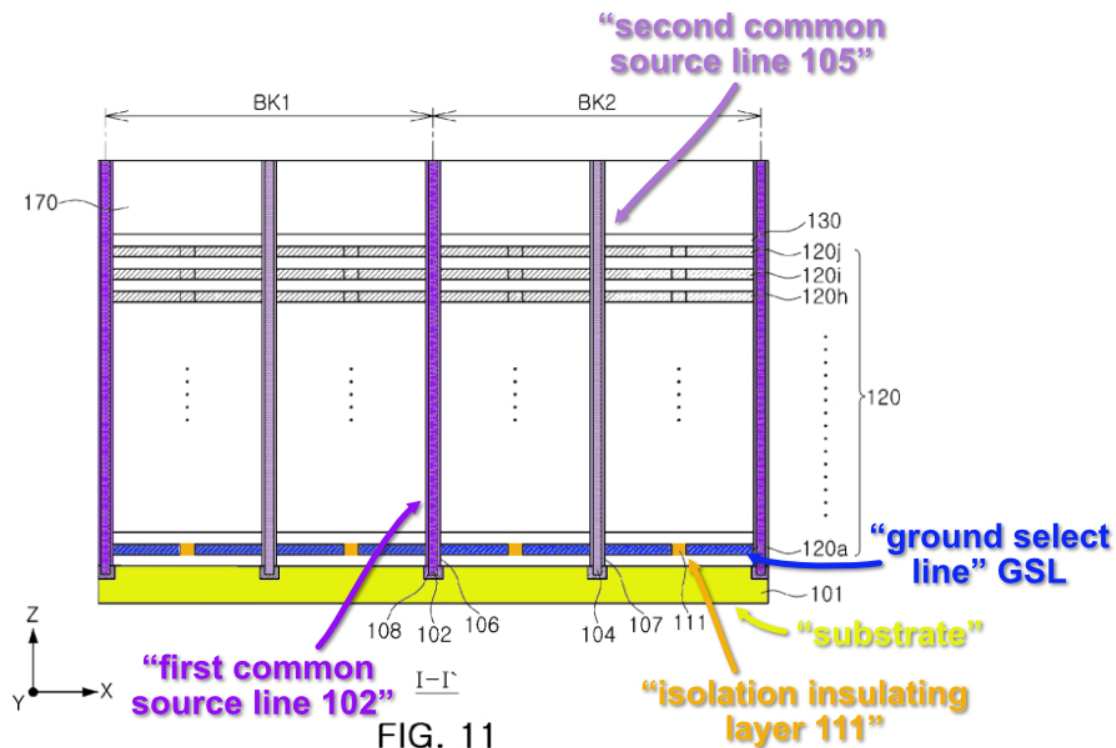
103. To achieve this, Park’s SSL and GSL “may be separated from each other between the ... unit areas....” Ex. 1004, 5:67-6:4.

104. Figures 3 and 11 provide examples of how this separation is achieved in Park. Figure 11 provides a cross-sectional view along line I-I' in Figure 3. Ex. 1004, 2:60-61.

105. As shown, “isolation insulating layers 111” (annotated orange below) formed in slits or openings through the GSL, along with “first common source lines 102” and “second common source lines 105” (annotated purple), separate the GSL

(annotated blue) into different “portions” “at the boundaries between the ... unit areas....” Ex. 1004, 6:8-12.

106. Four “isolation insulating layers 111” are shown. Other such layers are located behind portions 104 of the “second common source lines 105” (*see* Figure 3):



Ex. 1004, Fig. 11.

107. Again, the same isolation insulating layers are also shown in other figures, including Figure 3.

108. As shown in Figure 3’s top-down view, the “common source lines 102” and “105” (both annotated purple) and these “isolation insulating layers 111”

111. The device includes “multiple ... conductive layers stacked with ... insulator interposed....” Ex. 1005, [0003].

112. The layers include lower “source-side select gate” layers SGS, intermediate “word lines” WL, and an upper “drain-side select gate layer” SGD. Ex. 1005, [0003], [0048], [0074], [0166].

113. A conductive “interconnect portion LI ... is provided in [a] separation portion 60 (a slit ST)” passing through all the layers. Ex. 1005, [0065].

114. Shibata also divides its memory “block[s]” into smaller “string unit[s].” Ex. 1005, [0162]-[0163].

115. In Figure 16, a cross-sectional view of the memory structure, below, the memory block includes “two sub-blocks 200a and 200b subdivided by three separation portions 60 (slits ST)....” Ex. 1005, [0162]. One such slit is annotated in purple in Figure 16 below. The other two are not shown and would be located at the figure bounds. *See id.*

116. Sub-blocks 200a and 200b are divided into “string unit[s]” SU0-SU1 and SU2-SU3. According to Shibata, the select gate portions in each string unit can be “controlled electrically independently.” Ex. 1005, [0083].

117. To allow for this, “separation portion[s] 62a” (annotated orange below) are formed from slits filled with “insulating films” in its drain-side select gate

(annotated light blue) to divide that gate into four “independently” controllable pieces SGD0-SGD3. Ex. 1005, [0088]-[0090], [0166]-[0167].

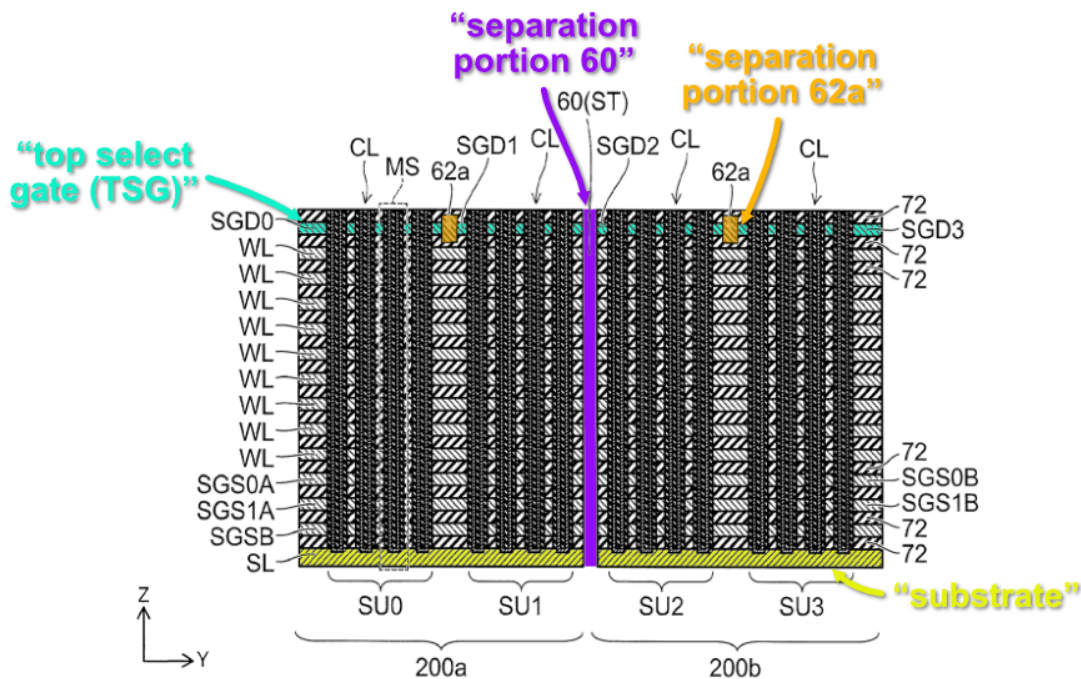


FIG. 16

Id., Fig. 16.

118. As shown in a top-down view below, these “separation portions” (again orange) “extend in the same direction as the separation portion 60 (the slit ST)” (purple). Ex. 1005, [0088].

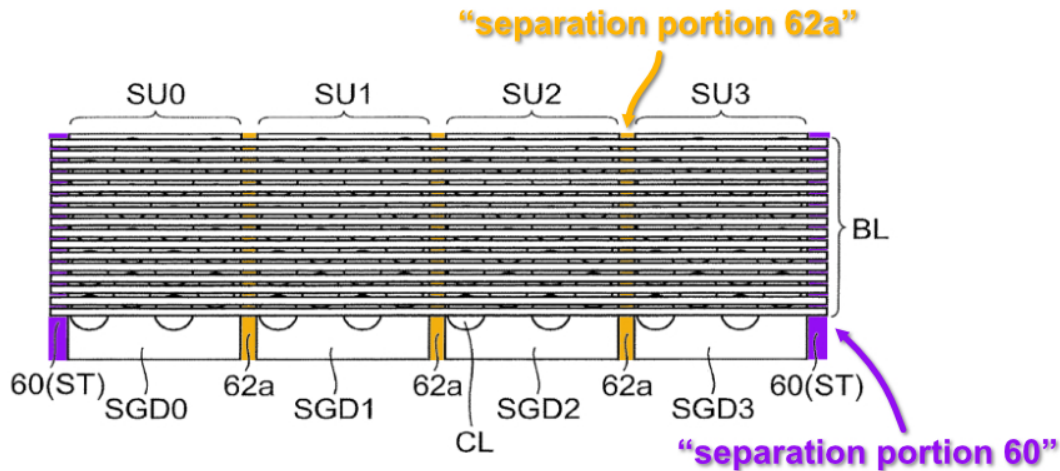


FIG. 47A

Id., Fig. 47A.

119. This is the case in all of Shibata's embodiments. (See Ex. 1005, Figs. 7A-7B, 14A-14B.

B. Ground 1: Claims 1-11 Are Obvious Over Park

120. In my opinion, a POSITA would have considered Park to be within the scope of the prior art and highly relevant to the patentability of the '623 patent's claims.

121. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Park renders claims 1-11 of the '623 patent obvious.

1. Claim 1

[1.Pre] "A memory device, comprising:"

122. In my opinion, to the extent this preamble language is limiting, it is taught by Park.

123. Park explains that it relates to a “3D memory device ... having a three-dimensional array of memory cells.” Ex. 1004, 1:14-17; *see also id.*, 1:31-32 (similarly referencing “a memory device”); 3:24-27 (explaining that “FIG. 1” shows a “memory device 1 according to an example”).

[1.A] “a substrate;”

124. In my opinion, Park includes the claimed “**substrate.**”

125. In particular, Park’s “memory device 100 ... include[s]” a “substrate 101” on which the various layers making up the device are formed. Ex. 1004, 10:34-35; *also id.*, 1:31-32 (explaining that the “memory device includes a substrate”).

126. Substrate 101 is annotated yellow in Figure 11 below:

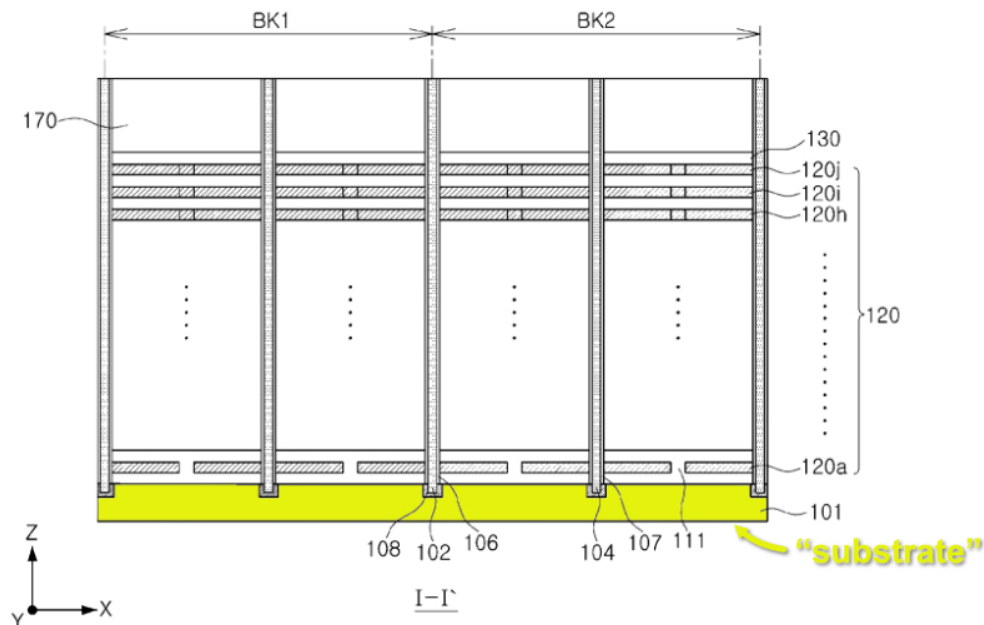


FIG. 11

Ex. 1004, Fig. 11 (annotated).

[1.B] “a bottom select gate (BSG) disposed over the substrate;”

127. This is taught by Park.

128. According to Park, its device’s “memory cell array” is formed from a “plurality of memory cell strings S.” Ex. 1004, 4:17-18.

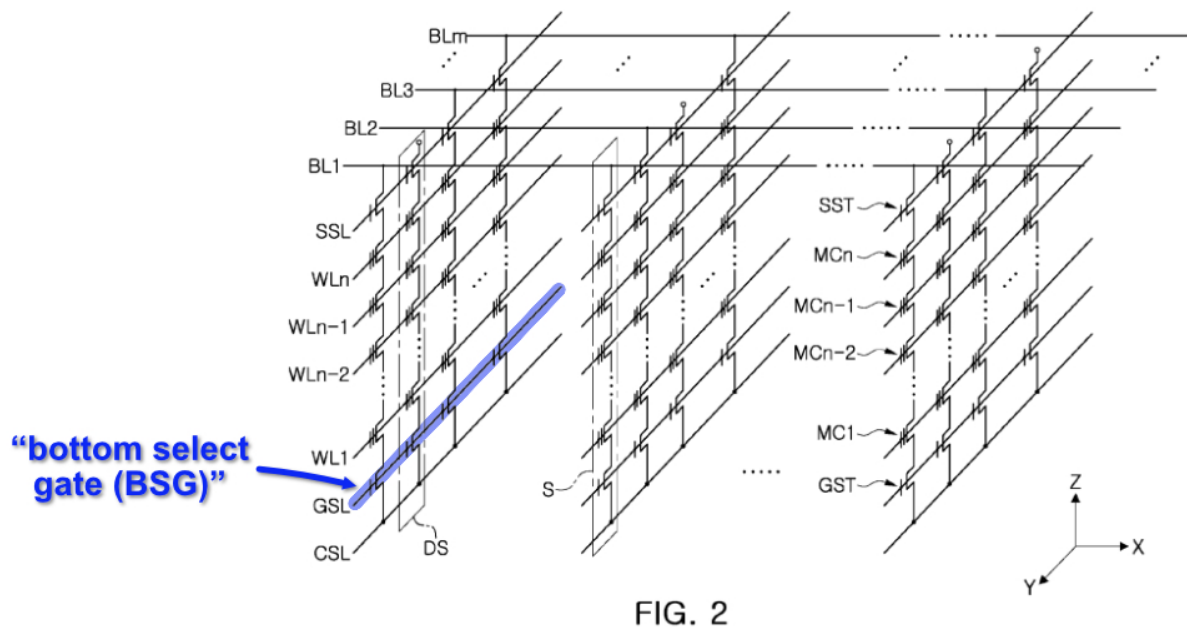
129. “[E]ach” string “include[s]” a lower “ground select transistor GST,” “memory cells MC1 to MCn[,]” and an upper “string select transistor SST,” all of which are “connected to each other in series[.]” Ex. 1004, 4:18-28. The “gate terminal” of “the ground select transistor GST” is “connected to a ground select line GSL.” *Id.*, 4:29-30. Each GST operates to connect an associated memory cell string to a “common source line CSL.” *Id.*, 4:30-32.

130. The ’623 patent, like Park, teaches a “3D-NAND memory device” with “vertical NAND memory cell strings” formed from “one or more bottom select transistors (BSTs), ... a plurality of memory cells (MCs),” and “one or more ... top select transistors (TSTs)” arranged “in series.” Ex. 1001, 1:37-46. A “bottom select gate (BSG)” operates to “control[.]” the “one or more bottom select transistors (BSTs)” for purposes of electrically connecting the associated memory strings to a “common source line (CSL)” at appropriate times during device operation *Id.*, 1:37-57.

131. Thus, while Park employs a different acronym than the ’623 patent (GSL versus BSG), in my opinion it nonetheless teaches the claimed “*bottom select*

gate (BSG)”: it includes a ground select line (GSL) that operates to control ground select transistors (GST) for purposes of connecting memory cell strings to a common source line (CSL). Ex. 1004, 4:18-32.

132. An example ground select line is annotated blue in Figure 2 below:



Ex. 1004, Fig. 2 (annotated).

133. Park also details where this ground select line (or GSL) is located with respect to its substrate.

134. In particular, Park’s memory device is formed from multiple “gate electrode layers 120” separated by “interlayer insulating layer[s] 170” that are “stacked on” its “substrate 101.” Ex. 1004, 10:35-41.

135. The lowest of these—located closest to the substrate—is “gate electrode layer 120a.” Ex. 1004, 10:55-56.

136. Thus, just as this claim requires, Park’s “*bottom select gate*” (its GSL) is “*disposed over the substrate.*”

137. Park’s GSL is highlighted blue in the annotated version of Figure 11 below. The substrate is again highlighted yellow:

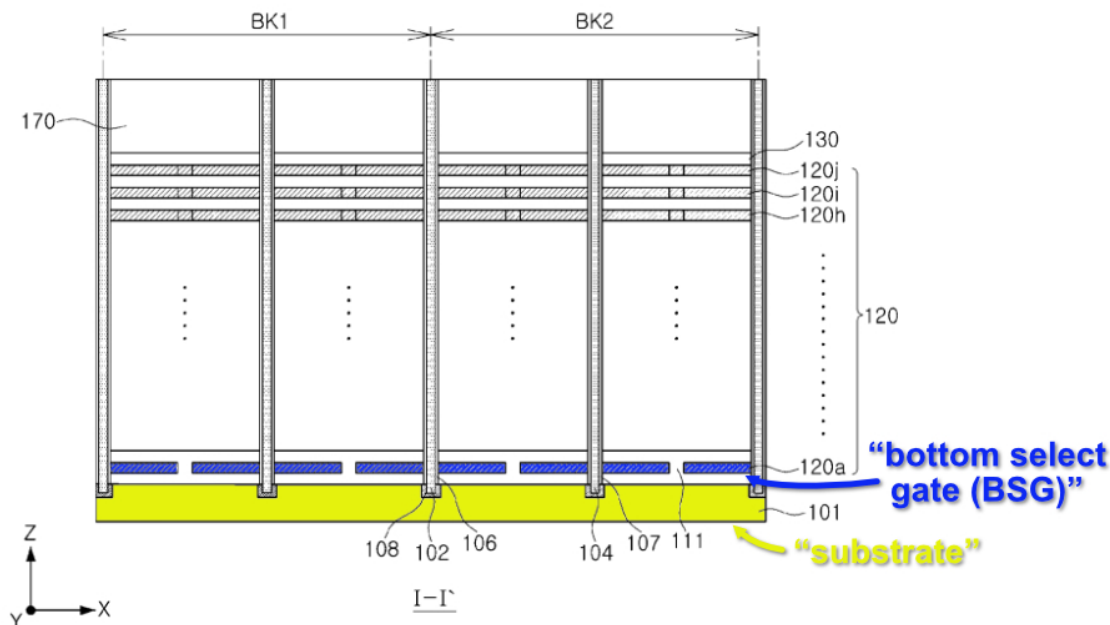


FIG. 11

Ex. 1004, Fig. 11 (annotated).

[1.C] “*a plurality of word lines positioned over the BSG with a staircase configuration;*”

138. This, in my opinion, is also taught by Park.

139. To begin, Park’s memory device includes “*a plurality of word lines.*”

140. In particular, as shown in Figure 2, Park’s “memory cell array 2” includes “a plurality of memory cells arranged in a plurality of rows and a plurality of columns.” Ex. 1004, 3:28-30.

141. Each row of “memory cell[s]” is connected to a “single word line WL.”

Ex. 1004, 3:28-36.

142. As a result, a string of “n memory cells MC1 to MCn connected to each other in series may be connected to n word lines WL1 to WLn for selecting the n memory cells...” Ex. 1004, 4:22-24; *see also id.*, 1:62-2:8 (explaining that Park’s device includes “a plurality of word lines”); 3:39-44 (“Each of the memory blocks may include a plurality of word lines WLs....”).

143. Example word lines WL1-WLn are highlighted red below:

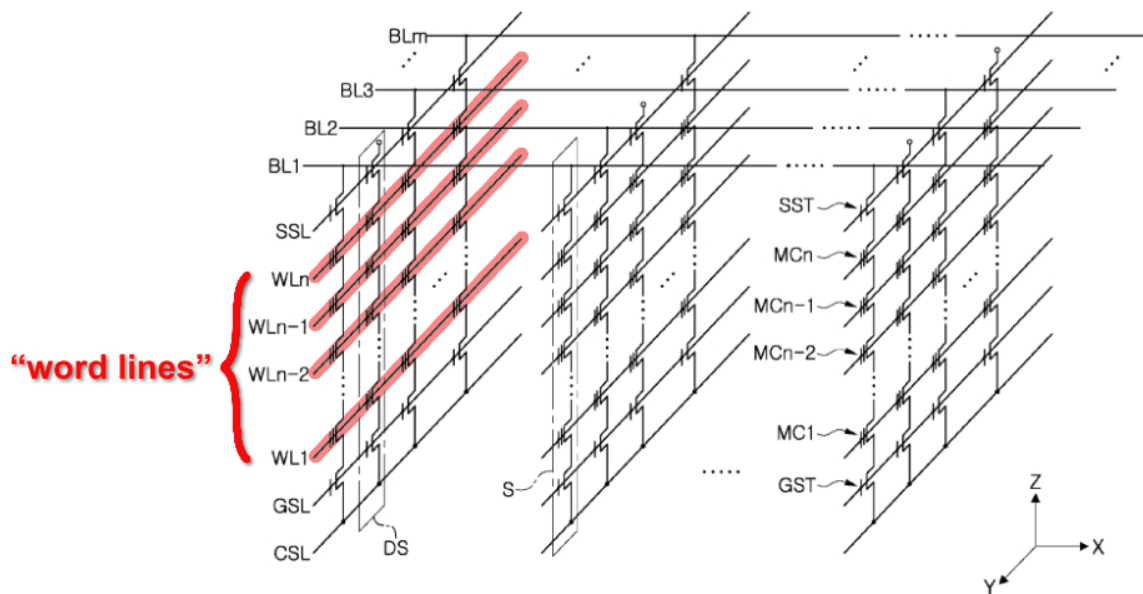


FIG. 2

Ex. 1004, Fig. 2 (annotated).

144. Next, Park’s word lines are “*positioned over the BSG.*”

145. Again, in Park’s device, multiple “gate electrode layers 120” are “stacked on” its “substrate 101.” Ex. 1004, 10:35-39; *see also id.*, 5:17-18 (“The gate structure GS may include a plurality of gate electrode layers stacked on a substrate 101.”); 6:49-55 (“[G]ate electrode layers 120” are “formed on the substrate 101”).

146. These “gate electrode layers 120 ... include at least one ground select line 120*a*, a plurality of word lines 120*b* to 120*i*, and at least one string select line 120*k* sequentially stacked in a layering direction from the upper surface of the substrate 101.” Ex. 1004, 6:65-7:2.

147. Annotated Figure 4 below provides an example. As shown, Park’s “**word lines**” (word lines 120*b* to 120*i*, annotated red) are all located over Park’s “**BSG**” (ground select line 120*a*, annotated blue):

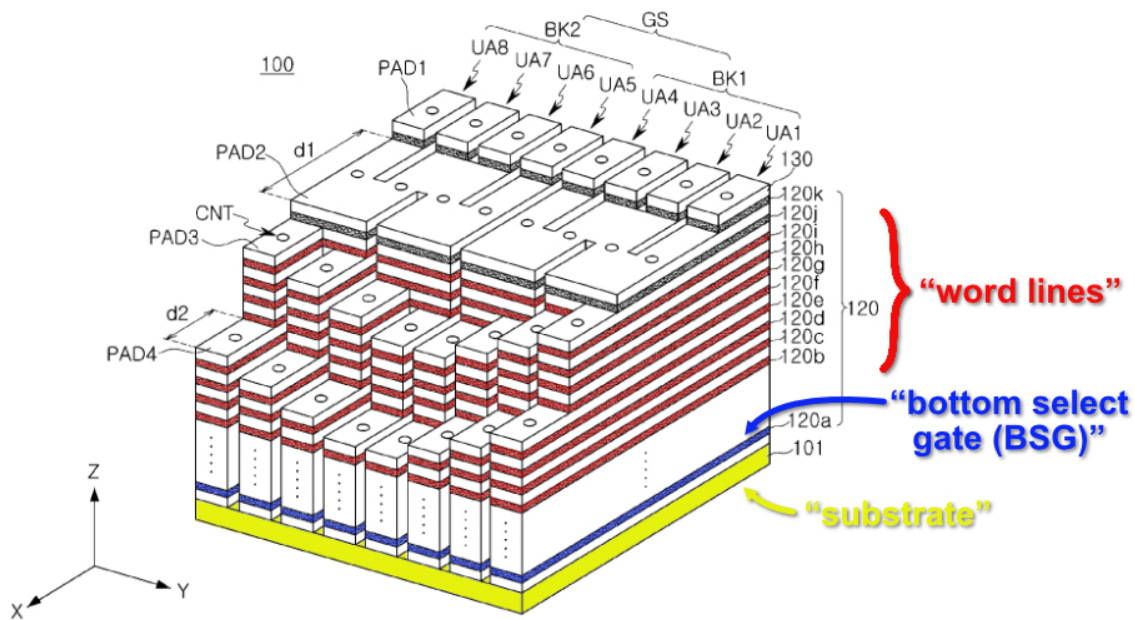


FIG. 4

Ex. 1004, Fig. 4 (annotated).

148. Park's word lines also have "*a staircase configuration*" as this limitation requires.

149. In particular, Park explains that its various "gate electrode layers ... may extend by different lengths" such that they have "a stepped structure." Ex. 1004, 6:56-60.

150. For instance, in Figure 4 above, "the word lines 120b to 120i" are "provided step-wise in both the first direction, e.g., the X-axis direction, and a second direction, for example, a Y-axis direction." Ex. 1004, 7:8-11; *see also id.*, 8:18-50 (similarly referencing "word lines" with a "step" structure); 11:62-65 (similar); Figs. 15, 25, 32.

[1.D] “a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;”

151. In my opinion, Park’s memory device also includes the claimed **“plurality of insulating layers.”**

152. According to Park, “a plurality of insulating layers may be disposed between the gate electrode layers to electrically separate the gate electrode layers from each other.” Ex. 1004, 5:17-23; *see also id.*, 6:49-52 (explaining that the “gate structure GS” includes “a plurality of insulating layers 130”); 10:35-37 (similarly referencing “interlayer insulat[ion]”).

153. These insulating layers may “include an insulating material such as silicon oxide or a silicon nitride, and in examples, may be a high density plasma (HDP) oxide layer or a tetra ethyl-ortho-silicate (TEOS) oxide layer.” Ex. 1004, 10:40-45.

154. Next, Park’s **“insulating layers”** are also located everywhere this limitation requires.

155. For instance, as shown in Figure 11 below, there is interlayer insulation 130 (annotated green) between **“the substrate”** (substrate 101, annotated yellow) and **“the BSG”** (ground select line 120*a*), between **“the BSG”** and **“the plurality of word lines”** (word lines 120*b*-120*i*, annotated red), and between the **“word lines”** themselves:

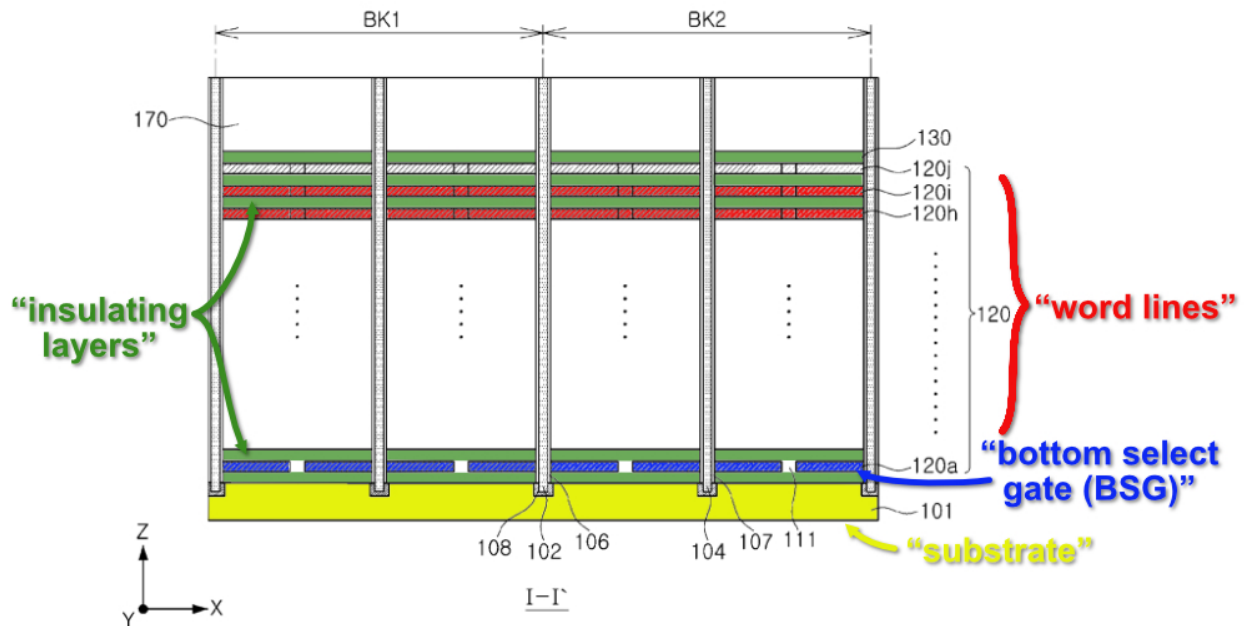


FIG. 11

Ex. 1004, Fig. 11 (annotated).

156. The presence of insulation in these locations is confirmed by Park's discussion of an exemplary memory device manufacturing method.

157. In particular, according to Park, "a first insulating layer IL1" followed by a "first sacrificial layer SL1" is first "formed on" the "substrate." Ex. 1004, 12:56-64; Fig. 19.

158. Then, additional alternating "insulating layers IL2 to IL16" and "sacrificial layers SL2 to SL15" are formed above the "first sacrificial layer." Ex. 1004, 13:4-17; Fig. 23.

159. The various “sacrificial layers” are removed in a later step and replaced with conductive material to form the lower “ground select line,” intermediate “word lines,” and upper “string select line.” Ex. 1004, 15:35-42; 16:3-16.

160. The end result is a structure in which there is insulation between the substrate and the gate electrode layer, between the gate electrode layer and the word lines, between each of the word lines, and between the last word line and the string select line. *See* Ex. 1004, Fig. 34.

[1.E] “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and”

161. This, in my opinion, is all rendered obvious by Park.

162. As explained in more detail below, Park’s “**BSG**” (its ground select line) is “*separate[d] ... into a plurality of sub-BSGs*” (ground select line portions specific to unit areas UA1-UA8) by “*one or more first dielectric trenches*” (isolation insulating layers 111).

163. According to Park, its “memory device 100” includes a “cell region CR” with a “gate structure GS” that can be “divided into a plurality of blocks BK1 and BK2.” Ex. 1004, 4:61-5:8. These blocks can then be further sub-divided into “unit areas.” *Id.*

164. For example, in Figure 3, “first block BK1 includes first to fourth unit areas UA1 to UA4” while “second block BK2 includes fifth to eighth unit areas UA5 to UA8.” Ex. 1004, 5:8-10.

165. According to Park, the “word lines” in each block are electrically connected and continuous across the unit areas. Ex. 1004, 5:54-60; *see also id.*, 7:44-50. This is because the isolation insulating layers only separates the GSL and not the word lines above. This can be seen, for instance, in Figures 6-10. *See id.*, Figs. 6-10.

166. But “[i]n order to independently control the memory cell devices of the first to eighth unit areas UA1 to UA8, the string select line and the ground select line may be separated from each other between the first to eighth unit areas UA1 to UA8.” Ex. 1004, 5:67-6:4.

167. Park goes on to explain that different “portions of the ground select line” are “separated from each other at the boundaries between the first to eighth unit areas UA1 to UA8 by ... first common source lines 102, the second common source lines 105, and isolation insulating layers 111.” Ex. 1004, 6:8-12; *see also id.*, 10:55-56 (“The gate electrode layer 120a forming the ground select line may be divided by the isolation insulating layer 111.”); 10:60-65 (“The ground select lines of the respective first to eighth unit areas UA1 to UA8 may be electrically separated from each other by the first and second lines 103 and 104 of the second common source

lines 105 and the isolation insulating layer 111 disposed between the first and second lines 103 and 104. Thus, the memory cells of the respective first to eighth unit areas UA1 to UA8 may be independently controlled.”).

168. Park’s isolation insulating layers 111 are shown in multiple figures. Figure 3 provides a top-down view.

169. As shown, the isolation insulating layers 111 (annotated orange) are located between common source lines 102, and extend lengthwise in the X-direction to close the gaps in common source lines 105 to separate blocks BK1 and BK2 into sub-units UA1-UA4 and UA5-UA8:

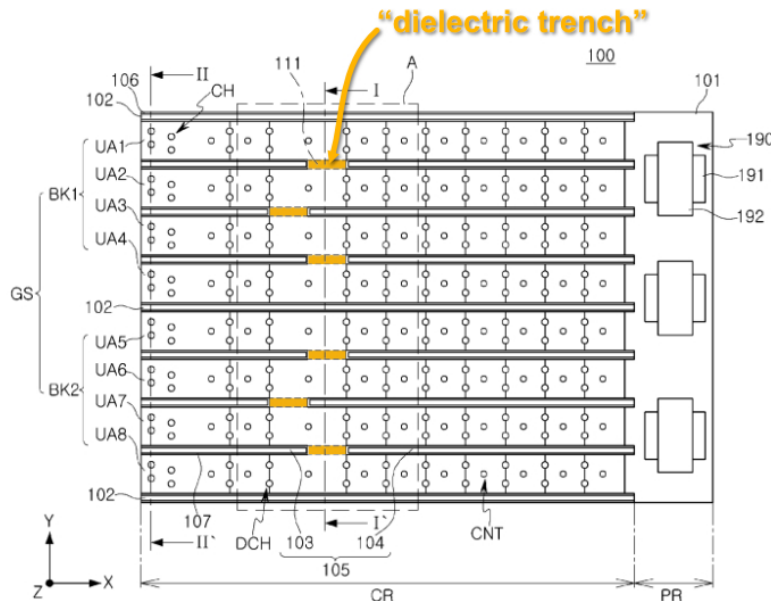


FIG. 3

Ex. 1004, Fig. 3 (annotated).

170. Figure 11 provides a cross-sectional view along line I-I’ from Figure 3. Four isolation insulating layers 111 (again annotated orange) are shown located

within and dividing—in combination with first and second lines 103 and 104—gate electrode layer 120a (the layer forming Park’s ground select line) into portions, each of which corresponds to one of the unit areas UA1-UA8:

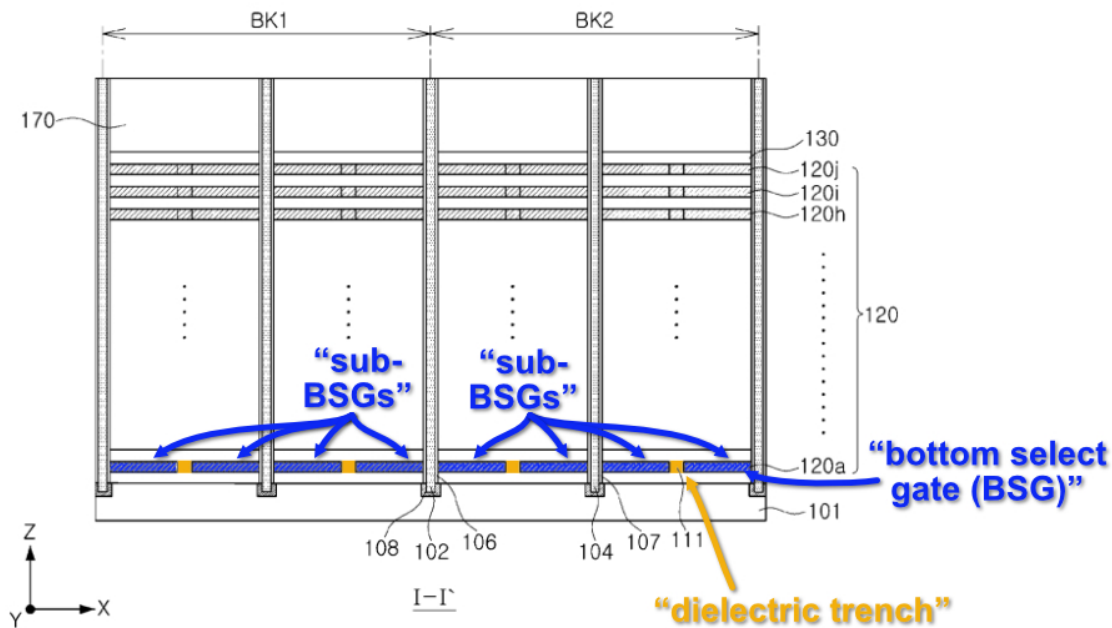


FIG. 11

Ex. 1004, Fig. 11.

171. This, in my opinion, is exactly what this claim limitation requires. Park includes *“one or more first dielectric trenches formed in the BSG”* (the isolation insulating layers 111 formed within the ground select line). These *“dielectric trenches” “extend[] in a length direction of the substrate”* (as shown in Figure 3, isolation insulating layers 111 extend lengthwise in the X-direction). Further, the *“dielectric trenches” “separate the BSG into a plurality of sub-BSGs”* (the isolation insulating layers 111 close the gaps in lines 103 and 104 causing Park’s

lower ground select line to be divided into portions corresponding to unit areas UA1-UA8). They are also made from a “*dielectric*” material such as a silicon oxide. *See* Ex. 1004, 15:45-49 (explaining that Park’s “isolation region[s]” can be formed with the “same material as the insulating layers IL”); 12:59-64 (referencing the use of “a silicon oxide” for Park’s “insulating layer[s]”)

172. While Park does not use the same language as claim 1 and call its isolation insulating layer 111 a “*trench*,” in my opinion a POSITA would nonetheless have understood that this is what it teaches.

173. Park explains that to form the isolation insulating layers 111, “opening regions OP” are “formed in the first sacrificial layer SL1” to “expose []” the underlying “[p]ortions of the first insulating layer IL1.” Ex. 1004, 12:65-13:1. This is shown in Figure 20 (providing a top view) and 21 (providing a cross-sectional view):

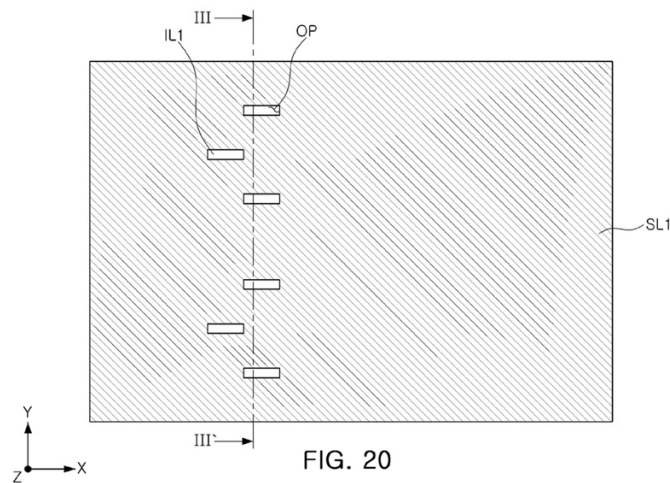


FIG. 20

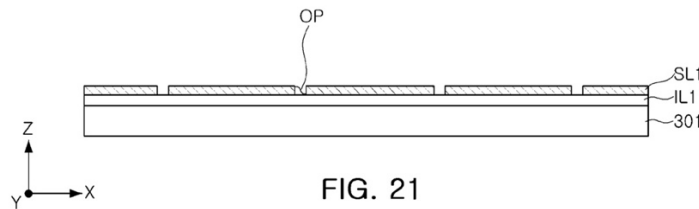


FIG. 21

Id., Figs. 20-21. Opening OP is structured as a trench extending in Figure 20's X-axis direction. *See id.* This opening is then "filled with an insulating material" to form the "isolation regions[]." *Id.*, 13:15-17. Thus, the isolation insulating layers are insulation filled trenches proceeding through one of Park's conductive layers. *See id.*, 12:65-13:1; 13:15-17; Figs. 11, 20-21. Subsequently, the GSL is formed and these trenches remain in place, resulting in the GSL (Park's "**bottom select gate**") having insulation trenches formed within it. *See id.*, 15:35-43, 16:3-37.

174. The '623 patent employs an analogous process to form its "dielectric trenches."

175. According to the patent, “trenches can be formed by” forming “trench openings” through the desired layers and then “fill[ing]” these “trench openings” with “a dielectric material.” Ex. 1001, 16:1-18; 17:43-55.

176. Moreover, “[i]n some embodiments (i.e., Gate-last Formation Technology),” the BSG, word lines, and other layers can be “formed firstly using sacrificial layers” that are only replaced with conductive material after all other processing steps—including the trench formation—are completed. Ex. 1001, 7:1-16; *see also id.*, 15:45-46 (explaining that the “BSG” in which the trench openings are formed can be “sacrificial layers”).

177. While there are some minor structural differences between Park’s isolation insulating layer 111 and the example “dielectric trenches” shown in certain of the ’623 patent’s figures, in my opinion none of this serves to distinguish Park from the ’623 patent’s claims.

178. For instance, in Figures 1A and 1B of the ’623 patent, dielectric trench 26 traverses nearly the entire length of depicted memory device 100 to divide BSG 62p into portions 62p-1 (associated with SUB-BLK1) and 62p-2 (associated with SUB-BLK2). *See* Ex. 1001, Figs. 1A-1B.

179. In Park, isolation insulating layers 111 do not extend across the full length of the memory device. Instead, they cooperate with common source lines 105

(which include second lines 103 and 104) to divide Park's ground select line into portions. *See, e.g.*, Ex. 1004, 6:8-12; Fig. 3.

180. Claim 1 requires only that the “dielectric trenches formed in the BSG ... separate the BSG into a plurality of sub-BSGs.” Nothing about the claim requires that the “dielectric trenches” perform this separation function completely by themselves without the help of any other structure.

181. Moreover, the '623 patent repeatedly explains that its figures are “merely examples and are not intended to be limiting.” Ex. 1001, 5:13-16; 5:33-36; 23:41-46.

182. While not identical to trenches in the '623 patent's figures, Park's isolation insulating layers 111 do exactly what the claim requires: if these layers were not present, the portions of Park's ground select line in unit areas UA1-UA4 (or unit areas UA5-UA8) would be electrically connected to each other through the gaps in common source lines 105, thereby forming a single ground select line spanning the entirety of BK1 (or BK2).

183. If, however, it is for some reason determined that the claimed “dielectric trenches” must themselves “separate” the “BSG” into “sub-BSG” completely on their own and not in cooperation with any other structure, in my opinion the claims would still be obvious over the combination of Park and Shibata for the reasons discussed in Ground 2 below.

184. Figure 1A of the '623 patent also depicts dielectric trench 26 extending through multiple conductive layers (62n, 62o, and 62p), the intervening insulation, and into substrate 10. *See* Ex. 1001, Fig. 1A.

185. Claim 1, however, requires only that the “dielectric trenches” be “formed in the BSG.” Ex. 1001, claim 1.

186. While Figure 1A does depict a portion of trench 26 within substrate 10, the '623 patent explains that this is simply an optional feature. *See, e.g.*, Ex. 1001, 7:42-44 (“In some embodiments, the first trenches 26 and 28 can extend into the HVPW 14....”); Fig. 8A (depicting example trenches 26 and 28 that do not extend into substrate 10).

187. In sum, Park’s isolation insulating trenches 111 perform the same function in the same way as the '623 patent’s dielectric trenches. They are located within the layer forming Park’s “BSG.” *E.g.*, Ex. 1004, 10:55-56 (“gate electrode layer 120a” is “divided by the isolation insulating layer 111”). And they divide that BSG layer into separate “sub-BSG” to allow for control of the memory on a sub-block basis. *Id.*, 5:67-6:4 (“separat[ion]” of the “ground select line” allows the device to “independently control the memory cell devices of the first to eighth unit areas UA1 to UA8”).

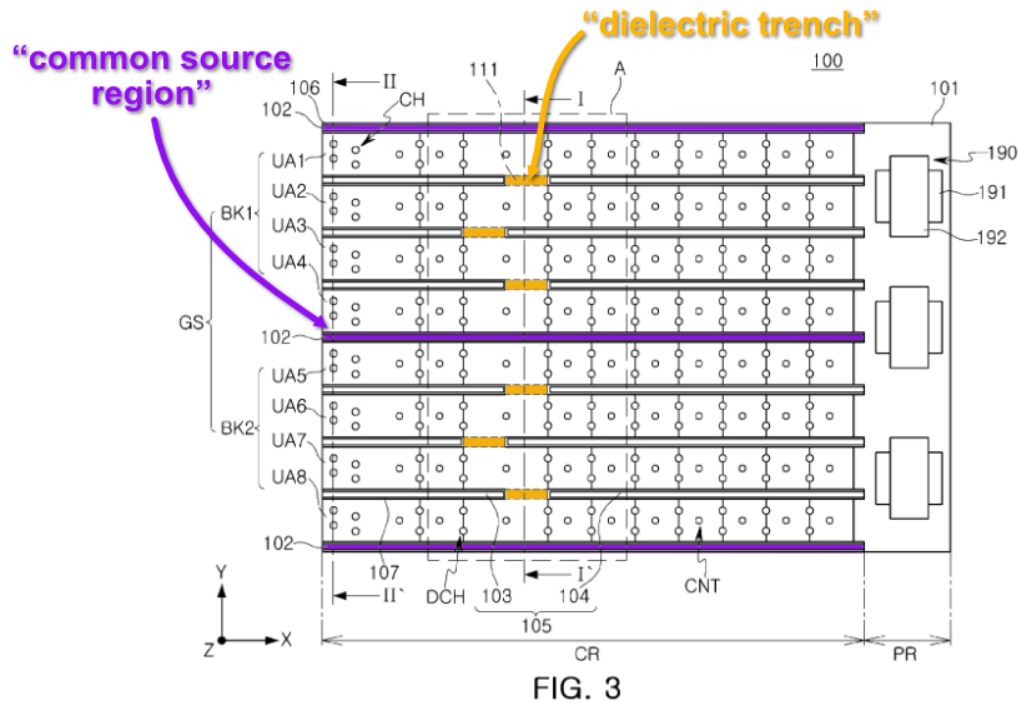
[1.F] “one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.”

188. In my opinion, Park teaches a memory device that includes the claimed **“common source regions.”**

189. According to Park, its memory device includes multiple “common source line[s] 102.” Ex. 1004, 7:40-43.

190. These “common source lines 102” “extend[] in the first direction, e.g., the X-axis direction” to “divide[]” the memory device into “first and second blocks BK1 and BK2....” Ex. 1004, 10:46-50; *see also id.*, 1:53-54 (referencing “a plurality of first common source lines each extending horizontally in the first direction, and interposed between the unit electrodes of the gate electrode layers”); 1:63-2:3 (noting that the “plurality of first common source lines extend[] horizontally in a first direction”).

191. As shown in Figure 3, the **“common source regions”** (common source lines 102, annotated purple) **“extend[]”** in the same **“length direction of the substrate”** (the X-axis direction) as Park’s **“dielectric trenches”** (the isolation insulating layers 111, annotated orange):



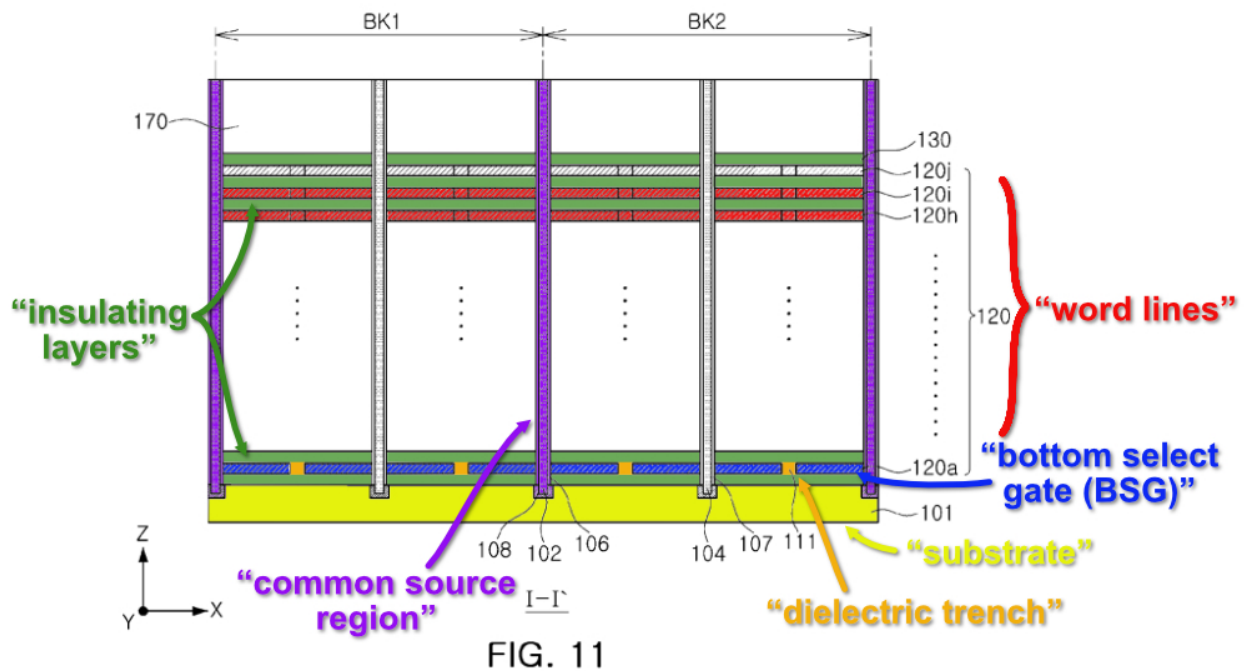
Ex. 1004, Fig. 3 (annotated).

192. Park also explains that its “common source lines 102” pass through and “divide[]” its various “gate electrode layers 120 and the interlayer insulating layer[s] 170,” including the lower “gate electrode layer 120 forming the ground select line.” Ex. 1004, 10:46-67.

193. This allows the “common source line 102” to be “connected to source regions 108 of the substrate 101 therebelow.” Ex. 1004, 11:1-3. Electrically connection is effected with “source regions 108 ... formed by injecting an impurity having a certain conductivity type into the substrate....” *Id.*, 11:3-6.

194. This, in my opinion, is what this limitation requires. Figure 11 provides an example. As shown, Park’s “**common source region**” (common source line 102,

annotated purple) “*extend through the BSG*” (ground select line 120a, annotated blue), “*the plurality of word lines*” (word lines 120b to 120i, annotated red), and “*the plurality of insulating layers*” (annotated green):



Ex. 1004, Fig. 11 (annotated).

2. Claim 2

195. Claim 2 depends on claim 1 and further requires:

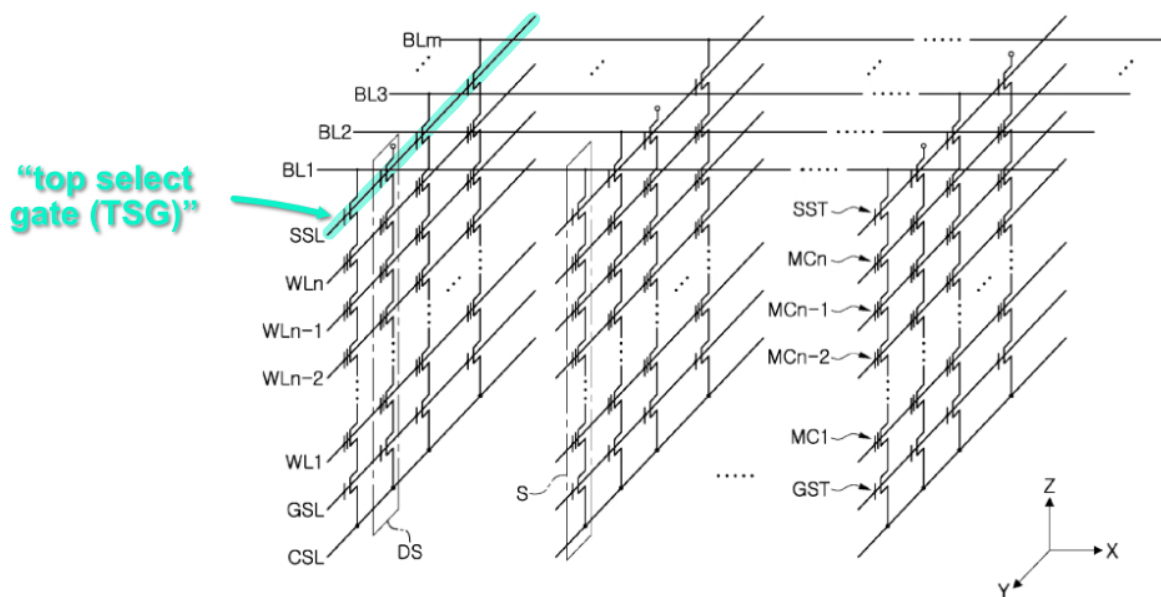
[2.A] “a top select gate (TSG) positioned over the plurality of word lines, the TSG and the plurality of word lines being spaced apart by the plurality of insulating layers; and”

196. This, in my opinion, is taught by Park.

197. Park explains that the “stack of gate electrode layers” forming its memory device includes not only a lower “ground select line” and an intermediate

“plurality of word lines[,]” but also “at least one string select line.” Ex. 1004, 1:63-2:1; *id.*, 7:20-29 (similarly discussing “string select line 120k”).

198. As shown in Figure 2, the upper “string select line SSL” (annotated light blue below) allows each memory cell string to be “connected to ... a bit line BL.” Ex. 1004, 3:30-34.



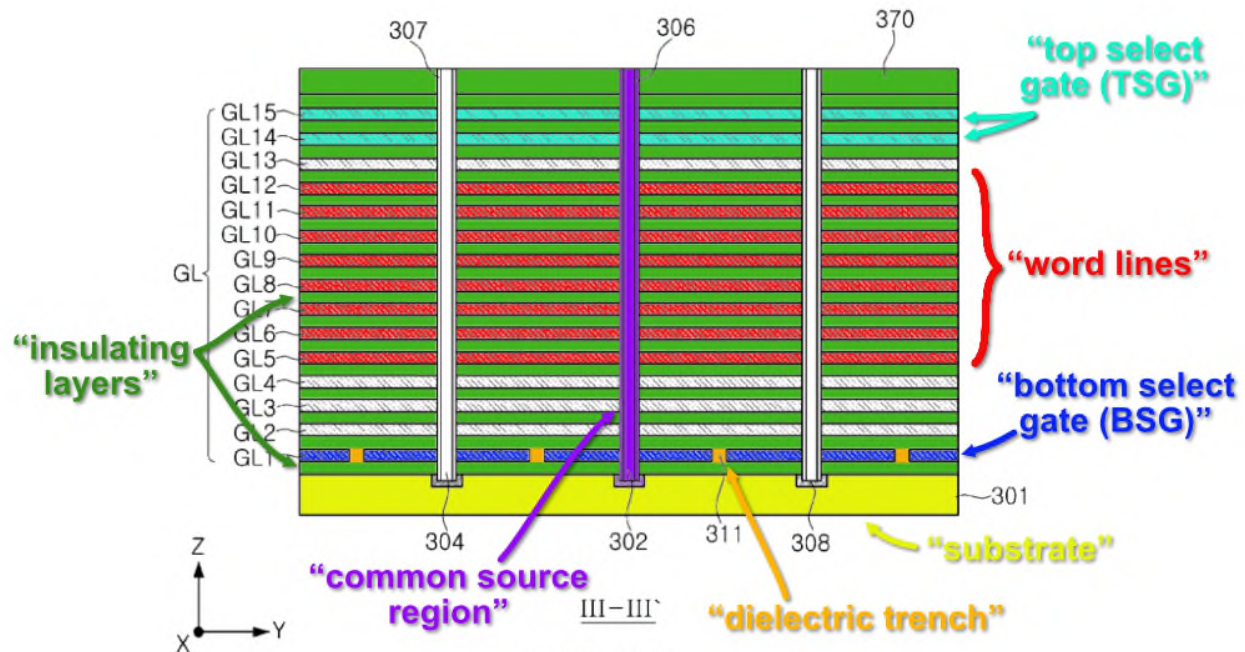
Id., Fig. 2 (annotated).

199. Further, according to Park, “a plurality of insulating layers” are “disposed between the gate electrode layers[,]” including the “word lines” and “string select line[,]” to electrically separate the gate electrode layers from each other.” Ex. 1004, 5:17-22.

200. Figure 36 provides an example. Here, “first gate electrode layer GL1 ... form[s] the ground select line.” Ex. 1004, 16:9-11. “The fifth to twelfth

gate electrode layers GL5 to GL12 ... form the word lines....” *Id.*, 16:13-14. “[T]he fourteenth and fifteenth gate electrode layers GL14 and GL15 may form the string select line.” *Id.*, 16:14-16.

201. As shown, there are a “**plurality of insulating layers**” (annotated green) between Park’s “**plurality of word lines**” (layers GL5-12) and the “**top select gate (TSG)**” (string select line layers GL14-15):



Ex. 1004, Fig. 36 (annotated).

[2.B] “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.”

202. This is also rendered obvious by Park.

203. In particular, Park teaches that in its memory device, both the upper “string select line” and the lower “ground select line” are “separated from each other

between the first to eighth unit areas UA1 to UA8” to allow the unit areas to be “independently control[led].” Ex. 1004, 5:65-6:12; *see also id.*, 7:19-29 (discussing “separat[ion]” of the “string select line” into portions); 16:22-37 (similarly explaining that the “ground select line may be divided into unit electrodes in each of the first to eighth unit areas UA1 to UA8 and the “string select line” is also “divided into separate unit electrodes in each” of these same “unit areas”).

204. Thus, as this claim requires, Park “*separate[s]*” its “*TSG*” (the upper string select line) into “*sub-TSGs*” (the portions of the string select line corresponding to unit areas UA1-UA8).

205. While Park does not provide an example of a device that effects this separation with “*one or more second dielectric trenches formed in the TSG*” that “*extend[] in the length direction of the substrate[,]*” a POSITA would nonetheless have considered this obvious in view of Park’s overall teachings.

206. According to Park, “isolation insulating layers 111” are employed to separate its lower ground select line into independently controllable portions. *See* Ex. 1004, 5:67-6:4; 10:55-57; *see also supra* discussion of limitation [1.E].

207. In some of Park’s embodiments—including that shown in Figures 3, 4, and 11—the upper string select line does not have the same physical extent as the lower ground select line. *See, e.g.*, Ex. 1004, Figs. 3, 4, and 11.

208. As a result, in these embodiments the upper string select line is not present over the portion of the ground select line where the “isolation insulating layers 111” are located. See Ex. 1004, Figs. 3, 4, and 11. Because of this, in these embodiments, Park is able to effect separation of the string select line using only “the first common source lines 102 and first lines 103 of the second common source lines 105.” *Id.*, 6:4-8.

209. Park explains, however, that this is only an “example.” Ex. 1004, 6:4-8. Thus, in other embodiments, the upper string select line is present over the locations where the lower ground select line is divided by the isolation insulating region 111.

210. Figure 36, reproduced below, provides an example of this:

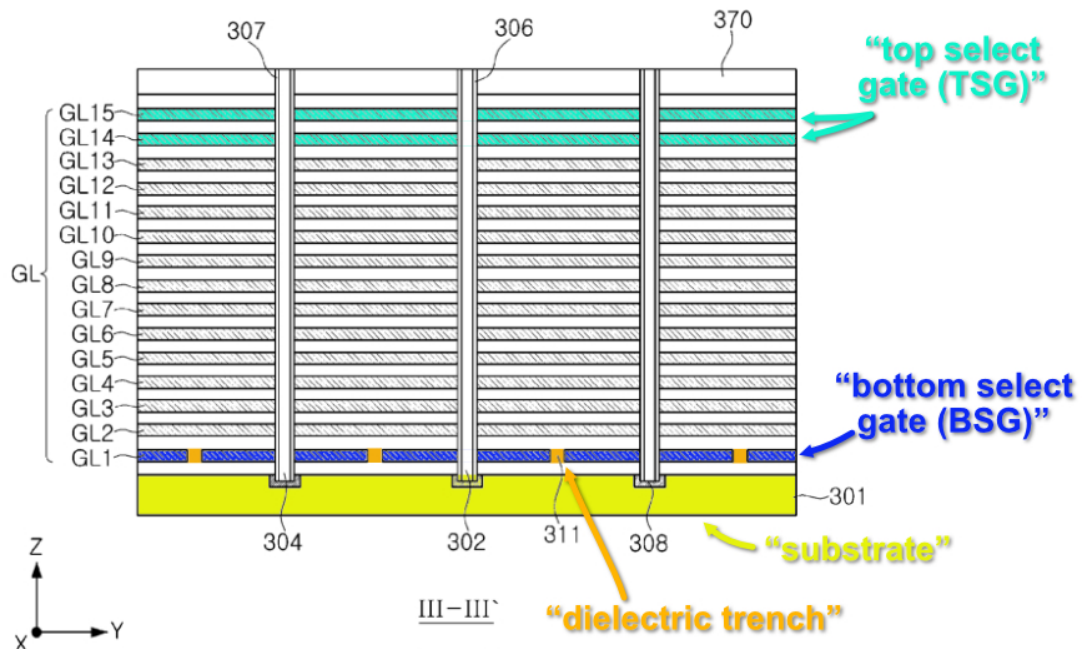


FIG. 36

Ex. 1004, Fig. 36 (annotated).

211. According to Park, in this figure “GL1 ... form[s] the ground select line.” Ex. 1004, 16:9-11. And “GL14 and GL15 ... form the string select line.” *Id.*, 16:14-16. As shown, the “ground select line” is “divided into separate unit electrodes ... by the isolation regions 311.” *Id.*, 16:22-26.

212. Park also explains that in this embodiment, string select line layers “GL14 and GL15” are also “separated from each other in separate regions in each of the first to eighth unit areas UA1 to UA8” like ground select layer “GL1.” Ex. 1004, 16:30-36.

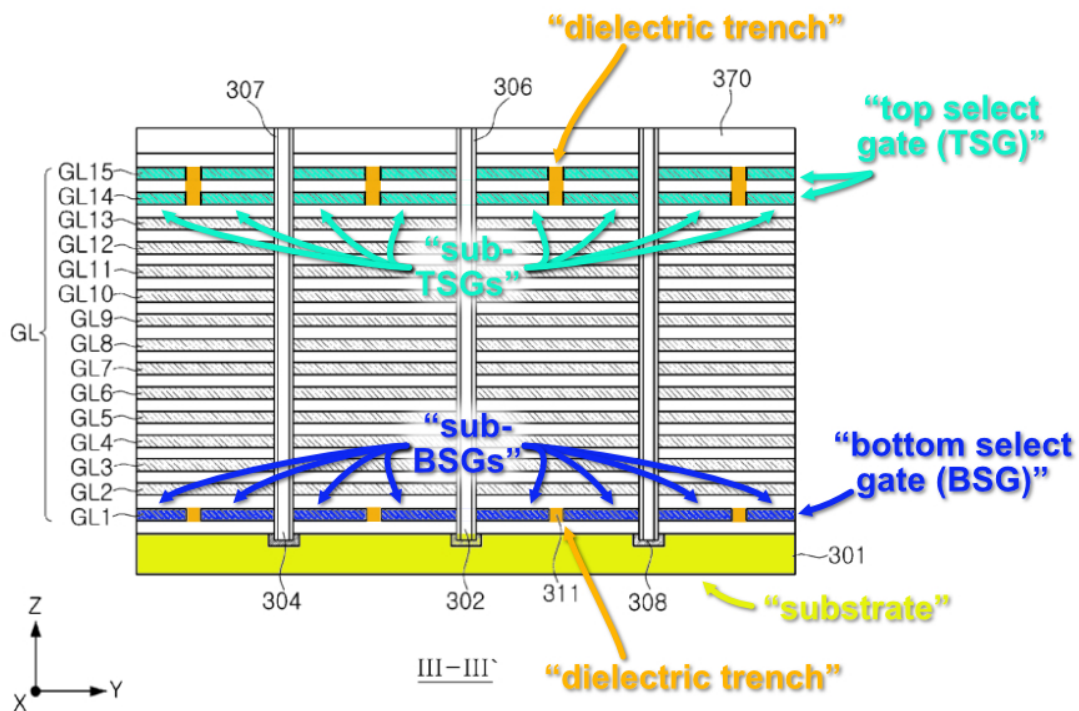
213. But unlike in Park’s other embodiments, the string select line is present in locations where it cannot be completely divided by the common source lines. *See* Ex. 1004, Fig. 36. Doing so would divide Park’s word lines which are meant to be electrically connected and shared across its memory blocks. *See* Ex. 1004, 7:44-56.

214. Given this, in my opinion a POSITA would have understood that other means to separate the string select line into portions is required.

215. The only other method for separating electrodes into portions set forth in Park is the use of “isolation insulating layers 111.”

216. Thus, in my opinion a POSITA would have recognized that one obvious way to achieve the missing but required separation would be to simply include

another “isolation insulating region 111” in the upper string select layer. An example of this is shown below:



Ex. 1004, Fig. 36 (annotated).

217. As shown, “*one or more second dielectric trenches*” (a separate set of isolation insulating regions) now divides Park’s “*TSG*” (the upper string select lines) into “*sub-TSGs*” (separate portions corresponding to unit areas UA1-UA8).

218. The same process used when forming the lower isolation insulating layers 111—forming an opening or trench and then filling it with dielectric material—would be used to form the new upper isolation layers.

219. In my opinion, a POSITA would have been motivated to use Park’s “isolation insulating layers 111” to divide its string select layers and would have expected to succeed when doing so.

220. I understand that it is typically obvious to combine two embodiments disclosed adjacent to each other in a prior art patent and does not require a leap of inventiveness. I also understand that predictable variations of the prior art’s teachings are also obvious.

221. In my opinion, this is all a POSITA would have considered the application of Park’s “isolation insulating layers 111” to its upper string select layer to be. Park already teaches that these layers can be used to divide select gates into portions. A POSITA would have considered use of the layers in other places—including to divide the string select lines—for the same purpose they already serve to be nothing more than a routine, obvious extension of Park’s existing teachings.

222. Indeed, confirming the obviousness of this approach, numerous prior art references use dielectric trenches for the same purpose. *See, e.g.*, Ex. 1017, 7:40-44, Fig. 3 (“string selection gate electrodes 202a and 202c” “separated” by “a cutting insulation pattern 118”); Ex. 1016, 6:5-15, Fig. 4A (“string select transistor SST” is “divided into a plurality of regions electrically separated” by “insulating layer 173”); Ex. 1018, [0058], Fig. 4B (“upper electrodes ELb ... may be spaced apart .. by an insulating separation pattern 50”).

223. Further, a POSITA also would have considered it obvious to include a dielectric trench in Park's upper string select layer because doing so would allow non-selected strings to be completely isolated on a unit area basis. This would in turn reduce parasitic capacitance.

224. To the extent this is not obvious over Park alone, in my opinion this limitation would have been obvious over the combination of Park and Shibata for the reasons discussed in Ground 2 below.

3. Claim 3

225. Claim 3 depends on claim 2 and further requires that:

[3] "the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate."

226. This, in my opinion, is rendered obvious by Park.

227. Park explains that both its "string select line" and "ground select line" are "separated from each other" in the same location: "between the first to eighth unit areas UA1 to UA8." Ex. 1004, 6:1-4; *see also id.*, 7:20-29 (similarly explaining that the select lines are "separated" "at the boundaries between" "unit areas UA1 to UA8"); 16:26-37 (similar).

228. This allows the "memory cells of the respective first to eighth unit areas UA1 to UA8 [to] be independently controlled." Ex. 1004, 10:65-67.

229. Again, as discussed in connection with claim 2, in certain of Park's embodiments, the SSL is located over the GSL. *See supra* discussion of claim 2, limitation [2.B].

230. Because both the SSL and the GSL are stacked this way and separated at the same location (the boundaries of unit areas UA1-UA8), a POSITA would have considered it obvious and understood that when dielectric trenches are used to effect this division, they will be *“aligned.”*

4. Claim 4

231. Claim 4 depends on claim 2 and further requires that:

[4] “one or more common source regions further pass through the TSG, and the one or more common source regions, the first dielectric trenches, and the second dielectric trenches extend parallel to each other in the length direction of the substrate.”

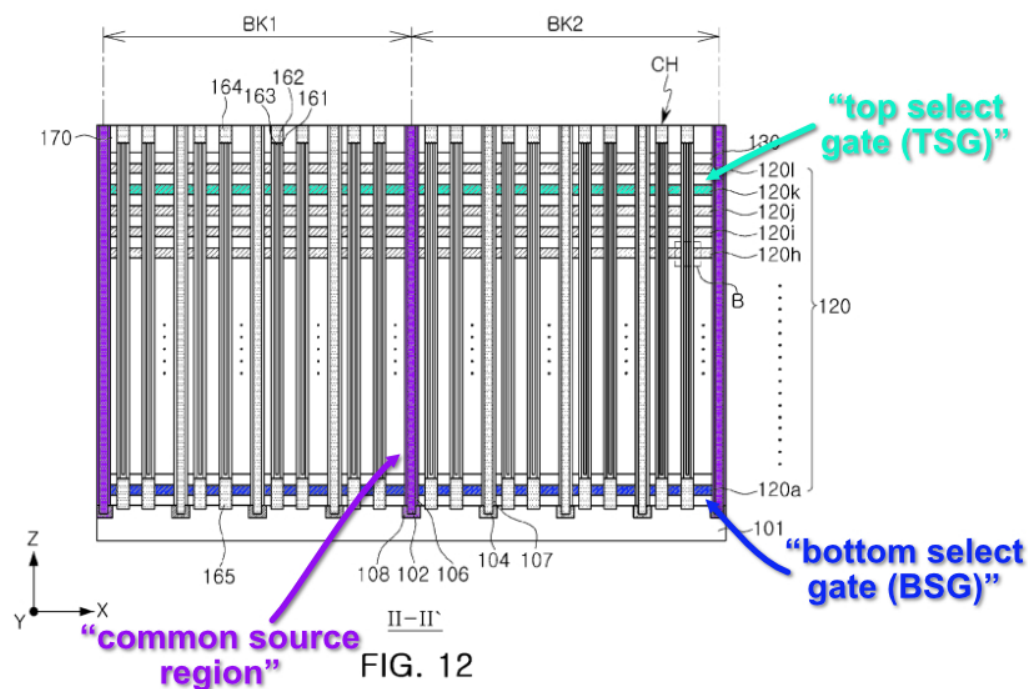
232. This, in my opinion, is rendered obvious by Park.

233. As explained when discussing claim 1 in Ground 1, Park's memory device includes *“one or more common source regions”* (the common source lines 102). *See supra* discussion of limitation [1.F].

234. According to Park, these common source lines 102 pass through all of its “gate electrode layers 120.” Ex. 1004, 10:46-67. This includes Park's *“TSG”* (string select line 120k). *See id.*, 2:1-3 (“a plurality of first common source lines divid[e] the gate structure into a plurality of blocks); 7:20-29, 40-42 (noting that “string select line 120k” is “separated” “at the boundaries between the first to eighth

unit areas UA1 to UA8” formed by, among other things, “the first common source line 102”).

235. This is shown in Figure 12. Park’s “*common source regions*” (common source lines 102, annotated purple) pass through all the gate electrode layers 120, including Park’s “*TSG*” (string select line 120k, annotated light blue):

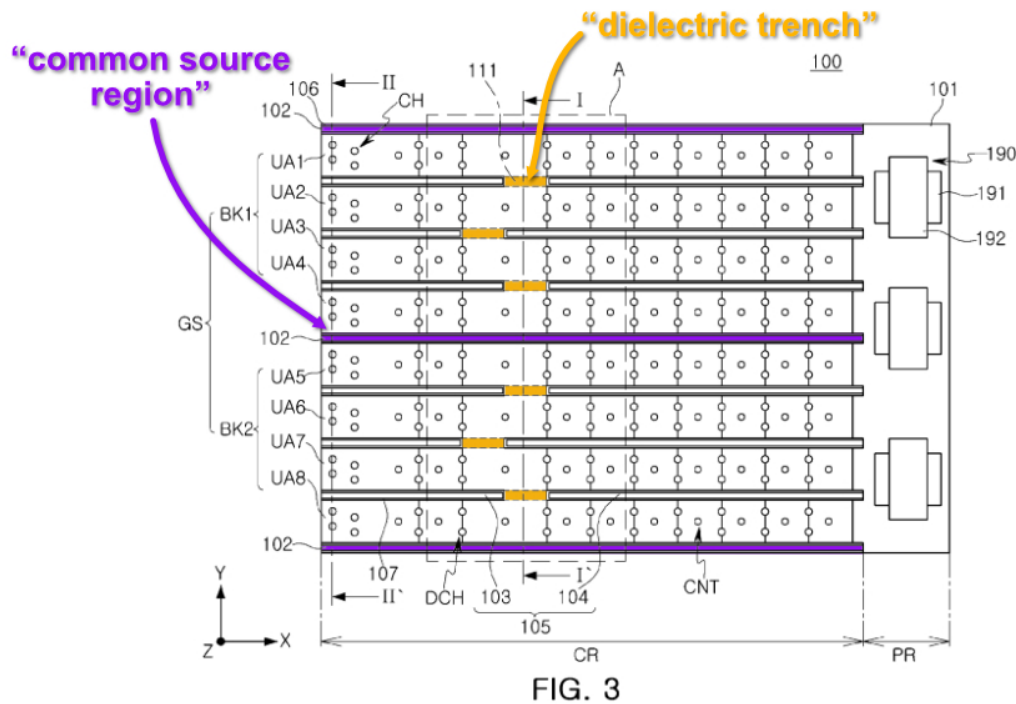


Ex. 1004, Fig. 12 (annotated).

236. In my opinion, Park’s “*common source regions*” also “*extend parallel to*” the “*first dielectric trenches, and the second dielectric trenches*” “*in the length direction of the substrate.*”

237. Per Park, common source lines 102 “extend[] in the first direction, e.g., the X-axis direction” to “divide[]” the memory device into “first and second blocks BK1 and BK2....” Ex. 1004, 10:46-49; *see also id.*, 1:53-54; 1:63-2:3.

238. As shown in Figure 3 below, Park’s “**dielectric trenches**” (isolation insulating regions 111 and the equivalent regions that would be present in the string select layer, annotated orange) extend in the same direction:



Ex. 1004, Fig. 3 (annotated).

5. Claim 5

239. Claim 5 depends on claim 2 and further requires:

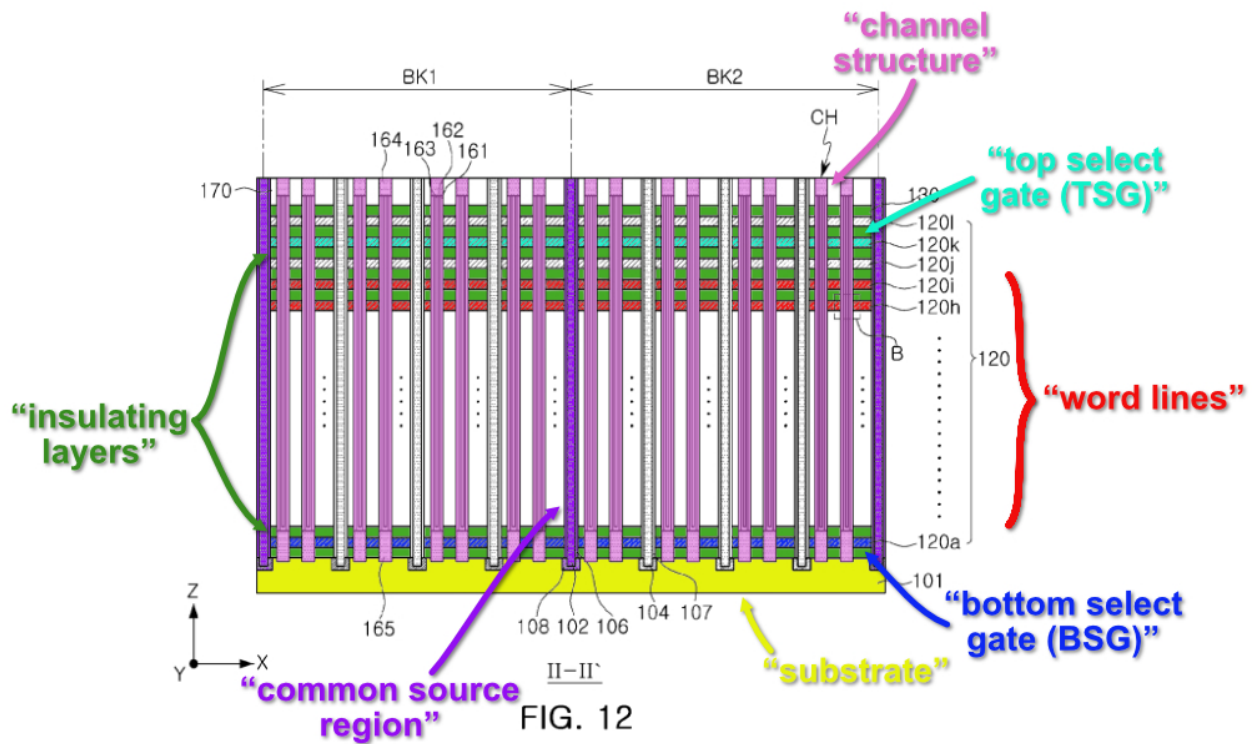
[5] “a plurality of channel structures formed over the substrate along a height direction of the substrate that is perpendicular to the substrate, wherein each of the plurality of channel structure passes through the BSG, the plurality of word lines, the TSG, and the plurality of insulating layers.”

240. This, in my opinion, is taught by Park.

241. Again, Park’s memory device “includes a plurality of channel structures extending vertically through ... the gate electrode layers so as to each extend in a direction perpendicular to the upper surface of the substrate.” Ex. 1004, 1:49-52; *see also id.*, 5:34-41 (explaining that “cell channel structures CH ... extend in ... the Z-axis direction, perpendicular to an upper surface of the substrate 101” to “penetrate through the gate electrode layers and a plurality of interlayer insulating layers disposed thereon.”); 11:11-14 (similar).

242. Figure 12—annotated below—shows this. A “***plurality of channel structures***” (channel structures CH, annotated pink) are “***over the substrate along a height direction of the substrate that is perpendicular to the substrate***” (the CH extend vertically in the Z-axis direction from substrate 101, annotated yellow).

243. Further, these “***channel structures***” “***pass[] through the BSG***” (ground select layer 120a, annotated blue), “***the plurality of word lines***” (the intermediate conductive layers, annotated red), “***the TSG***” (string select layer 120k), “***and the plurality of insulating layers***” (annotated green):



Ex. 1004, Fig. 12 (annotated).

6. Claim 6

244. Claim 6 depends on claim 1 and further requires:

[6] “a plurality of dummy channel structures formed along the a height direction of the substrate that is perpendicular to the substrate, the plurality of dummy channel structures passing through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate.”

245. This, in my opinion, is taught by Park.

246. Park’s memory device “includes a plurality of channel structures extending vertically through ... the gate electrode layers so as to each extend in a direction perpendicular to the upper surface of the substrate.” Ex. 1004, 1:49-52; *see also id.*, 4:64-65.

247. The “memory device” also includes “at least one dummy string DS” with “a dummy channel” “DCH[.]” Ex. 1004, 4:55-65; *see also id.*, 5:30-32 (referencing both “cell channel structures CH and the dummy channel structures DCH”).

248. The “cell channel structures CH may extend to the substrate 101 through the interlayer insulating layer 170 and the gate electrode layers 120a to 120l...” Ex. 1004, 11:11-14.

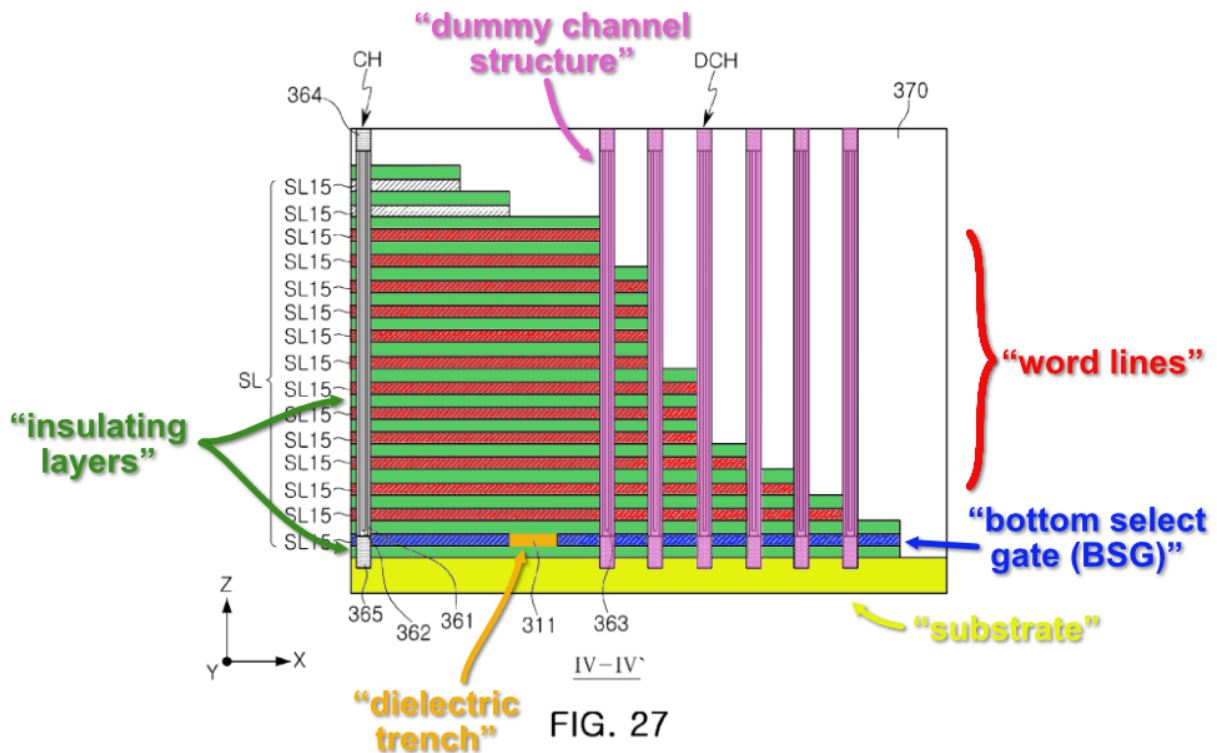
249. The “dummy channel structures DCH ... have a structure similar to that of the cell channel structures CH.” Ex. 1004, 11:19-21; *see also id.*, 5:34-41 (explaining that “cell channel structures CH and the dummy channel structures DCH ... extend in ... the Z-axis direction, perpendicular to an upper surface of the substrate 101” to “penetrate through the gate electrode layers and a plurality of interlayer insulating layers disposed thereon.”)

250. As exemplified in the below annotated version of Figure 27, Park teaches what this claim requires.

251. A “*plurality of dummy channel structures*” (the DCH, annotated pink) are “*formed along ... a height direction of the substrate that is perpendicular to the substrate*” (the DCH extend vertically in the Z-axis direction).

252. Further, these “*dummy channel structures*” “*pass[] through the BSG*” (the lowest sacrificial layer that will later be replace with conductive material,

annotated blue), ***“the plurality of word lines”*** (the intermediate sacrificial layers that will also be later replaced with conductive material, annotated red), ***“and the plurality of insulating layers”*** (annotated green), ***“to extend into the substrate”*** (annotated yellow):



Ex. 1004, Fig. 27 (annotated).

7. Claim 7

253. Claim 7 depends on claim 5 and further requires:

[7] “a plurality of memory cell sub-blocks, each of the memory cell sub-blocks including a plurality of respective channel structures that are connected to a same sub-BSG and to a same sub-TSG, each of the memory cell sub-blocks being operated individually.”

254. This, in my opinion, is taught by Park.

255. As explained above, Park's "memory device 100" includes a "cell region CR" with a "gate structure GS" that can be "divided into a plurality of blocks BK1 and BK2." Ex. 1004, 4:61-5:7. "[A] plurality of cell channel structures CH" pass through the blocks' "gate structure." *Id.*

256. Each block includes a portion of Park's "memory cell array" (and thus a portion of its cell channel structures CH). Ex. 1004, 3:39-40; *see also id.*, Fig. 3 (showing multiple channel structures CH in each block).

257. The blocks are further sub-divided into "unit areas." Ex. 1004, 3:39-40; *see also id.*, Fig. 3. For example, "first block BK1 includes first to fourth unit areas UA1 to UA4" while "second block BK2 includes fifth to eighth unit areas UA5 to UA8." *Id.*, 5:8-10.

258. And according to Park "the string select line and the ground select line may be separated from each other between the first to eighth unit areas UA1 to UA8." Ex. 1004, 6:2-5. This allows the unit areas to be "independently controlled." *Id.*, 7:17-29, 10:55-67.

259. In my opinion, Park's unit areas UA1-UA8 correspond to the claimed "***memory cell sub-blocks.***" Each unit area includes "***a plurality of respective channel structures***" (structures CH) that are "***connected to a same sub-BSG***" (the portion of the ground select line in the unit area) and "***to a same sub-TSG***" (the

9. Claim 9

263. Claim 9 depends on claim 5 and further requires that:

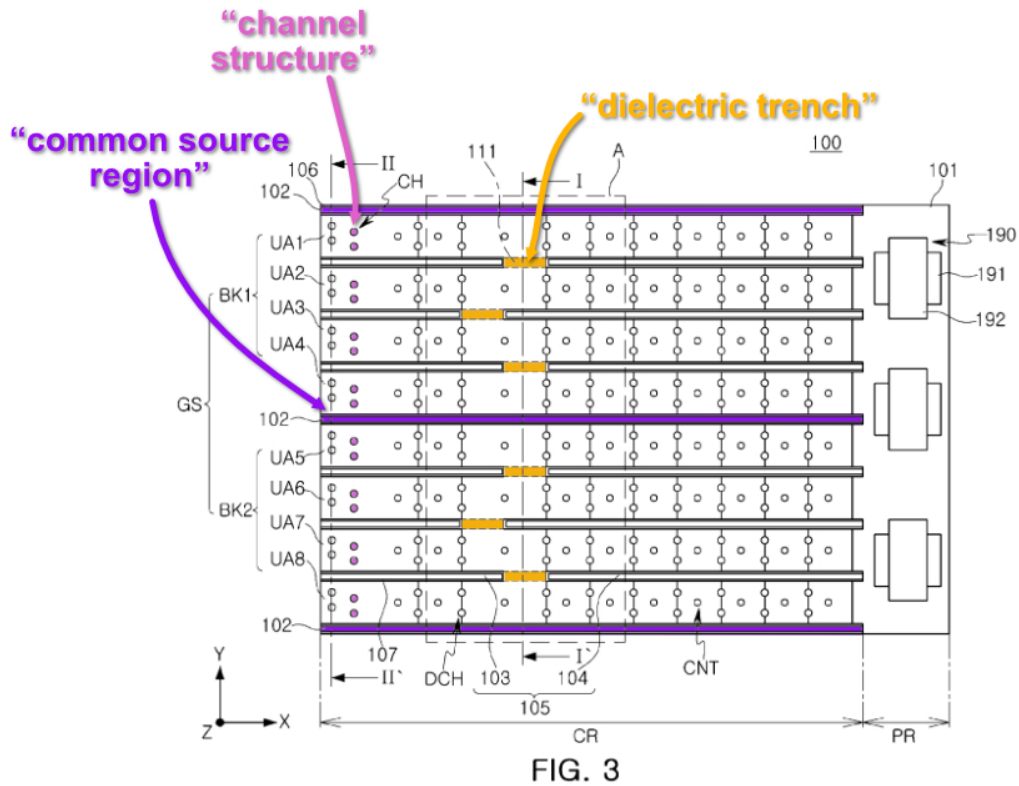
[9] “the one or more second dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate so that a plurality of channel structures are disposed therebetween.”

264. This, in my opinion, is taught by Park.

265. As explained above when discussing claim 3, a POSITA would have considered it obvious to locate Park’s “first dielectric trenches” and “second dielectric trenches” over each other. *See supra* discussion of claim 3.

266. This, in my opinion, results in what this claim requires.

267. The “*second dielectric trenches*” (annotated orange below) are “*alternatively disposed in the width direction of the substrate*” (the Y-axis direction) with the “*common source regions*” (common source lines 102). And there are a “*plurality of channel structures*” (channel structures CH, annotated pink) located between the trenches and common source regions:



Ex. 1004, Fig. 3 (annotated).

10. Claim 10

268. Claim 10 depends on claim 1 and further requires:

[10] “one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.”

269. This, in my opinion, is rendered obvious by Park.

270. Park teaches the claimed “*dummy BSGs*” that are “*between the plurality of word lines and the BSG*” and are “*spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.*”

271. According to Park, its “gate electrode layers may provide at least one dummy line between the string select line and the word lines or between the ground select line and the word lines.” Ex. 1004, 5:26-29; *see also id.*, 4:25-28 (explaining that “dumm[ies] ... may also be disposed between the ground select transistor GST and the first memory cell MC1, and between the string select transistor SST and the n-th memory cell MCn”); 7:2-7 (similarly referencing the inclusion of a “dummy line”); 16:9-17 (explaining that “dummy line[s]” may be located between both the “ground select line” and the “word lines,” and the “string select line” and the “word lines”).

272. All of Park’s gate electrode layers—including the dummy layers—are separated from adjacent layers by “insulating layers.” Ex. 1004, 5:17-26; 6:49-52; 10:34-45.

273. Next, a POSITA would have considered it obvious that Park’s “*first dielectric trenches*” (isolation insulating layers 111) would pass through not only its “*BSG*” (the ground select lines) but also its “*dummy BSG*” (the dummy lines adjacent to the ground select lines).

274. According to Park, its “dummy lines” may also be “separated,” e.g., by the common source. *E.g.*, Ex. 1004, 7:39-43.

275. And because Park associates these dummies with its select lines (*see* Ex. 1004, 5:26-29, 7:2-7), in my opinion a POSITA would have understood that at

least the dummies adjacent to the select lines would be—or at the very least obviously could be—structured and divided in the same way as the select lines themselves.

276. While Park does include embodiments where only its select lines—and not the dummy lines—are separated into portions corresponding to unit areas UA1-UA8, in my opinion a POSITA would have recognized that these are only non-limiting examples.

277. When the '623 patent was filed, a range of different separation structures were known and used in the prior art.

278. This includes structures separating only a single select gate layer, *see, e.g.*, Ex. 1004, Fig. 11 (layer 111 separating line 120a), or all the conductive layers, *see, e.g.*, Ex. 1005, Fig. 3 (element 60 separating a stack of conductive layers 70).

279. It was also known that a single dielectric trench could be structured to pass through and similarly divide multiple adjacent electrode layers. *See* Ex. 1018, [0058], Fig. 4B (trench 50 dividing two adjacent layers ELb).

280. There are other reasons why a POSITA would have considered it obvious to extend the dielectric trench through not only the select gate layers, but also at least some of the adjacent dummy select gate layers.

281. For instance, a POSITA would have understood that dummy cells, including dummy lower and upper select transistors, serve the purpose of

suppressing leakage current such as drain-induced barrier lowering current (DIBL) and trap assisted band-to-band tunneling current (BTBT) and suppressing hot-carrier injection (HCI). They also play a role in data disturb characteristics. *See, e.g.* Ex. 1012, 130 (explaining that dummies address the “floating body of the memory cells” along a “vertical channel” by, among other things, addressing the behavior of “hot carriers” “located at the edge of the NAND string”); 144 (similarly explaining that dummies “can reduce the voltage drop going from the self-boosting voltage to the voltage applied to the DSL” and “are helpful for inhibiting the hot carrier generation that might take place on the edge wordline (in practice, they reduce the lateral electric field).” A POSITA would have recognized that separating dummy BSG into sub-dummy BSGs, for example by using dielectric trenches, would have the potential to help the dummy BSGs in serving their purposes. This is because the loading effects on a specific sub-BSGs is reduced and more symmetrical. Separating dummy BSG into sub-dummy BSGs also would have had the potential to reduce the load on the drivers associated with each of the various sub-units. Given these potential benefits, a POSITA would have considered the extension of the dielectric trench through the dummy BSG layers to be an obvious design variation.

282. In view of these various known options, in my opinion, a POSITA would have considered it highly obvious that both Park’s GSL and the adjacent dummy layer would be divided by the same dielectric trench.

11. Claim 11

283. Claim 11 depends on claim 2 and further requires:

[11] “one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs, and spaced apart from the plurality of the word lines and the TSG by the plurality of insulating layers.”

284. This, in my opinion, is rendered obvious by Park.

285. As explained above when discussing claim 10, Park teaches that its memory device can include “dummy line[s]” between its “string select line” and the adjacent “word lines.” Ex. 1004, 5:26-29.

286. In my opinion, these dummy lines are the claimed “*dummy TSGs*.”

287. Moreover, a POSITA would have considered it obvious for Park’s “second dielectric trenches” to pass through not only its “*TSG*” (the string select line) but also its “*dummy TSGs*” (the dummy lines) for the same reasons explained in connection with claim 10.

288. Additionally, Park forms “dielectric trenches” by etching through already applied layers. *See* Ex. 1004, 12:65-13:1.

289. One well known and routinely used method employed in the prior art to control the extent of etching was the use of what is known as a timed etch. Here, an etchant capable of etching multiple different types of materials (including both conductive and intervening dielectric layers) is employed. The extent of etching is adjusted by controlling the amount of time during which the etchant is applied. A

POSITA would have recognized that problems can arise when using a timed etch. Application of the etchant for too long, or if etching occurs at a faster rate for some reason, could result in additional layers being unintentionally etched when there is no layer capable of stopping the etchant's progression. An example of this is shown in Figure 8B of Shibata. There, slit 61b is etched in not only an upper insulating layer 72 and the target sacrificial layer 71, but also a portion of the insulating layer 72 below the sacrificial layer. *See* Ex. 1005, Fig. 8B.

290. There is no such etch stop surface below Park's SSL. Because of this, a POSITA would have recognized that when a timed etch is employed with Park, as was routinely done in the prior art, this etching process has the potential to form a trench not only in the SSL but also in at least some of the adjoining dummy layers.

291. A POSITA would have recognized that one way to account for this and avoid problems encountered when engaging in a timed etch would have been to employ the dummy layers as a buffer. More particularly, one of the functions of the dummy layers would have been to provide a buffer ensuring that—while the trench enters some of the dummy layers—it does not reach the word lines. Showing this, it was known in the art that upper dummy gate electrodes can serve as a “buffer” between the “intermediate gate electrodes” (the word lines) and the “upper gate electrodes” (select gate lines) in a 3D NAND device. *See, e.g.,* Ex. 1021, [0060] (characterizing the upper dummy lines as “buffer ... electrode[s]”).

C. Ground 2: Claims 1-11 Are Obvious Over Park in View of Shibata

292. In my opinion, a POSITA would have considered Park and Shibata to both be within the scope of the prior art and highly relevant to the patentability of the '623 patent's claims.

293. As explained above in Ground 1, Park teaches (or renders obvious) everything claims 1-11 require, including the use of “dielectric trenches” to divide select gate layers into independently controllable portions.

294. In my opinion, claims 1-11 are also obvious for additional reasons when Shibata's teachings are applied to Park.

295. Shibata—like Park—teaches a “semiconductor memory device” with memory cells arranged in a “three-dimensional structure.” Ex. 1005, [0002]-[0003].)

296. Shibata divides its memory into independently controllable “unit[s].” *E.g.*, Ex. 1005, [0083], [0129], [0167], [0227], [0270].

297. Also, like Park, Shibata achieves this independent control by dividing one of its select gate layers into portions with trenches of dielectric material.

298. In particular, exemplified in Figure 16 below, multiple “separation portion[s] 62a” “pierce[] ... the drain-side select gate layer of the uppermost layer of the multiple conductive layers 70[.]” Ex. 1005, [0090].

299. This divides Shibata’s upper “***TSG***” (the select gate layers) into “***sub-TSGs***” (portions SDG0-SGD3):

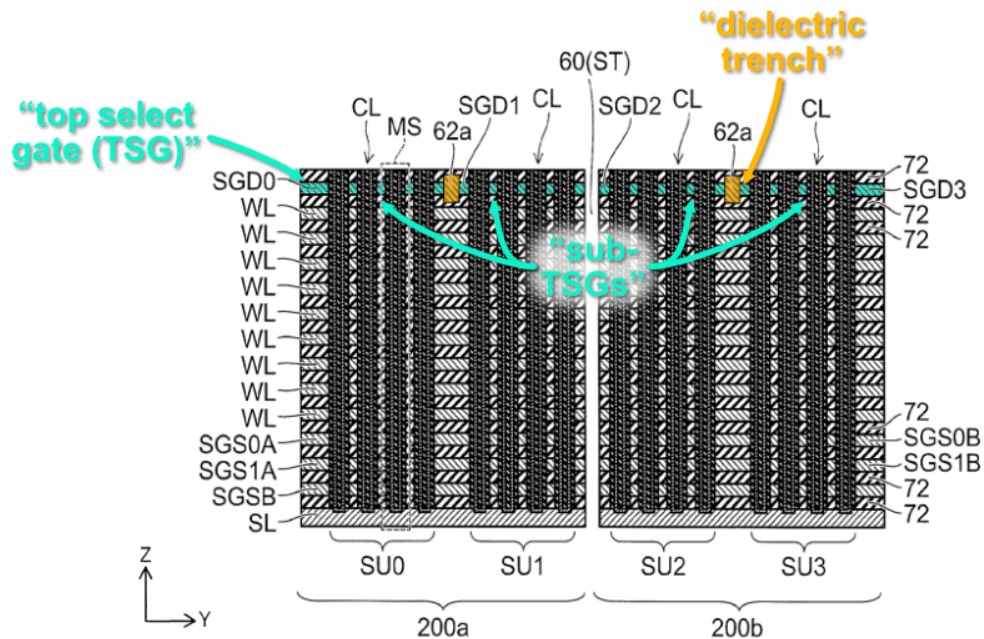


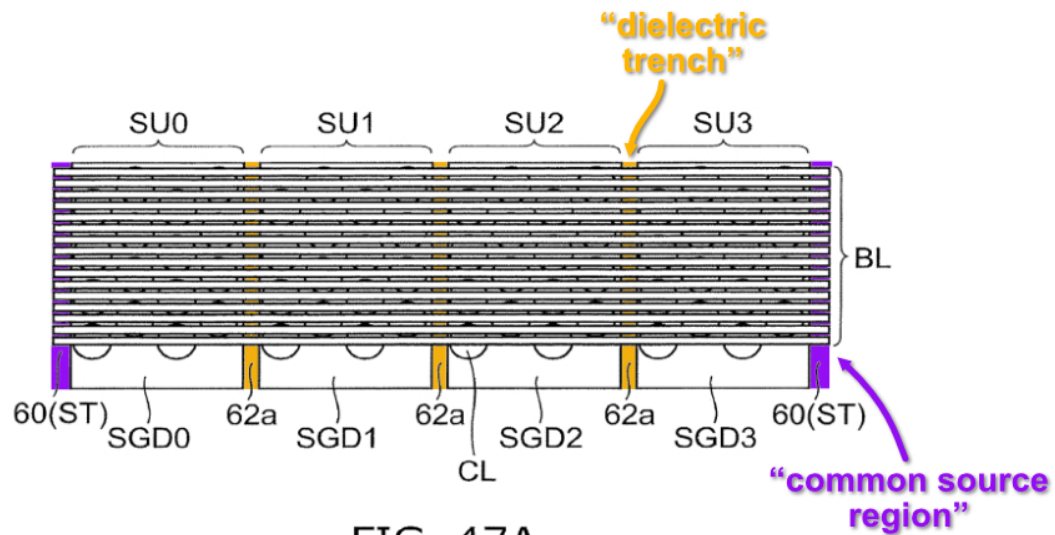
FIG. 16

Ex. 1005, Fig. 16 (annotated); *see also id.*, [0166].

300. The “separation portion 62a is an insulating film extending in the same direction as the separation portions 60 (the slits ST) piercing the entire stacked body 100.” Ex. 1005, [0166].

301. These slits can include an “interconnect portion LI” electrically connected to a lower common source “active region 10a of the substrate 10.” Ex. 1005, [0065].

302. Further, as shown below, Shibata’s “separation portion[s] 62a” traverse the entire length of its memory device for purposes of dividing the select gates:



Ex. 1005, Fig. 47A (annotated); *see also id.*, [0446].

303. In my opinion, applying this teaching to Park, a POSITA would have considered it obvious to eliminate Park's intermediate common source lines 105 and replace them with longer isolation insulating regions 111 with dimensions analogous to Shibata's separation portions 62a.

304. The below demonstrative provides one example of how this would be achieved:

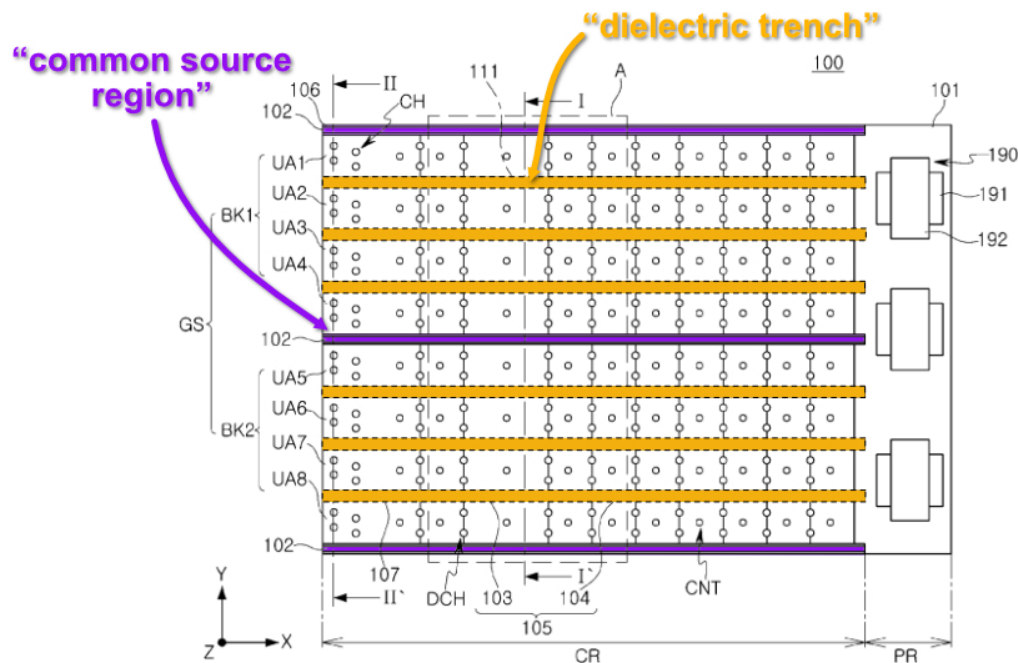


FIG. 3

305. Now, as adapted, Park includes longer ***“dielectric trench[es]”*** (the lengthened isolation insulation regions 111 shown in orange above) that span the length of its device to completely and by themselves separate its ***“BSG”*** (the ground select line) into ***“sub-BSGs”*** (portions associated with unit areas UA1-UA8).

306. Moreover, because the common source regions 105 that previously separated Park’s ***“TSG”*** (the upper string select line layers) into portions are no longer present, a POSITA also would have included ***“second dielectric trenches”***—in the form of Shibata’s “separation portion[s] 62a”—in Park’s ***“TSG.”***

307. This would allow Park’s upper string select line to continue to be divided into individually controllable portions providing various operational benefits. *See* Ex. 1004, 5:65-6:12; 7:19-29, 16:22-37; *see also supra* paragraph 223.

308. Shibata explains that using dielectric “separation portions” to effect division—instead of additional common source regions—results in an improved device. The dielectric “separation portions” “are narrower than the widths of the separation portions 60.” Ex. 1005, [0116].

309. So, by using the narrower separation portions instead of the wider common source regions to divide the memory blocks into sub-units, “it is possible to reduce the number of separation portions 60 (the slits ST) and reduce the planar size of the memory cell array.” Ex. 1005, [0118]; *see also id.*, [0154] (similarly explaining that “reduc[ing] the number of the separation portions 60 (the slits ST) having wide widths piercing the entire stacked body 100 ... reduce[s] the planar size of the memory cell array.”).

310. Other prior art includes similar teachings. *E.g.*, Ex. 1009, [0001] (explaining that “a large number of source contacts in a memory array ... may degrade the efficiency of the memory array and result in a large die size and a high fabrication cost”).

311. This, in my opinion, would have provided a POSITA with a strong motivation to replace Park’s wider common source lines 105 with additional, narrower dielectric trenches like Shibata’s separation portions 62a.

312. A POSITA would have recognized that doing so would allow Park’s memory device to be made smaller and at a lower cost per chip.

313. Alternatively, the device would be the same size, but there would be additional space for memory cell channels beneficially increasing the device's memory density.

314. While it would be improved, Park's device would continue to function as intended: the lower string select line and upper string select line would still be divided into portions allowing for independent control of unit areas UA1-UA8.

315. In my opinion, a POSITA also would have considered application of Shibata to Park to amount to nothing more than a routine, obvious design choice.

316. As shown by both Park and Shibata, it was known that select gates can be divided into individually controllable portions by either trenches of insulation or common source regions. In my opinion, a POSITA would have considered both design approaches when implementing Park.

317. A POSITA also would have had a reasonable expectation of success. Park already employs trenches of dielectric material to separate its select gates into independently controllable portions.

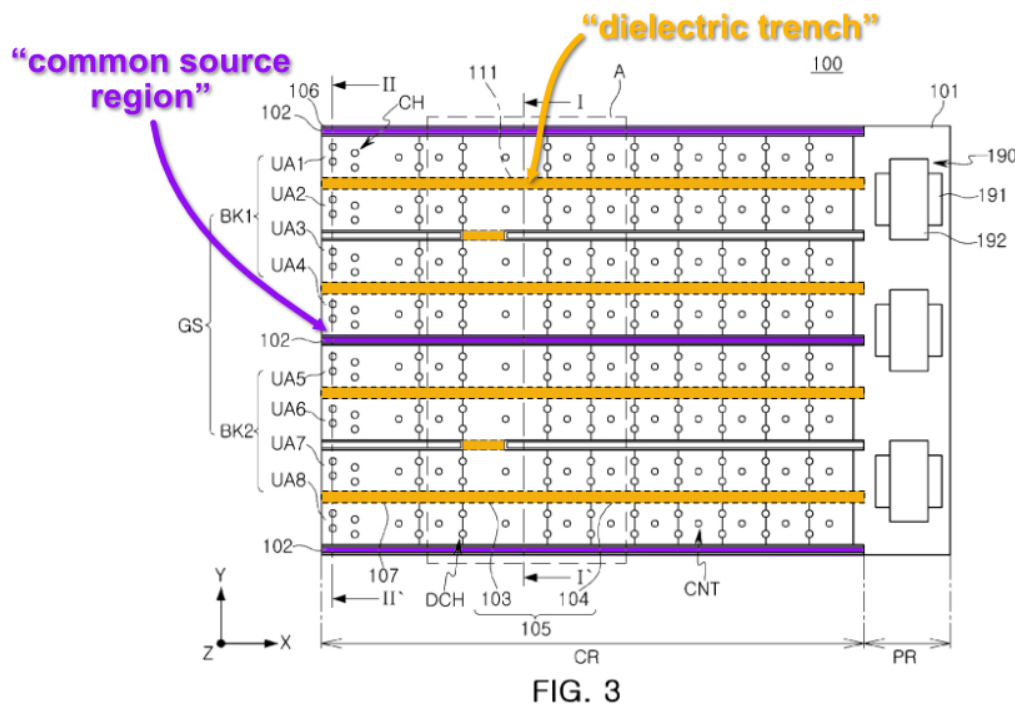
318. A POSITA would have considered lengthening Park's trenches, or including similar trenches in other gate layers, to be nothing more than an extension of an approach that Park already utilizes.

319. Park does imply that allowing "isolation regions" to face each other in a layer can present issues. *See, e.g.*, Ex. 1004, 15:35-16:2.

320. But Shibata proposes a solution to this. *See* Ex. 1005, [0324]-[0325].

321. In particular, if facing trenches of isolation inhibit the removal of sacrificial layers—resulting in “narrower” select gates with increased resistance—separate “drive circuits” can be employed in each individually controllable memory unit to maintain proper device operation. *See* Ex. 1005, [0446]-[0449].

322. In my opinion, a POSITA also would have recognized that any manufacturing issues could be minimized by replacing some—but not all—of Park’s common source lines 105 with isolation insulating layers 111:



323. In such a design, the vast majority of the layered structure is surrounded on both sides by lengthwise cuts that will eventually contain common source regions 102 and 105.

324. A POSITA would have recognized that this would ensure that the majority of the sacrificial layers are removed and replaced with conductive material, thereby improving device performance without the need for separate drivers.

D. Ground 3: Claims 1-11 Are Obvious Over Shibata in View of Park

325. In my opinion, a POSITA would have considered both Shibata and Park to be within the scope of the prior art and highly relevant to the patentability of the '623 patent's claims.

326. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Shibata and in view of Park renders claims 1-11 of the '623 patent obvious.

1. Claim 1

[1.Pre] "A memory device, comprising:"

327. To the extent this preamble language is limiting, in my opinion it is taught by Shibata.

328. In this regard, Shibata explains that it relates to a "semiconductor memory device." Ex. 1005, [0002].

[1.A] "a substrate;"

329. This, in my opinion, is taught by Shibata.

330. Shibata's memory device includes a "memory cell array 1" supported on "a substrate 10" with a "source layer (or source line) SL" on its upper surface. Ex. 1005, [0055].

331. "The substrate 10 is, for example, a silicon substrate." Ex. 1005, [0056]. "The source layer SL" can be "a semiconductor layer doped with an impurity...." *Id.* An "insulating layer 41" is present "between the substrate 10 and the source layer SL." *Id.*, [0056].

332. Shibata also teaches that the source layer SL (and associated insulating layer 41) can be replaced in any of its embodiments with an "active region (e.g., a P-type well) 10a" on the upper surface of "substrate 10." Ex. 1005, [0065].

333. This is shown in Figure 23. The "**substrate**" in this figure (the combination of substrate 10 and active region 10a) is highlighted yellow:

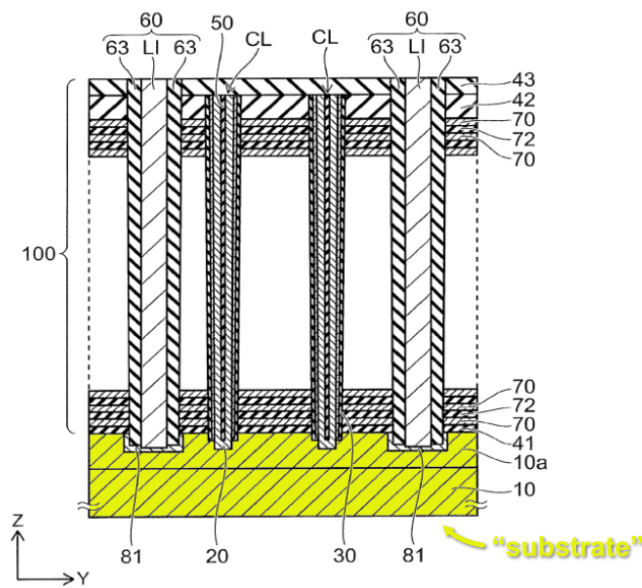


FIG. 23

Ex. 1005, Fig. 23 (annotated).

334. While Figure 2 depicts a device employing a source layer SL, in my opinion a POSITA would have understood that following Shibata's teachings, the source layer SL and the intervening insulating layer 41 could be replaced with an active region 10a like that shown in Figure 23.

335. This result would result in the following "**substrate**" (again annotated yellow):

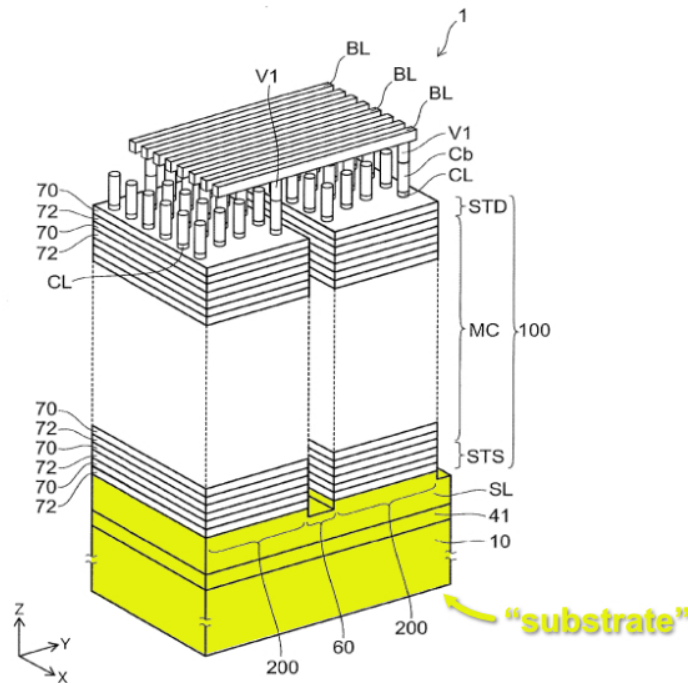


FIG. 2

Ex. 1005, Fig. 2 (annotated).

336. The same applies to Shibata's other figures: in all cases, an "active region ... 10a" on the upper surface of "substrate 10" could be employed in place of the source layer SL. Ex. 1005, [0065].

[1.B] "a bottom select gate (BSG) disposed over the substrate;"

337. This, in my opinion, is taught by Shibata.

338. Shibata's memory device includes a "stacked body 100" is located over its substrate and source layer. Ex. 1005, [0055].

339. The "stacked body" is formed from "multiple ... conductive layers stacked with an insulator interposed...." Ex. 1005, [0003]. Among the conductive layers are "select gates functioning as control gates of select transistors." *Id.*

340. "[T]he conductive layer 70 of at least the lowermost layer of the multiple conductive layers 70 functions as a control gate (a source-side select gate) of the source-side select transistor[s] STS." Ex. 1005, [0074]; *see also id.*, [0048] (explaining that the "memory device" includes multiple "select gate layers").

341. For example, in Figures 15 and 16 there is "one ... drain-side select gate layer[]" (labeled SGD) and "three ... source-side select gate layers" (labeled SGS0, SGS1, and SGSB). Ex. 1005, [0166].

342. Shibata's "**bottom select gate (BSG)**" (the lower source-side select gate or SGS layers) are annotated blue in Figure 15 below:

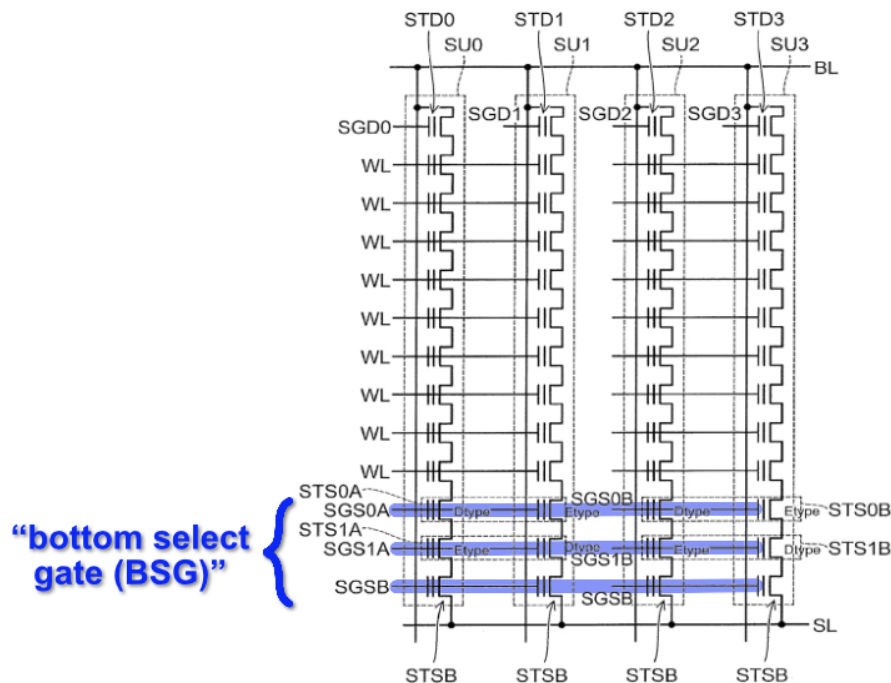


FIG. 15

Ex. 1005, Fig. 15 (annotated).

343. The same source side select gate layers are also depicted in Figure 16. As shown, they are stacked and *“disposed over”* Shibata’s substrate (the yellow annotated source layer SL, which again can be replaced with an active region 10a at the top of a substrate 10):

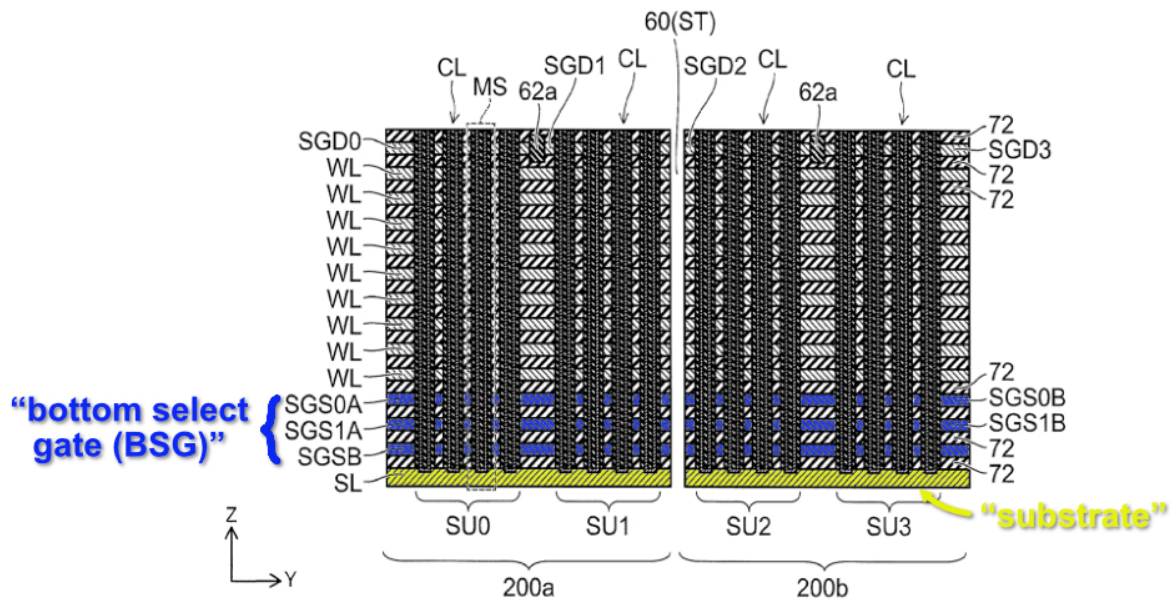


FIG. 16

Ex. 1005, Fig. 16 (annotated).

[1.C] “a plurality of word lines positioned over the BSG with a staircase configuration;”

344. This, in my opinion, is rendered obvious by Shibata.

345. Again, Shibata’s memory device includes “multiple ... conductive layers.” Ex. 1005, [0003].

346. These layers include layers of “word lines.” Ex. 1005, [0003]; *see also id.*, [0048] (explaining that the “memory device” includes “a plurality of ... word lines”)._

347. Per Shibata, “[t]he multiple layers of ... word lines WL are stacked between the drain-side select gate layer and the source-side select gate layers.” Ex. 1005, [0166].

348. Figure 15 shows a memory device including the required “*plurality of word lines*” (WL, annotated red):

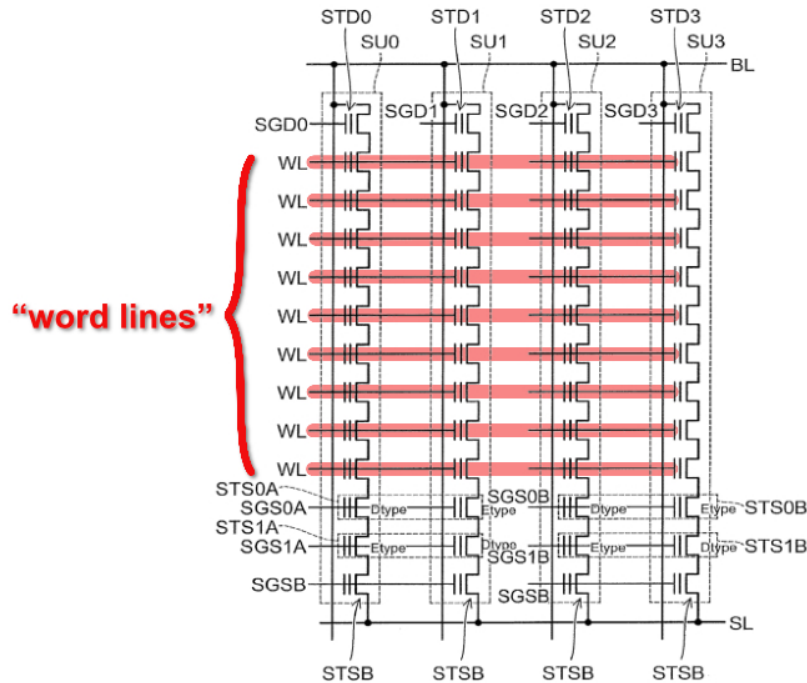


FIG. 15

Ex. 1005, Fig. 15 (annotated).

349. And as shown in Figure 16, these “*word lines*” (again annotated red) are “*positioned over the BSG*” (Shibata’s lower SGS layers, annotated blue):

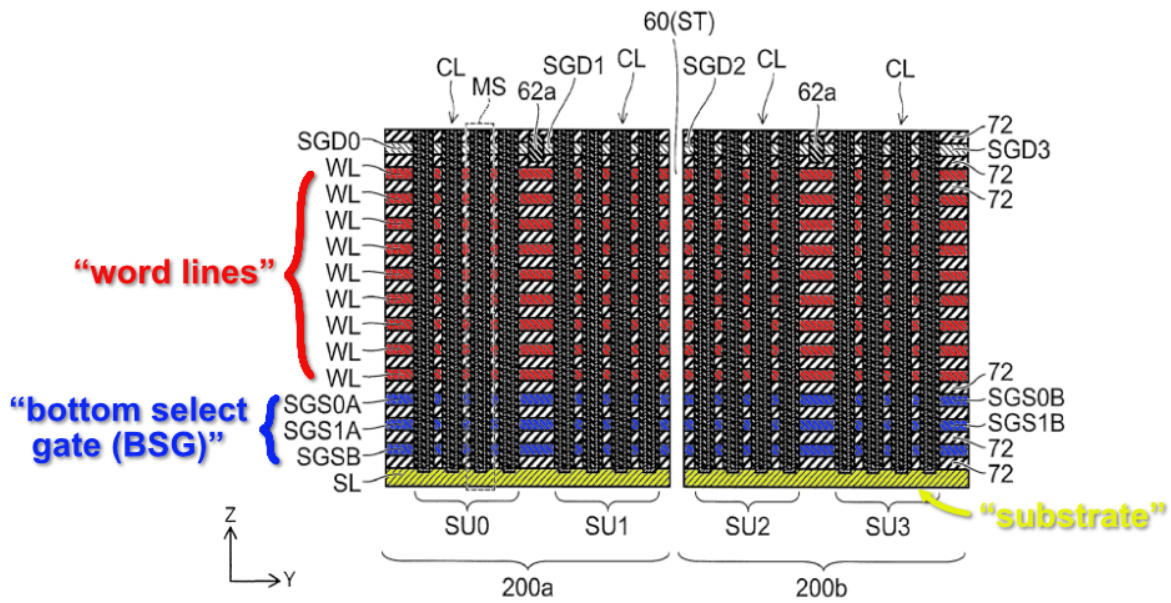


FIG. 16

Ex. 1005, Fig. 16 (annotated).

350. This limitation also requires that the *“word lines”* have a *“staircase configuration.”*

351. Shibata does not explicitly reference use of such a staircase, or discuss how electrical connection is made to its various word line layers.

352. Park, however, does. According to Park, a memory device’s “gate electrode layers”—including the word line layers—“may extend by different lengths” such that they have “a stepped structure” to allow electrical connection. Ex. 1004, 6:56-60; *see also id.*, 7:8-11 (discussing a memory device with “word lines 120*b* to 120*i*” with a “step-wise” arrangement); 8:18-50 (similarly referencing “word lines” with a “step” structure); 11:62-65 (similar); Figs. 15, 25, 32.

353. In my opinion, a POSITA would have considered it obvious to employ a “step” structure like that taught by Park with Shibata’s word lines.

354. A POSITA would have recognized that for Shibata’s memory device to function, its word lines must be electrically connected to control circuitry that supplies the word lines with signals at appropriate times during the device’s operation.

355. Shibata explains that its memory device has a “three-dimensional structure.” Ex. 1005, [003].

356. And when the ’623 patent was filed, one of the most common and routinely used methods to connect to the word lines of such a three-dimensional memory structure was via a staircase outside of the memory cell array. *See, e.g.*, Ex. 1006, 295-296 (explaining that in typical 3D NAND, “the control gates and the upper/lower SG are connected to the metal layers [via a] stair-like gate structure”); Ex. 1007, 7 (explaining that it is “common in 3D NAND” to employ a “staircase structure” to “build the connection to the wordlines and ... select gates”); Ex. 1011, [0003] (explaining that “[o]ne method of forming” required “electrical connection” to each of the “word lines” of a “conventional vertical memory array” “includes forming a so-called ‘stair step’ structure” in the word lines).

[1.D] “a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;”

357. In my opinion, Shibata also teaches a device including the required ***“plurality of insulating layers.”***

358. In particular, Shibata explains that there are “insulating layers 72 interposed” between each of the “multiple conductive layers 70” forming its “stacked body 100[.]” Ex. 1005, [0061].

359. There is also an “insulating layer 72” between the “source layer SL” (or active region 10a) “and the conductive layer 70 on the lowermost layer.” Ex. 1005, [0061].

360. Figure 16 below provides an example. As shown, there are ***“insulating layers”*** (insulating layers 72, annotated green) between the ***“substrate”*** (the SL / active region 10a, annotated yellow) and ***“BSG”*** (the SGS layers, annotated blue), between the ***“BSG”*** and ***“plurality of word lines”*** (the WL layers, annotated red), and between the ***“word lines”*** themselves:

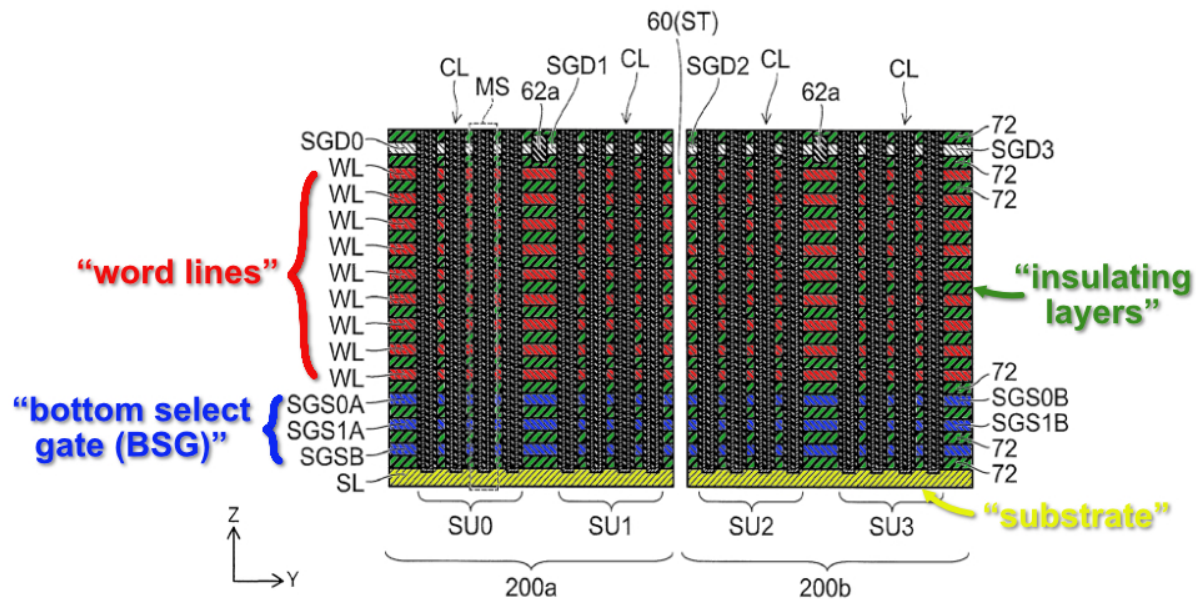


FIG. 16

Ex. 1005, Fig. 16 (annotated).

[1.E] “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and”

361. In my opinion, a POSITA would have considered this limitation obvious in view of the combined teachings of Shibata and Park.

362. Shibata explains that its memory can be divided into “block[s][,]” “sub-blocks,” and “string unit[s].” Ex. 1005, [0162]-[0163].

363. For example, in the embodiment shown in Figure 16, the memory includes “two sub-blocks 200a and 200b subdivided by three separation portions 60 (slits ST)...” Ex. 1005, [0162].

364. Each “sub-block” is then further divided into “string unit[s].” Ex. 1005, [0163].

365. In Figure 16, “first string unit SU0 and ... second string unit SU1” are in “sub-block 200a” while “third string unit SU2 and ... fourth string unit SU3 are disposed in the other sub-block 200b....” Ex. 1005, [0163].

366. Per Shibata, the portions of its select gates in each string unit can be “controlled electrically independently.” Ex. 1005, [0083].

367. The sub-blocks are surrounded by a “[s]eparation portion 60” that “extends in the X-direction” and passes through all the device’s layers. Ex. 1005, [0057].

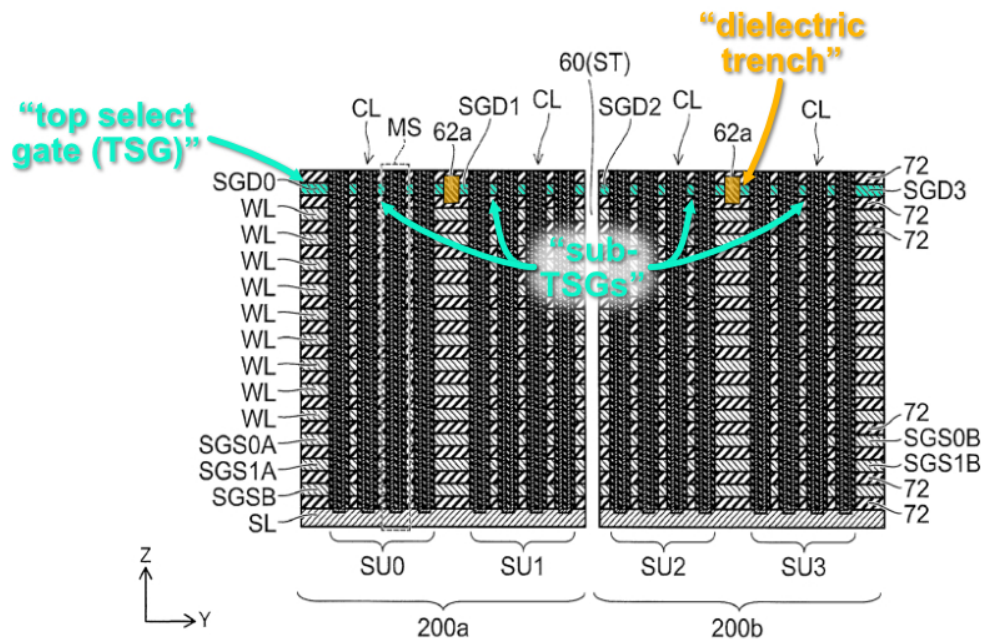
368. Different “separation portion[s] 62a” are located between the string units. Ex. 1005, [0088]-[0090].

369. In Figure 16, these “separation portions” are “insulating films that extend in the same direction as the separation portion 60 (the slit ST).” Ex. 1005, [0088]. “The separation portion 62a is disposed between” string units “adjacent to each other” and “pierces only the drain-side select gate layer of the uppermost layer of the multiple conductive layers 70, and does not divide the other conductive layers...” Ex. 1005, [0090]. The separation portions are formed from an “insulating film” such as “a silicon oxide film[.]” *Id.*, [0107], [0110].

370. In Figure 16, these “separation portion[s]” operate to divide the select gate into four pieces SGD0-SGD3. Ex. 1005, [0166].

371. Again, this allows “[t]he first to fourth drain-side select gates SGD0 to SGD3” to be “controlled electrically independently.” Ex. 1005, [0167].

372. In sum, and as this limitation requires, a POSITA would have understood Shibata to employ a “*dielectric trench*” (its separation portions 62a formed from an insulating material like silicon oxide) for purposes of separating one of its “*select gate[s]*” (the upper drain-side select gate layer) into “*sub*” gates (portions SGD0-3):



Ex. 1005, Fig. 16 (annotated).

373. While Shibata does not refer to its “separation portion” as a “trench,” this is what a POSITA would have understood it to be.

374. To form the portion, a “mask” is “formed on the stacked body 100” and “a slit ... is formed by RIE (reactive ion etching).” Ex. 1005, [0106]. “The slit ... pieces the mask 75, the insulating layer 72” and the “sacrificial layer 71” that will later be replaced with conductive material to form the select gate. *Id.*

375. The “slit” is then “fill[ed]” with “an insulating film (e.g., a silicon oxide film) 62” to form the “separation portion” that is present in the select gate layer. Ex. 1005, [0107]; *see also id.*, [0108]-[0109].

376. This process is shown, for instance, in Figures 8B and 8C below:



FIG. 8B

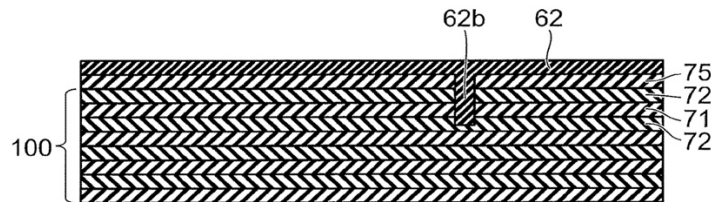


FIG. 8C

Ex. 1005, Figs. 8B-C.

377. While Shibata only employs its separation portion to divide its upper select gate and not its “**BSG**” as this limitation requires, in my opinion a POSITA would have considered it obvious to employ a similar approach in connection with its lower select gate.

378. To allow for control of its memory strings on a unit basis, Shibata employs both (1) separation portions that divide its upper select gate into units (*see* Ex. 1005, [0167]) and (2) multiple layers of bottom select gate to connect/disconnect the various string units with the lower source layer (*see* Ex. 1005, [0172], [0192]-[0200]).

379. While the multiple bottom select gates do facilitate control on a string unit basis, a POSITA would have recognized that they require additional manufacturing steps and increase the vertical size of Shibata's memory array.

380. Given this, a POSITA would have been motivated to consider other design alternatives that also allow for the same type of control Shibata already provides. Maintaining this unit control would have allowed Shibata's memory array to continue provide the benefits associated with such control, including improved granularity for array operation and reduced parasitic capacitance. *See also, e.g., supra* paragraph 223.

381. Park provides one such alternative. Rather than employing multiple bottom select gates, Park instead divides a single lower gate layer into multiple portions with isolation insulating layers 111. Ex. 1004, 5:67-6:12; 10:55-57.

382. Fig. 11 provides an example:

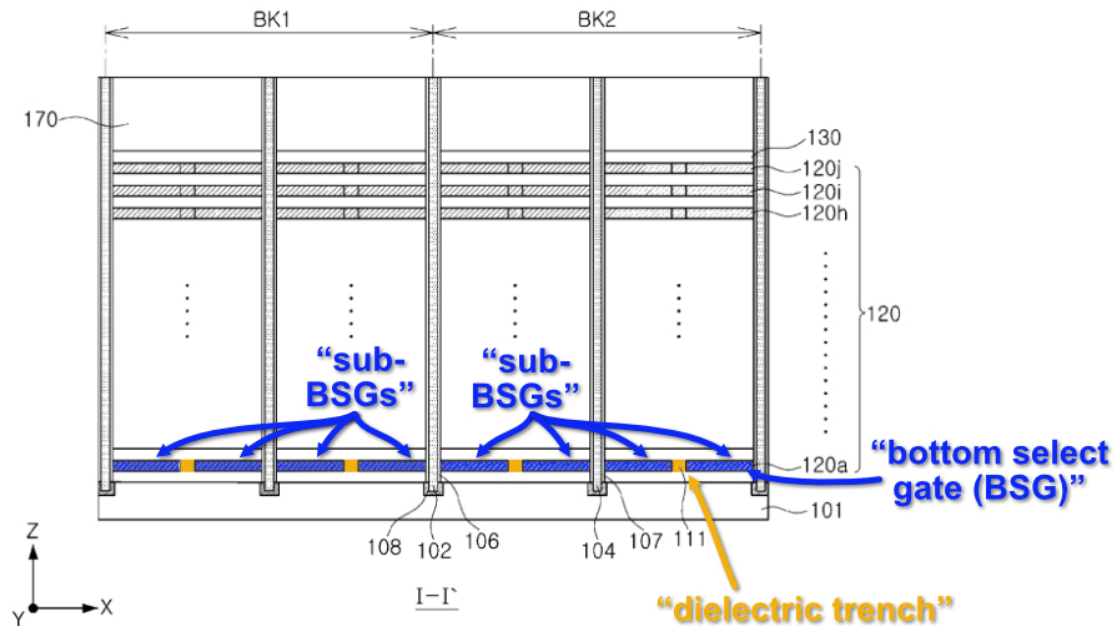
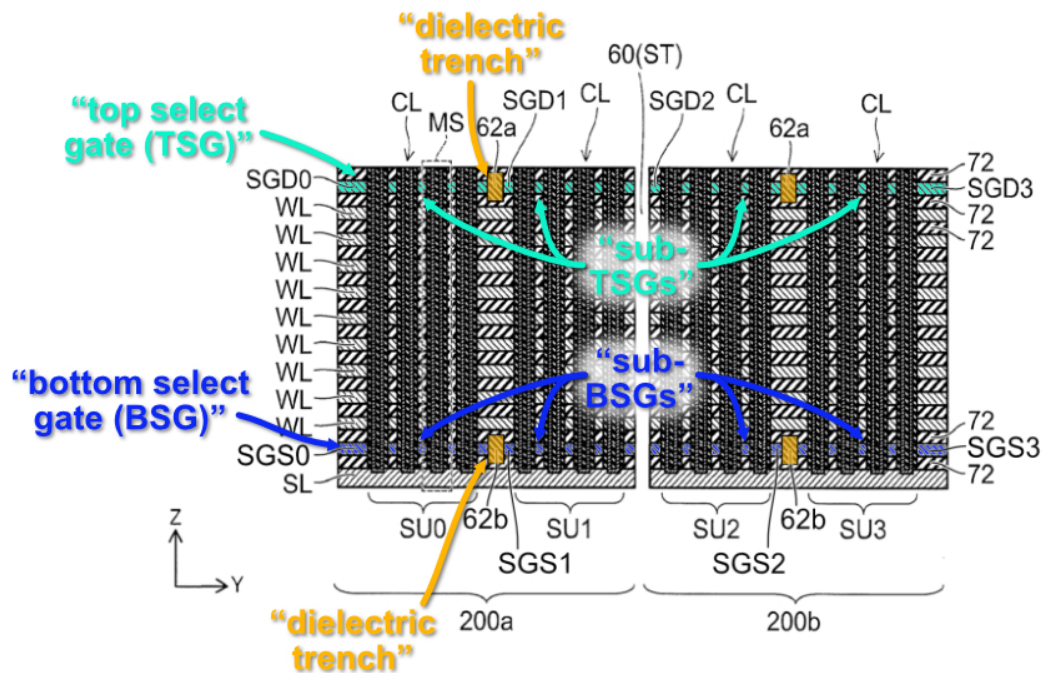


FIG. 11

Ex. 1004, Fig. 11 (annotated).

383. In my opinion, applying this to Shibata results in what this limitation requires.

384. Rather than multiple lower select gate layers, Shibata would employ a single ***“bottom select gate (BSG)”*** (lower source-side select gate or SGS layer) with ***“dielectric trenches”*** (additional separation portions 62b) ***“separat[ing] the BSG”*** into ***“sub-BSGs”*** (layer portions SGS0-SGS3). The below demonstrative created by modifying Shibata’s Figure 16 shows this. The three lower select gate layers have been replaced with a single such layer divided into portions by new separation portions 62b:



385. When the '623 patent was filed, a POSITA would have recognized that “[i]n order to reduce bit cost in 3D NAND cell, it is very important to increase the number of stacked cells.” Ex. 1006, 355.

386. Relatedly, “increasing [the] number of stacked cells is the only reasonable way to reduce the effective memory cell size in 3D cells.” Ex. 1006, 357; *see also id.*, 355; Ex. 1007, 2 (“The basic idea behind 3D NAND is to ‘grow’ cells in the vertical dimension, thus reaching a higher density per area.”); Ex. 1012, 139 (“[t]o reduce the bit size, the number of stacked cells needs to go up”).

387. But when additional layers are added to a 3D NAND device, it becomes more difficult to etch the hole in which the channel structure will be formed. Ex.

1006, 387. Further, the increased channel length resulting from added layers results in reduced cell current. *Id.*

388. This, in my opinion, would have motivated application of Park to Shibata.

389. Because Shibata's multiple bottom select gate would be replaced with a single divided gate, the number of word lines could be increased without impacting the overall height of Shibata's stack.

390. This would increase memory density without making it more difficult to etch the channel hole or impacting channel current. *See also* Ex. 1008, [0002], [0066] (explaining that there is "continuous pressure to reduce component dimensions and fit more components in a given amount of chip area" and that one of the ways to meet this goal is to "reduce an amount of memory cell string selection circuitry").

391. A POSITA also would have been motivated to apply Park to Shibata because doing so would have reduced the number of needed manufacturing steps.

392. The embodiment shown in Figure 16 of Shibata employs three bottom select gates, separated by three layers of insulation. Following Park's teachings, these six layers would be replaced by just two: a single bottom select gate (separated by dielectric trenches) and a single layer of insulation. Elimination of the other four

layers would remove some steps from the manufacturing process, increasing the manufacturing yield, and reducing manufacturing time and cost.

393. Moreover, a POSITA would have recognized that controlling isolation for the string units individually would have the added benefit of reducing the load on the drivers associated with each of the various sub-units.

394. Further, as shown by both Shibata and Park, it was well known that trenches of dielectric material could be used to divide select gates.

395. Numerous other references use trenches for the same purpose. *See, e.g.*, Ex. 1016, 7:40-42, Fig. 3 (employing a “cutting insulation pattern 118”); Ex. 1017, 6:5-15, Fig. 4A (employing a “insulating layer 173”); Ex. 1018, [0058], Fig. 4B (employing “insulating separation pattern 50”); Ex. 1019, [0158], Fig. 22 (employing “separation layer pattern 109”).

396. In my opinion, using this instead of some other method to separate Shibata’s bottom select gate into multiple portions would have been considered nothing more than routine design choice by a POSITA. In fact, this is an approach that Shibata already employs to separate its top select gate.

397. In my opinion, a POSITA also would have had a reasonable expectation of success.

398. Shibata already employs and is thus open to use of trenches of dielectric material to separate its select gate layers. In my opinion, a POSITA would have

considered use of this same approach to separate its bottom select gate to be nothing more than an extension of an approach Shibata already employs.

399. Moreover, Park would have confirmed to a POSITA that this approach can be successfully used to divide not only a memory device's top select gate, but also its bottom gate.

[1.F] “one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.”

400. This, in my opinion, is taught by Shibata.

401. According to Shibata, its memory device includes “an interconnect portion LI of a conductive material is provided in the separation portion 60 (a slit ST); and the lower end portion of the interconnect portion LI is caused to contact an N⁺-type semiconductor region 81 formed in the active region 10a of the substrate 10.” Ex. 1005, [0065].

402. This “interconnect portion LI” in the “separation portion 60”—the claimed “*common source regions formed over the substrate*”—is annotated purple in Figure 23 below.

403. As shown, it passes through Shibata's “*BSG*” (annotated blue), the “*word lines*” (annotated red), the intervening “*insulating layers*” (annotated green), and the “*TSG*” (annotated light blue):

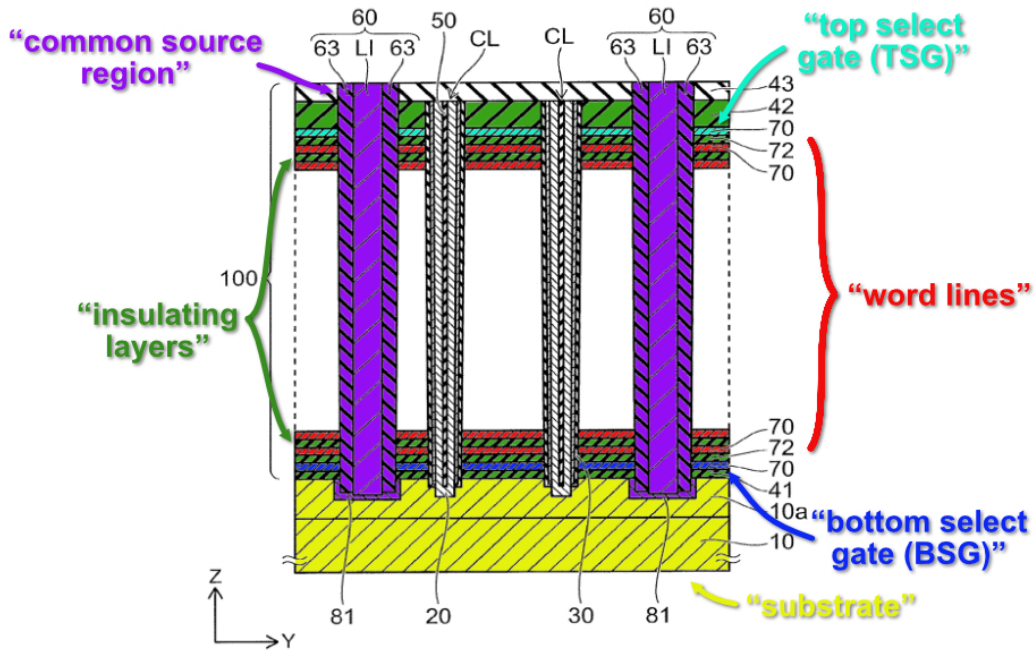


FIG. 23

Ex. 1005, Fig. 23 (annotated); *see also* Fig. 2.

404. Figure 16 similarly shows the common source region—again located in slit 60—passing through the memory device’s various layers:

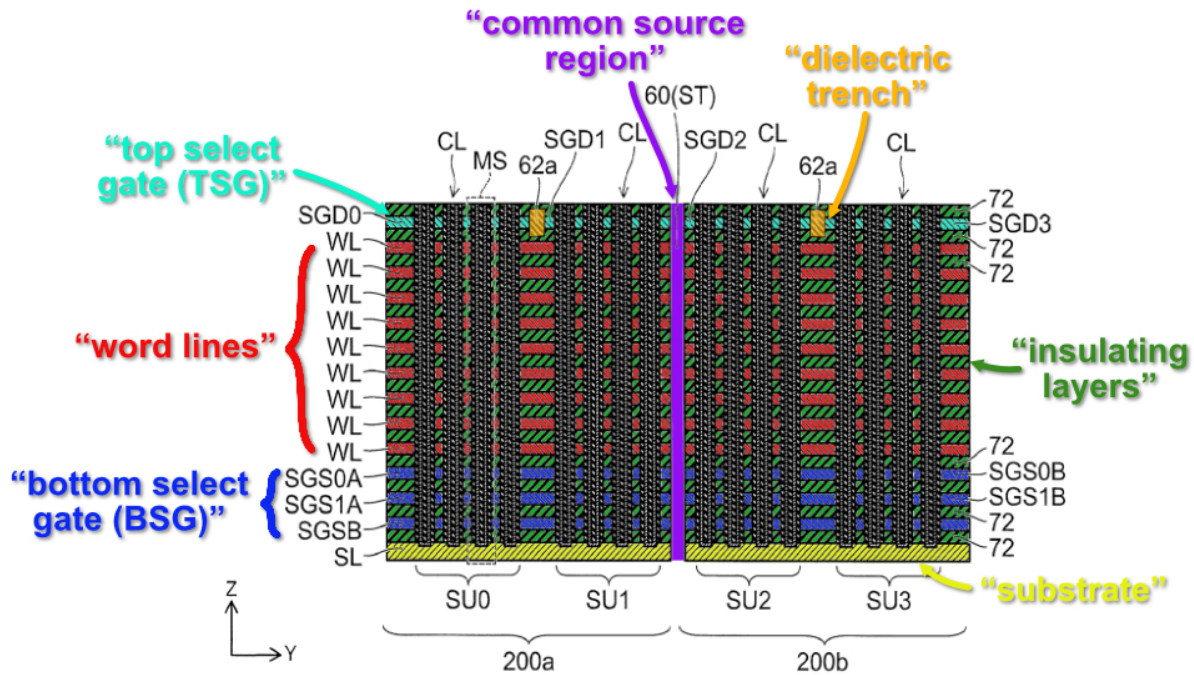
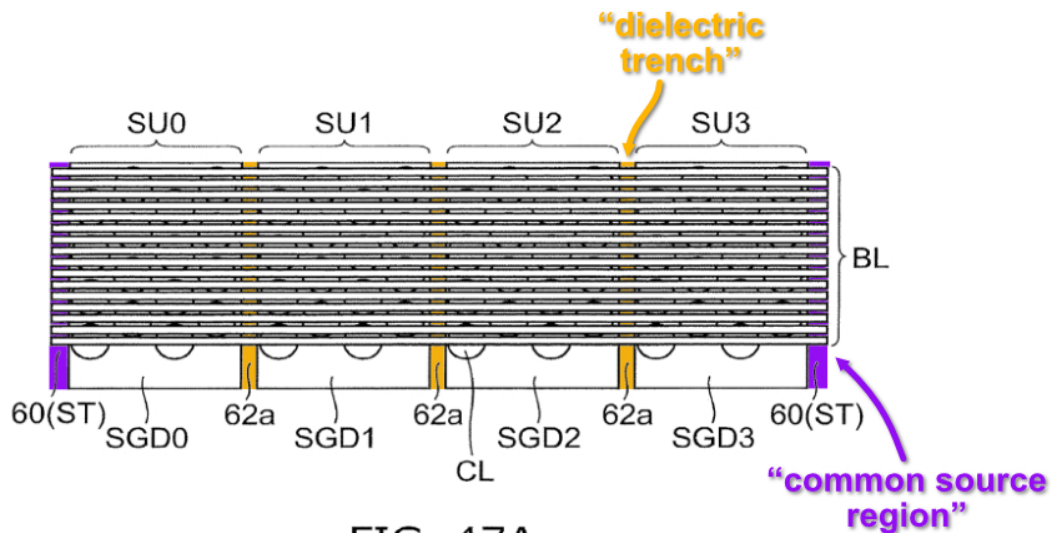


FIG. 16

Ex. 1005, Fig. 16 (annotated).

405. Shibata also teaches that its “separation portion 62a ... extend[s] in the same direction as the separation portions 60 (the slits ST) piercing the entire stacked body 100.” Ex. 1005, [0166].

406. Figure 47A provides an example. As shown, the “*common source region*” (annotated purple) “*extend[s]*” in the same “*length direction*” as the “*dielectric trench[es]*” (annotated orange):



Ex. 1005, Fig. 47A (annotated).

2. Claim 2

407. Claim 2 depends on claim 1 and further requires:

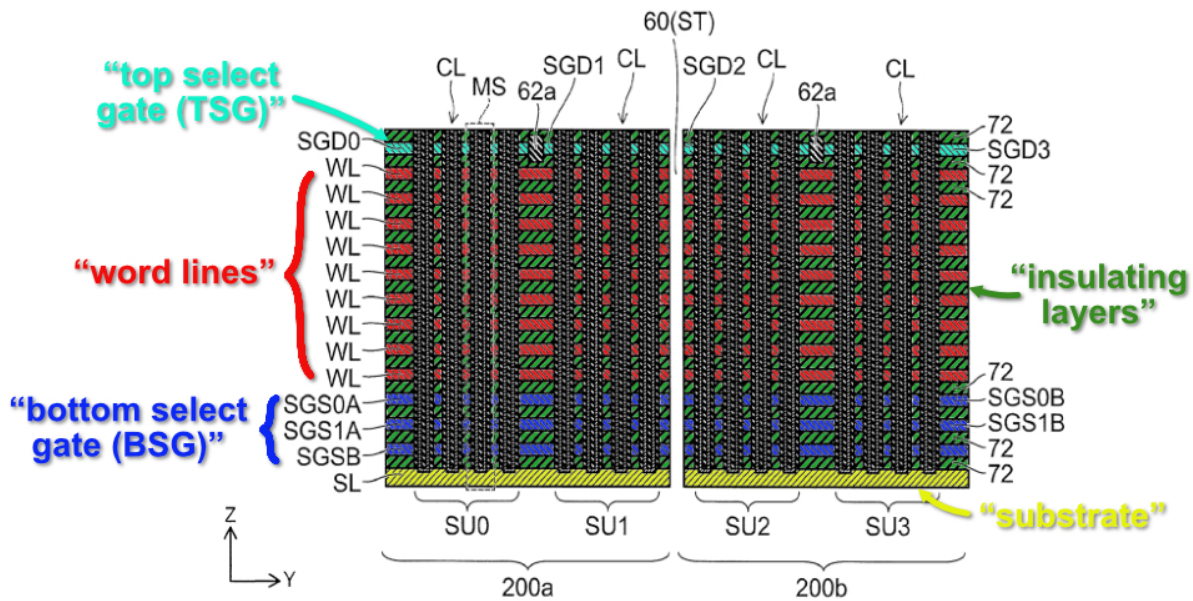
[2.A] “a top select gate (TSG) positioned over the plurality of word lines, the TSG and the plurality of word lines being spaced apart by the plurality of insulating layers; and”

408. Shibata, in my opinion, teaches what this claim requires.

409. Shibata explains that “at least the uppermost layer of the multiple conductive layers 70 functions as a control gate (a drain-side select gate). . . .” Ex. 1005, [0074]. This upper “drain-side select gate” is the claimed ***“top select gate (TSG).”***

410. Further, as explained, in Shibata, “insulating layers 72” are “interposed” between each of the “multiple conductive layers 70,” including the intermediate word lines. Ex. 1005, [0061].

411. Thus, Shibata's "**TSG**" is "**spaced apart**" from its "**word lines**" by a "**plurality of insulating layers**." This is shown below:



Ex. 1005, Fig. 16 (annotated).

[2.B] "**one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.**"

412. This is also taught by Shibata.

413. As explained when discussing claim 1, Shibata includes "**one or more second dielectric trench**" (separation portions 62a) that separate its "**TSG**" (the upper drain-side select gate layer) into "**sub-TSGs**" (portions SGD0-SDG3):

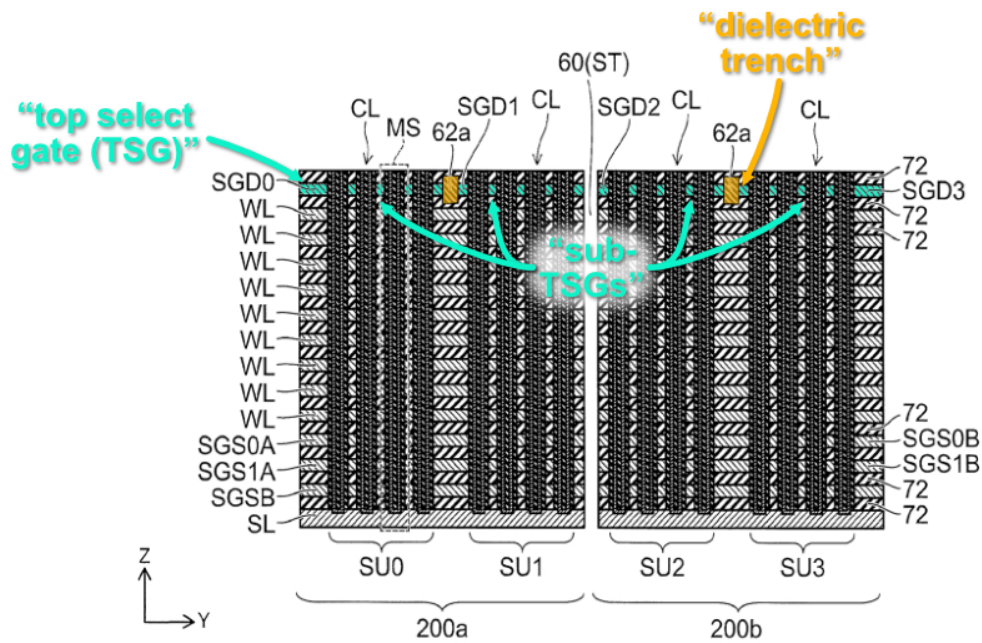


FIG. 16

Ex. 1005, Fig. 16 (annotated); *see also supra* discussion of limitation [1.E].

3. Claim 3

414. Claim 3 depends on claim 2 and further requires that:

[3] “the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate.”

415. Shibata in view of Park, in my opinion, renders what this claim requires obvious.

416. Shibata divides its memory blocks into “string units.” Ex. 1005, [0145] (“Any one of the string units ... inside the one block” can be “selected....”); [0194] (similar).

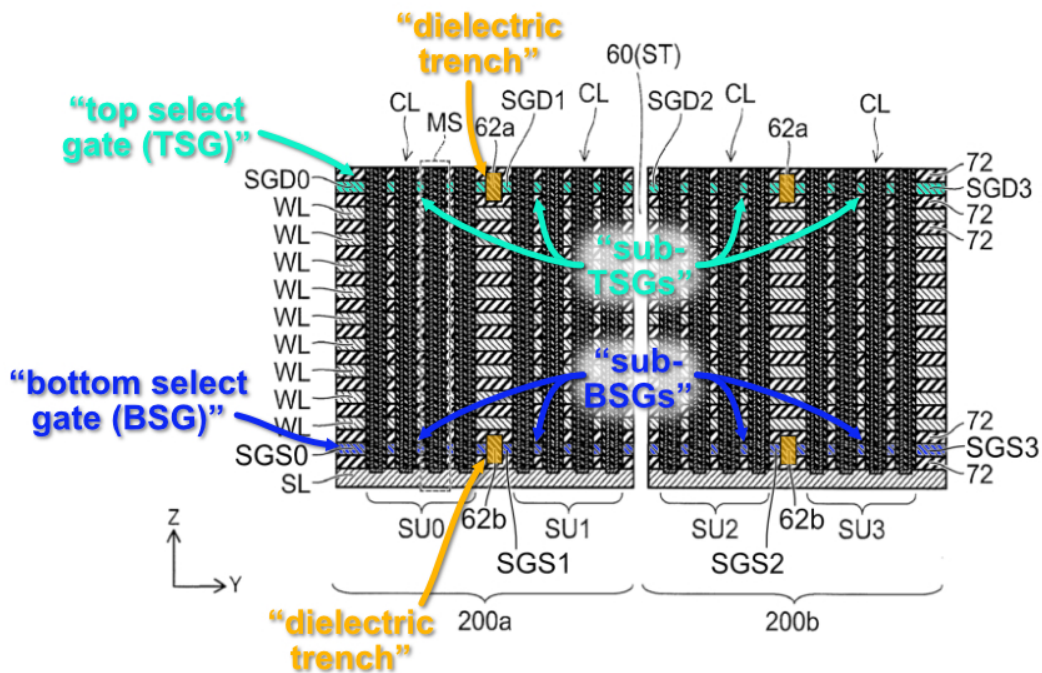
417. To allow for this, Shibata teaches that both its top and bottom select gates are structured such that they can be “controlled electrically independently” on a string unit basis. Ex. 1005, [0167], [0192]-[0200], [0227].

418. In Figure 16, “separation portion[s] 62a” divide Shibata’s top select gate. Ex. 1005, [0166]. The “separation portion[s] 62” are located between string units SU0-SU3. *See id.*, Fig. 16; [0168]-[0171].

419. Similarly, Park positions the “isolation insulating layers 111” dividing its lower select gate between individually controllable “unit areas.” Ex. 1004, 5:67-6:15.

420. Given all this, in my opinion a POSITA would have understood that the “*first dielectric trench[es]*” (the additional separation portions 62b added following Park’s teachings) dividing Shibata’s bottom select gate would also be located between the individually controllable string units SU0-SU3 such that they are “*aligned*” with the upper or “*second dielectric trench[es]*.”

421. Locating the trenches here would allow Shibata’s memory to continue to be controlled on a string unit basis:



4. Claim 4

422. Claim 4 depends on claim 2 and further requires that:

[4] “one or more common source regions further pass through the TSG, and the one or more common source regions, the first dielectric trenches, and the second dielectric trenches extend parallel to each other in the length direction of the substrate.”

423. Shibata in view of Park, in my opinion, renders what this claim requires obvious.

424. As explained when discussing claim 1, Shibata includes *“one or more common source regions”* (an interconnect portion LI within separation portion 60 / slit ST). *See supra* discussion of limitation [1.F].

425. As required, this *“common source region[]”* (annotated purple) passes through Shibata’s *“TSG”* (annotated light blue):

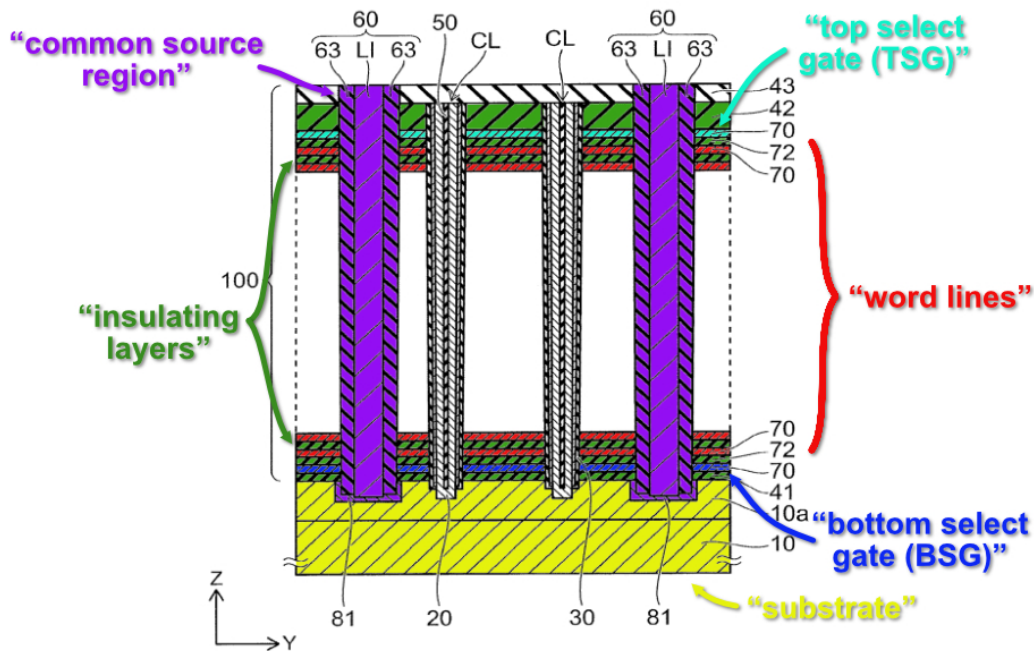


FIG. 23

Ex. 1005, Fig. 23 (annotated).

426. Shibata's "*common source regions*" also "*extend parallel to*" the "*first dielectric trenches, and the second dielectric trenches*" "*in the length direction of the substrate.*"

427. Per Shibata, the "separation portion[s] ... extend[]" in the same direction as the separation portions 60 (the slits ST) piercing the entire stacked body 100."

Ex. 1005, [0166].

428. This is shown in Figure 47A. Here, the "*common source region*" (annotated purple) "*extend[s]*" in the same "*length direction*" as the "*dielectric trench[es]*" (annotated orange).

429. Because both the “*first*” and “*second*” “*dielectric trenches*” are obviously located between the same string units, a POSITA would have understood that they both extend in the same direction:

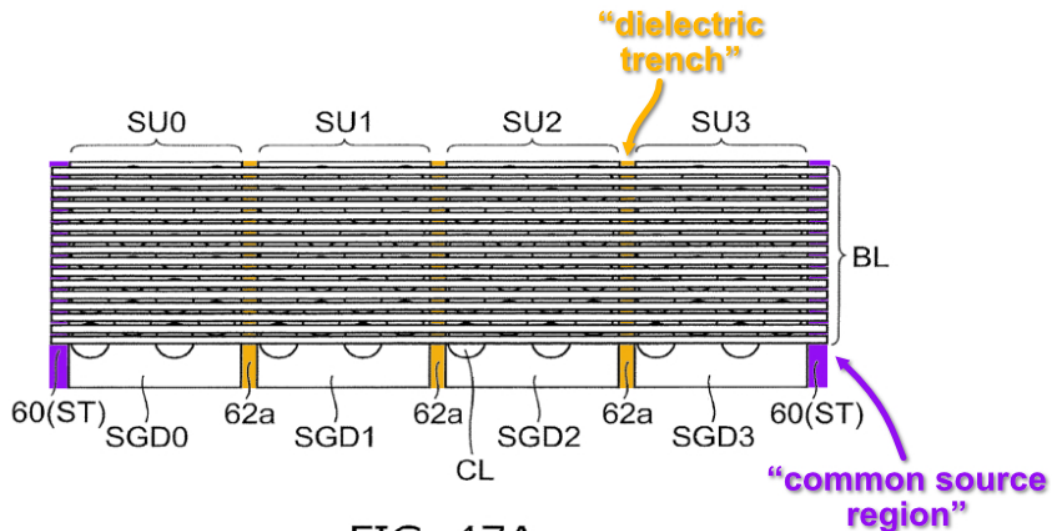


FIG. 47A

Ex. 1005, Fig. 47A (annotated).

5. Claim 5

430. Claim 5 depends on claim 2 and further requires:

[5] “a plurality of channel structures formed over the substrate along a height direction of the substrate that is perpendicular to the substrate, wherein each of the plurality of channel structure passes through the BSG, the plurality of word lines, the TSG, and the plurality of insulating layers.”

431. Shibata, in my opinion, teaches what this claim requires.

432. Shibata’s “memory device” includes a number of “memory strings” with “memory cells” arranged in “series in a first direction.” Ex. 1005, [0048].

433. Each memory string includes an associated “columnar portion[] CL.” Ex. 1005, [0055]. “The columnar portions CL are formed in substantially circular columnar configurations extending through the stacked body 100 in the stacking direction (the Z-direction).” *Id.*, [0059].

434. “The columnar portions CL pierce the stacked body 100 and reach the source layer SL” on the substrate. Ex. 1005, [0059]; *see also id.*, [0075] (noting that the “semiconductor body 20” of the columnar portions CL “pierces the multiple conductive layers 70 including the word lines [] and the select gates.”).

435. Figure 16—annotated below—shows this. A “***plurality of channel structures***” (channel structures CL, with one annotated pink) are “***over the substrate along a height direction of the substrate that is perpendicular to the substrate***” (the CL extend vertically in the Z-axis direction from substrate, annotated yellow).

436. Further, these “***channel structures***” “***pass[] through the BSG***” (the lower SGS layers, annotated blue), “***the plurality of word lines***” (the intermediate conductive layers, annotated red), “***the TSG***” (the upper SDG layer), “***and the plurality of insulating layers***” (annotated green):

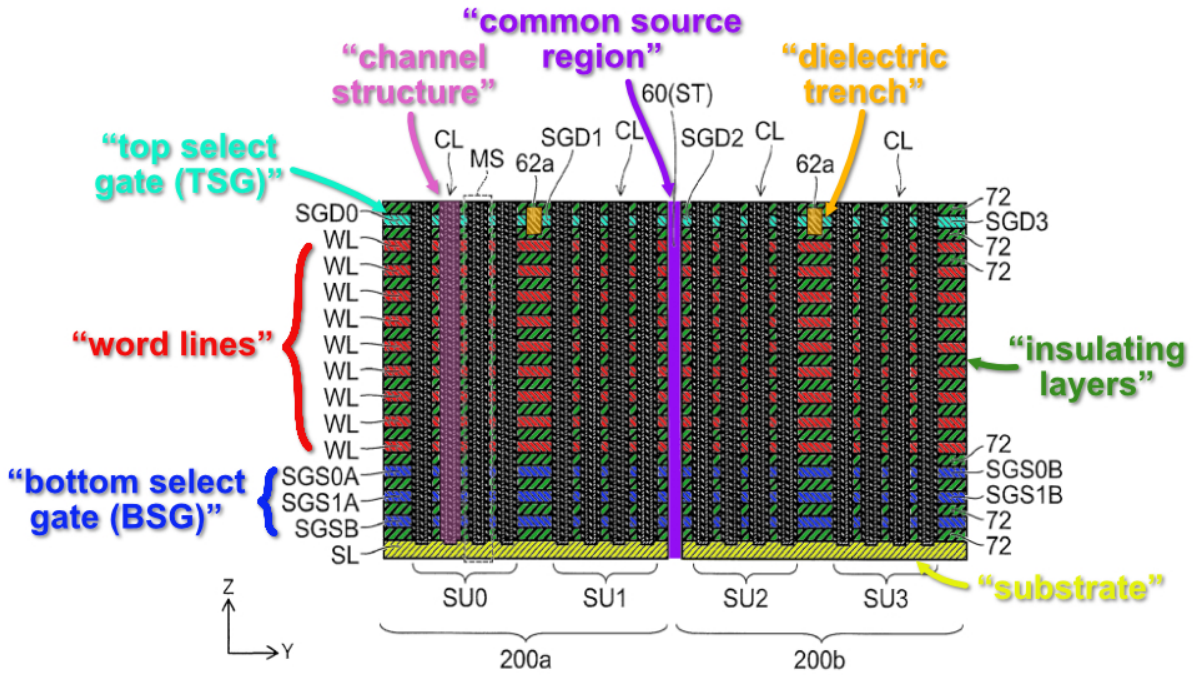


FIG. 16

Ex. 1005, Fig. 16 (annotated).

6. Claim 6

437. Claim 6 depends on claim 1 and further requires:

[6] “a plurality of dummy channel structures formed along the a height direction of the substrate that is perpendicular to the substrate, the plurality of dummy channel structures passing through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate.”

438. Shibata in view of Park, in my opinion, renders what this claim requires obvious.

439. Again, Shibata explains that its memory device includes “memory strings” with “memory cells” arranged in “series in a first direction” along a “columnar portion[] CL.” Ex. 1005, [0048], [0055]. As discussed, these columnar

portions pass through all of Shibata's various layers, including its "**BSG**," the "**word lines**," and its "**insulating layers**." See above discussion of claim 5.

440. Shibata does not, however, appear to make specific reference to the presence of the "**dummy channel structure**" required by this claim.

441. A POSITA would have understood that Shibata would nonetheless obviously include what this claim requires. This is because Shibata discloses replacing the sacrificial gate layers after formation of the stack, which requires a support structure so the stack does not collapse when the sacrificial gate layers are etched out between the dielectric layers. See Ex. 1005, [0103]-[0105], [0113].

442. Park provides an example of how a POSITA would have understood Shibata's memory to be structured. In particular, according to Park, a 3D NAND memory device can include multiple "dummy string[s] DS" with "a dummy channel" "DCH[.]" Ex. 1004, 4:55-65; see also *id.*, 5:30-32. These dummy strings and their associated channels have "similar" "structure" to the cell channels and thus also pass through the various memory layers. *Id.*, 11:19-21; Fig. 27 (depicting multiple dummy channel structures DCH). A POSITA would have recognized that employing the same structure for the dummy and memory strings would be beneficial in that it allows the structures to be formed at the same time following the same process steps. Further, according to Park, the "dummy channel structures ... may be provided to secure stability of the memory device" during manufacturing

when sacrificial layers are removed. *Id.*, 5:41-45. As noted above, Shibata also employs—and removes—sacrificial layers during manufacture of its memory. Ex. 1005, [0103]-[0105], [0113]. Because of this, a POSITA would have understood Shibata’s memory would obviously include the same dummy columns as referenced in Park. In particular, there would be dummy channel structure that—like the channels associated with Shibata’s other memory strings—pass through Shibata’s various dielectric and electrode layers and into the substrate.

443. Moreover, dummy columns were routinely used as support structures in the prior art. *See, e.g., id.*; Ex. 1023, 5:64-6:2 (explaining that “dummy” structures in a memory “mimic a physical property of another structure” and are present for purposes of performing “load carrying” functions). This would have further confirmed to a POSITA that Shibata would have obviously included the claimed ***“dummy channel structures.”***

7. Claim 7

444. Claim 7 depends on claim 5 and further requires:

[7] “a plurality of memory cell sub-blocks, each of the memory cell sub-blocks including a plurality of respective channel structures that are connected to a same sub-BSG and to a same sub-TSG, each of the memory cell sub-blocks being operated individually.”

445. Shibata, in my opinion, teaches what this claim requires.

446. According to Shibata, each “block” of its memory can be further divided into multiple separate “string units” such “SU0, SU1, and SU2.” Ex. 1005, [0079].

447. And each “string unit includes multiple memory strings MS” with associated “multiple columnar portions CL[.]” Ex. 1005, [0079].

448. Further, as explained in connection with claim 1, Shibata and Park teach a memory that divides its select gates with “separation portions” to allow the string units to be “controlled electrically independently.” Ex. 1005, [0083], [0129], [0167]. [0227], [0270]; *see also supra* discussion of limitation [1.E].

449. In my opinion, Shibata’s string units correspond to the claimed ***“memory cell sub-blocks.”***

450. Each string unit includes ***“a plurality of respective channel structures”*** (structures CL) that are ***“connected to a same sub-BSG”*** (portion of the bottom select gate) and ***“to a same sub-TSG”*** (portion of the upper select gate) such that they can be ***“operated individually.”***

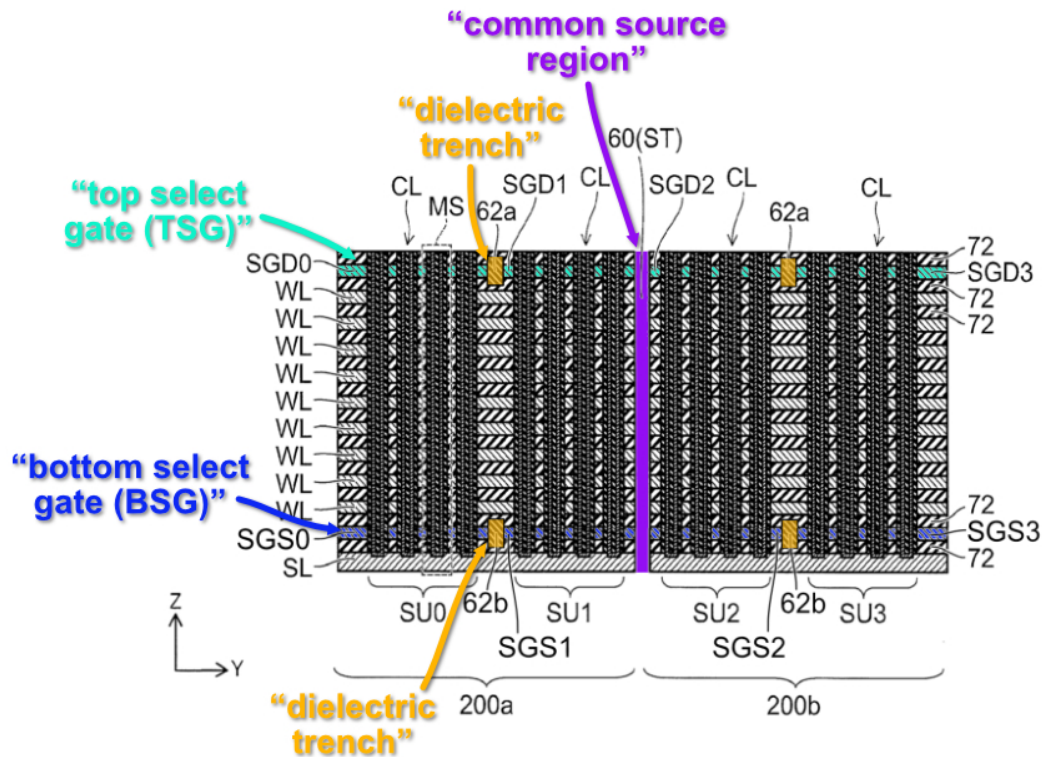
8. Claim 8

451. Claim 8 depends on claim 5 and further requires that:

[8] “the one or more first dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate.”

452. Shibata in view of Park, in my opinion, renders what this claim requires obvious.

453. More particularly, Shibata’s “*second dielectric trenches*” (separation portions 62a, annotated orange) are “*alternatively disposed in the width direction*” (the Y-axis direction) with the “*common source regions*” (interconnect portion LI within separation portion 60, annotated purple). Again, as explained, a POSITA would have considered it obvious that the “*first*” and “*second*” dielectric trenches that would be present when Park’s teachings are applied to Shibata would be aligned with each other. Thus, the “*first dielectric trenches*” also would have been obviously “*alternatively disposed*” with the “*common source regions*” in the same manner as the “*second dielectric trenches*[.]” This is shown in the below annotated version of the same demonstrative I discussed above—created by applying Park’s teachings to Figure 16 of Shibata—in connection with limitation [1.E]:



9. Claim 9

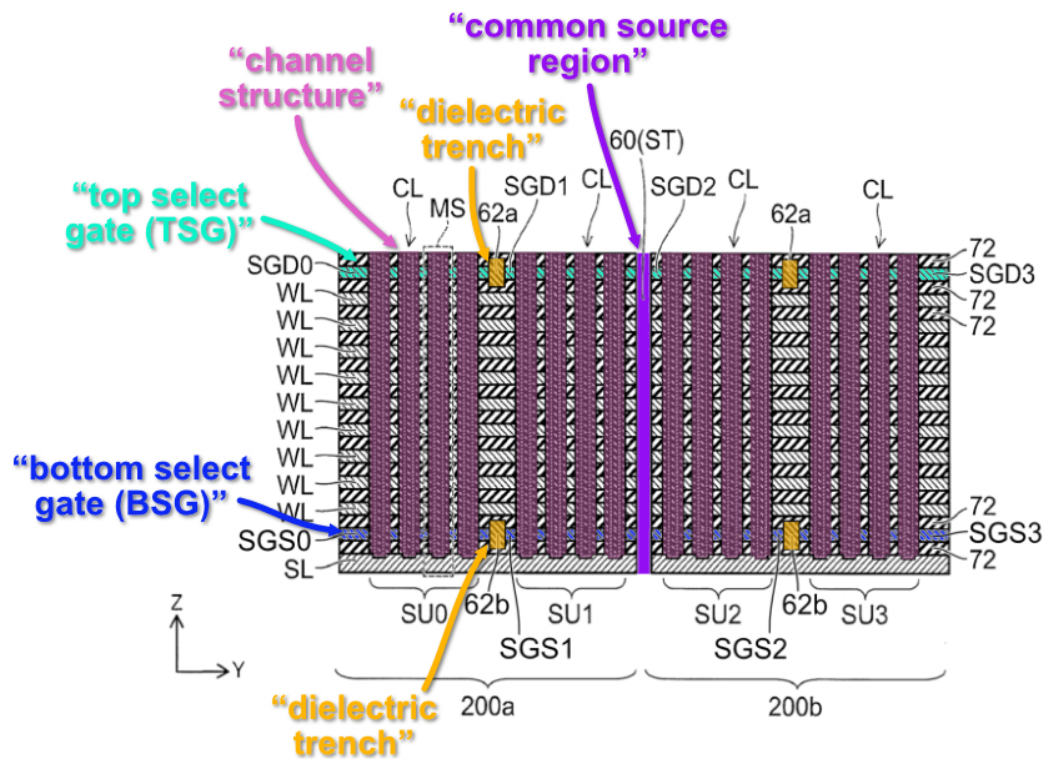
454. Claim 9 depends on claim 5 and further requires that:

[9] “the one or more second dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate so that a plurality of channel structures are disposed therebetween.”

455. Shibata, in my opinion, teaches what this claim requires.

456. As explained in connection with claim 8 and shown in the below demonstrative applying Park’s lower trenches to Shibata, Shibata’s “*dielectric trenches*” (the separation portions, annotated orange) are “*alternatively disposed in the width direction*” with the “*common source regions*” (interconnect portion LI within separation portion 60, annotated purple). (See *supra* discussion of claim 8).

457. Further, as also shown in the demonstrative below, each of Shibata’s string units SU0-SU3 includes multiple “*channel structures*” (structure CL, annotated pink) located between the “*dielectric trenches*” and “*common source regions*”:



10. Claim 10

458. Claim 10 depends on claim 1 and further requires:

[10] “one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.”

459. Shibata in view of Park, in my opinion, renders what this claim requires obvious.

460. According to Shibata, “a dummy word line may be provided between the drain-side select gate and the word lines and/or between the source side select gate and the word lines.” Ex. 1005, [0457].

461. The ’623 patent explains that “bottom dummy word lines” are the same as “dummy BSGs.” Ex. 1001, 6:44-48.

462. Given this, Shibata includes the claimed “**one or more dummy BSGs**” that are “**formed between the plurality of word lines and the BSG**”: it includes a “dummy word line” between its lower, source-side select gate layer and word lines.

463. A POSITA also would have considered it obvious that, when Park’s teachings are applied to Shibata, Shibata’s lower “**dielectric trench**” (the separation portions 62b) would “**separate**” not only its “**BSG**” (the lower select gate layer), but also its “**dummy BSG**” (the dummy line adjacent to the select gate layer).

464. While Shibata explains that its word lines are “provided commonly” across the string units (Ex. 1005, [0165]), it divides the select gates on a string unit basis (*see id.*, [0083], [0129], [0167]. [0227], [0270].)

465. Shibata places its dummies adjacent to and associates them with its select lines. Ex. 1005, [0457].

466. Given this, a POSITA would have understood that they would be—or at the very least obviously could be—structured and divided in the same way as the select lines themselves.

467. Next, Shibata teaches a range of different separation portion structures. For instance, “separation portion 62a” in Figure 16 passes through a single gate layer. *See* Ex. 1005, Fig. 16. Figure 3 employs two separation portions 62a and 62b separating adjacent conductive layers. *See id.*, Fig. 3. And another “separation portion 60” in Figure 3 is structured such that it passes through all of the conductive layers. *See id.*

468. I have also identified other references similarly discussing various known separation options in Section IX.B.10.

469. A POSITA would have considered use of all these known design alternatives when implementing Shibata.

470. In view of these various known options, a POSITA would have considered it highly obvious that both Shibata’s bottom select gate layer and the adjacent dummy layer would be divided by the same dielectric trench.

11. Claim 11

471. Claim 11 depends on claim 2 and further requires:

[11] “one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs, and spaced apart from the plurality of the word lines and the TSG by the plurality of insulating layers.”

472. Shibata, in my opinion, renders what this claim requires obvious.

473. As explained above when discussing claim 10, Shibata teaches that its memory device can include “dummy ... line[s]” “between the drain-side select gate the word lines.” Ex1005, [0457].

474. These dummy lines, in my opinion, are the claimed ***“dummy TSGs.”***

475. Moreover, a POSITA would have considered it obvious for Shibata’s ***“second dielectric trenches”*** to pass through not only its ***“TSG”*** (the upper for drain-side select gate) but also its ***“dummy TSGs”*** (the dummy lines) for the same reasons explained in connection with claim 10.

476. Additionally, Shibata also forms its “dielectric trenches” by etching through already applied layers. Ex. 1005, [0106].

477. As I explain above, POSITA would have recognized that one of the functions of the dummy layers would have been to provide a buffer ensuring that—while the trench enters some of the dummy layers—it does not reach the word lines.

See supra Section IX.B.11.

E. Secondary Considerations of Non-Obviousness

478. Based on my review of the '623 patent's prosecution history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims.

479. I am not separately aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like. Instead, as discussed above, it is my opinion that the subject matter embraced by the '623 patent's claims was known in and obvious over the prior art. Moreover, it is also my opinion the teachings of the prior art would have been expected to successfully function as or be usable with working 3D NAND memory devices.

Petition for *Inter Partes* Review of U.S. Patent No. 10,950,623
Declaration of Dr. Jack C. Lee

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: April 11, 2024

Location: Austin TX

Signature: 
DR. JACK C. LEE