

Docket No. 534753US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Yali SONG, et al.

SERIAL NO: New Application

ART UNIT:

FILING DATE: Herewith

EXAMINER:

FOR: NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME

FEE TRANSMITTAL

- ☐ No additional fee is required
- ☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- ☐ Track 1 Prioritized Examination

The Fee has been calculated as shown below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	14 - 20 =	0	x \$100 =	\$0.00
INDEPENDENT CLAIMS	1 - 3 =	0	x \$480 =	\$0.00
UTILITY APPLICATION SIZE FEE	54* - 100 = (* 72 x .75)	0 (each addtl. 50 sheets over 100)	x \$420 =	\$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ \$860 =	\$0.00
☐ LATE FILING OF DECLARATION			+ \$160 =	\$0.00
☐ NON-ELECTRONIC FILING FEE			+ \$400 =	\$0.00
☒ FILING FEE (\$320.00)	☒ SEARCH FEE (\$700.00)	☒ EXAMINATION FEE (\$800.00)	BASIC FEES	\$1,820.00
TOTAL OF ABOVE CALCULATIONS				\$1,820.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				\$0.00
☐ FILING FEE REDUCED IF E-FILED – SMALL ENTITY			+ \$-80 =	\$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ \$140 =	\$0.00
TOTAL				\$1,820.00

- ☐ Please charge Deposit Account No. **15-0030** in the amount of **\$0.00**
- ☒ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **\$1,820.00**.
- ☒ The Director is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**, with the **EXCEPTION** of deficiencies in fees for multiple dependent claims in new applications.

Submitted by: /Johnny Ma/
Johnny Ma
Registration No. 59,976

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 02/12)

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		
First Named Inventor/Applicant Name:		Yali SONG		
Filer:		Philippe Jean-Claude Signore/Nozomi Berger		
Attorney Docket Number:		534753US		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1820

Electronic Acknowledgement Receipt	
EFS ID:	41703213
Application Number:	17154054
International Application Number:	
Confirmation Number:	6569
Title of Invention:	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME
First Named Inventor/Applicant Name:	Yali SONG
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Nozomi Berger
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	534753US
Receipt Date:	21-JAN-2021
Filing Date:	
Time Stamp:	11:39:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1820
RAM confirmation Number	E20211KB39492699
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	534753US-ADS.pdf	1256137	no	9
			eb06cf501cec7b329edb1345683f86961a71c6d9		
Warnings:					
Information:					
2		534753US-NewApp.pdf	10174709	yes	81
			63f6df176b2d10d5aced3d0e813def11e35084bb		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Information Disclosure Statement (IDS) Form (SB08)		80	81	
	Transmittal Letter		79	79	
	Power of Attorney		77	78	
	Oath or Declaration filed		74	76	
	Drawings-only black and white line drawings		54	73	
	Specification		2	53	
	Transmittal of New Application		1	1	
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	35173	no	2
			1632723026beec2957d2b5d0308e5528ec732ce9		
Warnings:					
Information:					
Total Files Size (in bytes):			11466019		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	534753US
		Application Number	
Title of Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1		Remove	
Legal Name			
Prefix	Given Name	Middle Name	Family Name
	Yali		SONG
Residence Information (Select One) US Residency • Non US Residency Active US Military Service			
City	Wuhan, Hubei	Country of Residence ⁱ	CN
Mailing Address of Inventor:			
Address 1	No. 88 Weilai 3rd Road		
Address 2	East Lake High-tech Development Zone		
City	Wuhan, Hubei	State/Province	
Postal Code		Country ⁱ	CN
Inventor 2		Remove	
Legal Name			
Prefix	Given Name	Middle Name	Family Name
	Li Hong		XIAO
Residence Information (Select One) US Residency • Non US Residency Active US Military Service			
City	Wuhan, Hubei	Country of Residence ⁱ	CN
Mailing Address of Inventor:			
Address 1	No. 88 Weilai 3rd Road		
Address 2	East Lake High-tech Development Zone		
City	Wuhan, Hubei	State/Province	
Postal Code		Country ⁱ	CN
Inventor 3		Remove	
Legal Name			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	534753US
		Application Number	
Title of Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ming		WANG	
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service				
City	Wuhan, Hubei		Country of Residence ⁱ	CN
Mailing Address of Inventor:				
Address 1		No. 88 Weilai 3rd Road		
Address 2		East Lake High-tech Development Zone		
City	Wuhan, Hubei	State/Province		
Postal Code		Country ⁱ	CN	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	22850		
Email Address	oblonpat@oblon.com	Add Email	Remove Email

Application Information:

Title of the Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		
Attorney Docket Number	534753US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	20	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	534753US
		Application Number	
Title of Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		

Publication Information:
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	22850		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16/365725	2019-03-27
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/365725	Continuation of	PCT/CN2018/119908	2018-12-07
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	534753US
		Application Number	
Title of Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ^j	Filing Date (YYYY-MM-DD)	Access Code ^k (if applicable)	Remove

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	534753US
		Application Number	
Title of Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	534753US
		Application Number	
Title of Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Applicant	1	Remove		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.				
Clear				
Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor		
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest			
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:				
Name of the Deceased or Legally Incapacitated Inventor:				
If the Applicant is an Organization check here. ☒				
Organization Name	Yangtze Memory Technologies Co., Ltd.			
Mailing Address Information For Applicant:				
Address 1	No. 88 Weilai 3rd Road			
Address 2	East Lake High-Tech Development Zone			
City	Wuhan, Hubei	State/Province		
Country	CN	Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Applicant Data may be generated within this form by selecting the Add button.				
Add				

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	534753US
		Application Number	
Title of Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		

Assignee	1		
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.			
Remove			
If the Assignee or Non-Applicant Assignee is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1	No. 88 Weilai 3rd Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	State/Province	
Country ⁱ	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add			

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, all joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of all joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Johnny Ma/		Date (YYYY-MM-DD)	2021-01-21	
First Name	Johnny	Last Name	Ma	Registration Number	59,976
Additional Signature may be generated within this form by selecting the Add button. Add					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	534753US
		Application Number	
Title of Invention	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 534753US		SERIAL NO. New Application	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE Herewith		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2010/0320528 A1	12-23-2010	JEONG, J. et al.			
	AB	2018/0337195 A1	11/22/2018	JAYANTI, S., et al.			
	AC	10,134,747 B2	11/20/2018	LEE, N.J.			
	AD	10,141,372 B2	11-27-2018	PARK, J. et al. (corresponds to US 2019/0081105 A1)			
	AE	2016/0233270 A1	08-11-2016	TAKAKI, S. et al.			
	AF						
	AG						
	AH						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AI	103226973 A	07-31-2013	China		X	
	AJ	103680611 A	03-26-2014	China		X	
	AK	103680618 A	03-26-2014	China		X	
	AL	201834218 A	09/16/2018	Taiwan (with English abstract)		X	
	AM	201842601 A	12/01/2018	Taiwan (with English abstract)		X	
	AN	201834217 A	09/16/2018	Taiwan (with English abstract)		X	
	AO	108831886 A	11/16/2018	China (with English abstract)		X	
	AP	108933139 A	12/04/2018	China (with English abstract)		X	
	AQ	108933141 A	12/04/2018	China (with English abstract)		X	
	AR	2018-163970 A	10/18/2018	Japan (with English abstract)		X	
	AS	101118907 A	02-06-2008	China		X	
	AT	101315936 A	12-03-2008	China		X	
	AU	106601751 A	04-26-2017	China		X	
	AV	108431961 A	08-21-2018	China (with English abstract)		X	
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Combined Chinese Office Action and Search Report issued on Jul. 17, 2019, in Patent Application No. 201880002892.5, citing documents AA and AI-AK therein, 7 pages (with English Translation of Category of Cited Documents)					
	AX	International Search Report and Written Opinion of the International Search Authority issued on Sep. 18, 2019, in PCT/CN2018/119908, citing documents AD-AE and AS-AU therein, 9 pages					
	AY	Combined Chinese Office Action and Search Report issued on October 10, 2020 in Patent Application No. 202010103862.2 (with English translation of Categories of Cited Documents), citing documents AV therein, 7 pages					
	AZ					☒ Additional References sheet(s) attached	
Examiner						Date considered	
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 534753US		SERIAL NO. New Application	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	US-20200335514-A1	10-2020	XU; Qiang			
	AB	US-20200227555-A1	07-2020	Sun; Jian Hua			
	AC	US-20200185411-A1	06-2020	Hemer; Scott Brad			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW						
	AX						
	AY						
	AZ					☐ Additional References sheet(s) attached	
Examiner					Date considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yali SONG, et al.

SERIAL NO: New Application

GAU:

FILED: Herewith

EXAMINER:

FOR: NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

Applicant(s) wish to disclose the following information.

REFERENCES

☒ The applicant(s) wish to make of record the reference(s) listed on the attached form PTO-1449. Copies of the listed reference(s) were made of record in parent application Serial No. 16/365,725, filed March 27, 2019, as were either statements of relevancy or any readily available partial or full English translations of pertinent portions of any non-English language reference(s).

☐ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

☒ Please charge any additional fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

/Johnny Ma/

Johnny Ma

Registration No. 59,976

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 02/12)

**TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE
REGISTERED PRACTITIONERS**

NOTE: This form is to be submitted with the Power of Attorney by Applicant form to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	New Application		
Patent Number			
Filing Date	Herewith		
Issue Date			
First Named Inventor	Yali SONG		
Title	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME		
Art Unit			
Examiner Name			
Attorney Docket Number	534753US		
SIGNATURE of Applicant or Patent Practitioner			
Signature	/Johnny Ma/	Date	2021-01-21
Name	Johnny Ma	Telephone	703-413-3000
Registration Number	59,976		
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.			
■ *Total of <u>1</u> forms are submitted.			

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

22850

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

SIMON SHE-NING YANG

Title

CEO

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.431, 1.432, and 1.433. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application or PCT international application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 22850** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Yali SONG Date: 2019.03.14

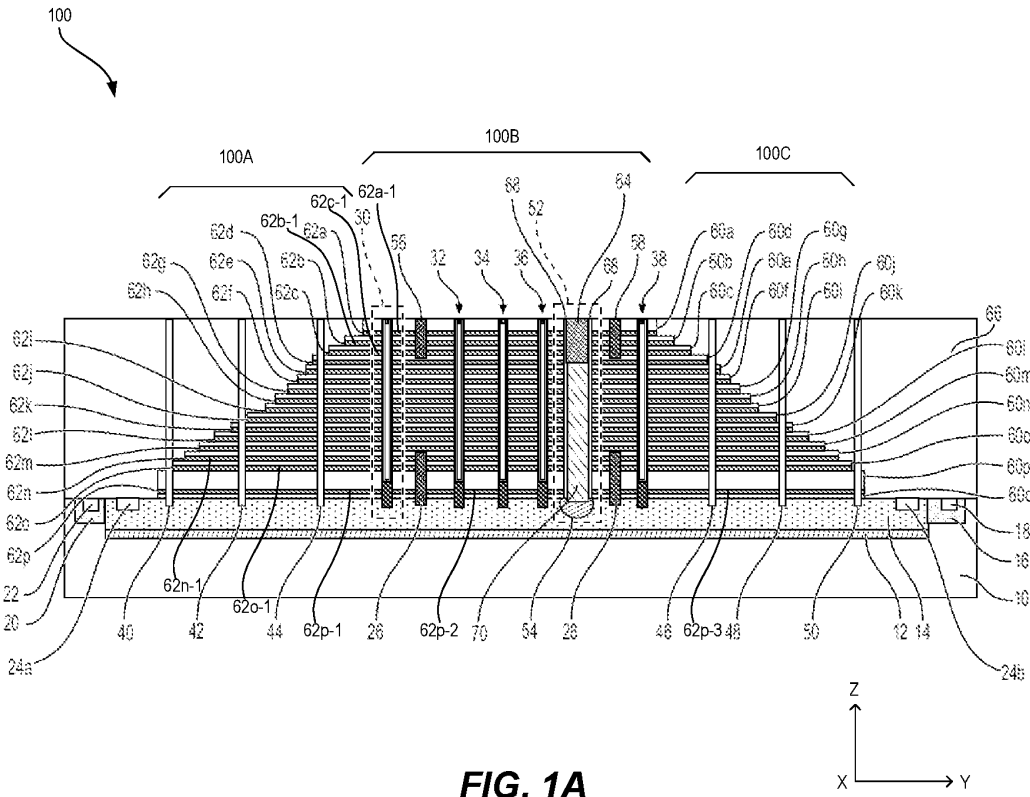
Signature of Inventor: Yali Song

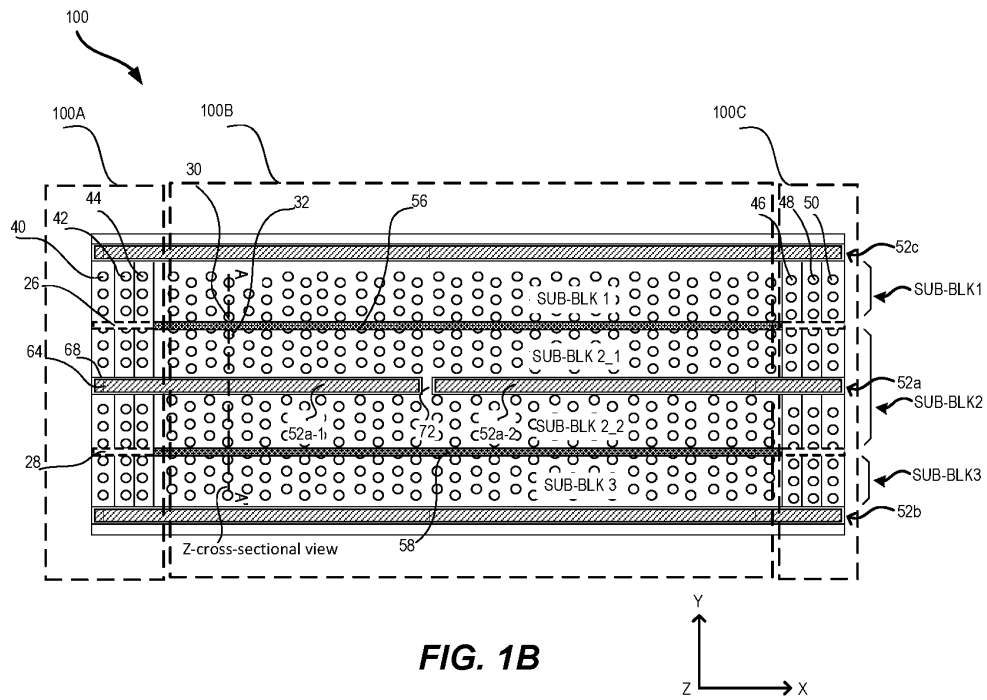
Inventor: Li Hong XIAO Date: 2019.03.14

Signature of Inventor: Sheng Xiao

Inventor: Ming WANG Date: 2019.03.14

Signature of Inventor: Ming Wang





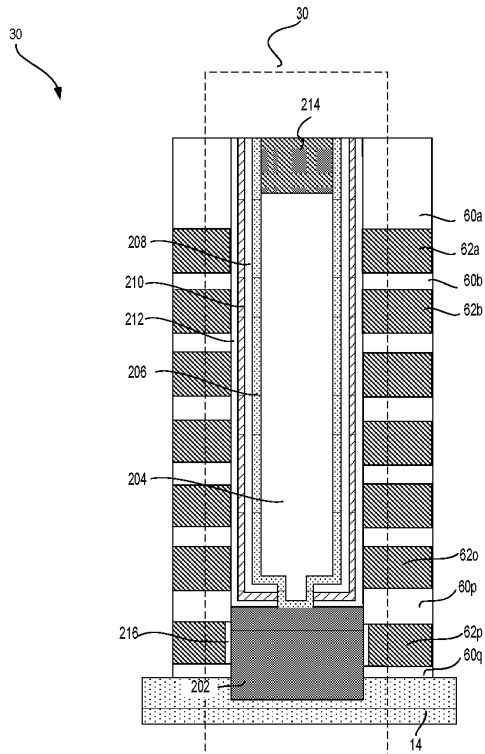


FIG. 1C-1

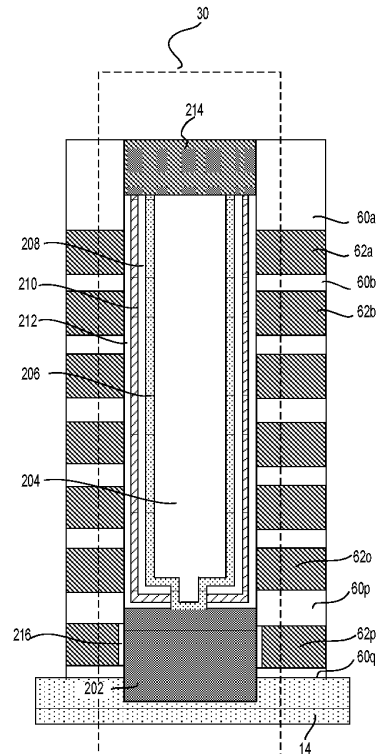


FIG. 1C-2

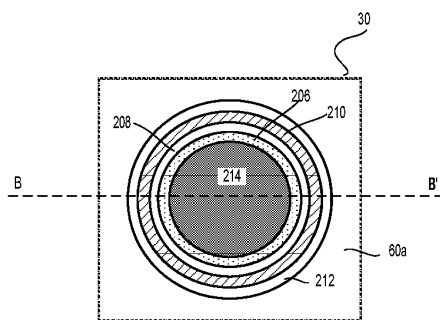


FIG. 1D-1

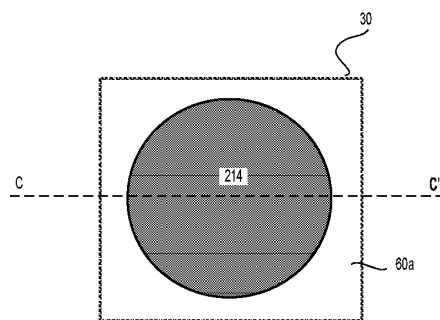


FIG. 1D-2

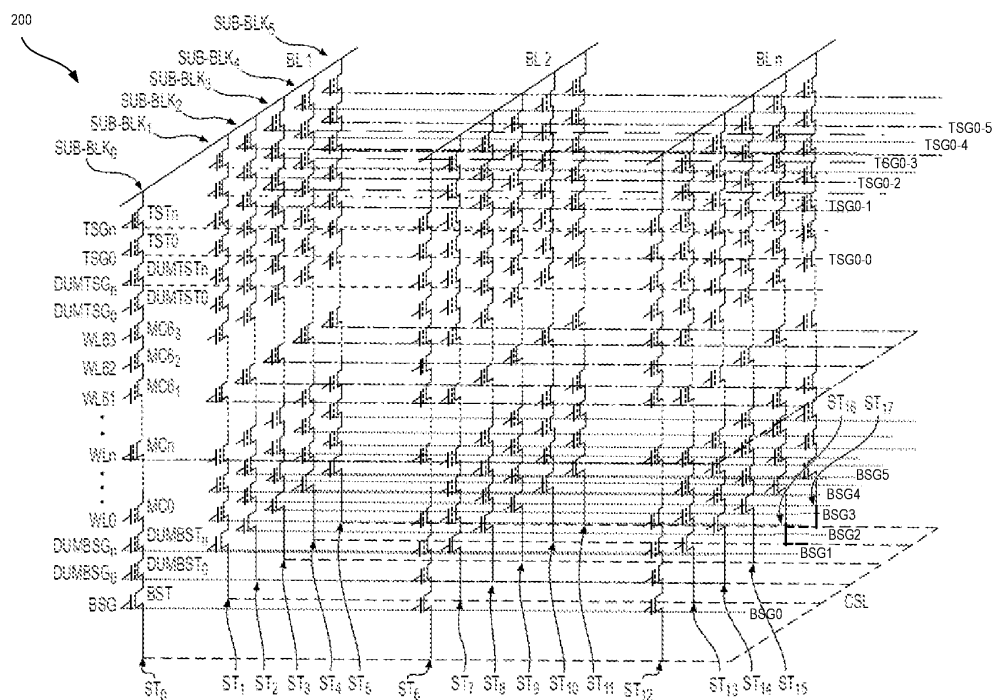


FIG. 1E

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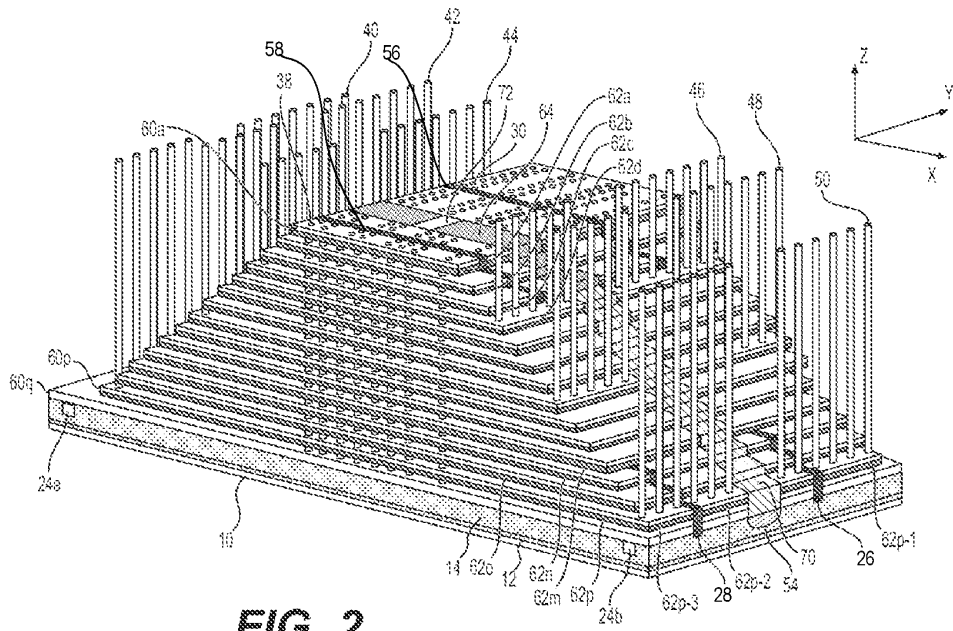
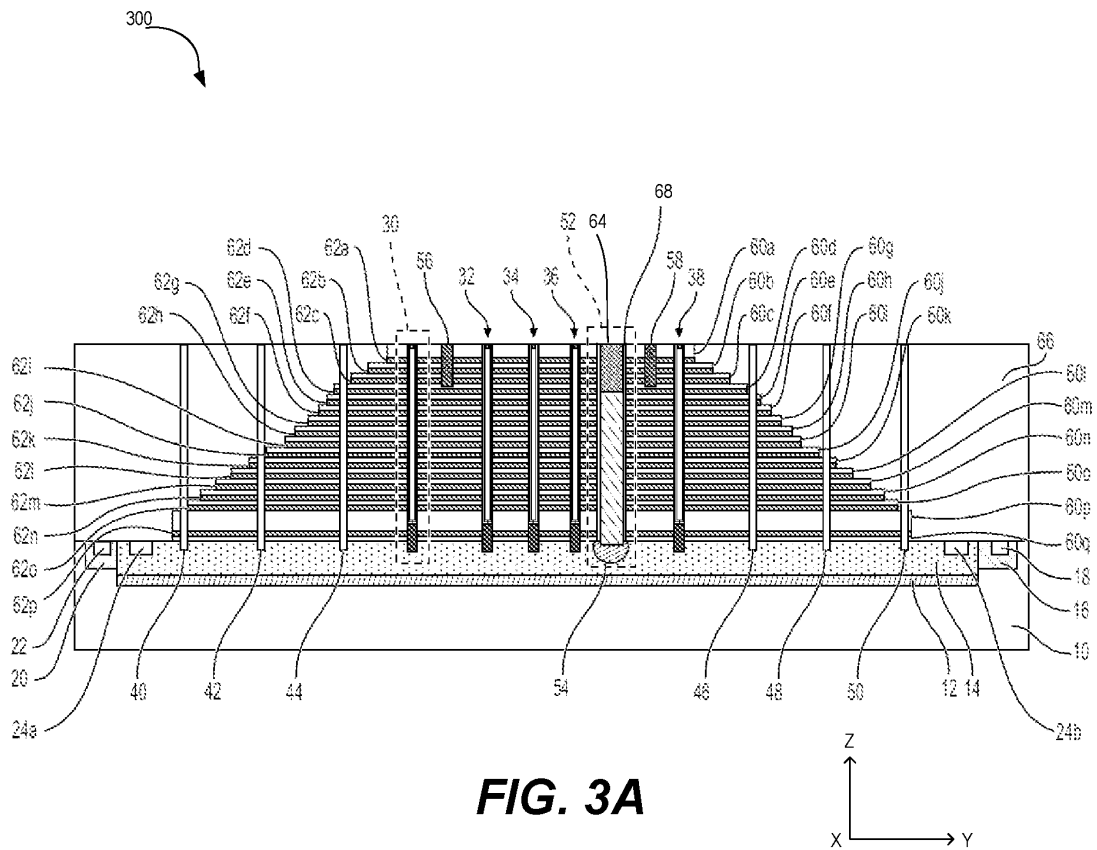


FIG. 2



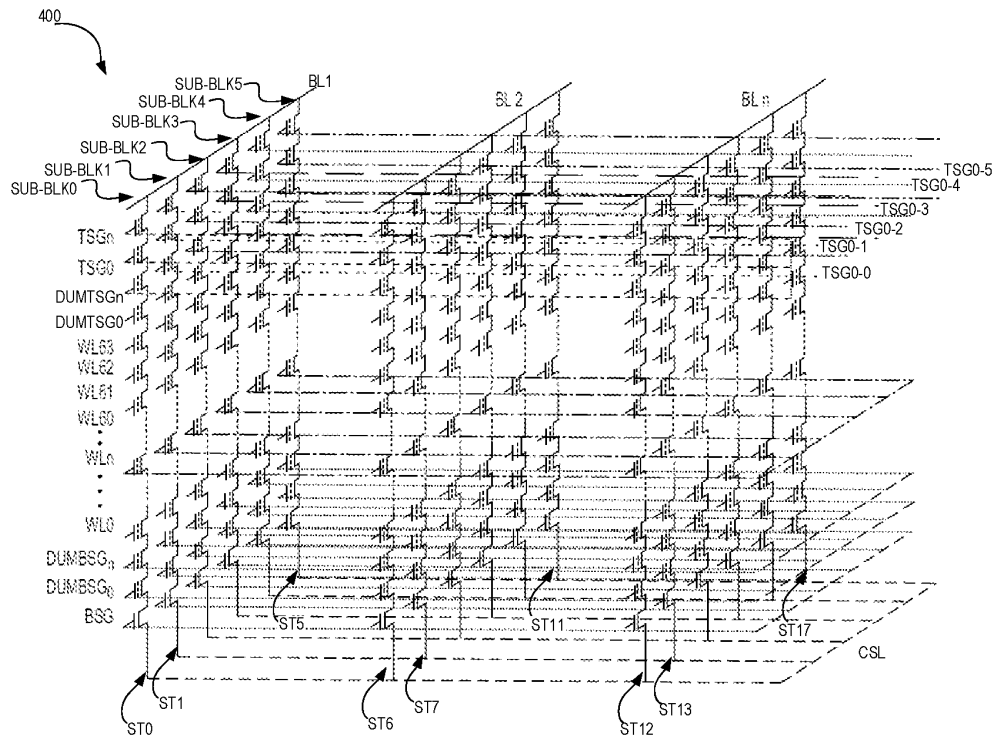


FIG. 3B

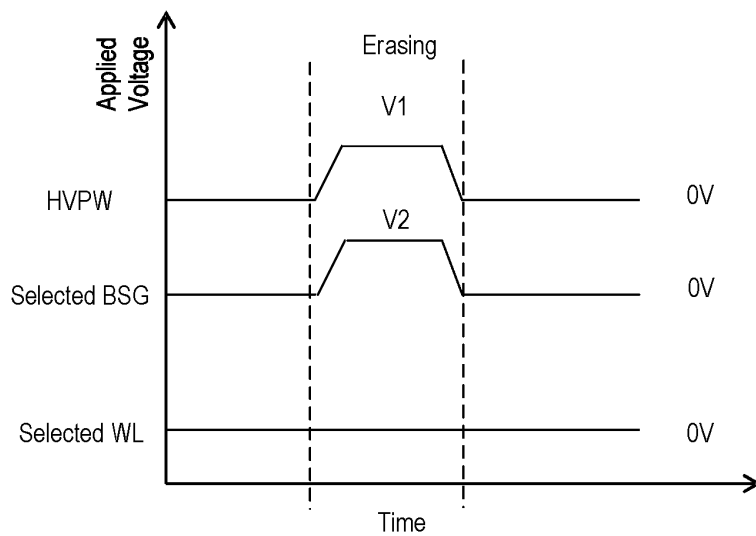


FIG. 4A

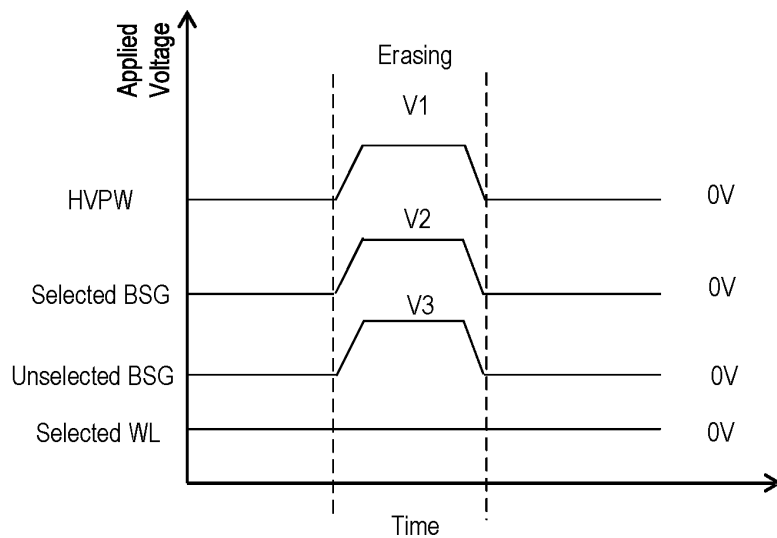


FIG. 4B

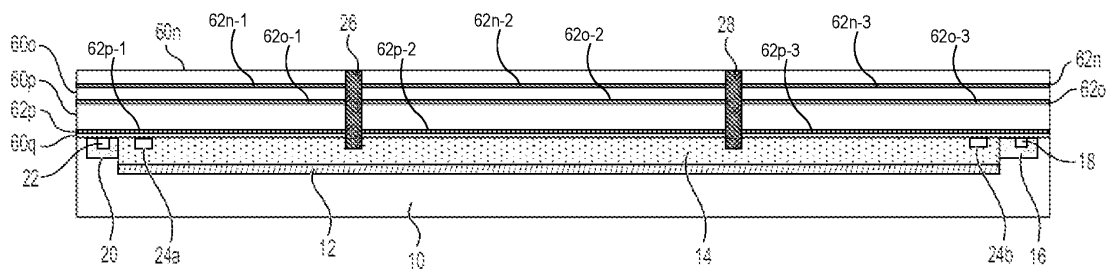


FIG. 5A

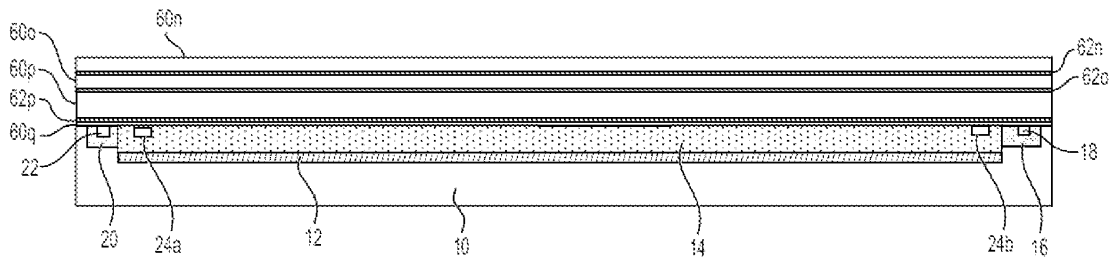
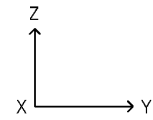
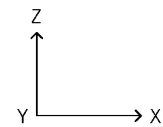


FIG. 5B



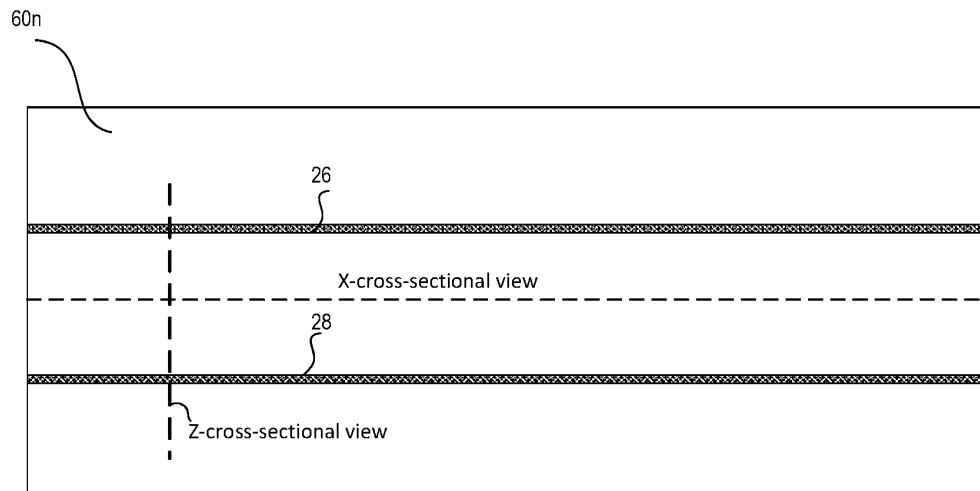


FIG. 5C

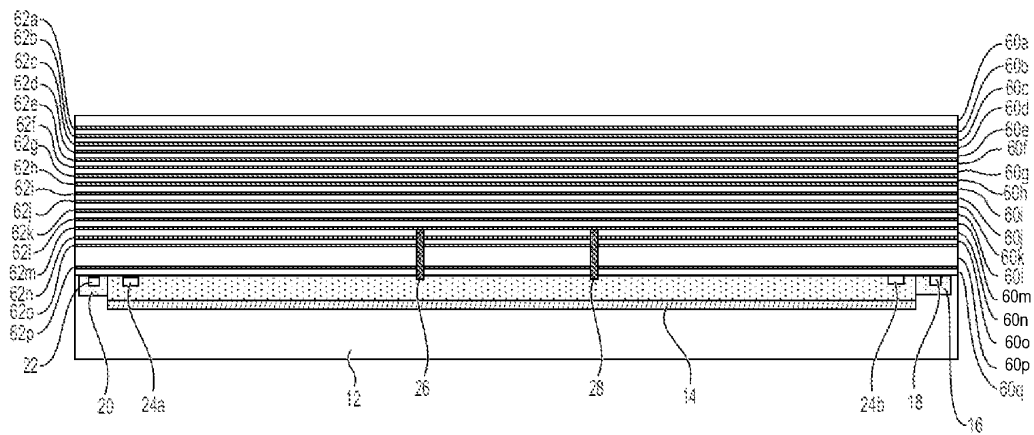
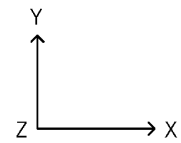
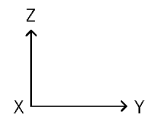


FIG. 6



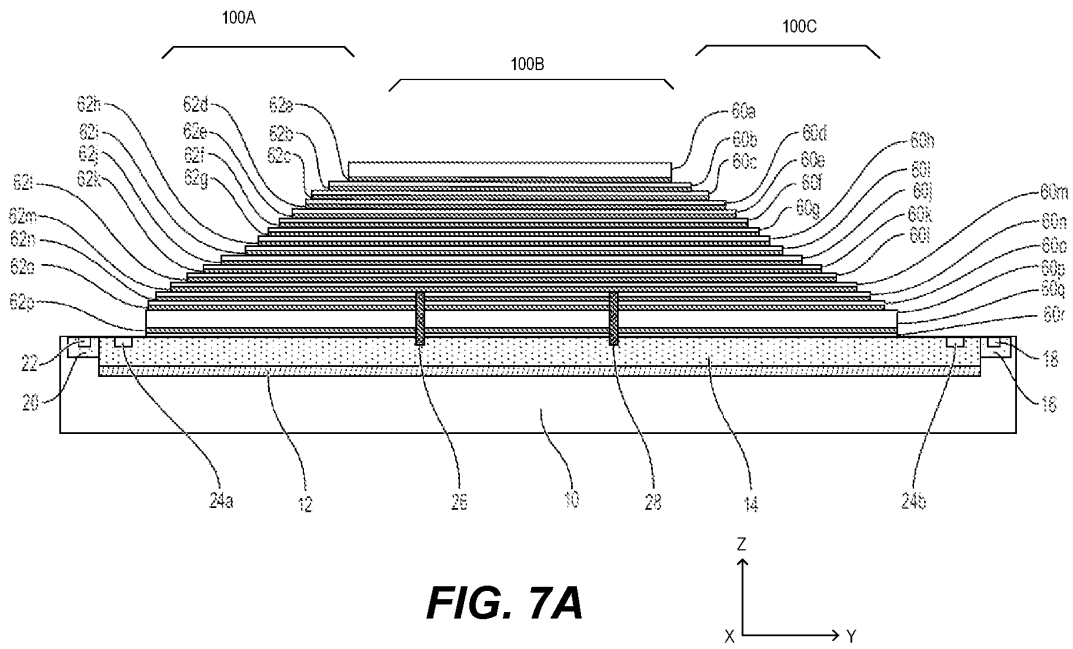


FIG. 7A

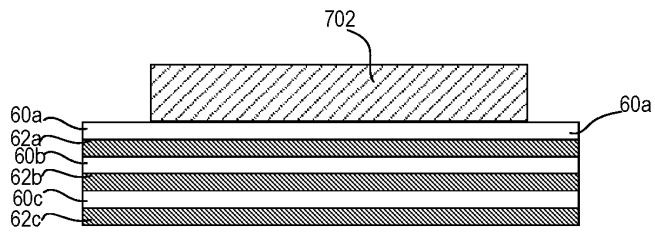


FIG. 7B

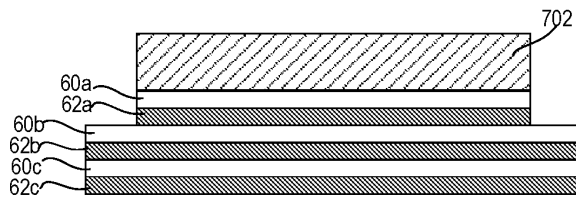


FIG. 7C

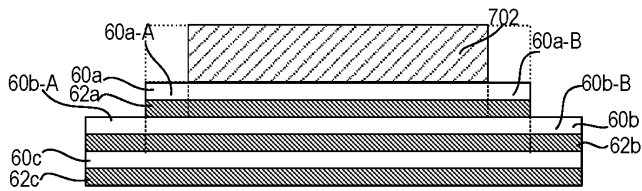


FIG. 7D

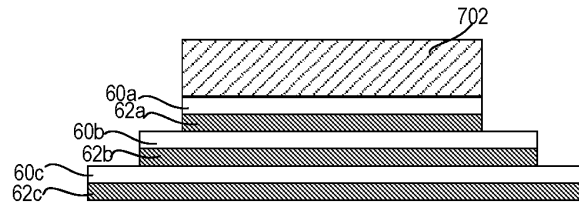


FIG. 7E

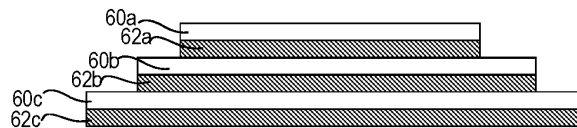


FIG. 7F

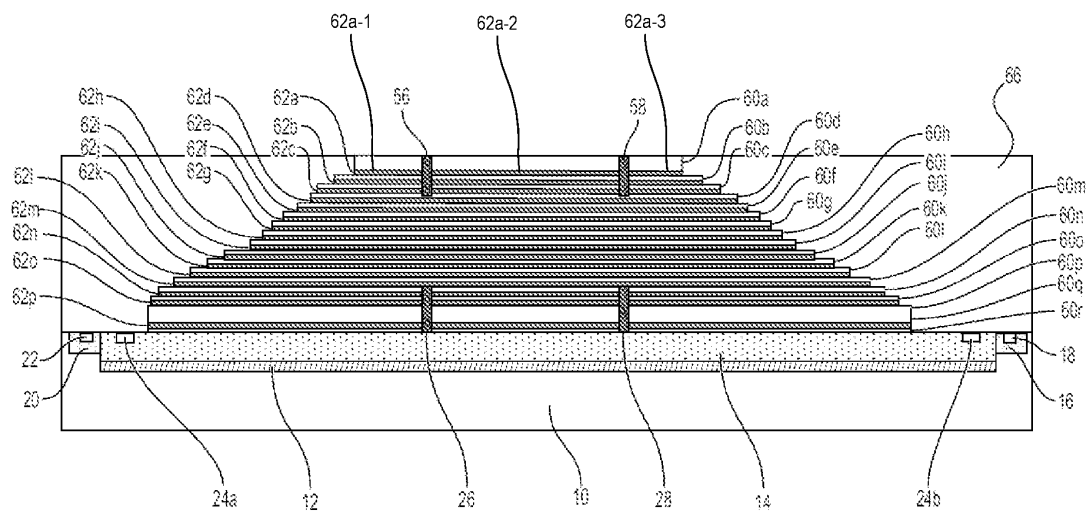


FIG. 8A

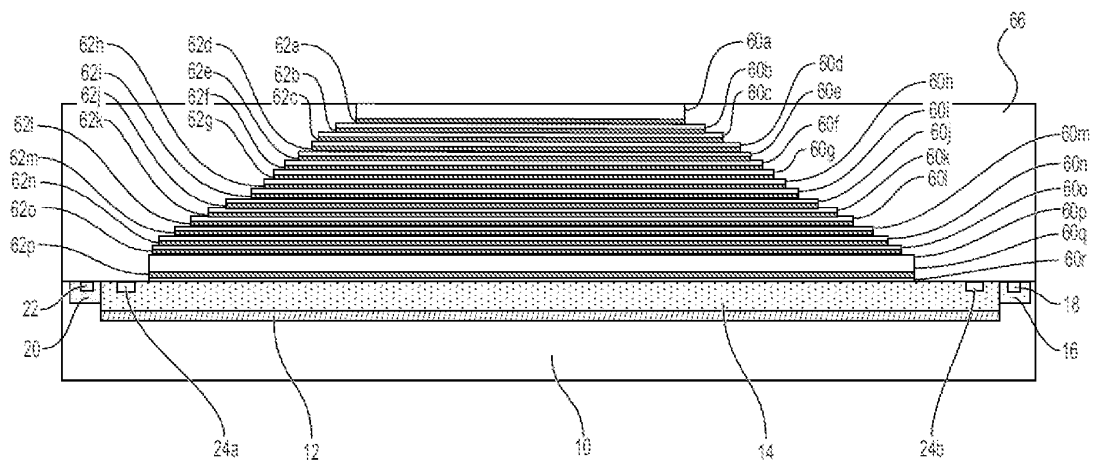
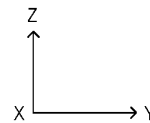
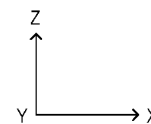


FIG. 8B



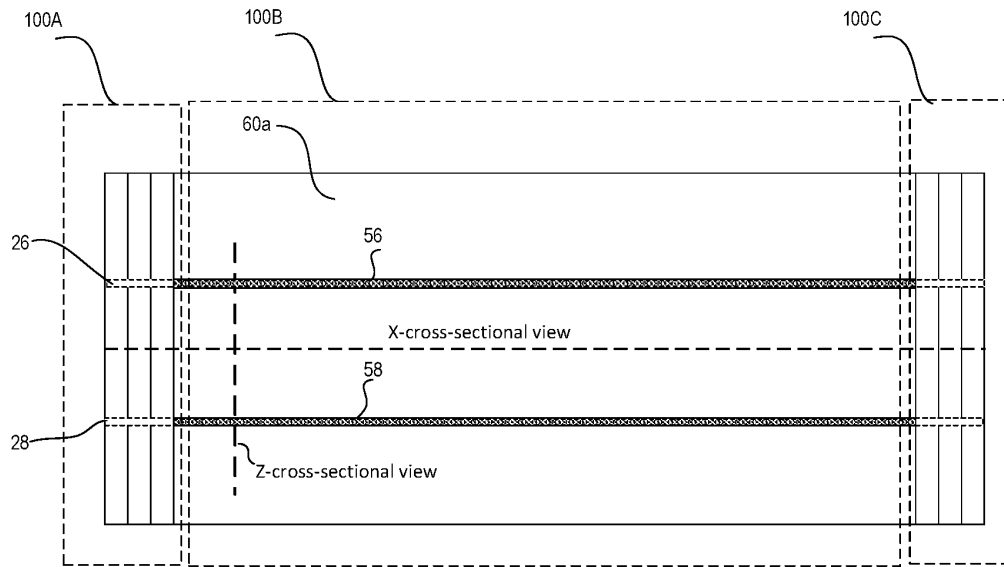


FIG. 8C

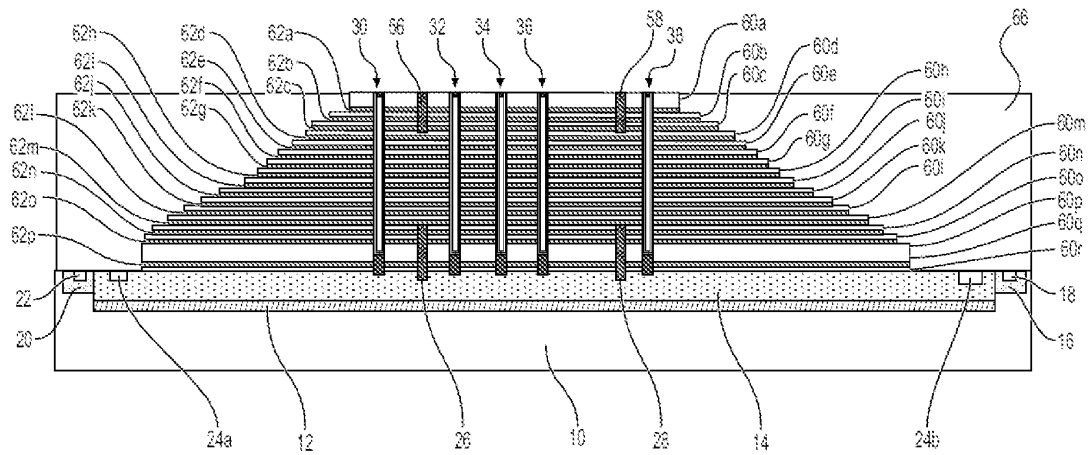
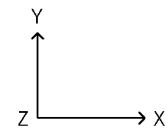
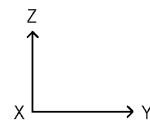


FIG. 9A



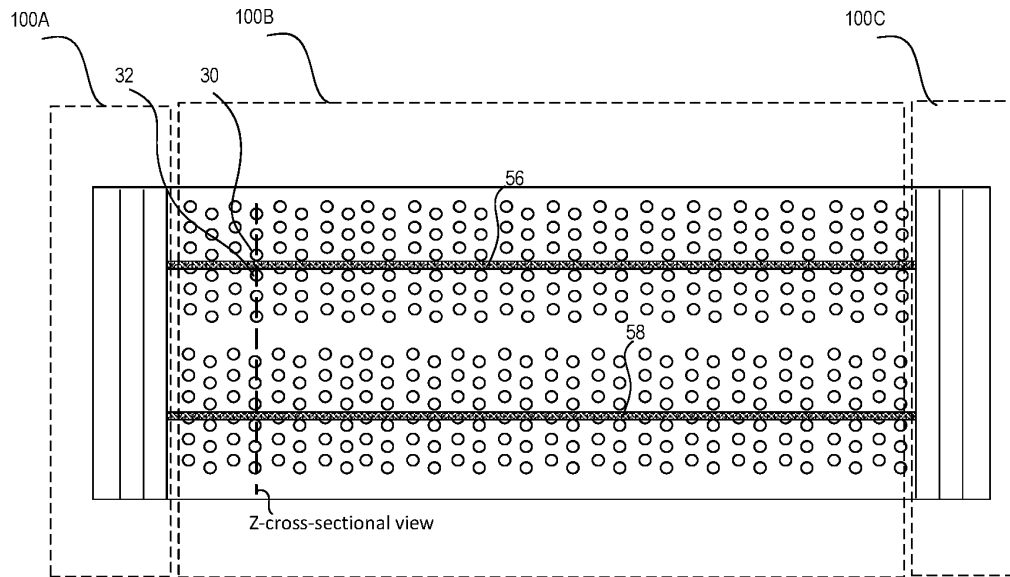


FIG. 9B

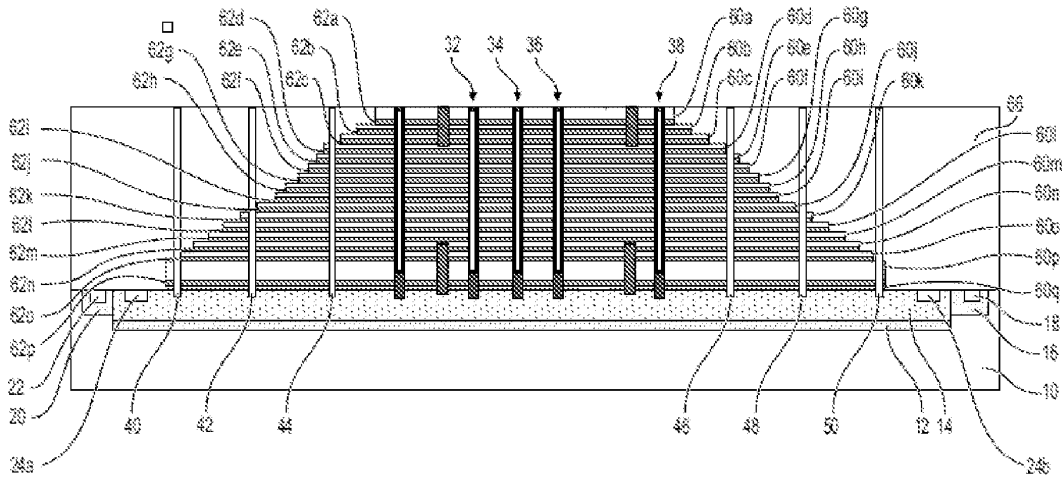
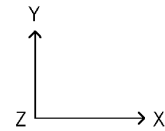
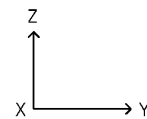


FIG. 10A



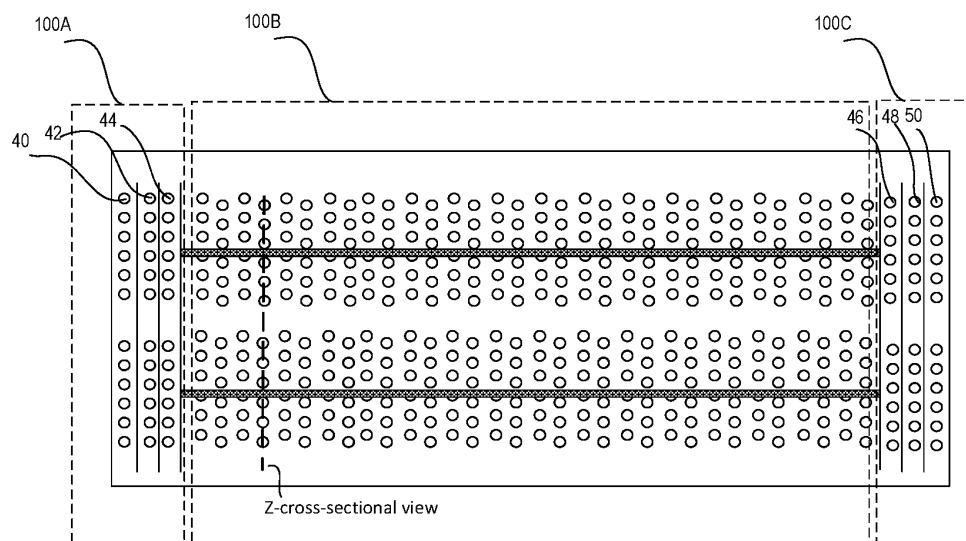
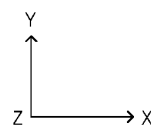


FIG. 10B



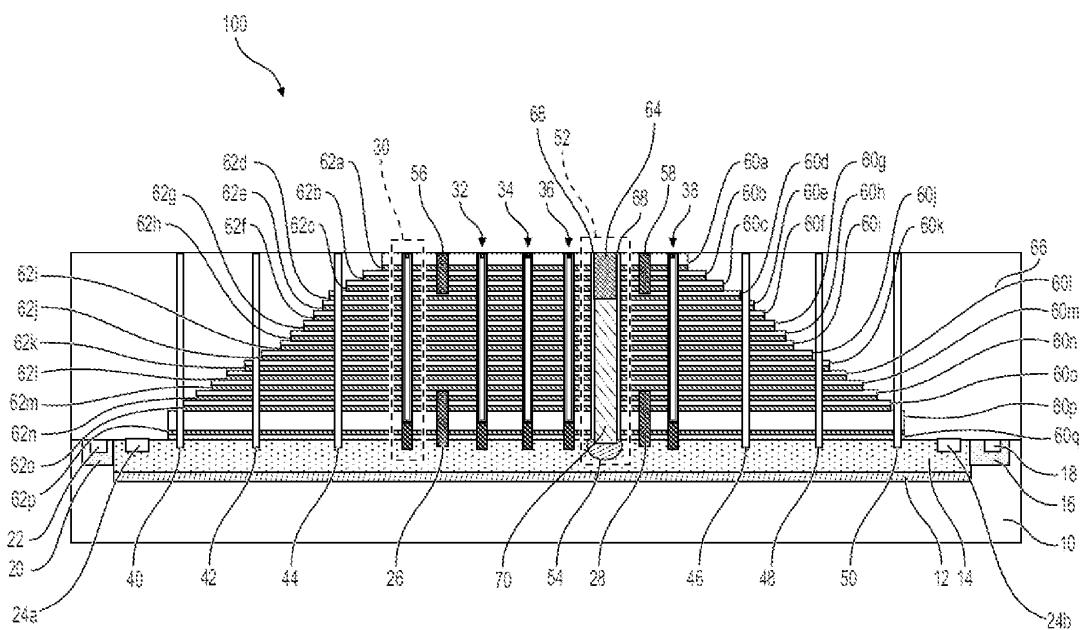
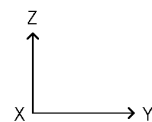
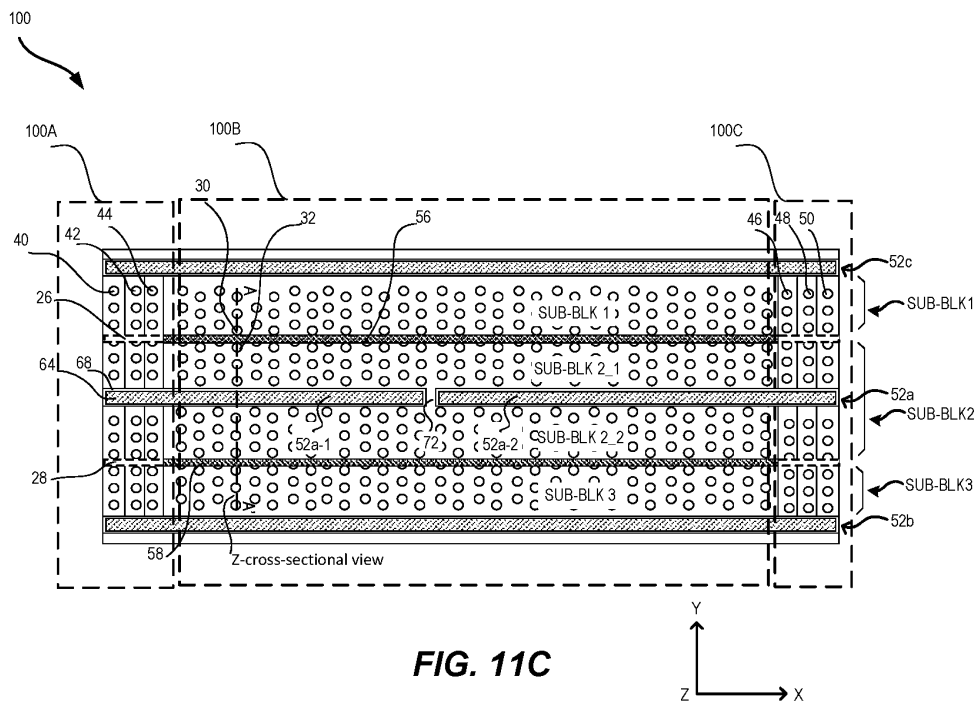
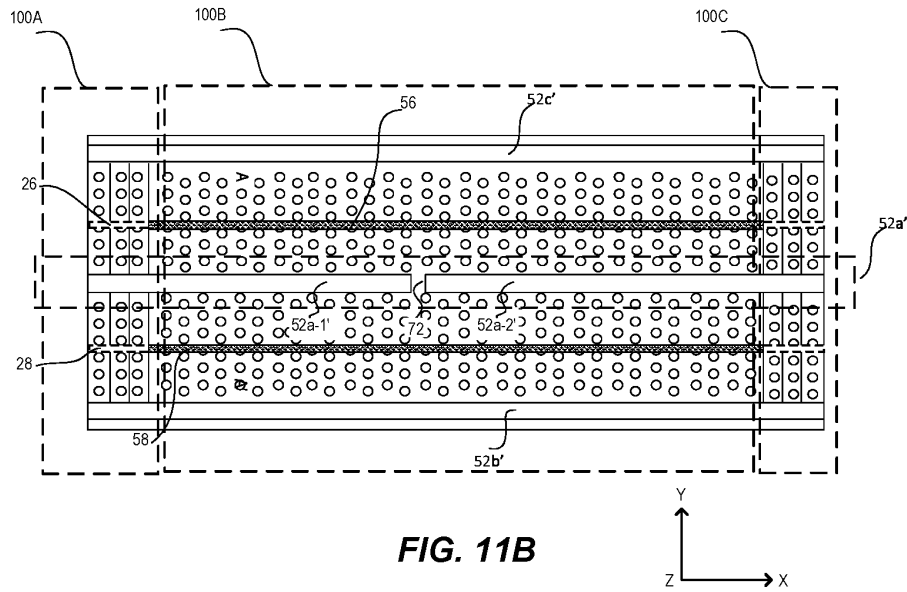


FIG. 11A





100

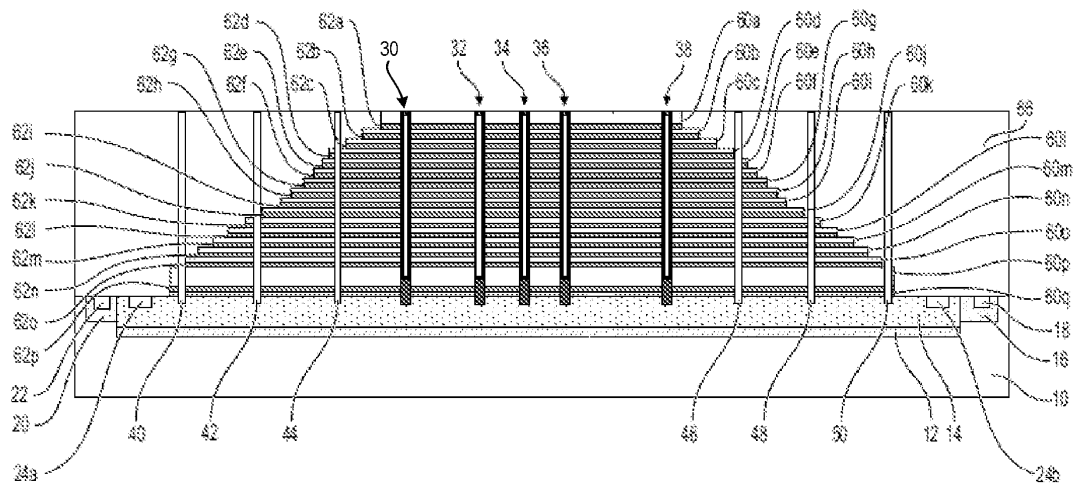
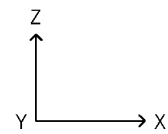


FIG. 11D



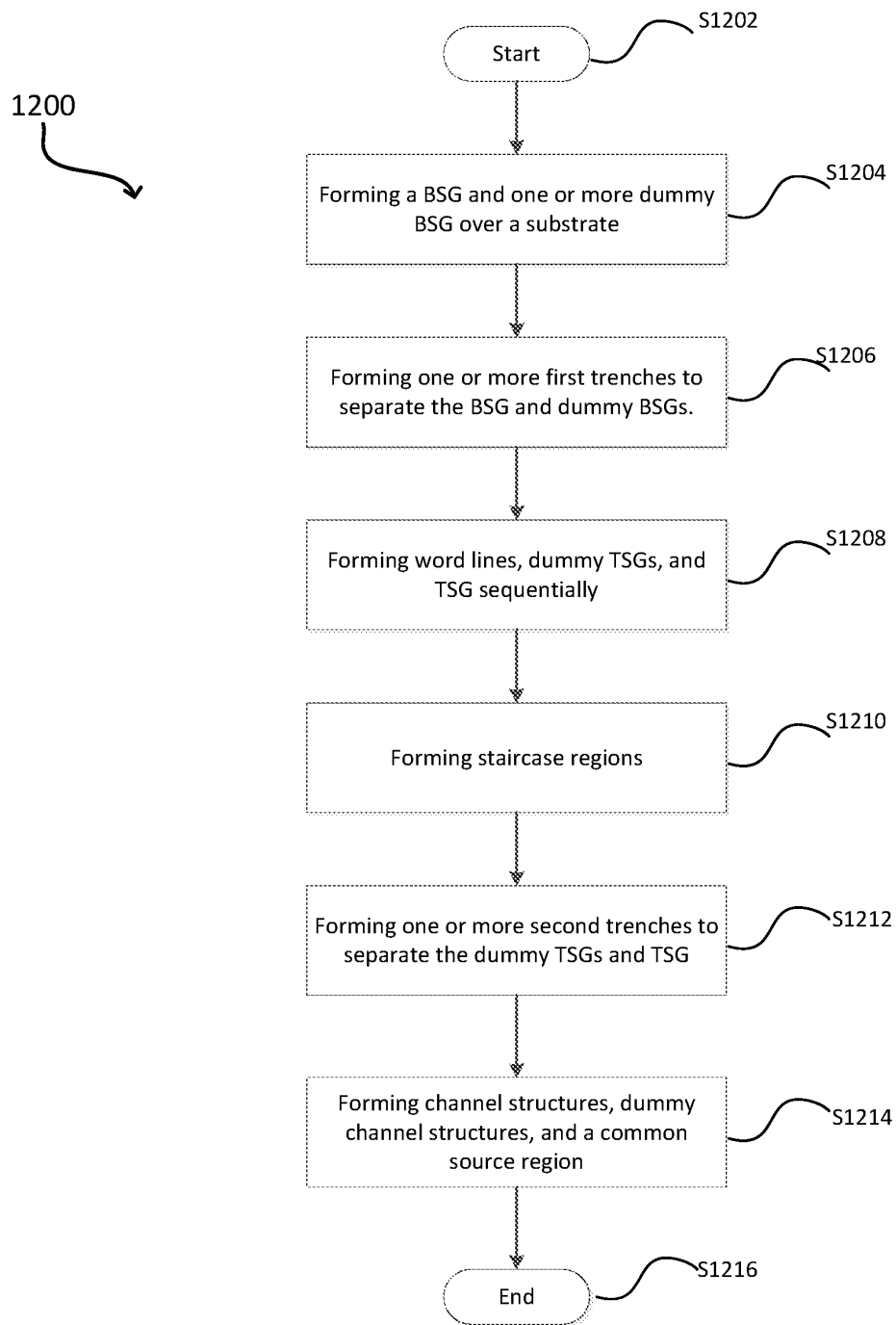


FIG. 12

NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME

RELATED APPLICATION

[0001] This application is a continuation of U.S. Patent Application Serial No. 16/365,725 filed on March 27, 2019, which is a continuation of International Application No. PCT/CN2018/119908, filed on December 7, 2018. The entire contents of the above-identified applications are incorporated herein by reference in their entirety.

BACKGROUND

[0002] As critical dimensions of devices in integrated circuits shrink to the limits of common memory cell technologies, designers have been looking to techniques for stacking multiple planes of memory cells to achieve greater storage capacity, and to achieve lower costs per bit.

[0003] A 3D-NAND memory device is an exemplary device of stacking multiple planes of memory cells to achieve greater storage capacity, and to achieve lower costs per bit. As 3D-NAND technology migrates towards high density and high capacity, especially from 64L to 128L architecture, the number of word line layers (or gate control layers) in a vertical direction perpendicular to a substrate has been increasing significantly. The increasing number of word line layers leads to a dramatic increase of block size of the 3D-NAND memory device, which in turn induces longer read and erase time, longer data transfer time, and lower storage efficiency.

SUMMARY

[0004] The inventive concepts relate to formation of a 3D-NAND memory device with a divided block structure and a method of performing a partial block erase based on the divided block structure.

[0005] A related 3D-NAND memory device can include a plurality of memory cell blocks or memory cell arrays. Each of the blocks can include a plurality of vertical NAND memory cell strings. The vertical NAND memory cell strings can each have one or more bottom select transistors (BSTs), one or more dummy BSTs, a plurality of memory cells (MCs), one or more dummy top select transistors (TSTs), and one or more TSTs that are disposed sequentially and in series over a substrate along a height direction (or Z direction) of the substrate. A source region of a lowermost BST in the each of the vertical NAND memory cell strings is connected to a common source line (CSL), and a drain region of an uppermost TST in the each of the vertical NAND memory cell strings is connected to a bit line. In the related 3D-NAND memory device, the vertical NAND memory cell strings of a same block can share a bottom select gate (BSG). The shared BSG accordingly controls all the BSTs of the vertical NAND memory cell strings in that block simultaneously during operating the related 3D-NAND memory device, such as erasing the related 3D-NAND memory device. As the related 3D-NAND memory device migrates to higher capacity with an increased block size, the shared BSG can induce longer erasing time, longer data transfer time, and lower storage efficiency.

[0006] In the disclosed 3D-NAND memory device, each of the blocks can be separated into a plurality of sub-blocks by dividing the shared BSG into a plurality of sub-BSGs

through one or more first dielectric trenches. Each of the sub-blocks accordingly has a respective sub-BSG, and each of the sub-blocks can be operated individually through controlling the respective sub-BSG. By introducing such a divided BSG structure, the disclosed 3D-NAND memory device can effectively reduce parasitic capacitance and coupling effects between the BSG and adjacent dielectric layers, and significantly improve V_t performance of the bottom select transistors (BSTs). In addition, the erasing time and data transfer time could be reduced significantly, and data storage efficiency can be improved as well.

[0007] In the disclosed 3D-NAND memory device, the each of sub-blocks can also have a respective sub-top select gate (sub-TSG) by dividing a shared/common TSG into a plurality of sub-TSGs through one or more second dielectric trenches. Each of the sub-TSGs can control a respective sub-block during a reading/programming operation. In some embodiments, the first and second dielectric trenches can be formed via a same reticle set so that a manufacturing cost can be reduced.

[0008] According to an aspect of the present disclosure, a memory device is provided. The memory device can include a substrate, a bottom select gate (BSG) disposed over the substrate, a plurality of word lines positioned over the BSG with a staircase configuration and a top select gate (TSG) positioned over the plurality of word lines. The memory device also includes a plurality of insulating layers disposed between the substrate, the BSG, the plurality of word lines, and the TSG. In the disclosed memory device, one or more first dielectric trenches are formed in the BSG and extend in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.

[0009] In addition, one or more second dielectric trenches are formed in the TSG and extend in the length direction (X-direction) of the substrate to separate the TSG into a plurality of sub-TSGs. The memory device further includes one or more common source regions that are formed over the substrate and extend in the length direction of the substrate. Each of the one or more common source regions extends through the BSG, the plurality of word lines, the TSG, and the plurality of insulating layers, and is electrically coupled with the substrate via a respective doped region. The one or more common source regions, the first dielectric trenches and the second dielectric trenches further extend parallel to each other along the length direction of the substrate.

[0010] In some embodiments, the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction (Y-direction) of the substrate and are spaced apart by the plurality of word lines.

[0011] The memory device also includes a plurality of channel structures formed over the substrate along a height direction (Z-direction) of the substrate that is perpendicular to the substrate. Each of the plurality of channel structure passes through the BSG, the plurality of word lines, the TSG and the plurality of insulating layers, and is electrically coupled with the substrate via a respective bottom channel contact that extends into the substrate. The each of the plurality of channel structures further includes a channel layer, a tunneling layer, a charge trapping layer, and a barrier layer.

[0012] The memory device also includes a plurality of dummy channel structures formed along the height direction of the substrate. The plurality of dummy channel structures pass through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate.

[0013] The memory device also includes a plurality of memory cell strings. Each of the memory strings includes a respective channel structure, a respective sub-BSG, the plurality of word lines, a respective sub-TSG, and the plurality of insulating layers that separate the respective sub-BSG, the plurality of word lines, and the respective sub-TSG from one another.

[0014] The memory device also includes a plurality of memory cell sub-blocks. Each of the memory cell sub-blocks including a respective plurality of memory cell strings that are connected to a same sub-BSG and to a same sub-TSG, and each of the memory cell sub-blocks is operated individually.

[0015] The memory device can further include a plurality of dummy channel structures formed along the height direction of the substrate. The plurality of dummy channel structures pass through the BSG, the plurality of word lines, the TSG and the plurality of insulating layers to extend into the substrate.

[0016] In some embodiments, the one or more first dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate so that a plurality of channel structures are disposed therebetween.

[0017] In some embodiments, the memory device further includes one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layers.

[0018] In some embodiments, the memory device further includes one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs, and spaced apart from the plurality of the word lines and the TSG by the plurality of insulating layers.

[0019] According to an aspect of the present disclosure, a method for manufacturing a memory device is provided. In the disclosed method, a bottom select gate (BSG) layer is formed over a substrate, one or more dummy BSG layers are formed over the BSG layer, and a plurality of first insulating layers are disposed between the substrate, the BSG layer, and the one or more dummy BSG layers. Next, one or more first dielectric trenches are formed. The one or more first dielectric trenches pass through the BSG layer, the one or more dummy BSG layers and the plurality of first insulating layers, and extend into the substrate along a length direction of the substrate. The BSG layer is separated by the one or more first dielectric trenches into a plurality of sub-BSG layers, and the one or more dummy BSG layers are separated by the one or more first dielectric trenches into a plurality of dummy sub-BSG layers.

[0020] In the disclosed method, a plurality of word line layers are subsequently formed over the dummy BSG layers, one or more dummy top select gates (TSG) layers are formed over the plurality of word line layers, a TSG layer is formed over the dummy BSG layers, and a plurality of second insulating layers are disposed between the dummy BSG layers, the plurality of word line layers, the one or more dummy TSG layers, and the TSG layer. Next, one or more second dielectric trenches are formed. The second dielectric trenches extend in the length direction of the substrate, and passes through the one or more dummy TSG layers, the TSG layer and a portion of the plurality of second insulating layers that separate an uppermost word line layer, the one or more dummy TSG layers, and the TSG layer from each other. The first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate and are spaced apart by the plurality of word line layers. The TSG layer is separated by the one or more second dielectric trenches into a plurality of sub-TSG layers, and the one or

more dummy TSG layers are separated by the one or more second dielectric trenches into a plurality of dummy sub-TSG layers.

[0021] According to yet another aspect of the present disclosure, a method for erasing a 3D-NAND memory device is provided. The 3D-NAND memory device are formed over a substrate and includes a plurality of vertical NAND strings in which a first block of the plurality of vertical NAND strings are connected to a first bottom select gate (BSG), a second block of the plurality of vertical NAND strings are connected to a second BSG, the first BSG and the second BSG are separated by a dielectric trench, and both the first block and the second block of vertical NAND strings are connected to a plurality of shared word lines. In the disclosed method, the substrate is set to a first voltage, the first BSG is set to a second voltage that is lower than the first voltage, the second BSG is set to a third voltage that is higher than the second voltage, and the one or more word lines are set to a fourth voltage that is equal to zero.

[0022] In some embodiments, the first block of the plurality of vertical NAND strings are erased through applying the second voltage to the first BSG, and the second block of the plurality of vertical NAND strings are not erased through applying the third voltage to the second BSG.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0024] Figure 1A is a cross-sectional view of a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0025] Figure 1B is a top down view of the 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0026] Figure 1C-1 is a first cross-sectional view of a channel structure in the 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0027] Figure 1D-1 is a first top down view of the channel structure in the 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0028] Figure 1C-2 is a second cross-sectional view of a channel structure in the 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0029] Figure 1D-2 is a second top down view of the channel structure in the 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0030] Figure 1E is an equivalent circuit diagram of a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0031] Figure 2 is a schematic perspective view of a 3D-NAND memory device in three-dimensions, in accordance with exemplary embodiments of the disclosure.

[0032] Figure 3A is a cross-sectional view of a related 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0033] Figure 3B is an equivalent circuit diagram of the related 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0034] Figure 4A is a schematic diagram of an operation parameter to erase a related 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0035] Figure 4B is a schematic diagram of another operation parameter to erase a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0036] Figures 5A through 11D are cross-sectional and top down views of various intermediary steps of manufacturing a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0037] Figure 12 is a flowchart of a process for manufacturing a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

DETAILED DESCRIPTION

[0038] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed features may be in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0039] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element

or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0040] FIG. 1A is a cross-sectional view of a 3D-NAND memory device (or memory device) 100, and FIG. 1B is a top down view of the 3D-NAND memory device 100 where the cross-sectional view of the 3D-NAND memory device 100 in FIG. 1A is obtained from a line A-A' along a Z-direction (i.e., height direction) of a substrate in FIG. 1B. Dashed lines in FIG. 1B indicate a perspective view.

[0041] As shown in FIG. 1A, the memory device 100 can have a substrate 10 made of silicon, a high voltage P-type Well (HVPW) 14 formed on a top portion of the substrate 10, and a deep N-type Well 12 that is disposed below the HVPW. The HVPW 14 extends from a top surface of the substrate 10 and into the substrate with a depth from 0.5 μm to 5 μm according to the design requirements. The HVPW 14 can have a top portion and a bottom portion. The top portion (not shown) of the HVPW 14 is level with the top surface of the substrate 10 and is doped with boron at a dopant concentration from 10^{11} cm^{-3} to 10^{14} cm^{-3} . The top portion of the HVPW 14 forms the array (i.e., memory cell region) P-Well. The array P-Well is also known as 'active tub' since voltages are applied to the tub during erasing or programming the memory device. The top portion can also be configured to create bipolar junction transistor (BJT) devices in periphery where control circuits occupy. The bottom portion (not shown) of the HVPW 14 is formed under the top portion and is doped with phosphorus at a dopant

concentration from 10^{11} cm^{-3} to 10^{14} cm^{-3} . The bottom portion creates a deep 'N-Tub' that helps isolate the array P-Well (i.e., the top portion) from the periphery P-Wells. The bottom portion can also be configured to create BJT devices in periphery.

[0042] The deep N-type Well 12 illustrated in FIG. 1A can be doped through a high energy implantation with phosphorus at a dopant concentration from 10^{11} cm^{-3} to 10^{14} cm^{-3} . The deep N-type Well 12 is formed under the HVPW 14, and extends into the substrate with a depth from 0.1 μm to 1 μm according to design requirements. In some embodiments, the deep N-type Well 12 can surround the HVPW 14 to isolate the HVPW 14 from adjacent components.

[0043] Still referring to FIG. 1A, the memory device 100 can also have one or more P⁺ regions 24a and 24b formed in the HVPW 14. The P⁺ regions extend from the top surface of the substrate 10 and into the substrate with a depth from 0.01 μm to 0.2 μm . The P⁺ regions can be doped with boron at a dopant concentration from 10^{14} cm^{-3} to 10^{18} cm^{-3} . In subsequent manufacturing steps, a respective array contact can be formed over each of the P⁺ regions, and the P⁺ regions are configured to reduce resistance between the array contacts and the HVPW.

[0044] Similarly, one or more N⁺ regions 18 and 22 can be formed in the substrate 10. The N⁺ regions 18 and 22 extend from the top surface of the substrate and extend into the substrate with a depth from 0.01 μm to 0.2 μm . The N⁺ regions can be doped with phosphorus at a dopant concentration from 10^{14} cm^{-3} to 10^{18} cm^{-3} . Over the N⁺ regions, one or more substrate contacts (not shown) can be formed in subsequent manufacturing steps, and the N⁺ regions are configured to reduce resistance between the substrate contacts and the substrate.

[0045] The disclosed memory device 100 can also include one or more high voltage N-type Wells (HVNW). Each of the N⁺ regions can be surrounded by a respective high voltage N-type Well (HVNW). For example, the N⁺ region 22 is surrounded by a HVNW 20, and the N⁺ region 18 is surrounded by a HVNW 16. The HVNWs can be formed by doping the substrate with phosphorus at a dopant concentration from 10^{11} cm^{-3} to 10^{14} cm^{-3} . The HVNWs extend from the top surface of the substrate and extend into the substrate 10 with a depth from 0.1 μm to 1 μm . The HVNWs are configured to isolate the N⁺ regions from adjacent components.

[0046] Still referring to FIG. 1A, a bottom select gate (BSG) 62p, one or more dummy BSGs (or bottom dummy word lines, such as 62n-62o), a plurality of word lines (e.g., 62d-62m), one or more dummy top select gates (TSGs) (or top dummy word lines, such as 62b-62c), and a TSG 62a are disposed sequentially over the substrate. In addition, a plurality of insulating layers, such as 17 insulating layers 60a-60q, are disposed between the substrate 10, the BSG, the dummy BSGs, the word lines, the dummy TSGs and the TSG to separate the substrate 10, the BSG, the dummy BSGs, the word lines, the dummy TSGs and the TSG from each other.

[0047] In some embodiments, the insulating layers 60, the BSG, the dummy BSGs, the word lines, the dummy TSGs and the TSG are alternatively stacked over the substrate 10 with a staircase configuration in which the TSG 62a and a uppermost insulating layer 60a have the smallest length, and the BSG 62p and a lowermost insulating layer 60q have the largest length.

[0048] It should be understood that FIG. 1A is merely an exemplary 3D-NAND memory device 100, and the 3D-NAND memory device 100 can include any number of

the BSG, the dummy BSG, the word line, the dummy TSG, and the TSG. For example, the 3D-NAND memory device 100 can have three BSGs, three TSGs, and 64 word lines.

[0049] In some embodiments (i.e. Gate-last Formation Technology), the BSG 62p, the dummy BSGs 62n-62o, the word lines 62d-62m, the dummy TSGs 62b-62c, and the TSG 62a illustrated in FIG. 1A are formed firstly using sacrificial layers (i.e. SiN). The sacrificial layers can be removed and replaced with a high K layer, glue layers and one or more metal layers. The high K layer can be made of aluminum oxide (Al_2O_3) and/or Hafnium oxide (HfO_2) and/or Tantalum oxide (Ta_2O_5), and/or something of high K (Dielectric Constant). The metal layer can be made of tungsten (W), Cobalt (Co), for example. The word lines can have a thickness in a range from 10 nm to 100 nm, according to requirements of product specification, device operation, manufacturing capabilities, and so on. In an embodiment of FIG. 1, the insulating layers 60 can be made of SiO_2 with a thickness from 5 nm to 50 nm.

[0050] Still referring to FIG. 1A, one or more first dielectric trenches (or first trenches), such as two first trenches 26 and 28, are formed in the one or more BSGs (e.g., 62p) and the one or more dummy BSGs (e.g., 62n-62o). The first trenches 26 and 28 extends in an X-direction (i.e., length direction) of the substrate 10 to separate the BSG 62p and the dummy BSGs 62n-62o layers into a plurality of sub-BSGs and sub-dummy BSGs, or to say, a plurality of cell strings. For example, three sub-BSGs 62p-1, 62p-2, and 62p-3 are included in embodiment shown in FIG. 1A. In addition, one or more second dielectric trenches (or second trenches), such as the two second trenches 56 and 58 illustrated in FIG. 1A, are formed in the one or more TSGs (e.g., 62a) and the

one or more dummy TSGs (e.g., 62b-62c). The second trenches also extend in the X-direction (length direction) of the substrate 10 to separate the TSG 62a and dummy TSGs 62b-62c into a plurality of sub-TSGs and sub-dummy TSGs. For example, a sub-TSG 62a-1, two sub-dummy TSGs 62b-1 and 62c-1 are illustrated in FIG. 1A. In some embodiments, the first trenches and the second trenches are optically aligned with each other in a Y-direction (i.e., a width direction, top-down view) of the substrate 10 and are spaced apart by the plurality of word lines 62d-62m. In some embodiments, the first and second trenches can have a CD 50 nm to 150 nm and are filled with SiO₂, SiON, SiOCN, or other suitable dielectric materials. In some embodiments, the first trenches 26 and 28 can extend into the HVPW 14 with a depth between 10 nm and 100 nm.

[0051] By introducing the first and second trenches into the memory device 100, the BSG and TSG are separated into a plurality of sub-BSGs and sub-TSGs. The sub-BSGs and sub-TSGs can divide the memory device 100 into a plurality of sub-blocks, or to say, a plurality of cell strings. Each of the sub-blocks has a respective sub-BSG and a respective sub-TSG. The each of the sub-blocks can be operated individually through controlling the respective sub-BSG and respective sub-TSG. Correspondingly, the disclosed 3D-NAND memory device 100 can precisely control a desired sub-block/array region so as to effectively reduce a programming time, a reading time, an erasing time and data transfer time, and significantly improve data storage efficiency.

[0052] Still referring to FIG. 1A, one or more common source regions (CSRs), such as one common source region 52, is formed over the substrate and extend in the X-direction (length direction) of the substrate. The common source region 52 passes through the BSG 62p, the dummy BSGs 62n-62o, the plurality of word lines 62d-62m, the dummy TSGs

62b-62c, the TSG 62a, and the plurality of insulating layers 60, and is electrically coupled with the substrate 10 via a doped region 54. The common source region 52, the first trenches 26 and 28, and the second trenches 56 and 58 extend parallel to each other in the X-direction (length direction) of the substrate 10. The common source region 52 can have side portions and a bottom portion to be electrically coupled with the doped region 54. A dielectric spacer 68 is formed along the side portions and in direct contact with the word lines 62d-62m and insulating layers 60. A conductive layer 70 is formed along the dielectric spacer 68 and over the doped region 54. The common source region 52 further includes a top contact 64 that is formed along the dielectric spacer 68 and over the conductive layer 70. The doped region 54 can be N-type doped through one or more ion implantation processes. In an embodiment of FIG. 1A, the dielectric spacer 68 is made of SiO₂, the conductive layer 70 is made of polysilicon, and the top contact 64 is made of tungsten.

[0053] In some embodiments, the common source region 52 can have a continuous configuration to extend along the X-direction (length direction) of the substrate. In some embodiments, the common source region 52 can be separated into two or more sub-CSRs. The sub-CSRs are aligned with each other in the X-direction of the substrate.

[0054] In the 3D-NAND memory device 100, a plurality of channel structures are formed over the substrate 10 along a Z-direction (or height direction) of the substrate. As shown in FIG. 1A, five channel structures 30, 32, 34, 36 and 38 are included. Each of the channel structures passes through the BSG, the dummy BSGs, the word lines, the dummy TSGs, the TSG and the insulating layers, and is electrically coupled with the substrate via a respective bottom channel contact that extends into the substrate. For

example, a channel structure 30 is electrically coupled with the substrate via a bottom channel contact 202 that is shown in FIG. 1C. In addition, each of the channel structures further includes a channel layer 206, a tunneling layer 208, a charge trapping layer 210, and a barrier layer 212, which has been shown in FIGS. 1C and 1D for details.

[0055] The memory device 100 can further include a plurality of dummy channel structures that are formed along the Z-direction (height direction) of the substrate. For example, six dummy channel structures 40, 42, 44, 46, 48, and 50 are included in the memory device 100. In some embodiments, the memory device 100 can be divided into three regions: Two staircase regions 100A and 100C and a core region 100B. As shown, the staircase regions 100A and 100C can be arranged on single or both sides of the central core region 100B of the memory device 100. The staircase regions 100A and 100C do not include any channel structures, and the core region 100B includes the plurality of channel structures. In some embodiments, the dummy channel structures are formed in the staircase regions 100A and 100C only, and pass through the BSG, the dummy BSGs, the word lines and the insulating layers to extend into the substrate. In other embodiments, the dummy channel structures can be formed in both the staircase regions 100A and 100C and the core region 100B. When the dummy channel structures are formed in the core region 100B, the dummy channel structures pass through the TSG, the dummy TSGs, the word lines, the dummy BSGs, and the BSG, and extend into the substrate. The dummy channel structures serve as sustain components to support the staircase regions and/or the core regions when sacrificial word lines are removed. In an embodiment of FIG. 1A, the dummy channel structures are made of SiO₂.

[0056] FIG. 1B is a top down view of the 3D-NAND memory device 100 in accordance with some embodiments of the disclosure. As shown in FIG. 1B, the memory device 100 can have three common source regions 52a-52c that extend along the X-direction (length direction) of the substrate 10. The common source regions 52b and 52C are disposed at two boundaries of the memory device 100 with a continuous configuration. The common source regions 52b and 52C can serve as common source regions for the memory device 100, and further isolate the memory device 100 from adjacent components. In some embodiments, the memory device 100 is one of memory cell blocks of a 3D-NAND chip (not shown). The common source regions 52b and 52C accordingly isolate the memory device 100 (or the memory cell block 100) from adjacent memory cell blocks of the 3D-NAND chip. The common source region 52a is disposed at a middle position of the memory device 100. The common source region 52a is separated into two or more sub-CSRs by one or more “H-Cuts”. As shown in FIG. 1B, the CSR 52a is separated by an H-cut 72 into two sub-CSRs 52a-1 and 52a-2.

[0057] Still referring to FIG. 1B, the first trenches 26 and 28, and the second trenches 56 and 58 are optionally aligned with each other at the Y direction (width direction) of the substrate 10. The first trenches and the second trenches are disposed between two adjacent common source regions. For example, the first trench 26 and the second trench 56 are aligned and disposed between a common source region 52a and a common source region 52b. In addition, the dummy channel structures 40, 42, and 44 are positioned at the staircase region 100A, and the dummy channel structures 46, 48, and 50 are positioned at the staircase region 100C. A plurality of channel structures, such as channel structures 30 and 32, are disposed in the core region 100B.

[0058] By introducing the first/second trenches, the 3D-NAND memory device 100 (or memory cell block 100) can be divided into a plurality of sub-blocks. For example, three sub-blocks SUB-BLK 1-3 are formed in FIG.1B. Each sub-block can have a respective sub-BSG and a respective sub-TSG. The sub-BSG is formed by separating the BSG 62p into three sub-BSGs (i.e., 62p-1, 62p-2, and 62p-3) by the first trenches, and the sub-TSG is formed by separating the TSG 62a into three sub-TSGs by the second trenches. It should be mentioned that the SUB-BLK 2 can have two portions SUB-BLK2_1 and SUB_BLK_2 that are electrically connected with each other through the H-Cut 72. Accordingly, The SUB-BLK 2 can have a larger size than the SUB-BLK 1 and SUB-BLK 3. Without the introduction of the first/second trenches, the memory device 100 (or the memory cell block 100) has a shared BSG, such as 62p, and a shared TSG, such as 62a.

[0059] It should be understood that FIG. 1B is merely an exemplary 3D-NAND memory device 100, and the 3D-NAND memory device 100 can include any number of first trenches or second trenches between two adjacent common source regions. For example, two or more first trenches or two or more second trenches can be disposed between two adjacent common source regions. The 3D-NAND memory device 100 can also include any number of common source regions.

[0060] FIG. 1C-1 is a first cross-sectional view of the channel structure 30 in the 3D-NAND memory device 100, and FIG. 1D-1 is a first top down view of the channel structure 30 where the cross-sectional view of FIG. 1C-1 is obtained from a line B-B' along a Z-direction (height direction) of a substrate in FIG. 1D-1. FIG. 1C-2 is a second cross-sectional view of the channel structure 30 and FIG. 1D-2 is a second top

down view where the cross-sectional view of FIG. 1C-2 is obtained from a line C-C' along a Z-direction (height direction) of a substrate in FIG. 1D-2.

[0061] As shown in FIGS. 1C-1/1D-1, the channel structure 30 can have a cylindrical shape with sidewalls and a bottom region. Of course, other shapes are possible. The channel structure 30 is formed along a Z-direction perpendicular to the substrate 10, and electrically coupled with the substrate 10 via a bottom channel contact 202 that is positioned at the bottom region of the channel structure. The channel structure 30 further includes a channel layer 206, a tunneling layer 208, a charge trapping layer 210, and a barrier layer 212. The barrier layer 212 is formed along the sidewalls of the channel structure 30 and over bottom channel contact 202. The barrier layer 212 is in direct contact with the word lines 62d-62m and the insulating layers 60. The charge trapping layer 210 is formed along the barrier layer 212 and over the bottom channel contact 202, and the tunneling layer 208 is formed along the charge trapping layer 210 and over the bottom channel contact 202. The channel layer 206 has side portions that is formed along the tunneling layer 208 and has a T-shape bottom portion that extends through bottom portions of the tunneling layer 208, the charge trapping layer 210, and the barrier layer 212 that are positioned over the bottom channel contact 202. The T-shape bottom portion of the channel layer 206 further is positioned over and in direct contact with the bottom channel contact 202. In addition, the tunneling layer 208, the charge trapping layer 210, and the barrier layer 212 can form an “L-foot” configuration in the channel structure 30. The L-foot configuration can include side portions that are formed along the sidewalls of the channel structure and a bottom portion over the bottom channel contact 202.

[0062] The channel structure 30 can also have a channel insulating layer 204 that is formed along the channel layer 206 to fill the channel structure 30. The channel insulating layer 204 can have a T-shape bottom portion that extends through bottom portions of the channel layer 206, the tunneling layer 208, the charge trapping layer 210, and the barrier layer 212 and lands on the channel layer 206. In some embodiments, the channel insulating layer 204 can include a void that is positioned in a middle position of the channel insulating layer 204. The channel structure 30 can further include a top channel contact 214 that is formed along the channel insulating layer 204 and in direct contact with the channel layer 206. The top channel contact 214 is positioned above the TSG 62a to prevent any electrical interference between the top channel contact 214 and the TSG 62a. In the channel structure 30, a gate dielectric layer 216 is further formed between the BSG 62p and the bottom channel contact 202. The gate dielectric layer 216 can be positioned between the insulating layer 60p and 60q, and have an annular shape to surround the bottom channel contact 202.

[0063] In an embodiment of FIGS. 1C-1/1D-1, the barrier layer 212 is made of SiO_2 . In another embodiment, the barrier layer 212 can include multiple layers, such as SiO_2 and Al_2O_3 . In an embodiment of FIGS. 1C-1/1D-1, the charge trapping layer 210 is made of SiN . In another embodiment, the charge trapping layer 210 can include a multi-layer configuration, such as a SiN/SiON/SiN multi-layer configuration. In some embodiments, the tunneling layer 208 can include a multi-layer configuration, such as a SiO/SiON/SiO multi-layer configuration. In an embodiment of FIGS. 1C-1/1D-1, the channel layer 206 is made of polysilicon via a furnace low pressure chemical vapor

deposition (CVD) process. The channel insulating layer 204 can be made of SiO₂, and the top and bottom channel contacts can be made of polysilicon.

[0064] As shown in FIGS. 1C-1/1D-1, the channel structure 30 can have a cylindrical shape. However, the present disclosure is not limited thereto, and the channel structures 30 may be formed in other shapes, such as a square pillar-shape, an oval pillar-shape, or any other suitable shapes.

[0065] FIGS. 1C-2/1D-2 provides another configuration to dispose the top channel contact 214 in the channel structure 30. As shown in FIGS. 1C-2/1D-2, the top channel contact 214 is formed along the insulating layer 60a and over the channel layer 206, tunneling layer 208, charge trapping layer 210, barrier layer 212, and channel insulating layer 204. A bottom surface of the top channel contact 214 is in direct contact with a top surface of the channel layer 206. Comparing to the top channel contact 214 in FIGS. 1C-1/1D-1, the top channel contact 214 in FIGS. 1C-2/1D-2 has a larger size which in turn provides a bigger process window to dispose a subsequently formed Via over the top channel contact.

[0066] FIG. 1E is an equivalent circuit diagram of a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure. As shown in FIG. 1E, the circuit diagram includes a memory cell block 200 or memory cell array 200. The memory cell block 200 can include a plurality of vertical NAND memory cell strings ST0-ST17. Each of the memory cell strings can have one or more bottom select transistors (BSTs), one or more dummy BSTs (DUMBSTs), a plurality of memory cells (MCs), one or more dummy top select transistors (DUMTSTs), and one or more TSTs. For example, a memory cell string ST0 can have a BST, two dummy BSTs (DUMBST0

and DUMBSTn), 64 memory cells MC0-MC63, two dummy TSTs (DUMTST0 and DUMTSTn), and two TSTs (TST0 and TSTn). A top end of each of the memory cell strings can be a drain region that is connected to a bit line (BL), and a bottom end of each of the memory cell strings can be a source region that is connected to a common source line (CSL). For example, the memory cell string ST0 is connected to a bit line BL1 through the drain region of the TSTn and is connected to a CSL through the source region of the BST.

[0067] The memory cell block 200 can be divided into six sub-blocks from SUB-BLK0 to SUB-BLK5 by the first and second trenches that are illustrated in FIG. 1A. Each of the sub-blocks can have a respective set of memory cell strings. For example, SUB-BLK0 can include a set of memory cell strings ST0, ST6 and ST12, and SUB-BLK1 can include another set of memory cell strings ST1, ST7 and ST13.

[0068] In a related memory cell block, such as a memory cell block 400 shown in FIG. 3B, a bottom select gate (BSG) of each of the memory cell strings are connected to each other and shared. Similarly, a dummy BSG of each of the memory cell strings is also connected to each other and shared. In the memory cell block 200, the bottom select gate BSG and the dummy BSGs (e.g., DUMBSG0 and DUMBSGn) can be separated into a plurality of sub-BSGs and sub-dummy BSGs by the first trenches, such as 26 and 28 illustrated in FIG. 1A. For example, the BSG can be separated by the first trenches into a plurality of sub-BSGs from BSG0 to BSG5. In addition, the top select gates TSGs (e.g., TSG0 and TSGn), and the dummy TSGs (e.g., DUMTSG0 and DUMTSGn) can be separated into a plurality of sub-TSGs and sub-dummy TSGs by the second trenches,

such as 56 and 58 illustrated in FIG. 1A. For example, the TSG0 can be separated by the second trenches into a plurality of sub-TSGs from TSG0-0 to TSG0-5.

[0069] Accordingly, the BSTs, the dummy BSTs, the dummy TSTs, and the TSTs in each of the sub-blocks can have respective control gates that are sub-BSGs, sub-dummy BSGs, sub-dummy TSGs and sub-TSGs respectively. For example, in SUB-BLK0, the BSTs of the strings ST0, ST6 and ST12 have an individual control gate of BSG0 that is formed by the first trenches to separate the control gate BSG, and the TST0s of the strings ST0, ST6, ST12 have an individual control gate of TSG0-0 that is formed by the second trenches to separate the control gate TSG. Similarly, in SUB-BLK1, the BSTs of ST1, ST7 and ST13 have a control gate of BSG1 and the TST0s of ST1, ST7 and ST13 have a control gate of TSG0-1. Without the introduction of the first/second trenches, the memory cell block 200 has shared BSG, dummy BSGs, dummy TSGs, and TSG. An exemplary shared BSG is illustrated in FIGS. 3A and 3B where the BSG of each of the memory cell strings are connected to each other and shared.

[0070] By introducing such a divided BSG structure, the disclosed 3D-NAND memory device can effectively reduce parasitic capacitance and coupling effects between the BSG and adjacent dielectric layers, and significantly improve V_t performance of the bottom select transistors (BSTs). In addition, the divided BSG structure allows erasing a specific sub-block rather than the entire memory cell block 200. Accordingly, the erasing time and data transfer time could be reduced significantly, and data storage efficiency can be improved as well. Further, the divided TSG structure allows reading/programming a specific sub-block rather than the entire memory cell block 200,

which in turn reduces the reading/programming time and improves the data transfer/storage efficiency.

[0071] In the memory cell block 200, the sub-blocks can share one or more word lines. For example, as shown in FIG. 1E, 18 MCNs in six sub-blocks are connected to each other and have a common/shared word line WLn. Similarly, other MCs in all six sub-blocks can also have common/shared word lines.

[0072] The each of the sub-blocks can have one or more bit line connections. For example, in sub-block SUB-BLK0, the memory cell string ST0 is connected to BL1, the memory cell string ST6 is connected to BL2, and the memory cell string ST12 is connected to BLn. In the disclosed memory cell block 200, all the 18 memory cell strings are connected to a same CSL (or common source region).

[0073] Still referring to FIG. 1E, each of the memory cell strings can be constituted by one or more sub-BSGs, one or more sub-dummy BSGs, a plurality of word lines, one or more sub-dummy TSGs, one or more sub-TSGs, and a channel structure that pass through the sub-TSGs, sub-dummy TSGs, word lines, sub-dummy BSGs, and sub-BSGs, and is electrically coupled to a substrate/a same common source region (i.e., CSL). For example, a memory cell string ST0 can be constituted by a channel structure 30, a sub-BSG 62p-1 (i.e., BSG0 in FIG. 1E), two sub-dummy BSGs 62n-1 and 62o-1, word lines 62d-62m, two sub-dummy TSGs 62b-1 and 62c-1, and a sub-TSG 62a-1 (i.e., TSG0-1 in FIG. 1E), which are illustrated in FIG. 1A. It should be noted that the TSGn is not illustrated in FIG. 1A. Accordingly, the bottom select transistor (BST) of the string ST0 can be constituted by the channel structure 30 and the sub-BSG 62p-1. A memory cell, such as MC63 can be constituted by the channel structure 30 and the word line 62d. The

top select transistor TST0 can be formed by the channel structure 30 and the sub-TSG 62a-1. The DUMSTST0 can be formed by the channel structure 30 and the sub-dummy TSG 62c-1. The common source line (CSL) illustrated in FIG. 1E can be the common source region 52 illustrated in FIG. 1A.

[0074] FIG. 2 is a schematic perspective view of a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure. As shown in FIG. 2, a plurality of dummy channel structures, such as 40, 42, 44, 46, 48, and 50 are disposed in the staircase regions. A plurality of channel structures, such as 30 and 38, are positioned in the core region. Two first trenches (26 and 28) and two second trenches (56 and 58) are formed along the X-direction, aligned at the Y-direction, and spaced apart from each other by a plurality of word lines 62d-62m. The first trenches separate the BSG 62p, the dummy BSGs (62n and 62o) into a plurality of sub-BSGs and a plurality of sub-dummy BSGs respectively. For example, three sub-BSGs 62p-1, 62p-2, and 62p-3 are included in embodiment shown in FIG. 2. Similarly, the second trenches separate the TSG 62a, the dummy TSGs (62b and 62c) into a plurality of sub-TSGs and a plurality of sub-dummy TSGs respective. A plurality of insulating layers 60a-60q are formed between the substrate, the BSG, the dummy BSGs, the word lines, the dummy TSGs, and the TSG. A common source region 52 is formed along the X-direction and disposed with the first and second trenches in parallel. The common source region 52 passes through the TSG, the dummy TSGs, the word lines, the dummy BSGs, and the BSG, and extends into the substrate 10. The common source region 52 is separated by the H-Cut 72 into two sub common source regions.

[0075] FIG. 3A is a cross-sectional view of a related 3D-NAND memory device 300 that is obtained along a Z-direction (height direction) of a substrate. Comparing to the memory device 100, the related 3D-NAND memory device 300 does not include the first trenches, such as 26 and 28 that are illustrated in FIG. 1A.

[0076] FIG. 3B illustrates an equivalent circuit diagram of the related 3D-NAND memory device 300. As shown in FIG. 3B, the circuit diagram includes a memory cell block or memory cell array 400. The memory cell block 400 can include six sub-blocks from SUB-BLK0 to SUB-BLK5 by the second trenches, such as 56 and 58 in FIG. 3A. Similar to the memory device 100, the top select gates TSGs (e.g., TSG0 and TSGn), and the dummy TSGs (e.g., DUMTSG0 and DUMTSGn) can be separated into a plurality of sub-TSGs and sub-dummy TSGs by the second trenches. For example, the TSG0 can be separated by the second trenches into a plurality of sub-TSGs from TSG0-0 to TSG0-5. Accordingly, each of the sub-blocks can have respective sub-TSGs and respective sub-dummy TSGs. For example, a sub-block SUB-BLK0 can have a sub-TSG TSG0-0, and a sub-block SUB-BLK1 can have a sub-TSG TSG0-1. The difference between the related 3D-NAND memory device 300 and the disclosed memory device 100 is that in the related 3D-NAND memory device 300, the BSG or dummy BSGs (e.g., DUMBSG0 and DUMBSGn) in each of the sub-blocks are connected to each other and shared.

[0077] FIG. 4A is a schematic diagram of an operation parameter to erase a related 3D-NAND memory device 300, in accordance with exemplary embodiments of the disclosure. Figure 4B is a schematic diagram of another operation parameter to erase a

3D-NAND memory device 100, in accordance with exemplary embodiments of the disclosure.

[0078] As shown in FIG. 4A, during erasing the related 3D-NAND memory device 300, the word lines that control the memory cells (MCs) are set to an operating voltage equal to zero volt (V). An input voltage applied to the HVPW, such as the HVPW 14 in FIG. 3A, can be set to a first operating voltage V1. The first operating voltage V1 can be positive and have a value between 18 V and 22 V. An input voltage to a selected BSG of a specific sub-block, such as SUB-BLK0 in FIG. 3B, can be set to a second operating voltage V2 that can be lower than the first operating voltage but still positive. For example, the second operating voltage V2 can be in a range from zero volt to 13 V. In addition, the dummy BSGs in the specific sub-block can be set to a switch voltage (not shown in FIG. 4A) that is 0.5 V-2 V lower than the second operating voltage V2. In some embodiments, the selected BSG and the selected dummy BSGs in the specific sub-block can be set to float.

[0079] A detailed erasing process can be described base on the channel structure 30 that is illustrated in FIGS. 1C and 1D and the memory cell string ST0/sub-block SUB-BLK0 that is illustrated in FIGS. 1E and 3B. It should be mentioned again, the memory cell string ST0 can be constituted by the channel structure 30 and the surrounding BSG, dummy BSGs, word lines, dummy TSGs, and TSG that are illustrated in FIGS. 1C and 1D.

[0080] As shown in FIGS. 1C and 1D, when the first operating voltage is applied to the HVPW 14, the first operating voltage V1 is electrically coupled to the channel layer 206 via the bottom channel contact 202. Because the word lines 62d-62m are all set to

an operating voltage equal to zero volt, the channel layer 206 forms a relatively high electric potential with respect to the word lines. The formed high electric potential attracts the electrons that are trapped in the charge trapping layer 210 back to the channel layer 206. In addition, holes can be injected into the channel layer by the first operating voltage V1 from the HVPW 14/common source region 52. The injected holes can sustain a positive potential in the channel layer and further recombine with the attracted electrons in the channel layer 206. When the electron-hole recombination is completed, the memory cell string ST0 is erased. Accordingly, the input voltages V1, V2 are set to zero volt.

[0081] During the easing operation, the selected BSG is either set to float or set to the second operating voltage V2 that allows the selected BSG to stay at a positive voltage relatively lower than the first voltage V1 that is applied to the HVPW 14. Such a relative lower voltage can reduce the electric field across the gate dielectric (e.g., gate dielectric layer 216 shown in FIG. 1C) and the reduced electric field in turn can prevent the gate dielectric layer from breaking down. In some embodiments, the second voltage V2 applied to the selected BSG can further help generate hole through a gate induced drain leak (GIDL) effect and improve the holes to flow from the substrate to a top portion of the channel layer 206 (e.g., a position close to the TSG).

[0082] In some embodiments, the dummy BSGs are either set to float or set to the switch voltages (not shown). The applied switch voltages can be reduced gradually in the direction from BSG 62p toward word line 62m. A gradual reduction in the voltage on dummy BSGs in the direction from BSG toward word lines may reduce the electric field between the BSG (set at a high voltage) and word lines (set at a low voltage, such

as zero), hence reducing carrier generation between BSG and word lines and eliminating erase disturb.

[0083] Since the related memory device 300 has a common or shared BSG, when the second voltage V2 is applied to the BSG of string ST0/SUB-BLK0 during the easing operation, the bottom select transistors (BSTs) in rest of 17 memory cell strings ST1-ST17 can also be affected and turned on by the second operating voltage V2. Correspondingly, the erasing operation can take place in all six sub-blocks. As the 3D-NAND memory device migrates to higher capacity with an increasing block size, the common/shared BSG can induce longer erasing time, longer data transfer time, and lower storage efficiency.

[0084] FIG. 4B is a schematic diagram of another operation parameter to erase a 3D-NAND memory device 100. As shown in FIG. 1E, each of the sub-blocks illustrated in FIG. 1E can have a respective sub-BSG that is formed by introducing the first trenches to separate the BSG. When an erasing operation is started, the second voltage V2 can be applied to a respective sub-BSG of a selected sub block. For example, if the SUB-BLK0 is selected, the second voltage V2 can be applied to the corresponding sub-BSG BSG0. In addition, a third voltage V3 can be applied to a respective sub-BSG of an un-selected sub block. For example, if the SUB-BLK1 is un-selected, the third voltage V3 can be applied to the corresponding sub-BSG BSG1. The third voltage V3 can be close to the first voltage V1 and higher than the second voltage V2. For example, the V3 can be ranged from 18 V to 25 V. The relative higher third voltage V3 with respect to the second voltage V2 can repeal the holes that are generated from the HVPW/substrate and inhibiting the holes from flowing into the channel layer of the un-

selected sub-block. Accordingly, the erasing process can take place in the selected sub-block only, and the erasing time and data transfer time could be reduced significantly, and data storage efficiency can be improved as well.

[0085] Figures 5A through 11D are cross-sectional and top down views of various intermediary steps of manufacturing a 3D-NAND memory device 100 in accordance with exemplary embodiments of the disclosure.

[0086] FIG. 5A is a cross-sectional view that is obtained along a Z-direction (i.e., height direction) of a substrate. As shown in FIG. 5A, a plurality of doped regions 12, 14, 16, 18, 20, 22, and 24 are formed in a substrate 10 based on a photolithography process and a doping and/or ions implantation process. The doped regions in FIG. 5A may be substantially similar to the doped regions discussed above with reference to FIG. 1A. In order to form the doped regions, a patterned mask can be formed over the substrate by the photolithography process. The patterned mask exposes desired regions of the substrate that need dopant. A doping process, such as an ion implantation process, an in situ doped epitaxial growth, a plasma doping process (PLAD), or other methods as known in the art, can be applied to transfer suitable dopant into the exposed regions of the substrate 10. A dopant concentration, a doping profile, and a doping depth can be controlled by adjusting the energy, angle and dopant type of the doping process.

[0087] Over the substrate 10, a bottom select gate (BSG) 62p, two dummy BSGs 62n-62o, and a plurality of first insulating layers 62n-62q can be subsequently formed. The substrate 10, BSG 62p and the dummy BSGs 62n-62o are spaced apart from each other by the first insulating layers 60n-60q.

[0088] The BSG 62p and the two dummy BSGs 62n-62o can be sacrificial layers that are made of SiN. The sacrificial layers can be removed and replaced with a high K layer and a metal layer in future manufacturing steps. The BSG 62p and the two dummy BSGs 62n-62o can have a thickness in a range from 10 nm to 100 nm. The first insulating layer can include SiO, SiCN, SiOCN, or other suitable materials. The first insulating layers 60n-60q can have a thickness from 5 nm to 50 nm. Any suitable deposition process can be applied to form the BSG, the dummy BSGs and the first insulating layers, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), diffusion, or any combination thereof.

[0089] Still referring to FIG. 5A, two first trenches 26 and 28 can be formed in the BSG 62p and dummy BSGs 62n-62o when the BSG, dummy BSGs and the first insulating layers are stacked over the substrate 10. The first trenches 26 and 28 extends in a X-direction (i.e., a length direction) of the substrate 10 to separate the BSG 62p and the dummy BSGs 62n-62o into a plurality of sub-BSGs and sub-dummy BSGs. For example, three sub-BSGs 62p-1 to 62p-3, and three sub-dummy BSGs 62n-1 to 62n-3 are included in FIG. 5A.

[0090] The first trenches 26 and 28 can have a CD from 50 nm to 150 nm. The first trenches can be filled with SiO₂, SiON, SiOCN, or other suitable dielectric materials. In some embodiments, the first trenches 26 and 28 can extend into the HVPW 14 with a depth between 10 nm and 100 nm. The first trenches can be formed by a photolithography process, a subsequent etching process, filling with dielectric materials then CMP (Chemical Mechanical Polish) when necessary. For example, a patterned mask stack can be formed over the insulating layer 60n by the photolithography

process. A subsequent etching processing can be introduced to etch through the insulating layers, the BSG, the dummy BSGs and further extend into the HVPW 14 to form two trench openings. The trench openings then can be filled with a dielectric material, such as SiO₂, SiON, SiOCN, or other suitable materials by applying a chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), diffusion, or any combination thereof. A surface planarization may be performed to remove any excessive dielectric materials over the insulating layer 60n.

[0091] FIG. 5B is cross-sectional view that is obtained along an X-direction (a length direction) of the substrate, and FIG. 5C is a top down view to illustrate a final structure when the first trenches 26 and 28 are formed. As shown in FIG. 5B, the first trenches 26 and 28 cannot be observed when the cross-sectional view is made along the X-direction (length direction) of the substrate 10. In FIG. 5C, the insulating layer 60n is shown as a top surface and the two first trenches 26 and 28 extend along the length direction of the substrate and further separate the substrate 10 into three equal regions.

[0092] In FIG. 6, a plurality of word lines 62d-62m, two dummy top select gates (TSGs) 62b-62c, and a TSG 62a are sequentially formed on the first insulating layer 60n. A plurality of second insulating layers 60a-60m are also deposited over the first insulating layer 60n. The word lines 62d-62m, the dummy TSGs 62b-62c, and the TSG 62a are spaced apart from each other by the second insulating layers 60a-60m. The word lines 62d-62m, the dummy TSGs 62b-62c, and the TSG 62a can be sacrificial layers that are made of SiN and have a thickness in a range from 10 nm to 100 nm. The sacrificial layers can be removed and replaced with a high K layer and a metal layer in the future manufacturing steps. The second insulating layers 60a-60m can have a

thickness between 5 nm and 50 nm, and include SiO₂, SiCN, SiOCN, or other suitable materials. Any suitable deposition process can be applied to form the TSG, the dummy TSGs and the second insulating layers, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), diffusion, or any combination thereof.

[0093] In FIG. 7A, two staircase regions 100A and 100C are formed. The formation of the two staircase regions 100A and 100C can be illustrated in exemplary manufacturing steps that are shown in FIGS. 7B-7F. As shown in FIG. 7B, a plurality of word lines 62a-62c and a plurality of insulating layers 60a-60c can be formed and disposed alternatively. As mentioned above, the word line 62a can function as the TSG, and the 62b-62c can function as the dummy TSGs. A patterned mask stack 702 can be formed on the insulating layer 60a. The patterned mask stack 702 exposes two end portions of the insulating layer 60a. The mask stack 702 can include an amorphous carbon hard-mask layer, a dielectric anti-reflective coating (DARC), a bottom anti-reflective coating (BARC) layer, and a photoresist layer. In some other embodiments, the mask stack 702 can be only photoresist for staircase formation. The mask stack 702 can be patterned according to any suitable technique, such as a lithography process (e.g., photolithography or e-beam lithography) which may further include photoresist coating (e.g., spin-on coating), soft baking, mask aligning, exposure, post-exposure baking, photoresist developing, rinsing, drying (e.g., spin-drying and/or hard baking), and the like.

[0094] In FIG. 7C, a first plasma etching process can be performed to remove the exposed end portions of the insulating layer 60a. The first plasma etching process

further removes portions of underlying word line 62a that are not protected by the mask stack 702 and stops on the insulating layer 60b by a precise process control. In FIG. 7D, a trim process can be applied to remove portions of the mask stack 702 from two ends to expose the insulating layer 60a further. The exposed portions of the insulating layer 60a can be two end portions 60a-A and 60a-B. In addition, the insulating layer 60b can have exposed end portions 60b-A and 60b-B.

[0095] In FIG. 7E, a second etching process can be performed. The second etching process can remove the exposed end portions 60a-A and 60a-B from insulation layer 60a. By precisely controlling the second etching process either through an etching time or end point traces, the second etching process further removes portions of word line 62a under the 60a-A and 60a-B and stops on the insulating layer 60b. In the meanwhile, the exposed end portions 60b-A and 60b-B from insulating layer 60b and portions of word line 62b under the 60b-A and 60b-B can be removed simultaneously. Upon the completion of the second etching process, two staircase regions can be formed at two sides. In FIG. 7F, a subsequent plasma ashing can be applied to remove the remaining mask stack 702. Briefly, a multi-cycle Trim - Etch process on multiple masks (As illustrated in FIGS. 7B-7F) can be applied to form the staircase regions 100A and 100C in FIG. 7A.

[0096] In FIG. 8A, two second trenches 56 and 58 can be formed in the TSG 62a and dummy TSGs 62b-62c. The second trenches 56 and 58 extend in the X-direction (i.e., a length direction) of the substrate 10 to separate the TSG 62a and the dummy TSGs 62b-62c into a plurality of sub-TSGs, and a plurality of sub-dummy TSGs respectively. For example, three sub-TSGs 62a-1, 62a-2, and 62a-3 can be included in FIG. 8A. In some

embodiments, the second trenches 56 and 58 can be aligned with the first trenches 26 and 28 in the Y-direction (width direction) of the substrate.

[0097] The second trenches 56 and 58 can have a CD 50 nm to 150 nm and include SiO₂, SiON, SiOCN, or other suitable dielectric materials. The second trenches can be formed by a photolithography process and a subsequent etching process. For example, a patterned mask stack can be formed over the insulating layer 60a based on the photolithography process. The subsequent etching processing is introduced to etch through the insulating layers 60a-60d, the TSG 62a, the dummy TSGs 62b-62c and stop on the word line 62d to form two trench openings. The trench openings then can be filled with a dielectric material, such as SiO₂, SiON, SiOCN, or other suitable materials by applying a chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), diffusion, or any combination thereof. A surface planarization, such as a CMP process, can be performed to remove any excessive dielectric materials over the insulating layer 60a. After the surface planarization, the dielectric material that remains in the trench openings forms the second trenches.

[0098] FIG. 8B is cross-sectional view that is obtained along the X-direction (length direction) of the substrate, and FIG. 8C is a top down view to illustrate a final structure when the second trenches 56 and 58 are formed. As shown in FIG. 8B, both the first and the second trenches cannot be observed when the cross-sectional view is made along the X-direction (length direction) of the substrate 10. In FIG. 8C, the insulating layer 60a is a top layer. The second trenches 56 and 58 are formed along the length direction of the substrate and further are aligned with the first trenches 26 and 28 in the Y-direction (width direction) of the substrate 10. The first trenches and the second trenches together

separate the substrate 10 into three regions (or sub-blocks). In addition, two staircase regions 100A and 100C are positioned at two sides and a core region 100B is positioned in middle of the substrate.

[0099] FIG. 9A is a cross-sectional view obtained in the Z-direction (height direction) of the substrate to illustrate the formation of a plurality of channel structures. In order to form the channel structures, a plurality of channel openings can be formed firstly. The channel openings can be formed through a photolithography process to form a patterned mask and a subsequent etching process to transfer the patterns of the mask. The formed channel openings can pass through the TSG, the dummy TSGs, the word lines, the dummy BSGs, and the BSG, and further extend into the HVPW 14. Each of the channel openings can have side portions and a bottom portion to expose the HVPW 14. When the channel openings are formed, a plurality of bottom channel contacts, such as the bottom channel contact 202 illustrated in FIG. 1C, can be formed at the bottom portions of the channel openings. Each of the channel openings can have a respective bottom contact at the bottom portion. The bottom channel contacts can protrude from the BSG 62p, and a top surface of each of the bottom channel contacts can be positioned between the BSG 62p and the dummy BSG 62o.

[0100] Still referring to FIG. 9A, once the bottom channel contacts are formed, a barrier layer, a charge trapping layer, and a tunneling layer can be formed sequentially along the side portions of the channel openings and over the bottom channel contacts. A subsequent anisotropic plasm etching can be applied to remove portions of the barrier layer, the charge trapping layer, and the tunneling layer that are disposed over the bottom channel contacts to form a plurality of interconnect opening. Each interconnect

opening exposes a respective bottom channel contact. A channel layer can be formed subsequently along the side portions of the channel openings and further extends through the interconnect openings to connect the bottom channel contacts.

[0101] Once the channel layer is formed, the channel layer can have side portions that are formed along the tunneling layer and a T-shape bottom portion that extends through bottom portions of the tunneling layer, the charge trapping layer, and the barrier layer that are positioned over the bottom channel contact. The T-shape bottom portion of the channel layer is in direct contact with the bottom channel contact, which can be shown in FIGS. 1C and 1D. In addition, the tunneling layer, the charge trapping layer, and the barrier layer can form an L-foot configuration in the channel openings. The L-foot configuration can include side portions that are formed along the sidewalls of the channel openings and a bottom portion over the bottom channel contacts.

[0102] In some embodiments, once the channel layer is formed, a subsequent annealing process can be applied, one is to release wafer stress, the other is to reduce defects (dangling bonds), in some cases, it's also to transform the channel layer into polycrystalline. In some embodiments, the formation of the channel structure further includes forming a channel insulating layer over the channel layer to fill the channel openings, and forming a top channel contact over the channel insulating layer and the top channel contact is in direct contact with the channel layer. A detailed channel structure can be illustrated in FIGS. 1C and 1D.

[0103] FIG. 9B is top down view to illustrate the formation of a plurality of channel structures. As shown in FIG. 9B, the plurality of channel structures can be formed in the core region 100B and separated by the second trenches 56 and 58 into 3 sub-blocks.

[0104] FIG. 10A is a cross-sectional view obtained in the Z-direction (height direction) of the substrate to illustrate the formation of a plurality of dummy channel structures 40, 42, 44, 46, 48, and 50. The dummy channel structures serve as sustain components to support the staircase regions 100A and 100C and/or the core regions 100B when sacrificial word lines are removed and replaced with metals. In order to form the dummy channel structures, a plurality of dummy channel openings can be formed firstly. The dummy channel openings can be formed through a photolithography process to form a patterned mask and a subsequent etching process to transfer the patterns of the mask. The dummy channel openings can be formed in the staircase regions. The formed dummy channel openings can pass through the word lines, the dummy BSGs, and the BSG, and further extend into the HVPW 14. Each of the dummy channel openings can have side portions and a bottom portion to expose the HVPW 14. When the dummy channel openings are formed, a dielectric layer can be formed to fill the dummy channel openings. The dielectric layer can include SiO₂, SiCN, SiOCN, or other suitable materials. A subsequent surface planarization, such as a CMP process, may be required to remove any excessive dielectric layer over the insulating layer 60a. Once the surface planarization is completed, the dielectric layer that remains in the dummy channel openings forms the dummy channel structures.

[0105] In some embodiments, the dummy channel structures can have a critical dimension (CD) between 50 nm and 200 nm. In some embodiments, the dummy channel structures can extend into the HVPW 14 with a depth between 10 nm and 200 nm. The dummy channel structures can have a circular shape. In some embodiments, the dummy channel structures can have non-circular shapes, such as a capsule shape, a rectangular

shape, an arc shape, a bone shape, and the like. The non-circular shapes can be adjusted by two or more parameters, such as width, length, arc radius, arc angle, and the like. Further, in some embodiments, the non-circular shapes can be arranged in a symmetric pattern or in a non-symmetric pattern with regard to other contacts in the staircase regions.

In some embodiments, the dummy channel structures can be formed before the staircase region is formed. In some embodiments, the dummy channel structures can be formed in the core region. Accordingly, the dummy channel structures can pass through the BSG, the dummy BSGs, the plurality of word lines, the dummy TSGs, the TSG and the plurality of insulating layers to extend into the substrate. In some embodiments, the dummy channel structures can be formed with the channel structure together and have a similar structure to the channel structure. For example, the dummy structure can also include a barrier layer, a trapping layer, a tunneling layer, and a channel layer.

[0106] FIG. 10B is top down view to illustrate the formation of the plurality of dummy channel structures. As shown in FIG. 10B, the plurality of dummy channel structures can be formed in the two staircase regions 100A and 100C, and also core region 100B (Especially, at the transition zones of core to staircase regions).

[0107] FIG. 11A is a cross-sectional view obtained in the Z-direction (height direction) of the substrate to illustrate the formation of one or more common source regions. In order to form the channel structures, one or more common source openings can be formed firstly. The common source openings can be formed through a photolithography process to form a patterned mask and a subsequent etching process to transfer the patterns of the mask. The formed common source openings pass through

the TSG, the dummy TSGs, the word lines, the dummy BSGs, and the BSG, and further extend into the HVPW 14. Each of the common source openings can have side portions and a bottom portion that extend into the HVPW. The common source openings can further extend along the X-direction (Length direction) of the substrate, and are parallel disposed with the first and second trenches.

[0108] FIG. 11B shows an exemplary embodiment of the formation of the common source openings. As shown in FIG. 11B, two common source openings 52b' and 52c' are formed at two boundaries of the substrate with a continuous configuration. The common source regions 52a and 52c can be subsequently formed within the common source openings 52b' and 52c' respectively. A common source opening 52a' is formed at a middle position of the substrate. The common source opening 52a' can include two or more sub-openings based on the formed pattern of mask. For example, two sub-openings 52a-1' and 52a-2' are included in FIG. 11B. A space between the two sub-openings 52a-1' and 52a-2' forms an H-Cut, such as the H-Cut 72 in FIG. 11B. Common source regions 52a-1 and 52a-2 can be formed within the two sub-openings 52a-1' and 52a-2' respectively.

[0109] After the common source openings are formed, subsequent manufacturing steps to complete the formation of the common source regions can be different between a gate first manufacturing flow and a gate last manufacturing flow. In the gate first manufacturing flow, an ion implantation can be subsequently applied to form a dope region, such as the doped region 54, at the bottom portion of each of the common source openings. A dielectric spacer, such as the dielectric spacer 68, can be formed along the side portions of the common source openings and over the doped regions. An

anisotropic plasm etching can be implemented to remove bottom portion of the dielectric spacer formed over the doped regions to expose the doped regions. A conductive layer, such as the conductive layer 70, can be deposited along the dielectric spacer and fill the common source openings. The conductive layer can be recessed afterward by an etching process, and a top contact, such as the top contact 64, can be formed along the dielectric spacer and over the conductive layer. When the top contact is formed, formation of a common source region is completed and the complete common source region 52 can be illustrated in FIG. 11A.

[0110] However, in the gate last manufacturing flow, when the common source openings are formed, the BSG, dummy BSGs, word lines, dummy TSGs, and TSG are subsequently removed to form a plurality of vacancies by a wet etching chemical that is introduced through the common source openings. An ion implantation can be thereafter applied to form the dope region (e.g., 54) at the bottom portion of each of the common source openings. Following the implantation step, the BSG, dummy BSGs, word lines, dummy TSGs, and TSG are re-formed by filling the vacancies with a high-K layer plus metal layers through the common source openings. Next, a dielectric spacer, such as the dielectric spacer 68, can be formed along the side portions of the common source openings and over the doped regions. A followed anisotropic plasm etching can be implemented to remove bottom portion of the dielectric spacer formed over the doped regions to expose the doped regions. A conductive layer, such as the conductive layer 70, can be deposited along the dielectric spacer and fill the common source openings. The conductive layer can be recessed afterward by an etching process, and a top contact, such as the top contact 64, can be formed along the dielectric spacer and over

the conductive layer. When the top contact is formed, formation of the common source regions is completed and the complete common source regions can be illustrated in FIG. 11A.

[0111] After the formation of the common source regions, a final 3D-NAND memory device 100 is formed which is identical to the memory device 100 illustrated in FIG. 1A.

[0112] FIG. 11C is top down view to illustrate the formation of one or more common source regions. As shown in FIG. 11C, the memory device 100 can have three common source regions 52a-52c. The common source regions 52a-52c are formed along the X-direction (length direction) of the substrate 10 and are disposed at two boundaries and a middle position of the memory device 100. The common source regions 52b and 52C are disposed at two boundaries of the memory device 100 with a continuous configuration. The common source region 52a is disposed at a middle position of the memory device 100. The common source region (CSR) 52a is separated by the H-cut 72 into two sub-CSRs 52a-1 and 52a-2. The first trenches 26 and 28, and the second trenches 56 and 58 are aligned with each other at the Y direction (width direction) of the substrate 10. The first trenches and the second trenches are disposed between two adjacent common source regions.

[0113] FIG. 11D is a cross-sectional view obtained in the X-direction (length direction) of the substrate to illustrate the final structure of the memory device 100. As shown in FIG. 11D, the first trenches, the second trenches and the common source regions cannot be observed from the cross-sectional view that is obtained in the X-direction (length direction) of the substrate.

[0114] FIG. 12 is a flowchart of a process 1200 for manufacturing a 3D-NAND memory device 100 in accordance with some embodiments. The process 1200 begins at step 1204 where one or more BSGs and one or more dummy BSGs are formed sequentially over a substrate. In addition, a plurality of first insulating layers are formed between the substrate, the BSGs and the dummy BSGs. The substrate can include a plurality of doped regions to reduce the resistance between the substrate and subsequently formed contact structures. The substrate, BSGs and dummy BSGs are spaced apart from each other by the first insulating layers.

[0115] In step 1206 of the process 1200, one or more first trenches are formed in the BSGs and dummy BSGs. The first trenches pass through the BSGs, dummy BSGs, and the first insulating layers, and extend into the substrate. The first trenches further extend along a X-direction (length direction) of the substrate. The first trenches separate the BSGs, the dummy BSGs into a plurality of sub-BSGs, and sub-dummy BSGs. In some embodiments, steps 1204 and 1206 can be performed as illustrated with reference to FIGS. 5A-5C.

[0116] The process 1200 then proceeds to step 1208 where a plurality of word lines, one or more dummy TSGs, and one or more TSGs are stacked over the dummy BSGs sequentially. In addition, a plurality of second insulating layers are formed over the dummy BSGs and disposed between the dummy BSGs, the word lines, the dummy TSGs, and TSGs. In some embodiments, step 1208 can be performed as illustrated with reference to FIG. 6.

[0117] In step 1210, one or more staircase regions can be formed. The staircase regions are configured to provide spaces to form dummy channel structure as well as

word line contacts (not shown). The formation of the staircase regions can be implemented by alternatively repeating a mask patterning process and a plasma etching process. The formed staircase regions are positioned at two sides of the substrate and a core region is positioned in the middle. In some embodiments, step 1208 can be performed as illustrated with reference to FIGS. 7A-7F.

[0118] The process 1200 proceeds to step 1212 where one or more second trenches are formed in the dummy TSGs and the TSGs. The second trenches extend along the length direction of the substrate. The second trenches further pass through the dummy TSG, the TSGs and a portion of the second insulating layers therebetween. The first trenches and the second trenches are aligned with each other in a width direction of the substrate and are spaced apart by the plurality of word line layers. The TSGs are separated by the second trenches into a group of sub-TSGs, and the TSGs are separated by the second trenches into a group of sub-dummy TSGs. In some embodiments, step 1212 can be performed as illustrated with reference to FIGS. 8A-8C.

[0119] In step 1214 of the process 1200, a plurality of channel structures can be formed in the core region. The formation of the channel structures can be performed as illustrated with reference to FIGS. 9A-9B. Next, a plurality of dummy channel structures can be formed in the staircase regions. The formation of the dummy channel structures can be performed as illustrated with reference to FIGS. 10A-10B.

[0120] It should be understood that the channel structures can also be formed before the staircase region is formed. In some embodiments, the dummy channel structures can be formed in the core region. In some embodiments, the dummy channel structures can be formed with the channel structure together and have a similar structure to the

channel structure. For example, the dummy structure can also include a barrier layer, a trapping layer, a tunneling layer, and a channel layer.

[0121] Still in step 1214, one or more common source regions can be formed after the formation of the dummy channel structures. The common source regions extend through the BSGs, the dummy BSGs, the word lines, the dummy TSGs, the TSGs, and the first and second insulating layers. Each of the common source regions is electrically coupled with the substrate via a respective doped region. The common source regions, the first trenches and the second trenches further extend parallel to each other along the length direction of the substrate. In some embodiments, the formation of the common source regions further includes removing the BSGs, the dummy BSGs, the word lines, the dummy TSGs, and the TSGs, and re-forming the BSGs, the dummy BSGs, the word lines, the dummy TSGs, and the TSGs with a high-K layer and metal layers. In some embodiments, the formation of the common source regions can be performed as illustrated with reference to FIGS. 11A-11D.

[0122] It should be noted that additional steps can be provided before, during, and after the process 1200, and some of the steps described can be replaced, eliminated, or performed in different order for additional embodiments of the process 1200. In subsequent process steps, various additional interconnect structures (e.g., metallization layers having conductive lines and/or vias) may be formed over the 3D-NAND memory device 100. Such interconnect structures electrically connect the 3D-NAND memory device 100 with other contact structures and/or active devices to form functional circuits. Additional device features such as passivation layers, input/output structures, and the like may also be formed.

[0123] The various embodiments described herein offer several advantages over related memory devices. For example, in the related memory devices, a plurality of memory cell blocks or memory cell arrays can be included. Each of the blocks can include a plurality of vertical NAND memory cell strings. In the related memory device, the vertical NAND memory cell strings in a same block can have a common/shared bottom select gate (BSG). The shared BSG accordingly controls all the bottom select transistors (BSTs) of the vertical NAND memory cell strings in that block simultaneously during operating the related 3D-NAND memory device, such as erasing the related 3D-NAND memory device. As the related 3D-NAND memory device migrates to higher capacity with an increasing block size, the shared BSG can induce longer erasing time, longer data transfer time, and lower storage efficiency.

[0124] In the disclosed memory device, each of the blocks is separated into a plurality of sub-blocks by dividing the shared BSG into a plurality of sub-BSGs through one or more first trenches. Each of the sub-blocks has a respective sub-BSG, and each of the sub-blocks can be operated individually through controlling the respective sub-BSG. By introducing such a divided BSG structure, the disclosed 3D-NAND memory device can effectively reduce parasitic capacitance and coupling effects between the BSG and adjacent dielectric layers, and significantly improve V_t performance of the bottom select transistors (BSTs). In addition, the erasing time and data transfer time could be reduced significantly, and data storage efficiency can be improved as well.

[0125] In the disclosed memory device, the each of sub-blocks can further have a respective sub-top select gate (sub-TSG) by dividing a shared TSG into a plurality of sub-TSGs through one or more second trenches. Each of the sub-TSGs can control a

respective sub-block during a reading/programming operation. In some embodiments, the first and second trenches can be formed via a same reticle set so that a manufacturing cost can be reduced.

[0126] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A memory device, comprising:

a stack of alternating word line layers and insulating layers over a substrate, the stack including an array region and a first staircase region that are positioned adjacent to each other and arranged in a length direction of the substrate, the word line layers including a bottom select gate (BSG) over the substrate;

first dielectric trenches formed in the BSG of the word line layers and extending in the length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and

a first common source region (CSR) formed over the substrate and extending in the length direction of the substrate, the first CSR further extending through the word line layers, and the insulating layers in a height direction of the substrate, wherein the first CSR is arranged between two adjacent first dielectric trenches of the first dielectric trenches.

2. The memory device of claim 1, wherein the word line layers further include a top select gate (TSG) positioned over the substrate and the BSG.

3. The memory device of claim 2, further comprising:

second dielectric trenches formed in the TSG of the word line layers and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.

4. The memory device of claim 1, further comprising a second staircase region.

5. The memory device of claim 4, wherein the array region is positioned between the first staircase region and the second staircase region in the length direction of the substrate.

6. The memory device of claim 5, wherein:

the memory device further includes a second CSR and a third CSR that are formed over the substrate, extend in the length direction of the substrate, and further extend through the word line layers, and the insulating layers in the height direction of the substrate,

the second CSR, the first CSR, and the third CSR are arranged sequentially in a width direction of the substrate so that the two adjacent first dielectric trenches of the first dielectric trenches are arranged between the second CSR and the third CSR,

the second CSR, the first CSR, and the third CSR extend in parallel to each other in the length direction of the substrate, and

the second CSR, the first CSR, and the third CSR extend through the first staircase region, the array region, and the second staircase region sequentially in the length direction of the substrate.

7. The memory device of claim 1, wherein the first CSR has a discontinuous profile that includes a first portion and a second portion being aligned in the length direction of the substrate.

8. The memory device of claim 6, further comprising:

a plurality of channel structures that extend through the word line layers and the insulating layers in the height direction of the substrate, positioned in the array region, and arranged between the second CSR and the third CSR.

9. The memory device of claim 6, further comprising:

a plurality of dummy channel structures that extend through the word line layers and the insulating layers in the height direction of the substrate, positioned in the first staircase region and the second staircase region, and arranged between the second CSR and the third CSR.

10. The memory device of claim 3, wherein the first CSR is arranged between two adjacent second dielectric trenches of the second dielectric trenches.

11. The memory device of claim 2, wherein the TSG is an uppermost word line layer of the word line layers.

12. The memory device of claim 1, wherein the BSG is a lowermost word line layer of the word line layers.

13. The memory device of claim 5, wherein the first dielectric trenches extend through the first staircase region, the array region, and the second staircase region in the length direction of the substrate.

14. The memory device of claim 3, wherein the second dielectric trenches extend through the array region in the length direction of the substrate.

ABSTRACT

A memory device includes a stack of alternating word line layers and insulating layers over a substrate. The word line layers includes a bottom select gate (BSG) positioned over the substrate. The memory device includes first dielectric trenches that are formed in the BSG of the word line layers and extend in the length direction of the substrate to separate the BSG into a plurality of sub-BSGs. The memory device also includes a first common source region (CSR) that is formed over the substrate and extends in the length direction of the substrate. The first CRS further extends through the word line layers and the insulating layers in a height direction of the substrate, where the first CSR is arranged between two adjacent first dielectric trenches of the first dielectric trenches.

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Document Date: 01/21/2021

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
17/154,054	01/21/2021	2827	1820	534753US	14	1

CONFIRMATION NO. 6569

22850

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FILING RECEIPT



0000000123080639

Date Mailed: 02/03/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 22850

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Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/154,054**

Projected Publication Date: 05/13/2021

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Title

NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 17/154,054	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	14	minus 20 = *				x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
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PUBLICATION NOTICE



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The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569
22850	7590	06/24/2021		
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER AUDUONG, GENE NGHIA	
			ART UNIT	PAPER NUMBER
			2825	
			NOTIFICATION DATE	DELIVERY MODE
			06/24/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OBLONPAT@OBLON.COM
iahmadi@oblon.com
patentdocket@oblon.com

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 1/21/2021 is being considered by the examiner.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

5. Claims 1-14 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-11 of U.S. Patent No. 10, 650,623. Although the claims at issue are not identical, they are not patentably distinct from each other because they are claiming the similar scope of the invention, claiming a memory device, comprising:

a stack of alternating word line layers and insulating layers over a substrate, the stack including an array region and a first staircase region that are positioned adjacent to each other and arranged in a length direction of the substrate, the word line layers including a bottom select gate (BSG) over the substrate;

first dielectric trenches formed in the BSG of the word line layers and extending in the length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and a first common source region (CSR) formed over the substrate and extending in the length direction of the substrate, the first CSR further extending through the word line layers, and the insulating layers in a height direction of the substrate, wherein the first CSR is arranged between two adjacent first dielectric trenches of the first dielectric trenches.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to GENE N AUDUONG whose telephone number is (571)272-1773. The examiner can normally be reached on M-F 8:30 a.m. - 4:30 p.m. EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander George Sofocleous can be reached on (571) 272-0635. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to

the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GENE N AUDUONG/
Primary Examiner, Art Unit 2825

<i>Notice of References Cited</i>	Application/Control No. 17/154,054		Applicant(s)/Patent Under Reexamination SONG et al.	
	Examiner GENE N AUDUONG		Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9299718-B2	03-2016	Park; Jintaek	H01L27/1157	1/1
*	B	US-10930661-B2	02-2021	Chen; Jun	H01L27/11582	1/1
*	C	US-10950623-B2	03-2021	Song; Yali	H01L27/1157	1/1
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner GENE N AUDUONG	Art Unit 2825

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483, G11C16/14, H01L23/528, H01L27/11565, H01L27/1157, H01L27/11556, H01L27/11551	06/15/2021	GA

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
East search, Prior art search, Inventor name search	06/15/2021	GA

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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SHEET 1 OF 2

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 534753US		SERIAL NO. New Application	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE Herewith		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2010/0320528 A1	12-23-2010	JEONG, J. et al.			
	AB	2018/0337195 A1	11/22/2018	JAYANTI, S., et al.			
	AC	10,134,747 B2	11/20/2018	LEE, N.J.			
	AD	10,141,372 B2	11-27-2018	PARK, J. et al. (corresponds to US 2019/0081105 A1)			
	AE	2016/0233270 A1	08-11-2016	TAKAKI, S. et al.			
	AF						
	AG						
	AH						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AI	103226973 A	07-31-2013	China			X
	AJ	103680611 A	03-26-2014	China			X
	AK	103680618 A	03-26-2014	China			X
	AL	201834218 A	09/16/2018	Taiwan (with English abstract)			X
	AM	201842601 A	12/01/2018	Taiwan (with English abstract)			X
	AN	201834217 A	09/16/2018	Taiwan (with English abstract)			X
	AO	108831886 A	11/16/2018	China (with English abstract)			X
	AP	108933139 A	12/04/2018	China (with English abstract)			X
	AQ	108933141 A	12/04/2018	China (with English abstract)			X
	AR	2018-163970 A	10/18/2018	Japan (with English abstract)			X
	AS	101118907 A	02-06-2008	China			X
	AT	101315936 A	12-03-2008	China			X
	AU	106601751 A	04-26-2017	China			X
	AV	108431961 A	08-21-2018	China (with English abstract)			X
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Combined Chinese Office Action and Search Report issued on Jul. 17, 2019, in Patent Application No. 201880002892.5, citing documents AA and AI-AK therein, 7 pages (with English Translation of Category of Cited Documents)					
	AX	International Search Report and Written Opinion of the International Search Authority issued on Sep. 18, 2019, in PCT/CN2018/119908, citing documents AD-AE and AS-AU therein, 9 pages					
	AY	Combined Chinese Office Action and Search Report issued on October 10, 2020 in Patent Application No. 202010103862.2 (with English translation of Categories of Cited Documents), citing documents AV therein, 7 pages					
	AZ					☒ Additional References sheet(s) attached	
Examiner	/GENE N AUDUONG/				Date considered	06/19/2021	
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.N.A/

Micron Ex. 1015, p. 112
Micron v. YMTc
IPR2024-00794

SHEET 2 OF 2

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 534753US		SERIAL NO. New Application	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	US-20200335514-A1	10-2020	XU; Qiang			
	AB	US-20200227555-A1	07-2020	Sun; Jian Hua			
	AC	US-20200185411-A1	06-2020	Herner; Scott Brad			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW						
	AX						
	AY						
	AZ					☐ Additional References sheet(s) attached	
Examiner	/GENE N AUDUONG/				Date considered	06/19/2021	
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.N.A/

Micron Ex. 1015, p. 113
Micron v. YMTC
IPR2024-00794

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17	("20100320528" "20180337195" "10134747" "10141372" "20160233270").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:34
L2	58,706	(G11C16/0483 or G11C16/14 or H01L23/528 or H01L27/11565 or H01L27/1157 or H01L27/11556 or H01L27/11551).cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:40
L3	1,438	cell same3 stack\$3 same3 substrate same3 bottom same3 top same3 select\$3 same3 common same3 source same3 region same3 trench same3 dielectric	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:47
L4	673	2 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:50
L5	0	1 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:50
L6	8	1 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:51
L7	270	4 and (common near3 source near3 region)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:52
L8	243	7 and extend\$3 and arrang\$3 and gate	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:53
L9	87	8 and staircase	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:54
L10	47	9 and length	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:54

L11	9	10 and @ad<="20181207"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:55
L12	26	9 and @ad<="20181207"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/06/19 17:56

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L13	5	(cell and stack\$3 and substrate and bottom and top and select\$3 and common and source and region and trench and dielectric and arrang\$3 and gate).clm.	US-PGPUB; USPAT	OR	ON	2021/06/19 17:57

6/19/2021 6:18:43 PM

C:\Users\gauduong\Documents\EAST\Workspaces\From 5-2021.wsp

DOCKET NO: 534753US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :
YALI SONG, ET AL. : EXAMINER: AUDUONG, GENE NGHIA
SERIAL NO: 17/154,054 :
FILED: JANUARY 21, 2021 : GROUP ART UNIT: 2825
FOR: NOVEL 3D NAND MEMORY :
DEVICE AND METHOD OF FORMING
THE SAME

AMENDMENT UNDER 37 C.F.R. § 1.111

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

In response to the Office Action dated June 24, 2021, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

IN THE SPECIFICATION

Please amend the Title on page 1 as follows:

NOVEL 3D NAND MEMORY DEVICE ~~AND METHOD OF FORMING~~
~~THE SAME~~ WITH SELECT GATE CUT

REMARKS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1-14 are pending in the present application. No claims are amended or added in this response. No new matter is introduced.

In the Office Action, the title of the invention was objected to as not descriptive; and Claims 1-14 were rejected on the ground of non-statutory double patenting as being unpatentable over Claims 1-11 of U.S. Patent No. 10,650,623.

Regarding the objection to the title, the title has been amended to read “NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT”. Accordingly, the objection to the title is believed to have been overcome.

In response to the non-statutory double patenting rejections of Claims 1-14, submitted herewith is a Terminal Disclaimer. Applicant notes that the “filing of a Terminal Disclaimer simply serves the statutory function of removing the rejection of double patenting, and raises neither a presumption nor estoppel on the merits of the rejection.” Quad Environmental Technologies Corp. v. Union Sanitary District, 946 F2d 870, 20 USPQ 2d 1392 (Fed. Cir. 1991). Therefore, Applicant’s filing of the attached disclaimer is provided solely to facilitate a timely resolution to the prosecution of this application, and should not be interpreted as an admission as to the merits of the obviated rejection. Accordingly, it is respectfully requested that the rejections of Claims 1-14 on the ground of non-statutory double patenting be withdrawn.

For the reasons discussed above, no further issues are believed to be outstanding in the present application and the present application is believed to be in condition for formal allowance. Therefore, a Notice of Allowance for Claims 1-14 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the below-listed telephone number.

Respectfully Submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

/Johnny Ma/

Johnny Ma
Attorney of Record
Registration No. 59,976

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 07/09)

Electronic Acknowledgement Receipt	
EFS ID:	43697990
Application Number:	17154054
International Application Number:	
Confirmation Number:	6569
Title of Invention:	NOVEL 3D NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME
First Named Inventor/Applicant Name:	Yali SONG
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Nozomi Berger
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	534753US
Receipt Date:	07-SEP-2021
Filing Date:	21-JAN-2021
Time Stamp:	15:26:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		534753US.pdf	167442	yes	5
			4d262fd5d1665aff7a5d96a501d365d39185d7a2		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Amendment/Req. Reconsideration-After Non-Final Reject	2	2
	Specification	3	3
	Applicant Arguments/Remarks Made in an Amendment	4	5
Warnings:			
Information:			
Total Files Size (in bytes):		167442	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 17/154,054
Applicants: Yali SONG, et al.
Filing Date: January 21, 2021
For: NOVEL 3D NAND MEMORY DEVICE AND METHOD OF
FORMING THE SAME
Group Art Unit: 2825
Examiner: AUDUONG, GENE NGHIA

Commissioner:

Attached hereto for filing are the following papers:

AMENDMENT

Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **\$0.00** to cover any required fees. In the event any variance exists between the submitted amount and the U.S. Patent and Trademark Office fees for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. **15-0030**. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

/Johnny Ma/

Johnny Ma

Registration No. 59,976

Customer Number

22850

(703) 413-3000 (phone)
(703) 413-2220 (fax)
(OMMN 02/12)

OBLON, McCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET ■ ALEXANDRIA, VIRGINIA 22314 ■ U.S.A.
TELEPHONE: 703-413-3000 ■ FACSIMILE: 703-413-2220 ■ WWW.OBLON.COM



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569
22850	7590	01/05/2022		
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER BERMUDEZ LOZADA, ALFREDO	
			ART UNIT	PAPER NUMBER
			2825	
			NOTIFICATION DATE	DELIVERY MODE
			01/05/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OBLONPAT@OBLON.COM
iahmadi@oblon.com
patentdocket@oblon.com

DETAILED ACTION

Notice of AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This action is responsive to the following communications: the Amendment filed September 7, 2021.

Claims 1-14 are pending. Claim 1 is independent.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be

commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-5 and 11-14 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-2 and 4 of U.S. Patent No.

10,950,623. Although the claims at issue are not identical, they are not patentably distinct from each other because: application claims 1, 4-5 and 12 are anticipated by 10,950,623 claim 1. Claims 2-3 and 11 are anticipated by 10,950,623 claim 2. Claims 13-14 are anticipated by 10,950,623 claim 4.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any

correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claims 1-5 and 10-12 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Shibata et al. (U.S. 2019/0122734; hereinafter “Shibata”) as supported by Fukuzumi et al. (“Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory”).

Regarding independent claim 1, Shibata discloses a memory device (**Fig. 3**), comprising:

a stack of alternating word line layers (**Fig. 3: 70**) and insulating layers (**Fig. 3: 72**) over a substrate (**Fig. 3: 10**), the stack including an array region and a first staircase region (**see page 2, par. 0055, see also Fukuzumi et al. Fig. 1: Toshiba’s BiCS shows the 3D view, which demonstrates 3D NAND strings have a staircase structure for their “alternating word line and insulating” layers because there needs to be via connections to upper metal lines that connect the NAND strings SSL, WL, and GSL to the row/block decoder**) that are positioned adjacent to each other and arranged in a length direction of the substrate (**Fig. 3: 10**), the word line layers including a bottom select gate (BSG) over the substrate (**Fig. 16: SGSs**);

first dielectric trenches formed in the BSG of the word line layers and extending in the length direction of the substrate to separate the BSG into a plurality of sub-BSGs **(Fig. 3: elements 60 separate the first 70s lines over the substrate 10 where the SGS are located)**; and

a first common source region (CSR) **(Fig. 3: CL)** formed over the substrate **(Fig. 3: 10)** and extending in the length direction of the substrate **(Fig. 3: 10)**, the first CSR further extending through the word line layers **(Fig. 3: 70)**, and the insulating layers **(Fig. 3: 72)** in a height direction of the substrate **(Fig. 3: 10)**, wherein the first CSR is arranged between two adjacent first dielectric trenches of the first dielectric trenches **(Fig. 3: CL is between 60s)**.

Regarding claim 2, Shibata discloses wherein the word line layers **(Fig. 3: 70)** further include a top select gate (TSG) **(Fig. 3: SGDs)** positioned over the substrate **(Fig. 3: 10)** and the BSG **(Fig. 16: SGSs)**.

Regarding claim 3, Shibata discloses second dielectric trenches **(Fig. 3: 62a and 62b)** formed in the TSG of the word line layers **(Fig. 3: 70)** and extending in the length direction of the substrate **(Fig. 3: 10)** to separate the TSG into a plurality of sub-TSGs **(see page 3, par. 0081)**.

Regarding claim 4, Shibata discloses a second staircase region **(Fig. 2 is a portion of a memory device with staircase regions, as supported by Fukuzumi et al. Fig. 1: Toshiba's BiCS shows the 3D view, which demonstrates 3D NAND strings have a staircase structure for their "alternating word line and insulating" layers because there needs to be via connections to upper metal lines that connect the NAND strings SSL, WL, and GSL to the row/block decoder)**.

Regarding claim 5, Shibata discloses wherein the array region is positioned between the first staircase region and the second staircase region in the length direction of the substrate (**Fig. 2 is a portion of a memory device with staircase regions and an array region, as supported by Fukuzumi et al. Fig. 1: Toshiba's BiCS shows the 3D view, which demonstrates 3D NAND strings have a staircase structure for their "alternating word line and insulating" layers because there needs to be via connections to upper metal lines that connect the NAND strings SSL, WL, and GSL to the row/block decoder**).

Regarding claim 10, Shibata discloses wherein the first CSR (**Fig. 3: CL**) is arranged between two adjacent second dielectric trenches of the second dielectric trenches (**Fig. 3: 62a and 62b**).

Regarding claim 11, Shibata discloses the TSG is an uppermost word line layer of the word line layers (**Fig. 3: SGDs are located at the top lines of 70s**).

Regarding claim 12, Shibata discloses wherein the BSG is a lowermost word line layer of the word line layers (**Fig. 16: SGSs are located at the lowest lines 70s**).

Response to Arguments

Applicant's arguments with respect to claims 1-14 have been considered but are moot because the new ground of rejection does not rely on any reference applied in the prior rejection of record for any teaching or matter specifically challenged in the argument.

Furthermore, Applicant asserts that a Terminal Disclaimer was submitted to overcome the current Non-Statutory Double Patenting Rejection, see Applicant's Remarks page 3. However, the Terminal Disclaimer does not appear on record.

Allowable Subject Matter

Claims 6-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 6, there is no teaching or suggestion in the prior art of record to provide the recited memory device further includes a second CSR and a third CSR that are formed over the substrate, extend in the length direction of the substrate, and further extend through the word line layer, and the insulating layers in the height direction of the substrate, the second CSR, the first CSR, and the third CSR are arranged sequentially in a width direction of the substrate so that the two adjacent first dielectric trenches of the first dielectric trenches are arranged between the second CSR and the third CSR, the second CSR, the first CSR, and the third CSR extend in parallel to each other in the length direction of the substrate, and the second CSR, the first CSR, and the third CSR extend through the first staircase region, the array region, and the second staircase region sequentially in the length direction of the substrate.

Regarding claim 7, there is no teaching or suggestion in the prior art of record to provide the recited first CSR has a discontinuous profile that includes a first portion and a second portion being aligned in the length direction of the substrate.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Feeley et al. (U.S. 2014/0036590) and Ishikawa et al. (U.S. 2010/0323505).

Feeley et al. teach a 3D NAND memory device with each of the SGDs of the plurality of string may be separated from one another.

Ishikawa et al. teach a stacked structure comprising insulating layers between each adjacent pair of upper select gates, and it is also possible to divide the lower select gate into a plurality like the upper select gates.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALFREDO BERMUDEZ LOZADA whose telephone number is (571)272-0877. The examiner can normally be reached 7:00AM-3:30PM EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander G Sofocleous can be reached on 571-272-0635. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For

Application/Control Number: 17/154,054
Art Unit: 2825

Page 9

additional questions, contact the Electronic Business Center (EBC) at 866-217-9197
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Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alfredo Bermudez Lozada/
Primary Examiner, Art Unit 2825

Notice of References Cited	Application/Control No. 17/154,054		Applicant(s)/Patent Under Reexamination SONG et al.	
	Examiner ALFREDO BERMUDEZ LOZADA		Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20190122734-A1	04-2019	Shibata; Noboru	G11C16/0483	1/1
*	B	US-20140036590-A1	02-2014	Feeley; Peter Sean	G11C16/16	365/185.11
*	C	US-20100323505-A1	12-2010	ISHIKAWA; Masao	H01L21/31144	438/492
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Fukuzumi et al., Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory (Year: 2007)
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483, G11C16/14, H01L23/528, H01L27/11565, H01L27/1157, H01L27/11556, H01L27/11551	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	185.17	12/30/2021	ABL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

Search Notes		
Search Notes	Date	Examiner
East search, Prior art search, Inventor name search	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL
PE2E Search all databases	12/30/2021	ABL
IP.com	12/30/2021	ABL
Consulted with Alex Sofocleous (SPE)	12/30/2021	ABL
Inventor and Assignee searched	12/30/2021	ABL

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
Interference search		09/30/2021	GA

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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BIB DATA SHEET

CONFIRMATION NO. 6569

SERIAL NUMBER 17/154,054	FILING or 371(c) DATE 01/21/2021 RULE	CLASS 365	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. 534753US		
APPLICANTS Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA INVENTORS Yali SONG, Wuhan, CHINA; Li Hong XIAO, Wuhan, CHINA; Ming WANG, Wuhan, CHINA; ** CONTINUING DATA ***** This application is a CON of 16/365,725 03/27/2019 PAT 10950623 which is a CON of PCT/CN2018/119908 12/07/2018 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/01/2021						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/GENE N. AUDUONG/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CHINA	SHEETS DRAWINGS 20	TOTAL CLAIMS 14	INDEPENDENT CLAIMS 1
ADDRESS OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314 UNITED STATES						
TITLE NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT						
FILING FEE RECEIVED 1820	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2	"20210143179"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2021/12/28 01:58 PM
L2	8	("10134747" OR "10141372" OR "20100320528" OR "20160233270" OR "20180337195" OR "20200185411" OR "20200227555" OR "20200335514").pn.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 05:40 AM
L3	3	"10650623"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:00 AM
L4	11	bsg AND csr AND tsg	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:04 AM
L5	17794	(3d OR three-dimension\$2 OR (three dimension\$2) OR 3-dimension\$2 OR vertical OR stack) near2 nand	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:35 AM
L6	44	staircase AND ((bottom select gate) OR bsg) AND ((top select gate) OR tsg) AND ((common source) OR csr)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L7	44	6 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L8	235	trench WITH (divid\$3 OR separat\$3 OR cut) WITH (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L9	105	8 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L10	13760	5 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:33 AM
L11	1032	5 AND (stair OR step) AND ((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:34 AM
L12	129	((dielectric OR insulat\$3) near2 trench) WITH (select (gate OR	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:36 AM

L13	118	transistor)) 12 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:37 AM
L14	3796	365/185.17.ccls.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:31 AM
L15	56814	((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:32 AM
L16	57	15 AND 14	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:33 AM
L17	1	15 AND 14 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:36 AM
L18	16647	g11c16/0483.cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:42 AM
L19	345	18 AND 15	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L20	25	18 AND 15 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L21	17953	(h01I27/11582,11565,1 1568,11567,1157).cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:56 AM
L22	2190	15 AND 21	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L23	666	15 AND 21 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L24	49	15 AND 21 AND (common NEAR source) AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L25	6	(sub-ssg OR sub-sst OR sub-gst OR sub-gsg OR sub-bsg)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:10 AM
L26	1646	(multiple OR plurality) NEAR select NEAR gate	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:11 AM
L27	448	5 AND 26	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:15 AM
L28	286	5 AND 26 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:27 AM
L29	1	"20210295918"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:11 AM
L30	56	(divid\$3 OR separat\$3 OR cut) near2(plurality OR multiple) near2 (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:35 AM
L31	2	"20140036590"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:51 AM
L32	9	"10950623"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	ADJ	ON	ON	2021/12/30 05:42 AM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L33	790	yangtze.as.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L34	63353	song.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L35	29984	xiao.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L36	252871	wang.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L37	4	33 AND 34 AND 35 AND 36	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L38	9	8 AND 33	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:03 AM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/154,054		Filing Date 01/21/2021		☐ To be Mailed			
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO											
APPLICATION AS FILED - PART I											
		(Column 1)		(Column 2)							
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		x \$100 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		x \$480 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL					
APPLICATION AS AMENDED - PART II											
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	04/15/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0			x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0			x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE		0	
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=			x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=			x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.								LIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".								/TRACEY T BELL/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".											
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DOCKET NO: 534753US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :
YALI SONG, ET AL. : EXAMINER: BERMUDEZ LOZADA,
ALFREDO
SERIAL NO: 17/154,054 :
FILED: JANUARY 21, 2021 : GROUP ART UNIT: 2825
FOR: NOVEL 3D NAND MEMORY :
DEVICE WITH SELECT GATE CUT

AMENDMENT UNDER 37 C.F.R. § 1.111

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

In response to the Office Action dated January 5, 2022, please amend the above-
identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page
2 of this paper.

Remarks begin on page 5 of this paper.

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A memory device, comprising:

a stack of alternating word line layers and insulating layers over a substrate, the stack including an array region and a first staircase region that are positioned adjacent to each other and arranged in a first length direction of the substrate, the word line layers including a bottom select gate (BSG) over the substrate;

first dielectric trenches ~~formed in the BSG of the word line layers and extending in the length direction of the substrate~~ extending in a height direction of the substrate through the BSG to separate the BSG into a plurality of sub-BSGs and partially through the stack; and

a first common source region (CSR) formed over the substrate and extending in [[the]] a second length direction of the substrate, the first CSR further extending through the word line layers [[,]] and the insulating layers in [[a]] the height direction of the substrate, wherein the first CSR is arranged between two adjacent first dielectric trenches of the first dielectric trenches.

2. (Original) The memory device of claim 1, wherein the word line layers further include a top select gate (TSG) positioned over the substrate and the BSG.

3. (Currently Amended) The memory device of claim 2, further comprising:

second dielectric trenches formed in the TSG of the word line layers and extending in the second length direction of the substrate to separate the TSG into a plurality of sub-TSGs.

4. (Original) The memory device of claim 1, further comprising a second staircase region.

5. (Currently Amended) The memory device of claim 4, wherein the array region is positioned between the first staircase region and the second staircase region in the first length direction of the substrate.

6. (Currently Amended) The memory device of claim 5, wherein:

the memory device further includes a second CSR and a third CSR that are formed over the substrate, extend in the second length direction of the substrate, and further extend through the word line layers, and the insulating layers in the height direction of the substrate,

the second CSR, the first CSR, and the third CSR are arranged sequentially in a ~~width~~ the first length direction of the substrate so that the two adjacent first dielectric trenches of the first dielectric trenches are arranged between the second CSR and the third CSR,

the second CSR, the first CSR, and the third CSR extend in parallel to each other in the second length direction of the substrate, and

the second CSR, the first CSR, and the third CSR extend through the first staircase region, the array region, and the second staircase region ~~sequentially~~ respectively in the second length direction of the substrate.

7. (Currently Amended) The memory device of claim 1, wherein the first CSR has a discontinuous profile that includes a first portion and a second portion being aligned in the second length direction of the substrate.

8. (Original) The memory device of claim 6, further comprising:

a plurality of channel structures that extend through the word line layers and the insulating layers in the height direction of the substrate, positioned in the array region, and arranged between the second CSR and the third CSR.

9. (Original) The memory device of claim 6, further comprising:

a plurality of dummy channel structures that extend through the word line layers and the insulating layers in the height direction of the substrate, positioned in the first staircase region and the second staircase region, and arranged between the second CSR and the third CSR.

10. (Original) The memory device of claim 3, wherein the first CSR is arranged between two adjacent second dielectric trenches of the second dielectric trenches.

11. (Original) The memory device of claim 2, wherein the TSG is an uppermost word line layer of the word line layers.

12. (Original) The memory device of claim 1, wherein the BSG is a lowermost word line layer of the word line layers.

13. (Currently Amended) The memory device of claim 5, wherein the first dielectric trenches extend through the first staircase region, the array region, and the second staircase region in the second length direction of the substrate.

14. (Currently Amended) The memory device of claim 3, wherein the second dielectric trenches extend through the array region in the second length direction of the substrate.

REMARKS

Claims 1-14 are pending in this application. By this Amendment, claims 1, 3, 5-7 and 13-14 are amended for clarity. No new matter is added. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

The courtesies extended to Applicant's representative by Examiner Lozada at the interview held on 03/29/2022 are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below, which constitute Applicant's separate record of the substance of the interview.

Applicants appreciate the indication that claims 6-9 contain allowable subject matter. However, for at least the reasons discussed herein, Applicant respectfully asserts that all claims 1-14 are allowable.

The Office Action rejects claims 1-5 and 11-14 on the ground of nonstatutory double patenting as being unpatentable over claims 1-2 and 4 of U.S. Patent No. 10,950,623. In response, Applicant submits herewith a terminal disclaimer to overcome the double patenting rejection. Therefore, Applicant respectfully requests reconsideration and withdraw of the rejections of pending claims on the ground of nonstatutory double patenting.

The Office Action rejects claims 1-5 and 10-12 under 35 U.S.C. §102(a)(2) as being anticipated by Shibata et al. (U.S. Pat. No. 2019/0122734; hereinafter "Shibata") in view Fukuzumi et al. (Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory; hereafter "Fukuzumi"). Applicant respectfully traverses these rejections.

Specifically, Applicant asserts that Shibata or Fukuzumi, either alone or in combination, fail to disclose or suggest (1) first dielectric trenches *extending in a height direction of the substrate* through the BSG to separate the BSG into a plurality of sub-BSGs and *partially through the stack*, and (2) a first common source region (CSR) *extending through*

the word line layers and the insulating layers in the height direction of the substrate, as recited in independent claim 1.

As discussed during the interview, Shibata is directed to a semiconductor device including a separation portion 60 that extends all the way through the stack body 100 in the Z direction (see e.g. Figs. 2 and 3 and [0057]-[0058] of the specification). Therefore, the separation portion 60 divides not only a BSG, but also the word line layers, as well as a top select gate if there is one. In other words, the separation portion 60 divides the stack body 100 into multiple blocks 200 in the Y direction.

Apparently, the Office Action claims that the CL in Shibata teaches the first CSR in the present application. As shown in Figs. 3 and 4 and [0063], [0066]-[0067] of the specification, the CL includes a core film 50 surrounded by a semiconductor body 20 which is further surrounded by a memory film 30 having a tunneling insulating film 31, a charge storage film 32 and a blocking insulating film 33. Note that the semiconductor body 20 functions as a channel. That is, the CL and the semiconductor body 20 may respectively correspond to the channel structure 30 and the channel layer 206 in the present application (see e.g. Figs. 1A and 1C-1 and [0054] and [0061]-[0063] of the specification). Shibata does not teach the first CSR, but instead teaches a horizontal source layer (SL) positioned below the stack body 100 (see e.g. Fig. 3 and [0055]-[0057] and [0061] of the specification).

Accordingly, Shibata does not disclose or suggest a semiconductor device including at least (1) first dielectric trenches extending in a height direction of the substrate through the BSG to separate the BSG into a plurality of sub-BSGs and partially through the stack, and (2) a first CSR extending through the word line layers and the insulating layers in the height direction of the substrate, as recited in independent claim 1. The remaining reference to Fukuzumi is applied in the Office Action for teachings recited in the dependent claims and fails to correct the deficiencies as discussed above.

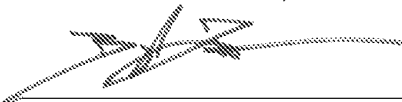
In view of the above, Applicant respectfully submits that the independent claims are allowable. The dependent claims are therefore also allowable by virtue of their dependencies, as well as for the additional features that they recite. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully Submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.



John S. Kern
Attorney of Record
Registration No. 42,719

Bogdan A. Zinchenko
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(OMMN 07/09)

Docket No. 534753US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yali SONG, et al.

SERIAL NO: 17/154,054

GAU: 2825

FILED: January 21, 2021

EXAMINER: BERMUDEZ LOZADA,
ALFREDO

FOR: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

TERMINAL DISCLAIMER

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

Now comes the undersigned, Attorney of Record in the present application, who avers as follows:

YANGTZE MEMORY TECHNOLOGIES CO., LTD. is the owner of the entire right, title and interest in and to the invention claimed and disclosed in the above-captioned patent application by virtue of assignment, said Assignment having been recorded in the U.S. Patent and Trademark Office at reel no. 048707, frame(s) 0673.

YANGTZE MEMORY TECHNOLOGIES CO., LTD. hereby disclaims the terminal part of any patent granted on the above-captioned application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. 154 and 173 as shortened by any terminal disclaimer of U.S. Patent No. 10,950,623, and hereby agrees that any patent so granted on said above-captioned application shall be enforceable only for and during such period that it and Patent No. 10,950,623 are commonly owned. This agreement runs with any patent granted on the above-captioned application and is binding upon the grantee, its successors or assigns.

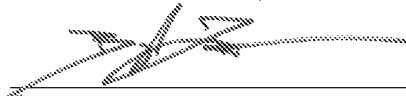
YANGTZE MEMORY TECHNOLOGIES CO., LTD. does not disclaim any terminal part of any patent granted on the above-captioned application that would extend to the full statutory term as defined in 35 U.S.C. 154 and 173 as shortened by any terminal disclaimer of U.S. Patent No. 10,950,623 in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321(a), has all claims canceled by a reexamination certificate, is reissued, or is otherwise terminated prior to the expiration of its statutory term as shortened by any terminal disclaimer, except for the separation of common ownership stated above.

Respectfully Submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

April 15, 2022

Date Signed



John S. Kern

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Bogdan A. Zinchenko
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Electronic Patent Application Fee Transmittal				
Application Number:		17154054		
Filing Date:		21-Jan-2021		
Title of Invention:		NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT		
First Named Inventor/Applicant Name:		Yali SONG		
Filer:		Philippe Jean-Claude Signore/Kristin Newett		
Attorney Docket Number:		534753US		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 1 month with \$0 paid	1251	1	220	220
Miscellaneous:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	170	170
Total in USD (\$)				390

Electronic Acknowledgement Receipt	
EFS ID:	45484822
Application Number:	17154054
International Application Number:	
Confirmation Number:	6569
Title of Invention:	NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT
First Named Inventor/Applicant Name:	Yali SONG
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Kristin Newett
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	534753US
Receipt Date:	15-APR-2022
Filing Date:	21-JAN-2021
Time Stamp:	12:59:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 390
RAM confirmation Number	E20224ED00391861
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		534753USAMENDMENT.pdf	6639789	yes	10
			1c6ffc52ae582d4b48e4640355f4b3481b363412		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Extension of Time		2	2	
	Amendment/Request for Reconsideration-After Non-Final Rejection		3	3	
	Claims		4	6	
	Applicant Arguments/Remarks Made in an Amendment		7	9	
	Terminal Disclaimer Filed		10	10	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	40497	no	2
			1caa7872bf2e6415e9ed07ea3c549e411ca0c188		
Warnings:					
Information:					
Total Files Size (in bytes):			6680286		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No. 534753US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Yali SONG, et al.

SERIAL NO: 17/154,054

ART UNIT: 2825

FILING DATE: January 21, 2021

EXAMINER: BERMUDEZ LOZADA, ALFREDO

FOR: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

FEE TRANSMITTAL

- ☐ No additional fee is required
- ☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- ☐ Track 1 Prioritized Examination

The Fee has been calculated as shown below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	14 - 20 =	0	x \$100 =	\$0.00
INDEPENDENT CLAIMS	1 - 3 =	0	x \$480 =	\$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ \$860 =	\$0.00
☐ LATE FILING OF DECLARATION			+ \$160 =	\$0.00
☐ NON-ELECTRONIC FILING FEE			+ \$400 =	\$0.00
BASIC FEES				\$0.00
TOTAL OF ABOVE CALCULATIONS				\$0.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				\$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ \$140 =	\$0.00
TOTAL				\$0.00

- ☐ Please charge Deposit Account No. **15-0030** in the amount of _____
- ☒ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **\$390.00**.
- ☒ The Director is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**, with the **EXCEPTION** of deficiencies in fees for multiple dependent claims in new applications.
- ☒ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030.

Submitted by: _____

John S. Kern

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Customer Number

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(OMMN 02/12)

Bogdan A. Zinchenko
Registration No.: 57,473

Docket No. 534753US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yali SONG, et al.

SERIAL NO: 17/154,054

GAU: 2825

FILED: January 21, 2021

EXAMINER: BERMUDEZ LOZADA,
ALFREDO

FOR: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

REQUEST FOR EXTENSION OF TIME
UNDER 37 C.F.R. 1.136

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

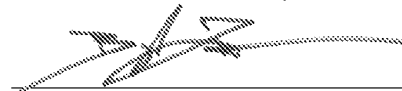
It is hereby requested that a **one** month extension of time be granted to May 5, 2022 for

- ☒ filing a response to the Official Action dated: January 5, 2022
- ☐ responding to the requirements in the Notice of Allowability dated:
- ☐ responding to the Notice to File Missing Parts of Application dated:
- ☐ filing a Notice of Appeal. A timely response to the final rejection, due has been filed.
- ☐ filing an Appeal Brief. A Notice of Appeal was filed on:
- ☐ Applicant claims small entity status. See 37 CFR 1.27.

The required fee of \$220.00 is being made by credit card payment online (if electronically filed), or is attached hereto (if paper filed), and any further charges may be made against the Attorney of Record's Deposit Account No. 15-0030.

Respectfully Submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.



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Customer Number

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(OMMN 07/09)

Bogdan A. Zinchenko
Registration No.: 57,473

Application Number * 17/154,054 *	Application/Control No. 17/154,054	Applicant(s)/Patent under Reexamination SONG et al.	
	Examiner BERMUDEZ LOZADA, ALFREDO	Art Unit 2825	
Document Code - DISQ		Internal Document - DO NOT MAIL	

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed: <u>15 April 2022</u>	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
/JEAN PROCTOR/ Technology Center: <u>OPLC</u> Telephone: <u>(571)272-1040</u> _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

22850 7590 04/26/2022
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
BERMUDEZ LOZADA, ALFREDO	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/26/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569

TITLE OF INVENTION: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	07/26/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22850 7590 04/26/2022
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569

TITLE OF INVENTION: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	07/26/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
BERMUDEZ LOZADA, ALFREDO	2825	365-185170

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. **NOTE:** If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569
22850	7590	04/26/2022	EXAMINER	
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314			BERMUDEZ LOZADA, ALFREDO	
			ART UNIT	PAPER NUMBER
			2825	
DATE MAILED: 04/26/2022				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/154,054	Applicant(s) SONG et al.	
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Amendment of 04/15/2022.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-14 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
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DETAILED ACTION

Notice of AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This action is responsive to the following communications: the Amendment filed April 15, 2022.

Claims 1-14 are pending. Claim 1 is independent.

Allowable Subject Matter

Claims 1-14 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to independent claim 1, there is no teaching or suggestion in the prior art of record to provide the recited first dielectric trenches extending in a height direction of the substrate through the BSG to separate the BSG into a plurality of sub-BSGs and partially through the stack, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALFREDO BERMUDEZ LOZADA whose telephone number is (571)272-0877. The examiner can normally be reached 7:00AM-3:30PM EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander G Sofocleous can be reached on 571-272-0635. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alfredo Bermudez Lozada/
Primary Examiner, Art Unit 2825

<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483, G11C16/14, H01L23/528, H01L27/11565, H01L27/1157, H01L27/11556, H01L27/11551	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	185.17	12/30/2021	ABL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

Search Notes		
Search Notes	Date	Examiner
East search, Prior art search, Inventor name search	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL
PE2E Search all databases	12/30/2021	ABL
IP.com	12/30/2021	ABL
Consulted with Alex Sofocleous (SPE)	12/30/2021	ABL
Inventor and Assignee searched	12/30/2021	ABL
search updated	04/19/2022	ABL

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
Interference search		09/30/2021	GA
G11C	16/14	04/19/2022	ABL
G11C	16/0483	04/19/2022	ABL
G11C	16/04	04/19/2022	ABL
365	185.17	04/19/2022	ABL
H01L	27/11582	04/19/2022	ABL

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.	
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825	

CPC						
Symbol					Type	Version
H01L	/	27	/	11582	F	2013-01-01
G11C	/	16	/	0483	I	2013-01-01
G11C	/	16	/	14	I	2013-01-01
H01L	/	21	/	31116	I	2013-01-01
H01L	/	23	/	528	I	2013-01-01
H01L	/	27	/	11565	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	29	/	0847	I	2013-01-01
H01L	/	29	/	1037	I	2013-01-01
H01L	/	21	/	0276	A	2013-01-01
H01L	/	21	/	31144	A	2013-01-01

CPC Combination Sets					
Symbol				Type	Set
	/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	19 April 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220419A

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.	
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825	

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G11C	/	16	/ 04
NON-CLAIMED			
/	/	/	/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
365	185.17

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	19 April 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220419A

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	4	10												
2	2	6	11												
3	3	14	12												
7	4	12	13												
8	5	5	14												
9	6														
13	7														
10	8														
11	9														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	19 April 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220419A

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2	"20210143179"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2021/12/28 01:58 PM
L2	8	("10134747" OR "10141372" OR "20100320528" OR "20160233270" OR "20180337195" OR "20200185411" OR "20200227555" OR "20200335514").pn.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 05:40 AM
L3	3	"10650623"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:00 AM
L4	11	bsg AND csr AND tsg	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:04 AM
L5	17794	(3d OR three-dimension\$2 OR (three dimension\$2) OR 3-dimension\$2 OR vertical OR stack) near2 nand	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:35 AM
L6	44	staircase AND ((bottom select gate) OR bsg) AND ((top select gate) OR tsg) AND ((common source) OR csr)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L7	44	6 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L8	235	trench WITH (divid\$3 OR separat\$3 OR cut) WITH (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L9	105	8 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L10	13760	5 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:33 AM
L11	1032	5 AND (stair OR step) AND ((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:34 AM
L12	129	((dielectric OR insulat\$3) near2 trench) WITH (select (gate OR	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:36 AM

L13	118	transistor)) 12 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:37 AM
L14	3796	365/185.17.ccls.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:31 AM
L15	56814	((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:32 AM
L16	57	15 AND 14	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:33 AM
L17	1	15 AND 14 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:36 AM
L18	16647	g11c16/0483.cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:42 AM
L19	345	18 AND 15	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L20	25	18 AND 15 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L21	17953	(h01I27/11582,11565,1 1568,11567,1157).cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:56 AM
L22	2190	15 AND 21	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L23	666	15 AND 21 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L24	49	15 AND 21 AND (common NEAR source) AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L25	6	(sub-ssg OR sub-sst OR sub-gst OR sub-gsg OR sub-bsg)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:10 AM
L26	1646	(multiple OR plurality) NEAR select NEAR gate	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:11 AM
L27	448	5 AND 26	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:15 AM
L28	286	5 AND 26 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:27 AM
L29	1	"20210295918"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:11 AM
L30	56	(divid\$3 OR separat\$3 OR cut) near2(plurality OR multiple) near2 (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:35 AM
L31	2	"20140036590"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:51 AM
L32	9	"10950623"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	ADJ	ON	ON	2021/12/30 05:42 AM

L33	790	yangtze.as.	EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L34	63353	song.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L35	29984	xiao.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L36	252871	wang.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L37	4	33 AND 34 AND 35 AND 36	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L38	9	8 AND 33	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:03 AM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	2752	G11C16/04.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N2	17261	G11C16/0483.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N3	3863	G11C16/14.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N4	3796	365/185.17.CCLS.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N5	12813	H01L27/11582.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N6	0	N5 AND N4 AND N3 AND N2 AND N1	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N7	598	N1 AND N2	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N8	39	N1 AND N2 AND N3	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N9	2365	N4 AND (N1 OR N2 OR N3 OR N5)	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N10	2935	N5 AND (N1 OR N2 OR N3 OR N4)	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N11	1277	(bsg).clm.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N12	88549	(crs).clm.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N13	0	N11 AND N12 AND N10	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N14	0	N11 AND N12 AND N9	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM

N15	0	N11 AND N12 AND N8	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:01 PM
N16	0	N11 AND N12 AND N7	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:01 PM



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6569

SERIAL NUMBER 17/154,054	FILING or 371(c) DATE 01/21/2021 RULE	CLASS 365	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. 534753US	
APPLICANTS Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA INVENTORS Yali SONG, Wuhan, CHINA; Li Hong XIAO, Wuhan, CHINA; Ming WANG, Wuhan, CHINA; ** CONTINUING DATA ***** This application is a CON of 16/365,725 03/27/2019 PAT 10950623 which is a CON of PCT/CN2018/119908 12/07/2018 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/01/2021					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /ALFREDO BERMUDEZ LOZADA/ Acknowledged Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY CHINA	SHEETS DRAWINGS 20	TOTAL CLAIMS 14	INDEPENDENT CLAIMS 1
ADDRESS OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314 UNITED STATES					
TITLE NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT					
FILING FEE RECEIVED 1820	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 534753US		SERIAL NO. 17/154,054	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE January 21, 2021		GROUP 2825	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2018/0240527 A1	8/23/2018	ZHANG, et al.			
	AB	2017/0040061 A1	2/9/2017	YEH, et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Extended European Search Report issued April 5, 2022 in European Application No. 18942303.1 (references AA-AB cited herein)					
	AX						
	AY						
	AZ					☐ Additional References sheet(s) attached	
Examiner					Date considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Electronic Patent Application Fee Transmittal				
Application Number:		17154054		
Filing Date:		21-Jan-2021		
Title of Invention:		NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT		
First Named Inventor/Applicant Name:		Yali SONG		
Filer:		Philippe Jean-Claude Signore/Kristin Newett		
Attorney Docket Number:		534753US		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
Total in USD (\$)				260

Electronic Acknowledgement Receipt	
EFS ID:	45642899
Application Number:	17154054
International Application Number:	
Confirmation Number:	6569
Title of Invention:	NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT
First Named Inventor/Applicant Name:	Yali SONG
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Kristin Newett
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	534753US
Receipt Date:	05-MAY-2022
Filing Date:	21-JAN-2021
Time Stamp:	14:15:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 260
RAM confirmation Number	E202255E15272560
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		534753USIDS.pdf	3895927	yes	12
			ab225450c66bc5d9e4f5e1d26aeceaf3b4f4637		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Patent Term Adjustment Statement under 37 CFR 1.704(d) filed with an IDS		1	1	
	Transmittal Letter		2	2	
	Information Disclosure Statement (IDS) Form (SB08)		3	3	
	Non Patent Literature		4	12	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38241	no	2
			540b99f684794aa403947907f71252c90400a8bb		
Warnings:					
Information:					
Total Files Size (in bytes):			3934168		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

**PATENT TERM ADJUSTMENT
STATEMENT UNDER 37 CFR 1.704(d)**

Application Number	17/154,054
Filing Date	January 21, 2021
First Named Inventor	Yali SONG, et al.
Art Unit	2825
Examiner Name	BERMUDEZ LOZADA, ALFREDO
Practitioner Docket No.	534753US

APPLICANT HEREBY STATES THE FOLLOWING (please review 37 CFR 1.704(d) before filing this form):

- ☐ Each item of information contained in the information disclosure statement was first cited in any communication from a patent office in a counterpart foreign or international application or from the Office, and this communication was not received by any individual designated in 37 CFR 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

AND/OR

- ☒ Each item of information contained in the information disclosure statement is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in 37 CFR 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

INSTRUCTIONS:

- **This form will not satisfy the requirement of 37 CFR 1.97(e).** The present statement is filed under 37 CFR 1.704(d) and will not substitute for compliance with any of the requirements of 37 CFR 1.97 and 1.98. For an information disclosure statement to comply with 37 CFR 1.97(c) or (d), the information disclosure statement must be accompanied by a statement under 37 CFR 1.97(e) not with standing any statement filed under 37 CFR 1.704(d).
- The present form (PTO/SB/133) should be filed concurrently with the information disclosure statement to derive benefit under 37 CFR 1.704(d).

Signature /John S. Kern/

Date 5/5/2022

Typed or
printed name John S. Kern

Practitioner
Registration Number 42,719

Note: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below*.

* Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yali SONG, et al.

SERIAL NO: 17/154,054

GAU: 2825

FILED: January 21, 2021

EXAMINER: BERMUDEZ LOZADA,
ALFREDO

FOR: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the reference(s) listed on the attached form PTO-1449 and/or accompanying documents from a corresponding foreign application. Copies of the listed reference(s) are attached, where required, as are either statements of relevancy, English translations of the categories of cited documents for foreign search reports or English translations of foreign Office Actions which provide the statement of relevancy for the foreign language references cited therein, or any readily available partial or full English translations of pertinent portions of any non-English language reference(s).
- ☒ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

/John S. Kern/

John S. Kern

Registration No. 42,719

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 02/12)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569
22850	7590	05/12/2022		
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER BERMUDEZ LOZADA, ALFREDO	
			ART UNIT	PAPER NUMBER
			2825	
			NOTIFICATION DATE	DELIVERY MODE
			05/12/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OBLONPAT@OBLON.COM
iahmadi@oblon.com
patentdocket@oblon.com

Supplemental Notice of Allowability	Application No. 17/154,054	Applicant(s) SONG et al.	
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the IDS of 05/05/2022.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-14 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 05/05/2022. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	--

DETAILED ACTION

Notice of AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This action supplements the Notice of Allowance mailed April 26, 2022 to consider the new Information Disclosure Statement of May 5, 2022.

Claims 1-14 are pending. Claim 1 is independent.

Information Disclosure Statement

Acknowledgment is made of applicant's Information Disclosure Statement (IDS) filed on May 5, 2022. This IDS has been considered.

Allowable Subject Matter

Claims 1-14 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to independent claim 1, there is no teaching or suggestion in the prior art of record to provide the recited first dielectric trenches extending in a height direction of the substrate through the BSG to separate the BSG into a plurality of sub-BSG and partially through the stack, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALFREDO BERMUDEZ LOZADA whose telephone number is (571)272-0877. The examiner can normally be reached 7:00AM-3:30PM EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander G Sofocleous can be reached on 571-272-0635. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alfredo Bermudez Lozada/
Primary Examiner, Art Unit 2825

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

CPC						
Symbol					Type	Version
H01L	/	27	/	11582	F	2013-01-01
G11C	/	16	/	0483	I	2013-01-01
G11C	/	16	/	14	I	2013-01-01
H01L	/	21	/	31116	I	2013-01-01
H01L	/	23	/	528	I	2013-01-01
H01L	/	27	/	11565	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	29	/	0847	I	2013-01-01
H01L	/	29	/	1037	I	2013-01-01
H01L	/	21	/	0276	A	2013-01-01
H01L	/	21	/	31144	A	2013-01-01

CPC Combination Sets					
Symbol				Type	Version
	/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	09 May 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220509

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G11C	/	16	/ 04
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
365	185.17

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	09 May 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220509

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	4	10												
2	2	6	11												
3	3	14	12												
7	4	12	13												
8	5	5	14												
9	6														
13	7														
10	8														
11	9														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	09 May 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220509

<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483, G11C16/14, H01L23/528, H01L27/11565, H01L27/1157, H01L27/11556, H01L27/11551	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	185.17	12/30/2021	ABL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
--	--

Search Notes 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

Search Notes		
Search Notes	Date	Examiner
East search, Prior art search, Inventor name search	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL
PE2E Search all databases	12/30/2021	ABL
IP.com	12/30/2021	ABL
Consulted with Alex Sofocleous (SPE)	12/30/2021	ABL
Inventor and Assignee searched	12/30/2021	ABL
search updated	04/19/2022	ABL
search updated	05/09/2022	ABL
New IDS considered	05/09/2022	ABL

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
Interference search		09/30/2021	GA
G11C	16/14	04/19/2022	ABL
G11C	16/0483	04/19/2022	ABL
G11C	16/04	04/19/2022	ABL
365	185.17	04/19/2022	ABL
H01L	27/11582	04/19/2022	ABL

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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SHEET 1 OF 1

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 534753US		SERIAL NO. 17/154,054	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE January 21, 2021		GROUP 2825	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2018/0240527 A1	8/23/2018	ZHANG, et al.			
	AB	2017/0040061 A1	2/9/2017	YEH, et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Extended European Search Report issued April 5, 2022 in European Application No. 18942303.1 (references AA-AB cited herein)					
	AX						
	AY						
	AZ					☐ Additional References sheet(s) attached	
Examiner	/Alfredo Bermudez Lozada/ (05/09/2022)				Date considered	05/09/2022	
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ABL/

Micron Ex. 1015, p. 191
Micron v. YMTC
IPR2024-00794

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2	"20210143179"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2021/12/28 01:58 PM
L2	8	("10134747" OR "10141372" OR "20100320528" OR "20160233270" OR "20180337195" OR "20200185411" OR "20200227555" OR "20200335514").pn.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 05:40 AM
L3	3	"10650623"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:00 AM
L4	11	bsg AND csr AND tsg	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:04 AM
L5	17794	(3d OR three-dimension\$2 OR (three dimension\$2) OR 3-dimension\$2 OR vertical OR stack) near2 nand	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:35 AM
L6	44	staircase AND ((bottom select gate) OR bsg) AND ((top select gate) OR tsg) AND ((common source) OR csr)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L7	44	6 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L8	235	trench WITH (divid\$3 OR separat\$3 OR cut) WITH (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L9	105	8 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L10	13760	5 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:33 AM
L11	1032	5 AND (stair OR step) AND ((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:34 AM
L12	129	((dielectric OR insulat\$3) near2 trench) WITH (select (gate OR	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:36 AM

L13	118	transistor)) 12 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:37 AM
L14	3796	365/185.17.ccls.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:31 AM
L15	56814	((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:32 AM
L16	57	15 AND 14	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:33 AM
L17	1	15 AND 14 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:36 AM
L18	16647	g11c16/0483.cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:42 AM
L19	345	18 AND 15	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L20	25	18 AND 15 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L21	17953	(h01I27/11582,11565,1 1568,11567,1157).cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:56 AM
L22	2190	15 AND 21	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L23	666	15 AND 21 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L24	49	15 AND 21 AND (common NEAR source) AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L25	6	(sub-ssg OR sub-sst OR sub-gst OR sub-gsg OR sub-bsg)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:10 AM
L26	1646	(multiple OR plurality) NEAR select NEAR gate	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:11 AM
L27	448	5 AND 26	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:15 AM
L28	286	5 AND 26 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:27 AM
L29	1	"20210295918"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:11 AM
L30	56	(divid\$3 OR separat\$3 OR cut) near2(plurality OR multiple) near2 (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:35 AM
L31	2	"20140036590"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:51 AM
L32	9	"10950623"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	ADJ	ON	ON	2021/12/30 05:42 AM

L33	790	yangtze.as.	EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2021/12/30 07:02 AM
L34	63353	song.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L35	29984	xiao.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L36	252871	wang.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L37	4	33 AND 34 AND 35 AND 36	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L38	9	8 AND 33	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:03 AM
L39	3	"20180240527"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/05/09 08:15 AM
L40	0	20170040061+	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/05/09 08:15 AM
L41	10	"20170040061"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/05/09 08:16 AM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default	Plurals	British	Time Stamp
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05/09/2022 08:19:03 AM
Workspace: 17154054

Page 3 of 4
AB

				Operator		Equivalents	
N1	2752	G11C16/04.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N2	17261	G11C16/0483.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N3	3863	G11C16/14.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N4	3796	365/185.17.CCLS.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N5	12813	H01L27/11582.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N6	0	N5 AND N4 AND N3 AND N2 AND N1	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N7	598	N1 AND N2	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N8	39	N1 AND N2 AND N3	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N9	2365	N4 AND (N1 OR N2 OR N3 OR N5)	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N10	2935	N5 AND (N1 OR N2 OR N3 OR N4)	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N11	1277	(bsg).clm.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N12	88549	(crs).clm.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N13	0	N11 AND N12 AND N10	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N14	0	N11 AND N12 AND N9	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N15	0	N11 AND N12 AND N8	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:01 PM
N16	0	N11 AND N12 AND N7	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:01 PM

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 534753US		SERIAL NO. 17/154,054	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE January 21, 2021		GROUP 2825	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2012/0273956 A1	11/1/2012	WATANABE			
	AB	2014/0035024 A1	2/6/2014	NOH			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Australian Examination Report issued May 5, 2022 in Australian Application No. 2018451633					
	AX	Singaporean Search Report completed April 28, 2022 in Singaporean Application No. 11202104885P					
	AY	Singaporean Written Opinion issued April 29, 2022 in Singaporean Application No. 11202104885P					
	AZ					☐ Additional References sheet(s) attached	
Examiner					Date considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Electronic Patent Application Fee Transmittal				
Application Number:		17154054		
Filing Date:		21-Jan-2021		
Title of Invention:		NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT		
First Named Inventor/Applicant Name:		Yali SONG		
Filer:		Philippe Jean-Claude Signore/Kristin Newett		
Attorney Docket Number:		534753US		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
Total in USD (\$)				260

Electronic Acknowledgement Receipt	
EFS ID:	45825189
Application Number:	17154054
International Application Number:	
Confirmation Number:	6569
Title of Invention:	NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT
First Named Inventor/Applicant Name:	Yali SONG
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Kristin Newett
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	534753US
Receipt Date:	27-MAY-2022
Filing Date:	21-JAN-2021
Time Stamp:	16:36:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 260
RAM confirmation Number	E20225QG37090498
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		534753USIDS.pdf	3997304	yes	12
			2606e8bc0d00b6c17a9a185ec494eb8475dc4caa		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Patent Term Adjustment Statement under 37 CFR 1.704(d) filed with an IDS		1	1	
	Transmittal Letter		2	2	
	Information Disclosure Statement (IDS) Form (SB08)		3	3	
	Non Patent Literature		4	5	
	Non Patent Literature		6	7	
	Non Patent Literature		8	12	
	Warnings:				
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38241	no	2
			3194d2432f56e1b1629d6a42e9bd919d068894b6		
Warnings:					
Information:					
Total Files Size (in bytes):			4035545		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

**PATENT TERM ADJUSTMENT
STATEMENT UNDER 37 CFR 1.704(d)**

Application Number	17/154,054
Filing Date	January 21, 2021
First Named Inventor	Yali SONG, et al.
Art Unit	2825
Examiner Name	BERMUDEZ LOZADA, ALFREDO
Practitioner Docket No.	534753US

APPLICANT HEREBY STATES THE FOLLOWING (please review 37 CFR 1.704(d) before filing this form):

- ☐ Each item of information contained in the information disclosure statement was first cited in any communication from a patent office in a counterpart foreign or international application or from the Office, and this communication was not received by any individual designated in 37 CFR 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

AND/OR

- ☐ Each item of information contained in the information disclosure statement is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in 37 CFR 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

INSTRUCTIONS:

- **This form will not satisfy the requirement of 37 CFR 1.97(e).** The present statement is filed under 37 CFR 1.704(d) and will not substitute for compliance with any of the requirements of 37 CFR 1.97 and 1.98. For an information disclosure statement to comply with 37 CFR 1.97(c) or (d), the information disclosure statement must be accompanied by a statement under 37 CFR 1.97(e) not with standing any statement filed under 37 CFR 1.704(d).
- The present form (PTO/SB/133) should be filed concurrently with the information disclosure statement to derive benefit under 37 CFR 1.704(d).

Signature /John S. Kern/

Date 5/27/2022

Typed or
printed name John S. Kern

Practitioner
Registration Number 42,719

Note: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below*.

* Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yali SONG, et al.

SERIAL NO: 17/154,054

GAU: 2825

FILED: January 21, 2021

EXAMINER: BERMUDEZ LOZADA,
ALFREDO

FOR: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the reference(s) listed on the attached form PTO-1449 and/or accompanying documents from a corresponding foreign application. Copies of the listed reference(s) are attached, where required, as are either statements of relevancy, English translations of the categories of cited documents for foreign search reports or English translations of foreign Office Actions which provide the statement of relevancy for the foreign language references cited therein, or any readily available partial or full English translations of pertinent portions of any non-English language reference(s).
- ☒ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

/John S. Kern/

John S. Kern

Registration No. 42,719

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 02/12)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569
22850	7590	06/14/2022		
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER BERMUDEZ LOZADA, ALFREDO	
			ART UNIT	PAPER NUMBER
			2825	
			NOTIFICATION DATE	DELIVERY MODE
			06/14/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OBLONPAT@OBLON.COM
iahmadi@oblon.com
patentdocket@oblon.com

Supplemental Notice of Allowability	Application No. 17/154,054	Applicant(s) SONG et al.	
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the IDS of 05/27/2022.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-14 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 05/27/2022.	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____	7. ☐ Other _____
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____	

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
--	--

DETAILED ACTION

Notice of AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This action supplements the Notice of Allowance mailed May 12, 2022 to consider the new Information Disclosure Statement of May 27, 2022

Claims 1-14 are pending. Claim 1 is independent.

Information Disclosure Statement

Acknowledgment is made of applicant's Information Disclosure Statement (IDS) filed on May 27, 2022. This IDS has been considered.

Allowable Subject Matter

Claims 1-14 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to independent claim 1, there is no teaching or suggestion in the prior art of record to provide the recited first dielectric trenches extending in a height direction of the substrate through the BSG to separate the BSG into a plurality of sub-BSG and partially through the stack, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALFREDO BERMUDEZ LOZADA whose telephone number is (571)272-0877. The examiner can normally be reached 7:00AM-3:30PM EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander G Sofocleous can be reached on 571-272-0635. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alfredo Bermudez Lozada/
Primary Examiner, Art Unit 2825

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

CPC						
Symbol				Type	Version	
H01L	/	27	/	11582	F	2013-01-01
G11C	/	16	/	0483	I	2013-01-01
G11C	/	16	/	14	I	2013-01-01
H01L	/	21	/	31116	I	2013-01-01
H01L	/	23	/	528	I	2013-01-01
H01L	/	27	/	11565	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	29	/	0847	I	2013-01-01
H01L	/	29	/	1037	I	2013-01-01
H01L	/	21	/	0276	A	2013-01-01
H01L	/	21	/	31144	A	2013-01-01

CPC Combination Sets					
Symbol			Type	Set	Version
	/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	08 June 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220608

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G11C	/	16	/ 04
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
365	185.17

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	08 June 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220608

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	4	10												
2	2	6	11												
3	3	14	12												
7	4	12	13												
8	5	5	14												
9	6														
13	7														
10	8														
11	9														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	08 June 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220608

<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483, G11C16/14, H01L23/528, H01L27/11565, H01L27/1157, H01L27/11556, H01L27/11551	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	185.17	12/30/2021	ABL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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Search Notes 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

Search Notes		
Search Notes	Date	Examiner
East search, Prior art search, Inventor name search	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL
PE2E Search all databases	12/30/2021	ABL
IP.com	12/30/2021	ABL
Consulted with Alex Sofocleous (SPE)	12/30/2021	ABL
Inventor and Assignee searched	12/30/2021	ABL
search updated	04/19/2022	ABL
search updated	05/09/2022	ABL
New IDS considered	05/09/2022	ABL
New IDS considered	06/08/2022	ABL

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
Interference search		09/30/2021	GA
G11C	16/14	04/19/2022	ABL
G11C	16/0483	04/19/2022	ABL
G11C	16/04	04/19/2022	ABL
365	185.17	04/19/2022	ABL
H01L	27/11582	04/19/2022	ABL

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2	"20210143179"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2021/12/28 01:58 PM
L2	8	("10134747" OR "10141372" OR "20100320528" OR "20160233270" OR "20180337195" OR "20200185411" OR "20200227555" OR "20200335514").pn.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 05:40 AM
L3	3	"10650623"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:00 AM
L4	11	bsg AND csr AND tsg	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:04 AM
L5	17794	(3d OR three-dimension\$2 OR (three dimension\$2) OR 3-dimension\$2 OR vertical OR stack) near2 nand	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:35 AM
L6	44	staircase AND ((bottom select gate) OR bsg) AND ((top select gate) OR tsg) AND ((common source) OR csr)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L7	44	6 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L8	235	trench WITH (divid\$3 OR separat\$3 OR cut) WITH (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L9	105	8 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L10	13760	5 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:33 AM
L11	1032	5 AND (stair OR step) AND ((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:34 AM
L12	129	((dielectric OR insulat\$3) near2 trench) WITH (select (gate OR	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:36 AM

L13	118	transistor)) 12 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:37 AM
L14	3796	365/185.17.ccls.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:31 AM
L15	56814	((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:32 AM
L16	57	15 AND 14	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:33 AM
L17	1	15 AND 14 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:36 AM
L18	16647	g11c16/0483.cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:42 AM
L19	345	18 AND 15	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L20	25	18 AND 15 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L21	17953	(h01I27/11582,11565,1 1568,11567,1157).cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:56 AM
L22	2190	15 AND 21	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L23	666	15 AND 21 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L24	49	15 AND 21 AND (common NEAR source) AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L25	6	(sub-ssg OR sub-sst OR sub-gst OR sub-gsg OR sub-bsg)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:10 AM
L26	1646	(multiple OR plurality) NEAR select NEAR gate	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:11 AM
L27	448	5 AND 26	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:15 AM
L28	286	5 AND 26 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:27 AM
L29	1	"20210295918"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:11 AM
L30	56	(divid\$3 OR separat\$3 OR cut) near2(plurality OR multiple) near2 (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:35 AM
L31	2	"20140036590"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:51 AM
L32	9	"10950623"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	ADJ	ON	ON	2021/12/30 05:42 AM

L33	790	yangtze.as.	EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L34	63353	song.in.	(US-PGPUB; USPAT)		ADJ	ON	ON	2021/12/30 07:02 AM
L35	29984	xiao.in.	(US-PGPUB; USPAT)		ADJ	ON	ON	2021/12/30 07:02 AM
L36	252871	wang.in.	(US-PGPUB; USPAT)		ADJ	ON	ON	2021/12/30 07:02 AM
L37	4	33 AND 34 AND 35 AND 36	(US-PGPUB; USPAT)		ADJ	ON	ON	2021/12/30 07:02 AM
L38	9	8 AND 33	(US-PGPUB; USPAT)		ADJ	ON	ON	2021/12/30 07:03 AM
L39	3	"20180240527"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)		ADJ	ON	ON	2022/05/09 08:15 AM
L40	0	20170040061+	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)		ADJ	ON	ON	2022/05/09 08:15 AM
L41	10	"20170040061"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)		ADJ	ON	ON	2022/05/09 08:16 AM
L42	3	"20120273956"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,		ADJ	ON	ON	2022/06/08 10:28 AM

L43	10	"20140035024"	CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:30 AM
L44	46	"10141372"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:31 AM
L45	8	"20180130814"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:32 AM
L46	10	"20140035024"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:33 AM
L47	3	"20120273965"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	ADJ	ON	ON	2022/06/08 10:33 AM

L48	5	"20140138765"	EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:34 AM
L49	3	"20180261618"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:35 AM
L50	3	"20170200676"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:36 AM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	2752	G11C16/04.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N2	17261	G11C16/0483.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N3	3863	G11C16/14.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N4	3796	365/185.17.CCLS.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N5	12813	H01L27/11582.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N6	0	N5 AND N4 AND N3	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19

N7	598	AND N2 AND N1 N1 AND N2	(US-PGPUB; USPAT)	ADJ	ON	ON	02:59 PM 2022/04/19
N8	39	N1 AND N2 AND N3	(US-PGPUB; USPAT)	ADJ	ON	ON	02:59 PM 2022/04/19
N9	2365	N4 AND (N1 OR N2 OR N3 OR N5)	(US-PGPUB; USPAT)	ADJ	ON	ON	02:59 PM 2022/04/19
N10	2935	N5 AND (N1 OR N2 OR N3 OR N4)	(US-PGPUB; USPAT)	ADJ	ON	ON	02:59 PM 2022/04/19
N11	1277	(bsg).clm.	(US-PGPUB; USPAT)	ADJ	ON	ON	02:59 PM 2022/04/19
N12	88549	(crs).clm.	(US-PGPUB; USPAT)	ADJ	ON	ON	03:00 PM 2022/04/19
N13	0	N11 AND N12 AND N10	(US-PGPUB; USPAT)	ADJ	ON	ON	03:00 PM 2022/04/19
N14	0	N11 AND N12 AND N9	(US-PGPUB; USPAT)	ADJ	ON	ON	03:00 PM 2022/04/19
N15	0	N11 AND N12 AND N8	(US-PGPUB; USPAT)	ADJ	ON	ON	03:01 PM 2022/04/19
N16	0	N11 AND N12 AND N7	(US-PGPUB; USPAT)	ADJ	ON	ON	03:01 PM 2022/04/19

SHEET 1 OF 1

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 534753US		SERIAL NO. 17/154,054	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE January 21, 2021		GROUP 2825	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2012/0273956 A1	11/1/2012	WATANABE			
	AB	2014/0035024 A1	2/6/2014	NOH			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Australian Examination Report issued May 5, 2022 in Australian Application No. 2018451633					
	AX	Singaporean Search Report completed April 28, 2022 in Singaporean Application No. 11202104885P					
	AY	Singaporean Written Opinion issued April 29, 2022 in Singaporean Application No. 11202104885P					
	AZ					☐ Additional References sheet(s) attached	
Examiner	/Alfredo Bermudez Lozada/ (06/08/2022)				Date considered	06/08/2022	
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ABL/

Micron Ex. 1015, p. 219
Micron v. YMTC
IPR2024-00794



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6569

SERIAL NUMBER 17/154,054	FILING or 371(c) DATE 01/21/2021 RULE	CLASS 365	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. 534753US	
APPLICANTS Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA INVENTORS Yali SONG, Wuhan, CHINA; Li Hong XIAO, Wuhan, CHINA; Ming WANG, Wuhan, CHINA; ** CONTINUING DATA ***** This application is a CON of 16/365,725 03/27/2019 PAT 10950623 which is a CON of PCT/CN2018/119908 12/07/2018 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/01/2021					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /ALFREDO BERMUDEZ LOZADA/ Acknowledged Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY CHINA	SHEETS DRAWINGS 20	TOTAL CLAIMS 14	INDEPENDENT CLAIMS 1
ADDRESS OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314 UNITED STATES					
TITLE NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT					
FILING FEE RECEIVED 1820	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Form PTO 1449 (Modified)		INFORMATION DISCLOSURE STATEMENT		ATTY DOCKET NO. 534753US		SERIAL NO. 17/154,054	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE January 21, 2021		GROUP 2825	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,989,317 B1	01/24/2006	RADENS et al.			
	AB	2018/0286678 A1	10/04/2018	LEE			
	AC	2007/0287293 A1	12/13/2007	HAN et al.			
	AD	2015/0263029 A1	09/17/2015	KIM et al.			
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		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AO	108807404A	11/13/2018	China (with English Abstract)		x	
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	AY						
	AZ					☐ Additional References sheet(s) attached	
Examiner					Date considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Electronic Patent Application Fee Transmittal				
Application Number:		17154054		
Filing Date:		21-Jan-2021		
Title of Invention:		NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT		
First Named Inventor/Applicant Name:		Yali SONG		
Filer:		Philippe Jean-Claude Signore/Nicole Brown		
Attorney Docket Number:		534753US		
Filed as Large Entity				
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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
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Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
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RAM confirmation Number	E20226RG34534967
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	c404.pdf	2059566	no	15
			25a69707dbbb221114c3d77c0ee4b5bdd50e6c15		
Warnings:					
Information:					
2	Foreign Reference	jp958.pdf	6634477	no	17
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Warnings:					
Information:					
3		753res.pdf	1358196	yes	21
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
	Non Patent Literature		3	14	
	Non Patent Literature		15	21	
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	38265	no	2
			21b8e874af2b3140ee9d987b8c3bab1a568 8d4c8		
Warnings:					
Information:					
Total Files Size (in bytes):			10090504		

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New Applications Under 35 U.S.C. 111

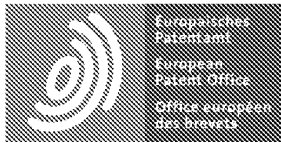
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



Espacenet

CN108807404A Semiconductor manufacturing method and semiconductor structure

Applicants: YANGTZE MEMORY TECH CO LTD

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Classifications:

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Semiconductor manufacturing method and semiconductor structure

Abstract

The present invention provides a contact hole forming method for forming a contact hole in a step region of a three-dimensional memory device and a three-dimensional memory device using the method. A method for a contact hole includes the steps of forming a semiconductor structure having a step region including a first step region and a second step region and alternately stacked by at least one dielectric layer and at least one conductive layer; forming a first step region contact hole and a second step region contact hole until the first step region contact hole contacts the conductive layer of the first step region layer; and forming a protective layer on the side wall and bottom surface of the contact hole in the first step region; a step of consuming the protective layer and contacting the contact hole of the second step region with the conductive layer of the second step region.



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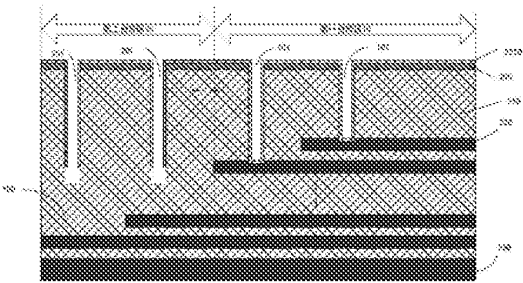
权利要求书2页 说明书7页 附图4页

(54)发明名称

半导体制造方法及半导体结构

(57)摘要

本发明提供一种在三维存储器件中的台阶区形成接触孔的接触孔形成方法及使用了该方法的三维存储器件。该接触孔形成方法包括：形成具有包括第一台阶区和第二台阶区且由至少一个介质层和至少一个导电层交替堆叠而成的台阶区的半导体结构的步骤；形成第一台阶区接触孔及第二台阶区接触孔，直至第一台阶区接触孔与第一台阶层的导电层相接触的步骤；以及在第一台阶区接触孔的侧壁及底面形成保护层的步骤；消耗保护层，并使第二台阶区接触孔与第二台阶区的导电层相接触的步骤。



1. 一种接触孔形成方法,用于形成三维存储器件中台阶区的接触孔,其特征在于,包括下述工序:

半导体结构形成工序,该半导体结构具有台阶区,所述台阶区包括第一台阶区和位于所述第一台阶区下方的第二台阶区,所述第一台阶区和所述第二台阶区均包含多个台阶结构,所述台阶结构由至少一个介质层和至少一个导电层交替堆叠而成;

接触孔第一形成工序,在所述第一台阶区及所述第二台阶区上,形成与所述第一台阶区的导电层对应的第一台阶区接触孔及与所述第二台阶区的导电层对应的第二台阶区接触孔,其中,所述第一台阶区接触孔与其对应的第一台阶区的导电层接触或者位于其对应的第一台阶区的导电层上方;

保护层形成工序,在所述第一台阶区接触孔的侧壁及底面形成保护层;以及

接触孔第二形成工序,使所述第二台阶区接触孔与其对应的第二台阶区的导电层接触,或者在使所述第二台阶区接触孔与其对应的第二台阶区的导电层接触的同时,使所述第一台阶区接触孔与其对应的第一台阶区的导电层接触。

2. 如权利要求1所述的接触孔形成方法,其特征在于,

在所述接触孔第一形成工序中,所形成的所述第二台阶区接触孔的深度比所述第一台阶区接触孔的深度要深。

3. 如权利要求1所述的接触孔形成方法,其特征在于,

在所述保护层形成工序中,还在所述第二台阶区接触孔的侧壁的至少一部分区域形成保护层,而所述第二台阶区接触孔的底面不形成保护层。

4. 如权利要求1所述的接触孔形成方法,其特征在于,

在所述接触孔第一形成工序中,根据所述台阶区所包含的所述台阶结构的数量来确定所述第一台阶区接触孔的深度。

5. 如权利要求1所述的接触孔形成方法,其特征在于,

在所述保护层形成工序中,根据所述台阶区所包含的所述台阶结构的数量来确定所述保护层的厚度。

6. 如权利要求1所述的接触孔形成方法,其特征在于,

在所述接触孔第一形成工序和所述接触孔第二形成工序中,使用同一掩模版。

7. 如权利要求1所述的接触孔形成方法,其特征在于,

所述保护层由导电材料构成。

8. 如权利要求7所述的接触孔形成方法,其特征在于,

所述保护层的材料为金属或金属硅化物。

9. 一种三维存储器件,其特征在于,包括:

台阶区,所述台阶区包括第一台阶区和位于所述第一台阶区下方的第二台阶区,所述第一台阶区和所述第二台阶区均包含多个台阶结构,所述台阶结构由至少一个介质层和至少一个导电层交替堆叠而成;

第一台阶区导电接触,所述第一台阶区导电接触形成于所述第一台阶区的导电层上,并与其对应的所述第一台阶区的导电层接触,至少部分所述第一台阶区导电接触包括第一材料层和第二材料层,所述第二材料层由不同于所述第一材料层的材料构成;

第二台阶区导电接触,所述第二台阶区导电接触形成于所述第二台阶区的导电层上,

并与其对应的所述第二台阶区的导电层接触。

10. 如权利要求9所述的三维存储器件,其特征在于,
所述第一材料层由导电材料构成。

11. 如权利要求10所述的三维存储器件,其特征在于,
所述第一材料层与其对应的所述第一台阶区的导电层接触,所述第二材料层形成在所述
所述第一材料层的侧壁。

12. 如权利要求10所述的三维存储器件,其特征在于,
所述第二材料层由导电材料构成,所述第二材料层与其对应的所述第一台阶区的导电
层接触,所述第二材料层形成在所述第一材料层的侧壁和底面。

13. 如权利要求9所述的三维存储器件,其特征在于,
所述三维存储器件为浮栅型三维NAND存储器或电荷俘获型三维NAND存储器。

半导体制造方法及半导体结构

技术领域

[0001] 本发明涉及半导体制造方法及使用了该半导体制造方法的半导体结构,尤其涉及在三维存储器件中的台阶区形成接触孔的方法及使用了该方法的三维存储器件。

背景技术

[0002] 随着半导体技术的不断发展,目前存储器制造技术已经逐步从简单的平面结构过渡到较为复杂的三维结构,通过将存储器单元三维地布置在衬底之上来提高集成密度。这种三维存储器件的技术研发是国际研发的主流之一。

[0003] 众所周知,在半导体的版图中,有源区、多晶硅和金属层之间的连接都需要通过接触孔或导通孔来实现。对于三维存储器件中台阶区接触孔的形成,由于三维存储器件中台阶区的台阶层数较多,因此,在接触孔形成步骤中,为了保证低层台阶有足够的过刻蚀(Over Etch)深度,高层台阶容易出现刻蚀穿透(Punch Through),从而无法满足工艺要求,进而使得产品良率降低。

[0004] 针对这种情况,目前业界通常选用多块掩膜版,针对高层台阶和低层台阶来分别形成接触孔。

发明内容

[0005] 发明所要解决的技术问题

[0006] 在通过使用多块掩膜版来分别形成高层台阶和低层台阶的接触孔的现有技术中,随着三维存储器件中台阶区的台阶层数的增加,相应地需要增加掩膜版的数量,由此将会导致生产成本的大幅增加。

[0007] 此外,由于需要使用不同的掩膜版来分别多次形成高层台阶和低层台阶的接触孔,制造工艺中的偏差不断累积变大,进而有可能导致最终产品无法满足工艺要求,使得产品良率降低。

[0008] 解决技术问题所采用的技术方案

[0009] 本发明是为了解决上述问题而完成的,其目的在于提供一种在三维存储器件中的台阶区形成接触孔的方法以及使用了该方法的三维存储器件。

[0010] 本发明所涉及的接触孔形成方法用于形成三维存储器件中台阶区的接触孔,其特征在于,包括下述工序:

[0011] 半导体结构形成工序,该半导体结构具有台阶区,所述台阶区包括第一台阶区和位于所述第一台阶区下方的第二台阶区,所述第一台阶区和所述第二台阶区均包含多个台阶结构,所述台阶结构由至少一个介质层和至少一个导电层交替堆叠而成;

[0012] 接触孔第一形成工序,在所述第一台阶区及所述第二台阶区上,形成与所述第一台阶区的导电层对应的第一台阶区接触孔及与所述第二台阶区的导电层对应的第二台阶区接触孔,其中,所述第一台阶区接触孔与其对应的第一台阶区的导电层接触或者位于其对应的第一台阶区的导电层上方;

- [0013] 保护层形成工序,在所述第一台阶区接触孔的侧壁及底面形成保护层;以及
- [0014] 接触孔第二形成工序,使所述第二台阶区接触孔与其对应的第二台阶区的导电层接触,或者在使所述第二台阶区接触孔与其对应的第二台阶区的导电层接触的同时,使所述第一台阶区接触孔与其对应的第一台阶区的导电层接触。
- [0015] 优选为,在所述接触孔第一形成工序中,所形成的所述第二台阶区接触孔的深度比所述第一台阶区接触孔的深度要深。
- [0016] 优选为,在所述保护层形成工序中,还在所述第二台阶区接触孔的侧壁的至少一部分区域形成保护层,而所述第二台阶区接触孔的底面不形成保护层。
- [0017] 优选为,在所述接触孔第一形成工序中,根据所述台阶区所包含的所述台阶结构的数量来确定所述第一台阶区接触孔的深度。
- [0018] 优选为,在所述保护层形成工序中,根据所述台阶区所包含的所述台阶结构的数量来确定所述保护层的厚度。
- [0019] 优选为,在所述接触孔第一形成工序和所述接触孔第二形成工序中,使用同一掩膜版。
- [0020] 优选为,所述保护层由导电材料构成。
- [0021] 优选为,所述保护层的材料为金属或金属硅化物。
- [0022] 此外,本发明所涉及的三维存储器件的特征在于,包括:
- [0023] 台阶区,所述台阶区包括第一台阶区和位于所述第一台阶区下方的第二台阶区,所述第一台阶区和所述第二台阶区均包含多个台阶结构,所述台阶结构由至少一个介质层和至少一个导电层交替堆叠而成;
- [0024] 第一台阶区导电接触,所述第一台阶区导电接触形成于所述第一台阶区的导电层上,并与其对应的所述第一台阶区的导电层接触,至少部分所述第一台阶区导电接触包括第一材料层和第二材料层,所述第二材料层由不同于所述第一材料层的材料构成;
- [0025] 第二台阶区导电接触,所述第二台阶区导电接触形成于所述第二台阶区的导电层上,并与其对应的所述第二台阶区的导电层接触。
- [0026] 优选为,所述第一材料层由导电材料构成。
- [0027] 优选为,所述第一材料层与其对应的所述第一台阶区的导电层接触,所述第二材料层形成在所述第一材料层的侧壁。
- [0028] 优选为,所述第二材料层由导电材料构成,所述第二材料层与其对应的所述第一台阶区的导电层接触,所述第二材料层形成在所述第一材料层的侧壁和底面。
- [0029] 优选为,所述三维存储器件为浮栅型三维NAND存储器或电荷俘获型三维NAND存储器。
- [0030] 发明效果
- [0031] 根据本发明所涉及的接触孔形成方法以及使用了该接触孔形成方法的三维存储器件,只需要使用一块掩膜版就能够在台阶层数较多的三维存储器件中形成台阶接触孔,而不会出现刻蚀穿透,大幅减少了掩膜版数量,缩减了生产成本。
- [0032] 此外,根据本发明所涉及的接触孔形成方法以及使用了该接触孔形成方法的三维存储器件,随着三维存储器件的技术发展,即使所堆叠的台阶层数继续增加,也不需要增加掩膜版的数量,大幅缩短了生产周期,进而缩减了生产成本。

[0033] 此外,根据本发明所涉及的接触孔形成方法以及使用了该接触孔形成方法的三维存储器件,由于在整个接触孔形成工序中只需要使用一块掩膜版就能够实现具有足够过蚀深度且可靠性较高的接触孔,因此,整个制造工艺偏差减小,三维存储器件的电气性能可靠性增加,进而提高了最终产品良率。

附图说明

[0034] 图1是表示本发明所涉及的三维存储器件的台阶区的剖视图。

[0035] 图2是表示本发明的实施方式1所涉及的接触孔形成方法的流程图。

[0036] 图3是表示本发明的实施方式1所涉及的接触孔第一形成工序的剖视图。

[0037] 图4是表示本发明的实施方式1所涉及的保护层形成工序的剖视图。

[0038] 图5是表示本发明的实施方式1所涉及的接触孔第二形成工序的剖视图。

[0039] 图6是表示本发明的实施方式3所涉及的接触孔第二形成工序的半导体结构的剖视图。

具体实施方式

[0040] 为了让本发明的上述目的、特征和优点能更明显易懂,以下结合附图对本发明的具体实施方式作详细说明。在各图中,对同一要素标注相同标号,并省略重复说明。此外,各图中的横向点划线和纵向点划线表示在横向和纵向分别省略了类似结构。

[0041] 在下面的描述中阐述了很多具体细节以便于充分理解本发明,但是本发明还可以采用其它不同于在此描述的其它方式来实施,因此本发明不受下面公开的具体实施例的限制。

[0042] 如本申请和权利要求书所示,除非上下文明确提示例外情形,“一”、“一个”、“一种”和/或“该”等词并非特指单数,也可包括复数。一般说来,术语“包括”与“包含”仅提示包括已明确标识的步骤和元素,而这些步骤和元素不构成一个排它性的罗列,方法或者设备也可能包含其他的步骤或元素。

[0043] 在详述本发明实施例时,为便于说明,表示器件结构的剖面图会不依一般比例作局部放大,而且所述示意图只是示例,其在此不应限制本发明保护的范围。此外,在实际制作中应包含长度、宽度及深度的三维空间尺寸。

[0044] 为了方便描述,此处可能使用诸如“之下”、“下方”、“低于”、“下面”、“上方”、“上”等等的空间关系词语来描述附图中所示的一个元件或特征与其他元件或特征的关系。将理解到,这些空间关系词语意图包含使用中或操作中的器件的、除了附图中描绘的方向之外的其他方向。例如,如果翻转附图中的器件,则被描述为在其他元件或特征“下方”或“之下”或“下面”的元件的方向将改为在所述其他元件或特征的“上方”。因而,示例性的词语“下方”和“下面”能够包含上和下两个方向。器件也可能具有其他朝向(旋转90度或处于其他方向),因此应相应地解释此处使用的空间关系描述词。此外,还将理解,当一层被称为在两层“之间”时,它可以是所述两层之间仅有的层,或者也可以存在一个或多个介于其间的层。

[0045] 在本申请的上下文中,所描述的第一特征在第二特征之“上”的结构可以包括第一和第二特征形成直接接触的实施例,也可以包括另外的特征形成在第一和第二特征之间的实施例,这样第一和第二特征可能不是直接接触。

[0046] (接触孔形成方法)

[0047] 实施方式1

[0048] 图1示出了本发明所涉及的三维存储器件中台阶区的剖视图。如图1所示,在例如为浮栅型三维NAND闪存的三维存储器件中,具有台阶区100和衬底230。台阶区100形成于衬底230的表面。

[0049] 台阶区100中,形成有第一台阶区10和第二台阶区20,第一台阶区10形成在第二台阶区20的上方。第一台阶区10具有台阶结构,由介质层210和导电层220沿垂直于台阶区100的表面的堆叠方向交替堆叠而成。同样地,第二台阶区20具有台阶结构,由介质层210和导电层220沿垂直于台阶区100的表面的堆叠方向交替堆叠而成。此外,在台阶区100表面还形成有硬掩膜层200,构成用于形成接触孔的掩膜版。

[0050] 为了便于说明,图1中举例示出了第一台阶区10和第二台阶区20分别具有两层介质层210及导电层220的结构,但介质层210及导电层220的层数并不限于此,它们的层数可以为一层,也可以为三层以上。

[0051] 在图1的示例中省略了中间若干层台阶结构,按照台阶结构距离台阶区表面的深浅,将台阶区100中上两层台阶结构作为第一台阶区,将台阶区100中最下两层的台阶结构作为第二台阶区来进行了说明,但此处第一台阶区和第二台阶区中所包含的台阶结构的数量并没有特别的限制,可以根据制造过程中的实际情况来进行选择,例如将距离台阶区表面较浅的若干个台阶结构选作为第一台阶区,将位于第一台阶区以下的若干个台阶结构选作为第二台阶区,只要第二台阶区位于第一台阶区下方即可。

[0052] 此外,图1所示的台阶区100所具有的介质层210、导电层220的材料及形成方式均没有特别的限定,使用本领域通用的材料及形成方式即可。例如,介质层210使用氧化硅,而导电层220使用钨。

[0053] 图2示出了本发明的实施方式1所涉及的接触孔形成方法的流程图。

[0054] 如图2所示,首先进行半导体结构形成工序(S101),在该工序S101中,形成图1所示的半导体结构。

[0055] 其次,进行接触孔第一形成工序(S102),在该工序S102中,利用硬掩膜层200构成的掩膜版,利用刻蚀工艺,在第一台阶区10中,与第一台阶区10的导电层220相对应地形成第一台阶区接触孔101,与此同时,在第二台阶区20中,与第二台阶区20的导电层220相对应地形成第二台阶区接触孔201,直至第一台阶区接触孔101与台阶结构中的导电层220相接触,即导电层220中的至少一部分被蚀刻消耗。

[0056] 图3示出了经过接触孔第一形成工序后得到的半导体结构的剖视图。如图3所示,经过接触孔第一形成工序,在第一台阶区和第二台阶区分别形成两个第一台阶区接触孔101和两个第二台阶区接触孔201。两个第一台阶区接触孔101与相应的导电层220相接触,即导电层220中的至少一部分被蚀刻消耗。此外,所形成的两个第二台阶区接触孔201的深度均比两个第一台阶区接触孔101的深度要深。

[0057] 在图3的示例中,示出了在第一台阶区和第二台阶区分别形成两个接触孔的示例,但接触孔的数量并不限于此,根据第一台阶区和第二台阶区所包含的台阶数量,工序S102中所形成的接触孔的个数可以分别为一个,也可以分别为三个以上。

[0058] 此外,在图3所示的示例中,示出了利用刻蚀工艺形成接触孔的示例,但形成接触

孔的方式并不限于此,也可以使用本领域通用的其他方法。并且,在本示例中,采用各向异性较好的等离子体干法刻蚀工艺,但刻蚀工艺并不限于此,也可以使用本领域通用的其他刻蚀工艺。

[0059] 接着,进行保护层形成工序(S103),在该工序S103中,利用沉积工艺,在工序S102后残留的硬掩膜层200表面进一步沉积形成保护层2210。

[0060] 图4示出了经过保护层形成工序后得到的半导体结构的剖视图。如图4所示,通过控制沉积工艺进行的时间,使得第一台阶区的两个第一台阶区接触孔101的侧壁及底面被保护层2210覆盖。由于沉积条件相同,且第二台阶区的第二台阶区接触孔201的深度比第一台阶区接触孔101要深,因此,相应地,第二台阶区的两个第二台阶区接触孔201的侧壁的只有一部分被保护层2210覆盖,而第二台阶区接触孔201的底面没有被保护层2210覆盖或者所覆盖的保护层2210非常薄。此处,图4仅示出了第二台阶区接触孔201的底面没有被保护层2210覆盖的示例。

[0061] 另外,为了确保下道工序中第一台阶区接触孔101的底面不会出现刻蚀穿通(Punch Through),根据台阶区100所包含的台阶结构的数量来确定保护层2210的厚度。该厚度可通过控制沉积工艺的时间来实现。

[0062] 在图4的示例中,示出了通过沉积工艺来形成保护层2210的示例,但形成保护层2210的方式并不限于此,也可以使用本领域通用的其他方法。在本示例中,作为沉积工艺,使用化学气相沉积、物理气相沉积或原子层沉积,但沉积工艺并不限于此,也可以使用本领域通用的其他沉积工艺。

[0063] 此外,对于保护层形成工序(S103)中形成的保护层2210的材料,可以采用导电材料,也可以采用非导电材料。优选使用导电材料,例如金属或金属硅化物。保护层2210的材料可以与导电层220的材料相同,例如使用钨,也可以与导电层220的材料不同,例如使用硅化钨。

[0064] 最后,进行接触孔第二形成工序(S104),在该工序S104中,利用与工序S102中相同的掩膜版继续进行刻蚀,消耗保护层,直至第二台阶区接触孔201的底面与第二台阶区台阶结构中的导电层220相接触。

[0065] 图5示出经过接触孔第二形成工序后得到的半导体结构的剖视图。如图5所示,第一台阶区的两个第一台阶区接触孔101的侧壁及底面的保护层2210均因蚀刻被消耗,均没有出现刻蚀穿通。与此相对,第二台阶区的两个第二台阶区接触孔201的侧壁的保护层2210也因蚀刻被消耗,并且经过进一步的蚀刻,两个第二台阶区接触孔201均与第二台阶区的导电层220相接触,具有足够的过刻蚀深度,确保了电气性能的可靠性。如上所述,根据图2所示的接触孔形成方法,能够在使用同一掩膜版的情况下,在具有多层台阶结构的三维存储器件的台阶区形成具备足够的过刻蚀深度且可靠性较高的接触孔,从而大幅减少了掩膜版数量,缩减了生产成本。

[0066] 此外,根据图2所示的接触孔形成方法,即使三维存储器件的台阶区的台阶层数继续增加,也不需要增加掩膜版的数量,大幅缩短了生产周期,进而缩减了生产成本。

[0067] 此外,根据图2所示的接触孔形成方法,由于在整个接触孔形成工序中只需要使用一块掩膜版,因此,整个制造工艺偏差减小,三维存储器件的电气性能可靠性增加,进而提高了最终产品良率。

[0068] 实施方式2

[0069] 实施方式2所涉及的接触孔形成方法与实施方式1的不同之处在于：

[0070] 在实施方式1的接触孔第一形成工序(S102)中，在第一台阶区10及第二台阶区20上，形成与第一台阶区10的导电层220对应的第一台阶区接触孔101、以及与第二台阶区20的导电层220对应的第二台阶区接触孔201，直至第一台阶区接触孔101与台阶结构中的导电层220相接触，即导电层220中的至少一部分被蚀刻消耗。

[0071] 而在本实施方式2的接触孔第一形成工序(S102)中，在第一台阶区10及第二台阶区20上，形成与第一台阶区10的导电层220对应的第一台阶区接触孔101、以及与第二台阶区20的导电层220对应的第二台阶区接触孔201，直至第一台阶区接触孔101位于台阶结构中的导电层220上方，即导电层220没有被蚀刻消耗(未图示)。

[0072] 相应地，在实施方式2的接触孔第二形成工序(S104)中，利用与工序S102中相同的掩膜版继续进行刻蚀，消耗保护层，使第二台阶区接触孔201与第二台阶区台阶结构中的导电层220相接触，与此同时使第一台阶区接触孔101与第一台阶区台阶结构中的导电层220相接触。

[0073] 实施方式2的其他工序与实施方式1相同，根据实施方式2的接触孔形成方法，也能够获得与实施方式1相同的效果。

[0074] 实施方式3

[0075] 图6示出实施方式3中经过接触孔第二形成工序后得到的半导体结构的剖视图。实施方式3与实施方式1、2的不同之处在于，在实施方式1、2的图5中仅示出了第一台阶区接触孔101的侧壁的保护层2210、第二台阶区接触孔201的侧壁的保护层2210完全被消耗的示例，但并不限于此。

[0076] 在实施方式3中，如图6所示，经过接触孔第二形成工序后，保护层2210并未完全被消耗，从而在第一台阶区接触孔101及第二台阶区接触孔201的侧壁的至少一部分残留有保护层2210。

[0077] 此外，虽然未进行图示，但在保护层2210为导电材料的情况下，第一台阶区接触孔101的底面也可以残留有保护层2210。

[0078] 由此，根据实施方式3的接触孔形成方法，除了能够获得与实施方式1、2相同的效果之外，在实际工艺中，还可以降低工艺难度，且不会对最终半导体器件的电气性能造成影响。

[0079] (三维存储器件)

[0080] 实施方式3中，通过在所形成的接触孔中进一步填充用于导电接触的填充物300，从而可得到具有下述结构的三维存储器件。

[0081] 如图6所示，该三维存储器件包括：台阶区，该台阶区包括第一台阶区10和位于第一台阶区10下方的第二台阶区20，第一台阶区10和第二台阶区20均包含多个台阶结构，该台阶结构由至少一个介质层210和至少一个导电层220交替堆叠而成；第一台阶区导电接触，该第一台阶区导电接触形成于第一台阶区10的导电层220上，并与其对应的所述第一台阶区10的导电层220接触，至少部分第一台阶区导电接触包括作为第一材料层的填充物300、以及作为第二材料层的保护层2210，保护层2210采用不同于填充物300的材料；以及第二台阶区导电接触，该第二台阶区导电接触形成于第二台阶区20的导电层220上，并与其对

应的第二台阶区20的导电层220接触。

[0082] 优选为,填充物300由导电材料构成。

[0083] 优选为,填充物300与其对应的第一台阶区10的导电层220接触,而保护层2210形成在填充物300的侧壁。

[0084] 此外,虽然未进行图示,但在保护层2210也由导电材料构成的情况下,保护层2210可以形成在填充物300的侧壁和底面,且保护层2210与其对应的第一台阶区10的导电层220接触。

[0085] 此外,具有上述结构的三维存储器件例如为浮栅型三维NAND存储器或电荷俘获型三维NAND存储器。

[0086] 关于该三维存储器件的其他细节,例如存储阵列的结构、周边互连等,并非本发明的重点,在此不再展开描述。

[0087] 本申请使用了特定词语来描述本申请的实施例。如“一个实施例”、“一实施例”、和/或“一些实施例”意指与本申请至少一个实施例相关的某一特征、结构或特点。因此,应强调并注意的是,本说明书中在不同位置两次或多次提及的“一实施例”或“一个实施例”或“一替代性实施例”并不一定是指同一实施例。此外,本申请的一个或多个实施例中的某些特征、结构或特点可以进行适当的组合。

[0088] 虽然本发明已以较佳实施例揭示如上,然其并非用以限定本发明,任何本领域技术人员,在不脱离本发明的精神和范围内,当可作些许的修改和完善,因此本发明的保护范围当以权利要求书所界定的为准。

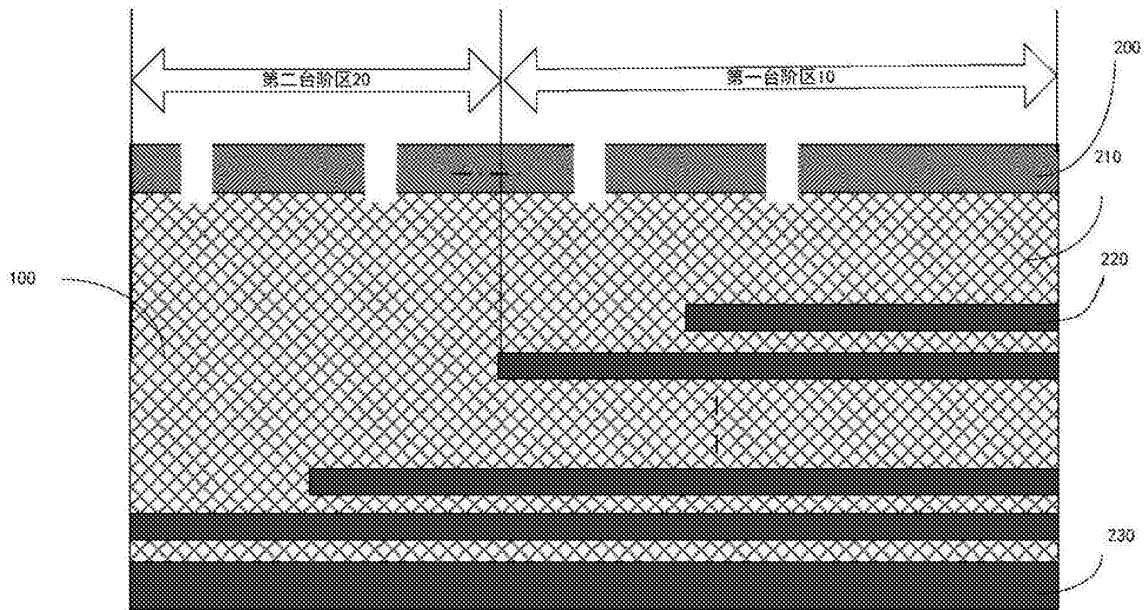


图1

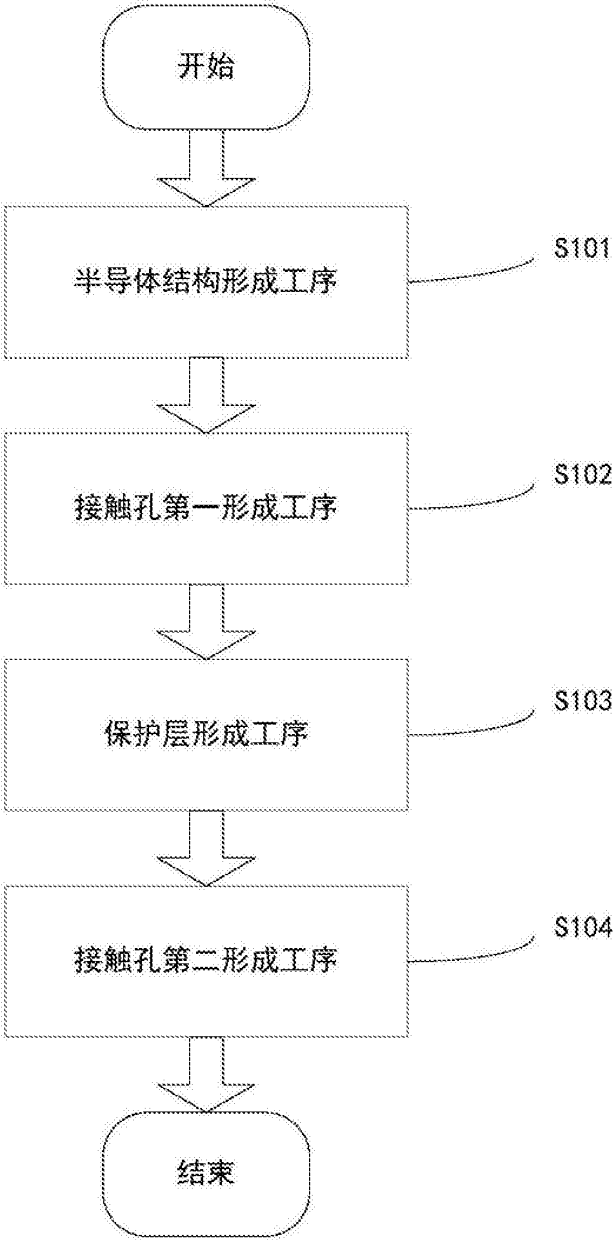


图2

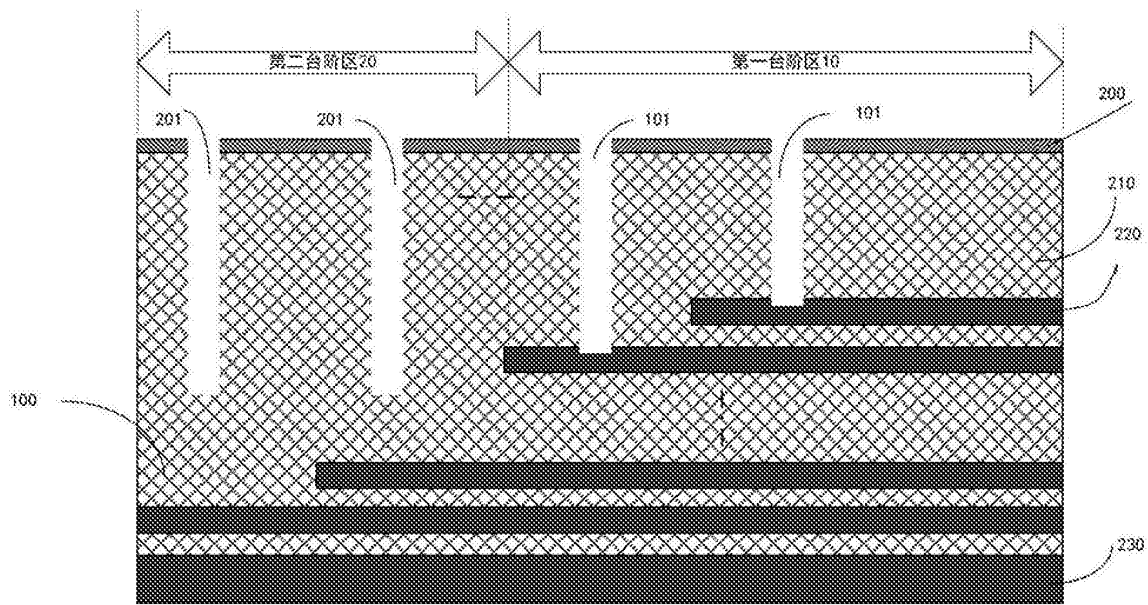


图3

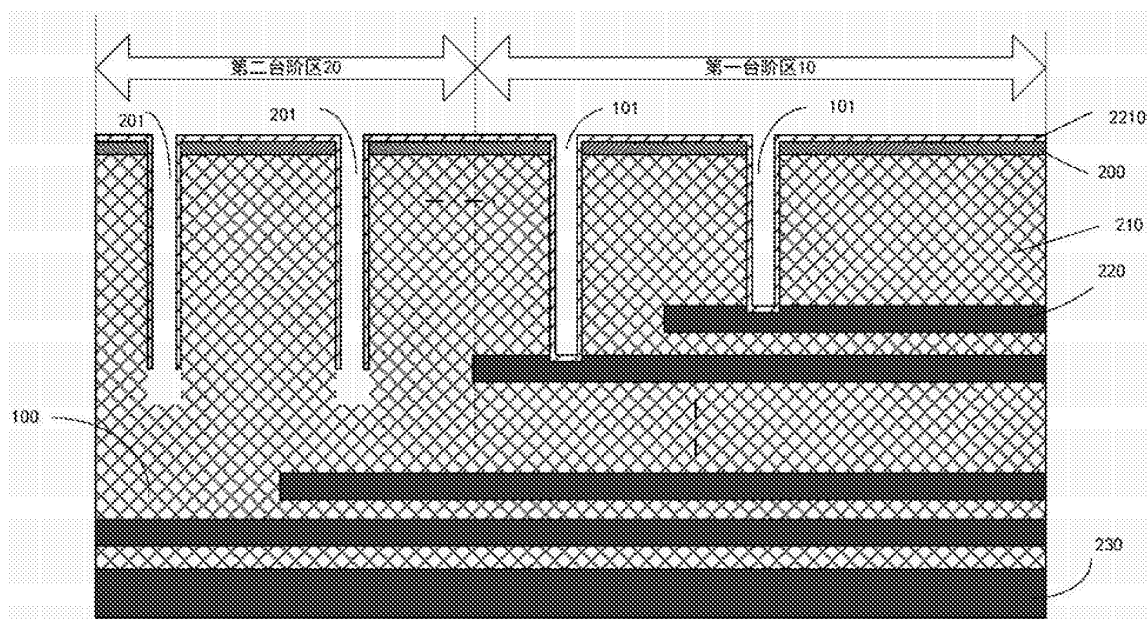


图4

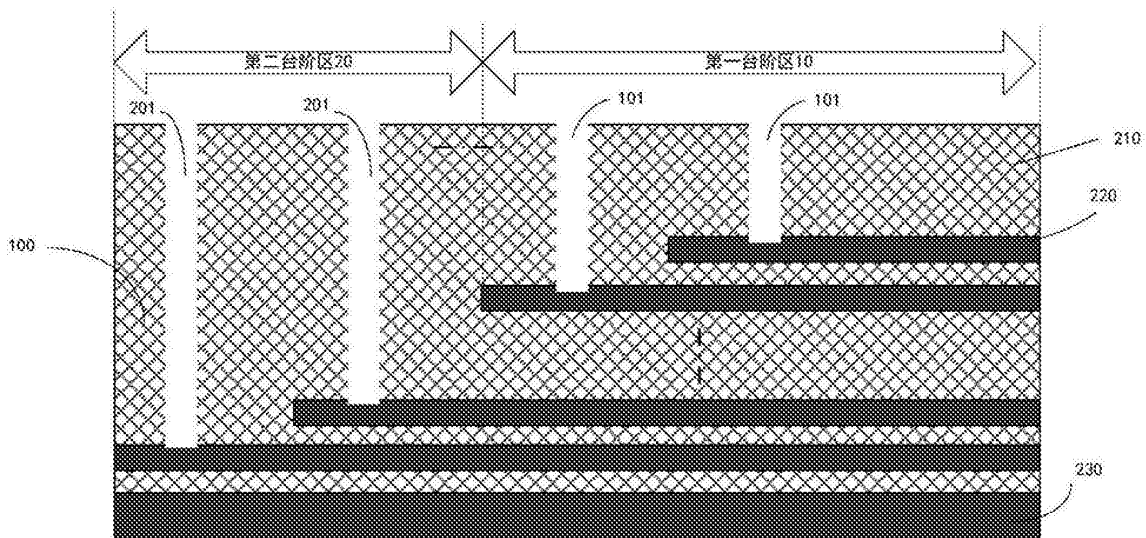


图5

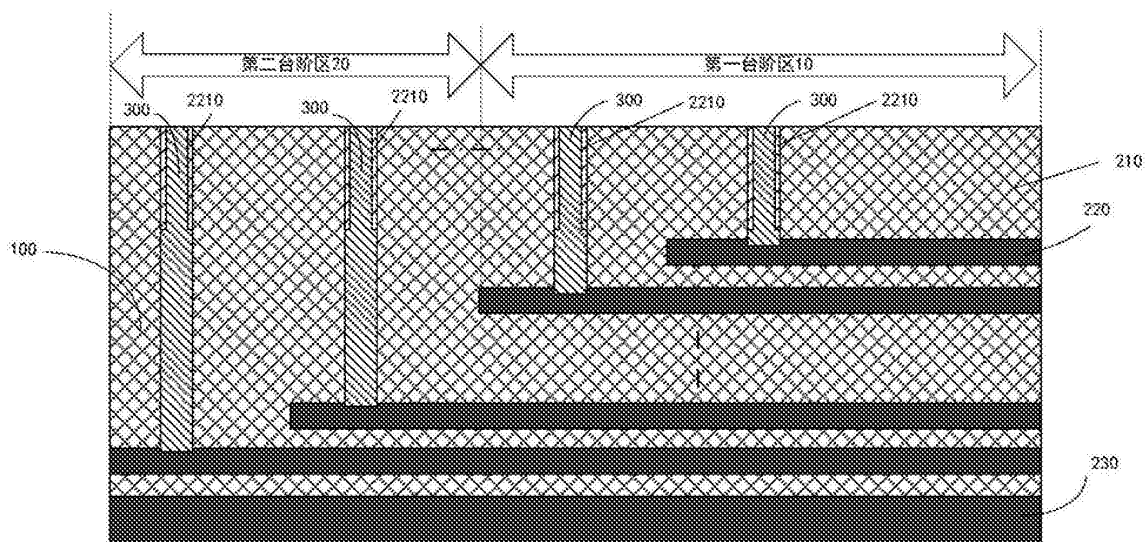
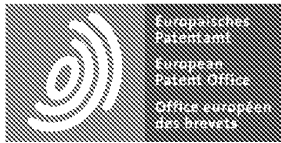


图6



Espacenet

JP2011060958A SEMICONDUCTOR DEVICE, AND METHOD OF MANUFACTURING THE SAME

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SEMICONDUCTOR DEVICE, AND METHOD OF MANUFACTURING THE SAME

Abstract

PROBLEM TO BE SOLVED: To provide a semiconductor device in which variance in bottom part diameter among a plurality of contact holes differing in depth is suppressed, and to provide a method of manufacturing the semiconductor device. SOLUTION: The semiconductor device includes: a laminate having a stepped structure portion wherein a plurality of conductive layers WL1 to WL4 are processed into a staircase pattern; an interlayer insulating layer 43 provided covering the stepped structure portion; and contact electrodes 60 provided in a plurality of contact holes 61 to 64 which are formed penetrating the interlayer insulating layer 43 to reach the conductive layers WL1 to WL4 of respective corresponding stages, wherein the plurality of contact holes 61 to 64 are substantially equal in bottom-part hole diameter and the contact hole reaching the lower stage-side conductive layer is deeper and larger in upper-end hole diameter than the contact hole reaching the upper stage-side conductive layer.

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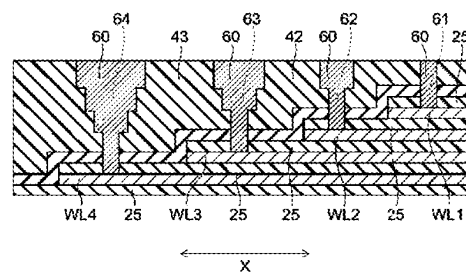
(54) 【発明の名称】 半導体装置及びその製造方法

(57) 【要約】

【課題】 深さの異なる複数のコンタクトホール61の底部径のばらつきを抑制する半導体装置及びその製造方法を提供する。

【解決手段】 本発明の半導体装置は、複数の導電層WL1～WL4が階段状に加工された階段構造部を有する積層体と、階段構造部を覆って設けられた層間絶縁層43と、層間絶縁層43を貫通し、それぞれが対応する各段の導電層WL1～WL4に達して形成された複数のコンタクトホール61～64の内部に設けられたコンタクト電極60とを備え、複数のコンタクトホール61～64の底部の孔径は略同じであり、下段側の導電層に達するコンタクトホールは、上段側の導電層に達するコンタクトホールよりも深く、上端部の孔径が大きい。

【選択図】 図3



【特許請求の範囲】**【請求項 1】**

複数の導電層と複数の絶縁層とがそれぞれ交互に積層され、前記複数の導電層が階段状に加工された階段構造部を有する積層体と、

前記階段構造部を覆って設けられた層間絶縁層と、

前記層間絶縁層を貫通し、それぞれが対応する各段の前記導電層に達して形成された複数のコンタクトホール of の内部に設けられたコンタクト電極と、

を備え、

前記複数のコンタクトホールの底部の孔径は略同じであり、下段側の前記導電層に達するコンタクトホールは、上段側の前記導電層に達するコンタクトホールよりも深く、上端部の孔径が大きいことを特徴とする半導体装置。

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【請求項 2】

導電層と絶縁層とを交互に複数積層する工程と、

前記導電層と前記絶縁層との積層体の一部を階段状に加工する工程と、

前記階段状に加工された導電層を覆う層間絶縁層を形成する工程と、

前記層間絶縁層を貫通し、それぞれが対応する各段の前記導電層に達する複数のコンタクトホールを形成する工程と、

前記コンタクトホールの内部にコンタクト電極を設ける工程と、

を備え、

前記コンタクトホールを形成する工程は、

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下段側の前記導電層上に形成されるコンタクトホールの方が上段側の前記導電層上に形成されるコンタクトホールよりも孔径が大きくなるように、前記複数のコンタクトホールを前記層間絶縁層に形成する工程と、

前記コンタクトホールの側壁に犠牲膜を形成し、相対的に孔径の小さな少なくとも 1 つのコンタクトホールに対してはその内部を前記犠牲膜で埋める工程と、

前記犠牲膜で埋められていないコンタクトホールの底部の下方の前記層間絶縁層を、前記側壁に形成された前記犠牲膜をマスクにしてエッチングする工程と、

前記コンタクトホール内の前記犠牲膜を除去する工程と、

を有することを特徴とする半導体装置の製造方法。

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【請求項 3】

前記側壁に前記犠牲膜を形成することで、前記犠牲膜で埋められていない少なくとも 1 つのコンタクトホールにおける前記犠牲膜の内側の孔径を、前記犠牲膜で埋められたコンタクトホールの底部の孔径と略同じにすることを特徴とする請求項 2 記載の半導体装置の製造方法。

【請求項 4】

前記犠牲膜の内側の孔径が、前記犠牲膜で埋められたコンタクトホールの底部の孔径と略同じとされた前記コンタクトホールに対して、前記コンタクトホールの底部の下方の前記層間絶縁層を、前記側壁に形成された前記犠牲膜をマスクにしてエッチングした後、追加の犠牲膜の埋め込みを行うことを特徴とする請求項 3 記載の半導体装置の製造方法。

【請求項 5】

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前記積層体における前記階段状に加工された部分を、前記層間絶縁層とは異なる材料のストッパー層で覆った後で、前記ストッパー層上に前記層間絶縁層を形成し、

前記層間絶縁層を貫通して前記ストッパー層に達したコンタクトホールに対して、前記犠牲膜の埋め込みを行うことを特徴とする請求項 2 ～ 4 のいずれか 1 つに記載の半導体装置の製造方法。

【発明の詳細な説明】**【技術分野】****【0001】**

本発明は、半導体装置及びその製造方法に関する。

【背景技術】

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【0002】

メモリデバイスにおけるコントロールゲートとして機能する導電層と、絶縁層とを交互に複数積層した積層体にメモリホールを形成し、そのメモリホールの内壁に電荷蓄積層を形成した後、メモリホール内にシリコンを設けることでメモリセルを3次元配列する技術が、例えば特許文献1に提案されている。

【0003】

また、特許文献1には、積層された複数の導電層のそれぞれを上層配線と接続させるための構造として、導電層の階段構造が開示されている。すなわち、導電層を下層ほど長くなるようにしている。そして、階段構造を覆う層間絶縁層に各導電層に達するコンタクトホールを形成し、そのコンタクトホール内にコンタクト電極が埋め込まれる。

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【0004】

コンタクトホールはエッチングにより形成されるが、そのときコンタクトホールの深さが深くなるほど底部径が小さくなる傾向がある。深さの異なる各コンタクトホール間での底部径の差は、各導電層とコンタクト電極との接触面積の差となり、階層の異なるメモリセル間での特性ばらつきにつながるおそれがある。

【先行技術文献】

【特許文献】

【0005】

【特許文献1】特開2007-266143号公報

【発明の概要】

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【発明が解決しようとする課題】

【0006】

本発明は、深さの異なる複数のコンタクトホールの底部径のばらつきを抑制する半導体装置及びその製造方法を提供する。

【課題を解決するための手段】

【0007】

本発明の一態様によれば、複数の導電層と複数の絶縁層とがそれぞれ交互に積層され、前記複数の導電層が階段状に加工された階段構造部を有する積層体と、前記階段構造部を覆って設けられた層間絶縁層と、前記層間絶縁層を貫通し、それぞれが対応する各段の前記導電層に達して形成された複数のコンタクトホールの内部に設けられたコンタクト電極と、を備え、前記複数のコンタクトホールの底部の孔径は略同じであり、下段側の前記導電層に達するコンタクトホールは、上段側の前記導電層に達するコンタクトホールよりも深く、上端部の孔径が大きいことを特徴とする半導体装置が提供される。

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また、本発明の他の一態様によれば、導電層と絶縁層とを交互に複数積層する工程と、前記導電層と前記絶縁層との積層体の一部を階段状に加工する工程と、前記階段状に加工された導電層を覆う層間絶縁層を形成する工程と、前記層間絶縁層を貫通し、それぞれが対応する各段の前記導電層に達する複数のコンタクトホールを形成する工程と、前記コンタクトホールの内部にコンタクト電極を設ける工程と、を備え、前記コンタクトホールを形成する工程は、下段側の前記導電層上に形成されるコンタクトホールの方が上段側の前記導電層上に形成されるコンタクトホールよりも孔径が大きくなるように、前記複数のコンタクトホールを前記層間絶縁層に形成する工程と、前記コンタクトホールの側壁に犠牲膜を形成し、相対的に孔径の小さな少なくとも1つのコンタクトホールに対してはその内部を前記犠牲膜で埋める工程と、前記犠牲膜で埋められていないコンタクトホールの底部の下方の前記層間絶縁層を、前記側壁に形成された前記犠牲膜をマスクにしてエッチングする工程と、前記コンタクトホール内の前記犠牲膜を除去する工程と、を有することを特徴とする半導体装置の製造方法が提供される。

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【発明の効果】

【0008】

本発明によれば、深さの異なる複数のコンタクトホールの底部径のばらつきを抑制する半導体装置及びその製造方法が提供される。

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【図面の簡単な説明】

【0009】

【図1】本発明の実施形態に係る半導体装置におけるメモリセルアレイの模式斜視図。

【図2】同メモリセルアレイにおける要部の拡大断面図。

【図3】本発明の実施形態に係る半導体装置における階段状コンタクト構造部の模式断面図。

【図4】図3に示す階段状コンタクト構造部の形成方法を示す模式断面図。

【図5】図4に続く工程を示す模式断面図。

【図6】図5に続く工程を示す模式断面図。

【図7】図6に続く工程を示す模式断面図。

【図8】図7に続く工程を示す模式断面図。

【図9】図8に続く工程を示す模式断面図。

【図10】図9に続く工程を示す模式断面図。

【図11】本発明の実施形態に係る半導体装置における階段状コンタクト構造部の他の具体例を示す模式断面図。

【図12】本発明の実施形態に係る半導体装置におけるメモリストリングの他の具体例を示す模式斜視図。

【発明を実施するための形態】

【0010】

図1は、本発明の実施形態に係る半導体装置におけるメモリセルアレイの構成を例示する模式図である。なお、図1においては、図を見易くするために、メモリホール内に形成された絶縁膜以外の絶縁部分については図示を省略している。また、以下の実施形態では半導体としてシリコンを例示するが、シリコン以外の半導体を用いてもよい。

【0011】

また、本明細書においては、説明の便宜上、XYZ直交座標系を導入する。この座標系においては、基板10の主面に対して平行な方向であって相互に直交する2方向をX方向及びY方向とし、これらX方向及びY方向の双方に対して直交する方向をZ方向とする。複数の導電層WL1～WL4はZ方向に積層されている。

【0012】

基板10上には図示しない絶縁層を介してバックゲートBGが設けられている。バックゲートBGは、例えば不純物が添加され導電性を有するシリコン層である。バックゲートBG上には、複数の導電層WL1～WL4と、図示しない絶縁層とが交互に積層されている。導電層WL1～WL4の層数は任意であり、本実施形態においては例えば4層の場合を例示する。導電層WL1～WL4は、例えば不純物が添加され導電性を有するシリコン層である。

【0013】

導電層WL1～WL4は、X方向に延在する溝によって複数のブロックに分断されている。あるブロックにおける最上層の導電層WL1上には図示しない絶縁層を介してドレイン側選択ゲートDSGが設けられている。ドレイン側選択ゲートDSGは、例えば不純物が添加され導電性を有するシリコン層である。そのブロックに隣接する別のブロックにおける最上層の導電層WL1上には図示しない絶縁層を介してソース側選択ゲートSSGが設けられている。ソース側選択ゲートSSGは、例えば不純物が添加され導電性を有するシリコン層である。

【0014】

ソース側選択ゲートSSG上には図示しない絶縁層を介してソース線SLが設けられている。ソース線SLは、例えば不純物が添加され導電性を有するシリコン層である。あるいは、ソース線SLとして金属材料を用いてもよい。ソース線SL及びドレイン側選択ゲートDSG上には、図示しない絶縁層を介して複数本のビット線BLが設けられている。各ビット線BLは、Y方向に延在している。

【0015】

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基板 10 上の前述した積層体には、U 字状のメモリホールが複数形成されている。ドレイン側選択ゲート DSG を含むブロックには、ドレイン側選択ゲート DSG 及びその下の導電層 WL1 ~ WL4 を貫通し Z 方向に延在するメモリホールが形成され、ソース側選択ゲート SSG を含むブロックには、ソース側選択ゲート SSG 及びその下の導電層 WL1 ~ WL4 を貫通し Z 方向に延在するメモリホールが形成されている。それら両メモリホールは、バックゲート BG 内に形成され Y 方向に延在するメモリホールを介してつながっている。

【0016】

メモリホールの内部には、U 字状の半導体層としてシリコンボディ 20 が設けられている。ドレイン側選択ゲート DSG とシリコンボディ 20 との間のメモリホールの内壁には、ゲート絶縁膜 35 が形成されている。ソース側選択ゲート SSG とシリコンボディ 20 との間のメモリホールの内壁には、ゲート絶縁膜 36 が形成されている。各導電層 WL1 ~ WL4 とシリコンボディ 20 との間のメモリホールの内壁には、絶縁膜 30 が形成されている。バックゲート BG とシリコンボディ 20 との間のメモリホールの内壁にも、絶縁膜 30 が形成されている。絶縁膜 30 は、例えば一对のシリコン酸化膜でシリコン窒化膜を挟んだ ONO (Oxide-Nitride-Oxide) 構造を有する。

【0017】

図 2 は、シリコンボディ 20 が導電層 WL1 ~ WL4 及び層間の絶縁層 25 を貫通する部分の拡大断面を示す。

【0018】

導電層 WL1 ~ WL4 とシリコンボディ 20 との間には、導電層 WL1 ~ WL4 側から順に第 1 の絶縁膜 31、電荷蓄積層 32 及び第 2 の絶縁膜 33 が設けられている。第 1 の絶縁膜 31 は導電層 WL1 ~ WL4 に接し、第 2 の絶縁膜 33 はシリコンボディ 20 に接し、第 1 の絶縁膜 31 と第 2 の絶縁膜 33 との間に電荷蓄積層 32 が設けられている。

【0019】

シリコンボディ 20 はチャネルとして機能し、導電層 WL1 ~ WL4 はコントロールゲートとして機能し、電荷蓄積層 32 はシリコンボディ 20 から注入される電荷を蓄積するデータ記憶層として機能する。すなわち、シリコンボディ 20 と各導電層 WL1 ~ WL4 との交差部分に、チャネルの周囲をコントロールゲートが囲んだ構造のメモリセルが形成されている。

【0020】

本実施形態に係る半導体装置は、データの消去・書き込みを電氣的に自由に行うことができ、電源を切っても記憶内容を保持することができる不揮発性半導体記憶装置である。例えば、メモリセルはチャージトラップ構造のメモリセルである。電荷蓄積層 32 は、電荷（電子）を閉じこめるトラップを多数有し、例えばシリコン窒化膜からなる。第 2 の絶縁膜 33 は、例えばシリコン酸化膜からなり、電荷蓄積層 32 にシリコンボディ 20 から電荷が注入される際、または電荷蓄積層 32 に蓄積された電荷がシリコンボディ 20 へ拡散する際に電位障壁となる。第 1 の絶縁膜 31 は、例えばシリコン酸化膜からなり、電荷蓄積層 32 に蓄積された電荷が、導電層 WL1 ~ WL4 へ拡散するのを防止する。

【0021】

再び図 1 を参照すると、ドレイン側選択ゲート DSG を貫通するシリコンボディ 20 とドレイン側選択ゲート DSG との間にはゲート絶縁膜 35 が設けられ、これらはドレイン側選択トランジスタ DST を構成する。シリコンボディ 20 におけるドレイン側選択ゲート DSG より上方に突出する上端部は、対応する各ビット線 BL に接続されている。

【0022】

ソース側選択ゲート SSG を貫通するシリコンボディ 20 とソース側選択ゲート SSG との間にはゲート絶縁膜 36 が設けられ、これらはソース側選択トランジスタ SST を構成する。シリコンボディ 20 におけるソース側選択ゲート SSG より上方に突出する上端部は、ソース線 SL に接続されている。

【0023】

バックゲートBG、このバックゲートBG内に設けられたシリコンボディ20及びバックゲートBGとシリコンボディ20との間の絶縁膜30は、バックゲートトランジスタBGTを構成する。

【0024】

ドレイン側選択トランジスタDSTとバックゲートトランジスタBGTとの間には、導電層WL1をコントロールゲートとするメモリセルMC1と、導電層WL2をコントロールゲートとするメモリセルMC2と、導電層WL3をコントロールゲートとするメモリセルMC3と、導電層WL4をコントロールゲートとするメモリセルMC4が設けられている。

【0025】

バックゲートトランジスタBGTとソース側選択トランジスタSSTの間には、導電層WL4をコントロールゲートとするメモリセルMC5と、導電層WL3をコントロールゲートとするメモリセルMC6と、導電層WL2をコントロールゲートとするメモリセルMC7と、導電層WL1をコントロールゲートとするメモリセルMC8が設けられている。

【0026】

ドレイン側選択トランジスタDST、メモリセルMC1～MC4、バックゲートトランジスタBGT、メモリセルMC5～MC8およびソース側選択トランジスタSSTは、直列接続され、1つのメモリストリングを構成する。このようなメモリストリングがX方向及びY方向に複数配列されていることにより、複数のメモリセルMC1～MC8がX方向、Y方向及びZ方向に3次的に設けられている。

【0027】

次に、図3は、各導電層WL1～WL4を、図示しない上層配線と接続させるためのコンタクト領域の断面構造を示す。このコンタクト領域は、図1に示すメモリセルアレイ領域よりもX方向に見て外側の領域である。図3では、図1では省略した層間の絶縁層を絶縁層25として示している。

【0028】

前述した積層体の一部はコンタクト領域で階段状に加工されている。すなわち、下層の導電層ほどX方向の長さが長くされている。

【0029】

この階段構造部はストッパー層42で覆われ、そのストッパー層42上に層間絶縁層43が設けられている。例えば、ストッパー層42はシリコン窒化物であり、層間絶縁層43はシリコン酸化物である。

【0030】

層間絶縁層43及びストッパー層42には複数のコンタクトホール61～64が形成されている。それぞれのコンタクトホール61～64は、階段状に加工された各段の対応する導電層WL1～WL4に達している。

【0031】

各コンタクトホール61～64内にはコンタクト電極60が設けられている。コンタクト電極60としては、例えばチタン、窒化チタンなどの密着性に優れたバリアメタルと、タンゲステン、銅、ルテニウムなどの埋め込み性に優れた金属との組み合わせを用いることができる。バリアメタルは各コンタクトホール61～64の内壁に形成され、その内側にタンゲステンなどが埋め込まれる。各導電層WL1～WL4は、コンタクト電極60を介して、図示しない上層の配線と接続される。

【0032】

コンタクトホール61は、層間絶縁層43、ストッパー層42及びその下の絶縁層25を貫通して導電層WL1に達する。コンタクトホール61の孔径は深さ方向でほぼ一定である。あるいは、コンタクトホール61は、上端部から底部にかけて徐々に孔径が縮小していく逆円錐台状に形成されていてもよい。

【0033】

コンタクトホール62は、層間絶縁層43、ストッパー層42及びその下の絶縁層25

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を貫通して導電層WL2に達する。コンタクトホール62は、深さ方向の途中で段が形成され、底部の孔径よりも上端部の孔径の方が大きい。

【0034】

コンタクトホール63は、層間絶縁層43、ストッパー層42及びその下の絶縁層25を貫通して導電層WL3に達する。コンタクトホール63は、深さ方向の途中で段が形成され、底部の孔径よりも上端部の孔径の方が大きい。

【0035】

コンタクトホール64は、層間絶縁層43、ストッパー層42及びその下の絶縁層25を貫通して導電層WL4に達する。コンタクトホール64は、深さ方向の途中で段が形成され、底部の孔径よりも上端部の孔径の方が大きい。

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【0036】

層間絶縁層43の上面は平坦化され、その上面からの各コンタクトホール61～64の深さは異なる。より下層（下段）の導電層に達するコンタクトホールほど深くなっている。すなわち、導電層WL1に達するコンタクトホール61よりも導電層WL2に達するコンタクトホール62の方が深く、このコンタクトホール62よりも導電層WL3に達するコンタクトホール63の方が深く、このコンタクトホール63よりも導電層WL4に達するコンタクトホール64の方が深い。

【0037】

各コンタクトホール61～64の底部の孔径は略同じである。また、深いコンタクトホールほど、上端部の孔径が大きい。すなわち、コンタクトホール61よりもコンタクトホール62の方が上端部の孔径が大きく、コンタクトホール62よりもコンタクトホール63の方が上端部の孔径が大きく、コンタクトホール63よりもコンタクトホール64の方が上端部の孔径が大きい。

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【0038】

次に、本実施形態に係る半導体装置における階段状コンタクト構造部の形成方法を、図4～図10を参照して説明する。

【0039】

まず、図4（a）に示す積層体を形成する。例えば、CVD（chemical vapor deposition）法により、図1に示すバックゲートBG上に、絶縁層25と導電層WL1～WL4とを交互に形成する。

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【0040】

この積層体の形成後、メモリセルアレイ領域の積層体に対しては図1に例示したメモリセルアレイが形成される。メモリセルアレイ領域の外側の階段状コンタクト領域の積層体に対しては、図4（b）に示すように階段状の加工が行われる。具体的には、最上層の絶縁層25上に形成した図示しないレジスト膜の平面サイズを縮小するスリミング工程と、そのレジスト膜をマスクにしてそれぞれ一層分の絶縁層25及び導電層をエッチングする工程とを複数回繰り返す。階段構造部の各段の導電層WL1～WL4上には絶縁層25が残される。

【0041】

階段構造部の形成後、図5（a）に示すように、階段構造部を覆うストッパー層42を形成する。ストッパー層42は例えばシリコン窒化物からなる。ストッパー層42の形成後、その上に層間絶縁層43を形成し、平坦化する。層間絶縁層43は例えばシリコン酸化物からなる。

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【0042】

次に、図5（b）に示すように、層間絶縁層43上に第1のマスク材44を形成し、さらに第1のマスク材44上に第2のマスク材45を形成する。例えば、第1のマスク材44は有機膜であり、第2のマスク材45はシリコン酸化膜である。

【0043】

第2のマスク材45上にはレジスト膜46が形成される。レジスト膜46はパターンニングされ、複数の開口51～54が形成される。複数の開口51～54は、開口径がそれぞれ

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れ異なる。上段側の導電層上に位置する開口に比べて、下段側の導電層上に位置する開口の方が開口径が大きくなっている。例えば、最上段の導電層WL 1上に形成された開口5 1の開口径を2 aとすると、上から2段目の導電層WL 2上に形成された開口5 2の開口径は、開口5 1の開口径の2倍の4 aにしている。上から3段目の導電層WL 3上に形成された開口5 3の開口径は、開口5 1の開口径の3倍の6 aにしている。上から4段目の導電層WL 4上に形成された開口5 4の開口径は、開口5 1の開口径の4倍の8 aにしている。

【0044】

次に、レジスト膜4 6をマスクにして、図6 (a)に示すように、第2のマスク材4 5及び第1のマスク材4 4を、層間絶縁層4 3が露出するまで、例えばRIE (Reactive Ion Etching) 法でエッチングする。レジスト膜4 6の開口5 1の下には、その開口5 1の開口径2 aと略同じ孔径のホール5 5が形成される。レジスト膜4 6の開口5 2の下には、その開口5 2の開口径4 aと略同じ孔径のホール5 6が形成される。レジスト膜4 6の開口5 3の下には、その開口5 3の開口径6 aと略同じ孔径のホール5 7が形成される。レジスト膜4 6の開口5 4の下には、その開口5 4の開口径8 aと略同じ孔径のホール5 8が形成される。またこのとき、第1のマスク材4 4と同じ有機物系のレジスト膜4 6は消費され除去される。

【0045】

次に、第1のマスク材4 4及び第2のマスク材4 5をマスクにして、図6 (b)に示すように、層間絶縁層4 3を例えばRIE法でエッチングする。このとき、層間絶縁層4 3と同じシリコン酸化物系の第2のマスク材4 5は消費され、除去される。

【0046】

ホール5 5の下の層間絶縁層4 3にはホール5 5の孔径と略同じ孔径のコンタクトホール6 1が形成され、ホール5 6の下の層間絶縁層4 3にはホール5 6の孔径と略同じ孔径のコンタクトホール6 2が形成され、ホール5 7の下の層間絶縁層4 3にはホール5 7の孔径と略同じ孔径のコンタクトホール6 3が形成され、ホール5 8の下の層間絶縁層4 3にはホール5 8の孔径と略同じ孔径のコンタクトホール6 4が形成される。したがって、コンタクトホール6 1の上端部の孔径は2 a、コンタクトホール6 2の上端部の孔径は4 a、コンタクトホール6 3の上端部の孔径は6 a、コンタクトホール6 4の上端部の孔径は8 aとなる。

【0047】

このときのエッチングは、最上段の導電層WL 1上に形成されるコンタクトホール6 1の底部が、ストッパー層4 2に達するまで行われる。下段側の他のコンタクトホール6 2～6 4の底部は層間絶縁層4 3中にとどまる。

【0048】

層間絶縁層4 3のエッチングでは、シリコン窒化物系のストッパー層4 2に対してシリコン酸化物系の層間絶縁層4 3の方がエッチングレートが高くなるように組成等が調整された例えばフルオロカーボンを含むガスが用いられる。また、後述するストッパー層4 2のエッチングでは、シリコン酸化物系の絶縁層2 5に対してシリコン窒化物系のストッパー層4 2の方がエッチングレートが高くなるように組成等が調整された例えばフルオロカーボンを含むガスが用いられる。

【0049】

次に、図7 (a)に示すように、犠牲膜8 0を形成する。犠牲膜8 0は、第1のマスク材4 4の上面と各コンタクトホール6 1～6 4の内壁(側壁及び底部)に形成される。このとき犠牲膜8 0の膜厚が等方的に例えばaとなるように制御する。最も孔径の小さいコンタクトホール6 1の孔径は2 aであり、よって対向する側壁間の距離が2 aである。このため、コンタクトホール6 1の側壁に膜厚aの犠牲膜8 0が形成されることで、コンタクトホール6 1内は犠牲膜8 0で埋められる。

【0050】

他のコンタクトホール6 2～6 4の側壁にも膜厚aの犠牲膜8 0が形成される。したが

って、犠牲膜 80 が形成される前の状態で孔径が 4 a であったコンタクトホール 62 においては、側壁に形成された犠牲膜 80 の内側の孔径が 2 a になる。犠牲膜 80 が形成される前の状態で孔径が 6 a であったコンタクトホール 63 においては、側壁に形成された犠牲膜 80 の内側の孔径が 4 a になる。犠牲膜 80 が形成される前の状態で孔径が 8 a であったコンタクトホール 64 においては、側壁に形成された犠牲膜 80 の内側の孔径が 6 a になる。

【0051】

犠牲膜 80 は、例えばフロロカーボンなどの炭素とフッ素を含む膜である。これは、例えば CF_4 、 CH_4 、 CH_2F_2 、 H_2 などの原料ガスを用いた CVD 法で形成される。

【0052】

次に、RIE 法によるエッチングを行う。これにより、図 7 (b) に示すように、第 1 のマスク材 44 の上面及びコンタクトホール 62～64 の底部の犠牲膜 80 が除去される。さらに、犠牲膜 80 が除去されたコンタクトホール 62～64 の底部に対してエッチングを続け、その下方の層間絶縁層 43 をエッチングする。このとき、各コンタクトホール 62～64 の側壁に形成された犠牲膜 80 がマスクとなり、追加エッチングによって得られた各コンタクトホール 62～64 の底部の孔径はそれぞれ 2 a、4 a、6 a となる。

【0053】

このときのエッチングは、コンタクトホール 62 の底部が、ストッパー層 42 に達するまで行われる。下段側の他のコンタクトホール 63、64 の底部は層間絶縁層 43 中にとどまる。

【0054】

このエッチング前にコンタクトホール 61 内は犠牲膜 80 で埋められ、全体がマスクされているため、底部の深さ方向の位置及び孔径が変動しない。すなわち、コンタクトホール 61 の底部の孔径は 2 a に維持される。また、側壁に形成された犠牲膜 80 をマスクとした上記追加エッチングによりストッパー層 42 に達したコンタクトホール 62 の底部の孔径も 2 a となる。

【0055】

以降、前述したような犠牲膜 80 の形成とエッチングとを繰り返す。

【0056】

すなわち、図 8 (a) に示すように、再び、第 1 のマスク材 44 上およびまだ犠牲膜 80 で埋まっていないコンタクトホール 62～64 内に追加の犠牲膜 80 を形成する。このときも犠牲膜 80 の膜厚を等方的に例えば a となるように制御する。これにより、1 回目の犠牲膜 80 の形成により孔径が 2 a に狭められたコンタクトホール 62 内が犠牲膜 80 で埋まる。

【0057】

この 2 回目の犠牲膜 80 が形成される前の状態で孔径が 4 a であったコンタクトホール 63 においては、側壁に形成された犠牲膜 80 の内側の孔径が 2 a になる。2 回目の犠牲膜 80 が形成される前の状態で孔径が 6 a であったコンタクトホール 64 においては、側壁に形成された犠牲膜 80 の内側の孔径が 4 a になる。

【0058】

次に、RIE 法によるエッチングを行う。これにより、図 8 (b) に示すように、第 1 のマスク材 44 の上面及びコンタクトホール 63、64 の底部の犠牲膜 80 が除去される。さらに、犠牲膜 80 が除去されたコンタクトホール 63、64 の底部に対してエッチングを続け、その下方の層間絶縁層 43 をエッチングする。このとき、各コンタクトホール 63、64 の側壁に形成された犠牲膜 80 がマスクとなり、このときの追加エッチングによって得られた各コンタクトホール 63、64 の底部の孔径はそれぞれ 2 a、4 a となる。

【0059】

このときのエッチングは、コンタクトホール 63 の底部が、ストッパー層 42 に達するまで行われる。残りのコンタクトホール 64 の底部は層間絶縁層 43 中にとどまる。

【0060】

このときのエッチング前にコンタクトホール61、62内は犠牲膜80で埋められ、全体がマスクされているため、底部の深さ方向の位置及び孔径が変動しない。すなわち、コンタクトホール61、62の底部の孔径は2aに維持される。また、側壁に形成された犠牲膜80をマスクとしたこのときの追加エッチングによりストッパー層42に達したコンタクトホール63の底部の孔径は2aとなる。

【0061】

次に、図9(a)に示すように、再び、第1のマスク材44上およびまだ犠牲膜80で埋まっていないコンタクトホール63、64内に追加の犠牲膜80を形成する。このときも犠牲膜80の膜厚を等方的に例えばaとなるように制御する。これにより、前回(2回目)の犠牲膜80の形成により孔径が2aに狭められたコンタクトホール63内が犠牲膜80で埋まる。

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【0062】

この3回目の犠牲膜80が形成される前の状態で孔径が4aであったコンタクトホール64においては、側壁に形成された犠牲膜80の内側の孔径が2aになる。

【0063】

次に、RIE法によるエッチングを行う。これにより、図9(b)に示すように、第1のマスク材44の上面及びコンタクトホール64の底部の犠牲膜80が除去される。さらに、犠牲膜80が除去されたコンタクトホール64の底部に対してエッチングを続け、その下方の層間絶縁層43をエッチングする。このとき、コンタクトホール64の側壁に形成された犠牲膜80がマスクとなり、このときの追加エッチングによって得られたコンタクトホール64の底部の孔径は2aとなる。このときのエッチングは、コンタクトホール64の底部がストッパー層42に達するまで行われる。

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【0064】

このときのエッチング前にコンタクトホール61～63内は犠牲膜80で埋められ、全体がマスクされているため、底部の深さ方向の位置及び孔径が変動しない。すなわち、コンタクトホール61～63の底部の孔径は2aに維持される。そして、側壁に形成された犠牲膜80をマスクとしたこのときの追加エッチングによりストッパー層42に達したコンタクトホール64の底部の孔径は2aとなる。したがって、この時点(底部がストッパー層42に達した状態)で、すべてのコンタクトホール61～64の底部の孔径は略同じにそろえられることになる。

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【0065】

次に、図10(a)に示すように、すべてのコンタクトホール61～64内から、例えばドライエッチングにより犠牲膜80を除去する。

【0066】

次に、各コンタクトホール61～64の底部の下ストッパー層42及びそのストッパー層42の下絶縁層25をRIE法でエッチングし、除去する。これにより、図10(b)に示すように、コンタクトホール61の底部に最上段の導電層WL1が露出し、コンタクトホール62の底部に上から2段目の導電層WL2が露出し、コンタクトホール63の底部に上から3段目の導電層WL3が露出し、コンタクトホール64の底部に上から4

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【0067】

以上説明した、第1のマスク材44のエッチング、層間絶縁層43のエッチング、犠牲膜80の形成、犠牲膜80のエッチング、層間絶縁層43の追加エッチング、・・・、犠牲膜80の除去、ストッパー層42のエッチング、絶縁層25のエッチング、という一連の工程は、ガス種、投入電力等の条件を切り替えつつ、所望の減圧雰囲気維持された同一チャンバー内で続けて行われる。処理内容ごとに、複数のチャンバー間で被処理体の移動及び搬出入を行う必要がなく効率的である。

【0068】

その後、酸素ガス等を用いたエッチングにより第1のマスク材44を除去した後、コン

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タクト電極形成前の前処理として、フッ化水素酸、硫化水素などを用いた薬液処理を行い、コンタクトホール61～64底部の自然酸化膜、R I E後の残留物、大気搬送中に付く汚染物質などをコンタクトホール61～64内から取り除く。

【0069】

次に、バリアメタル（例えばチタンと窒化チタン）をC V D法によりコンタクトホール61～64の内壁（側壁及び底部）に形成した後、熱処理を行い、各コンタクトホール61～64の底部の各導電層W L 1～W L 4をチタンシリサイド化させる。この後、バリアメタルの内側に、C V D法により例えばタングステンを埋め込み、図3に示すように、各コンタクトホール61～64内にコンタクト電極60を設ける。

【0070】

本実施形態によれば、深さの異なる複数のコンタクトホール61～64の底部の孔径を略同じにそろえることができる。これは、前述したように、各コンタクトホール61～64を形成するためのマスクの開口径と、犠牲膜80の膜厚とを適切に制御することで実現される。

【0071】

犠牲膜80を形成する前の段階ですでに所望の孔径とされたコンタクトホール61に対しては、1回目の犠牲膜80の形成時に犠牲膜80で埋めてしまう。1回目の犠牲膜80の形成では内部が犠牲膜80で埋め込まれないコンタクトホール62～64に対しては、2回目以降の犠牲膜80の形成工程で、側壁に犠牲膜80を形成して所望の孔径にする。その状態で下方へのエッチングを行うことで底部の犠牲膜80を除去すると共に底部の孔径を所望の孔径にすることができる。そして、底部が所望の孔径になったコンタクトホールに対しては犠牲膜80を埋め込んで、他のコンタクトホールの追加エッチング時にそれ以上加工が行われないようにする。

【0072】

各コンタクトホール61～64の底部の孔径が略同じということは、各段の導電層W L 1～W L 4と、各コンタクト電極60との接触面積、すなわち接触抵抗のばらつきを抑制できる。この結果、階層の異なるメモリセル間での特性ばらつきを抑制することができる。

【0073】

さらに、本実施形態によれば、深さの深いコンタクトホールほど、その上端部の孔径が大きいため、コンタクト電極60を埋め込みやすく、深さの深いコンタクトホールであっても空隙を生じさせることなく底部まで確実にコンタクト電極60を埋め込むことができる。

【0074】

また、深さの深いコンタクトホールは浅いコンタクトホールに比べて、各導電層と上層配線との間の経路が長くなるが、本実施形態では、深さの深いコンタクトホールは浅いコンタクトホールよりも上端部側が太くなっているため、深いコンタクトホール側での抵抗増大を抑えることができる。

【0075】

前述した実施形態では、各コンタクトホール61～64は1段階深くなるごとに上端部の孔径が逐次大きくされているが、上端部の孔径の変化は深さの変化に合わせた逐次的でなくてもよい。

【0076】

例えば、図11（a）に示すように、導電層W L 1に達するコンタクトホール61と導電層W L 2に達するコンタクトホール62とで上端部の孔径が同じであってもよい。あるいは、図11（b）に示すように、導電層W L 2に達するコンタクトホール62と導電層W L 3に達するコンタクトホール63とで上端部の孔径が同じであってもよい。あるいは、導電層W L 3に達するコンタクトホール63と導電層W L 4に達するコンタクトホール64とで上端部の孔径が同じであってもよい。

【0077】

例えば図 1 1 (a) の構造の場合、図 5 (b) の工程におけるレジスト膜 4 6 の開口 5 2 の開口径を開口 5 1 と同じ 2 a にし、開口 5 3 の開口径を 4 a にし、開口 5 4 の開口径を 6 a にして、上記実施形態と同様に図 6 (b) まで工程を進めていく。そして、図 6 (b) に対応する工程で、コンタクトホール 6 1 に続いてコンタクトホール 6 2 の底部がストッパー層 4 2 に達した時点で、層間絶縁層 4 3 に対する 1 回目のエッチングを停止し、1 回目の犠牲膜 8 0 の形成を行う。このとき、コンタクトホール 6 1、6 2 内は犠牲膜 8 0 で埋められる。以降、上記実施形態と同様に工程が進められていく。

【0078】

以上、具体例を参照しつつ本発明の実施形態について説明した。しかし、本発明は、それらに限定されるものではなく、本発明の技術的思想に基づいて種々の変形が可能である。

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【0079】

メモリストリングの構成は U 字状に限らず、図 1 2 に示すように I 字状であってもよい。図 1 2 には導電部分のみを示し、絶縁部分の図示は省略している。この構造では、基板 1 0 上にソース線 S L が設けられ、その上にソース側選択ゲート（または下部選択ゲート）S S G が設けられ、その上に導電層 W L 1 ~ W L 4 が設けられ、最上層の導電層 W L 1 とビット線 B L との間にドレイン側選択ゲート（または上部選択ゲート）D S G が設けられている。

【0080】

また、導電層 W L 1 ~ W L 4 とシリコンボディ 2 0 との間の絶縁膜構造は O N O (Oxid e-Nitride-Oxide) 構造に限らず、例えば電荷蓄積層とゲート絶縁膜との 2 層構造であってもよい。

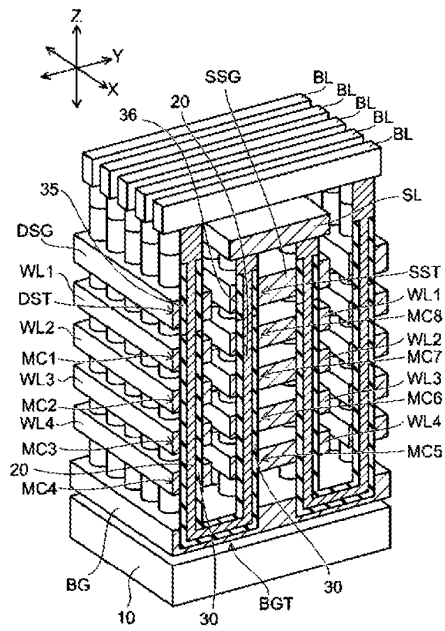
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【符号の説明】

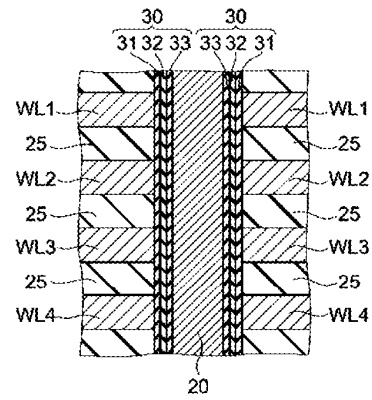
【0081】

2 0 …シリコンボディ、2 5 …絶縁層、3 2 …電荷蓄積層、4 2 …ストッパー層、4 3 …層間絶縁層、6 0 …コンタクト電極、6 1 ~ 6 4 …コンタクトホール、8 0 …犠牲膜、W L 1 ~ W L 4 …導電層

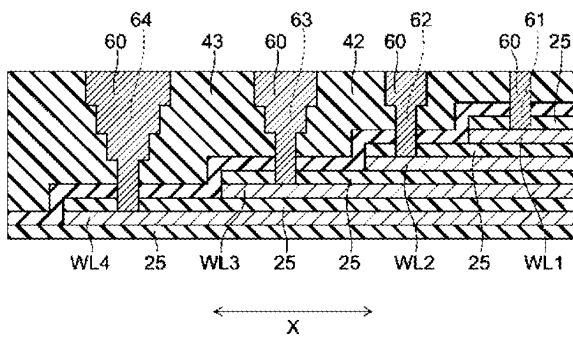
【 図 1 】



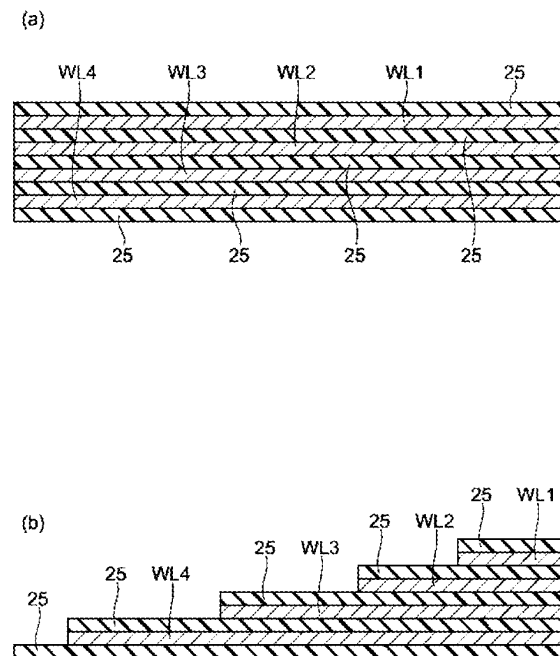
【图 2】



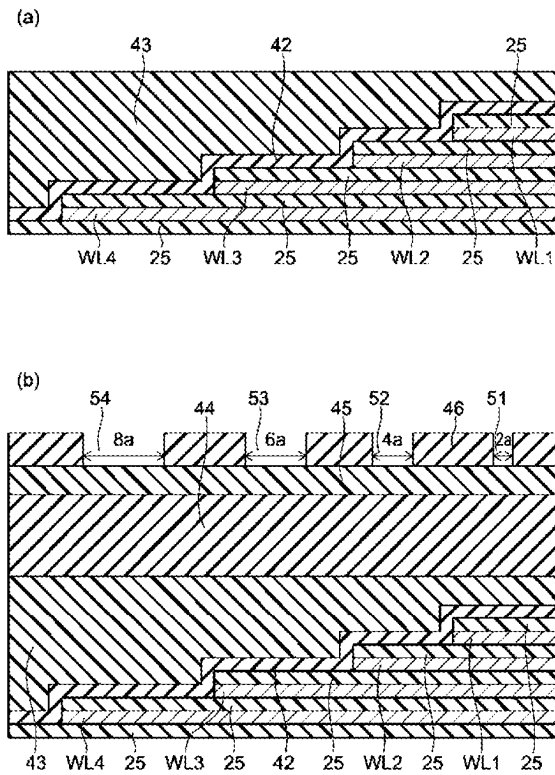
【 3 】



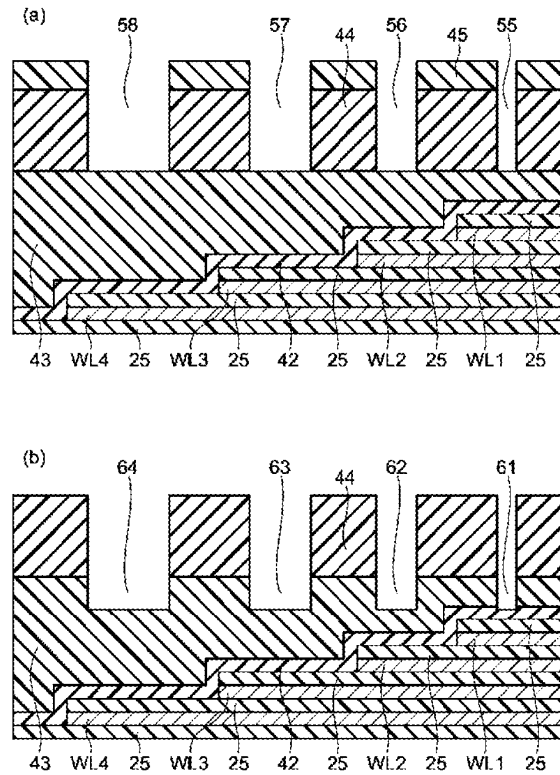
【 例 4 】



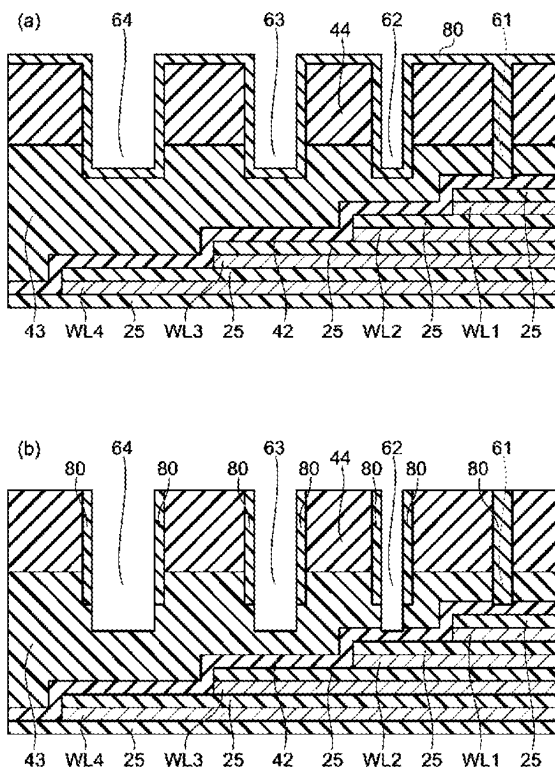
【図 5】



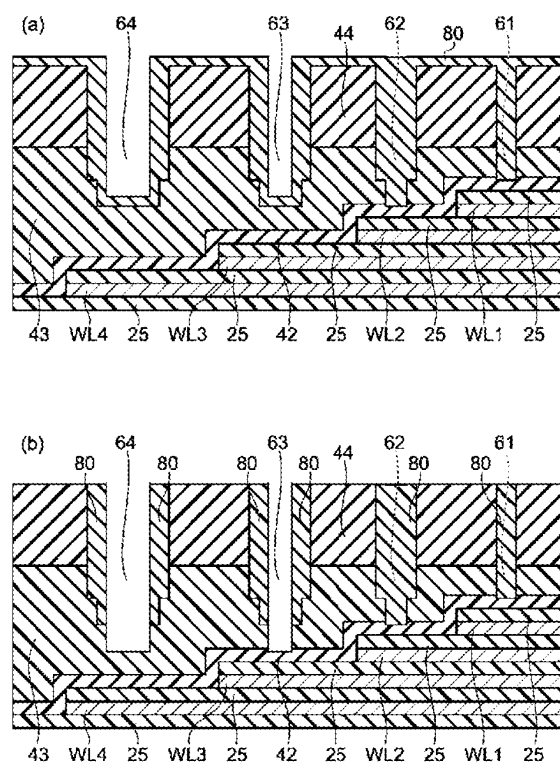
【図 6】



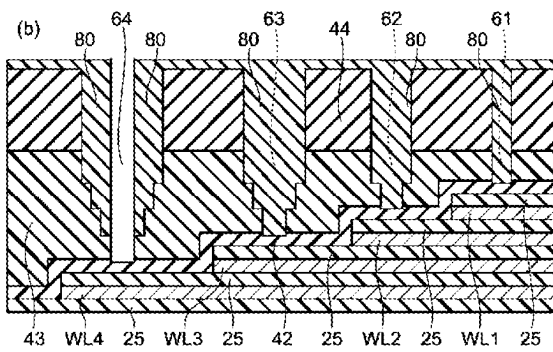
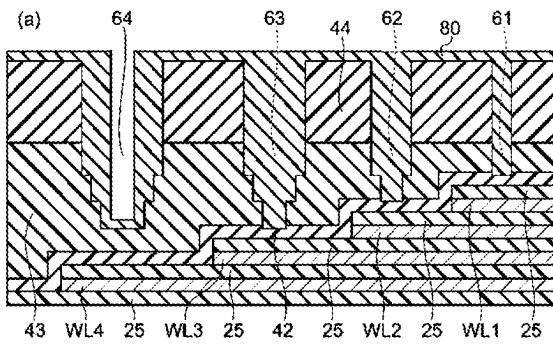
【図 7】



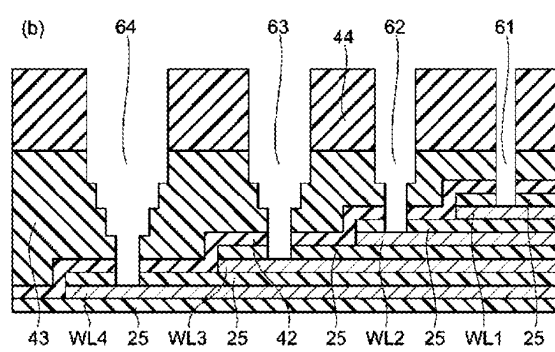
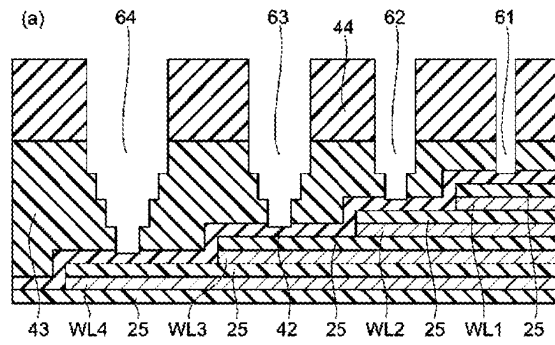
【図 8】



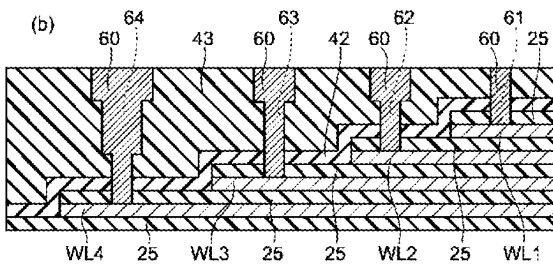
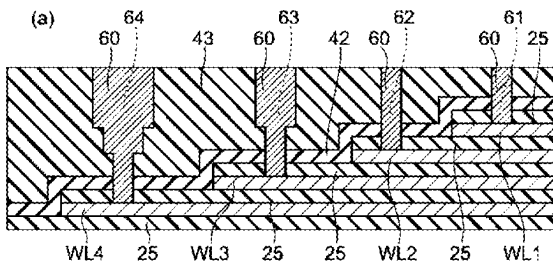
【図 9】



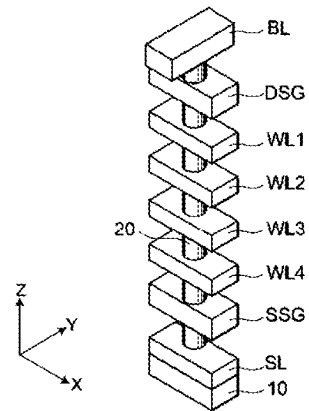
【図 10】



【図 11】



【図 12】



フロントページの続き

F ターム(参考) 5F083 EP18 EP22 EP30 EP33 EP34 EP48 EP49 EP76 GA10 GA27
JA04 JA35 JA37 JA38 JA39 JA40 JA53 KA01 KA05 KA11
LA12 LA16 LA20 MA05 MA06 MA16 PR03 PR06 PR07 PR10
5F101 BA45 BB02 BB08 BD16 BD21 BD22 BD30 BD34 BH14 BH23

Docket No. 534753US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yali SONG, et al.

SERIAL NO: 17/154,054

GAU: 2825

FILED: January 21, 2021

EXAMINER: BERMUDEZ LOZADA,
ALFREDO

FOR: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the reference(s) listed on the attached form PTO-1449 and/or accompanying documents from a corresponding foreign application. Copies of the listed reference(s) are attached, where required, as are either statements of relevancy, English translations of the categories of cited documents for foreign search reports or English translations of foreign Office Actions which provide the statement of relevancy for the foreign language references cited therein, or any readily available partial or full English translations of pertinent portions of any non-English language reference(s).
- ☒ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☐ Please charge any additional fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to deposit account number **15-0030**.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

/John S. Kern/

John S. Kern

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22850

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(OMMN 02/12)



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569
22850	7590	07/12/2022		
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER BERMUDEZ LOZADA, ALFREDO	
			ART UNIT	PAPER NUMBER
			2825	
			NOTIFICATION DATE	DELIVERY MODE
			07/12/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OBLONPAT@OBLON.COM
iahmadi@oblon.com
patentdocket@oblon.com

Supplemental Notice of Allowability	Application No. 17/154,054	Applicant(s) SONG et al.	
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the IDS of 06/28/2022.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-14 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 06/28/2022. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	--

DETAILED ACTION

Notice of AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This action supplements the Notice of Allowance mailed June 14, 2022 to consider the new Information Disclosure Statement of June 28, 2022.

Claims 1-14 are pending. Claim 1 is independent.

Information Disclosure Statement

Acknowledgment is made of applicant's Information Disclosure Statement (IDS) filed on June 28, 2022. This IDS has been considered.

Allowable Subject Matter

Claims 1-14 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to independent claim 1, there is no teaching or suggestion in the prior art of record to provide the recited first dielectric trenches extending in a height direction of the substrate through the BSG to separate the BSG into a plurality of sub-BSG and partially through the stack, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALFREDO BERMUDEZ LOZADA whose telephone number is (571)272-0877. The examiner can normally be reached 7:00AM-3:30PM EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander G Sofocleous can be reached on 571-272-0635. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alfredo Bermudez Lozada/
Primary Examiner, Art Unit 2825

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

CPC						
Symbol					Type	Version
H01L	/	27	/	11582	F	2013-01-01
G11C	/	16	/	0483	I	2013-01-01
G11C	/	16	/	14	I	2013-01-01
H01L	/	21	/	31116	I	2013-01-01
H01L	/	23	/	528	I	2013-01-01
H01L	/	27	/	11565	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	29	/	0847	I	2013-01-01
H01L	/	29	/	1037	I	2013-01-01
H01L	/	21	/	0276	A	2013-01-01
H01L	/	21	/	31144	A	2013-01-01

CPC Combination Sets					
Symbol	Type	Set	Ranking	Version	
/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	08 July 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220708

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G11C	/	16	/ 04
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
365	185.17

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	08 July 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220708

Issue Classification 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	4	10												
2	2	6	11												
3	3	14	12												
7	4	12	13												
8	5	5	14												
9	6														
13	7														
10	8														
11	9														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	08 July 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1A

U.S. Patent and Trademark Office

Part of Paper No.: 20220708

<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

CPC - Searched*		
Symbol	Date	Examiner
G11C16/0483, G11C16/14, H01L23/528, H01L27/11565, H01L27/1157, H01L27/11556, H01L27/11551	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	185.17	12/30/2021	ABL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

Search Notes		
Search Notes	Date	Examiner
East search, Prior art search, Inventor name search	06/15/2021	GA
Updated search	09/30/2021	GA
H01L 27/11582	12/30/2021	ABL
H01L 27/11565	12/30/2021	ABL
H01L 27/11568	12/30/2021	ABL
H01L 27/11567	12/30/2021	ABL
H01L 27/1157	12/30/2021	ABL
G11C 16/0483	12/30/2021	ABL
PE2E Search all databases	12/30/2021	ABL
IP.com	12/30/2021	ABL
Consulted with Alex Sofocleous (SPE)	12/30/2021	ABL
Inventor and Assignee searched	12/30/2021	ABL
search updated	04/19/2022	ABL
search updated	05/09/2022	ABL
New IDS considered	05/09/2022	ABL
New IDS considered	06/08/2022	ABL
New IDS considered	07/08/2022	ABL

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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<i>Search Notes</i> 	Application/Control No. 17/154,054	Applicant(s)/Patent Under Reexamination SONG et al.
	Examiner ALFREDO BERMUDEZ LOZADA	Art Unit 2825

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
Interference search		09/30/2021	GA
G11C	16/14	04/19/2022	ABL
G11C	16/0483	04/19/2022	ABL
G11C	16/04	04/19/2022	ABL
365	185.17	04/19/2022	ABL
H01L	27/11582	04/19/2022	ABL

/Alfredo Bermudez Lozada/ Primary Examiner, Art Unit 2825	
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SHEET 1 OF 1

Form PTO 1449 (Modified)		INFORMATION DISCLOSURE STATEMENT		ATTY DOCKET NO. 534753US		SERIAL NO. 17/154,054	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Yali SONG, et al.			
				FILING DATE January 21, 2021		GROUP 2825	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,989,317 B1	01/24/2006	RADENS et al.			
	AB	2018/0286678 A1	10/04/2018	LEE			
	AC	2007/0287293 A1	12/13/2007	HAN et al.			
	AD	2015/0263029 A1	09/17/2015	KIM et al.			
	AE	10,141,372 B2	11/27/2018	PARK, J. et al.			
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO	108807404A	11/13/2018	China (with English Abstract)			x
	AP	2011-60958	03/24/2011	Japan (with English Abstract)			x
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Extended European Search Report dated April 28, 2022, issued in corresponding patent application no. 19914915.4 (citing documents AA-AD and AO-AP)					
	AX	Office Action dated May 23, 2022, issued in corresponding Indian Patent Application No. 202127020980 (citing document AE)					
	AY						
	AZ					☐ Additional References sheet(s) attached	
Examiner	/Alfredo Bermudez Lozada/ (07/08/2022)				Date considered	07/08/2022	
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ABL/

Micron Ex. 1015, p. 270
Micron v. YMTC
IPR2024-00794

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2	"20210143179"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2021/12/28 01:58 PM
L2	8	("10134747" OR "10141372" OR "20100320528" OR "20160233270" OR "20180337195" OR "20200185411" OR "20200227555" OR "20200335514").pn.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 05:40 AM
L3	3	"10650623"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:00 AM
L4	11	bsg AND csr AND tsg	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:04 AM
L5	17794	(3d OR three-dimension\$2 OR (three dimension\$2) OR 3-dimension\$2 OR vertical OR stack) near2 nand	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:35 AM
L6	44	staircase AND ((bottom select gate) OR bsg) AND ((top select gate) OR tsg) AND ((common source) OR csr)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L7	44	6 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 06:39 AM
L8	235	trench WITH (divid\$3 OR separat\$3 OR cut) WITH (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L9	105	8 AND 5	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 07:02 AM
L10	13760	5 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:33 AM
L11	1032	5 AND (stair OR step) AND ((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:34 AM
L12	129	((dielectric OR insulat\$3) near2 trench) WITH (select (gate OR	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:36 AM

L13	118	transistor)) 12 AND (stair OR step)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 08:37 AM
L14	3796	365/185.17.ccls.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:31 AM
L15	56814	((dielectric OR insulat\$3) near2 trench)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:32 AM
L16	57	15 AND 14	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:33 AM
L17	1	15 AND 14 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:36 AM
L18	16647	g11c16/0483.cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:42 AM
L19	345	18 AND 15	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L20	25	18 AND 15 AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:43 AM
L21	17953	(h01I27/11582,11565,1 1568,11567,1157).cpc.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:56 AM
L22	2190	15 AND 21	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L23	666	15 AND 21 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L24	49	15 AND 21 AND (common NEAR source) AND stair	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 09:57 AM
L25	6	(sub-ssg OR sub-sst OR sub-gst OR sub-gsg OR sub-bsg)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:10 AM
L26	1646	(multiple OR plurality) NEAR select NEAR gate	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:11 AM
L27	448	5 AND 26	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:15 AM
L28	286	5 AND 26 AND (common NEAR source)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 10:27 AM
L29	1	"20210295918"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:11 AM
L30	56	(divid\$3 OR separat\$3 OR cut) near2(plurality OR multiple) near2 (select gate)	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:35 AM
L31	2	"20140036590"	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/29 11:51 AM
L32	9	"10950623"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	ADJ	ON	ON	2021/12/30 05:42 AM

L33	790	yangtze.as.	EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2021/12/30 07:02 AM
L34	63353	song.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L35	29984	xiao.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L36	252871	wang.in.	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L37	4	33 AND 34 AND 35 AND 36	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:02 AM
L38	9	8 AND 33	(US-PGPUB; USPAT)	ADJ	ON	ON	2021/12/30 07:03 AM
L39	3	"20180240527"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/05/09 08:15 AM
L40	0	20170040061+	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/05/09 08:15 AM
L41	10	"20170040061"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/05/09 08:16 AM
L42	3	"20120273956"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	ADJ	ON	ON	2022/06/08 10:28 AM

L43	10	"20140035024"	CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:30 AM
L44	46	"10141372"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:31 AM
L45	8	"20180130814"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:32 AM
L46	10	"20140035024"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:33 AM
L47	3	"20120273965"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	ADJ	ON	ON	2022/06/08 10:33 AM

L48	5	"20140138765"	EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:34 AM
L49	3	"20180261618"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:35 AM
L50	3	"20170200676"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/06/08 10:36 AM
L51	11	"6989317"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/07/08 10:17 AM
L52	3	"20180286678"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	ADJ	ON	ON	2022/07/08 10:19 AM

L53	3	"20070287293"	HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/07/08 10:20 AM
L54	2	"20150263029"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/07/08 10:21 AM
L55	46	"10141372"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	ADJ	ON	ON	2022/07/08 10:23 AM

PE2E SEARCH - Search History (Interference)

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N1	2752	G11C16/04.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N2	17261	G11C16/0483.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N3	3863	G11C16/14.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N4	3796	365/185.17.CCLS.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:58 PM
N5	12813	H01L27/11582.CPC.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N6	0	N5 AND N4 AND N3 AND N2 AND N1	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM

07/08/2022 10:46:21 AM
Workspace: 17154054

Page 6 of 7
AB

N7	598	N1 AND N2	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N8	39	N1 AND N2 AND N3	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N9	2365	N4 AND (N1 OR N2 OR N3 OR N5)	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N10	2935	N5 AND (N1 OR N2 OR N3 OR N4)	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 02:59 PM
N11	1277	(bsg).clm.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N12	88549	(crs).clm.	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N13	0	N11 AND N12 AND N10	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N14	0	N11 AND N12 AND N9	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:00 PM
N15	0	N11 AND N12 AND N8	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:01 PM
N16	0	N11 AND N12 AND N7	(US-PGPUB; USPAT)	ADJ	ON	ON	2022/04/19 03:01 PM



UNITED STATES PATENT AND TRADEMARK OFFICE

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 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6569

SERIAL NUMBER 17/154,054	FILING or 371(c) DATE 01/21/2021 RULE	CLASS 365	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. 534753US	
APPLICANTS Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA INVENTORS Yali SONG, Wuhan, CHINA; Li Hong XIAO, Wuhan, CHINA; Ming WANG, Wuhan, CHINA; ** CONTINUING DATA ***** This application is a CON of 16/365,725 03/27/2019 PAT 10950623 which is a CON of PCT/CN2018/119908 12/07/2018 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/01/2021					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /ALFREDO BERMUDEZ LOZADA/ Acknowledged Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY CHINA	SHEETS DRAWINGS 20	TOTAL CLAIMS 14	INDEPENDENT CLAIMS 1
ADDRESS OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314 UNITED STATES					
TITLE NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT					
FILING FEE RECEIVED 1820	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22850 7590 04/26/2022
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	01/21/2021	Yali SONG	534753US	6569

TITLE OF INVENTION: NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	07/26/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
BERMUDEZ LOZADA, ALFREDO	2825	365-185170

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Oblon, McClelland,
2 Maier & Neustadt, L.L.P.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Yangtze Memory Technologies Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Wuhan, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

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5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
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NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Kevin L. Hartman/Date 7/26/2022Typed or printed name Kevin L. HartmanRegistration No. 72,359

Electronic Patent Application Fee Transmittal				
Application Number:		17154054		
Filing Date:		21-Jan-2021		
Title of Invention:		NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT		
First Named Inventor/Applicant Name:		Yali SONG		
Filer:		Philippe Jean-Claude Signore/Candice Kinard		
Attorney Docket Number:		534753US		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	46274915
Application Number:	17154054
International Application Number:	
Confirmation Number:	6569
Title of Invention:	NOVEL 3D NAND MEMORY DEVICE WITH SELECT GATE CUT
First Named Inventor/Applicant Name:	Yali SONG
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Candice Kinard
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	534753US
Receipt Date:	26-JUL-2022
Filing Date:	21-JAN-2021
Time Stamp:	15:41:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E20227PF42150925
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	534753US.pdf	1299206	no	1
			eedbbfeb1dd5dcf8099065156cef555a087e fdu8		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37728	no	2
			380cf8f40500d7fc1fdc116c5e47dbe46f77 c53		
Warnings:					
Information:					
Total Files Size (in bytes):			1336934		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/154,054	08/30/2022	11430811	534753US	6569

22850 7590 08/10/2022
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional inventors):

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IR103 (Rev. 10/09)

Micron Ex. 1015, p. 284
Micron v. YMT
IPR2024-00794