

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00794

Patent 10,950,623

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Cho et al., “A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single-Level Modes,” IEEE J. of Solid-State Circuits, Vol. 36, No. 11, November 2001.
Ex. 2002	Lee et al., “Applications of AFM in semiconductor R&D and manufacturing at 45 nm technology node and beyond,” Metrology, Inspection, and Process Control for Microlithography, Vol. 7272, SPIE, 2009.
Ex. 2003	Xiao et al., “A high speed low power negative sensing architecture for 3D NAND Flash memory,” 2016 China Semiconductor Technology International Conference (CSTIC), Shanghai, China, 2016.
Ex. 2004	Bergonzoni, et al., “Reset Current Scaling in Phase-Change Memory Cells: Modeling and Experiments,” IEEE Transactions on Electron Devices, Vol. 59, No. 2, 283-291, Feb. 2012.
Ex. 2005	Seshan et al., Handbook of Thin Film Deposition, Abstract, 2018.
Ex. 2006	Choi et al., “Novel ESD protection transistor including SiGe buried layer to reduce local temperature overheating,” IEEE Transactions on Electron Devices, Vol. 43, No. 3, 479-489, March 1996.
Ex. 2007	Declaration of Jonathan Bradford

LIST OF ABBREVIATIONS

Abbreviation	Term
'623	U.S. Patent No. 10,950,623 (Ex. 1001)
Challenged Claims	'623 patent, claims 1-11
Office	U.S. Patent and Trademark Office
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Park	U.S. Patent No. 9,299,718
Patent Owner or PO	Yangtze Memory Technologies Company, Ltd.
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,950,623 (IPR2024-00794, Paper 1)
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Shibata	U.S. Pub. 2019/0122734

I. INTRODUCTION

Pursuant to § 42.107,¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to any Challenged Claim.

U.S. Patent 10,950,623 ("’623," Ex. 1001) is directed to an improved three-dimensional memory device with a divided block structure that provides a novel approach to address issues associated with conventional architectural memory device designs. In conventional memory device architecture at the time of filing the ’623, "the vertical NAND memory cell strings of a same block" shared a bottom select gate (BSG). ’623, 1:50-52. The shared BSG simultaneously controlled all of the bottom select transistors (BSTs) of the vertical NAND memory cell strings in a block during operation of the memory device. ’623, 1:53-57. However, as 3D NAND flash memory technology architecture developed and the number of vertical layers and bit density increased, the shared BSG architecture slowed down device

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

reading and data transfer operations, which decreased storage efficiency. '623, 1:57-60.

The '623 introduced a novel 3D NAND memory device architecture that included dielectric trenches in the memory device to separate the BSG into a plurality of sub-BSGs. '623, 7:45-47. The sub-BSGs “divide the memory device ... into a plurality of sub-blocks,” and “each of the sub-blocks can be operated individually through controlling the respective sub-BSG.” '623, 7:47-53. This architecture enables each of the sub-blocks to be precisely controlled, and reduces device operation (*i.e.*, programming, reading, erasing) time, speeds up data transfer, and improves storage efficiency. '623, 7:53-58. Accordingly, the claimed memory device architecture of the '623 overcomes shortcomings of the prior art. This new architecture taught by the '623 and recited in the claims is characterized by several features not found in the prior art, including one or more dielectric trenches that (1) are formed in the BSG and (2) extend along the substrate to separate a BSG into a plurality of sub-BSGs.

Institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to any of the Challenged Claims. Specifically, Petitioner sets forth three obviousness Grounds challenging '623 independent Claim 1 and its dependent Claims 2-11: Ground 1) Park (Ex. 1004) alone; Ground 2) Park in view of Shibata (Ex. 1005); and Ground 3) Shibata in view of Park. Not one of

these Grounds discloses or renders obvious even claim 1. Indeed, all three Grounds fail to teach the same limitation of independent claim 1: [1.e], which recites “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.”

Regarding Ground 1, Park’s isolation insulating layers 111 are not the claimed “dielectric trenches,” but are instead short and shallow regions that close the gaps formed between two collinear common source lines in the staircase region, where contacts to the memory’s word lines are formed. A similar feature in the ’623 between two collinear common source lines in the array region is referred by the specification as an H-cut—not a trench. Additionally, because Park’s isolation insulating layers 111 are very short features in the staircase region, Park fails to disclose that the insulating layers “extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” as required by limitation [1.e]. Instead, it is the second common source line that extends through the array region to divide the BSG into sub-BSGs.

Regarding Ground 2, Petitioner attempts to cure the deficiencies in Ground 1 by applying incompatible teachings of Shibata to Park. But these arguments are also misplaced for several reasons. First, as Petitioner admits, “Shibata only employs its separation portion to divide its *upper* drain-side select gate and not its ‘BSG.’” Pet. 74. Petitioner does not sufficiently explain why a POSITA would have been

motivated to apply these teachings of Shibata to Park, which would require significant changes to the configuration of Park's isolation insulating layers and common source lines. A POSITA looking at Park would not have made these modifications. Park teaches that long isolation insulating layers are undesirable because this may cause the incomplete removal of sacrificial layers and ultimately cause voids in the deposited conductive layers that form the word lines. In addition, Park teaches that having multiple isolation insulating layers side-by-side will prevent the flow of etching material in certain regions entirely. However, despite Park's express teachings against the use of long, side-by-side isolation regions, Petitioner's proposed combination does exactly that by "eliminat[ing] Park's second common source lines 105 and replac[ing] them with longer isolation insulating regions 111" "that span the length of its device." Pet. 59-60. Finally, contrary to Petitioner's arguments, a POSITA would not have been motivated to reduce the number of common source lines in Park because that would result in a suboptimal system with poorer speed, thermal management, reliability, accuracy, and device scalability. Thus, for these additional reasons, Ground 2 does not render the Challenged Claims obvious.

Regarding Ground 3, Petitioner proposes that in light of Park's teachings of isolation insulating layers in the purported BSG it would have been obvious to make two modifications to Shibata necessary to meet the limitations: 1) rather than

dividing just the upper drain-side select gates using separation portions 62a (as taught by Shibata), Shibata would employ “new additional separation portions 62b” to also divide the BSG into sub-BSGs; and 2) rather than employing multiple lower source-side select gate layers (as taught by Shibata), “Shibata would employ a single ‘bottom select gate (BSG).’” Pet. 74-75. But a POSITA would not have been motivated to make either of these proposed modifications. Park’s teachings of isolation insulating regions would not have motivated a POSITA to replicate Shibata’s dissimilar teachings of separation portions in completely different locations. Instead, Petitioner, and its expert, provide no more than conclusory assertions and ill-conceived rationales.

For at least these reasons and those discussed below, the Petition should be denied institution.

II. THE CLAIMED INVENTION OF THE ’623 PATENT

The claimed invention of the ’623 is directed to an improved “3D [three-dimensional] memory device with a divided block structure” that provides a novel approach to address issues—such as “longer erasing time, longer data transfer time, and lower storage efficiency”—associated with conventional architectural memory device designs containing a “shared BSG [bottom select gate]” architecture. ’623, 1:33-35, 1:57-60.

3D NAND flash memory technology architecture has been developed such that “the vertical NAND memory cell strings of a same block” share a bottom select gate (BSG). ’623, 1:50-52. The shared BSG “controls all of the BSTs [bottom select transistors] or vertical NAND memory cell strings in [a] block simultaneously” during operation of the memory device. ’623, 1:53-57. However, as the number of vertical layers and bit density increases, “the shared BSG can induce longer erasing time, longer data transfer time, and lower storage efficiency.” ’623, 1:57-60.

The claimed invention of the ’623 overcomes these device performance issues by introducing a novel 3D NAND memory device architecture that separates the memory cell blocks into a plurality of sub-blocks. ’623, 1:61-62. This architecture “divid[es] the shared BSG into a plurality of sub-BSGs,” so that each of the sub-blocks “can be operated individually through controlling the respective sub-BSG.” ’623, 1:61-67. Figure 1A, color-annotated below, shows a cross-sectional view of the ’623’s device with substrate 10:



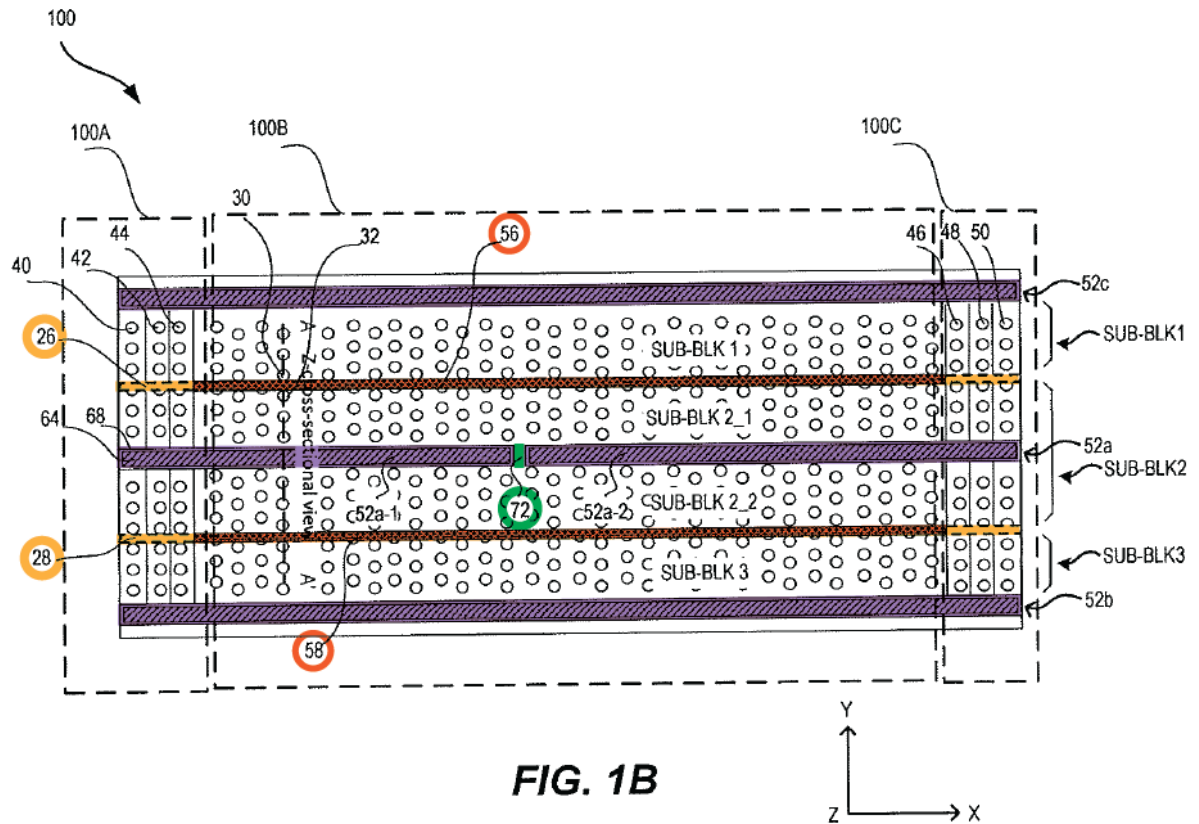
'623, Fig. 1A, 5:40-48. A **bottom select gate (BSG) 62p**, a “plurality of word lines (e.g., 62d-62m),” and a top select gate (TSG) 62a are “disposed sequentially over the substrate” ('623, 6:44-49). During this process, “a plurality of insulating layers” (insulating layers 60) are disposed between each of the layers that will form the BSG, word lines, and TSG. '623, 6:49-54. The **BSG**, word lines, and insulating layers 60 are “alternatively stacked over the substrate 10 with a staircase configuration.” '623, 6:55-61.

After the BSG is formed, the '623 teaches that “by introducing the first [] trenches into the memory device 100, the BSG [is] separated into a plurality of sub-BSGs.” '623, 7:45-47. Specifically, “one or more first dielectric trenches (or first trenches), such as two **first trenches 26 and 28**, are formed in the one or more BSGs

(e.g., 62p),” with the “**first trenches 26 and 28** extend[ing] in an X-direction (i.e., length direction) of the substrate 10 to separate the **BSG 62p**” into “a plurality of sub-BSGs.” ’623, 7:17-24. As depicted in Figure 1A, the dielectric trenches also extend into a Z-direction, traversing multiple conductive and insulation layers. After the TSG is formed, corresponding **second trenches 56 and 58** are “formed in the one or more TSGs (e.g., 62a).” ’623, 7:26-29. The **first trenches** and **second trenches** can have an inner critical dimension (“CD”) and extend into the high voltage P-type well (“HVPW”) formed on the top portion of the substrate 10 with a depth of 10 to 100 nanometers. ’623, 6:32-33, 7:39-41, 7:42-44. The dielectric trenches are filled with “suitable dielectric materials,” such as silicon dioxide (SiO₂), silicon oxynitride (SiON), and silicon oxycarbonitride (SiOCN). ’623, 7:42. The sub-BSGs “divide the memory device 100 into a plurality of sub-blocks,” or, in other words, “a plurality of cell strings,” and “each of the sub-blocks can be operated individually through controlling the respective sub-BSG.” ’623, 7:47-53. As such, the ’623’s memory device “can precisely control a desired sub-block/array region so as to effectively reduce a programming time, a reading time, an erasing time and data transfer time, and significantly improve data storage efficiency.” ’623, 7:53-58. Accordingly, the claimed memory device architecture of the ’623 overcomes shortcomings of the prior art.

The '623 further teaches that the memory device includes “one or more common source regions (CSRs), such as one **common source region 52**,” which is “formed over the substrate” and “extend[s] in the X-direction (length direction) of the substrate.” '623, 7:59-62. The CSR “passes through the BSG 62p,” “the plurality of word lines 62d-62m,” as well as “the plurality of insulating layers 60,” among other layers. '623, 7:62-66. Moreover, the CSR “is electrically coupled with the substrate 10 via a doped region 54.” '623, 7:66-67.

The '623 distinguishes the **first trenches** and **second trenches** (which divide the BSG and TSG, respectively) from the H-cut 72, which divides the common source region into **sub-CSRs 52a-1** and **52a-2**. Indeed, as depicted in Figures 1A, 3A and 11A, it is a short “**H-cut**”—not a trench—that divides the **common source region**. Figure 1B, color-annotated below, shows the same memory device of the '623 from a top-down view:



'623, Fig. 1B (annotated) 4:35-37. As illustrated in Figure 1B, three **common source regions, 52a-52c**, “extend along the X-direction (length direction) of the substrate 10.” '623, 8:67-9:2; *see also* '623, Figs. 11B-C. The “**common source region 52a** is separated” “by an **H-cut 72** into two sub-CSRs 52a-1 and 52a-2.”² '623, Fig. 1B, 9:14-18. Also illustrated in Figure 1B above, are two pairs of

trenches: **first trenches 26 and 28** in the BSG, which extend the length of the bottom select gate; and **second trenches 56 and 58**, which extend the length of the top select gate. In other words, the '623 teaches a region of the memory device, wherein a common source region is separated into sub-divisions by a cut—not a trench.

Claim 1, the only independent claim of the '623, is directed to aspects of the above-described invention:

[1.pre] A memory device, comprising:

[1.a] a substrate;

[1.b] a bottom select gate (BSG) disposed over the substrate;

[1.c] a plurality of word lines positioned over the BSG with a staircase configuration;

[1.d] a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;

[1.e] one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and

[1.f] one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.

III. FILE HISTORY

The '623 issued as a continuation of a foreign patent application, Korean Patent Application No. 10-2016-0091946, filed on July 20, 2016 in the Korean Intellectual Property Office. The claims of the '623 were allowed after consideration of numerous prior art references. Over the course of prosecution, over twenty references were considered by the Examiner. *See, e.g.*, Ex. 1002 (Part 2), 131, 139, 141, 144, 204.

In a Notice of Allowance dated November 16, 2020, the Examiner stated that the “prior art of record and considered pertinent to the applicant’s disclosures, especially when these limitations are considered within the specific combination claimed, does not teach or fairly disclose[]” the claimed invention. Ex. 1002 (Part 2), 127-130. The '623 issued on March 16, 2021.

IV. CLAIM CONSTRUCTION

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” § 42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A POSITA ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant extrinsic

evidence, although the claims and patent specification are the primary sources for construing claims. *Id.*, 1314-16.

The parties in the parallel district court proceeding have not yet exchanged proposed claim constructions. In its Petition, Petitioner contends that the terms of the '623 patent's claims do not require further construction and can be afforded their plain and ordinary meaning. Pet. 18. At this stage, Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the challenged claims for the purposes of institution. Patent Owner, however, reserves the right to raise claim construction issues if the Board institutes IPR, and to raise claim construction issues in the underlying district court proceedings.

V. BACKGROUND OF THE ASSERTED PRIOR ART

A. U.S. Patent 10,559,583 (“Park,” Ex. 1004)

Petitioner relies upon Park for all of the limitations of the independent Challenged Claims. Pet. 25-38. Park is directed to “a memory device having a three-dimensional array of memory cells” using “a vertical transistor structure in lieu of a conventional planar transistor structure.” Park, 1:15-27. The architecture of Park, however, is distinct from that of the '623 for at least the reason that Park does not use dielectric trenches that extend along the memory array to separate the

memory array into blocks, but instead uses a short isolation insulating region in the staircase region to divide the common source line.

Park's memory device includes a "cell region CR" containing "a plurality of gate electrodes layers sequentially stacked on a substrate" in "a Z-axis direction," which "may provide a string select line, word lines, and a ground select line."

Park, 2:14-17, 5:18-25. As illustrated in Figure 4 below, the cell region includes a "plurality of pad regions constituting a stepped structure" (*i.e.*, a staircase region), wherein the "cell contacts CNT" may be connected to the word lines:

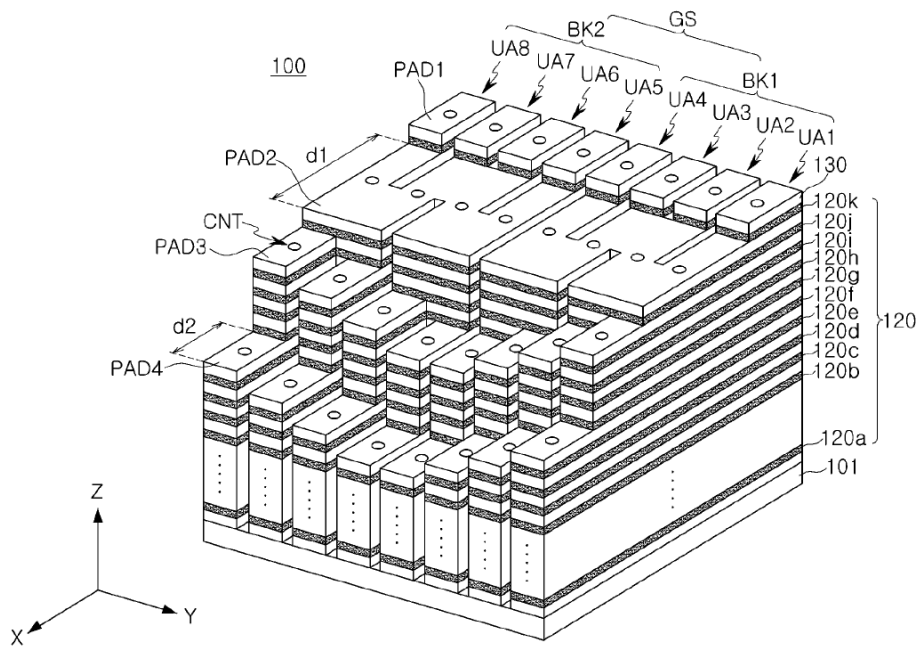


FIG. 4

Independent control of unit areas (*e.g.*, UA1 to UA8) is provided by the string select line and the ground select line, which "may be separated from each other at the boundaries between the first to eighth unit areas UA1 to UA8" "by the

first common source lines 102 and first lines 103 of the second common source lines 105” as shown in Figure 3 below:

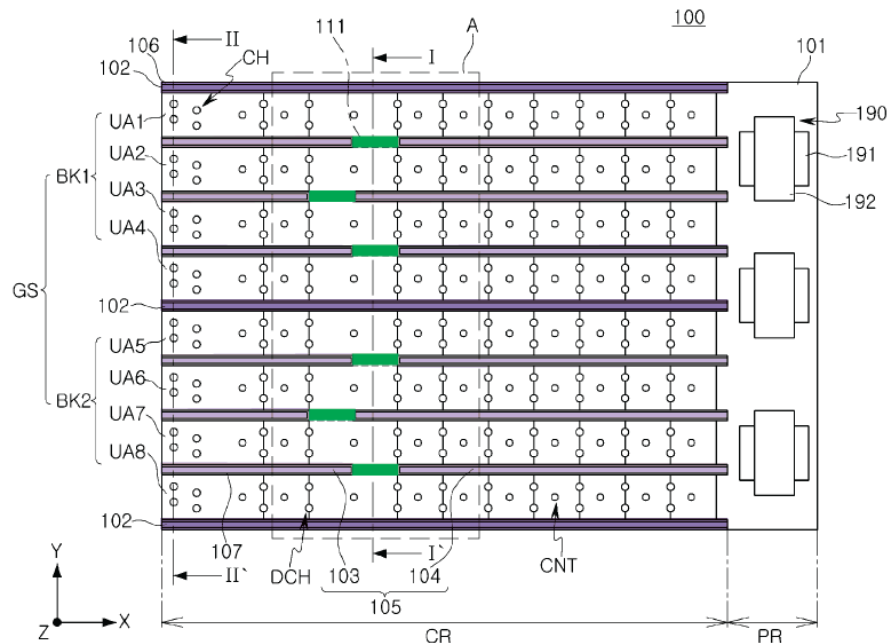


FIG. 3

Park, Fig. 3, Park, 6:4-8.

Park also uses isolation insulating layers 111 “disposed between the first and second lines 103 and 104 of the second common source lines 105” in the staircase region. Park, 6:8-12, 10:60-65. Instead of using a dielectric trench that extends along the length of the substrate to divide a bottom select gate (BSG), as illustrated above, Park’s memory device architecture entails common source lines to divide the ground select line (i.e., the purported BSG), and short isolation insulating layers to segment a subset of the common source lines within the staircase region. While these isolation insulating layers are dissimilar to

the '623's long dielectric trenches, they are very similar to the '623's disclosure of using "H-cuts," which are used to separate the '623's "common source region 52 ... into two or more sub-CSRs." *Compare* Park, Fig. 3 with '623, Fig. 1B, 13:19-20 ("The common source region 52 is separated by the H-Cut 72 into two sub common source regions.").

A cross-sectional view of Park's memory device "taken along line I-I' of FIG. 3" is depicted in Figure 11 below, where "only the second lines 104 of a portion of the **second common source lines 105** are illustrated."³ Park, 10:52-54. There, the gate electrode layers 120 are "divided into the first and second blocks BK1 and BK2 by the **first common source lines 102**." Park, 10:46-49. BK1 and BK2 are further "divided into the first and eight unit areas UA1 and UA8 by the **second common source lines 105**." Park, 10:49-54. **Gate electrode layer 120a** "form[s] the ground select line." Park, 10:55-56. The gate electrode layers (*i.e.*, **gate electrode layer 120a** to 120j) may be "electrically separated from each other by the first and second lines 103 and 104 of the **second common source lines 105** and the **isolation insulating layer 111** disposed between the first and second lines

³ Note the coordinate system for Figure 11 is different than that of Figure 3. In Figure 3, the axis along the line I-I' is the y-axis; whereas in Figure 11, the axis along the line I-I' is the x-axis. The z-axis remains the same in both figures.

103 and 104.” Park, 10:60-65. Recall, this enables the UA1 to UA8 to be “independently controlled.” Park, 10:66-67.

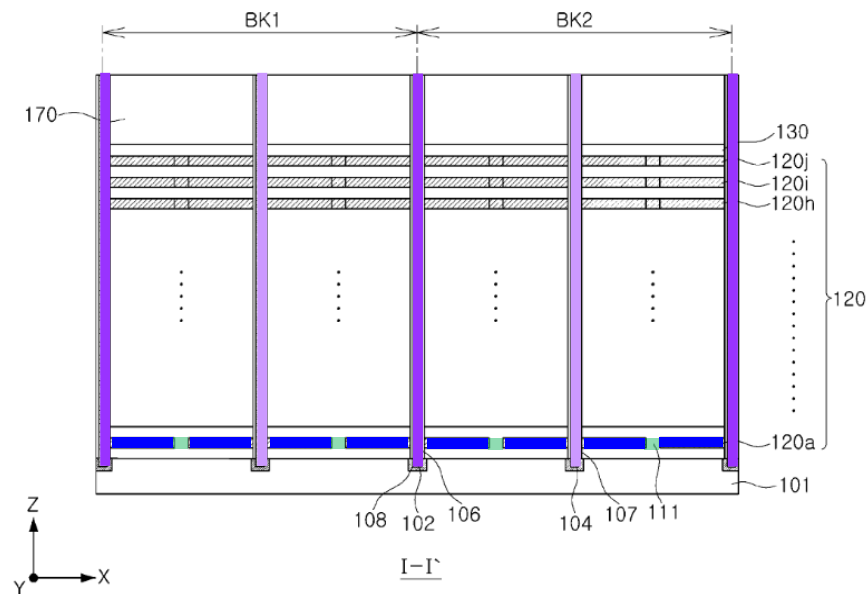
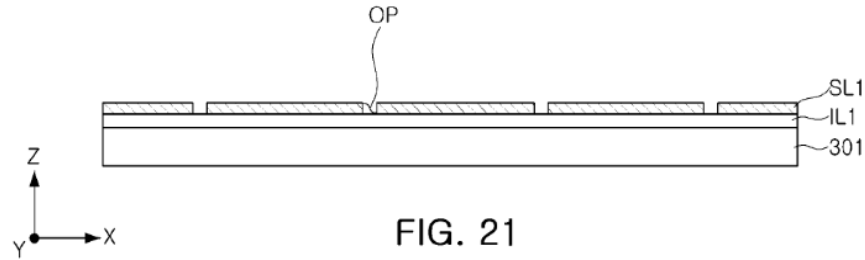


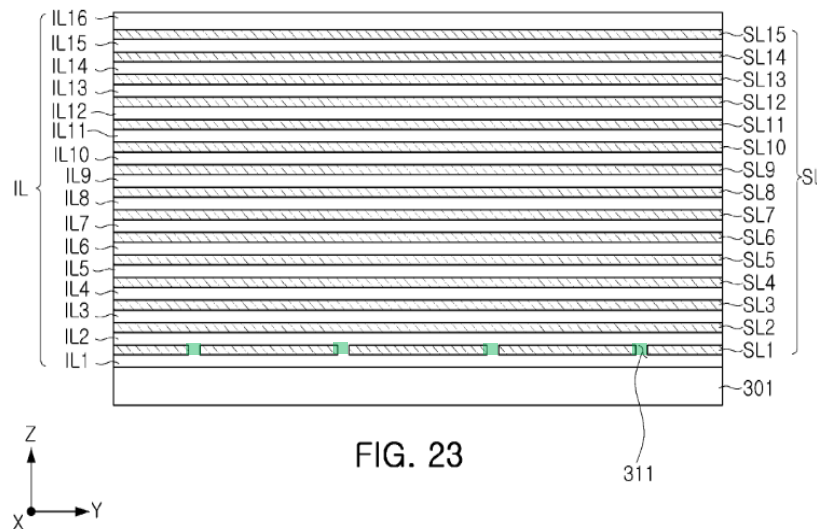
FIG. 11

Park, Fig. 11 (annotated).

Park discloses forming the insulating layer 111 (or 311 in Figures 18-36 illustrating the “memory device during the course of its manufacture”). Park teaches that the process of forming the opening regions includes “a first insulating layer IL1 and a first sacrificial layer SL1,” which are formed on a first substrate 301.” Park, 12:56-59. Figure 21 depicts the first sacrificial layer SL1 with an opening region (“OP”) in which the **isolation regions 311** are formed. Park, 12:65-13:1.



Park, Fig. 21. The OP regions are then “filled with an insulating material,” as depicted in Figure 23, to form **isolation regions 311**, which correspond to the **isolation insulating layers 111** of Figure 16:



Park, Fig. 23 (annotated), 13:15-17. Park teaches that the sacrificial layer is then etched away (*i.e.*, removed) “by an etching solution flowing through the first and second word line cuts WC1 and WC2,” depicted in Figure 29:

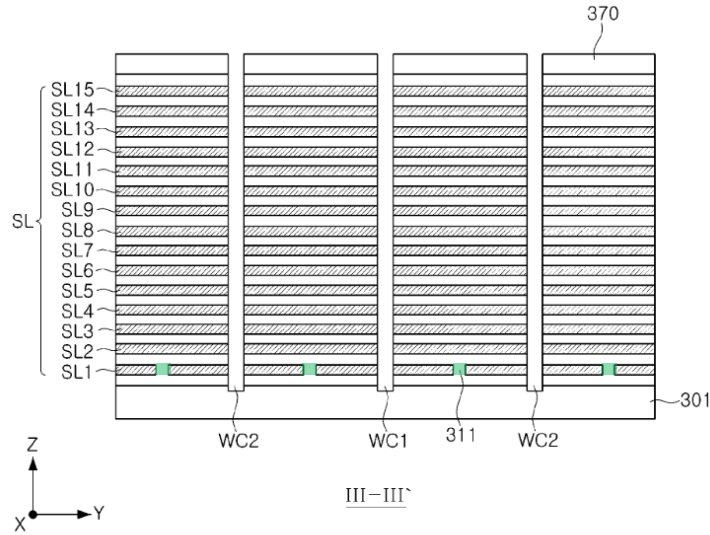


FIG. 29

Park, Fig. 29. After this etching process, “horizontal voids hv are formed,” which are depicted in Figure 31:

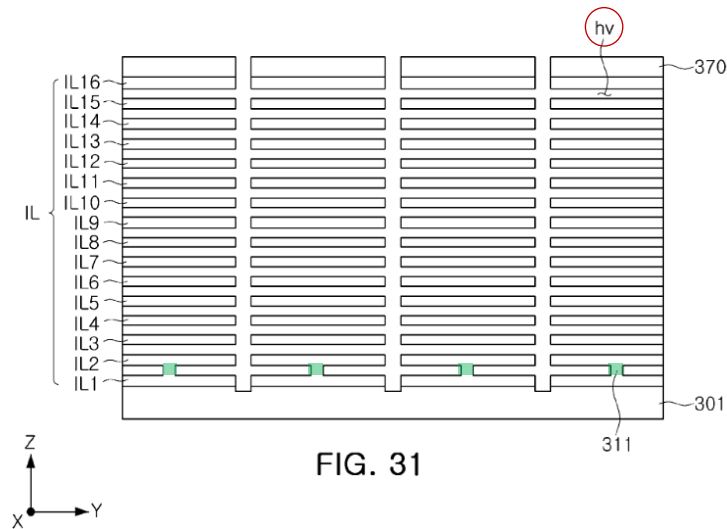
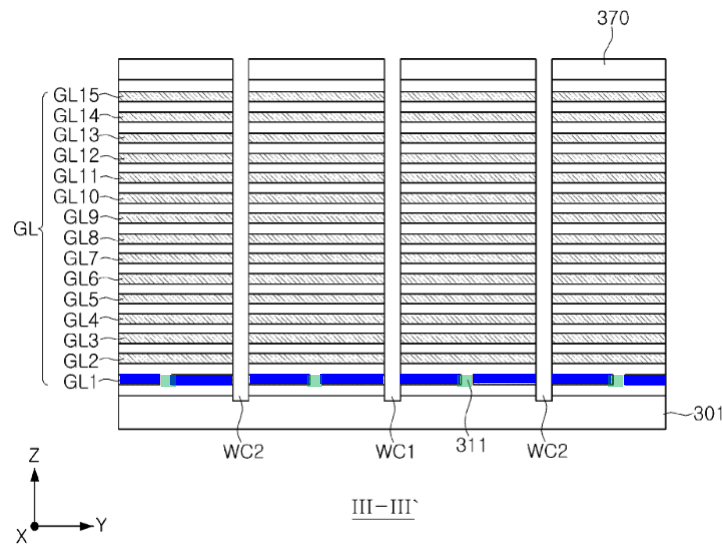


FIG. 31

Park, Fig. 31, 15:39-40. While the sacrificial layer has been etched away, the **isolation regions 311** remain. Park, 16:7-9. The voids are then filled with conductive material, which flows from the first and second word line cuts WC1

and WC2, to form the gate electrode layers. Park, 16:3-7. Figure 34 of Park

depicts the first gate electrode layer GL1, which forms the **ground select line**:



Park, Fig. 34 (annotated).

Park cautions against using long isolation regions because isolation regions can prevent the “proper[] secur[ing]” of the “inflow passage” through which the etching material (for removing sacrificial layers) and conductive material (for forming the gate layers) is introduced. Park, 15:53-59, 16:38-59. This is because the isolation regions separate the word line cuts (that eventually form the second common source lines) thereby “forming a relatively long path above the isolation regions 311” for the flow of etching and conductive materials. Park, 15:53-59. Moreover, when isolation regions are adjacent to one another, Park recognizes that there may be no inflow path to certain areas, and thus disposes the isolation regions “in zigzag form.” Park, 15:60-16:2.

B. U.S. Pub. 2019/0122734 (“Shibata,” Ex. 1005)

Petitioner relies upon combinations of Shibata and Park (Shibata in view of Park and Park in view of Shibata) for Grounds 2 and 3. Pet. 57-94. Shibata is directed to aspects of three-dimensional memory devices that has a “vertical transistor structure.” Shibata, [0067].

Petitioner generally relies on Shibata’s second embodiment as illustrated in Figure 16:

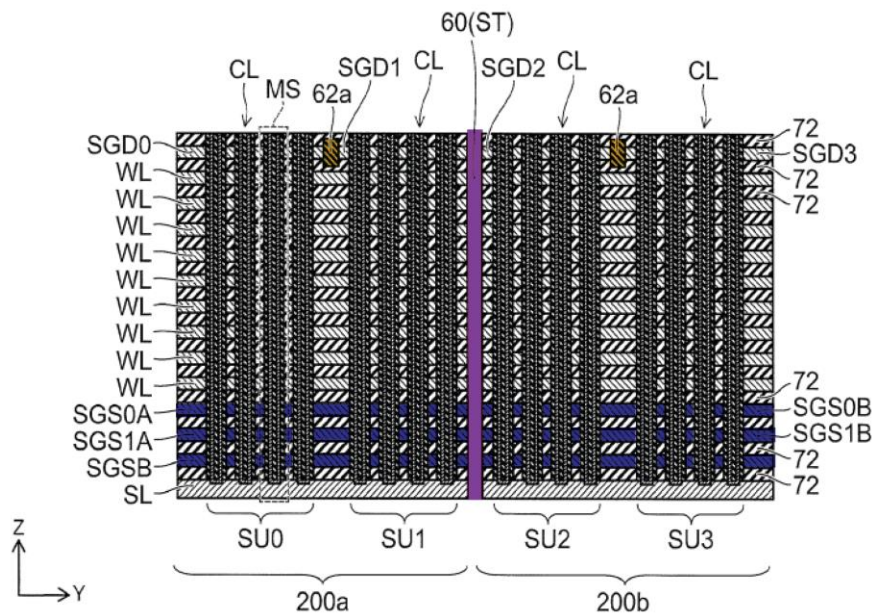


FIG. 16

Shibata, Fig. 16 (annotated). Shibata’s Figure 16 depicts a second embodiment with “two sub-blocks 200a and 200b subdivided by **separation portions 60** (slits ST) separated from each other in the Y-direction. Shibata, [0162]. Figure 16 additionally illustrates **separation portion 62a** of sub-block 200a and **separation portion 62a** of sub-block 200b. In this embodiment, there is a single-layer drain-

side select gate SGD0 and a **three-layer source-side select gate** and layers of word lines stacked between. Shibata, [0166]. Notably, Shibata's **separation portions 62a** do not divide the **source-side select gate**. Instead, the **source-side select gates** are divided in the Y-direction by the separation portions 60 (the slits ST) into "SGS0A," "SGS0B," "SGS1A," and "SGS1B." Shibata, [0178].

Petitioner also relies on Figure 47A, which is a plan view of the drain-side select gate layer divided into “SGD0,” “SGD1,” “SGD2,” and “SGD3”:

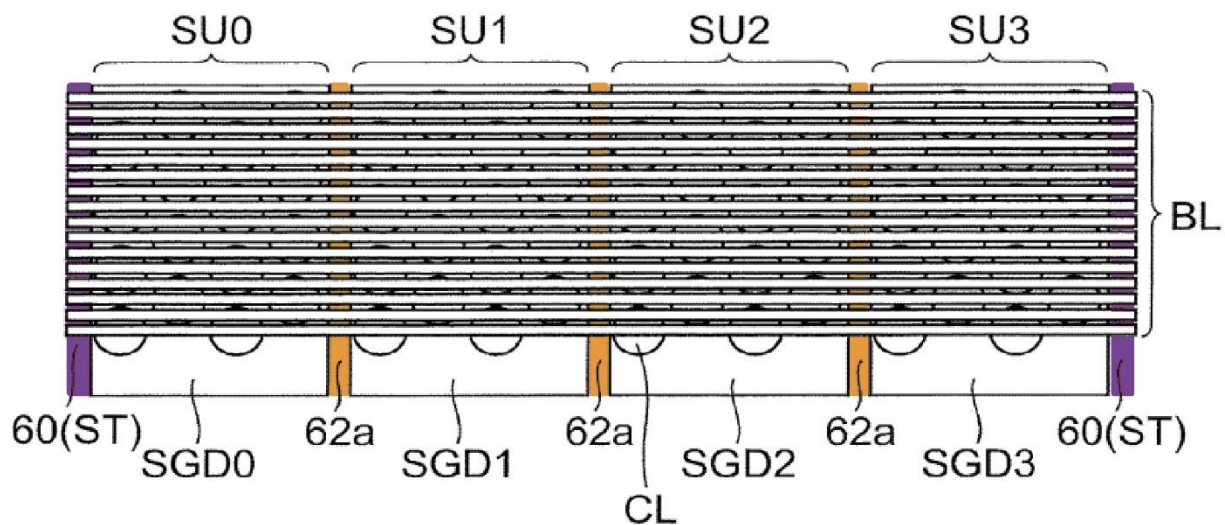


FIG. 47A

Shibata, Fig. 47A (annotated), [0444], [0446], [0047].⁴ As illustrated in Figure 47A, the **separation portions 62a** extend through the array region of the memory.

With regard to the first embodiment, Shibata also describes the “method for manufacturing the semiconductor memory device of the first embodiment.”

Shibata, [0103].⁵ Shibata’s process starts off with the structure as depicted in Figure 8A, where “the insulating layer 41 is formed on the substrate 10; the source

⁴ Note, that as illustrated in Figure 47A, Shibata’s first embodiment has a different configuration than that of Figure 16. For example, there are three **separation portions 62a** facing back-to-back instead of alternating with **separation portions 60**. In addition, the drain-side select gate SGD1 of Figure 47A is between two **separation portion 62a** instead of next to one of the **separation portions 60** (slits ST).

⁵ Note, Figures 8A through 11B are schematic cross-sectional views showing a method for manufacturing the semiconductor memory device of the first embodiment (Shibata, [0011]), but this embodiment differs from that illustrated in Figure 47 in that it has a three-layer drain-side select gate with three separation portions 62a, 62b, and 62c positioned at of these layers. While the configuration is different than that of the second embodiment, the method of manufacture is informative.

layer SL is formed on the insulating layer 41; and the stacked body 100 is formed on the source layer SL.” Shibata, [0104]. The “insulating layer 72 and sacrificial layer 71 are stacked alternately on the source layer SL.” Shibata, [0105].

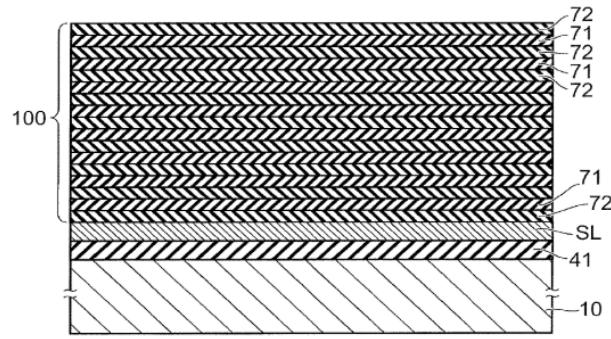


FIG. 8A

Shibata, Fig. 8A. As depicted in Figure 8B, silicon oxide film is formed on the top of the stacked body which serves as a mask. Shibata, [0106]. A slit, 61b, “pierces the mask 75, the insulating layer 72 of the uppermost layer, and the sacrificial layer 71 of the uppermost layer.” Shibata, [0106]. Slit 61b penetrates through the upper sacrificial layer 71 and terminates within the insulation layer 72.



FIG. 8B

As depicted in Figure 8C, “a separation portion 62b is formed inside the slit 61b” by filling the slit with an insulating material. Shibata, [0107]. This layer, called insulating film 62, is also deposited on mask 75. *Id.*

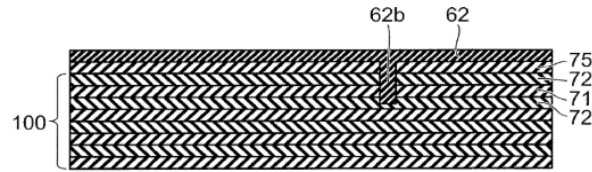


FIG. 8C

Mask 75 and the insulating film 62 are then removed and the final structure is depicted in Figure 9A. Shibata, [0107].



FIG. 9A

Subsequently, a sacrificial layer 71 and an insulating layer 72 are deposited, followed by the application of another mask layer 76 to generate a second slit, 61a, at another position. Shibata, [0108]-[0109]. Slit 62a is filled with insulating material to form separation portion 62a, depicted in Figure 9C below. Shibata, [0110].

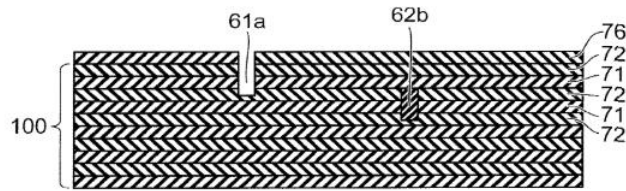


FIG. 9B

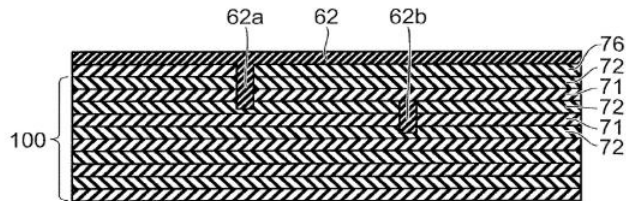


FIG. 9C

This sequence of steps is repeated to form a third separation portion, 62c. In total, Shibata teaches three separation portions—62a, 62b, and 62c—are situated at distinct locations along the Y-direction, as depicted in Figure 13, and which “divide drain-side select gate layers of different layers.” Shibata, [0155]. The sacrificial layers 71 are then removed through an etching process and replaced with conductive layers 60 to form the source gate drains and word lines. Shibata, [0155]. The separation portions segment the drain-side select gate layers into six—“SGD0A,” “SGD1A,” “SGD2A,” “SGD0B,” “SGD1B,” and “SGD2B”—each of which are “each controlled electrically independently.” Shibata, [0126]-[0129].

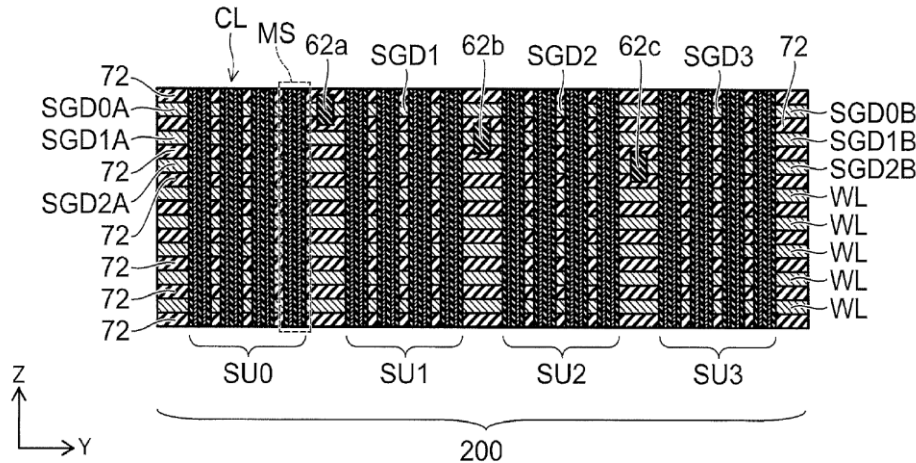


FIG. 13

Shibata, Fig. 13. As shown through this process, Shibata's separation portions are formed in a sacrificial layer prior to the removal of the sacrificial layer and replacement with conductive material that forms the drain-side select gate layers and source-side select gate layers. Moreover, Shibata teaches only adding the separation portions to the drain-side gate select lines and does not teach adding separation portions to the source-side select lines.

VI. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO THE CHALLENGED CLAIMS

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claims because Petitioner has failed to show that the cited references disclose the steps recited in each of the independent Challenged Claims: [1.e], which recites "one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality

of sub-BSGs.” As explained below, Petitioner cites to two references—Park and Shibata—and asserts that Park individually, Park in view of Shibata, or Shibata in view of Park, show these features. Each of Petitioner’s arguments fails.

A. Ground 1: Park Does Not Disclose or Render Obvious Multiple Independent Requirements of Limitation [1.e]

Petitioner fails to show that Park discloses or renders obvious multiple independent requirements of limitation [1.e]: “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” Petitioner incorrectly contends that this limitation is met by Park’s shallow and short isolation insulating layers that divide a source contact line in two. These isolation insulating layers, however, are “cuts” not “trenches” and do not extend along the length of the substrate to separate the BSG into a plurality of sub-BSGs. For at least these reasons, Petitioner has failed to show that Park teaches limitation [1.e].

For example, Petitioner incorrectly argues that the isolation insulating layers are “dielectric trenches.” Petitioner, however, ignored that the ’623 already describe features like isolation insulating layers but calls them “H-cuts” not “trenches.” Park also fails to disclose dielectric trenches that are “extending in the length direction” such that they “separate the BSG into a plurality of sub-BSGs,” as required by limitation [1.e]. Instead, Park discloses isolation insulating layers, which are not dielectric trenches nor do they function to separate a bottom select

gate. Furthermore, Park expressly teaches that it is the common source lines—not the isolation insulating layers—that separate the bottom select gate into sub-BSGs. Petitioner fails to show that a POSITA would have found it obvious to change its design such that isolation insulating layers, not common source lines, separate a bottom select gate. Petitioner also fails to show a POSITA would have found it obvious to change Park’s isolation insulating layers to take the form of dielectric trenches.

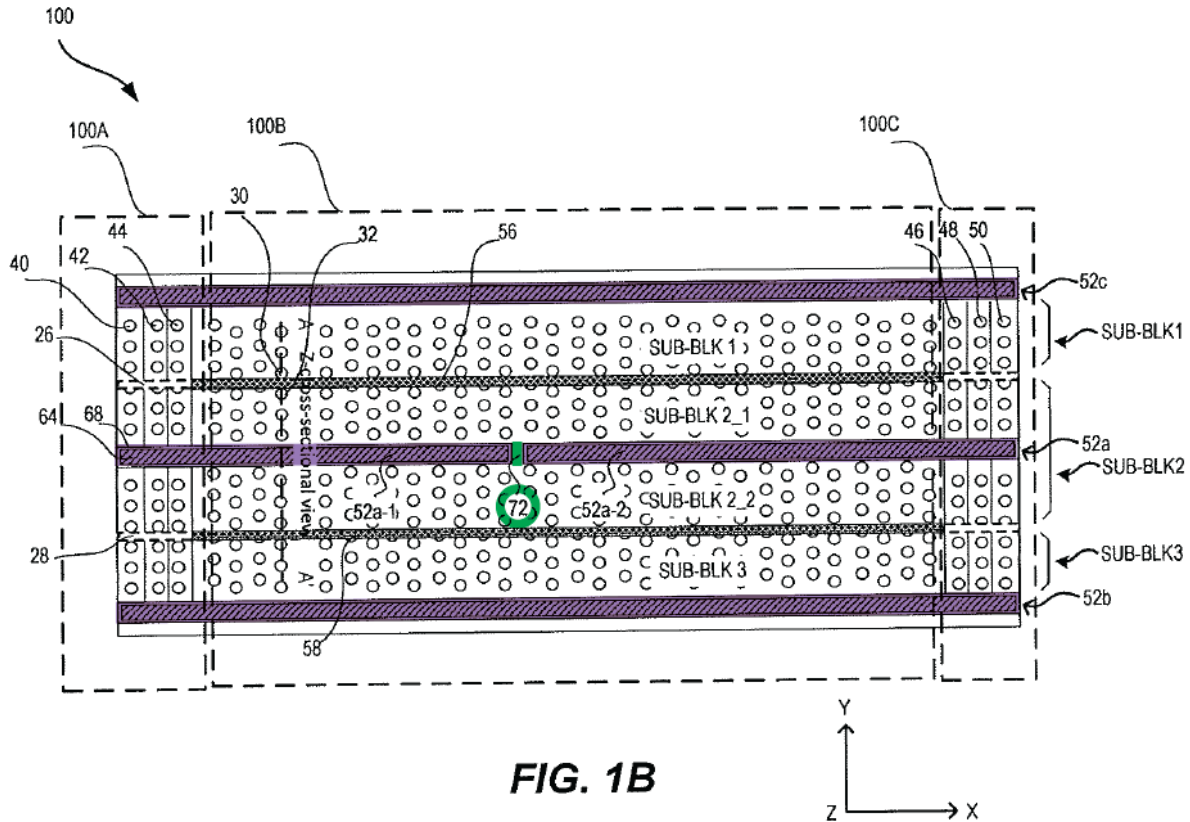
1. Park’s Isolation Insulating Layers Are Not “Trenches”

Petitioner fails to show that Park’s isolation insulating layer is a dielectric trench. Petitioner seemingly concedes that Park does not explicitly disclose a trench (*see* Pet. 33-36), and attempts to salvage Park through unreasonable inferences and irrelevant, out-of-context comparisons to the ’623 invention to argue that a POSITA would have nonetheless understood that Park’s isolation insulating layer is a “dielectric trench[].”

First, Petitioner ignores that the ’623 distinguishes a gap in the common source lines—similar to Park’s isolation insulating layer—from the claimed “dielectric trench.” Specifically, the ’623 teaches an “H-cut” that is positioned between subdivisions of a common source region (CSR):

The common source region 52a is disposed at a middle position of the memory device 100. The common source region 52a is separated into two or more sub-CSRs by one or more “H-Cuts”. As shown in FIG. 1B, the **CRS 52a is separated by an H-cut 72 into two sub-CSRs 52a-1 and 52a-2.**

'623, 9:13-18 (emphasis added). Figure 1B of the '623 depicts this separation of the **common source region 52a** by an H-cut 72 (green):



'623, Fig. 1B (annotated). This H-cut that divides subdivisions of the common source region is like Park's **isolation insulating layer**, which, according to Petitioner, "close[s] the gaps in **common source lines 105**" (Pet. 31):

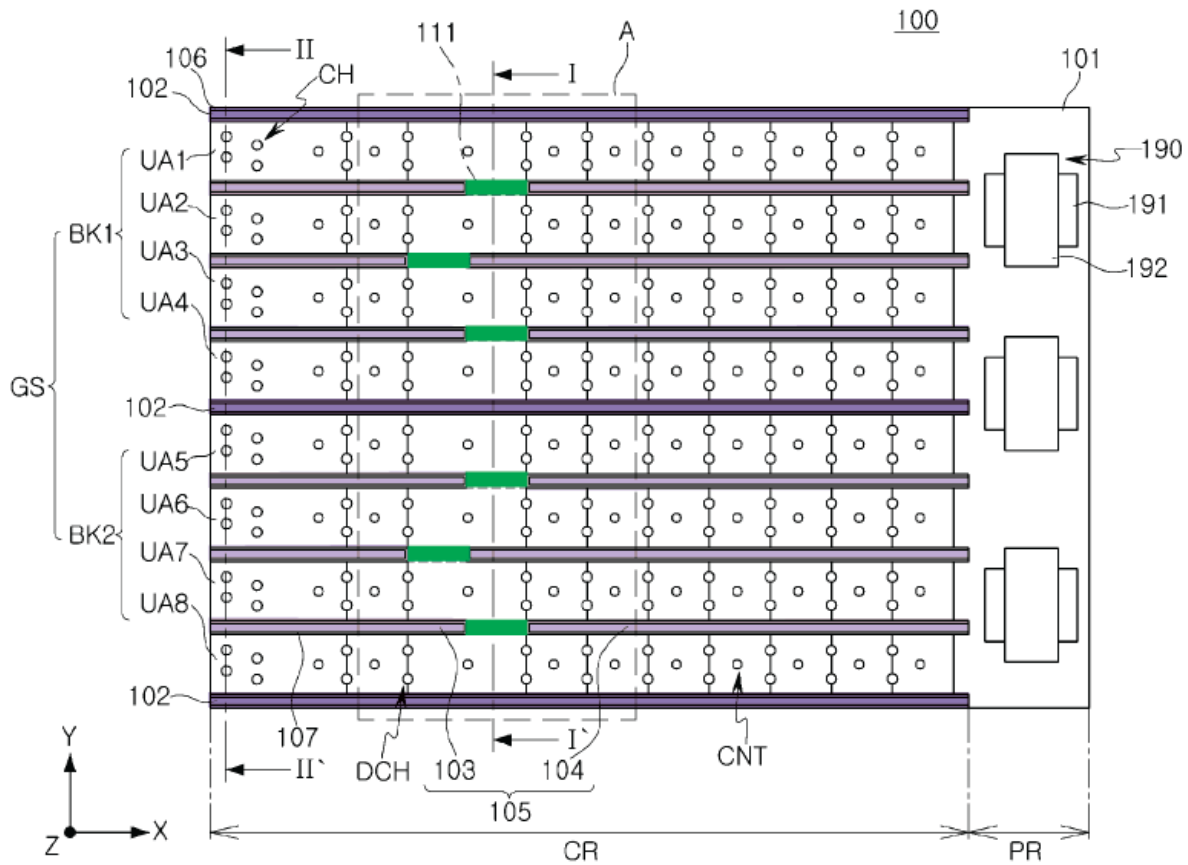
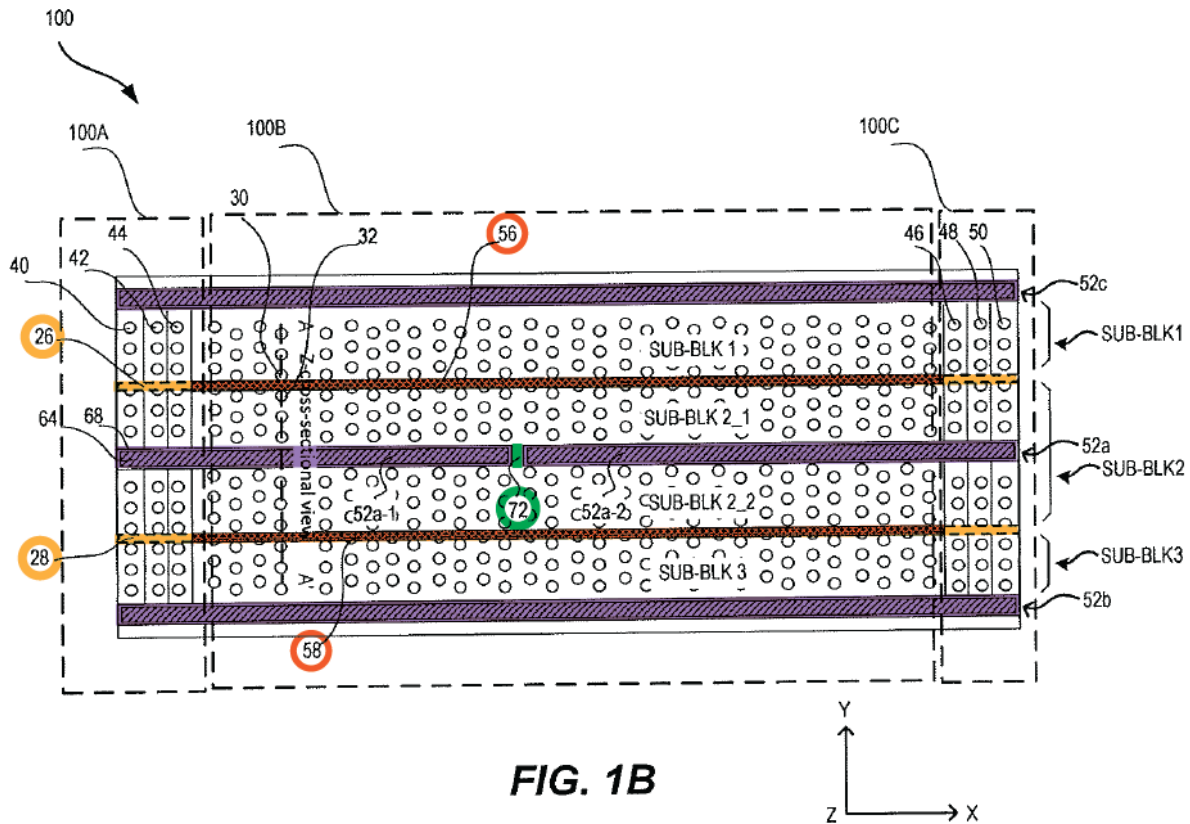


FIG. 3

Park, Fig. 3 (annotated). On the other hand, the '623 describes dielectric trenches, “**first trenches 26 and 28**” and “**second trenches 56 and 58**,” that extend along the BSG and TSG, respectively, and separate regions of the memory device:



'623, Fig. 1B (annotated); see also '623, 9:20-23.

The '623 repeatedly and consistently makes this distinction between an H-cut and trench, and thus the terms refer to two distinct components or features of a memory device. If the '623 had intended to teach that a common source region is separated into sub-regions by trenches, it would have expressly said so. Rather, the '623 teaches that this other type of feature that does so is an "H-cut." As the '623 makes clear, a separation of common source regions made by an "H-cut" is distinct from a separation made by a trench.

Despite the '623 making such a distinction, Petitioner failed to address why Park's isolation insulating layer is not an "H-cut" instead of a dielectric trench. Petitioner and its expert ignore that the '623 includes such a teaching. Instead, Petitioner attempts to draw flawed similarities between the fabrication processes of Park's isolation insulating layers and that of the '623's dielectric trenches. Petitioner's purported similarities, however, are inapposite. Pet. 34. Specifically, Petitioner contends that: (1) the process of forming dielectric trenches entails forming trenches using "'trench openings' through the desired layers and then 'fill[ing]' these 'trench openings' with 'dielectric material'" (Pet. 34 (citations removed)), and (2) the process of forming Park's "isolating regions" includes "fill[ing]" an "[o]pening OP [] structured as a trench extending in Figure 20's X-axis" with "insulating material" (Pet. 34 (citations removed)). But regardless of whether the process of forming isolation insulating layers is similar to that of forming the '623 dielectric trenches, the final structures formed are not the same, and Petitioner has failed to explain why Park's isolation insulating layers, which are short regions that separate the second common source line similar to the '623's "H-cuts," is specifically a trench and not a cut.

Accordingly, Petitioner fails to show that Park's isolation insulating layer is a dielectric trench.

2. Park’s Isolation Insulating Layers Do Not “Extend[] in a Length Direction of the Substrate to Separate the BSG Into a Plurality of Sub-BSGs”

Park’s isolation insulating layers do not separate the BSG as required by the claims. Limitation [1.e] further requires that the claimed trenches “extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” Park’s isolation insulating layers instead divide Park’s second common source lines. As Petitioner admits, “[i]solation insulating layers 111 close[] the gaps in common source lines 105.” Pet. 31.

For instance, Park teaches that its memory device has a plurality of “**first common source lines 102**” and “**second common source lines 105**.” Each of the second common source lines are composed of a first section, *i.e.*, “first lines 103,” and a second section, *i.e.*, “second lines 104.” *See, e.g.*, Park, 16:55-59; *see also* Park, 1:59-61. As illustrated in Figure 3 of Park below, the first lines 103 and second lines 104, each extend horizontally along the x-direction, and are *separated* from each other in the x-direction by a short gap in the staircase region of the memory device:

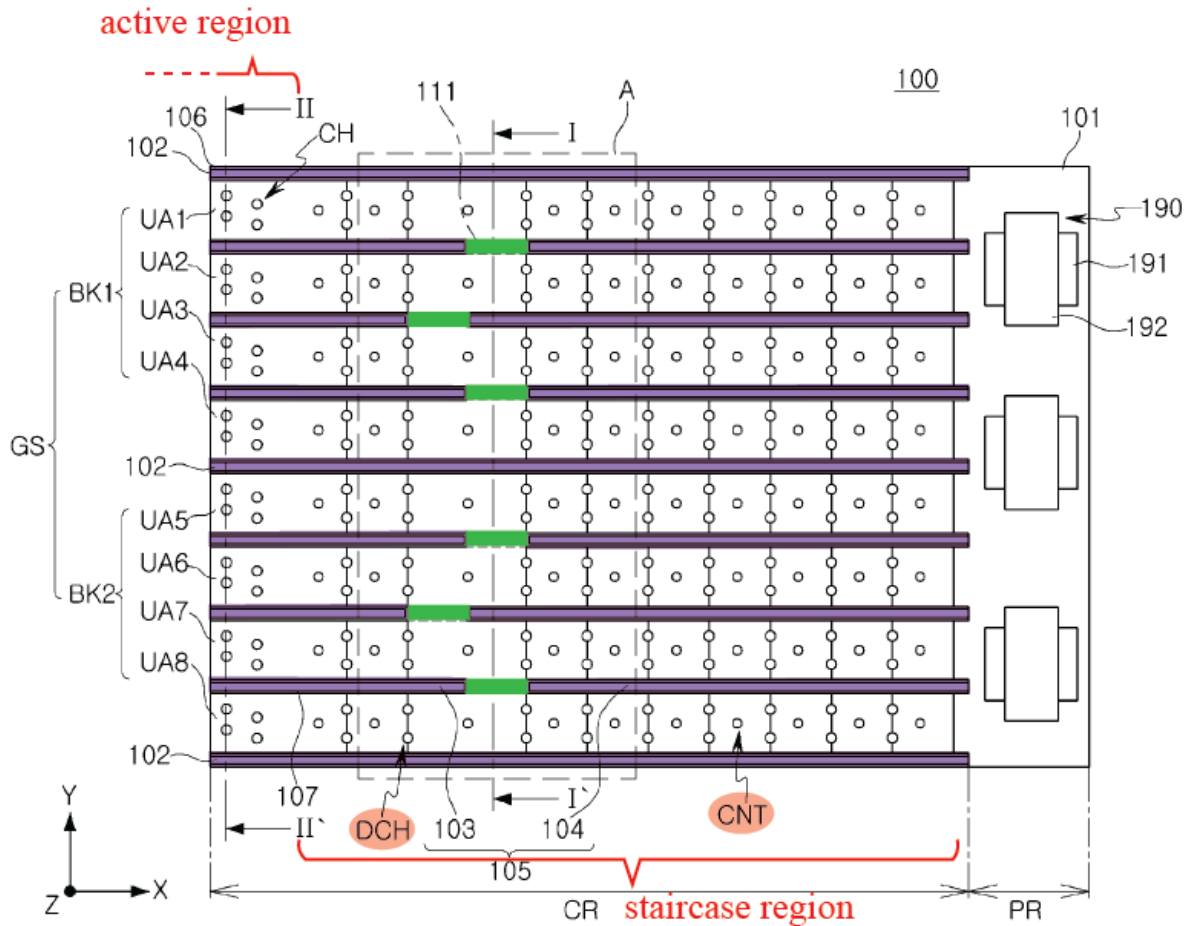


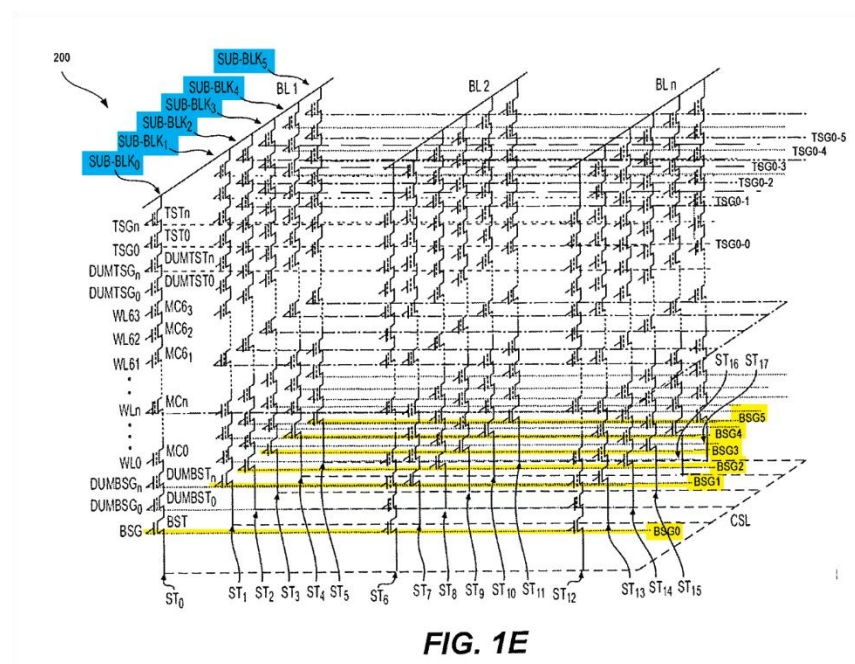
FIG. 3

Park Fig. 3 (annotated). Park further discloses that in this gap an “isolation insulating layer 111 [is] disposed between the first and second lines 103 and 104.”. Park, 10:63-65. Accordingly, the **isolation insulating layer 111** is a short cut along the **second common source lines 105**, that separates the first and second lines 103 and 104. Figure 3 of Park also shows that the **isolation insulating layers** extend no more than just the distance from the center of one dummy channel (DCH) and the center of an adjacent contact (CNT), as such it does not separate the BSG.

Moreover, the isolation insulating layers do not separate the BSG into a plurality of sub-BSGs because Park's **isolation insulating layers** are in the staircase region and not the active region. As the '623 explains, within each block the sub-BSG controls the string of memory cells:

“In the related 3D-NAND memory device, the vertical NAND memory cell strings of a same block can share a bottom select gate (BSG). The shared BSG accordingly controls all the BSTs of the vertical NAND memory cell strings in that block simultaneously during operating the related 3D-NAND memory device, such as erasing the related 3D-NAND memory device.”

'623, 1:50-57 (emphasis added). This is further illustrated in Figure 1E, which shows a circuit diagram confirming that each sub-BSG, BSG0 to BSG5, is coupled to the three cell strings of each sub block, SUB-BLK0 to SUB-BLK5, respectively:



'623 Fig. 1E (annotated). Therefore, the division of BSGs into sub-BSGs is in the active region, where each sub-BSG can individually control the cell strings of its sub-block—not in the staircase region, where there are no cell strings. Because Park's isolation insulating layers 111 are limited to the staircase region, they do not "extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs."

Petitioner's assertion that the isolation insulating layers separate Park's gate select line into portions corresponding to unit areas UA1-UA8 (Pet. 30-33) mischaracterizes Park's teachings. The unit area UA1-UA8 are not separated solely by the isolation insulating layers; rather, Park teaches that they are separated by second common source lines in conjunction with the isolation insulating layers. For example, Park states, "The first and second blocks BK1 and BK2 may be divided into the first and eighth unit areas UA1 and UA8 **by the second common source lines 105.**" Park, 16:49-52 (emphasis added). As another example, Park states, "**Each of the second common source lines 305 separating the first and eighth unit areas UA1 and UA8 from each other** in each of the first and second blocks BK1 and BK2...." Park, 16:55-59 (emphasis added). Park also discloses that "ground select lines of the respective first to eighth unit areas UA1 to UA8 may be electrically separated from each other **by the first and second lines 103 and 104 of the second common source lines 105 and the isolation insulating**

layer 111 disposed between the first and second lines 103 and 104.” Park, 10:60-65 (emphasis added).

While Petitioner correctly recognizes that, only in “cooperat[ion] with common source lines 105,” is Park’s GSL divided into portions by the isolation insulating layer (Pet. 35 (*citing* Park, 6:8-12; Fig. 3)), Petitioner incorrectly argues that “[n]othing about the claim requires that the ‘dielectric trenches’ perform this ‘separat[ion]’ function completely by themselves without the help of any other structure.” Pet. 35. The opposite is true. Nothing in the claims (nor the specification) suggests that the function of separating the BSG into a plurality of sub-BSGs may be met by a completely different feature than the claimed dielectric trenches. As described above, each isolation insulating layer extends no further than from one dummy channel to an adjacent contact. In contrast, the dielectric trenches of the ’623 patent extend the entire length of the memory device, thereby “separating” the BSG into a plurality of sub-BSGs.

For at least the reasons provides above, Park fails to teach or render obvious the claimed dielectric trenches that extend in a length direction of the substate to separate the BSG into a plurality of sub-BSGs.

B. Ground 2: Park in View of Shibata Does Not Disclose or Render Obvious Limitation [1.e]

For the numerous reasons set forth in §VI.A, Park fails to disclose or render obvious “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” In Ground 2, Petitioner attempts to address some of these deficiencies by applying disclosures from Shibata to Park’s memory device. Petitioner’s Ground 2, however, not only fails to cure the identified problems discussed above, but by proposing a combination based on hindsight and misinterpretation of the references, also fails to show that a POSITA would have made the proposed modifications to Park.

Petitioner relies on certain disclosures of Shibata’s first and second embodiments. Pet. 58-59; Shibata, [0016], [0047]. Petitioner asserts that Shibata, as depicted below, discloses “multiple ‘**separation portion[s] 62a**’ [that] pierce[] the drain-side select gate layer of the uppermost layer of the multiple conductive layers 70. ... This divides Shibata’s upper TSG (the **drain-side select gate layers**) into sub-TSGs (portions SDG0-SGD3)”:

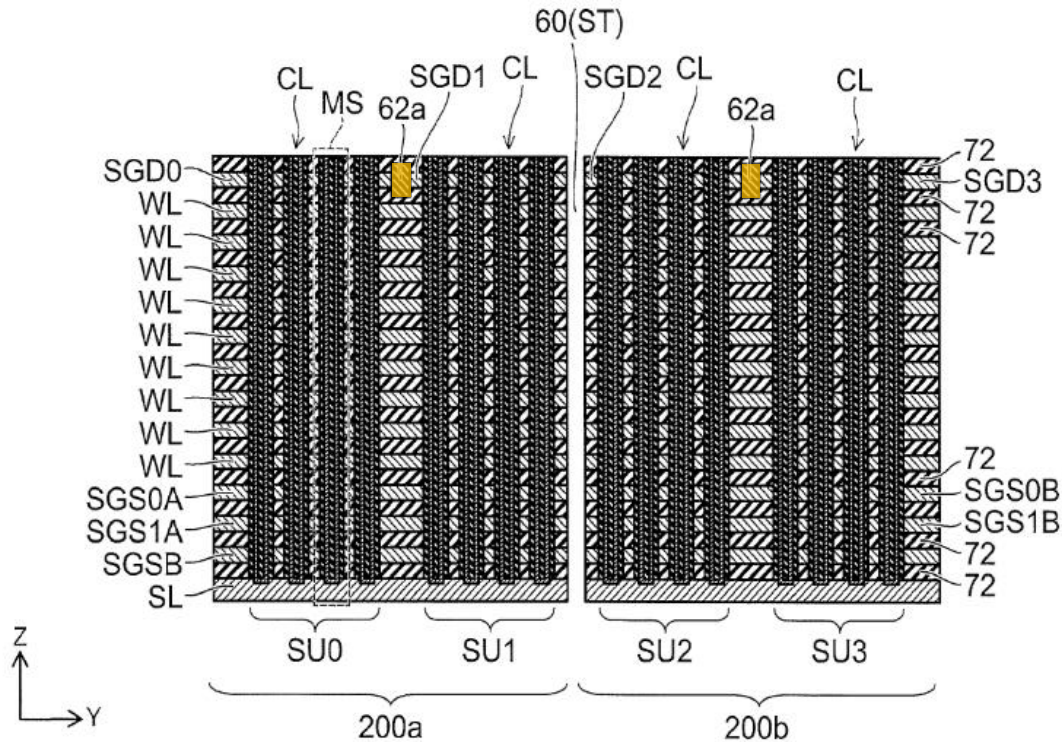


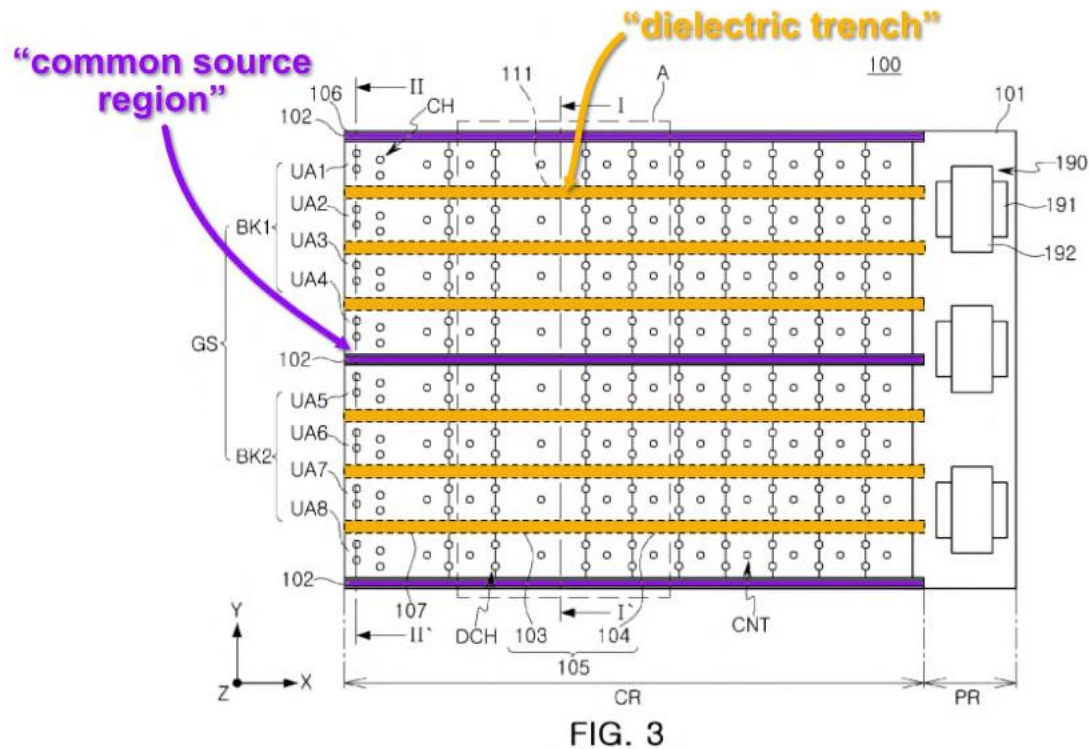
FIG. 16

Shibata, Fig. 16 (annotated); Pet. 58 (citing Shibata, [0090], [0166], Fig. 16).

Petitioner further contends that “Shibata’s “separation portion[s] 62a” traverse the entire length of its memory device for purposes of dividing the select gates.” Pet. 59 (citing Fig. 47A).

Petitioner then wrongly contends that based on the teachings of Shibata, “a POSITA would have eliminated Park’s second common source lines 105 and replace[d] them with **longer isolation insulating regions 111** with dimensions analogous to Shibata’s separation portions 62a.” *Cf.* Pet. 59-60. According to Petitioner, the “lengthened isolation insulating regions 111” would “span the

length of its device to completely, and by themselves, separate its BSG (the lower GSL) into sub-BSGs” as illustrated in Petitioner’s figure:



Pet. 60 (modifying Park, Fig. 3). Contrary to the Petitioner’s arguments, however, the resulting device fails to meet the claims, and a POSITA would not have combined Park with Shibata to arrive at the claimed invention.

1. A POSITA Would Not Have Applied Shibata’s Teachings to Park to Arrive at the Claimed Limitation

Petitioner wrongly contends that “a POSITA would have eliminated Park’s second common source lines 105 and replace[d] them with longer isolation insulating regions 111 with dimensions analogous to Shibata’s separation portions 62a.” Cf. Pet. 59-60.

First, Petitioner’s argument fails for at least the reasons that Shibata discloses that the **separation portions 62a** traverse only the **uppermost** drain-side select gate layer of the memory stack, such that they contribute to the separation of only the **top** select gate, rather than the **bottom** select gate. Shibata teaches that the separation portion 62a “divides the drain-side select gate layer into a first drain-side select gate SGD0 and a second drain-side select gate SGD1” of one sub-block and “divides the drain-side select gate layer into a third drain-side select gate SGD2 and a fourth drain-side select gate SGD3,” in another sub-block, as depicted in Figure 16 above, in the previous subsection. Shibata, [0166]. Shibata teaches that the separation portion 62a does not extend further to divide the source-side select gate layers (labeled “SGS0A,” “SGS1A,” “SGS0B,” “SGS1B,” and “SGSB” in Figure 16 above). Shibata provides no teaching that its **separation portions 62a** also traverse the lower source-side select gate layers such that they separate the bottom select gate layers. Nor does Shibata teach adding additional **separation portions 62a** to the source-side select gate layers to separate the bottom select gate layers. Indeed, Shibata expressly teaches not to extend the separation portions 62a to divide additional conductive layer, such as a bottom select gate:

“The separation portion 62a is disposed between the first string unit SU0 and the second string unit SU1 adjacent to each other in the Y-direction, **pierces only the drain-side select gate layer of the**

uppermost layer of the multiple conductive layers 70, ***and does not divide the other conductive layers*** of the multiple conductive layers 70.”

Shibata, [0137] (emphasis added). In other words, Shibata teaches separation portions 62a do not divide the bottom select gate layers, which are on the drain-side and are conductive layers of a memory device. And yet, Petitioner’s combined system requires exactly what Shibata fails to teach: to have the separation portions 62a extend into in a length direction of the substrate such as to reach and separate the ***bottom*** select gate (BSG) into a plurality of sub-BSGs. Petitioner’s cited disclosures from Shibata that teach separating the top select gate layers do not provide the required teaching. *See generally* Pet. 58-61.

Second, a POSITA would not have been motivated to make Petitioner’s proposed combination because Park teaches to not make such a combination. Park actively discourages elongating the isolation insulating layers because the longer paths by which the etching solution must flow could prevent the complete removal of the sacrificial layer and cause voids in the gate electrode layers GLs.⁶ *See*

⁶ In addition to showing that a POSITA would not have made the proposed change, these teachings in Park amount to a teaching away from the proposed combination. *See In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994) (“[I]n general, a reference will teach away if it suggests that the line of development flowing from the reference’s disclosure is unlikely to be productive of the result sought by the applicant.”); *see*

generally, Park, 15:35-16:49. Moreover, Park also discourages placing isolation insulating layers side-by-side, as they are in Petitioner’s modified Figure 3 of Park reproduced above, because it would block the flow of etching solution from the sides and again prevent the removal of sacrificial layers and formation of active layers. *Id.*

Referring to Figure 30, Park explains that sacrificial layers SL are “removed by an etching solution flowing through the first and second word line cuts WC1 and WC2.” Park, 15:35-37. These “word line cuts WC1 and WC2” correspond to the “regions in which common source lines” 102 and 105 are subsequently formed. Park, 15:20-22. In other words, the openings that later form the first and second common source lines are first used as the passage through which etching solution is administered to remove the sacrificial layers. These same word line cuts WC1 and WC2 are also used to deposit conductive material in the openings left by the removal of the sacrificial layer in order to later form the gate electrode layers GL. Park, 16:38-40. The problem recognized by Park is that the “isolation regions 311” (corresponding to Park’s Figure 11’s isolation insulating layer 111) prevents the flow of the etchant and conductive materials. *See* Park, 15:54-55 (referring to

also Arctic Cat Inc. v. Bombardier Recreational Prods. Inc., 876 F.3d 1350, 1360 (Fed. Cir. 2017).

“relatively long [flow] path above the isolation regions 311 in which the second word line cuts may be separated from each other”). That is, the problem is two-fold: first, because there is no word line cut in any of the layers above the isolation insulating layer, the flow path is relatively long; and second, because etching solution and metal do not flow through isolation insulating layers, there is no flow to regions between isolations insulating layers. *See* Park, Fig. 30 (illustrating the “inflow passage R” stemming from each of the word line cuts). Thus, where the “inflow passage of the [etching solution] is not properly secured, a portion of the sacrificial layer SL may remain without being removed.” Park, 15:56-59.

Similarly, this may generate a “void” when depositing the conductive material to form the BSG and word lines, the very same defect that Park seeks to avoid during fabrication. Park, 16:44-49.

Thus, Park teaches that Petitioner’s proposed modification, as illustrated below, would result in a memory device that has missing BSG where the sacrificial layer SL between the isolation insulating regions is never removed, and poorly formed word lines in the regions above the longer isolation insulating layers.

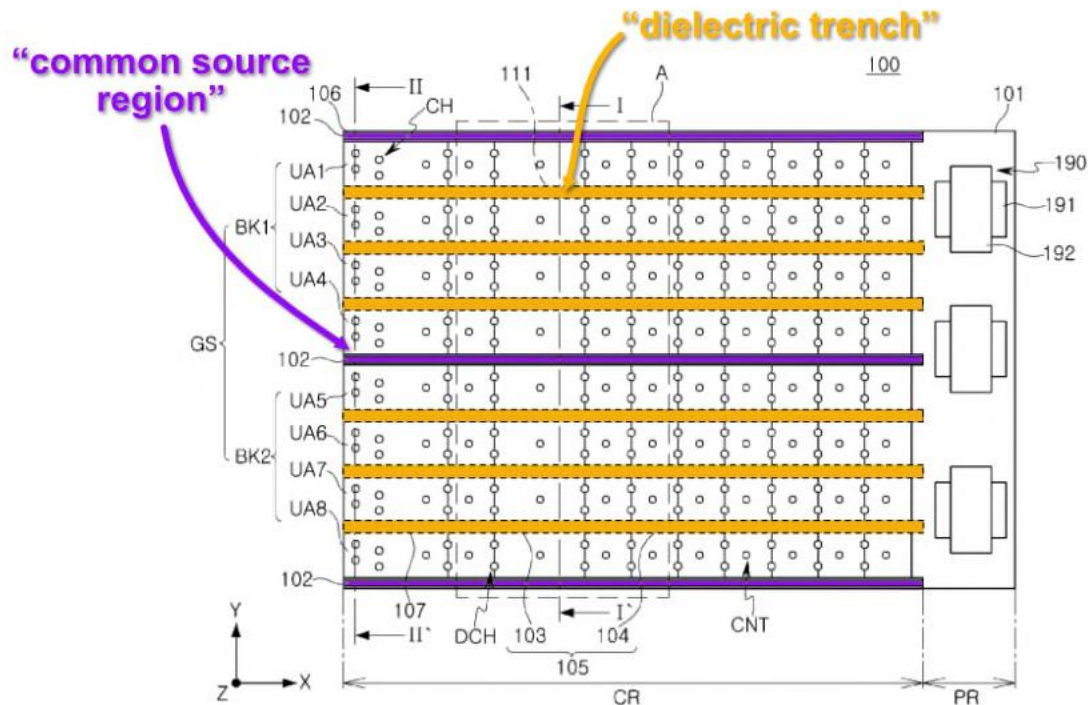


FIG. 3

Pet. 60 (Petitioner's demonstrative modifying Park, Fig. 3).

Indeed, Park is so concerned with this problem that, even for its short isolation insulating layers 111 (which are only as long as the distance between dummy channel and contact), Park proposes staggering the isolation insulating layers 111. Park, 15:60-16:2. Staggering, however, is not possible when the isolation insulating layers are modified to span the entire memory array as proposed.

Petitioner’s argument that Shibata resolves the operability problem by providing “drive circuits” (Pet. 62) is wrong for several reasons. Shibata provides no solution to Park’s concern that longer isolation insulating layers facing one another could prevent effective replacement of the sacrificial layer and generate

voids in the BSG and word lines. *See* Park, 9:31-35, 15:56-49, 16:44-49. Shibata also does not teach connecting multiple “drive circuits” to the source-side select gates, which are positioned in the harder to reach bottom layers of the stack, but instead teaches connecting multiple drivers to the drain-side select gates which are at the top of the stack. *See* Shibata, [0447]-[0448]. Finally, Shibata’s driver configuration is a fixed solution (which entails permanently connecting two drive circuits to certain drain-side select gates and only one drive circuit to others). *See* Shibata, [0447]-[0448]. As a fixed solution, connecting multiple drivers to certain drain-side select gates is practical for addressing predictable differences in resistances recognized by Shibata. Shibata, [0325] (recognizing that the “resistance of the drain-side select gate not adjacent to the slit ST easily can be higher than the resistance of the drain-side select gate adjacent to the slit ST”). Shibata’s fixed solution, however, is not practical for addressing unpredictable variations in word line quality due to variations in efficient flow paths.

Petitioner’s backup argument “replacing some—but not all—of Park’s common source lines” (Pet. 62-63) also fails. As illustrated below, even in Petitioner’s drawing there remains the problem facing isolation insulating layers (highlighted in teal) where there is no flow path from the “common source region” (marked purple by Petitioner):

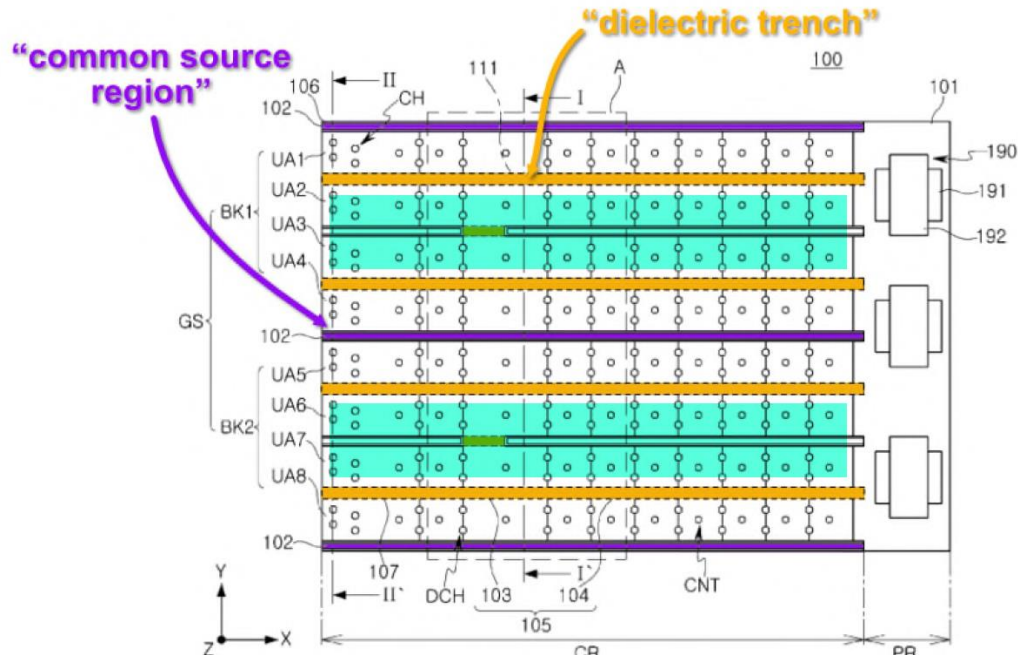


FIG. 3

And to the extent it is argued that it would have been obvious to alternate placement of Park's common source regions and the modified isolation insulating layers, this would still exacerbate the ineffective etching above these extended isolation regions that Park cautions against because as Park explains, the "path above the isolation regions [] in which the second word line cuts WC2 may be separated from each other" will be "relatively long." Park, 15:53-56. Regardless, such a solution is not based on any identified motivation, but on impermissible hindsight.

Third, a POSITA further would not have been motivated to replace Park's second common source lines 105 with longer isolation insulating regions 111 analogous to Shibata's separation portions 62a because doing so would reduce the

number of common source lines in the memory device. Instead of having a total of eight common source lines (see Park, Fig. 3 depicting two first common source lines 102 and six second common source lines 105), the proposed combined system would eliminate six second common source lines, leaving only two first common source lines. This results in a 75% reduction in the number of common source lines.

A POSITA would have understood that reducing the number of common sources lines would have several adverse effects on the memory device, including: (1) higher resistances in the remaining source lines leading to reduced read and write speeds, (2) increased heat generation owing to higher currents carried in the remaining source lines, (3) increased electrical stress on the remaining source lines leading to a reduced device lifespan, (4) significant voltage drops across the remaining source lines, adversely affecting the accuracy of reading, writing, programming and erasing operations of the memory device, and (5) increased crosstalk leading to more signal interference and increased error rates. *See e.g.*, Ex. 2001, 5 (stating “[d]ecreasing the CSL resistance can reduce the CSL noise”); Ex. 2002, 6 (explaining that CSLs should be “lines of low resistance” as to not adversely impact memory speeds); Ex. 2003, 2-3 (explaining that voltages on the CSL can impact the memory device speeds, such as read speed); Ex. 2004, 6-7 (stating “higher current densities may contribute, directly or indirectly” to device

degradation); Ex. 2005, 2 (stating that “[h]igher current densities ... give rise to greater heat generation and combine to increase electromigration failures”); Ex. 2006, 8 (stating “heat generation in [a] semiconductor increases as the current density increases”).

While reducing the number of common source lines may lead to a reduction of the memory array area, this would only exacerbate the very problem that Park intends to avoid. Specifically, reducing the number of common sources lines would only increase the long “inflow paths” and thus worsen any problems with etching of the sacrificial layer and deposition of the gate layers. A POSITA, therefore, would not have simply removed source lines because any purported benefit from reducing the memory array would have come at a significant trade-off in memory device performance, including in speed, thermal management, reliability, longevity, accuracy, and device scalability, which Petitioner fails to address. Accordingly, a POSITA would not have been motivated to modify Park as to remove the second common source lines, as Petitioner’s proposed combined system requires.

C. Ground 3: Petitioner Fails to Show That Shibata in View of Park Discloses or Renders Obvious Claim 1

Ground 3 of the Petition incorrectly argues that Shibata in view of Park renders claim 1 of the ’623 obvious. Petitioner generally relies upon the teachings

of Shibata for each of the limitations, but for limitation [1.e], the Petition sets forth two flawed modifications to Shibata's memory in light of Park's teachings.

For each of the limitation [1.b], [1.c], [1.d], and [1.f], which recites a "bottom select gate" (BSG), Petitioner argues that the "lower source-side select gate or SGS layers" of Shibata's second embodiment is the bottom select gate BSG, as illustrated below:

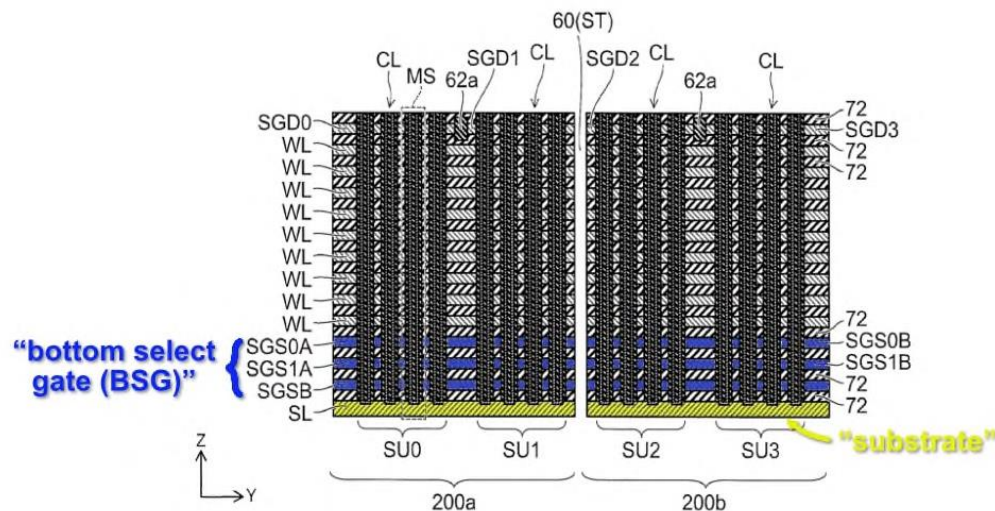


FIG. 16

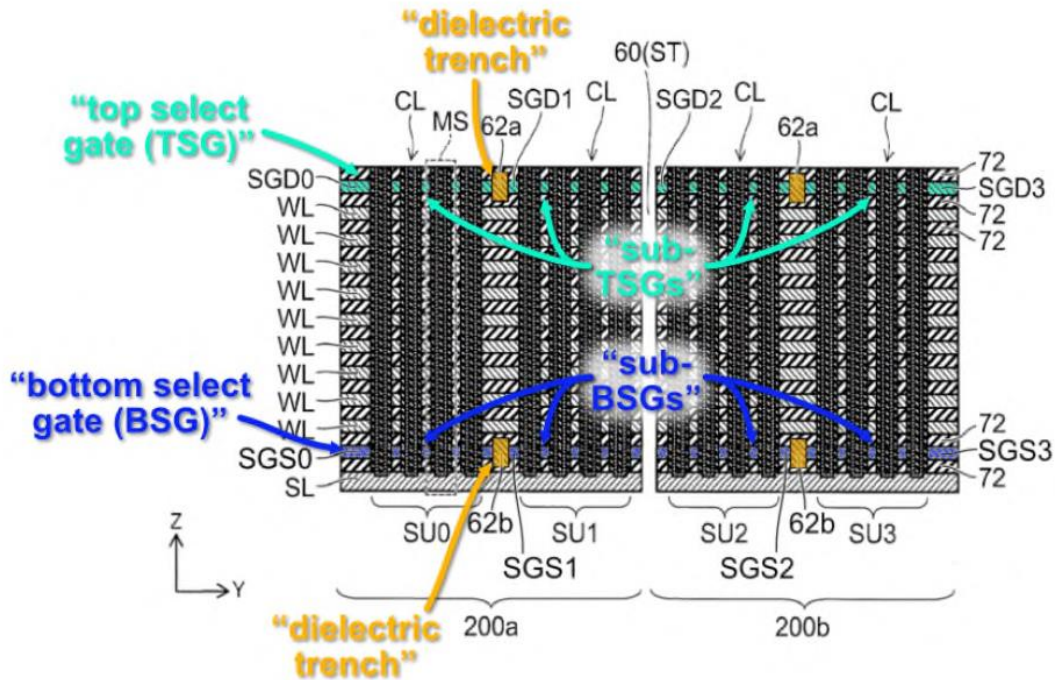
Pet. 65-67 (Petitioner's annotations).⁷ As shown in the above figure, the purported bottom select gate includes three layers: "SGS0A," "SGS1A," and "SGSB."

Shibata's three lower source-side select gates provides selective connection of the

⁷ Note that Shibata uses the acronym "SL" to refer to "source layer," Shibata's purported substrate, whereas Park uses the same acronym, SL, to refer to "sacrificial layer."

four string units SU0-SU3 to the source layer without relying on a dielectric trench. See Shibata, Fig. 16, Fig. 22A, [0196]-[0218]. For the purposes of limitation [1.e], which recites a “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” Petitioner further relies on Shibata’s teachings of “separation portions.” Pet. 72 (citing Shibata, [0107], [0110]). Shibata, however, teaches that these separation portions “pierce[] only the drain-side select gate layer of the **uppermost** layer of the multiple conductive layers 70”—not the source-side select gate layers, which are the **lowermost** layer(s). Shibata, [0090].

In an attempt to meet limitation [1.e], Petitioner abandons its mapping of Shibata for limitations [1.b], [1.c], [1.d], and [1.f], and instead argues it would have been obvious to “employ a single ‘bottom select gate (BSG)’ (lower source-side select gate or SGS layer) with ‘dielectric trenches’ (new additional separation portions 62b) ‘separate[ing] the BSG’ into ‘sub-BSGs’ (new layer portions SGS0-SGS3)” as illustrated in the Petition’s reimagined diagram:



Pet. 76 (Petitioner’s demonstrative). Specifically, Petitioner argues that (1) it would have been obvious to use Shibata’s “separation portion” (used to divide its upper drain-side select gate) “in connection with its lower source-side select gate”; and (2), in light of Park, it would have been obvious to “replace[]” “Shibata’s multiple bottom select gate layers ... with a single divided gate layer.” Pet. 74-78.

Petitioner's combination fails for at least two reasons. First, Petitioner has failed to show that Shibata in view of Park teaches or renders obvious each and every limitation of claim 1. And second, a POSITA would not have been motivated to make the multiple proposed modifications to Shibata necessary to meet the claim limitation.

1. Petitioner Fails to Map Its Proposed Combination to Every Element of the Challenged Claims

As an initial matter, Petitioner has failed to meet its burden to show that the purported bottom select gate of the proposed combination of Shibata and Park meets each and every requirement of the claims.

As previously discussed, for the purposes of limitations [1.b], [1.c], [1.d], and [1.f], Petitioner relies upon Shibata's second embodiment lower source-side select gate or SGS layers, including layers SGS0A, SGS1A, and SGSB. *See generally*, Pet. 65-71, 79-81. However, for the purposes of limitation [1.e] alone, Petitioner argues that "Shibata's multiple bottom select gate layers would be replaced with a single divided gate layer" (Pet. 77)—Petitioner fails to show that each of the other limitations would be met by such a modified bottom select gate. *See, e.g.*, Pet. 65-67 (addressing element [1.b], which recites "a bottom select gate (BSG) disposed over the substrate"), 67-70 (addressing element [1.c], which recites "a plurality of word lines positioned over the BSG with a staircase configuration"), 70-71 (addressing element [1.d], which recites "a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines"), 79-81 (addressing element [1.f], which recites "one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the

BSG, the plurality of word lines, and the plurality of insulating layers”). For this reason, Petitioner has failed to meet its burden of proof for Ground 3.

2. Petitioner Fails to Show That a POSITA Would Have Been Motivated to Apply Park’s Teachings to Divide Shibata’s Lower Gate Layer into Multiple Portions

Petitioner’s alleged motivations to combine Park’s teachings to Shibata rely on conclusory arguments and impermissible hindsight.

As explained in §VI.B.1, Shibata’s separation portion 62a separates the uppermost drain-side select gate layer, *i.e.*, the purported top select gate—not the source-side select gate layers, *i.e.*, the purported bottom select gate. Recognizing this shortcoming of Shibata, Petitioner argues that a POSITA would have found it obvious to do two things: (1) rather than dividing just the upper drain-side select gates using separation portions 62a, Shibata would employ “new additional separation portions 62b” to also divide the BSG into sub-BSGs (Pet. 74); and (2) rather than employ multiple lower source-side select gate layers, “Shibata would employ a single ‘bottom select gate (BSG)’” (Pet. 74-75). Petitioner’s proposed modifications to Shibata, however, rely upon the flawed premise that Park provides an alternative to Shibata’s multiple bottom select gates, which “facilitate control on a string unit basis” and thus would motivate the changes. Pet. 74-75. Specifically, Petitioner points to Park’s isolation insulating layers 111 that purportedly “divide[]

a single lower gate layer into multiple portions.” Pet. 75 (citations omitted). But Petitioner’s obviousness argument fails for several reasons.

First, Petitioner’s obviousness analysis is fraught with flawed premises and conclusory arguments, and ultimately succumbs to reliance on impermissible hindsight. For example, Petitioner’s primary motivation is that “[w]hile the multiple bottom select gates can facilitate control on a string unit basis, a POSITA would have recognized that they require additional manufacturing steps and make Shibata’s memory array taller” and that this would have motivated consideration of other design alternatives like Park. Pet. 74-75 (*citing* Ex. 1003, ¶¶ 377-380). The only support given for this flawed and conclusory argument, however, is nothing more than the a near-verbatim statements made by its expert. Ex. 1003, ¶¶ 377-380. Neither Petitioner nor its expert provides any other support.

Second, Petitioner’s argument is also flawed because it attempts to equate Park’s isolation insulating layers 111 and Shibata’s separation portion 62a. As described in greater detail in §VI.A.1, Park’s isolation insulating layers are not trenches that separate the bottom gate structure, but instead are short H-cuts that just “close the gaps in common source lines 105.” Pet. 31. Moreover, Park’s isolation insulating structures are in an entirely different region of the memory than Shibata’s separation portions. As previously discussed, Park’s **isolation insulating structures** are short structures in the staircase region, not in the array region:

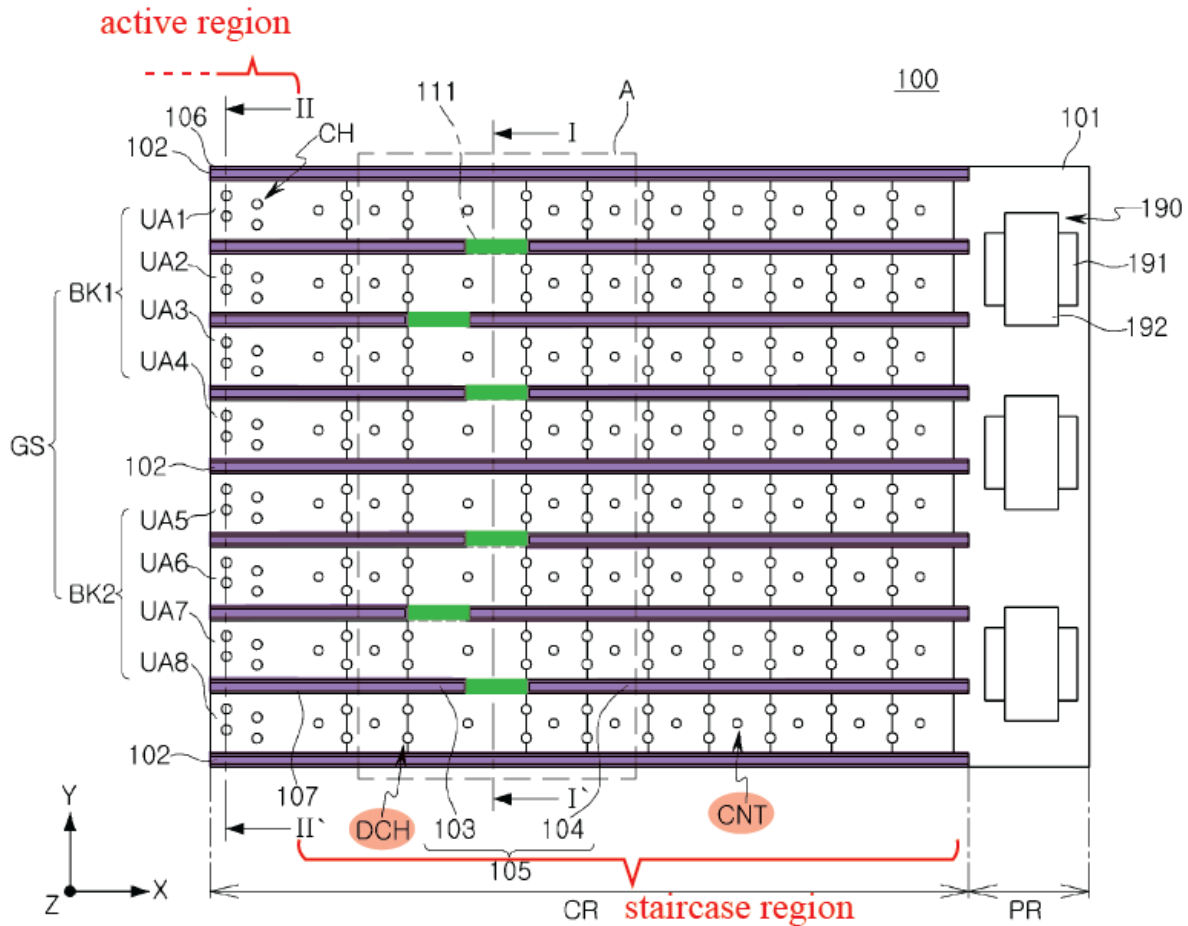


FIG. 3

Park Fig. 3 (showing **isolation insulating structures 111** between dummy channel structures (DCH) and an adjacent contact (CNT) to the word lines in the staircase region, not the active region); *see also* Park, 10:56-60 (“The isolation insulating layer 111 may be disposed below the connecting electrodes 129b to 129i connecting the unit electrodes of the gate electrode layers 120, forming the word lines, to each other.”). On the other hand, Shibata’s **separation portions** extend the length of the array region of the memory device:

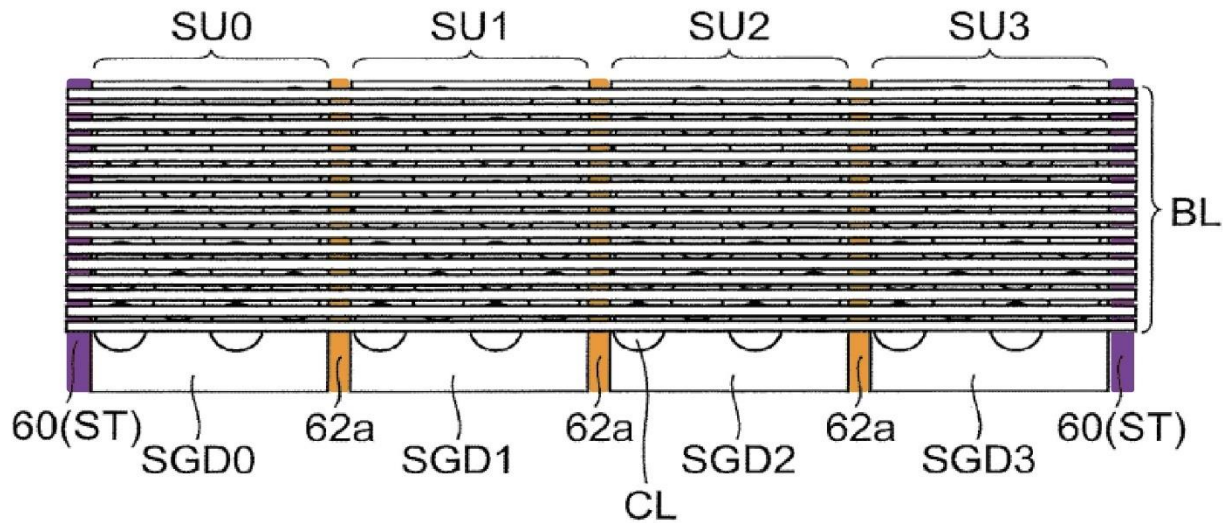


FIG. 47A

Shibata, Fig. 47A.

Indeed, as Petitioner admits, “Shibata does not reference a staircase.” Pet. 69. Therefore, even if a POSITA would have recognized that Shibata’s three-layer bottom gate design “require[d] additional manufacturing steps and ma[de] Shibata’s memory array taller” (Pet. 74), that does not mean a POSITA would look to Park’s unrelated teaching directed to short isolation insulating structures 111 in the staircase region to modify Shibata. Absent a motivation to apply Park’s teachings, Petitioner’s obviousness argument relies on impermissible hindsight. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”).

Third, Petitioner's argument that "it was well known that trenches of dielectric material could be used to divide select gates" (Pet. 78), also falls flat. Not one of the four references cited by Petitioner shows it was well known to use trenches to divide both the top and bottom select gate (as set forth by Ground 3). Indeed, three of them do not even disclose using the purported dielectric trenches in the bottom select gate. *See* Ex. 1016, 6:5-15, 10:15-18, Fig. 4A (employing a "insulating layer 173" in the "uppermost gate electrode layer 136"); Ex. 1017, 7:40-42, Fig. 3 ("employing a "cutting insulation pattern 118" in the upper "string selection gate electrodes 202."); Ex. 1018, [0058], Fig. 4B (employing "insulating separation pattern 50" in the "upper electrodes ELb located at the highest level"). As for the fourth reference, at best, it discloses similar isolation insulating regions as Park, which are no more than short H-cuts, but in the staircase region. *See* Ex. 1019, Figs. 21-22, Fig. 24, [0154], [0160]-[0161]. As such, none of the references cited by Petitioner or Petitioner's experts provides motivation to use Shibata's separation portions to divide both upper drain-side select gates and lower source-side select gates.

Lastly, contrary to Petitioner's conclusory argument that the proposed combination "would reduce the number of needed manufacturing steps," this is unsupported by the evidence. Pet. 77. Once again, the only support cited by Petitioner is a near-identical statement by its expert. But neither Petitioner nor its

expert cite any evidence. Indeed, on the face of it, the statement is wrong. The proposed combination, which requires the formation of additional separation regions 62b in the source-side gate layer would at minimum require additional photolithography steps, etching steps, and filling procedures that neither Petitioner nor its expert considered.

As the above reasons demonstrate, modifying Shibata to have a single-layer BSG results in significant complexity and would have further dissuaded a POSITA from applying Park's teachings to the memory device, let alone from having a reasonable expectation of success.

VII. CONCLUSION

The Petition should be denied institution, as Petitioner has failed to establish a likelihood that it would prevail with respect to any of the Challenged Claims based on the Grounds presented in the Petition.

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Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(c)(1). According to the word-processing system's word count, the brief contains 9,946 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: July 29, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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