

Applications of AFM in semiconductor R&D and manufacturing at 45 nm technology node and beyond

Moon-Keun Lee^{*a}, Minjung Shin^b, Tianming Bao^a, Chul-Gi Song^b, Dean Dawson^a, Dong-Chul Ihm^b, Vladimir Ukraintsev^a

^aVeeco Instruments Inc., 112 Robin Hill Rd., Santa Barbara, CA 93117, USA;

^bSamsung Electronics Co., Ltd. San#16 Banwol-dong, Hwasung-city, Gyeonggi-do, 445-701, Korea

ABSTRACT

Continuing demand for high performance microelectronic products propelled integrated circuit technology into 45 nm node and beyond. The shrinking device feature geometry created unprecedented challenges for dimension metrology in semiconductor manufacturing and research and development. Automated atomic force microscope (AFM) has been used to meet the challenge and characterize narrower lines, trenches and holes at 45nm technology node and beyond. AFM is indispensable metrology techniques capable of non-destructive full three-dimensional imaging, surface morphology characterization and accurate critical dimension (CD) measurements. While all available dimensional metrology techniques approach their limits, AFM continues to provide reliable information for development and control of processes in memory, logic, photomask, image sensor and data storage manufacturing. In this paper we review up-to-date applications of automated AFM in every mentioned above semiconductor industry sector. To demonstrate benefits of AFM at 45 nm node and beyond we compare capability of automated AFM with established in-line and off-line metrologies like critical dimension scanning electron microscopy (CDSEM), optical scatterometry (OCD) and transmission electronic microscopy (TEM).

Keywords: atomic force microscopy, in-line metrology, three-dimensional imaging, surface morphology, process control, CDSEM, TEM, optical scatterometry

1. INTRODUCTION

As the integrated circuit technology advances to the 45 nm node and beyond in semiconductor industry, there is increasing need to search for the complementary metrology to ensure integrity of critical process control. It is because metrologists in the field have recently noticed the weakness of scanning electron microscopy (CDSEM) and optical scatterometry (OCD) which have been considered as dominant metrologies for in-line control of various processes like line/trench etching, recessed features, holes, etc. Precision as a metric for metrology quality is replaced with more comprehensive measurement uncertainty in the 2007 edition of international technology roadmap for semiconductors (ITRS) [1]. Several new components of uncertainty besides the precision have to be considered. Today two of them, sampling uncertainty and sample-to-sample measurement bias variation, are often dominant in the combined uncertainty of measurement. An automated AFM is a promising candidate metrology which is capable of sub-nanometer sampling uncertainty and bias variation. As a result of this, for quite some time AFM has been adopted by the industry as a reference metrology in process control of semiconductor wafer manufacturing.

Table 1 lists various dimensional metrology techniques available today [2]. Due to its unique characteristics 3-dimensional AFM (3D-AFM) has been demanded by the industry of memory, logic, photomask, data storage and CMOS image sensor (CIS). This article focuses on uniqueness and merits of AFM with respect to CDSEM, OCD and also off-line metrologies like TEM and cross-section SEM (X-SEM).

Table 1. Comparison of 3D-AFM with other dimension metrology techniques.

Collateral	CDSEM	OCD	Dual-Beam	TEM	3D-AFM
Areas of Use	Process control OPC & RET modeling Engineering	Process control Litho evaluation	Failure analysis Engineering	Reference tool Failure analysis Engineering	Accurate reference tool Engineering Process control OPC & RET modeling
Sample interaction	Shrinking Charging Carbonization	Bleaching (especially for spectral tools)	Destructive Gallium contamination Shrinking	Destructive Shrinking Warping	Non-destructive No contamination No sample dependent bias
3D Capability	2D [XY]	2D [XZ] (3D [XYZ] is under test)	2D [XZ]	2D [XZ] or [XY]	3D [XYZ]
Cost per site	Low	Lowest	High	Very high	Moderate
MAM time	4-5 sec	2-4 sec	30-90 sec	2-4 hours	10-40 sec
Precision (Gate CD)	ca. 0.5 nm (3s)	ca. 0.3 nm (3s)	ca. 1-2 nm (3s)	ca. 1-2 nm (3s)	ca. 1.0 nm (3s)
Uncertainty (Gate CD)	ca. 2.0 nm (3s)	ca. 2.0 nm (3s)	ca. 2.4 nm (3s)	ca. 2.2 nm (3s)	ca. 1.0 nm (3s)
Uncertainty (Gate SWA)	ca. 0.8 deg (3s)	ca. 0.7 deg (3s)	ca. 0.6 deg (3s)	ca. 0.6 deg (3s)	ca. 0.2 deg (3s)
Limitations	Less than 15 nm CD Variable bias for 2D & dense features Material & profile bias dependence	Gate SWA bias starting 45 nm Bottom CD bias starting 45nm STI CD variable bias starting 65nm Model parms cross-correlation	Limited sampling Shrinking Charging Sample dependent edge definition	Limited sampling Shrinking Warping Sample dependent edge definition	Less than 35 nm spaces 10 nm blind bottom zone

2. COMMON APPLICATIONS

2.1 Critical Dimension (CD), Line Width Roughness (LWR) and Line Edge Roughness (LER)

Demand for CD and shape analysis of gate, resist and STI is rapidly growing at 45nm technology node and beyond. TEM and CDSEM are widely used for CD applications today. However, turn-around time for TEM is from several hours to up to several days. This is often unacceptable. CDSEM is much faster but does not provide any vertical line/trench profile information. 3D-AFM offers detailed line profile information based on multiple cross-sections within a minute (see Fig. 1). At the same time uncertainty of 3D-AFM data is superior to TEM since local sampling uncertainty of the mean line CD is minimized through extensive averaging along the line.

Linewidth variation becomes more and more critical for lithographic and etching process steps at 45nm node and beyond. OCD averages LWR/LER and thus can not monitor CD variation. CDSEM provides roughness information averaged along line/trench vertical profile and has tendency to underestimate LWR/LER. As shown in Fig. 1 (c), 3D-AFM offers full 3D, nanometer resolution, accurate and repeatable LWR/LER data.

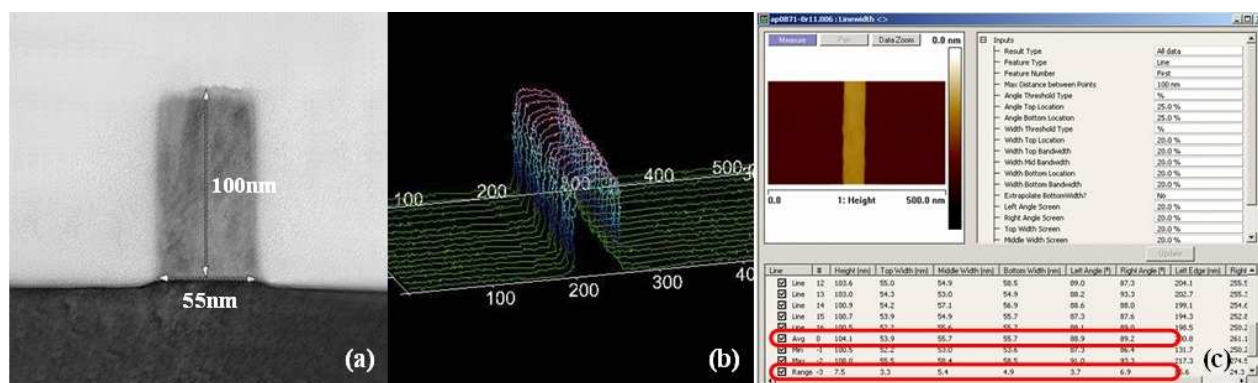


Fig. 1. (a) TEM image of isolated poly gate line, (b) 3D-AFM image of the same poly gate line and (c) linewidth analysis data of AFM tool.

2.2 Sidewall Roughness

Sidewall roughness (SWR) is an essential characteristic of advanced photoresist for smaller design nodes. SWR impacts interconnect barrier metal integrity and electrical properties of a metal lines as well as transistor gate performance. Nevertheless it is difficult to measure photoresist SWR using current in- and off-line metrology techniques. TEM and X-SEM can not reliably measure photoresist SWR due to resist shrinkage and poor statistics. CDSEM and OCD are not sensitive to sidewall roughness. As reported by J. Foucher et al. [3] [4], 3D-AFM provides high resolution, repeatable measurements of LWV, LER and SWR (Fig. 2). This data can then be used by lithography engineers to accelerate process development through adopting 3D-AFM metrology.

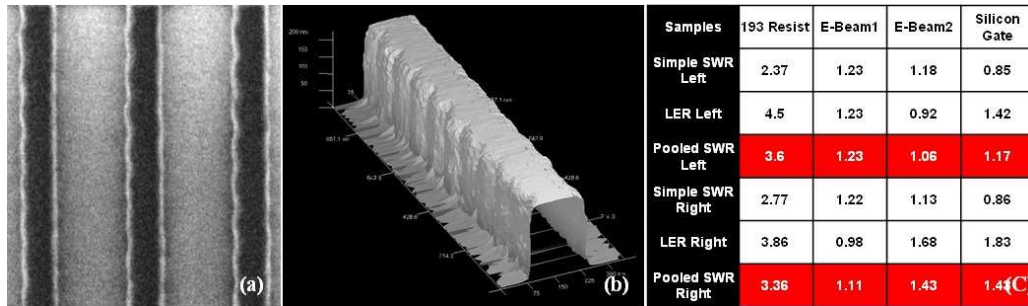


Fig. 2. (a) CDSEM image of poly gate lines, (b) 3D-AFM image of one poly gate line and (c) line edge roughness and sidewall roughness data of gate lines [4].

2.3 Shallow Trench Isolation (STI) Profile, Effective Field Height (EFH) & Divot Analysis

STI profiling, including depth, line/trench CD and sidewall angle, is an important process control step required for stable performance of devices at 45 nm node and beyond. The top corner Si rounding of STI may significantly impact threshold voltage (V_t) of the transistor through an increase of the leakage current. However, the top corner Si rounding is not easily monitor in-line. Off-line X-SEM and TEM are widely used today for the top corner Si rounding. OCD could be a good metrology choice for array of cells (example: DRAM). However, OCD is limited to repeated patterns only. Today, it is not an in-line solution for STI monitoring in peripheral area of memory, cell area of SRAM or logic devices. 3D-AFM can directly characterize the top corner Si rounding as well as full sidewall profile of any device as shown in Fig. 3 (a).

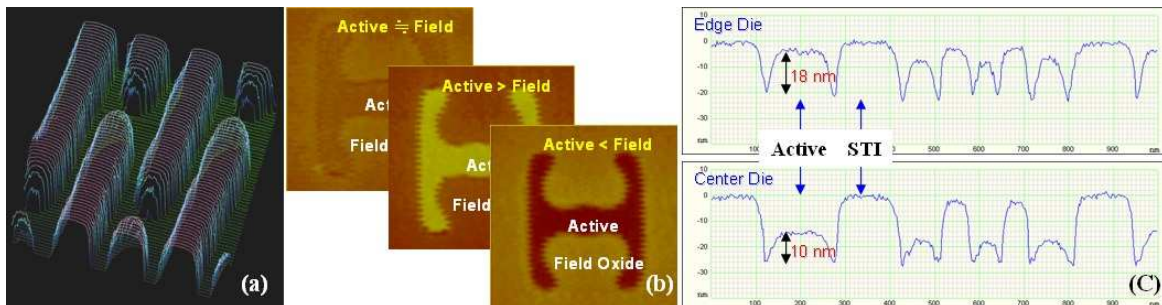


Fig. 3. (a) 3D-AFM image of STI array in cell area of DRAM device, (b) AFM images of EFH for various CMP conditions and (c) divot profiles by AFM for logic circuit.

Since chemical-mechanical polishing (CMP) has been introduced to STI process module, product yield is strongly impacted by post CMP wafer uniformity. The effective field height (EFH) is field silicon oxide height with respect to active silicon area. EFH out of specification is a very common reason for SRAM and logic failure. After CMP, the EFH can vary across the wafer. Changes in the EFH significantly impact the integrity of the following gate patterning as well as poly-Si thickness and, therefore, threshold characteristics of transistors.

A divot is a small notch observed between the STI (silicon oxide) and active area. The divot forms during wet STI processing. The STI divot strongly impacts the performance of narrow channel transistors. Therefore, in-line monitoring of divot becomes essential at 45 nm node and beyond.

The STI Divot and EFH present at most, only a few nanometers of topography. To add to this metrology challenge, the post CMP EFH can change topography within a single wafer. CD-SEM and OCD are barely, if at all, capable of measuring such small changes in topography. TEM and X-SEM are capable but are, of course, destructive. The AFM is

sensitive to topography changes less than a nanometer and is non-destructive. This permits the use of AFM as an inline monitor that is able to measure individual devices at the STI module. As shown in Figs. 3 (b) and (c), AFM can characterize divot depth and width, planarity of field oxide & active area as well as measure EFH and its polarity.

2.4 Cu CMP Process and Plug Recess

Cu CMP process is needed at 45 nm node and beyond for memory devices. However, Cu CMP process for 45 nm memory is not fully characterized and understood yet. Stylus-type profiler has a lateral resolution limit and high shearing force preventing its use for 45 nm CMP process characterization. AFM profiler is a superior metrology tool capable of global planarity, local topography, dishing & erosion and roughness measurements. Measurements can be done in a single mm-long scan as showed in Fig. 4. The depth of Cu plug recess has an impact on the following interconnection processes like low-k deposition or Cu deposition. With diameter of the plug as small as the node of technology AFM becomes the only metrology for plug recess control at 45nm technology node and beyond.

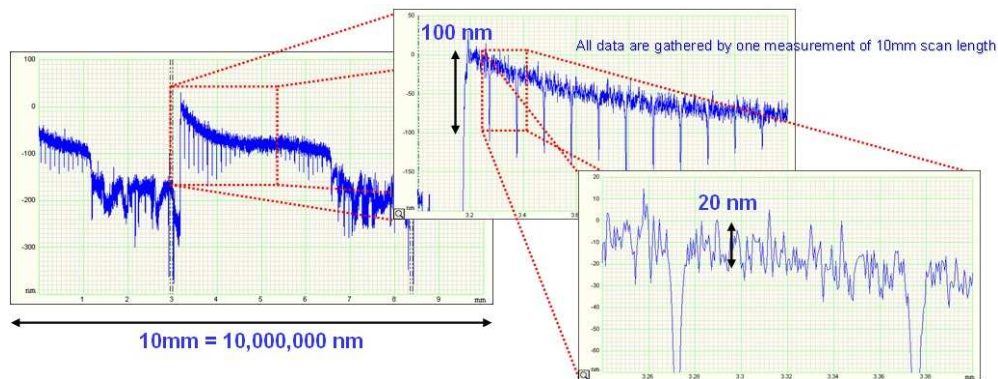


Fig. 4. Profile of AFM image in profiler mode crossing cell and peripheral area of DRAM device.

2.5 Roughness Control

Surface roughness control is required at various steps through semiconductor device manufacturing. Some of them are: SOI and Si substrates, epitaxial SiGe, poly-Si, low-k and high-k dielectrics, W, Al and Cu metals as deposited and post-CMP. The need of across wafer roughness uniformity monitoring is increasing with every technology node. AFM is a complete metrology solution for reliable roughness monitoring. Fig. 5 (a) and (b) show examples of roughness analysis.

Result of AFM roughness measurement strongly depends on probe sharpness. Conical shape Si probes have been used for roughness measurements historically because of their small apex radius of curvature and low cost. However, Si probe lifetime is too short for high-load manufacturing use and even for R&D. As demonstrated by Fig. 5 (c), significant progress in probe lifetime is recently achieved through employment of cylindrical shape probes made of the hard materials like carbon nanotube (CNT) or high-dense carbon (HDC).

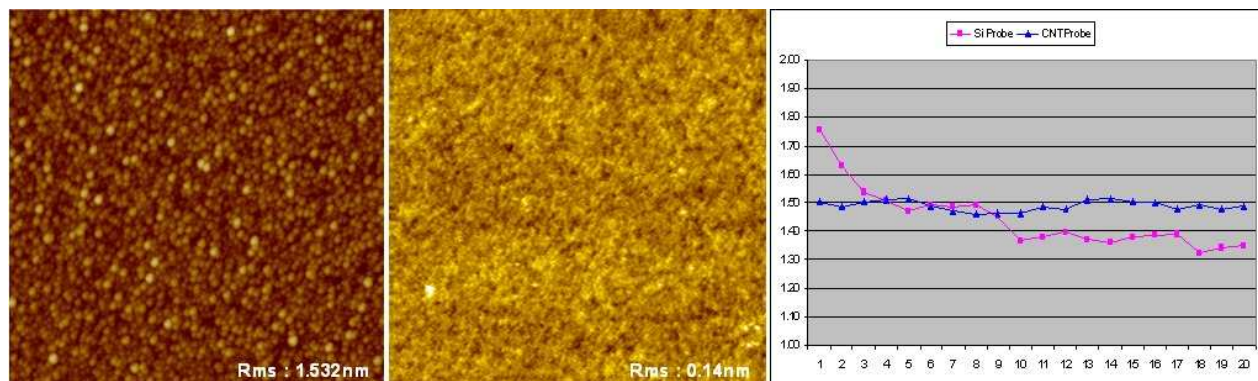


Fig. 5. (a) AFM image of 20 nm thickness W, (b) AFM image of bare Si wafer and (c) the repeatability of AFM roughness measurement on W thin film using conical Si and CNT probe.

2.6 Reference Metrology System (RMS)

As mentioned above, the 2007 edition of ITRS has instigated a move away from measurement precision as a metrology acceptance metric toward more relevant measurement uncertainty. This move reflects the wide concern of industry about limitations of current CD metrology tools such as OCD and CDSEM which have significant hidden measurement bias variation. Additional off-line metrologies, which historically were used for accurate line CD and profile measurements, are no longer suitable for process control since unpractical number of measurements (samples) is required to achieve required low measurement uncertainty. AFM as a complementary non-destructive reference metrology helps to overcome limitations of current baseline CD metrology techniques and prolong their use. AFM can be used to establish NIST-traceability of OCD and CDSEM measurements for various materials such as silicon, resist, dielectrics and metals.

Good example of reference metrology application of CD-AFM is measurement conducted on the single crystal critical dimension reference material (SCCDRM) by the NIST scientist R. Dixon [5]. In this work 3D-AFM has been used as a reference measurement system (RMS) for traceable measurements of height and width of crystalline Si line. High resolution transmission electron microscopy (HRTEM) was used as an indirect method of AFM tip width calibration. The AFM and HRTEM results which were used for the tip width calibration are shown in Fig. 6.

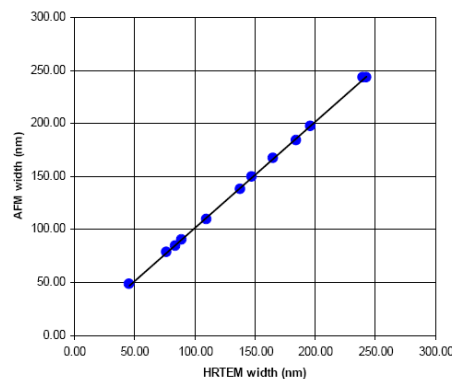


Fig. 6. Correlation between 3D-AFM and HRTEM measurements. The observed slope is consistent with unity – indicating that the two methods have consistent scale calibration. The average offset between the results was used to correct the tip width calibration [5].

3. MEMORY DEVICE APPLICATIONS

3.1 Fin Field Effect Transistor (Fin-FET)

Fin-FET structure is one potential solution for memory and logic devices at 45 nm node and beyond. In the double-gated Fin-FET (see Fig. 7) the fin area between two gates acts as a channel and the fin height & width correspond to the channel width & thickness, respectively. Control of the fin dimensions is critical to device performance. Variability in fin dimensions arises from line height, width and profile variations introduced during fin formation. Top down 2D CDSEM is not sufficient for 3D fin CD control. 3D-AFM is a good candidate for fin CD metrology with sub-nm uncertainty.

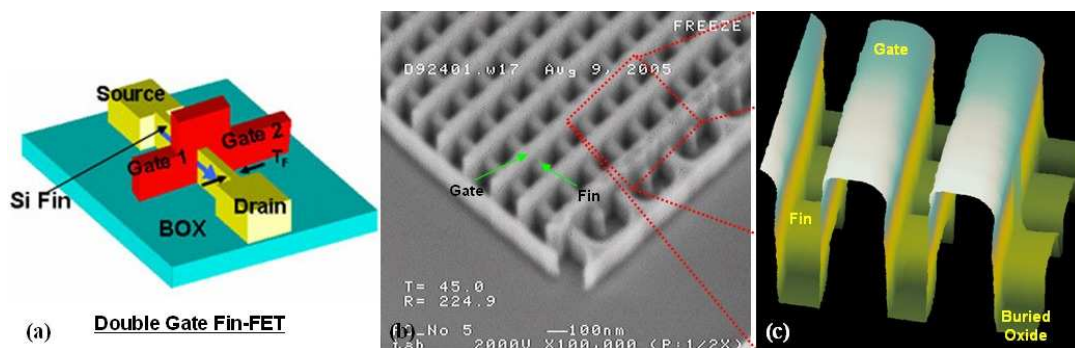


Fig. 7. (a) Schematic diagram of Fin-FET [6], (b) SEM image of FinFET structure on oxide layer and (c) 3D-AFM image of FinFET.

3.2 Selective Epitaxial Growth (SEG)

Elevated source/drain is a dual solution which reduces the junction leakage and also so-called short channel effect. During selective epitaxial growth, however, decreased thickness of epitaxial layer typically occurs at interfaces between the epitaxial layer and the dielectric spacer or field oxide. Specifically, thinner faceted regions cause localized deeper dopant penetration during ion implantation and that in turn diminishes SEG benefits. Therefore, profile of Si epitaxial layer should be monitored. OCD is not sensitive to the profile variation, while in-line 3D-AFM can image facets of the epitaxial layer and characterize SEG process as shown in Fig. 8 [7].

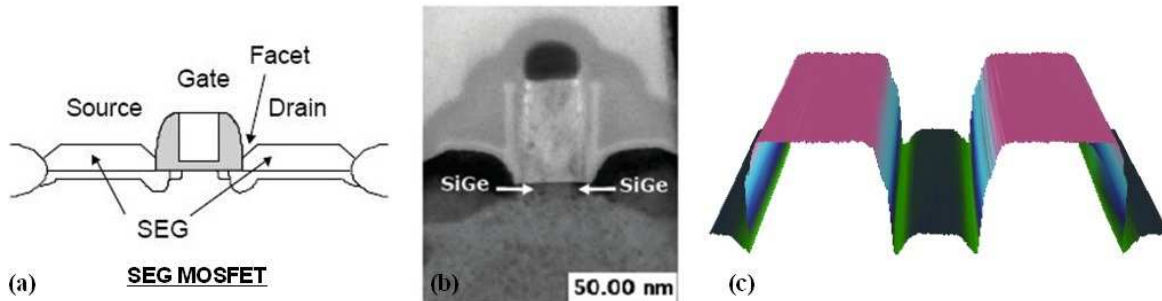


Fig. 8. (a) Schematic diagram of SEG MOSFET device, (b) X-SEM image of SiGe SEG MOSFET structure and (c) 3D-AFM image of faceted regions.

3.3 Common Source Line

A pair of common source lines (CSL) is intermittently located next to 32 gates array in flash device. Profile of the CSL needs to be monitored at each process step to assure lines of low resistance which impacts memory speed. As of now, process engineers measure dense lines in peripheral area using OCD and correlate results to CSL in cell area. However, micro-loading effects become non-linear and less predictable at 45 nm node and beyond. As a result, engineers are facing new challenges in CSL process control. CDSEM is used for line CD control only and can not characterize CSL profile. 3D-AFM provides CSL process control including height, CD and sidewall angle. AFM can measure CSL directly and do that at any process step (Fig. 9).

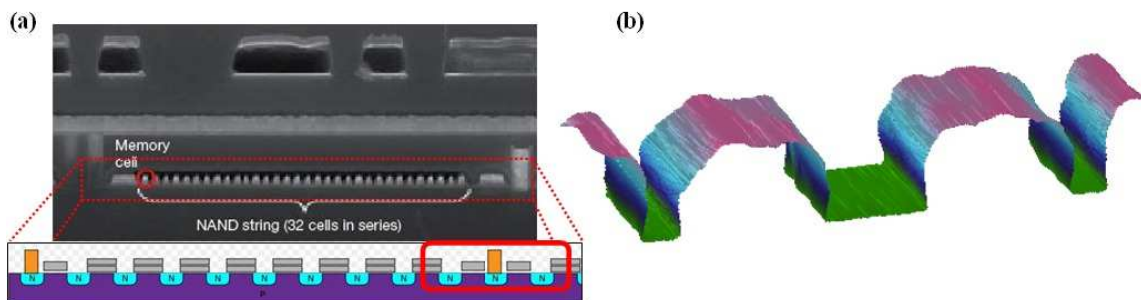


Fig. 9. (a) Schematic diagram of NAND string of flash memory device [8] and (b) 3D-AFM image of CSL in red line box.

3.4 Storage Node, Contact Hole and Via

Depth monitoring of storage nodes, contact holes and interconnect vias becomes a critical metrology to assure hole's bottom opening. Failure to open the bottom causes fatal yield drop. CDSEM and OCD have difficulty to detect a few nanometer thick residues at the bottom of extremely narrow hole. AFM operating in deep trench (DT) mode provides accurate non-destructive depth metrology over a wide range (Fig. 10).

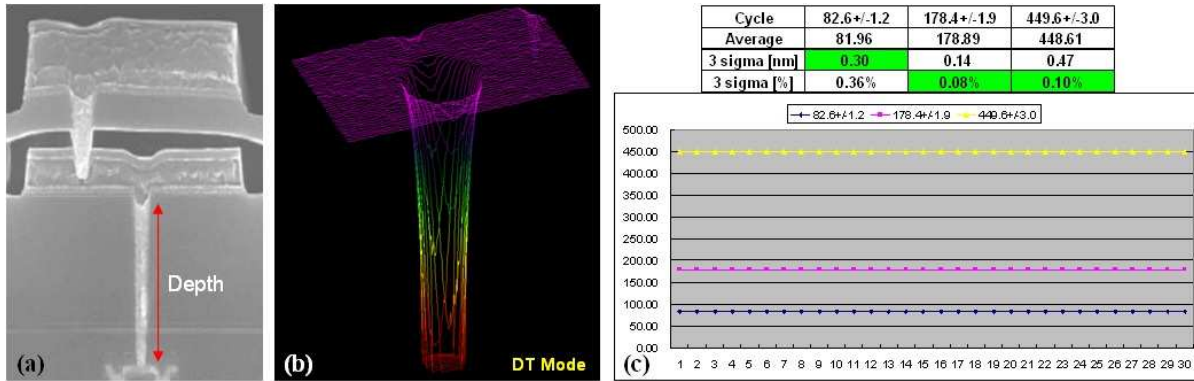


Fig. 10. (a) X-SEM image of contact hole, (b) DT mode AFM image of contact hole and (c) AFM depth measurement repeatability demonstrated on SI-traceable standards.

3.5 Poly-Si and W Etch-Back

Metrology of recessed contact hole after etch-back process (Fig. 11) is becoming an issue as diameter of the contact is getting smaller. OCD has a difficulty to measure the recess. X-SEM can do that but sampling uncertainty of the measurement is high since recess distribution could be noticeably wide. AFM offers non-destructive recess metrology with prudent statistics as shown in Fig. 11 (c).

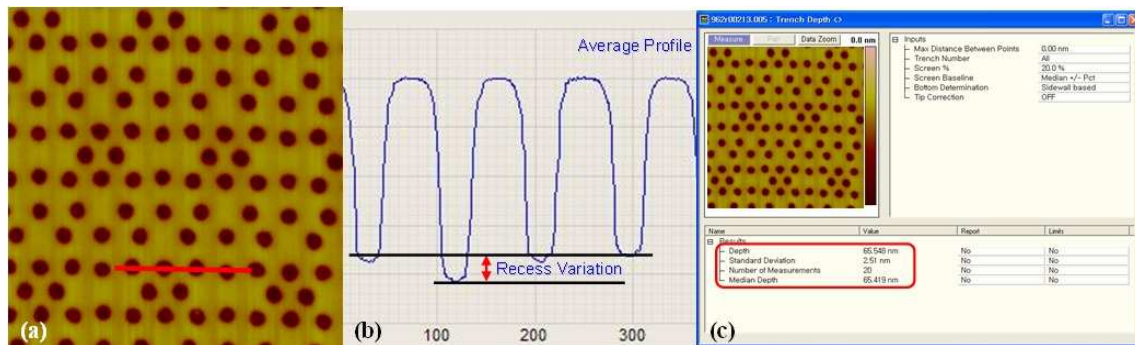


Fig. 11. (a) AFM image of etch backed contact hole array, (b) sectional profile of AFM image showing recess variation and (c) the statistical and quantitative results of recessed poly-Si contact holes by special analysis function of AFM tool.

4. LOGIC DEVICE APPLICATIONS

4.1 Recessed Gate

Importance of 3D metrology has been stressed by the 2007 edition of ITRS. A good example of 3D metrology is characterization of strained channel transistor recess. Strained channel transistors have been introduced as device speed improvement measure. Fig. 12 (a) illustrates concept of strained channel transistor [9]. An epitaxial SiGe is embedded into source/drain recess regions to induce compressive stress on channel region. Proximity of SiGe to the channel and, therefore, the recess undercut define the channel stress which directly impacts transistor performance. Both CDSEM and OCD are not sensitive enough to characterize the undercut profile. 3D-AFM is considered as promising and accurate metrology for measuring the undercut profile.

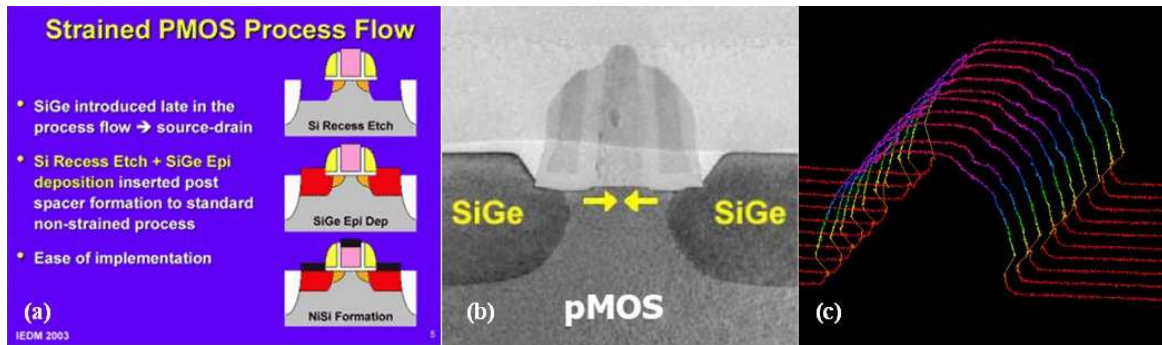


Fig. 12. (a) Schematic diagram of strained transistor process [9]. (b) TEM image of strained pMOS transistor and (c) 3D-AFM image of isolated transistor with recessed drain and source regions.

4.2 Sidewall Spacer Geometry

As shown by Fig. 13 (a), sidewall spacers are crucial for proper control of lateral position and overlap of sequential doping implants (shallow S/D extension, halo and deep S/D) with respect to the edge of the transistor gate. The spacers determine the channel length, junction geometry and abruptness. Therefore, spacer dimensions are directly related to the final transistor electrical performance. A variety of spacer structures can be used to tailor the S/D junction and to maximize drive current while maintaining low parasitic capacitance of the transistor [2]. By tuning deposited film thicknesses (CD), anisotropic reactive ion etch processing (CD and profile), and optimizing implant dose/energy, one can achieve desired S/D extension, buffer and S/D design. Therefore, sidewall spacer CD and profile control is crucial for transistor performance control. However, spacer thickness and profile measurements are extremely challenging and continue to be problematic for most available thin film and CD metrologies including x-ray, optics, acoustic and e-probe based techniques.

During final pre-silicide spacer etching, poly silicon on the sidewall of the gate can get exposed. When spacer pull-down from top of gate becomes too large in Fig. 13 (b), there is a chance of device shortage (bridges can form between gate and source/drain). Spacer engineering requires 3D characterization of sidewall thickness, profile, and spacer pull-down value through sequential steps of the gate processing. To get such information, one would need to measure exactly the same gate several times through the processing to evaluate the effects of etch and cleaning processes on the gate profiles. It is difficult to control the pull-down since CDSEM and OCD are not sensitive to subtle variation in gate stack profile. A direct measurement of the pull-down by 3D-AFM is possible. Such measurement does not require simulations (cf. OCD) or scrapping of wafers (cf. X-SEM or TEM).

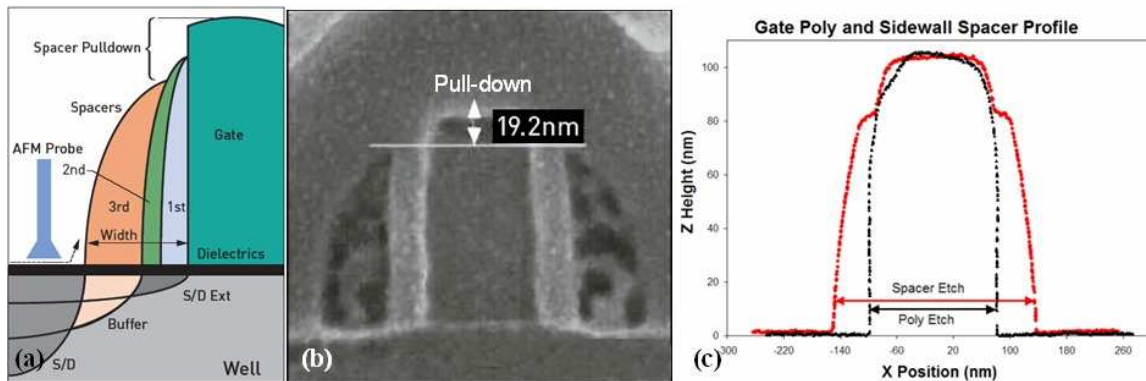


Fig. 13. (a) Schematics of multiple sidewall spacers and S/D junctions (showing one gate side only), (b) TEM image of gate with multiple spacers and (c) sequential AFM images of the same gate through spacer processing [2].

4.3 Dual Stress Liner (DSL)

In the end of 2004, AMD and IBM announced another technological breakthrough in sub-45nm node transistor performance [10]. The new strained silicon process called “dual stress liner” simultaneously enhances performance of both types of semiconductor transistors (n-channel and p-channel) by stretching silicon in one transistor and compressing it in the other using conventional thin film materials. DSL has been used to further enhance device speed. It is critical to

characterize three dimensional profile of nitride liner as the shape difference before tensile material deposition and after its removal indicates how much tensile material has been left behind. The stack is too complex for OCD. X-SEM and TEM cannot access the same site before and after processing. CDSEM is not sensitive to profile and shape. 3D-AFM can be used to estimate the remaining tensile material directly by scanning on the same site (Fig. 14).

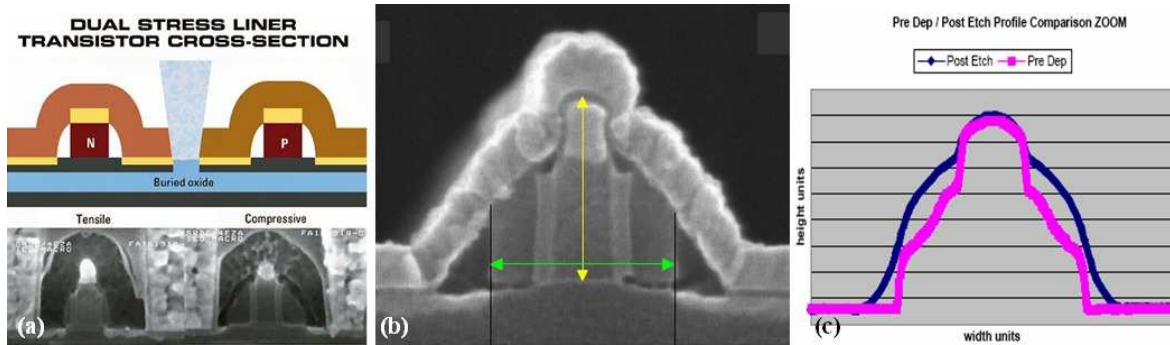


Fig. 14. (a) Schematic diagram of dual stress liner process and corresponding X-SEM images [10], (b) X-SEM image of DSL gate and (c) sequential AFM profiles of gate before and after deposition and etching of nitride spacer.

4.4 Dual Damascene

Cu dual damascene integration is the most advanced interconnect scheme (Fig. 15). Sidewall profile of low-k dielectrics can significantly affect growth of barrier metal and Cu seed layer. There are several reports that low-k dielectrics can be damaged by various processes such as etching, stripping, cleaning, and pore sealing [11]. SEM is not a good solution to characterize low-k material because it is known to cause CD shrinkage of low-k materials. Until now dual-beam and TEM metrologies are commonly used for characterization of structures and defects in low-k interconnect. These techniques are destructive and difficult to use for in-line process monitoring. AFM is accurate, non-destructive 3D metrology fully capable of characterizing low-k dual damascene structures (Fig. 15).

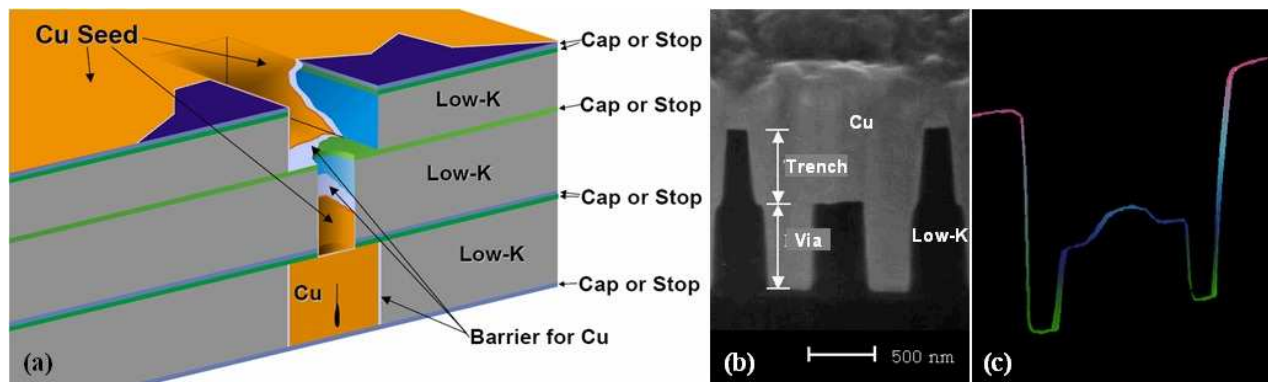


Fig. 15. (a) Schematic diagram of dual damascene structure [12], (b) X-SEM image of Cu-deposited dual damascene trench and via structure and (c) AFM profile of dual damascene structure.

5. PHOTOMASK APPLICATIONS

5.1 Defect Review

Defect control specifications of photomask products are tighter than that of final wafer products. Any imperfection of photomask will be transferred to sample pattern resulting in yield and productivity drop. Defect review is a critical procedure in mask production since photomask can be potentially repaired. Once defect is found 3D characterization of the defect is needed to decide on feasibility of its repair. CDSEM is the most widely used metrology for defect review. However, CDSEM can not provide topography of defect. 3D-AFM can characterize any defect in detail in full 3D. Photomask repair equipment is using AFM already to estimate initial defect volume and control progress of repairing.

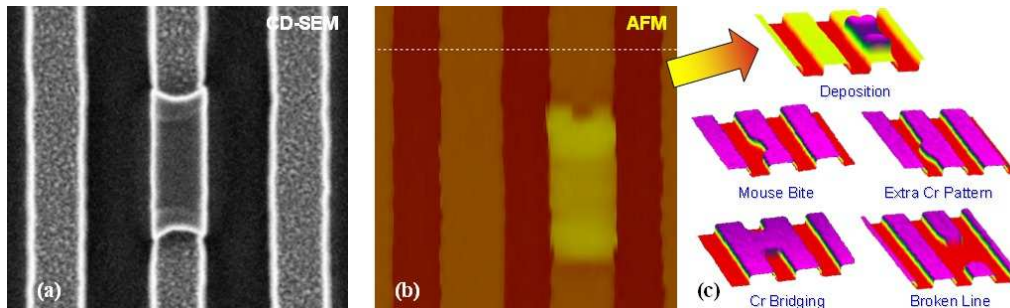


Fig. 16. (a) CDSEM and corresponding (b) 3D-AFM images of deposition-type photomask defect. (c) Various types of photomask defects.

5.2 Optical Proximity Correction (OPC)

Diffraction effects become more significant at 45 nm node and beyond. Biases between dense and isolated lines as well as foreshortening of line ends and corner rounding are commonly observed problems. Optical proximity correction adjusts mask design to compensate for these imaging deficiencies. In practice, OPC is often used to correct for biases arising from etch processes and even to implement small changes to the design to enhance the process latitude of marginal features [13]. As follows from Fig. 17 (c), CDSEM bias varies significantly with material, feature density and type of pattern. CDSEM is failing to provide accurate feedback for OPC. AFM probe-sample interaction is extremely localized and free from any proximity effects. Therefore, AFM is the most accurate tool for OPC feedback without bias variation related to feature shape, density and type.

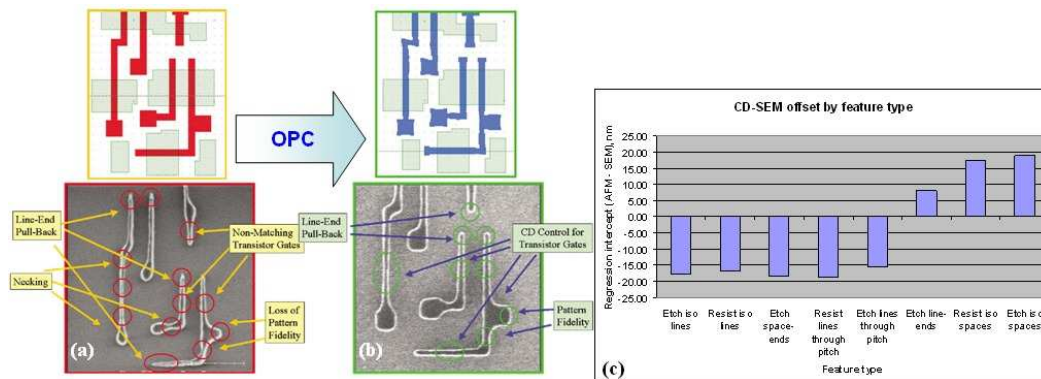


Fig. 17. (a) Original design with no OPC and the corresponding wafer print, (b) OPC-ed design and the corresponding wafer print [13]. (c) CDSEM offset by feature type showing that CDSEM bias is feature dependent.

5.3 Phase Shift Photomask

Phase shift photomask is a critical resolution enhancement tool used at 45 nm node to get better image resolution by utilizing destructive interference to prohibit exposure in areas where resist exposure is not desired. Attenuated phase shift masks (AttPSM) form their patterns through adjacent areas of quartz and, for example, molybdenum silicide (MoSi). Unlike chrome, MoSi allows a small percentage of the light to pass through (typically 6% or 18%). However, thickness of MoSi is chosen so that light that passes through is 180° out of phase with the light that passes through the neighboring clear quartz areas. The light that passes through the MoSi areas is too weak to expose the resist, however the phase delta serves to "push" the intensity down to be "darker" than similar features in conventional chrome mask. The result is a sharper intensity profile which allows smaller features to be printed on the wafer [14]. Thickness of MoSi layer should be tightly controlled for 180° phase shift. OCD can not be a solution for in-line MoSi process monitoring due to model limitations. Stylus-type profiler could be used but it has poor sensitivity and repeatability to measure the critical depth. TEM and X-SEM are expensive, slow and destructive. Therefore, AFM is a unique metrology providing quick, accurate, material independent data on MoSi thickness and overall photomask topography.

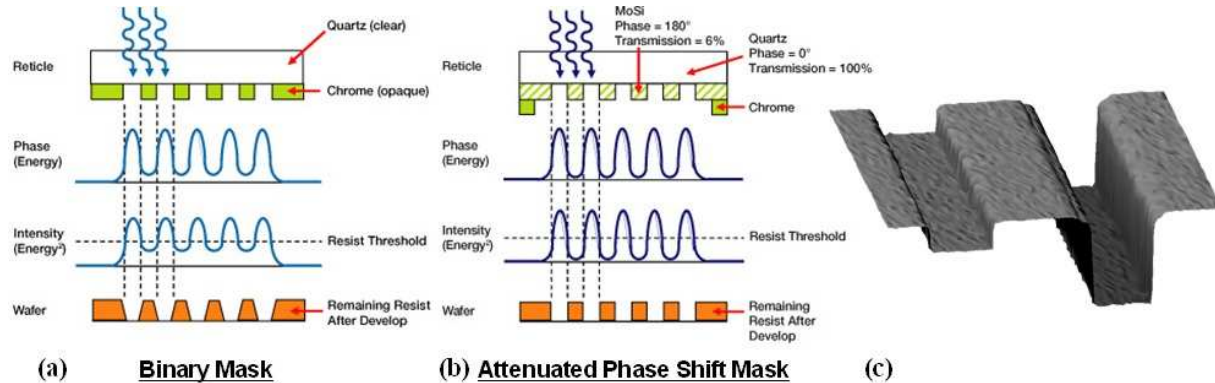


Fig. 18. Schematic diagram explaining the principle of (a) conventional binary mask and (b) phase shift mask [14]. (c) AFM image of MoSi layer of phase shift mask.

6. CIS APPLICATIONS

6.1 Microlens

The digital camera has become a ubiquitous part of modern personal electronic devices. The key light gathering devices of these cameras is the microlens that focuses light through a color filter and onto a photodiode. To improve image resolution and to fit into smaller and smaller end user device form factors, manufacturers have had to invent new and unique methods of packing large numbers of microlenses into smaller and smaller foot prints without compromising light gathering efficiency. As the shape of the microlens determines how well the lens is able to focus the light onto the photodiode, controlling microlens shape is critical for improving device quality and yield. In today's most cutting edge imaging devices, the lens shape varies across the microlens array. The AFM is able to perform precise topographical measurements over multiple microlenses in a single image. Each individual microlens is then measured for lateral dimensions as well as height, and sidewall angles. Lastly, an RMS error to a fit of either a sphere or an ellipse provides an overall metric to the shape of each microlens.

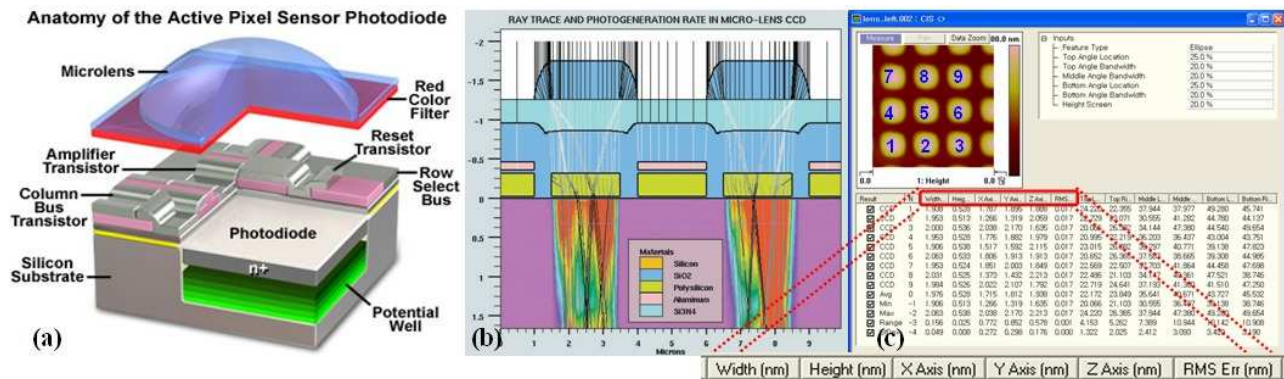


Fig. 19. (a) Schematic diagram of CIS device [15], (b) data of photo generation rate affected by microlens shape [16] and (c) dimensions of microlens measured by AFM.

6.2 Color Filter

In the imaging sensor device, crosstalk between pixels causes degradation of spatial resolution, color mixing and leads to image noise when the device makes an integrated image by collection of light information. Characteristics of crosstalk and photo-sensitivity show contrary trend to one another as a function of color filter thickness. However, color filter layer has an extremely rough surface to measure the height of it. OCD can not show the reliable thickness for such rough features. AFM is the easiest way to monitor the color filter thickness using robust statistical analysis.

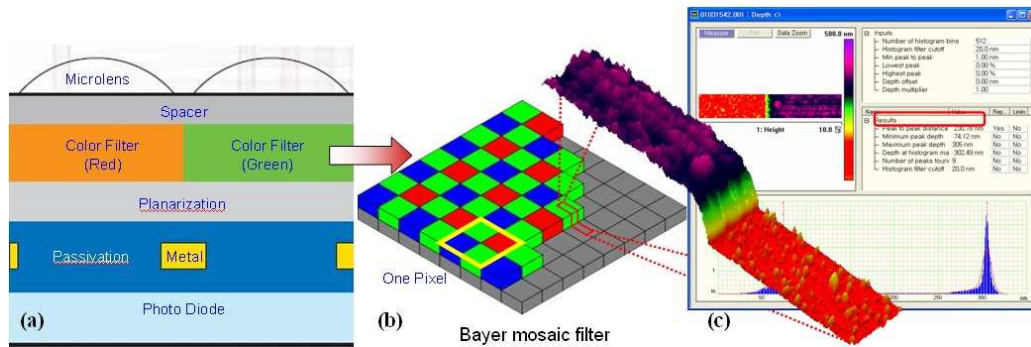


Fig. 20. (a) Vertical schematic diagram of CIS device [17], (b) Bayer mosaic filter configuration for color filter [18] and (c) the color filter height data by AFM.

7. CONCLUSION

Shrinking device dimensions and tight process windows demand sub-nanometer accuracy of metrology for CD control. X-SEM and TEM are commonly used today for cross-sectional characterization and accurate CD metrology of modern devices. Things are changing. 3D-AFM replaces the off-line destructive techniques with the most accurate, statistically prudent and quick in-line metrology. The 2007 edition of ITRS is calling for a new comprehensive metric for metrology - uncertainty. It may take some time for the industry to adopt the new metric. As of today AFM is the most promising technique capable of 3D CD metrology with sub-nanometer uncertainty. To gain industry's full recognition, robustness and ease-of-use of AFM should be further improved to meet demanding requirements of semiconductor manufacturing. This is the challenge we are facing.

REFERENCES

- [1] Metrology, International Technology Roadmap for Semiconductors, 2007 Edition.
- [2] T. Bao, et al., "Control Sidewall Spacer Geometry with Next-Generation", Veeco Instruments Inc. Application Note #115, (2008).
- [3] J. Foucher et al., "Impact of Acid Diffusion Length on Resist LER and LWR measured by CD-AFM and CD SEM" Proc. SPIE Vol. 6518 (2007).
- [4] J. Foucher et al., "Sidewall Roughness Analysis with a 3D CD-AFM", Veeco Technical Seminar, July (2005).
- [5] Semiconductor Microelectronics and Nanoelectronics Programs, NIST (2007).
- [6] Freescale website, <http://www.freescale.com/webapp/sps/site/overview.jsp?nodeId=0ST287482180CAE>.
- [7] Semiconductor International China website, <http://article.sichinamag.com/2006-07/200678042739.htm>.
- [8] Wikipedia website, http://en.wikipedia.org/wiki/NAND_flash.
- [9] T. Ghani et al., "A 90nm high-volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors." IEDM Technical Digest, pp. 978-980 (2003).
- [10] H.S. Yang et al., "Dual Stress Liner for High Performance sub-45nm Gate Length SO1 CMOS Manufacturing", IEDM Technical Digest, pp. 1075-1077 (2004).
- [11] E. T. Ogawa et al., "Electromigration Reliability Issues in Dual-Damascene Cu Interconnections", IEEE Transactions on Reliability, VOL. 51, NO. 4, pp. 403-419, Dec. (2002).
- [12] P. Josh Wolf, "Overview of Dual Damascene Cu/Low-k Interconnect", Presentation at NSF Science and Technology Center, August, (2003).
- [13] C. Spence, "Mask Data Preparation Issues for the 90 nm Node: OPC Becomes a Critical Manufacturing Technology", Future Fab Intl. Issue 16 (2004).
- [14] ASML website, <http://www.asml.com/asml/show.do?ctx=10448&rid=6851>.
- [15] Olympus website, <http://www.olympusmicro.com>.
- [16] Silvaco "Luminous" brochure, http://www.silvaco.fr/products/vwf/atlas/luminous/luminous_04.pdf, (2008).
- [17] TSMC brochure, "TSMC CMOS Image Sensor Technology", (2006).
- [18] Wikipedia website, http://en.wikipedia.org/wiki/Bayer_filter.