

A HIGH SPEED LOW POWER NEGATIVE SENSING ARCHITECTURE FOR 3D NAND FLASH MEMORY

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ABSTRACT

A new sensing architecture aiming at negative threshold voltage detection for 3D NAND Flash memory cells is proposed. This sensing architecture does not need triple well devices and negative voltage supplies. In this architecture, we apply 2 V to source line (SL) rather than 0V which is always used in conventional method. We prove that this architecture is feasible by Technology Computer Aided Design (TCAD) simulation. We have also designed a sense amplifier (SA) to support the proposed sensing architecture. This SA has advantages including lower noise, 9.4% faster read speed, and 51.6% lower power consumption compared to the conventional counterpart.

INTRODUCTION

Nowadays, 3D NAND Flash has attracted great attentions due to its superiority in high storage density [1-3]. However, there is a wide negative threshold voltage distribution in 3D NAND Flash memory due to charge trap mechanism [4]. In conventional negative sensing architecture, negative pump and triple well devices are needed to sense memory cells which have negative threshold voltage. But negative pump increases the design complexity of the peripheral circuit, and triple well devices increase the difficulty and cost of the fabrication process. D'alessandro, et al. proposed a method to sense threshold voltage of -2 V without triple well devices and negative pump [5]. But the SA they proposed has disadvantages such as slow read speed, large power consumption and noise.

In this paper, a novel negative sensing architecture (NSA) is proposed which is suitable for 3D NAND Flash memory based on TCAD simulation. And our proposed SA shows better performance on read noise, read speed, and power consumption.

EXPERIMENT

The Realization of NSA

We propose a negative sensing architecture for a cell string of the Terabit Cell Array Transistor (TCAT) structure, as shown in Figure 1. Our device model is a 6-layers TCAT structure. And it contains 2 layers of select gates (GSL and SSL) and 4 layers of memory device (CG0 to CG3). Electrical properties of CG1 were studied

through TCAD simulation, and the threshold voltage distribution of CG1 after programming operation is -2 V to 3 V. Thus, the CG1 needs to be applied -2 V to 3 V in conventional sensing architecture. In the proposed NSA, the gate voltage range of CG1 is 0 V to 5 V, and no negative voltage is needed. Therefore, it does not need triple well devices and negative voltages. We applied 2 V to the Source Line, and 2.45 V to the bit line (BL). The poly-Si channel can be boosted to 2 V. The V_{gs} is from -2 V to 3 V when CG1 increases from 0 V to 5 V. And there is no body effect in 3D NAND Flash memory. Thus, it can accurately sense cell's threshold voltage of -2 V to 3 V.

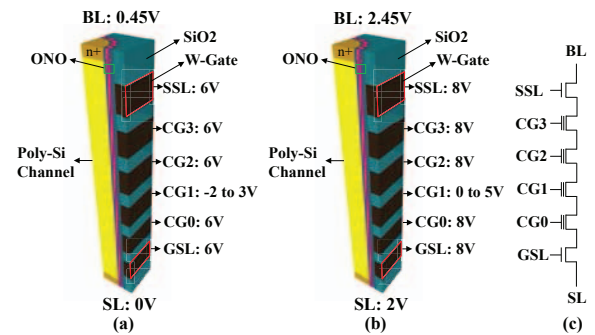


Figure 1: (a) The conventional NSA for a cell string of TCAT. (b) The proposed NSA and its bias condition. (c) The schematic of the string.

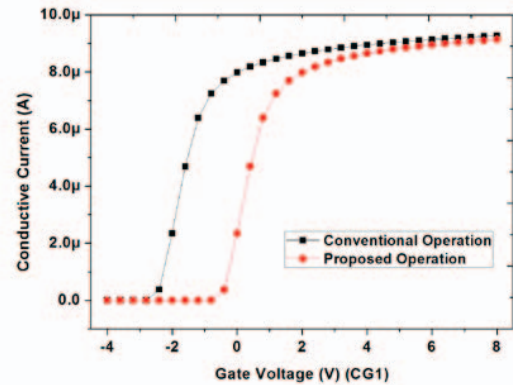


Figure 2: The I-V curve of the string. The threshold voltage of CG1 cell is -2 V. In the conventional operation, the turn-on voltage of CG1 is -2 V. While in the proposed one, it is 0 V.

In our method, all the bias voltages are 2V higher than those in conventional ones. Suppose the threshold voltage

of CG1 cell is -2 V. CG1 needs to be applied -2 V to sense the cell in conventional architecture, but it only needs 0 V in the proposed NSA (Figure 2).

High Speed Low Power SA

The proposed SA and its timing are shown in Figure 3 and Figure 4 respectively. The SA includes pre-charge circuit, structure I, structure II and sensing circuit. And the VDD is 2.5 V. The pre-charge circuit consists of transistor T3. Since T3 is a NMOS transistor, it can be shut off when node SEN is 3.3 V. Structure I is made up of NMOS T4 and diode-connected NMOS T5. T4 makes the BL charged faster. T5 can prevent the current flowing from BL to node SEN during sensing period. T5 has low barrier, and is easy to be integrated in the array of SA. Structure II is a transfer gate, and its enable signal is the data stored in the latch. The sensing circuit is composed of transistor T0, T1, T2 and a latch. T1 will be turned on when the voltage of node SEN is lower than 1.7 V. There is a capacitance C_c which is 20fF, connected to node SEN. The voltage of node SEN will be controlled by BOOST_SEN through capacitive coupling.

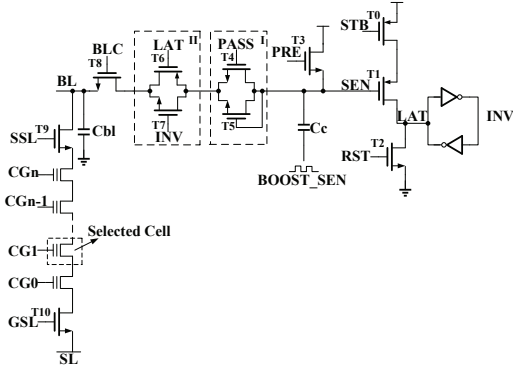


Figure 3: The proposed SA and a connected string.

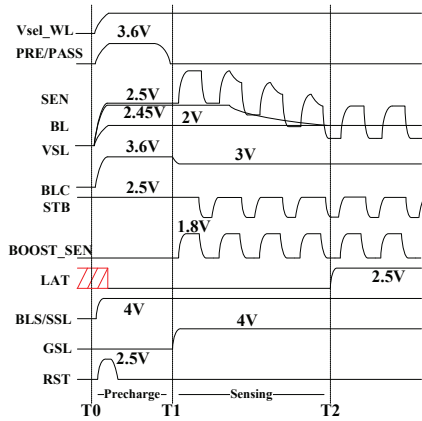


Figure 4: The single read operation of the SA. It includes the pre-charge period and the sensing period.

There are two periods in a single read operation (SRO). In the pre-charge period, the node SEN is pre-charged to VDD, and the BL is clamped at 2.45 V by

transistor T8. At the same time, the latch is reset to '0', SL is set to 2 V and BLC arises to 3.6 V. Due to body effect of transistor T8, BLC needs 3.6 V to clamp BL at 2.45 V. During sensing period, transistor T4 is off and node SEN is boosted to high level when BOOST_SEN rises. Simultaneously, the voltage of BLC will be reduced to 3 V. The voltage of node SEN drops when the string is conductive and BOOST_SEN is high. After several clocks, the voltage of node SEN becomes lower than that of BL when BOOST_SEN falls if the string is conductive. It is because the diode-connected NMOS can prevent the current flowing from BL to node SEN. The latch will flip to "1" when the voltage of node SEN is lower than 1.7 V. When the latch is "1", the transfer gate will cut off the node SEN and BL. Our proposed structure is suitable for multi-bit storage technology, but in our simulation, we just show two read operations for adjacent states, when we read high threshold voltage cells (HTVC), the low threshold voltage cells (LTVC) do not have current. Thus, the power consumption will be reduced.

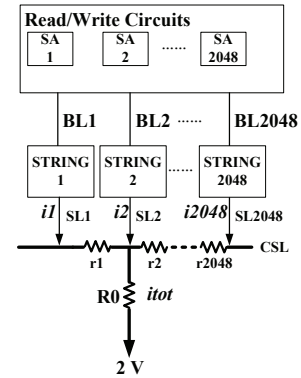


Figure 5: The parasitic resistance model of Common Source Line (CSL) and wire.

We simulate a model of 2048 strings and SAs as shown in Figure 5. All the SLs of the string are connected to the CSL. The CSL and the wire to pump which generates 2 V have parasitic resistance. The parasitic resistance becomes larger with the page increasing. In our simulation, we assume the total parasitic resistance is 38.6 Ω , 1024 of our string models have low threshold voltage cells, and other 1024 string models have high threshold voltage cells.

Figure 6 shows the timing of two read operations for the 2048-string-SA model. The voltage of selected WL is 3 V and 3.25 V for LTVC and HTVC respectively. LTVC and HTVC are in two adjacent states. The high voltage of BOOST_SEN is 1.8 V. From the timing of node SEN (green curve), it shows that the voltage of node SEN will drop lower than 1.7 V when we read the LTVC, but it will not drop down to 1.7 V again when we read the HTVC. Along with the data read out from LTVC being stored in the latch, the transfer gate shuts off the path from node SEN to BL. If there is no transfer gate in SA, for SAs

connected to LTVC, the voltage of node SEN will drop down to 1.7 V again while reading the HTVC. And the current of LTVC will bounce the CSL higher when we read HTVC. Thus, noise will be generated in CSL. The voltage elevation on CSL will make the current of the string smaller, and the read speed of HTCV will become slow.

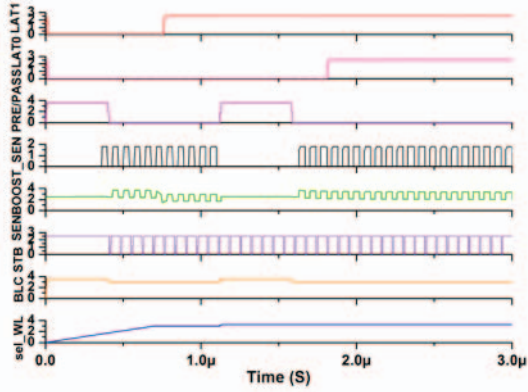


Figure 6: The timing of two read operations for adjacent states. There are 2048 strings and SAs in the model.

RESULTS AND DISCUSSIONS

We show two read operation results of LTVC and HTVC in Figure 7. The proposed SA is 80 ns and 160 ns faster than the conventional one for LTVC and HTVC respectively. The read time of LTVC and HTVC is 0.85 μ s and 1.98 μ s for conventional SA, and 0.77 μ s and 1.82 μ s for proposed one. Therefore, the proposed SA is 9.4% faster than the conventional one referred in [5].

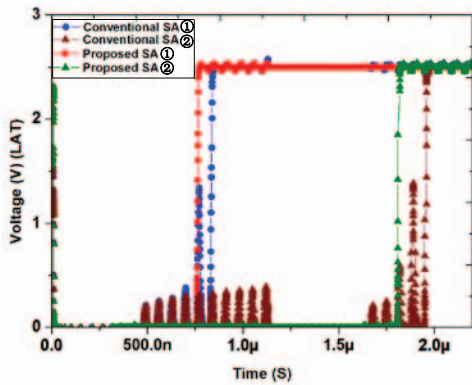


Figure 7: Two read results of latches. ①refer to LTVC, ② refer to HTVC and conventional SA referred in [5].

The difference between LTVC and HTVC is because the current of LTVC bounces the CSL. Figure 8 shows the CSL bouncing phenomenon. When reading the HTVC, the proposed SA reduces the voltage of CSL which influences the read speed. From the result, we can get that it reduces about 0.1 V. The power consumption of conventional SA referred in [5] is 2.473 mW, and that of proposed SA is

1.196 mW, reducing power consumption by 51.6%. This is because there is no current in LTVC for the proposed SA when we have a read operation for the HTVC.

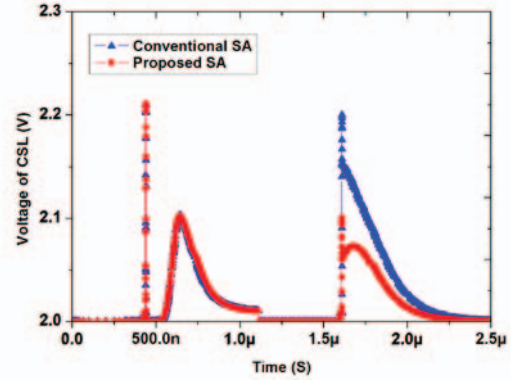


Figure 8: The CSL bouncing phenomenon. The blue curve means the voltage of CSL for conventional SA, the red one is the voltage of CSL for the proposed SA.

CONCLUSIONS

In this paper, we have proposed a new NSA for negative threshold voltage sensing in 3D NAND Flash memory. And we have also designed a SA to support the sensing method. In this NSA, we do not need triple well devices and negative voltage supplies. And the TCAD simulation result proves that the new NSA is suitable for 3D NAND Flash memory. The SA we designed has advantages including lower noise, 9.4% faster read speed, and 51.6% lower power consumption compared to the conventional counterpart referred in [5].

ACKNOWLEDGEMENTS

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