

Reset Current Scaling in Phase-Change Memory Cells: Modeling and Experiments

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Abstract—The operation of a phase-change memory cell is studied, with special regard to programming performance, by means of analytical and TCAD numerical modeling and experimental characterization. Dependence of the reset current on geometrical properties of the heater element is analyzed through the study of heat flux from the heater element to the phase-change material. A simple electrothermal analytical model is implemented, which allows the prediction of the cell reset current value as a function of heater geometrical parameters. Analytical predictions are compared with good agreement to extensive experimental measurements. The effects of power dissipation are studied, showing that cell power efficiency strongly depends on its geometrical properties.

Index Terms—Device scaling, modeling, nonvolatile memory devices, phase-change memory (PCM).

I. INTRODUCTION

DURING recent years, phase-change memory (PCM) has emerged as a suitable and promising technology, candidate for future developments in the nonvolatile memory field, due to its characteristics of fast speed, scalability, manufacturability, reliability, and power consumption [1], [2].

In PCM, data storage is accomplished by means of the (reversible) process of phase change of a chalcogenide material between amorphous and crystalline states, which is triggered by material heating and cooling (i.e., melting and quenching), where the amorphous or crystalline outcome of the process depends substantially on the chosen cooling procedure [3], [4].

Depending on device architecture, heat transmission from a heater element to the chalcogenide material can be a key issue to determine programming operation efficiency; in order to optimize cell performance, besides physical materials properties, device geometry plays a critical role, the extensive analysis of which is the aim of this work.

Significantly high current levels are required in order to perform the reset operation, where the chalcogenide material phase is converted from the crystalline (low resistance) to the amorphous state (high resistance). High current levels may represent a constraint for the architecture definition, since they can limit the scaling down of selection transistor dimensions and the capability of programming several cells in parallel. In addition, overall power consumption and device reliability may

be affected by high current intensities. The constant scaling down—toward next technology generations—of device dimensions, operating voltages, and power consumption requires consistent scaling down of operating current levels. Device design strategies dedicated to current control and reduction are therefore of critical importance. To this purpose, solutions were proposed that involve material engineering (in terms of heater electrical resistivity and chalcogenide melting temperature) and geometry engineering [6]–[18]. In this paper, we analyze the latter approach by studying the effects of geometry engineering on a specific PCM cell architecture (“wall” [5], [25]), where heat is generated by Joule effect inside a heater element and transmitted to the phase-change material through their contact interface.

In this paper, 3-D TCAD electrothermal simulation results are presented, showing that, in the analyzed “wall” architecture, heat is generated inside the heater element and flows out toward the surrounding heat sinks, including the chalcogenide storage element.

We then introduce an analytical electrothermal model, where heat transmission is studied in terms of heat fluxes through the heater element’s surfaces. The model allows the prediction of memory cell reset current as a function of the heater’s geometrical parameters, as well as the analysis of device thermal efficiency. Current density inside the heater element, which can be a critical reliability issue, is also calculated.

Analytical and numerical results are then compared with experimental measurements, performed on devices manufactured with different heater geometries, showing very good agreement between theory and experiments. The proposed methodology is therefore capable of addressing geometry and power scaling issues with consistent and reliable prediction capacity.

II. DEVICE ARCHITECTURE

We have studied a specific PCM cell architecture (“wall” [5], [25]), where a chalcogenide material strip lays on top of a thin heater element. The contact area between the heater and the phase-change material covers the whole width of the chalcogenide strip [see Fig. 1(a)].

Within this architecture, as it will be shown in the following section on TCAD modeling, heat is generated by Joule effect inside the heater element and then transmitted to the chalcogenide through the contact area interface [Fig. 1(b) shows the temperature distribution in the device, as calculated with 3-D TCAD simulation, during reset operation]. Maximum device temperature is therefore achieved inside the heater, and in order to melt the chalcogenide, temperatures higher than 900 K have

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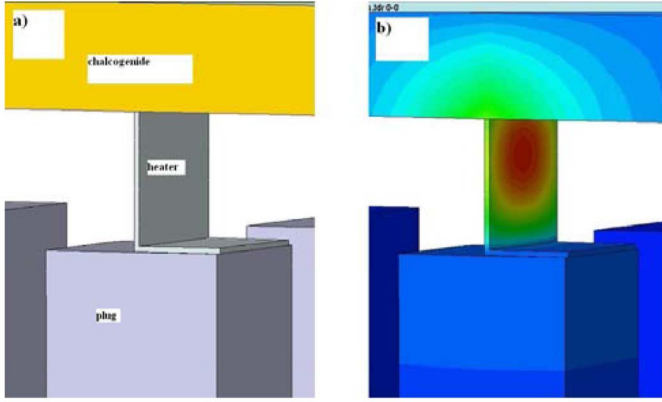


Fig. 1. (a) PCM “wall” memory cell architecture. (b) Temperature distribution during reset operation. Insulating materials are set transparent.

to be reached into the phase-change material strip. To this purpose, current flows into the heater/chalcogenide series. The individual memory cell is selected by means of a selection transistor (MOSFET or bipolar junction transistor, depending on the technology architecture), which constitutes the third element of the whole electrical series.

The heater element is therefore surrounded, all around its lateral surfaces, by insulating materials and electrically connected, from above, to the chalcogenide strip and, from below, to a contact plug leading to the selection transistor.

We define as “reset current” (I_{reset}) the minimum current value required to cause, after a programming cycle, the proper phase change from crystalline to amorphous in a given volume of the chalcogenide material. With such architecture, it is important, when studying the system behavior, to evaluate both electrical current flow through the heater/chalcogenide series and heat fluxes through all of the involved interfaces.

III. TCAD MODELING

TCAD modeling tools [19] were used to simulate the electrothermal behavior of the device during reset operation. A 3-D model of the device, including a MOSFET selection device and the first metallization level, was implemented, where physical properties of materials were derived from published results ([20]–[22] and references therein) or direct measurements. The electrical resistivity temperature dependence of the doped TiN alloy used for the heater element and of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ used for storage are taken account of by means of simple linear models with negative temperature coefficient that allow fair reproduction of experimental measurements in the studied temperature range.

Simulations were carried on by solving the semiconductor equations with the standard drift and diffusion methodology and the heat diffusion equation. The adopted simulation tools allow the study of both temperature distributions and heat fluxes. It is therefore possible to analyze both qualitatively and quantitatively the impact of geometry scaling on the internal thermal state and dynamics.

The 3-D model used for these electrothermal simulations was tested versus available experimental data under several oper-

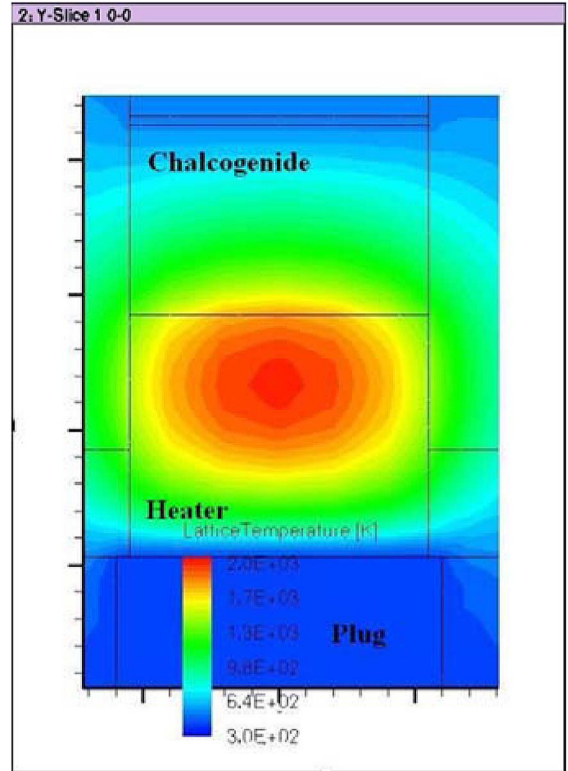


Fig. 2. Simulated internal temperature distribution for $I = I_{\text{reset}}$. Two-dimensional section orthogonal to the chalcogenide strip. The maximum temperature peak lies inside the heater element.

ating bias conditions (i.e., reading and programming, both set and reset operation, and stationary and transient). It has proven to be capable of reproducing and predicting operating regimes with good agreement to experiments, in terms of measured reading and programming currents as functions of the applied bias voltages, and of reset current scaling with heater geometry [26]. We therefore consider this numerical approach a reliable tool to provide qualitative and quantitative physical insight into cell operation mechanisms.

Fig. 2 shows the simulated internal temperature distribution on a 2-D section of the device, orthogonal to the chalcogenide strip shown in Fig. 1. The snapshot was taken for $I = I_{\text{reset}}$, where I_{reset} was experimentally measured on a structure with the same geometry. It is clearly seen that the maximum temperature peak lies inside the heater element. This localization is a direct consequence of heat flowing through all of the heater interfaces with surrounding materials, which determines the stationary temperature profile; more specifically, the distance between the heater/chalcogenide interface and the maximum temperature peak is caused by efficient heat transfer toward the chalcogenide itself. Fig. 3 shows the simulated heat flux intensity and vectors on the same 2-D section. Maximum flux intensity is observed close to the interface between the heater and the contact plug, due to the very high thermal conductivity of the metal plug. Vectors in Fig. 3 show that heat flows from inside the heater toward the external heat sinks. This should be considered a distinctive feature of this specific architecture, related to the implementation of very thin heater elements, manufactured with high electrical resistivity materials, which

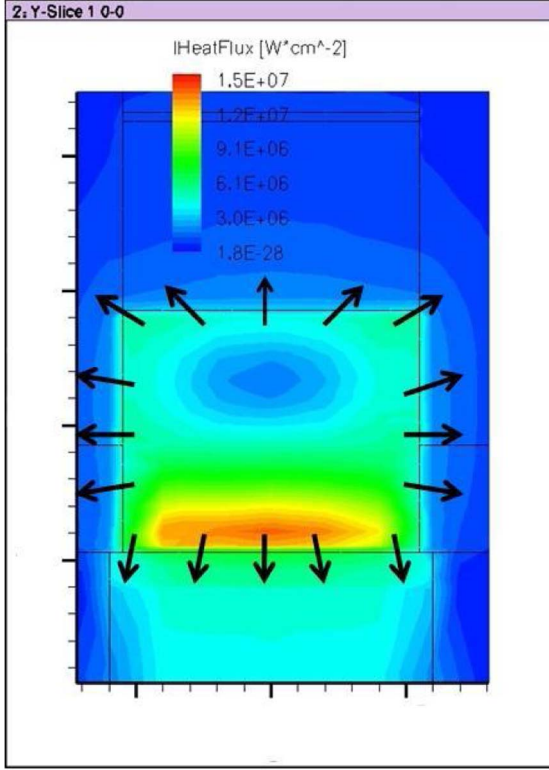


Fig. 3. Simulated heat flux distribution for $I = I_{\text{reset}}$. Two-dimensional section orthogonal to the chalcogenide strip. Maximum flux intensity is observed at the heater/contact plug interface. Heat flows from inside the heater toward the external heat sinks.

cause the largest part of Joule heating to take place inside the heater itself. It is expected that, due to the contact plug draining such high heat flux intensity, only a small part of generated Joule heat will contribute to chalcogenide melting.

As suggested by temperature distribution in Fig. 1(b), the chalcogenide volume to be heated above 900 K can be approximated by a cylindroid, whose base is described in Fig. 4 and whose height coincides with heater element width w . Within this approximation, the chalcogenide volume to be heated is

$$V = wr \left(\frac{\pi}{2} r + t \right). \quad (1)$$

By comparing experiments and TCAD simulations, for several heater geometries, it is found that, when $I = I_{\text{reset}}$, the value of r , which is the vertical extension of the region where $T > 900$ K, is about 40.0 nm, not dependent on heater geometry. This value will be used in the following to determine the power per unit volume required in order to achieve the reset state.

IV. ANALYTICAL MODELING

Numerical and analytical modeling of PCM cells operation has been the subject of several research works (see, e.g., [6], [21], [29]–[32], and references therein). Both approaches provide useful insight into device physics and operation. In the cell architecture design process, analytical modeling of cell programming operation can be of utmost importance since it requires less computing time and power with respect to the

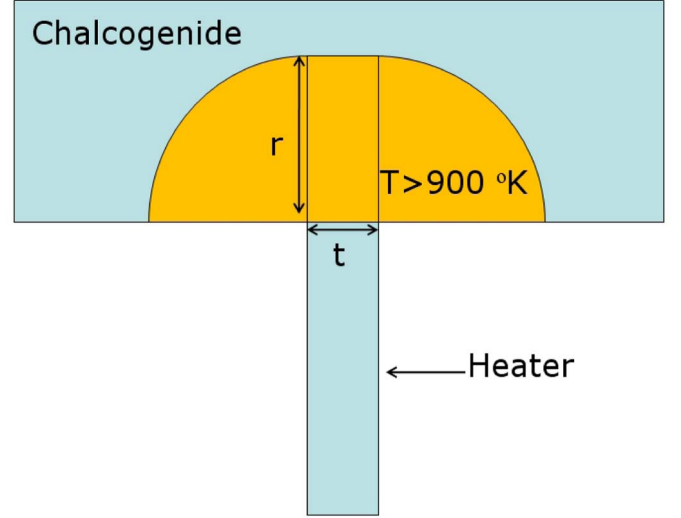


Fig. 4. Two-dimensional cross section of the heated chalcogenide volume. t is the heater element thickness, and r is the vertical extension of the heated region.

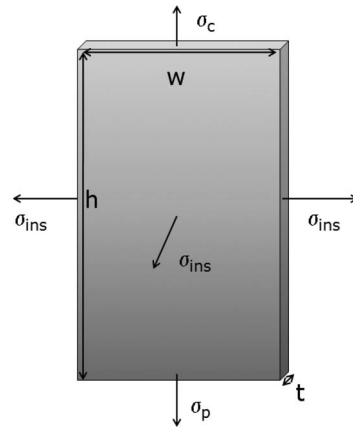


Fig. 5. Solid model of the heater element. Arrows represent heat fluxes through the parallelepiped faces. σ_x represents the thermal conductivity of element x . Thickness t is typically orders of magnitude smaller than w and h .

numerical approach and can provide deeper understanding of the involved physical processes. To this purpose, we introduce here a compact analytical electrothermal model, with the aim of predicting the scaling of cell reset current as a function of cell geometry.

In this model, the heater element is described by a parallelepiped (see Fig. 5): its upper face represents the heater/chalcogenide interface, the lower face represents the heater/plug interface, and lateral faces represent the heater/insulator interfaces. We then attribute to all of the parallelepiped faces the thermal properties (i.e., thermal conductivity values) of the materials whose interface they represent and study heat flux from within the heater to the external environment by means of a network of thermal conductance values in parallel with each other. We hypothesize that only heat flowing through the upper heater surface contributes to chalcogenide melting, whereas the contributions coming from all of the other surfaces are dissipated in the heat sink.

Such approach involves a number of approximations, whose legitimacy will be verified by comparison of model results to experimental measurements.

- All generated power flows out of the heater element. This is a consequence of studying a stationary network, whereas in real operation, an electrical and thermal transient is involved, and a fraction of generated power is required to heat the heater element itself.
- Heat flux is uniform all over the parallelepiped faces and proportional to adjacent materials thermal conductivity values. (In general, heat flux uniformity might be false.)
- Possible contributions of heat flowing out from lateral surfaces of the heater, close to the heater/chalcogenide interface, are neglected.
- Heater resistivity is supposed to be constant with respect to temperature.
- Thermal boundary resistances (TBRs) of the interfaces between the heater and surrounding heat sinks have the same relative impact on all of the bulk thermal conductivity values in series with the interfaces.

By assuming direct proportionality between heat fluxes and thermal conductivity values of heat-receiving materials, we are imposing equal temperature gradients in the Fourier law of heat conduction across all interfaces. According to numerical simulations, this may lead to a slight error in the evaluation of heat flux toward the bottom plug. This error should, however, affect an interface area, which, in this architecture, is orders of magnitude smaller than heater/insulator lateral interfaces and therefore provides a minor contribution to the overall heat flux.

The impact of TBRs on cell operation has been studied in recent years: it is known [27], [28], [33] that this effect can play an important role in cell architectures, where heat is generated inside the chalcogenide layer, since TBRs contribute to confine generated heat, therefore improving programming efficiency. Measurements of the TBR at the interfaces between chalcogenide and surrounding materials have been performed [27]. To the best of our knowledge, however, analogous measurements are not available for materials used in heater manufacturing, hence, as a first approximation, the above proposed assumption on the uniform relative impact of TBRs. In the following model equations, this assumption means that the σ_x bulk conductivity values are all renormalized by the same factor in order to include the contribution of TBRs.

In order to study Joule power production in the heater, we also need to know the electrical properties (electrical resistivity: ρ) of the heater material.

The whole system is therefore defined by three geometrical parameters (height: h , width: w , and thickness: t); three thermal parameters (chalcogenide, insulator, and plug thermal conductivity values: σ_c , σ_{ins} , and σ_p); and one electrical parameter (heater electrical resistivity: ρ).

Within this frame, by calculating the network of parallel conductance values, we may evaluate the amount of power that flows through the upper heater surface, which is the amount of power that will usefully contribute to chalcogenide melting

(effective power: P_{eff}). Thus

$$P_{eff} = \frac{\sigma_c w t}{(\sigma_c w t + 2\sigma_{ins} h(w + t) + \sigma_p w t)} R I^2 \quad (2)$$

or

$$P_{eff} = \frac{\sigma_c h}{(\sigma_c w t + 2\sigma_{ins} h(w + t) + \sigma_p w t)} \rho I^2. \quad (3)$$

Equations (2) and (3) take into account the ratio between the upper surface area and the whole parallelepiped area, as well as differently weighted contributions, due to different values of thermal conductivity of the materials adjacent to the heater.

It is also useful to define a quantity that we will call “thermal efficiency” (η). Thus

$$\eta = \frac{P_{eff}}{P_{tot}} = \frac{\sigma_c w t}{(\sigma_c w t + 2\sigma_{ins} h(w + t) + \sigma_p w t)}. \quad (4)$$

Equation (4) represents the fraction of the overall generated Joule power that is actually transferred to the chalcogenide, thus providing an estimation of the thermal efficiency of the system. We also define a quantity p (effective power per unit volume), which will be useful when dealing with the study of the scaling of electrical and thermal properties with w , h , and t (width, height, and thickness of the heater element). Thus

$$p = \frac{P_{eff}}{V}. \quad (5)$$

We can now experimentally determine a quantity p_0 , which is the *average reset effective power per unit volume to be melted*, by actually measuring I_{reset} on one or more given cells and substituting in (2) and (5). p_0 is the average power per unit volume [where V is given by (1)] that we have to transmit to the chalcogenide layer in order to achieve the phase transition that characterizes cell reset operation. When p_0 is known, we can express I_{reset} for a generic cell, whose h , w , t , ρ , and σ_x parameters are known, as follows:

$$I_{reset} = \sqrt{\frac{p_0 w^2 r t (\frac{\pi}{2} r + t)}{\eta \rho h}}. \quad (6)$$

Equation (6) states that I_{reset} is the current value required, on a generic cell, to transfer an effective power per unit volume p_0 to the chalcogenide material, so that the same thermal conditions that took place during the experimental determination of p_0 are reproduced and the phase transition can take place.

Capability of predicting the reset current intensity as a function of geometrical parameters is of primary importance when dealing with the definition of memory cell architecture: I_{reset} affects power consumption and reliability and may be limited by current driving capability of the selection transistors; one of the possible strategies adopted to scale down reset current consists in increasing the heater element resistance, so that higher Joule heat is generated. We will show in the following that, according to our model, the geometry scaling strategy adopted in order to increase heater resistance affects both thermal efficiency and reliability issues.

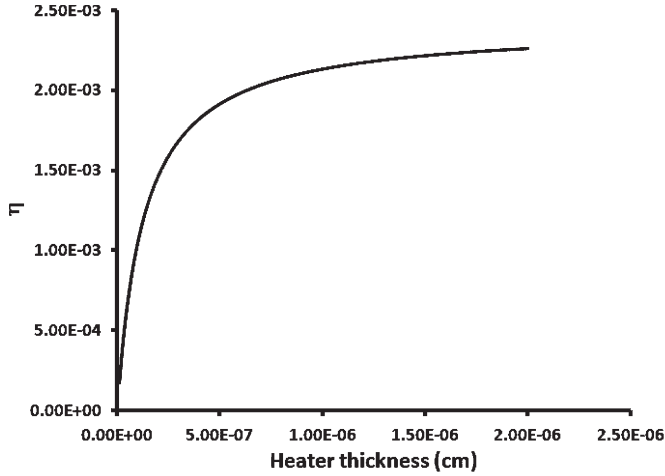


Fig. 6. Thermal efficiency η [see (3)] versus heater thickness t . Heater height and width are kept constant.

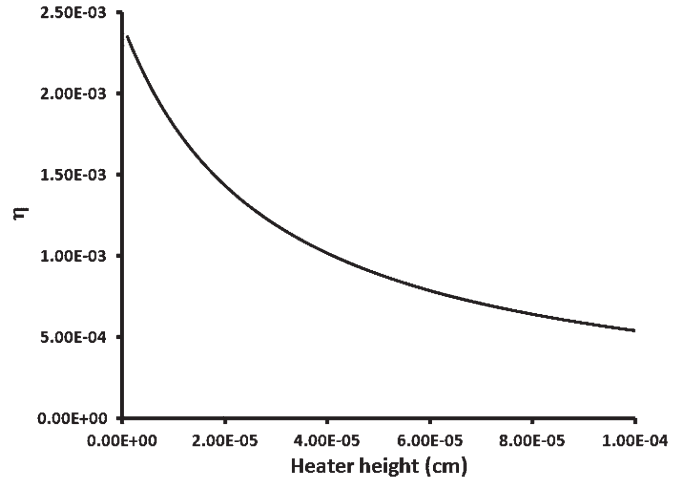


Fig. 7. Thermal efficiency η [see (3)] versus heater height h . Heater thickness and width are kept constant.

V. MODEL RESULTS

Equations (2)–(6) can be analyzed in order to study how geometry scaling affects cell reset performance. In this section, we will define an arbitrary (but realistic, in terms of the ratios among thermal conductivity values of different materials) set of physical parameters (σ_x and ρ) and study the dependence of I_{reset} on the geometrical parameters, by letting them independently change.

Analysis of thermal efficiency η [see (4)] shows that different behaviors are expected when different geometric parameters are scaled.

- By using the heater's thickness as the scaling parameter, we observe (see Fig. 6) that the fraction of the total generated power that is transferred to the chalcogenide decreases with decreasing thickness. This effect is due to the reduction in the contact interface area between the heater and the chalcogenide: heat flux toward the chalcogenide is hindered by contact area reduction.
- When the heater's height is used as the scaling parameter, the thermal efficiency trend is opposite (see Fig. 7): η decreases with increasing height. In this case—with constant heater/chalcogenide contact area—thermal efficiency is affected by power dissipation through the heater's lateral surfaces, whose area increases with increasing h .
- When we let the heater's width change at constant t and h (see Fig. 8), η stays almost constant for high w values. This happens because, by changing the heater's width, we change the heater/chalcogenide contact area, but we also proportionally change the chalcogenide volume to be melted; hence, power required to achieve the phase transition is constant. The observed reduction in η at low w is due to power dissipation through the heater's thin edges, which do not scale down.

It is worth noting that, with this cell architecture, in all of the examined geometry scaling schemes, thermal efficiency is determined by geometric (w , h , t , and interface areas ratios) and physical (σ_x) parameters. A significant part of the overall generated power is dissipated with no impact on cell

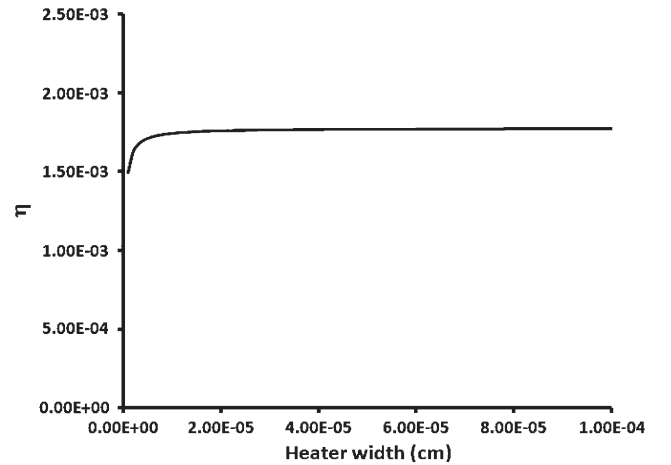


Fig. 8. Thermal efficiency η [see (3)] versus heater width w . Heater thickness and height are kept constant.

programming operation. This effect is due to power generation inside the heater, to the small contact area between the heater and the chalcogenide, and to the high thermal conductivity of the contact plug below the heater itself, which drains a large amount of generated Joule heat.

We also observe that, while thermal efficiency shows similar behaviors, with respect to heater resistance, when t and h are scaled (efficiency decreases with increasing heater resistance), the trend is different when w is scaled, where η stays almost constant as a function of R . This makes us expect that different I_{reset} dependency values on different geometric variables should also be observed.

A. Reset Current

From (6), we can study the dependence of I_{reset} on the heater geometrical variables t , h , and w . To compare the different scaling regimes, we will plot I_{reset} as a function of heater resistance, choosing the scales that will allow the simplest functional representations.

- Fig. 9 shows the dependence of I_{reset} on $\sqrt{1/R}$ when heater thickness is the independent variable. It is clear

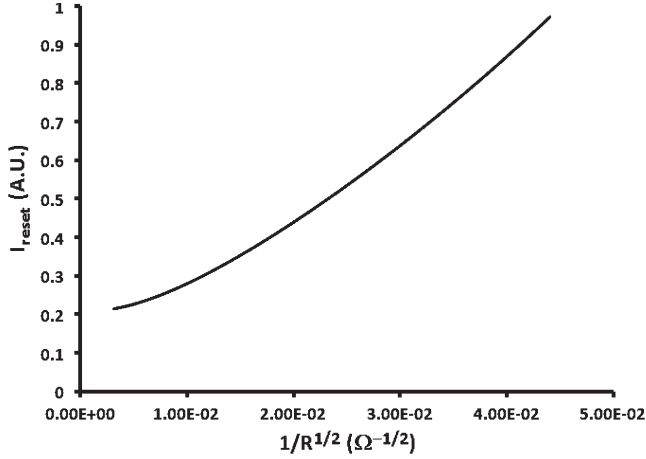


Fig. 9. Reset current [see (6)] versus $1/R^{1/2}$ when scaling heater thickness t . Heater height and width are kept constant.

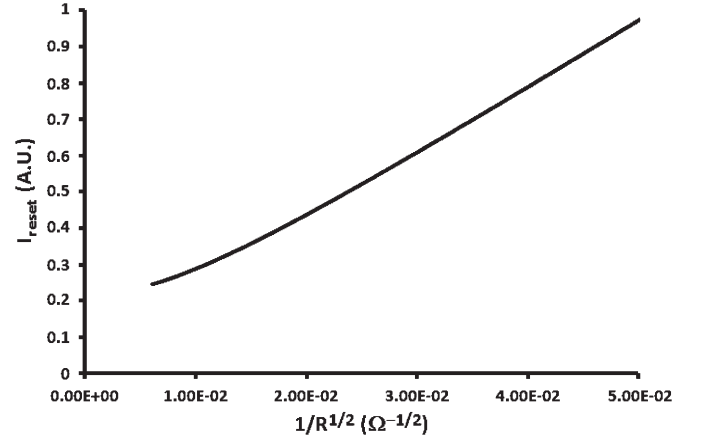


Fig. 10. Reset current [see (6)] versus $1/R^{1/2}$ when scaling heater height h . Heater thickness and width are kept constant.

that a simpler law such as $I_{\text{reset}} \propto \sqrt{1/R}$ does not hold here, where a significant deviation from linearity is observed for high heater resistance values. Our model clarifies that the nonlinearity of the I_{reset} curve is due to the above observed behavior of thermal efficiency (see Fig. 6): when, at high R , efficiency decreases, additional current is required in order to compensate for power dissipation. As a result, when $1/R \rightarrow 0$, I_{reset} tends to a finite value, different from 0. At low R values (high t), the dependence of I_{reset} on $\sqrt{1/R}$ is superlinear, due to the increasing chalcogenide volume to be heated.

- Fig. 10 shows the dependence of I_{reset} on $\sqrt{1/R}$ when the heater height is the independent variable. When plotted versus $\sqrt{1/R}$, at high R values, the dependence of I_{reset} in the height scaling scheme is very similar to what we have seen when scaling heater thickness. This happens because, in both these scaling schemes, thermal efficiency decreases with increasing heater resistance, and the chalcogenide volume to be melted stays almost constant. With this scaling scheme, at low R (low h), I_{reset} linearly goes with $\sqrt{1/R}$.
- The I_{reset} versus $1/R$ curve achieved when the heater width is the independent variable and t and h are kept constant is shown in Fig. 11. Now, the dependence of I_{reset} is almost linear on $1/R$. Still, a small deviation from linearity is observed for high R values, consistent with the analogous deviation observed in η (see Fig. 7), due to power dissipation through the heater's edges. The reset current scaling regime is clearly different from what is observed when changing t and h ; this happens because by scaling the heater width, we also scale the chalcogenide strip width and volume to be melted, which is not the case when t and h are changed.

We have illustrated in this section how our model explains the dependence of reset current on heater geometrical parameters, by letting them independently change to each other. It is clear, though, that one can modify more than one parameter of the heater element at the same time. In the general case, equation (6) will allow the prediction of the reset current value as a

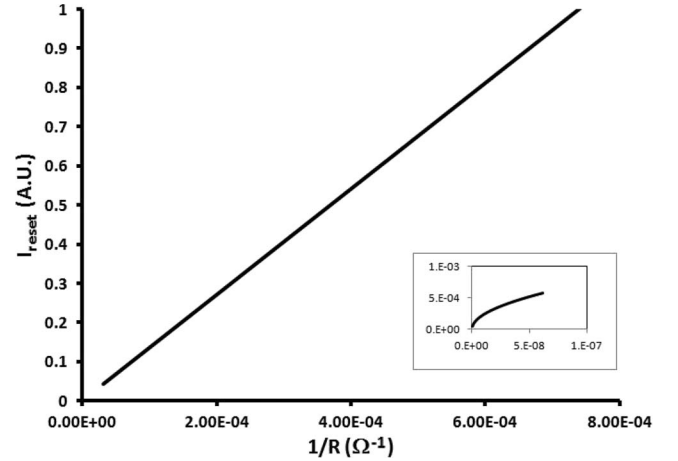


Fig. 11. Reset current [see (6)] versus $1/R$ when scaling heater width w . Heater thickness and height are kept constant. The inset shows that, for high R , I_{reset} tends to 0, deviating from linearity.

function of heater's geometry, whatever be the chosen scaling path.

B. Reset Current Density

The role of current density in the storage element with respect to device reliability and endurance has been discussed. It has been shown [23], [24] that a correlation exists between reset current density and cell endurance, where higher current densities may contribute, directly or indirectly, to cell endurance degradation.

From (6), we can easily calculate the reset current density J_{reset} in the heater element. Thus

$$J_{\text{reset}} = \frac{I_{\text{reset}}}{wt} = \sqrt{\frac{p_0 r \left(\frac{\pi}{2} r + t\right)}{\eta \rho h t}}. \quad (7)$$

Fig. 12 shows J_{reset} as a function of $\sqrt{1/R}$ when heater's resistance is tuned by independently changing t , h , and w .

Three definitely different trends are observed.

- When R is increased by reducing the heater's thickness, reset current density increases, because, although

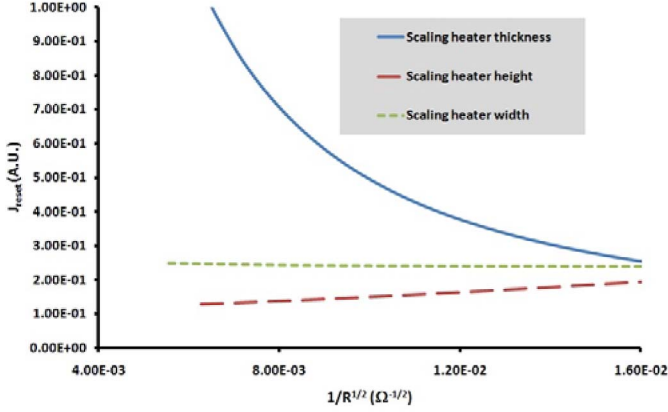


Fig. 12. Reset current density dependence on R [see Eq. (7)], following three different geometry scaling paths.

reset current is reduced, the heater's section and the heater/chalcogenide contact area are reduced as well as thermal efficiency.

- When R is increased by increasing the heater's height, reset current density decreases, as the heater's section is kept constant.
- When R is increased by reducing w , the heater's section decreases proportionally to the chalcogenide material volume to be melted; therefore, reset current density is almost constant as a function of R , with a small deviation at high R .

Deviations from linearity are observed in all of these three curves, once again due to power dissipation at high R values.

We have shown in this section that the herein proposed analytical model allows the evaluation of heater current density as a function of the chosen scaling scheme. These results show that the scaling scheme that is chosen in order to increase the heater element resistance can definitely affect reliability issues, directly or indirectly, in terms of electromigration or high local temperature-related effects. Our model offers a useful prediction tool to minimize reliability issues when defining the memory cell architecture and scaling path. In addition, the impact on current scaling and cell reliability of materials physical parameters, such as heater electrical resistivity ρ , can be studied by means of this analytical methodology.

VI. COMPARISON WITH EXPERIMENTAL RESULTS

In order to validate the proposed analytical model, extensive experimental measurements were carried out to experimentally characterize the dependence of the reset current on device geometry parameters. Memory cells with different heater thickness, height, and width—manufactured with a 90-nm technology node CMOS architecture [26]—were measured on statistically significant samples, and the achieved reset current values were compared with the predictions of our model.

The heater material resistivity value was directly measured with I - V measurements, and the average value of p_0 , to be used in (6), was extracted from I_{reset} measurements on several

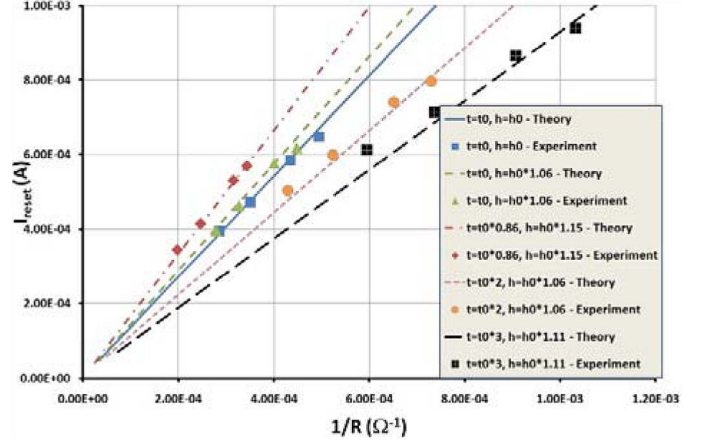


Fig. 13. Comparison of model predictions and experimental data for several values of the heater's geometrical parameters.

device sets, each with its own geometrical parameters. Thus

$$p_0 = \frac{I_{\text{reset}}^2 \eta \rho h}{w^2 r t \left(\frac{\pi}{2} r + t \right)} \quad (8)$$

where all parameters are known, η being a function only of the geometrical parameters and materials thermal properties, r is known by TCAD simulations, and I_{reset} is measured.

Due to the aforementioned assumption on TBRs, we are allowed to use for σ_x (which, according to (4), define η) the actually measured values of materials bulk conductivity, since the model equations that define P_{eff} and η depend only on the ratios among thermal conductivity values, which are clearly unchanged if the relative impact of TBRs on bulk conductivity values is given by a constant multiplicative factor.

These preliminary characterizations gave the following result:

$$p_0 = 4.3 \text{ mW } \mu\text{m}^{-3}$$

which does not depend on heater geometry. Actually, p_0 is a physical property of the chalcogenide material, indicating the average transmitted power per unit volume required to melt the chalcogenide. The experimental values of this parameter, together with the measured heater resistivity ρ , can be substituted in (6), thus allowing the calculation of I_{reset} for any given set of heater geometrical parameters. The results of this procedure are shown in Fig. 13, where experimental measurements are compared with theoretical predictions.

In Fig. 13, several curves are plotted, reporting I_{reset} versus $1/R$, where R was changed by letting heater width w change. Each curve corresponds to different heater height and thickness values.

Excellent agreement is observed between experiments and theory, confirming that (6) is a simple yet powerful compact tool, capable of predicting reset current scaling, once the physical and geometrical parameters of the device are known. Discrepancies between theory and experiment are observed only for the highest heater thickness values, where the constant temperature gradient approximation (see Section IV above)

might be too strong with respect to the increased heater/plug interface area.

It should be highlighted that both experimental and theoretical predictions show that I_{reset} is not determined by the heater resistance value alone, as significantly different reset current values are observed in Fig. 13 for equal resistance values. Our model explains that this effect is due to different thermal efficiencies, determined by the geometrical parameters of the heater itself.

VII. DISCUSSION AND CONCLUSION

Basing on the analysis of 3-D TCAD electrothermal simulation results, which show that, in the examined “wall” memory cell architecture, heat generation takes place inside the heater element, we have developed a simple analytical model, capable of predicting reset current value as a function of device geometric parameters. We have shown that, with this cell architecture, thermal efficiency can be modulated by geometry scaling in different ways, depending on the chosen scaling strategy: in general, efficiency decreases with increasing heater resistance. When resistance is increased by reducing the heater’s width, though, efficiency degradation is negligible on a wide resistance values range, as the melting chalcogenide volume scales down as well. Furthermore, materials physical properties and, definitely, the overall cell architecture may critically impact on thermal efficiency. We need, however, to take into account the tradeoff between the improvement of programming efficiency and a suitably wide reading window.

By substituting, in model equations, a given set of physical parameters, the analysis of reset current scaling was carried on, showing that different scaling strategies correspond to different current scaling modes.

More specifically, when geometric scaling is carried on at a constant chalcogenide volume (acting on the heater height), an almost linear dependence of I_{reset} on $1/R^{1/2}$ is observed, where deviations from linearity occur at high R values. In this scaling scheme, I_{reset} tends to a finite nonzero value when $1/R \rightarrow 0$, which can be easily calculated from model equations. When heater thickness is changed, the chalcogenide volume to be heated is almost constant at small thickness (high R) values; therefore, I_{reset} trend is similar to what we see when scaling h , deviating from linearity at high t values. Different behavior is predicted when the heater’s width is the independent variable: in this case, the chalcogenide volume to be melted linearly scales with w ; as a consequence, we observe almost linear dependence of I_{reset} on $1/R$, and $I_{\text{reset}} \rightarrow 0$ when $1/R \rightarrow 0$, still showing a deviation from linearity at high R values. Nonlinearities of the reset current are explained in terms of thermal efficiency dependence on geometry.

In the frame of the here proposed model, reset current density was also studied, showing that geometry scaling strategies can affect this physical parameter in a critical way: reducing heater’s thickness, although allowing reset current scaling, causes the increase in reset current density in the heater element, with a possible critical impact on device reliability and endurance.

Finally, predictions of the proposed analytical model were compared with experimental measurements, performed on statistically significant samples of PCM cells, manufactured with different heater geometric parameters. After experimental extraction of resistivity and effective power values, comparison of theoretical curves to experimental results showed excellent agreement.

The proposed analytical model can be readily extended to different architectures (e.g., PCM cells with a cylindrical heater), provided that heat generation takes place in the heater element, entirely out of the chalcogenide layer.

The excellent observed agreement between theoretical predictions of the model and experimental measurements confirms the legitimacy of the approximations highlighted in Section IV, which apparently do not affect the generality of model predictions. More specifically, with regard to TBRs, we can infer that, for this architecture, either the impact of TBRs is negligible with respect to bulk materials resistivities or our “constant relative TBR impact” assumption is suitable for modeling purposes, at least until actually measured TBR values for the involved interfaces are available.

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