



Handbook of Thin Film Deposition (Fourth Edition)

2018, Pages 19-41

Chapter 2 - Limits and Hurdles to Continued CMOS Scaling

Krishna Seshan

[Show more](#) ▼

[Outline](#) | [Share](#) [Cite](#)

<https://doi.org/10.1016/B978-0-12-812311-9.00002-5> ↗

[Get rights and content](#) ↗

Abstract

Limits or hurdles to scaling past 10nm are considered. Limits are categorized into different groups: practical and engineering limits such as the cost of fabricators is one; the other is the need for a new lithographic process, such as extreme UV, and perhaps X-Ray or E-beam. These are two practical and basic “limits.”

Scientific limits include various leakage currents in transistors with diminishing dimensions: limits to gate thickness, which are approaching 1 nm; contact pitch, which will challenge lithography.

Device design also limits scaling. The positions of source-gate-drains have recently been changed to provide an advantage in vertical gates, for instance. Doping and electrical parameters such as drive voltage and threshold voltage limit scaling; leakage currents are on the rise and are a cause for concern. Some questions regarding thermodynamic limits, induced instabilities, and noise immunity have been raised. Dopant fluctuations at an atomic scale give rise to V_t variation. These are contributors to difficulties in signal control and stability of the device and memory.

In the interconnect region, limits arise from increasing current density as the cross-section of the current carrying Cu lines decreases and the power and signal density increases. Higher current densities, together with increased metal layers, now exceeding nine layers of metal, give rise to greater heat generation and combine to increase electromigration failures.

As the number of transistors increases, the heat output density from the chip also increases. Greater demands will be placed on device cooling. These various limits are discussed. Ongoing efforts to go beyond these limits are considered.

Access through your organization

Check access to the full text by signing in through your organization.

Access through **your institution**

[Recommended articles](#)

References (0)

Cited by (11)

[A review on the mainstream through-silicon via etching methods](#)

2022, Materials Science in Semiconductor Processing

Citation Excerpt :

...However, it is difficult to improve IC performance by reducing feature size continually as the IC industry meets its turning point now. There will be many problems such as the decrease in thermal dissipation and the increase in leakage current and static power consumption when the size of complementary metal-oxide-semiconductor (CMOS) devices drops below 100 nm [2]. Fortunately, the emergence of three-dimensional integrated circuit (3D IC) solved these problems, which means multiple modules can be integrated into one system, effectively improved system integration level and performance while reducing power consumption, realizing the continuation of Moore's Law [3]...

[Show abstract](#) ✓

[Design of a W-band High-PAE Class A&AB Power Amplifier in 150nm GaAs Technology ↗](#)

2024, Transactions on Electrical and Electronic Materials

[Design of a W-band High-PAE Class A & AB Power Amplifier in 150nm GaAs Technology ↗](#)

2024, SSRN

[Design of a W-band High-PAE Class A&AB Power Amplifier in 150nm GaAs Technology ↗](#)

2024, arXiv

[A Stochastic Computing Scheme of Embedding Random Bit Generation and Processing in Computational Random Access Memory \(SC-CRAM\) ↗](#)

2023, IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

[Benchmarking and optimization of trench-based multi-gate transistors in a 40 nm non-volatile memory technology ↗](#)

2021, Proceedings - 2021 16th International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS 2021



[View all citing articles on Scopus ↗](#)

[View full text](#)

Copyright © 2018 Elsevier Inc. All rights reserved.



All content on this site: Copyright © 2024 Elsevier B.V., its licensors, and contributors. All rights are reserved, including those for text and data mining, AI training, and similar technologies. For all open access content, the Creative Commons licensing terms apply.

