

Novel ESD Protection Transistor Including SiGe Buried Layer to Reduce Local Temperature Overheating

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Abstract—This paper introduces a new NMOS electrostatic discharge (ESD) protection transistor which contains a buried SiGe narrow-bandgap layer between the source and the drain region. The simulations carried out by a two-dimensional simulator show that the ESD induced current flows mainly through the buried layer in the new structure, which strongly suppresses local overheating on the silicon surface. As a result, the peak lattice temperature for the Machine Model with 300 V level is 400°C in the new structure, which is much lower than in the normal structure, 1150°C. In the new structure, the parasitic bipolar turn-on is faster and the bipolar current gain (β) is higher than in the normal structure by as much as 8 ns and 10 times, respectively. The snapback voltage is reduced by 1.5 V in the new structure.

I. INTRODUCTION

WITH the decrease of the feature size and the total area available for VLSI ESD protection circuits, the design for a reliable and robust protection transistor has become a critical issue [1]. The major demands for protection transistors are fast turn-on behavior, effective voltage clamping, and high-current carrying. The NMOS ladder structure, which operates parasitic npn bipolar action to shunt high-level current caused by ESD stress, is commonly used as a protection transistor in CMOS circuits [2], [3]. However, the restricted size of the protection transistor which cannot shunt the ESD induced current sufficiently by its sluggish bipolar behavior, often causes ESD failures. Moreover, the local temperature overheating due to the non-uniform current density on the silicon surface in a protection device can be another reason for serious ESD failures. Therefore, a reliable protection transistor with fast turn-on bipolar action, low snapback voltage [4] and uniform current distribution is indispensable for future technologies.

In this paper, we suggest a new ESD protection transistor by adding a buried SiGe narrow-bandgap layer between the source and the drain region in a NMOS transistor. Until now, the Si/SiGe heterojunction has been extensively accepted due to its high compatibility with conventional silicon process technologies, such as heterojunction bipolar transistor (HBT's) [5], SiGe heterojunction p-channel MOSFET's [6] and SOI's [7]–[9]. Although the bandgap reduction is caused either by

the heavy doping or the germanium content, using germanium is reported to be a more practical method [7].

In this work, we present for the first time the following results: 1) using device simulation, it is shown that the fast turn-on of the parasitic bipolar behavior is achieved in a buried SiGe NMOS transistor during ESD stress due to the valence bandgap reduction in the layer, 2) since the ESD induced current flows mainly through the buried layer, the current localization and extremely high-lattice temperature on silicon surface can be avoided in the SiGe structure, and 3) the snapback voltage which clamps the power consumption on the drain edge during ESD stress is reduced by using the SiGe layer.

Following this introduction, the conventional scheme of ESD protection devices and their failure modes will be introduced. Then a new ESD protection device and its electrothermal simulation results and discussions will be presented compared to a normal Si transistor. Finally, conclusions will be reached.

II. CONVENTIONAL ESD PROTECTION DEVICES AND FAILURES

ESD is a high-current, short-duration event, and its hardness is influenced by both the process and the design of input and output protection circuits [1]. The ESD performance of any protection circuit is measured with either the Human Body Model (HBM) stress test according to MIL-STD or with the Machine Model (MM) stress test [10]. The first is for when a charged object is a person and the second is for when charged object is a machine. The MM provides a short duration, high-voltage pulse as would be likely when the pin of a charged device contacts a ground conductor while the HBM provides a relatively long duration current. Typical design targets for these test models are 300 V and 4000 V, respectively [1].

The typical elements for ESD protection are diodes, NMOS and PMOS transistors, BJT's, and SCR's or thyristors [12].

The required area for the dual-diode protection circuit is about 2000 μm^2 and the ESD level is 2–4 KV. Forward biased diode operates in conductivity modulation for high current resulting in reduction of resistance (R_{ON}) while the reverse biased diode has high R_{ON} . Since there may be damages at the internal chip using this process, it cannot be used in some DRAM's and ASIC libraries.

In the case of the NMOS protection circuit, the required area and ESD level are about 1000–8000 μm^2 and 2–8 KV,

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and its ESD performance can be determined by its area and current uniformity.

In SCR protection circuit, the required area and ESD level are $1500\mu\text{m}^2$ and 2–8 KV, respectively. Although its R_{ON} is small, it has a problem of potential latchup.

The required area and ESD level in the BJT protection circuit are $2500\text{--}7500\mu\text{m}^2$ and 2–8 KV. Although SCR and BJT protection circuits have excellent heat dissipation and higher ESD levels, the weak point is a high trigger voltage than that of NMOS.

The most common ESD protection device in MOS VLSI is a thin-oxide or thick field-oxide NMOS transistor. Excellent ESD protection can be designed by using sufficiently large devices which are called ladder or finger structures. A NMOS transistor is more efficient than a PMOS transistor because of the higher rate of impact ionization of electrons compared to the holes, resulting in easier turn-on under ESD conditions.

A simple schematic of typical NMOS protection transistor is shown in Fig. 1. When positive transient pulses are forced to the drain with the gate and the source connected to ground, the n^+/p diode at the drain is in reverse bias until avalanche breakdown begins [13]. It is reported that as the channel length decreases the NMOS breakdown characteristics exhibit a snapback phenomenon and this negative differential resistance is attributed to the positive feedback caused by bipolar turn-on of the source-substrate junction and initiated by electron-hole pairs generated in the depletion region. As the generated holes move toward the substrate region, the potential of the substrate and source becomes forward biased resulting in electron injection from the source [14]. The positive feedback causes more electron-hole pairs repeatedly, which further raises the substrate potential. As the current increases further, the second breakdown occurs by current localization due to the negative resistance coefficient of the silicon beyond a critical temperature (T_C) at which thermally generated carrier concentration becomes equal to the background doping concentration, which in turn increases T_C . Accordingly, local overheating regions are formed by the second breakdown. Once the temperature increases rapidly toward the melting temperature of silicon ($T_M = 1415^\circ\text{C}$), various ESD failures, such as metal melt filaments and polysilicon melt filaments, occur [1]. The local heat under reverse bias is proportional to the $J \cdot E$ product, where J is the current density and E is the electric field. If the heat is high enough to elevate the contact metallization over the melting point, metal melt filaments are formed, resulting in shorting of the source and the drain. Polysilicon melt filaments can be caused when the thin gate oxide is directly above the isotropic heat source and the heat spreads to the polysilicon gate causing melt filaments between the gate to the source. Gate-oxide breakdown damages in the internal circuit are also reported by the high vertical field ($\geq 10\text{ MV/cm}$) when the protection transistor has poor current driving capability for the ESD stress [15].

One of the main factors of ESD failures in the protection device is non-uniform current distribution during the ESD event. According to the experiment by A. Amerasekera *et al.* [15], the total active width of $4 \times 100\mu\text{m}$ ($W = 400\mu\text{m}$) four-gate multi-finger transistors is only $200\mu\text{m}$, which implies

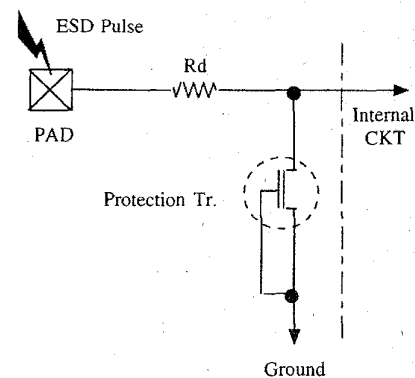


Fig. 1. Circuit schematic of a NMOS ESD protection transistor.

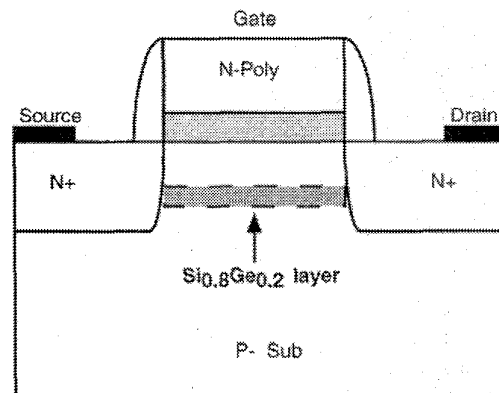


Fig. 2. Cross section of the new ESD protection NMOS transistor including a SiGe buried layer.

only half the number of the fingers are effective during the snapback operation because of the non-uniform current distribution and non-simultaneous triggering of all four gates. The discretization of turn-on thresholds in multi-finger structures is caused by both asymmetries between fingers due to process variations and the substrate resistance, which produces RC delays for triggering the adjacent fingers. The concentration of current density and electric field on the silicon surface can be another reason for ESD failures since it brings about local overheating on the silicon surface due to the large $J \cdot E$ heat source. Besides, inadequate bus connections, such as complex bussing, large bus resistance, inadequate contacts, and vias, are known as the common errors that bring about ESD failures.

Therefore, in order to avoid various ESD failures mentioned above, the protection transistor must be capable of shunting a high-level current during a fast ESD transient, while maintaining a low-voltage and low-power consumption with uniform current distribution.

III. NEW PROTECTION DEVICE

In order to improve the ESD failure thresholds for advanced processes, several schemes are available. One scheme is circuit and layout changes to reduce peak $J \cdot E$ product. The other scheme is to improve device characteristics of protection

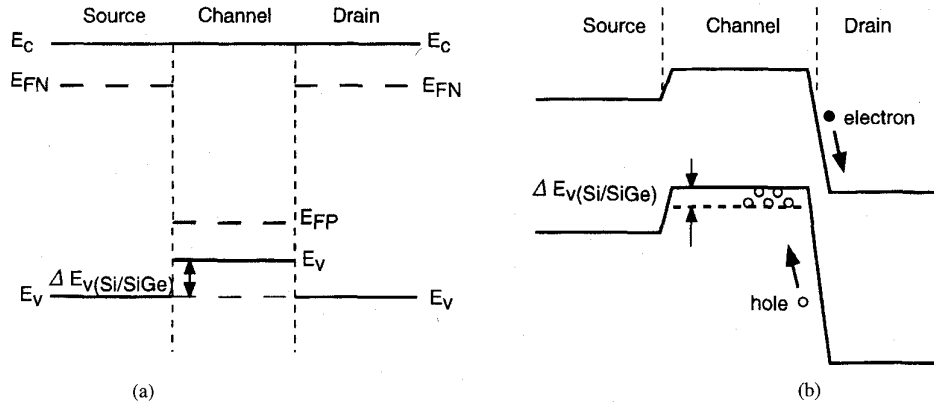


Fig. 3. Energy band diagrams of $n^+/p\text{-SiGe}/n^+$ structure (a) Energy band diagram of $n^+/p\text{-SiGe}/n^+$ structure (b) Hole collection by bandgap reduction.

TABLE I
COMPARISON OF ELECTRICAL CHARACTERISTICS
OF SiGe AND NORMAL TRANSISTORS

	SiGe	Normal
V_{th} (V)	0.40	0.41
I_{dsat} (A/ μm)	2.77×10^{-3}	2.74×10^{-3}
BV (V)	11.7	11.7

transistor by modifying process steps. However, modifying process steps would affect the optimized transistor performance and reliability [16]. For obtaining fast parasitic bipolar behavior without affecting the normal device characteristics, such as the threshold voltage, the breakdown voltage and the leakage current, we propose a new ESD protection device which includes a Si/SiGe buried layer added into a normal NMOS transistor.

Since silicon and germanium are atoms from column IV, the processing of SiGe is potentially compatible with existing silicon technology, and implanted germanium is commonly used to reduce boron diffusion in boron-implanted silicon without side effects. The application of Si/SiGe heterostructures has focused mainly on both bipolar and field-effect transistors. Recently, this has also been applied to SOI devices.

In heterojunction bipolar transistors (HBT's), the germanium exponentially alters the collector current for high-speed digital and microwave applications. A typical HBT's emitter has a bandgap that is wider than the bandgap in the base. The potential barrier formed at the emitter-base junction under such condition reduces the minority carrier injection from the base into the emitter to a significant level. This results in improved emitter efficiency and higher current gain. HBT's have been fabricated by using molecular-beam epitaxy (MBE) and chemical-vapor deposition (CVD), as well as limited-reaction processing (LRP) [5].

In field-effect transistors, lots of interest is given to high-mobility p-channel MOSFET's to overcome the inferior performance of p-channel MOSFET's in CMOS applications

caused by the lower hole mobility, typically two to three times less than the electron mobility [6]. Since the bandgap of the germanium is lower than that of the silicon, a discontinuity in the valence band is created in the Si/SiGe heterostructure, which can be effectively used to confine the mobile holes in the SiGe channel [17]. As a result, the holes in the quantum well can have a higher mobility since the surface scattering effect in conventional MOS transistors has been avoided. It is also applied to SOI devices in order to either improve channel mobility of PMOS [9] or eliminate the parasitic bipolar effect by adding it in the source region [7].

The main idea of the proposed ESD protection in this work is to improve the current gain using the SiGe layer as in the case of HBT's, since protection transistors turn on as bipolar transistors under ESD stress. Furthermore, because the layer is formed far below the silicon surface, the device operates as normal NMOS transistor during normal circuit operation. Therefore, we can use the advantages of both BJT's and MOSFET's by using a SiGe NMOS transistor as an ESD protection device.

The cross section of a new ESD protection transistor is shown in Fig. 2. The current gain of a parasitic bipolar (β) can be expressed as [8], [18], [19]

$$\beta \cong \frac{N_E D_{nB} W_E}{N_B D_{hE} W_B} e^{-\Delta E_g / kT} \quad (1)$$

where ΔE_g is the bandgap reduction between the base (substrate) and the emitter (source), D_{nB} is the electron diffusion constant in the base (substrate) region, and D_{hE} is the hole diffusion concentration in the emitter (source) region. N_E and N_B are the doping concentrations in the emitter and the base regions. W_E and W_B are the emitter length, namely the distance between source-substrate junction and the source contact, and base length, namely the effective channel length L_{eff} , respectively [8]. Fig. 3(a) shows the energy diagram of $n^+/p\text{-SiGe}/n^+$ structure and the conduction bandgap reduction is

$$\Delta E_{C(Si/SiGe)} = \chi_{Si} - \chi_{SiGe} \quad (2)$$

where χ is the electron affinity. For Si/SiGe structure, since $\chi_{Si} \cong \chi_{SiGe}$ and the conduction bandgap reduction at Si/SiGe

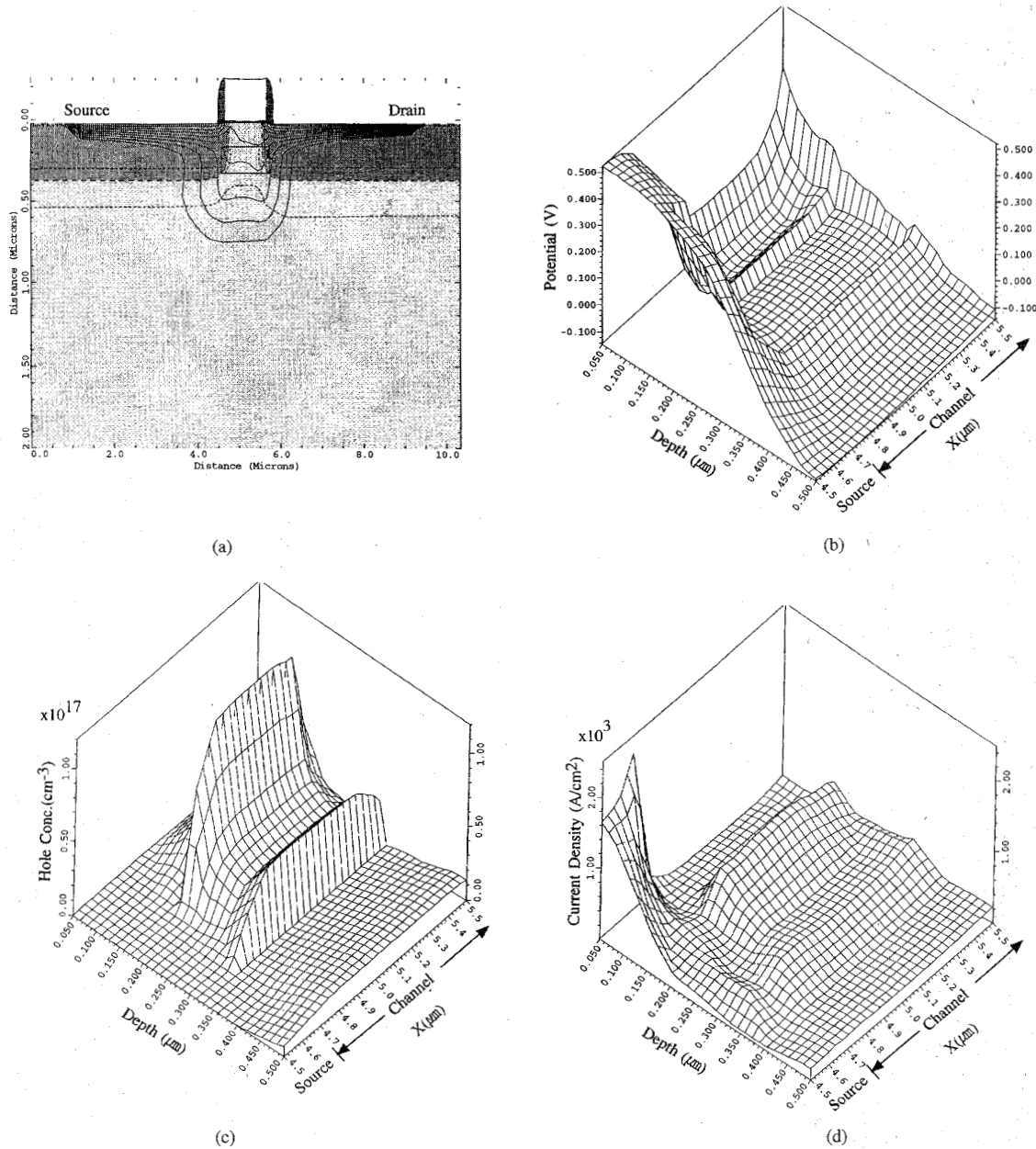


Fig. 4. Internal electrical characteristics of the SiGe transistor at 0.5 ns for Machine Model (MM) 300 V level (a) Current flowline (b) Potential distribution (c) Hole concentration (d) Current density distribution.

is less than 0.02 eV, most of the bandgap reduction occurs at the valence band

$$\begin{aligned} \Delta E_{V(\text{Si/SiGe})} &= \Delta E_C - (\Delta E_{g(\text{Si})} - \Delta E_{g(\text{SiGe})}) \\ &\cong -(\Delta E_{g(\text{Si})} - \Delta E_{g(\text{SiGe})}) \\ &= -\Delta E_{g(\text{Si/SiGe})}. \end{aligned} \quad (3)$$

Thus, the difference in the electron barriers between the base (substrate) and the emitter (source) becomes $-\Delta E_V$ [5], and (1) can be written as

$$\beta \cong \frac{N_E D_n B W_E}{N_B D_h E W_B} e^{\Delta E_V / kT}. \quad (4a)$$

The current gain of the parasitic bipolar transistor in a SiGe NMOS transistor can be improved exponentially as $\exp(\Delta E_V / kT)$. Meanwhile, as shown in Fig. 3(b), since the bandgap of the germanium is lower than that of the silicon, a quantum well can be formed, and the potential of the quantum well connected between the source and the drain region is relatively lower, it can lead to collect impact-ionization holes, which are generated by ESD stress on the high electric field region, the drain depletion region.

To achieve the rapid positive feedback and bipolar turn-on in ESD protection transistors, one of the effective ways is to increase the substrate potential [20]. At the beginning of

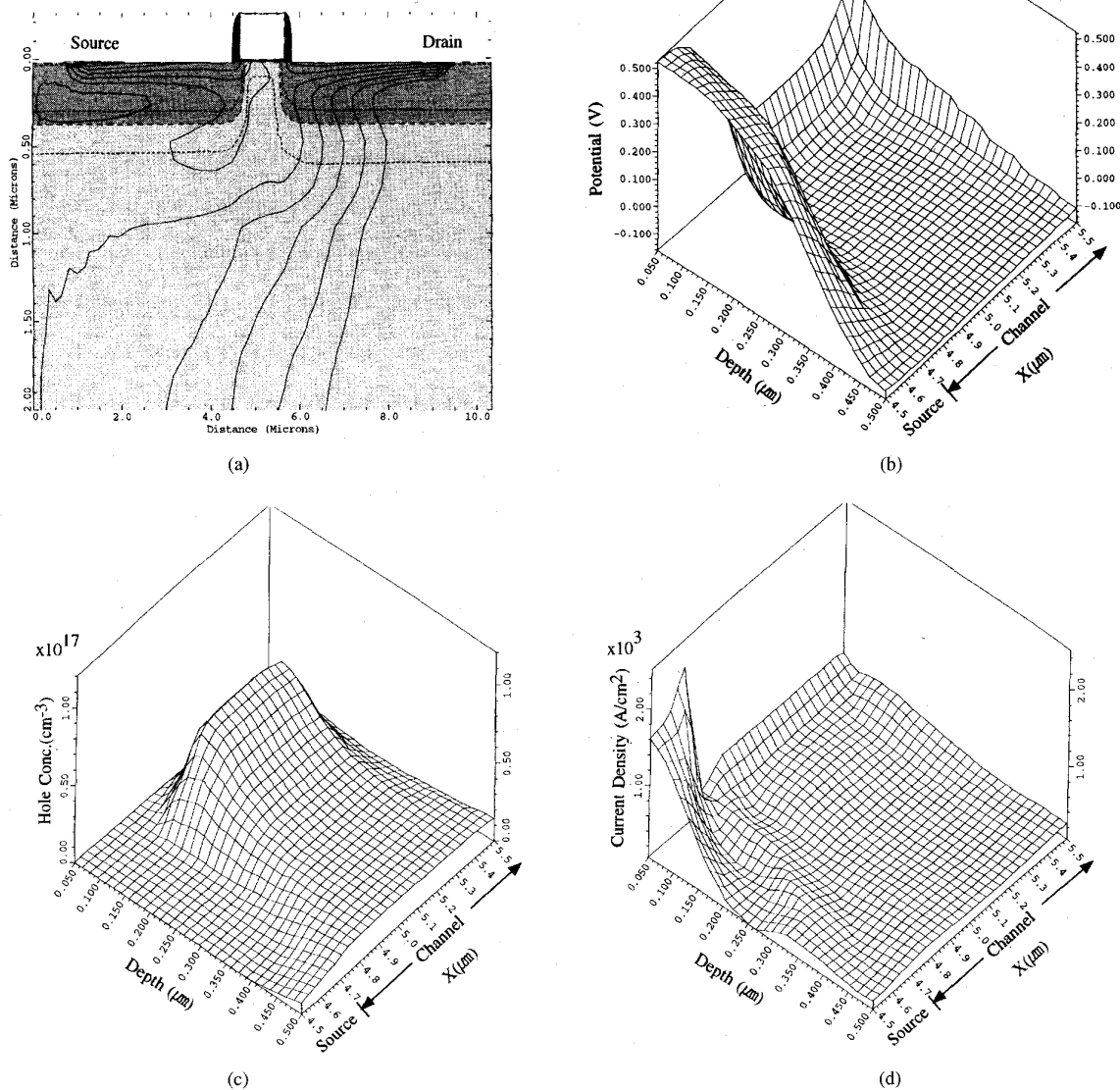


Fig. 5. Internal electrical characteristics of the normal transistor at 0.5 ns for MM 300 V level (a) Current flowline (b) Potential distribution (c) Hole concentration (d) Current density distribution.

ESD stress, since the SiGe layer effectively gathers generated holes, the potential in the layer becomes higher especially on the emitter (source) and base (substrate) junction region. The required time for enough forward bias to turn on the parasitic bipolar behavior is much shorter than that of the normal NMOS transistor. In addition, by using a SiGe protection transistor, it is expected that ESD induced current mainly flows through the buried layer on account of the quantum well, so that current localization and local temperature overheating can be effectively eliminated.

In order to observe the electrical and thermal characteristics of the new ESD protection transistor suggested earlier, a two-dimensional device simulator, TMA-MEDICI [21], was used.

To analyze the electrothermal phenomena for the ESD protection circuit containing the Si/SiGe heterojunction transistor, various analysis modules were included. This tool solves the electron and hole continuity equation, Poisson's equation and heat-flow equation self-consistently with temperature dependent models. In this work, the circuit and device parts are simulated at the same time with the device-circuit mixed module.

The characteristics of SiGe heterojunction are analyzed by the heterojunction analysis module. This module handles the properties of materials that meet at the heterojunction by including the energy bandgap parameters, electron affinity, density of state, various parameters for describing recombination.

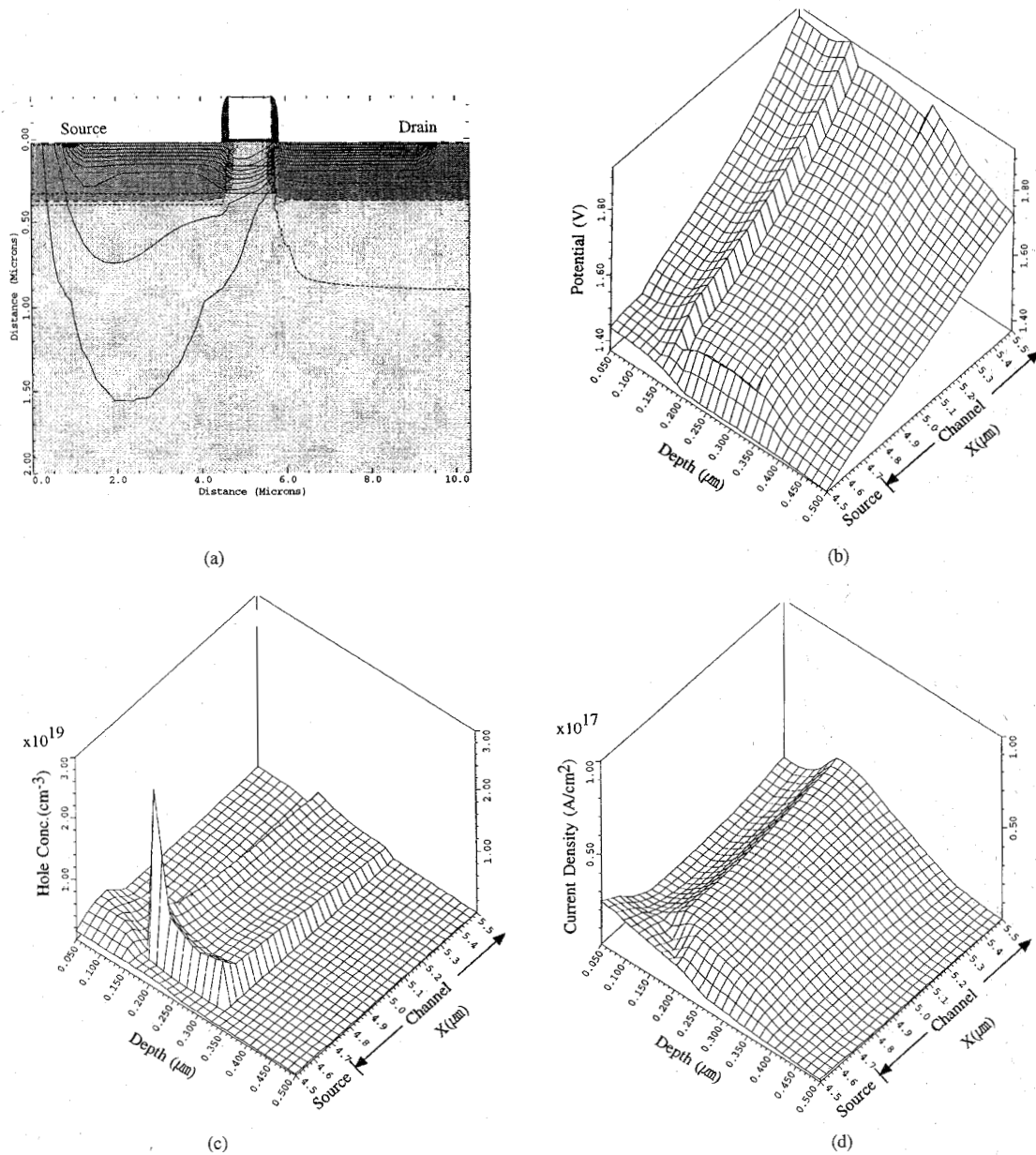


Fig. 6. Internal electrical characteristics of the SiGe transistor at 70 ns for MM 300 V level (a) Current flowline (b) Potential distribution (c) Hole concentration (d) Current density distribution.

nation, and mobility. Since intrinsic Fermi potential is not the general solution to Poisson's equation when solving for structures that contain heterojunction due to the property differences of adjacent materials, Poisson's equation must be written as [21]

$$\nabla^2(\psi - \theta) = \frac{\rho_s}{\epsilon} \quad (4b)$$

where θ is band structure parameter given by

$$\theta = \chi + \frac{E_g}{2q} + \frac{kT}{2q} \ln \frac{N_c}{N_v} \quad (5)$$

where χ is the electron affinity and N_c and N_v are effective density of states in the conduction band and valence band.

IV. SIMULATED DEVICE STRUCTURE

The NMOS transistor which includes a SiGe buried layer for ESD simulation was constructed by using a two-dimensional process simulator, TMA-TSUPREM4 [22]. The transistor is based on n^+ polysilicon technology with gate oxide thickness of 120 Å. The effective channel length and width are 0.7 μm and 135 μm, respectively. The SiGe layer is formed between the source and the drain region with thickness being 0.15 μm, which was assigned by the device simulator. The germanium content in the strained SiGe layer is 20%, and it strongly affects the current enhancement since the bandgap reduction increases as the portion of germanium content increases.

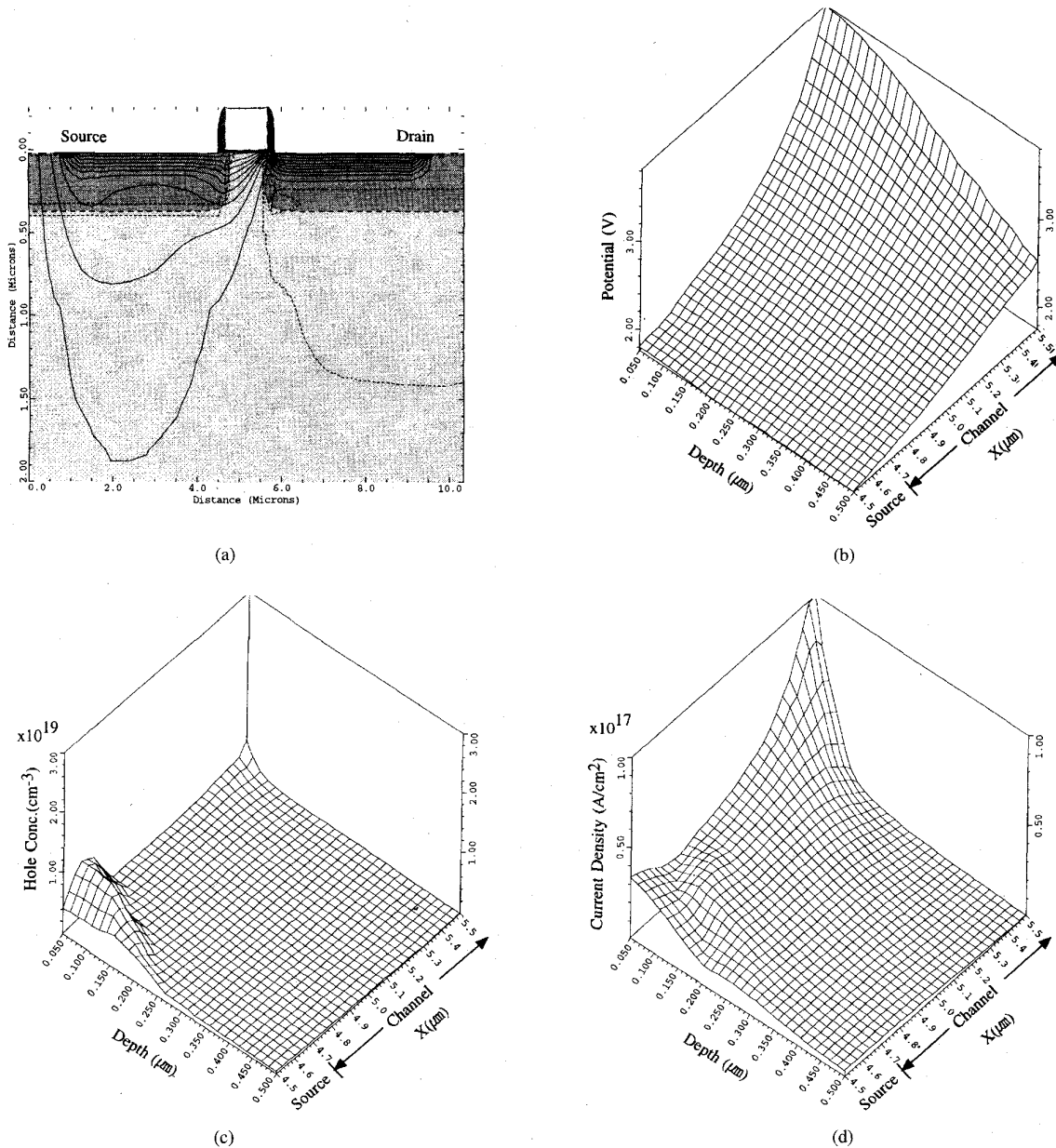


Fig. 7. Internal electrical characteristics of the normal transistor at 70 ns for MM 300 V level (a) Current flowline (b) Potential distribution (c) Hole concentration (d) Current density distribution.

In modern VLSI, it is quite common to introduce additional process steps like mask process or implantations to accommodate ESD effects. The SiGe NMOS transistor can be made by two possible fabrication ways. The first way is growth of a SiGe film. Top silicon is etched down around 2500 Å by RIE (Reactive Ion Etching) and then doped SiGe and following silicon layer are selectively grown using PH_3 , GeH_4 and Si_2H_6 gas chemistry. After then other standard CMOS processes such as gate oxidation, polysilicon and spacer formation and source/drain implantation can be followed [8]. The second way is to use Ge ion implantation. After the V_{th} channel implantation, Ge ions are implanted into the active area of protection transistor with its peak dopant concentration can be

formed around 3000 Å away from silicon surface. Recently, the Ge ion implantation has become a popular process [7], [9] and this technique will be simpler than the film growth for the new protection transistor. Although the melting point of Ge is lower than that of Si, since the Ge mole fraction is only 0.2 and the SiGe layer is formed far away from the overheating region (silicon surface), it would not cause a melting problem during ESD stress. Also, it has been reported that SiGe films with Ge mole fraction up to 0.6 are compatible with standard VLSI fabrication process [23].

In this work, the relative comparison of the electrical and thermal properties of SiGe and normal protection transistors is the main goal, while the precise temperature is not attainable.

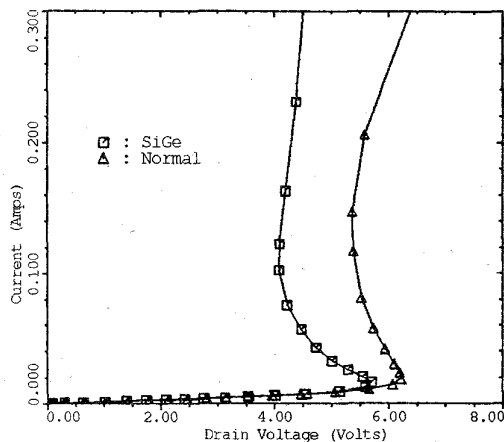


Fig. 8. Simulated snapback voltages (V_{sp}) for the SiGe (rectangle) and normal (triangle) protection transistors.

Prior to ESD simulation, we evaluated the basic electrical parameters, such as the threshold voltage (V_{th}), the drain saturation current (I_{dsat}) and the breakdown voltage (BV_{ds}) of the SiGe NMOS transistor compared to those of normal one. We found there are indeed no differences between two structures, as shown in Table I. Because the additional SiGe layer is formed underneath of the silicon surface, it hardly affects the normal device characteristics. Hence, no additional procedures are needed for using SiGe heterojunction structure as a protection transistor.

V. RESULTS AND DISCUSSIONS

To evaluate the characteristics of SiGe NMOS for ESD stress, the Machine-Model (MM) [24] with 300 V level was forced to the protection circuit. Then we investigated the internal device characteristics and the thermal variation as a function of time. The protection circuit for this work is illustrated in Fig. 1, which is composed of a protection transistor ($W/L = 135 \mu\text{m}/0.7 \mu\text{m}$), a diffusion resistor ($R_d = 5 \Omega$) and a simplified internal circuit, and the ESD stress is entered from an input PAD.

Figs. 4(a) and 5(a) show the current flowlines of the SiGe structure and the normal structure at 0.5 ns when the avalanche breakdown is about to occur. In the SiGe structure, although the complete parasitic bipolar action is not formed yet, most ESD induced current entered from the drain contact are moving away into the source region mainly along the buried layer. Whereas, in the normal NMOS structure, large amount of induced current flows down to the bottom of substrate, as shown in Fig. 5(a). This can be understood by monitoring their internal characteristics, such as the potential distribution, the hole concentration and the current density. In Fig. 4(b) and (c), in the SiGe case, a concave quantum well, whose potential is relatively lower, is formed between the source and the drain region caused by the bandgap reduction of the SiGe layer. In the normal case, the potential distribution versus the depth distance is almost flat so that the generated holes cannot be effectively collected near the source and the

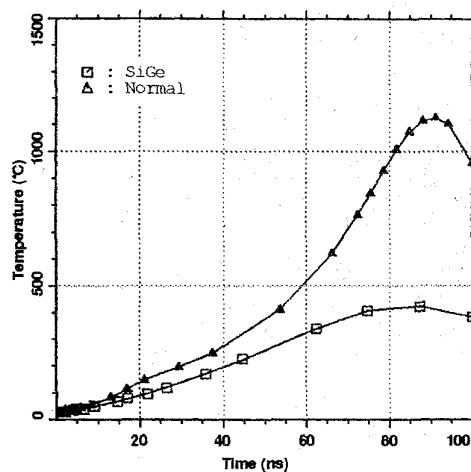


Fig. 9. Simulated peak temperature values for the SiGe (rectangle) and normal (triangle) protection transistors.

substrate junction region, as illustrated in Fig. 5(b) and (c). Due to the effect of the low potential in SiGe layer, it is shown that the hole concentration between the source and the drain region is higher ($p \cong 1.0 \times 10^{17} \text{ cm}^{-3}$) than that of the normal transistor ($p \cong 0.3 \times 10^{17} \text{ cm}^{-3}$). These holes raise the substrate potential and the forward bias needed for turning on the parasitic bipolar action between the emitter and the base is easily obtained in the SiGe structure.

In Figs. 6(a) and 7(a), complete bipolar actions are shown for two structures at 70 ns, at which time the peak current and the peak lattice temperature are produced. Here, we can obviously see the current localization near the drain and the bulk junction region on silicon surface in the normal transistor, as shown in Fig. 7(a), while most current flows mainly through the buried layer in the SiGe transistor, which strongly suppresses the current localization and local temperature overheating, as shown in Fig. 6(a). To understand the internal phenomena, Fig. 6(b)–(d) and Fig. 7(b)–(d) illustrate current densities, hole concentrations and potential distributions of the two structures, respectively. Similar to the initial stage at 0.5 ns, the quantum well still remains, and the potential is lower by 1.6 V than the normal one, as shown in Figs. 6(b) and 7(b), which means that the power consumption at drain region can be reduced by using the SiGe layer. In addition, the hole concentration inside of the SiGe layer is relatively higher ($p \cong 0.5 \times 10^{19} \text{ cm}^{-3}$) than that of the normal one ($p \cong 0.3 \times 10^{18} \text{ cm}^{-3}$) on account of the lower potential path, as shown in Figs. 6(c) and 7(c). Thus, most bipolar-induced-current passes through the path, which strongly suppresses the current localization, as shown in Fig. 6(d). The peak current density on the silicon surface in the SiGe structure is $J \cong 0.2 \times 10^{17} \text{ A/cm}^2$, while that of the normal transistor is $J \cong 1.0 \times 10^{17} \text{ A/cm}^2$, as plotted in Figs. 6(d) and 7(d). The higher current density causes the higher local temperature, since the heat generation in the semiconductor increases as the current density increases.

For evaluating the robustness of ESD protection transistors, the snapback voltage (V_{sp}) and the second breakdown current

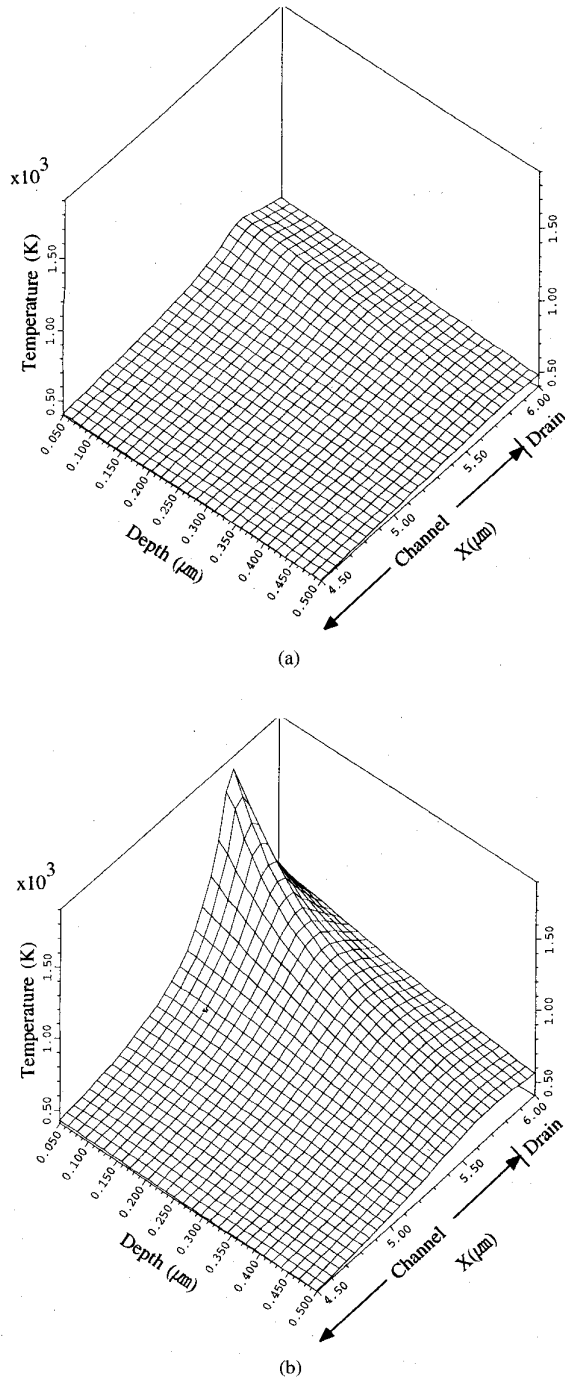


Fig. 10. Simulated peak temperature distribution (a) SiGe structure (b) normal structure.

(I_{t2}) in the voltage-current characteristics of the protection transistor are important parameters [1]. As shown in Fig. 8, the simulated V_{sp} of the SiGe transistor is 4 V, which is lower by 1.5 V than that of the normal transistor. According to C. Duvvury *et al.* [10], ESD performance is improved as V_{sp} decreases, since during the high-current ESD stress, the voltage is clamped at V_{sp} level. Thus, we expect that a SiGe protection transistor is more reliable for the ESD

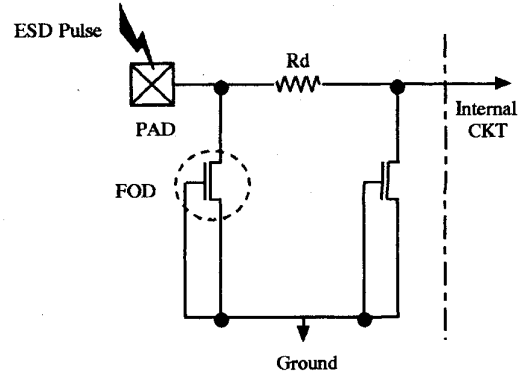


Fig. 11. Simplified equivalent circuit with Field-Oxide Device(FOD) and ladder type NMOS.

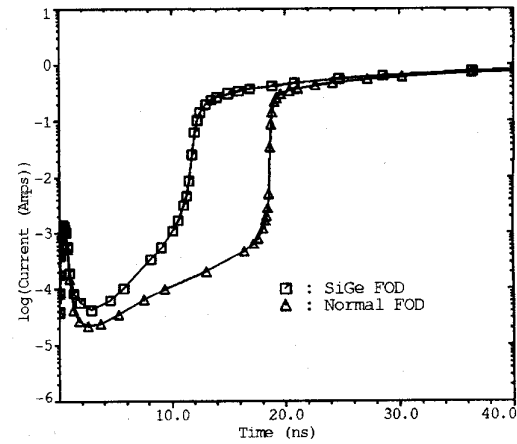


Fig. 12. Simulated time vs. current characteristics of SiGe and normal FOD.

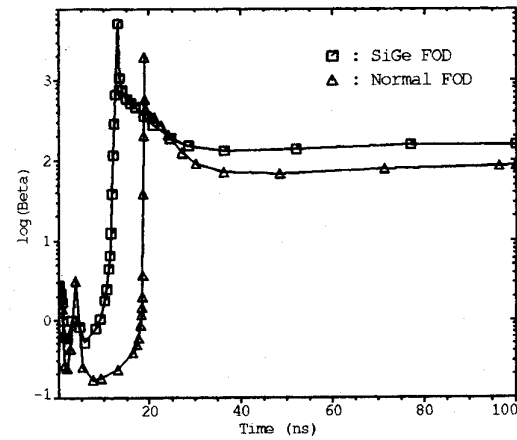


Fig. 13. Simulated bipolar current gains (β) of SiGe and normal FOD.

protection transistor by the lower V_{sp} which ensures less power consumption compared to that of the normal protection transistor. The simulated I_{t2} of the normal transistor is 0.5A while the second breakdown does not occur in the SiGe transistor.

In Fig. 9, the maximum temperatures of two protection transistors are plotted as a function of ESD stress time. The maximum temperature of the SiGe structure is 400°C, which is much lower than that of the normal structure, 1150°C. This result can be confirmed by monitoring temperature distributions of two structures, as shown in Fig. 10(a) and (b). Because of the lower current density in the SiGe structure, the peak temperature is lower than the normal transistor and is widely distributed along the drain junction region compared to the normal structure. When the peak current becomes higher, it causes various ESD failures that were mentioned at the previous section. To avoid the temperature overheating by ESD stress, there are few choices but to change the area of protection transistors. Though increasing the area of the transistor is one of the general ways, it leads to an additional area penalty. Therefore, using a SiGe protection transistor is an effective solution to avoid various ESD failures caused by the lattice overheating without area penalty and degraded electrical performances.

Bandgap engineering using a SiGe heterojunction layer can also be applied to the protection circuits with a Field Oxide Device (FOD), which is applied to the protection circuits to steer ESD induced current into the ground as a primary protection with a ladder structure transistor [25], [26]. If the FOD cannot begin the parasitic bipolar action quickly together with the ladder structure transistor, ESD failures can occur. In order to evaluate the turn-on speed of a FOD including a SiGe buried layer, simulation was also performed to the circuit composed of FOD and ladder structure NMOS transistors, as illustrated in Fig. 11. The channel length and width are 1.2 μm and 150 μm , respectively, and the thickness of field oxide is 4500 Å. Note that since the breakdown voltage of the FOD is higher than that of the ladder type transistor, the ladder transistor turns on earlier than the FOD. The actual turn-on of the FOD transistor is followed several nanoseconds later, operating as the primary protection transistor.

As a simulation result, in the case of a SiGe FOD, it turns on at 11 ns, which is faster by 8 ns than that of the normal FOD, as shown in Fig. 12. Also as expected in the previous section, the parasitic bipolar current gain (β) of the SiGe FOD is higher than the normal one by more than 10 times before 20 ns and 2 times after turning on the complete bipolar behavior, respectively, as illustrated in Fig. 13. Thus we can find that the SiGe layer can not only shorten the delay interval between the ladder type and the FOD, but also shunt larger current than the conventional FOD.

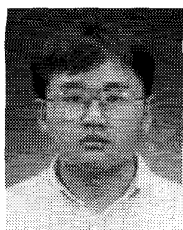
VI. CONCLUSIONS

The ESD performances of a SiGe layer protection transistor were studied compared to a normal NMOS protection transistor by using device simulation. The bandgap engineering with SiGe heterojunction layer was shown to be very efficient to shunt ESD induced current without affecting device degradation and area penalty. In a SiGe structure, the lower snapback voltage and faster parasitic bipolar turn-on condition were obtained. Since the SiGe layer provides uniform current distribution and suppresses the local temper-

ature overheating, the proposed SiGe layer protection transistor can be a prominent ESD protection transistor for future technologies.

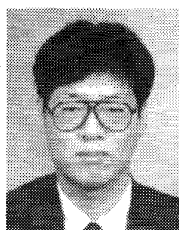
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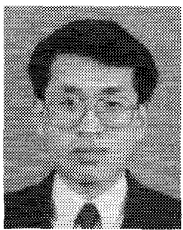
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