

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00794
Patent 10,950,923 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Micron Technology, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–11 of U.S. Patent No. 10,950,623 B2 (Ex. 1001, “the ’623 patent”). Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 8 (“Prelim. Resp.”). The Petition is supported by a declaration from Dr. Jack C. Lee. Ex. 1003 (“Lee Declaration”). The Preliminary Response is supported by a declaration by Dr. Jonathan Bradford. Ex. 2007 (“Bradford Declaration”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons given below, on this record, Petitioner has established a reasonable likelihood that it would prevail in showing the unpatentability of claims 1–11 of the ’623 patent. Accordingly, we institute an *inter partes* review as to claims 1–11 of the ’623 patent on all asserted grounds of unpatentability.

B. *Real Parties in Interest*

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 5. Patent Owner identifies itself as a real party-in-interest. Paper 4, 2.

C. *Related Matters*

The parties represent that the ’623 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and*

Micron Consumer Products Group, LLC, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 4, 2; Pet. 4.

Petitioner has also filed IPRs challenging other patents asserted in the district court cases, namely U.S. Patent Nos. 10,658,378 (IPR2024-00788), 10,861,872 (IPR2024-00789), 10,868,031 (IPR2024-00790), 10,937,806 (IPR2024-00791), 11,501,822 (IPR2024-00795), 11,468,957 (IPR2024-00792), and 11,600,342 (IPR2024-00793). Pet. 5.

D. The '623 Patent

The '623 patent is titled “3D NAND Memory Device and Method of Forming the Same.” Ex. 1001, code (54). The '623 patent issued from Application No. 16/365,725, filed on March 27, 2019, and claims priority via a continuation to PCT/CN/2018/119908, filed on December 7, 2018. *Id.* at code (63). The '623 patent relates to “formation of a 3D NAND memory device with a divided block structure.” *Id.* at 1:32–33.

E. Illustrative Claim

Claim 1 is illustrative, and recites as follows:¹

[1.Pre] A memory device, comprising:

[1.A] a substrate;

[1.B] a bottom select gate (BSG) disposed over the substrate;

[1.C] a plurality of word lines positioned over the BSG with a staircase configuration;

[1.D] a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;

[1.E] one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and

¹ Bracketed organization added as per the Petition.

[1.F] one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.

F. Evidence

Petitioner relies on the following patent document evidence.

Name	Patent Document	Exhibit
Park et al. ("Park")	US 10,559,583 B2	1004
Shibata et al. ("Shibata")	US 2019/0122734 A1	1005

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–11 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–11	103 ²	Park
1–11	103	Park, Shibata
1–11	103	Shibata, Park

II. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art [to which said subject matter pertains].” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any

² Petitioner asserts, and we accept for purposes of institution, that AIA 35 U.S.C. 103 applies to the ’623 patent. *See* Pet. 19.

differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.³ See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art [“POSITA”] at the critical time “would have had a bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 19 (citing Ex. 1003 ¶¶ 36–37). Petitioner further asserts that a POSITA “would have been aware of and generally knowledgeable about 3D NAND’s structure, its component parts, how it operates, and how it is controlled.” *Id.* Patent Owner does not provide any such assessment in its Preliminary Response. For purposes of this Decision, we adopt Petitioner’s proposed level of ordinary skill, as it appears to be consistent with the specification of the ’623 patent and the prior art of record.

C. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire

³ Neither party presents evidence or arguments regarding objective evidence of non-obviousness at this stage.

patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Here, neither party sets forth any claim construction. Pet. 18; Prelim. Resp. 12–13. However, in discussing Petitioner’s obviousness contentions, the parties dispute the term “trenches,” and the phrase, “the or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” Pet. 33–35 (arguing Park’s layer 111 is a “trench”), 35–36 (arguing that Park’s layer 111 in combination with Park’s lines 105 “separate” the BSG); PO Resp. 29–33 (arguing Park’s layer 111 is not a “trench”), 35–38 (arguing that Park’s layer 111 does not separate the BSG because Park’s lines 105 are also required for separation). We address these construction issues *infra* at Section II.D.2 of this decision. For the remainder of the claim limitations, we do not need to determine a particular construction, and instead construe the claims pursuant to § 42.100(b).

D. Obviousness over Park

Petitioner asserts that claims 1–11 are unpatentable under 35 U.S.C. § 103 as obvious over Park. Pet. 25. Patent Owner argues against this assertion. Prelim. Resp.

Upon consideration of Petitioner’s explanations and the totality of evidence in this current record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in showing that claims 1–11 are unpatentable under 35 U.S.C. § 103 as obvious over Park.

1. Park

Park is titled “Memory Device.” Ex. 1004, code (54). Park relates to a semiconductor memory device having “gate electrode layers stacked on an upper surface of a substrate and each including a plurality of unit electrodes

extending in a first direction, and a plurality of connecting electrodes connecting the unit electrodes to each other.” *Id.* at code (57). The device also includes “channel structures extending through the gate electrode layers in a direction perpendicular to the upper surface of the substrate, first common source lines extending in the first direction and interposed between the unit electrodes.” *Id.* The device further includes “second common source lines extending in the first direction between the first common source lines and each having a first line and a second line separated from each other in the first direction by the connecting electrodes.” *Id.*

2. Analysis of Claim 1

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 1. Patent Owner does not specifically argue against Petitioner’s assertions for limitations [1.Pre]–[1.D]; however, we draw no inference therefrom and Petitioner bears the burden of persuasion.

[1.Pre]–[1.D] A memory device, comprising: a substrate; a bottom select gate (BSG) disposed over the substrate; a plurality of word lines positioned over the BSG with a staircase configuration; a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines

Petitioner asserts that limitations [1.Pre]–[1.D] are taught by Park in the following manner. Petitioner points to Park’s description of a “3D memory device” that includes a “substrate 101” and a plurality of memory cell strings that each include a ground select transistor connected to a ground select line (“GSL”), which Petitioner asserts teaches the claimed “bottom select gate” because the GSL controls connection of the memory cell strings to a common source line in the same manner as the ’623 patent. Pet. 25–27 (citing Ex. 1004, 1:14–17, 1:31–32, 3:24–27, 4:17–30, 10:34–35, Fig. 11;

Ex. 1001, 1:37–46; Ex. 1003 ¶¶ 127–137). Petitioner further points to the plurality of Park’s word lines, “WL,” each of which are connected to a row of memory cells in memory cell array 2. *Id.* at 27–28 (citing Ex. 1004, 3:28–36, 1:62–2:8, 3:39–44, 4:22–24, Fig. 2; Ex. 1003 ¶¶ 138–143). Petitioner points to Figure 4 of Park as illustrating that the word lines 120*b-i* are positioned over the substrate and the ground select line 120*a*. *Id.* at 28–29 (citing Ex. 1004, Fig. 4, 6:65–7:2; Ex. 1003 ¶¶ 144–147). Petitioner asserts that the claimed “staircase configuration” of word lines is taught by Park’s “stepped structure” of gate electrode layers. *Id.* at 29 (citing Ex. 1004, 6:56–60, 7:8–11, 8:18–50, 11:62–65, Figs. 15, 25, 32; Ex. 1003 ¶¶ 148–150).

Petitioner asserts that the claimed insulating layers are taught by Park’s insulation layers 130 that are present between substrate 101 and ground select line 120*a*, and between the ground select line 120*a* and the word lines 120*b-i*. *Id.* at 29–30 (citing Ex. 1004, 5:17–23, 6:49–52, 10:35–37, 10:40–45, Fig. 11; Ex. 1003 ¶¶ 151–160).

Patent Owner does not, at this stage, argue against these assertions. Upon review of Park, we determine that Petitioner’s assertions are supported by the record in a manner sufficient for institution.

[1.E] one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs

Petitioner asserts that Park’s isolation insulating layers 111 teach the claimed dielectric trenches that separate Park’s ground select line into a plurality of sub-ground select lines; i.e., those portions specific to unit areas AU1–UA8. *Id.* at 30. Petitioner provides an annotated Figure 3:

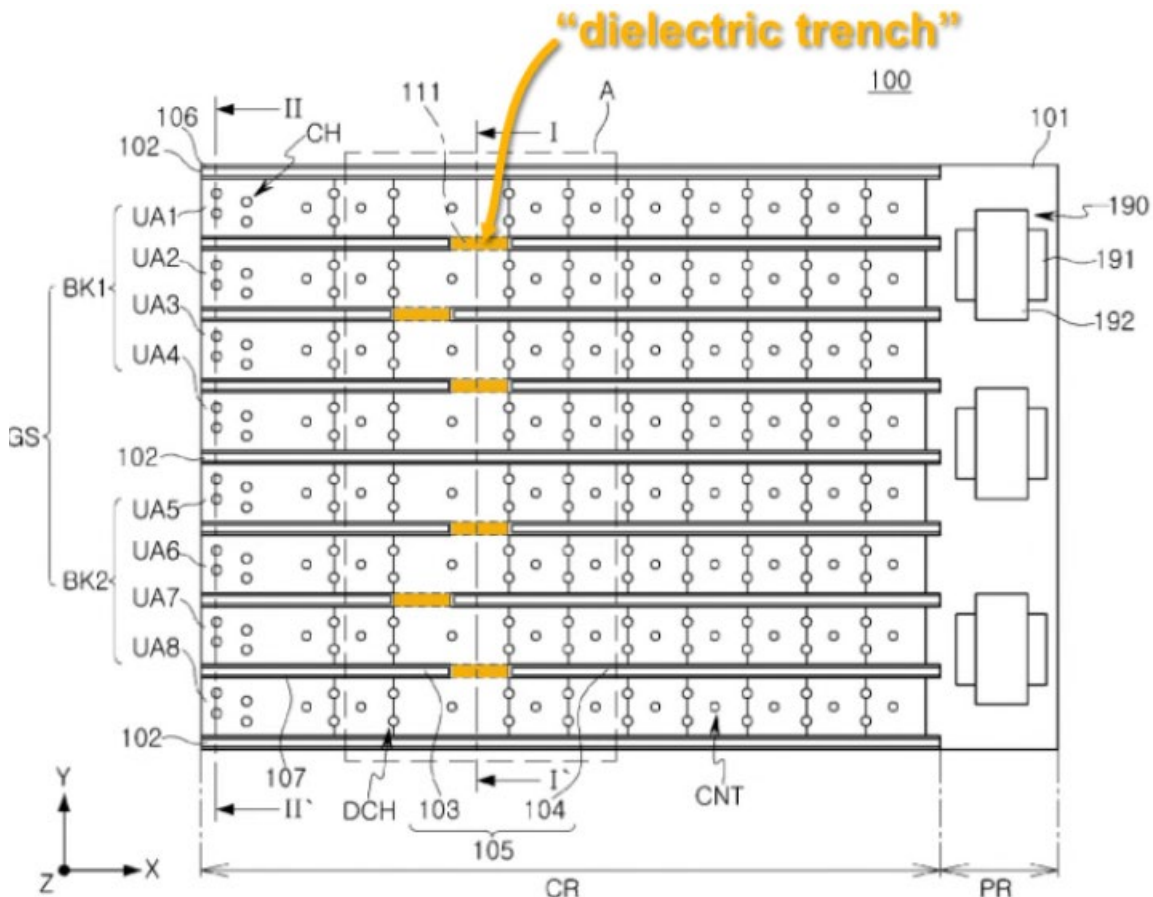


FIG. 3

Annotated Figure 3 portrays a “top-down view” showing isolation layers 111 (orange) located between common source lines 102, extending lengthwise to close the gaps between common source lines 105 and to separate the ground source line (“GSL”) in blocks BK1 and BK2 into unit areas UA1–UA8. *Id.* at 31.

Petitioner asserts that this teaches limitation [1.E]:

Park includes “one or more first dielectric trenches formed in the BSG” (isolation insulating layers 111 formed within its GSL). These “dielectric trenches” “extend[] in a length direction of the substrate” (layers 111 extend lengthwise in the X-axis direction). Further, the “dielectric trenches” “separate the BSG into a plurality of sub- BSGs” (layers 111 cause Park’s GSL to be divided into portions corresponding to unit areas UA1-UA8).

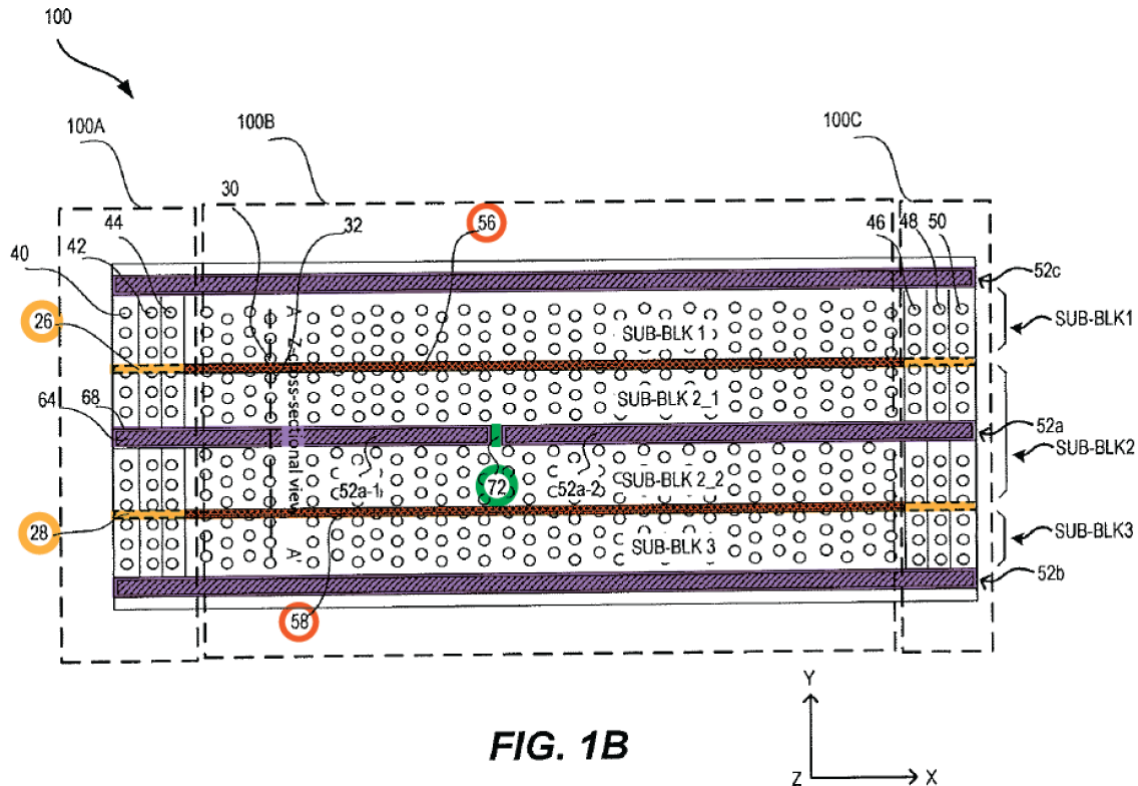
Pet. 32.

a) The “trench” limitation

Petitioner asserts that one having ordinary skill in the art would have understood layer 111 to teach a trench, because it is formed in the same manner as the trenches in the '623 patent. Petitioner asserts that Park's layer 111 is formed by creating an opening (a trench) that is filled with insulating material. *Id.* at 33 (citing Ex. 1004, 12:65–13:1, 13:15–17, Figs. 11, 20, 21). Petitioner asserts that the trenches in the '623 patent are formed in an analogous manner, by forming trench openings through the desired layers and then filling those openings with dielectric material. *Id.* (citing Ex. 1001, 16:1–18, 17:43–55. Petitioner asserts that both Park and the '623 patent employ sacrificial layers to form such trenches. *Id.* (citing Ex. 1001, 7:1–16, 15:45–46; Ex. 1004, 12:65–13:1; Ex. 1003 ¶¶ 172–176).

Patent Owner argues against Petitioner's characterization of Park's layers 111 as “trenches.” Prelim. Resp. 28–33. Patent Owner argues that Park's insulating layers are “cuts” and not “trenches.” *Id.* Specifically, Patent Owner argues that the '623 patent distinguishes an “H-cut” positioned between subdivisions of a common source region (CSR) from “trenches” that extend along the BSG and TSG. *Id.* at 29–31 (quoting Ex. 1001, 9:13–18 (“the **CRS 52a is separated by an H-cut 72 into two sub-CSRs 52a-1 and 52a-2**”)). Patent Owner argues that Park's layer 111 divides Park's common source regions in the same manner. *Id.* at 30 (citing Figure 1B). Patent Owner provides an annotated version of Figure 1B of the '623 patent

to illustrate this alleged similarity:



Annotated Figure 1B shows a top-down view of the 3D-NAND memory device 100, including common source regions 52a–52c extending along the X-direction (length direction) of substrate 10, in which common source region 52a is separated by an “H-Cut” 72 into two sub-CSRs 52a-1 and 52a-2, and in which “trenches” 26, 28, 56, and 58 are disposed between common source regions 52a and 52b. Prelim. Resp. 31–32; Ex. 1001, 8:65–9:27.

On the current record, Petitioner has sufficiently shown for purposes of institution that Park’s insulating layer 111 teaches a “trench” as set forth in claim 1. It is not determinative that Park does not term its layer 111 as a trench. In determining whether a claimed term is taught by the prior art, we are not confined to determining whether the prior art uses the identical term, but instead, we look “through the viewing glass of a person skilled in the art,” by reviewing evidence including the written description and drawings.

Brookhill-Wilk I, LLC. V. Intuitive Surgical, Inc., 334 F.3d 1294, 1298 (Fed. Cir. 2003). Petitioner asserts that Park’s layer 111 is formed in the same manner as the trenches in the ’623 patent; i.e., by forming trench openings through the desired layers and then filling those openings with dielectric material. *See* Ex. 1001, 7:39–41 (“trenches . . . are filled with . . . dielectric materials”). Patent Owner does not contest that the processes are similar or that both result in a dielectric-filled volume. Prelim. Resp. 33. Therefore, to the extent required to resolve Petitioner’s obviousness assertion over Park, at this stage of the proceeding we construe the claim term “trench” as encompassing a dielectric-filled opening in a layer. The parties are invited to address the meaning of the term “trench” during trial if they so desire, to the extent permitted by our rules.

Unlike Park’s dielectric-filled layer 111 and the dielectric-filled trenches 26, 28, 56, and 58 of the ’623 patent, H-cut 72 of the ’623 patent is described as electrically conducting, thereby undercutting Patent Owner’s analogy to Park’s electrically insulating layer 111. *See* Ex. 1001, 9:41–44 (“SUB-BLK2_1 and SUB-BLK[2_2 are] electrically connected with each other through the H-cut 72”), Fig. 1B; Ex. 1003 ¶ 182. Although the ’623 patent terms some openings as H-cuts, the insulating nature of Park’s insulating layer 111 supports Petitioner’s assertion that it teaches the claimed trench.

b) The “to separate the BSG into a plurality of sub-BSGs” limitation

With respect to the limitation that “the dielectric trenches . . . separate the BSG into a plurality of sub-BSGs,” Petitioner asserts that this is taught even where the trenches cooperate with other structure to perform such separation. *Id.* at 35 (citing Ex. 1004, 6:8–12, Fig. 3). Petitioner further

asserts that Park’s insulating layer 111 satisfies the claimed function because it “cooperates with common source lines to divide Park’s GSL into portions.” *Id.* Petitioner points to the ’623 patent as also using additional structure, in the form of common source regions 52c and 52b, to “play a role in separating the memory into blocks and sub-blocks.” *Id.* (citing Ex. 1001, Fig. 1B, 9:3–8).

Patent Owner further argues that Park’s insulating layers do not extend along the length of the substrate to separate the BSG into a plurality of separate BSGs. Prelim. Resp. 34–38. Patent Owner argues that regardless of any similarities in their formation, Park’s layer 111 is a short region that separates the second common source line, and thus, not a trench. *Id.* at 33. Patent Owner further argues that Park’s unit areas “UA1-UA8 are not separated solely by the isolation insulating layers; rather, Park teaches that they are separated by second common source lines in conjunction with the isolation insulating layers.” *Id.* at 37–38 (citing Ex. 1005, 16:55–59, 10:60–65). Patent Owner argues that the claimed separation must be performed solely by the trenches, because the “trenches of the ’623 patent extend the entire length of the memory device.” *Id.* at 38.

To resolve this dispute, we must construe the phrase “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” Beginning with the language of the claim, the phrase is centered on the trench and its function (or further structural limitation) of separating the BSG into a plurality of sub-BSGs. The phrase permits multiple trenches, rather than any single trench, to separate the BSG. The phrase does not explicitly state whether the separation of the BSG into a plurality of sub-

BSGs must be performed solely by the trenches, or whether other structural features may also cooperate in such a separation.

To assist in understanding the phrase at issue, we turn to the description in the disclosure of the '623 patent. As highlighted by Patent Owner, the '623 patent describes that “first trenches 26 and 28 extend in an X-direction (i.e., length direction) of the substrate 10 to separate the BSG 62p . . . into a plurality of sub-BSGs.” Ex. 1001, 7:17–24 (“for example, three sub-BSGs 62p-1, 62p-2, and 62p-3”); Prelim. Resp. 7–8. The separation is performed “by introducing the first and second trenches into the memory device,” which divides the memory cell block into a plurality of sub-blocks, i.e., sub-BSGs. Ex. 1001, 7:33–37 (“For example, sub-blocks SUB-BLK1–3 are formed in FIG. 1B.”), 7:45–47, 2:64–65 (“Each of the sub-blocks accordingly has a respective sub-BSG”). The trenches extend parallel to common source regions along the length direction of the substrate. *Id.* at 2:38–41.

As asserted by Petitioner, the '623 patent describes common source regions 52b and 52c at its sub-block boundaries. Ex. 1001, Fig. 1B, 9:3–8; Pet. 35. These common source regions, in the embodiments of Figure 1A and Figure 1B, “further isolate the memory device from adjacent components,” such as “from adjacent memory cell blocks.” Ex. 1001, 9:5–8. As tacitly admitted by Petitioner in its omission of common source region 52a (which separates sub-block 2 further into electrically connected portions sub-block 2_1 and 2_2), the '623 patent does not describe the common source regions performing any separation of the BSG (or block) into sub-BSGs (or sub-blocks). *See* Pet. 35; Ex. 1001, 9:13–14 (“The common source region 52a is disposed at a middle position of the memory device”); 9:41–44, Fig. 1B. Thus, in the described Figure 1A and Figure 1B

embodiments of the '623 patent, the common source regions define the boundaries of the sub-BSGs and isolate them from adjacent BSGs, but do not act within a single BSG to separate it.

In view of the claim language and the description in the '623 patent, we construe the phrase “the dielectric trenches . . . separate the BSG into a plurality of sub-BSGs” as requiring that the trenches separate the BSG into sub-BSGs, but that other components are not excluded from cooperating in the separation of the BSG into sub-BSGs. The '623 patent states that separation occurs “[b]y introducing the . . . trench[] into the memory device.” Ex. 1001, 7:45–47. Claim 1 does not require any particular structure of the memory device, and as discussed above, the described structures in the '623 patent, which are described as purely exemplary, indicate that structures such as the common source regions may assist in defining the boundaries of the BSG and sub-BSGs.

On the current record, Petitioner has sufficiently shown for purposes of institution that Park’s insulating layer 111 teaches a “trench” that “separate[s] the BSG into a plurality of sub-BSGs.” As acknowledged by Patent Owner, Park’s areas UA1-UA8 are separated by the common source lines *in cooperation with* isolation insulating layer 111. *See* Prelim. Resp. 37–38 (citing Ex. 1004, 6:8–12, 10:60–65, Fig. 3). Petitioner asserts that Park’s BSG would not be separated at certain points (i.e., gaps in its common source lines) if Park’s trench layers 111 were not there. Pet. 35–36. Petitioner asserts that the BSG is fully separated into sub-BSGs because the common lines 105 also divide the BSG, and the separation performed by the trenches causes the sub-BSGs to become completely separate. *Id.* Under our construction, this is sufficient to meet the “to separate” limitation of claim 1.

Moreover, at this stage of the proceeding, we do not understand claim 1 to require that the trench extend the entire length of the memory device, as argued by Patent Owner. Ex. 1001, 23:55–57. Instead, claim 1 states only that the claimed trench extends “in a length direction of the substrate.” *Id.* For purposes of institution, on the current record we determine that Petitioner’s assertions are persuasive on this issue.

Finally, Patent Owner argues that Park’s layer 111 does not separate the BSG into a plurality of sub-BSGs because Park’s layer is in the staircase region and not in the cell string-containing active region as described in the ’623 patent. Prelim. Resp. 36 (citing Ex. 1001, 1:50–57, Fig. 1E). However, we do not find this argument availing at this stage of the proceeding because Park clearly describes its layer 111 as being within, and dividing, its gate electrode layer 120; i.e., its BSG in its active region. Ex. 1004, 10:34–67. Moreover, the ’623 patent also describes that its staircase region has “dummy” BSGs that are separated into a plurality of sub-BSGs by trenches. Ex. 1001, 6:55–61, 8:38–64, 17:31–36. Therefore, on this record, Patent Owner’s argument does not detract from Petitioner’s persuasive showing that Park teaches limitation [1.E].

[1.F] one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.

Petitioner asserts that Park teaches common source regions through Park’s “common source line[s] 102.” Pet. 37. Petitioner further asserts that Park’s Figure 3 shows these source lines extending in the same X-axis direction as Park’s trenches 111. *Id.* (citing Ex. 1004, Fig. 3, 10:46–50). Petitioner further asserts that Park’s Figure 11 shows these source lines

extending through the BSG (GLS 120a), the plurality of word lines 120b–120i, and the plurality of insulating layers (annotated in green). *Id.* at 38 (citing Ex. 1004, Fig. 11; Ex. 1003 ¶¶ 188–194). Patent Owner does not specifically contest these assertions.

We agree that Petitioner’s assertion is supported by the record and, accordingly, that Petitioner has sufficiently shown that Park teaches limitation [1.F] for purposes of institution.

Conclusion

For the foregoing reasons, Petitioner has demonstrated a reasonable likelihood that it will prevail on showing that claim 1 is obvious over Park.

3. Analysis of Claims 2–11

Patent Owner does not specifically contest Petitioner’s assertions as to claims 2–11; however, the burden of proving unpatentability rests solely upon Petitioner. Upon review of these assertions, we determine that they are supported by the record such that Petitioner has demonstrated, by a reasonable likelihood, the unpatentability of claims 2–11 over Park.

E. Obviousness over Park and Shibata

Petitioner asserts that claims 1–11 are obvious over Park and Shibata, presenting two alternate theories. Pet. 57 (Park in view of Shibata), 63 (Shibata in view of Park). Because we have determined that Petitioner has shown a reasonable likelihood that at least one claim would have been obvious over Park, we need not determine the merits of Petitioner’s combinations of Park and Shibata for purposes of institution. However, we provide the following analysis, based on the current record, for purposes of furthering the proceedings at the trial phase.

1. Shibata

Shibata is titled “Semiconductor Memory Device.” Ex. 1005, code (54). Shibata relates to a semiconductor memory device having multiple alternating conductive and insulating layers, in which the conductive layers include multiple word lines functioning as control gates of memory cells and select gates functioning as control gates of select transistors. *Id.* ¶ 3.

2. Analysis of Claim 1, Limitation [1.e]

a) Park in view of Shibata

Petitioner applies Shibata’s teachings to address potential arguments that Park’s layers 111 do not teach “trenches” as claim 1 requires. Pet. 57. Petitioner points to Shibata’s separation portions 62a as dividing its drain-side select gate layer (i.e., its top select gate), causing the TSG to be divided into sub-TSGs. *Id.* at 58 (citing Ex. 1005 ¶¶ 2–3, 90, 166, Fig 16). Petitioner points to Shibata’s description of those portions as “extending in the same direction as the separation portions 60 (the slits ST) piercing the entire stacked body 100.” *Id.* at 59 (citing Ex. 1005 ¶¶ 65, 166). Petitioner asserts that one having ordinary skill in the art would have found it obvious to replace Park’s second common source lines 105 with longer insulating regions 111 analogous to Shibata’s separation portions 62a. *Id.* at 59. Petitioner provides the following illustration of its proposed combination:

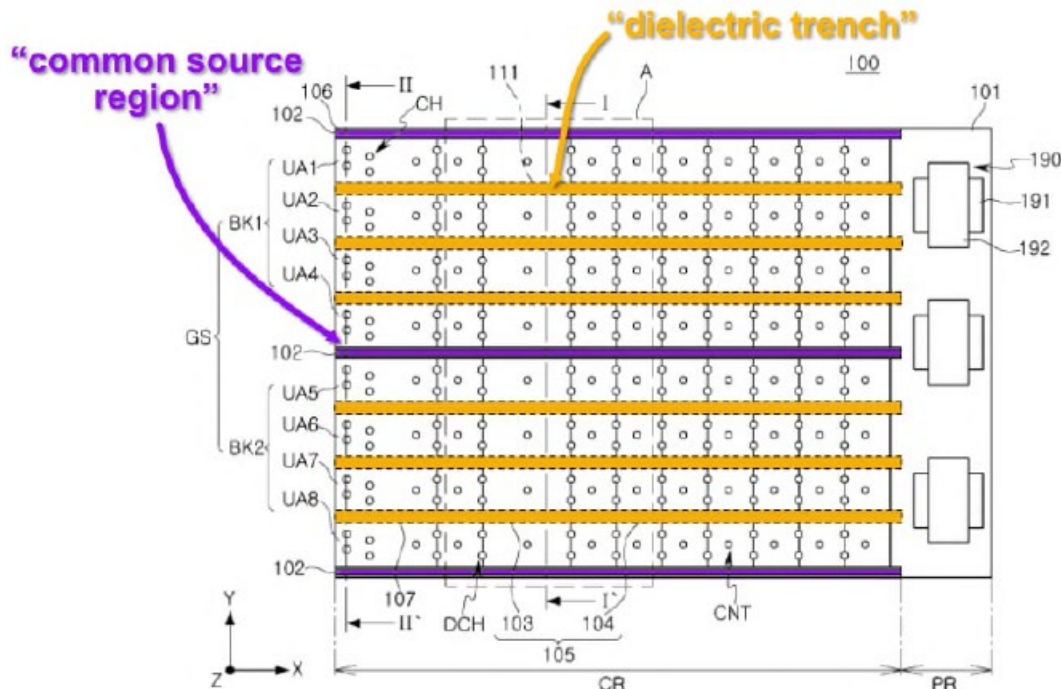


FIG. 3

Id. at 59–60 (citing and annotating Fig. 3). Petitioner’s annotated Figure 3 from Park depicts a “top-down view” showing isolation layers 111 (orange) replacing common source lines 105 and located between common source lines 102, extending lengthwise to separate the ground source line (“GSL”; i.e., the BSG) in blocks BK1 and BK2 into unit areas UA1–UA8 (i.e., sub-BSGs). *Id.* at 60. Petitioner’s combination would likewise include such trenches into Park’s TSG to allow Park’s upper SSL to continue to be divided into individually controllable portions, thereby performing the function of the replaced common source regions in the TSG. *Id.* (citing Ex. 1005, 5:65–6:12, 7:19–29, 16:22–37).

As motivation to perform such a replacement, Petitioner points to Shibata’s explanation that the use of dielectric separation portions as a replacement for some of the common source regions results in an improved device because it would reduce the planar size of the memory cell array. *Id.* at 61 (citing Ex. 1005 ¶¶ 118, 154). Petitioner points to additional evidence

in the record that reduction of common source regions are advantageous. *Id.* (citing Ex. 1009 ¶ 1 (“a large number of source contacts in a memory array ... degrade the efficiency of the memory array and result in a large die size and a high fabrication cost”)). Petitioner relies on testimony from its declarant, Dr. Lee, to support that the asserted replacement would result in a smaller device with additional memory density and would still perform its intended function. *Id.* (citing Ex. 1003 ¶¶ 308–314). Dr. Lee further testifies that such a combination would amount to nothing more than a routine, obvious design choice because “it was known that select gates can be divided into individually controllable portions by either trenches of insulation or common source regions,” and would have recognized that such combination would enjoy a reasonable expectation of success. *Id.* at 61–62 (citing Ex. 1003 ¶¶ 315–318). Petitioner further asserts, based upon testimony by Dr. Lee, that replacement of some of Park’s common lines with insulating layers “ensures that the majority of sacrificial layers are removed and replaced with conductive material, thereby improving device performance without the need for separate drivers.” *Id.* at 62–63 (citing Ex. 1003 ¶¶ 319–324).

Patent Owner argues that Shibata teaches that its separation portions traverse only the upper select gate layers, and specifically teaches not to extend its separation portions to separate the bottom select gate layers Prelim. Resp. 42–43 (citing Ex. 1005 ¶ 137). Thus, Patent Owner argues that a person having ordinary skill in the art would not have combined the teachings of Shibata with Park so as to separate the BSG into a plurality of sub-BSGs as required by claim 1. *Id.* at 43.

Patent Owner further argues that Park teaches away from the combination because Park “actively discourages elongating the isolation

insulating layers because the longer paths by which the etching solution must flow could prevent the complete removal of the sacrificial layer and cause voids in the gate electrode layers GLs.” *Id.* at 43–44 (citing Ex. 1004, 15:35–16:49). Patent Owner similarly argues that placing isolation layers side-by-side would block the flow of etching solution that is required to remove sacrificial layers and form active layers. *Id.* at 44 (citing Ex. 1004, 15:35–16:49). Patent Owner further supports its argument by pointing out that Park seeks to stagger its insulating layers 111, which would not be possible if those layers span the entire length of the memory array as proposed by Petitioner’s combination. *Id.* (citing Ex. 1004, 15:60–16:2). Patent Owner further argues that Petitioner has mischaracterized the potential advantages of Shibata, providing reasons why Shibata does not support Petitioner’s asserted combination and detailing adverse effects that would be caused by Petitioner’s proposed reduction of the number of common source lines. *Id.* at 46–50.

On the current record, Patent Owner has raised significant questions as to the desirability of Petitioner’s proposed combination. Although the determination of obviousness recognizes that many desirable design options involve both advantages and disadvantages, Patent Owner has called into question the technical merits of Petitioner’s proposed advantages while pointing to teachings in Park and Shibata that would lead away from Petitioner’s proposed alterations of Park with the teachings of Shibata.

b) Shibata in view of Park

In its alternative formulation of the Shibata-Park combination, Petitioner relies upon Shibata for all except the separation of bottom side select gates as set forth in limitation [1.e]. Pet. 63–81. Petitioner points to Shibata’s Figure 16 for support (shown as annotated by Petitioner):

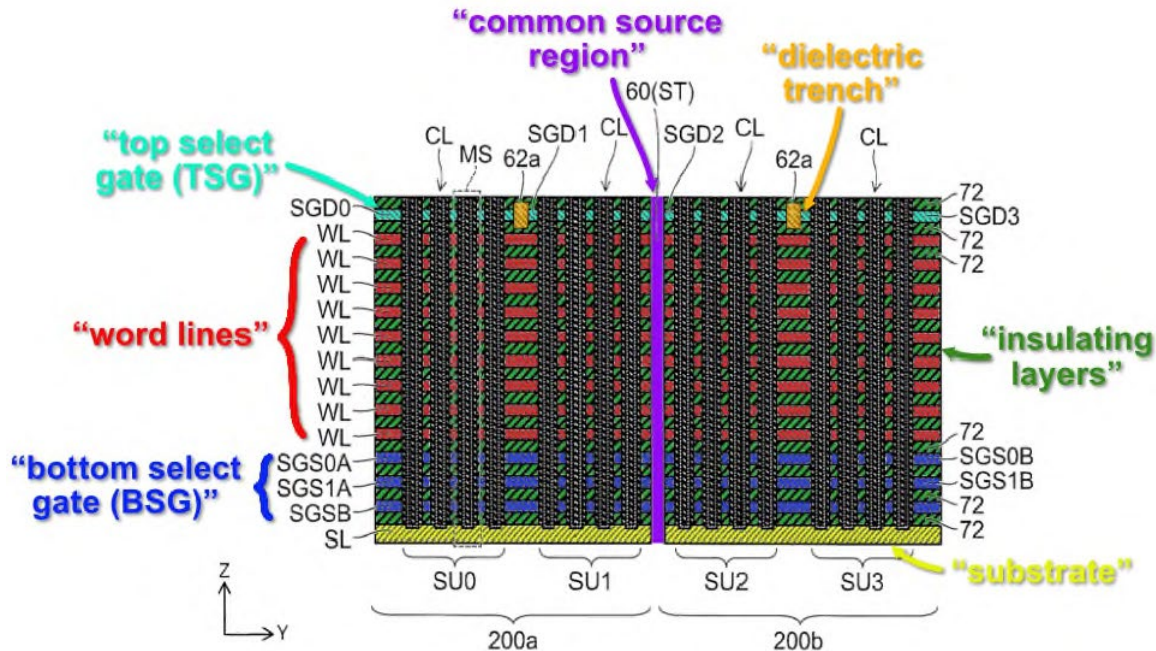


FIG. 16

Annotated Figure 16 shows a series of layers: bottom “substrate” layer SL, having an insulating layer 72 formed thereon, having three “bottom select gates (BSG)” SGSB, SGS1A, SGS0A formed thereon with insulating layers 72 therebetween, alternating “word lines” WL and insulating layers formed thereon, and “top select gate” SGD0 formed thereon with two “dielectric trenches” 62 forming a separation portion between different areas of the top select gate. *Id.* Petitioner asserts that it would have been obvious to use a single bottom select gate divided by dielectric trenches, in the same manner as the top select gate, instead of Shibata’s multiple bottom select gates, in view of Park’s teaching of a single divided bottom select gate, so as to reduce the height of the layers and the number of manufacturing steps and to reduce the load on the string unit drivers. *Id.* at 74–77 (citing Ex. 1003 ¶¶ 377–380, 385–393; Ex. 1004, Fig. 11, 5:67–6:12, 10:55–57).

Patent Owner first argues that such a combination with Park modifies the bottom select gate of Shibata to teach limitation [1.E], and renders

unclear how Petitioner’s reliance on Shibata’s unmodified bottom select gate for limitations [1.B], [1.C], [1.D], and [1.F]. Prelim. Resp. 54–55. We do not agree, because the combination only affects Shibata as to reducing the number of bottom select gates to one, which remains sufficient to teach the single recited bottom select gate in the disputed limitations of claim 1.

Patent Owner further argues that Petitioner’s motivation is conclusory and hindsight-based and, therefore, insufficient. *Id.* at 55–60. Patent Owner argues that the asserted benefits (reducing height and manufacturing steps) are unsupported by evidence beyond Dr. Lee’s statements. *Id.* at 56. We find this argument unavailing because Petitioner has cited multiple other sources for this statement of benefits. Pet. 76–77 (citing Ex. 1008 ¶¶ 2, 66 (“explaining that there is ‘continuous pressure to reduce component dimensions and fit more components in a given amount of chip area’ and that one of the ways to meet this goal is to ‘reduce an amount of memory cell string selection circuitry’”)); Ex. 1006, 355, 357; Ex. 1007, 2; Ex. 1012, 139. Moreover, Dr. Lee’s statements are further evaluated in view of their reasonableness based on the record; i.e., whether “[e]limination of . . . layers would remove some steps from the manufacturing process, reducing manufacturing time and cost” would be consistent with the record. Pet. 77 (citing Ex. 1003 ¶¶ 391–392).

Patent Owner further argues that Park’s layers 111 are inapposite because they are “H-cuts” that occur only in the staircase region; however, we find this argument unavailing for the same reasons as discussed for Petitioner’s asserted unpatentability over Park alone. Prelim. Resp. 56–58; *supra* §II(D)(2). Based upon our analysis for Park alone, and on our evaluation of Dr. Lee’s statements, we determine that Petitioner’s asserted reasons for combining Park’s teachings of a divided BSG with the relied-

upon teachings of Shibata are sufficient to meet Petitioner’s burden for institution.

Patent Owner further argues that Petitioner has not supported its assertion that it was “well known that trenches of dielectric material could be used to divide select gates.” Prelim. Resp. 59 (citing Pet. 78). Patent Owner argues that only Ex. 1019 shows isolating insulating regions in the BSG, but that those are inapposite because, like Park, they are H-cuts in the staircase region only. *Id.* (citing Ex. 1019 ¶¶ 154, 160–161). Patent Owner further argues that the remaining cited references show no more than Shibata; i.e., division of the top select gate. *Id.* (citing Ex. 1016, 6:5–15, 10:15–18, Fig. 4A (“uppermost gate electrode layer”); Ex. 1017, 7:40–42, Fig. 3 (“cutting insulation pattern 118” affecting “string selection gate electrodes 202”); Ex. 1018 ¶ 58, Fig. 4B (“upper electrodes ELb located at the highest level”)). However, Petitioner only asserted that it was well known “that trenches of dielectric material could be used to divide select gates” (Petition 78); as such, Petitioner’s evidence relating to the top select gates is sufficient to support that assertion. Nevertheless, we agree with Patent Owner that the cited references appear to show no more than that described by Shibata or Park, and that Petitioner does not show that it was well known in the art to separate a BSG as set forth in claim 1.

Further, Patent Owner has pointed to significant questions regarding Petitioner’s assertion that its combination would reduce the number of needed manufacturing steps, arguing that the combination would require “additional photolithography steps, etching steps, and filling procedures that neither Petitioner nor its expert considered.” Prelim. Resp. 59–60.

Based on the aforementioned aspects of current record, Patent Owner has called into question the merits of Petitioner's proposed advantages of combining Shibata and Park. This raises issues that are best resolved at trial.

III. CONCLUSION

For the reasons discussed above, we conclude Petitioner has shown a reasonable likelihood of prevailing with respect to at least one of claims 1–11. We determine that the record supports institution. Accordingly, we institute an *inter partes* review of all challenged claims under all grounds set forth in the Petition. 37 C.F.R. § 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”); *see SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (noting that the language of 35 U.S.C. § 314(b) “indicates a binary choice—either institute review or don’t”); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute as requiring “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

Our determination at this stage of the proceeding is based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which an *inter partes* review has been instituted. Our final decision will be based on the full record developed during trial.

IV. ORDER

For the foregoing reasons, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted for all asserted grounds on all asserted claims, i.e.:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–11	103(a)	Park
1–11	103(a)	Park, Shibata
1–11	103(a)	Shibata, Park

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

IPR2024-00794
Patent 10,950,623 B2

FOR PETITIONER:

K. Patrick Herman
Jeremy Jason Lang
Jared Bobrow
ORRICK, HERRINGTON & SUTCLIFFE LLP
pherman@orrick.com
jlang@orrick.com
jbobrow@orrick.com

FOR PATENT OWNER:

James L. Davis, Jr.
Christopher M. Bonny
Allen S. Cross
ROPES & GRAY LLP
James.L.Davis@ropesgray.com
Christopher.Bonny@ropesgray.com
Allen.Cross@ropesgray.com
YMTC-Micron-IPRs-Ropes-Service@ropesgray.com