

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00794

Patent 10,950,623

**PATENT OWNER'S RESPONSE
UNDER 37 C.F.R. § 42.120**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Cho et al., “A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single-Level Modes,” IEEE J. of Solid-State Circuits, Vol. 36, No. 11, November 2001.
Ex. 2002	Lee et al., “Applications of AFM in semiconductor R&D and manufacturing at 45 nm technology node and beyond,” Metrology, Inspection, and Process Control for Microlithography, Vol. 7272, SPIE, 2009.
Ex. 2003	Xiao et al., “A high speed low power negative sensing architecture for 3D NAND Flash memory,” 2016 China Semiconductor Technology International Conference (CSTIC), Shanghai, China, 2016.
Ex. 2004	Bergonzoni, et al., “Reset Current Scaling in Phase-Change Memory Cells: Modeling and Experiments,” IEEE Transactions on Electron Devices, Vol. 59, No. 2, 283-291, Feb. 2012.
Ex. 2005	Seshan et al., Handbook of Thin Film Deposition, Abstract, 2018.
Ex. 2006	Choi et al., “Novel ESD protection transistor including SiGe buried layer to reduce local temperature overheating,” IEEE Transactions on Electron Devices, Vol. 43, No. 3, 479-489, March 1996.
Ex. 2007	Declaration of Jonathan Bradford
Ex. 2008	Micron’s Preliminary Claim Constructions
Ex. 2009	Plaintiff’s Proposed Claim Constructions
Ex. 2010	January 17, 2025, Declaration of Dr. Kuhn (“KuhnII”)

LIST OF ABBREVIATIONS

Abbreviation	Term
'623	U.S. Patent No. 10,950,623 (Ex. 1001)
Challenged Claims	'623 patent, claims 1-11
Office	U.S. Patent and Trademark Office
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Park	U.S. Patent No. 9,299,718
Patent Owner or PO	Yangtze Memory Technologies Company, Ltd.
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,950,623 (IPR2024-00794, Paper 1)
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Shibata	U.S. Pub. 2019/0122734

I. INTRODUCTION

The references in Petitioner’s Grounds fail to disclose or render obvious the Challenged Claims of U.S. Patent No. 10,950,623 (“’623,” Ex. 1001). Petitioner sets forth three obviousness grounds: Park alone, Park in view of Shibata, and Shibata in view of Park. All three Grounds fail to render obvious, for example, various aspects of limitation [1.e], which is required by all Challenged Claims and recites “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.”

Regarding Ground 1 (Park alone), Park’s isolation insulating layers 111 are not the claimed “dielectric trenches formed in the BSG,” but instead are formed in a sacrificial layer. Additionally, because Park’s isolation insulating layers 111 are short features in the staircase region, Park fails to disclose that the insulating layers “extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” as required by limitation [1.e]. Instead, it is a separate feature—a common source line—that extends through the array region. Park also fails to disclose “dielectric trenches formed in the TSG,” as required by claim 2, because Park does not even have a TSG in the location where Petitioner proposes using a dielectric trench. Lastly, Park does not disclose dummy BSGs or dummy TSGs that are separated by dielectric trenches, as required by claim 10 and claim 11, respectively.

Regarding Ground 2 (Park in view of Shibata), Petitioner attempts to cure the deficiencies in Ground 1 by applying teachings of Shibata to Park, but Shibata's teachings do not cure Park's deficiencies, and regardless, a POSITA would not have been motivated to apply those teachings. First, as Petitioner admits, "Shibata only employs its separation portion to divide its **upper** drain-side select gate and not its 'BSG.'" Pet. 74. Second, Petitioner does not sufficiently explain why a POSITA would have been motivated to apply Shibata's teachings to Park, and Petitioner ignores significant reasons that a POSITA would not have made these modifications. Park teaches that long isolation insulating layers are undesirable because this may cause the incomplete removal of sacrificial layers and ultimately cause voids in the deposited conductive layers that form the word lines. In addition, Park teaches that having multiple isolation insulating layers side-by-side will prevent the flow of etching material in certain regions entirely. But Petitioner's proposed combination does exactly what Park teaches not to do. Petitioner's proposal would also reduce the number of common source lines in Park (replacing them with insulating layers), which would result in a suboptimal system with poorer speed, thermal management, reliability, accuracy, and device scalability. Finally, as to claims 10-11, Petitioner does not rely on Shibata for the claimed dummy BSGs or TSGs, and therefore these claims are not met for the same reasons discuss for Ground 1.

Regarding Ground 3 (Shibata in view of Park), Petitioner proposes that in light of Park’s purported teaching of isolation insulating layers in the alleged BSG, it would have been obvious to modify Shibata to use a single BSG and add insulating layers in the BSG, but there are once again significant gaps in Petitioner’s alleged motivations. Park’s teachings of isolation insulating regions would not have motivated a POSITA to replicate Shibata’s dissimilar teachings of separation portions in completely different locations. Petitioner and its expert rely on conclusory assertions and flawed analysis that ignore key differences between the references and fail to show how the purported benefits would be achieved.

As set forth herein, the Grounds presented in the Petition fail to make the required showing of obviousness.¹

II. THE ’623 PATENT

The claimed invention of the ’623 is directed to an improved “3D [three-dimensional] memory device with a divided block structure” that provides a novel approach to address issues—such as “longer erasing time, longer data transfer time, and lower storage efficiency”—associated with conventional architectural memory

¹ This Patent Owner Response is supported by the declaration of Dr. Kuhn. *See* Ex. 2010 (“KuhnII”), ¶¶1-40. All emphasis and color annotations have been added unless otherwise noted.

device designs containing a “shared BSG [bottom select gate]” architecture. ’623, 1:33-35, 1:57-60. KuhnII, ¶41.

3D NAND flash memory technology architecture has been developed such that “the vertical NAND memory cell strings of a same block” share a bottom select gate (BSG). ’623, 1:50-52. The shared BSG “controls all of the BSTs [bottom select transistors] or vertical NAND memory cell strings in [a] block simultaneously” during operation of the memory device. ’623, 1:53-57. However, as the number of vertical layers and bit density increases, “the shared BSG can induce longer erasing time, longer data transfer time, and lower storage efficiency.” ’623, 1:57-60. KuhnII, ¶42.

The claimed invention of the ’623 overcomes these device performance issues by introducing a novel 3D NAND memory device architecture that separates the memory cell blocks into a plurality of sub-blocks. ’623, 1:61-62. This architecture “divid[es] the shared BSG into a plurality of sub-BSGs,” so that each of the sub-blocks “can be operated individually through controlling the respective sub-BSG.” ’623, 1:61-67. Figure 1A, color-annotated below, shows a cross-sectional view of the ’623’s device with substrate 10:

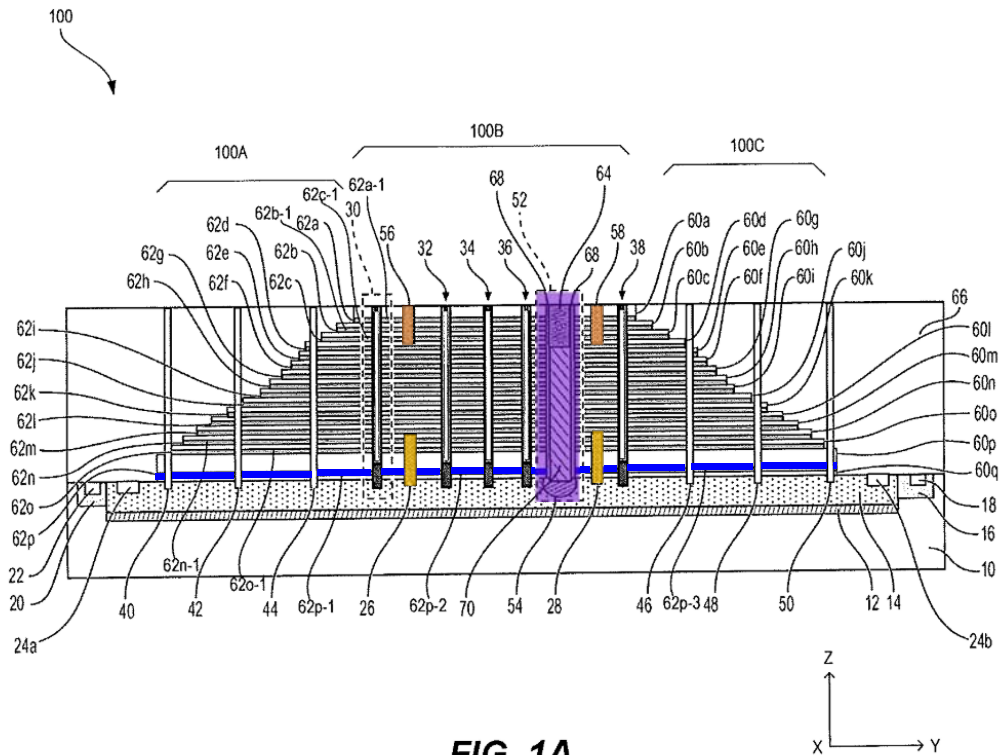


FIG. 1A

'623, Fig. 1A, 5:40-48. A **bottom select gate (BSG) 62p**, a “plurality of word lines (e.g., 62d-62m),” and a top select gate (TSG) 62a are “disposed sequentially over the substrate” ('623, 6:44-49). During this process, “a plurality of insulating layers” (insulating layers 60) are disposed between each of the layers that will form the BSG, word lines, and TSG. '623, 6:49-54. The **BSG**, word lines, and insulating layers 60 are “alternatively stacked over the substrate 10 with a staircase configuration.” '623, 6:55-61. KuhnII, ¶43.

After the BSG is formed, the '623 teaches that “by introducing the first [] trenches into the memory device 100, the BSG [is] separated into a plurality of sub-BSGs.” '623, 7:45-47. Specifically, “one or more first dielectric trenches (or first trenches), such as two **first trenches 26 and 28**, are formed in the one or more BSGs

(e.g., 62p),” with the “**first trenches 26 and 28** extend[ing] in an X-direction (i.e., length direction) of the substrate 10 to separate the **BSG 62p**” into “a plurality of sub-BSGs.” ’623, 7:17-24. KuhnII, ¶44.

Forming the first trenches in the BSG rather than a sacrificial layer introduces significant advantages. **First**, when the trenches are formed in a sacrificial layer, forming trenches that are close to each other risks jeopardizing the gate replacement process. **Second**, by forming the trenches in the existing BSG, it is possible to divide the BSG into sub-BSGs using trenches that extend the length of the array. **Third**, forming the trenches in the existing BSG removes the need to use a gate replacement process. All these advantages help improve structural integrity. ’623, 1:57-2:7, 22:63-23:33. KuhnII, ¶¶45-47.

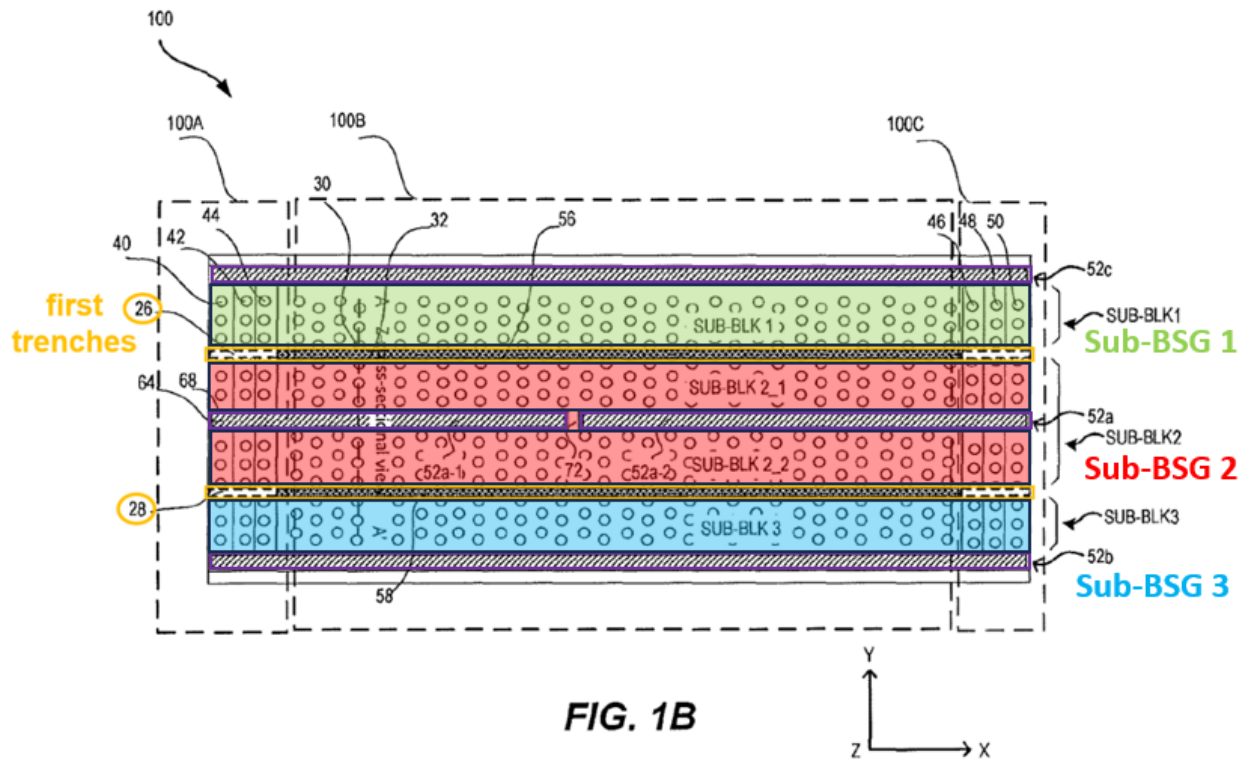
As depicted in Figure 1A, the dielectric trenches also extend in a Z-direction, traversing multiple conductive and insulation layers. After the TSG is formed, corresponding **second trenches 56 and 58** are “formed in the one or more TSGs (e.g., 62a).” ’623, 7:26-29. The dielectric trenches are filled with “suitable dielectric materials.” ’623, 7:42. Dividing the TSG in this manner (by forming a trench(es) in the TSG) offers many of the same advantages as for a BSG discussed above. ’623, 1:57-2:7, 22:63-23:33. KuhnII, ¶48.

The sub-BSGs “divide the memory device 100 into a plurality of sub-blocks,” or, in other words, “a plurality of cell strings,” and “each of the sub-blocks can be

operated individually through controlling the respective sub-BSG.” ’623, 7:47-53. As such, the ’623’s memory device “can precisely control a desired sub-block/array region so as to effectively reduce a programming time, a reading time, an erasing time and data transfer time, and significantly improve data storage efficiency.” ’623, 7:53-58. Accordingly, the claimed memory device architecture of the ’623 overcomes shortcomings of the prior art. KuhnII, ¶49.

The ’623 further teaches that the memory device includes “one or more common source regions (CSRs), such as one **common source region 52**,” which is “formed over the substrate” and “extend[s] in the X-direction (length direction) of the substrate.” ’623, 7:59-62. The CSR “passes through the BSG 62p,” “the plurality of word lines 62d-62m,” as well as “the plurality of insulating layers 60,” among other layers. ’623, 7:62-66. Moreover, the CSR “is electrically coupled with the substrate 10 via a doped region 54.” ’623, 7:66-67. KuhnII, ¶50.

The ’623 distinguishes the **first trenches** and **second trenches**, which divide the BSG and TSG into sub-BSGs and sub-TSGs, from the **common source region**, which does not divide the BSG or TSG into sub blocks. Figure 1B, color-annotated below, shows the same memory device of the ’623 from a top-down view:



'623, Fig. 1B (annotated), 4:35-37. As illustrated in Figure 1B, three **common source regions, 52a-52c**, “extend along the X-direction (length direction) of the substrate 10.” '623, 8:67-9:2; *see also* '623, Figs. 11B-C. The “**common source region 52a** is separated” “by an H-cut 72 into two sub-CSRs 52a-1 and 52a-2” such that “two portions **SUB-BLK2_1 and SUB-BLK_2** ... are electrically connected with each other through the H-Cut 72.”² '623, Fig. 1B, 9:14-18, 9:41-44. Also

² The term “H-cut” refers to the “H” shape formed by the process. As illustrated in '623 Figure 1B, the H-cut 72 forms the cross portion of the “H,” which is rotated 90 degrees.

illustrated in Figure 1B above, are two pairs of trenches: **first trenches 26 and 28** in the BSG, which extend the length of the bottom select gate, and **second trenches 56 and 58** which extend the length of the top select gate (for clarity, the second trenches 56 and 58 are not color annotated because they overlay on top of the first trenches, but in a higher layer). As discussed and shown in the figure, **first trenches 26 and 28** “separate the BSG 62p ... into a plurality of sub-BSGs.” ’623, 7:17-26. The **common source regions**, in contrast, do not. The ’623 explains that “[w]ithout the introduction of the **first/second trenches**, the memory device 100 (or the memory cell block 100) has a shared BSG.” ’623, 9:46-49. KuhnII, ¶51.

Claim 1, the only independent claim of the ’623, is directed to aspects of the above-described invention:

[1.pre] A memory device, comprising:

[1.a] a substrate;

[1.b] a bottom select gate (BSG) disposed over the substrate;

[1.c] a plurality of word lines positioned over the BSG with a staircase configuration;

[1.d] a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;

[1.e] one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and

[1.f] one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the

one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.

III. FILE HISTORY

The claims of the '623 were allowed after consideration of numerous prior art references. Over the course of prosecution, over twenty references were considered by the Examiner before concluding that the “prior art of record and considered pertinent to the applicant’s disclosures ... does not teach or fairly disclose[]” the claimed invention. *See, e.g.*, Ex. 1002 (Part 2), 127-131, 139, 141, 144, 204. The '623 issued on March 16, 2021. KuhnII, ¶¶53-54.

IV. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this proceeding only, Patent Owner does not object to the definition of a person of ordinary skill in the art (“POSITA”) proffered by Petitioner and adopted by the Board at institution. Pet. 19. The Challenged Claims are valid regardless of the precise definition used for a POSITA. KuhnII, ¶¶55-59.

V. CLAIM CONSTRUCTION

Other than the terms identified below, Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of the *inter partes* review. Patent Owner, however, reserves the right to modify or elaborate on its proposed constructions and to raise further claim construction issues in the parallel district court proceedings. KuhnII, ¶60.

The parties exchanged proposed claim constructions in the parallel district court proceeding. Exs. 2008-2009. The claim construction disputes in district court do not impact the issues raised in this Response.

A. “dielectric trenches formed in the BSG” (Claim 1)

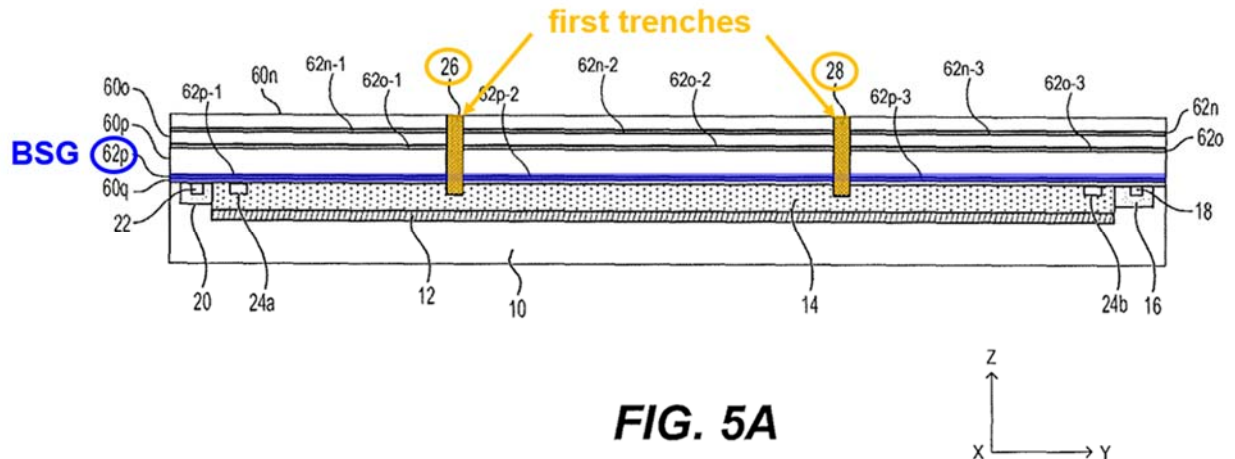
The term “dielectric trenches formed in the BSG” by its plain meaning does not encompass dielectric trenches that are formed in another structure instead of a BSG, such as a sacrificial layer.³ This interpretation is supported by the plain language of the claims, as well as the specification. By presenting prior art that forms a structure in a sacrificial layer and mapping it to the “formed in the BSG” limitation (Pet. 33-34), Petitioner is relying on an implicit claim construction that departs from the express language of the claims, and which is not supported by the intrinsic record. KuhnII, ¶61.

First, the claim language recites that the “one or more first dielectric trenches **formed in the BSG**” (bottom select gate) rather than formed in some other type of structure, such as a sacrificial layer. Petitioner’s interpretation effectively reads the term “BSG” out of the claims. KuhnII, ¶62. The claim also recites that the

³ The Board does not need to reach whether the claim encompasses features that are formed only partially in a BSG because the alleged dielectric trenches in the prior art are formed entirely in a structure other than a BSG. *See* §VII.A.1.

trenches are “formed in” the BSG and not merely “in” the BSG, which Petitioner ignores. Moreover, the surrounding claim language confirms that the claim does not encompass dielectric trenches that are formed in another structure other than BSG. The claim requires that the dielectric trenches are “formed in the BSG and extending in a length direction of the substrate **to separate the BSG into a plurality of sub-BSGs,**” which means that there must be an existing BSG such that forming the dielectric trench separates the BSG into a plurality of sub-BSGs. KuhnII, ¶62.

Second, the specification supports the plain meaning of the claim term as not encompassing dielectric trenches that are formed in another structure instead of a BSG. The ’623 details the gate-first manufacturing flow (“process 1200”) in Fig. 12, which lists, among others, “step 1204 where one or more **BSGs** and one or more dummy BSGs are formed sequentially over a substrate,” and “step 1206 [where] one or more **first trenches** are formed in the **BSGs** and dummy BSGs.” ’623, 21:34-38, 45-46. The state of ’623’s device after these steps is depicted in Fig. 5A.



'623, Fig. 5A (annotated). As can be seen the figure, the trenches are formed in a BSG. KuhnII, ¶63. The specification, like the claims, also describes the trenches as separating the BSG into a plurality of sub-BSGs, which again confirms that there must be an existing BSG. For example, the '623 discloses “one or more first dielectric trenches (or first trenches), such as two first trenches 26 and 28, are formed in the one or more BSGs (e.g., 62p),” which “extend[] in an X-direction (i.e., length direction) of the substrate 10 to separate the BSG 62p and the dummy BSGs 62n-62o layers into a plurality of sub-BSGs and sub-dummy BSGs, or to say, a plurality of cell strings.” '623, 7:17-26. KuhnII, ¶63.

Petitioner's reliance on the specification is misplaced and is focused entirely on an unclaimed variation. Petitioner cites the '623 section which explains that in the gate-last manufacturing flow the first trenches would be formed in sacrificial layers. Pet. 34. In the cited section, referring to Figure 5A reproduced above, the '623 states that the layer labeled “62p” can be a sacrificial layer. '623, 15:45-48

(“The BSG 62p and the two dummy BSGs 62n-62o can be sacrificial layers that are made of SiN. The sacrificial layers can be removed and replaced with a high K layer and a metal layer in future manufacturing steps.”). However, this passage is not saying that a sacrificial layer is a BSG. Rather, it is saying that feature 62p shown in Figure 5, at this stage in the process, can be a sacrificial layer instead of a BSG. Indeed, a POSITA would have understood that a sacrificial layer made of SiN (an insulating material) is not a gate layer (i.e., is not a BSG). KuhnII, ¶64. As an insulator, it has none of the properties (e.g., conductivity) that would allow it to be used as a BSG, and as a sacrificial layer, it is not even present in the final device. KuhnII, ¶64. Thus, although the specification discloses a variation that uses a gate-last manufacturing process with a sacrificial layer, this variation is not claimed, and the claims are instead directed to the primary embodiment which describes structures associated with a gate-first process. KuhnII, ¶64.

Accordingly, the term “dielectric trenches formed in the BSG” does not encompass dielectric trenches that are formed in a structure other than a BSG, such as a sacrificial layer. KuhnII, ¶65.

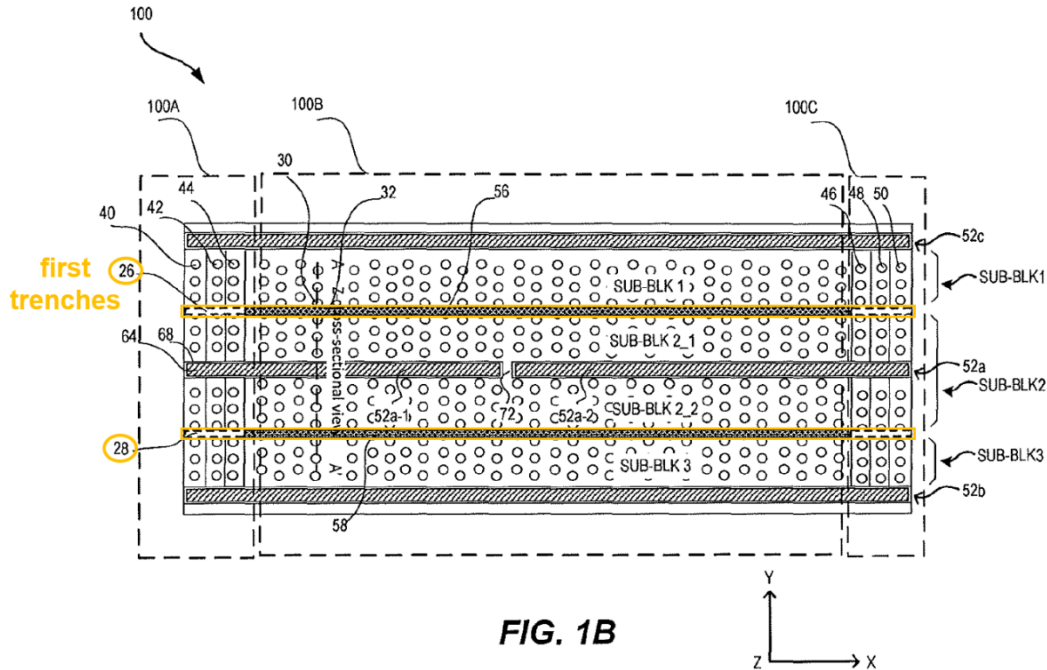
B. “one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” (Claim 1)

The claim limitation “one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs”

should be construed consistent with its plain meaning to require that the length of the dielectric trench is what separates the BSG into sub-BSGs. This construction is supported by the intrinsic record. KuhnII, ¶66.

First, the claims expressly recite that it is the length of the dielectric trenches that separates the BSG. The claims recite that the dielectric trenches are “**extending in a length direction** of the substrate **to separate the BSG** into a plurality of sub-BSGs”—that is, the claimed geometry of the dielectric trench “separate[s] the BSG into a plurality of sub-BSGs.” KuhnII, ¶67.

Consistent with the claims, the '623 specification also supports Patent Owner's construction because it consistently shows dielectric trenches that extend the length of the substrate in the active region to separate the BSG into a plurality of sub-BSGs. The '623 discloses “one or more first dielectric trenches (or first trenches), such as two first trenches 26 and 28, are formed in the one or more BSGs (e.g., 62p),” which “extend[] in an X-direction (i.e., length direction) of the substrate 10 to separate the BSG 62p and the dummy BSGs 62n-62o layers into a plurality of sub-BSGs and sub-dummy BSGs, or to say, a plurality of cell strings.” '623, 7:17-26. As shown in Figure 1B, below, the **dielectric trenches** (annotated in orange) extend from one staircase region to another (from 100A to 100C) and pass through the active region (central core region 100B), thereby forming a continuous structure that separates the BSG into sub-BSGs:

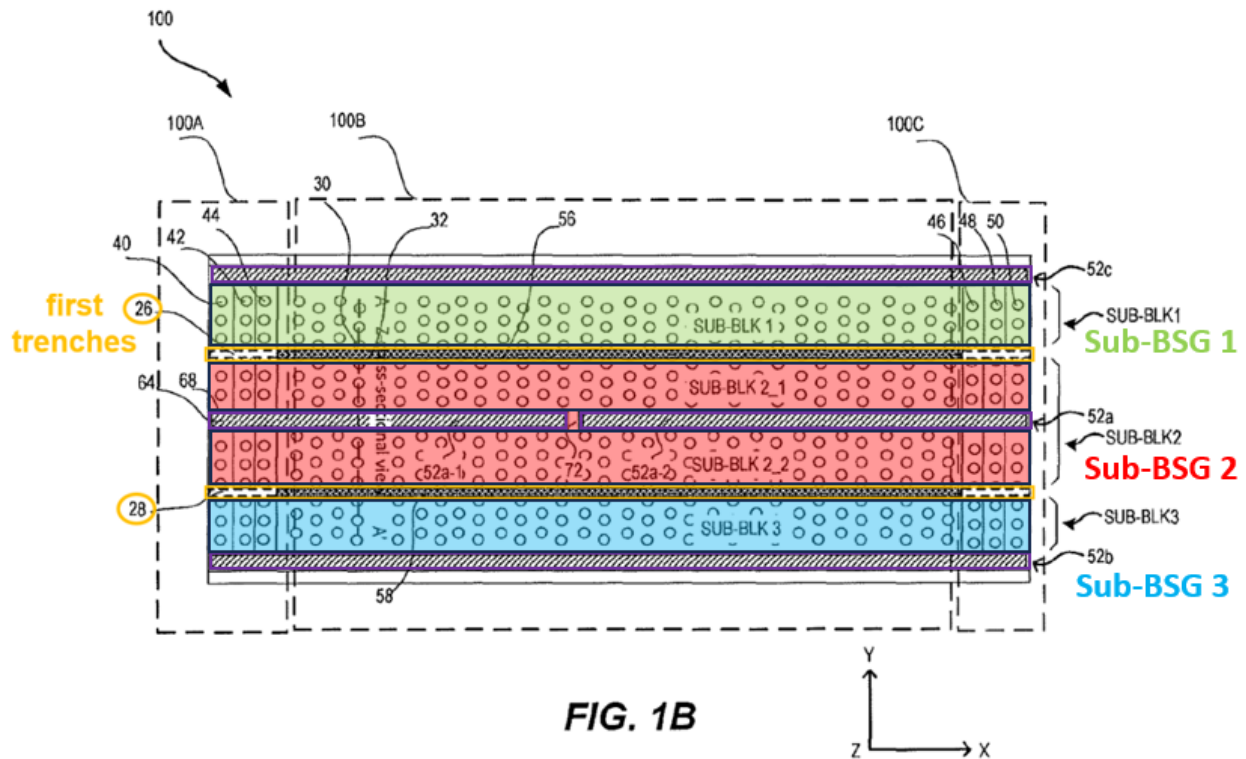


The '623 further explains that “[w]ithout the introduction of the first/second trenches, the memory device 100 (or the memory cell block 100) has a shared BSG.” ’623, 9:46-49. Thus, as described and a shown, the length of the dielectric trenches divides the BSG into sub-BSGs, and is the sole reason that the memory device has “sub-BSGs” as claimed. KuhnII, ¶168.

Patent Owner respectfully submits that the Board’s preliminary analysis in the Decision to Institute (“DI”) does not properly account for the intrinsic record. The Board “construe[d] the phrase ‘the dielectric trenches . . . separate the BSG into a plurality of sub-BSGs’ as requiring that the trenches separate the BSG into sub-BSGs, but that other components are not excluded from cooperating in the separation of the BSG into sub-BSGs.” DI 15. But because the construction addressed only the truncated phrase “the dielectric trenches . . . separate the BSG into a plurality of

sub-BSGs” (*id.*), it does not appear to take into account the requirement recited in the claims, and discussed above, that the extension of the dielectric trenches in the length direction is what separates the BSG into sub-BSGs: “**extending in a length direction** of the substrate **to separate the BSG** into a plurality of sub-BSGs.” KuhnII, ¶69.

Moreover, the Board’s conclusion that other components are not excluded from the separation of the BSG into sub-BSGs (DI 16) is not supported by the intrinsic record. First, the ’623 does not disclose that other components may separate the BSG into sub-BSGs. The Board cited common source regions 52 (DI 14 (citing (’623, Fig. 1B, 9:3-8)), but **common source regions 52 do not separate the BSG into sub-BSGs**. As shown in Figure 1, **common source regions 52a** is merely in the middle of a single **sub-BSG 2** (“SUB-BLK2”) and does not divide it into further sub-BSGs because there is an H-cut 72 that connects the two sides of the common source region such that both regions are part of the same sub-BSG. 9:15-19, 9:41-44 (“two portions SUB-BLK2_1 and SUB_BLK_2 ... are electrically connected with each other through the H-Cut 72”).



And while **common source regions 52b and 52c** are at the edge of sub-BSG and do help define the boundary, they too **do not separate the BSG into sub-BSGs**. The BSG is not present on the other side of common source regions 52b and 52c. All of this is further confirmed by the '623's express statement that "[w]ithout the introduction of the first/second trenches, the memory device 100 (or the memory cell block 100) has a shared BSG." '623, 9:46-49. KuhnII, ¶70.

Even if the common source regions divided the BSG into sub-BSGs (they do not), they are never shown working in tandem with the dielectric trench that extends in the length direction to separate the BSG into a plurality of sub-BSGs. Having

other structures act in cooperation for the *same boundary* would mean that the dielectric trench itself no longer “extend[s] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” as required by the claims. KuhnII, ¶71.

Thus, the claim limitation “one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” should be construed to require that the length of the dielectric trench is what separates the BSG into sub-BSGs. KuhnII, ¶72.

C. “one or more second dielectric trenches ... extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs” (Claim 1)

For the same reasons discussed in §V.B, the claim limitation “one or more second dielectric trenches ... extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs” should be construed to require that the length of the dielectric trench is what separates the TSG into sub-TSGs. KuhnII, ¶73.

VI. THE PRIOR ART REFERENCES RELIED UPON⁴

A. U.S. Patent 10,559,583 (“Park,” Ex. 1004)

Petitioner relies upon Park for all of the limitations of the independent Challenged Claims. Pet. 25-38. Park is directed to “a memory device having a three-dimensional array of memory cells” using “a vertical transistor structure in lieu of a conventional planar transistor structure.” Park, 1:15-27. The architecture of Park, however, is distinct from that of the ’623 for at least the reason that Park does not use dielectric trenches that extend along the memory array to separate the memory array into blocks, but instead uses a short isolation insulating region in the staircase region to divide the common source line. KuhnII, ¶74.

Park’s memory device includes a “cell region CR” containing “a plurality of gate electrodes layers sequentially stacked on a substrate” in “a Z-axis direction,” which “may provide a string select line, word lines, and a ground select line.” Park, 2:14-17, 5:18-25. As illustrated in Figure 4 below, the cell region includes a “plurality of pad regions constituting a stepped structure” (*i.e.*, a staircase region), wherein the “cell contacts CNT” may be connected to the word lines:

⁴ For the purposes of the present IPR proceeding only, Patent Owner does not contest that the Park and Shibata references qualify as prior art to the ’623.

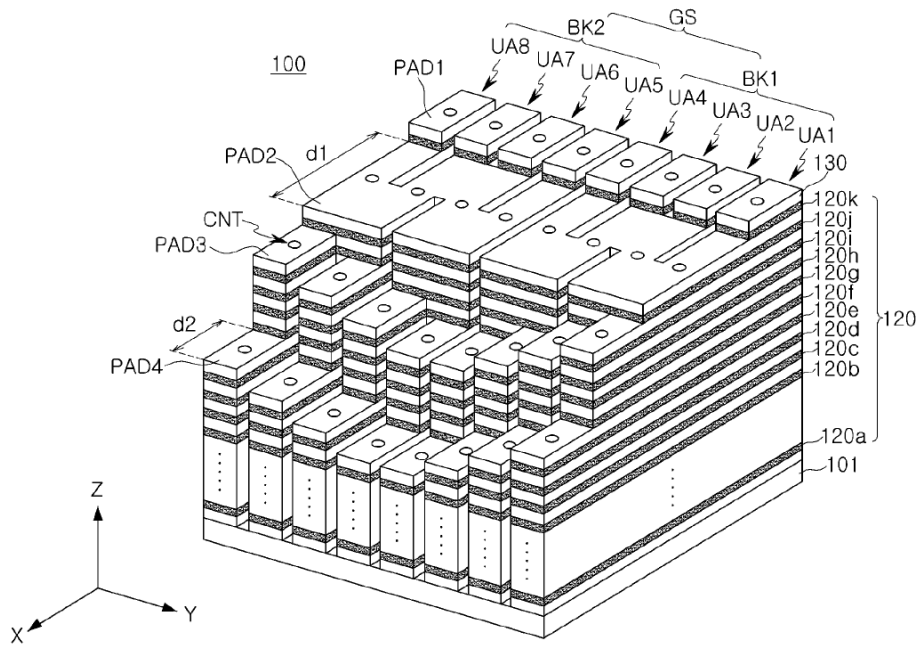


FIG. 4

KuhnII, ¶75.

Independent control of unit areas (*e.g.*, UA1 to UA8) is provided by the string select line and the ground select line, which “may be separated from each other at the boundaries between the first to eighth unit areas UA1 to UA8” “by the **first common source lines 102** and **first lines 103** of the **second common source lines 105**” as shown in Figure 3 below:

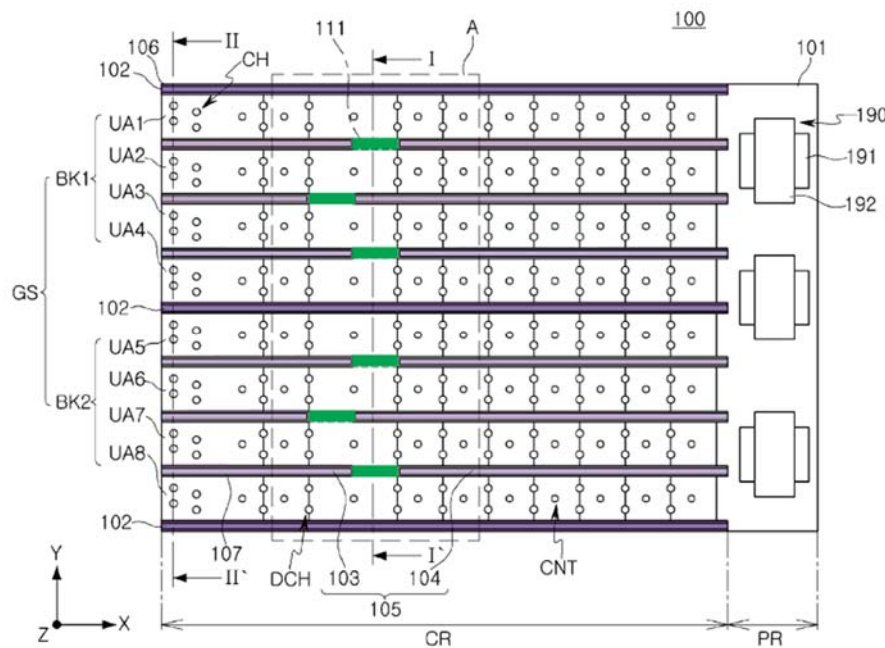


FIG. 3

Park, Fig. 3, Park, 6:4-8. KuhnII, ¶76.

Park also uses **isolation insulating layers 111** “disposed between the **first and second lines 103 and 104** of the **second common source lines 105**” in the staircase region. Park, 6:8-12, 10:60-65. Instead of using a dielectric trench that extends along the length of the substrate to divide a bottom select gate (BSG), Park’s memory device architecture entails **common source lines** to divide the ground select line (*i.e.*, the purported BSG), and short **isolation insulating layers** to segment a subset of the **common source lines** within the staircase region. While these **isolation insulating layers** are dissimilar to the ’623’s long dielectric trenches that separate the BSG into sub-BSGs, they are very similar to the ’623’s disclosure of using “H-cuts,” which instead are used to separate the ’623’s “common source

region 52 ... into two or more sub-CSRs.” *Compare* Park, Fig. 3 with ’623, Fig. 1B, 13:19-20 (“The common source region 52 is separated by the H-Cut 72 into two sub common source regions.”). KuhnII, ¶77.

A cross-sectional view of Park’s memory device “taken along line I-I’ of FIG. 3” is depicted in Figure 11 below, where “only the second lines 104 of a portion of the **second common source lines 105** are illustrated.”⁵ Park, 10:52-54. There, the gate electrode layers 120 are “divided into the first and second blocks BK1 and BK2 by the **first common source lines 102**.” Park, 10:46-49. BK1 and BK2 are further “divided into the first and eight unit areas UA1 and UA8 by the **second common source lines 105**.” Park, 10:49-54. **Gate electrode layer 120a** “form[s] the ground select line.” Park, 10:55-56. While this cross-section within the staircase region shows **isolation insulating layer 111** between sections of the **gate electrode layer 120a**, that is due to the location of this particular cross-section, and it is actually primarily the **second common source lines 105** that separates the **gate electrode layer 120a**, as discussed and shown above in Fig. 3.

⁵ Note the coordinate system for Figure 11 is different than that of Figure 3. In Figure 3, the axis along the line I-I’ is the y-axis; whereas in Figure 11, the axis along the line I-I’ is the x-axis. The z-axis remains the same in both figures.

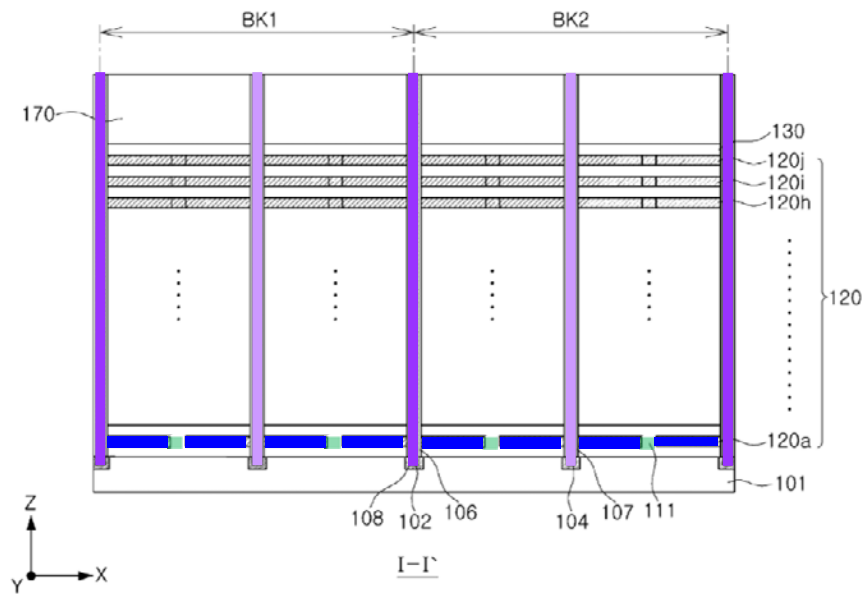
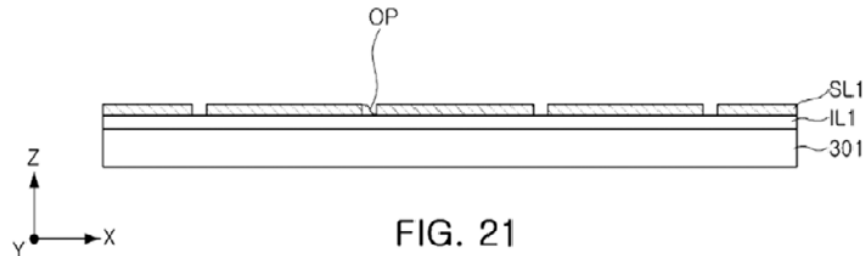


FIG. 11

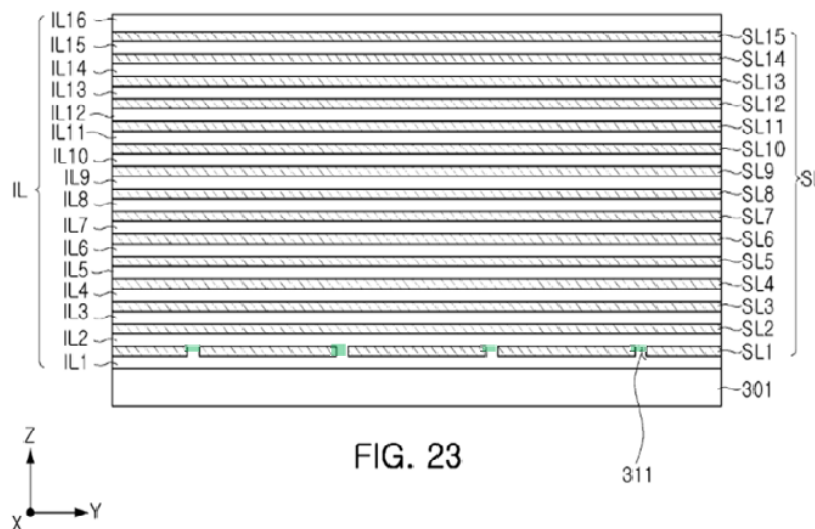
Park, Fig. 11 (annotated). KuhnII, ¶78.

Importantly, Park cautions against using long isolation regions (e.g., to separate a gate electrode layer) because isolation regions can prevent the “proper[] secur[ing]” of the “inflow passage” through which the etching material (for removing sacrificial layers) and conductive material (for forming the gate layers) is introduced. Park, 15:53-59, 16:38-59. This is because the isolation regions separate the word line cuts (that eventually form the second common source lines) thereby “forming a relatively long path above the isolation regions 311” for the flow of etching and conductive materials. Park, 15:53-59. Moreover, when isolation regions are adjacent to one another, Park recognizes that there may be no inflow path to certain areas, and thus disposes the isolation regions “in zigzag form.” Park, 15:60-16:2. KuhnII, ¶79.

Park's **isolation regions 311** are formed in a sacrificial layer, rather than in a gate electrode. Park teaches forming the insulating layer 111 (or 311 in Figures 18-36 illustrating the “memory device during the course of its manufacture”). Park teaches that the process of forming the opening regions includes “a first insulating layer IL1 and a first sacrificial layer SL1,” which are formed on a first substrate 301.” Park, 12:56-59. Figure 21 depicts the first sacrificial layer SL1 with an opening region (“OP”) in which the **isolation regions 311** are formed. Park, 12:65-13:1.



Park, Fig. 21. The OP regions are then “filled with an insulating material,” as depicted in Figure 23, to form **isolation regions 311**, which correspond to the **isolation insulating layers 111** of Figure 16:



Park, Fig. 23 (annotated), 13:15-17. Park teaches that the sacrificial layer is then etched away (*i.e.*, removed) “by an etching solution flowing through the first and second word line cuts WC1 and WC2,” depicted in Figure 29:

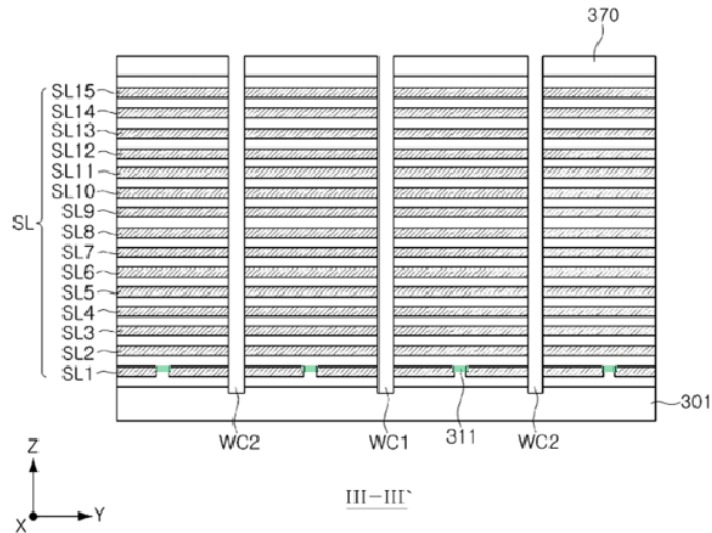


FIG. 29

Park, Fig. 29. After this etching process, “horizontal voids hv are formed,” which are depicted in Figure 31:

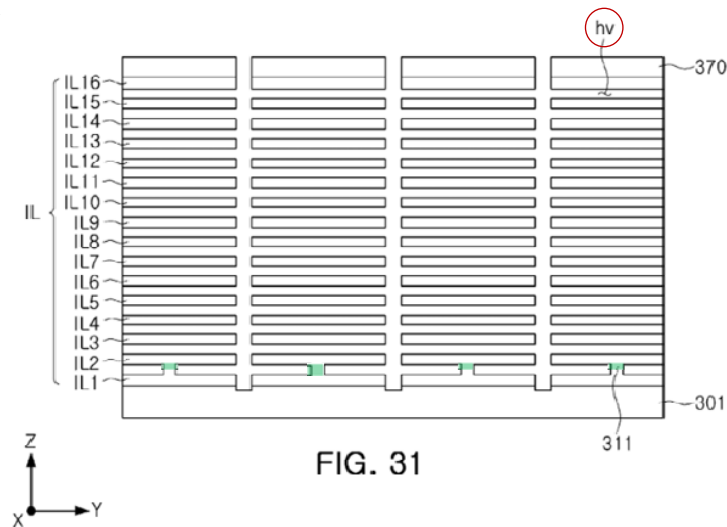
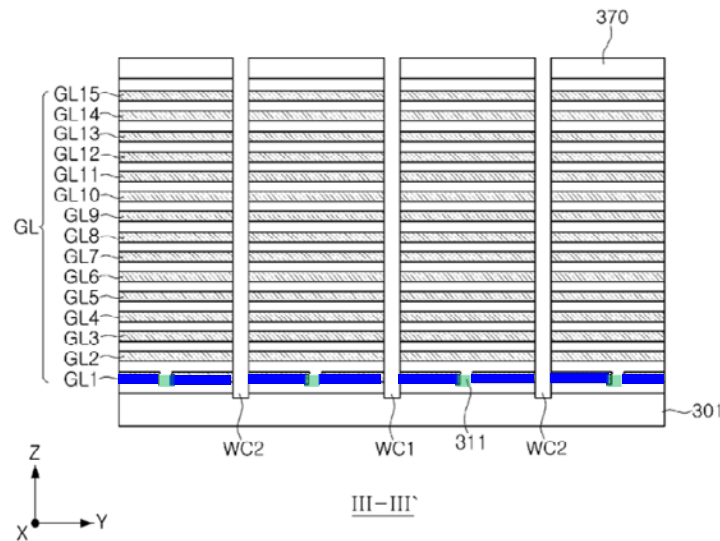


FIG. 31

Park, Fig. 31, 15:39-40. While the sacrificial layer has been etched away, the **isolation regions 311** remain. Park, 16:7-9. The voids are then filled with conductive material, which flows from the first and second word line cuts WC1 and WC2, to form the gate electrode layers. Park, 16:3-7. Figure 34 of Park depicts the first gate electrode layer GL1, which forms the **ground select line**:



Park, Fig. 34 (annotated). KuhnII, ¶80.

B. U.S. Pub. 2019/0122734 (“Shibata,” Ex. 1005)

Petitioner relies upon combinations of Shibata and Park (Shibata in view of Park and Park in view of Shibata) for Grounds 2 and 3. Pet. 57-94. Shibata is directed to aspects of three-dimensional memory devices that have a “vertical transistor structure.” Shibata, [0067]. KuhnII, ¶81.

Petitioner generally relies on Shibata’s second embodiment as illustrated in Figure 16:

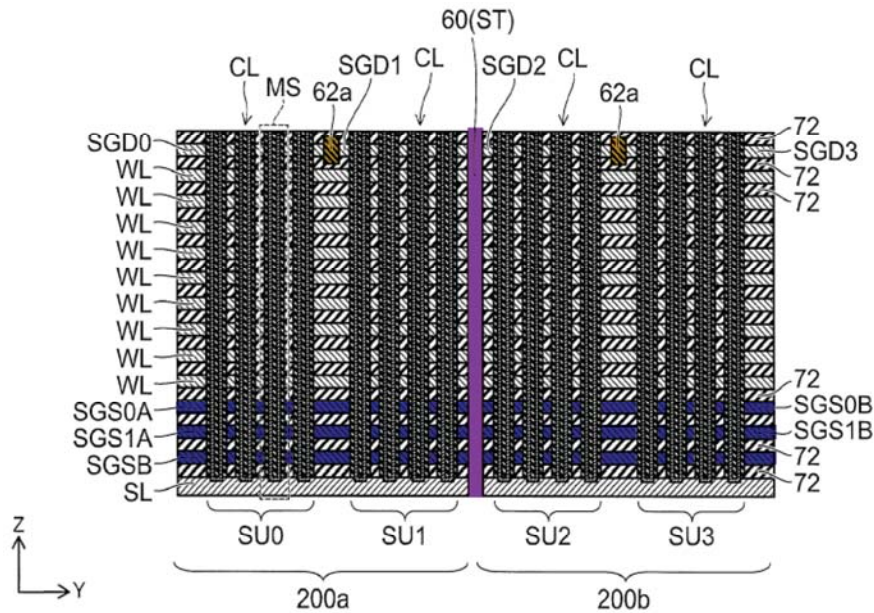


FIG. 16

Shibata, Fig. 16 (annotated). Shibata’s Figure 16 depicts a second embodiment with “two sub-blocks 200a and 200b subdivided by three **separation portions 60** (slits ST) separated from each other in the Y-direction.” Shibata, [0162]. Figure 16 additionally illustrates **separation portion 62a** of sub-block 200a and **separation portion 62a** of sub-block 200b. In this embodiment, there is a single-layer drain-side select gate SGD0 and a **three-layer source-side select gate** and layers of word lines stacked between. Shibata, [0166]. Notably, Shibata’s **separation portions 62a** do not divide the **source-side select gate**. Instead, the **source-side select gates** are divided in the Y-direction by the separation portions 60 (the slits ST) into “SGS0A,” “SGS0B,” “SGS1A,” and “SGS1B.” Shibata, [0178]. KuhnII, ¶82.

Petitioner also relies on Figure 47A, which is a plan (top-down) view of the drain-side select gate layer divided into “SGD0,” “SGD1,” “SGD2,” and “SGD3”:

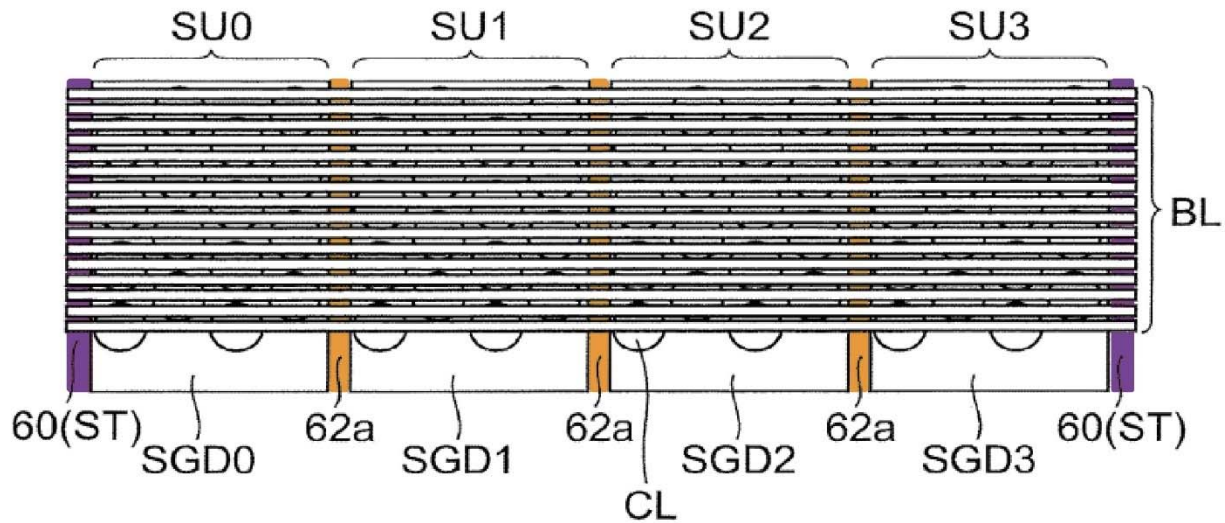


FIG. 47A

Shibata, Fig. 47A (annotated), [0444], [0446], [0047].⁶ As illustrated in Figure 47A, the **separation portions 62a** extend through the array region of the memory. KuhnII, ¶83.

Shibata's separation portions are formed in a sacrificial layer rather than in the conductive material that forms the select gate layers, and Shibata teaches adding

⁶ Note that as illustrated in Figure 47A, Shibata's first embodiment has a different configuration than that of Figure 16. For example, there are three **separation portions 62a** facing back-to-back instead of alternating with **separation portions 60**. In addition, the drain-side select gate SGD1 of Figure 47A is between two **separation portion 62a** instead of next to one of the **separation portions 60** (slits ST). KuhnII, 83.

the separation portions to only the drain-side gate select lines (near the top of the device) and does not teach adding separation portions to the source-side select lines (near the bottom of the device). KuhnII, ¶84. This is described in Shibata in connection with the first embodiment. Shibata, [0103].⁷ In total, Shibata teaches three separation portions—62a, 62b, and 62c—are situated at distinct locations along the Y-direction, as depicted in Figure 13, and which “divide drain-side select gate layers of different layers.” Shibata, [0155]. The sacrificial layers 71 are then removed through an etching process and replaced with conductive layers 60 to form the source gate drains and word lines. Shibata, [0155]. The separation portions segment the drain-side select gate layers into six—“SGD0A,” “SGD1A,” “SGD2A,” “SGD0B,” “SGD1B,” and “SGD2B”—each of which are “each controlled electrically independently.” Shibata, [0126]-[0129].

⁷ Figures 8A through 11B show a method for manufacturing the semiconductor memory device of the first embodiment (Shibata, [0011]), but this embodiment differs from that illustrated in Figure 47 in that it has a three-layer drain-side select gate with three separation portions 62a, 62b, and 62c positioned at of these layers. While the configuration is different than that of the second embodiment, the method of manufacture is informative. KuhnII, ¶84.

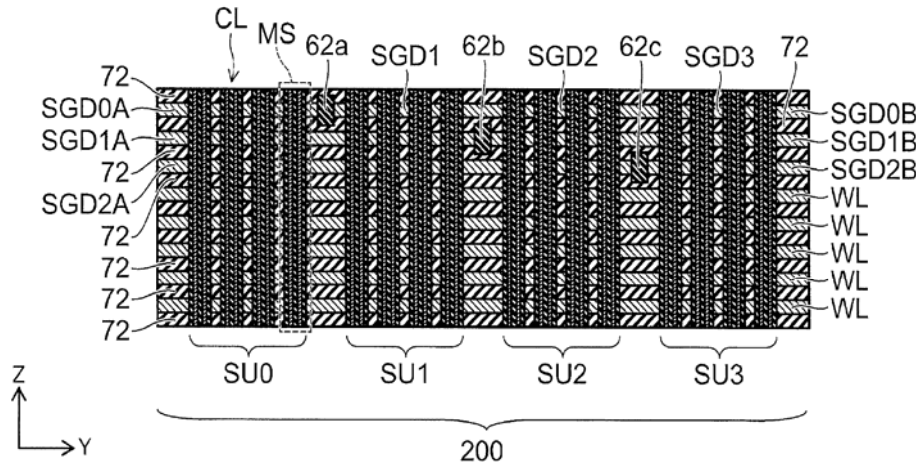


FIG. 13

Shibata, Fig. 13. KuhnII, ¶85.

VII. GROUND 1: PARK DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-11

Park fails to disclose or render obvious the Challenged Claims at least because Park fails to disclose or render obvious multiple elements of claim 1—the sole independent claim. For example, Park’s isolation insulating layers are not “dielectric trenches formed in the BSG” and do not “extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” Park also does not disclose or render obvious “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs” as required by claim 2, and similar deficiencies apply to claim 3 as well. Finally, for claims 10 and 11, Park does not disclose or render obvious insulating layer to separate “dummy BSGs” and “dummy TSGs” into “dummy sub-BSGs” and “dummy sub-TSGs,” respectively. KuhnII, ¶86.

A. Independent Claim 1: Park Does Not Disclose or Render Obvious Multiple Requirements of Limitation [1.e]

Petitioner fails to show that Park discloses or renders obvious at least two requirements of limitation [1.e]: “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” Park’s isolation structures (alleged dielectric trenches) are formed in a sacrificial layer rather than a BSG, and the short isolation structures do not separate the BSG into a plurality of sub-BSG’s. KuhnII, ¶87.

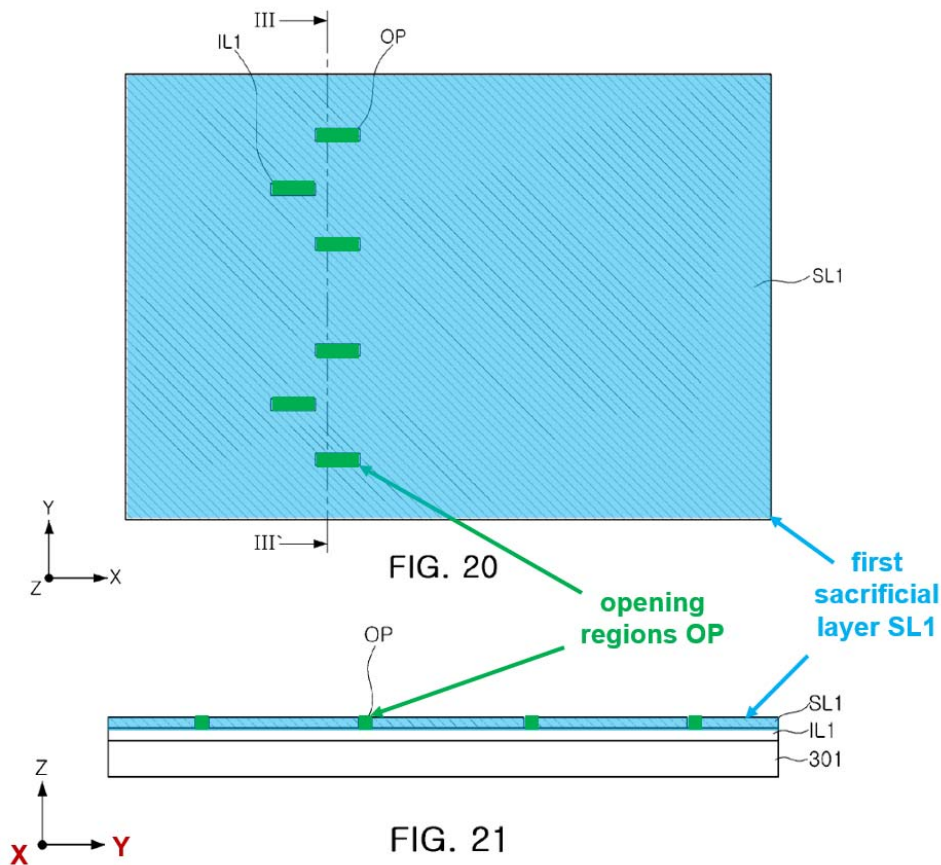
1. Park’s Isolation Insulating Layers Are Not “Dielectric Trenches Formed in the BSG” (Limitation [1.e])

Petitioner fails to show that Park’s alleged dielectric trench (isolation insulating layers) are formed in the purported bottom select gate (BSG) (ground select line (GSL)) because Park’s isolation insulating layers are formed in an entirely different structure—a sacrificial layer. KuhnII, ¶88.

Claim 1 requires “**one or more first dielectric trenches formed in the BSG** and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” As discussed in §V.A, the term “dielectric trenches formed in the BSG” does not encompass dielectric trenches that are formed in another structure other than a BSG, such as a sacrificial layer. KuhnII, ¶89.

Petitioner maps Park’s “isolation insulating layer” to the claimed dielectric trenches (Pet. 30-34), but Park’s isolation insulating layer are formed in a sacrificial

layer rather than a BSG. Specifically, as shown below, Park’s **isolation insulating layers** are formed by forming “**opening regions OP**” in the “**first sacrificial layer SL1**” and then filling the opening regions “with an insulating material.” Park, 12:65-13:17.



Park, Figs. 20-21 (annotated).⁸ Petitioner appears to concede, as it must, that the isolation insulating layers are “formed in the sacrificial layer SL1.” See Pet. 33

⁸ In Park’s Fig. 21, the X and Y axes seem to be mislabeled, which is corrected in the annotated figure.

(citing Park, 12:65-13:1)). Moreover, because the alleged isolation insulating layers are formed in the sacrificial layer rather than a BSG, they are not formed in the BSG “to separate the BSG into a plurality of sub-BSGs,” as claimed, and thus do not perform the important BSG separation function of the ’623. Petitioner’s arguments for this term are entirely premised on its implicit claim construction, which as discussed in §V.A is incorrect. KuhnII, ¶90.

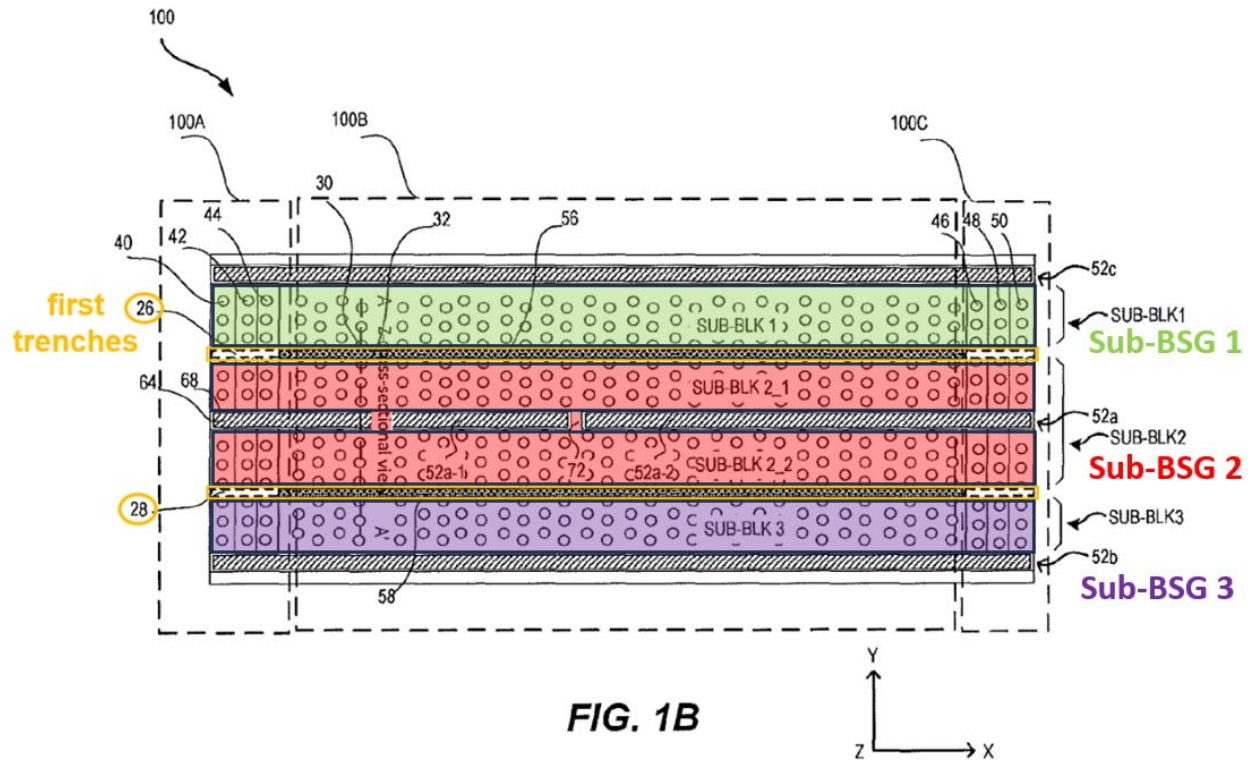
Accordingly, Petitioner fails to show that Park’s isolation insulating layer is formed in the BSG. KuhnII, ¶91.

2. Park’s Isolation Insulating Layers Do Not “Extend[] in a Length Direction of the Substrate to Separate the BSG Into a Plurality of Sub-BSGs” (Limitation [1.e])

Park fails to disclose that its alleged dielectric trenches (isolation insulating layers) “extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” as required by the Challenged Claims because Park’s isolation insulating layers are short separations limited to the staircase region. KuhnII, ¶92.

Claim 1 requires “one or more first dielectric trenches ... **extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.**” As discussed in §V.B, this limitation requires that the length of the dielectric trench is what separates the BSG into sub-BSGs. KuhnII, ¶93. For example, the ’623 shows dielectric trenches 26 and 28 that extend the length of the substrate,

from one staircase region to the other and through the active region, to separate the BSG in sub-BSGs:



'623, Fig. 1B. KuhnII, ¶93.

In contrast, Petitioner maps this element to isolation insulating layers in Park, which as shown below are short cuts through the common source lines.

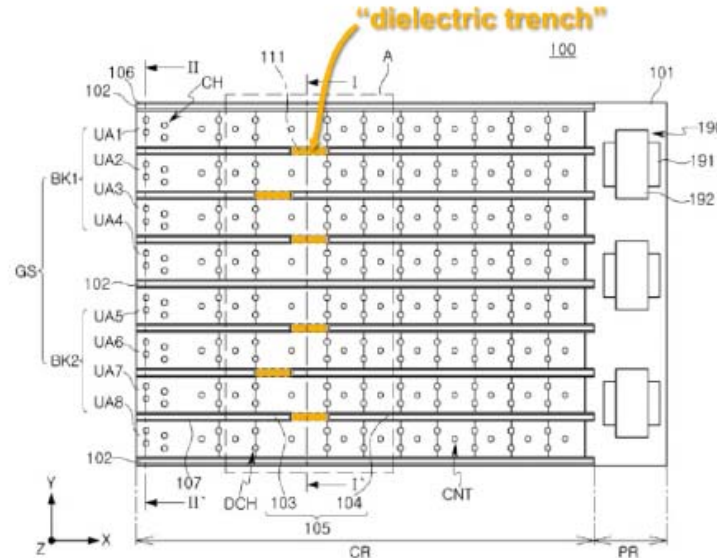


FIG. 3

Fig. 3 (annotated by Petitioner, Pet. 30-31). KuhnII, ¶94.

Park's isolation insulating layers do not extend in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs as required by the Challenged Claims. The isolation insulating layers are merely short cuts in the common source line and do not even extend into the active region, and therefore are not a feature that extends in the length direction of the substrate to separate the alleged BSG into sub-BSGs. For instance, as shown below in Figure 3, Park teaches that its memory device has a plurality of **"first common source lines 102"** and **"second common source lines 105."** Each of the second common source lines are composed of a first section, *i.e.*, **"first lines 103,"** and a second section, *i.e.*, **"second lines 104."** See, *e.g.*, Park, 16:55-59; see also Park, 1:59-61. The **first lines 103 and second lines 104 of the common source lines** each extend horizontally along

the x-direction, and have short gaps (annotated in green) in the staircase region of the memory device:

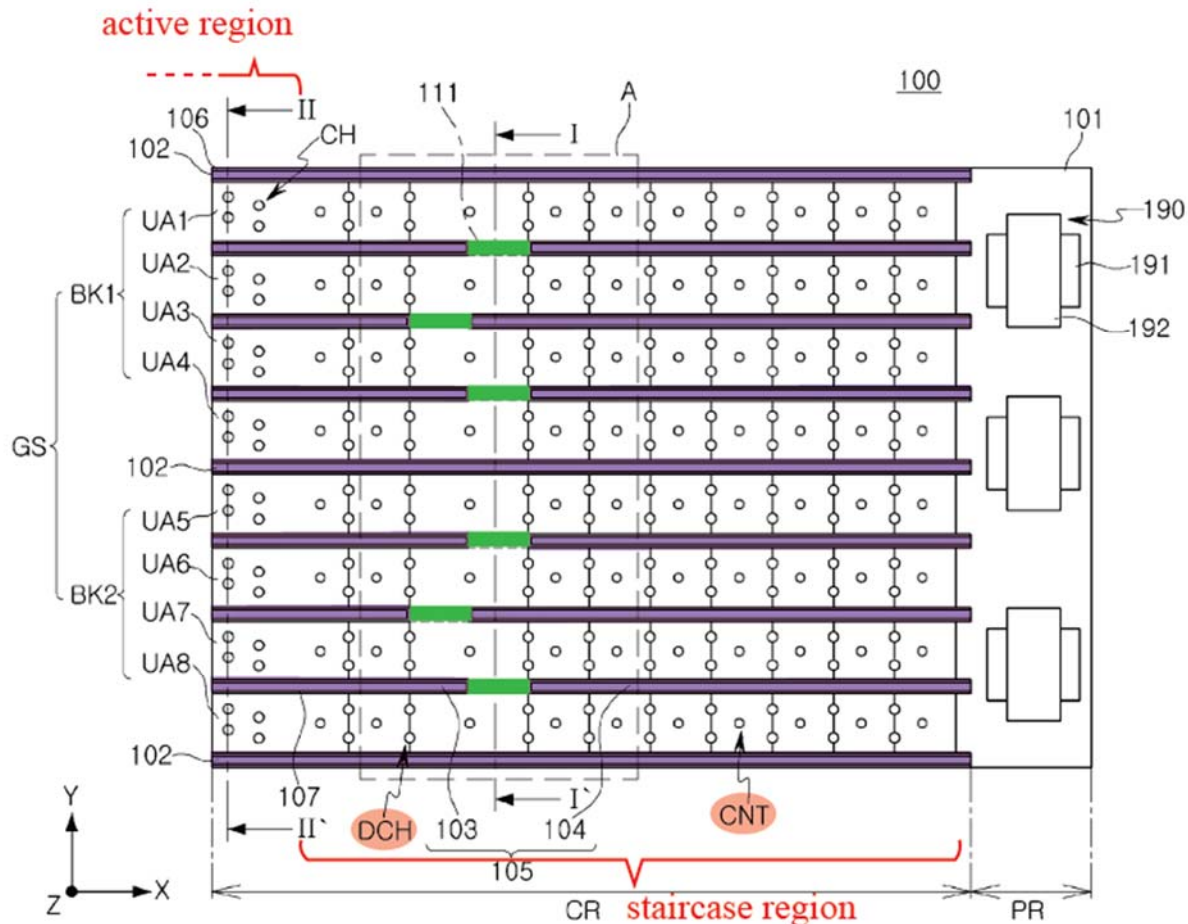


FIG. 3

Park Fig. 3 (annotated). Park further discloses that in this gap an “isolation insulating layer 111 [is] disposed between the first and second lines 103 and 104.”. Park, 10:63-65. Accordingly, the **isolation insulating layer 111** is a short division in the **second common source lines 105** that separates the first and second lines 103 and 104. Figure 3 of Park also shows that the **isolation insulating layers** extend no more than just the distance from the center of one dummy channel (DCH) and the

center of an adjacent contact (CNT). Moreover, Park’s **isolation insulating layers** are small, localized regions in the staircase structure, confined to the very edge of the memory array with the dummy channel structures **DCH** and cell contacts **CNT**, completely outside the active region—i.e., away from the majority of the BSG that Petitioner claims it separates. KuhnII, ¶95.

Thus, Park isolation insulating layers do not extend in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs as required by the Challenged Claims. In its Institution Decision, the Board found that this limitation is met by “common source lines *in cooperation with* isolation insulating layer 111” (DI 15 (emphasis in original)), but the conclusion was based on an incorrect preliminary claim construction. See §V.B. Under the proper construction, which requires that the length of the dielectric trench is what separates the BSG into sub-BSGs, Park’s short isolation insulating layers 111 do not satisfy the claim. KuhnII, ¶96.

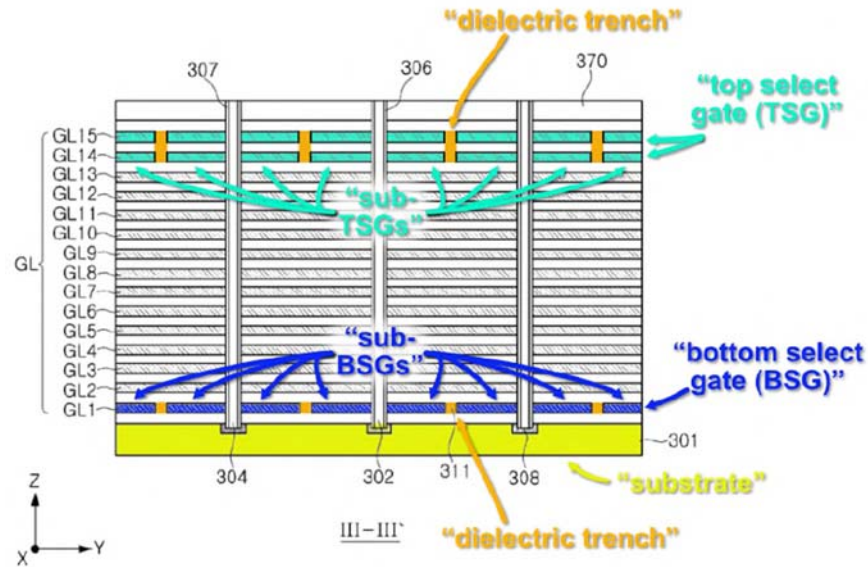
For at least the reasons provided above, Park fails to disclose or render obvious the claimed dielectric trenches that extend in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs. KuhnII, ¶97.

B. Claim 2: Park Does Not Disclose or Render Obvious “One or More Second Dielectric Trenches Formed in the TSG and Extending in the Length Direction of the Substrate to Separate the TSG into a Plurality of Sub-TSGs”

Park does not disclose any dielectric trenches formed in the TSG, as required by claim 2, and Petitioner has not shown that it would have been obvious to modify Park to include any such trenches, let alone trenches that extend in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs. KuhnII, ¶98.

Claim 2 recites “one or more second dielectric trenches ... extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.” As discussed in §V.C, this limitation requires that the length of the dielectric trench is what separates the TSG into sub-TSGs. KuhnII, ¶99.

Park does not disclose any dielectric trench that even arguably separates the TSG into a plurality of sub-TSGs, as Petitioner concedes. Pet. 41. Accordingly, Petitioner instead argues that it would have been obvious to modify Park to “include another isolation insulating region 111” in the upper SSL layers, and presents a modified version of Figure 36, copied below, to illustrate the proposed modification that has dielectric trenches in the alleged TSG directly above the alleged dielectric trenches (isolation insulating layers) in the alleged BSG. Pet. 43.

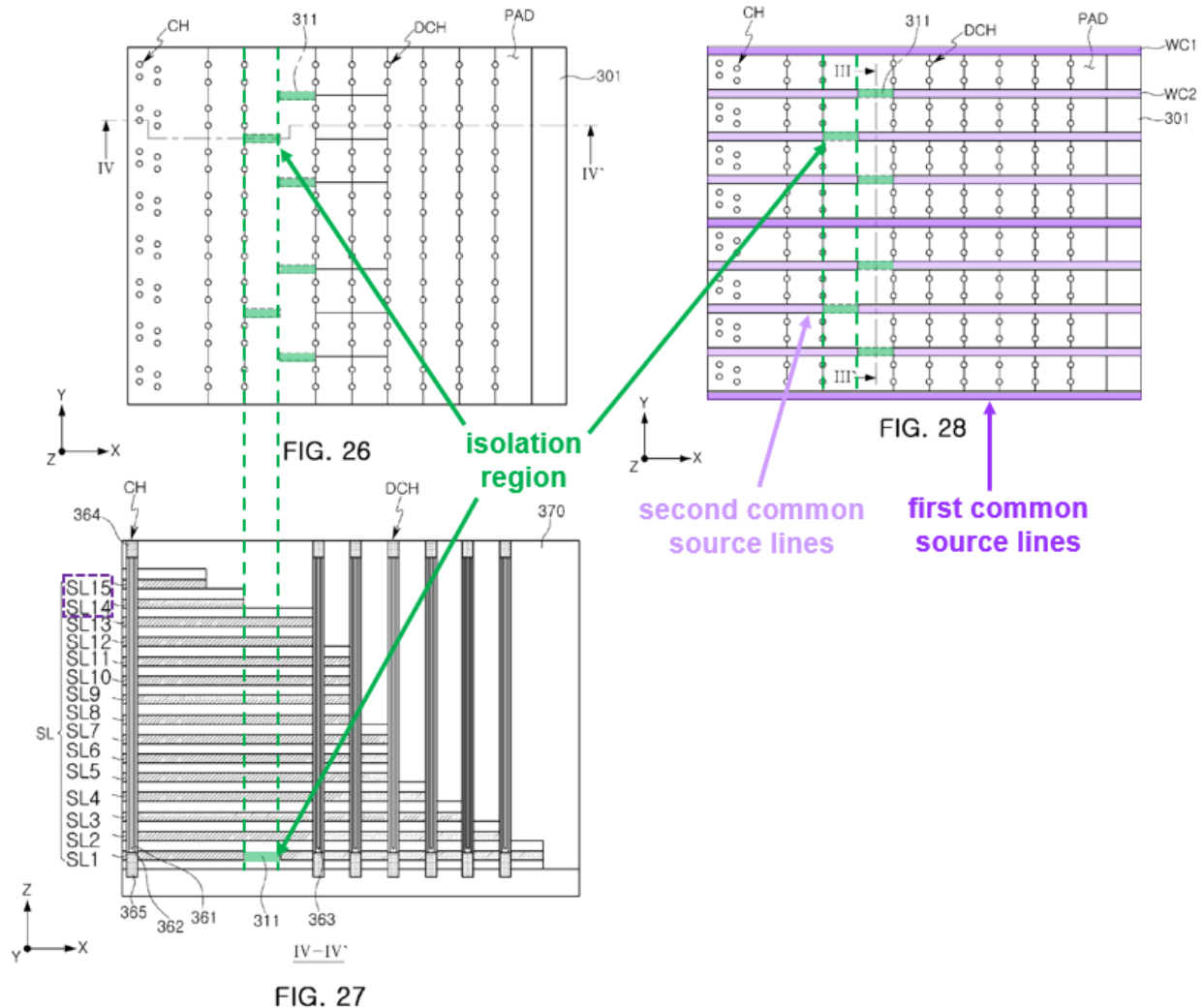


Park, Fig. 36 (modified and annotated by Petitioner at Pet. 43). KuhnII, ¶100.

A POSITA would not have modified Park to include an isolation insulating layer in the alleged TSG (SLL) because **there is no TSG in the region where Petitioner proposes adding the isolation insulating layer, because the TSG ends before it reaches that location.**⁹ Petitioner’s proposed modification is to add an isolation insulating layer in the alleged TSG in a very specific location—directly above the isolation insulating layer in the alleged BSG. Pet. 43-45. But as Petitioner concedes, Park’s source upper select line (SSL), *i.e.*, the purported TSG, does not

⁹ Petitioner’s proposed modification relies on errors in several of the cross-sections, as explained in detail below, which Petitioner wrongly contends is a separate embodiment. KuhnII, ¶104.

extend into the staircase region as much as Park's GSL, and as a result, "is not present over the portion of the GSL [alleged BSG] divided by 'isolation insulating layers 111.'" Pet. 41. This is also shown below in connection with Figs. 26-28, where the isolation insulating region 311 is highlighted in green.



Park, Figs. 26-28 (annotated).¹⁰ As seen in Park's Figures 26-27, which show the device at the same stage of its manufacture, the sacrificial layers SL14 and SL15 do not extend to the right vertically above (in the Y direction) **isolation regions 311**. Thus, in that location there is no TSG in which to add the proposed isolation region. The upper common source lines (alleged TSG) simply end before they reach that location. Therefore, while the SSL (alleged TSG) is separated into portions, it is separated entirely by the common source lines, and not by any dielectric trench. Park, 6:4-8 ("In an example, portions of the string select line may be separated from each other at boundaries between the first to eighth unit areas UA1 to UA8 by the first common source lines 102 and first lines 103 of the second common source lines 105."). And while the **first common source lines** and the **second common source lines** are shown with **isolation regions 311** in the top-down view of Figure 28, that is only because the depicted features represent the bottom layer, e.g., SL1 (the alleged BSG), where the common source lines extend much further into the staircase region. KuhnII, ¶101.

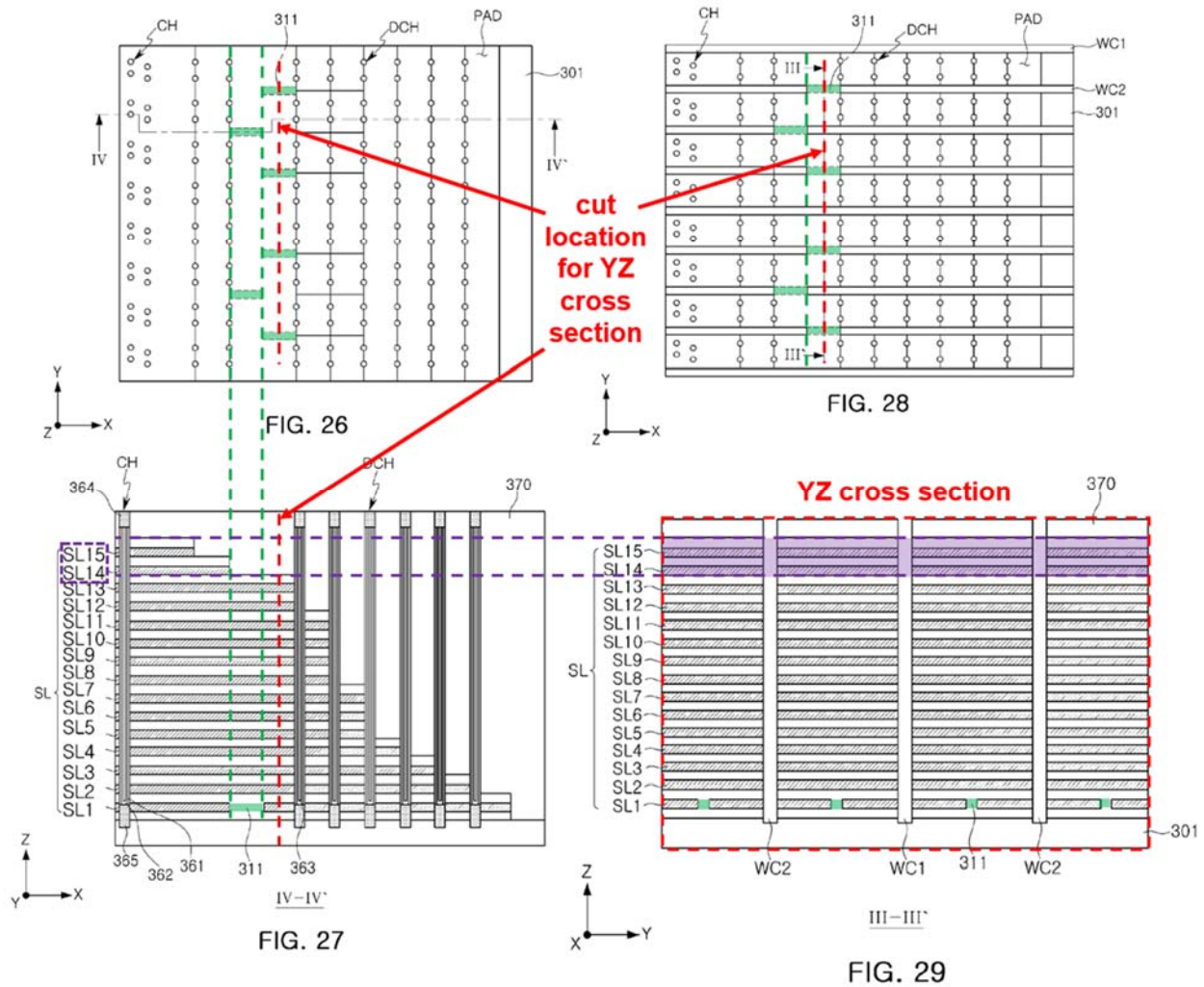
¹⁰ In Park's Figure 27, all the sacrificial layers are mislabeled as "SL15" rather than the correct labeling which can be found in Figure 25. This is corrected in the annotated version of Fig. 27 shown here. KuhnII, ¶101.

The alleged TSG (SSL) is shorter on top than the lower layers (and thus prevented from including the proposed isolation insulating layer) in order to form the “stepped structure” (staircase structure) of the ends of the gate electrode layers that is critical to Park’s disclosure. Park, 6:56-64. This stepped structure enables “pad regions” that host “cell contacts CNT” that are necessary in order to supply voltage to the gate electrodes. Park, 7:60-8:6. Park does not disclose an embodiment where the SSL (alleged TSG) has the same physical extent as its GSL (alleged BSG), which would have contradicted its teachings. KuhnII, ¶102.

Petitioner asserts that Park has “other embodiments” where “the upper SSL is located over the portion of the GSL divided by isolation insulating layers” and Park’s Figure 36 relates to such an embodiment (Pet. 41), but Petitioner is incorrect—the entire series of Figures 18 through 36 depict the same embodiment. Specifically, Figures 18 through 36 depict the same embodiment at different stages of its manufacture. Park, 12:53-55 (“FIGS. 18 through 36 are views illustrating a method of manufacturing a memory device according to *an* example of the present inventive concept.”). KuhnII, ¶103.

Petitioner nonetheless maintains that Figure 36 of Park shows that the SSL (alleged TSG) is present above the isolation insulating layer 311 (Pet. 41-42), but the cross section view of Figure 36 includes an error and mistakenly shows all of the layers present in the device—the top layers do not extend to where the cross section

is located. For example, an analysis of the cross section that results in Figure 29 reveals that the top four layers (SL15 to SL 14), which are highlighted in the figure, are not present in that region and should not have been depicted in Figure 36 (or in 29):



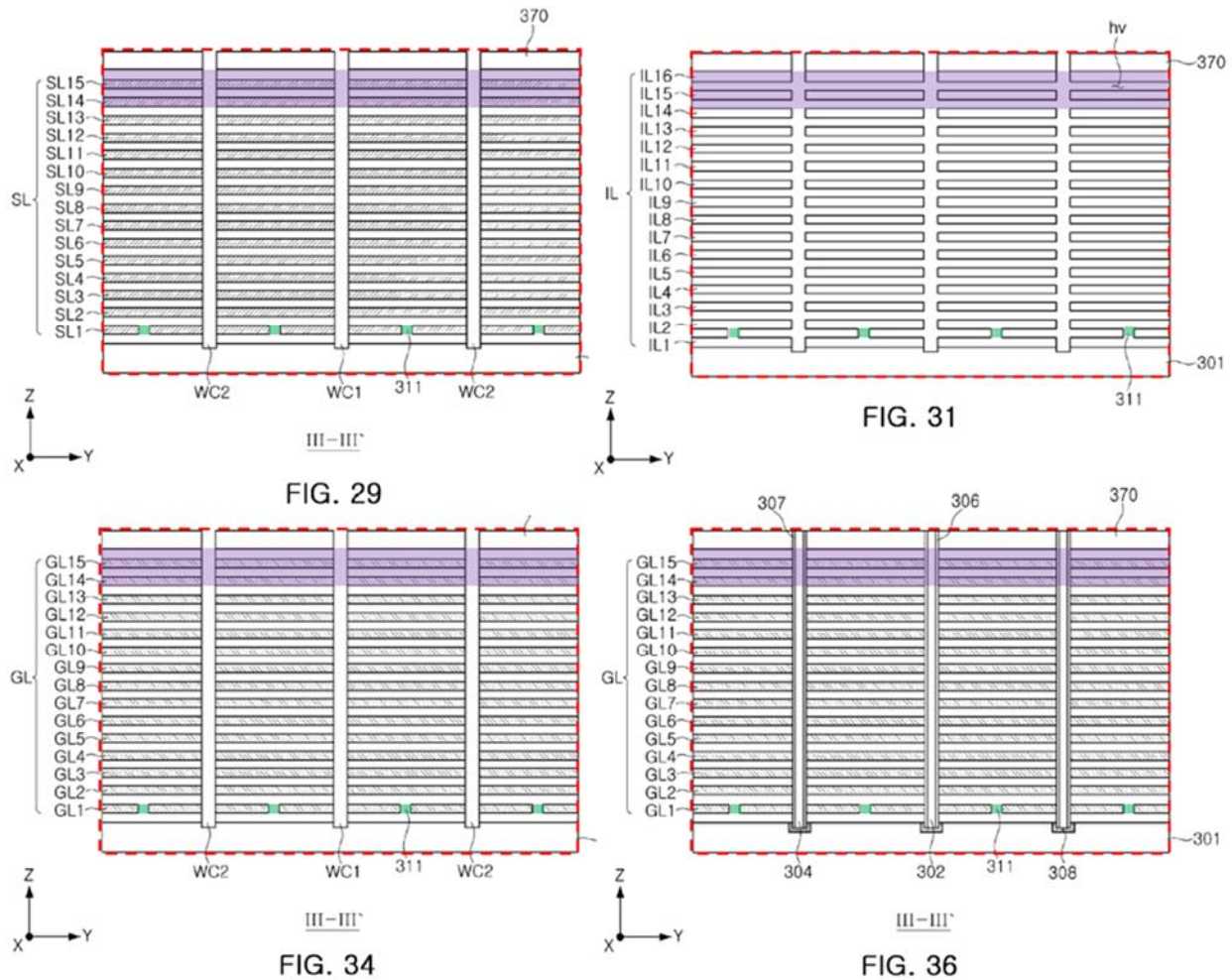
Park, Figs. 26-29 (annotated). The following steps illustrate the issue:

- 1) The YZ cross section in Figure 29 is taken along the III-III' line depicted in Figure 28. Park, Figs. 28-29.¹¹
- 2) Figure 28 provides the same view of the device as Figure 26 but at a later stage of its manufacture. The III-III' line can thus be carried over to Figure 26. Park, Figs. 26, 28.
- 3) The XZ cross section in Figure 27 is taken along the IV-IV' line depicted in Figure 26. Park, Figs. 26-27. Thus, the two figures can be aligned as shown below to reveal where the YZ cross section of Figure 29 is located in Figure 27. The cross section does not include the top four layers present in the device at that stage: IL16, SL15, IL15, and SL14 (the insulating layers IL1 through IL16 are not labeled in Figures 27 and 29 but they are labeled in, e.g., Figure 23).

Likewise, Figures 31, 34, and 36 provide the same view of the device as Figure 29 but at later stages of its manufacture. In particular, Figure 31 depicts the device after the removal of the sacrificial layers SL, forming “horizontal voids” (“hv”) in their place, Figure 34 depicts the device after the horizontal voids are filled to form gate

¹¹ Park mistakenly states “FIGS. 27, 29 and 31 are cross-sectional views take [sic] along lines IV-IV' of FIGS. 26, 28 and 30” (Park, 3:11-12), but Figure 29 itself indicates it is a cross-sectional view taken along line III-III' (of Figure 28).

electrode layers GL1 through GL15, and Figure 36 depicts the device after the common source lines are formed in the word line cuts. Park, 15:35-45, 16:3-16, 16:50-55. KuhnII, ¶104.



Park, Figs. 29, 31, 34, 36. As a result, in all for of these cross sections, the highlighted top layers are depicted by error and are not in fact present. And, again, interpreting these errors as an “other embodiment” as Petitioner proposes would conflict with Park’s teachings because it would eliminate the necessary stepped structures used for cell contacts, rendering Park’s device inoperable. KuhnII, ¶104.

Thus, there is no alleged TSG at the location of Petitioner's proposed modification, and a POSITA could not have made such a modification. KuhnII, ¶105. Petitioner's entire argument is based on a non-existent embodiment where the SSL extends farther into the edge of the device than it actually does, and as a result Petitioner is attempting to solve an imaginary problem by introducing trenches to separate SSLs even though they are already completely separated into by the common source lines. KuhnII, ¶105.

Petitioner's arguments about combining different embodiments (Pet. 44) fail because Petitioner does not combine different embodiments. Similarly, Petitioner's arguments about applying Park's teachings about "isolation insulating layers" in its GSL to its SSL (Pet. 44) also fail, because the problem those teachings address (*i.e.*, separating the GSL into portions in combination with the common source lines in the staircase region) is not present for the SSL, as the SSL does not extend into the staircase and is already separated into portions. Therefore, a POSITA would have had no motivation to modify Park's SSL to include similar isolation insulating layers. KuhnII, ¶106.

Even if it would have been possible and obvious to make the proposed modification to Park, Petitioner's proposed trenches are not "extending in the length direction of the substrate" as required by claim 2. Petitioner proposes adding narrow isolation regions to the SSL based on the use of such isolation regions in the GSL,

but these isolation regions are not “extending in the length direction of the substrate” for the same reasons discussed in relation to the isolation regions in the GSL. See §VII.A.2. Here, “the length direction” in claim 2 has its antecedent in “a length direction” of claim 1 and thus is Park’s X direction. Yet Petitioner does not even attempt to depict the proposed cuts in a view that would show whether they extend in the purported length direction of the substrate, *i.e.*, the X direction. But for claim 3, Petitioner clarifies that it is proposing adding cuts of the same length above as insulating layer 111 (Pet. 47-48), confirming that the mapping fails for the same reasons discussed in Section VII.A.2. KuhnII, ¶107.

Accordingly, Petitioner fails to show that Park discloses or renders obvious second dielectric trenches formed in the TSG and that the purported second dielectric trenches extend in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs. KuhnII, ¶108.

C. Claim 3: Park Does Not Disclose or Render Obvious “the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate”

For claim 3, the Petition does not address which direction is the “width direction” (Pet. 45), and thus Petitioner has not shown that the alleged first and second dielectric trenches are “aligned with each other in a width direction of the substrate” as required by claim 3. In addition, regardless of which direction is the “width direction,” Petitioner’s mapping again requires adding an isolation insulating

layer in the SSL above the isolation insulating layer 111 in the GSL (Pet. 45), where there is no SSL present, and thus Park fails for claim 3 for the same reasons discussed above for claim 2. KuhnII, ¶109.

D. Claim 10: Park Does Not Disclose or Render Obvious “One or More Dummy BSGs That Are Formed Between the Plurality of Word Lines and the BSG, Separated by the One or More First Dielectric Trenches into a Plurality of Dummy Sub-BSGs”

Petitioner has not shown that Park discloses or renders obvious this limitation because Park nowhere discloses separating the alleged dummy BSGs with dielectric trenches, and Petitioner fails to identify any motivation for using isolation insulating layers 111 to perform such separation. KuhnII, ¶110.

Petitioner concedes that Park discloses only embodiments “where only its select lines—and **not the dummy lines**—are separated into portions corresponding to unit areas,” but asserts that it would have been obvious to separate Park’s dummy lines. Pet. 55-56. However, Park does not teach that its dummy lines should be separated into unit areas; rather, they are separated into blocks and remain connected within the blocks by the “connecting electrodes,” just like the word lines. Park, 7:30-43 (in particular, disclosing that the “dummy lines of each of the first and second blocks” are “separated from each other by the first common source line 102 disposed between the first and second blocks.”). Petitioner states that this “could” be done (Pet. 55-56), which is not the proper test for obviousness. The question for obviousness is whether a POSITA would have been motivated to make this change,

which Petitioner fails to show. *In re Nuvasive, Inc.*, 842 F.3d 1376 (Fed. Cir. 2016). KuhnII, ¶111.

Petitioner points to examples of structures that pass through and divide multiple layers in other references (Shibata, Ex. 1018), but provides no motivation for this modification except a vague reference to “improv[ing] electrical performance” and referring to the declaration of Dr. Lee. Pet. 55-56. Dr. Lee quotes Ex. 1012 to explain the function of dummy word lines and asserts that “[a] POSITA would have recognized that separating dummy BSG into sub-dummy BSGs ... would have the potential to help the dummy BSGs in serving their purposes” “because the loading effects on a specific sub-BSGs [sic] is reduced and more symmetrical.” Ex. 1003, ¶281. He goes on to claim “[s]eparating dummy BSG into sub-dummy BSGs also would have had the potential to reduce the load on the drivers associated with each of the various sub-units.” *Id.* These statements are entirely conclusory and not supported by the cited reference. He does not address, for example, why “the loading effects” on a specific sub-BSG would be “reduced and more symmetrical,” or why “the load on the drivers associated with each of the various sub-units” would be reduced. It is not possible to discern the reasoning for these purported benefits from Dr. Lee’s declaration. In fact, the word “load” in connection with this issue only appears in the above quotes. Without properly explaining how the proposed modification provides the purported benefits,

Petitioner fails to show that a POSITA would have been motivated to make said modification. KuhnII, ¶¶112-114.

Petitioner also fails to explain how a POSITA would have achieved this modification in Park's device. Park specifically teaches forming isolation regions in its first sacrificial layer and subsequently forming the remaining layers on top. Park, 12:65-13:7. Forming deeper isolation regions would have required etching through multiple layers composed of different materials, rather than a single layer composed of one material. Petitioner does not address these challenges, let alone attempt to explain how a POSITA would have overcome them. KuhnII, ¶115.

Accordingly, Petitioner fails to show that Park discloses or renders obvious dummy BSGs that are separated by the first dielectric trenches into a plurality of dummy sub-BSGs. KuhnII, ¶116.

E. Claim 11: Park Does Not Disclose “One or More Dummy TSGs That Are Formed Between the Plurality of Word Lines and the TSG, Separated by the One or More Second Dielectric Trenches into a Plurality of Dummy Sub-TSGs”

Park does not disclose or render obvious this limitation because a POSITA would not have been motivated to add dielectric trenches in the proposed manner. KuhnII, ¶117.

First, as explained above regarding claim 2, Park does not disclose any dielectric trenches formed in the alleged TSG (SSL), and Petitioner has not shown

that it would have been obvious to modify Park to include any such trenches. KuhnII, ¶118.

Second, Petitioner has not shown that it would have been obvious to have those trenches pass through dummy TSGs as Petitioner proposes. Pet. 56-57. For this modification Petitioner refers back to the reasons relating to claim 10 (Pet. 56), which are refuted above. KuhnII, ¶119.

Third, Petitioner asserts that a POSITA would have used “at least some of the adjoining dummy layers” as buffer to ensure that the etching of the purported trenches in the SSL “does not reach the word lines.” Pet. 57. Petitioner’s reasoning is not supported by the evidence and relies entirely on conclusory statements by Dr. Lee. KuhnII, ¶120.

Dr. Lee asserts that in the process of etching trenches into Park’s SSL (which Park does not disclose), a POSITA would have used a timed etch (Ex. 1003, ¶289), which is an etch process that is left to proceed for a specific, carefully determined length of time and then is stopped before it etches any further and damages the device, but Park’s manufacturing process does not suggest a timed etch because Park discloses using selective etching. KuhnII, ¶¶121-122; Park, 12:59-61, 13:4-11. A selective etch is an etch process that is designed to etch the target material significantly faster than the non-target materials, such that it is possible to stop the etch on a specific layer. KuhnII, ¶122. Thus, due to the “problems [that] can arise

when using a timed etch,” as Dr. Lee puts it (Ex. 1003, ¶289), a POSITA would have been dissuaded from using a timed etch to enable Park to be modified to form isolation regions in the SSL. KuhnII, ¶122.

Dr. Lee asserts that due to the uncertainties involved in timed etching, a POSITA would have employed the dummy SSL layers as a buffer (Ex. 1003, ¶¶290-291), but rather than presenting examples of this practice in contemporaneous literature, Dr. Lee’s citation of Ex. 1021 merely provides an example where a dummy gate electrode is also referred to as a buffer gate electrode without identifying a connection with etching. Ex. 1021, [0060]. KuhnII, ¶123.

Further, Dr. Lee does not explain how this process would result in the dummy SSL being separated into multiple dummy sub-SSLs, as claim 11 requires. If a dummy SSL were used as a buffer in the process of etching isolation regions in the alleged TSG above it, the intention would be that the buffer (i.e., the dummy SSL) is at most only partially etched—i.e., merely enough to ensure that the actual target of the etch (the alleged TSG above it) is etched all the way through. If the etch were allowed to go completely through the dummy SSL, then it would start to etch the word line below it. This would risk damaging the word line and therefore would defeat the purpose of using a buffer layer in the first place. In short, using the dummy SSL as a buffer would result in it remaining as a single connected unit—at most only

partially etched—rather than separating the dummy SSL into dummy sub-SSLs as required by claim 11. KuhnII, ¶124.

Accordingly, Petitioner fails to show that Park discloses dummy TSGs that are separated by the second dielectric trenches into a plurality of dummy sub-TSGs. KuhnII, ¶125.

VIII. GROUND 2: PARK IN VIEW OF SHIBATA DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-11

Park in view of Shibata does not disclose or render obvious the Challenged Claims at least because (1) Shibata fails to address the deficiency of Park with respect to Limitation [1.e], and (2) Petitioner has not shown that a POSITA would have been motivated to apply Shibata’s teachings to Park. And as to the added limitations of claims 10-11, Petitioner does not rely on Shibata to address the deficiencies described for Ground 1, and so Ground 2 fails for the same reasons. KuhnII, ¶126.

A. Independent Claim 1: The Combination of Park and Shibata Does Not Render Obvious Limitation [1.e]

Petitioner fails to show that Park in view of Shibata renders obvious limitation [1.e] for at least three reasons: (1) Shibata does not address the deficiencies in Park and therefore the combination does not render obvious dielectric trenches “formed in the BSG,” (2) the combination also does not render obvious dielectric trenches that “extend[] in a length direction of the substrate to separate the BSG into a

plurality of sub-BSGs,” and (3) Petitioner fails to show that a POSITA would have been motivated to apply Shibata’s teachings to Park. KuhnII, ¶127; Shibata, Fig. 16 (annotated); Pet. 58 (citing Shibata, [0090], [0166], Fig. 16).

1. Shibata’s Separation Portions Are Not “Formed in the BSG” and Do Not “Extend[] in a Length Direction of the Substrate to Separate the BSG Into a Plurality of Sub-BSGs” (Limitation [1.e])

Park in view of Shibata does not cure the deficiency of Ground 1 because Shibata’s separation portions 62a, which Petitioner proposes adding to Park, contribute to the separation of only the top select gate and not the bottom select gate. Thus, the addition of Shibata still does not result in a dielectric structure that is (1) “formed in the BSG” and (2) “extend[s] the length direction of the substrate to separate the BSG into a plurality of sub-BSGs” as required by Limitation [1.e]. KuhnII, ¶128.

For the reasons set forth in §VII.A, Park fails to disclose or render obvious “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” In Ground 2, Petitioner attempts to address these deficiencies by applying disclosures from Shibata to Park’s memory device. Petitioner’s Ground 2, however, fails to cure the identified problems discussed above. KuhnII, ¶129.

Petitioner relies on certain disclosures of Shibata’s first and second embodiments. Pet. 58-59; Shibata, [0016], [0047]. Petitioner asserts that Shibata,

as depicted below, discloses “multiple ‘**separation portion[s] 62a**’ [that] pierce[] the drain-side select gate layer of the uppermost layer of the multiple conductive layers 70. ... This divides Shibata’s upper TSG (the **drain-side select gate layers**) into sub-TSGs (portions SDG0-SGD3)”:

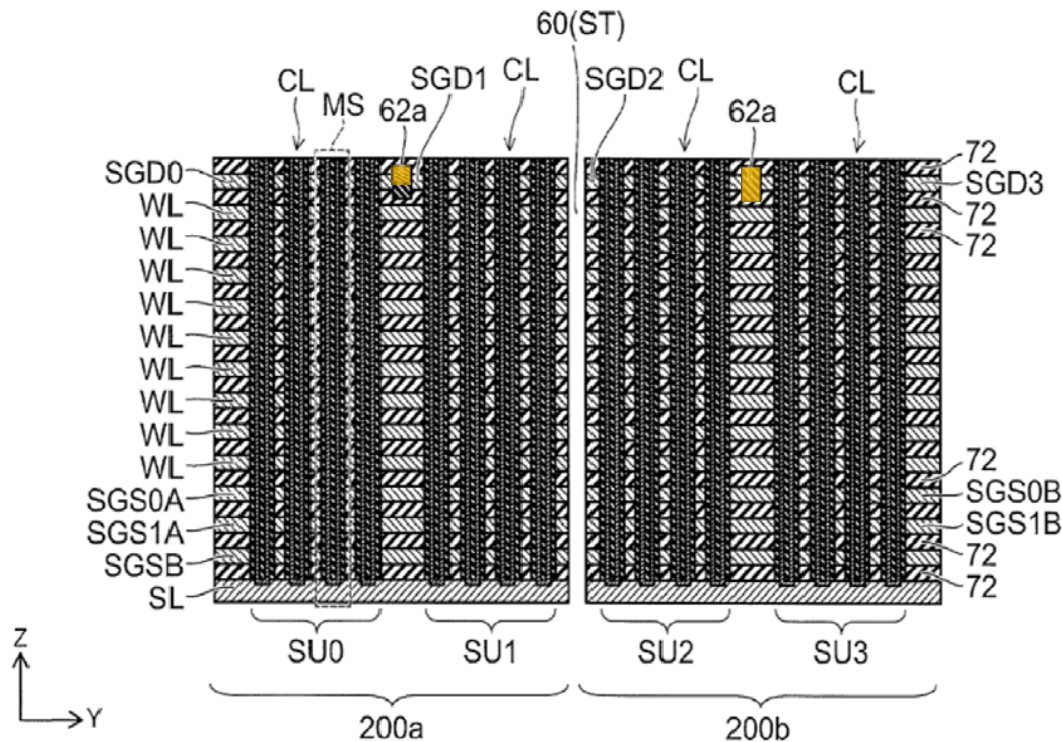
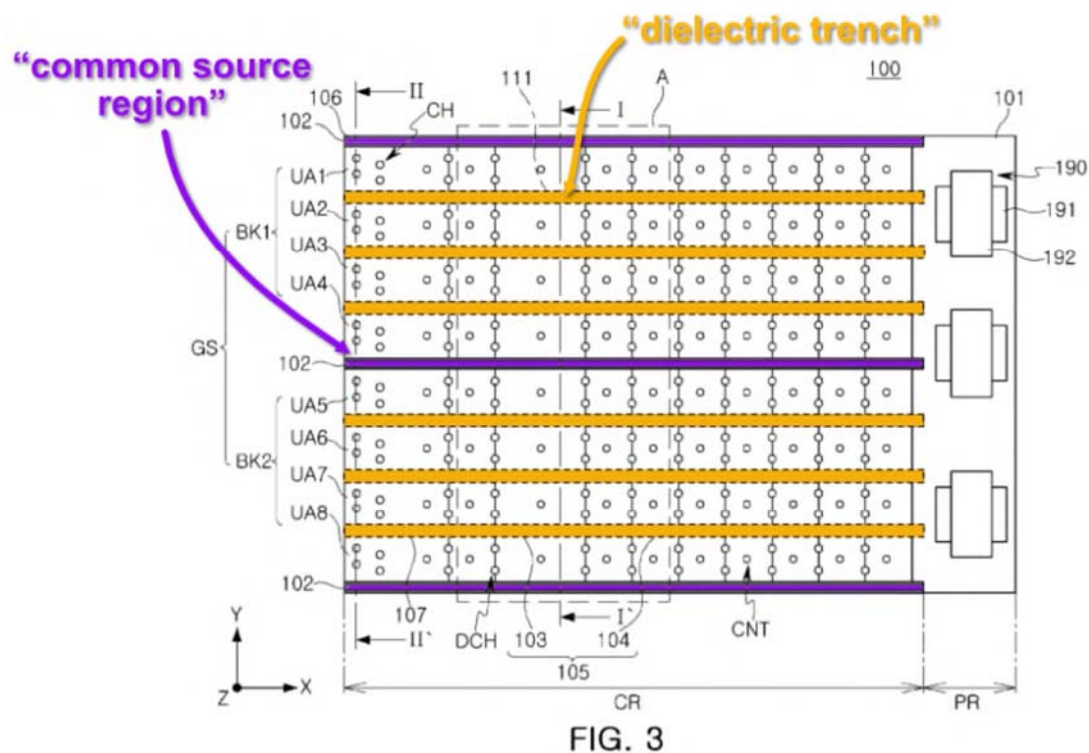


FIG. 16

Shibata, Fig. 16 (annotated); Pet. 58 (citing Shibata, [0090], [0166], Fig. 16). Petitioner further contends that “Shibata’s “separation portion[s] 62a” traverse the entire length of its memory device for purposes of dividing the select gates.” Pet. 59 (citing Fig. 47A). KuhnII, ¶130.

Petitioner then contends that based on the teachings of Shibata, “a POSITA would have eliminated Park’s second common source lines 105 and replace[d] them

with **longer isolation insulating regions 111** with **dimensions analogous to Shibata's separation portions 62a.**" *Cf.* Pet. 59-60. According to Petitioner, the "lengthened isolation insulating regions 111" would "span the length of its device to completely, and by themselves, separate its BSG (the lower GSL) into sub-BSGs" as purportedly illustrated in Petitioner's figure:



Pet. 60 (modifying Park, Fig. 3). KuhnII, ¶131.

Contrary to the Petitioner's arguments, however, the resulting device fails to meet the claims because Shibata discloses that its **separation portions 62a** traverse only the **uppermost** drain-side select gate layer of the memory stack, such that they contribute to the separation of only the **top** select gate, rather than the **bottom** select gate. For example, Shibata teaches that the separation portion 62a "divides the drain-

side select gate layer into a first drain-side select gate SGD0 and a second drain-side select gate SGD1” of one sub-block and “divides the drain-side select gate layer into a third drain-side select gate SGD2 and a fourth drain-side select gate SGD3,” in another sub-block, as depicted in Figure 16. Shibata, [0166]. Shibata teaches that, as can be seen in Figure 16, the separation portion 62a does not extend further to divide the source-side select gate layers (labeled “SGS0A,” “SGS1A,” “SGS0B,” “SGS1B,” and “SGSB” in Figure 16, below).

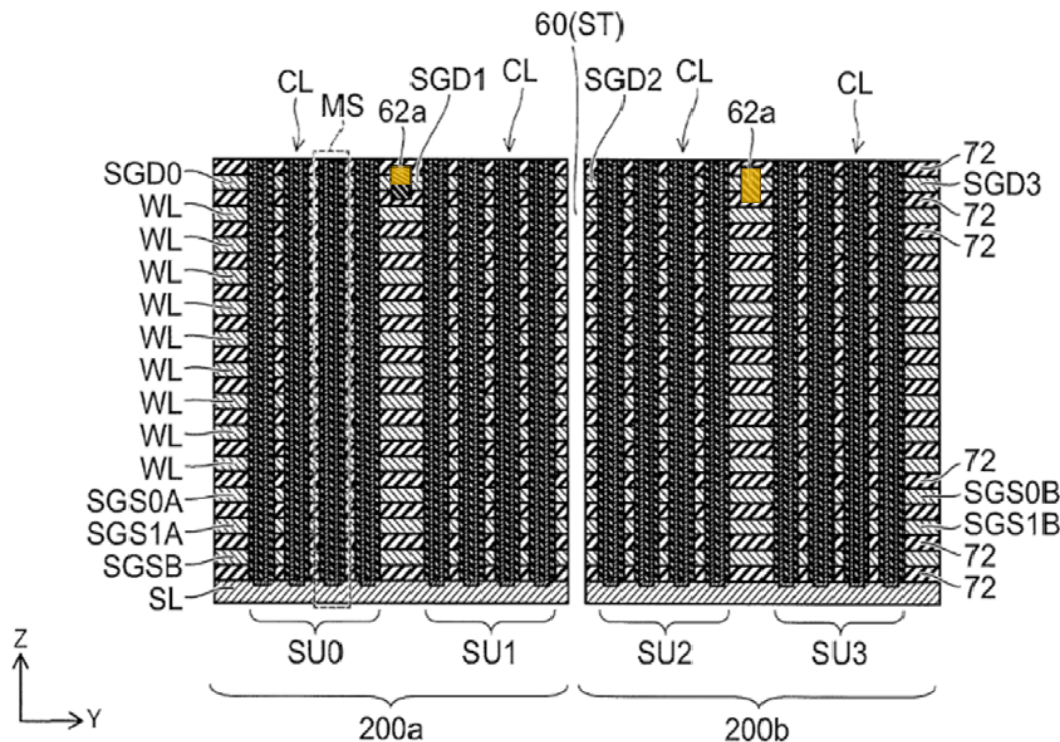


FIG. 16

Shibata, Figure 16. KuhnII, ¶132.

Shibata provides no teaching that its **separation portions 62a** also traverse the lower source-side select gate layers such that they separate the bottom select gate

layers. Nor does Shibata teach adding additional **separation portions 62a** to the source-side select gate layers to separate the bottom select gate layers. Indeed, Shibata expressly teaches not to extend the separation portions 62a to divide additional conductive layer, such as a bottom select gate:

“The separation portion 62a is disposed between the first string unit SU0 and the second string unit SU1 adjacent to each other in the Y-direction, **pierces only the drain-side select gate layer of the uppermost layer** of the multiple conductive layers 70, **and does not divide the other conductive layers** of the multiple conductive layers 70.”

Shibata, [0137]. In other words, Shibata teaches separation portions 62a do **not** divide the bottom select gate layers, which are on the drain-side and are conductive layers of a memory device. Thus, Petitioner’s cited disclosures from Shibata that teach separating the top select gate layers do not provide the teachings that are missing from Park. *See generally* Pet. 58-61. KuhnII, ¶133.

Accordingly, Petitioner fails to show that Park in view of Shibata render obvious an isolation insulating layer (1) formed in the BSG and (2) extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs. KuhnII, ¶134.

2. A POSITA Would Not Have Been Motivated to Apply Shibata's Teachings to Park

In addition, by proposing a combination based on hindsight and misinterpretation of the references, Petitioner also fails to show that a POSITA would have been motivated to make the proposed modifications to Park in view of Shibata's teachings. KuhnII, ¶135.

A POSITA would not have been motivated to make Petitioner's proposed combination because Park teaches not to make such a combination. Park actively discourages elongating the isolation insulating layers because the longer paths by which the etching solution must flow could prevent the complete removal of the sacrificial layer and cause voids in the gate electrode layers GLs.¹² See Park, 15:35-16:49. Moreover, Park discourages placing isolation insulating layers side-by-side, as they are in Petitioner's modified Figure 3 of Park reproduced above, because it

¹² In addition to showing that a POSITA would not have made the proposed change, these teachings in Park amount to a teaching away from the proposed combination. See *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994) (“[I]n general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant.”); see also *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017). KuhnII, ¶136.

would block the flow of etching solution from the sides and again prevent the removal of sacrificial layers and formation of active layers. *Id.* KuhnII, ¶136.

To explain these issues further, and with reference to Figure 30, Park discloses that sacrificial layers SL are “removed by an etching solution flowing through the first and second **word line cuts WC1 and WC2.**” Park, 15:35-37. These “**word line cuts WC1 and WC2**” correspond to the “regions in which common source lines 102 and 105 are subsequently formed. Park, 15:20-22. In other words, the openings that later form the first and second common source lines are first used as the passage through which etching solution is administered to remove the sacrificial layers. These same **word line cuts WC1 and WC2** are also used to deposit conductive material in the openings left by the removal of the sacrificial layer in order to later form the gate electrode layers GL. Park, 16:38-40.

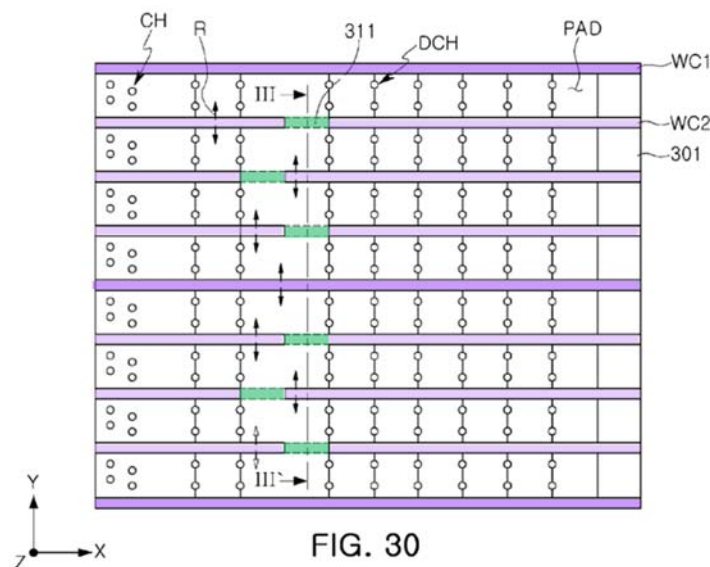
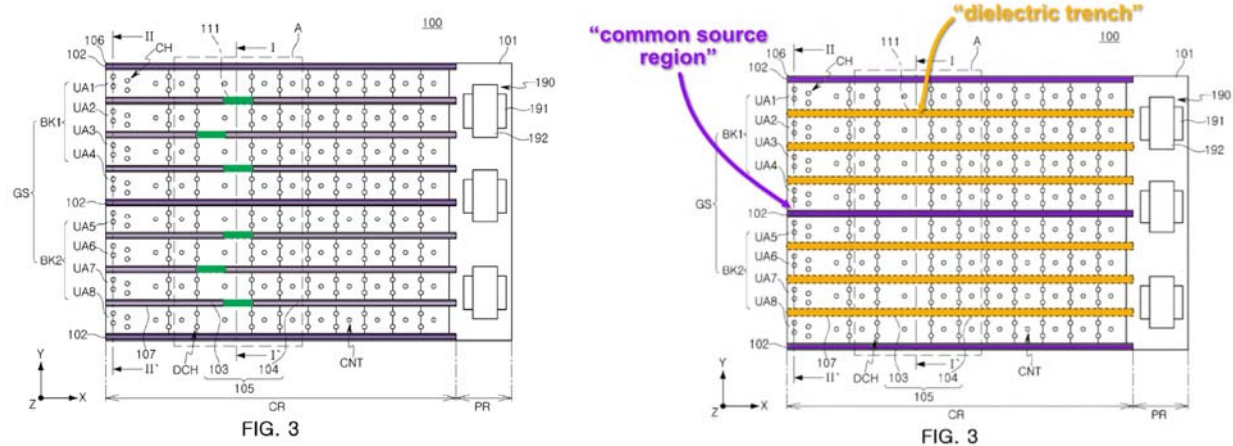


FIG. 30

The problem recognized by Park is that the “**isolation regions 311**” (corresponding to Park’s Figure 11’s **isolation insulating layer 111**) prevents the flow of the etchant and conductive materials, which is the reason for their short length. *See* Park, 15:54-55 (referring to “relatively long [flow] path above the isolation regions 311 in which the second word line cuts may be separated from each other”). That is, the problem is two-fold: first, because there is no word line cut in any of the layers above the isolation insulating layer, the flow path is relatively long; and second, because etching solution and metal do not flow through isolation insulating layers, there is no flow to regions between isolations insulating layers. *See* Park, Fig. 30 (illustrating the “inflow passage R” stemming from each of the word line cuts). Thus, where the “inflow passage of the [etching solution] is not properly secured, a portion of the sacrificial layer SL may remain without being removed.” Park, 15:56-59. Similarly, this may generate a “void” when depositing the conductive material to form the BSG and word lines, the very same defect that Park seeks to avoid during fabrication. Park, 16:44-49. KuhnII, ¶137.

Thus, Park teaches that Petitioner’s proposed modification—which replaces short **isolation insulating layers 111** with much longer **dielectric trenches**, as illustrated below—would result in a memory device that, due to long flow paths, has missing BSG where the sacrificial layer SL between the isolation insulating regions

is never removed, and has poorly formed word lines in the regions above the much longer proposed **dielectric trenches**.



Park, Fig. 3 (left is the unmodified version annotated by Patent Owner; right is Petitioner's demonstrative at Pet. 60 modifying the figure). KuhnII, ¶138.

Indeed, Park is so concerned with this problem that, even for its short isolation insulating layers 111 (which are only as long as the distance between dummy channel and contact), Park proposes staggering the **isolation insulating layers 111**, as shown below. Park, 15:60-16:2. Staggering, however, is not possible when the isolation insulating layers are modified to span the entire memory array as proposed by Petitioner. KuhnII, ¶139.



FIG. 3

Petitioner’s argument that Shibata resolves the operability problem by providing “drive circuits” (Pet. 62) is wrong for several reasons. Shibata provides no solution to Park’s concern that longer isolation insulating layers facing one another could prevent effective replacement of the sacrificial layer and generate voids in the BSG and word lines. *See* Park, 9:31-35, 15:56-49, 16:44-49. Shibata also does not teach connecting multiple “drive circuits” to the source-side select gates, which are positioned in the harder to reach bottom layers of the stack, but instead teaches connecting multiple drivers to the drain-side select gates which are at the top of the stack. *See* Shibata, [0447]-[0448]. Finally, Shibata’s driver configuration is a fixed solution (which entails permanently connecting two drive circuits to certain drain-side select gates and only one drive circuit to others). *See*

Shibata, [0447]-[0448]. As a fixed solution, connecting multiple drivers to certain drain-side select gates is practical for addressing predictable differences in resistances recognized by Shibata. Shibata, [0325] (recognizing that the “resistance of the drain-side select gate not adjacent to the slit ST easily can be higher than the resistance of the drain-side select gate adjacent to the slit ST”). Shibata’s fixed solution, however, is not practical for addressing unpredictable variations in word line quality due to variations in efficient flow paths. KuhnII, ¶140.

Petitioner’s backup argument—“replacing some, but not all, of Park’s common source lines” (Pet. 62-63)—also fails. As illustrated below, even in Petitioner’s drawing there remains the problem facing isolation insulating layers (highlighted in teal) where there is no flow path from the “common source region” (marked purple by Petitioner):

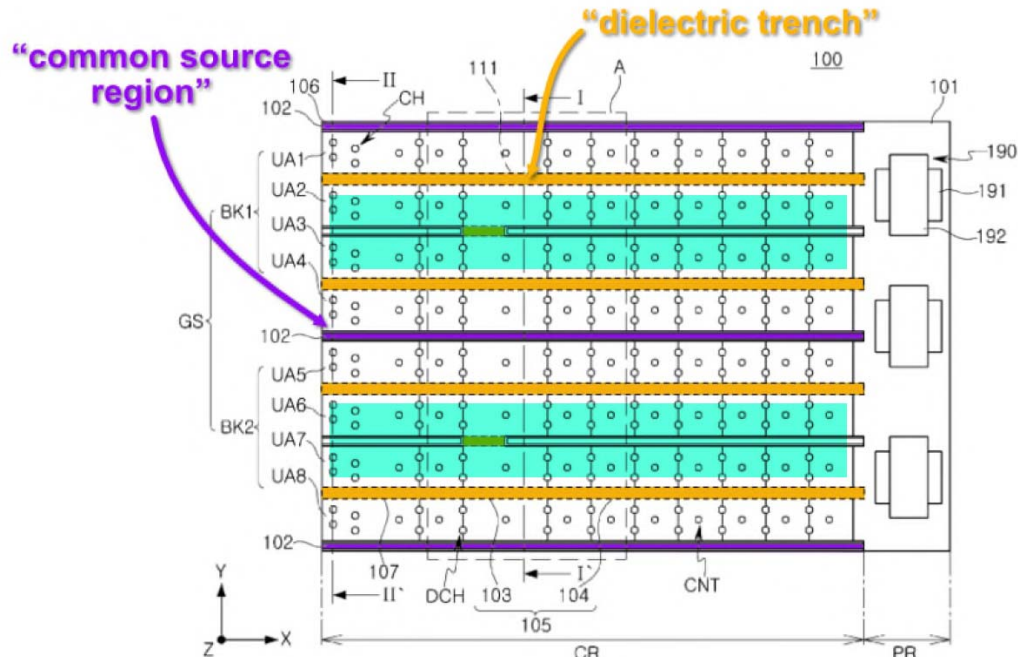


FIG. 3

And to the extent it is argued that it would have been obvious to alternate placement of Park's common source regions and the modified isolation insulating layers, this would still exacerbate the ineffective etching above these extended isolation regions that Park cautions against because as Park explains, the "path above the isolation regions [] in which the second word line cuts WC2 may be separated from each other" will be "relatively long." Park, 15:53-56. Regardless, such a solution is not based on any identified motivation, but on impermissible hindsight. KuhnII, ¶¶141-142.

A POSITA further would not have been motivated to replace Park's second common source lines 105 with longer isolation insulating regions 111 analogous to Shibata's separation portions 62a because doing so would reduce the number of common source lines in the memory device. Instead of having a total of eight

common source lines (*see* Park, Fig. 3 depicting two first common source lines 102 and six second common source lines 105), the proposed combined system would eliminate six second common source lines, leaving only two first common source lines. This results in a 75% reduction in the number of common source lines. KuhnII, ¶143.

A POSITA would have understood that reducing the number of common sources lines would have several adverse effects on the memory device, including: (1) higher resistances in the remaining source lines leading to reduced read and write speeds, (2) increased heat generation owing to higher currents carried in the remaining source lines, (3) increased electrical stress on the remaining source lines leading to a reduced device lifespan, (4) significant voltage drops across the remaining source lines, adversely affecting the accuracy of reading, writing, programming and erasing operations of the memory device, and (5) increased crosstalk leading to more signal interference and increased error rates. *See e.g.*, Ex. 2001, 5 (stating “[d]ecreasing the CSL resistance can reduce the CSL noise”); Ex. 2002, 6 (explaining that CSLs should be “lines of low resistance” as to not adversely impact memory speeds); Ex. 2003, 2-3 (explaining that voltages on the CSL can impact the memory device speeds, such as read speed); Ex. 2004, 6-7 (stating “higher current densities may contribute, directly or indirectly” to device degradation); Ex. 2005, 2 (stating that “[h]igher current densities ... give rise to

greater heat generation and combine to increase electromigration failures”); Ex. 2006, 8 (stating “heat generation in [a] semiconductor increases as the current density increases”). KuhnII, ¶144.

While reducing the number of common source lines may lead to a reduction of the memory array area, this would only exacerbate the very problem that Park intends to avoid. Specifically, reducing the number of common sources lines would only increase the long “inflow paths” and thus worsen any problems with etching of the sacrificial layer and deposition of the gate layers. A POSITA, therefore, would not have simply removed source lines because any purported benefit from reducing the memory array would have come at a significant trade-off in memory device performance, including in speed, thermal management, reliability, longevity, accuracy, and device scalability, which Petitioner fails to address. Accordingly, a POSITA would not have been motivated to modify Park as to remove the second common source lines, as Petitioner’s proposed combined system requires. KuhnII, ¶145.

Thus, Petitioner fails to show that a POSITA would have been motivated to modify Park in view of Shibata. KuhnII, ¶146.

B. Claims 10-11: Park in View of Shibata Also Does Not Render Obvious These Claims

Petitioner does not rely on Shibata for the claimed dummy BSGs or TSGs, and does not include any additional analysis of these elements beyond its analysis in

Ground 1 (Park), and therefore these claims are not met for the same reasons discussed for Ground 1. KuhnII, ¶147.

IX. GROUND 3: PETITIONER FAILS TO SHOW THAT SHIBATA IN VIEW OF PARK DISCLOSES OR RENDERS OBVIOUS CLAIMS 1-11

Shibata in view of Park does not disclose or render obvious the Challenged Claims at least because Petitioner has not shown that a POSITA would have been motivated to apply Park’s teachings to Shibata—its analysis fails to address numerous concerns with the combination, is supported by conclusory assertions, and ultimately is guided by hindsight. And as to the added limitations of claims 10-11, Petitioner does not rely on Shibata to address the deficiencies described for Ground 1, and so the Ground 3 fails for the same reasons. KuhnII, ¶148.

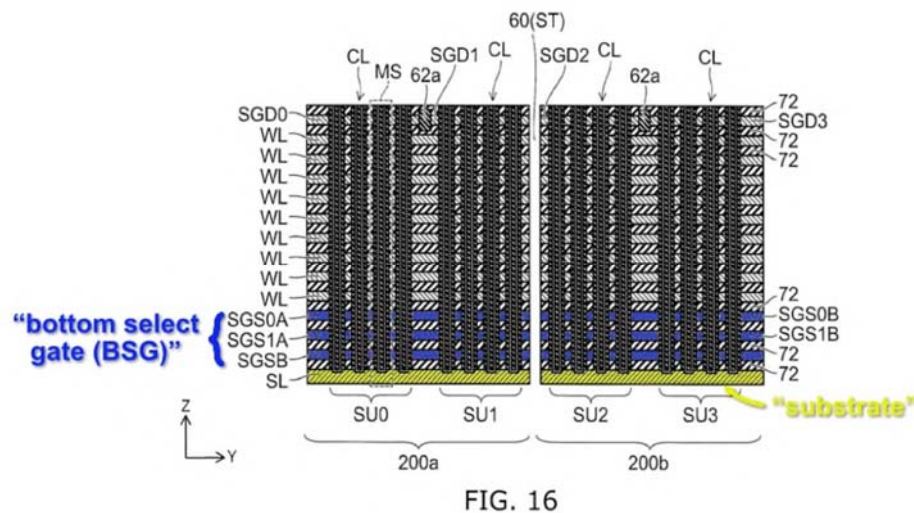
A. Independent Claim 1: Petitioner Fails to Show That a POSITA Would Have Been Motivated to Apply Park’s Teachings to Divide Shibata’s Lower Gate Layer into Multiple Portions

Again relying on impermissible hindsight, conclusory assertions, and misinterpretations of the references, Petitioner fails to show that a POSITA would have been motivated to make the proposed modifications to Shibata in view of Park. KuhnII, ¶149.

Ground 3 of the Petition incorrectly argues that Shibata in view of Park renders the Challenged Claims obvious. Petitioner generally relies upon the teachings of Shibata for each of the limitations, but for limitation [1.e], the Petition

sets forth two flawed modifications to Shibata's memory in light of Park's teachings. KuhnII, ¶150.

For each of limitations [1.b], [1.c], [1.d], and [1.f], which recite a "bottom select gate" (BSG), Petitioner argues that the "lower source-side select gate or SGS layers" of Shibata's second embodiment is the bottom select gate BSG, as illustrated below:

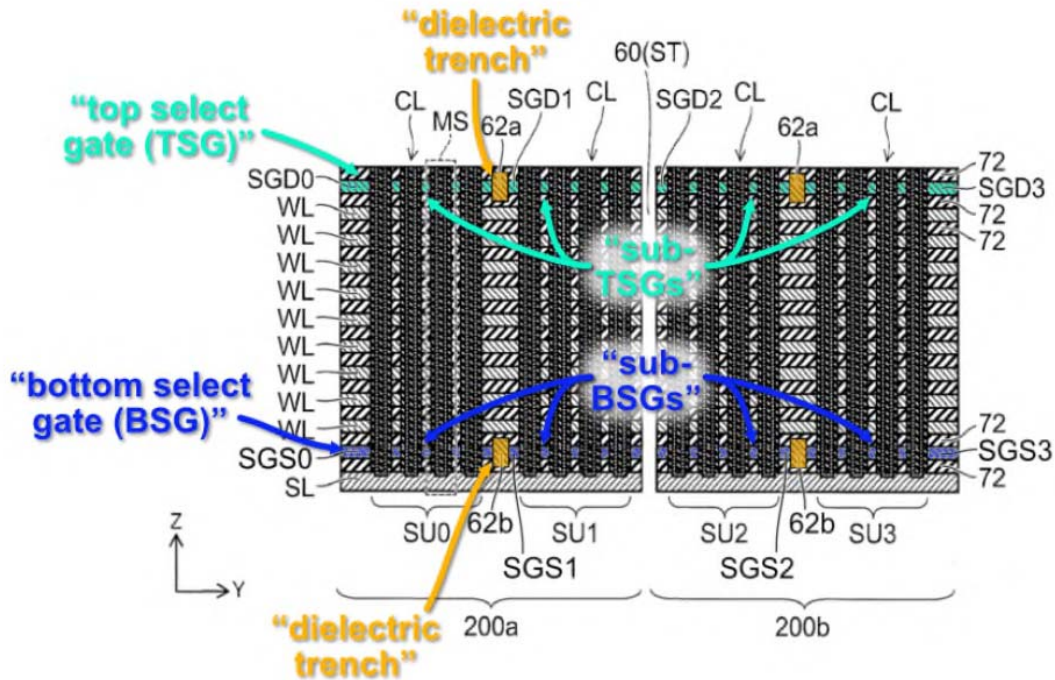


Pet. 65-67 (Petitioner's annotations).¹³ As shown in the above figure, the purported bottom select gate includes three layers: "SGS0A," "SGS1A," and "SGSB." Shibata's three lower source-side select gates provide selective connection of the four string units SU0-SU3 to the source layer without relying on a dielectric trench.

¹³ Note that Shibata uses the acronym "SL" to refer to "source layer," Shibata's purported substrate, whereas Park uses the same acronym, SL, to refer to "sacrificial layer."

See Shibata, Fig. 16, Fig. 22A, [0196]-[0218]. For the purposes of limitation [1.e], which recites “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” Petitioner further relies on Shibata’s teachings of “separation portions.” Pet. 72 (citing Shibata, [0107], [0110]). Shibata, however, teaches that these separation portions “pierce[] only the drain-side select gate layer of the **uppermost** layer of the multiple conductive layers 70”—not the source-side select gate layers, which are the **lowermost** layer(s). Shibata, [0090]. KuhnII, ¶151.

Recognizing this shortcoming of Shibata, Petitioner abandons its mapping of Shibata for limitations [1.b], [1.c], [1.d], and [1.f] and argues for limitation [1.e] that a POSITA would have found it obvious to do two things: (1) rather than dividing just the upper drain-side select gates using separation portions 62a, Shibata would employ “new additional separation portions 62b” to also divide the BSG into sub-BSGs (Pet. 74); and (2) rather than employ multiple lower source-side select gate layers, “Shibata would employ a single ‘bottom select gate (BSG)’” (Pet. 74-75). This proposed modification is illustrated in the Petition’s reimagined diagram:



Pet. 76 (Petitioner’s demonstrative). KuhnII, ¶¶152-154.

Petitioner’s proposed modifications to Shibata, however, rely upon the flawed premise that Park provides an alternative to Shibata’s multiple bottom select gates, which “facilitate control on a string unit basis” and thus would motivate the changes. Pet. 74-75. Specifically, Petitioner points to Park’s isolation insulating layers 111 that purportedly “divide[] a single lower gate layer into multiple portions.” Pet. 75 (citations omitted). But Petitioner’s obviousness argument fails for several reasons. KuhnII, ¶155.

First, Petitioner’s obviousness analysis is fraught with flawed premises and conclusory arguments, and ultimately succumbs to reliance on impermissible hindsight. For example, Petitioner’s primary motivation is that “[w]hile the multiple

bottom select gates can facilitate control on a string unit basis, a POSITA would have recognized that they require additional manufacturing steps and make Shibata's memory array taller" and that this would have motivated consideration of other design alternatives like Park. Pet. 74-75 (*citing* Ex. 1003, ¶¶ 377-380). Neither Petitioner nor its expert explain how Park achieves a reduction in manufacturing steps, particularly given that etching and replacing portions of the bottom select gate with insulating material would add additional manufacturing steps at the same time that other steps are removed. KuhnII, ¶156.

Second, Petitioner's argument is also flawed because it attempts to equate Park's isolation insulating layers 111 and Shibata's separation portion 62a. As described in greater detail in relation to Ground 1, Park's isolation insulating layers are not extensive trenches that separate the bottom gate structure, but instead are short sections that just "close the gaps in common source lines 105." Pet. 31. Moreover, Park's isolation insulating structures are in an entirely different region of the memory than Shibata's separation portions. As previously discussed, Park's **isolation insulating structures** are short structures in the staircase region, not in the array region:

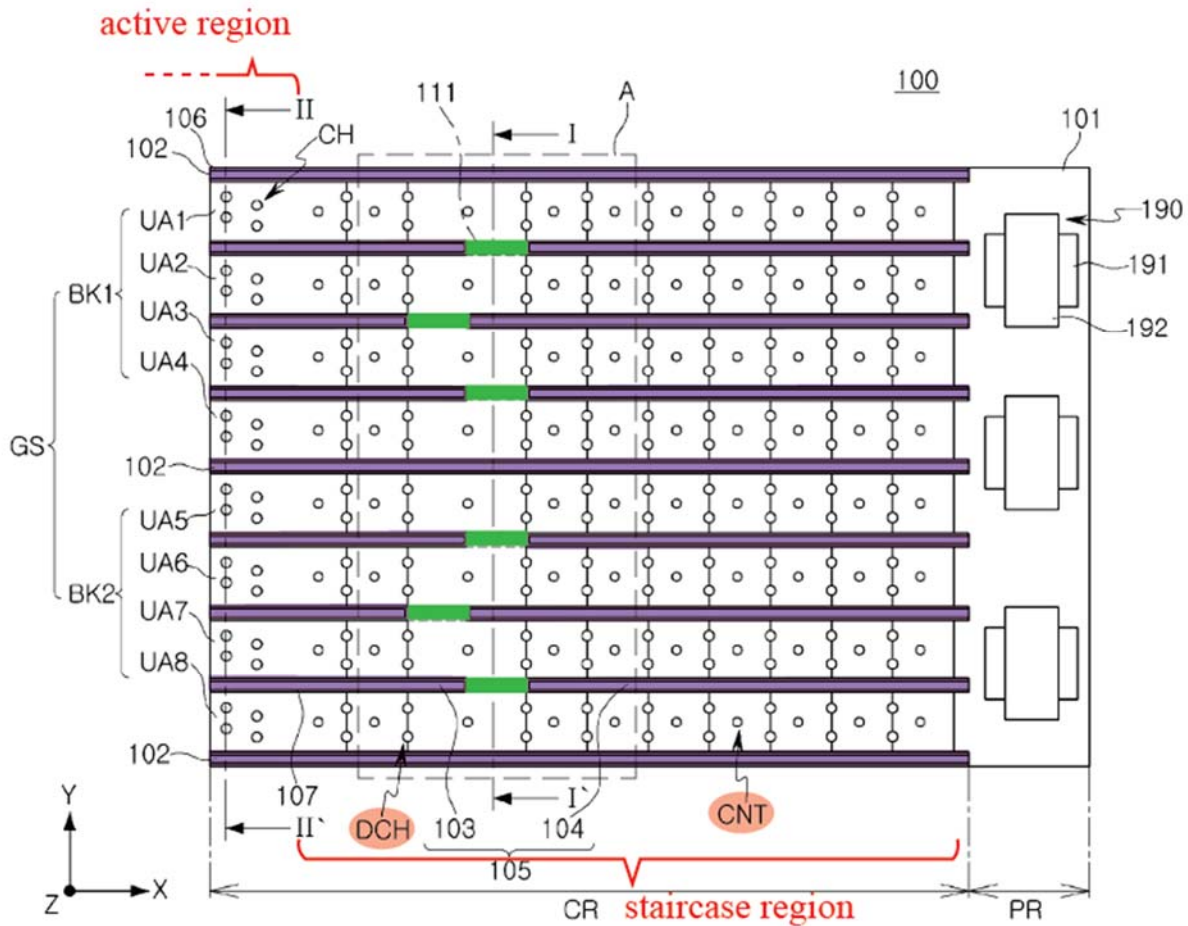


FIG. 3

Park Fig. 3 (showing **isolation insulating structures 111** between dummy channel structures (DCH) and an adjacent contact (CNT) to the word lines in the staircase region, not the active region); *see also* Park, 10:56-60 (“The isolation insulating layer 111 may be disposed below the connecting electrodes 129b to 129i connecting the unit electrodes of the gate electrode layers 120, forming the word lines, to each other.”). On the other hand, Shibata’s **separation portions** extend the length of the array region of the memory device:

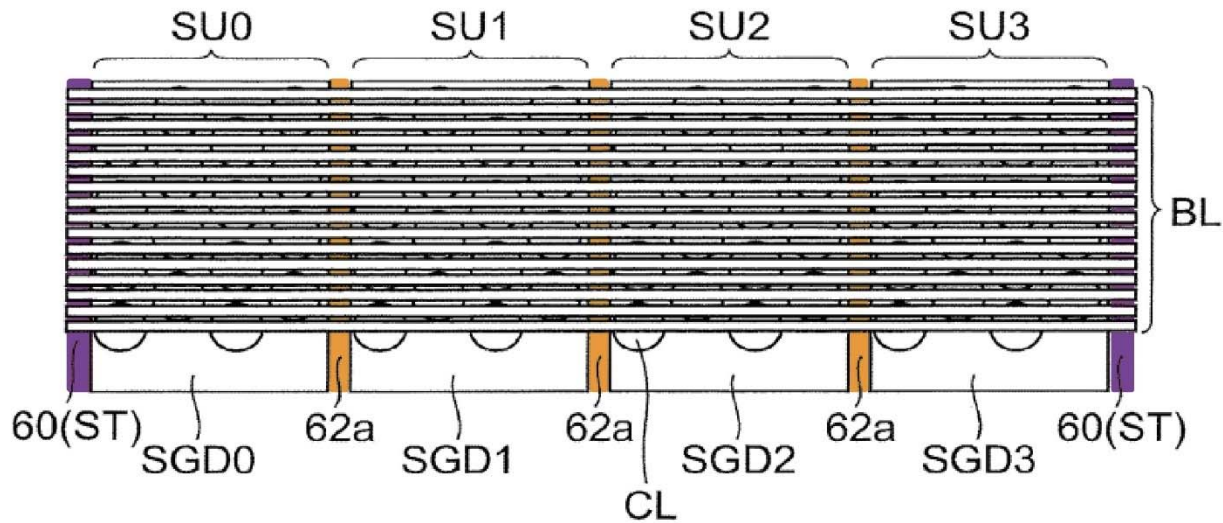


FIG. 47A

Shibata, Fig. 47A. KuhnII, ¶157.

Indeed, as Petitioner admits, “Shibata does not reference a staircase” (Pet. 69), and so even if a POSITA would have recognized that Shibata’s three-layer bottom gate design “require[d] additional manufacturing steps and ma[de] Shibata’s memory array taller” (Pet. 74), that does not mean a POSITA would look to Park’s unrelated teaching directed to short isolation insulating structures 111 in the staircase region—a region Shibata does not even disclose or reference—to modify Shibata. Absent a motivation to apply Park’s teachings, Petitioner’s obviousness argument relies on impermissible hindsight. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”). KuhnII, ¶158.

Third, Petitioner’s argument that “it was well known that trenches of dielectric material could be used to divide select gates” (Pet. 78) also falls flat. Not one of the four references cited by Petitioner shows that it was well known to use trenches to divide both the top and bottom select gate (as set forth by Ground 3). Indeed, three of them do not even disclose using the purported dielectric trenches in the bottom select gate. *See* Ex. 1016, 6:5-15, 10:15-18, Fig. 4A (employing a “insulating layer 173” in the “uppermost gate electrode layer 136”); Ex. 1017, 7:40-42, Fig. 3 (“employing a “cutting insulation pattern 118” in the upper “string selection gate electrodes 202.”); Ex. 1018, [0058], Fig. 4B (employing “insulating separation pattern 50” in the “upper electrodes ELb located at the highest level”). As for the fourth reference, it discloses, at best, similar isolation insulating regions as Park, which are no more than short sections in the staircase region. *See* Ex. 1019, Figs. 21-22, Fig. 24, [0154], [0160]-[0161]. As such, none of the references cited by Petitioner or Petitioner’s expert provides motivation to modify Shibata’s separation portions to divide both upper drain-side select gates and lower source-side select gates. As the Board determined, “the cited references appear to show no more than that described by Shibata or Park, and that Petitioner does not show that it was well known in the art to separate a BSG as set forth in claim 1.” DI 24. KuhnII, ¶159.

Lastly, Petitioner’s conclusory argument that the proposed combination “would reduce the number of needed manufacturing steps” is unsupported by the

evidence. Pet. 77. Once again, the only support cited by Petitioner is a near-identical statement by its expert. Neither Petitioner nor its expert cite any evidence. Indeed, on the face of it, the statement is wrong. The proposed combination, which requires the formation of additional separation regions 62b in the source-side gate layer, would at minimum require additional photolithography steps, etching steps, and filling procedures that neither Petitioner nor its expert considered. KuhnII, ¶160. For example, Shibata teaches forming a simple stacked structure for the bottom of the stack:

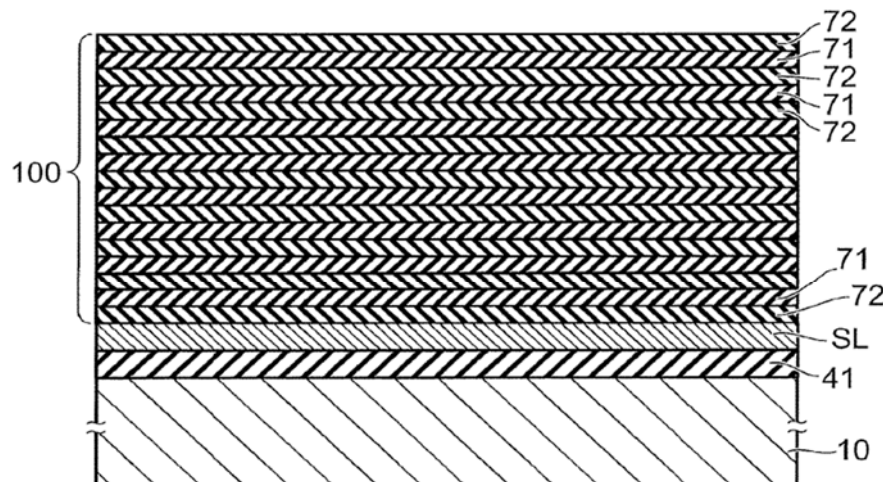


FIG. 8A

Shibata, [0104], Fig. 8A. To modify Shibata to include separation regions to divide the alleged BSG at the bottom of the stack, the formation of the stacked body 100 would have to be disrupted to, at minimum, (1) form a mask, (2) form slits by etching, and (3) form insulating material into the slits. Thus, contrary to Petitioner's

conclusory assertion, Petitioner's combination would actually increase the number of manufacturing steps. KuhnII, ¶160.

As the above reasons demonstrate, modifying Shibata to have a single-layer BSG results in significant complexity and would have further dissuaded a POSITA from applying Park's teachings to the memory device, let alone with a reasonable expectation of success. KuhnII, ¶161.

Thus, Petitioner fails to show that a POSITA would have been motivated to modify Park in view of Shibata. KuhnII, ¶162.

B. Claims 10-11: Shibata in View of Park Also Does Not Render Obvious These Claims

Petitioner relies on Park's teaching of an alleged trench in the alleged BSG and TSG for these elements and its analysis is similar to its analysis of Park Ground 1 (Park), and therefore these elements are not met for the same reasons discuss for Ground 1. KuhnII, ¶163.

X. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the '623 are anticipated or obvious. KuhnII, ¶¶164-166. Accordingly, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.

Dated: January 17, 2025

Respectfully submitted,

ROPES & GRAY LLP

By: /James L. Davis, Jr./

James L. Davis, Jr.

Reg. No. 57,325

ROPES & GRAY LLP

1900 University Avenue, 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650-617-4794

James.L.Davis@ropesgray.com

Andrew T. Radsch

(*pro hac vice* forthcoming)

ROPES & GRAY LLP

1900 University Ave., 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650-617-4011

Andrew.Radsch@ropesgray.com

Christopher M. Bonny

Reg. No. 63,307

ROPES & GRAY LLP

1900 University Ave., 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650-617-4011

Christopher.Bonny@ropesgray.com

Allen S. Cross

Reg. No. 74,729

ROPES & GRAY LLP

2099 Pennsylvania Avenue, NW

Washington, D.C. 20006-6807

Phone: 202-508-4708

Allen.Cross@ropesgray.com

Attorneys for Patent Owner, Yangtze Memory Technologies Co. Ltd.

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE under 37 C.F.R. § 42.120 complies with the type-volume limitation in 37 C.F.R. § 42.24(a)-(b). According to the word-processing system's word count, the brief contains 13,954 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: January 17, 2025

Respectfully submitted,

By: /James L. Davis, Jr./
James L. Davis, Jr.
Reg. No. 57,325
ROPES & GRAY LLP

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

Lead Counsel	Back-up Counsel
K. Patrick Herman Registration No. 75,018 (pherman@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 51 West 52nd Street New York, NY 10019 T: 212-506-5000; F: 212-506-5151 P52PTABDocket@orrick.com PTABDocketJL2@orrick.com PTABDocketJ3B3@orrick.com micron-ymtc_ohs@orrick.com	Jeremy Jason Lang Registration No. 73,604 (jlang@orrick.com) Jared Bobrow <i>Pro Hac Vice</i> (jbobrow@orrick.com)
<i>Counsel for Petitioner Micron Technology, Inc.</i>	

Dated: January 17, 2025

By: /Jonathan Bradford/
Name: Jonathan Bradford

ROPES & GRAY LLP