

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00794
Patent 10,950,623

**DECLARATION OF KELIN KUHN, Ph.D. IN SUPPORT OF PATENT
OWNER'S RESPONSE**

Executed this 17th day of January, 2025 in Winthrop, Washington.

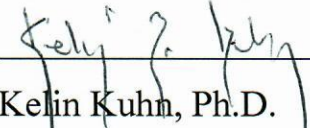

Kelin Kuhn, Ph.D.

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	QUALIFICATIONS	2
III.	MY ASSIGNMENT AND BASES OF OPINIONS	7
IV.	SUMMARY OF MY OPINIONS	9
V.	APPLICABLE LEGAL STANDARDS	12
A.	Claim Construction.....	12
B.	Anticipation	13
C.	Obviousness.....	13
D.	Claim Dependency	15
VI.	THE '623 PATENT	16
A.	Overview of the '623 Patent.....	16
B.	Listing of the Challenged Claims.....	23
C.	File History of the '623 Patent	25
VII.	LEVEL OF ORDINARY SKILL IN THE ART	26
VIII.	CLAIM CONSTRUCTION FOR THE '623 PATENT	28
A.	“formed in the BSG” (Claim 1).....	28
B.	“one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” (Claim 1)	31
C.	“one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” (Claim 1)	36
IX.	THE ASSERTED PRIOR ART	36
A.	U.S. Patent No. 10,559,583 (“Park,” Ex. 1004).....	36
B.	U.S. Patent Pub No. 2019/0122734 (“Shibata,” Ex. 1005).....	44
X.	PETITIONER’S GROUND 1: PARK DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-11	49
A.	Independent Claim 1: Park Does Not Disclose or Render Obvious Multiple Requirements of Limitation [1.e]	50

(a)	Park’s Isolation Insulating Layers Are Not “Dielectric Trenches Formed in the BSG” (Limitation [1.e]).....	51
(b)	Park’s Isolation Insulating Layers Do Not “Extend[] in a Length Direction of the Substrate to Separate the BSG Into a Plurality of Sub-BSGs” (Limitation [1.e])	53
B.	Claim 2: Park Does Not Disclose or Render Obvious “One or More Second Dielectric Trenches Formed in the TSG and Extending in the Length Direction of the Substrate to Separate the TSG into a Plurality of Sub-TSGs”	58
C.	Claim 3: Park Does Not Disclose or Render Obvious “the First Dielectric Trenches and the Second Dielectric Trenches Are Aligned with Each Other in a Width Direction of the Substrate”	67
D.	Claim 10: Park Does Not Disclose or Render Obvious “One or More Dummy BSGs That Are Formed Between the Plurality of Word Lines and the BSG, Separated by the One or More First Dielectric Trenches into a Plurality of Dummy Sub-BSGs”	68
E.	Claim 11: Park Does Not Disclose “One or More Dummy TSGs That Are Formed Between the Plurality of Word Lines and the TSG, Separated by the One or More Second Dielectric Trenches into a Plurality of Dummy Sub-TSGs”	72
XI.	PETITIONER’S GROUND 2: PARK IN VIEW OF SHIBATA DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-11.....	74
A.	Independent Claim 1: The Combination of Park and Shibata Does Not Render Obvious Limitation [1.e]	75
(a)	Shibata’s Separation Portions Are Not “Formed in the BSG” and Do Not “Extend[] in a Length Direction of the Substrate to Separate the BSG Into a Plurality of Sub-BSGs” (Limitation [1.e])	75
(b)	A POSITA Would Not Have Been Motivated to Apply Shibata’s Teachings to Park.....	80
B.	Claims 10-11: Park in View of Shibata Also Does Not Render Obvious These Claims	89
XII.	PETITIONER’S GROUND 3: PETITIONER FAILS TO SHOW THAT SHIBATA IN VIEW OF PARK DISCLOSES OR RENDERS OBVIOUS CLAIMS 1-11	89

A.	Independent Claim 1: Petitioner Fails to Show That a POSITA Would Have Been Motivated to Apply Park’s Teachings to Divide Shibata’s Lower Gate Layer into Multiple Portions	90
C.	Claims 10-11: Shibata in View of Park Also Does Not Render Obvious These Claims	100
II.	CONCLUSION.....	100

I, Kelin Kuhn, Ph.D., hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Yangtze Memory Technologies Company, LTD (“YMTC”) in the above captioned *inter partes* review of U.S. Patent No. 10,950,623 (Ex. 1001, “’632 patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’623 patent (“Petition”) and the April 11, 2024 Declaration of Dr. Jack Lee (Ex. 1003). The arguments raised in Dr. Lee’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Lee’s declaration, and vice-versa. As explained in Sections X-XII (discussing the Grounds raised in the Petition), the invalidity arguments raised in the Petition do not show that the prior art anticipates or renders obvious any of the Challenged Claims, and the arguments raised in Dr. Lee’s declaration are insufficient for similar reasons.

2. I am being compensated for my time at my usual consulting rate of \$600 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with

Patent Owner (“PO”) in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

3. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. QUALIFICATIONS

4. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

5. I received my B.S., magna cum laude, in Electrical Engineering from the University of Washington, Seattle in 1980, and received an M.S. and a Ph.D. in Electrical Engineering from Stanford University in 1985. I undertook post-doctoral work at Stanford from 1985 to 1987.

6. I am presently retired from industry. However, I still periodically engage in engineering projects for select clients and have a small business (Confluence Technology Services) to support that activity.

7. I am also currently an adjunct professor of Materials Science and Engineering at Cornell University, where my research interests are in the areas of quantum materials, post-CMOS technology, and spintronics.

8. For nearly a decade, beginning in 1987, I held faculty positions at the University of Washington, Seattle, beginning as a Research Assistant Professor in Material Science and Engineering, then as Assistant Professor in Electrical and Computer Engineering, and finally as a tenured Associate Professor of Electrical and Computer Engineering. During this period, I worked in III-V molecular beam epitaxy and optoelectronics, and was awarded the University's highest accolade for a faculty member, the Distinguished Teaching Award, in 1995.

9. In 1997, I joined Intel Corporation ("Intel") at the Aloha Campus in Oregon as a Senior Process Engineer. I focused on front-end integration on the Intel 0.35 μ m process technology. In this role, I was responsible for the silicide section of the process flow, interaction with the reliability community, and integration on the CMOS camera chip project.

10. In 1999, I was transferred to Portland Technology Development at Ronler Acres, Oregon, as a Senior Process Engineer. I worked on front-end integration on the 130 nm CMOS generation. In this role, I was responsible for the isolation section of the process flow as well as integration of Optical Proximity Correction technologies into 130 nm.

11. In 2001, I advanced to the title of Principal Engineer. In 2002, I was promoted to the role of Process Program Manager for Intel's 90 nm communications process technology. Over a three-year period, my team developed a derivative

analog/RF technology (including a SiGe bipolar junction transistor (“BJT”)) on top of Intel’s premium 90 nm microprocessor process.

12. In 2004, I advanced to the title of Senior Principal Engineer and was promoted to the role of Device Technology Manager of the pathfinding team at Intel that was responsible for the high-k metal-gate transistor architecture of Intel’s 45 nm microprocessor processor technology. I received an Intel Achievement Award in 2006 for my work on the high-k metal gate.

13. In 2007, I achieved the title of Intel Fellow and became Director of Advanced Device Technology. Fellow is the highest level of technical achievement within Intel, with approximately 50 Fellows among approximately 100,000 total employees. My work evolved to a strategic role in overseeing the transition of advanced device technologies from research into development. In this role, I played an active part in the transfer of transistor technology for the 32 nm node, 22 nm node, and 14 nm node (the last two nodes involving Intel’s FinFET device). I received a second Intel achievement award in 2008 for my work on Intel’s FinFET device.

14. In 2009, my title remained the same, but my role transitioned from development (in Portland Technology Development, at Ronler Acres) to research (in the Components Research Group, still at Ronler Acres). From 2009 until my retirement from Intel in 2014, I researched advanced device architectures for Intel processes in the five-to-ten year time frame.

15. While much of my later work at Intel still remains confidential, certain aspects of my work during this period are featured in my book CMOS And Beyond: Logic Switches for Terascale Integrated Circuits (Co-Editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015), as well as in my paper “Considerations for Ultimate CMOS Scaling” (IEEE Trans. on Elec. Dev., Vol. 59, No. 7, 2012), winner of the 2013 Paul Rappaport Award.

16. Since my retirement in 2014, my consulting work has included a variety of semiconductor related projects. While the detailed technical content is, of course, protected by client confidentiality, these projects include, FinFETs, vertical power transistors, solar cells, conventional (planar) MOS, and flash.

17. I am the author of more than 100 technical papers in electronics and photonics. I am currently the Associate Editor in Chief (AEiC) of IEEE Electron Device Letters, having served as an editor since 2015, and as AEiC since 2024.

18. A few of my other representative journal publications include: “Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results,” (Symposium on VLSI Technology, 2012); “Process Technology Variation,” (IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011); “A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging,” (2007 IEEE International Electron Devices Meeting); and “Comparison

of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm,” (IEEE Electron Device Letters, Vol. 32, No. 9, 2011).

19. A few representative book chapters include, “The Magic of MOSFET Manufacturing”, Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8. Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616).

20. I am an inventor on approximately 80 granted U.S. patents in the field of semiconductor technology.

21. A few of my other relevant honors include being a Fellow at the Institute of Electrical and Electronics Engineers (“IEEE”), a recipient of the IEEE Frederik Philips Award (2016), a recipient of the IEEE Paul Rappaport Award (2013), the recipient of eleven Intel Divisional Awards, and election to the National Academy of Engineering (2023). Earlier in my career, I received the NSF Presidential Young Investigator Award.

22. As specifically relevant to this project, I want to highlight the 3’D gate-last vertical gate-all-around (GAA) devices and the 3’D vertical GAA arrays that are discussed at some length in “Considerations for Ultimate CMOS Scaling” (see Fig. 15 in particular). I also want to highlight on-going proprietary and confidential

work, in the matter of Silicon Storage Technology, Inc. vs. Taiwan Semiconductor Manufacturing Company involving flash.

23. Attached as Exhibit 1 to this report is a current copy of my curriculum vitae, which outlines my academic, professional and experiential qualifications in the semiconductor and integrated circuit industries, as well as a list of publications I have authored and co-authored and presentations I have given.

III. MY ASSIGNMENT AND BASES OF OPINIONS

24. I have been asked to provide my opinions as to the scope and content of the '623 patent as well as the prior art presented by Petitioner and Dr. Lee in the Petition. Specifically, I have been asked to opine on what a person of ordinary skill in the art would have understood the '623 patent to disclose, and I have been asked to provide my opinions concerning whether Park (Ex. 1004), Park in view of Shibata (Ex. 1005), or Shibata in view of Park discloses or renders obvious claims 1-11 of the '623 patent.

25. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited in the Petition, Preliminary Response, and herein including those listed below:

Exhibit No.	Reference
N/A	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,950,623 (IPR2024-00794, Paper 1)
Ex. 1001	U.S. Patent No. 10,950,623 B2 to Song et al.
Ex. 1002	File History of U.S. Patent No. 10,950,623 B2 to Liu et al.
Ex. 1003	Declaration of Dr. Jack Lee ("Lee")

Ex. 1004	U.S. Patent No. 9,299,718 B2 to Park et al. (“Park”)
Ex. 1005	U.S. Patent Publ. No. 2019/0122734 A1 to Shibata et al. (“Shibata”)
Ex. 1006	Aritome, “NAND Flash Memory Technologies” (2016)
Ex. 1007	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
Ex. 1008	U.S. Patent Publ. No. 2015/0162084 A1 to Morooka et al.
Ex. 1009	U.S. Patent Publ. No. 2015/0255478 A1 to Tanzawa
Ex. 1010	U.S. Patent No. 9,589,978 to Yip
Ex. 1011	U.S. Patent Publ. No. 2017/0062337 A1 to Park et al.
Ex. 1012	Micheloni et al., “Inside Solid State Drives (SSDs)”
Ex. 1016	U.S. Patent No. 10,355,010 B2 to You et al.
Ex. 1017	U.S. Patent No. 9,299,718 B2 to Park et al.
Ex. 1018	U.S. Patent Publ. No. 2019/0035798 A1 to Hwang et al.
Ex. 1019	U.S. Patent Publ. No. 2015/0137216 A1 to Lee et al.
Ex. 1021	U.S. Patent Pub. 2019/0214404 A1 to Ahn et al.
Ex. 1023	U.S. Patent No. 8,945,996 to Tang et al.
N/A	Patent Owner’s Preliminary Response (IPR2024-00794, Paper 8)
Ex. 2001	Cho et al., “A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single-Level Modes,” IEEE J. of Solid-State Circuits, Vol. 36, No. 11, November 2001.
Ex. 2002	Lee et al., “Applications of AFM in semiconductor R&D and manufacturing at 45 nm technology node and beyond,” Metrology, Inspection, and Process Control for Microlithography, Vol. 7272, SPIE, 2009.
Ex. 2003	Xiao et al., “A high speed low power negative sensing architecture for 3D NAND Flash memory,” 2016 China Semiconductor Technology International Conference (CSTIC), Shanghai, China, 2016.
Ex. 2004	Bergonzoni, et al., “Reset Current Scaling in Phase-Change Memory Cells: Modeling and Experiments,” IEEE Transactions on Electron Devices, Vol. 59, No. 2, 283-291, Feb. 2012.
Ex. 2005	Seshan et al., Handbook of Thin Film Deposition, Abstract, 2018.
Ex. 2006	Choi et al., “Novel ESD protection transistor including SiGe buried layer to reduce local temperature overheating,” IEEE Transactions on Electron Devices, Vol. 43, No. 3, 479-489, March 1996.
N/A	Decision Granting Institution of <i>Inter Partes Review</i> of U.S. Patent No. 10,950,623 (IPR2024-00794, Paper 9)

26. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

27. All emphases (such as bolding, underlying, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. SUMMARY OF MY OPINIONS

28. It is my opinion that Park does not disclose or render obvious claims 1-11 of the '623 patent at least because:

- Park does not disclose or render obvious “one or more first dielectric trenches formed in the BSG,” as required by independent claim 1 (from which claims 2-11 depend).
- Park does not disclose or render obvious “one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” as required by claim 1.
- Park does not disclose or render obvious “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.” as required by claim 2.

- Park does not disclose or render obvious “the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate,” as required by claim 3.
- Park does not disclose or render obvious “one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs,” as required by claim 10.
- Park does not disclose or render obvious “one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs,” as required by claim 11.

29. It is my opinion that Park in view of Shibata does not render obvious claims 1-11 of the '623 patent at least because:

- Park in view of Shibata does not render obvious “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” as required by claim 1.

- A POSITA would not have applied Shibata's teachings to Park to elongate the isolation insulating layers.
- Park in view of Shibata does not render obvious "one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs," as required by claim 10.
- Park in view of Shibata does not render obvious "one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs," as required by claim 11.

30. It is my opinion that Shibata in view of Park does not disclose or render obvious claims 1-11 of the '623 patent at least because:

- A POSITA would not have been motivated to apply Park's teachings to divide Shibata's lower gate layer into multiple portions.
- Shibata in view of Park does not render obvious "one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs," as required by claim 10.

- Shibata in view of Park does not render obvious “one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs,” as required by claim 11.

V. APPLICABLE LEGAL STANDARDS

31. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

A. Claim Construction

32. I was informed, unless otherwise noted, I should give claim terms their ordinary and customary meaning as understood by a person of skill in the art at the time of the invention. I was informed and I understand that the words of the patent’s claims and the context in which the term is used in the claims can be highly instructive in ascertaining the term’s meaning. I further understand that the terms of a claim are to be interpreted in the context of the entire patent, including the patent’s other claims, its specification and its figures.

33. I have been further instructed that a patent’s “prosecution history” may often provide helpful evidence about how the Patent Office and the applicant understood the patent and its claims. Therefore, I have been instructed that claim terms should also be interpreted in light of the patent’s prosecution history. In

addition to the claims, the specification, the figures, and the prosecution history, I have been instructed that certain “extrinsic evidence” such as scientific or technical references may also help inform the way in which the person of ordinary skill in the art might understand the claim term. I have been instructed that extrinsic evidence must always be considered in the context of the intrinsic evidence.

B. Anticipation

34. I have been informed by counsel that a patent claim is invalid as anticipated if each element of that claim is present either explicitly or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or possibly contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

C. Obviousness

35. I understand that a claim is unpatentable if it would have been obvious to a person of ordinary skill in the art at the time the invention was made. I understand that a claim could have been obvious from a single prior art reference or from a combination of two or more prior art references. I understand that an obviousness analysis requires an understanding of the scope and content of the prior

art, any differences between the invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

36. I further understand that a claim would have been obvious if it unites old elements with no change to their respective functions or alters prior art by mere substitution of one element for another known in the field, and that combination yields predictable results. Also, I understand that obviousness does not require physical combination or bodily incorporation, but rather consideration of what the combined teachings would have suggested to persons of ordinary skill in the art at the time of the invention.

37. While it may be helpful to identify a reason for this combination, I understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious. I understand that a claim would have been obvious if a person of ordinary skill in the art would have had

reason to combine multiple prior art references or add missing features to reproduce the invention recited in the claims.

38. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the invention, the failure of others to make the invention, praise of the invention by those having ordinary skill in the art, and copying of the invention by others in the field. I understand that there must be a nexus, that is, a connection, between any such secondary considerations and the invention.

39. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

D. Claim Dependency

40. I understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the

limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

VI. THE '623 PATENT

A. Overview of the '623 Patent

41. The claimed invention of the '623 is directed to an improved “3D [three-dimensional] memory device with a divided block structure” that provides a novel approach to address issues—such as “longer erasing time, longer data transfer time, and lower storage efficiency”—associated with conventional architectural memory device designs containing a “shared BSG [bottom select gate]” architecture. '623, 1:33-35, 1:57-60.

42. 3D NAND flash memory technology architecture has been developed such that “the vertical NAND memory cell strings of a same block” share a bottom select gate (BSG). '623, 1:50-52. The shared BSG “controls all of the BSTs [bottom select transistors] or vertical NAND memory cell strings in [a] block simultaneously” during operation of the memory device. '623, 1:53-57. However, as the number of vertical layers and bit density increases, “the shared BSG can induce longer erasing time, longer data transfer time, and lower storage efficiency.” '623, 1:57-60.

43. The claimed invention of the '623 overcomes these device performance issues by introducing a novel 3D NAND memory device architecture that separates the memory cell blocks into a plurality of sub-blocks. '623, 1:61-62. This

architecture “divid[es] the shared BSG into a plurality of sub-BSGs,” so that each of the sub-blocks “can be operated individually through controlling the respective sub-BSG.” ’623, 1:61-67. Figure 1A, color-annotated below, shows a cross-sectional view of the ’623’s device with substrate 10:

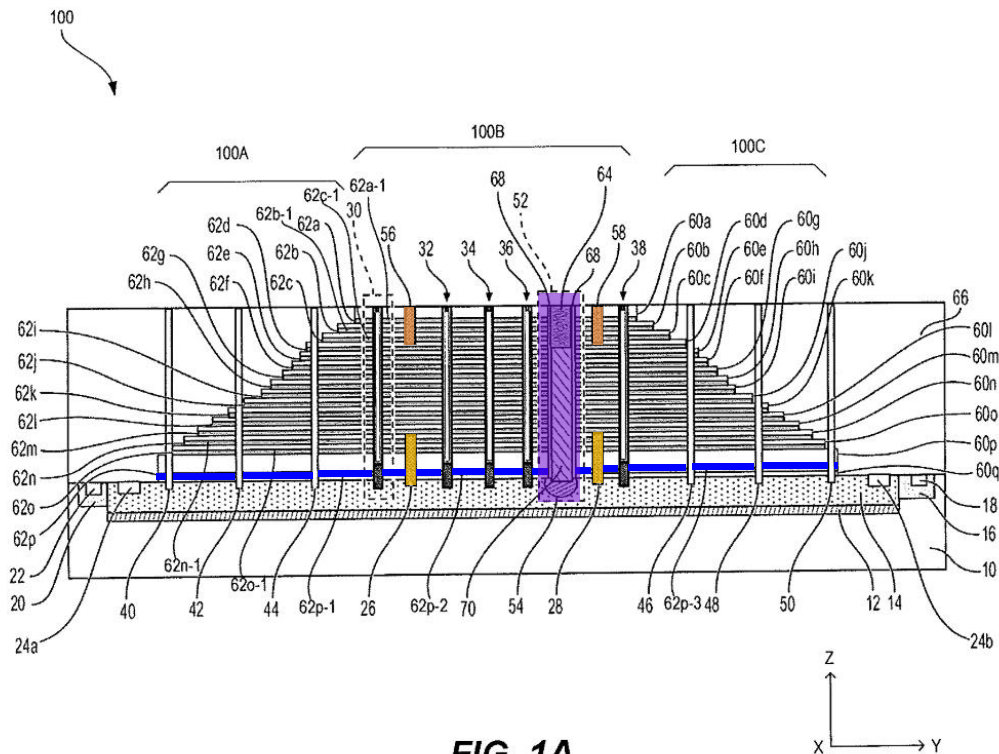


FIG. 1A

’623, Fig. 1A, 5:40-48. A **bottom select gate (BSG) 62p**, a “plurality of word lines (e.g., 62d-62m),” and a top select gate (TSG) 62a are “disposed sequentially over the substrate” (’623, 6:44-49). During this process, “a plurality of insulating layers” (insulating layers 60) are disposed between each of the layers that will form the BSG, word lines, and TSG. ’623, 6:49-54. The **BSG**, word lines, and insulating layers 60

are “alternatively stacked over the substrate 10 with a staircase configuration.” ’623, 6:55-61.

44. After the BSG is formed, the ’623 teaches that “by introducing the first [] trenches into the memory device 100, the BSG [is] separated into a plurality of sub-BSGs.” ’623, 7:45-47. Specifically, “one or more first dielectric trenches (or first trenches), such as two **first trenches 26 and 28**, are formed in the one or more BSGs (e.g., 62p),” with the “**first trenches 26 and 28** extend[ing] in an X-direction (i.e., length direction) of the substrate 10 to separate the **BSG 62p**” into “a plurality of sub-BSGs.” ’623, 7:17-24.

45. Forming the first trenches in the BSG rather than a sacrificial layer introduces significant advantages. **First**, when the trenches are formed in a sacrificial layer, forming trenches that are close to each other risks jeopardizing the gate replacement process. As I discuss further below in §X.A.(b), extensive trenches that are close to each other may block the passage of etchants, sacrificial materials that are removed, and gate materials. These concerns are not present when the trenches are formed in the existing BSG rather than a sacrificial layer, and as a result, a BSG can be divided into more sub-BSGs. This helps achieve the benefit of the ’623 invention, i.e., separating each of the blocks into a plurality of sub-blocks and improving speed, efficiency and control, while improving structural integrity. ’623, 1:57-2:7, 22:63-23:33.

46. **Second**, by forming the trenches in the existing BSG, it is possible to divide the BSG into sub-BSGs using trenches that extend the length of the array. In contrast, forming a long trench in the sacrificial layer before the gate replacement process that leads to the formation of the BSG could have the aforementioned issues. As a result, other, more complicated ways of separating a BSG into a plurality of sub-BSGs may be required. For example, Park teaches patterning isolation regions and combining them with common source lines. Forming the trenches in the BSG allows for a simpler and more robust manufacturing process to achieve the '623's goals.

47. **Third**, forming the trenches in the existing BSG removes the need to use a gate replacement process. Although a common method, gate replacement process has several disadvantages, such as the risk of structural collapse due to surface tension and vacuum forces, particularly in the staircase region where there are not as many structures to provide support, jeopardizing structural integrity. Gate replacement also adds manufacturing steps, which may increase manufacturing time and cost.

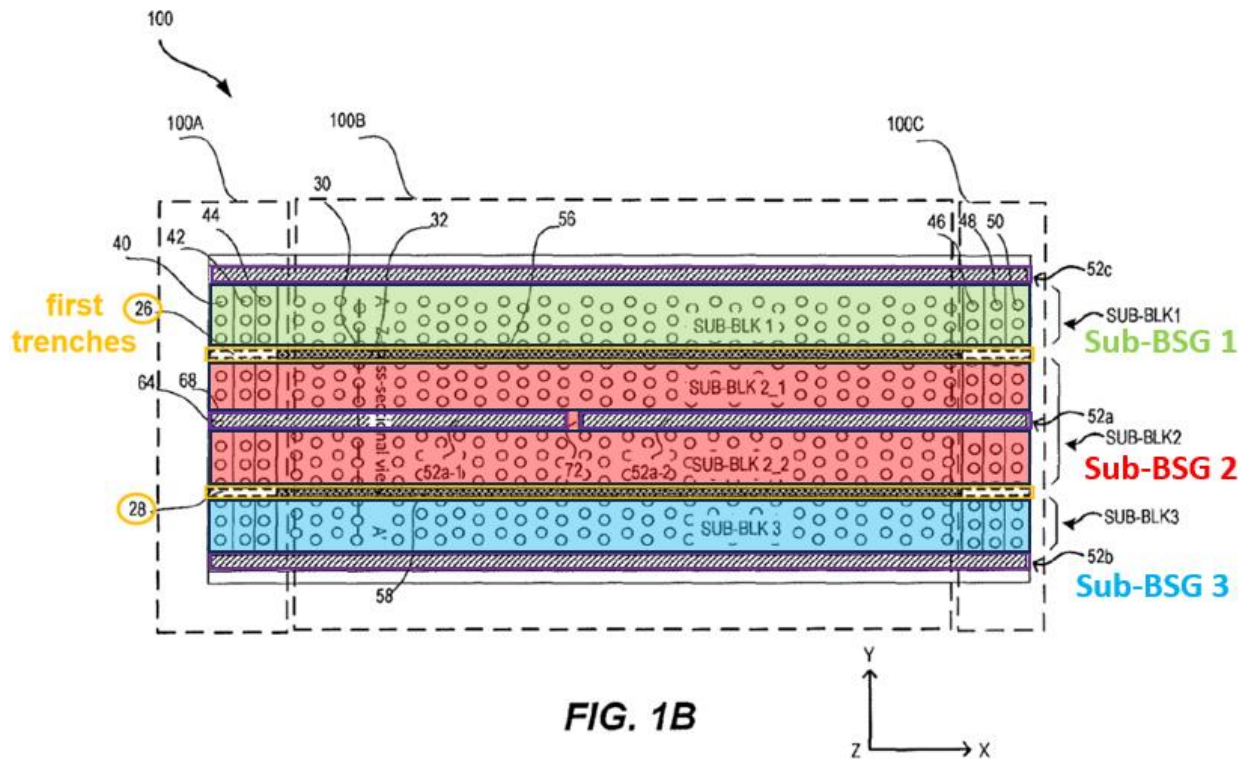
48. As depicted in Figure 1A, the dielectric trenches also extend in a Z-direction, traversing multiple conductive and insulation layers. After the TSG is formed, corresponding **second trenches 56 and 58** are “formed in the one or more TSGs (e.g., 62a).” '623, 7:26-29. The dielectric trenches are filled with “suitable

dielectric materials,” such as silicon dioxide (SiO_2), silicon oxynitride (SiON), and silicon oxycarbonitride (SiOCN). ’623, 7:42. Dividing the TSG in this manner (by forming a trench(es) in the TSG) offers many of the same advantages as for a BSG discussed above. The specification further explains: “In the disclosed 3D-NAND memory device, the each of sub-blocks can also have a respective sub-top select gate (sub-TSG) by dividing a shared/common TSG into a plurality of sub-TSGs through one or more second dielectric trenches. Each of the sub-TSGs can control a respective sub-block during a reading/programming operation. In some embodiments, the first and second dielectric trenches can be formed via a same reticle set so that a manufacturing cost can be reduced.” ’623, 2:8-16; see also 23:26-33.

49. The sub-BSGs “divide the memory device 100 into a plurality of sub-blocks,” or, in other words, “a plurality of cell strings,” and “each of the sub-blocks can be operated individually through controlling the respective sub-BSG.” ’623, 7:47-53. As such, the ’623’s memory device “can precisely control a desired sub-block/array region so as to effectively reduce a programming time, a reading time, an erasing time and data transfer time, and significantly improve data storage efficiency.” ’623, 7:53-58. Accordingly, the claimed memory device architecture of the ’623 overcomes shortcomings of the prior art.

50. The '623 further teaches that the memory device includes “one or more common source regions (CSRs), such as one **common source region 52**,” which is “formed over the substrate” and “extend[s] in the X-direction (length direction) of the substrate.” '623, 7:59-62. The CSR “passes through the BSG 62p,” “the plurality of word lines 62d-62m,” as well as “the plurality of insulating layers 60,” among other layers. '623, 7:62-66. Moreover, the CSR “is electrically coupled with the substrate 10 via a doped region 54.” '623, 7:66-67.

51. The '623 distinguishes the **first trenches** and **second trenches**, which divide the BSG and TSG into sub-BSGs and sub-TSGs, from the **common source region**, which does not divide the BSG or TSG into sub blocks. Figure 1B, color-annotated below, shows the same memory device of the '623 from a top-down view:



'623, Fig. 1B (annotated), 4:35-37. As illustrated in Figure 1B, three **common source regions, 52a-52c**, “extend along the X-direction (length direction) of the substrate 10.” '623, 8:67-9:2; *see also* '623, Figs. 11B-C. The “**common source region 52a** is separated” “by an H-cut 72 into two sub-CSRs 52a-1 and 52a-2” such that “two portions **SUB-BLK2_1 and SUB-BLK_2** ... are electrically connected with each other through the H-Cut 72.” '623, Fig. 1B, 9:14-18, 9:41-44. The term “H-cut” refers to the “H” shape formed by the process. As illustrated in '623 Figure 1B, the H-cut 72 forms the cross portion of the “H,” which is rotated 90 degrees. Also illustrated in Figure 1B above, are two pairs of trenches: **first trenches 26 and 28** in the BSG, which extend the length of the bottom select gate, and **second**

trenches 56 and 58 which extend the length of the top select gate (for clarity, the second trenches 56 and 58 are not color annotated because they overlay on top of the first trenches, but in a higher layer). As I discuss and show in the figure, **first trenches 26 and 28** “separate the BSG 62p ... into a plurality of sub-BSGs.” ’623, 7:17-26. The **common source regions**, in contrast, do not. The ’623 explains that “[w]ithout the introduction of the **first/second trenches**, the memory device 100 (or the memory cell block 100) has a shared BSG.” ’623, 9:46-49.

B. Listing of the Challenged Claims

52. For reference, claims 1-11 (“Challenged Claims”) of the ’623 Patent are reproduced below:

[1.pre] A memory device, comprising:

[1.a] a substrate;

[1.b] a bottom select gate (BSG) disposed over the substrate;

[1.c] a plurality of word lines positioned over the BSG with a staircase configuration;

[1.d] a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;

[1.e] one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and

[1.f] one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.

[2.pre] The memory device of claim 1, further comprising:

[2.a] a top select gate (TSG) positioned over the plurality of word lines, the TSG and the plurality of word lines being spaced apart by the plurality of insulating layers; and;

[2.b] one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.

[3] The memory device of claim 2, wherein the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate.

[4] The memory device of claim 2, wherein the one or more common source regions further pass through the TSG, and the one or more common source regions, the first dielectric trenches, and the second dielectric trenches extend parallel to each other in the length direction of the substrate.

[5] The memory device of claim 2, further comprising:
a plurality of channel structures formed over the substrate along a height direction of the substrate that is perpendicular to the substrate, wherein each of the plurality of channel structure passes through the BSG, the plurality of word lines, the TSG, and the plurality of insulating layers.

[6] The memory device of claim 1, further comprising:
a plurality of dummy channel structures formed along the a height direction of the substrate that is perpendicular to the substrate, the plurality of dummy channel structures passing through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate.

[7] The memory device of claim 5, further comprising a plurality of memory cell sub-blocks, each of the memory cell sub-blocks including a plurality of respective channel structures that are connected to a same sub-BSG and to a same sub-TSG, each of the memory cell sub-blocks being operated individually.

[8] The memory device of claim 5, wherein the one or more first dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate.

[9] The memory device of claim 5, wherein the one or more second dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate so that a plurality of channel structures are disposed therebetween.

[10] The memory device of claim 1, further comprising one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.

[11] The memory device of claim 2, further comprising one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs, and spaced apart from the plurality of the word lines and the TSG by the plurality of insulating layers.

C. File History of the '623 Patent

53. The '623 issued as a continuation of a foreign patent application, Korean Patent Application No. 10-2016-0091946, filed on July 20, 2016 in the Korean Intellectual Property Office. The claims of the '623 were allowed after consideration of numerous prior art references. Over the course of prosecution, over twenty references were considered by the Examiner. *See, e.g.*, Ex. 1002 (Part 2), 131 (List of References Cited by Examiner, listing three references), 139 (List of References Cited by Applicant on July 31, 2019 and Considered by Examiner, listing nine references), 141 (List of References Cited by Applicant on September 30, 2019 and Considered by Examiner, listing five references), 144 (List of References Cited by Applicant on July 31, 2019 and Considered by Examiner, listing four references),

204 (List of References Cited by Applicant on December 11, 2020 and Considered by Examiner, listing one reference).

54. In a Notice of Allowance dated November 16, 2020, the Examiner stated that the “prior art of record and considered pertinent to the applicant’s disclosures, especially when these limitations are considered within the specific combination claimed, does not teach or fairly disclose[]” the claimed invention. Ex. 1002 (Part 2), 127-130. The ’623 issued on March 16, 2021.

VII. LEVEL OF ORDINARY SKILL IN THE ART

55. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA” (person of ordinary skill in the art) or “POSA,” as of the time of the invention.

56. I have been asked to consider the level of ordinary skill that someone in the field of technology of the ’623 patent would have had at the time the claimed invention disclosed in the ’623 patent was made. In determining the level of ordinary skill in the art, I considered the following: (1) the levels of education and experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology.

57. In my opinion, a person of ordinary skill in the art capable of reading and understanding the claims of the ’623 patent at the time of the invention would

have had at least a bachelor's degree in electrical engineering, computer engineering, or a similar discipline, along with at least 2 years of professional experience with semiconductor memory devices, or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

58. In this case, Dr. Lee has asserted in his declaration that a person of ordinary skill in the art at the time of the invention described in the '623 patent:

would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

Lee, ¶36.

59. In view of my educational background and years of experience, including my many years of experience developing and manufacturing MOS transistors, 3D MOS transistors, monolithic 3D gate-all-around transistors, and memory devices, I both met and exceeded the qualifications of a person of ordinary skill in the art as of the earliest possible priority date of the '623 Patent in July 2016. That is true under both my own definition of a person of ordinary skill in the art, as well as under Dr. Lee's definition, and my opinions as set forth herein are the same regardless of which definition of a person of ordinary skill in the art is applied.

VIII. CLAIM CONSTRUCTION FOR THE '623 PATENT

60. I have been asked to opine on the scope and content of the '623 patent and what a person of ordinary skill in the art would have understood the '623 patent to disclose and teach as it relates to the terms “dielectric trenches formed in the BSG,” “one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” and “one or more second dielectric trenches ... extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.”

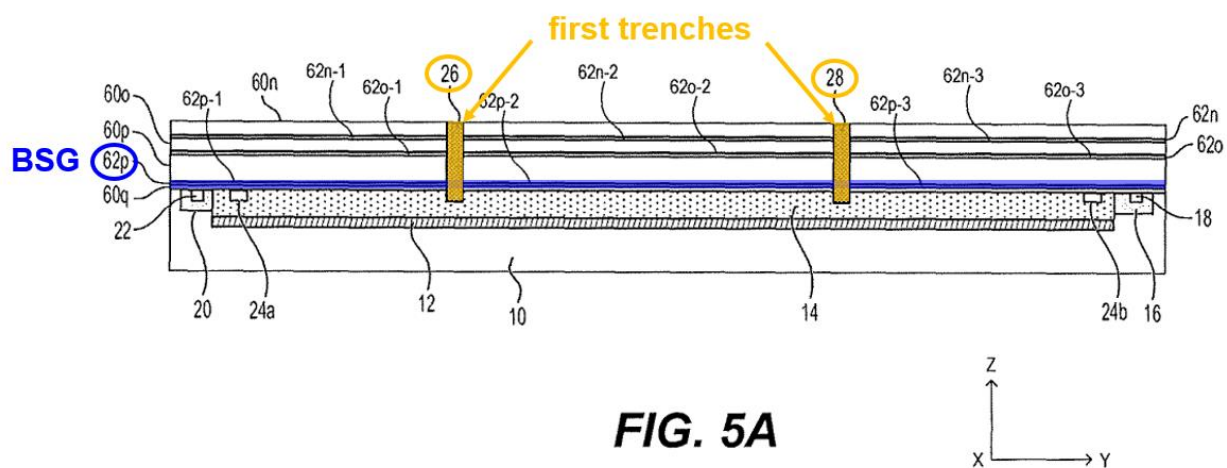
A. “dielectric trenches formed in the BSG” (Claim 1)

61. The term “dielectric trenches formed in the BSG” by its plain meaning does not encompass features that are formed in another structure other than a BSG, such as a sacrificial layer. This interpretation is supported by the plain language of the claims, as well as the specification. In contrast, Petitioner relies on prior art that forms a structure in a sacrificial layer and then argues that it satisfies the “dielectric trenches formed in the BSG” limitation. Pet. 33-34. This does not satisfy the plain and ordinary meaning of the limitation.

62. The claim language recites that the “one or more first dielectric trenches **formed in the BSG**” (bottom select gate)—as opposed to formed in some other type of structure, such as a sacrificial layer. Petitioner’s interpretation eliminates the “BSG” part of the limitation. Moreover, the claim language requires the trench

formed in the BSG to divide the BSG into sub-BSGs—not to divide some other structure into subparts. Moreover, the surrounding claim language confirms that the claim does not encompass dielectric trenches that are formed in another structure other than BSG. The claim requires that the dielectric trenches are “formed in the BSG and extending in a length direction of the substrate **to separate the BSG into a plurality of sub-BSGs,**” which means that there must be an existing BSG such that forming the dielectric trench separates the BSG into a plurality of sub-BSGs.

63. The specification also supports the plain meaning of the claim term. The '623 details the gate-first manufacturing flow ("process 1200") in Fig. 12, which lists, among others, "step 1204 where one or more **BSGs** and one or more dummy BSGs are formed sequentially over a substrate," and "step 1206 [where] one or more **first trenches** are formed in the **BSGs** and dummy BSGs." '623, 21:34-38, 45-46. The state of '623's device after these steps is depicted in Fig. 5A.



'623, Fig. 5A (annotated). As shown in the figure, the trenches are formed in a BSG. The specification, like the claims, also describes the trenches as separating the BSG into a plurality of sub-BSGs, which again confirms that there must be an existing BSG. For example, the '623 discloses "one or more first dielectric trenches (or first trenches), such as two first trenches 26 and 28, are formed in the one or more BSGs (e.g., 62p)," which "extend[] in an X-direction (i.e., length direction) of the substrate 10 to separate the BSG 62p and the dummy BSGs 62n-62o layers into a plurality of sub-BSGs and sub-dummy BSGs, or to say, a plurality of cell strings." '623, 7:17-26.

64. Petitioner cites the '623 section that explains that in the gate-last manufacturing flow the first trenches would be formed in sacrificial layers. Pet. 34. In the cited section, referring to Figure 5A reproduced above, the '623 states that the layer labeled "62p" can be a sacrificial layer. '623, 15:45-48 ("The BSG 62p and the two dummy BSGs 62n-62o can be sacrificial layers that are made of SiN. The sacrificial layers can be removed and replaced with a high K layer and a metal layer in future manufacturing steps."). However, this passage is not saying that a sacrificial layer is a BSG. Rather, it is saying that feature 62p shown in Figure 5, at this stage in the process, can be a sacrificial layer instead of a BSG. Indeed, a POSITA would have understood that a sacrificial layer made of SiN (an insulating material) is not a gate layer and is certainly not a bottom select gate. As an insulator,

it has none of the properties (e.g., conductivity) that would allow it to be used as a BSG. Moreover, as a sacrificial layer, it is not present in the final device. Thus, although the specification discloses a variation that uses a gate-last manufacturing process with a sacrificial layer, this variation is not claimed, and the claims are instead directed to the primary embodiment, which describes structures associated with a gate-first process.

65. Accordingly, the term “dielectric trenches formed in the BSG” does not encompass dielectric trenches that are formed in a structure other than a BSG, such as a sacrificial layer.

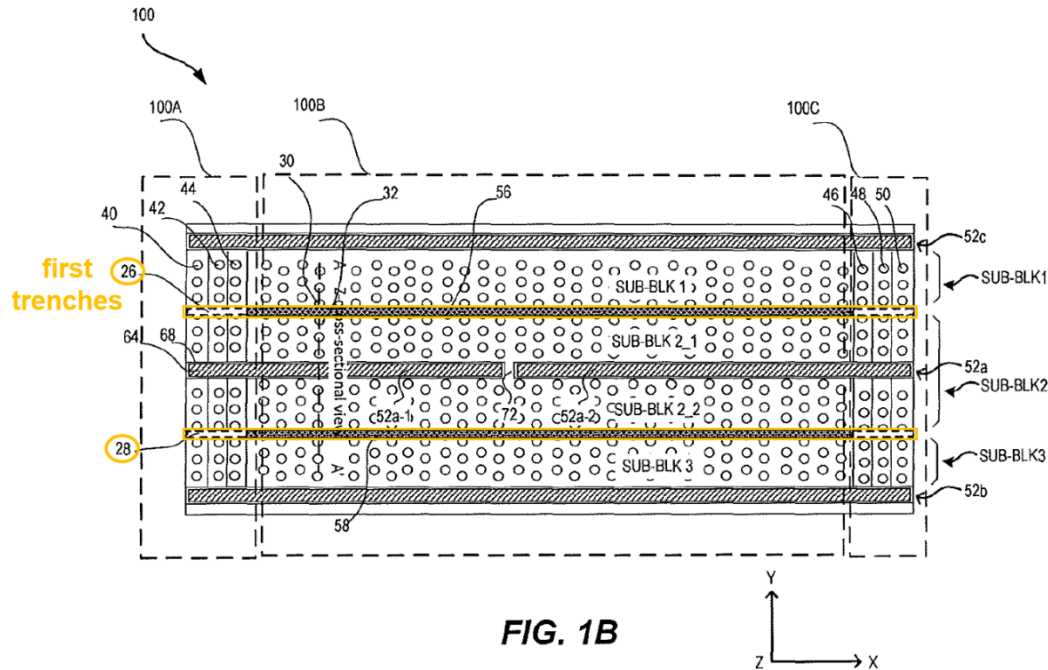
B. “one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” (Claim 1)

66. The claim limitation “one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” should be construed consistent with its plain meaning to require that the length of the dielectric trench is what separates the BSG into sub-BSGs. This construction is supported by the intrinsic record.

67. The claims expressly recite that it is the length of the dielectric trenches that separates the BSG. The claims recite that the dielectric trenches are “**extending in a length direction** of the substrate **to separate the BSG** into a plurality of sub-

BSGs”—that is, the claimed geometry of the dielectric trench “separate[s] the BSG into a plurality of sub-BSGs.”

68. Consistent with the claims, the '623 specification also supports this construction because it consistently shows dielectric trenches that extend the length of the substrate in the active region to separate the BSG into a plurality of sub-BSGs. The '623 discloses “one or more first dielectric trenches (or first trenches), such as two first trenches 26 and 28, are formed in the one or more BSGs (e.g., 62p),” which “extend[] in an X-direction (i.e., length direction) of the substrate 10 to separate the BSG 62p and the dummy BSGs 62n-62o layers into a plurality of sub-BSGs and sub-dummy BSGs, or to say, a plurality of cell strings.” '623, 7:17-26. As shown in Figure 1B, below, the **dielectric trenches** (annotated in orange) extend from one staircase region to another (from 100A to 100C) and pass through the active region (central core region 100B), thereby forming a continuous structure that separates the BSG into sub-BSGs:

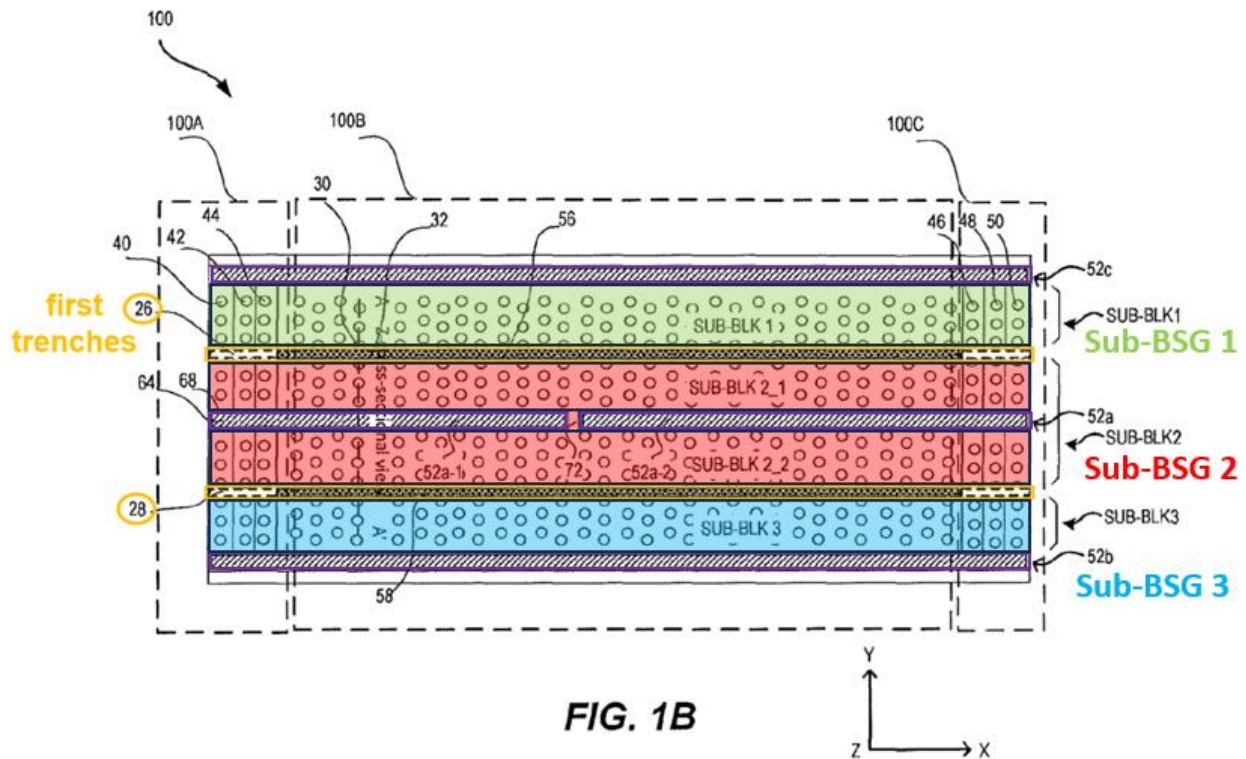


The '623 further explains that “[w]ithout the introduction of the first/second trenches, the memory device 100 (or the memory cell block 100) has a shared BSG.” ’623, 9:46-49. Thus, as described and as shown, the length of the dielectric trenches divides the BSG into sub-BSGs, and is the reason that the memory device has “sub-BSGs” as claimed.

69. I understand that the Board preliminarily “construe[d] the phrase ‘the dielectric trenches . . . separate the BSG into a plurality of sub-BSGs’ as requiring that the trenches separate the BSG into sub-BSGs, but that other components are not excluded from cooperating in the separation of the BSG into sub-BSGs.” Decision to Institute (“DI”) 15. I respectfully disagree. Because the construction addressed only the truncated phrase “the dielectric trenches . . . separate the BSG into a plurality of sub-BSGs” (*id.*), it does not appear to take into account the requirement

recited in the claims, and discussed above, that the extension of the dielectric trenches in the length direction is what separates the BSG into sub-BSGs: **“extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.”**

70. Moreover, the '623 does not disclose that other components may separate the BSG into sub-BSGs. The Board cited common source regions 52 (DI 14 (citing ('623, Fig. 1B, 9:3-8)), but **common source regions 52 do not separate the BSG into sub-BSGs**. As shown in Figure 1, **common source regions 52a** is merely in the middle of a single **sub-BSG 2** (“SUB-BLK2”) and does not divide it into further sub-BSGs because there is an H-cut 72 that connects the two sides of the common source region (like the cross-bar in a capital “H”) such that both regions are part of the same sub-BSG. 9:15-19, 9:41-44 (“two portions SUB-BLK2_1 and SUB_BLK_2 ... are electrically connected with each other through the H-Cut 72”).



And while **common source regions 52b and 52b** are at the edge of sub-BSG and do help define the boundary, they too **do not separate the BSG into sub-BSGs**. The BSG is not present on the other side of common source regions 52b and 52b. All of this is further confirmed by the '623's statement that "[w]ithout the introduction of the first/second trenches, the memory device 100 (or the memory cell block 100) has a shared BSG." '623, 9:46-49.

71. The common source regions are also never shown working with the dielectric trench that extends in the length direction to separate the BSG into a plurality of sub-BSGs. Having other structures act in cooperation for the **same boundary** would mean that the dielectric trench itself no longer "extend[s] in a length

direction of the substrate to separate the BSG into a plurality of sub-BSGs” as required by the claims.

72. Thus, the claim limitation “one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs” should be construed to require that the length of the dielectric trench is what separates the BSG into sub-BSGs.

C. “one or more second dielectric trenches ... extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs ” (Claim 1)

73. For the same reasons I discuss in §VI.B, the claim limitation “one or more second dielectric trenches ... extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs” should be construed to require that the length of the dielectric trench is what separates the TSG into sub-TSGs.

IX. THE ASSERTED PRIOR ART

A. U.S. Patent No. 10,559,583 (“Park,” Ex. 1004)

74. Park is directed to “a memory device having a three-dimensional array of memory cells” using “a vertical transistor structure in lieu of a conventional planar transistor structure.” Park, 1:15-27. The architecture of Park, however, is distinct from that of the ’623 at least because Park does not use dielectric trenches that extend along the memory array to separate the memory array into blocks, but instead uses

a short isolation insulating region in the staircase region to divide the common source line.

75. Park's memory device includes a "cell region CR" containing "a plurality of gate electrodes layers sequentially stacked on a substrate" in "a Z-axis direction," which "may provide a string select line, word lines, and a ground select line." Park, 2:14-17, 5:18-25. As illustrated in Figure 4 below, the cell region includes a "plurality of pad regions constituting a stepped structure" (*i.e.*, a staircase region), wherein the "cell contacts CNT" may be connected to the word lines:

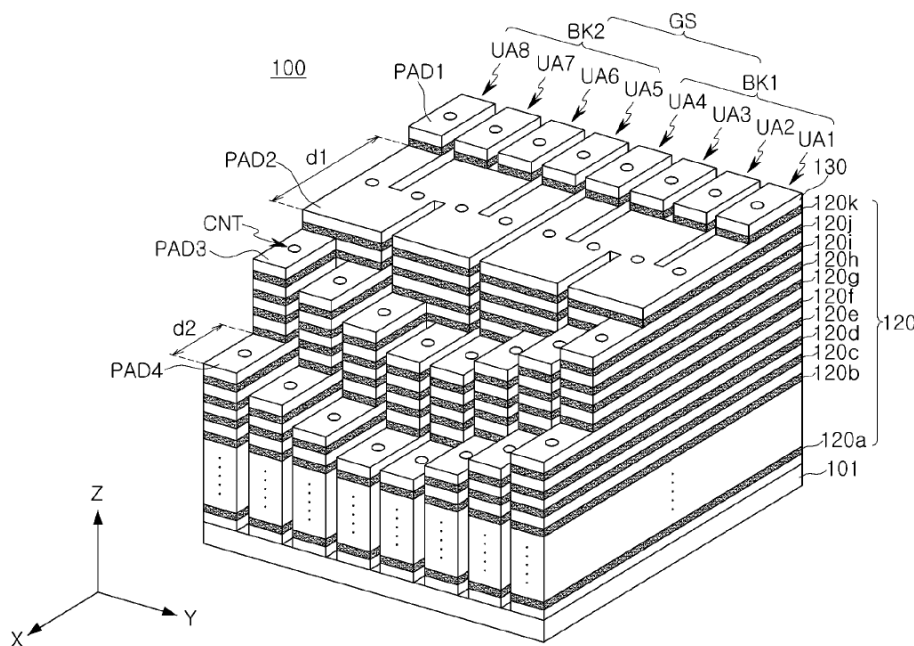


FIG. 4

76. Independent control of unit areas (*e.g.*, UA1 to UA8) is provided by the string select line and the ground select line, which "may be separated from each other at the boundaries between the first to eighth unit areas UA1 to UA8" "by the

first common source lines 102 and **first lines 103** of the **second common source lines 105**” as shown in Figure 3 below:

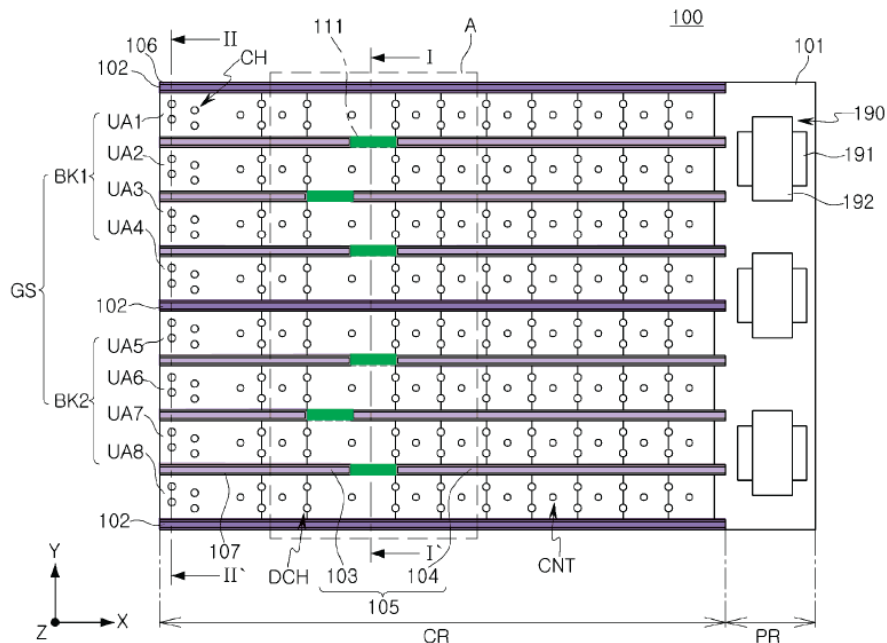


FIG. 3

Park, Fig. 3, Park, 6:4-8.

77. Park also uses **isolation insulating layers 111** “disposed between the **first and second lines 103 and 104** of the **second common source lines 105**” in the staircase region. Park, 6:8-12, 10:60-65. Instead of using a dielectric trench that extends along the length of the substrate to divide a bottom select gate (BSG), Park’s memory device architecture relies on **common source lines** to divide the ground select line (*i.e.*, the alleged BSG), and short **isolation insulating layers** to segment a subset of the **common source lines** within the staircase region. While these **isolation insulating layers** are dissimilar to the ’623’s long dielectric trenches that

separate the BSG into sub-BSGs, they are very similar to the '623's disclosure of using "H-cuts," which instead are used to separate the '623's "common source region 52 ... into two or more sub-CSRs." *Compare* Park, Fig. 3 with '623, Fig. 1B, 13:19-20 ("The common source region 52 is separated by the H-Cut 72 into two sub common source regions.") (discussed above in §VIII.B).

78. A cross-sectional view of Park's memory device "taken along line I-I' of FIG. 3" is depicted in Figure 11 below, where "only the second lines 104 of a portion of the **second common source lines 105** are illustrated." Park, 10:52-54. (Note the coordinate system for Figure 11 is different than that of Figure 3. In Figure 3, the axis along the line I-I' is the y-axis; whereas in Figure 11, the axis along the line I-I' is the x-axis. The z-axis remains the same in both figures.) There, the gate electrode layers 120 are "divided into the first and second blocks BK1 and BK2 by the **first common source lines 102**." Park, 10:46-49. BK1 and BK2 are further "divided into the first and eight unit areas UA1 and UA8 by the **second common source lines 105**." Park, 10:49-54. **Gate electrode layer 120a** "form[s] the ground select line." Park, 10:55-56. While this cross-section within the staircase region shows **isolation insulating layer 111** between sections of the **gate electrode layer 120a**, that is due to the location of this particular cross-section, and it is actually primarily the **second common source lines 105** that separates the **gate electrode layer 120a**, as I discuss and show above in Fig. 3.

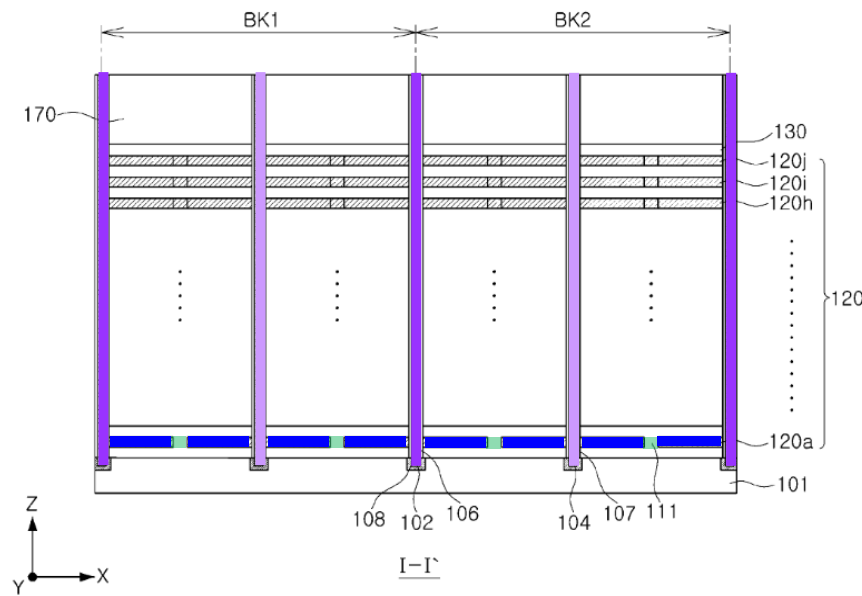
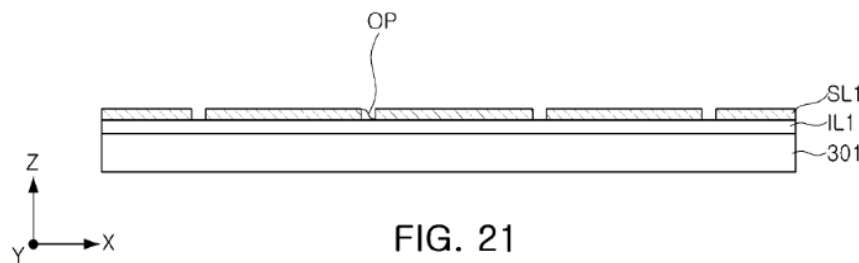


FIG. 11

Park, Fig. 11 (annotated).

79. Park cautions against using long isolation regions (e.g., to separate a gate electrode layer) because isolation regions can prevent the “proper[] secur[ing]” of the “inflow passage” through which the etching material (for removing sacrificial layers) and conductive material (for forming the gate layers) is introduced. Park, 15:53-59, 16:38-59. This is because the isolation regions separate the word line cuts (that eventually form the second common source lines) thereby “forming a relatively long path above the isolation regions 311” for the flow of etching and conductive materials. Park, 15:53-59. Moreover, when isolation regions are adjacent to one another, Park recognizes that there may be no inflow path to certain areas, and thus disposes the isolation regions “in zigzag form.” Park, 15:60-16:2.

80. Park's **isolation regions 311** are formed in a sacrificial layer, rather than in a gate electrode. Park discusses forming the insulating layer 111 (or 311 in Figures 18-36 illustrating the “memory device during the course of its manufacture”). Park states that the process of forming the opening regions includes “a first insulating layer IL1 and a first sacrificial layer SL1,” which are formed on a first substrate 301.” Park, 12:56-59. Figure 21 depicts the first sacrificial layer SL1 with an opening region (“OP”) in which the **isolation regions 311** are formed. Park, 12:65-13:1.



Park, Fig. 21. The OP regions are then “filled with an insulating material,” as depicted in Figure 23, to form **isolation regions 311**, which correspond to the **isolation insulating layers 111** of Figure 16:

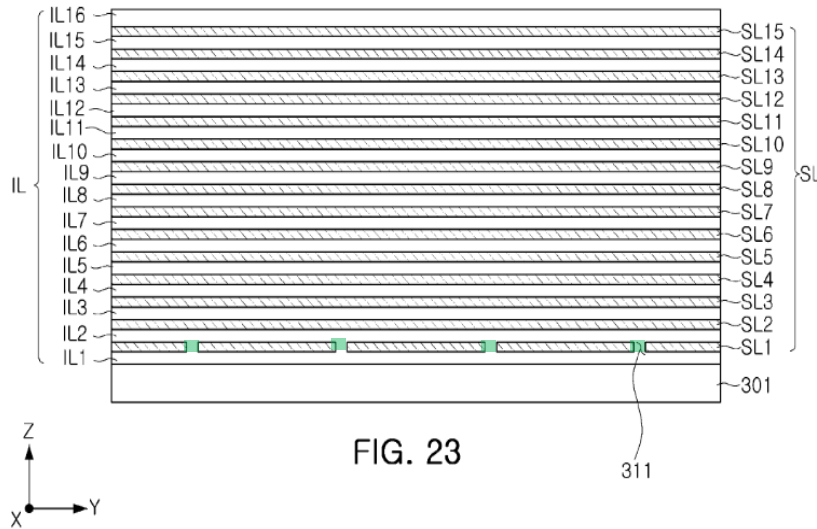


FIG. 23

Park, Fig. 23 (annotated), 13:15-17. Park states that the sacrificial layer is then etched away (*i.e.*, removed) “by an etching solution flowing through the first and second word line cuts WC1 and WC2,” depicted in Figure 29:

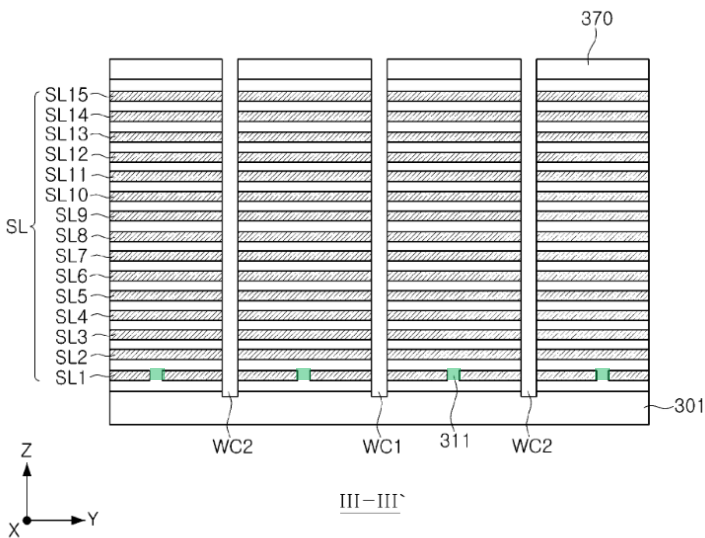
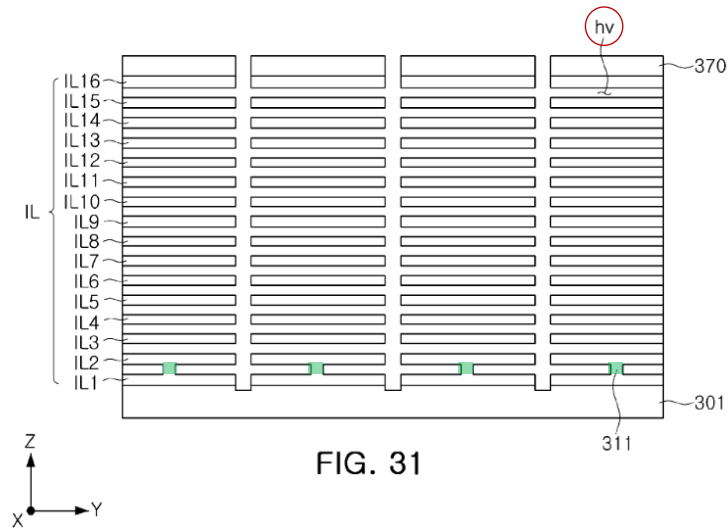
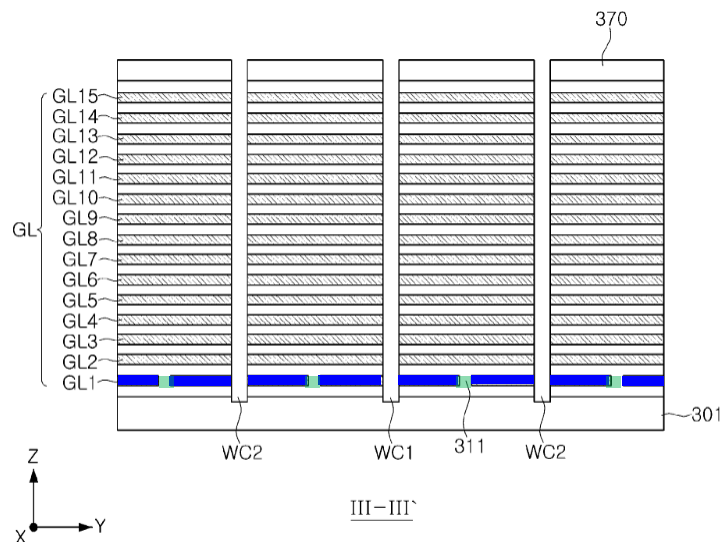


FIG. 29

Park, Fig. 29. After this etching process, “horizontal voids hv are formed,” which are depicted in Figure 31:



Park, Fig. 31, 15:39-40. While the sacrificial layer has been etched away, the **isolation regions 311** remain. Park, 16:7-9. The voids are then filled with conductive material, which flows from the first and second word line cuts WC1 and WC2, to form the gate electrode layers. Park, 16:3-7. Figure 34 of Park depicts the first gate electrode layer GL1, which forms the **ground select line**:



Park, Fig. 34 (annotated).

B. U.S. Patent Pub No. 2019/0122734 (“Shibata,” Ex. 1005)

81. Petitioner relies upon combinations of Shibata and Park (Shibata in view of Park and Park in view of Shibata) for Grounds 2 and 3. Pet. 57-94. Shibata is directed to aspects of three-dimensional memory devices that have a “vertical transistor structure.” Shibata, [0067].

82. Petitioner generally relies on Shibata’s second embodiment as illustrated in Figure 16:

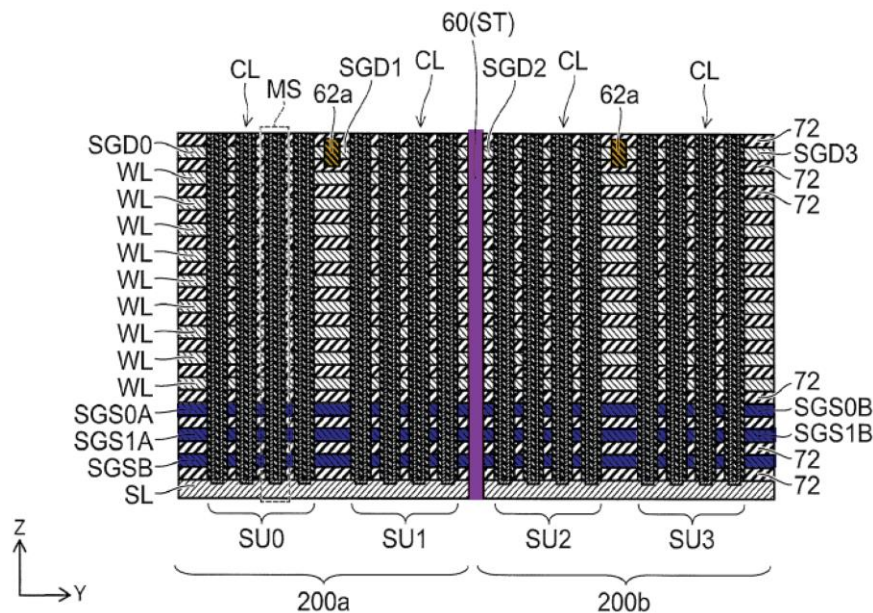


FIG. 16

Shibata, Fig. 16 (annotated). Shibata’s Figure 16 depicts a second embodiment with “two sub-blocks 200a and 200b subdivided by three **separation portions 60** (slits ST) separated from each other in the Y-direction.” Shibata, [0162]. Figure 16 additionally illustrates **separation portion 62a** of sub-block 200a and **separation portion 62a** of sub-block 200b. In this embodiment, there is a single-layer drain-

side select gate SGD0 and a **three-layer source-side select gate** and layers of word lines stacked between. Shibata, [0166]. Notably, Shibata's **separation portions 62a** do not divide the **source-side select gate**. Instead, the **source-side select gates** are divided in the Y-direction by the separation portions 60 (the slits ST) into "SGS0A," "SGS0B," "SGS1A," and "SGS1B." Shibata, [0178].

83. Petitioner also relies on Figure 47A, which is a plan (top-down) view of the drain-side select gate layer divided into "SGD0," "SGD1," "SGD2," and "SGD3":

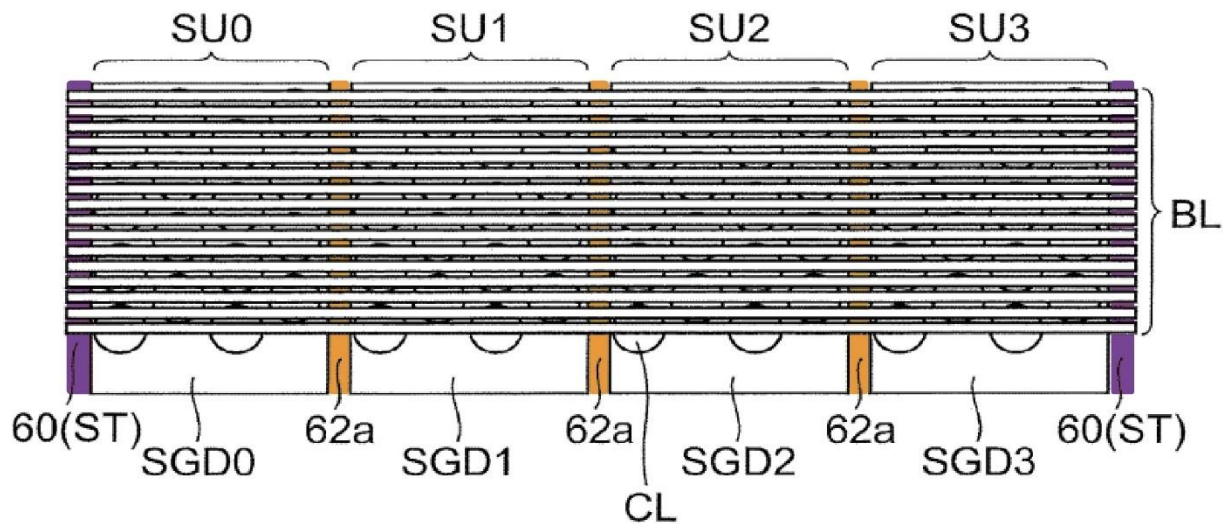


FIG. 47A

Shibata, Fig. 47A (annotated), [0444], [0446], [0047]. As illustrated in Figure 47A, the **separation portions 62a** extend through the array region of the memory. Note, that as illustrated in Figure 47A, Shibata's first embodiment has a different configuration than that of Figure 16. For example, there are three **separation**

portions 62a facing back-to-back instead of alternating with separation portions 60. In addition, the drain-side select gate SGD1 of Figure 47A is between two separation portion 62a instead of next to one of the separation portions 60 (slits ST).

84. Shibata's separation portions are formed in a sacrificial layer instead of in the conductive material that forms the select gate layers. Shibata also states that adding the separation portions to only the drain-side gate select lines (near the top of the device) and does not discuss adding separation portions to the source-side select lines (near the bottom of the device). This is described in Shibata in connection with the first embodiment, where Shibata describes the "method for manufacturing the semiconductor memory device of the first embodiment." Shibata, [0103]. (Note, Figures 8A through 11B are schematic cross-sectional views showing a method for manufacturing the semiconductor memory device of the first embodiment (Shibata, [0011]), but this embodiment differs from that illustrated in Figure 47 in that it has a three-layer drain-side select gate with three separation portions 62a, 62b, and 62c positioned at of these layers. While the configuration is different than that of the second embodiment, the method of manufacture is informative.)

85. Shibata's process starts off with the structure as depicted in Figure 8A, where "the insulating layer 41 is formed on the substrate 10; the source layer SL is

formed on the insulating layer 41; and the stacked body 100 is formed on the source layer SL.” Shibata, [0104]. The “insulating layer 72 and sacrificial layer 71 are stacked alternately on the source layer SL.” Shibata, [0105].

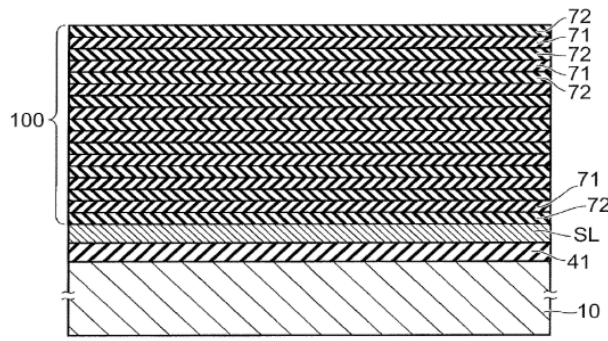


FIG. 8A

Shibata, Fig. 8A. As depicted in Figure 8B, silicon oxide film is formed on the top of the stacked body which serves as a mask. Shibata, [0106]. A slit, 61b, “pierces the mask 75, the insulating layer 72 of the uppermost layer, and the sacrificial layer 71 of the uppermost layer.” Shibata, [0106]. Slit 61b penetrates through the upper sacrificial layer 71 and terminates within the insulation layer 72.



FIG. 8B

As depicted in Figure 8C, “a separation portion 62b is formed inside the slit 61b” by filling the slit with an insulating material. Shibata, [0107]. This layer, called insulating film 62, is also deposited on mask 75. *Id.*



FIG. 8C

Mask 75 and the insulating film 62 are then removed and the final structure is depicted in Figure 9A. Shibata, [0107].



FIG. 9A

Subsequently, a sacrificial layer 71 and an insulating layer 72 are deposited, followed by the application of another mask layer 76 to generate a second slit, 61a, at another position. Shibata, [0108]-[0109]. Slit 62a is filled with insulating material to form separation portion 62a, depicted in Figure 9C below. Shibata, [0110].

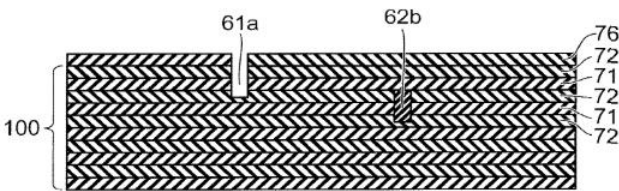


FIG. 9B

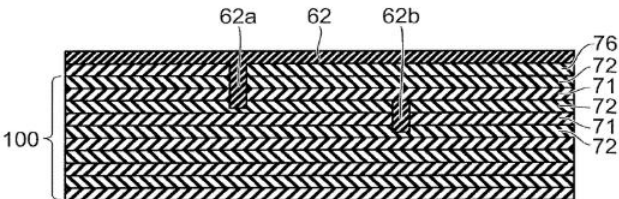


FIG. 9C

This sequence of steps is repeated to form a third separation portion, 62c.

In total, Shibata states that three separation portions—62a, 62b, and 62c—are situated at distinct locations along the Y-direction, as depicted in Figure 13, and which “divide drain-side select gate layers of different layers.” Shibata, [0155]. The sacrificial layers 71 are then removed through an etching process and replaced with conductive layers 60 to form the source gate drains and word lines. Shibata, [0155]. The separation portions segment the drain-side select gate layers into six—“SGD0A,” “SGD1A,” “SGD2A,” “SGD0B,” “SGD1B,” and “SGD2B”—each of which are “each controlled electrically independently.” Shibata, [0126]-[0129].

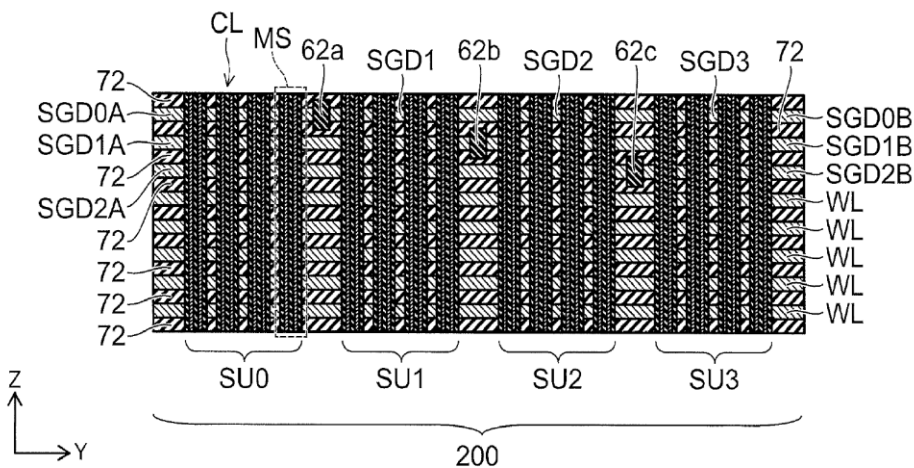


FIG. 13

Shibata, Fig. 13.

X. PETITIONER’S GROUND 1: PARK DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-11

86. For the reasons explained below, it is my opinion that Park does not disclose or render obvious the Challenged Claims at least because Park does not

disclose or render obvious multiple elements of claim 1—the sole independent claim. For example, Park’s isolation insulating layers are not “dielectric trenches formed in the BSG” and do not “extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” Park also does not disclose or render obvious “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs” as required by claim 2, and similar deficiencies apply to claim 3 as well. Finally, for claims 10 and 11, Park does not disclose or render obvious insulating layer to separate “dummy BSGs” and “dummy TSGs” into “dummy sub-BSGs” and “dummy sub-TSGs,” respectively.

A. Independent Claim 1: Park Does Not Disclose or Render Obvious Multiple Requirements of Limitation [1.e]

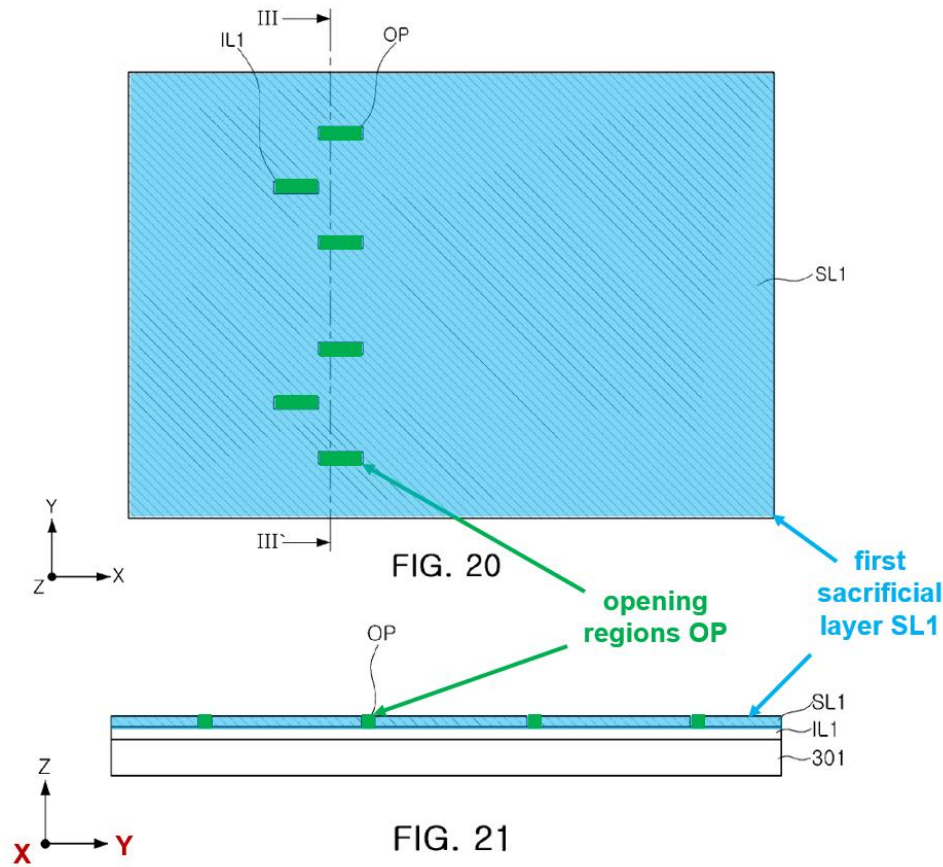
87. Petitioner does not show that Park discloses or renders obvious at least two requirements of limitation [1.e]: “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” Park’s isolation structures (alleged dielectric trenches) are formed in a sacrificial layer rather than a BSG, and the short isolation structures do not separate the BSG into a plurality of sub-BSG’s.

(a) Park’s Isolation Insulating Layers Are Not “Dielectric Trenches Formed in the BSG” (Limitation [1.e])

88. Petitioner does not show that Park’s alleged dielectric trench (isolation insulating layers) is formed in the purported bottom select gate (BSG) (ground select line (GSL)) because Park’s isolation insulating layers are formed in a different structure—a sacrificial layer.

89. Claim 1 requires “**one or more first dielectric trenches formed in the BSG** and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” As I discuss in §VIII.A, the term “formed in the BSG” does not encompass features that are formed in another structure other than a BSG, such as a sacrificial layer.

90. Petitioner maps Park’s “isolation insulating layer” to the claimed dielectric trenches (Pet. 30-34), but Park’s isolation insulating layer are formed in a sacrificial layer rather than a BSG. Specifically, as shown below, Park’s **isolation insulating layers** are formed by forming “**opening regions OP**” in the “**first sacrificial layer SL1**” and then filling the opening regions “with an insulating material.” Park, 12:65-13:17.



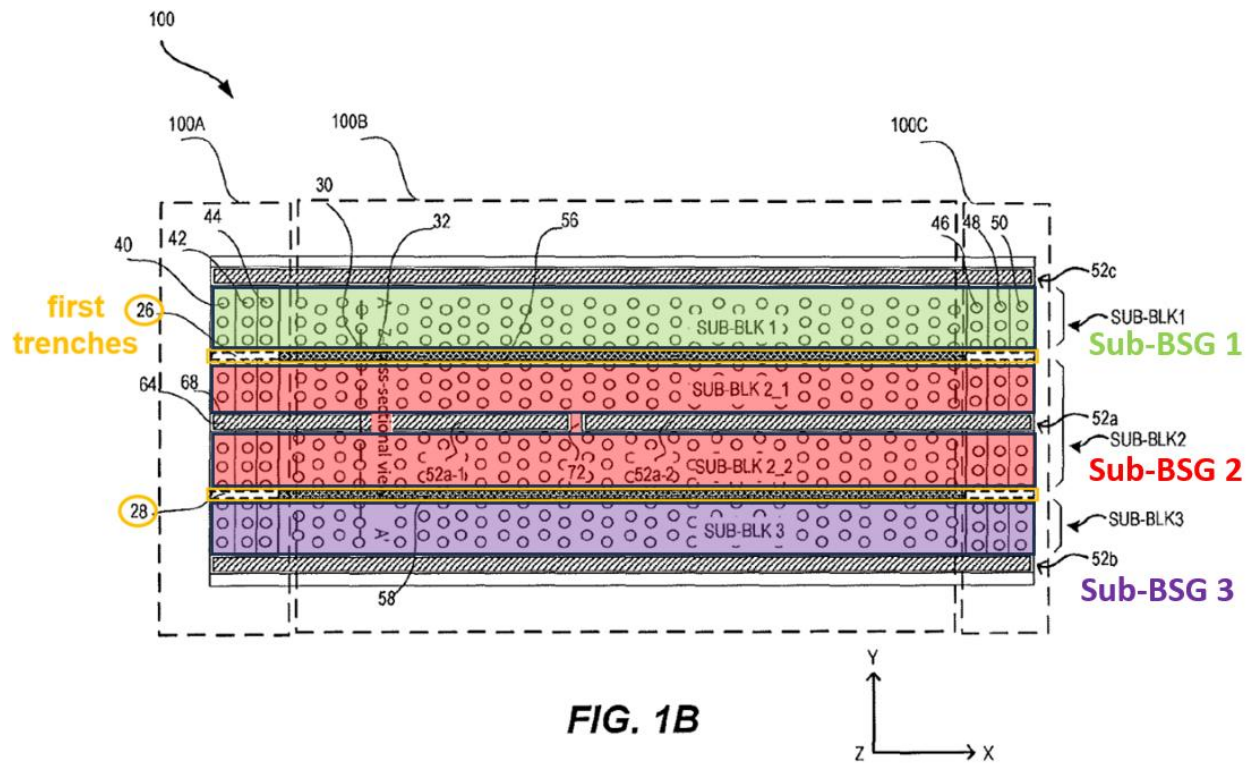
Park, Figs. 20-21 (annotated – in Park’s Fig. 21, the X and Y axes seem to be mislabeled, which is corrected in the annotated figure). Moreover, because the alleged isolation insulating layers are formed in the sacrificial layer rather than a BSG, they are not formed in the BSG “to separate the BSG into a plurality of sub-BSGs,” as claimed, and thus do not perform the important BSG separation function of the ’623. Thus, the isolation insulating layer also is not formed to “separate the BSG into a plurality of sub-BSGs.” Rather, there is no BSG that is divided into sub-BSGs.

91. Accordingly, Petitioner does not show that Park's isolation insulating layer is formed in the BSG.

(b) Park's Isolation Insulating Layers Do Not "Extend[] in a Length Direction of the Substrate to Separate the BSG Into a Plurality of Sub-BSGs" (Limitation [1.e])

92. Park does not disclose that its alleged dielectric trenches (isolation insulating layers) "extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs" as required by the Challenged Claims because Park's isolation insulating layers are short separations limited to the staircase region.

93. Claim 1 requires that the claimed trenches "**extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.**" As I discuss in §VIII.B, the limitation "one or more first dielectric trenches ... extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs" requires that the length of the dielectric trench is what separates the BSG into sub-BSGs. For example, the '623 shows dielectric trenches 26 and 28 that extend the length of the substrate, from one staircase region to the other and through the active region, to separate the BSG in sub-BSGs:



'623, Fig. 1B.

94. Petitioner maps this element to isolation insulating layers in Park, which as shown below are short cuts through the common source lines.



Fig. 3 (annotated by Petitioner, Pet. 30-31).

95. Park's isolation insulating layers do not extend in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs as required by the Challenged Claims. The isolation insulating layers are merely short cuts in the common source line and do not even extend into the active region, and therefore are not a feature that extends in the length direction of the substrate to separate the alleged BSG into sub-BSGs. For instance, as shown below in Figure 3, Park states that its memory device has a plurality of "first common source lines 102" and "second common source lines 105." Each of the second common source lines are composed of a first section, *i.e.*, "first lines 103," and a second section, *i.e.*, "second lines 104." *See, e.g.*, Park, 16:55-59; *see also* Park, 1:59-61. The first lines 103 and second lines 104 of the common source lines each extend horizontally along

the x-direction, and have short gaps (annotated in green) in the staircase region of the memory device:

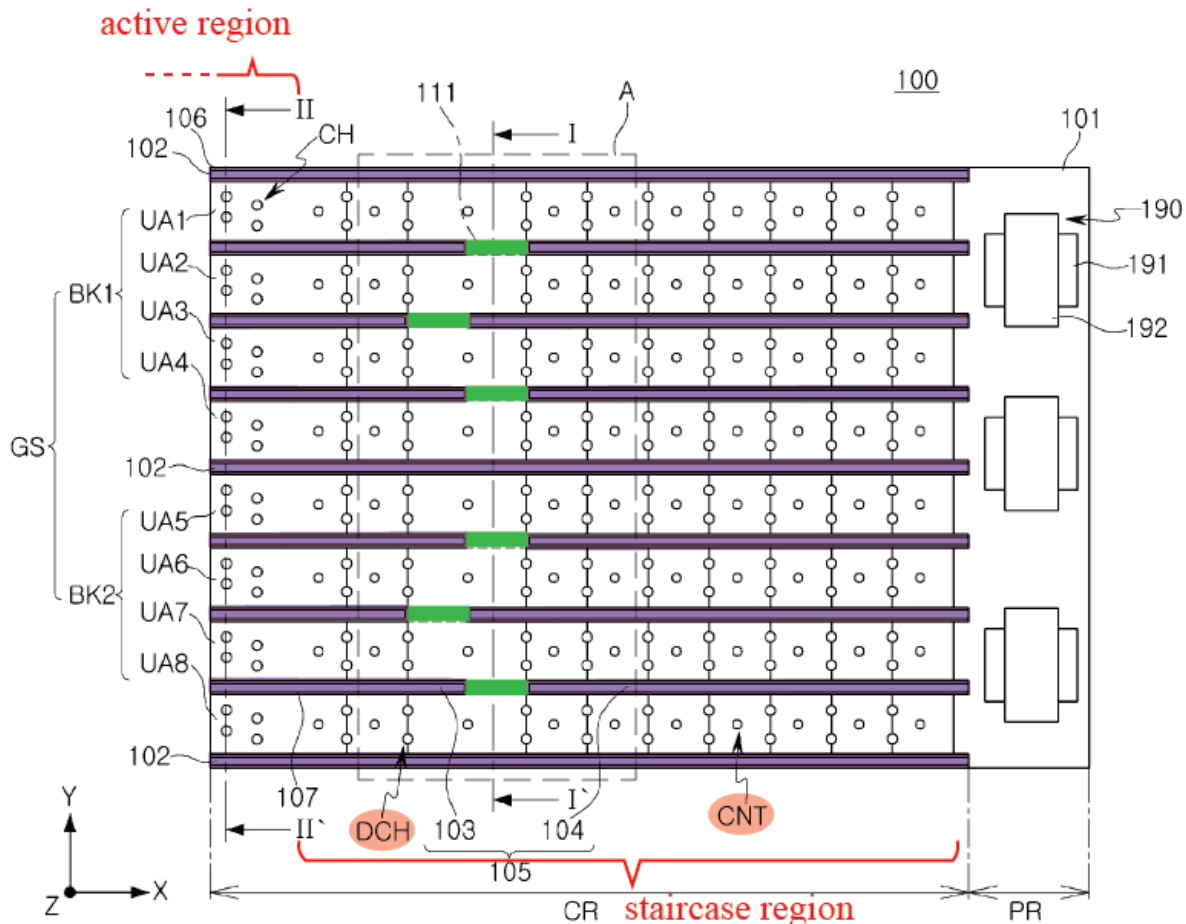


FIG. 3

Park Fig. 3 (annotated). Park further discloses that in this gap an “isolation insulating layer 111 [is] disposed between the first and second lines 103 and 104.” Park, 10:63-65. Accordingly, the **isolation insulating layer 111** is a short division in the **second common source lines 105** that separates the first and second lines 103 and 104. Figure 3 of Park also shows that the **isolation insulating layers** extend no more than just the distance from the center of one dummy channel (DCH) and the

center of an adjacent contact (CNT). Moreover, Park’s **isolation insulating layers** are small, localized regions in the staircase structure, confined to the very edge of the memory array with the dummy channel structures **DCH** and cell contacts **CNT**, completely outside the active region—i.e., away from the majority of the BSG that Petitioner argues it separates.

96. Thus, Park’s isolation insulating layers do not extend in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs as required by the Challenged Claims. In its Institution Decision, the Board found that this limitation is met by “common source lines *in cooperation with* isolation insulating layer 111” (DI 15 (emphasis in original)), but I respectfully disagree as the conclusion was based on an incorrect preliminary claim construction. See §VIII.B. Under the proper construction, which requires that the length of the dielectric trench is what separates the BSG into sub-BSGs, Park’s short isolation insulating layers 111 do not satisfy the claim.

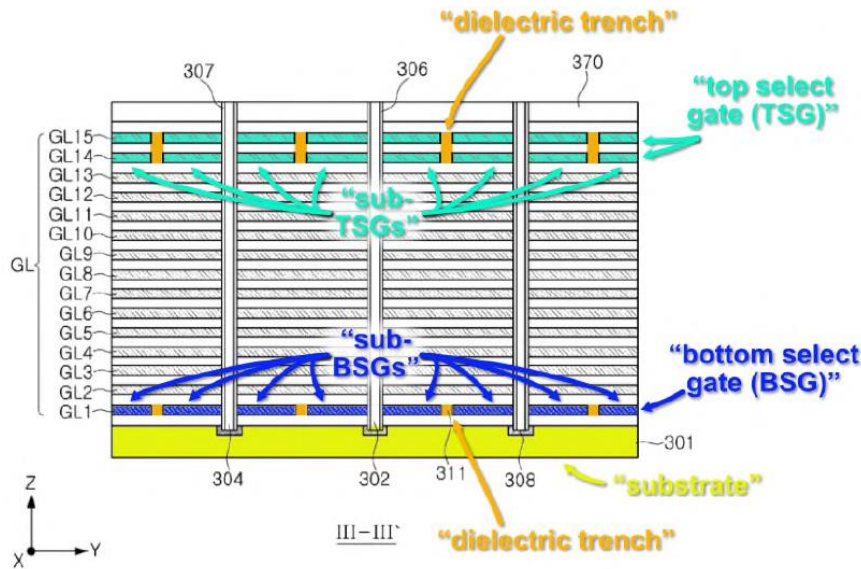
97. Thus, Park does not disclose or render obvious the claimed dielectric trenches that extend in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.

B. Claim 2: Park Does Not Disclose or Render Obvious “One or More Second Dielectric Trenches Formed in the TSG and Extending in the Length Direction of the Substrate to Separate the TSG into a Plurality of Sub-TSGs”

98. Park does not disclose any dielectric trenches formed in the TSG, as required by claim 2, and Petitioner has not shown that it would have been obvious to modify Park to include any such trenches, let alone trenches that extend in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.

99. Claim 2 recites “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.” As I discuss in §VIII.C, the limitation “one or more first dielectric trenches ... extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs” requires that the length of the dielectric trench is what separates the TSG into sub-TSGs.

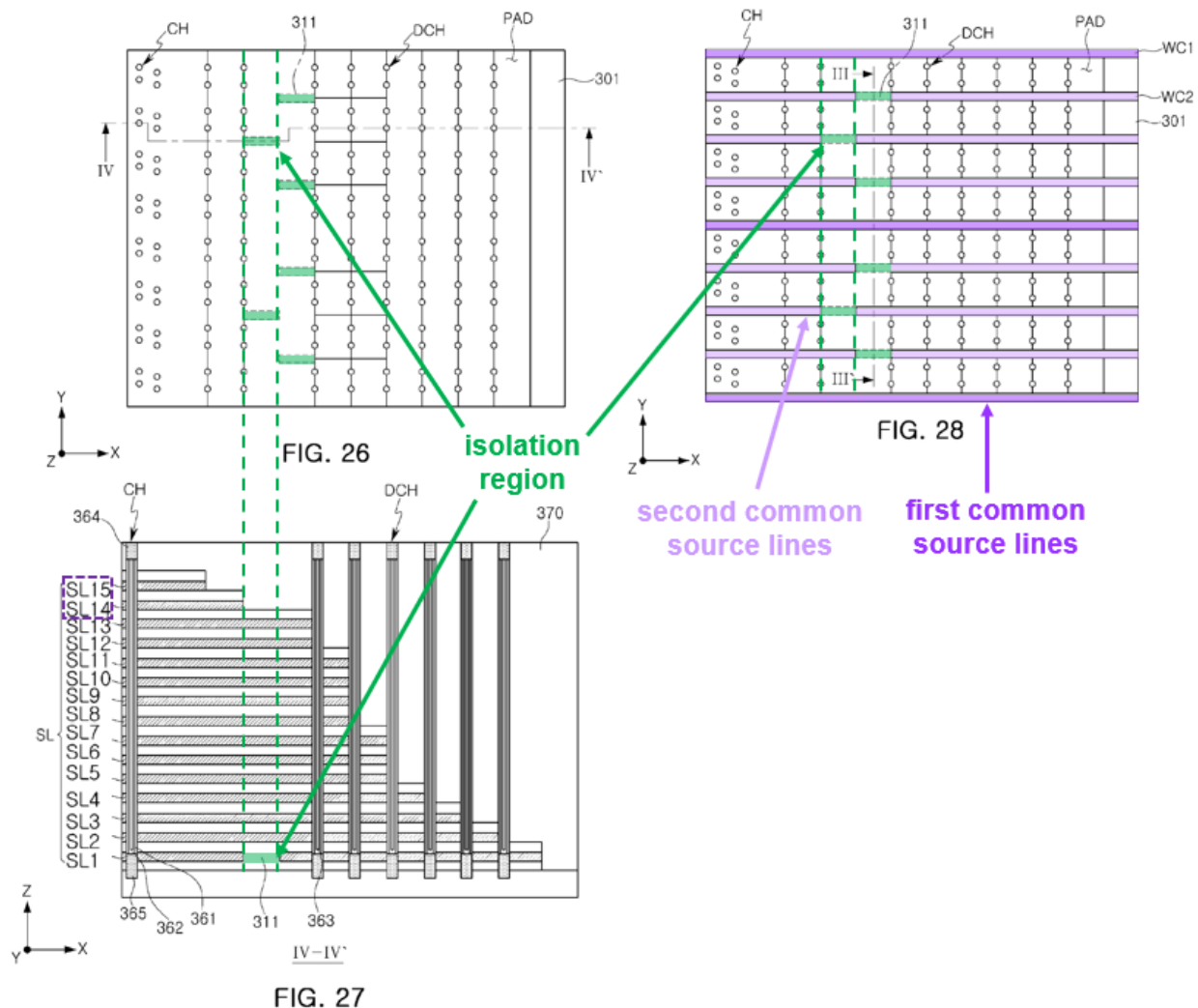
100. Park does not disclose any dielectric trench that separates the TSG into a plurality of sub-TSGs. Petitioner instead argues that it would have been obvious to modify Park to “include another isolation insulating region 111” in the upper SSL layers, and presents a modified version of Figure 36, see below, to illustrate the proposed modification that has dielectric trenches in the alleged TSG directly above the alleged dielectric trenches (isolation insulating layers) in the alleged BSG. Pet. 43.



Park, Fig. 36 (modified and annotated by Petitioner at Pet. 43). But Petitioner’s proposed modification relies on errors in several of the cross-sections, as explained in detail below, which Petitioner wrongly contends is a separate embodiment.

101. A POSITA would not have modified Park to include an isolation insulating layer in the alleged TSG (SSL) because **there is no TSG in the region where Petitioner proposes adding the isolation insulating layer, because the TSG ends before it reaches that location.** Petitioner’s proposed modification is to add an isolation insulating layer in the alleged TSG directly above the isolation insulating layer in the alleged BSG. Pet. 43-45. But as Petitioner admits, Park’s source upper select line (SSL), *i.e.*, the purported TSG, does not extend into the staircase region as much as Park’s GSL, and as a result, **“is not present over the portion of the GSL [alleged BSG] divided by ‘isolation insulating layers 111.’** Pet.

41. This is also shown below in connection with Figs. 26-28, where the isolation insulating region 311 is highlighted in green.



Park, Figs. 26-28 (annotated). In Park's Figure 27, as printed on the patent, all the sacrificial layers are mislabeled as "SL15" instead of the correct sequential labeling which can be found in Figure 25. This mislabeling is corrected in the annotated version of Fig. 27 shown here. As seen in Park's Figures 26-27, which show the device at the same stage of its manufacture, the sacrificial layers SL14 and SL15 do

not extend to the right vertically above (in the Y direction) **isolation regions 311**. Thus, in that location there is no TSG in which to add the proposed isolation region. The upper common source lines (alleged TSG) simply end before they reach that location. Therefore, while the SSL (alleged TSG) is separated into portions, it is separated entirely by the common source lines, and not by any dielectric trench. This is also expressly stated in Park. Park, 6:4-8 (“In an example, portions of the string select line may be separated from each other at boundaries between the first to eighth unit areas UA1 to UA8 by the first common source lines 102 and first lines 103 of the second common source lines 105.”). And while the **first common source lines** and the **second common source lines** are shown with **isolation regions 311** in the top-down view of Figure 28, that is only because the depicted features represent the bottom layer, e.g., SL1 (the location of the alleged BSG), where the common source lines extend much further into the staircase region, and not the top layer, e.g., SL15 (the location of the alleged TSG).

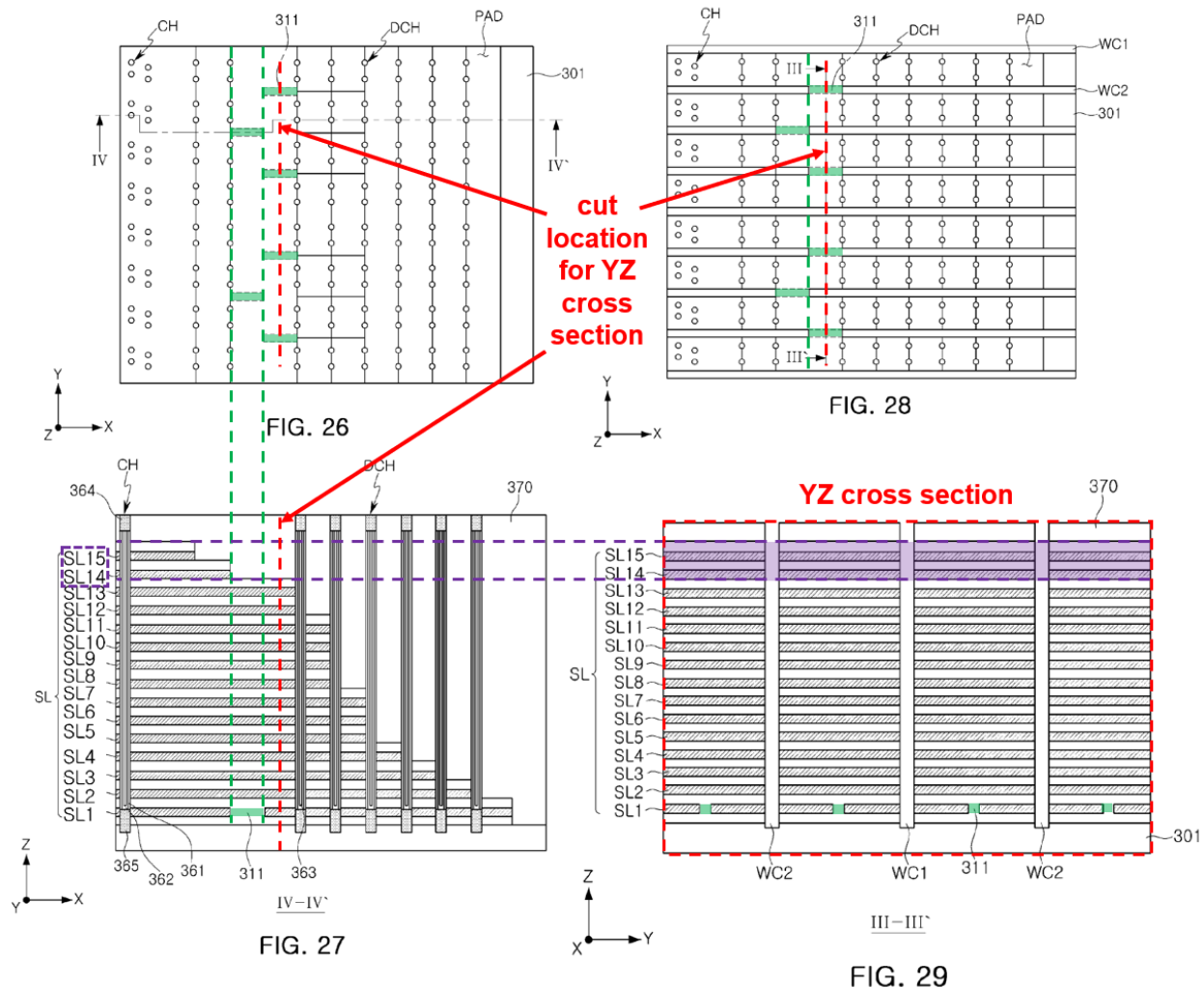
102. The alleged TSG (SSL) is shorter on top than the lower layers (and thus prevented from including the proposed isolation insulating layer) in order to form the “stepped structure” (staircase structure) of the ends of the gate electrode layers that is critical to Park’s disclosure. Park, 6:56-64. This stepped structure enables “pad regions” that host “cell contacts CNT” that are necessary to supply voltage to the gate electrodes. Park, 7:60-8:6. Park does not disclose an embodiment where

the SSL (alleged TSG) has the same physical extent as its GSL (alleged BSG), which would have eliminated the stepped structure and the cell contacts CNT, contradicting its disclosures. Petitioner does not address the removal of the stepped structure, which is the logical result of the proposed modification, rendering Park's device inoperable.

103. Petitioner asserts that Park has “other embodiments” where “the upper SSL is located over the portion of the GSL divided by isolation insulating layers” and Park's Figure 36 relates to such an embodiment (Pet. 41), but Petitioner is incorrect—the entire series of Figures 18 through 36 depict the same embodiment. Specifically, Figures 18 through 36 depict the same embodiment at different stages of its manufacture. Park, 12:53-55 (“FIGS. 18 through 36 are views illustrating a method of manufacturing a memory device according to *an* example of the present inventive concept.”).

104. Petitioner nonetheless maintains that Figure 36 of Park shows that the SSL (alleged TSG) is present above the isolation insulating layer 311 (Pet. 41-42), but the cross section view of Figure 36 includes an error and mistakenly shows all of the layers present in the device—the top layers do not extend to where the cross section is located. For example, an analysis of the cross section that results in Figure 29 reveals that the top four layers (SL15 to SL 14), which are highlighted in the

figure, are not present in that region and should not have been depicted in Figure 36 (or in 29):



Park, Figs. 26-29 (annotated). The following steps illustrate the issue:

- 1) The YZ cross section in Figure 29 is taken along the III-III' line depicted in Figure 28. Park, Figs. 28-29 (Park mistakenly states “FIGS. 27, 29 and 31 are cross-sectional views take [sic] along lines IV-IV' of FIGS. 26, 28 and 30” (Park, 3:11-12), but Figure 29 itself indicates it is a cross-sectional view taken along line III-III' (of Figure 28)).

- 2) Figure 28 provides the same view of the device as Figure 26 but at a later stage of its manufacture. The III-III' line can thus be carried over to Figure 26. Park, Figs. 26, 28.
- 3) The XZ cross section in Figure 27 is taken along the IV-IV' line depicted in Figure 26. Park, Figs. 26-27. Thus, the two figures can be aligned as shown below to reveal where the YZ cross section of Figure 29 is located in Figure 27. The cross section does not include the top four layers present in the device at that stage: IL16, SL15, IL15, and SL14 (the insulating layers IL1 through IL16 are not labeled in Figures 27 and 29 but they are labeled in, e.g., Figure 23).

Likewise, Figures 31, 34, and 36 provide the same view of the device as Figure 29 but at later stages of its manufacture. In particular, Figure 31 depicts the device after the removal of the sacrificial layers SL, forming “horizontal voids” (“hv”) in their place, Figure 34 depicts the device after the horizontal voids are filled to form gate electrode layers GL1 through GL15, and Figure 36 depicts the device after the common source lines are formed in the word line cuts. Park, 15:35-45, 16:3-16, 16:50-55.

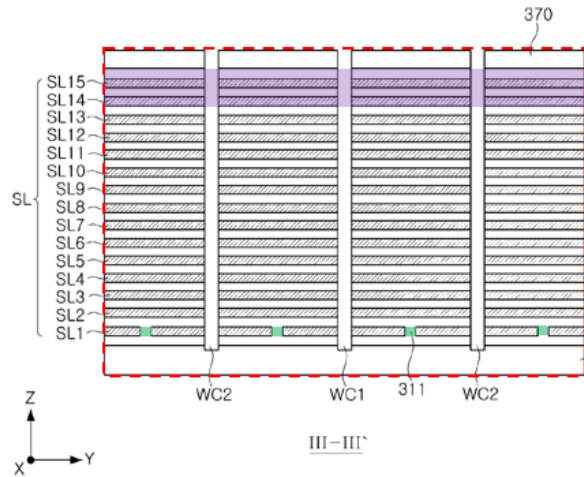


FIG. 29

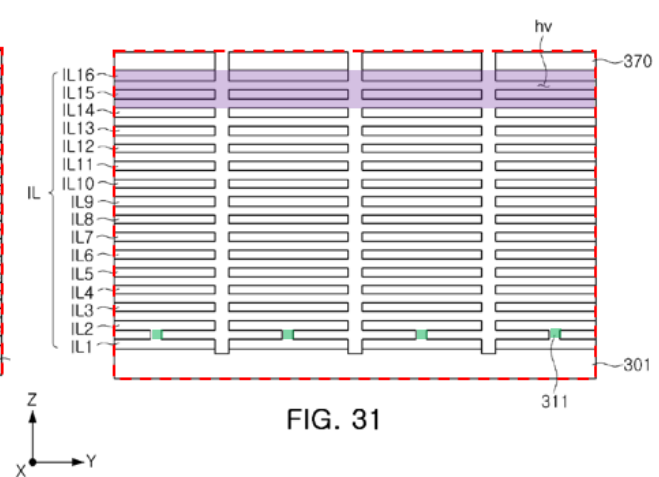


FIG. 31

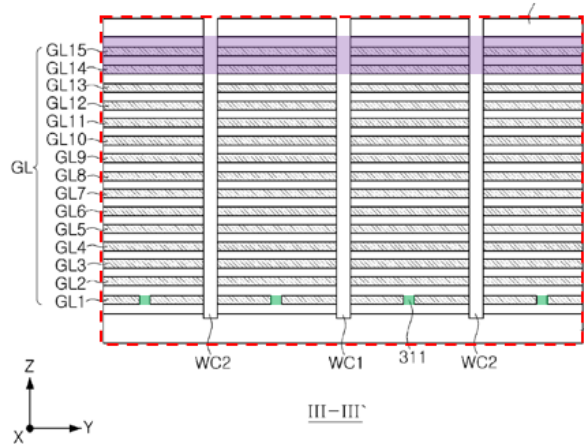


FIG. 34

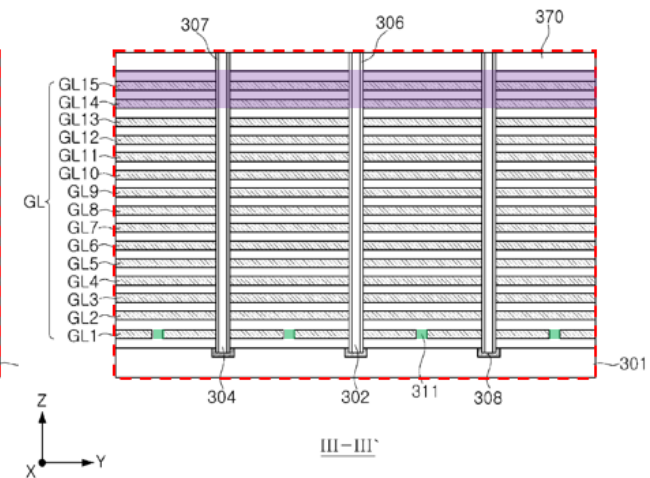


FIG. 36

Park, Figs. 29, 31, 34, 36. As a result, in all for of these cross sections, the highlighted top layers are depicted by error and are not in fact present. And, again, interpreting these errors as an “other embodiment” as Petitioner proposes would conflict with Park’s disclosures because it would eliminate the necessary stepped structures used for cell contacts, rendering Park’s device inoperable. For example, Park does not explain how the device would operate if the gate lines are not accessed via the cell contacts CNT on the stepped structure. Park never does so because it does not present such alternative embodiment.

105. Thus, there is no alleged TSG at the location of Petitioner's proposed modification, and a POSITA could not have made such a modification. Petitioner's argument is based on a non-existent embodiment where the SSL extends farther into the edge of the device than it actually does, and as a result Petitioner is attempting to solve an imaginary problem by introducing trenches to separate SSLs even though they are already completely separated into by the common source lines.

106. Petitioner's arguments about combining different embodiments (Pet. 44) are misplaced because Petitioner does not combine different embodiments. Similarly, Petitioner's arguments about applying Park's disclosures about "isolation insulating layers" in its GSL to its SSL (Pet. 44) also are insufficient, because the problem those disclosures address (*i.e.*, separating the GSL into portions in combination with the common source lines in the staircase region) is not present for the SSL, as the SSL does not extend into the staircase and is already separated into portions. Therefore, a POSITA would not have had a motivation to modify Park's SSL to include similar isolation insulating layers.

107. Petitioner's proposed trenches also are not "extending in the length direction of the substrate" as required by claim 2. Petitioner proposes adding narrow isolation regions to the SSL based on the use of such isolation regions in the GSL, but these isolation regions are not "extending in the length direction of the substrate" for the same reasons I discuss in relation to the isolation regions in the GSL. *See*

§X.A.(a). Here, “the length direction” in claim 2 refers back to “a length direction” of claim 1 and thus is Park’s X direction. Yet Petitioner does not depict the proposed cuts in a view that would show whether they extend in the purported length direction of the substrate, *i.e.*, the X direction. But for claim 3, Petitioner clarifies that it is proposing adding cuts of the same length above as insulating layer 111 (Pet. 47-48), confirming that the mapping is insufficient for the same reasons I discuss in §X.A.(b).

108. Accordingly, Petitioner does not show that Park discloses or renders obvious second dielectric trenches formed in the TSG and that the purported second dielectric trenches extend in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.

C. Claim 3: Park Does Not Disclose or Render Obvious “the First Dielectric Trenches and the Second Dielectric Trenches Are Aligned with Each Other in a Width Direction of the Substrate”

109. For claim 3, the Petition does not address which direction is the “width direction” (Pet. 45), and thus Petitioner has not shown that the alleged first and second dielectric trenches are “aligned with each other in a width direction of the substrate” as required by claim 3. In addition, regardless of which direction is the “width direction,” Petitioner’s mapping again requires adding an isolation insulating layer in the SSL above the isolation insulating layer 111 in the GSL, where there is no SSL present, and thus Park also not disclose or render obvious claim 3 for at least the same reasons I discuss above for claim 2.

D. Claim 10: Park Does Not Disclose or Render Obvious “One or More Dummy BSGs That Are Formed Between the Plurality of Word Lines and the BSG, Separated by the One or More First Dielectric Trenches into a Plurality of Dummy Sub-BSGs”

110. Petitioner has not shown that Park discloses or renders obvious “one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs” because Park nowhere discloses separating the alleged dummy BSGs with dielectric trenches, and Petitioner does not identify any motivation for using isolation insulating layers 111 to perform such separation.

111. Park discloses only embodiments “where only its select lines—and **not the dummy lines**—are separated into portions corresponding to unit areas,” but Petitioner asserts that it would have been obvious to separate Park’s dummy lines. Pet. 55-56. I disagree. Park does not disclose that its dummy lines should be separated into unit areas; rather, they are separated into blocks and remain connected within the blocks by the “connecting electrodes,” just like the word lines. Park, 7:30-43 (in particular, disclosing that the “dummy lines of each of the first and second blocks” are “separated from each other by the first common source line 102 disposed between the first and second blocks.”). Petitioner states that this “could” be done (Pet. 55-56), which I understand not to be the proper test for obviousness. The question for obviousness is whether a POSITA would have been motivated to make this change, which Petitioner does not show.

112. Petitioner points to examples of structures that pass through and divide multiple layers in other references (Shibata, Ex. 1018), but does not provide any motivation for this modification other than referring to “improv[ing] electrical performance” and the declaration of Dr. Lee. Pet. 55-56. But this vague argument is inapplicable to the question of structures that pass through and divide multiple layers.

113. Petitioner points to Dr. Lee (Ex. 1003, ¶281) where Dr. Lee states that “[f]or instance, a POSITA would have understood that dummy cells, including dummy lower and upper select transistors, serve the purpose of suppressing leakage current such as drain-induced barrier lowering current (DIBL) and trap assisted band-to-band tunneling current (BTBT) and suppressing hot-carrier injection (HCI)” and that “[t]hey also play a role in data disturb characteristics,” and cites to pages 130 and 144 in Ex. 1012. These effects that Dr. Lee mentions, such as DIBL, BTBT, and HCI, are effects between the source and drain of transistors; that is, these are vertical effects in 3D NAND devices, not lateral effects. Closer inspection of pages 130 and 144 of Exhibit 1012 (which is a book chapter from Micheloni’s “Inside Solid State Drives (SSDs)”) confirms that this discussion is about electrical effects in the vertical direction (i.e. perpendicular to the substrate), which can be mitigated by adding additional layers such as word line layers or control gate layers. Ex. 1012, 130 (“Why dummy layers? Mainly because of the floating body of the memory cells

with vertical channel. In fact, during the programming operations, hot carriers are generated by *the high lateral electric field located at the [vertical] edge of the NAND string*. Therefore, these hot carriers keep the voltage on the channel low during the programming operation of the first wordline (i.e. Program Disturb). *Dummy wordlines before [i.e., below] the first WL* are an effective and simple solution to this problem.”) (emphasis added). Micheloni’s discussion is not about structures which pass through and divide multiple layers. Put another way, Dr. Lee’s citation has been misapplied to the concept of “improv[ing] electrical performance” for structures that pass through and divide multiple layers.

114. Dr. Lee goes on to claim “[a] POSITA would have recognized that separating dummy BSG into sub-dummy BSGs, for example by using dielectric trenches, would have the potential to help the dummy BSGs in serving their purposes. This is because the loading effects on a specific sub-BSGs is reduced and more symmetrical. Separating dummy BSG into sub-dummy BSGs also would have had the potential to reduce the load on the drivers associated with each of the various sub-units.” Ex. 1003, ¶281. I disagree. These statements are not supported by the cited reference. He does not address, for example, why “the loading effects” on a specific sub-BSG would be “reduced and more symmetrical,” or why “the load on the drivers associated with each of the various sub-units” would be reduced. It is not possible to discern the reasoning for these purported benefits from Dr. Lee’s

declaration. In fact, the word “load” in connection with this issue only appears in the above quotes. Without properly explaining how the proposed modification provides the purported benefits, Petitioner does not show that a POSITA would have been motivated to make said modification.

115. Petitioner also does not explain how a POSITA would have achieved this modification in Park’s device. Park specifically discusses forming isolation regions in its first sacrificial layer and subsequently forming the remaining layers on top. Park, 12:65-13:7. Forming deeper isolation regions would have required etching through multiple layers composed of different materials, rather than a single layer composed of one material. Etching through multiple layers of different materials requires etching methods beyond using an etchant that is selective between two materials, such as timed etching, which is not at all contemplated by Park. Petitioner does not address these challenges, let alone attempt to explain how a POSITA would have overcome them.

116. Accordingly, Petitioner does not show that Park discloses or renders obvious dummy BSGs that are separated by the first dielectric trenches into a plurality of dummy sub-BSGs.

E. Claim 11: Park Does Not Disclose “One or More Dummy TSGs That Are Formed Between the Plurality of Word Lines and the TSG, Separated by the One or More Second Dielectric Trenches into a Plurality of Dummy Sub-TSGs”

117. Park does not disclose or render obvious “one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs” because a POSITA would not have been motivated to add dielectric trenches in the proposed manner.

118. First, as explained above regarding claim 2, Park does not disclose any dielectric trenches formed in the alleged TSG (SSL), and Petitioner has not shown that it would have been obvious to modify Park to include any such trenches.

119. Second, Petitioner has not shown that it would have been obvious to have those trenches pass through dummy TSGs as Petitioner proposes. Pet. 56-57. For this modification Petitioner refers to the reasons relating to claim 10 (Pet. 56), which are incorrect as discussed above.

120. Third, Petitioner asserts that a POSITA would have used “at least some of the adjoining dummy layers” as buffer to ensure that the etching of the purported trenches in the SSL “does not reach the word lines.” Pet. 57. Petitioner’s reasoning is not supported by the evidence and relies entirely on conclusory statements by Dr. Lee.

121. Dr. Lee asserts that in the process of etching trenches into Park's SSL (which Park does not disclose), a POSITA would have used a timed etch (Ex. 1003, ¶289), which is an etch process that is left to proceed for a specific, carefully determined length of time and then is stopped before it etches any further and damages the device. However, due to the "problems [that] can arise when using a timed etch," as Dr. Lee says (Ex. 1003, ¶289), a POSITA would have been dissuaded from using a timed etch to enable Park to be modified to form isolation regions in the SSL.

122. In addition, Park discloses using selective etching. Park, 12:59-61, 13:4-11. A selective etch is an etch process that is designed to etch a target material at a rate significantly faster than a non-target material, permitting the etch to "stop" very precisely on a particular layer. In the case of Park, a POSITA would recognize that multiple layers of materials with two different etch selectivities (as specified by Park, 13:4-15) would permit a variety of different recipes, which could accurately "stop" on any specific layer.

123. Dr. Lee asserts that due to the uncertainties involved in timed etching, a POSITA would have employed the dummy SSL layers as a buffer (Ex. 1003, ¶¶290-291), but rather than presenting examples of this practice in contemporaneous literature, Dr. Lee's citation of Ex. 1021 merely provides an example where a

dummy gate electrode is also referred to as a buffer gate electrode without identifying a connection with etching. Ex. 1021, [0060].

124. Further, Dr. Lee does not explain how this process would result in the dummy SSL being separated into multiple dummy sub-SSLs, as claim 11 requires. If a dummy SSL were used as a buffer in the process of etching isolation regions in the alleged TSG above it, the intention would be that the buffer (i.e., the dummy SSL) is at most only partially etched—i.e., merely enough to ensure that the actual target of the etch (the alleged TSG above it) is etched all the way through. If the etch were allowed to go completely through the dummy SSL, then it would start to etch the word line below it. This would risk damaging the word line and therefore would defeat the purpose of using a buffer layer in the first place. In short, using the dummy SSL as a buffer would result in it remaining as a single connected unit—at most only partially etched—rather than separating the dummy SSL into dummy sub-SSLs as required by claim 11.

125. Accordingly, Petitioner does not show that Park discloses dummy TSGs that are separated by the second dielectric trenches into a plurality of dummy sub-TSGs.

XI. PETITIONER’S GROUND 2: PARK IN VIEW OF SHIBATA DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-11

126. For the reasons explained below, it is my opinion that Park in view of Shibata does not disclose or render obvious the Challenged Claims at least because

(1) Shibata does not address the deficiency of Park with respect to Limitation [1.e], and (2) Petitioner has not shown that a POSITA would have been motivated to apply Shibata's disclosures to Park. And as to the added limitations of claims 10-11, Petitioner does not rely on Shibata to address the deficiencies described for Ground 1, and so Ground 2 fails for the same reasons.

A. Independent Claim 1: The Combination of Park and Shibata Does Not Render Obvious Limitation [1.e]

127. Petitioner does not show that Park in view of Shibata renders obvious limitation [1.e] for at least three reasons: (1) Shibata does not address the deficiencies in Park and therefore the combination does not render obvious dielectric trenches “formed in the BSG,” (2) the combination also does not render obvious dielectric trenches that “extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” and (3) Petitioner does not show that a POSITA would have been motivated to apply Shibata's disclosures to Park. Pet. 58 (citing Shibata, [0090], [0166], Fig. 16).

(a) Shibata's Separation Portions Are Not “Formed in the BSG” and Do Not “Extend[] in a Length Direction of the Substrate to Separate the BSG Into a Plurality of Sub-BSGs” (Limitation [1.e])

128. Park in view of Shibata does not cure the deficiency of Ground 1 because Shibata's separation portions 62a, which Petitioner proposes adding to Park, contribute to the separation of only the top select gate and not the bottom select gate.

Thus, the addition of Shibata still does not result in a dielectric structure that is (1) “formed in the BSG” and (2) “extend[s] the length direction of the substrate to separate the BSG into a plurality of sub-BSGs” as required by Limitation [1.e].

129. For the reasons set forth in §X.A, Park does not disclose or render obvious “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.” In Ground 2, Petitioner attempts to address these deficiencies by applying disclosures from Shibata to Park’s memory device. Petitioner’s Ground 2, however, does not cure the identified problems I discuss above.

130. Petitioner relies on certain disclosures of Shibata’s first and second embodiments. Pet. 58-59; Shibata, [0016], [0047]. Petitioner asserts that Shibata, as depicted below, discloses “multiple ‘separation portion[s] 62a’ [that] pierce[] the drain-side select gate layer of the uppermost layer of the multiple conductive layers 70. ... This divides Shibata’s upper TSG (the drain-side select gate layers) into sub-TSGs (portions SDG0-SGD3)”:

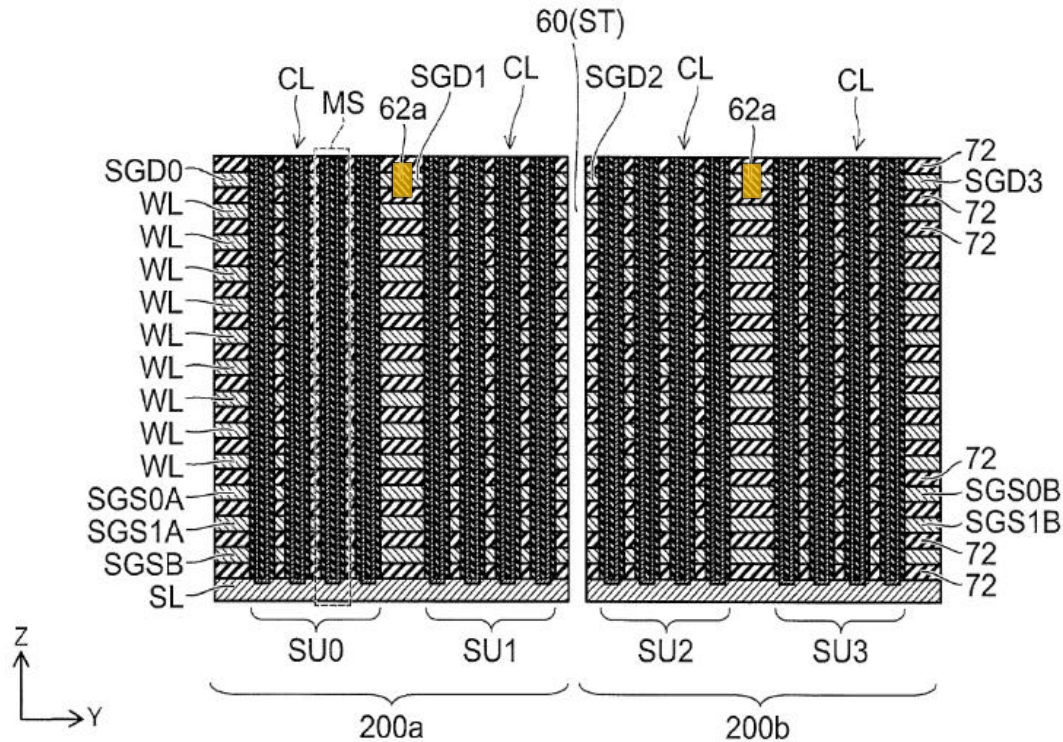


FIG. 16

Shibata, Fig. 16 (annotated); Pet. 58 (citing Shibata, [0090], [0166], Fig. 16). Petitioner further contends that “Shibata’s “separation portion[s] 62a” traverse the entire length of its memory device for purposes of dividing the select gates.” Pet. 59 (citing Fig. 47A).

131. Petitioner then contends that based on the disclosures of Shibata, “a POSITA would have eliminated Park’s second common source lines 105 and replace[d] them with **longer isolation insulating regions 111** with **dimensions analogous to Shibata’s separation portions 62a**.” Cf. Pet. 59-60. According to Petitioner, the “lengthened isolation insulating regions 111” would “span the length

of its device to completely, and by themselves, separate its BSG (the lower GSL) into sub-BSGs” as purportedly illustrated in Petitioner’s figure:

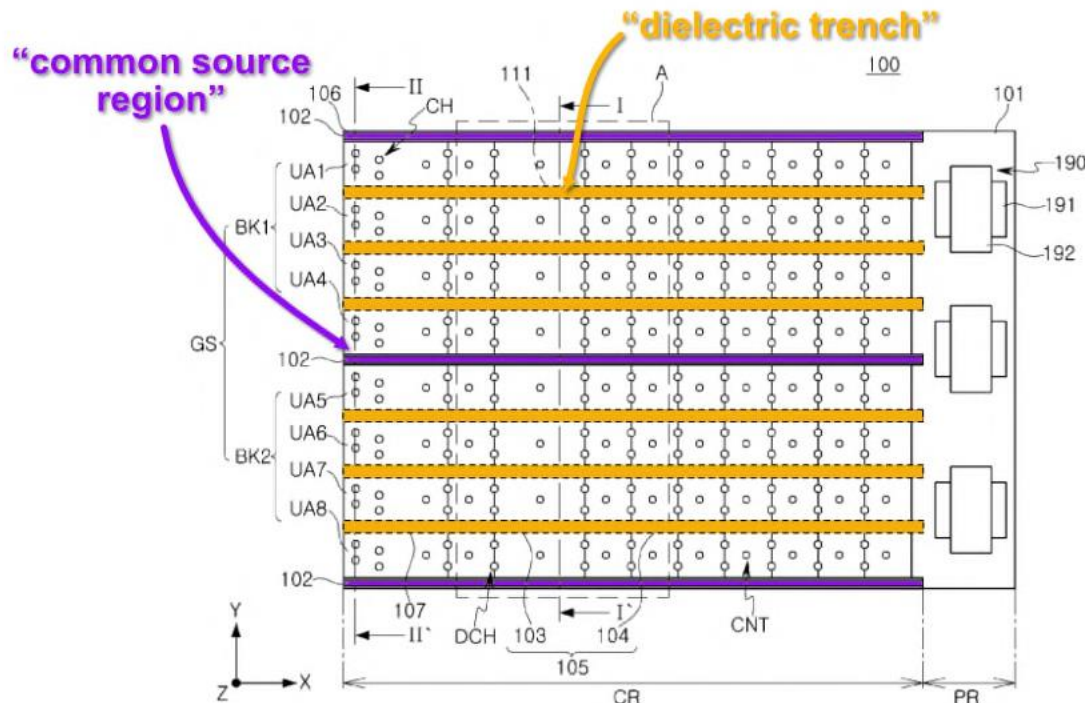


FIG. 3

Pet. 60 (modifying Park, Fig. 3).

132. Contrary to the Petitioner’s arguments, however, the resulting device does not meet the claims because Shibata discloses that its **separation portions 62a** traverse only the **uppermost** drain-side select gate layer of the memory stack, such that they contribute to the separation of only the **top** select gate, rather than the **bottom** select gate. For example, Shibata discloses that the separation portion 62a “divides the drain-side select gate layer into a first drain-side select gate SGD0 and a second drain-side select gate SGD1” of one sub-block and “divides the drain-side select gate layer into a third drain-side select gate SGD2 and a fourth drain-side

select gate SGD3,” in another sub-block, as depicted in Figure 16. Shibata, [0166].

Shibata discloses that, as can be seen in Figure 16, the separation portion 62a does not extend further to divide the source-side select gate layers (labeled “SGS0A,” “SGS1A,” “SGS0B,” “SGS1B,” and “SGSB” in Figure 16, below).

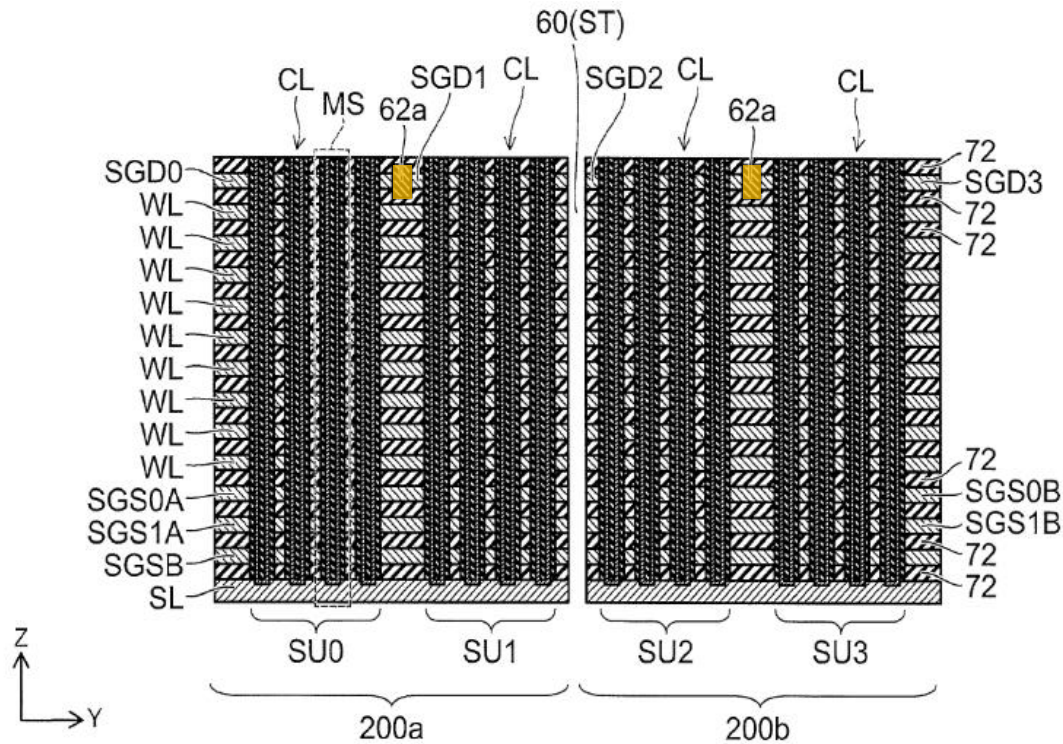


FIG. 16

Shibata, Figure 16.

133. Shibata provides no disclosure that its **separation portions 62a** also traverse the lower source-side select gate layers such that they separate the bottom select gate layers. Nor does Shibata disclose adding additional **separation portions 62a** to the source-side select gate layers to separate the bottom select gate layers.

Indeed, Shibata says to not to extend the separation portions 62a to divide additional conductive layer, such as a bottom select gate:

“The separation portion 62a is disposed between the first string unit SU0 and the second string unit SU1 adjacent to each other in the Y-direction, **pierces only the drain-side select gate layer of the uppermost layer** of the multiple conductive layers 70, **and does not divide the other conductive layers** of the multiple conductive layers 70.”

Shibata, [0137]. In other words, Shibata discloses that separation portions 62a do **not** divide the bottom select gate layers, which are on the drain-side and are conductive layers of a memory device. Thus, Petitioner’s cited disclosures from Shibata that disclose separating the top select gate layers do not provide the disclosures that are missing from Park. *See generally* Pet. 58-61.

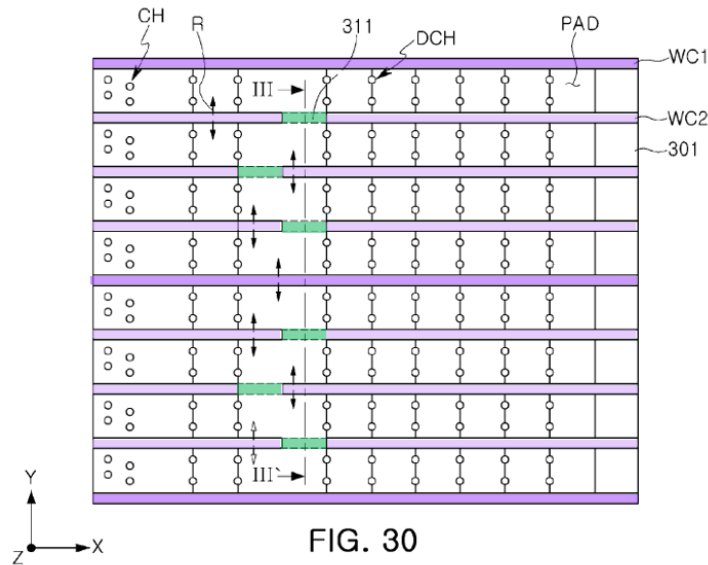
134. Accordingly, Petitioner does not show that Park in view of Shibata render obvious an isolation insulating layer (1) formed in the BSG and (2) extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.

(b) A POSITA Would Not Have Been Motivated to Apply Shibata’s Teachings to Park

135. In addition, by proposing a combination based on hindsight and misinterpretation of the references, Petitioner also does not show that a POSITA would have been motivated to make the proposed modifications to Park in view of Shibata’s disclosures.

136. A POSITA would not have been motivated to make Petitioner's proposed combination because Park says to not to make such a combination. Park discourages elongating the isolation insulating layers because the longer paths by which the etching solution must flow could prevent the complete removal of the sacrificial layer and cause voids in the gate electrode layers GLs. See Park, 15:35-16:49. Moreover, Park discourages placing isolation insulating layers side-by-side, as they are in Petitioner's modified Figure 3 of Park reproduced above, because it would block the flow of etching solution from the sides and again prevent the removal of sacrificial layers and formation of active layers. *Id.*

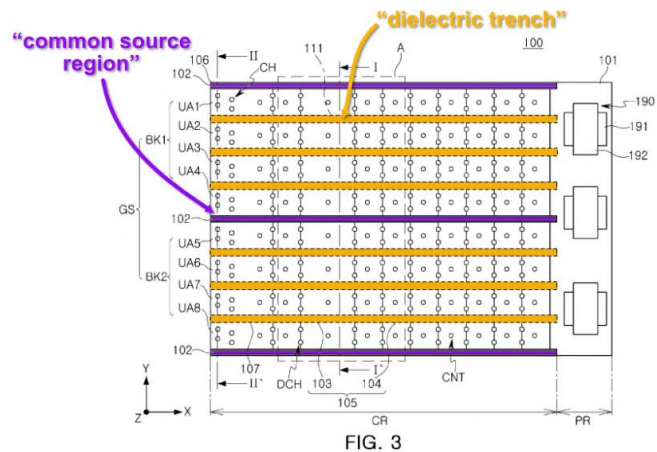
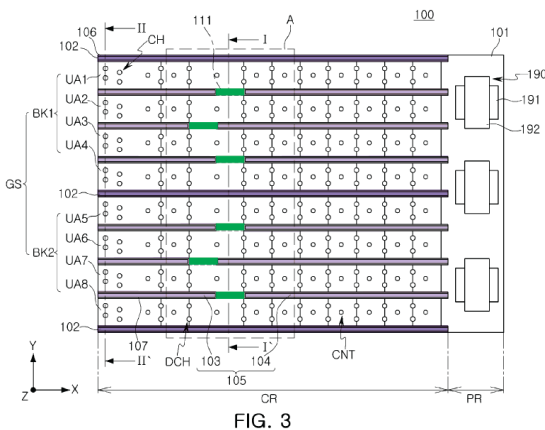
137. To explain these issues further, and with reference to Figure 30, Park discloses that sacrificial layers SL are "removed by an etching solution flowing through the first and second **word line cuts WC1 and WC2**." Park, 15:35-37. These "**word line cuts WC1 and WC2**" correspond to the "regions in which common source lines" 102 and 105 are subsequently formed. Park, 15:20-22. In other words, the openings that later form the first and second common source lines are first used as the passage through which etching solution is administered to remove the sacrificial layers. These same **word line cuts WC1 and WC2** are also used to deposit conductive material in the openings left by the removal of the sacrificial layer in order to later form the gate electrode layers GL. Park, 16:38-40.



The problem recognized by Park is that the “**isolation regions 311**” (corresponding to Park’s Figure 11’s **isolation insulating layer 111**) prevents the flow of the etchant and conductive materials, which is the reason for their short length. See Park, 15:54-55 (referring to “relatively long [flow] path above the isolation regions 311 in which the second word line cuts may be separated from each other”). That is, the problem is two-fold: first, because there is no word line cut in any of the layers above the isolation insulating layer, the flow path is relatively long; and second, because etching solution and metal do not flow through isolation insulating layers, there is no flow to regions between isolations insulating layers. See Park, Fig. 30 (illustrating the “inflow passage R” stemming from each of the word line cuts). Thus, where the “inflow passage of the [etching solution] is not properly secured, a portion of the sacrificial layer SL may remain without being removed.” Park, 15:56-59. Similarly, this may generate a “void” when depositing the conductive material to

form the BSG and word lines, the very same defect that Park seeks to avoid during fabrication. Park, 16:44-49.

138. Thus, Park says that Petitioner's proposed modification—which replaces short **isolation insulating layers 111** with much longer **dielectric trenches**, as illustrated below—would result in a memory device that, due to long flow paths, has missing BSG where the sacrificial layer SL between the isolation insulating regions is never removed, and has poorly formed word lines in the regions above the much longer proposed **dielectric trenches**.



Park, Fig. 3 (left is the unmodified version annotated by Patent Owner; right is Petitioner's demonstrative at Pet. 60 modifying the figure).

139. Indeed, Park is so concerned with this problem that, even for its short isolation insulating layers 111 (which are only as long as the distance between dummy channel and contact), Park proposes staggering the **isolation insulating layers 111**, as shown below. Park, 15:60-16:2. Staggering, however, is not possible

when the isolation insulating layers are modified to span the entire memory array as proposed by Petitioner.

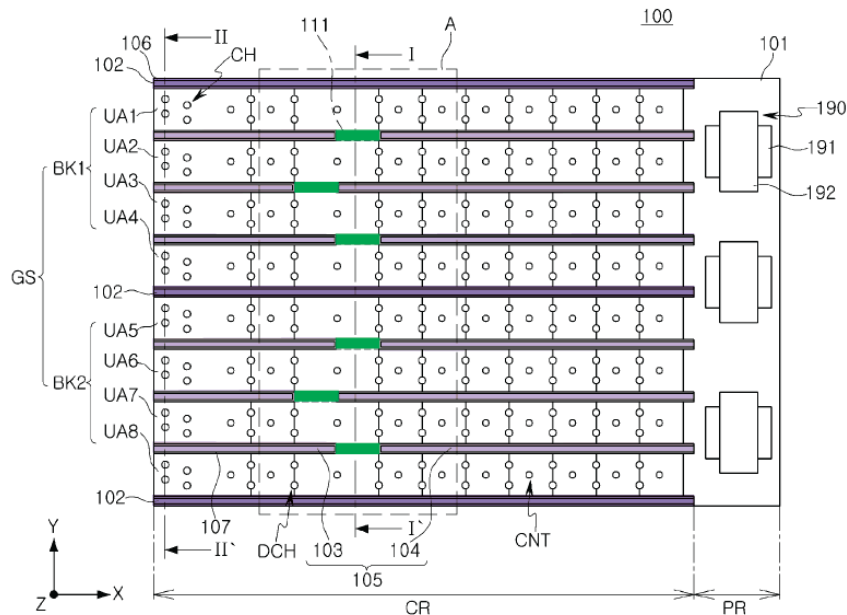


FIG. 3

Park, Fig. 3 (annotated).

140. Petitioner’s argument that Shibata resolves the operability problem by providing “drive circuits” (Pet. 62) is wrong for several reasons. Shibata provides no solution to Park’s concern that longer isolation insulating layers facing one another could prevent effective replacement of the sacrificial layer and generate voids in the BSG and word lines. *See* Park, 9:31-35, 15:56-49, 16:44-49. Shibata also does not disclose connecting multiple “drive circuits” to the source-side select gates, which are positioned in the harder to reach bottom layers of the stack, but instead discloses connecting multiple drivers to the drain-side select gates which are

at the top of the stack. *See* Shibata, [0447]-[0448]. Finally, Shibata’s driver configuration is a fixed solution (which entails permanently connecting two drive circuits to certain drain-side select gates and only one drive circuit to others). *See* Shibata, [0447]-[0448]. As a fixed solution, connecting multiple drivers to certain drain-side select gates is practical for addressing predictable differences in resistances recognized by Shibata. Shibata, [0325] (recognizing that the “resistance of the drain-side select gate not adjacent to the slit ST easily can be higher than the resistance of the drain-side select gate adjacent to the slit ST”). Shibata’s fixed solution, however, is not practical for addressing unpredictable variations in word line quality due to variations in efficient flow paths, which is what would be introduced by Petitioner’s proposed modification.

141. Petitioner’s backup argument—“replacing some, but not all, of Park’s common source lines” (Pet. 62-63)—is also flawed. As illustrated below, even in Petitioner’s drawing there remains the problem facing isolation insulating layers (highlighted in teal) where there is no flow path from the “common source region” (marked purple by Petitioner):

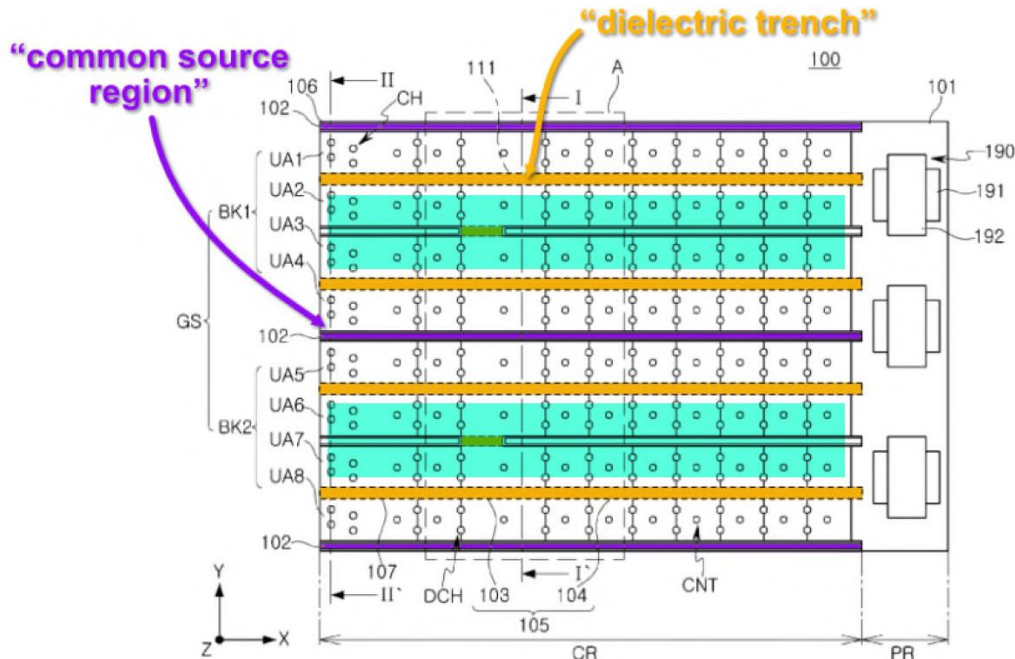


FIG. 3

Park, Fig. 3 (annotated by Petitioner at Pet. 63).

142. And to the extent it is argued that it would have been obvious to alternate placement of Park’s common source lines and the modified isolation insulating layers, this would still exacerbate the ineffective etching above these extended isolation regions that Park cautions against. Park explains that the “path above the isolation regions [] in which the second word line cuts WC2 may be separated from each other” will be “relatively long.” Park, 15:53-56. Replacing even some of the common source lines with long dielectric trenches that block the inflow passage of the etchant goes directly against Park’s repeated warnings that “a portion of the sacrificial layers SL may remain without being removed.” Park, 15:56-59; *see also* 15:60-16:2, 16:38-49.

143. A POSITA further would not have been motivated to replace Park's second common source lines 105 with longer isolation insulating regions 111 analogous to Shibata's separation portions 62a because doing so would reduce the number of common source lines in the memory device. Instead of having a total of eight common source lines (*see* Park, Fig. 3 depicting two first common source lines 102 and six second common source lines 105), the proposed combined system would eliminate six second common source lines, leaving only two first common source lines. This results in a 75% reduction in the number of common source lines.

144. A POSITA would have understood that reducing the number of common sources lines would have several adverse effects on the memory device:

- It causes higher resistances in the remaining source lines leading to degraded read and write speeds. *See e.g.*, Ex. 2002, 6 (explaining that CSLs should be “lines of low resistance” as to not adversely impact memory speeds).
- It increases heat generation and associated failure mechanisms due to higher currents carried in the remaining source lines. *See e.g.*, Ex. 2005, 2 (stating that “[h]igher current densities ... give rise to greater heat generation and combine to increase electromigration failures”), Ex. 2006, 8 (stating “heat generation in [a] semiconductor increases as the current density increases”).

- It increases electrical stress on the remaining source lines leading to a reduced device lifespan. *See e.g.*, Ex. 2004, 6-7 (stating “higher current densities may contribute, directly or indirectly” to device degradation).
- It causes significant voltage drops across the remaining source lines, adversely affecting the accuracy of reading, writing, programming and erasing operations of the memory device. *See e.g.*, Ex. 2001, 5 (stating “[d]ecreasing the CSL resistance can reduce the CSL noise”), Ex. 2003, 2-3 (explaining that voltages on the CSL can impact the memory device speeds, degrading read speed, and causing increased noise).
- It increases crosstalk leading to more signal interference and increased error rates.

145. While reducing the number of common source lines may lead to a reduction of the memory array area, this would only exacerbate the very problem that Park intends to avoid. Specifically, reducing the number of common sources lines would only increase the long “inflow paths” that Park is concerned with shortening (Park, 9:40-48, 10:13-16, 11:52-55, 12:30-38, 12:47-52, 15:53-59, 15:60-16:2, 16:38-49) and thus worsen any problems with etching of the sacrificial layer and deposition of the gate layers, such as forming of defects or voids (Park, 9:40-48, 11:52-55, 12:30-38). A POSITA, therefore, would not have simply removed source

lines because any purported benefit from reducing the memory array would have come at a significant trade-off in memory device performance, including in speed, thermal management, reliability, longevity, accuracy, and device scalability, which Petitioner does not address. Accordingly, a POSITA would not have been motivated to modify Park as to remove the second common source lines, as Petitioner's proposed combined system requires.

146. Thus, Petitioner does not show that a POSITA would have been motivated to modify Park in view of Shibata.

B. Claims 10-11: Park in View of Shibata Also Does Not Render Obvious These Claims

147. Petitioner does not rely on Shibata for the claimed dummy BSGs or TSGs, and does not include any additional analysis of these elements beyond its analysis in Ground 1 (Park), and therefore these claims are not met for the same reasons discuss for Ground 1.

XII. PETITIONER'S GROUND 3: PETITIONER DOES NOT SHOW THAT SHIBATA IN VIEW OF PARK DISCLOSES OR RENDERS OBVIOUS CLAIMS 1-11

148. For the reasons explained below, it is my opinion that Shibata in view of Park does not disclose or render obvious the Challenged Claims at least because Petitioner has not shown that a POSITA would have been motivated to apply Park's disclosures to Shibata. And as to the added limitations of claims 10-11, Petitioner

does not rely on Shibata to address the deficiencies described for Ground 1, and so the Ground 3 fails for the same reasons.

A. Independent Claim 1: Petitioner Does Not Show That a POSITA Would Have Been Motivated to Apply Park’s Teachings to Divide Shibata’s Lower Gate Layer into Multiple Portions

149. Petitioner does not show that a POSITA would have been motivated to make the proposed modifications to Shibata in view of Park.

150. Ground 3 of the Petition incorrectly argues that Shibata in view of Park renders the Challenged Claims obvious. Petitioner generally relies upon the disclosures of Shibata for each of the limitations, but for limitation [1.e], the Petition sets forth two problematic modifications to Shibata’s memory in light of Park’s disclosures.

151. For each of limitations [1.b], [1.c], [1.d], and [1.f], which recite a “bottom select gate” (BSG), Petitioner argues that the “lower source-side select gate or SGS layers” of Shibata’s second embodiment is the bottom select gate BSG, as illustrated below:

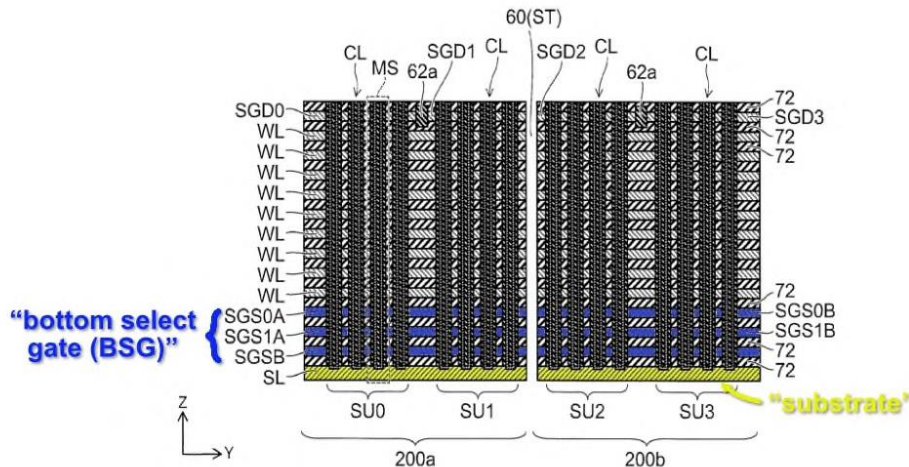
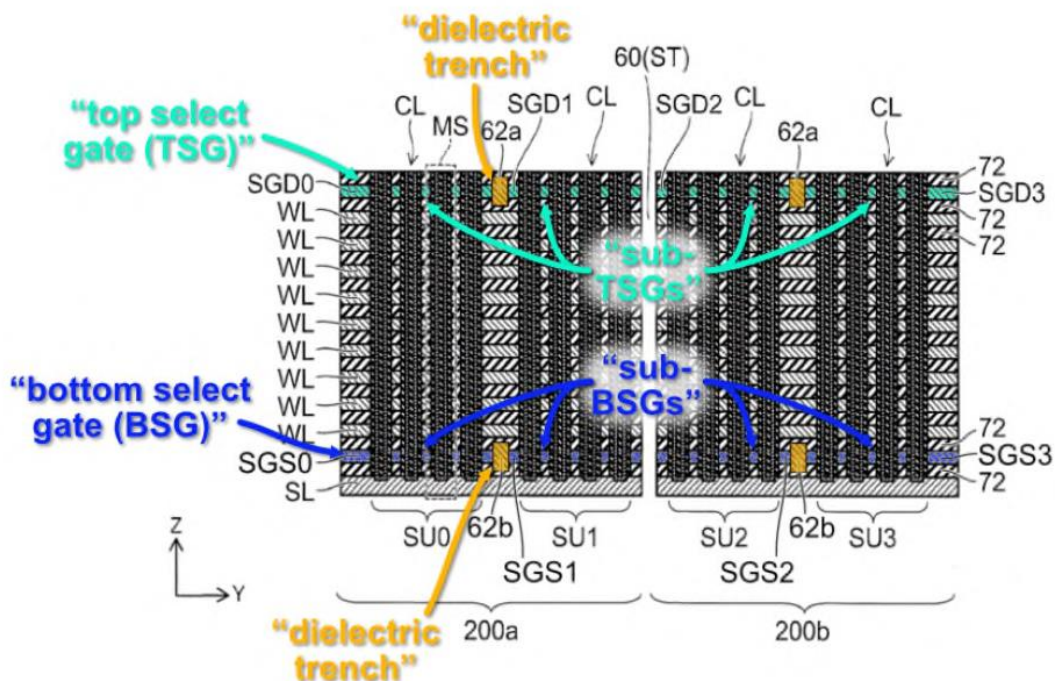


FIG. 16

Pet. 65-67 (Petitioner’s annotations). (Note that Shibata uses the acronym “SL” to refer to “source layer,” Shibata’s purported substrate, whereas Park uses the same acronym, SL, to refer to “sacrificial layer.”) As shown in the above figure, the purported bottom select gate includes three layers: “SGS0A,” “SGS1A,” and “SGSB.” Shibata’s three lower source-side select gates provide selective connection of the four string units SU0-SU3 to the source layer without relying on a dielectric trench. See Shibata, Fig. 16, Fig. 22A, [0196]-[0218]. For the purposes of limitation [1.e], which recites “one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs,” Petitioner further relies on Shibata’s disclosures of “separation portions.” Pet. 72 (citing Shibata, [0107], [0110]). Shibata, however, says that these separation portions “pierce[] only the drain-side select gate layer of the **uppermost**

layer of the multiple conductive layers 70”—not the source-side select gate layers, which are the **lowermost** layer(s). Shibata, [0090].

152. Recognizing this shortcoming of Shibata, Petitioner abandons its mapping of Shibata for limitations [1.b], [1.c], [1.d], and [1.f] and argues for limitation [1.e] that a POSITA would have found it obvious to do two things: (1) rather than dividing just the upper drain-side select gates using separation portions 62a, Shibata would employ “new additional separation portions 62b” to also divide the BSG into sub-BSGs (Pet. 74); and (2) rather than employ multiple lower source-side select gate layers, “Shibata would employ a single ‘bottom select gate (BSG)’” (Pet. 74-75). This proposed modification is illustrated in the Petition’s reimagined diagram:



Pet. 76 (Petitioner's demonstrative).

153. These modifications to Shibata (Pet. 74-75, reflecting Lee, ¶¶ 381-384) are modifications to Figure 16 of Shibata. Figure 16 of Shibata (relating to the second embodiment of Shibata) is reproduced below, as a reminder that this embodiment uses three select source gate layers at the bottom of the stack, not just one.

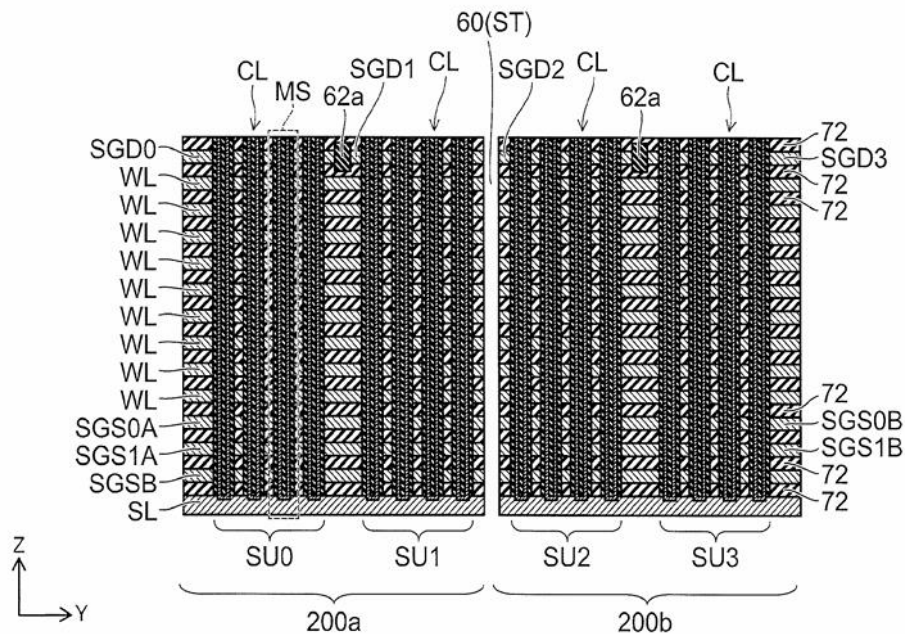


FIG. 16

Shibata, Fig. 16.

154. Moreover, Figure 16 (and the related second embodiment) follows a general disclosure of Shibata where “n” strings require “a plurality of layers of word lines and (n-1) layers of select gate layers.” Shibata, Abstract. Saying this another way, Shibata says that the selection of additional NAND strings should be done by adding additional select gate layers rather than by adding additional trenches. As a

specific example, Figure 16 (which is part of the Figures 16-22 of the second embodiment, and also is the figure modified by Dr. Lee) discloses that three gate select source layers (and one gate select drain layer) are necessary when the device is divided into 200a and 200b sub-blocks with two string units in each block. More tellingly, Figures 17-22 (also in the second embodiment) increases this to five gate select source layers (and one gate select drain layer) when there is a single 200 block with four string units.

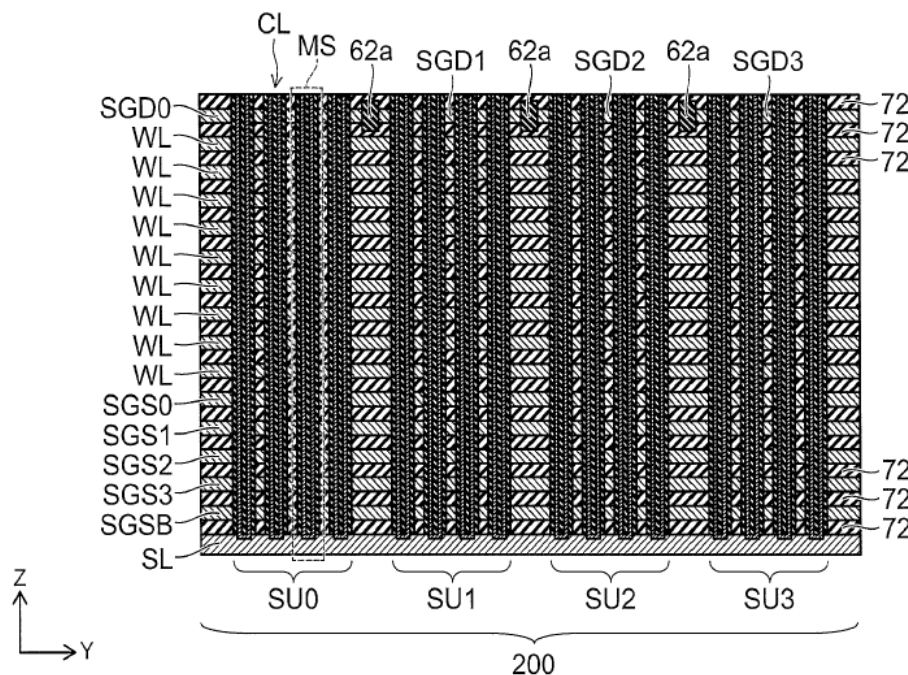


FIG. 19

Shibata, Fig. 19. As such, the concept proposed by the Petitioner (namely that “Shibata would employ a single ‘bottom select gate (BSG)’”) is directly opposed to the disclosures of Shibata (even for the embodiment that the Petitioner attempts to use to illustrate the concept).

155. Moreover, Petitioner’s proposed modifications to Shibata rely upon the flawed premise that Park provides an alternative to Shibata’s multiple bottom select gates, which “facilitate control on a string unit basis” and thus would motivate the changes. Pet. 74-75. Specifically, Petitioner points to Park’s isolation insulating layers 111 that purportedly “divide[] a single lower gate layer into multiple portions.” Pet. 75 (citations omitted). But Petitioner’s obviousness argument is incorrect for several reasons.

156. First, Petitioner’s primary motivation is that “[w]hile the multiple bottom select gates can facilitate control on a string unit basis, a POSITA would have recognized that they require additional manufacturing steps and make Shibata’s memory array taller” and that this would have motivated consideration of other design alternatives like Park. Pet. 74-75 (*citing* Ex. 1003, ¶¶ 377-380). Neither Petitioner nor its expert explain how Park achieves a reduction in manufacturing steps, particularly given that etching and replacing portions of the bottom select gate with insulating material would add additional manufacturing steps at the same time that other steps are removed.

157. Second, Petitioner attempts to equate Park’s isolation insulating layers 111 and Shibata’s separation portion 62a. As described in greater detail in relation to Ground 1, Park’s isolation insulating layers are not extensive trenches that separate the bottom gate structure, but instead are short sections that just “close the

gaps in common source lines 105.” Pet. 31. Moreover, Park’s isolation insulating structures are in an entirely different region of the memory than Shibata’s separation portions. As I explain above, Park’s **isolation insulating structures** are short structures in the staircase region, not in the array region:

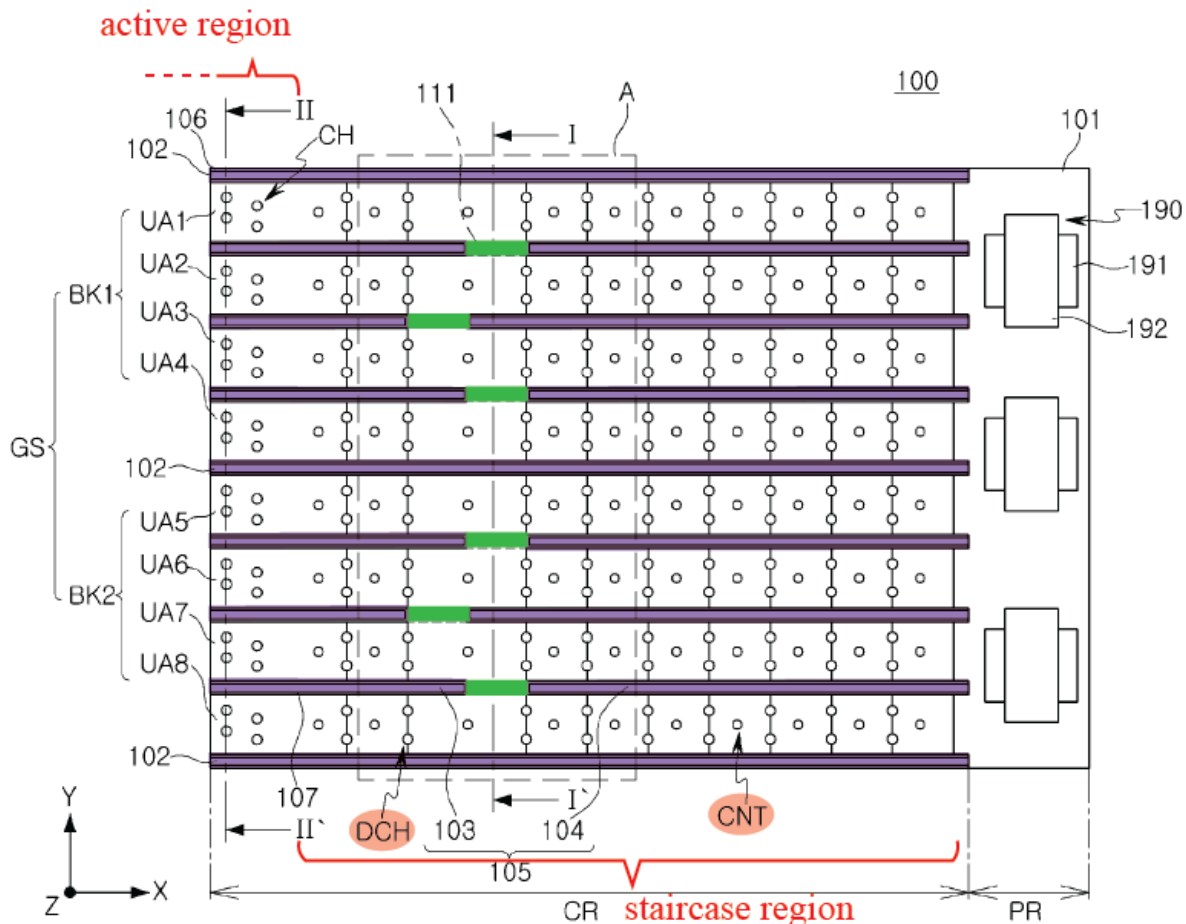


FIG. 3

Park Fig. 3 (showing **isolation insulating structures 111** between dummy channel structures (DCH) and an adjacent contact (CNT) to the word lines in the staircase region, not the active region); *see also* Park, 10:56-60 (“The isolation insulating layer 111 may be disposed below the connecting electrodes 129b to 129i connecting

the unit electrodes of the gate electrode layers 120, forming the word lines, to each other.”). On the other hand, Shibata’s **separation portions** extend the length of the array region of the memory device:

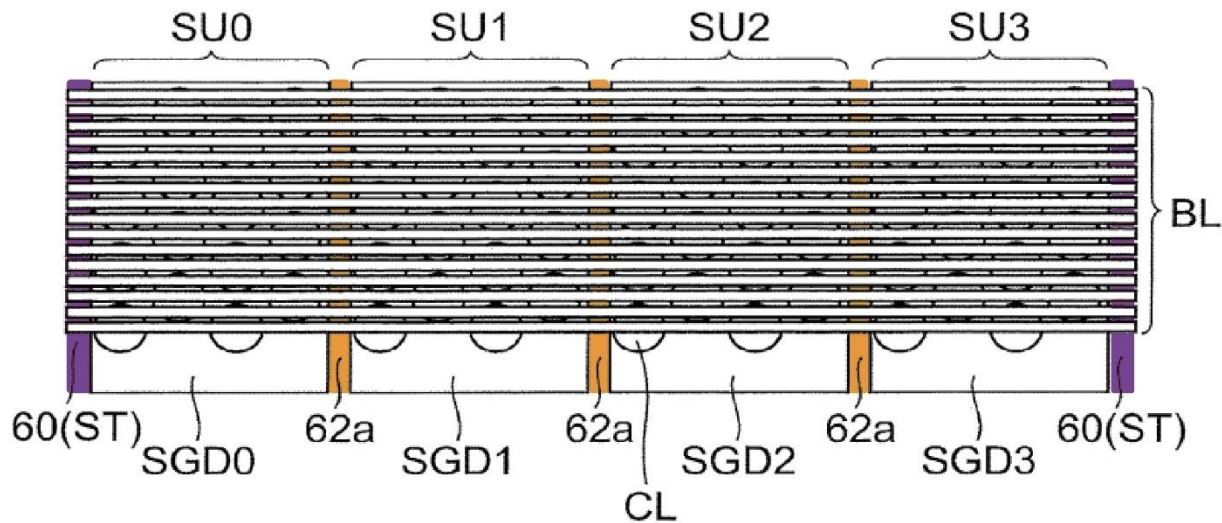


FIG. 47A

Shibata, Fig. 47A.

158. Indeed, as Petitioner admits, “Shibata does not reference a staircase” (Pet. 69), and so even if a POSITA would have recognized that Shibata’s three-layer bottom gate design “require[d] additional manufacturing steps and ma[de] Shibata’s memory array taller” (Pet. 74), that does not mean a POSITA would look to Park’s unrelated disclosure directed to short isolation insulating structures 111 in the staircase region—a region Shibata does not even have—to modify Shibata.

159. Third, I also disagree with Petitioner’s argument that “it was well known that trenches of dielectric material could be used to divide select gates” (Pet.

78). Not one of the four references cited by Petitioner shows that it was well known to use trenches to divide both the top and bottom select gate (as set forth by Ground 3). Indeed, three of them do not even disclose using the purported dielectric trenches in the bottom select gate. *See* Ex. 1016, 6:5-15, 10:15-18, Fig. 4A (employing a “insulating layer 173” in the “uppermost gate electrode layer 136”); Ex. 1017, 7:40-42, Fig. 3 (“employing a “cutting insulation pattern 118” in the upper “string selection gate electrodes 202.”); Ex. 1018, [0058], Fig. 4B (employing “insulating separation pattern 50” in the “upper electrodes ELb located at the highest level”). As for the fourth reference, it discloses similar isolation insulating regions as Park, which are no more than short sections in the staircase region. *See* Ex. 1019, Figs. 21-22, Fig. 24, [0154], [0160]-[0161]. As such, none of the references cited by Petitioner or Petitioner’s expert provides a motivation to modify Shibata’s separation portions to divide both upper drain-side select gates and lower source-side select gates.

160. Lastly, Petitioner’s argument that the proposed combination “would reduce the number of needed manufacturing steps” is unsupported by the evidence. Pet. 77. Once again, the only support cited by Petitioner is a near-identical statement by its expert. Neither Petitioner nor its expert cite any evidence. Indeed, on the face of it, the statement is wrong. The proposed combination, which requires the formation of additional separation regions 62b in the source-side gate layer, would

at minimum require additional photolithography steps, etching steps, and filling procedures that neither Petitioner nor its expert considered. For example, Shibata teaches forming a simple stacked structure for the bottom of the stack:

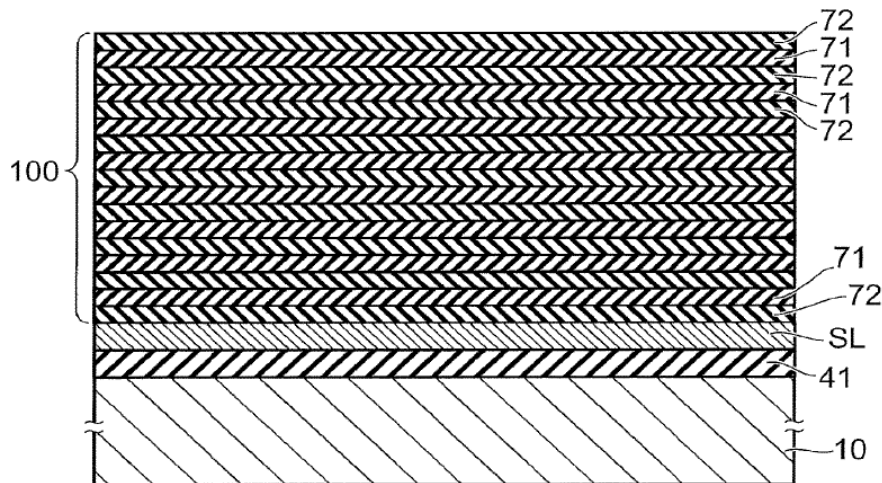


FIG. 8A

Shibata, [0104], Fig. 8A. To modify Shibata to include separation regions to divide the alleged BSG at the bottom of the stack, the formation of the stacked body 100 would have to be disrupted to, at minimum, (1) form a mask, (2) form slits by etching, and (3) form insulating material into the slits. Thus, Petitioner's combination would actually increase the number of manufacturing steps.

161. As the above reasons demonstrate, modifying Shibata to have a single-layer BSG results in significant complexity and would have further dissuaded a POSITA from applying Park's disclosures to the memory device, let alone with a reasonable expectation of success.

162. Thus, Petitioner does not show that a POSITA would have been motivated to modify Park in view of Shibata.

C. Claims 10-11: Shibata in View of Park Also Does Not Render Obvious These Claims

163. Petitioner relies on Park's disclosure of an alleged trench in the alleged BSG and TSG for these elements and its analysis is similar to its analysis of Park Ground 1 (Park), and therefore these elements are not met for the same reasons discuss for Ground 1.

II. CONCLUSION

164. For at least the reasons discussed above, it is my opinion that Petitioner has not demonstrated that any of the Challenged Claims of the '623 patent are anticipated or obvious.

165. This declaration represents my opinions that I have formed to date on the specific issues for which I have been asked to opine and based on the material currently available to me. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also, I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

166. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the

knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

APPENDIX A

CURRICULUM VITAE
Dr. Kelin J. Kuhn

CONTACT INFORMATION:

Kelin J. Kuhn
P.O. Box 609
Winthrop, WA 98862
kjkuhn@confluence-tech.com

EDUCATION:

Ph.D., Electrical Engineering, Stanford University, Stanford, CA. June 1985
M.S., Electrical Engineering, Stanford University, Stanford, CA. June 1985
B.S., Electrical Engineering, University of Washington, Seattle, WA. March 1980
(magna cum laude)

PRESENT ROLE:

**Confluence Technology Services, Winthrop, WA (kjkuhn@confluence-tech.com);
present role**

Dr. Kuhn's business (Confluence Technology Services) supports a variety of engineering services in electronics and photonics, with emphasis on CMOS and beyond-CMOS technologies.

**Cornell University, Ithaca, NY; Materials Science and Engineering (kjk236@cornell.edu)
2014 to date**

Position: Adjunct Professor
Key Collaborator: Darrell Schlom

Prof. Kuhn's role is collaborating with a diverse group of faculty (both at Cornell and elsewhere) for establishment of long-term research programs in the area of valleytronics, inverse-design, quantum materials, post-CMOS technology, and spintronics.

CLIENTS / SIGNIFICANT INTERACTIONS POST-2014:

Bayes PLLC: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *Inter Partes Review of U.S. Patent Nos. 8,803,214 And 10,475,737*.

Pillsbury Winthrop Shaw Pittman LLP: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *MicroSemi Corporation v. Commissioner of Internal Revenue*.

Ropes and Gray: Initiated 2023 and on-going. Technical evaluation and consulting on the matters related to *Yangtze Memory Technologies Company, LTD. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 5-23-cv-05792*.

Heim, Payne & Chorush: Initiated 2023 and on-going. Technical evaluation and consulting representing *Microchip Corporation* and its subsidiary *Silicon Storage Technology, Inc.* with regards to a dispute with *Taiwan Semiconductor Manufacturing Company*.

Smith Baluch LLP: Initiated 2022 and on-going. Technical evaluation and consultation to advise and assist Smith Baluch LLP matters relating to semiconductor processing.

Carter Arnett: Initiated 2022 and ongoing. Technical evaluation and consultation to advise and assist Carter Arnett PLLC in representing *Katana Silicon Technologies, LLC* in IPR2022-00763 and litigation related to Case No. 6:22-cv-00191 (W.D. Tex), adverse to *GlobalFoundries, Inc., GlobalFoundries, U.S. Inc., and GlobalFoundries U.S. 2 LLC*.

Mintz: Completed 2022-2023. Technical evaluation and consulting representing *Daedalus Prime LLC* with regards to the ITC Case: 337-TA-133, Certain Semiconductor Devices, Mobile Devices Containing Same (Taiwan Semiconductor Manufacturing Company).

Heim, Payne & Chorush: Completed 2021-2023. Technical evaluation and consulting representing *Arigna Technology Limited* with regards to IPR2021-01321 (*Volkswagen*) and IPR2021-01382 (*Infineon*).

Quinn Emanuel Urquhart & Sullivan: Believed complete 2021-2023. Technical evaluation and consulting representing *Hanwha* with regards to ITC Inv. No. 337-TA-1271.

Ropes and Gray: Completed 2021-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Lawrence and Phillips: Completed 2021-2022. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.* with regards to *inter partes* reviews (IPRs) filed by Samsung.

Wolf Greenfield: Completed 2020-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.* with regards to *inter partes* reviews (IPRs) filed by Micron.

Hueston Henningan: Completed 2020-22. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.*

Skadden Arps: Initiated 2020 and on-going. Technical consulting for the *Audit Committee of the Intel Board of Directors* on matters related to Technology Development.

PARADIM: Initiated 2016 and on-going. PARADIM's mission is to create new interface materials with unprecedented properties for the next generation of electronic devices. Dr. Kuhn

is a member of the External Advisory Committee. In this role, Dr. Kuhn provides technical and management support with regards to PARADIM operations.

Quinn Emanuel Urquhart & Sullivan: Completed, 2020-2021. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Susman Godfrey: Completed 202-2023. Technical evaluation and consulting with regards to *Arigna Technology Limited* on matters related to CMOS transistor design.

Womble Bond Dickinson: Completed, 2020. Technical consulting for KIPB LLC (formerly KAIST IP US LLC) on an *ex parte reexamination* (“EPR”) proceeding in the United States Patent and Trademark Office with regards to patent 6,885,055.

Womble Bond Dickinson: Completed, 2019-2020. Technical evaluation and consulting in the matter of *KIPB LLC v. Samsung Electronics et al.* Dr. Kuhn supported this litigation for the plaintiff as an expert witness, including completion of the Infringement and Rebuttal Reports, as well as completing a deposition conducted on the contents of the Infringement and Rebuttal Reports. This case was settled out of court in September 2020.

Lathrop Gage: Completed, 2018-2020. Technical evaluation and consulting for KIPB LLC (formerly KAIST IP US LLC) on Korean Patent 10-0458288 (Korean counterpart to US 6,885,055).

Ropes & Gray: Completed, 2018. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Qualcomm Inc. et al.*

GlaserWeil: Completed, 2016-2018. Technical evaluation and consulting in the matter of *KAIST IP US LLC v. Samsung Electronics Co., Ltd., Case No. 2:16-cv-01314*. Dr. Kuhn supported this litigation for the plaintiff as an expert witness. This included IPR proceedings (a total of 6 IPRs were presented to the PTO in this case). This also included completion and submission of the Claim Construction Declaration, the Infringement Report, and the Rebuttal Report, as well as depositions conducted on the contents of these Reports. This case went to trial June 11-15, where Dr. Kuhn presented both Direct testimony on infringement (6/12/18) and Rebuttal (6/14/18) testimony on validity.

yoR Labs Inc.: Completed. 2015-2017. yoR Labs is a medical instrumentation start-up, focusing on non-invasive medical imaging instrumentation. Dr. Kuhn served first as a member of the External Advisory Committee and later as a member of the Board of Directors. In this role, Dr. Kuhn provided technical and management support with regards to yoR labs operations.

Oregon State University, Department of Electrical Engineering and Computer Science: Completed. 2015 to 2018: Professor-courtesy. Prof. Kuhn’s role was establishment of long-term research programs in the area advanced CMOS technology and post-CMOS technology.

FORMER ROLES (2014 and PRIOR)

Intel, Portland, OR, (advanced development / research) 2008-2014 (retired in 2014)

Grade level: 12 (Fellow)

Manager: Mike Mayberry, VP

Dr. Kuhn's role was researching advanced device architectures for Intel processes in the 5-10 year time frame. While much of her work as an Intel Fellow remains proprietary, some of the public domain aspects are captured in her book *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge, 2015) and her paper "Considerations for Ultimate CMOS Scaling," (IEEE Trans. on Elec. Dev., Vol: 59, No: 7, 2012, pp. 1813 – 1828 which won the Paul Rappaport Award). She received an Intel IAA in 2008 for her work on the TriGate transistor.

Intel, Portland, OR, (45nm Device technology manager in pathfinding) 2004-2008

Grade level: 10/11 (Principal Engineer / Sr. Principal Engineer)

Manager: Mark Bohr, Senior Intel Fellow / Kaizad Mistry, VP

Dr. Kuhn's role was as device technology manager of the pathfinding team responsible for the high-k metal-gate transistor architecture for Intel's 45nm microprocessor processor technology. She received an Intel IAA in 2006 for her work on high-k metal-gate.

Intel, Portland, OR, (90nm communication process manager) 2001-2004+

Grade level: 9/10 (Sr. Engineer / Principal engineer)

Manager: Scott Thompson (was Intel Fellow at the time, now a professor at Univ. of Florida).

Dr. Kuhn's role in this time frame was Process Program Manager of the team responsible for Intel's 90nm communications process technology. Over a 4-year period, this team developed a derivative analog/RF technology (including a SiGe BJT) on top of Intel's premium 90nm microprocessor process.

Other Intel experience:

Intel, Portland, OR, (130nm front-end integration engineer) 1998-2001

Intel, Portland, OR, (0.35um front-end integration engineer) 1997-1998

Grade level: 7-9 (Sr. engineering grades)

During the 130nm generation, Dr. Kuhn was an integration engineer responsible for the isolation section of the flow. 130nm was the last of the "classic" CMOS generations, and her work in that generation was updating the isolation process. She had the satisfaction of watching the work she did in the 130nm successfully scale through 90nm, 65nm, 45nm, and 32nm, with little change in the base process.

Dr. Kuhn joined Intel on the 0.35um generation as a sustaining integration engineer in F15. She was responsible for the silicide section of the flow. Additionally, she participated in the DIVD camera chip project (Intel's historical project to build CMOS camera chips).

Other relevant experience:

Univ. of Washington, Seattle, WA (Assoc. Prof., Ass't. Prof., Res. Ass't. Prof.), 1987-1997

Dr. Kuhn held faculty positions at the University of Washington (in Seattle) for roughly a decade in the order of Research Assistant Professor (Materials Science and Engineering), Assistant Professor (Electrical and Computer Engineering), and Associate Professor (Electrical and Computer Engineering). She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. While at the Univ. of Washington, she achieved distinction in both research and teaching.

Highlights include:

- University of Washington, Distinguished Teaching Award, 1995 (UW's highest level of achievement for a faculty member)
- NSF Presidential Young Investigator award, 1991-6 (The National Science foundation is the most prestigious funding agency for faculty and the NSF PYI award is the most prestigious national level award for junior faculty).
- Single-author on a textbook, Laser Engineering, Prentice-Hall, 1998, ISBN 0-02-366921-7 (this is a mezzanine text discussing the theory and practice of building conventional and diode laser systems).

BOOKS

Laser Engineering, (sole author) Prentice-Hall, 1998, ISBN 0-02-366921-7

CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015, ISBN 978-1107043183).

BOOK CHAPTERS

“The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8.

Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616) .

AWARDS:

Elected to the National Academy of Engineering (2023)
IEEE Frederik Philips Award (2016)
IEEE Paul Rappaport Award (2013)
IEEE Fellow (2011)

Intel Achievement Awards (Intel's highest technical award): IAA 2006 (for HiK-MG) and IAA 2008 (for key contributions to Intel's 22nm TriGate technology)

Intel Divisional Awards: Turbo operation (2009), RF Vccmin (2007), TCC (2005), SCD 1213.4 SCD/ICG (2004), LAD NW/Ophir A-1 (2003), SiGe BJT (2002), Hitachi etch (2002), 2um2SRAM (2001), Gamma Test chip (2000), Certification P854.6 (1999), F15 ISO 9000 (1998)

Academic Engineer of the Year Award, Puget Sound Engineering Council, 1996

University of Washington, Distinguished Teaching Award, 1995

College of Engineering, Outstanding Faculty Achievement Award, 1994

NSF Presidential Young Investigator award, 1991-6

NSF Research Initiation Award, 1989-91

IBM Graduate Fellowship, 1983-5

Hertz Graduate Fellowship, 1982-3

National Merit Scholar, 1976-80

JOURNAL PUBLICATIONS:

49. "First principles modeling of defects in the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system", G. Greene-Diniz, K. Kuhn, P. Hurley, and J. Greer, *J. Appl. Phys.*, Vol. 121, No. 7, Jan. 2017.

48. "Doping top-down e-beam fabricated germanium nanowires using molecular monolayers," B. Long, G. Alessio Verni, J. O'Connell, M. Shayesteh, A. Gangnaik, Y.M. Georgiev, P. Carolan, D. O'Connell, K.J. Kuhn, S.B. Clendenning, R. Nagle, R. Duffy, and J.D. Holmes, *Materials Science in Semiconductor Processing*, Vol. 62, May 2017, pp. 196-200.

47. "Device Physics Modeling of Surfaces and Interfaces from an Induced Gap State Perspective," J. Wager and K. Kuhn, *Critical Reviews in Solid State and Materials Science*, Oct. 4, 2016.

46. "Adhesion Limits and Design Criteria for Nanorelays", Kevin L. Lin, Graham L. W. Cross, Peter Gleeson, Johann P. de Silva, Alejandro Levander, Jorge A. Muñoz, Chytra Pawashe, Alexis Potie, Patrick Theofanis, John J. Boland, and Dr. Kuhn J. Kuhn, *IEEE Trans. on Elec. Dev.*, Vol. 63, No. 1, Jan. 2016, 465-470.

45. Distributive Quasi-Ballistic Drift Diffusion Model Including Effects of Stress and High Driving Field, Roza Kotlyar,, Rafael Rios, Cory E. Weber, Thomas D. Linton, Mark Armstrong and Dr. Kuhn Kuhn, *IEEE Trans. on Elec. Dev.*, Vol. 62, No. 3, March 2015. Pp. 743-750.

44. Improved MOSFET characterization technique for single channel length, scaled transistors, Ferdousi, F., Rios, R., Kuhn K.J. *Solid State Electronics*, Vol. 104, pp. 44-6, Feb. 2015

43. Capacitance and Conductance for an MOS System in Inversion, with Oxide Capacitance and Minority Carrier Lifetime Extractions, Monaghan, S. O'Connor, E., Rios, R., Ferdousi, F., Floyd, L., Ryan, E., Cherhaoui, K., Povey, I.M., Kuhn, K.J., Hurley, P.K. *IEEE Transactions on Electron Devices*, Vol. 61, No. 12, pp. 4176-85, Dec. 2014.

42. First principle-based analysis of single-walled carbon nanotube and silicon nanowire Junctionless transistors, Ansari, L., Feldman, B., Faga, G., Martinez, L.C., Haverty, M.G., Kuhn, K.J., Shankar, S., Greer, J.C., IEEE Transactions on Nanotechnology, Vol. 12, No. 6, pp. 1075-81, Nov. 2013.
41. Scaling Limits of Electrostatic Nanorelays, Pawashe, C., Lin, K., Kuhn, K.J., IEEE Transactions on Electron Devices, Vol. 60, No. 9, pp. 2936-42, Sept. 2013,
40. Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors, Kotlyar, R.; Avci, U.E.; Cea, S.; Rios, R.; Linton, T.D.; Kuhn, K.J.; Young, I.A., Applied Physics Letters, v 102, n 11, March 18, 2013.
39. Effects of alternating current voltage amplitude and oxide capacitance on mid-gap interface state defect density extractions in InGaAs capacitors, Monaghan, Scott ; O'Connor, Eamon ; Povey, Ian M. ; Sheehan, Brendan J. ; Cherkaoui, Karim ; Hutchinson, Barry J. A. ; Hurley, Paul K. ; Ferdousi, Fahmida ; Rios, Rafael ; Kuhn, Dr. Kuhn J. ; Rahman, Anisur, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Vol: 31 , No: 1, 2013, pp: 01A119 - 01A119-8.
38. Considerations for Ultimate CMOS Scaling, Dr. Kuhn J. Kuhn, invited review paper, IEEE Trans. on Elec. Dev., Vol: 59 , No: 7, 2012 , pp. 1813 – 1828 (won the Paul Rappaport Award)
37. Does the low hole transport mass in <110> and <111> Si nanowires lead to mobility enhancements at high field and stress: a self-consistent tight-binding study, R. Kotlyar, T. D. Linton, R. Rios, M. D. Giles, S. M. Cea, K. J. Kuhn, Michael Povolotskyi, Tillmann Kubis, and Gerhard Klimeck, Vol: 111 , No: 12, 2012, pp 123718 - 123718-11
36. Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm, Rios, R.; Cappellani, A.; Armstrong, M.; Budrevich, A.; Gomez, H.; Pai, R.; Rahhal-orabi, N.; Kuhn, K., IEEE Electron Device Letters, Vol. 32, No. 9, 2011, pp. 1170 - 1172
35. Process Technology Variation, Kuhn, K.J.; Giles, M.D.; Becher, D.; Kolar, P.; Kornfeld, A.; Kotlyar, R.; Ma, S.T.; Maheshwari, A.; Mudanai, S., IEEE Transactions on Electron Devices, Aug. 2011, vol.58, no.8, pp. 2197-208.
34. Moore's crystal ball: Device physics and technology past the 15nm generation, Kuhn, K.J., Microelectronic Engineering, July 2011, vol.88, no.7, pp. 1044-9.
33. Variability in nanoscale CMOS technology, Kuhn, K.J., K. Sci. China Inf. Sci. (2011) 54: 936. doi:10.1007/s11432-011-4219-6 (May 5, 2011).
32. Compressive Uniaxial Stress Bandstructure Engineering for Transferred-Hole Devices, Kotlyar, R.; Giles, M.D.; Mudanai, S.P.; Kuhn, K.J.; Cea, S.M.; Linton, T.D.; Pillarisetty, R.; IEEE Elec. Dev. Lett. Vol. 31, No. 8, 2010, pp. 878-880.

31. Managing process variation in Intel's 45 nm CMOS technology, Kuhn, K., Kenyon, C., Kornfeld, A., et al. Intel Technology Journal Volume: 12 Issue: 2 Pages: 93-4 Published: 17 June 2008
30. Analytical Modeling of Output Conductance in Long-Channel Halo-Doped MOSFETs, Electron Devices, Mudanai, S.; Shih, W.-K.; Rios, R.; Xi, X.; Rhew, J.-H.; Kuhn, K.; Packan, P.;, IEEE Transactions on Volume 53, Issue 9, Sept. 2006 Page(s):2091 - 2097
29. A 90-nm logic technology featuring strained-silicon, Thompson, S.E.; Armstrong, M.; Auth, C.; Alavi, M.; Buehler, M.; Chau, R.; Cea, S.; Ghani, T.; Glass, G.; Hoffman, T.; Jan, C.-H.; Kenyon, C.; Klaus, J.; Kuhn, K.; Zhiyong Ma; McIntyre, B.; Mistry, K.; Murthy, A.; Obradovic, B.; Nagisetty, R.; Phi Nguyen; Sivakumar, S.; Shaheed, R.; Shifren, L.; Tufts, B.; Tyagi, S.; Bohr, M.; El-Mansy, Y., IEEE Transactions on Electron Devices, vol.51, no.11, Nov. 2004. p. 1790-7.
28. Integration of mixed-signal elements into a high-performance digital CMOS process. Kuhn, K.J.; Ahmed, S.; Vandervoom, P.; Murthy, A. Intel Technology Journal, no.2, 2002
27. Elevated temperature performance of pseudomorphic AlGaAs/InGaAs MODFETs. Zurek, S.J.; Darling, R.B.; Kuhn, K.J.; Foisy, M.C. IEEE Transactions on Electron Devices, vol.45, no.1, Jan. 1998. p. 2-8
26. Synthetic wide bandpass X-ray polarizers. Cross, J.O.; Bennett, B.R.; Bell, M.I.; Kuhn, K.J. Applied Physics Letters, vol.70, no.17, 28 April 1997. p. 2224-6
25. Electro-optic polymer light modulator based on surface plasmon resonance. Jung, C.; Yee, S.; Kuhn, K. Applied Optics, vol.34, no.6, 20 Feb. 1995. p. 946-9
24. A "hands-on" course in consumer electronics design. Hannaford, B.; Kuhn, K. Mechatronics, vol.5, no.7, Oct. 1995. p. 753-62 Journal Paper
23. Finite element solutions to GaAs-AlAs quantum wells with connection matrices at heterojunctions. Li, T.L.; Kuhn, K.J. Journal of Computational Physics, vol.115, no.2, Dec. 1994. p. 288-95
22. Integrated optics waveguide modulator based on surface plasmon resonance. Jung, C.; Yee, S.; Kuhn, K. Journal of Lightwave Technology, vol.12, no.10, Oct. 1994. p. 1802-6
21. Effects of spin-orbit interaction on the envelope-function equations for semiconductor heterostructures. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.50, no.12, 15 Sept. 1994. p. 8589-601
20. Effects of mass discontinuity on the numerical solutions to quantum wells using the effective mass equation. Li, T.L.; Kuhn, K.J. Journal of Computational Physics, vol.110, no.2, Feb. 1994. p. 292-300

19. Validity of the connection-matrix approach to GaAs-Al/sub x /Ga/sub $1-x$ /As quantum wells. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.49, no.4, 15 Jan. 1994. p. 2608-14
18. Optical properties due to intersubband transitions in n-type quantum wells including the effects of the exchange interaction. Sengers, A.J.; Tsang, L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.48, no.20, 15 Nov. 1993. p. 15116-22
17. Band-offset ratio dependence on the effective-mass Hamiltonian based on a modified profile of the GaAs-Al/sub x /Ga/sub $1-x$ /As quantum well. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.47, no.19, 15 May 1993. p. 12760-70
16. Use of active loads with MSM photodetectors in digital GaAs MESFET photoreceivers. Darling, R.B.; Youn, H.J.; Kuhn, K.J. Journal of Lightwave Technology, vol.10, no.11, Nov. 1992. p. 1597-605
15. Mobility of strained and dislocated In/sub x /Ga/sub $1-x$ /As semiconductor material. Kuhn, K.J.; Darling, R.B. IEEE Transactions on Electron Devices, vol.39, no.6, June 1992. p. 1288-94
14. Dislocation scattering in n-type modulation doped Al/sub 0.3/Ga/sub 0.7/As/In/sub x /Ga/sub $1-x$ /As/Al/sub 0.3/Ga/sub 0.7/As quantum wells. Zhao, D.; Kuhn, K.J. IEEE Transactions on Electron Devices, vol.38, no.12, Dec. 1991. p. 2582-9
13. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in Al/sub x /Ga/sub $1-x$ /As/GaAs/Al/sub x /Ga/sub $1-x$ /As quantum wells. Kuhn, K.J.; Iyengar, G.U.; Yee, S. Journal of Applied Physics, vol.70, no.9, 1 Nov. 1991. p. 5010-17
12. Electric field effects in AlGaAs-GaAs symmetric and asymmetric coupled quantum wells. Juang, C.; Kuhn, K.J.; Darling, R.B. IEEE Journal of Quantum Electronics, vol.27, no.9, Sept. 1991. p. 2122-8
11. Effect of etch treatment prior to Schottky contact fabrication on In/sub 0.05/Ga/sub 0.95/As. Johnson, M.J.; Kuhn, K.J.; Darling, R.B. Applied Physics Letters, vol.58, no.17, 29 April 1991. p. 1893-5
10. An enhanced and linear Stark shift in n-i-n AlGaAs/GaAs symmetric and asymmetric coupled quantum wells. Kuhn, K.J.; Cheng Juang; Darling, R.B. Journal of Applied Physics, vol.69, no.5, 1 March 1991. p. 3135-41
9. AlGaAs-GaAs multiple-quantum-well spectrally tunable photoconductors. Youn, H.J.; Darling, R.B.; Kuhn, K.J. IEEE Photonics Technology Letters, vol.3, no.2, Feb. 1991. p. 159-61
8. Effect of AlGaAs window and buffer layers on the response characteristics of GaAs photoconductive detectors. Youn, H.J.; Darling, R.B.; Kuhn, K.J. Applied Physics Letters, vol.57, no.19, 5 Nov. 1990. p. 2001-3

7. Selective etching of GaAs and Al/sub 0.30/Ga/sub 0.70/As with citric acid/hydrogen peroxide solutions. Juang, C.; Kuhn, K.J.; Darling, R.B. Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena), vol.8, no.5, Sept.-Oct. 1990. p. 1122-4
6. Stark shift and field-induced tunneling in Al/sub x/Ga/sub 1-x/As/GaAs quantum-well structures. Juang, C.; Kuhn, K.J.; Darling, R.B. Physical Review B (Condensed Matter), vol.41, no.17, 15 June 1990. p. 12047-53
5. An indium-free substrate holder for radiative heating of quarter-wafer molecular-beam epitaxy samples. Kuhn, K.J. Review of Scientific Instruments, vol.61, no.1, pt.1, Jan. 1990. p. 184-5
4. Variation in GaAs surface oxide desorption temperature as a function of shuttered aluminum oven temperature. Kuhn, K.J.; Pubanz, G.A. Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films), vol.7, no.6, Nov.-Dec. 1989. p. 3265-8
3. Static gas conduction cooled slab geometry Nd:glass laser. Reed, M.; Kuhn, K.; Unternahrer, J.; Byer, R.L. IEEE Journal of Quantum Electronics, vol.QE-21, no.5, May 1985. p. 412-14
2. The slab geometry laser. I. Theory. Eggleston, J.M.; Kane, T.J.; Kuhn, K.; Unternahrer, J. IEEE Journal of Quantum Electronics, vol.QE-20, no.3, March 1984. p. 289-301
1. Implementation of Distributed Microprocessor Systems in Custom Heavy Trucks, K.J. Kuhn, 1979-80 IEEE Student Papers, Vol. TT0114 IEEE, pg. 334-342.

CONFERENCE PUBLICATIONS

54. Bias temperature instability variation on SiON/Poly, HK/MG and trigate architectures, C. Prasad, M. Agostinelli, J. Hicks, S. Ramey, C. Auth, K. Mistry, S. Natarajan, P. Packan, I. Post, S. Bodapati, M. Giles, S. Gupta, S. Mudani and K. Kuhn, 2014 IEEE International Reliability Physics Symposium (IRPS), June 2014.
53. Semiconductors Stand Aside, the Age of Metals is Here! K. Kuhn, A. Sanchez, C. George, R. Rios, J. Clarke, J. Greer, Lester Eastman Conference, Cornell, May 2014.
52. The ultimate CMOS device and beyond, Kuhn, K.J. ; Avci, U. ; Cappellani, A. ; Giles, M.D. ; Haverty, M. ; Seiyon Kim ; Kotlyar, R. ; Manipatruni, S. ; Nikonov, D. ; Pawashe, C. ; Radosavljevic, M. ; Rios, R. ; Shankar, S. ; Vedula, R. ; Chau, R. ; Young, I. 2012 IEEE International Electron Devices Meeting (IEDM), pp. 171-174.
51. Understanding the feasibility of scaled III-V TFET for logic by bridging atomistic simulations and experimental results, Avci, U.E. ; Hasan, S. ; Nikonov, D.E. ; Rios, R. ; Kuhn, K. ; Young, I.A., Symposium on VLSI Technology (VLSIT), 2012, pp: 183 – 184.
50. Beyond the Planar Transistor: Progress in Next Generation Switches, K. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

49. Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation, K. Kuhn, INFOS 2011 (June 22, 2011, France)
48. Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET, Avci, U.E.; Rios, R.; Kuhn, K.J.; Young, I.A., IEEE Conference on Nanotechnology (IEEE-NANO), 2011 11th, pp. 869 – 872
47. Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic, Avci, U.E.; Rios, R.; Kuhn, K.; Young, I.A., 2011 Symposium on VLSI Technology (VLSIT), 2011 , pp. 124 – 125
46. CMOS scaling for the 22nm node and beyond: Device physics and technology, Kuhn, K.J., 2011 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2011 , pp. 1 – 2
45. Past, Present and Future: SiGe and CMOS Transistor Scaling. K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, ECS 2010, Oct. 10, Las Vegas, CA, USA.
44. Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, K. J. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.
43. CMOS transistor scaling past 32nm and implications on variation, K. Kuhn, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA, pp. 241-246.
42. Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, K. Kuhn, Nikkei Electronics Symposium, June 29th, 2010.
41. Technology options for 22nm and beyond, K. Kuhn, Technology, Kuhn, K.J.; Liu, M.Y.; Kennel, H.; 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.
40. CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California
39. Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.
38. Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.
37. CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

36. Future device scaling: beyond traditional CMOS, Tyagi, S., Auth, C., Ban, I., et al., 2009 2nd International Workshop on Electron Devices and Semiconductor Technology (IEDST), 1-2 June 2009, Mumbai, India, (IEDST) Pages: 4 pp. Published: 2009
35. Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.
34. Moore's law past 32 nm: future challenges in device scaling, Kuhn, K.J., 2009 13th International Workshop on Computational Electronics (IWCE 2009), 27-29 May 2009, Beijing, China, (IWCE 2009) Pages: 6 pp. Published: 2009
33. 22 nm Device Architecture and Performance Elements, K.J. Kuhn, IEEE International Electron Devices Meeting, 15-17 December 2008, San Francisco, CA, USA , IEDM short course.
32. High performance hi-k + metal gate strain enhanced transistors on (110) silicon, Packan, P., Cea, S., Deshpande, H., Kuhn, K., et. al. IEDM 2008. IEEE International Electron Devices Meeting, 15-17 December 2008, San Francisco, CA, USA, IEDM 2008. IEEE International Electron Devices Meeting. Technical Digest Pages: 4 pp. Published: 2008
31. 45 nm high-k + metal gate strain-enhanced transistors, Auth, C., Cappellani, A., Chun, J.-S., Kuhn, K. et al, 2008 Symposium on VLSI Technology, 17-20 June 2008, Honolulu, HI, USA, Pages: 128-9 Published: 17 June 2008
30. Dielectric breakdown in a 45 nm high-K/metal gate process technology, Prasad, C., Agostinelli, M., Auth, C., Kuhn, K. et al, 2008 IEEE International Reliability Physics Symposium (IRPS), 27 April-1 May 2008, Phoenix, AZ, USA, Pages: 667-8 Published: 2008
29. BTI reliability of 45 nm high-K + metal-gate process technology, Pae, S., Agostinelli, M., Brazier, M., Kuhn, K, et al. 2008 IEEE International Reliability Physics Symposium (IRPS), 27 April-1 May 2008, Phoenix, AZ, USA, (IRPS) Pages: 352-7 Published: 2008
28. Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4 Published: 2007
27. A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging, Mistry, K., Allen, C., Auth, C., Kuhn, K. et al., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA , IEDM '07 Pages: 247-50 Published: 2007
26. High performance 35nm L/sub GATE/ CMOS transistors featuring NiSi metal gate (FUSI), uniaxial strained silicon channels and 1.2nm gate oxide, Ranade, P.; Ghani, T.; Kuhn, K.; Mistry, K.; Pae, S.; Shifren, L.; Stettler, M.; Tone, K.; Tyagi, S.; Bohr, M.; Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International, 5-7 Dec. 2005 Page(s):4 pp.

25. Noise performance of 90 nm CMOS technology, Becher, D.; Banerjee, G.; Basco, R.; Hung, C.; Kuhn, K.; Wei-Kai Shih, 2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535). Piscataway, NJ, USA: IEEE, 2004. p. 17-20 Vol.1. Conference Paper.
24. A comparison of state-of-the-art NMOS and SiGe HBT devices for analog/mixed-signal/RF circuit applications, Kuhn, K.; Basco, R.; Becher, D.; Hattendorf, M.; Packan, P.; Post, I.; Vandervoorn, P.; Young, I., 2004 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.04CH37526). Gaithersburg, MD, USA: Widerkehr and Associates, 2004. p. 224-5. Conference Paper.
23. A 90 nm communication technology featuring SiGe HBT transistors, RF CMOS, precision R-L-C RF elements and 1 /spl mu/m/sup 2/ 6-T SRAM cell, Kuhn, K.; Agostinelli, M.; Ahmed, S.; Chambers, S.; Cea, S.; Christensen, S.; Fischer, P.; Gong, J.; Kardas, C.; Letson, T.; Henning, L.; Murthy, A.; Muthali, H.; Obradovic, B.; Packan, P.; Pae, S.W.; Post, I.; Putna, S.; Raol, K.; Roskowski, A.; Soman, R, "" Electron Devices Meeting, 2002. IEDM '02. Digest. International , 8-11 Dec. 2002 Page(s): 73 -76
22. A 90 nm Generation BiCMOS Technology for Analog, Mixed-signal, and RF Applications, K. Kuhn, S. Chambers, C. Kardas, T. Letson, A.-Murthy and P. Packan, Intel Process Technology Conference, October, 17, 2002. (Best of session paper award)
21. Scaling challenges for 0.13 mu m generation shallow trench isolation, Kuhn, K.J.; Din-how Mei; Post, I.; Neiryneck, J., 2001 IEEE International Symposium on Semiconductor Manufacturing. ISSM 2001. Conference Proceedings (Cat. No.01CH37203). Piscataway, NJ, USA: IEEE, 2001. p. 187-90 Conference Paper
20. Scaling challenges for 0.13 mu m generation shallow trench isolation, Kuhn, K.J.; Din-how Mei; Post, I.; Neiryneck, J., and Au, W., Intel Process Technology Conference, October, 10, 2000.
19. Electrical critical dimension metrology for 100 nm linewidths and below. Grenville, A.; Coombs, B.; Hutchinson, J.; Kuhn, K. Proceedings of the SPIE - The International Society for Optical Engineering, vol.4000, pt.1-2, 2000. p. 452-9 Conference Paper
18. The performance of a wide band X-ray Bragg polarizer grown by molecular beam epitaxy, Cross, J.O.; Bennett, B.R.; Bell, M.I.; Kuhn, K.J., , AIP Conference Proceedings, no.417, 1997. p. 117
17. Solving the 3 and 4 state laser systems, Dr. Kuhn Kuhn, regular paper, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.
16. An integrated course in laser engineering, K. Kuhn, regular paper #1232, ASEE 1996 annual conference, Washington DC, June 22-26, 1996.

15. Development of a course in Consumer Electronics, K. Kuhn and B. Hannaford, regular paper #3232, ASEE 1996 annual conference, Washington DC, June 22-26, 1996.
14. An Erbium-doped fiber laser, C. Cornish and K. Kuhn, 1995 Progress in Electromagnetics Research Symposium, July 24-28, 1995.
13. Development of a course in Consumer Electronics, K. Kuhn and B. Hannaford, Session 3B, Mechatronics Conference, Stanford, July 15-17, 1994.
12. Integrated optical waveguide modulator using long range surface plasmon resonance, C. Jung, S. Yee and K. Kuhn, OSA Integrated Photonics Research Conference, San Francisco, CA. February 17-19 (1994)
11. Evaluation of an ion-exchanged integrated optic waveguide for solution phase chemical sensing. Kuhn, K.J.; Burgess, L.W. Proceedings of the SPIE - The International Society for Optical Engineering, vol.1796, 1993. p. 332-42 Conference Paper
10. A. Sengers, G. Iyengar, L. Tsang and K. Kuhn, "Optical Properties due to Intersubband Transitions in n-type Quantum Wells Including the Effects of the Exchange Interaction", 1993 March meeting of the American Physical Society, Seattle, WA 22-26 March 1993.
9. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in $\text{Al}_{\text{sub } x}/\text{Ga}_{\text{sub } 1-x}/\text{As}/\text{GaAs}/\text{Al}_{\text{sub } x}/\text{Ga}_{\text{sub } 1-x}/\text{As}$ quantum wells. Iyengar, G.U.; Kuhn, K.J.; Yee, S. In: Gallium Arsenide and Related Compounds 1991. Proceedings of the Eighteenth International Symposium. Bristol, UK: IOP, 1992. p. 431-6 Conference Paper
8. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$ quantum wells, G. Iyengar, K. Kuhn, and S. Yee, Conference Proceedings, 17th International Symposium on GaAs and Related Compounds, September 9-12, 1991; Seattle, WA.
7. Applications of Molecular Beam Epitaxy to Integrable Optical Devices, K.J. Kuhn, Professional program, Northcon/88, October 5, 1988.
6. Laser annealing of AlGaAs, E. Riemer, K. Song, K. Kuhn and T. Stoebe, Atomic and Molecular Processing of Electronics and Ceramic Materials, 23 Conf. on Ceramic Science, UW, August 30 to September 3, 1987.
5. Amplified Spontaneous Emission in Slab Lasers, D.C. Brown, K.J. Kuhn, Kotik K. Lee and R.L. Byer, paper WE-5, Conference on Lasers and Electro-optics (CLEO), Anaheim, CA, June 1984.
4. Progress in high peak and average power lasers for soft X-ray production. Byer, R.L.; Kuhn, K.; Reed, M.; Trail, J. Proceedings of the SPIE - The International Society for Optical Engineering, vol.448, 1984. p. 2-7 Conference Paper

3. Conductive-cooling of Slab Lasers, K.J. Kuhn, T.J. Kane, and R.L. Byer, paper WE-3, 1982 Annual meeting of the Optical Society of America, Tucson, Arizona, October 1982.
2. Progress in slab geometry solid state lasers. Eggleston, J.M.; Kane, T.; Kuhn, K.; Byer, R.L. Proceedings of the SPIE - The International Society for Optical Engineering, vol.335, 1982. p. 104-8 Conference Paper
1. Implementation of distributed microprocessor systems in custom heavy trucks. Kuhn, K.J. In: Wescon/80 Conference Record. El Segundo, CA, USA: Electron. Conventions, 1980. p. SS2-3/1-8 Conference Paper.

PATENTS

	PAT. NO.	Title
1	11,302,777	Integration methods to fabricate internal spacers for nanowire devices
2	11,195,919	Method of fabricating a semiconductor device with strained SiGe fins and a Si cladding layer
3	11,139,400	Non-planar semiconductor device having hybrid geometry-based active region
4	11,024,714	Nanowire transistor fabrication with hardmask layers
5	10,991,799	Silicon and silicon germanium nanowire structures
6	10,825,752	Integrated thermoelectric cooling
7	10,804,357	Integration methods to fabricate internal spacers for nanowire devices
8	10,636,871	Silicon and silicon germanium nanowire structures
9	10,593,804	Non-planar semiconductor device having hybrid geometry-based active region
10	10,586,868	Non-planar semiconductor device having hybrid geometry-based active region
11	10,580,899	Nanowire structures having non-discrete source and drain regions
12	10,580,860	Integration methods to fabricate internal spacers for nanowire devices
13	10,535,770	Scaled TFET transistor formed using nanowire with surface termination
14	10,424,580	Semiconductor devices having modulated nanowire counts
15	10,283,589	Integration methods to fabricate internal spacers for nanowire devices
16	10,121,861	Nanowire transistor fabrication with hardmask layers
17	10,121,856	Integration methods to fabricate internal spacers for nanowire devices
18	10,115,822	Methods of forming low band gap source and drain structures in microelectronic devices
19	10,109,711	CMOS FinFET device having strained SiGe fins and a strained Si cladding layer on the NMOS channel
20	10,074,573	CMOS nanowire structure
21	10,074,357	Integrated acoustic phase array
22	10,026,829	Semiconductor device with isolated body portion
23	9,978,636	Isolated and bulk semiconductor devices formed on a same bulk substrate
24	9,947,805	Nanowire-based mechanical switching device
25	9,935,205	Internal spacers for nanowire transistors and method of fabrication thereof
26	9,935,107	CMOS FinFET device with dual strained cladding layers on relaxed SiGe fins, and method of fabricating the same
27	9,926,193	Magnetic nanomechanical devices for stiction compensation

28	9,911,835	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
29	9,893,167	Integration methods to fabricate internal spacers for nanowire devices
30	9,882,053	Molded dielectric fin-based nanostructure
31	9,859,368	Integration methods to fabricate internal spacers for nanowire devices
32	9,825,130	Leakage reduction structures for nanowire transistors
33	9,812,524	Nanowire transistor devices and forming techniques
34	9,691,843	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
35	9,680,013	Non-planar device having uniaxially strained semiconductor body and method of making same
36	9,673,302	Conversion of strain-inducing buffer to electrical insulator
37	9,614,060	Nanowire transistor with underlayer etch stops
38	9,608,059	Semiconductor device with isolated body portion
39	9,595,581	Silicon and silicon germanium nanowire structures
40	9,583,602	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
41	9,583,491	CMOS nanowire structure
42	9,564,522	Nanowire structures having non-discrete source and drain regions
43	9,559,160	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
44	9,508,796	Internal spacers for nanowire transistors and method of fabrication thereof
45	9,484,447	Integration methods to fabricate internal spacers for nanowire devices
46	9,472,613	Conversion of strain-inducing buffer to electrical insulator
47	9,425,212	Isolated and bulk semiconductor devices formed on a same bulk substrate
48	9,412,872	N-type and P-type tunneling field effect transistors (TFETs)
49	9,385,221	Nanowire transistor with underlayer etch stops
50	9,362,074	Nanowire-based mechanical switching device
51	9,355,242	Method and apparatus for managing and accessing personal data
52	9,343,559	Nanowire transistor devices and forming techniques
53	9,287,576	Self-powered internal medical device
54	9,258,114	Quantum key distribution (QSD) scheme using photonic integrated circuit (PIC)
55	9,224,810	CMOS nanowire structure
56	9,183,829	Integrated acoustic phase array

57	9,129,829	Silicon and silicon germanium nanowire structures
58	9,129,827	Conversion of strain-inducing buffer to electrical insulator
59	9,105,344	Shut-off mechanism in an integrated circuit device
60	9,087,863	Nanowire structures having non-discrete source and drain regions
61	9,064,944	Nanowire transistor with underlayer etch stops
62	9,029,221	Semiconductor devices having three-dimensional bodies with modulated heights
63	9,012,284	Nanowire transistor devices and forming techniques
64	8,890,120	Tunneling field effect transistors (TFETs) for CMOS approaches to fabricating N-type and P-type TFETs
65	8,853,741	Junctionless accumulation-mode devices on decoupled prominent architectures
66	8,766,372	Copper-filled trench contact for transistor performance improvement
67	8,753,942	Silicon and silicon germanium nanowire structures
68	8,558,279	Non-planar device having uniaxially strained semiconductor body and method of making same
69	8,507,948	Junctionless accumulation-mode devices on prominent architectures, and methods of making same
70	8,487,348	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
71	8,269,283	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
72	8,258,057	Copper-filled trench contact for transistor performance improvement
73	7,999,607	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
74	7,888,710	CMOS fabrication process utilizing special transistor orientation
75	7,737,770	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
76	7,312,485	CMOS fabrication process utilizing special transistor orientation
77	6,627,506	Thin tensile layers in shallow trench isolation and method of making same
78	6,368,931	Thin tensile layers in shallow trench isolation and method of making same
79	4,617,669	Method and apparatus for pumping laser slabs
80	4,563,763	Method and apparatus for cooling a slab laser

INVITED TECHNICAL PRESENTATIONS/SEMINARS :

Invited panel, IEDM, Variation and the End of the World, December, 2013.

Keynote, The End of Scaling?, ICTC, December 2013.

Invited seminar, CMOS and Beyond, Portland State University, October, 2013.

Keynote panel, CMOS and Beyond: Future Device Technology, ENF 2013, Ireland, June 2013.

Invited seminar, CMOS and Beyond: Future Device Technology for the Mobile World, IDF, May 2013.

Invited Workshop, The Future is Already Here: Evolving Concepts in Device and Materials Technology, AMAT, March 2013.

Invited paper, "The Ultimate CMOS Device and Beyond," IEDM 2012, San Francisco.

Invited talk, Beyond Simply Small: Progress in Advanced Transistor Architectures, Cornell, November 2012.

Invited seminar, Demystifying Moore's Law How it Really Works!, IDF, Sept. 2012, San Francisco.

Invited talk, The Ultimate CMOS Device and Beyond, Ireland, April 2012.

Keynote: "MOS scaling for the 22nm node and beyond: Device physics and technology," April 24, 2011, Taiwan, VLSI-TSA

Plenary: "Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation," INFOS 2011 (June 22, 2011, France)

Keynote: "Beyond the Planar Transistor: Progress in Next Generation Switches," Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

Invited seminar - "Polishing Moore's Crystal Ball: Advanced Transistor Architectures ...and Beyond," K. Kuhn, March 30th. 2011, MIT, MTL seminar series.

Invited seminar - "Emerging Devices: Moore's Law and Advanced Transistor Architectures," K. Kuhn, Varian Technology Symposium, March 31st. 2011.

Keynote: "Scaling Electronics:Trends and Bottlenecks," K. Kuhn, April 4th. 2011, MIT Microphotonics meeting.

Invited seminar - "Gazing into Moore's Crystal Ball: Transistor Scaling after the 15nm node," K. Kuhn, Feb. 17th, 2010, Berkeley.

IEDM 2010 Short Course chair for 15nm technology, December 2010.

Plenary: Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS 2010, Oct. 10, Las Vegas, CA, USA.

Keynote: Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

Plenary: CMOS transistor scaling past 32nm and implications on variation, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA

Keynote: Technology options for 22nm and beyond, K. Kuhn, 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

Invited seminar: Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, Nikkei Electronics Symposium / June 29th, 2010.

Plenary - CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California

Keynote - Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.

Plenary - Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.

Invited talk - CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

Keynote - Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.

Invited talk - Moore's law past 32 nm: future challenges in device scaling, Kuhn, K.J., 2009 13th International Workshop on Computational Electronics (IWCE 2009), 27-29 May 2009, Beijing, China, (IWCE 2009) Pages: 6 pp. Published: 2009

Invited – International Electron Device meeting – short course.
http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_22nm_Device.pdf

Invited seminar - "45nm High-k + Metal Gate Logic Technology," K. Kuhn, May 2008, MIT, MTL laboratory.

Invited talk - Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4

Invited seminar - "CMOS Transistor Architecture Challenges and Opportunities," K. Kuhn, September 2005, MIT, MTL laboratory.

Keynote - "Nanotechnology Challenges and Opportunities," K. Kuhn, January 2005, MIT, MTL laboratory.

Invited seminar - "Transistor Scaling and its Impact on Analog/RF Device Performance", Dr. Kuhn Kuhn, March 2005, Stanford University, invited seminar.

Invited seminar - "Advanced transistor architecture approaches and their implications for device and circuit performance," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2004.

Invited seminar - "Moore's Law meets Materials Science", Dr. Kuhn Kuhn, September 2004, University of Washington.

Invited seminar - "Centrino, convergence of computing and communications," November 2003, Dr. Kuhn Kuhn, Stanford University, invited seminar.

Invited seminar - "Challenges in the parallel development of the 90nm communications (121x) and microprocessor (1262) process technologies," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2003.

Invited seminar - "RF/analog integration with 90nm digital CMOS", Dr. Kuhn Kuhn, MIT invited seminar, March 2003

Invited seminar - "Femtosecond pulse laser technology", Dr. Kuhn Kuhn, Oregon State University, March 10, 1997.

Invited talk- "Symbolic Solvers and their impact on engineering education", Dr. Kuhn Kuhn, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.

KELIN J. KUHN: LISTING OF CASE WORK

Trial Experience:

ACORN SEMI, LLC, vs. SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR, INC.; AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, Case No. 2:19-CV-00347-JRG EASTERN DISTRICT OF TEXAS, MARSHALL DIVISION. Validity: Enablement only. Settlement with Samsung on enablement before trial. I did not attend trial.

KIPB LLC v. SAMSUNG ELECTRONICS CO., LTD. et al., Case No.: 2:19-cv-0056-JRG-RSP. UNITED STATES DISTRICT COURT, EASTERN DISTRICT OF TEXAS, MARSHALL DIVISION. Opening Report and Rebuttal Report. Settlement with Samsung before trial. Trial cancelled.

KAIST IP US LLC v. SAMSUNG ELECTRONICS CO., LTD. et al., GLOBALFOUNDRIES, INC.; et al., and QUALCOMM INC. Case No.: 2:16-cv-01314-JRG-RSP UNITED STATES DISTRICT COURT, EASTERN DISTRICT OF TEXAS, MARSHALL DIVISION. Opening Report and Rebuttal Report. I presented Opening and Rebuttal at trial. Trial 6-11-18 to 6-15-18.

Deposition testimony:

Case No. AU:22-CV-00852-RP. Katana Silicon Technologies LLC -v- GlobalFoundries, Inc., et al. December 10, 2024. Opening and Validity.

ITC Inv. No. 337-TA-1336. Daedalus Prime LLC v. TSMC. July 18, 2023. Validity.

IPR2021-01321. Arigna Technology Limited v. Volkswagen, Inc. '867 patent. August 5, 2022

IPR2021-01382. Arigna Technology Limited v. Infineon Technologies AG. '867 patent. July 11, 2022.

Case No. 6:20-cv-178-ADA. IP Bridge v. Micron. September 17, 2021. Opening and validity.

IPR2020-01183, 01204, 01205, 01206, 01207, 01279 and 01282. Acorn v. Samsung. July 6-7, 2021

IPR2020-01007. IP Bridge v. Micron. '041 patent. May 18, 2021.

IPR2020-01008. IP Bridge v. Micron. '047 patent. May 3, 2021.

Case No. 2:19-CV-00347-JRG. Acorn v. Samsung IPRs. April 6-7, 2021. IPR

Case No. 2:19-CV-00347-JRG. Acorn v. Samsung. December, 26, 2020. Enablement.

Case No.: 2:19-cv-0056-JRG-RSP. KIPB LLC v. Samsung. August 3, 2020. Opening and validity.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. March 16, 2018. Opening and validity.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. November 2, 2017. Claim construction.

Reports/Declarations:

Case No. 01-21-0002-5445. TSMC v. SST. August 21, 2024. Trade secret Use.

IPR2024-00789. Yangtze v. Micro, U.S. Patent 10,861,872. July 29, 2024. POPR

Reexam No. 90/015,321. U.S. Patent No. 6,291,861. June 20th, 2024. Declaration/EPR.

Case No. 1:22-CV-852-RP. Katana v. GlobalFoundries. February 23rd, 2024. Validity

Case No. 1:22-CV-852-RP. Katana v. GlobalFoundries. December 20th, 2023. Infringement

Case No. 01-21-0002-5445. TSMC v. SST. July 21, 2023. Opposition to Motion to Compel.

ITC Inv. No. 337-TA-1336. Daedalus Prime LLC v. TSMC. July 18, 2023. Validity.

IPR2021-01321. Arigna Technology Limited v. Volkswagen, Inc. '867 patent. August 5, 2022

IPR2021-01382. Arigna Technology Limited v. Infineon Technologies AG. '867 patent. July 11, 2022.

Case No. 6:20-cv-178-ADA. IP Bridge v. Micron. September 10, 2021. Validity.

Case No. 6:20-cv-178-ADA. IP Bridge v. Micron. August 13, 2021. Opening.

IPR2020-01183, 01204, 01205, 01206, 01207, 01279 and 01282. Acorn v. Samsung. July 6-7, 2021

IPR2020-01007. IP Bridge v. Micron. '041 patent. February 28, 2021.

IPR2020-01008. IP Bridge v. Micron. '047 patent. February 28, 2021.

Case No. 2:19-CV-00347-JRG. Acorn v. Samsung IPRs. April, 21, 2020. IPR

Case No. 2:19-CV-00347-JRG. Acorn v. Samsung. December, 12, 2020. Enablement.

Case No.: 2:19-cv-0056-JRG-RSP. KIPB LLC v. Samsung. July 23, 2020. Opening and validity.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. 2018. Opening and validity.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. 2018. IPR.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. 2017. Claim construction