UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No. IPR2024-00794
U.S. Patent No. 10,950,623

PETITIONER'S REPLY

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,950,623 B2 to Song et al.
1002	File History of U.S. Patent No. 10,950,623 to Song et al.
1003	Declaration of Dr. Jack C. Lee ("Lee")
1004	U.S. Patent No. 10,559,583 B2 to Park et al. ("Park")
1005	U.S. Patent Publ. No. 2019/0122734 A1 to Shibata et al. ("Shibata")
1006	Aritome, "NAND Flash Memory Technologies" (2016)
1007	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1008	U.S. Patent Publ. No. 2015/0162084 A1 to Morooka et al.
1009	U.S. Patent Publ. No. 2015/0255478 A1 to Tanzawa
1010	U.S. Patent No. 9,589,978 to Yip
1011	U.S. Patent Publ. No. 2017/0062337 A1 to Park et al.
1012	Micheloni et al., "Inside Solid State Drives (SSDs)" (2nd Ed. 2018)
1013	Docket from Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 3:23-cv-05792-RFL
1014	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1015	File History of U.S. Patent No. 11,430,811 (Appl. No. 17/154,054) to Song et al.

1016	U.S. Patent No. 10,355,010 B2 to You et al.
1017	U.S. Patent No. 9,299,718 B2 to Park et al.
1018	U.S. Patent Publ. No. 2019/0035798 A1 to Hwang et al.
1019	U.S. Patent Publ. No. 2015/0137216 A1 to Lee et al.
1020	*Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc*. and Micron Consumer Products Group, LLC, Case No. 3:23-cv-05792-RFL, Zoom Civil Minute Order, dated February 22, 2024 (Dkt. No. 42)
1021	U.S. Patent Pub. 2019/0214404 A1 to Ahn et al.
1022	*Curriculum Vitae* of Dr. Jack C. Lee
1023	U.S. Patent No. 8,945,996 to Tang et al.
1024	Declaration of Jared Bobrow in Support of Petitioner's Motion for Admission *Pro Hac Vice*
1025	Reply Declaration of Dr. Jack C. Lee ("Lee Reply")
1026	Transcript of the April 2, 2025 Deposition of Kelin Kuhn, Ph.D.

I. INTRODUCTION

Patent Owner's response proposes erroneous claim constructions, fails to account for the totality of the prior art's disclosures, and is replete with irrelevant, unsupported assertions. When the claims are properly construed—and the totality of the prior art's teachings is considered—the '623 patent's claims are plainly all obvious.

Patent Owner spends the bulk of its response responding to Ground 1 (obviousness over Park). But here Patent Owner does nothing more than try to graft a variety of additional limitations from the specification onto the claims. The Board already addressed—and rejected—most of these claim construction arguments when instituting. It should do so again here. As the Board properly found, the claims do not require trenches that span the entire length of the memory. Nor do the claims exclude devices in which the trenches cooperate with other structure to separate a memory's BSG into sub-BSG. And the claims are not product-by-process claims. There is nothing in the claims—or the specification—that requires that the claimed "dielectric trench" be manufactured in a conductive layer (a "gate first" method) as opposed to a sacrificial layer (a "gate last" method). Instead, the specification says the opposite: either manufacturing method can be used. And both methods result in the exact same memory device.

Patent Owner's other arguments about Park are no better. For instance, it argues that Park does not render claims 2 and 3 obvious. Although it concedes that certain of Park's figures depict an undivided TSG over the portion of the memory where isolation insulating layer 111 is located (thus necessitating a matching layer 111 in the TSG), it argues that this is an "error." It is not. Park repeatedly explains that its memory can have different dimensions and layouts. It is Patent Owner's narrow reading of Park—which effectively negates swaths of the reference—that is in "error" here.

Nor has Patent Owner offered any meaningful rebuttal to the Petition's other grounds. In response to Ground 2, Patent Owner argues that Park "actively discourages" use of longer dielectric trenches like those taught by Shibata. It does not. Instead, Park presents a variety of design alternatives that ***facilitate*** the use of larger trenches. And when addressing Ground 3, Patent Owner does not even discuss (let alone dispute) the primary motivation for applying Park's lower trenches to Shibata: doing so would increase the number of layers available for word lines, thereby improving memory density. Instead, it spends its time improperly assessing the references in isolation and quibbling over the total number of manufacturing steps the combination of Shibata and Park would employ. This—like all of Patent Owner's arguments—does not rebut the Petition's strong showing of obviousness.

II. ARGUMENT

A. Ground 1: Obviousness Over Park

Ground 1 explained why Park renders many of the '623 patent's claims obvious. *See* Petition (Paper 1), 25-57.

1. *Claim 1*

Claim 1 is the patent's sole independent claim. The only thing Patent Owner identifies as missing from Park is the claimed ***"dielectric trenches."*** Although Park includes trenches—its isolation insulation layers 111—that are indisputably located in and divide Park's bottom select gate layer, Patent Owner argues that this is not what claim 1 requires. But Patent Owner's argument is premised entirely on erroneous claim constructions. The Board already addressed—and rejected—many of these proposed constructions. *See* Institution Decision (Paper 9), 15-17. The rest of Patent Owner's assertions are either legally erroneous or ignore the '623 patent's disclosure. There is simply no basis in the record for limiting the claims in the way Patent Owner proposes.

Patent Owner first argues that Park lacks ***"dielectric trenches formed in the BSG"*** in claim 1. Response, 32. Although claim 1 is an apparatus claim, Patent Owner asserts that it somehow requires the "dielectric trench" to be ***manufactured*** in a particular way: the trench must be made in conductive "BSG" layer itself as opposed to "some other type of structure, such as a sacrificial layer." *Id.* Patent Owner then argues that this distinguishes Park because Park's layers 111 are

manufactured in sacrificial layers that are replaced with conductive material later (*i.e.*, Park employs a "gate last" instead of a "gate first" process). *Id.*, 32-33. In other words, Patent Owner construes "dielectric trenches formed in the BSG" as a product-by-process limitation.

This argument fails, of course, because the claim phrase is not a product-by-process limitation. Claim 1 is an apparatus claim that requires a "memory device." It is not a method claim. Moreover, while the '623 patent's specification does mention different methods of manufacturing the claimed device—including a "gate first manufacturing flow" and "gate last manufacturing flow" (Ex. 1001, 20:28-31)—Patent Owner mentioned neither in the claims. If Patent Owner intended to limit the claims to only one of these methods, it would have said so using the specification language. It did not. Rather than requiring any particular manufacturing method, the claim term "formed in" simply specifies where the "dielectric trenches" are ***located***: within the "BSG" layer. The word "formed" is used this way repeatedly in the '623 patent. For instance, the patent explains that Figure 1A—which depicts a fully manufactured device—shows "two first trenches 26 and 28" that "are ***formed in*** the one or more BSGs…." Ex. 1001, 7:17-20 (emphasis added). This is referring to where the trenches are in the device, not their method of manufacture. Likewise, the patent explains that its trenches are "***formed along*** the X-direction." *See id.*, 13:1-3; 17:67-18:2 (emphasis added). Again, this

is a reference to the trenches' orientation within the device. Nor does anything else about the claims (or the specification) operate to impose a manufacturing process requirement. Patent Owner argues that because the trench must "separate the BSG into a plurality of sub-BSGs," this somehow requires a specific method of manufacturing. *See* Response, 10. But this is simply referring to what the trench does: its presence separates the BSG into a plurality of sub-BSGs.

Next, even if claim 1 did for some reason require use of a particular process (it does not), this is irrelevant to patentability. "In determining validity of a product-by-process claim, the focus is on the ***product and not the process of making it***." *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1369 (Fed. Cir. 2009) (emphasis added). This is because an "old product is not patentable even if it is made by a new process." *Id.* at 1370. Thus, in almost all cases, process limitations do not serve to limit apparatus claims. *See id.* The only time such a limitation matters is "if the process by which a product is made imparts structural and functional differences." *KAMSTRUP A/S v. Axioma Metering UAB*, 43 F.4th 1374, 1381 (Fed. Cir. 2022). Here, the final memory device will be the same regardless of the process used. The '623 patent itself concedes this. The patent details use of both a "gate first manufacturing flow" (where the trenches are formed directly in conductive layers) and a "gate last manufacturing flow" (where the trenches are formed in temporary sacrificial layers that are later replaced with conductive material). Ex.

1001, 20:28-21:9. Regardless of which process is employed, the exact same "memory device 100" of "FIG. 1A" results. *Id.*; *see also* Ex. 1026, 16:13-17:22, 24:5-25:22 (Patent Owner's expert confirming that the same device is produced by both specification methods).

If this were not enough, Patent Owner's narrowing construction improperly seeks to read an embodiment out of the scope of the claims. Again, the specification makes clear that the claimed "dielectric trenches" can be manufactured via either a "gate first" or "gate last" process. *Id.*, 20:28-21:9; 7:1-11 (similarly noting that "BSG 62p" can be "formed firstly using sacrificial layers" in "some embodiments). Patent Owner argues that the claims require a "gate first" process, which reads out the specification's "gate last" process. Absent a clear specification disclaimer or requirement in the language of the claim, "claim terms" are not to be "interpret[ed] … in a way that excludes embodiments disclosed in in the specification." *Oatley Co. v. IPS Corp.*, 514 F.3d 1271, 1276-77 (Fed. Cir. 2008); *see also Google LLC v. EcoFactor, Inc.*, 92 F.4th 1049, 1058 (Fed. Cir. 2024). Here, there is no specification disclaimer. Both "gate first" and "gate last" processes are identified as acceptable.

Patent Owner next argues that Park lacks ***"one or more first dielectric trenches"*** that ***"extend[] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs."*** Response, 34. Like its product-by-process argument, this is also contrary to the law and the '623 patent: Patent Owner improperly seeks

to graft structure features from the embodiments in the specification onto the claims. Indeed, the Board has already expressly addressed—and rejected—the very same claim construction argument. Institution Decision, 15 ("structures such as the common source regions may assist in defining the boundaries of the BSG and sub-BSGs"), 16 ("we do not understand claim 1 to require the trench to extent the entire length of the memory device").

Patent Owner begins by arguing that the claims somehow impose length and location requirements on the "dielectric trenches." According to Patent Owner, it is the "length of the dielectric trenches" that must operate to "separate the BSG." *Id.*, 14. In other words, the trenches apparently must extend the ***whole length*** of the BSG. Patent Owner also appears to argue that claim somehow requires the trenches to be in "array" portion of memory and not somewhere else (like the memory's staircase region). *Id.*, 36. Using this narrow interpretation, Patent Owner faults Park because its isolation insulating layers 111 are only "short cuts in the common source line and do not even extend into the active region" of the memory. *Id.*

None of this is required. Claim 1 of the '623 patent requires only that the "dielectric trenches" be "formed in the BSG" and "extend" in the length direction of the "substrate." There is no requirement that that trenches have any particular length, let alone that they extend the entire length of the BSG. There is also no requirement that the trenches be in the array portion of the memory as opposed to elsewhere.

Indeed, the '623 patent's example trenches extend into the memory's staircase region. *E.g.*, Ex. 1001, Fig. 1B. There is, of course, an example in the '623 patent's specification of a memory with a trench spanning the entire BSG. But "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004). There is nothing of the sort here. Instead, the '623 patent repeatedly explains that it is ***not*** to be limited to its examples. *E.g.*, Ex. 1001, 5:13-16 ("[s]pecific examples" in specification are "merely examples and are not intended to be limiting."); 23:36-46 ("other … structures" besides those specifically depicted can be used).

Next, the claims also do not say that the trenches must separate the BSG entirely on their own. All that is required is that the trenches "separate the BSG into a plurality of sub-BSGs." This is what the '623 patent means when it explains that "[w]ithout the introduction of the first/second trenches, the memory device 100 … has a shared BSG…." Ex. 1001, 9:46-59; 12:7-9. It is the presence of the trenches that causes the BSG to be separated. This can of course occur either with or without the help of other structure, so long as the trench plays a role in the separation. Indeed, the '623 patent itself does not separate its BSG using ***only*** dielectric trenches. While

a side of each sub-BSG is bounded by a trench in the patent's examples, the other side is bounded by common source region. Without this common source, the sub-BSG would join with and be electrically connected to an adjacent sub-BSG. An example of this is shown in Figure 1B below:

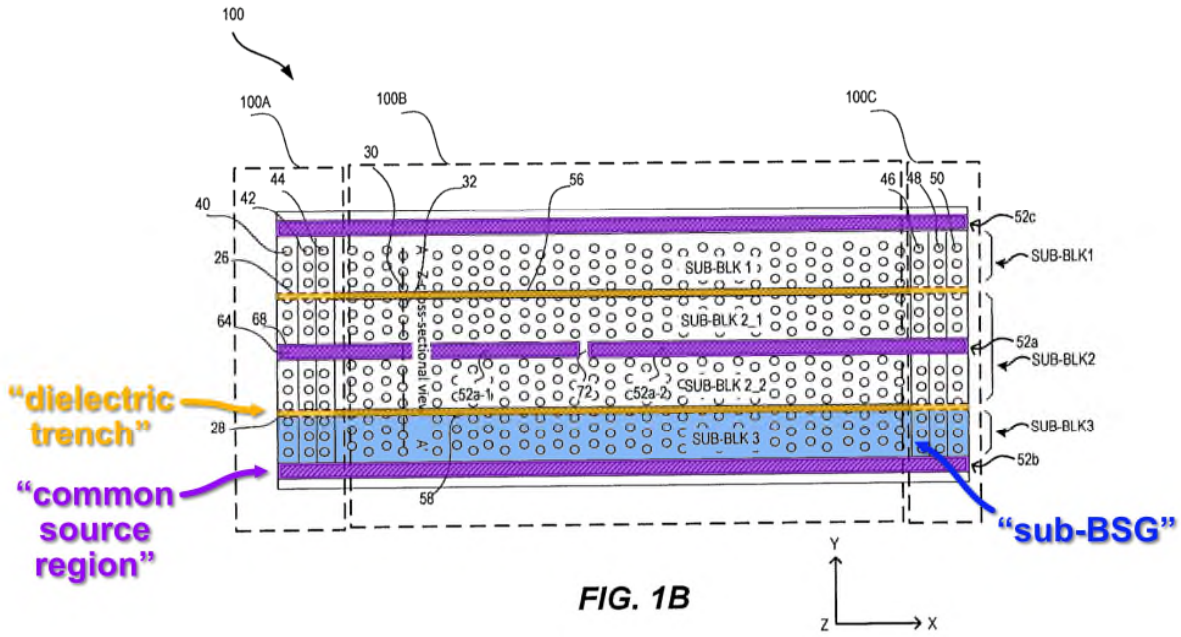


FIG. 1B

Id., Fig. 1B (annotated).

Patent Owner argues that this is not an example of the use of both a trench and a common source to separate a BSG because, in its view, "BSG is not present on the other side of the common source regions 52b and 52c." Response, 18. This is wrong. Device 100 in Figure 1B may be "one of the memory cell blocks" of a larger memory device. Ex. 1001, 9:8-10. Because device 100 is just one of many blocks, there will be further blocks of memory above and below what is shown in the figure. And in such circumstances, "[t]he common source regions 52b and 52c accordingly isolate

… memory cell block 100 … from adjacent memory cell blocks…." Ex. 1001, 9:10-13; *see also* Ex. 1026, 34:4-15, 41:23-42:16 (Patent Owner's expert recognizing that common source lines perform isolation function). Patent Owner's interpretation of claim 1—which requires that the trenches alone separate BSG into sub-BSG—would read this embodiment out of claims. Such a construction "is rarely, if ever, correct." *SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1378-79 (Fed. Cir. 2013).

Nor are Park's layers 111 "very similar" to the '623 patent's "H-cuts." Response, 22. The H-cuts are filled with conductive material to ***join*** adjacent gate layers. Ex. 1001, 9:36-46; *see also* Ex. 1026, 30:5-18. Park's layers 111 electrically ***separate*** its BSG. Park, 6:8-12.

In sum, Patent Owner has pointed to nothing in the claims or specification that even remotely supports its limiting claim constructions. Instead, it repeatedly ignores the law and the '623 patent's own teachings.

2. *Claims 2 and 3*

Dependent claims 2 and 3 require a second set of "dielectric trenches" in a memory's "top select gate (TSG)" layer. Ex. 1001, Claims 2-3. The Petition explained that in Park, both the bottom and top select gate layers are meant to be divided into the same, separately controllable sub-units. Petition, 40-41. In some of Park's embodiments, the top select gate layer has a reduced physical extent such that the required division of this layer is accomplished by Park's common source lines.

Id. But Park ***also*** teaches—or at the very least obviously directs a POSITA towards—a memory where the TSG layer is located over the portion of the BSG layer that is divided by isolation insulation layers 111. *Id.*, 41-42. In such a device, both layers would obviously have been separated with analogous isolation insulation layers 111. *Id.*, 43.

Patent Owner does not challenge that it would have been obvious to employ isolation insulation layers 111 in Park's TSG layer if this layer is co-extensive with (and located over the divided portion of) Park's BSG layer. Instead, Patent Owner argues only that in Park, there is purportedly no need to use layers 111 because "the TSG ends before it reaches that location." Response, 40. While Patent Owner concedes that many of Park's figures do in fact show the TSG over the portion of the BSG that is divided by layers 111, this is purportedly an "error" that "mistakenly shows all of the layers present in the device." *Id.*, 43.

This is not a case where there is some sort of "obvious error of a typographical or similar nature" in Park "that would be apparent to one of ordinary skill in the art." *LG Electronics, Inc. v. ImmerVision, Inc.*, 39 F.4th 1364, 1372 (Fed. Cir. 2022). Instead, Park not only unambiguously depicts un-divided conductive layers GL14 and GL15 directly over isolation layers 311 in Figure 36, but it explains multiple times in its specification that these layers are meant to be the device's top "string

select line[s]." *E.g.*, Park, 16:26-30; 16:20-37. Park does the same in Figure 29. *Id.*, Fig. 29.

Patent Owner would have the Board read all this out of Park. Its only justification for doing so is that Park includes other, different figures that are drawn in a way more to Patent Owner's liking. For instance, Figure 27 depicts a device in which the top two conductive layers (Park's TSG) are not present over the depicted isolation layer 311. *Id.*, Fig. 27. But the primary purpose of Figure 27 is not to provide some sort of definitive view that dictates the exact size and shape of Park's conductive layers across all its embodiments. Instead, the figure is primarily meant to depict an "interlayer insulating layer 370" that conformally covers all of Park's "pad regions PAD" along with a series of "channel structures CH and a plurality of dummy channel structures DCH…." *Id.*, 13:35-44.

Moreover, Park repeatedly expresses that its figures are only "***examples***" of its "inventive concept." *Id.*, 2:43-47, 18:4-9 (emphasis added). Likewise, Park explains that while its device's "connecting electrodes" can be "disposed in different positions in the first direction" in "each gate electrode layer" as shown in some of its example figures, lower layers can alternatively be "disposed below" upper layers. *Id.*, 8:59-9:2; *see also* 12:13-21 (referencing examples in which "connecting electrodes" are "formed at the same positions in the … X-axis direction…"). Park also explains that its isolation insulation regions are not required to have a fixed

location in all embodiments and may instead "be formed in different positions in … [the] X-axis direction." *Id.*, 12:65-13:3. Thus, Park is plainly open to and renders obvious electrode layers with different sizes and physical extents. It is also open to and discloses trenches present at different device locations. Given this, a POSITA would not consider Figure 36 to include an "error." Instead, it is simply representative of the breadth of Park's disclosure. Ex. 1025, ¶¶ 8-22. In any event, even if there were an "error" in Park (there is not), it is just as likely that it is Figure 27—and not all of Figures 21, 29, 31, 34, and 36—that wrongly depicts the TSG's physical extent.

Next, sizing Park's TSG such that it is located over the portion of the BSG including the trenches—as Park shows in multiple of its figures—also does not "contradict[]" Park's teachings as Patent Owner argues. Response, 43. Again, nothing in Park requires its trenches to be in any particular location vis-à-vis its upper select gate. *E.g.*, *id.*, 12:65-13:3. Instead, the trenches can have various locations in the "X-axis direction" in Park's figures, including a location that positions them underneath the uppermost gate electrode layer. *Id.* Nothing about this would contradict Park's teachings. Connection with Park's pads would still be effectuated in the same way discussed elsewhere in Park. Ex. 1025, ¶¶ 23-24.

Patent Owner concludes its discussion of these claims by re-making the same claim construction arguments it made in connection with claim 1. Response, 47-49. These lack merit for same reasons discussed above. *See supra* Section II.A.1.

3. *Claims 10 and 11*

Claims 10 and 11 require that the claimed "memory device" include "dummy BSGs" and "dummy TSGs" that are also "separated by … dielectric trenches." Ex. 1001, Claims 10, 11. As explained in the Petition, Park includes dummy lines between its select gate layers and word lines. Petition, 54-55. The Petition also explained why it would have been obvious for Park's isolation insulating layers 111 to separate not only the select gates, but also these dummy lines. *Id.*

According to Patent Owner, the Petition was purportedly insufficient because it simply noted that Park's dummies "could" be separated by dielectric trench. Response, 49. This is not what the Petition argued. Instead, the Petition both (1) pointed to examples in prior art where multiple layers in a memory (as opposed to just a single layer) are in fact divided by dielectric trenches, and (2) provided technical explanation of why dummies would be divided in this fashion in Park. Petition, 55-56. In particular, Dr. Lee explained that doing so would obviously improve the memory's electrical performance. Ex. 1003, ¶ 281. Dummy cells connected to the dummy lines in a memory serve various important purposes, including suppressing leakage current and avoiding data disturb. *Id.* And as

explained by Dr. Lee, separating the dummies on the same sub-block basis as the select gates—using the same dielectric trenches—would help the dummies perform these functions by making the "loading effects" across the memory "more symmetrical." *Id.* In other words, both the select transistors and dummy transistors would be subjected to the same load on their gate (rather than different loads) because the associated gate electrodes would be similarly divided. *Id.;* Ex. 1025, ¶¶ 26-29. This symmetrical loading is what would improve memory performance. *Id.* In response, Patent Owner offers nothing beyond bald denial. Rather than explaining why the Petition and Dr. Lee are wrong, Patent Owner and its expert simply purport not to understand Dr. Lee. *E.g.*, Ex. 2010, ¶ 114. This type of conclusory non-argument does nothing to rebut the Petition's showing. *E.g., Coalition for Affordable Drugs VII LLC v. Pozen Inc.*, Case IPR2015-01680, Paper 18 at 15 (Feb. 11, 2016) ("[c]onclusory assertions … are not persuasive"). Moreover, despite purportedly not "understanding" Dr. Lee's opinions, Patent Owner did not even ask Dr. Lee any questions about these opinions at his deposition. Indeed, Patent Owner did not even file the transcript of Dr. Lee's deposition with its response (effectively conceding that it did not—despite trying—identify any issues with anything Dr. Lee has said).

Patent Owner also wrongly argues that "Petitioner … fails to explain how a POSITA would have achieved this modification of Park's device." Response, 51. According to Patent Owner, "[f]orming deeper isolation regions would have required

etching through multiple layers." *Id.* While this is of course true, numerous prior art references teach this very thing. *E.g.*, Shibata, Fig. 3 (element 60 separates multiple layers); Ex. 1018, [0058] (multiple layers separated by trench 50). Patent Owner also argues that Park cannot employ a trench spanning multiple layers because it purportedly uses only "selective" etching that removes only single layers at a time. Response, 52. There is no such limitation in Park. Park does reference removal of both "sacrificial" and "insulating" layers at the same time. Park, 13:18-25. This is all that is required to form the trenches of claims 10 and 11. Ex. 1025, ¶¶ 30-31; Ex. 1026, 9:23-10:21 (both selective and timed etches known). Once again, Patent Owner points to distinctions that have no basis in the prior art. Finally, Patent Owner wrongly notes that forming a trench through dummy layers risks "etch[ing] the word line below it." Response, 53. The presence of ***multiple*** dummy layers—some of which serve as a "buffer"—avoids this very thing. Ex. 1003, ¶¶ 285, 289-291.

B. Ground 2: Obviousness Over Park and Shibata

Ground 2 in the Petition demonstrated why the claims are obvious over the combination of Park and Shibata. Petition, 57-63. Following Shibata's teachings, a POSITA would have considered it obvious to reduce the number of common source regions in Park and make Park's isolation insulation layers 111 longer. *Id.*

Patent Owner begins its discussion of this ground by repeating its erroneous claim construction arguments. Response, 55-57. These fail for the same reasons explained above. *See supra* Section II.A.1.

Patent Owner then argues that the combination of Park and Shibata would still not teach what the claims require because Shibata's trenches "traverse only the uppermost drain-side select gate layers." Response, 57. The Petition did not argue that Park and Shibata would be bodily grafted together, using Park's lower trenches and Shibata's upper trenches in the exact same physical form they are depicted in Park and Shibata's figures. Instead, it argued that a POSITA would have followed Shibata's teachings—including its teaching that a memory can employ longer trenches—for purposes of ***modifying*** Park. Patent Owner's bodily incorporation arguments are non-responsive and irrelevant. *Allied Erecting v. Genesis Attachments*, 825 F.3d 1373, 1381 (Fed. Cir. 2016) ("The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference[.]")

Patent Owner next argues that a POSITA would not have applied Shibata to Park because Park purportedly "actively discourages" the combination. Response, 60. It does nothing of the sort. Park does reference a "problem" that may be encountered when "etching" "sacrificial layers." Park, 15:35-63. But this problem only arises when using an "etching solution" like "phosphoric acid" to remove

"sacrificial layers." *Id.* And according to Park, use of this particular method is only meant to be "an example." *Id.*, 15:35-42. A POSITA would have readily understood that other, known etching methods could also be used to remove Park's sacrificial layers. This could include, for instance, dry plasma etching. Ex. 1025, ¶¶ 32-37. Unlike wet etching using a "solution" like that in Park's example, dry etching allows for more consistent performance in confined structures. *Id.*; *see also* Ex. 1026, 10:22-11:17 (both wet and dry etches "foundational for many years" when '623 patent filed).

Next, Park itself already presents a variety of ways to minimize any etching problem that may be encountered when using wet etching. A POSITA would have understood that this would have readily allowed Park to accommodate larger (and more) isolation insulation layers 111, just as Shibata teaches. For example, "second dummy channel structures DCH2" may be formed near layers 111 to "shorten inflow passages of phosphoric acid and conductive material therethrough in a process of forming gate electrodes." Park, 11:52-55; *see also* Fig. 14. This, according to Park, completely avoids any "degradation of the characteristics of the memory device" that results from incomplete etching. *Id.*, 11:55-59. Alternatively, "open regions corresponding to … vertical insulating layers 209" or "209A" (teal below) can "shorten the inflow passages of the phosphoric acid and the conductive material"

providing full access to the sacrificial layers. *Id.*, 12:10-52; *see also* Figs. 16-17. This allows for formation of longer trenches that are not staggered from each other:

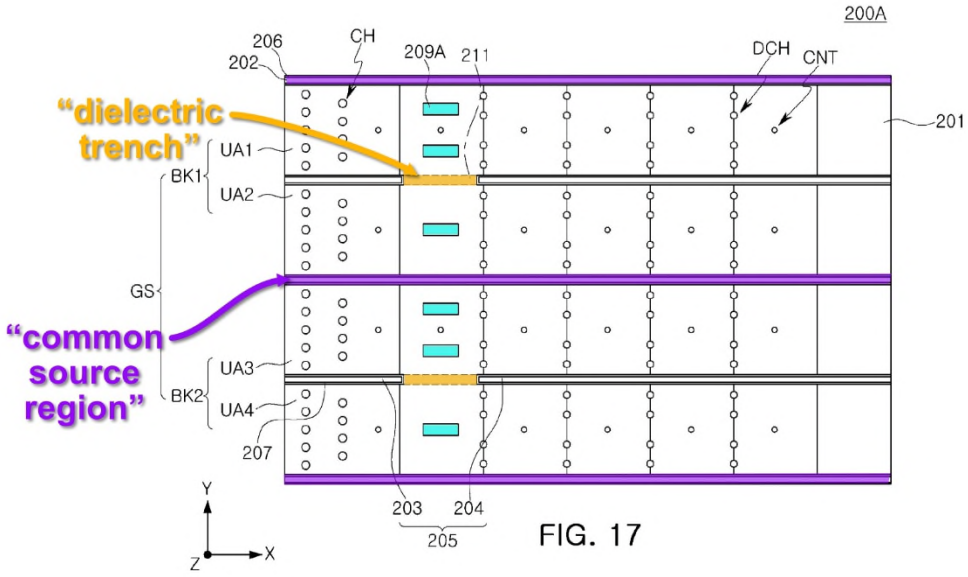


FIG. 17

Id., Fig. 17 (annotated). Thus, far from "discourag[ing]" a POSITA, Park presents various design alternatives that ***allow*** for modifications of the size, shape, and location of its trenches. Ex. 1025, ¶¶ 38-43.

Next, Patent Owner is also wrong when it argues that "Shibata provides no solution to Park's concern." Response, 64. Shibata discusses—and provides a solution to—the very issue identified by Park. According to Shibata, the location of its dielectric filled "separation portion[s] 62a" may impact the replacement of sacrificial layers with conductive "select gate[s,]" resulting in narrower gates with increased "resistance" (which may "delay" "access time"). Shibata, ¶ [0325]. If this occurs, the gate "drive circuits" can be adjusted to ensure proper operation. *Id.*, ¶¶ [00446]-[0450]. This in turn allows for long separation portions 62a that span the

entirety of the memory and directly face each other without ***any*** intervening common source regions. *E.g., id.*, Figs 46, 47A. This is exactly how the Petition proposed modifying Park. *See* Petition, 60 (showing Park with trenches indistinguishable from those in Shibata). If Shibata accommodates this type of trench—and there is no dispute here that it can—then there is no reason Park cannot as well.

Patent Owner relatedly argues that a POSITA would not consider employing Shibata's tailored drivers with Park's bottom select gate because it is a "fixed solution" that is supposedly "not practical for addressing unpredictable variations in word line quality." Response, 65. But Shibata states that its drivers are usable for this very purpose. *See* Shibata, [0324]-[0325], [0446]-[0449]. Patent Owner and its expert are once again seeking to change the prior art to their own liking. These types of statements—which are directly contrary to the record (and cite nothing to support this contradiction)—are entitled to no weight. *Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1378 (Fed. Cir. 2017) (arguments "plainly inconsistent with the record" cannot show non-obviousness).

Next, Patent Owner is wrong when it argues that there would be "no flow path" allowing for the removal of sacrificial layers across wide swaths of Park's device. Response, 65. Here, Patent Owner completely ignores that etchant will still flow into Park's device via all of Park's remaining common source lines (including both those shown in dark purple and those in light purple below):

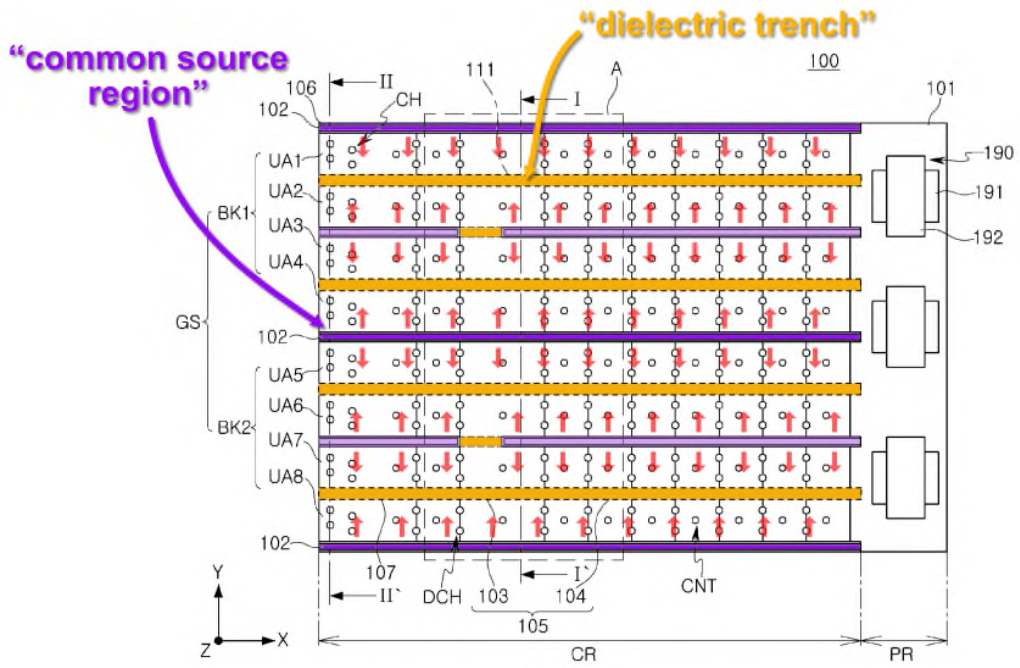


FIG. 3

Ex. 1025, ¶¶ 44-46; Ex. 1026, 45:1-11. As shown, almost all of the device is subjected to significant etchant flow. *Id.* And a POSITA would have recognized that any problem areas could be readily addressed by (1) employing any of the methods Park teaches (such as the use of dummy channels to supplement flow) or (2) using Shibata's tailored drivers. *Id.*, ¶ 47.

Finally, Patent Owner's argument that a POSITA would not replace Park's common source lines with trenches because doing so would purportedly have "adverse effects on the memory device" is at odds with the record. ***None*** of the references Patent Owner cites teaches that there is some sort of minimum quantum of common source lines that must be present in a memory for proper operation. Indeed, the references say virtually nothing about 3D NAND or its operation. *See*

generally Response, 67; *see also* Ex. 1025, ¶¶ 48-53; Ex. 1026, 46:2-56:18 (confirming that papers do not discuss common source line design). Moreover, any current density issues are readily addressable simply by employing a lower resistance conductor or making remaining common source lines slightly wider. Ex. 1025, ¶ 54. Nor would removing common source lines be contrary to "the problem that Park intends to avoid." Response, 68. Park itself includes examples employing fewer common source lines. *Compare* Park, Figs. 3 (9 lines), 16-17 (5 lines); Ex. 1026, 63:12-25. It also says that its device should be designed in a way that "***increas[es]*** the capacity of a memory device and the degree of integration thereof." Park, 17:1-5 (emphasis added). This is what application of Shibata does: by eliminating common source lines, more memory cells can be included, thereby increasing the capacity of the memory without increasing its physical size.

C. Ground 3: Obviousness Over Shibata and Park

Ground 3 demonstrated why Shibata—when modified following Park's teachings—renders the challenged claims obvious. Petition, 63-94. Shibata already employs dielectric trenches to separate its TSG into separately controllable sub-TSGs. As explained in the Petition, following Park's teachings, a POSITA would have considered it obvious to also include a separate set of trenches that similarly separate Shibata's BSG. Petition, 71-78.

Patent Owner does not contest that the combination of Shibata and Park discloses—at least separately—everything that the claims require. Instead, it only challenges the motivation to combine. But in doing so, Patent Owner does little more than use boilerplate language, calling the Petition's detailed explanation "flawed," "conclusory," and based on supposedly "impermissible hindsight." Response, 72. The opposite is true. The Petition explained in detail why it would have been obvious to apply Park to Shibata. It is Patent Owner's analysis that is flawed and unsupported.

To begin, Patent Owner spends the bulk of this portion of its response addressing Shibata and Park ***separately***. For instance, Patent Owner notes that Park employs only "short structures in the staircase region" to separate its select gate layers. Response, 73-74. This ignores, however, that Shibata's separation portions 62a span the entirety of its memory. *E.g.*, Shibata, Fig. 47A. Likewise, Patent Owner argues that in Shibata, separation portions 62a are only located in the "uppermost layer." Response, 71. Park, however, teaches the use of dielectric trenches to separate a memory's bottom select gate layer. *E.g.*, Park, Fig. 11. Other references do the same. *E.g.*, Ex. 1019, [0158], Fig. 22 (employing "separation layer pattern 109" to divide a lower select gate). These types of arguments—which fail to account for the collective teachings of the art—are irrelevant. *Allied Erecting*, 825 F.3d at 1381.

Next, Patent Owner failed to even address—let alone dispute—the primary motivation for applying Park's teachings to Shibata. As explained, applying Park would have allowed "the number of word lines" in Shibata to be "increased without impacting the overall height of Shibata's stack." Petition, 76-77. This in turn would have beneficially increased the size of Shibata's memory. *Id.* Because the art was constantly seeking to increase memory size and density, this would have served as a strong motivation to replace Shibata's multiple lower select gates with a single, separated select gate. *Id.* Patent Owner fails to dispute this.

Although Patent Owner does argue that "[n]either Petitioner nor its expert explain how Park achieves a reduction in manufacturing steps" (Response, 72-73), this is only a secondary benefit. Again, the primary benefit—which Patent Owner failed to dispute—is increased memory size. Moreover, Patent Owner itself showed why use of Park simplifies manufacturing. Shibata's example memory employs three lower select gates (SGS0A, SGS1A, SGSB). *E.g.*, Shibata, Fig. 16. Each of these includes an associated layer of insulation. *Id.* This example structure will thus require the use of six deposition steps during manufacture (one for each select gate and insulating layer). Replacing Shibata's three select gate layers with a single, separated layer following Park's teachings will require two deposition steps (one for the select gate and another for the associated layer of insulation). Ex. 1025, ¶¶ 55-63. Additionally, as Patent Owner itself notes, employing Park require only two

additional steps: "form[ing] a mask" and then "form[ing] slits by etching." Ex. 2010, ¶ 160; Ex. 1025, ¶¶ 55-63. So, application of Park ***would*** reduce manufacturing steps: Shibata's six step process would be reduced to four. *Id.*, ¶ 62. But again, whether manufacturing is simplified is of no moment. The fact that Park allows Shibata's memory to include additional word line layers indisputably motivates combination.

III. CONCLUSION

For the reasons explained above—and in the Petition—the '623 patent's claims are unpatentable as obvious.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: April 11, 2025

/K. Patrick Herman/

K. Patrick Herman, Reg. No. 75,018
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019
Telephone: (212) 506-3596
Email: P52PTABDocket@orrick.com

Attorneys for Petitioner

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing reply complies with the type-volume limitation in 37 C.F.R. § 42.24. According to the utilized word-processing system's word count, the reply contains 5,591 words.

Dated: April 11, 2025

By: */K. Patrick Herman/*

K. Patrick Herman (Reg. No. 75,018)
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019-6142
Telephone: (212) 506-3596
P52PTABDocket@orrick.com

Counsel for Petitioner.

CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing paper and associated exhibits were caused to be served via email on the following counsel of record for Patent Owner on April 11, 2025:

James L. Davis, Jr. (James.L.Davis@ropesgray.com)
Andrew T. Radsch (Andrew.Radsch@ropesgray.com)
Christopher M. Bonny (Christopher.Bonny@ropesgray.com)
Allen S. Cross (allen.cross@ropesgray.com)
YMTC-Micron-IPRs-Ropes-Service@ropesgray.com
ROPES & GRAY LLP

/K. Patrick Herman/

K. Patrick Herman (Reg. No. 75,018)
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019-6142
Telephone: (212) 506-3702
P52PTABDocket@orrick.com