

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2024-00794
U.S. Patent No. 10,950,623

REPLY DECLARATION OF DR. JACK C. LEE

I, Dr. Jack C. Lee declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to reply to certain of the opinions set forth in the January 17, 2025 declaration of Kelin Kuhn, Ph.D. submitted by Patent Owner in an *inter partes* review proceeding relating to U.S. Patent No. 10,950,623, which I refer to herein as the ’623 patent.

3. I am being compensated at my current standard consulting rate, plus reimbursement for any reasonable expenses. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

4. The prior declaration I submitted in connection with this proceeding, which I understand has been designated as Ex. 1003, sets forth among other topics my educational background and professional experience (Ex. 1003, ¶¶ 5-13 and associated Exhibit 1022), my understanding of the law (*id.*, ¶¶ 18-33), an overview

of pertinent technical background (*id.*, ¶¶ 39-64), an overview of the '623 patent and its prosecution history (*id.*, ¶¶ 65-87), the knowledge and characteristics of a person having ordinary skill in the art (*id.*, ¶¶ 34-38), and certain claim construction opinions (*id.*, ¶¶ 88-91).

5. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, my work with those of ordinary skill at the time of the alleged invention, and my general experience in the field of art.

6. I have also reviewed and considered the materials listed in my prior declaration (*id.*, ¶ 17), the Board's Institution Decision (Paper 9), Patent Owner's Response (Paper 12), the Kuhn Declaration (Ex. 2010), and the following materials to the extent relevant to my opinions:

Exhibit	Description
2001	Cho et al., "A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single-Level Modes," IEEE J. of Solid-State Circuits, Vol. 36, No. 11, November 2001
2002	Lee et al., "Applications of AFM in semiconductor R&D and manufacturing at 45 nm technology node and beyond," Metrology, Inspection, and Process Control for Microlithography, Vol. 7272, SPIE, 2009.
2003	Xiao et al., "A high speed low power negative sensing architecture for 3D NAND Flash memory," 2016 China Semiconductor Technology International Conference (CSTIC), Shanghai, China, 2016.

2004	Bergonzoni, et al., “Reset Current Scaling in Phase-Change Memory Cells: Modeling and Experiments,” IEEE Transactions on Electron Devices, Vol. 59, No. 2, 283-291, Feb. 2012.
2005	Seshan et al., Handbook of Thin Film Deposition, Abstract, 2018
2006	Choi et al., “Novel ESD protection transistor including SiGe buried layer to reduce local temperature overheating,” IEEE Transactions on Electron Devices, Vol. 43, No. 3, 479-489, March 1996

II. RESPONSE TO CERTAIN OF PATENT OWNER’S ARGUMENTS

7. The paragraphs below respond to certain of the arguments and assertions made by Patent Owner and Dr. Kuhn in this proceeding. In these paragraphs, I address only a fraction of the opinions and assertions Dr. Kuhn set forth in her declaration. The fact that I do not respond to any particular opinion expressed by Dr. Kuhn should not be considered to indicate agreement with that opinion

A. Park – Claims 2 and 3

8. Claim 2 of the ’623 patent requires “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.” Claim 3 depends on claim 2.

9. As I explained in my prior declaration, Figure 36 of Park depicts a memory where a TSG—which is meant to be divided into separately controllable sub-TSGs—is located over the portion of Park’s memory where the BSG is

separated by the isolation insulating layers 111. I explained that a POSITA would have considered it obvious to include analogous layers 111 in the TSG in such circumstances to divide the TSG into sub-TSG as intended. *See* Ex. 1003, ¶¶ 205-223.

10. Dr. Kuhn responds to this by asserting that “there is no TSG in the region where Petitioner proposes adding the isolation insulating layer, because the TSG ends before it reaches that location.” Ex. 2010, ¶ 101.

11. Dr. Kuhn’s statement is directly contradicted by what is shown in Park’s figures, including Figure 36. Dr. Kuhn thus attempts to avoid this contradiction by asserting that Park’s figures include an “error.” *E.g., id.*, ¶ 104.

12. In my opinion, there is no error in Park. Instead, Dr. Kuhn is improperly attempting to impose limits on Park’s disclosure that simply are not there.

13. First, Park depicts un-divided conductive layers GL14 and GL15 directly over isolation regions 311 in multiple figures, including Figures 23 (showing undivided sacrificial layers 14 and 15 over divided sacrificial layer 1), Figure 29 (showing undivided sacrificial layers 14 and 15 and upper covering field insulation 370 over divided sacrificial layer 1), Figure 31 (showing formation of openings, where there are no openings in layers 14 and 15 above openings in layer 1), Figure 34 (showing undivided conductive layers 14 and 15 covered by field insulation 370

over divided conductive layer 1), and Figure 36 (again showing undivided conductive layers 14 and 15 covered by field insulation 370 over divided conductive layer 1). Further, Park also explains what these depicted undivided layers are in its specification, stating multiple times that they are meant to be the device's top "string select line[s]." *E.g.*, Park, 16:26-30; 16:20-37.

14. So, Dr. Kuhn is not opining that there is just one error. Instead, she has taken the position that Park erroneously drew five separate figures and then misdescribed the depicted layers in multiple textual passages.

15. This, in my opinion, is an extremely unreasonable and unjustified conclusion to reach. No reasonable POSITA would arrive at such a conclusion.

16. Dr. Kuhn points to the view provided in Figure 27 of Park and takes the position that all of Park must be arranged in exactly the same way shown in this figure. *See* Ex. 2010, ¶ 104.

17. A POSITA reading Park (at least one open to properly interpreting the reference), would not interpret Figure 27 to limit the reach of Park's disclosure. The figure is not meant to dictate the exact size and shape of Park's conductive layers across all its embodiments.

18. Instead, the figure is only meant to provide an example of the use of an upper "interlayer insulating layer 370" (or field insulating layer) that conformally

covers all of Park’s “pad regions PAD” along with a series of “channel structures CH and a plurality of dummy channel structures DCH....” Park, 13:35-44.

19. Further, rather than saying that its memory must be arranged in exactly the same way in all cases—with layers always positioned in exactly the same way relative to each other (which is how Dr. Kuhn apparently interprets Park)—Park expresses that its figures are meant only to depict “*examples*” of its “inventive concept.” *Id.*, 2:43-47. Similarly, Park explains that only “various examples of the inventive concept have been shown.” *Id.*, 18:4-9

20. Park also explains that its components can have different locations relative to each other. For example, its device’s “connecting electrodes” can be “disposed in different positions in the first direction” in “each gate electrode layer” as shown in some of Park’s example figures. And in some cases, the lower layers can alternatively be “disposed below” upper layers. *Id.*, 8:59-9:2; *see also id.*, 12:13-21 (referencing another example in which “connecting electrodes connecting the unit electrodes forming the word lines may be formed at the same positions in the first direction (the X-axis direction)”).

21. Further, Park also explains that its isolation insulation regions are not required to have a fixed location in all embodiments. Instead, they may instead “be formed in different positions in a first direction, for example, an X-axis direction.” *Id.*, 12:65-13:3. This reveals the primary issue with Dr. Kuhn’s analysis: she fails

to account for the fact that Park's gate electrodes can have different shapes, different relative locations, and different overlaps. She also fails to account for the fact that Park's layer 111 can have different locations. Instead, she improperly assumes that these components must be in exactly the same place in every figure. But this is not what Park teaches.

22. Because Park is plainly open to electrode layers with different sizes and physical extents, and because it is also open to trenches with different locations, a POSITA would not consider Figure 36 (or any other Park figure) to include an "error." Instead, it is simply representative of the breadth of Park's disclosure. The undivided, upper TSG layers are shown located over Park's layer 111 because this is one arrangement Park contemplates.

23. Further, I disagree that interpreting Park's figure as shown would "conflict with Park's disclosures because it would eliminate the necessary stepped structures used for cell contacts, rendering Park's device inoperable." Ex. 2010, ¶104. Dr. Kuhn arrives at this opinion only because she either fails (or refuses) to consider that isolation insulating layer 111 itself can be located in different places in the X-axis direction in Park's figures. Again, as I have explained, this is something Park expressly contemplates. Park, 12:65-13:3. Moving layer 111 towards the left in, for instance, Figure 3 of Park would situate it under both Park's BSG and TSG and would have no impact whatsoever on the stepped structure, the ability to

properly interconnect with Park's various gate electrode layers, or Park's operability. Dr. Kuhn does not appear to appreciate (or ignores) this.

24. In summary with respect to Claim 2, although Park does not explicitly depict trench division of the TSG, applying the same trench isolation technique to the TSG would represent a predictable structural adaptation. A POSITA would have found it obvious to extend the trenching approach for the BSG to the TSG, as doing so aligns with Park's overall design approach. Regarding Claim 3, a POSITA would have implemented aligned dielectric trenches as a straightforward design choice, recognizing that alignment enhances symmetry and promotes consistent electrical performance across the memory array.

B. Park – Claims 10 and 11

25. Claims 10 and 11 respectively require that the memory include “dummy” BSG and TSG that are also divided by “dielectric trenches.”

26. As I explained in my prior declaration, a POSITA would have considered it obvious to also divide these dummy layers (1) because Park associates them with the adjacent select gate layers, (2) because it was known that trenches can (and do) separate multiple adjacent layers, and (3) because separating both the select gates and the associated dummies would improve the electrical performance of Park's device. *See* Ex. 1003, ¶¶ 274-281.

27. With respect to electrical performance, a POSITA would have recognized and known that dummy cells connected to the dummy lines in a memory serve various important purposes, including suppressing leakage current and avoiding data disturb. In modern 3D NAND memory architectures, it was known that dummy cells are not merely passive filler structures; they play a critical electrical role in maintaining the integrity of the memory array, especially near the edges. These dummy cells are typically located at the periphery of each NAND string and are controlled by dummy gate lines — either dummy word lines or dummy select gates — that extend across the memory array. Although dummy cells do not store user data, they are designed to emulate the electrostatic environment of active memory cells. This helps prevent abrupt discontinuities in the electric field distribution, which can otherwise give rise to charge trapping anomalies, disturb behavior, or unintentional threshold voltage shifts in adjacent active cells. Furthermore, dummy cells suppress leakage currents by stabilizing the channel potential and gate field gradient near the edges, thus shielding internal active cells from abnormal parasitic effects. Therefore, a POSITA would have recognized that dummy cells are deliberately integrated into memory designs to ensure electrical uniformity, data retention reliability, and overall device robustness.

28. A POSITA also would have recognized that separating the dummies on the same sub-block basis as the select gates with dielectric trenches (instead of

allowing them to extend continuously across the memory like the word lines) would help the dummies perform these functions by making the “loading effects” across the memory “more symmetrical.” In a 3D NAND memory array where the BSG and TSG are divided into sub-blocks using dielectric trenches, each resulting sub-gate becomes electrically isolated and can be independently controlled. If the dummy gate electrodes — such as the dummy BSG or dummy TSG — are not similarly divided and instead extend continuously across the array, a POSITA would have recognized that they will exhibit different electrical behavior from the subdivided select gates. Specifically, the longer length of the undivided dummy gates leads to greater total gate capacitance and increased interconnect resistance, which can result in higher RC (resistance $\times$ capacitance) time constants and non-uniform voltage propagation along the gate line. This electrical mismatch introduces asymmetries between the dummy transistors and the adjacent select transistors, limiting the ability of the dummy cells to function as accurate electrical analogs of the cells located near the periphery of the memory array. By contrast, a POSITA would have known that dividing the dummy gate electrodes in alignment with the select gate sub-blocks allows for more consistent electrical loading conditions—both in terms of resistance, capacitance, and capacitive coupling — across the entire structure. This improved uniformity enhances the ability of the dummy cells to emulate the electrical

environment of neighboring active cells, thereby more effectively contributing to suppression of unwanted leakage and data disturb mechanisms.

29. A POSITA would have recognized that both the select transistors and dummy transistors would be subjected to the same load on their gate (rather than different loads), as the associated gate electrodes would be similarly divided. In NAND memory devices, the term “load on the gate” refers to the combined electrical effects that influence how a signal propagates through a gate electrode. These include the gate line’s resistance, its parasitic capacitance to neighboring structures (such as adjacent gates or channel regions), and capacitive coupling to other conductive layers. When select gate electrodes are divided into shorter segments — i.e., sub-gates — using dielectric trenches, the overall RC delay for each gate segment is reduced. This results in more uniform and faster voltage transitions along the gate, improving switching behavior and timing precision within each sub-block. However, if the dummy gate electrodes remain undivided, their longer span increases resistance and capacitance, leading to slower signal propagation, uneven voltage distribution, and greater susceptibility to coupling noise. These effects create mismatches in electrical behavior between the dummy transistors and the adjacent select transistors. A POSITA would have recognized that by dividing the dummy gates in a manner consistent with the select gates — i.e., using the same dielectric trenches to form sub-dummy gates — a designer ensures that both sets of transistors

experience comparable gate loading. This electrical symmetry helps the dummy cells maintain stable gate potentials under dynamic operation, thereby improving their ability to suppress leakage current and reduce unwanted interference such as data disturb. As a result, the overall performance and reliability of the memory array is enhanced through more consistent electrical behavior across all sub-blocks.

30. I also disagree with Dr. Kuhn’s opinion that my prior declaration “does not explain how a POSITA would have achieved ... modification in Park’s device.” Ex. 2010, ¶ 115. According to Dr. Kuhn, creating a trench that passes through multiple layers requires a “timed etch, which is not at all contemplated by Park.” *Id.* This is simply wrong. Park not only “contemplated” but actually uses timed etches. Park explains that the etching method it employs is able to remove both “sacrificial” and “insulating” layers at the same time (which a POSITA would have understood entails the use of a timed etch). Park, 13:18-25.

31. Further, I note that the prior art contains numerous examples of trenches extending through multiple layers. This clearly shows that such structures were not only achievable, but were routinely done in the art. *See, e.g.*, Shibata, Fig. 3 (element 60 separates multiple stacked layers); Ex. 1018, [0058] (multiple layers separated by trench 50). These disclosures confirm that extending trenches through multiple levels, including into dummy regions, was well within the ordinary skill of a POSITA. Accordingly, prior art such as Park and Shibata supports the use of dummy

gate structures with trenching, and extending those trenches into dummy regions would have been a straightforward and predictable design choice for a POSITA. Nor would employing a timed etch to form a trench in Park's upper select gate and dummy layers risk etching the word lines below it. A POSITA would have understood that multiple dummy layers are included for this very purpose. By including multiple dummy layers—some of which are divided by an etched trench and others of which are not—the dummies serve as a buffer preventing etching of the word lines below.

C. Application of Shibata to Park

32. I also explained in my prior declaration why a POSITA would have considered it obvious to apply Shibata's teachings to Park and make Park's layers 111 longer. *See* Ex. 1003, ¶¶ 292-324.

33. Dr. Kuhn asserts that a POSITA would not have applied Shibata to Park because Park purportedly "discourages elongating the isolation insulating layers because the longer paths by which the etching solution must flow could prevent the complete removal of the sacrificial layer and cause voids in the gate electrode layers GLs." Ex. 2010, ¶ 136.

34. I disagree. Once again, Dr. Kuhn's opinion is based on an extremely narrow reading of Park that does not account for everything it teaches (let alone everything a POSITA would have known).

35. I recognize that Park does reference a “problem” that may be encountered when “etching” “sacrificial layers.” *See* Park, 15:35-63. Park also makes clear, however, that this “problem” is one that arises when using an “etching solution” like “phosphoric acid” to remove “sacrificial layers.” *Id.* Park characterizes this method of etching as “an example.” *Id.*, 15:35-42.

36. In my opinion, a POSITA would have known and understood that alternative etching techniques were also available to remove Park’s sacrificial layers. This would include, for instance, dry plasma etching. In contrast to wet etching using a “solution” as illustrated in Park’s example, dry etching is less inhibited by narrow paths and is capable of reaching confined regions more effectively. This ensures more consistent performance even in complex or confined structures. Thus, the “problem” discussed in Park would not arise when employing dry etching methods.

37. The fact that Park does not explicitly reference these types of etching is not pertinent. They were well known and thus would have been considered for use in place of Park’s “example” method. That is plainly what Park means when it uses the word “example”: wet etching with phosphoric acid is only meant to be a non-limiting example. Dr. Kuhn does not appear to engage in such an analysis. She does not consider the other types of etching known in the art. Instead, all she does is note that Park references etching with phosphoric acid.

38. Next, even if a POSITA continued to employ a wet etch technique using phosphoric acid, Park provides a variety design and manufacturing approaches that are specifically intended to allow for different sized and shaped layers 111 (including layers 111 with increased length) while minimizing any problems.

39. Because of this, in my opinion, a POSITA would have understood that this would have readily allowed Park to accommodate larger (and more) isolation insulation layers 111 like those in Shibata.

40. For example, Park explains that “second dummy channel structures DCH2” may be formed in the area of the layers 111 to “shorten inflow passages of phosphoric acid and conductive material therethrough in a process of forming gate electrodes.” Park, 11:52-55; *see also id.*, Fig. 14. Forming these dummy channels in the area of layers 111 avoids any “degradation of the characteristics of the memory device” that results from incomplete etching. *See id.*, 11:55-59.

41. Next, Park explains that “open regions corresponding to ... vertical insulating layers 209” or “209A” can also be employed to “shorten the inflow passages of the phosphoric acid and the conductive material.” *Id.*, 12:10-52; *see also id.*, Figs. 16-17.

42. As shown below, including these open regions (annotated in teal) allows for formation of longer trenches that are not staggered from each other.

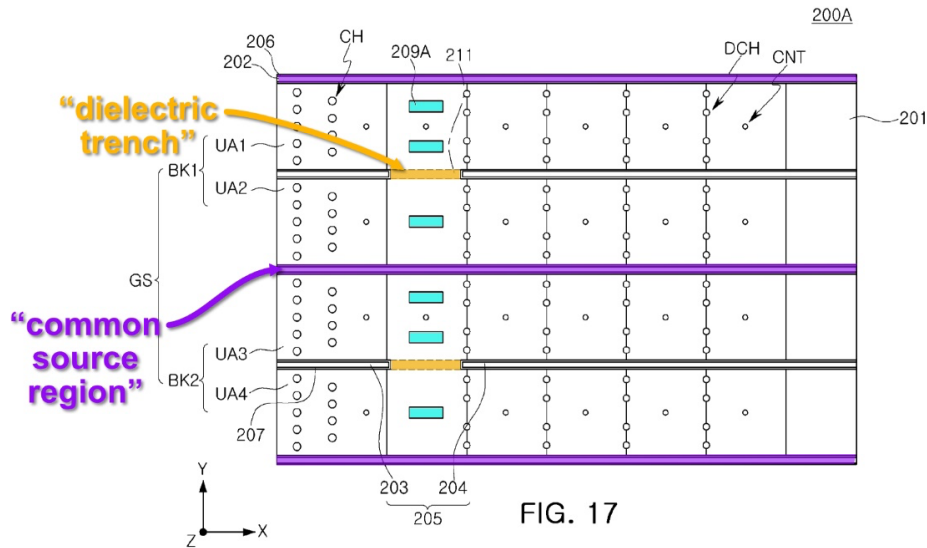


FIG. 17

Id., Fig. 17 (annotated).

43. So, Park does not “discourage” a POSITA from using longer trenches. Instead, it encourages this not only by showing embodiments that employ longer trenches, but by providing design alternatives that are specifically meant to allow for adjustments to the size, shape, and location of its trenches.

44. Dr. Kuhn is also wrong when she asserts that there would be “no flow path” allowing for the removal of sacrificial layers in certain areas of Park’s device. Ex. 2010, ¶ 141. Dr. Kuhn identifies areas where she claims there will be no flow in light green in the demonstrative from her declaration reproduced below:

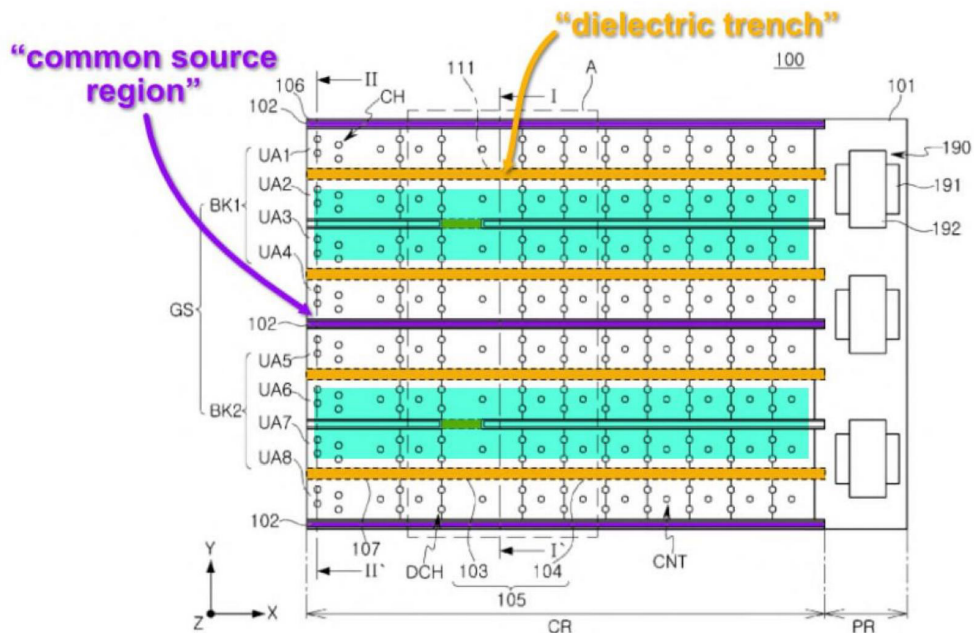


FIG. 3

Id.

45. Dr. Kuhn, however, inexplicably ignores that there are remaining common source lines 103 and 104 located right down the middle of the green area she annotates. And etchant will still flow into Park's device via not only the dark purple common source lines, but also these remaining common source lines (shown in light purple below):

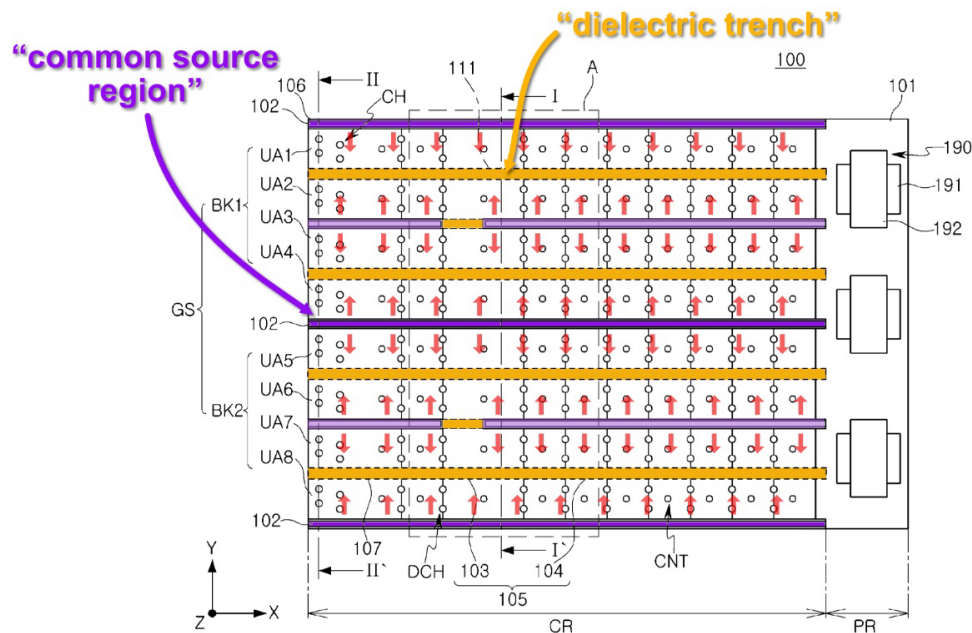


FIG. 3

46. Because of this, the vast majority of Park’s device will still be subjected to significant etchant flow, including the green areas highlighted by Dr. Kuhn.

47. Moreover, a POSITA would have recognized that any problem areas where etchant flow is less than ideal could be readily addressed by (1) employing any of the methods that Park teaches (such as the use of dummy channels to supplement flow discussed above) or (2) using Shibata’s tailored drivers (which I discussed in my prior declaration at Ex. 1003, ¶¶ 320-321).

48. Finally, I disagree with Dr. Kuhn’s opinion that removal of certain of Park’s common source lines would have “adverse effects on the memory device.” Ex. 2010, ¶ 144.

49. Dr. Kuhn cites a number of documents (including Exhibits 2001-2006), but none of those suggests that any sort of minimum quantum of common source lines must pass vertically through a memory device to achieve proper performance.

50. Instead, at best, the documents Dr. Kuhn cites appear to relate to either the resistance of or noise experienced by the single common source line located at the source-side of a NAND memory's array (i.e., located below the memory). *See generally id.*

51. None of these documents even depicts the type of “common source region” required by the claims here (i.e., one that passes vertically through a memory array). None explains that there is any benefit or advantage deriving from the use of such a region (let alone more such regions). Thus, Dr. Kuhn appears to have manufactured her opinion entirely on her own without any support whatsoever in a cited document. A summary of each document follows:

- **Ex. 2001:** This document relates to dual-mode MLC/SLC switching, not common source line (or “CSL”) routing or isolation. While the document does reference “noise,” a POSITA would have recognized that the use of more dielectric trenches would reduce lateral capacitive coupling which would in turn reduce crosstalk, not increase it.
- **Ex. 2002:** This document relates to AFM-based metrology and does not address CSL resistance as a limitation in 3D NAND design. Even

assuming CSL resistance increases marginally, a POSITA would have understood that such a trade-off is acceptable if the selective reduction of CSLs through the use of dielectric trenches enables meaningful improvements in control granularity, sub-block program/erase performance, and electrical isolation (as it does here).

- **Ex. 2003:** This document discusses bit line pre-charging and sensing, not source line design or topology. In any case, a POSITA would have understood that modern NAND architectures incorporate localized charge pumps and level shifters to manage voltage regulation, thereby mitigating any adverse effects from potential CSL voltage drops.
- **Ex. 2004:** This document focuses on phase-change memory (PCM), which has completely different failure mechanisms than NAND flash. In NAND, gate oxide wear-out, retention loss, and disturb are more critical than source-line stress. Moreover, in NAND, mitigation techniques (e.g., staggered program schedules or duty cycle balancing) were known to address current-related degradation.
- **Ex. 2005:** This document discusses CMOS scaling challenges broadly, not CSL routing in NAND.
- **Ex. 2006:** This document addresses ESD transistors, not memory array layout or CSL design.

52. Further, these references note that there are other factors to consider (which Dr. Kuhn has entirely ignored). For instance, “Decreasing the CSL resistance can reduce the CSL noise at the expense of chip size.” Ex. 2001, p. 5.

53. Consistent with this, Park itself says that its device should be designed in a way that “increas[es] the capacity of a memory device and the degree of integration thereof.” Park, 17:1-5 (emphasis added). Park also itself already includes examples that employ fewer common source lines, thereby making room for additional memory cell strings. Park, Figs. 16-17 (showing a memory with only 5 common source regions, fewer than the 9 employed in Figure 3).

54. A POSITA would have recognized that this is exactly what application of Shibata’s teachings to Park does: by eliminating common source lines, more memory cells can be included, thus increasing the capacity of the memory without increasing its physical size. Additionally, even if there were some sort of issue with the current density in Park’s common source lines (there is not), a POSITA would have readily understood that this would be addressed by straightforward design choices such as: slightly widening remaining CSLs, using metal layers with lower resistivity (e.g., Cu or W), and/or reducing the number of concurrently active strings per sub-block.

D. Application of Park to Shibata

55. I disagree with Dr. Kuhn’s opinion that applying Park to Shibata (and replacing Shibata’s multiple lower select gates with a single divided/separated gate) would not simplify manufacturing.

56. Shibata’s figures depict the use of three lower select gates (labeled (SGS0A, SGS1A, SGSB). *See, e.g.,* Shibata, Fig. 16.

57. Each of these includes an associated, intervening layer of insulation. *See id.*

58. Because there are three select gate layers and three associated insulating layers, manufacture of this structure will take at least 6 steps (one deposition step for each gate and insulating layer).

59. Replacing Shibata’s three select gate layers with a single, separated layer following Park’s teachings will require two deposition steps: one for the remaining select gate and another for the associated layer of insulation.

60. Additionally, as Dr. Kuhn notes, employing Park requires two additional steps: “form[ing] a mask” and then “form[ing] slits by etching” would be required. Ex. 2010, ¶ 160.

61. While Dr. Kuhn references a third step — “form[ing] insulating material into the slits” — this could be accomplished at the same time the next insulating layer in the stack is added. A separate step would not be required.

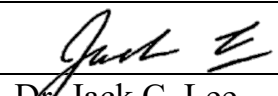
62. So, application of Park would in fact reduce manufacturing steps: Shibata's six step process (3 gate depositions, 3 insulating layer depositions) would be reduced to four (1 gate deposition, 1 mask, 1 etch, 1 insulating layer deposition).

63. This, however, is plainly a secondary benefit. As I explained in my prior declaration, the primary benefit of applying Park's teachings to Shibata is that doing so would allow Shibata to include additional wordline layers thus increasing the total number of memory cells without increasing the overall size of Shibata's memory. *See* Ex. 1003, ¶¶ 385-390.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: April 11, 2025

Location: Austin TX

Signature: 
Dr. Jack C. Lee