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Transcript of Jack Lee, Ph.D.

Date: May 28, 2025

Case: Micron Technology, Inc. -v- Yangtze Memory Technologies Company, LTD.
(PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

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Micron v. YMTC
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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

- - - - - x

MICRON TECHNOLOGY, INC. :
Petitioner, : Case IPR2024-00794
v. :
YANGTZE MEMORY TECHNOLOGIES : U.S. Patent No.
COMPANY, LTD., : 10,950,623
Patent Owner. :

- - - - - X

Videotaped Deposition of JACK C. LEE, Ph.D.
Conducted Virtually
Wednesday, May 28, 2025
9:01 a.m. EDT

Job No.: 585429
Pages 1 - 102
Reported by: Debra A. Whitehead

1 Videotaped Deposition of JACK C. LEE, Ph.D.,
2 conducted virtually.
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5 Pursuant to notice, before Debra Ann Whitehead,
6 E-Notary Public in and for the Commonwealth of
7 Virginia.
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A P P E A R A N C E S

ON BEHALF OF PETITIONER:

K. PATRICK HERMAN, ESQUIRE

ORICK, HARRINGTON & SUTCLIFFE LLP

51 West 52nd Street

New York, New York 10019-6142

(212) 506-3596

ON BEHALF OF PATENT OWNER:

ALLEN S. CROSS, ESQUIRE

ROPES & GRAY LLP

2099 Pennsylvania Avenue, NW

Washington, DC 20006

(202) 508-4708

ALSO PRESENT:

KELLI WELCH, Video Specialist

C O N T E N T S

EXAMINATION OF JACK C. LEE, Ph.D.	PAGE
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By Mr. Cross	6
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EXHIBITS MARKED IN TODAY'S SESSION

(None marked)

EXHIBITS MARKED IN PRIOR SESSIONS

(Not attached)

DEPOSITION EXHIBIT	PAGE
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P R O C E E D I N G S

VIDEO SPECIALIST: Here begins Media
Number 1 in the videotaped deposition of Jack Lee,
Ph.D.; in the matter of Micron Technology, Inc., v
Yangtze Memory Technologies Company, LTD; in the
United States Patent and Trademark Office, before
the Patent Trial and Appeal Board; Case Number
IPR2024-00794.

Today's date is May 28th, 2025. The time
on the video monitor is 9:01 a.m. eastern time.
The remote videographer today is Kelli Welch,
representing Planet Depos. All parties of this
video deposition are attending remotely.

Would counsel please voice-identify
themselves and state whom they represent.

MR. CROSS: Allen Cross from Ropes &
Gray, on behalf of Yangtze Memory Technologies.

MR. HERMAN: Patrick Herman from Orrick,
Herrington & Sutcliffe, here on behalf of
Petitioner Micron.

VIDEO SPECIALIST: The court reporter
today is Debbie Whitehead, representing Planet

1	Depos.	09:02:16
2	The witness will now be sworn.	09:02:30
3	JACK C. LEE, Ph.D.,	09:02:30
4	having been duly sworn, testified as follows:	09:02:33
5	EXAMINATION BY COUNSEL FOR PATENT OWNER	09:02:33
6	BY MR. CROSS:	09:02:33
7	Q Good morning, Dr. Lee.	09:02:36
8	A Good morning.	09:02:40
9	Q Can you just for the record state where	09:02:40
10	you're currently located?	09:02:45
11	A I'm currently located in Austin, Texas.	09:02:49
12	Q And can you let us know what's in front	09:02:55
13	of you? Is it just the computer monitor, or do	09:03:01
14	you have other documents in front of you?	09:03:04
15	A No, I don't have any document in front of	09:03:06
16	me.	09:03:09
17	Q Do you have anything else up on the	09:03:09
18	screen other than the Zoom deposition?	09:03:13
19	A No.	09:03:17
20	Q You understand that you're under oath	09:03:18
21	today?	09:03:22
22	A Yes.	09:03:22

1	Q	I know we've gone through this in other	09:03:22
2		depositions, but just as a reminder. I'll be	09:03:27
3		asking the questions, and you'll be answering	09:03:31
4		them. If you don't mind, please wait for me to	09:03:33
5		finish, and I'll try to wait for you to finish.	09:03:36
6		Is there any reason why you cannot	09:03:41
7		testify truthfully and fully today?	09:03:43
8	A	No.	09:03:46
9	Q	And if I ask a question that you don't	09:03:46
10		understand, you'll ask for a clarification,	09:03:50
11		otherwise I'll assume that you understand the	09:03:53
12		question. Correct?	09:03:55
13	A	Yes.	09:03:58
14	Q	For today's deposition, how did you	09:03:58
15		prepare?	09:04:04
16	A	I read my reply declaration and all the	09:04:07
17		relevant documents related to my reply	09:04:20
18		declaration.	09:04:24
19	Q	And when you say, all the relevant	09:04:28
20		documents related to your reply declaration, what	09:04:32
21		does that entail?	09:04:38
22	A	Do you have -- would you mind, do you	09:04:44

1	have my reply declaration?	09:04:46
2	Q I do. We can get into that a little bit	09:04:51
3	later. But did you review anything outside of	09:04:54
4	what you cited in your reply declaration?	09:04:57
5	A I reviewed all the documents cited in my	09:05:11
6	declarations. I may have reviewed other	09:05:19
7	references, but I don't recall exactly. But	09:05:27
8	mainly what I cited in my declarations.	09:05:38
9	Q So what you cited in your first and	09:05:43
10	second declarations is what you primarily	09:05:45
11	reviewed?	09:05:47
12	A Yes.	09:05:51
13	Q You're very familiar with the 3D NAND	09:05:51
14	fabrication process. Correct?	09:06:08
15	A Yes.	09:06:09
16	Q And you've, in fact, fabricated 3D NAND	09:06:09
17	memory devices?	09:06:16
18	A My student and I have work on related	09:06:18
19	fabrication issues related to 3D NAND.	09:06:32
20	Q And what would those fabrication issues	09:06:39
21	be?	09:06:40
22	A For example, if you look in my CV, that I	09:06:43

1	have many publication related to nonvolatile	09:06:52
2	memory application, which is what 3D NAND is	09:06:56
3	about; such as, what is the issues in fabrication	09:07:01
4	related to tunnel oxide, charge storage layer, and	09:07:15
5	blocking oxide, dielectrode, and so on and so	09:07:24
6	forth.	09:07:31
7	Q Would you agree that those same issues	09:07:31
8	apply to 2D NAND memory devices?	09:07:37
9	MR. HERMAN: Objection. Form. It's	09:07:40
10	outside the scope of direct.	09:07:41
11	A I -- can you repeat that question?	09:07:58
12	Q Would you agree that the issues you	09:08:00
13	identified are the same types of issues you would	09:08:03
14	encounter when fabricating 2D memory devices?	09:08:07
15	MR. HERMAN: Same objection.	09:08:12
16	A I think you're asking me something I	09:08:15
17	didn't really address in my reply declarations.	09:08:20
18	Am I missing something? Can you point to where I	09:08:28
19	address this issue in my reply declarations?	09:08:37
20	Q We can get to that in a little bit. But	09:08:41
21	you testified that you had worked on related	09:08:52
22	fabrication issues related to 3D NAND.	09:08:54

1	What were you working on when you came	09:08:59
2	across those fabrication issues?	09:09:04
3	A Well, there are many issues. Again, I	09:09:11
4	don't think I addressed the issue related to your	09:09:13
5	question in my reply declaration. And my	09:09:18
6	understanding is that that is not something	09:09:25
7	specifically that I prepared for testifying today.	09:09:35
8	Q You agree that today's deposition is	09:10:00
9	related to the fabrication of 3D NAND memory	09:10:02
10	devices?	09:10:05
11	MR. HERMAN: Objection. Form.	09:10:07
12	A I understand that today's testimony is	09:10:15
13	related to my reply declaration.	09:10:19
14	Q Do you recall whether or not you	09:10:26
15	addressed 3D NAND memory in your reply	09:10:28
16	declaration?	09:10:32
17	A If possible, can you point out to where	09:10:37
18	that is in my reply declaration?	09:10:43
19	Q Dr. Lee, do you not recall whether or not	09:10:50
20	your reply declaration addresses 3D NAND memory?	09:10:53
21	MR. HERMAN: Objection. Form.	09:10:59
22	A It will be great if you can point out	09:11:05

1	where in my declaration, reply declaration, that I	09:11:06
2	addressed this particular topic you are referring	09:11:12
3	to.	09:11:16
4	Q That wasn't my question, Dr. Lee. If you	09:11:19
5	can provide an answer, do you recall whether or	09:11:23
6	not your reply declaration is directed to 3D NAND	09:11:26
7	memory?	09:11:29
8	MR. HERMAN: Objection. Form.	09:11:32
9	A My reply declaration focuses on	09:11:50
10	responding to Dr. Kuhn's opinion set forth in her	09:11:55
11	declaration.	09:12:11
12	Q Dr. Lee, when did you review your	09:12:17
13	declaration?	09:12:20
14	A When did I review which declaration?	09:12:29
15	Q When was the last time you reviewed your	09:12:31
16	rebuttal declaration, your second declaration	09:12:38
17	filed in this matter?	09:12:40
18	A Do you mean my reply declaration?	09:12:43
19	Q Yes.	09:12:47
20	A Yesterday and the day before.	09:12:53
21	Q Do you recall whether or not you	09:13:02
22	addressed 3D NAND memory in your declaration?	09:13:04

1	MR. HERMAN: Objection. Form.	09:13:09
2	A I understand that this is not a memory	09:13:19
3	test. So if you can point to where in my reply	09:13:21
4	declaration that I address the issues that related	09:13:26
5	to your question, I would really appreciate it.	09:13:31
6	Q Do you know what patent this deposition	09:13:33
7	is about?	09:13:40
8	A This deposition is related to the '623	09:13:51
9	patent.	09:13:57
10	Q Is the '623 patent directed towards 3D	09:13:59
11	NAND memory?	09:14:02
12	A Do you have a copy of the '623 patent	09:14:13
13	that I can take a look?	09:14:17
14	Q Did you review the '623 patent in	09:14:19
15	preparing for this deposition?	09:14:21
16	A Yes.	09:14:24
17	Q When was the last time you reviewed the	09:14:24
18	'623 patent?	09:14:28
19	A Probably a few days ago.	09:14:34
20	Q Do you remember whether or not the '623	09:14:36
21	patent is directed towards 3D NAND memory?	09:14:38
22	A Yes, it is related to 3D memory device.	09:14:48

1	Q	Do you recall whether or not your	09:14:52
2		declaration is directed towards 3D NAND memory?	09:15:01
3	A	Which declaration?	09:15:10
4	Q	Either.	09:15:11
5	A	My original declaration and my reply	09:15:20
6		declarations?	09:15:23
7	Q	That's correct. Are either of those two	09:15:25
8		declarations directed towards 3D NAND memory?	09:15:27
9		MR. HERMAN: Objection. Form.	09:15:31
10	A	Well, both of my declarations, my	09:15:40
11		original declaration and my reply declaration, are	09:15:49
12		related to the '623 patent, which is related to	09:15:55
13		the 3D NAND memory device and fabrications. So,	09:16:00
14		therefore, the original declaration is related to	09:16:12
15		3D NAND memory and fabrications. And my reply	09:16:22
16		declaration focuses on respond to Dr. Kuhn's	09:16:30
17		declarations and which is related to '623 patent,	09:16:36
18		and, therefore, indirectly related to the 3D NAND.	09:16:44
19		But the focus is on responding to	09:16:52
20		Dr. Kuhn's declaration.	09:16:57
21	Q	Now, since you agree that your reply	09:17:01
22		declaration is directed towards 3D NAND memory	09:17:11

1	devices, would it be fair to ask you questions	09:17:14
2	about --	09:17:17
3	A Hello?	09:17:45
4	(Discussion off the record; technical	09:17:51
5	difficulty.)	09:18:05
6	Q So now that we agree that your reply	09:18:05
7	declaration is directed towards 3D NAND memory	09:18:09
8	devices, would it be fair to ask you questions	09:18:11
9	about fabrication of 3D NAND memory and the issues	09:18:13
10	that arise during fabrication?	09:18:18
11	A I believe that today's testimony is	09:18:32
12	related to my reply declarations. The	09:18:35
13	fabrications of 3D NAND memory device is something	09:18:43
14	I believe that I addressed in my first declaration	09:18:51
15	and it is not something specifically that I have	09:19:06
16	prepared for my testimony today.	09:19:13
17	Q So to the best of your recollection, your	09:19:21
18	reply declaration is not directed towards the	09:19:26
19	fabrication of 3D NAND memory.	09:19:29
20	Is that correct?	09:19:31
21	MR. HERMAN: Objection. Form.	09:19:32
22	A Again, my reply declaration is to respond	09:19:33

1	to Dr. Kuhn's opinion in her declaration. And the	09:19:48
2	topic that you're asking me is -- were addressed	09:20:05
3	in my original declaration.	09:20:12
4	Q Was the same topic addressed in your	09:20:18
5	reply declaration?	09:20:21
6	A My reply declaration focuses on	09:20:31
7	responding to the opinion that Dr. Kuhn provided	09:20:32
8	in her declaration and not specifically focus on	09:20:44
9	the fabrications of 3D NAND memory devices.	09:20:58
10	Q So it's your testimony that Dr. Kuhn did	09:21:06
11	not address 3D NAND memory fabrication in her	09:21:10
12	declaration?	09:21:14
13	MR. HERMAN: Objection. Form.	09:21:16
14	A I understand that the deposition is not a	09:21:30
15	memory test. So if you can give me Dr. Kuhn's	09:21:32
16	declaration, that would be helpful. But in a very	09:21:37
17	general sense, Dr. Kuhn's declaration is -- was	09:21:45
18	addressing my opinion in my original declaration,	09:22:02
19	I believe. And which, of course, all of it is	09:22:07
20	related to '623 patent, which is, as I mentioned	09:22:14
21	before, is related to 3D NAND fabrications and	09:22:21
22	devices.	09:22:25

1	Q	If everything is related to 3D NAND	09:22:29
2		fabrication and devices, is it fair to say that	09:22:32
3		your reply declaration is directed towards 3D NAND	09:22:35
4		fabrication?	09:22:39
5	MR. HERMAN:	Objection. Form.	09:22:41
6	A	Not directly.	09:22:46
7	Q	Not directly?	09:22:47
8	A	Again, my reply declarations is direct to	09:22:52
9		my respond to Dr. Kuhn's opinion in her	09:23:04
10		declaration.	09:23:09
11	Q	So it's your testimony today that your	09:23:16
12		reply declaration is not directly related to 3D	09:23:21
13		NAND memory fabrication.	09:23:23
14	MR. HERMAN:	Objection. Form.	09:23:28
15	A	Again, I was asked to respond to	09:23:33
16		Dr. Kuhn's opinion in her declaration, and	09:23:40
17		indirectly related to the 3D NAND fabrication,	09:23:55
18		that the focus of my reply declaration is to	09:24:06
19		respond to her opinion.	09:24:12
20		So if you like to ask me questions	09:24:17
21		specifically related to 3D NAND fabrication, I	09:24:20
22		would appreciate that you give me my reply	09:24:27

1	declarations and point to where I have addressed	09:24:33
2	directly 3D NAND fabrication issue that you like	09:24:41
3	to ask me.	09:24:48
4	Q Dr. Lee, do you believe that you're an	09:24:54
5	expert in this field of -- strike that.	09:25:03
6	Dr. Lee, are you at least at the level of	09:25:09
7	a POSITA as you set forth in this IPR?	09:25:13
8	A Yes, I believe so.	09:25:23
9	Q And, Dr. Lee, you've been retained as an	09:25:26
10	expert in this IPR. Correct?	09:25:28
11	A Yes.	09:25:30
12	Q Why have you been retained as an expert?	09:25:30
13	A What do you mean, "why"?	09:25:45
14	Q Have you been retained as an expert	09:25:47
15	because of your expertise in semiconductor	09:25:49
16	fabrication?	09:25:53
17	A I believe so.	09:25:57
18	Q And have you been retained as an expert	09:26:00
19	in this case because you have experience with 3D	09:26:03
20	NAND technology?	09:26:06
21	A I believe so.	09:26:09
22	Q As an expert in this case, can you please	09:26:11

1	tell me what issues -- strike that.	09:26:14
2	As an expert in this case, would it be	09:26:32
3	fair to ask you questions about 3D NAND	09:26:34
4	fabrication?	09:26:36
5	MR. HERMAN: Objection. Form.	09:26:40
6	A You can ask me about 3D NAND fabrication	09:26:50
7	issue. And I believe that I address some of these	09:26:54
8	issue, including technology background, in my	09:27:07
9	original declaration, and it is not something	09:27:12
10	specifically that I prepared for my testimony	09:27:18
11	today. But you can ask. And if you can provide	09:27:23
12	me my reply declaration. And if you have specific	09:27:29
13	question related to my original declaration,	09:27:41
14	please provide that as well.	09:27:47
15	Q Previously you mentioned issues in	09:27:56
16	fabrication of 3D NAND structures include issues	09:28:01
17	related to tunnel oxide, charge storage layer, and	09:28:05
18	blocking oxide, and others.	09:28:09
19	Do you recall that?	09:28:14
20	A Well, those are just some examples.	09:28:19
21	Q Are there other examples of issues that	09:28:21
22	you've dealt with during your experience	09:28:25

1	fabricating devices that relate to 3D NAND?	09:28:27
2	A Well, my student and I have worked on	09:28:40
3	various issues that directly or indirectly related	09:28:43
4	to 3D NAND. For example, etching is one issue	09:28:49
5	that is -- that is related to 3D NAND. And we	09:28:55
6	have done a lot of work in related to etching,	09:29:07
7	whether it's selective etch or time etch.	09:29:13
8	We also study various dielectrics, as I	09:29:18
9	mentioned tunnel, tunneling dielectric, blocking	09:29:31
10	dielectric, interlayer insulating dielectric, and	09:29:39
11	so on and so forth.	09:29:57
12	So there are various issues directly or	09:29:59
13	indirectly related to 3D NAND that we have	09:30:05
14	studied.	09:30:09
15	Q Have you ever fabricated a 3D NAND	09:30:18
16	device?	09:30:33
17	A You mean by myself?	09:30:37
18	Q Yeah. Have you ever worked on the actual	09:30:41
19	fabrication process?	09:30:42
20	A That the entire 3D NAND? What -- so	09:30:48
21	remember, 3D NAND is a very complicated device.	09:30:56
22	And a company with a team of people, and engineers	09:31:10

1 and technicians, work together to fabricate a 3D
2 NAND chip. It is not something that a person -- a
3 single person can design and fabricate and the
4 entire 3D NAND and packages by themselves.

5 So to answer your question that I,
6 myself, have studied, together with my students,
7 various issues related to 3D NAND memory device.
8 And we -- we have fabricated individual memory
9 cell, and including, as I mentioned, etching
10 issues, dielectric issues, contact issues, metal
11 issues.

12 But if you are saying 3D NAND device,
13 yes, we have -- we have fabricated individual 3D
14 NAND memory cell. But in terms of the entire
15 megabit, gigabit 3D NAND, I don't think any one
16 single person would be able to fabricate such
17 device by themselves. It require a team of
18 engineers and technicians to do so.

19 Q When you fabricated the 3D memory cell,
20 did you use photolithography?

21 A Yes.

22 Q Can you describe the process of how

09:31:13

09:31:18

09:31:24

09:31:31

09:31:35

09:31:41

09:31:49

09:31:57

09:32:06

09:32:12

09:32:19

09:32:24

09:32:27

09:32:32

09:32:43

09:32:50

09:32:53

09:32:57

09:32:59

09:33:10

09:33:16

09:33:16

1	photolithography works?	09:33:20
2	A Well, photolithography involve imaging of	09:33:28
3	a -- of a mask -- through a mask. And it also	09:33:33
4	related to what is called the photoresist process.	09:33:47
5	So it's a standard process in	09:34:08
6	semiconductor fabrications which essentially	09:34:17
7	transfer the image from the mask onto a wafer.	09:34:25
8	So the process, like I said, involve	09:34:38
9	coating of a layer called photoresist --	09:34:42
10	photoresist, which is light sensitive and resist	09:34:52
11	to certain chemical. And then you expose the	09:34:56
12	photoresist through a mask, or sometimes called a	09:35:08
13	photo mask. The mask contain the information of	09:35:16
14	the integrated circuit.	09:35:22
15	The next step involve development of the	09:35:30
16	photoresist using chemical solutions, which would	09:35:36
17	remove the exposed portion of the photoresist or	09:35:46
18	unexposed portion of the photoresist, depending on	09:35:57
19	whether it is a so-called positive photoresist or	09:36:04
20	negative photoresist.	09:36:06
21	The next step will be some type of	09:36:12
22	etching if this is for etching steps or some kind	09:36:18

1 of dopant, for example ion implantations. 09:36:25

2 So the final step after you transfer the 09:36:35

3 image to the photoresist and then use the 09:36:45

4 photoresist to either etch the underlying layer or 09:36:48

5 to dope the substrate with impurity such as 09:36:54

6 arsenic or boron, the final step is to remove the 09:37:01

7 photoresist, followed by cleaning of the wafers. 09:37:07

8 So that's generally the process of 09:37:13

9 photo -- photolithography in semiconductor 09:37:19

10 manufacturing. I mean, this is just an overview 09:37:22

11 of what photolithography is. And I don't think I 09:37:30

12 described this in my reply declarations or the 09:37:37

13 original, my first declaration. 09:37:45

14 Q Are you familiar with the term "hard 09:37:49

15 mask"? 09:38:01

16 A I don't think I describe this in my reply 09:38:05

17 declaration. If I miss something, can you point 09:38:12

18 that out, point that to me? 09:38:15

19 Q Before we do that, are you familiar with 09:38:18

20 the term "hard mask"? 09:38:37

21 A Yes. 09:38:49

22 Q Can you explain what a hard mask is? 09:38:49

1	A	Well, a hard mask is something that is	09:38:56
2		very durable, in general etch resistant and so,	09:39:12
3		therefore, is hard, and is used as a masking layer	09:39:23
4		for either etching of the underlying layer or	09:39:30
5		doping of the underlying layer.	09:39:39
6	Q	Is there a reason why you would use a	09:39:51
7		hard mask instead of just a photoresist as a	09:39:54
8		masking layer for depositing dopants or etching	09:39:56
9		underlying layers?	09:40:00
10	MR. HERMAN:	Objection. Outside the	09:40:06
11		scope of direct.	09:40:07
12	A	Then I understand that this testimony is	09:40:13
13		related to my reply declaration. And if that is	09:40:17
14		something that I address in my reply declaration,	09:40:24
15		can you please point that out to me where I said	09:40:32
16		so?	09:40:36
17	Q	Do you need to see your reply declaration	09:40:46
18		in order to answer the question?	09:40:48
19	A	No. But I'm saying that the focus of my	09:40:51
20		declaration -- focus of my testimony today I	09:40:55
21		believe is related to my reply declaration, and	09:41:00
22		your question is outside of my -- outside of scope	09:41:09

1	of my testimony. But I will answer your question	09:41:14
2	that the reason why hard mask is used instead of	09:41:22
3	just photoresist is because hard mask is made of	09:41:25
4	material such as silicon dioxide, silicon nitride.	09:41:30
5	And those material can with stand high	09:41:40
6	temperature, whereas a photoresist cannot	09:41:43
7	withstand high temperature and cannot withstand	09:41:48
8	certain chemical solution.	09:41:53
9	So, therefore, a hard mask is used -- you	09:41:58
10	can think of a hard mask as an intermediate	09:42:04
11	patterning layer that transfer the pattern from	09:42:08
12	the photoresist to a silicon dioxide layer,	09:42:14
13	so-called hard mask, or silicon nitride layer.	09:42:24
14	Those are known as hard mask. And those material	09:42:28
15	can better withstand high temperature.	09:42:37
16	So if the dopant process require high	09:42:42
17	temperature, photoresist cannot withstand as such	09:42:48
18	at high temperature, and hard mask is used. And	09:42:59
19	if the process require etching of certain	09:43:05
20	chemicals photoresist cannot withstand, then hard	09:43:15
21	mask is also used.	09:43:23
22	So in short, you can think of hard mask	09:43:24

1	as an intermediate patterning layer.	09:43:28
2	Does that make sense?	09:43:35
3	Q That makes sense. Thank you.	09:43:37
4	In your fabrication experience when you	09:43:43
5	fabricated memory cells for 3D NAND, did you use	09:43:45
6	chemical vapor deposition?	09:43:51
7	A Again, I believe that I am here to	09:44:00
8	describe my -- to answer question related to my	09:44:11
9	reply declaration, and your question is not	09:44:14
10	something that I specifically prepared for	09:44:27
11	testifying today.	09:44:33
12	But to answer your question, in various	09:44:36
13	process, whether it's fabricating a 3D NAND cell	09:44:42
14	or studying of certain dielectric, yes, we have	09:44:50
15	used many times -- "we" meaning my student under	09:44:58
16	my supervision -- have used many times so-called	09:45:04
17	chemical vapor deposition, CVD.	09:45:12
18	Q When you said that you fabricated a	09:45:16
19	memory cell for 3D NAND, do you mean a memory cell	09:45:21
20	string or just an individual memory cell?	09:45:29
21	A You know, I have 35 years of experience	09:45:39
22	as a faculty and as a researcher in the	09:45:44

1 Microelectronic Research Center at UT Austin, 09:45:49
2 University of Texas in Austin. I do not recall 09:45:55
3 every single fabrication experiment that we used, 09:46:01
4 that we have conducted. 09:46:10

5 But to answer your question, I believe 09:46:15
6 that we have, my student and I have fabricated 09:46:18
7 individual vertical 3D -- 3D NAND memory cell. 09:46:25
8 And I don't recall exactly whether we have 09:46:35
9 fabricate a string of 3D NAND devices. We might, 09:46:38
10 we might not have. I don't recall. 09:46:46

11 Q Have you and your students also 09:46:48
12 fabricated 2D NAND memory cells? 09:47:08

13 MR. HERMAN: Objection. Form. It's 09:47:15
14 outside the scope of direct. 09:47:16

15 A Can you point to where I -- where in my 09:47:27
16 reply declaration or original declaration that I 09:47:29
17 addressed this issue? 09:47:36

18 Q Do you need to review your reply 09:47:38
19 declaration in order to answer whether or not you 09:47:41
20 and your students have fabricated 2D memory cells? 09:47:42

21 MR. HERMAN: Objection. Form. 09:47:47

22 A I believe this is outside the scope of 09:47:49

1 the deposition today. But to answer your 09:47:54
2 question, the answer is yes. 09:48:00

3 Q Do you agree that conceptually the 09:48:02
4 difference between 2D NAND and 3D NAND is that 3D 09:48:23
5 NAND, rather than arranging memory cell in a 09:48:28
6 two-dimensional array, 3D NAND arranges cells in a 09:48:31
7 three-dimensional array? 09:48:36

8 MR. HERMAN: Objection to form. Also 09:48:38
9 outside the scope of direct. 09:48:39

10 A Yeah, I -- again, that is not something 09:48:46
11 specifically I prepared for my testimony today. 09:48:49

12 But to answer your question, a 2D NAND 09:48:56
13 is -- you can think of it as a planar NAND 09:49:02
14 devices. Memory cells arranges side by side on a 09:49:08
15 single semiconductor flat layer. So it's a 09:49:13
16 horizontal planar layout. 09:49:23

17 Whereas 3D NAND is a memory cell -- 3D 09:49:28
18 NAND is a memory devices that memory cells are 09:49:33
19 stacked vertically in multiple layer, creating a 09:49:43
20 3D structure. It's more like a skyscraper instead 09:49:49
21 of a parking lot. 09:50:00

22 So 3D NAND is a vertical stacked layer 09:50:08

1 structure, whereas 2D NAND is a horizontal planar 09:50:11
2 structure. 09:50:16

3 Q So conceptually would it be fair to say 09:50:19
4 that a 3D NAND structure could be conceived by 09:50:22
5 starting from the 2D strand building block and 09:50:25
6 then turning the 2D NAND string up side? 09:50:29

7 MR. HERMAN: Objection to form. It's 09:50:34
8 outside the scope of direct. 09:50:35

9 A In fact, I believe that that is something 09:50:42
10 I address in my first, my original declaration. 09:50:44
11 Yeah, conceptually you can think of it as turning 09:50:51
12 a horizontal planar structure by 90 degree and 09:50:56
13 make it a vertical stacked structure. 09:51:08

14 But that's very simplistic. And 09:51:11
15 obviously there are other changes, not just 09:51:19
16 turning the 2D NAND to a vertical configuration. 09:51:21

17 Q But both the 2D NAND and 3D NAND 09:51:31
18 structures would have a common source line. 09:51:34

19 Correct? 09:51:40

20 MR. HERMAN: Objection to form. It's 09:51:40
21 outside the scope of direct. 09:51:42

22 A Again, that is not something I prepare 09:51:48

1	for for my testimony today.	09:51:56
2	If there is some -- if that is something	09:52:07
3	that I addressed in my reply declaration or my	09:52:10
4	original declaration, I would -- I would like to,	09:52:15
5	if you can point out to me where I address it in	09:52:26
6	my declaration.	09:52:30
7	Q Are you unable to answer the question	09:52:38
8	without referring to your reply declaration?	09:52:41
9	A Again, my understanding is that today's	09:52:57
10	deposition focuses on my reply declaration. Your	09:53:02
11	question is outside the scope of today's	09:53:17
12	deposition.	09:53:21
13	To answer your question, yes, both 2D	09:53:22
14	NAND and 3D NAND architectures include a common	09:53:26
15	source line. But of course their fabrications and	09:53:32
16	the structure and the implementations are	09:53:37
17	different due to the layout of the memory cell.	09:53:42
18	Q Is the function of the common source line	09:53:50
19	the same in 2D NAND and 3D NAND architectures?	09:53:53
20	MR. HERMAN: Objection. Form. It's	09:53:57
21	outside the scope of direct.	09:53:58
22	A This is not something that I specifically	09:54:04

1	prepared for my testimony today. So your question	09:54:07
2	is that are the function the same, the function of	09:54:20
3	the common source line the same for 2D NAND and 3D	09:54:26
4	NAND.	09:54:29
5	Is that correct?	09:54:31
6	Q That's correct.	09:54:33
7	A So the common source line is basically a	09:54:39
8	shared source for multiple strings of memory	09:54:50
9	cells. So whether it is a 2D NAND or 3D NAND, the	09:55:00
10	function remain the same. But the implementations	09:55:06
11	and the structure are different for 3D NAND and 2D	09:55:13
12	NAND because of the layout are very different.	09:55:19
13	Does that make sense?	09:55:27
14	Q Yeah. So to get into that, what are the	09:55:29
15	structural differences of the common source line	09:55:39
16	in a 2D NAND versus a 3D NAND?	09:55:40
17	MR. HERMAN: Objection. Outside the	09:55:46
18	scope of direct.	09:55:47
19	A Okay. So again, this is not something	09:55:52
20	that I address in my reply declaration. And I	09:55:54
21	don't think I address that even in my original	09:56:00
22	declaration. But I will answer your question.	09:56:02

1 In the 2D NAND, a common source line is a 09:56:11
2 metal line that run horizontally because 2D NAND 09:56:14
3 is a horizontal. And the purpose, again, and the 09:56:20
4 function of the common source line is connect the 09:56:38
5 source terminal of the select transistors of the 09:56:42
6 memory cell in the string. 09:56:56

7 In a 3D NAND design, the common source 09:57:03
8 line is embedded through the memory string and 09:57:09
9 connected to the source end of the vertical memory 09:57:27
10 string across the array. 09:57:31

11 So the structure is quite different. One 09:57:41
12 is a horizontal metal routing layer in 2D NAND, 09:57:49
13 and the other one is a -- you can think of it as a 09:57:54
14 deep trench configuration structure. 09:58:01

15 So obviously there are a lot more details 09:58:13
16 than I just talk about, but overall that's the key 09:58:18
17 difference. One is a horizontal structure; the 09:58:24
18 other one is a 3D structure, a vertical structure. 09:58:28

19 Does that make sense? 09:58:40

20 Q That makes sense. 09:58:41

21 When you say that the common source line 09:58:53
22 in a 3D NAND is a deep trench structure, what do 09:58:55

1	you mean by that?	09:59:04
2	A Well, because 3D NAND is a vertical	09:59:17
3	structure, right; and the source line, the source	09:59:27
4	terminal, is usually at the bottom of the 3D NAND	09:59:36
5	string, and the common source line, as I	09:59:46
6	mentioned, is to provide a shaped source contact,	09:59:52
7	right, for all the vertical NAND string.	10:00:07
8	So in order to contact to the source	10:00:15
9	terminal at the bottom of these vertical string, a	10:00:24
10	deep trench is etched across the wafer and cut	10:00:34
11	through the vertical string and physically	10:00:40
12	intersect at the bottom portion of the vertical	10:00:53
13	channel pillars.	10:01:03
14	Because the source terminal is beneath	10:01:11
15	all these layers. And the reason why a deep	10:01:18
16	trench is used, because it is the most efficient	10:01:25
17	way of -- of contacting to the source -- to the	10:01:31
18	common source.	10:01:42
19	Q What do you mean that the deep trench is	10:01:49
20	etched across the wafer?	10:01:56
21	A Through the wafer. You can say through	10:02:00
22	the -- through the -- cut through the vertical	10:02:02

1 string, basically, that's what I mean, across the 10:02:06
2 wafer, through the wafer. 10:02:08

3 Q I'm a bit confused by what you mean by 10:02:13
4 "across the wafer" and "through the wafer." 10:02:16
5 Aren't those opposite? 10:02:18

6 A Yeah, I -- perhaps I should not have used 10:02:20
7 the word "across." A deep trench is cut through 10:02:26
8 the vertical string of the array. Because I'm 10:02:30
9 thinking that it's not just one deep trench, it's 10:02:44
10 many deep trench, right, for the -- for the -- to 10:02:49
11 contact various source terminal. 10:02:54

12 So what I mean is that it's not just one 10:03:00
13 deep trench form in the entire -- entire 3D NAND 10:03:03
14 chip. There are many common source line. And so, 10:03:11
15 therefore, the trench is -- is etched not just in 10:03:20
16 one location, but across the wafer. 10:03:32

17 Also, in general, common source line is 10:03:36
18 not like a pillar form; usually it's a -- you can 10:03:39
19 think of it as a vertical planar -- vertical -- 10:03:44
20 it's not like a columnar structure but, rather, 10:03:54
21 vertical plane you can think of it. 10:04:05

22 Q And so a common source line is typically 10:04:06

1	a vertical plane that cuts through the -- you said	10:04:15
2	the vertical string?	10:04:23
3	What's the vertical string?	10:04:31
4	A Vertical NAND string. Because the NAND	10:04:33
5	string is in a vertical configuration. So common	10:04:36
6	source line in the 3D NAND is basically	10:04:43
7	implemented using a deep trench that cut	10:04:48
8	through -- cut across the array. Meaning that it	10:04:58
9	is not just a vertical pillar, but a -- you can	10:05:01
10	think of it as a plane -- a vertical plane. And	10:05:04
11	is go all the way to the base of the vertical NAND	10:05:19
12	string. And, of course, if it is a common source	10:05:29
13	line, which means that it is filled with a	10:05:35
14	conductive material.	10:05:39
15	Q So if it goes through the vertical NAND	10:05:46
16	string, does it go through the memory cells or	10:05:49
17	just through the word lines?	10:05:57
18	A No, the word lines are insulated with	10:06:04
19	insulators. And, no, it doesn't go through the	10:06:07
20	memory cell.	10:06:13
21	Q I guess where I'm getting confused is	10:06:16
22	what the NAND string is. Because my understanding	10:06:20

1	is that the NAND string were the actual memory	10:06:24
2	cells.	10:06:28
3	A No. It's -- I'm talking about, like, the	10:06:29
4	NAND structure when you have word line, insulating	10:06:37
5	line, word line, insulating line, and so on and so	10:06:41
6	forth.	10:06:45
7	And so the common source line basically	10:06:47
8	cut through all those NAND structures that	10:06:50
9	consists of, you know, 128 layers of word lines	10:07:00
10	and insulating.	10:07:09
11	Q I get it. So the common source line is a	10:07:15
12	vertical planar structure that is a deep trench	10:07:18
13	through the alternating stack of word lines and	10:07:22
14	insulating line -- and insulating layers between	10:07:26
15	them. Correct?	10:07:29
16	MR. HERMAN: Objection. Form. Also	10:07:30
17	outside the scope of direct.	10:07:34
18	A You can say that. I'm not sure -- yeah,	10:07:39
19	it's -- it's cutting through layers of word lines	10:07:42
20	and insulating layer that separating the word	10:07:46
21	lines.	10:07:52
22	Q And you said it's typically not just a	10:07:52

1	pillar that goes through but a vertical plane?	10:07:54
2	A Yeah. If you, for example, if you show	10:08:03
3	me the '623 patent, it shows the top view of the	10:08:11
4	common source line.	10:08:24
5	MR. CROSS: We've been going for about an	10:08:29
6	hour. Would you like a five-minute break?	10:08:30
7	THE WITNESS: Sure.	10:08:36
8	MR. CROSS: Okay.	10:08:37
9	VIDEO SPECIALIST: We are going off the	10:08:38
10	record at 10:08.	10:08:39
11	(A recess was taken.)	10:08:40
12	VIDEO SPECIALIST: We are back on the	10:14:21
13	record at 10:14.	10:14:27
14	BY MR. CROSS:	10:14:30
15	Q Dr. Lee, before we took a break we talked	10:14:33
16	a little bit about the fabrication of 3D NAND	10:14:40
17	structures and your experience using	10:14:44
18	photolithography and chemical vapor deposition in	10:14:47
19	fabricating memory cells for 3D NAND.	10:14:50
20	Do you recall that?	10:14:53
21	A (No response.)	10:15:13
22	Q Dr. Lee, just confirming you can hear me?	10:15:14

1	Hello?	10:15:19
2	MR. HERMAN: I can hear you.	10:15:24
3	Are you there, Dr. Lee?	10:15:26
4	THE WITNESS: Hello?	10:15:32
5	Q Hi, Dr. Lee. Can you hear me?	10:15:35
6	A Hello?	10:15:40
7	MR. HERMAN: We can hear you, Dr. Lee.	10:15:41
8	But maybe your volume is low.	10:15:43
9	A Okay. Yeah. Yeah. Yeah. I got it now.	10:15:46
10	Sorry about that.	10:15:48
11	Q You can hear me now?	10:15:51
12	A Yes. I actually put it on -- yeah. My	10:15:52
13	volume was very low, so ...	10:15:58
14	Q Okay.	10:16:00
15	A Thank you, sir.	10:16:01
16	Q So do you recall before we took a break	10:16:02
17	we talked a little bit about your experience	10:16:06
18	fabricating 3D NAND memory cells and using	10:16:08
19	photolithography and chemical vapor deposition?	10:16:12
20	A Yeah. Though I believe that that's not	10:16:16
21	the focus of my deposition today.	10:16:20
22	Q For the process of developing the	10:16:26

1	photoresist and exposing the photoresist, is that	10:16:29
2	done in the chemical vapor deposition chamber?	10:16:34
3	MR. HERMAN: Objection. Form. It's	10:16:39
4	outside the scope of direct.	10:16:41
5	A Not only that is outside of chemical	10:16:52
6	vapor deposition chamber, it is in a completely	10:16:58
7	different room or so-called different bay of the	10:17:03
8	clean room.	10:17:09
9	The photoresist is sensitive to lights	10:17:12
10	that are -- has UV component. So therefore, it	10:17:20
11	has to -- all the process related to photoresist,	10:17:23
12	including exposure, development, and -- and so on,	10:17:27
13	all done in a room, so-called yellow light room,	10:17:38
14	which does not have UV light component. Whereas	10:17:42
15	the CVD process is done in a different bay, which	10:17:48
16	the light might have contained a UV component.	10:17:58
17	Q You mentioned imaging of a mask through a	10:18:01
18	mask during the photolithography process.	10:18:18
19	Can you explain what you meant by that?	10:18:25
20	A Oh, can you repeat the question, please?	10:18:36
21	Q You mentioned that during the photoresist	10:18:38
22	process you image a mask through a mask.	10:18:42

1	Is that what you meant to say?	10:19:00
2	A I am not sure if I understand your	10:19:04
3	question.	10:19:05
4	So when you -- when I say that imaging	10:19:08
5	through a photo mask, it's basically a concept	10:19:11
6	related to photolithography. As I mentioned	10:19:21
7	before, photolithography is where the pattern is	10:19:27
8	transferred onto the semiconductor wafer using UV	10:19:31
9	light.	10:19:39
10	So a photo mask, you can think of it as a	10:19:42
11	very high-resolution, high-precision stencil.	10:19:47
12	It's usually on a glass or quartz plate and coated	10:19:56
13	with chrome, usually. And a UV light is projected	10:20:08
14	through the photomask, right, onto the wafer that	10:20:24
15	has been coated with photoresist.	10:20:29
16	A photoresist, once again, is called	10:20:34
17	photoresist because it is sensitive to UV light.	10:20:37
18	So the transparent regions of the photomask, which	10:20:47
19	is not coated with chrome, will let the light	10:20:52
20	through; while the nontransparent, the opaque	10:20:58
21	region coated with chrome, which contain the	10:21:04
22	circuit pattern, that opaque region will block the	10:21:16

1	UV light.	10:21:21
2	So therefore, what's happening in the	10:21:25
3	mask, the image on the mask will form an optical	10:21:32
4	image onto the photoresist. Now, in general in	10:21:43
5	the modern photolithography tool, like what you	10:21:56
6	call the stepper, the lens system is such that	10:22:00
7	it's focused and reduce the mask to the size of	10:22:06
8	the mask image, the image of the size and focus	10:22:12
9	and reduce a pattern by, say, ten to one or five	10:22:18
10	to one, depending on the particular machine.	10:22:24
11	Then after that you would develop the	10:22:33
12	photoresist so that for a positive photoresist the	10:22:44
13	exposed region will wash away. For negative	10:22:51
14	photoresist the unexposed region will wash away.	10:22:57
15	And, therefore, the pattern that is laid out on	10:23:02
16	the mask will transfer to the wafer precisely and	10:23:13
17	with high resolution layer by layer in	10:23:30
18	semiconductor manufacturing.	10:23:36
19	Again, this is just a very rough	10:23:42
20	explanations of what is a photomask and how is	10:23:51
21	that implemented in a photolithography process.	10:24:00
22	Does that make sense?	10:24:06

1	Q	That makes sense.	10:24:08
2		And is alignment critical during the	10:24:13
3		photolithography process?	10:24:16
4	A	Of course it is.	10:24:18
5		MR. HERMAN: Objection. Form. Outside	10:24:19
6		the scope --	10:24:21
7		THE WITNESS: I apologize, Patrick.	10:24:22
8	A	Your question is whether alignment is	10:24:27
9		critical.	10:24:32
10	Q	During the photolithography process.	10:24:35
11		MR. HERMAN: Objection. Form. Also	10:24:37
12		outside the scope of direct.	10:24:40
13		MR. CROSS: Just to clean up the question	10:24:42
14		and answer that --	10:24:44
15	Q	Is alignment critical during the	10:24:49
16		photolithography process?	10:24:53
17		MR. HERMAN: Same objections.	10:24:54
18	A	Again, my understanding is that the	10:24:58
19		testimony today, the deposition today, focuses on	10:25:02
20		my reply declaration. That is not something that	10:25:06
21		I address in my reply declaration nor my original	10:25:11
22		declaration. And it's not something that I	10:25:18

1 specifically prepared for my testimony today. 10:25:23

2 But to answer your question, yes, 10:25:33

3 alignment is absolutely critical in photoresist -- 10:25:36

4 in photolithography process. Because in a modern 10:25:44

5 IC processing it's not just one mask; it's dozens 10:25:56

6 and sometimes even hundreds of layers. And each 10:26:03

7 layer require a photoresist -- photomask. 10:26:08

8 So the mask that you try to use to 10:26:18

9 project the image onto the photoresist of the 10:26:28

10 wafer must be precisely aligned with the existent 10:26:33

11 features from the previous layer. 10:26:44

12 Any misalignment can cause a short, 10:26:47

13 electric short, can cause an electric opening, and 10:26:53

14 essentially an incorrect image placement, 10:27:07

15 incorrect feature placement. And which can 10:27:12

16 basically ruin the entire chip. 10:27:18

17 So yes, alignment is extremely critical. 10:27:23

18 Q Is alignment critical during the chemical 10:27:28

19 vapor deposition steps? 10:27:36

20 MR. HERMAN: Objection. Form. It's 10:27:42

21 outside the scope of direct. 10:27:43

22 A So, once again, all these questions are 10:27:47

1 not described in my reply declaration, and I don't 10:27:52
2 think I address it in my original declaration, 10:27:58
3 neither. And that's not something that I prepared 10:28:03
4 for to testify today. 10:28:07

5 And your question is whether alignment is 10:28:14
6 critical in CVD, chemical vapor -- chemical vapor 10:28:18
7 deposition process. Is that correct? 10:28:23

8 Q That's correct. 10:28:27

9 A A chemical vapor deposition is -- is a 10:28:31
10 process in which it -- you deposit a thin film 10:28:40
11 solid material by injecting a gaseous precursors. 10:28:55
12 And this chemical gas will react at the surface or 10:29:18
13 decompose onto the wafer. And there are various 10:29:28
14 different kind of chemical vapor deposition, but 10:29:30
15 that has nothing to do with alignment. 10:29:32

16 Q Sorry, to clarify, is your answer that 10:29:46
17 alignment is not critical during the chemical 10:29:48
18 vapor deposition process? 10:29:51

19 MR. HERMAN: Objection. Form. Also 10:29:53
20 outside the scope of direct. 10:29:54

21 A I'm not sure if I understand your 10:29:57
22 question. 10:29:59

1	Q	Sorry. You said that it has nothing to	10:30:02
2		do with alignment. Does that mean that alignment	10:30:04
3		is not critical during the CVD process?	10:30:07
4	A	A CVD process is -- CVD process is a	10:30:11
5		process that chemical gas react at the surface of	10:30:20
6		the wafer to form a film, whether it is a silicon	10:30:35
7		film or silicon dioxide film, through chemical	10:30:47
8		reaction.	10:30:53
9		So, no, alignment is not critical in the	10:30:57
10		CVD itself, because CVD is a blanket deposition	10:31:04
11		process, not a patterning steps. And CVD is a	10:31:09
12		process that coated the entire wafer uniformly in	10:31:20
13		general. And so it does not rely on a mask or	10:31:27
14		specific alignment, and is a blanket depositions	10:31:43
15		of material, such as oxide, nitride, polysilicon	10:31:51
16		metal across the entire surface of the wafer.	10:31:58
17		Alignment is critical after the CVD	10:32:08
18		process, when, you know -- when you need to have a	10:32:14
19		precision alignment to ensure a correct circuit	10:32:24
20		fabrication. But the alignment is not critical in	10:32:31
21		a CVD process itself. There's no alignment in CVD	10:32:43
22		process. It's a blanket deposition process.	10:32:52

1	Does that make sense?	10:32:55
2	Q So --	10:32:56
3	A A patterning step --	10:32:59
4	Q To clarify, if I wanted to put down an	10:33:02
5	alternating layer of dielectrics or alternating	10:33:06
6	layers of deposition, you wouldn't have to align	10:33:10
7	those different layers. Right?	10:33:12
8	If I have one layer then another layer	10:33:14
9	then another layer, they don't have to be aligned.	10:33:16
10	MR. HERMAN: Objection. Form.	10:33:21
11	A Again, these questions are outside the	10:33:26
12	scope of this deposition. And my understanding is	10:33:32
13	that the testimony today is focused on the reply	10:33:37
14	declarations. And if that is something that I	10:33:40
15	specifically address in my reply declaration, can	10:33:50
16	you point that where I said in my reply	10:33:54
17	declaration -- forget that. I know it's not in	10:33:58
18	that.	10:34:04
19	So if all you're interested is have a	10:34:06
20	blanket depositions of oxide, conductive layer,	10:34:12
21	oxide, conductive layer, and so on and so forth,	10:34:18
22	yeah, a CVD process can achieve that. And again,	10:34:24

1 it is not a patterning step. 10:34:29

2 Q So you can deposit using CVD in multiple 10:34:33
3 players without worrying about alignment; you can 10:34:44
4 just do one after the other? 10:34:47

5 MR. HERMAN: Objection. Form. 10:34:52

6 A I'm not sure your question -- what your 10:34:54
7 question directly related to. Okay? Because it's 10:35:01
8 phrased so general and it might -- depending on 10:35:10
9 the context you're referring to. 10:35:16

10 But if all you -- all you are looking for 10:35:18
11 is a blanket deposition of an insulating layer, a 10:35:20
12 conductive layer, and blanket deposition of 10:35:28
13 another layer of insulating, another layer of 10:35:32
14 conductive layer, yes, a CVD process and other 10:35:34
15 deposition process can be used for blanket 10:35:40
16 deposition purposes. 10:35:46

17 CVD, chemical vapor deposition or 10:35:51
18 other -- other deposition process such as PVD, 10:35:56
19 physical vapor deposition, can be used to achieve 10:36:00
20 blanket deposition. They are not a patterning 10:36:09
21 step. 10:36:10

22 Q Could you deposit those layers of 10:36:14

1	insulating layers and conductive layers in the	10:36:19
2	same deposition chamber?	10:36:28
3	A What do you mean by that?	10:36:42
4	First of all, once again, I'm going to	10:36:49
5	repeat it again, this is not what I'm come here	10:36:50
6	today. My understanding is that the testimony	10:36:58
7	today is focused on my reply declaration.	10:37:01
8	So, can you clarify your question,	10:37:11
9	please? What do you mean by "in the same	10:37:14
10	chamber"? Does that mean the same -- because	10:37:17
11	depending on the configuration of the system, one	10:37:21
12	can say, Yeah, you can deposit insulating layer	10:37:33
13	and conductive layer in the same chamber or a	10:37:41
14	cluster of chamber.	10:37:45
15	Is that what you mean by clustering,	10:37:49
16	cluster, or is it a single chamber?	10:37:52
17	Q So you mentioned during photolithography	10:37:56
18	you have to take the wafer to a different room in	10:38:11
19	order to perform photolithography.	10:38:16
20	Do you have to take the wafer to a	10:38:21
21	different room to deposit different materials?	10:38:22
22	MR. HERMAN: Objection. Form.	10:38:26

1 A Again, that's not the focus of my 10:38:33
2 testimony today. The focus is on my reply 10:38:34
3 declaration. 10:38:38

4 Q Okay. 10:38:41

5 A But the answer is, it depends. It 10:38:42
6 depends on where the -- where the CVD depositions 10:38:45
7 for the insulating layer, where the CVD deposition 10:38:51
8 in the conductive layer. If they are in the same 10:39:00
9 room, no, you don't have to -- you don't have to 10:39:03
10 take it out to move to another room. 10:39:06

11 In fact, it is possible to deposit both 10:39:10
12 the insulating layer and conductive layer in the 10:39:13
13 same chamber, but obviously not at the same time. 10:39:16
14 They are done sequentially. And usually that 10:39:19
15 is -- you have to be very careful because you 10:39:31
16 don't want to -- you want to make sure that 10:39:34
17 there's no cross-contamination. The precursor got 10:39:36
18 to be compatible in order to do it in the same 10:39:43
19 chamber. 10:39:45

20 So in general, that's what I mean by what 10:39:46
21 you -- that's what I -- why I want you to clarify 10:39:51
22 your question. There's something called a cluster 10:39:54

1 tool, which means that you have a vacuum 10:39:58
2 environment with multiple subchamber. 10:40:02

3 One chamber is used for conductive layer, 10:40:09
4 another chamber for insulating layer, another 10:40:14
5 layer is for a different material, and so on and 10:40:17
6 so forth. Okay? 10:40:20

7 So to answer your question that you can 10:40:26
8 deposit insulating layer and conductive layer in 10:40:28
9 the same chamber, obviously not simultaneously. 10:40:33
10 And the best way to do it is use a cluster tool. 10:40:39

11 Q So to deposit multiple layers using CVD, 10:40:46
12 you could do so without ever leaving the vacuum of 10:40:51
13 the chemical vapor deposition tool. 10:40:55

14 Is that fair? 10:40:57

15 MR. HERMAN: Objection. Form. Also 10:40:58
16 outside the scope of direct. 10:41:01

17 A Again, my understanding is today's 10:41:03
18 testimony is focused on my reply declaration. I 10:41:07
19 don't think I address that in my reply 10:41:12
20 declaration, nor my original declaration. 10:41:16

21 And, yes, if you use, for example, a 10:41:21
22 cluster tool, you can deposit both insulating 10:41:25

1 layer and conductive layer without breaking 10:41:32
2 vacuum. But again, it required very careful -- 10:41:40
3 very careful process control to avoid 10:41:53
4 cross-contamination particles and many other 10:41:57
5 issues. 10:42:04

6 Let me make sure that my answer to your 10:42:17
7 questions, all these process-related questions, 10:42:20
8 are very general, a rough overview of the process. 10:42:29
9 A lot of details might have been -- I'm sure that 10:42:39
10 is -- is not there and should not be taken out of 10:42:46
11 context. 10:42:52

12 MR. CROSS: I'm going to upload a 10:43:14
13 previously marked exhibit to the chat. And it's 10:43:21
14 marked as Exhibit 2001. 10:43:29

15 (Exhibit 2001, previously marked, not 10:43:31
16 attached.) 10:43:33

17 Q So if you could open that up, please. 10:43:33

18 If you could let me know when you have it 10:44:02
19 open. 10:44:03

20 A It won't open. One second. Let me see. 10:44:14
21 How do I open that? One second. I'm sorry. I'm 10:44:19
22 having trouble. 10:44:34

1	Okay.	10:44:56
2	Q Do you recognize this document, Dr. Lee?	10:44:57
3	A Yes. I believe this is the document that	10:45:04
4	Dr. Kuhn cited in his -- in her declaration, if I	10:45:19
5	recall correctly.	10:45:25
6	Can you -- if it is possible, can you	10:45:25
7	upload her declaration so that I can make sure	10:45:32
8	that's the case, and my reply declaration?	10:45:35
9	Q Well, if you could just please read off	10:45:47
10	the title of the document.	10:45:51
11	Is this document directed towards NAND	10:46:06
12	flash memory?	10:46:08
13	A I believe so.	10:46:10
14	Q If you go to Page 5. It should read at	10:46:23
15	the bottom of the document, Page 5.	10:46:38
16	A Where are you looking at?	10:46:44
17	Q In bold on the bottom of the page it	10:46:45
18	should say, Page 5. There are Bates numbers, or	10:46:48
19	Bates stamp.	10:46:55
20	A Which section are you looking for? Can	10:46:57
21	you read that for me?	10:46:58
22	Q Sorry, are you ability to get to Page 5	10:46:59

1	and you're just waiting for me to direct you to	10:47:06
2	the language?	10:47:08
3	A I'm here on Page 5. Page 5. It's a lot	10:47:13
4	of information. Which recollection are you	10:47:18
5	referring to and can you read that for me, that	10:47:19
6	section that you are interested in?	10:47:22
7	Q Yeah. So the last paragraph on the left	10:47:24
8	column. It mentions common source lines.	10:47:29
9	Correct?	10:47:33
10	A There is a word called "common source	10:48:12
11	line." I'm not sure what -- yeah, that's	10:48:16
12	mentioned that. Is that what you mean?	10:48:24
13	Q Yeah. So you agree that this NAND flash	10:48:26
14	memory includes common source lines?	10:48:35
15	Dr. Lee, are you --	10:49:06
16	A I'm trying to read it. It's been a while	10:49:07
17	that I read this. Would you mind letting me read	10:49:10
18	it a little bit?	10:49:12
19	Q Yeah. Just let me know when you're done	10:49:13
20	reading.	10:49:16
21	A Because I don't want to read it out	10:49:20
22	of ...	10:49:22

1	Okay. So hold on. Sorry. So this	10:49:51
2	document specifically on Page 5 discusses the	10:51:52
3	difference -- the differences in noise behavior	10:52:02
4	between the --	10:52:09
5	Q Dr. Lee, all I asked was whether or not	10:52:10
6	this NAND structure has a common source line.	10:52:12
7	Can you answer that?	10:52:14
8	MR. HERMAN: Objection. Form.	10:52:17
9	A Hold on, let me see.	10:52:34
10	Well, it discuss about common source	10:52:36
11	line. Your -- what is your question?	10:52:39
12	Q Does this NAND structure have a common	10:52:42
13	source line?	10:52:47
14	A I have to read it. It's been a while	10:53:21
15	that I read this. Hold on one second. I'm trying	10:53:26
16	to search for ...	10:54:00
17	Yes, it does. The NAND structure	10:54:17
18	discussed in this document does have a common	10:54:20
19	source line.	10:54:23
20	Q Great. Thank you. You can close that.	10:54:25
21	A Okay.	10:54:38
22	MR. CROSS: I will upload to chat a	10:54:40

1	document previously marked as Exhibit 2002.	10:54:43
2	(Exhibit 2002, previously marked, not	10:54:46
3	attached.)	10:54:48
4	Q You can let me know when that's open.	10:54:48
5	A Okay.	10:55:18
6	Q Do you recognize this document?	10:55:18
7	A Not exactly.	10:55:34
8	Q Well, this document is titled	10:55:35
9	Applications of AFM in Semiconductor R&D and	10:55:38
10	Manufacturing At 45 Nanometer Technology Node and	10:55:45
11	Beyond.	10:55:48
12	Is that right?	10:55:49
13	A That's what it says, yes.	10:55:50
14	Q Do you see in the middle of the abstract	10:55:50
15	it says, "AFM continues to provide reliable	10:55:54
16	information for development and control of	10:56:02
17	processes in memory"?	10:56:03
18	A Right. In the abstract itself?	10:56:07
19	Q Yeah, in the abstract itself, about seven	10:56:09
20	lines down it says, and I quote, AFM continues to	10:56:16
21	provide reliable information for development and	10:56:20
22	control of processes in memory, end quote.	10:56:22

1	Do you agree?	10:56:30
2	A That's what it says, yes.	10:56:32
3	Q Turn to Page 6 of the document.	10:56:33
4	A Sorry. Page what?	10:56:47
5	Q Yeah. If you look at the Bates numbers	10:56:49
6	at the bottom, it should read IPR2024-00794, Page	10:56:51
7	6.	10:56:56
8	A Okay.	10:57:05
9	Q Do you see Section 3.3, labeled Common	10:57:05
10	Source Lines?	10:57:09
11	A 3.3, yes.	10:57:17
12	Q Do you see the label for the Figure 9?	10:57:19
13	Is that directed towards the schematic diagram of	10:57:29
14	a NAND string of flash memory device?	10:57:33
15	A Are you looking at the figure or ...	10:57:42
16	Q Yeah. I'm just asking, is that Figure A	10:57:46
17	a schematic diagram of a NAND string flash memory	10:57:50
18	device?	10:57:53
19	A Figure A? Figure 9A?	10:57:56
20	Q Yes.	10:57:59
21	A Yes, it's a schematic diagram of a NAND	10:58:03
22	string of a flash memory device.	10:58:06

1	Q	And does this NAND memory device have a	10:58:08
2		common source line?	10:58:19
3	A	Yes.	10:58:27
4	Q	Well, you can close that. And if we go	10:58:28
5		to --	10:58:47
6		MR. CROSS: I'm sorry, I'll upload a	10:58:48
7		document previously marked as Exhibit 2003.	10:58:50
8		(Exhibit 2003, previously marked, not	10:58:53
9		attached.)	10:58:57
10	Q	If you can let me know when that's	10:58:57
11		loaded.	10:59:00
12	A	Okay.	10:59:16
13	Q	Do you recognize this document?	10:59:16
14	A	Yes.	10:59:27
15	Q	Can you read the title, please.	10:59:27
16	A	A High Speed Low Power Negative Sensing	10:59:36
17		Architecture For 3D NAND Flash Memory.	10:59:40
18	Q	So this document is directed towards 3D	10:59:43
19		flash memory. Correct?	10:59:48
20	A	I believe so.	10:59:51
21	Q	And in the Introduction, can you read out	10:59:51
22		loud the last paragraph of the Introduction?	10:59:57

1	A	The last -- oh, paragraph.	11:00:05
2	Q	The last paragraph of the introduction.	11:00:09
3		If you could read that, please.	11:00:11
4	A	Okay. If you don't mind, you can read it	11:00:12
5		better than me.	11:00:15
6	Q	Sure. Do you agree it reads, "In this	11:00:17
7		paper, a novel negative sensing architecture (NSA)	11:00:21
8		is proposed which is suitable for 3D NAND Flash	11:00:25
9		memory based on TCAD simulation. And our proposed	11:00:29
10		SA shows better performance on read noise, read	11:00:36
11		speed, and power consumption"?	11:00:41
12	A	Yes.	11:00:47
13	Q	So do you agree that this document is	11:00:48
14		directed towards the structure and operation of 3D	11:00:51
15		NAND flash memory?	11:00:58
16		MR. HERMAN: Objection. Form.	11:01:00
17	A	I'm not sure if that's -- is the focus of	11:01:06
18		this, all it talk about. But the -- can you	11:01:13
19		repeat the question?	11:01:34
20	Q	Sure. Do you agree that this paper is at	11:01:35
21		least directed in part to 3D NAND flash	11:01:39
22		architecture and operation?	11:01:43

1	A	Well, it's directed to a 3D NAND memory.	11:01:57
2		And as you read, the last paragraph of the	11:02:08
3		introduction is related to high-speed, low-power	11:02:11
4		sensing architecture.	11:02:22
5	Q	So that would include the operation of 3D	11:02:29
6		NAND memory?	11:02:41
7	A	Well, the operation of 3D NAND is a very	11:02:56
8		general term. This is focusing on the certain	11:02:58
9		aspect of the 3D NAND operation, focusing on the	11:03:04
10		negative sensing architecture.	11:03:11
11	Q	Does this document discuss the read	11:03:16
12		operation of 3D NAND memory?	11:03:19
13	A	Where do you see that?	11:03:33
14	Q	In the paragraph that I read.	11:03:34
15	A	It talk about the speed of the read --	11:03:46
16		the read speed, yeah.	11:03:54
17	Q	Would you agree that this document talks	11:03:58
18		in part about 3D NAND operations, including the	11:04:00
19		read operation?	11:04:03
20	A	Yeah, the document does discuss --	11:04:07
21		appears to be discuss the read operation of the 3D	11:04:12
22		NAND flash memory.	11:04:15

1 Q Do you agree that this document talks 11:04:20
2 about the 3D NAND flash memory architecture? 11:04:22

3 A When you talk about "3D NAND 11:04:32
4 architecture," that's a very general term. The 11:04:34
5 paper focus on a specific aspect of the 3D NAND 11:04:38
6 architecture; namely, the sensing architecture. 11:04:42

7 Q Do you know what it means by "the sensing 11:04:49
8 architecture"? 11:04:51

9 A Well, sensing architecture is a -- 11:04:58
10 related to the read operation. Is that what you 11:05:06
11 mean? Is that what you mean by the -- by your 11:05:15
12 question? 11:05:20

13 Q I was just asking if you understood what 11:05:21
14 the document means by "sensing architecture." 11:05:23

15 A Well, a sensing architecture -- I have 11:05:26
16 not read this document for quite some time. But 11:05:34
17 in general, a sensing architecture is related to a 11:05:41
18 certain design to sense or to detect the stored 11:05:47
19 data in the memory cell during the read operation. 11:05:58

20 Q Do you know if this 3D NAND memory 11:06:29
21 architecture includes a common source line? 11:06:41

22 A Can you point out where it include that? 11:06:47

1	Yeah?	11:06:56
2	Q Sure. Can you turn to Page 2?	11:06:57
3	A Page 2.	11:07:00
4	Q Yeah. If you look at Figure 5 on Page 2.	11:07:04
5	Can you read the caption for Figure 5?	11:07:08
6	A Yeah, you go ahead and read it, if you	11:07:15
7	can.	11:07:17
8	Q Sure. Do you agree that it reads "Figure	11:07:17
9	5: The parasitic resistance model of common	11:07:19
10	source line CSL and wire."	11:07:23
11	A Yes.	11:07:32
12	Q And that common source line is depicted	11:07:32
13	in the figure. Correct?	11:07:35
14	A CSL, yes.	11:07:36
15	Q And that's part of the 3D NAND structure.	11:07:37
16	Correct?	11:07:40
17	A Yes.	11:07:46
18	Q So you'd agree that this 3D NAND memory	11:07:46
19	device includes a common source line. Correct?	11:07:50
20	A Yes. It's about -- it does include the	11:07:57
21	common source line, but that's not the focus. The	11:08:06
22	focus is more on the sensing architecture.	11:08:09

1	Q	And if you read the language directly	11:08:15
2		beneath the caption of Figure 5, is that directed	11:08:17
3		towards the parasitic capacitance of a common	11:08:20
4		source line?	11:08:24
5	A	Would you mind read that?	11:08:28
6	Q	Sure. It reads, "We simulate a model of	11:08:29
7		2,048 strings and SAs as shown in Figure 5. All	11:08:34
8		the SLs of the string are connected to the CSL.	11:08:41
9		The CSL and the wire to pump which generates 2	11:08:46
10		volt have" parasitic capacitance -- strike that.	11:08:52
11		It says, "parasitic resistance. The parasitic	11:08:55
12		resistance becomes larger with the page	11:09:00
13		increasing. In our simulation, we assume the	11:09:03
14		total parasitic resistance is 38.6 ohms, 1024, of	11:09:04
15		our string models have low-threshold voltage	11:09:10
16		cells, and other 1024 string models have	11:09:14
17		high-threshold voltage cells?	11:09:20
18		Did I read that correctly?	11:09:22
19	A	I believe so.	11:09:23
20	Q	Is this document directed towards the	11:09:24
21		parasitic resistance in a common source line of a	11:09:30
22		3D NAND memory device?	11:09:35

1 A Well, it is -- the focus of this document 11:10:02
2 is related to the sensing architecture of -- of 11:10:05
3 the 3D NAND. So in this -- I don't want to take 11:10:17
4 it out of context. 11:10:44

5 So your question is that whether it 11:10:48
6 discussed a parasitic resistance of the common 11:10:55
7 source line. Yeah, it seems to that. Yes, from 11:10:59
8 this paragraph it seems to discuss that the 11:11:11
9 document discuss the parasitic resistance of the 11:11:16
10 common source line. 11:11:21

11 Yeah, I think I -- to answer your 11:11:34
12 question, the answer is that yeah, it does discuss 11:11:36
13 parasitic resistance of the common source line. 11:11:43

14 Q Can you describe what parasitic 11:11:50
15 resistance is? 11:11:51

16 A Well, parasitic, the word "parasitic," 11:11:55
17 means unwanted. Right? It in general refer to 11:12:01
18 unintended or unavoidable resistance. In a 11:12:17
19 electrical component, electrical interconnects, or 11:12:25
20 electrical material, is unintended and unavoidable 11:12:40
21 resistance that are not deliberately designed to 11:12:50
22 have such resistance. 11:13:04

1 So parasitic resistance can occur in 11:13:10
2 metal lines, contacts, semiconductor material. 11:13:15
3 Again, parasitic means unwanted, because it can 11:13:21
4 degrade the performance of the chip by causing -- 11:13:27
5 you know, if you have resistance, then you have 11:13:38
6 voltage drop along the line, you can reduce the 11:13:41
7 signal speed. Because any parasitic resistance 11:13:49
8 will add to the so-called the RC time constant. 11:13:54
9 Any unwanted resistance can increase the 11:14:01
10 heating and the power consumption, and all kinds 11:14:05
11 of issues. The timing might be -- might be out 11:14:10
12 of -- out of match, and mismatched, and so on and 11:14:15
13 so forth. 11:14:18
14 Q You mentioned RC time constant. 11:14:19
15 Can you explain what that is? 11:14:22
16 A Well, when you have a circuit, it is 11:14:31
17 basically -- RC time constant is basically a time 11:14:38
18 related to resistance times the capacitance in 11:14:43
19 series. It basically describe how quickly a 11:14:52
20 circuit charge or discharge through a series 11:15:00
21 combination or parallel combination of the 11:15:15
22 resistance and capacitance. 11:15:16

1	So that's -- in general sense, that's	11:15:22
2	what it is. It is important because in circuits,	11:15:25
3	including memory -- memory circuits, you want to	11:15:32
4	minimize so-called the RC time constant in order	11:15:35
5	to achieve high-speed operation.	11:15:39
6	Q Could we go to the last page.	11:15:57
7	Can you read the last sentence of the	11:16:04
8	conclusion? Or if you'd like I can read it.	11:16:06
9	A Sure. Why don't you read that.	11:16:11
10	Q Do you read that SA stands for sensing	11:16:13
11	amplifier?	11:16:18
12	A No.	11:16:19
13	Q Okay. Let's turn back to Page 1.	11:16:20
14	A I don't know it's -- sorry. Yeah.	11:16:28
15	Sensing architecture. Yeah, sensing amplifier in	11:16:30
16	the abstract, you're right.	11:16:33
17	Q Okay. So sensing amplifier, or, sorry,	11:16:34
18	sense amplifier for SA, and source line for SL.	11:16:38
19	Correct? Sorry, to rephrase.	11:16:43
20	Do you agree that SL stands for source	11:16:50
21	line and that SA stands for sense amplifier?	11:16:53
22	A Where do you see the SL in that	11:16:57

1	Conclusion?	11:17:00
2	Q No. Sorry. It's in the abstract.	11:17:01
3	A I thought you talked -- were asking me	11:17:06
4	about the conclusion. Now you're asking me --	11:17:10
5	Q I just wanted to confirm that we have the	11:17:15
6	same understanding of what these terms mean	11:17:17
7	because I have used SL in the past in reading some	11:17:20
8	language.	11:17:23
9	So just for clarity, if we turn to the	11:17:23
10	abstract, do you agree that SL stands for source	11:17:26
11	line and that SA stands for sense amplifier?	11:17:29
12	A I believe that that's what the abstract	11:17:37
13	stated.	11:17:40
14	Q All right. And then turning back to the	11:17:41
15	conclusion on Page 3. Do you agree that it reads,	11:17:46
16	"The SA we designed has advantages including lower	11:17:48
17	noise," 9.5 percent -- or "9.4 percent faster read	11:17:52
18	speed, and 51.6 percent lower power consumption	11:17:57
19	compared to the conventional counterpart referred	11:18:03
20	in Reference 5"?	11:18:06
21	A Yes.	11:18:09
22	Q So you mentioned that parasitic	11:18:09

1	capacitance affects signal speed or read speed?	11:18:17
2	A In general, RC time constant delay the	11:18:27
3	speed of the signal transitioned.	11:18:35
4	Q And that would affect the read speed?	11:18:38
5	A Well, in general, RC time constant affect	11:19:05
6	the signal power performance. And if it is a read	11:19:09
7	separation, yeah, it's -- this RC time constant is	11:19:24
8	high. If the parasitic resistance is high, then,	11:19:29
9	yes, it would also affect the read speed.	11:19:39
10	Q And would the parasitic resistance affect	11:19:41
11	the power consumption?	11:19:45
12	A I think I meant that I told you before	11:19:58
13	the parasitic resistance degrade the performance.	11:20:02
14	One of the problem -- one of the causes is heating	11:20:08
15	and increased power consumption.	11:20:14
16	Q Did you deal with this issue when	11:20:17
17	fabricating memory cell devices?	11:20:29
18	A I'm not sure what you mean by "this	11:20:35
19	issue."	11:20:36
20	Q This issue of parasitic capacitance and	11:20:37
21	resistance.	11:20:42
22	A Our team look at various aspect of the	11:20:45

1	device that we fabricated, including parasitic	11:20:49
2	resistance and parasitic capacitance.	11:20:56
3	MR. CROSS: We've been going for a little	11:21:03
4	over an hour. Would you like to take a -- we can	11:21:04
5	take a five-minute break, or if you want longer?	11:21:10
6	THE WITNESS: Sure.	11:21:14
7	VIDEO SPECIALIST: We are going off the	11:21:17
8	record at 11:21.	11:21:18
9	(A recess was taken.)	11:21:20
10	VIDEO SPECIALIST: We are back on the	11:30:30
11	record at 11:30.	11:30:32
12	BY MR. CROSS:	11:30:40
13	Q Dr. Lee, I am going to upload to chat an	11:30:42
14	exhibit previously marked as Exhibit 1003.	11:30:45
15	(Exhibit 1003, previously marked, not	11:30:49
16	attached.)	11:31:09
17	Q If you can let me know when that's	11:31:09
18	uploaded.	11:31:12
19	Dr. Lee, just to confirm, you're pulling	11:31:38
20	up Exhibit 1003. Right?	11:31:40
21	A Yes.	11:31:43
22	Q Okay. Let me know when it's up.	11:31:44

1	A	It's up.	11:31:50
2	Q	Great. Do you recognize this document,	11:31:51
3		Dr. Lee?	11:31:56
4	A	Yeah. I believe this is my opening	11:31:59
5		declaration, or the original declaration for this	11:32:07
6		IPR.	11:32:10
7	Q	If you can turn to Page 88 of your	11:32:11
8		declaration.	11:32:30
9	A	So my understanding is that this	11:32:39
10		declaration -- this deposition focuses on my reply	11:32:47
11		declaration, not my original declaration. And	11:32:49
12		that is something that I have not specifically	11:33:00
13		prepared to testify today.	11:33:06
14	Q	In your reply declaration, did you	11:33:12
15		discuss the Park reference?	11:33:14
16	A	Can you upload the -- my reply	11:33:22
17		declaration and tell me where I said so?	11:33:24
18	Q	Do you not recall whether or not your	11:33:31
19		reply declaration covered the Park reference?	11:33:34
20	A	My understanding is that this is not a	11:33:42
21		memory test. So if you can upload my reply	11:33:43
22		declaration, I would really appreciate it.	11:33:49

1	Q	Before I do that, based on just your	11:33:55
2		recollection of the reply declaration that you	11:34:02
3		reviewed yesterday, do you remember whether or not	11:34:06
4		it covered discussions about the Park reference?	11:34:09
5	A	It is my understanding that you are	11:34:18
6		refusing to upload my reply declaration?	11:34:19
7	Q	To answer this question, yes.	11:34:24
8	A	What was the question again?	11:34:36
9	Q	Do you recall whether or not your rely	11:34:37
10		declaration covers discussions of the Park	11:34:40
11		reference?	11:34:42
12	A	Yes, I do. In my reply declaration, yes,	11:34:48
13		I indeed discuss Park reference.	11:34:57
14	Q	In your Park declaration -- sorry.	11:35:01
15		Strike that.	11:35:07
16		In your reply declaration do you discuss	11:35:08
17		petitioner's grounds?	11:35:14
18	A	Can you repeat that question again?	11:35:20
19	Q	Sure. In your reply declaration do you	11:35:22
20		discuss petitioner's grounds, which are based on	11:35:24
21		the Park reference?	11:35:27
22	A	Yes, we -- I discuss the argument related	11:35:35

1	to the Park prior art references.	11:35:43
2	Is that what you mean by ground?	11:35:51
3	Q Yeah, the grounds of invalidity that	11:35:53
4	petitioner set forth in its petition.	11:35:58
5	So turning back to your first	11:36:07
6	declaration, do you recognize this figure on Page	11:36:11
7	88?	11:36:15
8	A Do you mean in 3, Figure 3?	11:36:26
9	Q Yeah. Figure 3. Do you recognize that	11:36:30
10	annotated figure from your declaration?	11:36:35
11	A Yes. That's the figure from the Park	11:36:58
12	reference. But -- yeah, from the Park reference,	11:37:10
13	annotated.	11:37:19
14	Q Is it also modified?	11:37:22
15	A Can you upload the Park reference,	11:37:29
16	please?	11:37:37
17	MR. CROSS: Okay, I've uploaded a	11:37:46
18	document previously marked as Exhibit 1004, which	11:37:48
19	is U.S. Patent Number 10,559,583, also referred to	11:37:55
20	as Park.	11:38:02
21	(Exhibit 1004, previously marked, not	11:38:04
22	attached.)	11:38:19

1	Q	And once you have that open, you can go	11:38:19
2		to PDF Page 5.	11:38:21
3	A	Okay. In Figure 3?	11:38:22
4	Q	So comparing Figure 3 from the Park	11:38:37
5		reference to Figure 3 in your declaration, did you	11:38:40
6		modify this figure?	11:38:45
7	A	Yes.	11:38:54
8	Q	How did you modify it?	11:38:54
9	A	So as explained in my declaration, my	11:39:03
10		first declaration, which is not the focus of	11:39:11
11		today's deposition, if you look at Figure -- I	11:39:14
12		mean Paragraph 305, I said that, "Now, as adopted,	11:39:25
13		Park includes longer dielectric trenches (the	11:39:40
14		lengthened isolation insulation regions 111 shown	11:39:49
15		in orange above) that span the length of its	11:39:55
16		device to completely and by themselves separate	11:40:01
17		its BSG (the ground select line) into sub-BSGs	11:40:05
18		(portions associated with units -- unit areas UA1,	11:40:13
19		capital U, capital A-1, to UA8."	11:40:18
20		So that's the modification.	11:40:26
21	Q	Do you agree that there are only three	11:40:37
22		common source regions in this figure?	11:40:39

1	A	Again, my understanding is today's	11:40:58
2		deposition focuses on my reply declaration, not on	11:40:59
3		my original declaration.	11:41:05
4		But to answer your question, as shown in	11:41:10
5		this Figure 3 on Page 88, that common source line,	11:41:14
6		also called common source region, is highlight in	11:41:23
7		purple color, and there are three common source	11:41:27
8		lines or common source regions.	11:41:34
9	Q	Do you agree that between the middle	11:41:43
10		common source region and the top common source	11:41:54
11		region, there are three dielectric trenches?	11:41:56
12	A	Yes.	11:41:59
13	Q	Do you agree that between the first	11:42:00
14		dielectric trench and the second dielectric trench	11:42:05
15		there are no common source lines?	11:42:07
16	A	What do you mean by "the first"?	11:42:11
17	Q	Sorry. Do you agree that between the top	11:42:14
18		dielectric trench and the middle dielectric trench	11:42:19
19		there, there are no common source regions?	11:42:24
20	A	The middle? What do you mean by middle?	11:42:29
21		The middle between the top two common source line?	11:42:32
22	Q	Yeah. But to clarify, we can just say,	11:42:36

1	do you see that there are three common -- sorry.	11:42:40
2	Strike that.	11:42:43
3	Do you see that there are three	11:42:44
4	dielectric trenches between the top common source	11:42:46
5	region and the middle common source region?	11:42:52
6	A Yes.	11:42:55
7	Q Of those three dielectric trenches, do	11:42:55
8	you see that there are no common source regions	11:42:59
9	between the top dielectric trench and the middle	11:43:01
10	dielectric trench. Correct?	11:43:04
11	A Yes.	11:43:08
12	Q Do you agree that there are no common	11:43:08
13	source regions between the middle dielectric	11:43:11
14	trench and the bottom dielectric trench of the	11:43:16
15	previously mentioned three dielectric trenches?	11:43:19
16	A Yes.	11:43:21
17	Q By lengthening the isolation insulation	11:43:22
18	Regions 111, did you remove common source regions?	11:43:55
19	A Are you say -- are you asking whether	11:44:31
20	are -- when you say "removed," remove from where?	11:44:45
21	Q If you look at Figure 3 of Park, were	11:44:50
22	there more common source regions?	11:44:57

1	A	What are you referring to?	11:45:07
2	Q	So looking at Figure 3 of Park, what is	11:45:08
3		your understanding of the elements labeled 103 and	11:45:17
4		104?	11:45:20
5	A	Those are common source line.	11:45:21
6	Q	Okay. Is that different than what you	11:45:23
7		were referring to as common source region?	11:45:27
8	A	They're the same.	11:45:30
9	Q	In your adapted Figure 3 on Page 88 of	11:45:31
10		your declaration, did you remove Elements 103 and	11:45:39
11		104 from Park's Figure 3?	11:45:43
12	A	Yes. I replaced 103 and 104 with	11:45:50
13		dielectric trench.	11:45:54
14	Q	When you replaced the common source	11:45:57
15		regions or the common source lines 103 and 104	11:46:01
16		with the dielectric trench, did it increase the	11:46:04
17		capacity of the memory device?	11:46:09
18	A	So, first of all, the focus of my	11:46:55
19		deposition today is not on my original	11:47:08
20		declaration; it's focused on my reply	11:47:19
21		declarations --	11:47:24
22	Q	I can stop you right there.	11:47:24

1	MR. HERMAN: Counsel, allow the witness	11:47:27
2	to answer his question. Wait your turn, and then	11:47:29
3	ask your question. No more interrupting, please.	11:47:31
4	A So I think it is -- I have to read my	11:47:45
5	declaration again to see whether I address the	11:48:01
6	issues of whether it has increased or not.	11:48:10
7	But in general, removing the common	11:48:32
8	source line and adopted the dielectric trench, as	11:48:47
9	discussed in Shibata, can be used to increase the	11:49:02
10	memory capacitors by reducing the layout area	11:49:12
11	consumption, and enable denser array density.	11:49:21
12	So again, the focus of my today	11:49:32
13	deposition is on reply declaration but not on my	11:49:44
14	original declaration. But you can see that	11:49:51
15	Paragraph 303 explained that a common source line	11:49:56
16	consumed the horizontal layout area.	11:50:04
17	Paragraph 304 and 305 describe how the	11:50:13
18	dielectric trench that use in Shibata, how that	11:50:26
19	allowed the -- how that can eliminate the need for	11:50:37
20	large shared common source line.	11:50:47
21	And then Paragraph 306 argue -- discusses	11:51:01
22	that removing CSL would free up, right, the	11:51:11

1 routing area. So more memory, right? When the 11:51:22
2 model is freed up, we see that that can allow 11:51:40
3 higher array density. 11:51:43
4 So that's a -- it's a design trade-off. 11:51:45
5 Right? That you sacrifice CSL, common source 11:51:51
6 line, and boost the capacity of the memory cells. 11:52:07
7 And so the figure are not drawn to scale, 11:52:17
8 obviously. So the common source line usually 11:52:26
9 occupy a much larger area. 11:52:33
10 So to answer your question, yes, removing 11:52:43
11 CSL, the common source line, increase the memory 11:52:49
12 capacity. 11:52:54
13 Q Okay. Turning back to Figure -- your 11:52:58
14 adapted Figure 3. Park uses a gate-last 11:53:10
15 replacement. Correct? 11:53:25
16 A Yes. 11:53:35
17 Q And gate-last replacement process 11:53:36
18 requires a common source region trenches in order 11:53:44
19 to remove the sacrificial layers before depositing 11:53:46
20 the word line layers. Correct? 11:53:50
21 A I -- can you repeat that again? So 11:54:12
22 the -- you're saying that the gate-last process in 11:54:18

1	the -- Park?	11:54:26
2	Is that right?	11:54:34
3	Q I am referring to the gate-last process	11:54:36
4	in Park.	11:54:40
5	A Can you point to where I mention --	11:54:47
6	discuss that?	11:54:50
7	Q Are you familiar with the term "gate-last	11:54:50
8	replacement process"?	11:55:25
9	A Yes.	11:55:26
10	Q Can you explain what the gate-last	11:55:26
11	replacement process is?	11:55:30
12	A Let me show you. In fact, I describe	11:55:44
13	that in Paragraph -- hold on one second.	11:55:58
14	Q I'm seeing it in --	11:56:04
15	A Ah.	11:56:05
16	Q I'm looking at Paragraph 159 and maybe	11:56:07
17	the ones before that.	11:56:12
18	A 159. Hold on. Let me get there.	11:56:23
19	Because gate-last process normally	11:56:26
20	happened in 3D NAND, but also in semiconductors	11:56:28
21	that -- in Paragraph -- you said one fifty --	11:56:39
22	Q Nine.	11:56:47

1	A	Perhaps a better paragraph might be in	11:57:14
2		Paragraph 176.	11:57:16
3	Q	Sure.	11:57:27
4	A	If you don't mind reading that.	11:57:29
5	Q	Sure. Paragraph 176 reads, Moreover,	11:57:34
6		quote, in some embodiments (i.e., Gate-last	11:57:45
7		Formation Technology, end quote, the BSG, word	11:57:49
8		lines, and other layers can be, quote, formed	11:57:54
9		firstly using sacrificial layers, end quote, that	11:57:57
10		are only replaced with conductive material after	11:58:00
11		all other processing steps, including the trench	11:58:03
12		formation -- are completed.	11:58:06
13		Citing Exhibit 1001 at various locations,	11:58:13
14		explaining that the BSG in which the trench	11:58:16
15		openings are formed can be sacrificial layers.	11:58:19
16	A	Right. So that's essentially what	11:58:24
17		gate-last process is, is what is described here.	11:58:27
18		And the previous paragraph describes -- also	11:58:39
19		describe how essentially make use of the gate-last	11:58:41
20		process. That the trench -- the trenches can be	11:58:50
21		formed by forming trench openings through a	11:58:53
22		desired layers, and then filling these trench	11:58:59

1 opening with a dielectric material. That is 11:59:04
2 essentially a gate-last process. 11:59:09

3 Again, gate-last process is not only used 11:59:14
4 in 3D NAND but also in CMOS fabrications. 11:59:19

5 Q Do you agree that the replacement process 11:59:27
6 is conducted through the common source regions; 11:59:33
7 that is, the etchant material and then the 11:59:39
8 subsequent word line material is introduced 11:59:46
9 through the common source regions? 11:59:49

10 A So your question is does the gate-last 11:59:57
11 process -- is the gate-last process used in the 11:59:59
12 common source line of Park? Is that what you're 12:00:08
13 asking? 12:00:16

14 Q I think the other way around. Isn't the 12:00:21
15 common source region, where the common source line 12:00:24
16 eventually is formed, isn't that region used to 12:00:28
17 introduce the etchant material and the word line 12:00:35
18 material? 12:00:43

19 A I'm not sure if I understand your 12:00:43
20 question. 12:00:45

21 Q How does -- 12:00:47

22 A How does the word line come into play? 12:00:48

1	The common source line in Park is also formed	12:00:51
2	using gate-last process, that it is formed -- the	12:00:56
3	common source line I believe is formed early in	12:01:05
4	the process, where you etch a deep trench and then	12:01:07
5	eventually filled it with conductive materials.	12:01:15
6	Q So before you fill it with conductive	12:01:20
7	material, is it your understanding that the gate	12:01:23
8	lines are formed by removing the sacrificial	12:01:30
9	material through the common source regions using	12:01:33
10	etchant?	12:01:39
11	A Wait a minute. I thought the -- the CSL	12:01:53
12	would form before the word lines or the gate in	12:02:16
13	actual were fabricated. Where do you read that?	12:02:22
14	Q So if you turn back to the Park reference	12:02:28
15	that's Exhibit 1004?	12:03:05
16	A You know ...	12:03:07
17	Q Sorry, did you say something?	12:03:25
18	A Yeah. This is the first declaration.	12:03:28
19	And the focus of today's deposition is on my reply	12:03:50
20	declaration. So I'm not sure why you keep asking	12:03:53
21	question related to my original declaration.	12:03:59
22	Because those were -- have been deposited early, is	12:04:06

1	that this year or late last year.	12:04:13
2	So to answer your question, I'm going to	12:04:22
3	have to read it again, because the original	12:04:23
4	declaration is not supposed to be in this	12:04:32
5	deposition. It's not something that I	12:04:34
6	specifically prepared for.	12:04:37
7	Q Is that the end of your answer? I don't	12:04:41
8	want to interrupt.	12:04:45
9	A Your question is that whether --	12:05:02
10	Q I asked you to turn to the Park	12:05:06
11	reference.	12:05:07
12	A Okay. Park reference. Okay. Where?	12:05:08
13	Q Okay. Column 15, Line 35 through 37.	12:05:10
14	A Column what? Fifteen?	12:05:26
15	Q Uh-huh.	12:05:27
16	A Column 15, Line 35 to ...	12:05:37
17	Sorry. You said 35?	12:05:49
18	Q Line 35 to 37.	12:05:59
19	A Okay. Okay.	12:06:07
20	Q Do you know what the word line cuts WC1	12:06:24
21	and WC2 are? And if you'd like, you can turn to	12:06:31
22	Figure 30.	12:06:47

1	A	Figure 30.	12:06:57
2	Q	Do you know what the WC1 and WC2 are?	12:07:21
3	A	I think WC1 is so-called I believe word	12:07:25
4		line cut, cut across the gate in actual area. And	12:07:30
5		WC2 is a second word line cut.	12:08:03
6	Q	So does this refresh your recollection of	12:08:14
7		how the gate replacement process uses the trenches	12:08:16
8		formed during the common source line formation as	12:08:21
9		an avenue to introduce the etchant material to	12:08:28
10		remove the sacrificial layers and introduce the	12:08:32
11		gate material?	12:08:36
12	A	Yeah, I mean, the gate-last process, is	12:09:12
13		that what you mean?	12:09:17
14	Q	Does the gate-last process use these	12:09:18
15		trenches in introducing the etchant material and	12:09:21
16		gate material? And by "these trenches" I mean WC1	12:09:29
17		and WC2.	12:09:38
18	A	So are you saying that the -- does WC1	12:09:44
19		and WC2 make use of the gate-last process?	12:09:47
20	Q	No. I'm saying does the gate-last	12:09:53
21		process use WC1 and WC2 in order to form the gates	12:09:56
22		in the 3D NAND structure?	12:10:05

1	A	Does the gate-last process apply to WC1	12:10:12
2		and WC2 in order to form the what? In order to	12:10:17
3		form the gate electrode?	12:10:32
4	Q	Do you agree that in the gate-last	12:10:34
5		process sacrificial layers are used?	12:10:36
6	A	Yes.	12:10:38
7	Q	How are those sacrificial layers removed?	12:10:39
8	A	Well, as shown in Figure 31, it is used	12:10:46
9		by etching.	12:11:04
10	Q	How does the etching get to the	12:11:08
11		sacrificial layers?	12:11:10
12	A	Well, etching is -- depending on what	12:11:18
13		kind of etching you use can easily diffuse through	12:11:26
14		the layer and etch through the layer. And Park,	12:11:35
15		the example, the example that Park uses make use	12:11:55
16		of the phosphoric acid etching. But that just an	12:12:07
17		example and is not limiting.	12:12:18
18	Q	In Column 15, Lines 35 through 37, does	12:12:29
19		it say that the etching solution is flowing	12:12:36
20		through the first and second word line cuts, WC1	12:12:38
21		and WC2?	12:12:41
22	A	Can you repeat that? Can you go to --	12:12:45

1	what column is this?	12:12:47
2	Q In Column 15, Lines 35 through 37, does	12:12:48
3	Park say that the etching solution is flowing	12:12:55
4	through the first and second word line cuts, WC1	12:12:58
5	and WC2?	12:13:02
6	A Yeah, the sacrificial layer SL may be	12:13:23
7	removed by etching solution flowing through the	12:13:25
8	first and second WC1, WC2 -- first and second word	12:13:28
9	line cut WC1, WC2.	12:13:34
10	Q So do you agree that the etching solution	12:13:40
11	is introduced through WC1 and WC2 during the	12:13:41
12	gate-replacement process?	12:13:50
13	A During the gate-last process.	12:14:09
14	Q Do you see a difference between	12:14:11
15	gate-replacement process and gate-last process?	12:14:15
16	A It is basically the same.	12:14:17
17	Q Okay.	12:14:19
18	A So your question is that does the etching	12:14:22
19	solution flow through the first and second word	12:14:25
20	line cuts, WC1 and WC2, in the gate-last process	12:14:28
21	or the gate-replacement process. The answer is	12:14:40
22	yes.	12:14:43

1	Q	In your modified figure on Page 88 of	12:14:44
2		your first declaration --	12:14:50
3	A	Okay. Hold on. Let me get back there	12:14:53
4		again. Sorry. Page 88. Yeah.	12:14:56
5	Q	Through what avenue is the etchant	12:15:08
6		introduced into this figure? Or strike that.	12:15:13
7		On Page 88, Figure 3, your adapted Park	12:15:19
8		figure, through what avenue would the etchant	12:15:25
9		material be introduced in order to perform the	12:15:29
10		gate-replacement process?	12:15:33
11	A	"Through what avenue"?	12:15:58
12		What do you mean by that?	12:15:59
13	Q	Where does the etchant material flow from	12:16:01
14		in your figure during the gate-replacement	12:16:14
15		process?	12:16:18
16	A	Well, you submerge the entire chip	12:16:26
17		into -- into a phosphoric acid. And it go through	12:16:30
18		any opening that -- in the -- in the layout. So	12:16:35
19		I'm not sure if I understand your question, that	12:16:51
20		etching can go through various parts -- various	12:16:55
21		regions, various region. For example, go through	12:17:02
22		the common source region during the sacrificial	12:17:07

1	layer -- I mean, in the -- when the sacrificial	12:17:12
2	layer is removed. And so, you know, that is a lot	12:17:15
3	of etching going through there.	12:17:26
4	And furthermore ...	12:17:29
5	Q Sorry, did you have more to say?	12:17:51
6	A Hold on one second. Sorry.	12:17:53
7	Furthermore, on Figure 17 Park also	12:18:28
8	explain that they can use the open regions, right,	12:18:36
9	209 or 209A can also be used to allow the flow of	12:18:46
10	the phosphoric acid. And so if you see in Figure	12:19:05
11	17 that the -- the material, the 209, right, or	12:19:15
12	better yet 211, the trenches which are now longer	12:19:44
13	than before are now staggered to each other.	12:19:54
14	Because you don't need to worry about the flow of	12:19:59
15	phosphoric acid.	12:20:03
16	So to answer your question, the flow of	12:20:07
17	the etchant is -- is going through various	12:20:11
18	regions, and including as shown in Figure 17.	12:20:26
19	Q In your adapted Figure 3 on Page 88,	12:20:32
20	where is 209?	12:20:43
21	MR. HERMAN: Objection. Form. Outside	12:20:47
22	the scope of direct.	12:20:49

1	A	So in Figure 3, the modified Figure 3,	12:21:03
2		does not describe the 209A. But what I'm saying	12:21:15
3		is that Park teaches using an open area, such as	12:21:21
4		209, right, to allow the flow of phosphoric acid.	12:21:34
5		And therefore the -- this method would allow the	12:21:53
6		formation of trenches that are longer.	12:22:06
7		And as you notice in Figure 17, the	12:22:14
8		trenches are not -- doesn't have to be staggered,	12:22:18
9		don't have to be staggered as in the previous	12:22:22
10		figure.	12:22:28
11	Q	What do you mean, "the previous figure"?	12:22:29
12	A	As in Figure 3 of -- of Park.	12:22:35
13	Q	Are Figure 3 and Figure 17 the same	12:22:51
14		device?	12:22:57
15		MR. HERMAN: Objection. Form.	12:22:58
16	A	It can be. It can make use of the 209A,	12:23:03
17		the open region so-called, in order to improve the	12:23:21
18		etching capability.	12:23:30
19	Q	So if you can turn to Column 4, Lines 59	12:23:38
20		through 60?	12:24:02
21	A	Column 4, Line 50 to 60?	12:24:02
22	Q	Fifty-nine to 60.	12:24:17

1 Do you agree that it reads that Figure 3 12:24:27
2 is a schematic plan view of a memory device 100? 12:24:29

3 A It says that Figure 3 is a schematic plan 12:24:36
4 view of a memory device 100 according to an 12:24:39
5 example of the present inventive concept. In 12:24:48
6 other words, that this is simply an example, that 12:24:56
7 it's not meant to be limiting. 12:25:00

8 Q Okay. So what's your understanding of 12:25:06
9 the difference between an example and an 12:25:07
10 embodiment? 12:25:09

11 MR. HERMAN: Objection. Form. Outside 12:25:13
12 the scope of direct. 12:25:17

13 A I'm not a lawyer. Perhaps you can tell 12:25:24
14 me. 12:25:31

15 My understanding is that the example, for 12:25:38
16 example -- for example. Sorry. That example is 12:25:45
17 basically an illustration to demonstrate certain 12:25:55
18 aspect of an embodiment. And in general it is not 12:26:13
19 limiting. 12:26:22

20 For example, in this case phosphoric acid 12:26:24
21 may be used to remove the sacrificial layer, 12:26:29
22 that's an example. 12:26:33

1	An embodiment, I don't know how to	12:26:38
2	describe that, is basically a version of the	12:26:40
3	invention, an implementation of the invention, or	12:26:50
4	specific implementation of the -- of the invention	12:27:05
5	I believe.	12:27:12
6	So typically it describe the features and	12:27:16
7	the methods and the configurations. And it	12:27:29
8	describe how the inventions is practiced, or can	12:27:41
9	be practiced.	12:27:49
10	Q Okay.	12:27:51
11	A Again, you're the -- you're the lawyers.	12:27:53
12	But I believe that that's the gist of the	12:27:59
13	difference between example and embodiment. Yeah.	12:28:02
14	Q In your view does Park disclose any	12:28:10
15	embodiments?	12:28:13
16	MR. HERMAN: Objection. Form. It's	12:28:15
17	outside the scope of direct.	12:28:18
18	A I know for sure that they disclose --	12:28:34
19	Park disclose -- discloses many -- some examples.	12:28:44
20	Let's see. Hold on. Can I -- I have to read	12:28:56
21	through the -- this is 1004. Right? Exhibit	12:28:58
22	1004. I'm search -- sorry, I am trying to search	12:29:15

1	the word embodiment in Park. Unless my search is	12:29:47
2	not functioning well, I don't see -- hold on one	12:30:04
3	second.	12:30:13
4	I search the word embodiment, it doesn't	12:30:38
5	seem to appear unless I -- unless the searching is	12:30:40
6	not functioning well.	12:30:52
7	Do you see any?	12:31:04
8	Q My question is not whether or not the	12:31:06
9	word appears. I am asking whether or not Park	12:31:08
10	discloses any embodiments?	12:31:10
11	A Well, that's why I'm trying to see if I	12:31:11
12	can search for the word embodiment.	12:31:13
13	Q No. I did a keyword search as well. I	12:31:18
14	didn't see any reference to an embodiment.	12:31:21
15	A Yeah, I mean, there is a lot of examples.	12:31:25
16	If you search the word example, there's a lot of	12:31:29
17	examples. But there's no -- it doesn't seem to	12:31:32
18	disclose any embodiments.	12:31:36
19	Q So it doesn't have any embodiments?	12:31:41
20	MR. HERMAN: Objection.	12:31:44
21	A I don't know.	12:31:44
22	MR. HERMAN: Objection. Form. Also	12:31:45

1	outside the scope of direct.	12:31:47
2	A Yeah, I mean, this is not the focus of my	12:31:48
3	testimony today. And I have not considered this	12:31:53
4	questions, whether -- whether Park disclose	12:32:07
5	embodiments or not. And it's not something I	12:32:11
6	specifically prepared to testify today.	12:32:16
7	So to answer your question, you and I	12:32:25
8	searched the word "embodiment" in the document,	12:32:30
9	and we don't see -- we couldn't find any. So does	12:32:34
10	that mean there is no embodiment? It appears to	12:32:40
11	be that there's no embodiment.	12:32:43
12	Q If you can turn to Paragraph 207 on Page	12:32:48
13	63 of your declaration?	12:32:51
14	A My original declaration?	12:32:53
15	Q Uh-huh.	12:32:59
16	A Hold on. Paragraph 207?	12:33:05
17	Q Uh-huh.	12:33:17
18	A Yes.	12:33:44
19	Q In your original declaration, did you	12:33:45
20	think that Park had embodiments?	12:33:49
21	MR. HERMAN: Objection. Form. Also	12:33:52
22	outside the scope of direct. And mischaracterizes	12:33:53

1	the witness's testimony.	12:33:55
2	Q Sure. I'll rephrase.	12:34:09
3	In Paragraph 207 of your first	12:34:11
4	declaration, do you refer to Park's embodiments,	12:34:12
5	including that shown in Figures 3, 4, and 11?	12:34:14
6	A That's the word I use. I might have	12:34:43
7	incorrectly used the word "embodiments." Perhaps	12:34:46
8	it should be "examples."	12:34:49
9	And again, that the figures in Park are	12:34:54
10	just examples, and they're not limiting. And if I	12:35:15
11	misused the word in my original declaration,	12:35:26
12	instead of examples as in for example. In the	12:35:35
13	Paragraph 207, perhaps I should say in some of	12:35:42
14	Park's examples. Because when we searched the	12:35:47
15	word "embodiment," there is no embodiment, the	12:35:54
16	word "embodiment." So yeah.	12:35:58
17	Q So turning to Paragraph 212, do you also	12:36:08
18	refer to Park's embodiments that include string	12:36:11
19	select line layers GL14 and GL15?	12:36:29
20	A 212?	12:36:40
21	Q Yeah.	12:36:41
22	A Again, that now that we tried to search	12:36:43

1	the word "embodiments" in Park and we don't see	12:36:44
2	any, perhaps in my declaration I should have said	12:36:46
3	Park also explain that in this example string	12:36:53
4	select line layers GL14 and GL15. But a person of	12:37:01
5	ordinary skill in the art, reading Park, would	12:37:10
6	understand that these are merely examples, and not	12:37:17
7	intend to be -- intended to be limiting.	12:37:22
8	Q And in Paragraph 13 do you refer to other	12:37:25
9	embodiments in Park?	12:37:28
10	A Paragraph 13?	12:37:36
11	Q I'll restate it.	12:37:38
12	In Paragraph 213 do you refer to Park's	12:37:43
13	other embodiments?	12:37:45
14	A Yeah, I -- again, that it appears at this	12:37:51
15	point that Park does not disclose any embodiments.	12:37:55
16	And perhaps I should have used the word "example"	12:38:04
17	instead of "embodiments."	12:38:11
18	And again, a person of ordinary skill in	12:38:21
19	the art would understand, looking at Park, that	12:38:22
20	those are all merely examples, and not intended to	12:38:29
21	be limiting.	12:38:33
22	Q Okay. If you can go back to Park, Column	12:38:35

1	12, Line 39 through 42. Let me restate that.	12:38:53
2	If you can turn to Park, Column 12, Line	12:39:12
3	41 through 42. Does that read, In the memory	12:39:15
4	device 200A according to the example illustrated	12:39:22
5	in Figure 17, vertical insulating layers 209A may	12:39:26
6	be spaced from first and second common source	12:39:33
7	lines 202 and 205?	12:39:38
8	A Yes.	12:39:40
9	MR. CROSS: All right. If we can take a	12:39:52
10	ten-minute break?	12:39:53
11	THE WITNESS: Sure.	12:39:54
12	VIDEO SPECIALIST: We are going off the	12:39:56
13	record at 12:39.	12:39:57
14	(A recess was taken.)	12:39:59
15	VIDEO SPECIALIST: We are back on the	12:49:13
16	record at 12:49. Thank you, Counsel.	12:49:16
17	MR. CROSS: And, Dr. Lee, I'm uploading	12:49:20
18	to the chat exhibit -- or a document previously	12:49:23
19	marked as Exhibit 1025.	12:49:26
20	(Exhibit 1025, previously marked, not	12:49:29
21	attached.)	12:49:36
22	BY MR. CROSS:	12:49:36

1	Q	Once you've opened it, can you let me	12:49:36
2		know?	12:49:38
3	A	Okay.	12:49:38
4	Q	If you can turn to Page 4 of your	12:50:05
5		declaration?	12:50:27
6	A	Yes.	12:50:34
7	Q	You have a section entitled Park, Claims	12:50:34
8		2 and 3?	12:50:39
9	A	Yes.	12:50:40
10	Q	You're referring to the same Park that	12:50:40
11		we've been reviewing today?	12:50:42
12	A	Yes.	12:50:43
13	Q	If you turn to Page 14 of your	12:50:43
14		declaration.	12:51:04
15	A	Okay.	12:51:10
16	Q	You have a section entitled Application	12:51:10
17		of Shibata to Park.	12:51:12
18		Is that correct?	12:51:15
19	A	Yes.	12:51:16
20	Q	And that's referring to modifications of	12:51:16
21		Park based on teachings from Shibata?	12:51:22
22		Is that correct?	12:51:25

1	A	Yes.	12:51:26
2	Q	And in this section if you turn to Page	12:51:29
3	17.		12:51:32
4	A	Yes.	12:51:38
5	Q	You refer to a Figure 17 of Park.	12:51:38
6		Is that correct?	12:51:40
7	A	Yes.	12:51:41
8	Q	And that's the same figure we've been	12:51:41
9	discussing today?		12:51:43
10	A	Yes.	12:51:44
11	Q	And if you turn to the next page.	12:51:44
12	A	Yes.	12:51:48
13	Q	Actually, if you can turn to Page 19.	12:51:48
14	A	Yes.	12:51:55
15	Q	This is a modification of Park's Figure	12:51:58
16	3. Correct?		12:52:00
17	A	Yes.	12:52:01
18	Q	Can you turn to Page 20.	12:52:01
19	A	Yes.	12:52:38
20	Q	Paragraph 51 refers to common source	12:52:38
21	regions. Correct?		12:52:45
22	A	It's about the documents that's cited by	12:52:54

1	Dr. Kuhn related to common source region.	12:52:57
2	Q And specifically in that paragraph you	12:53:01
3	refer to --	12:53:07
4	A Can you hold on one second? My cat is	12:53:08
5	making a lot of noise, so I need to put it --	12:53:12
6	sorry about that. Hold on one second.	12:53:14
7	Q Not a problem.	12:53:18
8	A I apologize.	12:55:25
9	Q That's fine. Not a problem.	12:55:26
10	Let's see. Turning to Paragraph 51.	12:55:30
11	A Yes.	12:55:35
12	Q You provide a summary for Exhibit 2001,	12:55:36
13	Exhibit 2002, and Exhibit 2003. Correct?	12:55:46
14	A Yes.	12:55:50
15	Q And those are the same three documents we	12:55:50
16	reviewed today?	12:55:52
17	A Yes.	12:55:53
18	Q And if you go to Page 23 of your	12:55:53
19	declaration?	12:56:01
20	A Yes.	12:56:01
21	Q In Paragraph 58 you discuss the	12:56:01
22	manufacturing steps, including deposition steps.	12:56:16

1	Correct?	12:56:19
2	A Specifically about the deposition steps	12:56:25
3	for the Shibata of the depositions select gate	12:56:33
4	layer and the associated insulating layers. And	12:56:48
5	that manufacturing of these structure would take	12:57:04
6	at least six steps.	12:57:07
7	Q And in Paragraph 60 you start talking	12:57:13
8	about additional steps of forming a mask.	12:57:16
9	Correct?	12:57:21
10	A Yes, Paragraph 60 says that Additionally,	12:57:25
11	as Dr. Kuhn notes, Employing Park requires two	12:57:29
12	additional steps: Forming a mask and then forming	12:57:35
13	slits by etching would be required.	12:57:42
14	However, I explain in Paragraph 62	12:57:49
15	actually that would reduce the manufacturing steps	12:58:01
16	from six steps to four steps.	12:58:04
17	Q And one of those steps would be the mask	12:58:05
18	step. Correct?	12:58:09
19	A One of the four steps is a mask and an	12:58:12
20	etch. One of the four steps is mask, and one of	12:58:19
21	the four steps is etching.	12:58:26
22	Q Okay. And what do you mean by mask?	12:58:33

1 A Well, remember we discussed what is a 12:58:41
2 photomask in the process of photolithography, 12:58:44
3 that's what I mean by mask. 12:58:50

4 MR. CROSS: All right. Well, thank you, 12:58:55
5 Dr. Lee. I have no further questions. 12:58:59

6 THE WITNESS: Thank you. 12:59:02

7 MR. HERMAN: I don't have any questions 12:59:03
8 either. So with that, Dr. Lee, I think we are 12:59:04
9 done for the day. 12:59:06

10 THE WITNESS: Thank you. 12:59:07

11 VIDEO SPECIALIST: This ends the 12:59:09
12 deposition of Dr. Jack Lee. We are going off the 12:59:10
13 record at 12:59 p.m. eastern time. 12:59:12

14 (Off the record at 12:59 p.m. EDT.)

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ACKNOWLEDGMENT OF DEPONENT

I, JACK C. LEE, Ph.D., do hereby
acknowledge that I have read and examined the
foregoing testimony, and the same is a true,
correct and complete transcription of the
testimony given by me, and any corrections appear
on the attached Errata sheet signed by me.

(DATE)

(SIGNATURE)

C E R T I F I C A T E

I, Debra Ann Whitehead, E-Notary Public in and for
the Commonwealth of Virginia, do hereby certify:

That JACK C. LEE, Ph.D., the witness whose
deposition is hereinbefore set forth, was duly sworn
by me before the commencement of such deposition and
that such deposition was taken virtually and is a
true record of the testimony given by such witness.

I further certify that the adverse party,
MICRON TECHNOLOGY, INC., was represented by counsel
at the deposition.

I further certify that the deposition of
JACK C. LEE, Ph.D., occurred virtually, on
Wednesday, May 28th, 2025, from 9:01 a.m. to 12:59
p.m. EDT.

1 I further certify that I am not related to
2 any of the parties to this action by blood or
3 marriage, I am not employed by or an attorney to any
4 of the parties to this action, and that I am in no
5 way interested, financially or otherwise, in the
6 outcome of this matter.

7
8 IN WITNESS WHEREOF, I have hereunto set my
9 hand this 3rd day of June, 2025.

10
11 My commission expires:
12 October 31, 2027

13
14  

15 -----
16 E-NOTARY PUBLIC IN AND FOR THE
17 COMMONWEALTH OF VIRGINIA
18
19
20
21
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