MICRON TECHNOLOGY, INC.

Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Patent Owner

Case No. IPR2024-00794

U.S. Patent No. 10,950,623

Micron's Hearing Demonstratives

July 30, 2025

Overview of the ’623 Patent

> The inventive concepts relate to formation of a 3D NAND memory device with a divided block structure and a method of performing a partial block erase based on the divided block structure.

> In the disclosed 3D-NAND memory device, each of the blocks can be separated into a plurality of sub-blocks by dividing the shared BSG into a plurality of sub-BSGs through one or more first dielectric trenches. Each of the

Ex. 1001 (’623 Patent), 1:33-36, 1:61-64;
see also Paper 1 (Petition), 15-16.

The ’623 Patent’s Claims

1. A memory device, comprising:

a substrate;

a bottom select gate (BSG) disposed over the substrate;

a plurality of word lines positioned over the BSG with a staircase configuration;

a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;

one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and

one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.

Ex. 1001 (’623 Patent), Claim 1

The ’623 Patent’s Claims

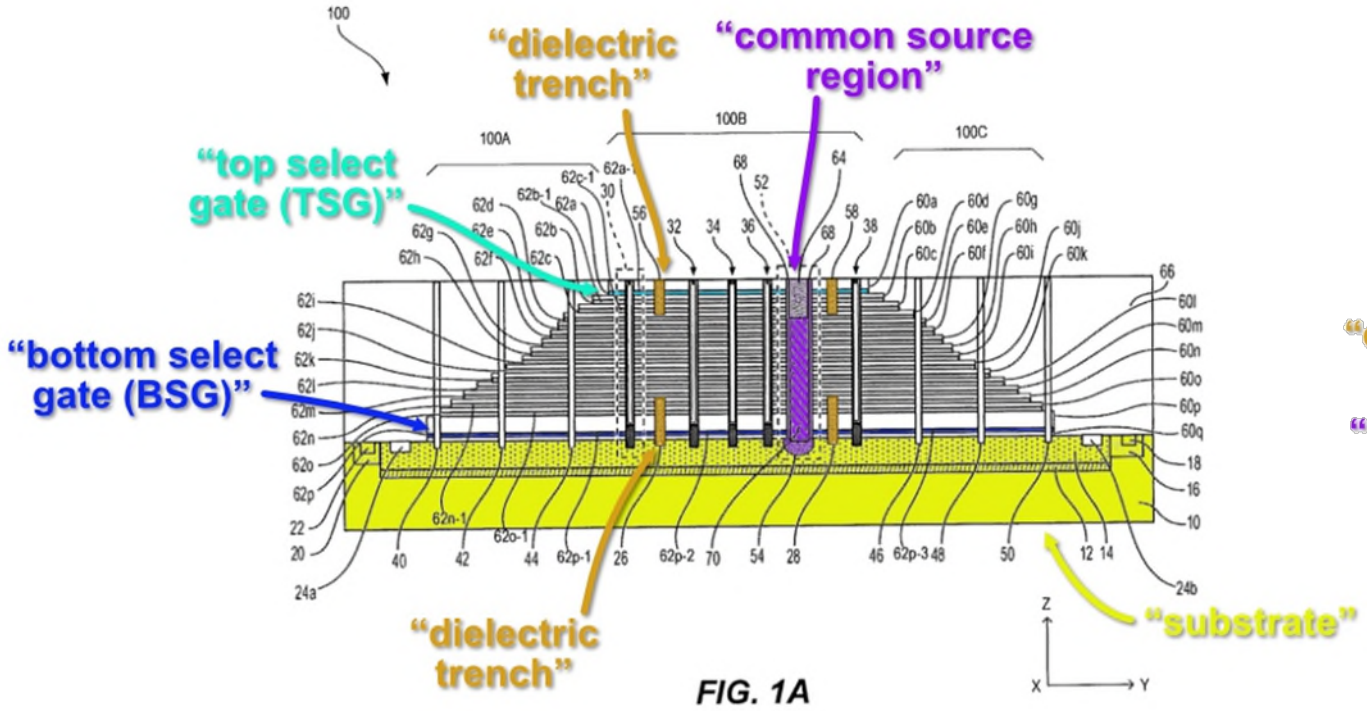


FIG. 1A

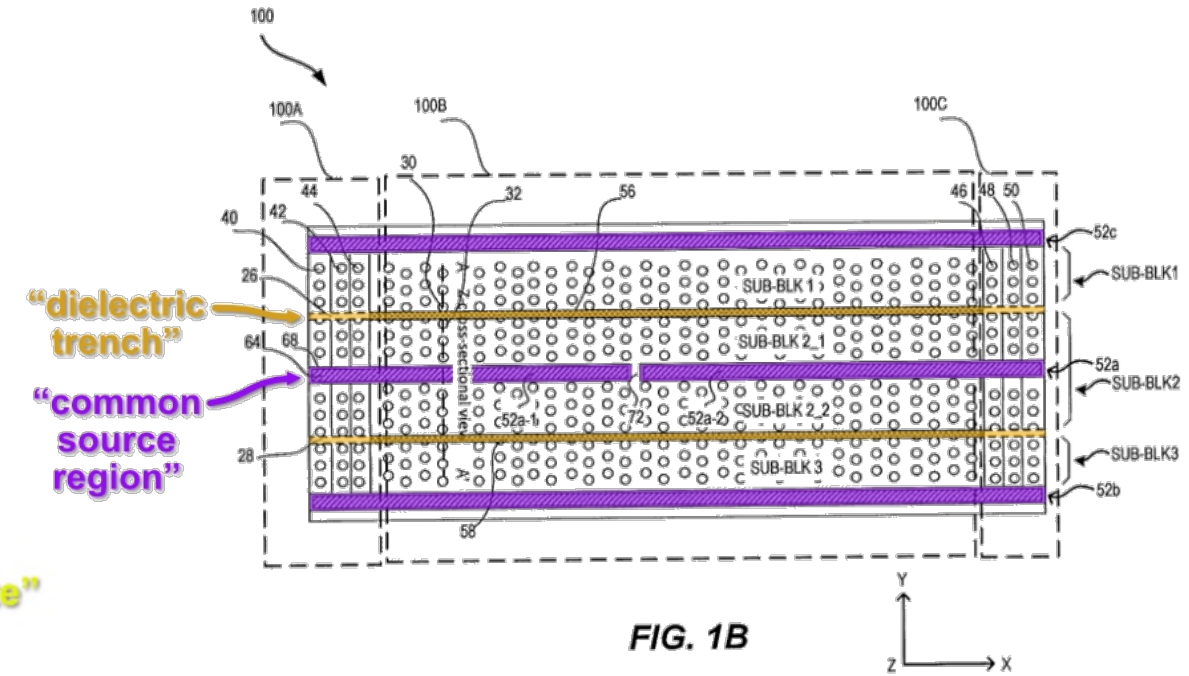


FIG. 1B

Ex. 1001 (’623 Patent), Figs. 1A, 1B; see also Paper 1 (Petition), 17-18.

THE PETITION'S GROUNDS

Instituted Grounds

Ground	Prior Art	Claims
1	Park	1-11 obvious
2	Park + Shibata	1-11 obvious
3	Shibata + Park	1-11 obvious

Paper 1 (Petition), 7-8.

Overview of Park

The present inventive concept relates to a memory device. In particular, the present inventive concept relates to a 3D memory device, i.e., a memory device having a three-dimensional array of memory cells.

form the word lines. In order to independently control the memory cell devices of the first to eighth unit areas UA**1** to UA**8**, the string select line and the ground select line may be separated from each other between the first to eighth unit areas UA**1** to UA**8**. In an example, portions of the string select line may be separated from each other at boundaries between the first to eighth unit areas UA**1** to UA**8** by the first common source lines **102** and first lines **103** of the second common source lines **105**. Moreover, portions of the ground select line may be separated from each other at the boundaries between the first to eighth unit areas UA**1** to UA**8** by the first common source lines **102**, the second common source lines **105**, and isolation insulating layers **111**.

Ex. 1004 (Park), 1:13-17; 5:67-6:12;
see also Paper 1 (Petition), 19-20.

Overview of Park

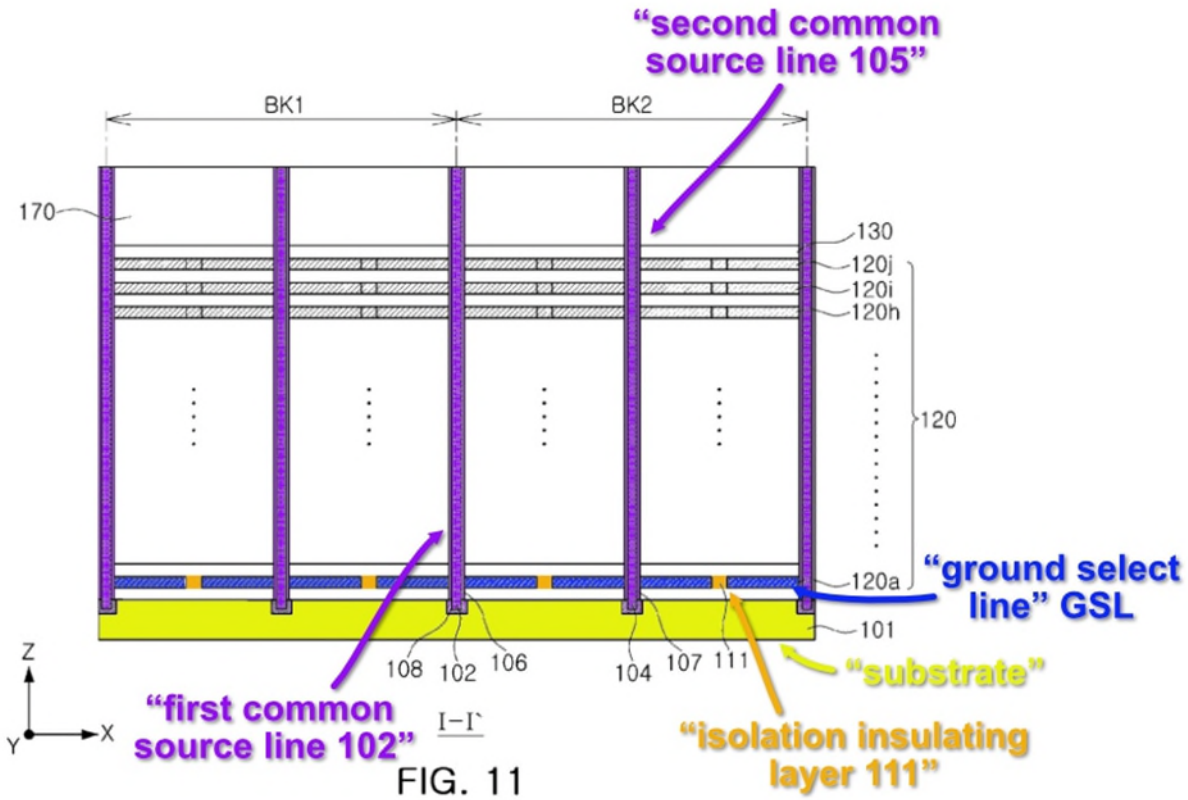


FIG. 11

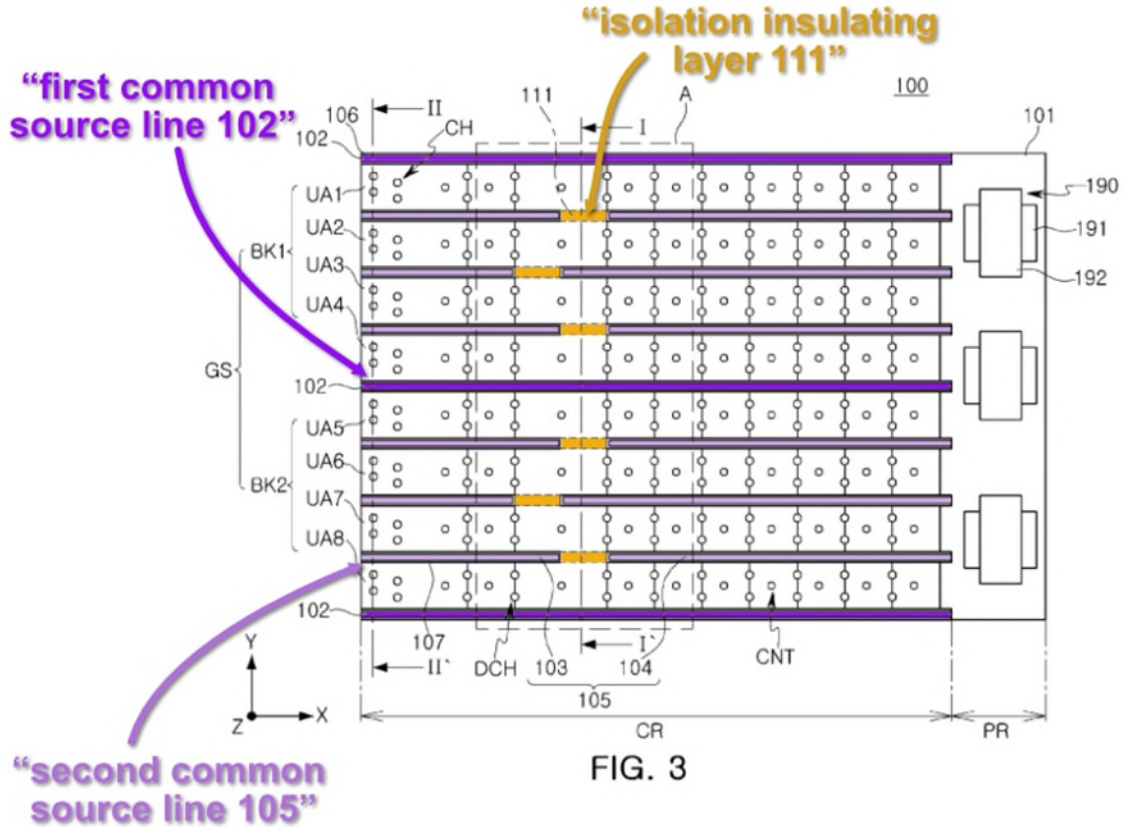


FIG. 3

Ex. 1004 (Park), Figs. 3, 11;
see also Paper 1 (Petition), 21-22.

Overview of Shibata

[0003] A memory device that has a three-dimensional structure including a stacked body including multiple layers of conductive layers stacked with an insulator interposed, a semiconductor body provided inside a memory hole piercing the stacked body, and a charge storage portion provided between the semiconductor body and the conductive layers has been proposed. The multiple layers of conductive layers include multiple word lines functioning as control gates of memory cells, and select gates functioning as control gates of select transistors.

[0083] The first drain-side select gate SGD**0**A, the second drain-side select gate SGD**1**A, the third drain-side select gate SGD**0**B, and the fourth drain-side select gate SGD**1**B each are controlled electrically independently.

[0166] In the example shown in FIG. **16**, one layer of the drain-side select gate layers and three layers of the source-side select gate layers are provided. The multiple layers of the word lines WL are stacked between the drain-side select gate layer and the source-side select gate layers. The three layers of the source-side select gate layers are stacked between the source layer SL and the word line WL of the lowermost layer. In each of the sub-blocks **200***a* and **200***b*, the drain-side select gate layer is divided into two select gates in the Y-direction by the separation portion **62***a*. The separation portion **62***a* of the one sub-block **200***a* divides the drain-side select gate layer into a first drain-side select gate SGD**0** and a second drain-side select gate SGD**1**. The separation portion **62***a* of the other sub-block **200***b* divides the drain-side select gate layer into a third drain-side select gate SGD**2** and a fourth drain-side select gate SGD**3**. The separation portion **62***a* is an insulating film extending in the same direction as the separation portions **60** (the slits ST) piercing the entire stacked body **100**.

Ex. 1005 (Shibata), [0003], [0083], [0166]
see also Paper 1 (Petition), 22-23.

Overview of Shibata

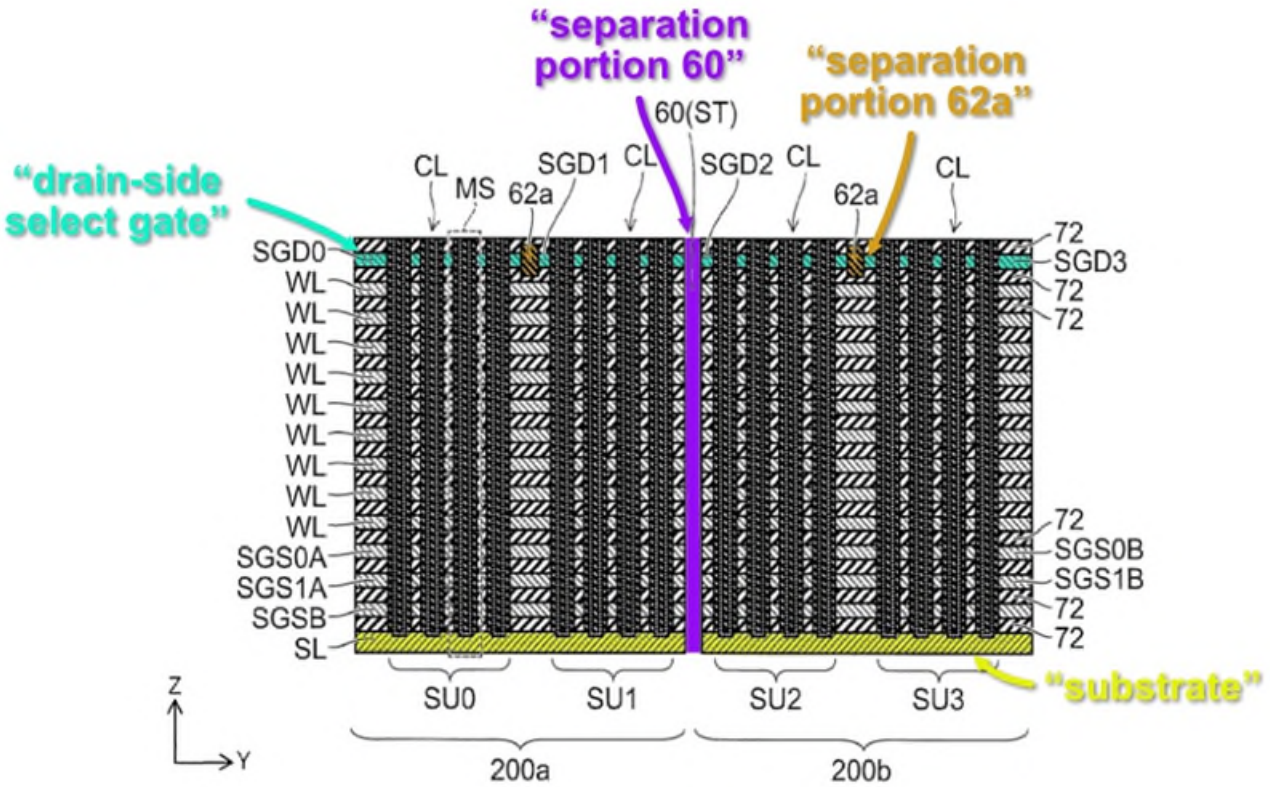


FIG. 16

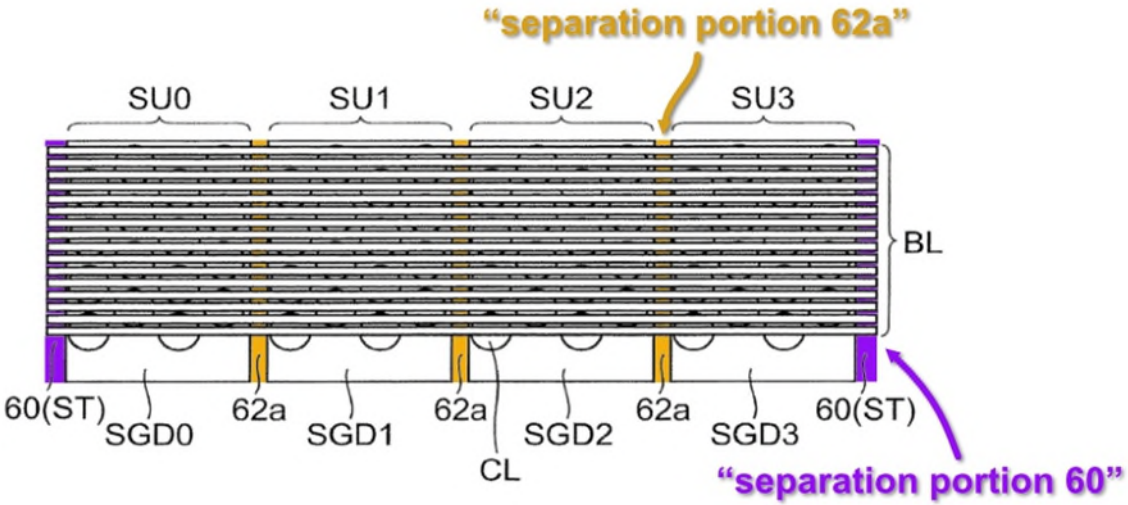


FIG. 47A

Ex. 1005 (Shibata), Figs. 16, 47A;
see also Paper 1 (Petition), 24.

THE PARTIES' REMAINING DISPUTES

Overview of Remaining Disputes

- **Does Park disclose the claimed "dielectric trenches"?** *(Ground 1)*
- **Does Park render the "second dielectric trenches" required by claims 2 and 3 obvious?** *(Ground 1)*
- **Does Park render the "dummy" BSGs and TSGs of claims 10 and 11 obvious?** *(Ground 1)*
- **Would it have been obvious to apply Shibata to Park?** *(Ground 2)*
- **Would it have been obvious to apply Park to Shibata?** *(Ground 3)*

PARK TEACHES THE CLAIMED “DIELECTRIC TRENCHES”

Patent Owner's Arguments Are Entirely Premised on Erroneous Claim Constructions

Patent Owner's Erroneous Positions:

- ❌ Claim 1 is a product-by-process claim requiring that the "dielectric trenches" be manufactured in a conductive BSG layer.
- ❌ The "dielectric trenches" must extend the entire length of the substrate such that they separate the BSG into sub-BSG by themselves.

Paper 12 (Response), 32-34.

Patent Owner Is Incorrect:

- The claims are ***not*** product-by-process claims. It ***makes no difference*** if the claimed "dielectric trenches" are manufactured in the final conductive layer or a temporary sacrificial material.
- The "dielectric trenches" may ***cooperate*** with other structure to separate the BSG into sub-BSG.

Paper 14 (Reply), 3-10.

Claim 1 is an Apparatus Claim: It Specifies Only the *Structure* of the Claimed "Dielectric Trenches," Not Their Method of Manufacture

1. A memory device, comprising:

a substrate;

a bottom select gate (BSG) disposed over the substrate;

a plurality of word lines positioned over the BSG with a staircase configuration;

a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;

one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and

one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.

Ex. 1001 ('623 Patent), Claim 1

The ’623 Patent Uses the Term “Formed In” to Refer to the *Location* of the “Dielectric Trenches”

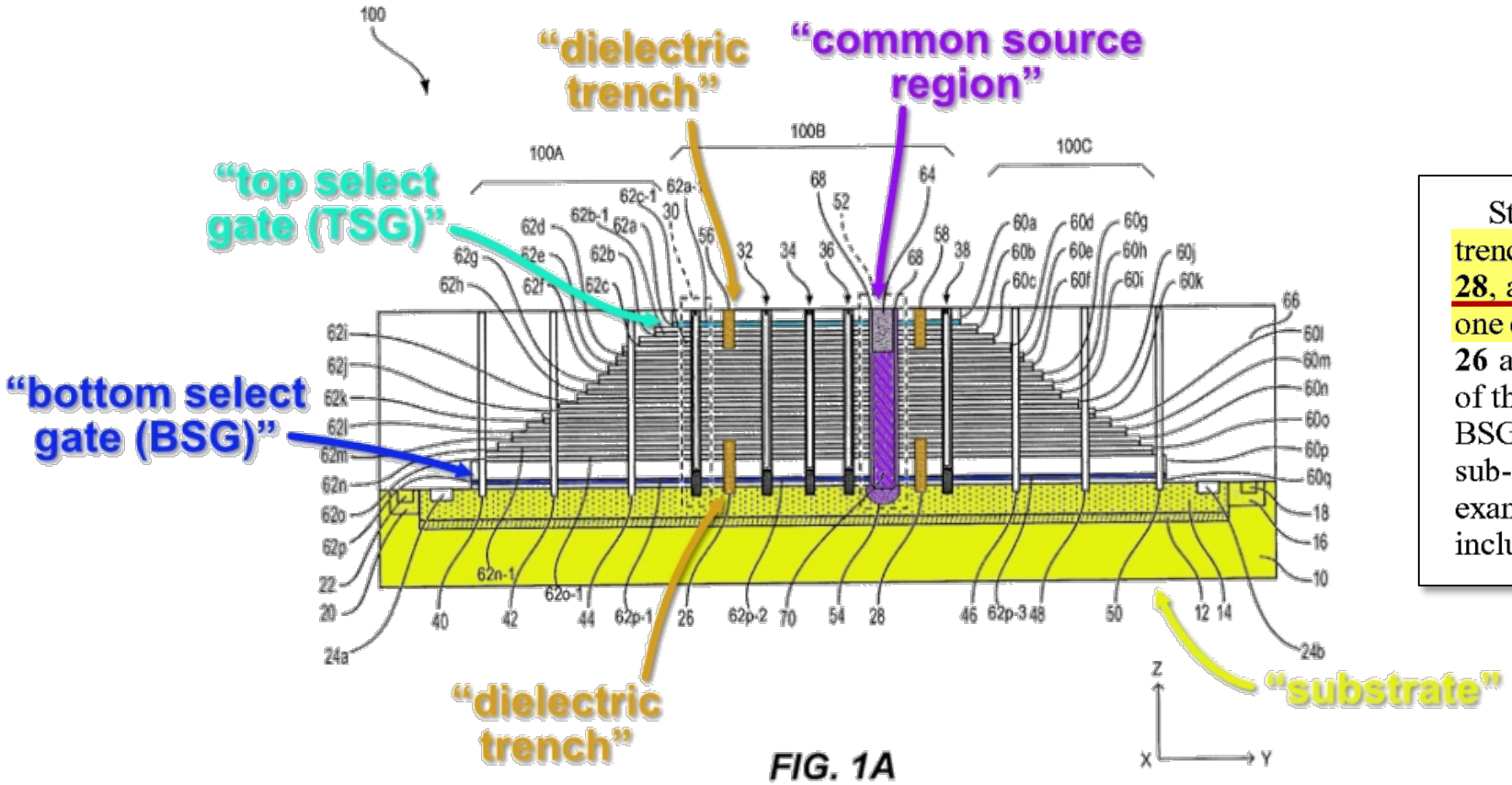


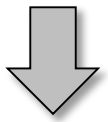
FIG. 1A

Still referring to FIG. **1**A, one or more first dielectric trenches (or first trenches), such as two first trenches **26** and **28**, are formed in the one or more BSGs (e.g., **62***p*) and the one or more dummy BSGs (e.g., **62***n*-**62***o*). The first trenches **26** and **28** extends in an X-direction (i.e., length direction) of the substrate **10** to separate the BSG **62***p* and the dummy BSGs **62***n*-**62***o* layers into a plurality of sub-BSGs and sub-dummy BSGs, or to say, a plurality of cell strings. For example, three sub-BSGs **62***p*-**1**, **62***p*-**2**, and **62***p*-**3** are included in embodiment shown in FIG. **1**A. In addition, one

Ex. 1001 (’623 Patent), 7:17-26, Fig. 1A; see also Paper 14 (Reply) at 4.

The *Same* "Memory Device" Results Regardless of Whether a "Gate First" or "Gate Last" Manufacturing Method is Employed

> After the common source openings are formed, subsequent manufacturing steps to complete the formation of the common source regions can be different between a gate first manufacturing flow and a gate last manufacturing flow. In



> After the formation of the common source regions, a final memory device **100** is formed which is identical to the memory device **100** illustrated in FIG. **1A**.

Ex. 1001 ('623 Patent), 20:28-31, 21:7-9;
see also Paper 14 (Reply) at 5-6.

Patent Owner's Expert Agreed That "Gate First" and "Gate Last" Manufacturing Methods Produce the Same Memory Device

Q. So I understand that, but my question is: In the '623 patent, the '623 patent contemplates in its specification, at least, putting aside the claims, in its specification, contemplates using either a gate-first or a gate-last process to produce the memory device that's shown in Figure 1a; true?

MR. CROSS: Objection. Form.

THE WITNESS: So the specification certainly describes both the gate-first and the gate-last process, and it is also clear in the specification that Figure 1a is an exemplary structure of the 3D-NAND device.

Q. And the patent does not identify any differences in that memory device 100 depending on whether a gate-first or a gate-last process flow is employed, true?

MR. CROSS: Objection. Form.

THE WITNESS: There are not two figures. For example, a Figure 1a and Figure 1a prime that are associated with a gate-first and a gate-last process. There is a single Figure 1a.

BY MR. HERMAN:

Q. Associated with both of those processes, correct?

MR. CROSS: Objection. Form.

THE WITNESS: I think it would be exemplary of an embodiment.

Ex. 1026 (Kuhn Depo.), 17:8-22, 25:7-22; see also Paper 14 (Reply) at 6.

Patent Owner's Construction Reads the '623 Patent's "Gate-Last" Embodiment Out of the Claims

In some embodiments (i.e. Gate-last Formation Technology), the BSG **62***p*, the dummy BSGs **62***n*-**62***o*, the word lines **62***d*-**62***m*, the dummy TSGs **62***b*-**62***c*, and the TSG **62***a* illustrated in FIG. **1**A are formed firstly using sacrificial layers (i.e. SiN). The sacrificial layers can be removed and replaced with a high K layer, glue layers and one or more metal layers. The high K layer can be made of aluminum

After the common source openings are formed, subsequent manufacturing steps to complete the formation of the common source regions can be different between a gate first manufacturing flow and a gate last manufacturing flow. In

. . .

However, in the gate last manufacturing flow, when the common source openings are formed, the BSG, dummy BSGs, word lines, dummy TSGs, and TSG are subsequently removed to form a plurality of vacancies by a wet etching chemical that is introduced through the common source openings. An ion implantation can be thereafter applied to form the dope region (e.g., **54**) at the bottom portion of each of the common source openings. Following the implantation step, the BSG, dummy BSGs, word lines, dummy TSGs, and TSG are re-formed by filling the vacancies with a high-K layer plus metal layers through the common source openings. Next, a dielectric spacer, such as the dielectric spacer

Ex. 1001 ('623 Patent), 7:1-8, 20:28-60
see also Paper 14 (Reply) at 6.

The Board Properly Found When Instituting that the "Dielectric Trenches" Do Not Need to Divide the BSG on Their Own

> In view of the claim language and the description in the '623 patent, we construe the phrase "the dielectric trenches . . . separate the BSG into a plurality of sub-BSGs" as requiring that the trenches separate the BSG into sub-BSGs, but that other components are not excluded from cooperating in the separation of the BSG into sub-BSGs. The '623 patent states that separation occurs "[b]y introducing the . . . trench[] into the memory device." Ex. 1001, 7:45–47. Claim 1 does not require any particular structure of the memory device, and as discussed above, the described structures in the '623 patent, which are described as purely exemplary, indicate that structures such as the common source regions may assist in defining the boundaries of the BSG and sub-BSGs.

Paper 9 (Institution Decision) at 15.

The Presence of the "Dielectric Trenches"—Which Are "Exemplary"—Merely Has to Cause the BSG to Be Separated

the SUB-BLK land SUB-BLK **3**. Without the introduction of the first/second trenches, the memory device **100** (or the memory cell block **100**) has a shared BSG, such as **62***p*, and a shared TSG, such as **62***a*.

It should be understood that FIG. **1**B is merely an exemplary 3D NAND memory device **100**, and the 3D NAND memory device **100** can include any number of first trenches or second trenches between two adjacent common source regions. For example, two or more first trenches or two or more second trenches can be disposed between two adjacent common source regions. The 3D NAND memory device **100** can also include any number of common source regions.

Ex. 1001 ('623 Patent), 9:46-59;
see also Paper 14 (Reply) at 8.

The ’623 Patent Itself Separates a “sub-BSG” from an Adjacent “sub-BSG” On One of its Sides Using Only a “Common Source Region”

components. In some embodiments, the memory device **100** is one of memory cell blocks of a 3D-NAND chip (not shown). The common source regions **52***b* and **52**C accordingly isolate the memory device **100** (or the memory cell block **100**) from adjacent memory cell blocks of the 3D-NAND chip. The common source region **52***a* is disposed at a middle position of the memory device **100**. The common

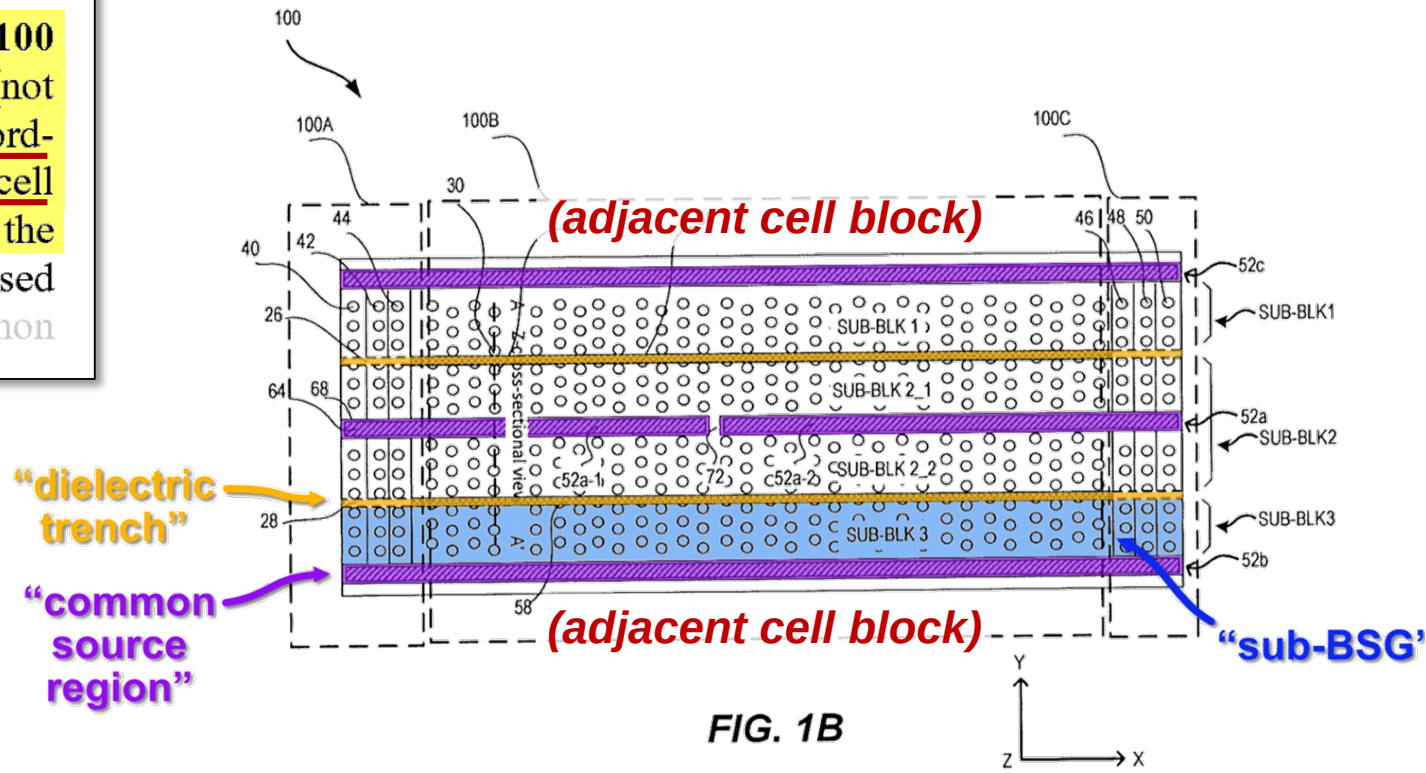


FIG. 1B

Ex. 1001 (’623 Patent), 9:8-13; Fig. 1B;
see also Paper 1 (Petition) at 35-36; Paper 14 (Reply) at 9-10.

PARK WOULD HAVE OBVIOUSLY EMPLOYED “SECOND DIELECTRIC TRENCHES”

The Obvious Modification to Park Set Forth in the Petition

Park modified to replicate its lower trenches in its upper layers, resulting in claim 2's ***"second" "dielectric trenches formed in the TSG"*** *forming* ***"a plurality of sub-TSGs":***

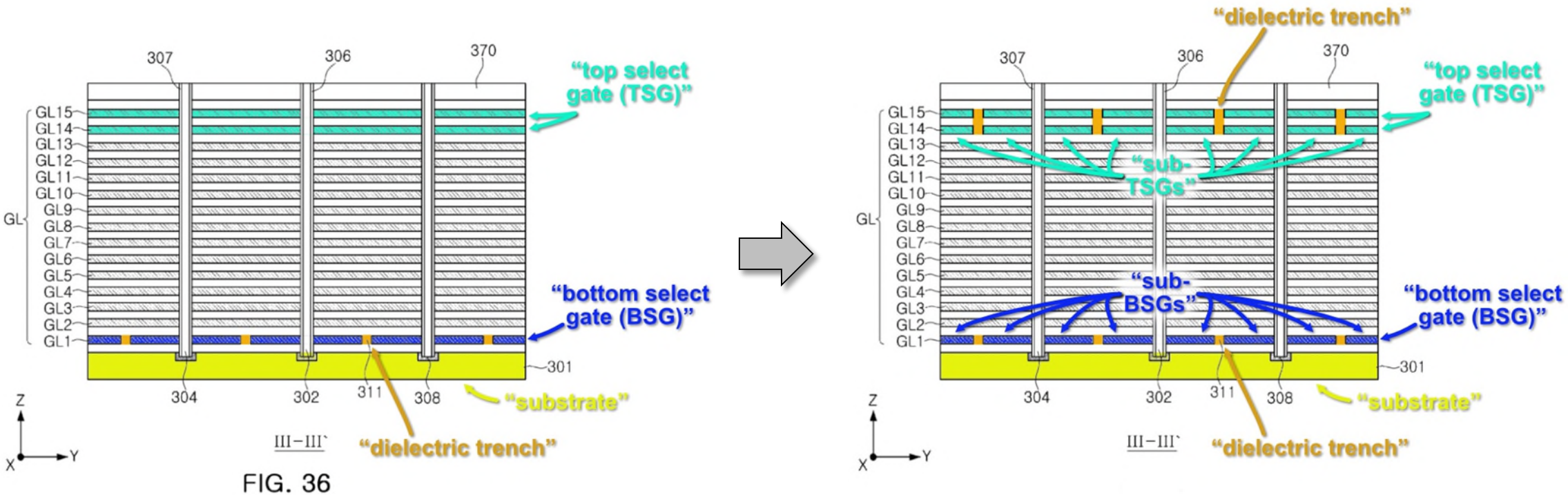


FIG. 36

Paper 1 (Petition) at 41-43.

Patent Owner Improperly Assumes that Park's Figures Include Errors

Patent Owner's Erroneous Positions:

❌ "A POSITA would not have modified Park to include an isolation insulating layer in the alleged TSG (SLL) because there is no TSG in the region where Petitioner proposes adding the … layer…. Figure 36 includes an error and mistakenly shows all of the layers present in the device…."

Paper 12 (Response), 40, 43.

Patent Owner Is Incorrect:

- No reasonable POSITA would conclude that ***five separate figures*** and ***multiple textual passages*** in Park all include errors.
- Park confirms that there is no error by separately teaching that its gate layers and isolation insulating layers 111 can have ***different locations and physical extents***.

Paper 14 (Reply), 3-10.

Park Depicts Its TSG (or the Sacrificial Layers / Etched Openings that Precede the TSG) as Existing Over the Area Where Its BSG Is Divided in *Five* Figures

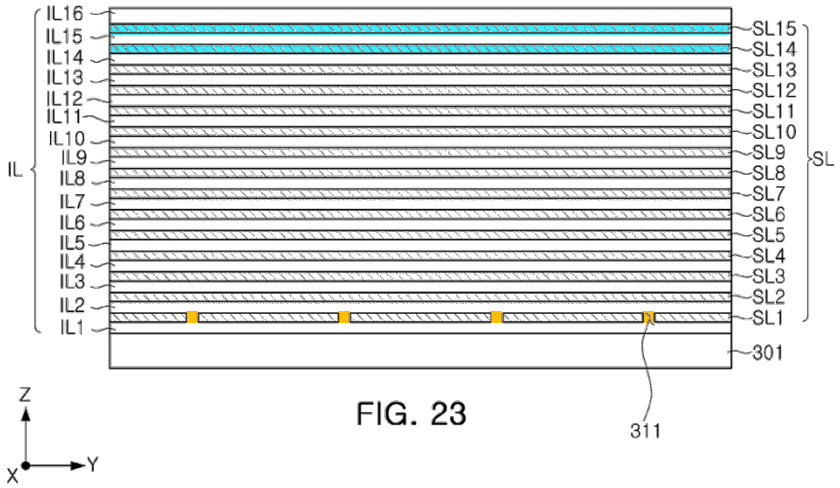


FIG. 23

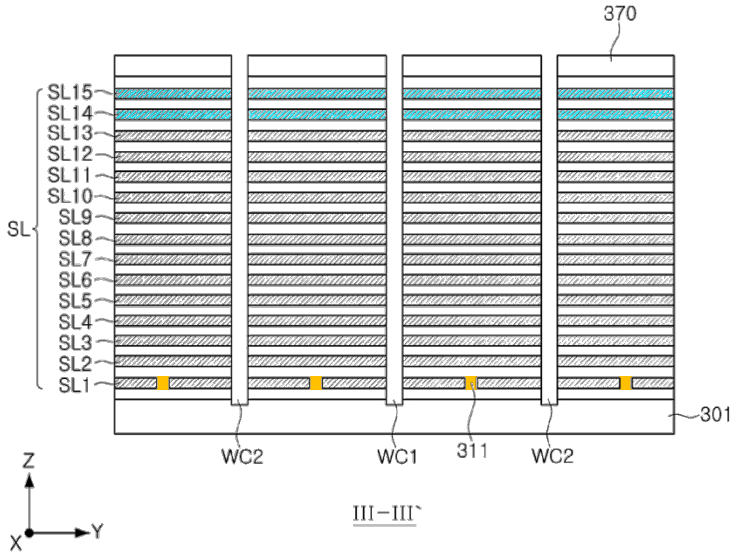


FIG. 29

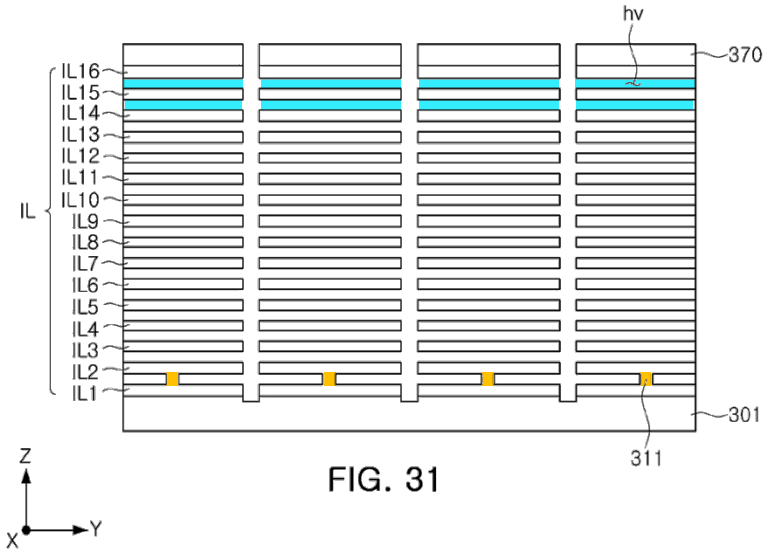


FIG. 31

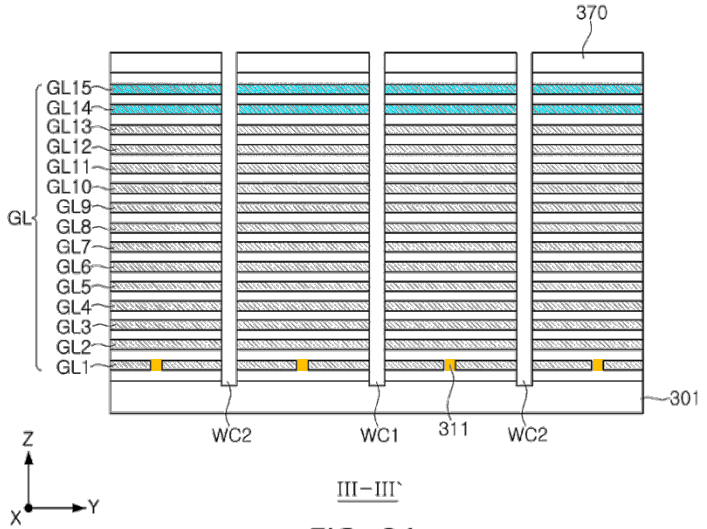


FIG. 34

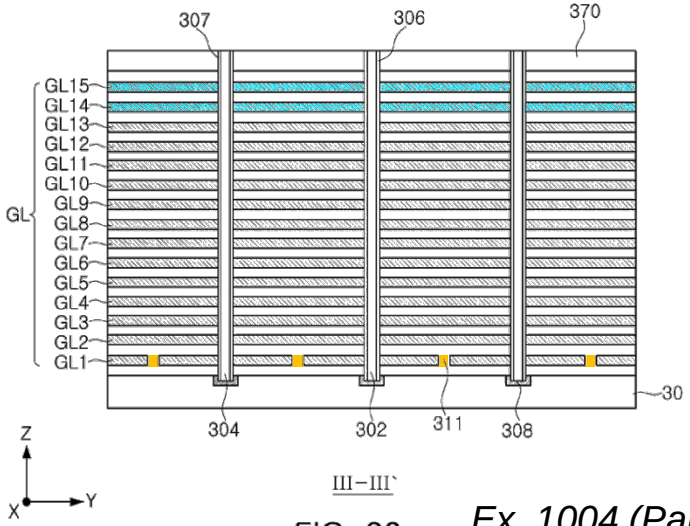


FIG. 36

Ex. 1004 (Park), Figs. 23, 29, 31, 34, 36; see also Paper 14 (Reply) at 12-13.

Park States that Figures 33-36 Depict Both the Top/String Select Layers and Lower Trenches

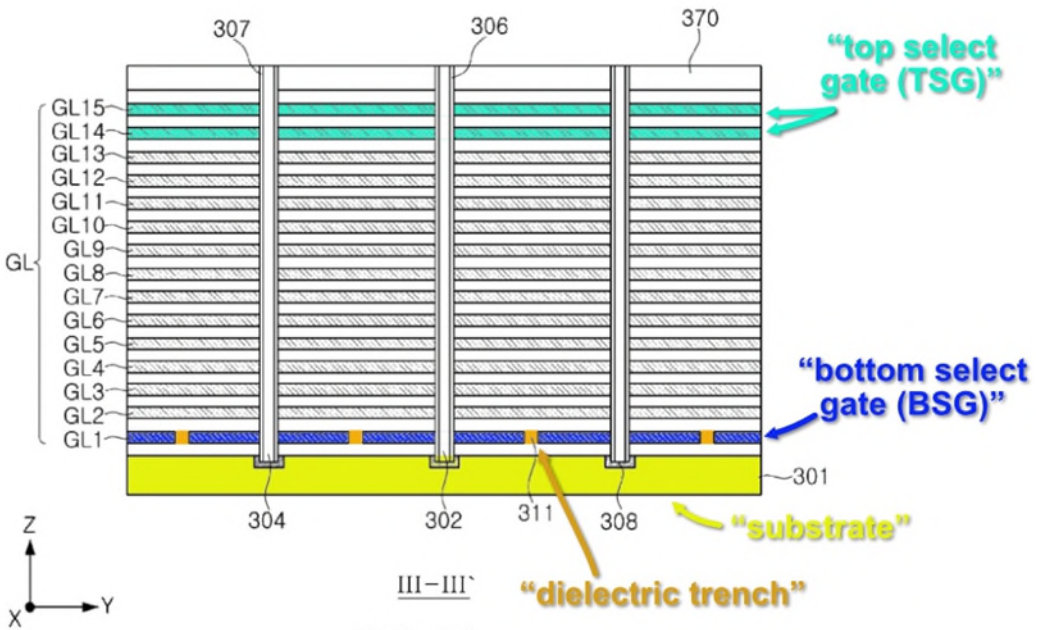


FIG. 36

by gate electrode layers GL. The gate electrode layers GL may form a ground select line, word lines, a dummy line, and a string select line. In the example illustrated in FIG. **34**, the first gate electrode layer GL**1** may form the ground select line, and the second to fourth gate electrode layers GL**2** to GL**4** and the thirteenth gate electrode layers GL**13** may form the dummy line. The fifth to twelfth gate electrode layers GL**5** to GL**12** may form the word lines, and the fourteenth and fifteenth gate electrode layers GL**14** and GL**15** may form the string select line.

collectively represented by a connecting electrode SE. The first gate electrode layer GL**1** forming the ground select line may be divided into separate unit electrodes in each of the first to eighth unit areas UA**1** to UA**8** by the isolation regions **311**. The fourteenth and fifteenth gate electrode layers GL**14** and GL**15** forming the string select line may be divided into separate unit electrodes in each of the first to eighth unit areas UA**1** to UA**8** by the first and second word line cuts WC**1** and WC**2**. As a result, the respective second to

Ex. 1004 (Park), 16:7-17, 16:22-30, Fig. 36;
see also Paper 1 (Petition) at 41-42; Paper 14 (Reply) at 11-12.

Figure 27 Is Intended to Show Park's Insulation 370 and Channel Structures (Not Impose Limits on Park's Conductive and Isolation Insulating Layer Layout)

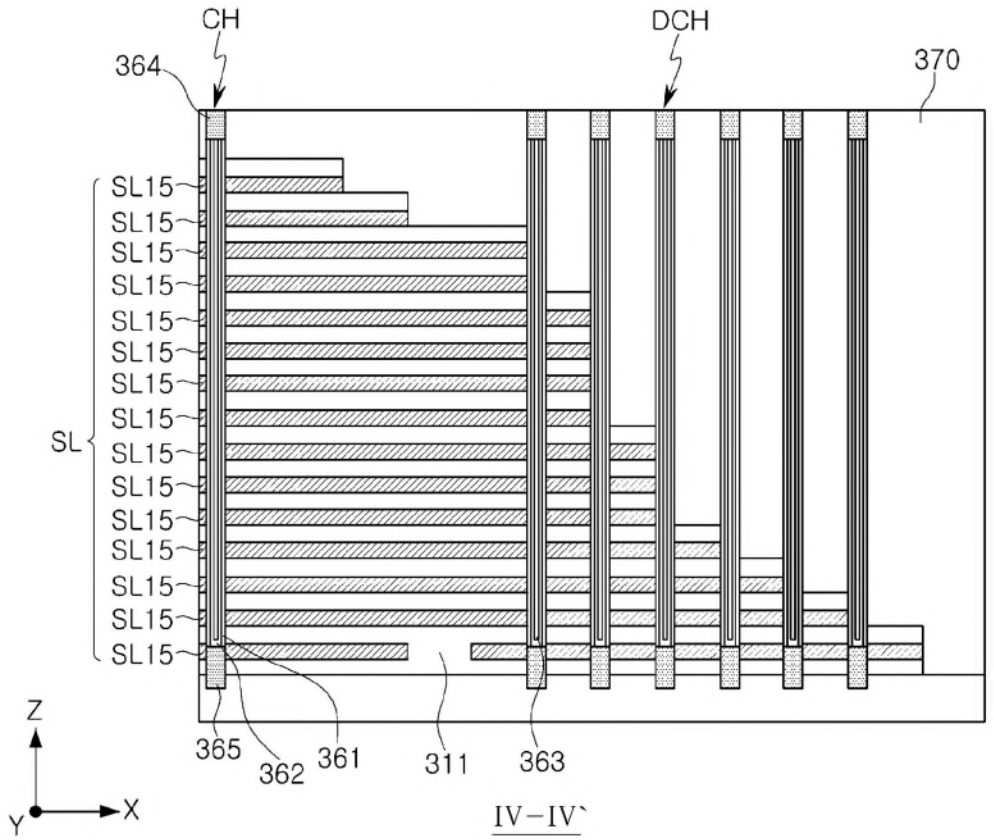


FIG. 27

Referring to FIGS. **26** and **27**, an interlayer insulating layer **370** may be formed on the pad regions PAD, and a plurality of cell channel structures CH and a plurality of dummy channel structures DCH may be formed. The interlayer insulating layer **370** may be formed on the pad regions PAD to cover the insulating layers IL and the sacrificial layers SL, and may include a silicon oxide or a silicon nitride. In an example, the interlayer insulating layer **370** may be formed by forming a plurality of layers of essentially the same material one on another.

Ex. 1004 (Park), 13:35-44, Fig. 27;
see also Paper 14 (Reply) at 12.

Park Explains That Its Electrodes and the Openings in Which Isolation Insulating Layers 111 Are Formed Can Have Different Locations and Physical Extents

While various examples of the inventive concept have been shown and described above, it will be apparent to those skilled in the art that modifications and variations could be made to such examples without departing from the scope of the present inventive concept as defined by the appended claims.

formed by the dummy line **120***j*. Furthermore, the connecting electrodes **129***f* to **129***i* may be disposed in different positions in the first direction, e.g., the X-axis direction, in each gate electrode layer **120** thereof.

connecting electrodes connecting the unit electrodes forming the word lines maybe formed at the same positions in the first direction (the X-axis direction) within each of the first and second blocks BK**1** and BK**2**, respectively.

Referring to FIGS. **20** and **21**, a plurality of opening regions OP may be formed in the first sacrificial layer SL**1**. Portions of the first insulating layer IL**1** may be exposed through the opening regions OP. At least a portion of the opening regions OP may be formed in different positions in a first direction, for example, an X-axis direction.

Ex. 1004 (Park), 8:59-9:2, 12:13-21, 12:65-13:3, 18:4-9; see also Paper 14 (Reply) at 11-12.

PARK RENDERS CLAIMS 10 AND 11 OBVIOUS

Park's *"Dielectric Trenches"* Would Have Obviously Extended Through Its *"Dummy BSGs"* and *"Dummy TSGs"* as Claims 10 and 11 Require

Patent Owner's Erroneous Positions:

- ❌ Petitioner only "states that" etching through multiple layers "'could' be done."
- ❌ "It is not possible to discern the reasoning" for modifying Park "from Dr. Lee's declaration."
- ❌ "Petitioner … fails to explain how a POSITA would have achieved … modification of Park's device."

Paper 12 (Response), 50-51.

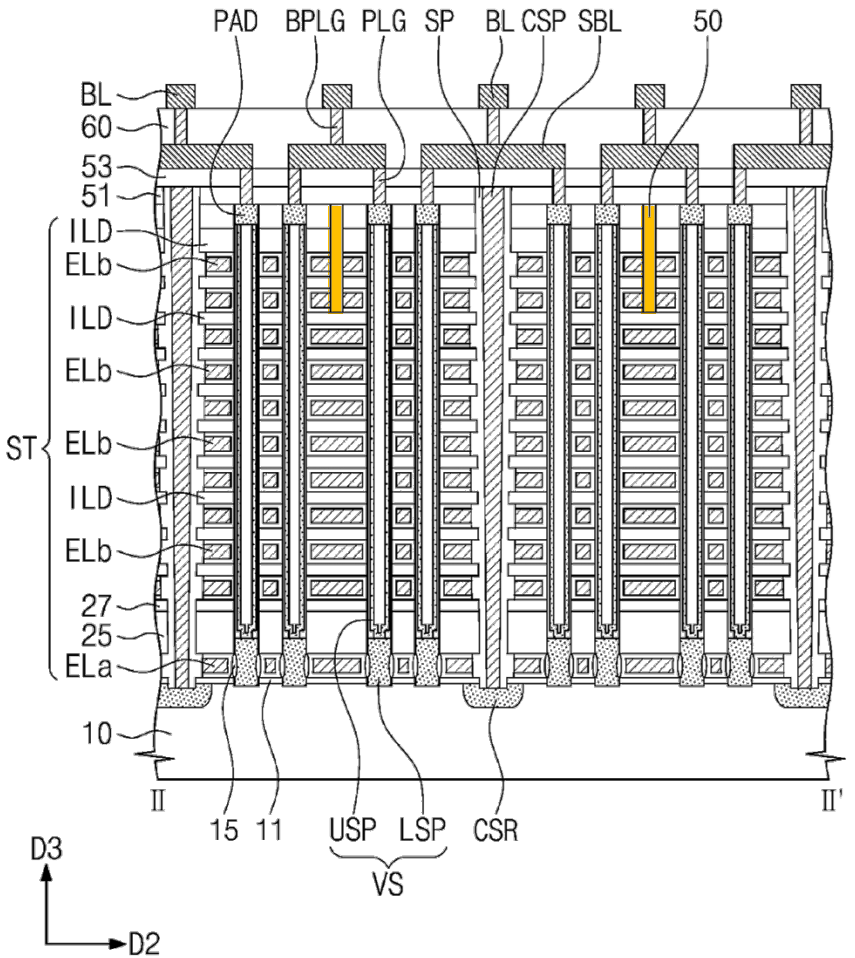
Patent Owner Is Incorrect:

- The prior art teaches that dielectric trenches can alternatively divide one, multiple, or even all of a memory's gate layers.
- Dr. Lee explained in detail why it would have been beneficial to divide both Lee's select gate and adjoining dummy layers.
- Park ***already*** discusses use of the same type of well-known timed etch required to make an opening through both sacrificial and insulating layers.

Paper 14 (Reply), 14-16.

It Was Known in the Art to Divide *Multiple* Select Gate Layers With Trenches of Insulation

FIG. 4B



> Furthermore, in the electrode structure ST, the upper electrodes ELb located at the highest level may be spaced apart from each other by an insulating separation pattern **50**, and may have a line shape extending in the first direction D**1**.

Ex. 1018 (Hwang), [0058], Fig. 4B;
see also Paper 1 (Petition) at 55-56; Paper 14 (Reply) at 16.

Dr. Lee Explained in Detail Why It Would Have Been Obvious to Separate Both Park's Dummy and Select Gate Layers

- Dummy gate layers operate to suppress leakage current, avoid unwanted hot-carrier injection, and minimize data disturb.

Ex. 1003 (Lee Decl.), ¶ 281; Ex. 1012 (Micheloni), 120; 144.

- Dividing both the dummy and select gate layers would "improve … electrical performance" and "help the dummy BSGs … serv[e] their purpose" by making "loading effects" "more symmetrical."

Ex. 1003 (Lee Decl.), ¶ 281; Ex. 1025 (Lee Reply), ¶¶ 26-29.

- "A POSITA would have recognized that by dividing the dummy gates in a manner consistent with the select gates – i.e., using the same dielectric trenches to form sub-dummy gates – a designer ensures that both sets of transistors experience comparable gate loading" allowing for more "stable gate potentials…."

Ex. 1025 (Lee Reply), ¶ 29.

see also Paper 1 (Petition) at 55-56; Paper 14 (Reply) at 16.

Timed Etches Were Not Only Admittedly Known in the Prior Art But They Are Referenced in Park

Referring to FIGS. **24** and **25**, pad regions PAD may be formed by etching the sacrificial layer SL and the insulating layer IL. FIG. **25** is a perspective view of region D of FIG.

Q. What is a "timed etch"?

A. So when one is etching a structure -- and, again, this is generally speaking of the textbook education level -- a timed etch is an etch that is not selective. Someone simply makes a pattern on the wafer, turns the etcher on and allows the etch to run for a certain length of time and turns the etcher off.

Q. Were timed etches also known at the time the '623 patent was filed?

A. Yes.

Ex. 1004 (Park), 13:18-25; Ex. 1026 (Kuhn Depo.), 10:10-21; see also Paper 14 (Reply) at 16.

IT WOULD HAVE BEEN OBVIOUS TO APPLY SHIBATA TO PARK

The Obvious Modification to Park (Following Shibata's Teachings) Set Forth in the Petition

*Park includes the claimed **"dielectric trenches"** that **"extend in a length direction of the substrate"** under the correct construction:*

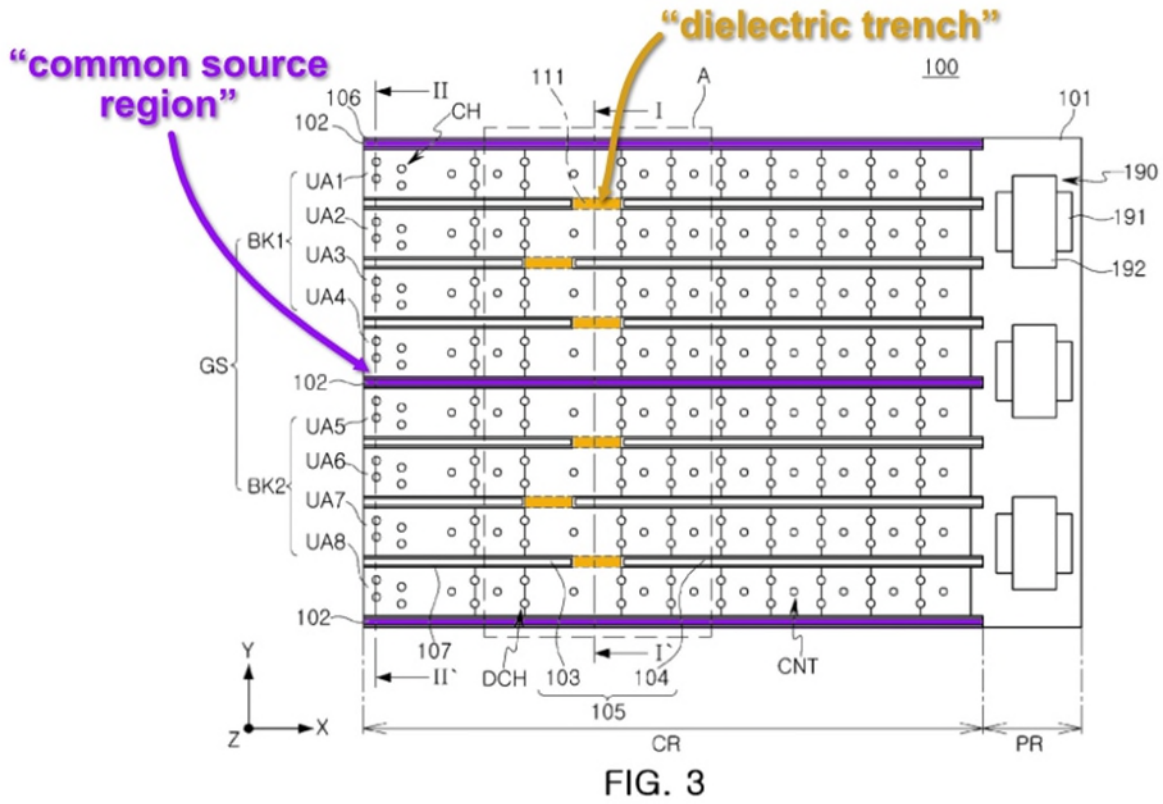


FIG. 3

*Park—when modified following Shibata—would have included longer **"dielectric trenches"** satisfying Patent Owner's erroneous construction:*

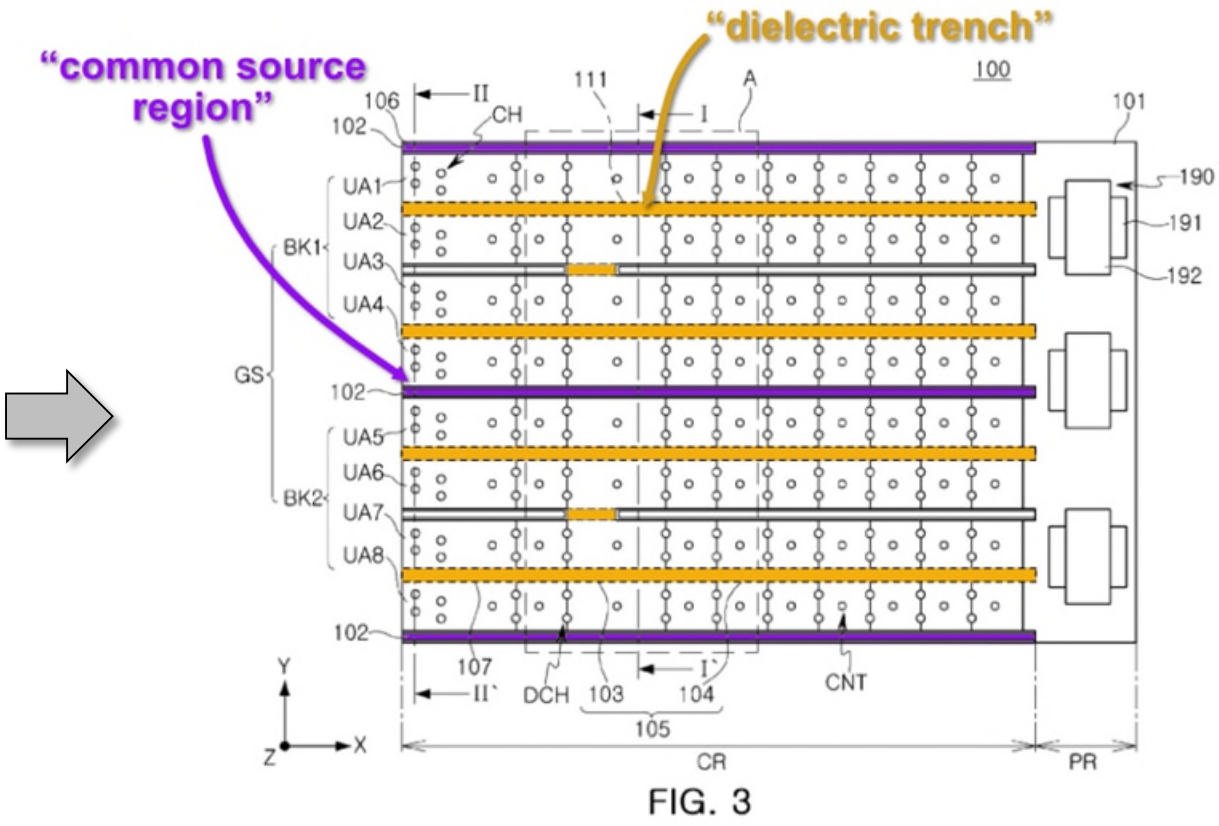


FIG. 3

Paper 1 (Petition) at 41-43.

Patent Owner's Arguments Are Contrary to the Prior Art

Patent Owner's Erroneous Positions:

- ❌ Park "actively discourages" combination with Shibata by referencing a potential "problem" encountered when etching sacrificial layers.
- ❌ Shibata provides "no solution" to the etching problem mentioned in Park.
- ❌ Reducing the number of common source regions in Park would have "adverse effects on the memory device."

Paper 12 (Response), 60, 64-65, 67.

Patent Owner Is Incorrect:

- Park ***allows for and facilitates*** the very modification discussed in the Petition.
- Shibata addresses the ***same*** problem discussed in Park.
- Park ***itself contemplates*** reducing the number of common source regions in its memory device.

Paper 14 (Reply), 17-22.

Park *Specifically Allows* Longer, Non-Staggered Dielectric Trenches

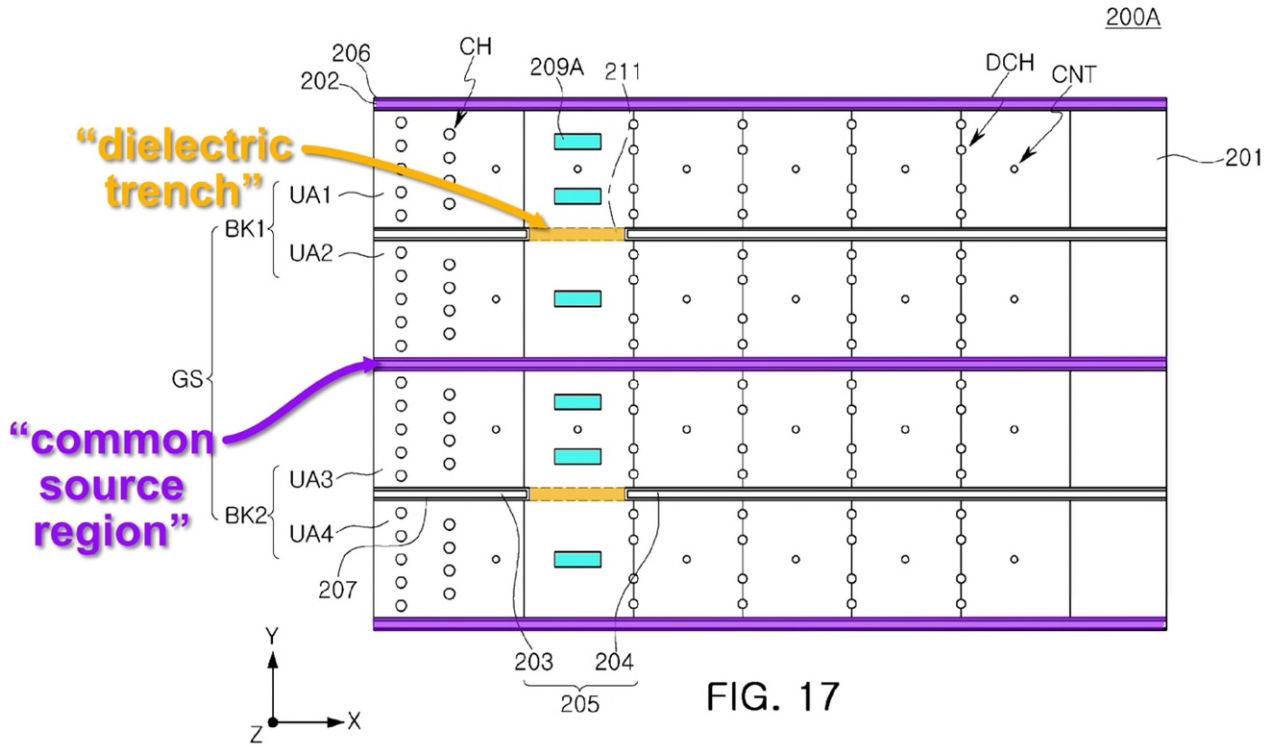


FIG. 17

lines **202**. In the memory device **200**A according to the example illustrated in FIG. **17**, vertical insulating layers **209**A may be spaced from first and second common source lines **202** and **205**. The vertical insulating layers **209** and **209**A may be disposed adjacent to the connecting electrodes connecting the unit electrodes forming the word lines in the first to fourth unit areas UA**1** to UA**4**. Because the inflow passages of the phosphoric acid and the conductive material would be longer in a region adjacent to the connecting electrodes, the vertical insulating layers **209** and **209**A are formed to thus shorten the inflow passages of the phosphoric acid and the conductive material.

Ex 1004 (Park), 12:41-52, Fig. 17;
see also Paper 14 (Reply) at 19.

Etchant Will Still Flow Through the Vast Majority of the Modified Park Structure

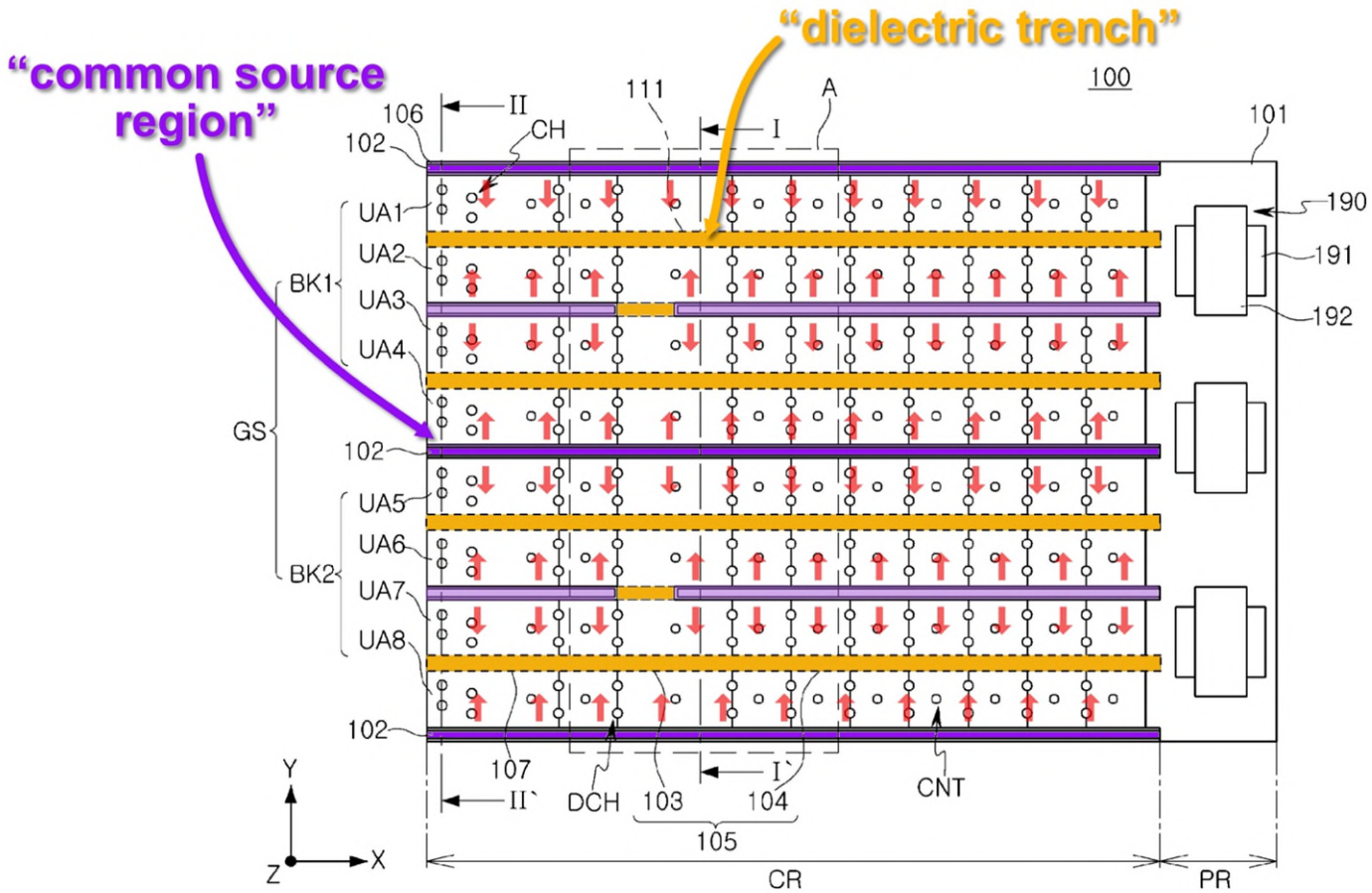


FIG. 3

Ex. 1003 (Lee Decl.), ¶¶ 319-323; Ex. 1025 (Lee Reply), ¶¶ 44-46; see also Paper 1 (Petition) at 62-63; Paper 14 (Reply) at 20-21.

Shibata *Also* Provides a Solution to Address Etchant Flow Issues

adjacent to the slit ST is easily ensured. On the other hand, the width of the portion of the drain-side select gate not adjacent to the slit ST between the separation portion **62***a* and the columnar portions CL easily can be narrower than the width of the portion between the slit ST and the columnar portions CL of the drain-side select gate adjacent to the slit ST. Accordingly, the resistance of the drain-side select gate not adjacent to the slit ST easily can be higher than the resistance of the drain-side select gate adjacent to the slit ST. This may increase the time constant of the drain-side select gate not adjacent to the slit ST and delay the access time.

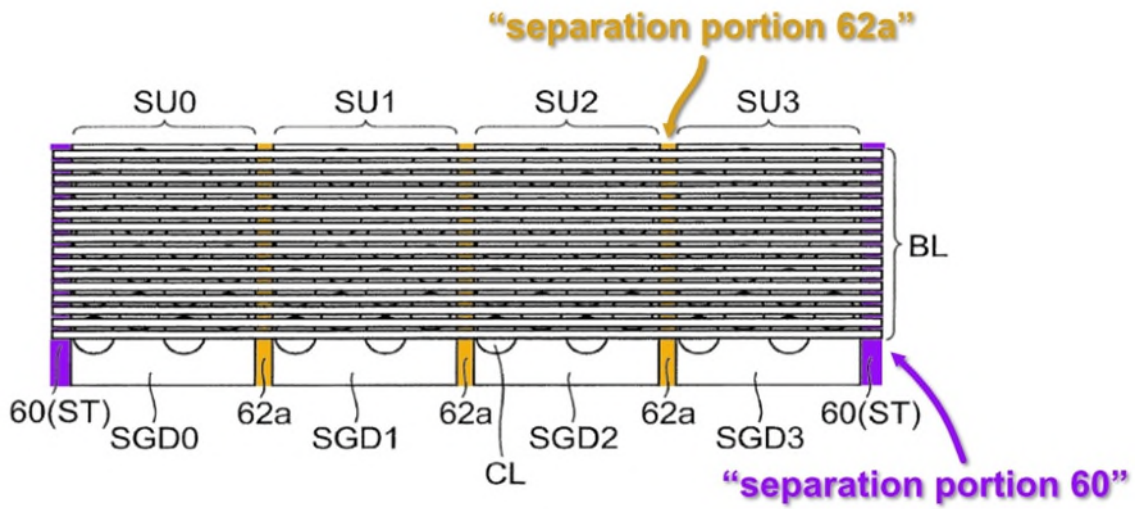


FIG. 47A

[0446] As shown in FIG. **46** and FIG. **47**A, the separation portions **62***a* divide the one drain-side select gate layer into the first drain-side select gate SGD**0**, the second drain-side select gate SGD**1**, the third drain-side select gate SGD**2**, and the fourth drain-side select gate SGD**3**.

[0447] As shown in FIG. **45**, the first drain-side select gate SGD**0** is connected to the drive circuit DRV**0**. The second drain-side select gate SGD**1** is connected to the drive circuit DRV**1**. The third drain-side select gate SGD**2** is connected to the drive circuit DRV**2**. The fourth drain-side select gate SGD**3** is connected to the drive circuit DRV**3**.

[0448] The second drain-side select gate SGD**1** is connected to the two drive circuits DRV**1** from both sides of the word line WL. The second drain-side select gate SGD**1** is driven from both sides of the word line WL. The third drain-side select gate SGD**2** is connected to the two drive circuits DRV**2** from both sides of the word line WL. The third drain-side select gate SGD**2** is driven from both sides of the word line WL.

[0449] Accordingly, even if the resistance of the drain-side select gate SGD**1**, SGD**2** is high, the rise time of the drain-side select gate SGD**1**, SGD**2** is not delayed as compared with the rise time of the other drain-side select gate SGD**0**, SGD**3**.

Ex 1005 (Shibata), [0325], [0446]-[0449];
see also Paper 1 (Petition) at 62; Paper 14 (Reply) at 20.

Park *Already Includes* Embodiments With Fewer Common Source Regions

9x common source lines 102 and 105:

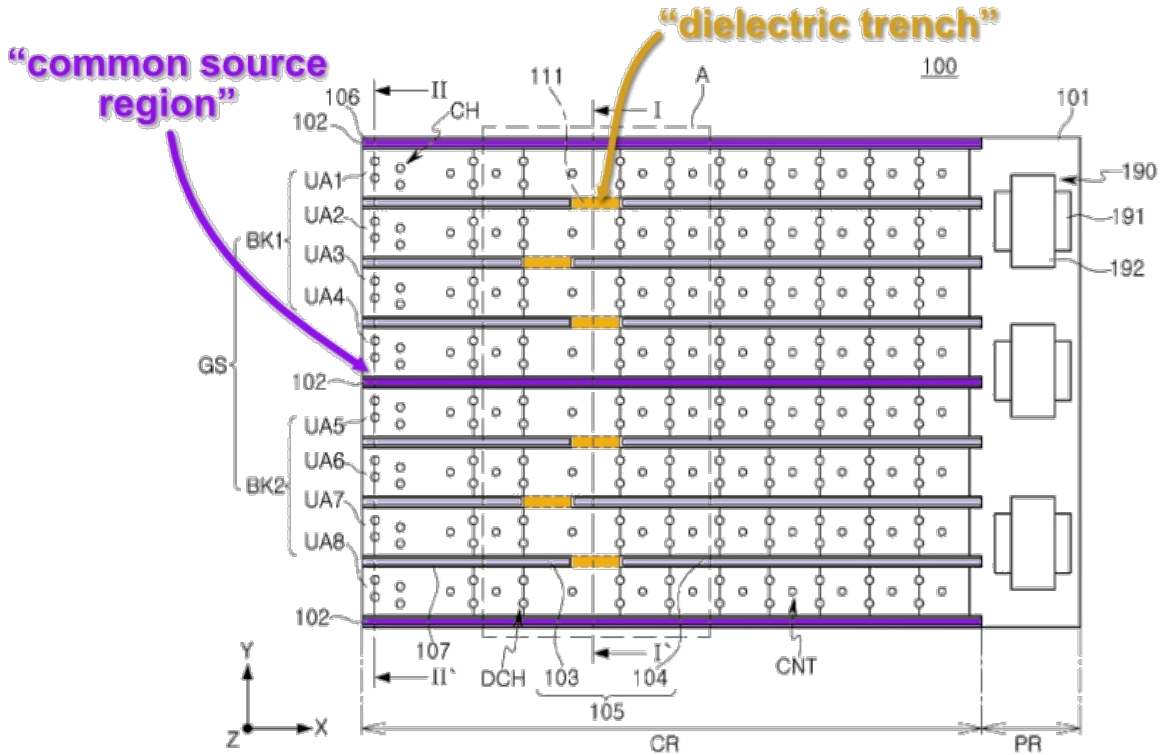


FIG. 3

5x common source lines 202 and 205:

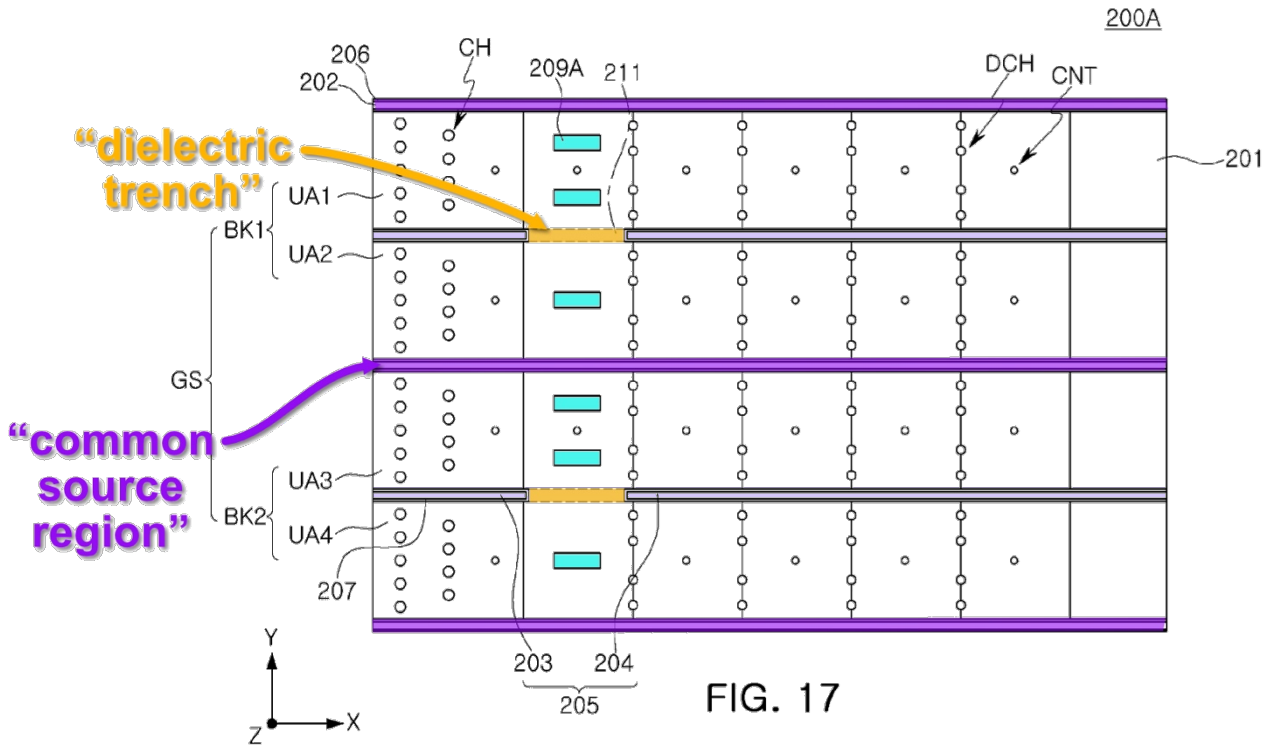


FIG. 17

Ex 1004 (Park), Figs. 3, 17;
see also Paper 14 (Reply) at 21-22.

Replacing Common Source Regions with Dielectric Trenches Increases Memory Density, Thus Furthering Park's Goals

Park:

Thus, a benefit of the inventive concept resides in that a degree of freedom of space utilization of a memory device may be increased such that a larger number of layers of word lines may be provided, thus increasing the capacity of a memory device and the degree of integration thereof.

Shibata:

[0118] Conversely, according to the embodiment, the separation portion **62***b* that has a smaller width than the separation portion **60** (the slit ST) divides the drain-side select gate layer of the second string unit SU**1** and the drain-side select gate layer of the third string unit SU**2**. Therefore, according to the embodiment, it is possible to reduce the number of the separation portions **60** (the slits ST) and reduce the planar size of the memory cell array.

Ex 1004 (Park), 17:1-5; Ex. 1005 (Shibata), [0118]
see also Paper 1 (Petition) at 60-61; Paper 14 (Reply) at 22.

IT WOULD HAVE BEEN OBVIOUS TO APPLY PARK TO SHIBATA

The Obvious Modification to Shibata (following Park's Teachings) Set Forth in the Petition

*Shibata modified to include claim 1's **"first" "dielectric trenches formed in the BSG"** resulting in **"a plurality of sub-BSGs"** as Park teaches:*

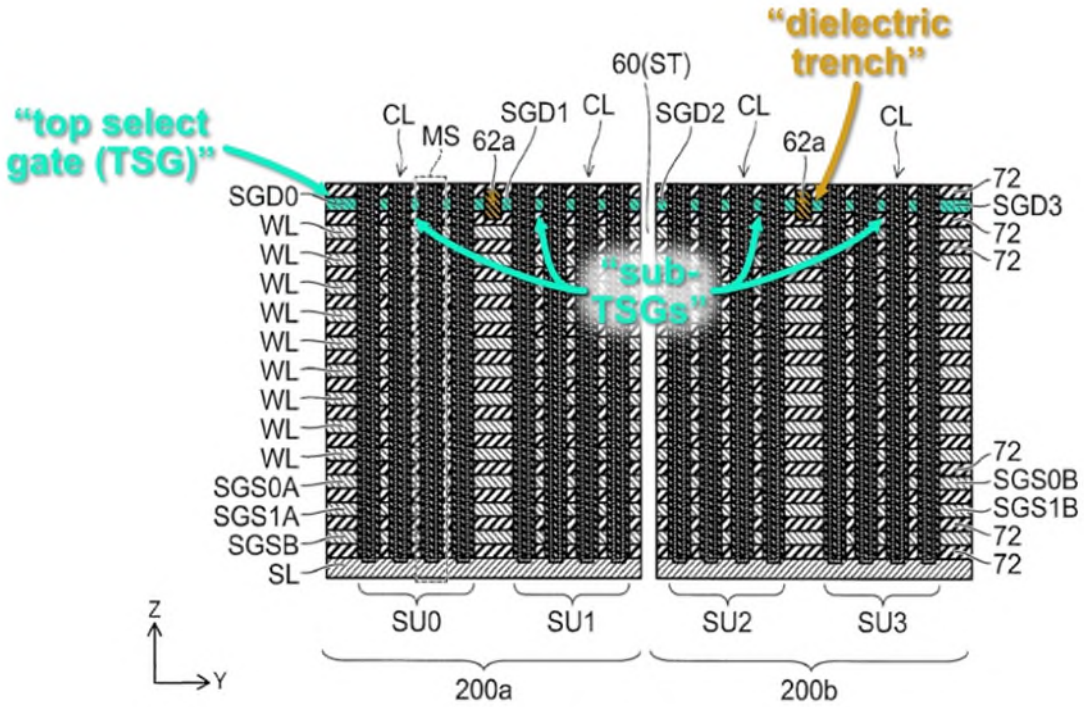
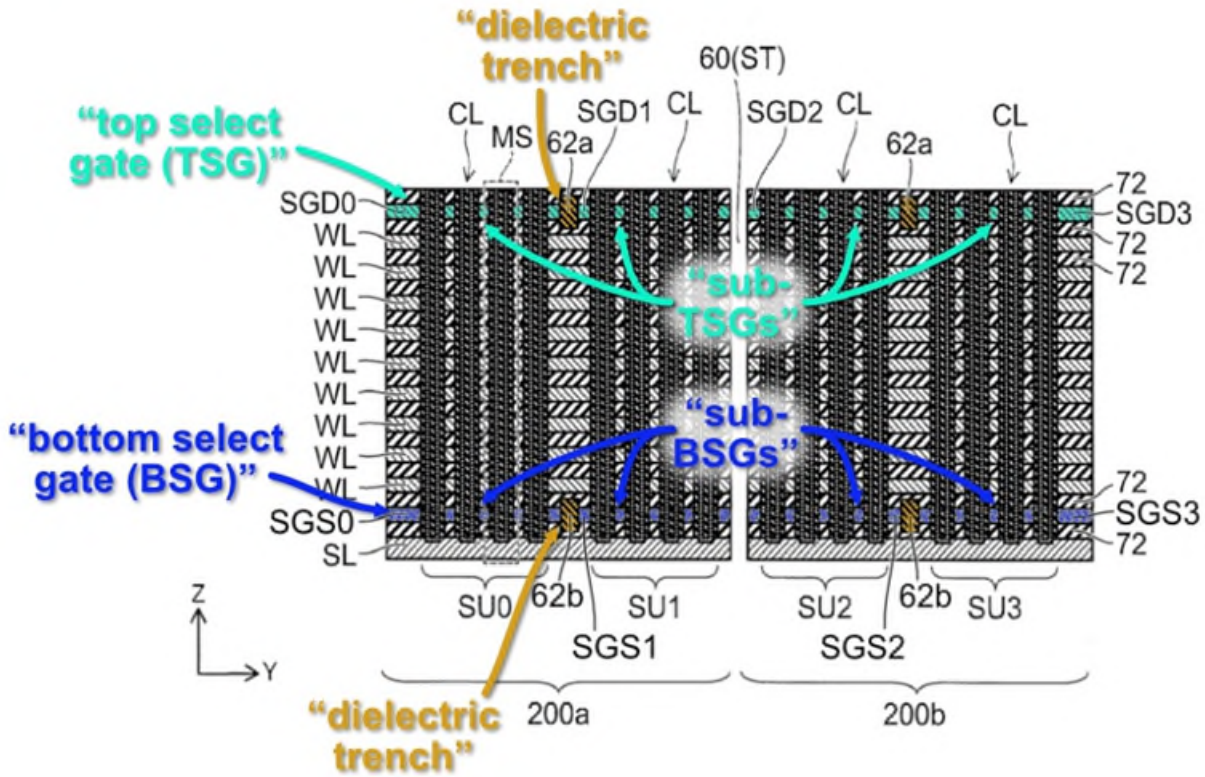


FIG. 16



Paper 1 (Petition) at 75-76.

Patent Owner Fails to Address What the Petition Actually Argued

Patent Owner's Erroneous Positions:

- ❌ The combination does not teach what the claims require because Park includes only "short structures in the staircase region."
- ❌ "[N]either Petitioner nor its expert explain how park achieves a reduction in manufacturing steps."

Paper 12 (Response), 72-74.

Patent Owner Is Incorrect:

- Patent Owner improperly addresses the prior art separately instead of in combination.
- Patent Owner ignores the primary benefit of the combination: increased memory density.

Paper 14 (Reply), 23-25.

Increasing the Number of Memory Cell Layers Indisputably Improves Shibata's Memory Device

In order to reduce bit cost in 3D NAND cell, it is very important to increase the number of stacked cells. In Section 8.7, serious problems of high aspect ratio process

Figure 8.4 shows the scaling trend of effective memory cell size in 16 stacked 3D NAND memory cells in comparison with 2D planar FG (P-FG) cells. It can be seen that 3D NAND memory cells cannot be effectively scaled down as feature size is scaled down, in comparison with P-FG MLC (planar FG MLC cells). It means that the increasing number of stacked cells is the only reasonable way to reduce the effective memory cell size in 3D cells.

The basic idea behind 3D NAND is to "grow" cells in the vertical dimension, thus reaching a higher density per area. The necessity stems from the fact that 2D NAND has reached lithographic limitations and no further shrinks are possible. Differently to building a house, where each floor

To reduce the bit size, the number of stacked cells needs to go up, but this causes a bunch of problems hard to solve, as shown in Fig. 5.28 [6].

Pillar's *Aspect Ratio* (AR) is definitely the first challenge to overcome; in a stack of 32 cells AR can already be as high as 30. In this context, hole etching and gate patterning are extremely difficult, but of paramount importance.

A possible solution to this problem is to divide the stacking process in more steps to reduce the corresponding AR. For example, a NAND string made of 128

Ex 1006 (Aritome), 355, 357; Ex. 1007 (Micheloni), 2; Ex 1012 (Micheloni II), 139; see also Paper 1 (Petition) at 76-77.