

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00794
Patent 10,950,623 B2

Record of Oral Hearing
Held: July 30, 2025

Before JO-ANNE M. KOKOSKI, KIMBERLY MCGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

IPR2024-00794
Patent 10,950,623 B2

APPEARANCES:

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The above-entitled matter came on for hearing on Wednesday, July 30, 2025, commencing at 1:00 p.m., at the U.S. Patent and Trademark Office, 600 Dulany Street, Alexandria, Virginia.

P R O C E E D I N G S

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JUDGE CYGAN: Good afternoon, this is Judge Cygan. Judges McGraw and Kokoski are present. Judge McGraw, are you able to hear us? We will now hear argument in Case number IPR2024-00794. This is U.S. Patent 10,950,623, between Petitioner Micron Technology and Patent Owner Yangtze Memory Technologies. Counsel for parties, starting with Petitioner, please introduce yourself.

MR. HERMAN: Good morning, Your Honors. This is Patrick Herman from Orrick, Herrington & Sutcliffe, here on behalf of Petitioner. With me are Jason Lang, also from Orrick, Petitioner's backup Counsel, and Kasper Larsen, the representative from Micron.

JUDGE CYGAN: And will you be doing the entire presentation?

MR. HERMAN: I will, Your Honor.

JUDGE CYGAN: Patent Owner?

MR. RADSCH: Good afternoon, Your Honors. Andrew Radsch from Ropes & Gray. I'm joined with me at the Counsel's table by Allen Cross, also from Ropes & Gray. We will be dividing the argument today for Patent Owner. Just want to note that Mr. Cross does qualify for the LEAP program. We've not put in a request for any extra time, but I thought it would be helpful just to note that.

JUDGE CYGAN: Okay.

MR. RADSCH: And then I'm joined by Jim Davis, Raj Chakraborty, also of Ropes & Gray, and by Daniel Chang from Yangtze Memory.

JUDGE CYGAN: Thank you, and welcome to the Board. Per our

1 hearing order, each party is provided with 60 minutes for oral argument.
2 The parties need not use the entirety of that time. Petitioner will argue first
3 and reserve time for rebuttal. Patent Owner will respond to Petitioner's
4 argument and may reserve time for a surrebuttal.

5 We have the demonstrations from each party. Please remember to
6 identify yourself when speaking. Please also identify the slide number when
7 you change slides so that we can follow along. And please mute yourself
8 when not speaking. Petitioner, how much time would you like to reserve for
9 rebuttal?

10 MR. HERMAN: Fifteen minutes, Your Honor.

11 JUDGE CYGAN: Fifteen minutes, okay. And you may begin.

12 MR. HERMAN: Good afternoon, Your Honors. We're here today
13 to talk about the '623 patent. Before addressing the parties' disputes, I'll
14 provide a very brief introduction to the patent and the prior art for context.

15 As shown on Slide 2 of Petitioner's demonstratives, the '623 patent
16 is generally directed to a 3D NAND memory device with a divided block
17 structure. According to the patent, the memory's blocks are each divided
18 into a plurality of sub-blocks. How is that done? By dividing the bottom
19 select gate, what the patent calls a BSG, into sub-BSGs, using what the
20 patent calls dielectric trenches.

21 Slide 3 shows Claim 1, the patent's only independent claim. The
22 claim is directed to a memory device. That memory device includes a
23 substrate. A bottom select gate is located above that substrate. This is
24 followed by a stack of word lines and insulating layers. Per the claims,
25 those layers must have a staircase configuration. Next, the claim specifies
26 that there are dielectric trenches formed in the BSG to separate the BSG into

1 a plurality of sub-BSGs. Finally, there are one or more common source
2 regions that pass through all the layers.

3 The claim also requires that the dielectric trenches and common
4 source region extend in the same length direction of the substrate. Slide 4
5 provides a graphical example. Figure 1A of the '623 patent is a cross-
6 sectional view. As shown, the bottom select gate, which is annotated blue,
7 and is very small in the figure, is divided into pieces by an orange dielectric
8 trench.

9 A common source region, which is shown in purple, passes
10 through all the layers from top to bottom and contacts the yellow substrate.
11 Figure 1B provides a top-down view. And as that figure shows, the trenches
12 extend in the same direction as the common source region.

13 So turning to Slide 6, this slide provides a summary of the grounds.
14 The petition relied on only two references, a reference to Park and a
15 reference to Shibata. Slide 7 provides a very brief overview of Park. Park,
16 just like the '623 patent, is directed to a 3D memory device. And Park also
17 divides its memory into individually controllable sub-blocks, which it calls
18 unit areas. How does it do that? As explained in the last highlighted
19 passage on the slide here, by interposing common source lines 102 and 105,
20 and isolation-insulation layers 111 between the unit areas to divide Park's
21 BSG, which Park calls a ground select line.

22 Turning to Slide 8, this slide includes annotated versions of
23 Figures 11 and 3 from Park. Figure 11 provides a cross-sectional view. As
24 shown, Park's bottom select gate, or ground select line, that's again annotated
25 in blue, is divided by orange isolation-insulating layers 111. Purple common
26 source lines pass through all the layers.

Figure 3 provides a top-down view. Here, the isolation-insulating layers 111 are shown to have a length and extend in the same direction as the purple common source lines. Turning to Slide 9, Shibata also relates to a 3D memory device. And like Park, it employs a separation portion 62 formed from insulation to divide a select gate layer, in particular Shibata's drain or top-side select gate, into pieces corresponding to different memory sub-blocks.

Slide 10 includes two figures from Shibata, Figures 16 and 47. Figure 16's cross-sectional view shows the insulation separation portion 62, located within and dividing Shibata's top select gate, which is highlighted in teal or light blue. Figure 47's top-down view shows the separation portions, again those are in orange, extending in the same direction as Shibata's common source, which it calls and labels as separation portion 60 in the figure.

So turning on to Slide 12, the parties have a number of disputes, spanning the petition's three grounds. I've listed them out here on the slide and will address each of them in turn. So moving to Slide 14, I'll start with Patent Owner's argument that Park's isolation-insulating layers 111 do not qualify as the claimed dielectric trenches. This argument is entirely premised on two erroneous claim constructions.

First, Patent Owner argues that Claim 1 is a product-by-process claim that requires the use of a particular manufacturing method. Second, Patent Owner argues that the dielectric trenches in the claims must separate the BSG entirely on their own. Both of these constructions are wrong.

So turning to Slide 15, Claim 1 is not a product-by-process claim. It's directed to a memory device, not a manufacturing method. So all that

1 matters is how the device is structured. Patent Owner hinges his arguments
2 on the words formed in in Claim 1. According to Patent Owner, “formed in”
3 means that the dielectric trenches need to be manufactured directly in the
4 BSG. And that's referred to in the party's briefing as a gate-first process.

5 And those trenches cannot, according to Patent Owner, be
6 manufactured in a sacrificial layer that is later replaced with conductive
7 material to become the BSG. And that's referred to as a gate-last process in
8 the party's briefing.

9 Respectfully, that isn't what “formed in” means in this apparatus
10 claim. “Formed in” in Claim 1 is simply referring to where the dielectric
11 trench is located. It must be located, present, or formed in the BSG. How it
12 got there is irrelevant for purposes of the claims. All that matters for
13 purposes of the claims is that the dielectric trench is in the BSG. In fact, the
14 entire dielectric trench limitation lists structural features. The trench must
15 be located in the BSG and extend in a particular direction. That's talking
16 about the physical characteristics of the trench, not how it's made.

17 Turning to Slide 16, this is also how the '623 patent's specification
18 uses the phrase formed in. You can see an example of that on this slide.
19 The passage on the right of the slide is discussing Figure 1A. What is Figure
20 1A? It depicts a complete and already manufactured memory device. And
21 what does the patent say about Figure 1A? It says that the figure shows
22 trenches 27 and 28 that are formed in one or more of the BSGs.

23 This isn't referring to how the trenches are manufactured. Instead,
24 the passage is using formed in to describe the location of the trenches as
25 depicted in the already manufactured and complete memory device of Figure
26 1A. Again, this is how the claim also uses the phrase “formed in” to refer to

1 the location of the claimed dielectric trenches in an already manufactured
2 memory device.

3 Next, even if one were to assume that Claim 1 is a product-by-
4 process claim and “formed in” refers to a specific method of manufacturing,
5 that still would not matter for purposes of the prior art. That is because the
6 Federal Circuit has repeatedly held that process limitations in an apparatus
7 claim do not constitute limitations with respect to the prior art in almost all
8 cases. In fact, process limitations will only matter if the process imparts
9 structural and functional differences to the end products. And it does not
10 here.

11 So turning to Slide 17, the specification references two different
12 manufacturing methods. A gate-first method, which I referred to earlier, and
13 a gate-last method. And according to the '623 patent specification, these two
14 methods result in the very same memory device that's shown in Figure 1A.

15 So the patent itself admits that regardless of whether one
16 manufactures the trenches in the BSG itself or manufactures the trenches in
17 a sacrificial layer that is later replaced with conductive material to become
18 the BSG, the very same end memory device is what's produced, what's
19 shown in Figure 1A. According to the patent, the process makes no
20 difference.

21 Indeed, Patent Owner's expert Dr. Kuhn admitted the same thing
22 during her deposition, as shown on Petitioner's Slide 18. According to Dr.
23 Kuhn, Figure 1A, that's the figure that shows an example of the patent's
24 memory device, is exemplary of both the patent's gate-first and gate-last
25 manufacturing methods.

26 The two processes produce the same memory device. There are

1 not two different figures showing two different memory devices that result
2 depending upon which manufacturing process is used. The same device
3 results regardless of the process.

4 Now, according to the Patent Owner, Patent Owner argues that a
5 memory formed using the gate-first method will be different from one
6 formed using a gate-last method. And Patent Owner says that, because in its
7 view, different conductive materials can purportedly be used for the gate
8 layers, depending upon whether a gate-first or gate-last manufacturing
9 method is employed.

10 It argues in its briefing that a gate-first method can use polysilicon,
11 while a gate-last method uses a high K dielectric and a metal. There are
12 multiple problems with this. First, Patent Owner is now reading not only a
13 process limitation, but also a BSG material limitation into the claims. The
14 claims here, however, simply refer to the BSG. They say nothing about the
15 process that's used to make the BSG or the trench that's within it. And they
16 also do not require the use of any particular conductive material.

17 Second, the '623 patent specification never even mentions or states
18 anywhere that its gate and word line layers can be made from polysilicon.
19 The specification only mentions the use of a high K and metal material to
20 make the bottom select gate. That's the only material that's identified for use
21 at all in connection with the gate layers. So Patent Owner is pointing to
22 completely different prior art, separate and apart from the '623 patent, that
23 discuss the use of polysilicon for gate layers.

24 So what Patent Owner is trying to do is it's trying to graft a
25 limitation into the claims requiring the use of a specific gate material that is
26 not even called out by the '623 patent itself. Petitioner submits that there's

1 no basis in either the claims or the specification to limit the claims this way.

2 So turning to Slide 19, another problem with Patent Owner's
3 construction is that it reads out one of the '623 patent's embodiments. The
4 '623 patent explains again and again that the memory device shown in its
5 figures can be manufactured using a gate-last method. Given that there's
6 nothing in the claims that requires a specific manufacturing method, there is
7 no reason to exclude this embodiment. That, however, is exactly what
8 Patent Owner is proposing.

9 So now I'll turn to the other claim construction disputes. So as
10 shown on Slide 20 -- well, so turning to Slide 20, Patent Owner is also
11 wrong that the claims exclude trenches like those in Park that do not extend
12 the full length of the substrate. As shown on this slide, this is an issue that
13 the Board already addressed in its institution decision. The Board found that
14 the claims only require that the trenches cause the BSG to be separated into
15 sub-BSG, and they may cooperate with other structure when performing that
16 function.

17 Petitioner submits that that preliminary finding was correct.
18 Nothing has changed that would require a different decision. So first, the
19 claims simply require trenches that are one, located in the BSG, two, extend
20 in the length direction of the substrate, so the same direction as the common
21 source region, and they must cause the BSG to be divided into sub-BSG.

22 There are no further requirements. There are no requirements
23 about how long the trenches need to be, there are no requirements that
24 prevent other structure from cooperating in that separation function. So
25 Patent Owner is once again reading limitations into the claims.

26 So the specification also does not require Patent Owner's limiting

1 construction. Yes, there are figures in the '623 patent specification that
2 provide examples of trenches that span the whole memory from end to end,
3 but the specification repeatedly says that those depicted trenches are just
4 examples.

5 So turning to Slide 21, the specification also explains what the
6 trenches are intended to do. In particular, the specification states that
7 without the introduction of the trenches, the memory would have a shared
8 BSG. So, again, the key feature of the '623 patent's trenches are number
9 one, they must be located in the BSG, and two, their presence, or their
10 introduction into the structure, results in the BSG being separated. And
11 that's exactly what Park's isolation-insulating layers 111 do.

12 If those isolation-insulating layer 111 were not present in Park,
13 Park would have a shared BSG. But because those isolation-insulating
14 layers are present, and they are located in the BSG, and they have a length
15 that extends in the same direction as the common source region, Park instead
16 has separate BSGs that are not electrically connected to each other.

17 So turning on to Slide 22. In the '623 patent, the trenches also
18 cooperate with each other, with other structure to divide the BSG. So Slide
19 22 includes a passage from column 9 of the '623 patent. Here, the '623
20 patent explains that while its figures show only a single memory block, there
21 may be additional memory blocks adjacent to, so either above or below, the
22 block that's depicted in the figure.

23 And if there are such adjacent blocks, the specification says that
24 the common source regions 52B and 52C, those are the common source
25 regions at the boundary of the depicted block, operate to separate the
26 depicted block from adjacent structure.

1 So you can see that in the annotation, the annotated version of
2 Figure 1B on the slide here. One sub-block is highlighted in blue, and that
3 one sub-block will have its own sub-BSG. And that sub-block is separated
4 from the sub-block located above it by an orange dielectric trench, but it's
5 separated on this other side from adjacent structure by a purple common
6 source region. So both a trench and a common source region, the trench is
7 on one side and the common source region is on the other, are used to
8 separate the sub-block and its associated sub-BSG from adjoining memory
9 structure.

10 Thus, Petitioner submits that the '623 patent's claims cannot be
11 construed to require that it be trenches alone that affect the separation of the
12 BSG into sub-BSG, because even the '623 patent does not do exactly that.

13 JUDGE CYGAN: Counselor, I have a question on that. Doesn't
14 the claim require that the trenches separate the BSG into plurality of BSGs?
15 And isn't this more separating sub-BSGs from each other or separating
16 BSGs from each other? What's your thought on how that separates a BSG
17 into sub-BSGs?

18 MR. HERMAN: So Your Honor is correct that the claim requires
19 dividing the BSG into sub-BSGs, but I believe the fact remains that that sub-
20 BSG would not exist as an independent structure unless the boundaries on
21 both sides are there, right? So for that sub-BSG to exist, the orange trench
22 on the top of the figure needs to be there, and the purple common source on
23 the bottom needs to be there, because that sub-BSG would be joined to the
24 adjacent block if that common source region wasn't there.

25 So both of those structures are fundamental to the existence of that
26 particular sub-BSG that's shown in the example figure here. But Your

1 Honor is correct that the claim requires dividing a BSG into multiple sub-
2 BSGs.

3 JUDGE CYGAN: And is your argument that the common source
4 region, at the edge of the BSG, itself performs the separation, or it assists the
5 dielectric trench in performing its separation?

6 MR. HERMAN: It does not do the separation itself, it assists. So,
7 again, both of those structures that are shown in this figure are together
8 cooperating to form the blue sub-BSG that's shown there. If either was
9 missing, that blue structure would not be present in its current form. Both of
10 them work together to make it exist.

11 JUDGE CYGAN: Okay. Thank you.

12 MR. HERMAN: So unless there are further questions on those
13 claim construction issues, I'll move on to the party's next dispute. So turning
14 to Slide 24, the petition explained that it also would have been obvious to
15 include trenches in both Park's bottom and top select gate layers. And an
16 example of such a modification is shown on the right side of the slide here.

17 So the left side of the slide includes Figure 36 from Park in its
18 current form. The right side of the slide shows a modified version of Figure
19 36 that includes trenches not only in the bottom select gate layer, but in the
20 top select gate layers that are shown immediately above that layer in Figure
21 36.

22 So turning now to Slide 25, Patent Owner does not dispute that a
23 POSITA would have had good reason to divide Park's top select gate layers
24 in the same way as the bottom select gate layers if those two layers are, in
25 fact, located over top of each other. Instead, as summarized on Slide 25, the
26 only argument that it makes is that, in Patent Owner's view, Park includes

1 what Patent Owner calls an error and mistakenly shows all of the layers as
2 being present over the divided portion of its BSG in certain of its figures.

3 Petitioner submits that there is no error in Park. Instead, Park
4 teaches different device configurations that are entirely consistent with what
5 is shown in later figures, like Figure 36.

6 So turning to Slide 26, what Patent Owner asked the Board to do is
7 find that, not just one figure, but five separate figures in Park are all drawn
8 in error. In every single figure that's shown on this slide, the top select gate
9 layers, or the sacrificial layers that will eventually turn into the top select
10 gates, or the openings that will eventually be filled with gate conductive
11 material, are shown over Park's dielectric trenches.

12 So for reference, I've highlighted the trenches in orange in the
13 lower level on the slide and the places where those top select gate layers will
14 go or already are present are shown in teal. So given that Park's memory
15 device is repeatedly depicted this way, it is not reasonable to assume, as
16 Patent Owner and his expert do, that every single one of these figures is
17 wrong and drawn in error. Park is plainly contemplating structures where
18 the top select gate is located over the portion of the bottom select gate with
19 the trench. Otherwise, it would not have shown that repeatedly in its figure.

20 And, again, Patent Owner does not contest that if there is a top
21 select gate over the trench, then it would have been obvious to include a
22 matching trench in the top select gate layer.

23 So next, turning to Slide 27, not only does Park depict top select
24 gate over its dielectric trenches in its figures, but it explains in text that those
25 figures are meant to show those top select gate layers. As seen on Slide 27,
26 Park is discussing Figure 34 and the figures that follow, including Figure 36.

1 And what does Park say? It explains that two of the depicted gate lines in
2 this figure are meant to be string select lines.

3 Park does not say that those string select lines are not shown in the
4 figure. It does not include any other similar language. Instead, Park
5 references and confirms that the layers are meant to be depicted in Figures
6 34, 35, and 36. So Patent Owner is asking the Board to find not only that
7 Park drew its figures wrong and in error, but also that it described what is
8 shown in those figures incorrectly. Once again, there's no reason to reach
9 such a finding. The prior art says what it says.

10 Now, why does Patent Owner believe that Figure 36 in Park
11 includes an error? So Slide 28 includes Figure 27 from Park. So this figure
12 is an example cross-section of Park's memory. In this figure, the top two
13 select gate layers are shown as not being located directly over the trench,
14 which is labeled 311 in this particular figure. So Patent Owner then argues
15 that all of Park's embodiments must look and be arranged exactly like this.

16 So Figure 27 imposes no such global limitation on Park. As noted
17 in the text to the right, this figure's primary purpose is to show insulating
18 layer 370, that's Park's field insulation, the large amount of insulation to the
19 right of the figure, and Park's channel and dummy channel structures. Those
20 are labeled CH and DCH in the figure.

21 So turning to Slide 29, rather than saying that all of its
22 embodiments must look exactly like Figure 27, Park in fact says the
23 opposite. So Park explains again and again that its memory can be modified.
24 You can see that in the passage from column 18 at the top of the slide. It
25 also repeatedly says, for instance, that column 2, line 43, and column 3, line
26 24, that its figures are meant to just be examples. And what are ways that its

1 figures can be modified or changed?

2 As shown in the bottom left, Park explains that interconnection
3 with its gate layers can be made in different ways. The connections can be
4 made on steps that all extend out in the x-direction, or they could be made
5 via steps that are in a different direction, resulting in differently shaped gate
6 layers. And as shown to the bottom right, the trenches can also be located at
7 different places in the x-direction in Park's memory.

8 So this means, Petitioner submits, that there's nothing inconsistent
9 with Figure 27, which shows the top two layers that are not located over the
10 trenches, and Figure 36, which does show that the top two select gate layers
11 are located over the trenches. Figure 36 simply shows, for instance, a trench
12 that has an x-direction location that puts it under the string select lines that
13 are shown in Figure 36. So in sum, there's no error in Park, Park just
14 broadly teaches a variety of memory devices with different layer and trench
15 configurations.

16 So the parties also dispute Park's teachings regarding Claims 10
17 and 11. So I'll turn to Slide 31 for that. Claims 10 and 11 required trenches
18 that pass through both the select gates and an adjacent dummy layer. So
19 according to the Patent Owner, the petition purportedly did not explain how
20 or why this would be done in Park, and Petitioner submits that that's simply
21 not the case.

22 So turning to Slide 32, the petition pointed to example dielectric
23 layers in the prior art that pass through just one layer, like what Park does,
24 that passes through all the layers of a memory. There's examples of that in
25 Shibata. Or as the example that's shown on the slide here depicts, there are
26 examples in the prior art of trenches that pass through two adjacent layers of

1 a memory.

2 In Park, the dummy layers are immediately adjacent to the select
3 gate layers and will be divided by this type of known dielectric trench that
4 passes through multiple layers of the gate electrodes.

5 So next, turning to Slide 33, the petition also explained why it
6 would be best to divide both the select gate and adjacent dummy layers. In
7 particular, the record here, and in particular Petitioner's expert, Dr. Lee,
8 explains that the dummies are meant to avoid signal issues along the
9 memory string. So Petitioner's expert, Dr. Lee, citing both texts and patents
10 discussing memory operation, explained that dividing the dummies in the
11 same way as adjacent select gate layers would allow them to better serve this
12 signal issue avoidance function.

13 So finally there's also no dispute that a person having ordinary skill
14 in the art would have known exactly how to form a trench that goes through
15 both a dummy layer and a select gate layer. The petition explained that this
16 would be accomplished by a timed etch. And as shown on Slide 34, not only
17 does Park itself already use time etches, at least when forming its contact
18 pads, that's what's shown in the passage on the left side of the slide.

19 But Patent Owner's expert also admitted, as shown on the right
20 side of the slide, that this type of timed etch was well known and in routine
21 use in the memory art. So unless there are further questions, I'll move on to
22 Petitioner's next ground, that's Ground 2.

23 As shown on Slide 36, in the event the Board agrees with Patent
24 Owner's construction of dielectric trench in a way that requires the trench to
25 extend the full length of the memory, Ground 2 of the petition explained that
26 it would have been obvious to modify Park to include longer trenches,

1 following Shibata's teachings. Now, Shibata explains that using more longer
2 trenches and fewer common source regions to divide the memory, as shown
3 by the demonstrative on the right-hand side of the slide, leaves more room
4 for memory cells.

5 So turning to Slide 37, Patent Owner argues that Park actively
6 discourages longer trenches. It also argues that Shibata provides no solution
7 to Park's purported concerns, and finally it argues that one cannot reduce the
8 number of common source regions in Park without negatively impacting the
9 operation of the memory. And Petitioner submits that none of these
10 arguments find support in the record.

11 Turning to Slide 38, I'll begin with the contention that Park
12 discourages longer trenches. According to Patent Owner, Park requires the
13 use of only short, staggered trenches because anything more could
14 purportedly cause problems when etching away sacrificial layers during
15 manufacture.

16 JUDGE CYGAN: Mr. Herman, can I ask you a question?

17 MR. HERMAN: Yes.

18 JUDGE CYGAN: In your combination, you're adding Shibata to
19 replace some of the common source regions?

20 MR. HERMAN: That's right.

21 JUDGE CYGAN: You're not extending the dielectric trench.
22 You're keeping the same dielectric trenches from Park, and you're replacing
23 the other common source regions with, basically, Shibata's dielectric
24 trenches, correct?

25 MR. HERMAN: So I'll turn back to explain that, to Petitioner's
26 Slide 36. So you'll see in this slide that we have kept some of Park's existing

1 isolation-insulation layers in one of the alternate modifications that we
2 proposed. So there are two of those shorter trenches, as you can see, that
3 remain behind in this particular version of the combination. But then others,
4 three of those shorter trenches, have been elongated by replacing those
5 particular common source regions with simply a longer trench.

6 So it's kind of a combination of both, what Park originally started
7 with, the shorter trenches, and what Shibata discloses, which is longer
8 trenches. So some of Park's shorter trenches can remain in this particular
9 implementation of the combination, while others of those shorter trenches
10 have been elongated and replaced with what Shibata teaches.

11 JUDGE CYGAN: In this combination, it's only the longer
12 trenches that are being read on the claim?

13 MR. HERMAN: Yes, Your Honor.

14 JUDGE MCGRAW: If I could ask a question. This is Judge
15 McGraw. How long of a length is required for the dielectric trench to have
16 before it separates the BSGs? Is there at least a minimal length that it would
17 need to have?

18 MR. HERMAN: So Petitioner's view is that there is no minimum
19 length as long as the claim is satisfied. So as long as the trench extends in
20 the same direction as the common source region, then the trench has -- and
21 performs the function the claim requires, right? It affects separation of the
22 BSG and the sub-BSG, then the claim would be satisfied. There is no
23 quantum or numerical limitation. So the trench could be a millimeter, it
24 could be ten millimeters. As long as it's extending in the right direction and
25 performs the right function, that's all that's required.

26 So this particular ground is assuming that Patent Owner is correct

1 and that the trench needs to extend the entire length, so from one side to the
2 other of the substrate. And it's Petitioner's view that that's not required, that
3 the trench can extend a shorter distance. So I will say that the trench cannot
4 be wider than it's long, because the trench is required to extend in the length
5 direction.

6 So a trench that essentially is short and very thick would not
7 qualify, because perhaps it would be extending in a different direction than
8 the common source region. But as long as the trench is long enough, such
9 that it extends in the same direction as the common source region, so it has a
10 length that's pointing in the correct direction, it's Petitioner's view that the
11 claim is satisfied. Does that answer Your Honor's question?

12 JUDGE MCGRAW: Yes, thank you.

13 MR. HERMAN: So turning back to Slide 38. So according to the
14 Patent Owner, Park requires the use of short staggered trenches because
15 anything more could purportedly cause problems when etching away
16 sacrificial layers during manufacture. But that's not the case. Park also
17 teaches that its memory can be designed with longer non staggered trenches,
18 and you can see that on Figure 17 of the slide here.

19 So how does Park accommodate those longer, not staggered
20 trenches? By temporarily including features 209A and 209 that allow for
21 better etchant flow around now longer trenches. Those are effectively holes
22 that are present during manufacture to allow etchant flow that are later filled
23 with insulation. So while they're present during manufacture, you will not
24 see them in the final device. Their sole purpose is to allow for non-
25 staggered, longer trenches.

26 So turning to Slide 39, Petitioner also explained how in one of its

1 modified versions of Park, etchant and conductive material are able to flow
2 virtually everywhere for purposes of removing the sacrificial layers, and
3 then flowing in the conductive materials to form the gate layers. And you
4 can see that flow with the red arrows on Slide 39, which surround everything
5 except the small original trenches 111 that remain in place in this modified
6 version of Figure 3.

7 And as we saw in the last slide, any etchant flow problems in those
8 areas are already addressed in Park with features like 209A and 209. So
9 next, as shown on Slide 40, Shibata provides yet another solution to the
10 problem that Patent Owner says Park is raising. As shown in Figure 47A of
11 Shibata, which is in the lower left corner of the slide, Shibata includes
12 multiple facing dielectric trenches, and there are no common source regions
13 between the trenches through which etchant can flow.

14 Again, this is not going to be a problem in Park because Park
15 includes features like 209 and 209A that do allow etchant to flow in these
16 areas, but Shibata says that even this particular configuration is not a
17 problem. According to Shibata, any conductive layer formation problems
18 that result from dielectric trenches that are structured and located in the way
19 shown in Figure 47A can be addressed by just including separate drive
20 circuits that are tailored to address the different resistances of the layers,
21 resulting from their manner of manufacture.

22 So Petitioner submits and explained in this petition, and in the
23 declaration of Dr. Lee, that given this, there is no reason why a person
24 having ordinary skill in the art would not do the same thing with Park if
25 there were some sort of layer formation problem.

26 So turning on to Slide 41. Patent Owner's argument that removing

1 common source regions creates a problem also finds no support in the prior
2 art. Indeed, as shown on this slide, Park itself contemplates memory with
3 both a greater number of common source regions, there's nine in Figure 3 on
4 the left-hand side of the slide, or a smaller number of common source
5 regions, there's only five in Figure 17 on the right-hand side of the slide.

6 Next, as shown on Slide 42, the art also explains that removing
7 common source regions is beneficial. According to Park, one of its goals is
8 to increase the capacity of its memory. You can see that on the left-hand
9 side. And as shown on the right-hand side of the slide, Shibata teaches that
10 using more dielectric trenches and fewer common source lines reduces the
11 overall size of the memory array, thus giving space for including more
12 memory cells.

13 So I'll conclude by addressing Ground 3, which modifies Shibata
14 in view of Park's teachings. So turning to Slide 44, Shibata divides its top
15 select gate with the dielectric trench. You can see that in Figure 16, to the
16 left. But rather than simply dividing its bottom select gate in the same way,
17 it uses, at least in its examples, multiple separate bottom select gates to allow
18 for control on a memory sub-block basis.

19 So the petition explained why it would have been obvious to
20 instead include trenches in the lower-level following Park's teachings, and
21 there's an example of how that would be done in the demonstrative on the
22 right-hand side of the slide.

23 So turning to Slide 45, Patent Owner responds by arguing that
24 Park's trenches are short, and thus do not satisfy the claims, and two, in its
25 view, employing Park would not simplify manufacturing. So the first
26 argument Petitioner submits improperly considers the prior art in isolation.

1 The petition did not argue that Park would be bodily grafted into Shibata.
2 Instead, it argued that Shibata's longer trenches, used in this upper select
3 gate layer, would be replicated in this lower layer. The second argument
4 addresses only one of the two reasons for combining the references.

5 Turning to Slide 46, as explained in the petition and as shown on
6 this slide, the primary reason for applying Park to Shibata is that it frees up
7 additional layers for use as word line layers. By using only a single bottom
8 select gate divided by trenches instead of multiple bottom select gates, there
9 could be more word line layers without increasing the overall height of the
10 memory. And as shown on this slide, this is particularly important and was
11 a goal the prior art was trying to achieve.

12 Again and again, the art explains that it is important to increase the
13 number of stacked cells in 3D NAND, to grow the memory in the vertical
14 direction, and to design the memory such that the number of stacked cells
15 goes up. So this is the primary benefit that Park's lower trenches provide,
16 and this, standing by itself, motivates application of Park to Shibata.

17 While the need to form fewer layers during manufacture also has
18 the potential to simplify things, this is just the secondary benefit. The
19 primary benefit is that the memory density is increased, and that is a goal
20 that virtually everyone in the prior art was trying to achieve. So the Patent
21 Owner does not dispute this. It did not even respond that this would
22 motivate the combination of Shibata and Park. Instead, it spends all its time
23 debating the number of manufacturing steps that are needed.

24 So Petitioner submits that the Board does not need to address this
25 particular manufacturing dispute, as the memory density increase discussed
26 in the petition and summarized in this slide here, standing alone, would

1 motivate combination.

2 JUDGE CYGAN: Counselor, can you explain a little bit how your
3 combination leads to an increase of the number of memory cells? Because
4 these references are not really talking about sub-BSGs. They're really
5 talking about moving from 2D to 3D, is that correct?

6 MR. HERMAN: So they're talking about moving from 2D to 3D,
7 but then also increasing the size of 3D memory for purposes of increasing its
8 degree of integration, or the amount of memory that fits in a particular space.
9 So they're talking about those two things.

10 And I can explain with reference to Slide 44. So as you see in
11 Slide 44, Figure 16 is Shibata's memory, and there are three bottom select
12 gate layers, which are labeled SGS0A, SGS1A, and SGSB. So three bottom
13 select gate layers. Now the way that that's been modified is by including
14 trenches in the bottom layer.

15 So instead of requiring three separate select gate layers to
16 effectuate individual sub-block control on the bottom, you can now get that
17 same control with just one divided layer, but you've eliminated two select
18 gate layers. But because those two select gate layers have been eliminated,
19 they can be replaced with word line layers without increasing the overall
20 height of the device. So you can have the same device height, just with two
21 extra word line layers. So by dividing the bottom layer with trenches,
22 you've now created more room for word line layers, which means more
23 room for memory cells.

24 JUDGE CYGAN: So it's the addition of the additional word line
25 layers, because you've removed --

26 MR. HERMAN: So essentially turning those two now unneeded

1 select gate layers into word line layers that can include memory cells.

2 JUDGE CYGAN: And this rationale only applies to Shibata in
3 view of Park, not Park in view of Shibata, correct?

4 MR. HERMAN: Yes, it's specific to that particular combination.

5 JUDGE CYGAN: Okay. Thank you.

6 MR. HERMAN: So if there are no further questions, I'll reserve
7 the remainder of my time for rebuttal.

8 JUDGE CYGAN: Okay. You have about two minutes left. I'll
9 give you 43 minutes, 17 minutes for rebuttal. Patent Owner, whenever
10 you're ready.

11 MR. RADSCH: Thank you, Your Honor.

12 JUDGE CYGAN: How much time did you want to reserve?

13 MR. RADSCH: Your Honor, if we could reserve 15 minutes for
14 rebuttal, please. Good afternoon, Your Honors. Again, my name is Andrew
15 Radsch for Patent Owner. I will be addressing the remarks today for Park,
16 the Ground 1, as well as the claim construction issues. And Mr. Cross, then,
17 will address the Ground 2 and Ground 3 issues, with respect to the proposed
18 combinations of Park and Shibata.

19 So to start with, Your Honors, I am on Patent Owner's slide
20 number -- you're going to see on the screen, it is Slide number 4. See if I
21 can make a full screen of this. This is on Slide 4 of the claim language, and
22 we've highlighted the two disputed limitations. First, dielectric trenches
23 formed in the BSG, and the second one, extending in a length direction of
24 the substrate to separate the BSG into a plurality of sub-BSGs. I'll start by
25 addressing those two claim construction issues.

26 So starting on Patent Owner's Slide 9, this is the term of dielectric

1 trenches formed in the BSG. And our construction -- Patent Owner's
2 construction, applies a plain meaning of formed in. “Formed” is a verb, and
3 Petitioner does not treat it as a verb. But formed refers to where something
4 is made, where something is manufactured. It is not simply a location.
5 Their construction reads out the word formed altogether and just deletes it
6 and reads the claim as referring to a dielectric trench in the BSG. That's not
7 what the claim language says.

8 They effectively treat the word formed as where something is
9 positioned in the device. If we go back to the claim language, when the
10 Patentee here wanted to refer to the position of something, as we see in
11 claim element 1C, it used the word positioned. That's a different word than
12 the word formed, but they're trying to treat them as synonymous. Formed is
13 a verb. It has to be given meaning as a verb. It refers to a process step. The
14 dielectric layer, or trench, rather, has to be formed in the BSG. If it's formed
15 in something else, it's not formed in the BSG.

16 Petitioner's Counsel said that formed is effectively a synonym for
17 located in or present in. That gives no meaning to the word formed, which,
18 again, is a verb, where something was made or created.

19 I am now on Patent Owner's Slide 10. That understanding of the
20 claim language is consistent with the intrinsic evidence. They are, as we
21 show in the top box here, so Petitioner argues that the claim term formed in
22 simply specifies where the dielectric trenches are located within the BSG
23 layer. So, again, they're treating the word formed as meaning within. Those
24 are not synonyms. They do not mean the same thing.

25 Now, they say that the specification describes formed as referring
26 to the location of something. That's simply incorrect. We show here on the

1 middle of Slide 10, this is with reference to the specification of the '623
2 patent, column 7, lines 17 to 20. It's referring to forming, consistent with the
3 claim language, forming the dielectric trench in the BSG. And the BSG has
4 already been formed.

5 JUDGE CYGAN: Counselor, can I ask you a question about some
6 of the language in column 7 of the '623 patent?

7 MR. RADSCH: Yes.

8 JUDGE CYGAN: If we take a look at lines, say, 1 through 7 of
9 the '623 patent, let me know when you're there.

10 MR. RADSCH: I am there, Your Honor, yes.

11 JUDGE CYGAN: It mentions that in the gate-last formation, the
12 BSG and other layers are formed firstly using sacrificial layers, and then the
13 sacrificial layers can be removed and replaced with the high K layer. So in
14 your reading, the formation is only that first part. So you wouldn't say that
15 the forming is sort of a two-part formation. You're saying the only
16 formation would be the sacrificial layers.

17 MR. RADSCH: I think, if I understand your question – so that
18 part of the specification is referring to the gate-last process?

19 JUDGE CYGAN: Right.

20 MR. RADSCH: Okay. And I think, at least there, it's using
21 formed in the same manner as we're arguing, which is formed means where
22 something is created. It means created, not located. And here, in their
23 argument, their reading of formed in would allow the dielectric trench to be
24 formed in a different substance, a sacrificial layer, that later becomes the
25 BSG. But that's not what the claim language says.

26 JUDGE CYGAN: That's what I was trying to focus on, whether or

1 not their interpretation isn't proper because, in your view, because it's
2 basically taking two steps to form those trenches. So it's forming it in one
3 layer, and then the second layer is done, and one way to read it would be
4 that's the formation. There's two steps to form that trench in that layer. It
5 feels like there's almost sort of a two-step formation going on at the
6 beginning of column 7.

7 MR. RADSCH: I would say that the formation in the gate-last
8 process of the BSG is, in fact, a multiple-step process. You first have to
9 create the sacrificial layers. You build up the rest of the stack. You then
10 introduce your etchant, and then you introduce your, you know, your
11 conductive material. So there's actually a lot of steps until you actually have
12 a BSG, and they're trying to argue that you can have the dielectric trench
13 formed at the beginning of that before there is any BSG.

14 JUDGE CYGAN: Right. It's just the language at the top of
15 column 7 says the BSGs are formed, but they're formed by using the
16 sacrificial layer, which is not -- you don't get the actual BSG until the second
17 step of that.

18 MR. RADSCH: Correct.

19 JUDGE CYGAN: So you couldn't form the BSG by itself with
20 just using the sacrificial layer. The formed firstly there seems to include a
21 multi-step process.

22 MR. RADSCH: Correct. I agree with that, Your Honor. So as we
23 point out on Slide 11, right, the specification's use of the phrase formed in
24 the BSG references existing BSGs, not some other layer that's been formed
25 in the BSG. And as Dr. Kuhn's unrebutted testimony explained, the only
26 reference to the form in the BSG here is with respect to the gate-first

1 manufacturing flow, where you first create the BSG, you finish completing
2 it, you have a BSG there, and then you form your dielectric trench in the
3 BSG.

4 So as Petitioner notes, it is absolutely the case that the specification
5 refers both to gate-last processes, as we just saw in the specification we just
6 discussed, as well as gate-first. But it's undisputed, as you say in the last
7 bullet on Slide 12, that in the gate-last process, the dielectric trench is
8 formed in a sacrificial layer, not a BSG. That does not meet the claim
9 language. That's what Dr. Lee, their expert, admits to. That doesn't match
10 the claim language.

11 JUDGE MCGRAW: Excuse me, this is Judge McGraw. Could
12 you address the argument that even if the claim is a product-by-process
13 claim that patentability is based on the final product and not the method of
14 making that product?

15 MR. RADSCH: Yes, Your Honor. So turning to Patent Owner's
16 Slide 14, this claim is a product-by-process. It requires a particular step be
17 made, the formation of the dielectric trench in the BSG. The Federal Circuit
18 has held, in multiple cases, that if the process by which a product is made
19 imparts structural and functional differences, distinguishing the claimed
20 product from the prior art, then those differences are relevant as evidence of
21 no anticipation, this is important, although those differences are not
22 explicitly part of the claim.

23 So Petitioner had argued that we're trying to read in additional
24 unclaimed limitations by arguing that there's a difference in what results
25 from the claimed process than from the prior art. But as the Federal Circuit
26 has said, you don't have to claim those additional elements for it to be part of

1 the analysis you perform in determining if the product is different from the
2 prior art.

3 The other point I'd make that's important here is that it is Petitioner
4 that bears the burden here. They have put forth no argument or evidence
5 that the product that results from the claimed process in the '623 is the same
6 as the structure and function of the prior art we're talking about here, Park.
7 They have not met their burden of proof to show invalidity, because they've
8 not done that analysis.

9 The only argument they made is in their Patent Owner response,
10 where they said, with respect to Figure 1 of the '623 patent, it says that that
11 Figure 1 could result from either a gate-first process or a gate-last process.
12 But that's not the correct comparison. As the Federal Circuit has said,
13 comparisons between the product that results from what's claimed and the
14 prior art -- excuse me, did not perform that comparison with respect to
15 whether there are structural and functional differences.

16 So as a first matter, they have not met their burden. But going
17 beyond that, we have put in significant and substantial evidence that has
18 been unrebutted that there are resulting differences in the gate-first and gate-
19 last process. In particular, there are both structural and functional
20 differences. And therefore, that's a patentable distinction to have the product
21 made by the particular claimed process.

22 So on Slide 15 of Patent Owner's slides, and here we're talking
23 about both what the '623 patent describes and what the state of the art
24 describes. The gate-last process uses high K layers and metal layers to
25 replace those sacrificial layers to form its gates. So you have these gates
26 formed of metal and high K dielectrics. That is in contrast to the gate-first

1 process that uses polysilicon for its gates. And there are functional
2 differences that result as, you know, we cite here in Exhibit 1007, it says that
3 that gate-last process results in optimized CT operations and word line
4 resistance --

5 JUDGE CYGAN: Counselor, how do we know that the gate-first
6 uses polysilicon gates?

7 MR. RADSCH: In the '623 patent, Your Honor?

8 JUDGE CYGAN: Right.

9 MR. RADSCH: The purpose of why we've cited the evidence here
10 in Exhibits 1007 and 1012, is that it discusses how those processes are
11 performed. And so the gate-first process uses polysilicon for the layer stack,
12 and the gate-last process uses high K layers and metal.

13 JUDGE CYGAN: Is this dependent on the type of item that's
14 being used, or is it -- how do we know this is representative of what must
15 happen in the patent?

16 MR. RADSCH: In the '623 patent itself, well, again, it does
17 describe gate-first and gate-last, and it doesn't describe specifically what
18 etchants you use, for example, what fills you use. But this is precisely what
19 is discussed in the art that we cited, and this is actually Petitioner's own
20 evidence, that these are the differences between the gate-first and gate-last
21 process. And they result in functional differences, as this art states.

22 The gate-last process results in gates with lower word line,
23 parasitic resistance, and results in faster reading and programming and
24 reading operations. So you know from the art how the specific processes for
25 gate-first and gate-last are performed, and that they result in both functional
26 and structural differences. And again, I think that's a point that they've made

1 no showing, and it's their burden here as well.

2 JUDGE CYGAN: You're pointing on Slide 15, to the advantage of
3 the gate-last which is the high K layer, which is discussed in the '623 patent.
4 The polysilicon is what you're arguing from the prior art, one would
5 understand the '623 patent you have used instead of the high K layer. And
6 why do we know that the polysilicon doesn't have the advantages of the high
7 K layer?

8 MR. RADSCH: I would say, if you look at exactly what's said in
9 the exhibit cited on Slide number 15, about the advantages and differences
10 of what results from the gate-last process as compared to the gate-first
11 process. The gate-last process results in metal gates with better borderline
12 parasitic resistance, and that's as compared to the gate-first process. So
13 looking at the Exhibit 1012 on the bottom, it's comparing gate-first versus
14 gate-last.

15 JUDGE CYGAN: And does Exhibit 1012 talk about using
16 polysilicon?

17 MR. RADSCH: I don't believe it does specifically, it's referring to
18 generally the gate-first versus gate-last process. The Exhibit 1007 refers
19 specifically to the polysilicon.

20 JUDGE CYGAN: So the way we need to sort of weave your
21 argument is that '623 patent is silent on the material used for the gate-first --

22 VTC: Excuse me, Judge.

23 JUDGE CYGAN: Yes.

24 VTC: This is VTC. I lost Judge McGraw.

25 JUDGE CYGAN: Okay. We'll go off the record until she's --

26 (Whereupon, the above-entitled matter went off the record at 2:03

1 p.m. and resumed at 2:06 p.m.)

2 JUDGE CYGAN: We'll go back on the record now. I've added a
3 little more time on. I think we left off with me trying to summarize your
4 argument about the difference between the gate-first and gate-last materials.
5 So the '623 patent, it specifies one material for gates, but it doesn't specify
6 that that's used for gate-first in particular.

7 The Exhibit 1007 is used to show the gate-first is exclusively used
8 with polysilicon for the gate-first. And the Exhibit 1012 mentions that
9 polysilicon will have different properties, let's say, than the gate-last
10 manufacturing, which is done with high K dielectrics.

11 Is there anything you'd like to point to which sort of supports the
12 point that polysilicon is necessary for gate-first and we can't take from its
13 absence in the '623 patent that the high K is not supposed to be sort of the
14 default layer for gate-first and gate-last? So how do we understand that
15 gate-first is not sort of used with the high K dielectric material but it has to
16 be used with polysilicon and therefore have different properties?

17 MR. RADSCH: So I'd say a couple of things, Your Honor. First,
18 I'd start with, again, I'd focus on who has the burden here, and they have not
19 addressed this at all. So they've not met their initial burden. Moving past
20 that, I don't know if you have to reach the specific conclusion that the '623's
21 gate-first process uses polysilicon. I think what the '623 patent says with
22 respect to the use of high K layers and metal layers, it's described only with
23 respect to the specific gate-last formation embodiments.

24 And that description is consistent with the art, where it describes
25 using high Ks and metals only with respect to gate-last. So I think a
26 POSITA would understand that high Ks and these metal layers for the gates,

1 that's only used in the gate-last process. That's what the totality of this
2 evidence shows. And this evidence also shows that there are differences that
3 result from those two processes.

4 So I don't think you necessarily need to find that polysilicon
5 specifically has to be used for the gate-first process in the '623 patent to
6 determine that there are functional and structural differences between gate-
7 first and gate-last process. Because that's what the evidence shows. And
8 this evidence has not been rebutted or addressed by that side at all, by the
9 Petitioner.

10 So again, I don't think you have to conclude necessarily that the
11 '623 has to use polysilicon. But there's no suggestion that in the gate-first
12 process, either in '623 or anywhere else in the industry, uses high K layers
13 together with metal layers to form its gates.

14 JUDGE CYGAN: And if we go with, I think, that conclusion,
15 where it's not necessarily polysilicon, but we have one gate layer, which we
16 have one option which is the gate-last, and that would have the beneficial
17 properties that Exhibit 1012 discusses, the beneficial properties associated
18 with it in the prior art. And then we would have the second alternative
19 embodiment which is simply silent as to its properties.

20 And from that, if we were to go with it not being a necessity to be
21 polysilicon, but simply an option, which would be something different,
22 would that alone show that it has different properties?

23 MR. RADSCH: I believe it would, because as the art explains, the
24 gate-first process, and this is, for example, what that 1012 says, the gate-first
25 process has different results and different structure and different functional
26 properties than the gate-last process.

1 JUDGE CYGAN: Okay. Thank you.

2 MR. RADSCH: So let me then turn to -- if there's no more
3 questions on the form then, I'd like to turn to the next claim construction
4 issue, which is the one or more first dielectric trenches -- and I'm on Slide
5 17, extending in a length direction of the substrate to separate the BSG into a
6 plurality of sub-BSGs.

7 And one thing I'd like to focus on here is the words extending to
8 separate. The way that the Petitioner has explained the claim language and
9 argued it is all that's required is an extension and a separation. That's not
10 what the claim language says. And going back to the claim language, it's the
11 extending to separate. So the extension has to be that which separates the
12 BSG into a plurality of sub-BSGs. It's not just that there is an extension and
13 that there is some separation. The result of the extension has to be that the
14 BSG is separated into sub-BSGs.

15 So the plain and ordinary meaning of this term, as explained on
16 Slide 18, is that the length of the dielectric trench is what separates the BSG
17 into sub-BSGs. If there are other elements that perform that function, the
18 claim isn't met because then the extension of the dielectric trench is not
19 separating the BSG into sub-BSGs.

20 Here we see on Slide 19 what the patent illustrates. This is
21 showing the dielectric trenches in yellow. They extend all the way across
22 the BSG. And I think, Judge McGraw, you had a question about how much
23 is required for there to be separation. There has to be complete extension.
24 Otherwise, there is no separation. And we see this in particular with respect
25 to Slide 20.

26 Slide 20, we've color-coded Figure 1B from the '623 patent. And

1 as the '623 patent describes, this is at column 9, lines 41 to 45. There is in
2 this image only three sub-BSGs, sub-BSG1, sub-BSG2, and sub-BSG3.
3 And what you'll notice in the middle is that common source region in the
4 middle of what's been color-coded red, which is sub-BSG2, has a small H
5 cut through it. So that extends almost all the way across.

6 So it's a very small opening, but it does not form two separate sub-
7 BSGs. That is a single sub-BSG because it is an electrical communication.
8 And so you have to have an extension all the way across to separate a BSG
9 into sub-BSGs. And that is what our construction of the term requires, and
10 that's what's shown in the intrinsic evidence.

11 JUDGE CYGAN: And Counselor, in the patent, neither one of the
12 trenches by itself meets your definition of extending, but together they
13 extend the full length. Is that correct?

14 MR. RADSCH: No, Your Honor. Each of the trenches shown
15 here extends the full length in the length direction. The first trench in yellow
16 extends the full length in the length direction. The second one does as well.

17 JUDGE CYGAN: Can we take a look at -- that's Figure 1B. Can
18 Figure 1B -- so you're discussing trench 26, correct? For example.

19 MR. RADSCH: Yes, 26 and 28 are the dielectric trenches that
20 separate the BSG into sub-BSGs.

21 JUDGE CYGAN: Okay. And the BSG only extends from what
22 length?

23 MR. RADSCH: The BSG is shown from the left-hand side to the
24 right-hand side of this image, as is the trenches. So if you circled in yellow
25 there, it extends all the way to the left of the image and all the way to the
26 right of the image. That trench extends all the way across. Otherwise, there

1 would be communication between those sub-BSGs and they would no
2 longer be a sub-BSG. That's what's shown in the red part. If there's any
3 connection, you do not have a sub-BSG.

4 JUDGE CYGAN: In the description, it mentions first trenches 26
5 and 28, and second trenches 56 and 58. So what's second trench 56?

6 MR. RADSCH: Could you point me to the column or the line of
7 the specification that you are referring to?

8 JUDGE CYGAN: Sure. It's column 8, line 1.

9 MR. RADSCH: Yeah, I'm just reviewing that portion of the
10 specification, Your Honor. So the portion of 56 and 58 that's shown there,
11 that separates the TSG, the top select gate. And the bottom select there, the
12 trench on the bottom extends the full width of that region as well.

13 JUDGE CYGAN: And so going back to Figure 1B, can you show
14 again where the BSG extends? It doesn't extend from the left to the right of
15 the figure. It only extends where 26 is. Is that correct?

16 MR. RADSCH: The bottom select gate extends across the same
17 width as the trench. They are co-equal width.

18 JUDGE CYGAN: And in this figure, the bottom select gate would
19 be 52a and 52b and 52c. Those are all the bottom select gates?

20 MR. RADSCH: The 52a, that is the common source region.

21 JUDGE CYGAN: Okay.

22 MR. RADSCH: The sub-BSG itself is the area that's labeled, for
23 example, sub-block 1, referred to as sub-BSG 1 there. It's annotated as sub-
24 BSG 1.

25 JUDGE CYGAN: Okay. I mean, that's part of my confusion. It
26 seems like there's two trenches, 26 and 56, that together are performing the

1 separation of sub-block 1 and sub-block 2 in that figure.

2 MR. RADSCH: If you look from a top-down view, the 56 and 58
3 is the top select gate. It's separating the top select gate. That comes at top-
4 down. At the bottom layer where the BSG is, you have the full extent of the
5 dielectric trench.

6 JUDGE CYGAN: Can you say that again and use the numbers in
7 the figure to help me understand a little better?

8 MR. RADSCH: Sure. For 56 and 58, those portions of the trench,
9 that separates the top select gate, the TSG layer, which is towards the top.
10 And so you're looking downwards, and what we've labeled as the trenches
11 26 and 28 also extend that full width of where the BSG is at the bottom. So
12 it's not cooperating with those other elements to do the separation.

13 JUDGE CYGAN: Is there a better figure, perhaps, to point to?

14 MR. RADSCH: Let's look at Figure 1A. I don't know if we have
15 that on the slide. If I direct you to Figure 1A of the '623 patent, you'll see
16 there -- so if you look at -- are you at Figure 1A, Your Honor? You'll see 56
17 and 58 are in the top select gate layer at the top. Those trenches do not
18 extend down to where the BSG is located at the bottom. So the two, 56 and
19 58, end at about the third layer of the stack or so. And the BSG is, again, at
20 the bottom of the image. So those trenches that are 56 and 58 do not extend
21 to the bottom.

22 So what you're seeing in Figure 1B, it's a top-down view. And so
23 you have a perspective of those trenches in that same location. They don't
24 extend down, 56 and 58, do not extend down into the BSG.

25 JUDGE CYGAN: Okay. And the BSG is -- which numbers
26 should we be looking at for the BSG portion?

1 MR. RADSCH: For the BSG on Figure 1A?

2 JUDGE CYGAN: Yes.

3 MR. RADSCH: That would be the -- I believe it is -- it's hard to
4 read where these are connected, I believe that is 62o, I believe.

5 JUDGE CYGAN: Okay.

6 MR. RADSCH: Allen can correct me if that's incorrect. But it's at
7 the bottom of what otherwise looks to be the staircase structure.

8 JUDGE CYGAN: And the substrate is --

9 MR. RADSCH: The substrate is multiple components --

10 JUDGE CYGAN: -- 14?

11 MR. RADSCH: Correct.

12 JUDGE CYGAN: Okay.

13 MR. RADSCH: Among others.

14 JUDGE CYGAN: And the trenches are extending in the length
15 direction of the substrate?

16 MR. RADSCH: That's correct. So here in Figure 1A, you have
17 the trenches, they're becoming in and out of the page. But what's important
18 as to your question about 56 and 58, those do not extend down from the top
19 layers to the bottom. So it has no role in separating the BSG.

20 JUDGE CYGAN: Thank you for that explanation.

21 MR. RADSCH: I'd like to address the one other issue that came
22 up with respect to these figures, whether the common source regions on the
23 periphery play a role in separating the BSG into the sub-BSG. They don't.
24 We're not talking about a boundary. What the claim requires is having an
25 element separate the BSG into sub-BSGs. What the blue common source
26 regions do is it defines the boundary of the BSG. But it plays no role in

1 separating that BSG into further sub-BSGs.

2 And while Petitioner argues there could be other BSGs on the top
3 or the bottom of Figure 1B, for example, those are other BSGs, not other
4 sub-BSGs. So the common source region plays no role in separating a given
5 BSG into sub-BSGs, which is what the claim term requires. So you see in
6 the intrinsic evidence, it's the dielectric trenches that alone separate the BSG
7 into sub-BSGs. And we submit that as how the claim term extending to
8 separate should be understood.

9 There is another claim term, Your Honor, that is not expressly
10 addressed, but we'd submit it as described in the paper, as it should be
11 construed in the same manner. That is the one or more second dielectric
12 trenches of the Claim 2 extending in the length direction. Likewise, it
13 requires that it extends across the length in order to perform the separation.

14 So I could then get into the arguments for the grounds. Ground 1
15 of Park, as we see here, the argument is that there's these short isolation-
16 insulating layers, green, that are the claimed dielectric trenches. That fails
17 for two reasons. One, there is no dispute that they're not formed in a BSG.
18 They're formed in a sacrificial layer. That's insufficient. There's no dispute
19 that they're formed in Park before there is BSG. You see here on Slide 26.

20 And then with respect to the claim term we were just discussing as
21 shown here on Slide 28. These isolation-insulating layers have a very, very
22 small extent. They do not extend to separate. To the extent there's any
23 separation occurring at all, it is principally by the common source lines in
24 Park. This is utterly unlike what is claimed and described in the '623 patent.
25 There's no extension in the length direction of those isolation-insulating
26 layers to separate the BSG and the sub-BSGs.

1 We now turn to Claim 2. And I'd like to just, with this claim, back
2 up just a little bit to orient ourselves on what the issues are with the
3 mapping. Firstly, Claim 2 depends on Claim 1, so it fails for all the same
4 reasons. But their mapping for Claim 2 onto Park is incorrect, as we pointed
5 out. But even if it was correct, it fails. So let me just step through that.

6 So what their proposal is, as shown here on Slide 30, is that one
7 would add dielectric trenches to Park's top select gate, the top layers, in the
8 same location as where the dielectric trenches are in the bottom select gate.
9 And as we have argued and I think established, the figures shown here on
10 Slide 30, as well as some of the other figures, contain errors in that it shows
11 that the top select gate lines are over the region in this image of where the
12 dielectric trenches are.

13 And as we pointed out in our briefing, we showed on Patent
14 Owner's response, page 44, we've mapped the images together to show how
15 these cross sections interrelate and to show why there's an error. They have
16 no answer to that. They don't say that our mapping is incorrect.

17 So either there's an error in the images, in which case their
18 mapping collapses, because that top select gate lines are not there. But if
19 their mapping, if the images are incorrect -- sorry, if the images are correct,
20 and you are to understand this to have the same extent, the top select gate
21 layers, to have the same extent as the bottom select gate layers, then their
22 whole argument collapses for a number of different reasons.

23 First of all, if you have the top select gate layers the same extent as
24 the bottom select gate layers, which is what they argue, you no longer have a
25 staircase structure. That's a requirement of Claim 1. So if you've read that
26 -- I mean, just to make clear, I'd like to just bring up what their argument is.

1 So this is Petitioner's reply brief at page 11. They have argued -- page 11,
2 here they summarize what their obviousness argument is. This is the top of
3 the paragraph shown on page 11.

4 They argue that Patent Owner does not challenge that it would
5 have been obvious to employee isolation-insulating layers 111 in Park's TSG
6 layer if this layer is coextensive with Park's BSG layer. That's their
7 proposed obviousness ground to make the top layer coextensive with the
8 bottom layer. But again, if you do that, as we explained in the papers, you
9 no longer have a staircase structure, which is a requirement of Claim 1. So
10 that's problem number one.

11 Secondly, there's no explanation anywhere in the petition of
12 combining those different embodiments. What they've argued is that those
13 images showing the coextensivity is a different embodiment. And they refer
14 to that specifically as a different embodiment in their petition. They've set
15 forth no argument anywhere in their petition about how one would combine
16 an embodiment with a staircase structure, with an embodiment that has no
17 staircase structure. Not only did that explain how one would do it, it
18 provided no motivation for combining the different embodiments.

19 So if you accept their theory that there is no mistakes in the
20 images, one would have to combine different embodiments in Park to reach
21 their argument about how Claim 2 should be mapped. And nowhere in the
22 petition would you find any argument for how or why those different
23 embodiments would be combined.

24 They've addressed their argument for why there's motivation to add
25 the insulating layer to the top. They've nowhere addressed combining those
26 different embodiments. So I think those are two fundamental points that in

1 either way, their arguments collapse. So firstly, as we've established, these
2 images are incorrect. So their mapping proposed to add dialectic trenches
3 where there is no top select gate layer. So it fails for that reason.

4 Here we see, on Slide 31, what the layout is of the different -- of
5 the staircase structure and the SSL at the top, that's what they mapped to the
6 top select gate layer, and that does not extend over the area where the
7 isolation layer is. So they admit, this is on Slide 32, they admit that in some
8 of Park's embodiments, the upper SSL does not have the same physical
9 extent as the lower GSL.

10 What's critical, as I was just saying, is that these are the
11 embodiments that they're relying upon for Ground 1. So if they're going to
12 say that there's other embodiments that they rely upon for Ground 2, they
13 would have had to set forth a basis for combining those different
14 embodiments, one that has a staircase structure and one that does not, and
15 they've done that nowhere.

16 As we see here in Figure 4, this shows another image of the
17 arrangement of the components. The top select gate layer over there is at the
18 top, and that does not extend anywhere over where the isolation layers are in
19 Park. This shows the staircase structure, which is a requirement of Claim
20 1C.

21 And again, their mapping as to Claim 2 would dispense with the
22 ability to have that staircase structure. They have been -- well, another
23 point, too, talking about on Slide 34, Park already has a solution for
24 separating its SSL layer into different unit areas without using insulating
25 layers. There's absolutely no need for them in that top layer anyway,
26 because they're separated by the common source lines.

1 So they introduce a new argument in their reply brief. They say,
2 after we've pointed out that their mapping is wrong, that they've misread the
3 figures, or if they haven't misread the figures, then that spark for no
4 motivation or reason to combine these disparate embodiments, they argue,
5 well, maybe one could, this is on Slides 37 and I'll turn to 38, maybe one
6 could move the location of the isolation layers. But just because they could
7 be moved doesn't mean that there would be a reason to move them under the
8 existing SSL layer at the top.

9 So they propose moving on the x-axis the isolation layers at the
10 bottom in order to place them under the top layer of SSL. So again, this is a
11 new theory not presented anywhere in the petition. It was introduced for the
12 first time in their reply brief because they got the mapping wrong. They
13 misunderstood the art. But there's been no reason to do that.

14 They've set forth, even if one were to even consider that argument,
15 they nowhere explain why one would do that. What would be the
16 motivation for moving them? In fact, it would create problems because it
17 would require one to move the common source lines that currently are
18 separating the top select gate layer in Park.

19 We briefly move on to Claim 3 because this is nowhere addressed
20 by Petitioner. As we pointed out in our briefing in the Patent Owner
21 response, Claim 3 requires an alignment in a particular direction, a width
22 direction, of the first and second dielectric trenches of Claim 2. Their entire
23 argument is basically summarized here on Slide 39. They just said that
24 under their theory of Claim 2 and having this coextensivity, there would be
25 alignment between the top and bottom dielectric trenches, the first and
26 second. Nowhere do they say they would be aligned in a width direction.

1 In order to make the allegation, they do not even claim or contend
2 or set forth what they believe that the width direction is. We pointed this out
3 in our Patent Owner reply. They did not address that in the Patent Owner
4 response. They did not address that in their reply brief. There's just an
5 evidentiary shortcoming with respect to Claim 3. Nowhere have they
6 addressed how that would be met.

7 Respect to, just very briefly, with respect to Claims 10 and 11,
8 these require the dummy -- Claim 10 requires dummy BSGs be separated
9 into dummy sub-BSGs. There's no disclosure anywhere in Park of
10 separating dummy BSGs into smaller blocks. In fact, they're connected by
11 connecting electrodes like the other word lines. Their proposed modification
12 would require forming deeper isolation regions.

13 So instead of just do a single layer at the bottom, you would now
14 have to form these dielectric trenches through multiple layers at the bottom.
15 It is in the name that that requires a change in the etching process. You can
16 no longer use a selective etching that Park discloses. And Park describes
17 using selective etching for forming insulation holes. That's at Park columns
18 12, lines 59 through 61, as well as column 13, 4 through 11.

19 So nowhere does Park describe using timed etches. They contend,
20 if you look at their Slide 34 where they contend that describes a timed etch,
21 it doesn't. It just says that -- I'm on Petitioner's Slide 34. They just say, the
22 specification states that pad regions, PAD, may be formed by etching the
23 sacrificial layer, SL, and the insulating layer, IL.

24 It says nothing about a timed etch. They have no expert testimony
25 that that refers to a timed etch. But their proposal for Claim 10 requires
26 substitution of this, of the patent's described selective etching process, with

1 the timed etching process, as their own expert admits there are drawbacks to
2 a timed etch.

3 Claim 11, I'll just move on to Slide number 44. Claim 11 suffers
4 from similar issues. What their argument is, is that having a dummy SSL, so
5 that's a layer below the top select gate layer, would serve as a buffer for the
6 etching process. But the claim requires that the dummy sub-TSG be
7 separated into sub-TSGs. And as Dr. Kuhn explained, if you're using that
8 sub-TSG layer as a buffer for the etching process, it would not be etched all
9 the way through. That's the purpose of the buffer.

10 So you would have no separation of the dummy TSG into sub-
11 TSGs. I see I'm getting close to our rebuttal time. I would like to turn to
12 Mr. Cross to address some of the issues with respect to Grounds 2 and 3.

13 MR. CROSS: And, Your Honors, I'll be addressing Grounds 2
14 first. This is applying Shibata to Park. Turning to Slide 46, Petitioner's
15 argument is outlined in red in the second box. This is where they eliminate
16 Park's second common source lines and replace them with longer isolation-
17 insulating regions with dimensions analogous to Shibata's separation
18 portions. This doesn't address or cure Park's deficiencies with regards to
19 dielectric trenches formed in the BSGs because the isolation-insulating
20 regions are still formed in the sacrificial layer before any bottom select gate
21 even exists.

22 Second, there's no motivation. One would not modify nor have
23 any reasonable expectation of success in forming these longer isolation-
24 insulation regions from the staircase region all the way into the active
25 region. There's no teaching in any of the references of having such long
26 dielectric trenches in the bottom select gate within the active region. That's

1 just something that's pulled out of thin air.

2 Third and fourth, these are new arguments. I can address those as
3 we go. Turning to Slide 48, as you can see, Shibata teaches only applying
4 its separation portion 62 only in the uppermost layers. That's in the SSL, not
5 in the BSG, which is the lowest layer. This is illustrated in Figure 16 on
6 Slide 49.

7 Turning to Park, Petitioner argues that Park allows for and
8 facilitates the very modifications discussed. That's not true. Park is
9 concerned with two aspects of the gate replacement process and the effects
10 that its isolation-insulating regions would cause. The first is providing
11 sufficient flow access for etching materials in order to remove the sacrificial
12 layers. Blocking those etching materials would cause incomplete gate
13 formation.

14 Similarly, providing enough flow access for the deposition of the
15 electrode materials in forming the layers afterwards and insufficient flow
16 would cause voids in the gate material. This could cause open circuits and
17 such.

18 Park's solutions to this in the very embodiment that Petitioner
19 relies upon, Figure 3, are twofold. First, the isolation-insulating layers are
20 staggered so that you don't have any that face each other and block the flow
21 of the etching materials of the deposition materials from both directions.
22 Second, they shorten the length of these insulating isolation layers in order
23 to decrease the length of the flow path in order to improve the process of
24 removing sacrificial layers and depositing the gate material.

25 On Slide 52, these are Petitioner's proposed modifications. And
26 you can see that this flies in the face of what Park has just taught. They

1 lengthen the dielectric trenches not just a little bit, but the entire length of the
2 BSG all the way from the staircase region through the active region. This
3 not only lengthens the isolation regions, making the flow path longer for
4 etching materials and deposition materials, but it also removes the
5 capabilities of being able to stagger these dielectric trenches. And that's
6 exactly what Dr. Kuhn explains in her statement there.

7 Petitioner also argues that Shibata addresses the same problems
8 discussed in Park. This is addressed in Slide 54. That's not true. Shibata in
9 this paragraph never mentions the gate replacement process or particularly
10 how the separation portions would have impact that in paragraph 325.
11 Instead, the very paragraph that precedes this explains that the separation
12 portion 62 are actually formed after the gates and word lines are formed.
13 This makes sense because these are formed at the very top.

14 So you can build your sacrificial layers and insulating layers, do
15 the gate replacement process, and then come in at the end and etch your
16 separation portions at the very end. And so it's not addressing the same
17 problem. Indeed, Dr. Kuhn says in paragraph 140, why the driver circuitry
18 have no bearing on the problems or issues that are addressed by Park. And
19 that's because a driver circuitry is a fixed solution, but whether voids occur
20 is unpredictable.

21 JUDGE CYGAN: Counselor, can we take a step back for a minute
22 on this?

23 MR. CROSS: Sure.

24 JUDGE CYGAN: Petitioner's main motivation was to reduce the
25 planar size of memory cell array by using Shibata's dielectric separation
26 portion as a replacement for some of the common source regions. Do you

1 take issue with that general statement, or is it just in doing so you encounter
2 difficulties with the etching process?

3 MR. CROSS: There's difficulties with the etching process,
4 whether or not it says space is immaterial because there's no teaching of
5 forming dielectric trenches in the BSG within the active region that's being
6 pulled out of thin air. And so where's the motivation? The fact that Shibata
7 teaches that in the top select gate, this may have benefits, has no bearing on
8 whether or not the dielectric trenches of Park's isolation-insulating layers in
9 the staircase region should be extended into the active region.

10 So it's more of an issue of reasonable expectation of success and
11 where these teachings are coming from. If that answers your question.

12 Finally, Park itself contemplates reducing the numbers of common
13 source regions. That's false. That was Petitioner's argument. They're
14 relying on entirely new embodiments of Figure 17 and Figure 14. These are
15 not addressed in petition. There's no motivation to combine these various
16 different embodiments. They alluded to structures 209 that are in Figure 17.
17 I'm sorry, this is addressed in Slide 56.

18 So the combination should be rejected as the new theory presented
19 for the first time in the reply, as well as having issues where they don't
20 address how adding these new elements 209 would be done in the active
21 region. And that would also significantly reduce the space dedicated to
22 memory, which would rebut the entire motivation in the first place to modify
23 Park. Moving -- is there --

24 JUDGE CYGAN: Counselor, is the new argument related to
25 minimizing etching problems? Is that the new argument?

26 MR. CROSS: The new argument, yes. Figure 17 provides new

1 structures in order to address the etching problem when the dialectic
2 trenches are slightly longer or facing one another.

3 JUDGE CYGAN: And the etching problem was something that
4 Petitioner acknowledged in the petition or was only acknowledged in the
5 Patent Owner's response?

6 MR. CROSS: I believe it was acknowledged in the petition as
7 well. It was also identified in the Patent Owner's response. But they're
8 adding new structures that were not contemplated in the combination and the
9 trial grounds.

10 JUDGE CYGAN: So is it that the Petitioner didn't present the
11 issue of the etching problem in the petition, or is it that they provided
12 additional areas of Park to address the comments in the Patent Owner's
13 response?

14 MR. CROSS: It's both. It's a new theory of how you would
15 propose the modification. And then it's also, they haven't fleshed it out.
16 They haven't said how you would apply elements 209A and 209, which are
17 only taught in the staircase region to structure this isolation-insulating region
18 that extends all the way through the active region. There's no thought or
19 there's no real contemplation that's been put into this theory.

20 JUDGE CYGAN: So the new areas that they're addressing are
21 different embodiments or different theories?

22 MR. CROSS: They're different embodiments, Figures 14 and
23 Figure 17 being applied to presumably the embodiment of Figure 3. I
24 believe that's their argument.

25 JUDGE CYGAN: Thank you.

26 MR. CROSS: With that, for Ground 3, I realize that I've gone into

1 the rebuttable time. So the primary point here is that neither Park nor
2 Shibata describes the dielectric trenches that divide the BSG and the sub-
3 BSGs within the active region. That teaching is nowhere. Motivation to
4 improve the memory only gets you as far as combining the bottom select
5 gates into a single layer, but it doesn't get you the trenches. And with that, if
6 there are no questions, I will reserve the rest of my time. Thank you.

7 JUDGE CYGAN: Okay. It's about nine minutes into your rebuttal
8 time. So that'll be six minutes surrebuttal time. Petitioner, you have 17
9 minutes for your rebuttal.

10 MR. HERMAN: So I'll begin by briefly responding to Patent
11 Owner's contention that Petitioner made new arguments in reply. So Patent
12 Owner mentions these purportedly new arguments going on 70 times in its
13 slides, and it brought them up multiple times today during its remarks.
14 Petitioner submits that nothing that it said in its reply constitutes a new
15 argument.

16 The Federal Circuit has clearly explained that an argument is
17 improper and new only if it affects a change in the grounds. So it's
18 improper, for instance, to point to new prior art or a new, different part of
19 existing prior art as teaching a required claim limitation or pointing to a
20 changed rationale for combination. But Petitioner has done no such thing
21 here. The arguments it made in reply are substantively the same as those it
22 made in the petition.

23 Petitioner has always argued that Park teaches that its upper string
24 select gate layer can extend over the portion of its bottom select gate layer
25 that includes the isolation-insulating layer 111. And that's what renders a
26 trench in the upper layer obvious. So that's not a new argument. It was part

1 of the petition. You can see that on pages 41 through 42 of the petition.

2 And Petitioner has always argued that it would have been obvious
3 to make Park's dielectric trenches longer and that a person having ordinary
4 skill in the art would not have seen etching problems as an impediment to
5 doing so. You can see that on pages 62 through 63 of the petition. All the
6 Petitioner has done here is explain why Patent Owner's arguments are
7 inconsistent and, in some cases, directly contradicted by what the prior art
8 actually says.

9 So that does not constitute a new argument. Pointing out the
10 technical problems and inconsistencies with Patent Owner's arguments while
11 making the very same arguments for unpatentability found in the petition is
12 a proper and fully appropriate reply. And again, that's all that Petitioner did
13 here. It pointed to portions of the art that contradict limits that Patent Owner
14 is trying to apply to the prior art.

15 Now with that out of the way, I'll return to Ground 1 and the Park
16 reference. First, when it comes to claim construction, there's absolutely no
17 reason to construe the claims as Patent Owner argues. So to begin, Claim 1
18 is not a product-by-process claim. It is directed to a memory device with a
19 particular structure. And all that matters for purposes of the claims is that
20 structure. It does not matter how the memory device is formed.

21 So starting with the claim language itself, the word formed in the
22 claims is not a verb. It is used to specify the structure of the claim trench,
23 i.e., where the trenches are. This also makes sense, Claim 1 is an apparatus
24 claim. It is not a method claim or a method of use claim.

25 Now the specification of the '623 patent does include columns and
26 columns of discussion of how to manufacture a memory device. So Patent

1 Owner plainly understood how to use language about manufacturing. It
2 talked about it for columns in its specification. So Patent Owner plainly
3 could have drawn claims to a manufacturing method if it so wanted. But it
4 did not. The claims in the '623 patent are directed to a memory device and
5 the structure that memory device has.

6 Yes, the claims use the phrase “formed in,” but again, that's plainly
7 just saying that the dielectric trenches are located in the BSG. It is not
8 imposing some sort of special manufacturing requirement on the claims. It
9 is not foreclosing the use of some manufacturing methods that are explicitly
10 referenced in the specification, but not others. It is not grafting on unstated
11 conductive material limitations.

12 That, however, is how Patent Owner reads the claims and
13 Petitioner submits that accepting that interpretation would be error. And that
14 error would be compounded because even if the claims are product-by-
15 process claims, it still wouldn't matter for purposes of patentability because
16 the '623 patent and Patent Owner's own expert, Dr. Kuhn, admit that exactly
17 the same device results regardless of whether the dielectric trench is
18 manufactured in the sacrificial layer or directly in the BSG.

19 So Petitioner submits that it has met its burden to show that the end
20 product is the same. The '623 patent admits it, and so does Dr. Kuhn.
21 Moreover, the only material for use with the conductive layers in the '623
22 patent is the high K in the metal material that's referenced in the
23 specification. And that's plainly intended for use with all of the '623 patent's
24 memories because it's the only material that the '623 patent discusses.

25 There's also no evidence in the record that polysilicon is necessary
26 or is even always used with a gate-first process. And the fact that both the

1 gate-last and gate-first memory process can apparently use the same material
2 should end the analysis. That means that it's not the manufacturing process
3 that's important or controls or has any bearing on the structure of the end
4 device. It's the specific material that's chosen for use with the conductive
5 layers.

6 But again, the claims here say nothing about manufacturing
7 method. They say nothing about the particular conductive materials that are
8 to be used. They only reference the BSG.

9 Now, this whole argument makes no sense for one more reason,
10 and that's because Claim 6 of the '623 patent requires the presence of
11 dummy channels. And what are those for? The '623 patent says those
12 dummy channels are present to support the layers during a gate-last process.
13 And you can see that in column 8 at line 60 through 64. So what Patent
14 Owner is doing is, it's interpreting Claim 1 in a way that negates the need for
15 structure that's required in dependent Claim 6. Doesn't make any sense.

16 I'll end by noting that, even in the gate-last process, the trench is
17 still formed in the BSG. The process of forming that particular trench
18 disbands more of the manufacturing. It starts by making the trench in the
19 sacrificial layer and it ends when the sacrificial layer is replaced with BSG.
20 So more steps, but you still formed the trench in the BSG in both the gate-
21 last and the gate-first process.

22 Likewise, the claims cannot be properly interpreted to exclude
23 Park's isolation-insulation layer 111 because of its length. There is no claim
24 requirement that the dielectric trenches extend the full length of the
25 substrate. There is no claim requirement that the dielectric trenches divide
26 the BSG entirely on their own. Instead, all the claim requires is that the

1 trenches be formed in the BSG, extend at the same length direction as the
2 common source, and cause the BSG to be divided into sub-BSG.

3 As long as those three requirements are met, Petitioner submits
4 that the claim is satisfied and Park meets all three. If layers 111 are located
5 in the BSG, they have a length and thus extend along the substrate in the
6 same direction as the common source and without layers 111, Park would
7 have a shared BSG. It's the layers 111 that complete the separation of the
8 BSG into sub-BSG. So all that Patent Owner has done here is point to
9 examples in the specification with longer trenches, but we don't limit claims
10 to just the examples.

11 So Patent Owner has also done nothing to show that there is
12 anything non-obvious about Claim 2. Here, Patent Owner does not even
13 dispute that it would have been obvious to include matching trenches in
14 Park's upper TSG layer if that layer is located over the portion of the BSG
15 that's divided by trenches. Instead, again, the only argument it makes is that
16 there's supposedly an error in the figures in Park showing a TSG with this
17 particular physical extent, but there is no such error.

18 Park's figures are meant to depict various design variations of its
19 memory device. They are not depicting exactly the same memory device in
20 every single figure. So Park shows the TSG over its trenches in five
21 separate figures, but not only that, but Park says again and again that its
22 figures are meant to be exemplary. Its layers can have different shapes and
23 different physical extents. Even isolation-insulation layer can be located in
24 different places. So what that means is that no one figure defines the outer
25 limit of Park's disclosure.

26 JUDGE CYGAN: Counselor, how would you address their

1 argument that in your -- in looking at the figures of Park that have the full
2 extent of the TSG at the top, that there's no staircase, a configuration
3 remaining in those?

4 MR. HERMAN: So the response to that is that Park has various
5 different examples of staircases. In some of its staircases, they extend in the
6 x-direction. In some of the examples, the staircases extend in the y-
7 direction. Figure 25 of Park is a good example of that because it has stairs
8 that extend in both of those directions. In the bottom of Figure 5, there's
9 stairs that extend in the x-direction. In the middle of Figure 5, there's stairs
10 that extend in the y-direction.

11 So what that means is that the gates can all extend the same
12 amount in the x-direction and yet still be stepped, and they're stepped in the
13 y-direction. And so Park contemplates both of those things. So just because
14 of its gate layers can all extend in the same amount in the x-direction, which
15 it says is one of its design variations that it contemplates and allows for, does
16 not mean that the staircase goes away. Because in all cases, Park intends
17 those stairs to be there. It's just the stairs are slightly differently configured.
18 Instead of stepping in the x-direction, they step in the y-direction.

19 And again, if Your Honors want an example of that, you can look
20 at Figure 25, which shows steps in both directions in the same device and is
21 an example of what Park is talking about. Some of the steps step in the x-
22 direction, other of the steps step in the y-direction, allowing the electrode
23 layers to extend the same distance in the x-direction.

24 JUDGE CYGAN: Okay.

25 MR. HERMAN: And another thing that Park discloses is that that
26 isolation-insulation layer 111, can move and be present in different locations

1 in different embodiments. For instance, in Figure 3, it's in one place. In
2 Figure 17, it's in a different place.

3 And also there's no motivation to combine issue here, and that's
4 because Park itself says that its layers can extend different ways, and Park
5 itself says that its trench can be relocated. So these are design variations that
6 Park itself already instructs one of ordinary skill in the art to consider. And
7 by instructing one of ordinary skill in the art to consider those designed by
8 variations, it also shows that Park is not limited in the way that Patent Owner
9 is arguing it's limited.

10 So moving on to Claims 10 and 11, here Patent Owner spends the
11 bulk of its time, at least in its briefing, arguing that it did not understand Dr.
12 Lee's testimony about how making a trench through both the select gate
13 layer and the dummy layer would improve the performance of Park's device.
14 But Patent Owner had two opportunities to question Dr. Lee about his
15 opinion that dividing Park's dummy lines in the same way as its select gate
16 would improve electrical performance. Patent Owner declined to do so. In
17 fact, it did not even file Dr. Lee's first deposition transcript, despite having
18 Dr. Lee sit for hours of questioning.

19 Moving on to Ground 2, Petitioner has provided yet another reason
20 why the claims are obvious. In particular, even if you find that long trenches
21 spanning the whole memory are for some reason required, and again they are
22 not, this is what the combination of Park and Shibata teach.

23 Shibata explains that memory can be improved and made more
24 dense if you use longer trenches and fewer common source regions, and
25 Park is amenable to that type of modification. It includes embodiments that
26 include fewer common source regions, and it includes embodiments that

1 allow its trenches to be made longer without giving rise to etching concerns.

2 So Patent Owner's arguments to the contrary are inconsistent with
3 all of this. Park does not foreclose longer trenches, or require only short
4 trenches, or require only staggered trenches. In fact, it includes
5 embodiments that are not configured in the way Patent Owner argues. The
6 art also does not say that reducing the number of common source regions
7 negatively impacts the memory. In fact, the art says the opposite. Using too
8 many common source regions consumes precious space that could otherwise
9 be used for memory cells.

10 So Patent Owner's arguments simply cannot be squared with what
11 the prior art actually says. So Patent Owner's arguments regarding Ground
12 3, Petitioner submits, also lack merit.

13 Here it spends all of its time either addressing the prior art in
14 isolation, or discussing only a fraction of the reasons for applying Park and
15 Shibata. This does not show non-obviousness. The petition did not say that
16 Park's short isolation-insulation layers 111 would be reproduced identically
17 in Shibata. Shibata already teaches longer dielectric trenches that span the
18 full length of its memory.

19 The petition simply said that those would be replicated in the lower
20 layer of Shibata using the exact same process that Shibata already teaches
21 for forming those layers for those trenches in its upper layer. And the
22 primary benefit for combining the references is the fact that applying Park's
23 teaching frees up more layers for memory cells, and Patent Owner has failed
24 to address, let alone meaningfully dispute that. So with that, I'd be happy to
25 answer any questions Your Honors have.

26 JUDGE CYGAN: No questions? Thank you very much. Patent

1 Owner, you have six minutes.

2 MR. RADSCH: Thank you, Your Honors. So starting first with
3 the claim construction of formed on, I wrote down what Petitioner's Counsel
4 said after saying that this claim doesn't matter how anything is made. He
5 said it does not matter how product is formed. He's using formed in its
6 normal sense of how something is made. That's exactly how the patent
7 claim uses the term. It is a product-by-process claim.

8 The only argument that Petitioner sets forth, was for how it met its
9 burden of showing that the resulting product of the '623 is not different from
10 the prior art. He claims that Dr. Kuhn admitted that the gate-first and gate-
11 last manufacturing methods produced the same memory device. That's the
12 heading on their Slide number 18, that's Petitioner's Slide number 18.

13 If you look at the testimony quoted from Dr. Kuhn there, it says
14 absolutely nothing of the sort. The question was whether the '623 describes
15 a gate-first process and a gate-last process. She agrees it describes both, and
16 then says that Figure A is an exemplary structure. That's what it says on the
17 left portion of what they quote, as well as on the right portion. That Figure
18 1A is an exemplary embodiment.

19 Nowhere in her deposition does she say that gate-last and gate-first
20 result in the same product. That's the only evidence they cite, and argued, as
21 meeting their burden of proof on that issue.

22 Regarding Claim 2, they've acknowledged now that their argument
23 is of coextensivity of the top layer, the SSL layer, over the bottom layer,
24 what they map as the bottom select gate layer, which would result in, as they
25 acknowledge, no more staircase structure in the x-direction. Nowhere did
26 they describe that anywhere in their briefing. That's the first argument

1 they've acknowledged today, is that there would be no more staircase in the
2 x-direction.

3 What the problem is for Claim 1, as set forth in the petition at page
4 29, they expressly rely upon the staircase in the x-direction for the staircase
5 element of the claim. They state that the Park's various gate electrode layers
6 may extend by different lengths. And they're talking about the length
7 direction, that's the x-direction. They now say, well, in Ground 2, you can
8 have a staircase only in the y-direction. That's nowhere described anywhere
9 in the petition.

10 In fact, the petition is silent on that issue completely, and nowhere
11 in the patent or the Petitioner reply. And it nowhere explained why there
12 would be a motivation to dispense with the staircase structure in the x-
13 direction, why there would be any reasonable expectation of success to
14 having a staircase only in the y-direction, and what the reason for doing that
15 would be. So that's nowhere described.

16 The petition also acknowledges, at page 41 of the petition, that the
17 embodiments, that what they're relying upon for Claim 2, are different
18 embodiments. And it nowhere said how those different embodiments meet
19 the requirements of Claim 1, nor how those different embodiments relied
20 upon for Claim 1 can be combined with the embodiments relied upon for
21 Claim 2, what the motivation combined would be, or that there's any
22 reasonable expectation for success. So their mapping for Claim 2 has to fail
23 because either those images are wrong, or if you accept that they're correct,
24 there's no more staircase structure that they're relying upon for Claim 1, if
25 there's been no discussion or explanation of the motivation to combine those
26 disparate embodiments.

1 And then with respect to the extending portion, it's not enough just
2 to extend somewhat and to have a separation. The claim expressly requires
3 that the -- this is as to Claim 1 -- that the extension is to separate. We talked
4 earlier about the different trenches that are formed. It's seen in Figure 1b. I
5 don't think they dispute at all that our reading was correct, that the trenches
6 56 and 58 are only in the top select gate layer, that's described at 7, 26, and
7 30 of the specification, and that trenches 26 and 28 are in the bottom select
8 gate layer and extend the full length to perform the separation as described
9 in the specification at columns 7, lines 20 through 24. And with that, Your
10 Honor, I will establish if there are any questions.

11 JUDGE CYGAN: Seeing no questions.

12 MR. RADSCH: Thank you, Your Honors.

13 JUDGE CYGAN: I'd like to thank Counsel for both parties for
14 your attendance and presentation. Appreciate the level of preparedness you
15 both exhibited today and good command of the record, which is very helpful
16 for the Board. I'd like to compliment your colleagues who did a fine job on
17 the demonstrative exhibits, which made it easier for us to follow the
18 arguments. A final written decision will be issued in due course. Please
19 make yourself available to the court reporter for any questions. And this
20 hearing is now adjourned.

21 (Whereupon, the above-entitled matter went off the record at 3:07
22 p.m.)

IPR2024-00794
Patent 10,950,623 B2

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