UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No. IPR2024-00794

U.S. Patent No. 10,950,623

PATENT OWNER'S NOTICE OF APPEAL

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Pursuant to 35 U.S.C. §§ 141, 142, and 319, and 37 C.F.R. §§ 90.2-90.3, notice is hereby given that Patent Owner Yangtze Memory Technologies Company, Ltd. ("Patent Owner") appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board ("Board") entered October 22, 2025 (Paper 30) in IPR2024-00794, and from all underlying orders, decisions, rulings, and opinions decided adversely to Patent Owner regarding this *inter partes* review of U.S. Patent No. 10,950,623 ("the '623 patent"). A copy of the Final Written Decision is attached.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal include, but are not limited to, the following: (1) the Board's determination that claims 1 and 6 of the '623 patent have been shown to be unpatentable; (2) the Board's determination that Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 6 of the '623 patent are unpatentable under 5 U.S.C. § 103; (3) the Board's consideration of the expert testimony, prior art, and other evidence in the record; (4) the Board's factual findings, conclusions of law or other determinations supporting or related to those

issues; as well as (5) all other issues decided adversely to Patent Owner in any orders, decisions, rulings, and opinions.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), this Notice is being filed with the Director of the United States Patent and Trademark Office, and a copy of this Notice is being concurrently filed with the Patent Trial and Appeal Board. In addition, a copy of this Notice and the required docketing fees are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit via CM/ECF.

Dated: October 23, 2025

By: */Andrew Radsch/*
Andrew Radsch
Admitted *Pro Hac Vice*
Counsel for Patent Owner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that, on October 23, 2025, the foregoing PATENT OWNER'S NOTICE OF APPEAL was:

(1) electronically filed through PTACTS

(2) filed by Express Mail to The Director of the United States Patent and Trademark Office at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

(3) filed in the U.S. Court of Appeals for the Federal Circuit using the Court's CM/ECF filing system and pay.gov to pay the filing fee electronically

(4) provided a courtesy copy via electronic mail to the following attorneys of record for the Petitioner listed below:

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Paper 30
Date: October 22, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00794
Patent 10,950,623 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Micron Technology, Inc. ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1–11 of U.S. Patent No. 10,950,623 B2 (Ex. 1001, "the '623 patent"). Paper 1 ("Pet."). Yangtze Memory Technologies Company, Ltd. ("Patent Owner") filed a Preliminary Response to the Petition. Paper 8 ("Prelim. Resp."). The Petition is supported by a declaration from Dr. Jack C. Lee. Ex. 1003 ("Lee Declaration"). The Preliminary Response is supported by a declaration by Dr. Jonathan Bradford. Ex. 2007 ("Bradford Declaration"). We instituted *inter partes* review as to claims 1–11 of the '623 patent on all asserted grounds of unpatentability. Paper 9 ("Inst. Dec.").

Patent Owner filed a Response, accompanied by a declaration of Dr. Kelin Kuhn. Paper 12 ("PO Resp."); Ex. 2010 ("Kuhn Decl."). Petitioner filed a Reply, accompanied by a Supplemental Declaration of Dr. Jack C. Lee, and a transcription of a deposition of Dr. Kuhn. Paper 14 ("Pet. Reply"); Ex. 1025 ("Lee Supp. Decl."); Ex. 1026 ("Kuhn Dep."). Patent Owner filed a Sur-reply, accompanied by a transcript of a deposition of Dr. Lee. Paper 17 ("PO Sur-reply"); Ex. 2011 ("Lee Dep."). We held an Oral Hearing with the parties on July 30, 2025, and a transcript was entered into the record. Paper 26 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner has shown by a preponderance of the evidence that claims 1 and 6 are unpatentable, and Petitioner has not shown by a preponderance of the evidence that claims 2–5 and 7–11 are unpatentable.

B. Real Parties in Interest

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 5. Patent Owner identifies itself as a real party-in-interest. Paper 4, 2.

C. Related Matters

The parties represent that the ’623 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 4, 2; Pet. 5.

Petitioner has also filed IPRs challenging other patents asserted in the district court case, namely U.S. Patent Nos. 10,658,378 (IPR2024-00788), 10,861,872 (IPR2024-00789), 10,868,031 (IPR2024-00790), 10,937,806 (IPR2024-00791), 11,501,822 (IPR2024-00795), 11,468,957 (IPR2024–00792), and 11,600,342 (IPR2024-00793). Pet. 5.

D. The ’623 Patent

The ’623 patent is titled “3D NAND Memory Device and Method of Forming the Same.” Ex. 1001, code (54). The ’623 patent issued from Application No. 16/365,725, filed on March 27, 2019, and claims priority via a continuation to PCT/CN/2018/119908, filed on December 7, 2018. *Id.* at code (63). The ’623 patent relates to “formation of a 3D NAND memory device with a divided block structure.” *Id.* at 1:32–33.

E. Illustrative Claim

Claim 1 is illustrative, and recites as follows:[1]

[1.Pre] A memory device, comprising:

[1.A] a substrate;

[1] Bracketed organization added as per the Petition.

[1.B] a bottom select gate (BSG) disposed over the substrate;

[1.C] a plurality of word lines positioned over the BSG with a staircase configuration;

[1.D] a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;

[1.E] one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and

[1.F] one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.

F. Evidence

Petitioner relies on the following patent document evidence.

Name	Patent Document	Exhibit
Park et al. ("Park")	US 10,559,583 B2	1004
Shibata et al. ("Shibata")	US 2019/0122734 A1	1005

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–11 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–11	103[2]	Park
1–11	103	Park, Shibata
1–11	103	Shibata, Park

[2] Petitioner asserts, and we accept on the complete trial record that AIA § U.S.C. 103 applies to the '623 patent. *See* Pet. 19.

II. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, "would have been obvious at the time the invention was made to a person having ordinary skill in the art [to which said subject matter pertains]." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.[3] *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art ("POSITA") at the critical time "would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience)." Pet. 19 (citing Ex. 1003 ¶¶ 36–37). Petitioner further asserts that a POSITA "would have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled." *Id.* Patent Owner does not object to this assessment, arguing that its claims are valid regardless of the precise definition. PO

[3] Neither party presents evidence or arguments regarding objective evidence of non-obviousness.

Resp. 10 (citing Ex. 2010). We adopt Petitioner's proposed level of ordinary skill, as it appears to be consistent with the specification of the '623 patent and the prior art of record.

C. Claim Construction

In an *inter partes* review, we construe a patent claim "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)." 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their "ordinary and customary meaning," which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

1. "formed in the BSG"

Patent Owner argues a construction of "dielectric trenches **formed in the BSG** and extending in a length direction of the substrate **to separate the BSG into a plurality of sub-BSGs**." PO Resp. 11–12 (emphasis modified). Patent Owner argues that this language requires that "there must be an existing BSG such that forming the dielectric trench separates the BSG into a plurality of sub-BSGs." *Id.* at 12; PO Sur-reply 7 (citing Ex. 2010 ¶ 64). Patent Owner argues that the claims are limited to the "gate-first" embodiment of process 1200, in which BSG gates are formed during step 1204, and trenches are subsequently formed in the BSGs and dummy BSGs during step 1206. PO Resp. 12 (citing Ex. 1001, 21:34–38, 45–46, Fig. 5A; Ex. 2010 ¶ 63). Such trenches "are formed in the one or more BSGs" and "extend[] . . . to separate the BSG 62p and the dummy BSGs 62n–62o into a plurality of sub-BSGs and sub-dummy BSGs." *Id.*at 13 (citing Ex. 1001, 7:17–26; Ex. 2010 ¶ 63). Patent Owner argues that this "formed in the one

or more BSGs" language in the gate-first embodiment matches that in the claims and limits the claims to the gate-first embodiment. PO Sur-reply 3.

Patent Owner argues that the claims exclude a second embodiment of the '623 patent, the "gate-last" process, in which such trenches are formed in insulating sacrificial layers instead of in a BSG. PO Resp. 13–14 (citing Ex. 2010 ¶ 64). Although such sacrificial layers are replaced by BSGs in a later manufacturing step, Patent Owner argues that this gate replacement embodiment, referred to as the "gate-last" process, is not within the scope of the claims because the trenches are not "formed in" the BSG, but are instead formed in insulative sacrificial layers and not a conductive BSG. *Id.* at 14 (citing Ex. 2010 ¶ 64); PO Sur-reply 3 (citing Ex. 2010 ¶ 63).

In response to Patent Owner's proposed construction, Petitioner argues that "'formed in' simply specifies where the 'dielectric trenches' are located: within the BSG layer." Pet. Reply 4. Petitioner also argues that each of the claims of the '623 patent are to a "memory device" and that nothing imposes any particular manufacturing process on the claimed memory device. *Id.* at 5.

We agree with Petitioner. As pointed out by Patent Owner, the "trenches formed in the BSG" language of claim 1 reflects specific description of the gate-first method of manufacturing, but not the gate-last method of manufacturing. Ex. 1001, 7:17–19 ("referring to Fig. 1A, one or more first dielectric trenches . . . are formed in the one or more BSGs"). However, as Petitioner points out, the claims are to a memory "device," not to a method of manufacturing or a device produced by specific manufacturing steps. Pet. Reply 1. During prosecution of the application that matured into the '623 patent, the Examiner determined that the device of claim 1 was distinct from a separately claimed method of manufacturing and

required restriction between the two classes of invention. Ex. 1002, 591. The Examiner's requirement stated that the memory device of claim 1 is not limited by the disclosed process of manufacture because "the process claims require . . . deposition steps of polysilicon whereas the product claims do not require any polysilicon." *Id.* Applicant agreed "without traverse" with the Examiner's determination and selected to pursue only the "device" claims. *Id.* at 596 ("Applicant elects, without traverse, Invention I, Claims 1–11, drawn to a device").[4]

The distinctiveness is also supported by the discussion in the '623 patent of "formed in the BSG" that describes its device separately from its method of formation. The '623 patent describes that "[i]n the disclosed memory device, one or more first dielectric trenches are formed in the BSG and extend in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs." Ex. 1001, 2:25–28. This description precedes, and is separate from, its description of an aspect of a process for manufacturing a memory device in which the BSG layer is formed and then "dielectric trenches are formed" that may "pass through the BSG layer" so that the "BSG layer is separated by the one or more first dielectric trenches into a plurality of sub-BSG layers." *Id.* at 3:30–45. The description of the device having trenches formed in the BSG, which is not limited to a particular manufacturing process, further supports Petitioner's contention that the "formed in the BSG" language is not limited to a particular manufacturing embodiment.

[4] Claims to the process of manufacture were cancelled prior to allowance. Ex. 1002, 612.

We also agree with Petitioner that the "formed in" language, as used in the disclosure of the '623 patent, does not necessarily exclude the gate-last embodiment. Pet. Reply 6. Petitioner points to the description of the gate-last embodiment in which the BSG can be "formed firstly using sacrificial layers." *Id.* (citing Ex. 1001, 7:1–11); *see also* Ex. 2011 (Lee Dep.), 78:5–12 ("the BSG . . . can be, quote, formed firstly using sacrificial layers, end quote, that are only replaced with conductive material after all other processing steps, including the trench formation -- are completed."). As stated by Dr. Kuhn, "at this stage in the process, [feature 62p] can be a sacrificial layer instead of a BSG." Ex. 2010 ¶ 64. To form a BSG, additional steps are required; i.e., the sacrificial layers are removed and replaced with a "high K layer and a metal layer," and the metal layer has the conductivity that allows it to be used as a BSG. *Id.*

Thus, both declarants agree that "formed" can include a multiple step process; i.e., "firstly" using sacrificial layers and secondly, replacement with the metal gate layer. Dr. Kuhn's testimony is supported by the '623 patent, which states that the "BSG 62*p* . . . can be sacrificial layers [that] can be removed and replaced." The description that the BSG "can be" a "sacrificial layer[]" that is "made of SiN" indicates that the '623 patent considers the BSG to encompass both the first-formed insulative sacrificial layer and the later-formed conductive metal layer. Thus, we agree with Petitioner that these steps, considered together, describe a trench "formed in the BSG" in the gate-last embodiment.

Patent Owner also argues that the claim requirement that the trenches "separate the BSG into a plurality of BSGs" indicates that "there must be an existing BSG such that forming the dielectric trench separates the BSG into a plurality of sub-BSGs." PO Resp. 12; Ex. 2010 ¶ 62. Patent Owner points

to the description in the ’623 patent of “‘trenches 26 and 28 [that] are formed in the one or more BSGs,’ which ‘extend[] in an X-direction . . . of the substrate 10 to separate the BSG . . . into a plurality of sub-BSGs.’” *Id.*at 13 (citing Ex. 1001, 7:17–26). Yet the ’623 patent describes that trenches perform this separation even in the gate-last embodiment. Ex. 1001, 15:22–15–65. The ’623 patent describes that Figure 5A represents trenches formed in the BSG that “extend[] in a X-direction of the substrate . . . to separate the BSG 62*p* . . . into a plurality of sub-BSGs.” Ex. 1001, 15:58–65. The description of Figure 5A includes the above-discussed statement that the BSG 62*p* can be a sacrificial layer which can be removed and replaced in future manufacturing steps. Ex. 1001, 15:45–48. Thus both the gate-first and gate-last embodiments describe the ability of the trenches to separate the BSG into a plurality of BSGs.

Patent Owner’s arguments that “formed in the BSG” causes claim 1 to be construed as a product-by-process claim are also unavailing. First, this argument presupposes that claim 1 is limited to the gate-first embodiment, which we do not agree with for the reasons discussed above. Even under a product-by-process construction, the claim would include the structures of both the gate-first and the gate-last embodiments. For that reason alone, Patent Owner’s product-by-process construction would not affect the scope of the claim in a manner relative to the disputed issues.

Second, the prosecution history indicates that the memory device of claims 1–11 is not limited by the processing steps described in the ’623 patent. Patent Owner argues that only the gate-first processing would result in a stack typically comprising polysilicon. PO Sur-reply 5. However, the Examiner’s restriction requirement was based on a construction in which “the product claims do not require any polysilicon.” Ex. 1002, 591.

Applicant agreed "without traverse" with the Examiner's determination. *Id.* at 596. Construing the claims now to require polysilicon would be inconsistent with the agreement reached during prosecution,[5] which provides further reason to reject a product-by-process construction that includes only the structure resulting from the gate-first embodiment.

Third, the record does not reflect that even under a product-by-process construction limited to the gate-first embodiment, the resulting memory device would necessarily have a different structure. *See Greenliant Sys., Inc. v. Xicor LLC*, 692 F.3d 1261, 1268 (Fed. Cir. 2012) (stating, "if the process by which a product is made imparts 'structural and functional differences' distinguishing the claimed product from the prior art, then those differences 'are relevant as evidence of no anticipation' although they 'are not explicitly part of the claim.'") (quoting *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1370 (Fed. Cir. 2009)). Patent Owner argues that the gate-last embodiment has insulating layers of high-K materials whereas the gate-first embodiment has insulating layers of "SiO, SiCN, SiOCN, or other suitable materials." PO Sur-reply 5. However, nothing in the record clarifies that a high-K material would not be one of the "other suitable materials" such that the gate-first and gate-last embodiments would have a different insulating layer material. To the contrary, the '623 patent describes a process 1200 such that after "trenches are formed in the BSGs" during step 1204, in "some embodiments, the formation of the common

[5] Moreover, because Applicant's agreement was "based on the understanding that Applicant is not prejudiced against filing one or more divisional applications that cover the non-elected claims," breaking the agreed-upon boundaries of the restriction requirement could potentially undermine the safeguards provided under 35 U.S.C. § 121 for any such divisional applications and any patents issued thereon.

source regions further includes removing the BSGs . . . and reforming the BSGs . . . with a high-K layer and metal layers" in step 1214. Ex. 1001, 21:45–46, 22:43–48. Process 1200 thus shows that the '623 patent's gate-first embodiment, like its gate-last embodiment, may perform a gate-replacement step to result in a high-K layer and metal layers. Thus, the record does not reflect that the claimed memory device would necessarily have a different structure due to the processing steps of the gate-first embodiment than from the gate-last embodiment.

Based upon the foregoing analysis of the language of the claims, the description in the '623 patent, the testimony of the experts, and the prosecution history of the '623 patent, we determine that the recitation of "trenches formed in the BSG" in claim 1 encompasses both the "gate-first" and the multi-step "gate-last" embodiments of the '623 patent.

2. "trenches . . . extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs"

Patent Owner argues that this term should be construed consistent with its plain meaning to require that the length of the dielectric trench is what separates the BSG into sub-BSGs. PO Resp. 14–15. Stated at this level of generality, there is no dispute between the parties. We determine that this statement is consistent with the disclosure of the '623 patent. *See* Ex. 1001, 15:61–64 (stating, "The first trenches 26 and 28 extends in a X-direction (i.e., a length direction) of the substrate 10 to separate the BSG 62p and the dummy BSGs 62n-62o into a plurality of sub-BSGs and sub-dummy BSGs.").

Patent Owner further argues that it is the trenches and only the trenches that separate the BSGs into sub-BSGs. PO Resp. 16–19; PO Sur-reply 7–11. Patent Owner argues that "[h]aving other structures act in

cooperation for the ***same boundary*** would mean that the dielectric trench itself no longer 'extend[s] in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs.'" PO Resp. 18–19. Patent Owner points to the '623 patent's express statement that "[w]ithout the introduction of the first/second trenches, the memory device 100 (or the memory cell block 100) has a shared BSG." *Id.* at 18 (citing Ex. 1001, 9:46–49; Ex. 2010 ¶ 70).

We do not agree that such arguments support Patent Owner's conclusion. Patent Owner acknowledges that two portions of a BSG that are connected at a small opening are not separated because both portions remain electrically connected to each other. *Id.* at 17 (stating, "common source regions 52a is merely in the middle of a single sub-BSG 2 ('SUB-BLK2') and does not divide it into further sub-BSGs because there is an H-cut 72 that connects the two sides of the common source region such that both regions are part of the same sub-BSG") (citing Ex. 1001, 9:15–19, 9:41–44) (emphasis omitted); Ex. 1026, 34:4–15, 41:23–42:16 (Dr. Kuhn attesting that common source regions may isolate adjacent BSGs). Patent Owner considers other portions of the BSG to be separated into sub-BSGs because there is no such connection between the sub-BSG portions. *Id.* at 17–18 (annotating Ex. 1001, Fig. 1B). Under such reasoning, the addition of a trench closing a gap between two neighboring BSG portions, thereby breaking the electrical connection therebetween, would "separate" the two BSG portions into further sub-BSGs. In its obviousness assertions, Petitioner argues for such an interpretation of the claim. *See* Pet. Reply 10 ("Park's layers 111 electrically ***separate*** its BSG").

Based on the above, we determine that the phrase "dielectric trenches formed in the BSG and extending in a length direction of the substrate to

separate the BSG into a plurality of sub-BSGs" requires that the trenches perform electrical separation between sub-BSGs, but does not require that the trenches act alone, extending from one end of the device to the other across the entire BSG. Similarly, the trenches need not have any particular length, and need only to have some length that performs that separation.

Patent Owner argues that every embodiment in the '623 patent describes that the trenches alone separate the BSG, and that the claims should therefore be read as including such a limitation. PO Sur-reply 10. Petitioner disagrees, arguing that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" Pet. Reply 8 (citing *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004)).

Such words or expressions of manifest exclusion may be found in "specific parameters" that describe the dimensions of the features in the claims. *Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1302 (Fed. Cir. 2004) (discussing *Brookhill-Wilk 1, LLC v Intuitive Surgical, Inc.*, 334 F.3d 1294 (Fed. Cir. 2003)). In *Brookhill-Wilk*, the court confronted the question of whether the claim term "remote location" must be construed as being "outside the operating room." *Brookhill-Wilk*, 333 F.3d at 1301–1302. The court determined that although the preferred embodiment described a surgeon located outside the operating room, and that certain beneficial objectives would be achieved thereby, the claim should not be limited thereto because such statements "do not indicate that the invention can only be used in such a manner." *Id.* at 1301. Statements that limit the claims may include, for example, "the present invention requires ..." or "the present

invention is ...” or “all embodiments of the present invention are. . . .” *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372 (Fed. Cir. 2014). Other such statements include descriptions of the feature as a “very important feature . . . in an aspect of the present invention,” accompanied by statements disparaging alternatives to that feature. *Id.* (citing *InproII Licensing, S.A.R.L. v. T-Mobile USA Inc.*, 450 F.3d 1350, 1354–55 (Fed. Cir. 2006)).

Petitioner argues, and we agree, that “the ’623 patent repeatedly explains that it is not to be limited to its examples.” Pet. Reply 8 (citing Ex. 1001, 5:13-16 (“[s]pecific examples” in specification are “merely examples and are not intended to be limiting.”); 23:36-46 (“other … structures” besides those specifically depicted can be used)). In reply, Patent Owner argues that *Liebel-Flarsheim* does not control because trenches acting alone to separate BSGs into sub-BSGs is “**a clear requirement of the claim language**; the specification’s embodiments simply confirm that understanding.” PO Sur-reply 10 (citing Ex. 2010 ¶ 68). However, Patent Owner does not identify, nor do we find, words or expressions in the ’623 patent claims or specification that manifestly exclude trenches acting in concert with other portions of the device to separate BSGs into sub-BSGs.

3. “trenches . . . extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs”

Patent Owner presents the same argument for the similar limitation of claim 2 that “one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.” PO Resp. 19. We determine that argument is persuasive only to the same extent as to the analogous BSG limitation in claim 1. Therefore, we construe this limitation as requiring that the length of

the dielectric trench is what separates the TSG into sub-TSGs. *Id.* However, for the same reasons expressed with respect to the BSG in claim 1, we decline to add further limitations as to the length of the claimed trench or the extent of its cooperation with other elements in separating the TSG.

4. Remaining considerations

Patent Owner asserts that the parties exchanged proposed constructions in the parallel district court proceeding. PO Resp. 11 (citing Exs. 2008–2009). Patent Owner argues that these constructions do not impact the issues in this proceeding. *Id.* In the parallel proceeding, Petitioner Micron asserted that "dielectric trenches" should be given its plain and ordinary meaning of "trenches with dielectric material inside the trench openings." Ex. 2008, 3. Patent Owner lists this Micron-proposed construction in its "YMTC Proposed Constructions" exhibit, submitted in the parallel district court proceeding. Ex. 2009, 8. We have considered this construction in our analysis, while noting the parties' dispute centers on whether the trenches are "formed in the BSG" and separating the BSG, rather than the structure of a trench.

For the remainder of the claim limitations, we do not need to determine a particular construction. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that "we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness over Park

Petitioner asserts that claims 1–11 are unpatentable under 35 U.S.C. § 103 as obvious over Park. Pet. 25. Patent Owner argues against this assertion. PO Resp. 32–54.

Upon consideration of the totality of arguments and evidence in the complete trial record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 6, but not claims 2–5 and 7–11, are unpatentable under 35 U.S.C. § 103 as obvious over Park.

1. Park

Park is titled "Memory Device." Ex. 1004, code (54). Park relates to a semiconductor memory device having "gate electrode layers stacked on an upper surface of a substrate and each including a plurality of unit electrodes extending in a first direction, and a plurality of connecting electrodes connecting the unit electrodes to each other." *Id.* at code (57). The device also includes "channel structures extending through the gate electrode layers in a direction perpendicular to the upper surface of the substrate, first common source lines extending in the first direction and interposed between the unit electrodes." *Id.* The device further includes "second common source lines extending in the first direction between the first common source lines and each having a first line and a second line separated from each other in the first direction by the connecting electrodes." *Id.*

2. Analysis of Claim 1

We begin our analysis of Petitioner's obviousness contentions with Petitioner's assertions as to claim 1. Patent Owner does not specifically argue against Petitioner's assertions for limitations [1.Pre]–[1.D]; however, we draw no inference therefrom and Petitioner bears the burden of persuasion.

> *[1.Pre]–[1.D] A memory device, comprising: a substrate; a bottom select gate (BSG) disposed over the substrate; a plurality of word lines positioned over the BSG with a staircase*

configuration; a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines

Petitioner asserts that limitations [1.Pre]–[1.D] are taught by Park in the following manner. Petitioner points to Park's description of a "3D memory device" that includes a "substrate 101" and a plurality of memory cell strings that each include a ground select transistor connected to a ground select line ("GSL"), which Petitioner asserts teaches the claimed "bottom select gate" because the GSL controls connection of the memory cell strings to a common source line in the same manner as the '623 patent. Pet. 25–27 (citing Ex. 1004, 1:14–17, 1:31–32, 3:24–27, 4:17–30, 10:34–35, Fig. 11; Ex. 1001, 1:37–46; Ex. 1003 ¶¶ 127–137). Petitioner further points to the plurality of Park's word lines, "WL," each of which are connected to a row of memory cells in memory cell array 2. *Id.* at 27–28 (citing Ex. 1004, 3:28–36, 1:62–2:8, 3:39–44, 4:22–24, Fig. 2; Ex. 1003 ¶¶ 138–143). Petitioner points to Figure 4 of Park as illustrating that the word lines 120*b-i* are positioned over the substrate and the ground select line 120*a*. *Id.* at 28–29 (citing Ex. 1004, Fig. 4, 6:65–7:2; Ex. 1003 ¶¶ 144–147). Petitioner asserts that the claimed "staircase configuration" of word lines is taught by Park's "stepped structure" of gate electrode layers. *Id.* at 29 (citing Ex. 1004, 6:56–60, 7:8–11, 8:18–50, 11:62–65, Figs. 15, 25, 32; Ex. 1003 ¶¶ 148–150).

Petitioner asserts that the claimed insulating layers are taught by Park's insulation layers 130 that are present between substrate 101 and ground select line 120*a*, and between the ground select line 120*a* and the word lines 120*b-i*. *Id.* at 29–30 (citing Ex. 1004, 5:17–23, 6:49–52, 10:35–37, 10:40–45, Fig. 11; Ex. 1003 ¶¶ 151–160).

Upon review of Park, we determine that Petitioner's assertions are supported by the record.

[1.E] one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs

Petitioner asserts that Park's isolation insulating layers 111 teach the claimed dielectric trenches that separate Park's ground select line into a plurality of sub-ground select lines; i.e., those portions specific to unit areas AU1–UA8. Pet. 30. Petitioner provides an annotated Figure 3:

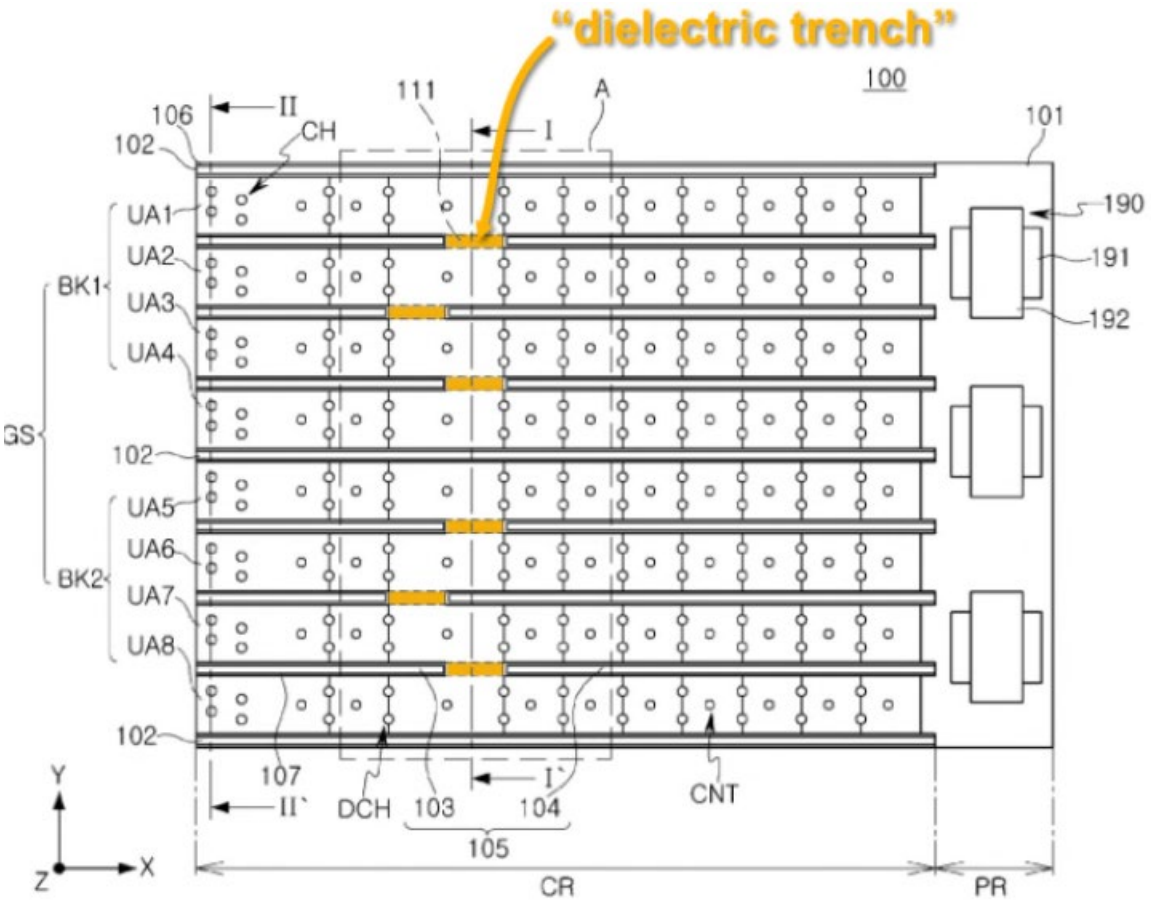


FIG. 3

Park's annotated Figure 3 portrays a "top-down view" showing isolation layers 111 (orange) located between common source lines 102, extending lengthwise to close the gaps between common source lines 105 and to

separate the ground source line ("GSL") in blocks BK1 and BK2 into unit areas UA1–UA8. *Id.* at 31.

Petitioner asserts that this teaches limitation [1.E]:

> Park includes "one or more first dielectric trenches formed in the BSG" (isolation insulating layers 111 formed within its GSL). These "dielectric trenches" "extend[] in a length direction of the substrate" (layers 111 extend lengthwise in the X-axis direction). Further, the "dielectric trenches" "separate the BSG into a plurality of sub- BSGs" (layers 111 cause Park's GSL to be divided into portions corresponding to unit areas UA1-UA8).

Pet. 32.

a) Whether Park's isolation insulating layers are "dielectric trenches formed in the BSG"

Patent Owner argues that Park does not teach the claimed trenches because its isolation insulating layers are formed in its sacrificial layer, not its BSG. PO Resp. 32–34; PO Sur-reply 3. Patent Owner's argument is based upon its proposed construction that excludes the embodiment of the '623 patent in which trenches are formed in a sacrificial layer that is later replaced by a BSG. PO Resp. 32. As discussed *supra*, we do not adopt this construction, and instead adopt a construction of "trenches formed in the BSG" that permits trenches to be formed in the BSG through a multistep process that can include formation of a trench in a sacrificial layer and replacement of the sacrificial layer. *Supra* § II.C.1. Consequently, we do not agree with Patent Owner's argument.

b) The "extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs" limitation

Petitioner asserts that Park's insulating layer 111 separates the BSG into a plurality of sub-BSGs because it "cooperates with common source lines to divide Park's GSL into portions." Pet. 35 (citing Ex. 1004, 6:8–12, Fig. 3). *Id.* Petitioner points to the '623 patent as also using additional

structure, in the form of common source regions 52c and 52b, to "play a role in separating the memory into blocks and sub-blocks." *Id.* (citing Ex. 1001, Fig. 1B, 9:3–8).

Patent Owner argues that Park's insulating layers do not extend along the length of the substrate to separate the BSG into a plurality of separate BSGs. PO Resp. 34–38; PO Sur-reply 10 (arguing that Park's insulating layers do not alone separate the BSG). Patent Owner argues that Park's layer 111 is a "short division in the second common source line." PO Resp. 37–38. Patent Owner further argues that Park's layers 111 exist in the staircase region of Park's memory device and "do not even extend into the active region and are therefore not a feature that extends in the length direction of the substrate to separate the alleged BSGs into sub-BSGs." *Id.* at 36–37; PO Sur-reply 7–9.

Petitioner has sufficiently shown that Park's insulating layer 111 teaches a "trench" that "separate[s] the BSG into a plurality of sub-BSGs." Petitioner asserts that Park's BSG would not be separated at certain points (i.e., gaps in its common source lines) if Park's trench layers 111 were not there. Pet. 35–36. Petitioner asserts that the BSG is fully separated into sub-BSGs because the common lines 105 also divide the BSG, and the separation performed by the trenches causes the sub-BSGs to become completely separate. *Id.*

We agree that Park's insulating layer, by providing insulation along a length direction of a substrate that would otherwise permit electrical connection between two portions of a single BSG, acts to separate a BSG into sub-BSGs. Patent Owner states that it is "primarily" common source lines of Park that separate and divide the gate electrode area's blocks BK1 and BK2 [BSGs] into unit areas UA1 and UA8, but admits that Park's

insulating layer 111 exists in-line with the common source lines and in between sections of the gate electrode layer. PO Resp. 22–23. Our construction of claim 1 does not require that the trench extend the entire length of the memory device, or that the trench be the sole structure separating the entire boundary of the sub-BSGs. *Supra* § II.C.2. Under our construction, Petitioner's showing is sufficient to show that Park's insulating layers 111 are dielectric trenches that separate the BSG into a plurality of sub-BSGs as required by claim 1.

With respect to Patent Owner's argument that Park's layers 111 do not separate the BSG into a plurality of sub-BSGs because Park's layers are in the staircase region and not in the cell string-containing active region as described in the '623 patent, we disagree. *See, e.g.*, PO Sur-reply 7–9. Patent Owner describes its BSGs, and its trenches that subdivide its BSGs, as spanning both the active and staircase regions. PO Sur-reply 9 (annotated Fig. 1B of the '623 patent showing BSGs in orange spanning both the active and staircase regions), 10 ("the trenches extend left and right . . . including through the staircase region, to separate the BSG into sub-BSGs"). Our construction does not require that the trenches act alone, extending from one end of the device to the other across the entire BSG. *Supra* § II.C.2. Similarly, the trenches need not have any particular length, and need only to have some length that performs that separation. *Id.* Thus, the presence of trenches in the staircase region in Park is not disqualifying because they admittedly act to complete the separation the BSG into sub-BSGs that span both the active and staircase regions of Park. *Id.* at 9 (Patent Owner's annotated Fig. 3 of Park).

Therefore, Patent Owner's argument does not detract from Petitioner's persuasive showing that Park teaches limitation [1.E].

> *[1.F] one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.*

Petitioner asserts that Park teaches common source regions through Park's "common source line[s] 102." Pet. 37. Petitioner further asserts that Park's Figure 3 shows these source lines extending in the same X-axis direction as Park's trenches 111. *Id.* (citing Ex. 1004, Fig. 3, 10:46–50). Petitioner further asserts that Park's Figure 11 shows these source lines extending through the BSG (GLS 120a), the plurality of word lines 120b–120i, and the plurality of insulating layers (annotated in green). *Id.* at 38 (citing Ex. 1004, Fig. 11; Ex. 1003 ¶¶ 188–194). Patent Owner does not specifically contest these assertions.

We agree that Petitioner's assertion is supported by the record and, accordingly, that Petitioner has sufficiently shown that Park teaches limitation [1.F].

Conclusion

For the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claim 1 is unpatentable as obvious over Park.

3. Analysis of Claims 2–11

a) Claim 2

Claim 2 depends from claim 1, and further recites,

> a top select gate (TSG) positioned over the plurality of word lines, the TSG and the plurality of word lines being spaced apart by the plurality of insulating layers; and
>
> one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.

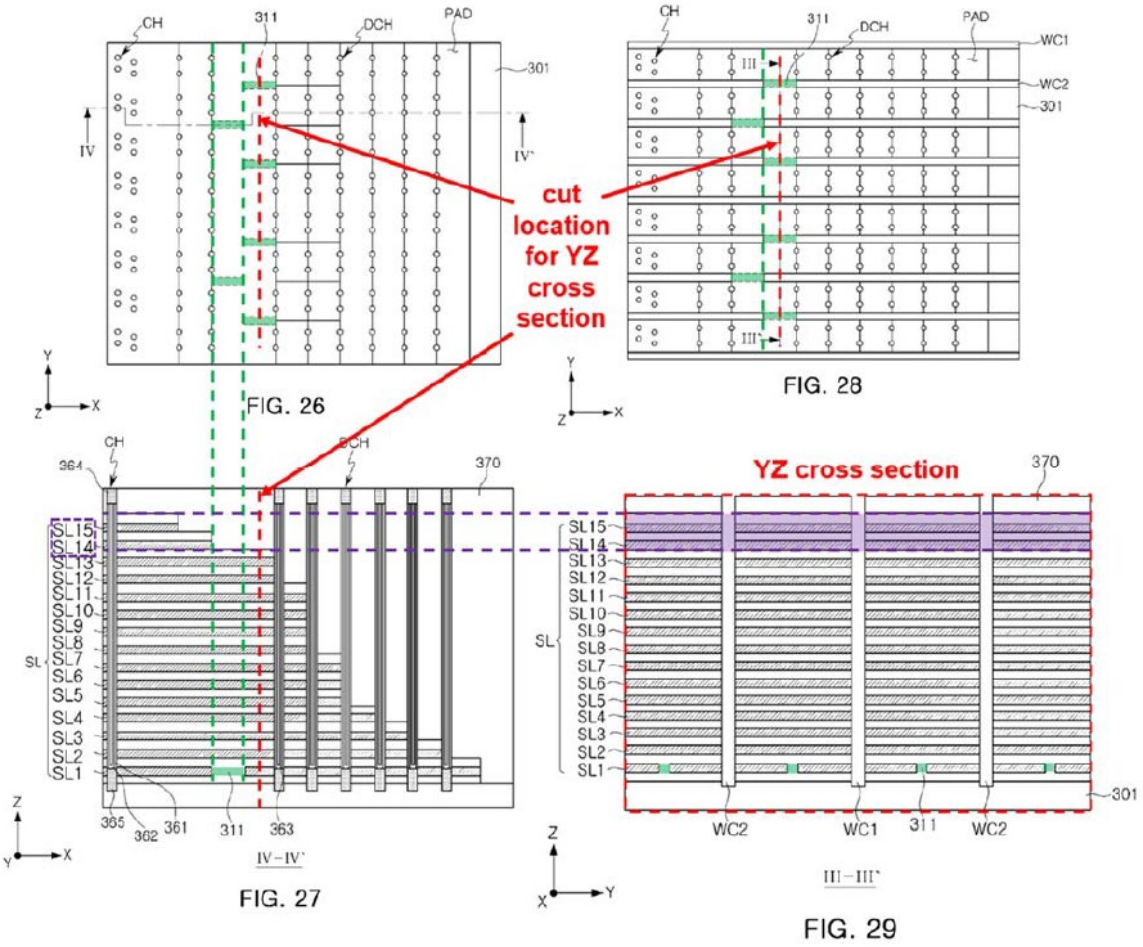
Ex. 1001, 24:4–10.

Petitioner asserts that Park's SSL layers GL14 and GL15 positioned over layers GL5–GL12, spaced apart by insulating layers, teach the claimed top select gate (TSG) positioned over word lines, spaced apart by a plurality of insulating layers. Pet. 39–40 (citing Ex. 1004, Fig. 36, 5:17–22, 16:9–11, 16:14–16; Ex. 1003 ¶¶ 196–201).

Petitioner asserts that although Park describes separately controllable unit areas in its TSG as in its BSG, Park does not provide any description of how its sub-TSGs are separated. *Id.* at 41. Petitioner asserts that a person having ordinary skill in the art would have considered the use of second dielectric trenches in the length direction of the substrate obvious in view of Park's use of such trenches to separate the BSGs into sub-BSGs. *Id.* (citing Ex. 1004, 5:67–6:4, 10:55–57, Figs. 3, 4, 11). Petitioner asserts that Park's use of common source lines in some embodiments to divide its SSL would not work for other embodiments because the SSL could not be completely divided by the common source lines without also dividing Park's word lines, which are meant to be electrically connected without division. *Id.* at 42 (citing Ex. 1004, 7:44–56, 16:22–26, 16:30–36, Fig. 36; Ex. 1003 ¶¶ 205–214). Petitioner asserts that to separate the SSL in those embodiments, it would have been obvious to use the type of isolation insulating layers 111 taught for use in the BSG as a routine, obvious extension of Park's existing teachings. *Id.*at 43–44 (citing Ex. 1003 ¶¶ 215–218, 220–223; Ex. 1016, 6:5–15, Fig. 4A; Ex. 1017, 7:40–44, Fig. 3; Ex. 1018 ¶ 58, Fig. 4B).

Patent Owner argues that Petitioner is wrong in reading Park to describe multiple embodiments, because Park describes a single embodiment in its Figures 18 through 36. PO Resp. 39–48 (citing Ex. 1004, 12:53–55; Ex. 2010 ¶ 103). Patent Owner argues that Park's Figure 36, upon which

Petitioner primarily relies, "includes an error and mistakenly shows all of the layers present in the device -- the top layers do not extend to where the cross section[al view of Figure 36] is located." *Id.* at 43–44. Patent Owner argues that Figure 36 represents a YZ cross-section along the "III-III'" line shown in Figure 28, which if aligned properly with the XZ cross-section of Figure 27 taken along the "IV-IV'" line shown in Figure 26, shows that there should be no top TSG layers in the area of the III-III' YZ cross-section. Patent Owner provides explanatory annotations of Figures 26–29:



Annotated Figures 26 through 28 show cut line III-III', highlighted in red on plan view Figure 28, incorporated into plan view Figure 26 and its IV-IV' cross-sectional view Figure 27. *Id.*; Ex. 1004, 3:5–12. Annotated Figure 29 highlights top layers SL14 and SL15 in purple, with dashed lines extending

to the layers SL14 and SL15 in Figure 27. Isolation layers 311 in SL1 are highlighted in green in each figure.

Patent Owner argues that when that error is accounted for, Park's top layers (TSGs) do not extend in the staircase regions of Park's device, and as such, do not extend over Park's insulation layers 111 (i.e., its "trenches"). *Id.* at 43 (citing Ex. 1004, 6:56–64, 7:60–8:6; Ex. 2010 ¶ 102).

Having reviewed the parties' arguments in light of the record, we determine that Petitioner has not shown by a preponderance of the evidence that claim 2 would have been obvious over Park. Regarding the alleged errors in Park, Petitioner states that "it is just as likely that it is Figure 27 -- and not all of Figures 21, 29, 31, 34, and 36 -- that wrongly depicts the TSG's physical extent." Pet. Reply 13.[6] However, Petitioner's burden is to show that the basis for its obviousness assertions are "more likely than not," not "just as likely," correct.

Petitioner relies on *LG Electronics v. ImmerVision* in support of its assertions based upon Park's contested figures, arguing that Figure 36 may be relied upon because it is unambiguous in its depiction and supported by multiple descriptions that layers SL14 and GL15 are meant to be the devices top "string select line[s]. Pet. Reply 11–12 (citing Ex. 1004, 16:26–30; 16:20–37; *LG Electronics v. ImmerVision*, 39 F.4th 1364, 1372 (Fed. Cir. 2022)). *LG Electronics* discusses an allegation that a certain teaching was "not . . . an actual teaching, but rather . . . an obvious error of a typographical or similar nature." *LG Electronics*, 39 F.4th at 1365. As discussed, the record reflects that a person having ordinary skill in the art

[6] We additionally note that Petitioner relies upon the correctness of Figure 27 for other assertions. *See, e.g.* Pet. 50 ("As exemplified by Figure 27 below, Park teaches what this claim requires").

would have recognized an inconsistency between at least Figures 27 and 36 that would have called into question the accuracy of either or both of those Figures. The obvious nature of the error is supported by Petitioner's lack of an alternative explanation for the inconsistency of the contested figures, Park's inconsistency in describing Figure 29 as a cross-section along both III-III' and IV-IV', Park's description of its staircase structure, and Dr. Kuhn's testimony that removal of the stepped structure would render Park's device inoperable. PO Resp. 45 n. 11 (citing Ex. 1004, 3:11–12, Fig. 29); Ex. 1004, 6:56–64; Ex. 2010 ¶ 102. Combined with Petitioner's explanation that the correctness of Figure 36 would be "just as likely," i.e., not more likely than its incorrectness, we determine that a person having ordinary skill in the art would have substantially discounted the conflicting teachings relied upon by Petitioner.

Beyond its reliance on such conflicting Figures, Petitioner asserts that Park provides a broad teaching that would include trenches in any particular location, including positions underneath Park's TSG layers. Pet. Reply 13 (citing Ex. 1004, 12:65–13:3; Ex. 1025 ¶¶ 23–24). Petitioner requires Park's teachings to be supplemented in two ways: that Park's isolation layers be placed under the TSG layers, and that Park's TSG layers be subdivided by isolation layers rather than common source lines. Petitioner admits that in Park's uncontested "embodiments," the common source lines are sufficient to subdivide its TSG layers. Pet. Reply 10. Thus, the only reason for isolation layers ("trenches") to be used in the TSG layers is if the TSG layers extend over an area for which common source lines may not be sufficient for such isolation. Petitioner has not provided any reason why Park teaches such extension of the TSG layers, except for the disputed Figures and the asserted breadth of Park's teaching. *Id.* at 11. Patent Owner has provided

credible reasons why such extension would not occur, citing the criticality of staircase structure lacking such upper SSL regions in providing pad regions to provide required electrical connections. PO Response 46 (citing Ex. 2010 ¶ 104), 43 (citing Ex. 1004, 6:56–64; Ex. 2010 ¶ 102). Patent Owner's arguments accord with Park's explicit disclosure, in which no isolating trenches appear in the TSGs because the common source lines perform the isolating function.

Petitioner also points to Park's statements that its connecting electrodes may be disposed in different positions in each gate electrode layer, with lower layers disposed below upper layers. Pet. Reply 12–13 (citing Ex. 1004, 8:59–9:2, 12:13–21, 12:65–13:13). However, Petitioner has not explained how such general descriptions support Petitioner's undescribed, particular configuration having TSG layers extending the full length of the BSG (or sufficiently so to extend over an isolation layer) in a manner consistent with Park's teaching of a staircase structure lacking such TSG layers in its staircase region. Based upon the totality of the evidence in the proceeding, we determine that Petitioner has not shown, by a preponderance of the evidence, that it would have been obvious to one having ordinary skill in the art to have looked to the teachings of dielectric trenches in Park's BSGs to provide one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs. Consequently, Petitioner has not shown that claim 2 would have been unpatentable as obvious over Park.

b) Claim 3–5, 7–9, and 11

Claims 3–5, 7–9, and 11 depend directly or indirectly from claim 2. Petitioner has not pointed to any teaching in its discussion of those claims that provides the limitation determined to be missing in claim 2.

Consequently, Petitioner has not shown that claims 3–5, 7–9, and 11 would have been unpatentable as obvious over Park.

c) Claim 6

Claim 6 depends from claim 1, and further recites, "further comprising: a plurality of dummy channel structures formed along the a height direction of the substrate that is perpendicular to the substrate, the plurality of dummy channel structures passing through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate." Ex. 1001, 24:26–32. Petitioner points to Park's dummy channels DCH extending perpendicular to the substrate through word lines WL, insulating layers, the lowest sacrificial layer that will be replaced with the BSG, and the substrate. Pet. 49–51 (citing Ex. 1004, Fig. 27; Ex. 1003 ¶¶ 244–252). Patent Owner does not contest this assertion. Upon review of the record, we determine that Petitioner's assertion is supported by the evidence, and that Petitioner has shown, by a preponderance of the evidence, that claim 6 would have been obvious over Park.

d) Claim 10

Claim 10 depends from claim 1, and further recites, "further comprising one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer." Ex. 1001, 24:48–53.

Petitioner points to Park's teaching that its dummy lines may be located between the GSL and word lines, and SSL and word lines, and that all of Park's gate electrode layers are separated from adjacent layers by insulating layers. Pet. 54–55 (citing Ex. 1004, 5:17–29, 16:9–17, 6:49–52,

10:34–45). Petitioner asserts that a person having ordinary skill in the art would have found it obvious that Park's isolation insulating layers 111 ("trenches") would pass through its dummy BSG layers as they pass through Park's BSG layers. *Id.* at 55. Petitioner asserts that Park describes that its dummy lines may be separated by the common source. *Id.* (citing Ex. 1004, 7:39–43). Petitioner asserts that use of the common source is only a non-limiting example in Park, and that a range of different structures were known, including separating all of the conductive layers, and that a single dielectric trench could divide multiple adjacent layers. *Id.* at 55–56 (citing Ex. 1003 ¶ 276; Ex. 1005, Fig. 3; Ex. 1018 ¶ 58). Because of the knowledge in the art, and because doing so would improve electrical performance, Petitioner asserts that a person having ordinary skill in the art would have found it obvious to have used dielectric trenches to divide Park's dummy BSG layers along with its BSG layers. *Id.* (citing Ex. 1003 ¶¶ 277–282).

Patent Owner argues that Park does not teach separation of its dummy lines into unit areas, but instead, that the dummy lines remain electrically connected within the blocks, just like the word lines. PO Resp. 49 (citing Ex. 1004, 7:30–43). Patent Owner further argues that Petitioner has not shown why a person having ordinary skill in the art would have found it obvious, because Petitioner merely states that it could have been done, and its purported advantage of improved electrical performance is based upon conclusory testimony not supported by evidence of record. *Id.*at 49–51 (citing Ex. 2010 ¶¶ 112–115). Patent Owner argues that Dr. Lee's conclusory assertions should be given no weight. PO Sur-reply 19 (citing *TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) ("[C]onclusory expert testimony is inadequate to support an obviousness determination.")).

Upon review of the evidence and arguments, we determine that Petitioner has insufficiently established its reason to apply dielectric trenches in Park's dummy BSG layers. Dr. Lee states that dummy cells suppress leakage current and hot-carrier injection, and play a role in data disturb characteristics. Ex. 1003 ¶ 281 (citing Ex. 1012, 130). However, Dr. Kuhn cites to the same source relied upon by Dr. Lee to show that these are source-to-drain effects, not lateral effects that would be affected by the asserted trenches in the dummy BSG layers. Ex. 2010 ¶ 113 (citing Ex. 1012, 130, 144). Dr. Lee attests that the use of trenches in dummy BSGs where TSGs are divided into sub-blocks using dielectric trenches would make loading effects more symmetrical, providing independent control. Ex. 1025 ¶¶ 28–29. However, we have determined in our discussion of Petitioner's claim 2 assertions that Petitioner has not shown the obviousness of dividing TSGs into sub-blocks using dielectric trenches. *Supra* § II.D.3.a. Absent trench-divided TSGs, Dr. Lee does not explain why the dummy BSGs, like the TSGs, may not be adequately subdivided by Park's common source lines as Park describes. Consequently, Petitioner has not shown that claim 10 would have been unpatentable as obvious over Park.

E. Obviousness over Park and Shibata

Petitioner asserts that claims 1–11 are obvious over Park in view of Shibata. Pet. 57.

1. Shibata

Shibata is titled "Semiconductor Memory Device." Ex. 1005, code (54). Shibata relates to a semiconductor memory device having multiple alternating conductive and insulating layers, in which the conductive layers include multiple word lines functioning as control gates of memory cells and select gates functioning as control gates of select transistors. *Id.* ¶ 3.

2. Park in view of Shibata

Petitioner asserts that Park teaches all limitations of claim 1 except for limitation [1.E]. Pet. 57. For limitation [1.E], Petitioner points to Shibata's separation portions 62a as dividing its drain-side select gate layer (i.e., its top select gate), causing the TSG to be divided into sub-TSGs. *Id.* at 58 (citing Ex. 1005 ¶¶ 2–3, 90, 166, Fig 16). Petitioner points to Shibata's description of those portions as "extending in the same direction as the separation portions 60 (the slits ST) piercing the entire stacked body 100." *Id.* at 59 (citing Ex. 1005 ¶¶ 65, 166). Petitioner asserts that one having ordinary skill in the art would have found it obvious to replace Park's second common source lines 105 with longer insulating regions 111 analogous to Shibata's separation portions 62a. *Id.* at 59. Petitioner provides the following illustration of its proposed combination:

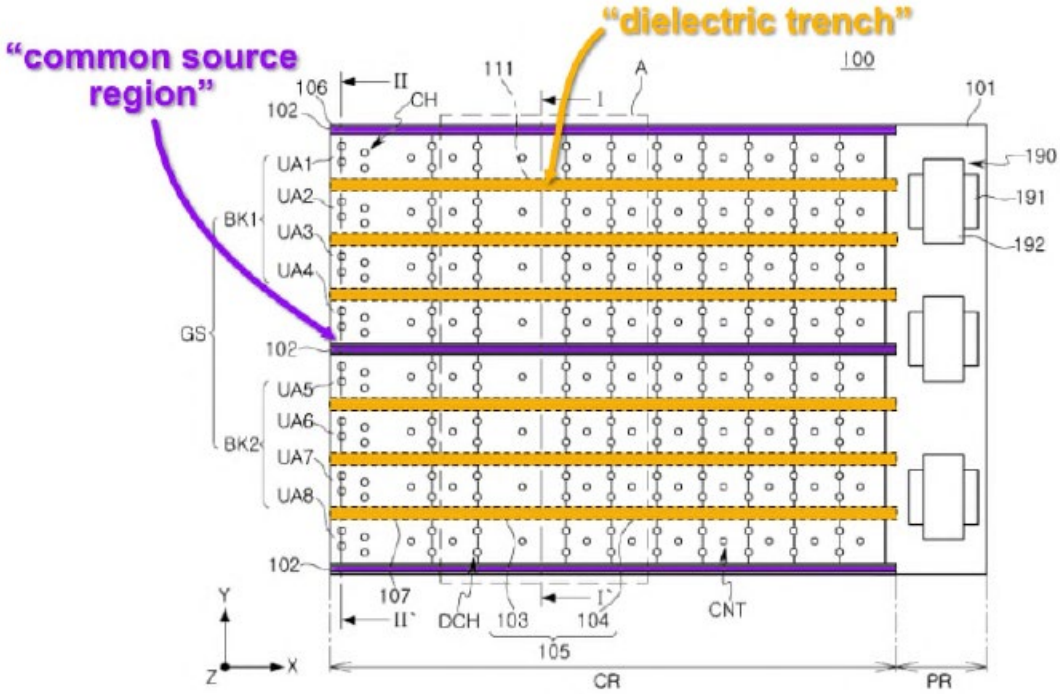


FIG. 3

Id. at 59–60 (citing and annotating modified Park Fig. 3). Petitioner's annotated Figure 3 from Park depicts a "top-down view" showing isolation

layers 111 (orange) replacing common source lines 105 and located between common source lines 102, extending lengthwise to separate the ground source line ("GSL"; i.e., the BSG) in blocks BK1 and BK2 into unit areas UA1–UA8 (i.e., sub-BSGs). *Id.* at 60. Petitioner's combination would likewise include such trenches into Park's TSG to allow Park's upper SSL to continue to be divided into individually controllable portions, thereby performing the function of the replaced common source regions in the TSG. *Id.* (citing Ex. 1005, 5:65–6:12, 7:19–29, 16:22–37).

Petitioner provides reasons to combine the teachings of Park and Shibata, including that such would be a routine, obvious design choice to divide select gates by trenches of insulation or common source regions. *Id.* at 61–62. Petitioner also asserts certain advantages for its combination, such as improving memory density or reducing device size. *Id.* at 61. We address Petitioner's assertions, and Patent Owner's arguments to the contrary, in the following analysis.

a) Patent Owner's "teaching away" arguments

Patent Owner first argues that Shibata teaches that its separation portions traverse only the upper select gate layers, and specifically teaches not to extend its separation portions to separate the bottom select gate layers.[7] PO Resp. 55–59 (citing Ex. 1005 ¶ 137). This argument does not address Petitioner's proposed combination. Petitioner proposes modifying Park to eliminate Park's second common source lines and replace them with longer versions of Park's BSG trenches analogously to Shibata's long dielectric separation portions in its TSG. Pet. 59. Accordingly, Patent

[7] Patent Owner's additional arguments concerning the "formed in the BSG" and "extend . . . to separate the BSG" limitations are based on deficiencies in Park, which are unavailing for the reasons discussed *supra* at § II.D.2.

Owner's argument does not decrease the persuasiveness of Petitioner's proposed combination.

Patent Owner next argues that Park teaches away from Petitioner's proposed combination because "Park actively discourages elongating the isolation insulating layers because the longer paths by which the etching solution must flow could prevent the complete removal of the sacrificial layer and cause voids in the gate electrode layers GLs." PO Resp. 60 & n.12 (citing Ex. 1004, 15:25–16:49; *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)). Patent Owner further argues that Park discourages placing isolating insulating layers side-by-side, as in Petitioner's proposed combination, because this "would block the flow of etching solution from the sides and again prevent the removal of sacrificial layers and formation of active layers." *Id.* at 60–61 (citing Ex. 2010 ¶ 136). Patent Owner points to Park's use of the common source line regions to deliver etchant that removes the sacrificial layer and to deposit conductive material that forms the gate electrode layers. *Id.* at 61 (citing Ex. 1004, 16:38–40). According to Patent Owner, Park's short isolation regions prevent such etchant delivery and metal deposition, and Park states that where the inflow passage of the etching solution is not properly secured, a portion of the sacrificial layer may remain without being removed. *Id.*at 62 (citing Ex. 1004, 15:56–59). Patent Owner argues that increasing the length of Park's isolation regions would increase the difficulty of providing etchant to all of the sacrificial layers, and may also leave voids of insufficient metal deposition. *Id.* (citing Ex. 1004, 16:44–49; Ex. 2010 ¶137).

As evidence that Park specifically discourages longer isolation insulating regions, Patent Owner points to Park's description of staggering even its short isolation layers 111. *Id.* at 63 (citing Ex. 1004, 15:60–16:2).

Patent Owner argues that such staggering would not be possible in Petitioner's full-width isolation layer combination. *Id.*(citing Ex. 2010 ¶139). Patent Owner argues that providing drive circuits, as proposed by Petitioner to remediate operability problems in the combination, would not address the etching or deposition problems identified by Park. *Id.* at 64. Patent Owner also argues that Petitioner's proposal to remove a number of common source lines in its combination would exacerbate the length of the long inflow paths, and thus worsen any etching and deposition problems. *Id.* at 68.

A reference may be said to teach away when a person of ordinary skill would be "discouraged from following the path set out in the reference" or "would be lead in a direction divergent from the path that was taken by the applicant." *Gurley*, 27 F.3d at 553; *Galderma Labs, L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013). We determine that although one embodiment of Park cautions against long or parallel isolation insulating regions, Park also describes that other techniques may mitigate the effects of long or parallel isolation insulating regions. Dr. Lee attests that Park describes other design and manufacturing approaches that are intended for differently sized and shaped layers 111 while minimizing any problems, including second dummy channel structures in the area of the layers 111, or vertical open regions 209, to shorten inflow passages, avoiding incomplete etching. Ex. 1025 ¶¶ 40–41 (citing Ex. 1004, 11:52–59, 12:10–52). Dr. Lee attests that use of such approaches is shown by Park to permit parallel insulating isolating regions 111, providing an annotated version of Park's Figure 17:

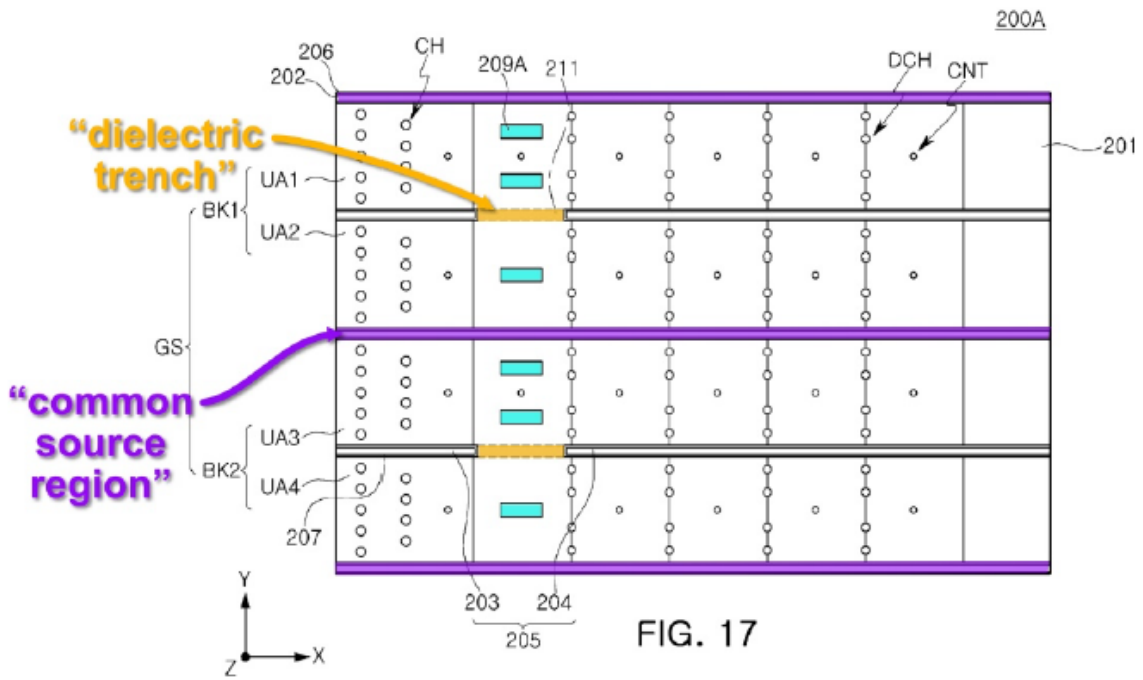


FIG. 17

Annotated Figure 17 of Park portrays open regions 209A in teal, dielectric trenches 211 (analogous to isolating regions 111 in Park's memory structure 100 embodiment relied upon by Petitioner) in yellow, and common source regions in purple. Park's use of parallel, longer isolating regions 211 in an alternate embodiment demonstrates that Park does not restrict its teachings to short, nonparallel isolating regions.

Further, Patent Owner admits that "Park suggests additional open regions [209A] may be effective" in the region shown in Figure 17 "to shorten the inflow passages." PO Sur-reply 24. Because Park suggests the use of additional open regions to shorten inflow, bypassing the restrictive insulating structures 211, Park does not teach away from alterations to its design that would lengthen inflow, such as longer isolation insulating regions. Thus, although Park acknowledges problems that may occur with longer or parallel insulating regions 111, Park's discussion of techniques to overcome those problems would encourage, not discourage, consideration of longer, parallel insulating regions.

Patent Owner argues that *only* the embodiment in Park relied upon by Petitioner may be considered in determining whether Park teaches away. PO Sur-reply 23–24. However, *Gurley* refers to the path set out in "the reference," i.e., the entirety of the reference. *Gurley*, 27 F.3d at 553. Park cannot fairly be said to lead away from parallel trenches or longer trenches because it also discloses parallel trenches and describes techniques to address issues that may arise when longer trenches are used.

We further disagree with Patent Owner that Petitioner's Reply improperly discusses why Park does not teach away because such discussion was not present in the Petition. PO Sur-reply 23. A petitioner may file a reply to a patent owner response that responds to arguments raised in that response or in the patent owner preliminary response. 37 C.F.R. § 42.23(b). Here, Patent Owner's Response and Patent Owner's Preliminary Response raised the issues relating to teaching away (Prelim. Resp. 43–44, PO Resp. 60), and Petitioner is permitted to address those.

b) Petitioner's "routine, obvious design choice" rationale

Patent Owner provides a broader argument that Petitioner has not provided sufficient reason to combine the teachings of Park and Shibata. PO Resp. 60–68. We begin with Petitioner's assertion that its combination "amounts to nothing more than a routine, obvious design choice" because it was known that select gates can be divided into individually controllable portions by either trenches of insulation or common source regions." Pet. 61–62 (citing Ex. 1003 ¶¶ 315–316).

In the absence of countervailing evidence, where "there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options." *KSR*, 550 U.S. at 421. We again consider the above-discussed statements of Park as to unfavorable

manufacturing issues that may result from parallel or longer trenches, and as to Park's techniques for mitigating such issues. *Supra* § II.E.2.a; *Arctic Cat, Inc. v. Bombardier Recreational Products, Inc.*, 876 F.3d 1350, 1363 (Fed. Cir. 2017) ("Evidence suggesting reasons to combine cannot be viewed in a vacuum apart from evidence suggesting reasons not to combine," even if the "evidence may not rise to the level of teaching away"). As discussed, Patent Owner presents substantial countervailing evidence as to the predictability of extended insulation length as a substitute for common source regions in a system taught by Park. Petitioner's recourse to multiple add-on structures, such as Park's additional open regions 209 (Petitioner's Reply 18–19) or Shibata's additional drive circuit (Petition 62), to rectify potential problems resulting from substituting insulation for commons source areas further indicates that insulation and common source regions are not simply interchangeable. *See Arctic Cat*, 876 F.3d at 1363–64 (finding that "potential hazards of the combination" indicated that the combination "would not have been a predictable solution yielding expected results."). Consequently, Petitioner has not persuasively shown that a person of ordinary skill in the art would have considered extended insulation length as a predictable substitute for common source regions, such that the mere existence of extended insulation length provides sufficient reason to perform such a substitution.

c) Petitioner's asserted advantages from its combination

We turn next to Petitioner's asserted advantages for substituting extended insulation length for Park's common source regions. Petitioner asserts that such substitution would reduce the planar size of the memory cell array or increase its memory density. Pet. 61 (citing Ex. 1005 ¶¶ 118, 154). Petitioner points to additional evidence in the record that reduction of

common source regions would be advantageous. *Id.* (citing Ex. 1009 ¶ 1 ("a large number of source contacts in a memory array … degrade the efficiency of the memory array and result in a large die size and a high fabrication cost")). Petitioner relies on testimony from its declarant, Dr. Lee, that the asserted replacement would result in a smaller device with additional memory density and would still perform its intended function. *Id.* (citing Ex. 1003 ¶¶308–314).

Patent Owner does not contest Petitioner's assertion that replacement of common source regions would result in a smaller memory array area. PO Resp. 68 ("reducing the number of common source lines may lead to a reduction of the memory array area"). However, Patent Owner argues that such reduction would result in multiple undesirable effects; i.e., a significant trade-off in memory device performance, including in speed, thermal management, reliability, longevity, accuracy, and device scalability. PO Resp. 68 (citing Ex. 2010 ¶145).

We determine that Petitioner has not shown that its combination would be viewed as advantageous. The Federal Circuit has recognized that "[a] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine." *Allied Erecting & Dismantling Co. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016) (alteration in original). However, Petitioner does not argue, and the evidence does not show, that the advantages accruing from decreasing the amount of common source layers would outweigh the disadvantages of a poorly formed memory structure.

Petitioner's combination would result in deleterious etching and deposition problems. Both parties agree that Park's common source regions (specifically, the openings that are later filled with common source material)

provide the passage through which etchant removes the sacrificial layers and by which gate electrode layers are deposited. PO Resp. 61 (citing Ex. 1004, 15:35–37, 15:20–22, 16:38–40); Pet. Reply 17–18. Both parties also agree that replacing common source regions with an insulator would block, in the replaced areas, such passage of etchant and depositing material, increasing the risk of incomplete gate electrode layers in the final memory device. PO Resp. 60–62; Pet. 62 (citing Ex. 1004, 15:35–16:2); Ex. 1025 ¶ 35. Petitioner admits that such blocking of etchant in its combination would have certain drawbacks; i.e., increased risk of poorly etched sacrificial layers. Pet. Reply 17 (citing Ex. 1004, 15:35–63). Petitioner does not contest that, absent some modification to Park, this would result in numerous undesirable properties of the resulting memory structure. *See id.* at 17–20 (presenting techniques to compensate for "any etching problem that may be encountered when using wet etching.").

We have reviewed Dr. Kuhn's testimony on these adverse effects from reducing the number of common source lines, and determine that such testimony is well supported by evidence. Ex. 2010 ¶ 144 (including "higher resistances in the remaining source lines leading to degraded read and write speeds" (citing Ex. 2002, 6), "increase[d] heat generation and associated failure mechanisms due to higher currents carried in the remaining source lines" (citing Ex. 2005, 2; Ex. 2006, 8), "increase[d] electrical stress on the remaining source lines leading to a reduced device lifespan" (citing Ex. 2004, 6–7), "caus[ing] significant voltage drops across the remaining source lines, adversely affecting the accuracy of reading, writing, programming, and erasing operations of the memory device" (citing Ex. 2003, 2–3)). These indicate significant drawbacks to Petitioner's combination.

Petitioner's putative advantages are based on improving the efficiency of a working memory array. Petitioner does not attempt to explain how the significant drawbacks of the combination (absent adding features discussed *infra*) are outweighed by efficiency gains due to reduction of common source regions. *See Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 (Fed. Cir. 2000) (stating that when considering whether a trade-off is desirable, the "benefits, both lost and gained, should be weighed against one another").

Consequently, Petitioner has not shown that a person having ordinary skill in the art would recognize any net advantage by combining the teachings of Park and Shibata.

d) Petitioner's reference to known techniques to overcome the combination's etching disadvantages

However, Petitioner points to four additional techniques that a person of ordinary skill in the art might use to augment its combination of Park and Shibata to minimize the above-described risks of incompletely formed gate layers. Pet. 62.

First, Petitioner proposes the use of Shibata's "'drive circuits' . . . in each individually controllable memory unit to maintain proper device operation." *Id.* (citing Ex. 1005 ¶¶ 324, 325, 446–449). Second, Petitioner argues that dry etching is another additional technique that a person having ordinary skill in the art would understand as causing less risk of etching problems than Park's wet etching solution. Pet. Reply 18. Third, Petitioner points to Park's embodiment in which dummy channel structures DCH2 may be formed near layers 111 to shorten inflow passages of the etchant. *Id.* (citing Ex. 1004, 11:52–55, Fig. 14). Fourth, Petitioner points to another embodiment in Park in which open regions 209 or 209A may be used to

shorten the inflow passages of both the etchant and the conductive material so as to provide full access to the sacrificial layers, permitting slightly longer trenches that are not staggered from each other. *Id.* at 18–19 (citing Ex. 1004, 12:50–52, Fig. 17).

We determine that Petitioner has not shown sufficient reason to combine the teachings of Park and Shibata. Petitioner does not sufficiently explain why one of ordinary skill in the art would consider any or all of Shibata's drive circuits, a dry etchant, Park's dummy channel structures, or Park's open regions would represent a desirable tradeoff such that it provides rationale to combine the teachings of Shibata with Park in spite of the combination's substantial disadvantages. *See In re Fulton*, 391 F.3d 1195, 1120 (Fed. Cir. 2005) ("Trade-offs often concern what is feasible, not what is, on balance, desirable. Motivation to combine requires the latter.")).

With respect to augmenting Petitioner's combination with Shibata's drive circuits, Petitioner argues that because Shibata's drive circuits are for the purpose of accommodating longer trenches in which the deposited metal gates are narrower and create increased resistance, there is no reason why those circuits would not work properly in Park for the same purpose. Pet. Reply 19–20 (citing Ex. 1005 ¶¶ 325, 446–450). However, Patent Owner raises concerns about such a solution: (1) that it does not address the creation of voids due to insufficient deposition, (2) that such drive circuits at the top of the stack in Shibata do not address difficulties in connecting drive circuits at the bottom the stack in Park, and (3) that such drive circuits are a fixed solution that would not address unpredictable variations in word line quality due to variations in efficient flow paths. PO Resp. 64–65 (citing Ex. 1004, 9:31–35, 15:56–49, 16:44–49; Ex. 1005 ¶¶ 325, 447, 448; Ex. 2010 ¶ 140).

With respect to substituting a dry etchant rather than a wet etchant, Petitioner argues that use of a dry etchant would avoid the etching problems noted by Park to accompany longer, parallel insulating layers because dry etchants are "less inhibited by narrow paths and [are] capable of reaching confined regions more effectively." Dr. Lee attests that other known etching methods that do not employ Park's exemplary wet etching solutions, such as dry plasma etching, are "less inhibited by narrow paths and is capable of reaching confined regions more effectively," which would "ensure[] more consistent performance even in complex or confined structures" such that "the 'problem' discussed in Park would not arise when employing dry etching methods." Ex. 1025 ¶¶ 32–37; *see also* Pet. Reply 18 (citing Ex. 1026, 10:22–11:17 (attesting that dry etches such as plasma or electron beam etches were "foundational for many years").

However, Patent Owner argues that Petitioner's support for substituting dry etchant relies solely on Dr. Lee's conclusory statements and a textbook description of dry etching. PO Sur-reply 23. We agree that neither suggests that a POSITA would have found it obvious or expected success using these methods. Petitioner has not shown that a person having ordinary skill in the art would have recognized a dry etchant to improve etching in a system like Park's. Nor has Petitioner discussed if dry etching requires additional equipment or procedures, or explained why a person having ordinary skill in the art would consider dry etching to be beneficial despite such additional requirements or potential drawbacks. *Winner Int'l Royalty*, 202 F.3d at 1349. Even here, where Petitioner relies on features outside of its combination for the combination's desirability, it may not simply ignore the considerations of incorporating such features. *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1332 (Fed. Cir. 2019)

(finding nonobviousness where the feature to be combined (a sensor) required additional procedures (diverting oil through a heat dissipator) such that the combination would need those additional features or degrade faster, leading to "an unappetizing combination.").

With respect to Park's dummy channels and open regions, Petitioner argues that Park states that the use of Park's dummy channel structures completely avoids any degradation of the characteristics of the memory device that results from incomplete etching. Pet. Reply 18–19 (citing Ex. 1004, 11:55–59, 12:50–52, Fig. 17). By providing such embodiments, Petitioner asserts that Park allows for modifications of the size, shape, and location of its trenches. *Id.* at 19.

With respect to Park's dummy channel and open region embodiments, Patent Owner further argues that combining these embodiments so as to provide open regions in the active region would significantly reduce space dedicated to memory cells. *Id.* at 24. Patent Owner further argues that Petitioner attempts to combine separate embodiments of Park's memory device; i.e., embodiments 100 and 200A, without explaining why a person having ordinary skill in the art would do so. *Id.* (citing Ex. 2011, 88:1–7, 94:2–8). Patent Owner argues that these modifications of Park to minimize etching problems were not raised in the Petition. PO Sur-reply 23.

We agree that the Petition did not mention Park's dummy channel/open area embodiments, despite the fact that each teaching appears in the references applied in that combination, underscoring that these embodiments are not part of Petitioner's proposed combination. *See* PO Sur-reply 23. Similarly, the Petition mentioned Shibata's drive circuit only to support its argument that a person of ordinary skill in the art would have had reasonable success in lengthening Park's trenches to replace Park's

common source lines. Pet. 61–62. Petitioner may not now alter its original assertions to include those features within its combination.

Instead, Petitioner treats these methods as being known techniques in the art that a person having ordinary skill in the art would recognize as providing solutions to the etching problems identified by Park. *Id.*; Pet. Reply 21 ("a POSITA would have recognized that any problem areas could be readily addressed by (1) employing any of the methods Park teaches (such as the use of dummy channels to supplement flow) or (2) using Shibata's tailored drivers.").

However, neither Shibata nor Park indicates that such teachings of drivers or dummy channels, were "evidently and indisputably within the common knowledge of those skilled in the art." *See K/S Himpp v. Hear-Wear Techs.*, LLC, 751 F.3d 1362, 1365–66 (Fed. Cir. 2014); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362–1363 (Fed. Cir. 2013) (finding "a party's claim about what one of ordinary skill in the relevant art would have known" when the party "established [it as] a prevalent, perhaps even predominant method" by "citing to extensive references of record"). Shibata does not represent its drive circuits as knowledge in the art, but as part of its inventive semiconductor memory device. Ex. 1005 ¶¶ 443, 448–449. Similarly, Park describes its dummy channel and its open regions as "examples of the present inventive concept." Ex. 1004, 11:52–59; 12:10–52. We determine that Petitioner has not shown that these features of Park and Shibata represent the knowledge in the art that a person having ordinary skill in the art would take into account when contemplating Petitioner's combination. Because these features were not known in the art, and Petitioner did not assert them as part of its combination in the Petition, Petitioners reliance upon them is unpersuasive.

Even were these features to be considered part of the combination in the Petition, Petitioner's approach to Shibata's drive circuit and Park's dummy channel/open region teachings results in a deficiency in its showing of reasonable expectation of success for its expressed combination of extending Park's insulative trenches to replace some of its common source lines. Petitioner relies solely on the fact that the references are capable of performing the relied-upon functions or could possess the relied-upon structure. *See, e.g.,* Pet. Reply 19–20 (stating, "If Shibata accommodates this type of trench . . . there is no reason Park cannot as well," and "Park itself already presents a variety of ways to minimize any etching problem that may be encountered when using wet etching"). But Park does not describe its dummy channel or open region teachings as generally applicable to all of its embodiments. And Petitioner needs to show a reason why the application of Shibata would be reasonably expected to have been successfully applied in Park, not merely state that there is "no reason" to expect that it would not be successful. *See DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1377 (Fed. Cir. 2018) (finding that even where two structures have "the same physical structure," applying the teachings of one structure to the other requires "additional, reasoned analysis."). The knowledge of one skilled in the art cannot bridge this gap, because these are inventive features of Park and Shibata.

Furthermore, Petitioner also has not sufficiently explained, for any of its proposed augmentations, how metal gate deposition would occur sufficiently in the most remote regions of the long, parallel insulating layers in Petitioner's Park-Shibata combination of such regions to avoid the risk of incomplete gate electrode layers in the final memory device that Patent Owner argues would result in a significant trade-off in memory device

performance, including in speed, thermal management, reliability, longevity, accuracy, and device scalability. PO Resp. 68 (citing Ex. 2010 ¶ 145). For example, Dr. Lee addresses only etching issues, not deposition issues. Ex. 1025, ¶¶ 32–47.

For the above-described reasons, Petitioner has not shown that any of dry etching, Shibata's drive circuit, Park's dummy channel, or Park's open regions, alone or in combination, would have led one having ordinary skill in the art to view Petitioner's Park-Shibata combination as desirable despite its acknowledged etching and deposition related drawbacks.

e) Petitioner's alternate combination

Petitioner alternately asserts that only some of Park's common lines need be replaced with insulating layers. Pet. 62. Petitioner asserts that replacement of some of Park's common lines with insulating layers "ensures that the majority of sacrificial layers are removed and replaced with conductive material, thereby improving device performance without the need for separate drivers." *Id.* at 62–63 (citing Ex. 1003 ¶¶ 319–324). However, replacing fewer common lines would result commensurately in less of the advantages associated with such replacement. Thus, to the extent that a person having ordinary skill in the art would recognize improved etching and deposition by replacing fewer common lines, that person would also recognize less advantage to be gained by such replacement. Petitioner does not quantify a degree of replacement such that a person of ordinary skill in the art would find that the advantages of partial common source replacement outweigh the disadvantages. Therefore, Petitioner has not persuasively shown that partial source replacement would be recognized by a person having ordinary skill in the art as a reason to modify Park with the teachings of Shibata.

f) Determination

Petitioner has not shown, by a preponderance of the evidence, that claim 1 would have been obvious over the combined teachings of Park and Shibata as proposed by Petitioner. Although Park does not teach away from Petitioner's combination, Petitioner has not shown that a person of ordinary skill in the art would have found it obvious, either as a routine design choice or for the purpose of decreasing the memory array size, by replacing some of Park's common source lines with Shibata's insulating layers. As detailed above, the evidence of record indicates that such a course of action would be fraught with the risk of incomplete manufacture leading to potentially severe operational problems. The evidence does not indicate that the risk of such problems would be sufficiently ameliorated by dry etching, Shibata's drive circuits, Park's dummy channels, and/or Park's open regions such that a person having ordinary skill in the art would pursue these options and consider Petitioner's combination to be a desirable option.

These deficiencies extend to Petitioner's assertions on claims 2–11, which rely on the same reason to combine Park and Shibata. Pet. 39–49. Consequently, we determine that Petitioner has not shown, by a preponderance of the evidence, that any of claims 1–11 would have been obvious over the combined teachings of Park and Shibata as proposed by Petitioner.

3. Shibata in view of Park

In its alternative formulation of the Shibata-Park combination, Petitioner relies upon Shibata for all except the separation of bottom side select gates as set forth in limitation [1.e]. Pet. 63–81. Petitioner points to Shibata's Figure 16 for support (shown as annotated by Petitioner):

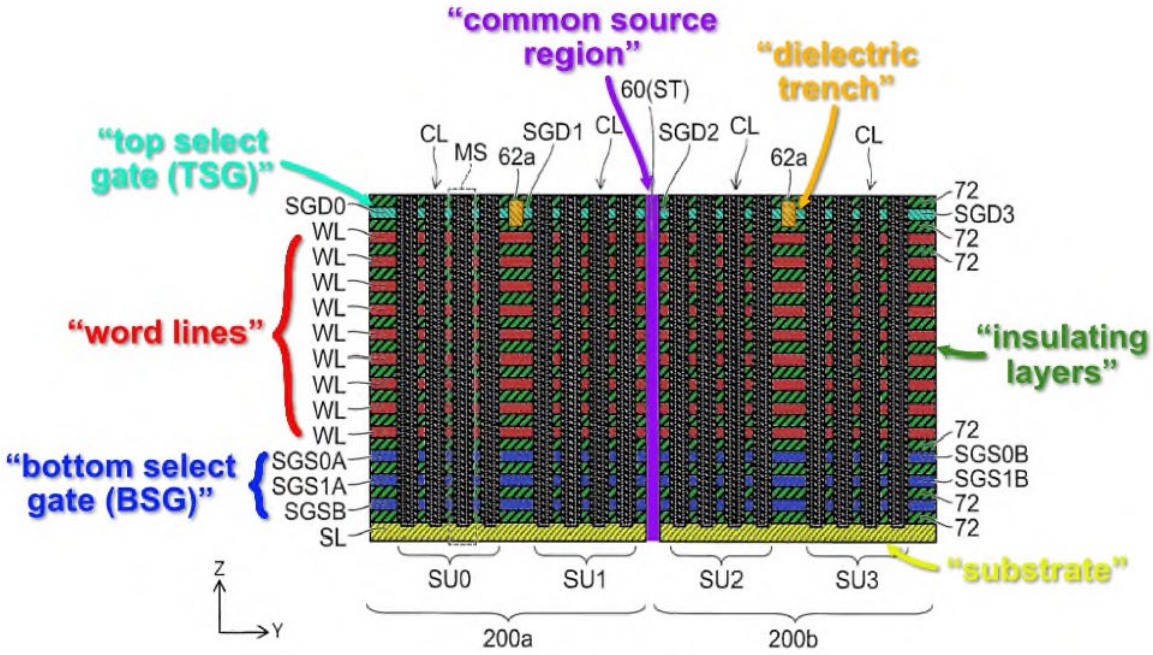


FIG. 16

Annotated Figure 16 shows a series of layers: bottom "substrate" layer SL, having an insulating layer 72 formed thereon, having three "bottom select gates (BSG)" SGSB, SGS1A, SGS0A formed thereon with insulating layers 72 therebetween, alternating "word lines" WL and insulating layers formed thereon, and "top select gate" SGD0 formed thereon with two "dielectric trenches" 62 forming a separation portion between different areas of the top select gate. *Id.* Petitioner asserts that it would have been obvious to replicate Shibata's dielectric trenches from its top select gate into its bottom select gate, and to use a single bottom select gate instead of Shibata's multiple bottom select gates, in view of Park's teaching of a single divided bottom select gate, so as to reduce the number of manufacturing steps and to reduce the load on the string unit drivers. *Id.* at 74–77 (citing Ex. 1003 ¶¶ 377–380, 385–393; Ex. 1004, Fig. 11, 5:67–6:12, 10:55–57). Petitioner further asserts that the "primary benefit . . . is increased memory size" because the number of word lines would be able to be increased. Pet. 76–77

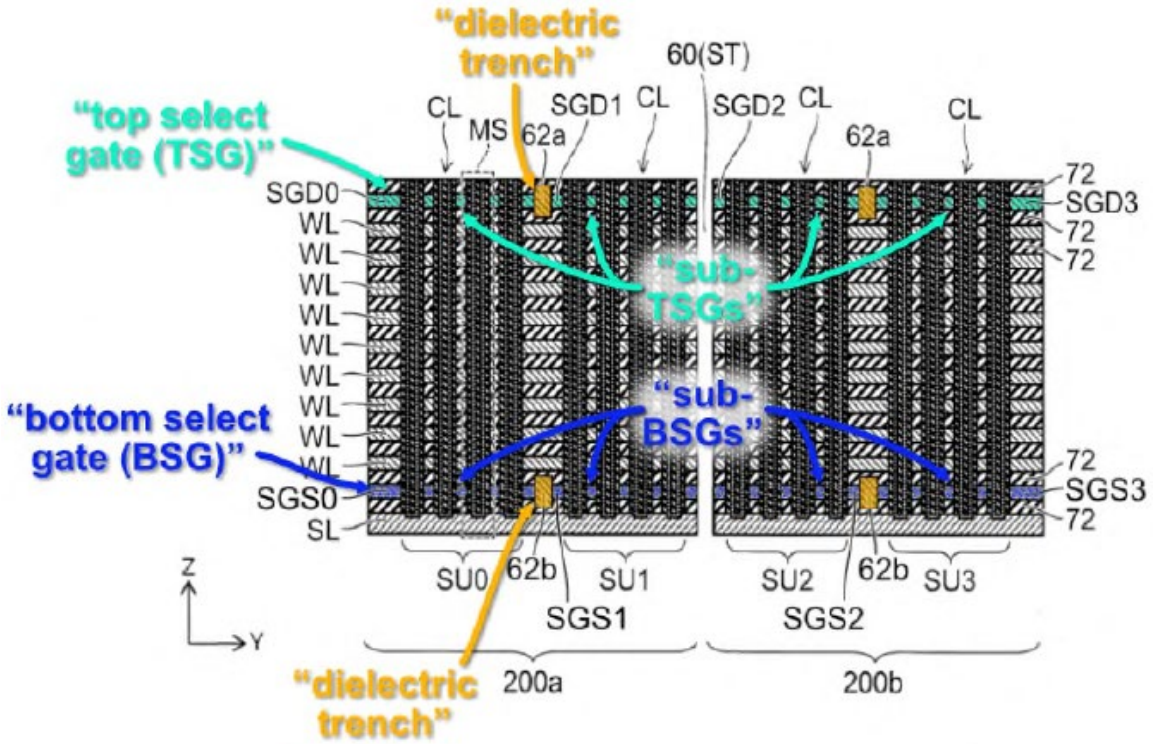
(citing Ex. 1003 ¶¶ 389–390); PO Sur-reply 24–25 ("The fact that Park allows Shibata's memory to include additional word line layers indisputably motivates combination.").

We determine that Petitioner has not shown, by a preponderance of the evidence, that it would have been obvious to one having ordinary skill in the art to combine the teachings of Shibata and Park. Petitioner's "primary benefit" is providing two additional word line layers in Shibata without altering the size of its memory device. Pet. Reply 24–25; Pet 77 ("the number of word lines could be increased without impacting the overall height of Shibata's stack") (citing Ex. 1003 ¶¶ 385–390; Ex. 1008 ¶ 2)). To do so, Petitioner points to a single reference in the prior art that uses a "hierarchical select gate configuration" to reduce an amount of memory cell string selection circuitry, and thereby increase device density. Pet. 77 (citing Ex. 1008 ¶ 66). Guided by this, Petitioner asserts, a person of ordinary skill in the art would have been motivated to look for design alternatives to Shibata's three-level BSB string control to reduce its size, and would have found a desirable alternative in Park's single, partitioned BSG layer. Pet. 74–76 (citing Ex. 1003 ¶¶ 380–382).

Patent Owner does not contest that two additional word line layers would be beneficial, but argues that Park's teachings are inapposite to Shibata because Park's isolation teachings are short sections confined to the staircase region, and Shibata does not have a staircase region, instead having end-to-end isolation structures in the array (not staircase) section of its TSG (not its BSG). PO Resp. 73–75 (citing Ex. 1004, Fig. 3, 10:56–60; Ex. 1005, 47A, Ex. 2010 ¶ 157; Pet. 69 ("Shibata does not reference a staircase")); PO Sur-reply 29.

Petitioner does not contest that Park's trenches are used outside the staircase region. Pet. Reply 23. Instead, Petitioner argues that Shibata teaches the use of separation portions 62a that "span the entirety of its memory," and that the combination therefore teaches trenches that may span the entirety of a memory. *Id.* (citing Ex. 1005, Fig. 47A). Yet Petitioner does not squarely address why a person having ordinary skill in the art would substitute in this manner, relying instead on the argument that they could so substitute. However, "[o]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated* to make the combinations or modifications of prior art to arrive at the claimed inventions." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015).

As pointed out by Patent Owner, Petitioner is not simply substituting a component from Park (such as Park's BSG divided by isolation regions 111 into sub-BSGs) into the device of Shibata. Instead, Petitioner depicts its combination as duplicating Shibata's top separation portions 62a, originally present in its TSG, and placing those into its BSG, as shown in Petitioner's demonstrative Figure:



Pet. 76. Petitioner explains that it is Shibata's TSG separation teaching (not Park's) being added to Shibata's BSG in its combination, because "these new portions 62b would match the existing portions 62a in position and dimension to ensure that the select gates continue to allow for the independent control of the memory on the same unit-basis taught in Shibata." *Id.* at 75–76 (citing Ex. 1003 ¶¶ 381–384).

In this way, Petitioner relies on Park as a "design alternative" to redesign the memory of Shibata. Ex. 1003 ¶¶ 380–381. However, Dr. Lee's motivation to consider other design alternatives is not to gain any new advantage, but to "allow for the same type of control Shibata already provides" and "to continue [to] provide the benefits associated with such control." *Id.* ¶ 380. This testimony does not explain why an "alternative" is needed to provide benefits already present in Shibata.

Dr. Lee's testimony illustrates the disconnect in Petitioner's reasoning. Petitioner relies on the prior art for a goal, i.e., adding word lines

to a memory stack without impacting the overall height. Ex. 1003 ¶¶385–386. Petitioner also relies on the prior art for a clue in reaching that goal; i.e., that it could be met by reducing an amount of memory cell string selection circuitry. *Id.* ¶ 390. Petitioner then relies on Park for a design alternative to do such reduction. *Id.* ¶ 388. However, Park does not teach reduction of memory cell string selection circuitry. Park simply has a divided BSG using isolation layers to control memory string circuitry. *Id.* ¶¶ 102–104, 381. Park's BSG teaching does not improve Shibata, which already has memory string circuitry that performs such control. *Id.* ¶ 381.

Thus, the improvement to Shibata (replicating its TSG layer to form a single layer BSG layer and replacing the excised BSG layers with word line layers) does not come from Park. Nor does it come from the prior art, except broadly speaking as a goal to be achieved. No teaching was identified to guide a person of ordinary skill in the art to remove two BSG layers from Shibata and replace them with word lines. The impetus for Petitioner's improvement comes from Petitioner's own creation of a new design of Shibata. The only reason of record for Petitioner to have done so is the recreation of Patent Owner's claim 1. However, a reason to combine should be found in the art, not in the challenged patent. *KSR*, 550 U.S. at 421 ("A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning."); *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) ("[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention."). As argued by Patent Owner, we determine that Petitioner's creation of a Shibata-Shibata combination, based on incomplete "design guidance" from Park, amounts to "impermissible hindsight." PO Resp. 55.

We are not persuaded by Petitioner's other purported advantages to the combination. Patent Owner argues that Petitioner's motivation is conclusory and hindsight-based and, therefore, insufficient. PO Resp. 69, 72–73. Patent Owner argues that the asserted benefits (reducing height and manufacturing steps) would not be achieved because a person having ordinary skill in the art would have recognized that reducing Shibata's bottom gate layers from three to one would have required additional manufacturing steps and make Shibata's memory array taller. *Id.* at 73, 77–78 (citing Ex. 1003 ¶¶ 377–380; Ex. 2010 ¶ 156).

We agree with Patent Owner that the evidence does not support Petitioner's assertion that modifying Shibata as proposed by Petitioner would simplify manufacturing. As pointed out by Patent Owner, both declarants agree that such a modification requires at least an additional mask step and an etching step. PO Sur-reply 30 (citing Ex. 1025 ¶¶ 60–62). Dr. Lee states, "application of Park would in fact reduce manufacturing steps: Shibata's six step process (3 gate depositions, 3 insulating layer depositions) would be reduced to four (1 gate deposition, 1 mask, 1 etch, 1 insulating layer deposition)." Ex. 1025 ¶ 62. However, Patent Owner argues that "not all steps are equal," because Dr. Lee testifies that a mask step requires 8 steps to perform, and requires movement of the wafer to a separate room. PO Sur-reply 30 (citing Ex. 2011, 20:19–22:13, 37:22–38:16, 49:11–50:11, 23:6–25:2). Patent Owner further cites Dr. Lee's statement that alignment of the wafer for photolithography is "extremely critical," and argues that the masking process adds additional complexity. Based on the testimony of Drs. Lee and Kuhn, we determine that Petitioner has not shown that modifying Shibata would simplify manufacturing, but would instead increase its

complexity such that Petitioner's proposed modification would be considered less advantageous by a person having ordinary skill in the art.

With respect to Petitioner's assertion that the combination would reduce the size of the memory array, Petitioner has not provided sufficient explanation in light of Patent Owner's arguments to the contrary. PO Resp. 73. Instead, Petitioner states that applying Park would allow the number of word lines to be increased "without impacting the overall height of Shibata's stack." Pet. Reply 24. In view of the above-discussed reliance on hindsight reasoning and insufficiently explained reasonable expectation of success, Petitioner has not persuasively shown that its combination would reduce the height of the memory array so as to provide motivation to combine the teachings.

With respect to Petitioner's argument that the combination would reduce the load on the drivers associated with each of the various sub-units, the only supporting evidence is a single statement to that effect from Dr. Lee. Ex. 1003 ¶ 393; Pet. 77 (citing same). Because Dr. Lee does not explain why such load reduction would be recognized as advantageous; i.e., whether it provides a noticeable or a minimal reduction in driver load, and because the statement is otherwise unsupported by evidence, we assign minimal weight to this statement.

Patent Owner further argues that Petitioner has not supported its assertion that it was "well known that trenches of dielectric material could be used to divide select gates." PO Resp. 76 (citing Pet. 78; Ex. 2010 ¶ 159). Patent Owner argues that the cited references show no more than Shibata; i.e., division of the top select gate. *Id.* (citing Ex. 1016, 6:5–15, 10:15–18, Fig. 4A ("uppermost gate electrode layer"); Ex. 1017, 7:40–42, Fig. 3 ("cutting insulation pattern 118" affecting "string selection gate

electrodes 202"); Ex. 1018 ¶ 58, Fig. 4B ("upper electrodes ELb located at the highest level")). However, Petitioner only asserted that it was well known "that trenches of dielectric material could be used to divide select gates" (Petition 78); as such, Petitioner's evidence relating to the top select gates is sufficient to support that assertion. Nevertheless, we agree with Patent Owner that the cited references appear to show no more than that described by Shibata or Park, and that Petitioner does not show that it was well known in the art to separate a BSG as set forth in claim 1.

We additionally consider as a whole all of the evidence and arguments presented for and against Petitioner's combination. To the extent that record reflects potential advantages (decreased height or increased memory density), the record also reflects potential disadvantages (increased manufacturing difficulty). Moreover, the record reflects that Petitioner has not established a persuasive reason why a person having ordinary skill in the art would have viewed the general teachings of Park and found reason to make the specific asserted alterations in Shibata that go beyond merely incorporating specific features in Park. Instead, we determine that any advantages identified by Petitioner result only from hindsight reconstruction of the claims. Consequently, the totality of the evidence does not support Petitioner's assertion that it would have been obvious to combine the features of Shibata in view of Park. These deficiencies extend to Petitioner's assertions on claims 2–11, which rely on the same reason to combine Shibata and Park. Pet. 39–49. Consequently, we determine that Petitioner has not shown, by a preponderance of the evidence, that any of claims 1–11 would have been obvious over the combined teachings of Shibata and Park as proposed by Petitioner.

III. CONCLUSION

After reviewing the record and weighing the evidence proffered by both parties, we determine that Petitioner has shown by a preponderance of the evidence that claims 1 and 6 are unpatentable, and that Petitioner has not shown by a preponderance of the evidence that claims 2–5 and 7–11 are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–11	103(a)	Park	1, 6	2–5, 7–11
1–11	103(a)	Park, Shibata		1–11
1–11	103(a)	Shibata, Park		1–11
Overall Outcome			1, 6	2–5, 7–11

IV. ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner has established by a preponderance of the evidence that claims 1 and 6 are unpatentable; and

ORDERED that Petitioner has not established by a preponderance of the evidence that claims 2–5 and 7–11 are unpatentable, and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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