

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00795
U.S. Patent No. 11,501,822
Issue Date: November 15, 2022

Title: NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,501,822
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,501,822 B2 to Jia et al.
1002	File History of U.S. Patent No. 11,501,822 B2 to Jia et al.
1003	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
1004	U.S. Patent No. 10,121,529 B2 to Lee (“Lee”)
1005	U.S. Patent No. 10,643,718 B2 to Zhao et al. (“Zhao”)
1006	Aritome, “NAND Flash Memory Technologies” (2016)
1007	Brown et al., “Nonvolatile Semiconductor Memory Technology” (1998)
1008	Cappelletti, et al., “Flash Memories” (1999)
1009	U.S. Patent No. 9,589,978 to Yip
1010	U.S. Patent No. 10,726,920 B2 to Yang
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1013	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1014	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1015	File History of U.S. Patent No. 11,081,164 (Appl 16-709,944) to Jia et al.
1016	File History of U.S. Patent No. 11,862,230 (Appl 17-965,527) to Jia et al.

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Exhibit	Description
1017	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
1018	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL

I. Introduction

Petitioner requests IPR of claims 1-9 and 11-19 of U.S. Patent 11,501,822 (“the ’822 patent”), assigned to Yangtze Memory Technologies Co., Ltd. (“Patent Owner”).

The ’822 patent relates to NAND memory devices. Quintessential prior art NAND memories are formed from numerous “strings” of memory cells. The cells in each string are connected in series. A top “select gate line” located at the string’s drain-side controls connection of the string to a bit line. This select gate is followed by a series of word lines that control access to the string’s memory cells. The string also includes a lower “select gate line” on the string’s source-side that controls connection to a lower common source. The word lines are selected one at a time—typically starting at the string’s source-side and moving towards the drain-side—and program voltages are applied to store data in the string’s memory cells.

The ’822 patent seeks to improve on this type of prior art NAND memory device by employing specific voltages during programming. The patent discusses a two-step programming process: the various lines connected to a NAND string are first pre-charged, and then programming voltages are applied. The patent tailors the applied pre-charge voltages to avoid a phenomenon known as “program disturb.” “Program disturb” involves the inadvertent programming of memory cells—either in adjacent strings or in the same string—not currently selected for programming.

To avoid program disturb, the '822 patent applies different pre-charge voltages to different groups of word lines. The broadest claims—like independent claims 1 and 11—simply require the application of three different voltages to three different groups of word lines. The patent's narrower claims—like dependent claims 2-3 and 12-13—require that the pre-charge voltage applied to a group must increase the further the group is away from the word line currently selected for programming.

There was nothing new about this. This Petition focuses on three exemplary references: (1) U.S. Patent No. 10,121,529 B2 (Ex. 1004, "Lee"), (2) U.S. Patent No. 10,643,718 B2 (Ex. 1005, "Zhao"), and (3) U.S. Patent No. 10,726,920 B2 (Ex. 1010, "Yang"). Lee, Zhao, and Yang—just like the '822 patent—all teach NAND memories that apply three different voltage pulses to three different groups of word lines during a pre-charge period for purposes of reducing program disturb.

Ground 1 focuses on Lee. Lee teaches a NAND memory with word lines grouped into, for instance, four groups. Just as the '822 patent requires, Lee applies increasingly higher pre-charge voltages to the wordline groups as the distance from the selected word line increases. This renders claims 1-3, 6, and 12-13 obvious.

Ground 2 focuses on Zhao. Zhao groups its NAND word lines into three groups depending on their location relative to the selected word line. Different pre-charge voltages are applied to the different groups. All the word lines on the drain-side of the selected word line are supplied with "Vprecharge." The first two adjacent

word lines on the source-side of the selected word line are supplied with “Vbypass.” The remainder of the source-side word lines are supplied with “Vss.” This renders all the broader claims that do not require a specific group ordering—including claims 1, 4-7, 9, 11, 14-16, and 18-19—obvious.

Ground 3 focuses on the combination of Zhao and Lee. Again, in Zhao, all of the drain-side word lines are supplied with “Vprecharge” during the pre-charge period. Lee explains that this approach may not be sufficient to mitigate program disturb. Lee improves program disturb resistance by dividing the drain-side word lines into multiple groups and applying increasingly higher pre-charge voltages to the different groups. Applying this teaching to Zhao renders claims 1-9 and 11-19 obvious.

Ground 4 focuses on Yang. Yang provides yet another example of a reference that applies different pre-charge voltages to different groups of word lines. Yang considers both word line position and prior programming when determining an appropriate pre-charge voltage. Word lines on the drain-side of a selected word line that do not connect to any previously programmed cells are supplied with “Vbypass.” Word lines on the drain-side of a selected word line that do connect to previously programmed cells are supplied with “Vpre_OD.” All dummy word lines are supplied with “Vpre_dmy.” Yang also provides an example where these groups are ordered in the way the ’822 patent’s narrower claims require. This renders claims

1-7, 9, 11-16, and 18-19 obvious.

II. Mandatory Notices

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. (“MTI”) and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

Patent Owner YMTC has asserted the ’822 patent and U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each of these asserted patents: IPR2024-00788 (’378 patent), IPR2024-00789 (’872 patent), IPR2024-00790 (’031 patent), IPR2024-00791 (’806 patent), IPR2024-00794 (’623 patent), IPR2024-00792 (’957 patent), and IPR2024-00793 (’342 patent).

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

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Petitioner consents to service by electronic mail at the following addresses: P52PTABDocket@orrick.com, PTABDocketJJL2@orrick.com, PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. Requirements for IPR

A. Grounds for Standing

Petitioner certifies that the '822 patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '822 patent on November 14, 2023. This petition was filed within 1 year of this date.

B. Identification of Challenge and Statement of Precise Relief Requested

Petitioner requests IPR of claims 1-9 and 11-19. This petition discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and is supported by the accompanying Declaration of David Kuan-Yu Liu, Ph.D. (“Liu,” Ex. 1003), a leading expert in the NAND field.

The application underlying the ’822 patent—U.S. App. 17/353,272—was filed June 21, 2021 and facially identifies itself as a continuation of a chain of applications leading back to an October 22, 2019 PCT filing. EX. 1001, Cover.

Petitioner relies on the following references: (1) Lee (Ex. 1004), (2) Zhao (Ex. 1005), and (3) Yang (Ex. 1010). These references are all prior art. *See* Section VIII.

Petitioner challenges the claims on the following grounds:

Ground 1: Claims 1-3, 6, and 11-13 obvious over Lee;

Ground 2: Claims 1, 4-7, 9, 11, 14-16, and 18-19 obvious over Zhao;

Ground 3: Claims 1-9 and 11-19 obvious over Zhao in view of Lee; and

Ground 4: Claims 1-7, 9, 11-16, and 18-19 obvious over Yang.

IV. Institution Should Be Granted

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds for a § 314 Discretionary Denial in this Case

There is a pending district court action involving the '822 patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of a parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '822 patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“*Fintiv*”). In particular: the district court may stay the case, any potential trial will occur years from now, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 12 (similar).

2. Proximity of the Court's Trial Date

On February 22, 2024, the district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1018. As a result, if IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1014 (statistics indicating that it takes on average 48.9 months to reach trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are months away from the exchange of infringement and invalidity contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Here, Patent Owner asserted eight different patents against Petitioner. *See* Ex. 1013. Yet, Petitioner proceeded with diligence filing a mere five months after being served with the original complaint and a little over two months after the filing of an amended

complaint. *See id.* This also weighs strongly in favor of institution.

4. Issue Overlap

Given the early stage of the parallel proceeding, it is not yet possible to determine the amount of overlap. Patent Owner has not yet served infringement contentions or identified the asserted claims. Moreover, should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under § 325(d) Would Be Inappropriate

The Patent Owner did not cite Lee, Zhao, or Yang during prosecution of the '822 patent or its parent application and the Examiner did not consider them. *See*

generally Ex. 1002, Ex. 1015. And as explained in this Petition, these references group word lines and apply different pre-pulse signals to the groups, which is the alleged point of novelty. This alone merits institution.

What's more, Lee, Zhao, and Yang are meaningfully different from the art that the Examiner did discuss. The Chen and Kim references, which the Examiner used to reject the claims in the '822 patent's parent, appear to teach only two different word line pre-charge voltages. *See infra* Section V.C. In contrast, Lee, Zhao, and Yang are not so limited: they teach memory systems that employ at least three different word line pre-charge voltages. Lee, Zhao, and Yang also apply these voltages to the same groups of word lines required by the '822 patent's claims. As a result, the Office has never specifically assessed unpatentability grounds like those at issue here.¹

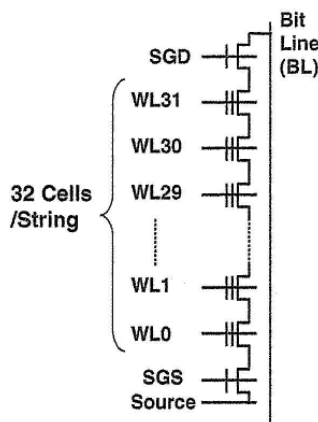
¹ The Patent Owner cited the published application version of Lee in a continuation application to the '822 patent. That is irrelevant, because the Examiner was unaware of Lee (or the published application) during the prosecution of the '822 patent. And the Examiner did not discuss Lee during prosecution of this continuation. Instead, the Examiner issued only a double patenting rejection in view of the '822 patent. *See* Ex. 1016, 218-224. Finally, at a minimum, the Examiner erred in overlooking Lee's teachings.

V. The '822 Patent

A. Technological Background

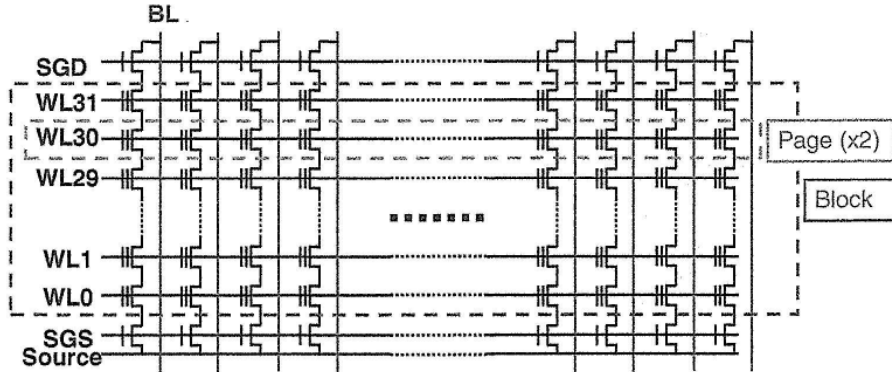
The '822 patent and the prior art discussed in this petition relate to NAND flash memory. “Flash memory” is a form of “non-volatile memory.” Ex. 1009, 1:24-26. “Non-volatile memory ... can retain its data values ... without the application of power.” *Id.*, 1:26-28. NAND flash stores data in a “cell” formed from a transistor. Ex. 1006, 38-39; Ex. 1012, 109; Liu, ¶¶ 40-50.

NAND cells are arranged in “strings” with multiple cells “connected in series.” Ex. 1006, 38. The cells are surrounded by “select transistors (SGD, SGS).” *Id.* The “SGD connects” at the string’s drain-side “to isolate it from a bit line (BL),” and the “SGS connects” at the string’s source-side “to isolate it from a source line (SL).” *Id.* Word lines connect to each memory cell. *Id.*, 38-39.

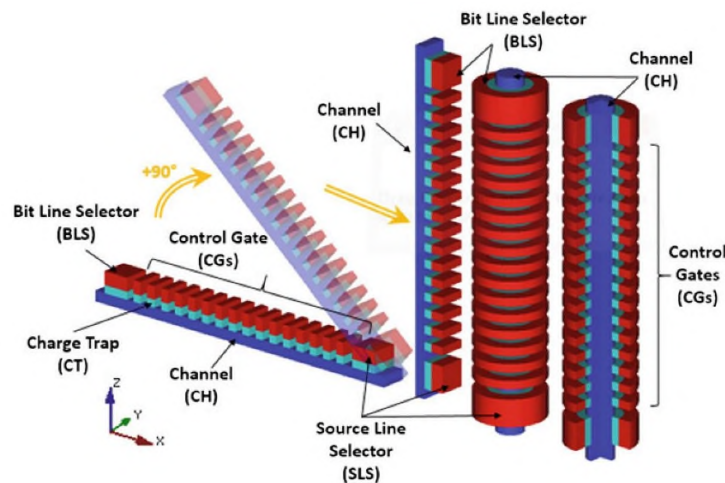


Id., 39.

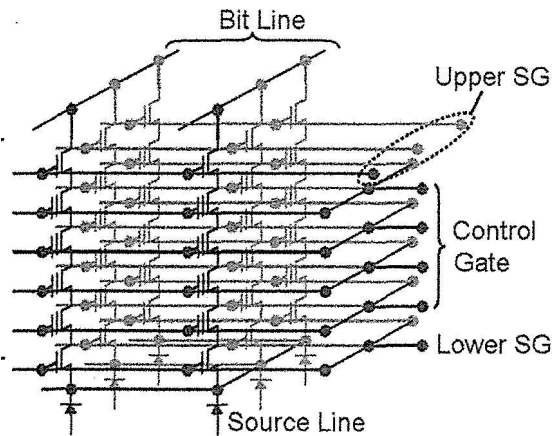
Early NAND devices were formed as two-dimensional arrays of cells. Ex. 1006, 38.



Id., 40. As shown, the cells are grouped into “page[s]” extending along the word lines and “block[s].” *Id.* “[R]ead and program operations are performed per page” while “the erase operation is performed per block.” *Id.*, 39. “[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed in 2006. *Id.*, 292. “[A] modern 3D NAND structure” ... “turn[s] the 2D NAND string upside” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1011, 3.



Ex. 1012, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1006, 296; *see also* Liu, ¶¶ 51-64.

To program a particular NAND memory cell in a memory string, a “high-voltage V_{pgm} ” is applied to the word line connected to the cell—known as the “selected” word line—while “keeping” the string’s bit line at “0V.” Ex. 1006, 44. This causes electron movement into the cell and raises the cell’s threshold voltage to a value within a specific range for purposes of storing data. *Id.*, 45. Because the selected word line also passes through cells in many other strings, an “inhibit” voltage is applied to these strings’ bit lines to prevent undesired programming. *Id.*, 46. A lower “ V_{pass} ” voltage is also applied to all unselected word lines. *Id.*, 44-46; Liu, ¶¶ 65-67.

Due to the close proximity of memory cells—and the application of these various different voltages—NAND is subject to a “phenomenon” known as “[p]rogram disturb.” Ex. 1006, 52. “Program disturb” involves “the threshold voltage ... of unselected cell[s]” undesirably “increas[ing] during program

operation.” *Id.*, 52-53. This is problematic, as cells not identified for programming modification may nonetheless enter a different/unintended programmed state. *Id.* “Program disturb” can occur both in the NAND string that includes the programmed cell and in adjacent strings. *Id.* It was known that applied voltages can be tailored to either avoid or minimize program disturb. *Id.* For instance, increasing the V_{pass} voltage applied to unselected word lines increases the so-called “boosting” voltage in adjacent NAND strings—a voltage that is induced in part by word line voltage—thereby reducing program disturb in those strings. *Id.* But this also has the effect of increasing program disturb in the string that includes the programmed cell. *Id.* A lower V_{pass} has the opposite effect, reducing program disturb in the string that includes the programmed cell, but increasing it in adjacent strings. *Id.*; *see also* Liu, ¶¶ 68-73.

B. Overview

The ’822 patent relates to a “non-volatile memory device”—such as a “three-dimensional (3D) NAND flash memory”—and an associated “control method....” Ex. 1001, 1:15-19.

The patent explains that typical “3D NAND memory architecture stacks memory cells vertically in multiple layers, achieving a higher density....” *Id.*, 1:29-32. “As more layers are added, the bit density increases, thus increasing ... storage capacity.” *Id.*, 1:32-33. But “[w]ith the layer increases, ... program disturb becomes

worse.” *Id.*, 1:34-35. One way to address this is to apply “[a] pre-pulse signal ... to an unselected bit line...” *Id.*, 1:34-37. Longer channels, however, “reduce[]” “[t]he effect” of such a “bit line pre-charge.” *Id.*, 1:39-41. The patent goes on to explain that “[a] traditional method for improving the bit line pre-charge effect is to extend the bit line pre-pulse time.” *Id.*, 1:41-44. But this results in slower programming. *Id.* Another “traditional method” entails “increas[ing] the voltage level of the bit line pre-pulse.” *Id.*, 1:44-48. This “increase[s] the risk of the breakdown” of the “bit line transistor.” *Id.*

In an effort to address these problems, the ’822 patent “appl[ies] word line pre-pulse signals with different voltage levels” for purposes of “reducing programming disturb.” *Id.*, 1:17-19. The further a word line is “away from the selected word line, the larger voltage level of the word line pre-pulse signal can be applied[.]” *Id.*, 4:39-43. According to the patent, this “enhance[s]” “the channel potential gradient” in the unselected NAND strings, which in turn “enhance[es] the pre-charge effect” and “reduc[es] programming disturb.” *Id.*, 4:54-59.

Figures 3 and 4 provide an example. Figure 3 shows a single “memory string.” *Id.*, 5:7-11. Connection of the “memory string” to an “unselected bit line BL” is controlled by a “top select gate line TSG” (green). *Id.*, 5:11-15. “[W]ord lines WL0 to WLn” pass through the memory string. *Id.*, 5:14-16. One of these—“WL0” (yellow)—is “the selected word line.” *Id.*, 5:18-20. The remaining word

lines are divided into a “first group” (blue “Bottom WL”), “second group” (orange “Middle WL”), and “third group” (purple “Top WL”). *Id.*, 5:19-34.

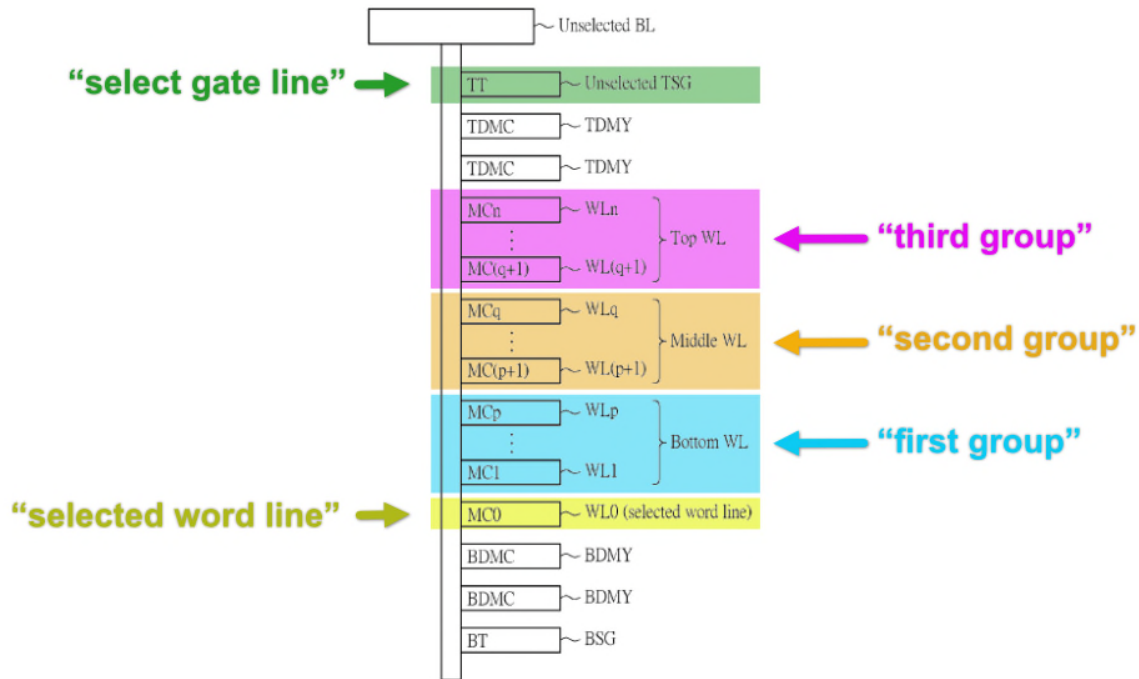
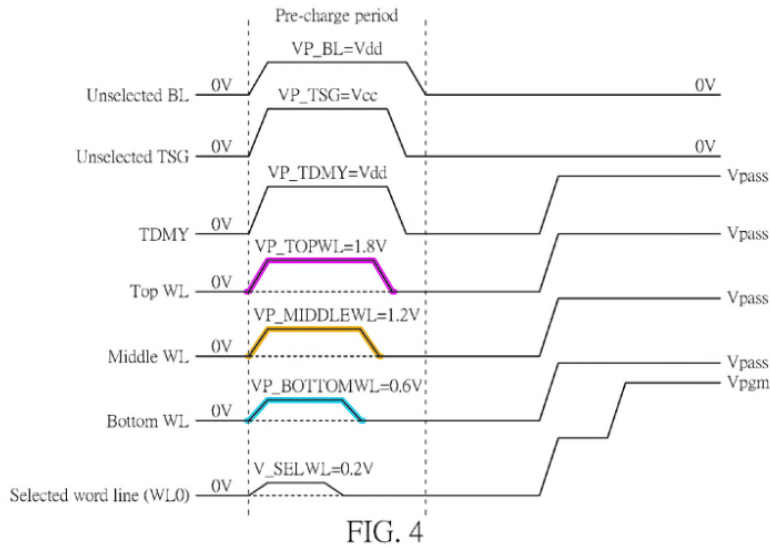


FIG. 3

Id., Fig. 3²

Figure 4 is a “signal timing diagram of” Figure 3’s “memory string[.]” *Id.*, 5:35-38. To improve the potential in the string’s channel and reduce program disturb, three different “word line pre-pulse signals”—labeled VP_BOTTOMWL (blue), VP_MIDDLEWL (orange), and VP_TOPWL (purple)—are applied to the three groups of word lines. *Id.*, 5:50-55. The voltage level of these signals increases with distance from the “selected word line”:

² All color added by Petitioner.



Id., Fig. 4; Liu, ¶¶ 77-93.

C. Prosecution History

The Examiner rejected the '822 patent only on double patenting grounds. *See generally* Ex. 1002. However, the Examiner rejected the patent's parent application—U.S. App. 16/709,944—over other prior art. This art included U.S. Patent No. 10,283,202 (“Chen”) and U.S. Pub. 2011/0194351 (“Kim”). *See* Ex. 1015, 79-87. The parent application's broader claims—unlike those in the '822 patent—required only a “plurality of word line pre-pulse signals.” *Id.*, 35. Because of this, the Examiner based the rejection on Chen's teaching of two different word line pre-pulse voltages (0 or 2V). *See id.*, 83-84. Kim similarly applied two different pre-pulse voltages (V2 or V3) to various word lines. *Id.*, 85. Applicant responded by amending the claims to require (1) “first,” “second,” and “third,” “pre-pulse signal” voltages, (2) that “first,” “second[,]” and “third” groups of word lines be arranged in

order between the “selected word line and the select gate line[,]” and (3) that the “voltage level” of the “pre-pulse signal” increase from the “first” to the “second” and then to the “third” “group[.]” *Id.*, 115-116. This resulted in allowance. *See id.*, 131-134.

VI. Claim Construction

The Board applies the same *Phillips* claim construction standard used by district courts. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). For purposes of this petition, Petitioner submits that the terms of the ’822 patent’s claims do not require further construction and can be afforded their plain and ordinary meaning. *See Liu*, ¶¶ 104-107.

VII. Level of Ordinary Skill in the Art

A POSITA in the field of the ’822 patent would have had a bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). *Liu*, ¶¶ 35-38. This POSITA would have been aware of and generally knowledgeable about NAND memory’s structure, its component parts, how it operates, and how it is controlled. *Id.*, ¶ 38.

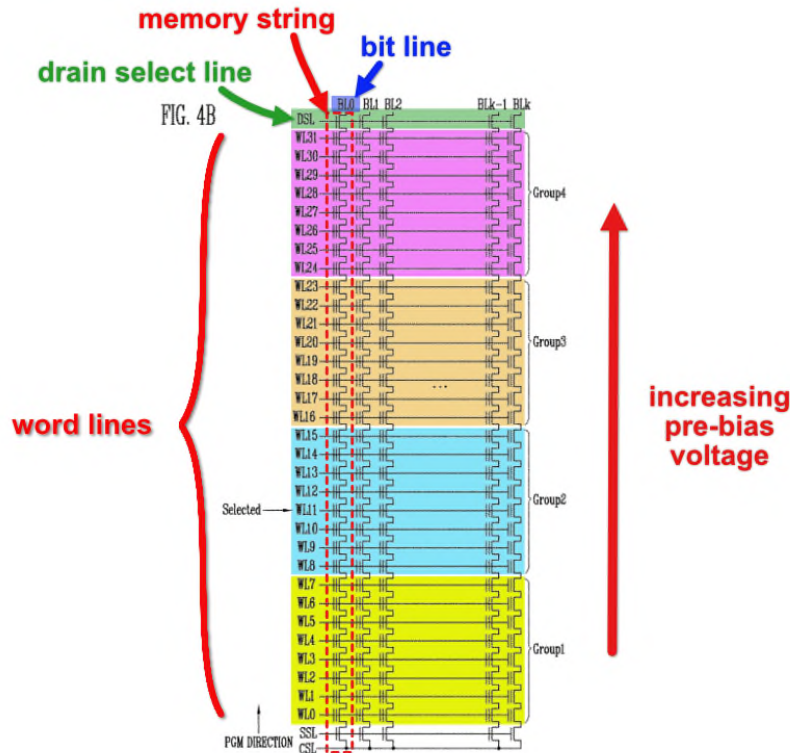
VIII. Prior Art Overview

A. Lee

Lee issued November 6, 2018. Lee, Cover. It is AIA § 102(a)(1) prior art. Lee teaches a “semiconductor memory device”—with “a three-dimensional structure”—that “mitigate[s] a program disturb phenomenon.” *Id.*, 1:52-56, 7:23-24. To facilitate this, Lee arranges its memory’s “word lines” into “a plurality of word line groups.” *Id.*, 2:4-5. Then, “different pre-bias voltages are applied” to the groups of word lines during a “precharge” step “depending on the respective positions of the word lines.” *Id.*, 1:62-2:3. “[T]he closer a word line group ... is to a drain select transistor in the memory cell array, the higher a pre-bias voltage to be applied to the word line may be.” *Id.*, 2:13-16. According to Lee, this accounts for “the resistance component” along a memory string’s channel and allows “the precharge level in the channel” to be “uniformly formed.” *Id.*, 8:47-51. This in turn “mitigate[s]” the “program disturb phenomenon.” *Id.*, 8:51-52.

Lee also includes examples. In these examples, multiple vertical memory “strings” are connected to a lower “source select line SSL[,]” “word lines” WL0-WL31, and upper “drain select line DSL.” Lee, 7:37-43. Each string also connects to a “corresponding bit line.” *Id.* In the more specific example shown in Figure 4B, the memory’s word lines WL0-WL31 are arranged into “first to fourth word line groups Group1 to Group4....” *Id.*, 9:36-40. The word lines are selected for

programming one at a time beginning at “WL0” and moving “toward ... WL31.” *Id.*, 8:22-25. And “the closer a group is to the drain select transistor, the higher” the “applied” “pre-bias voltage....” *Id.*, 9:41-55.



Id., Fig. 4B (annotated); Liu, ¶¶ 110-119.

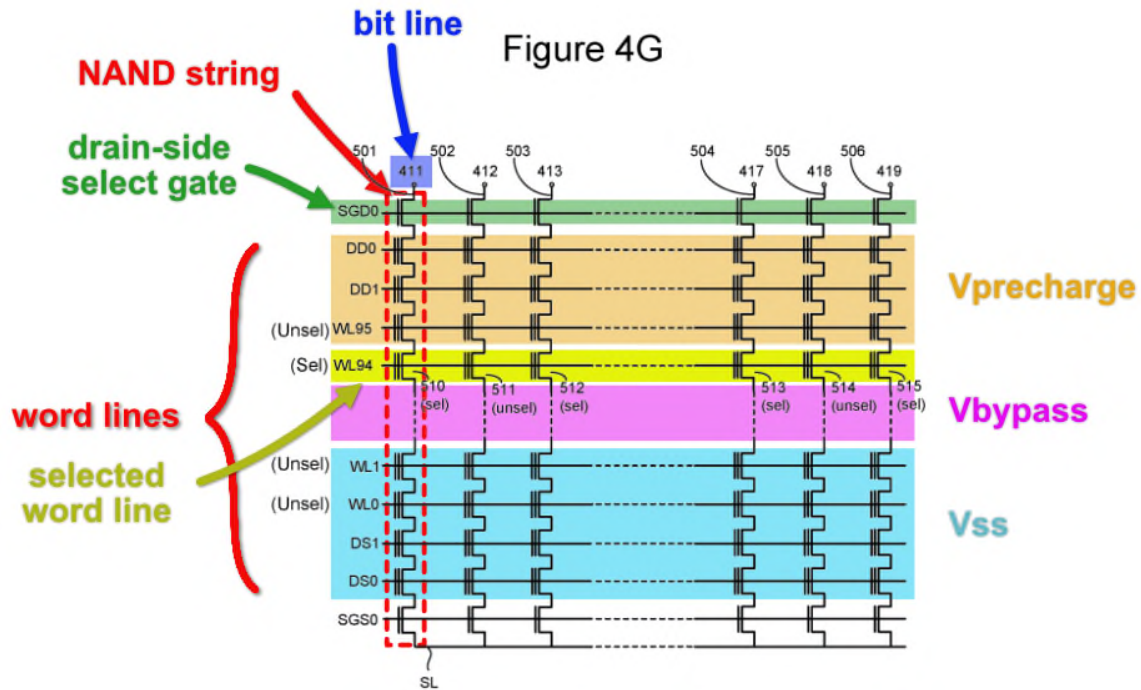
B. Zhao

Zhao was filed June 7, 2018. *See* Zhao, Cover. It is prior art under AIA § 102(a)(2). Zhao relates to “memory system 100” that “implements” various “countermeasures for avoiding program disturb.” *Id.*, 4:7-10. This memory can be “a three dimensional memory array” with multiple vertical “NAND strings.” *Id.*, 6:34-44. The “NAND strings” are connected to lower source-side and upper drain-

side select lines multiple dummy and data word lines, and “associated bit line(s).” *Id.*, 11:53-61; 12:6-13.

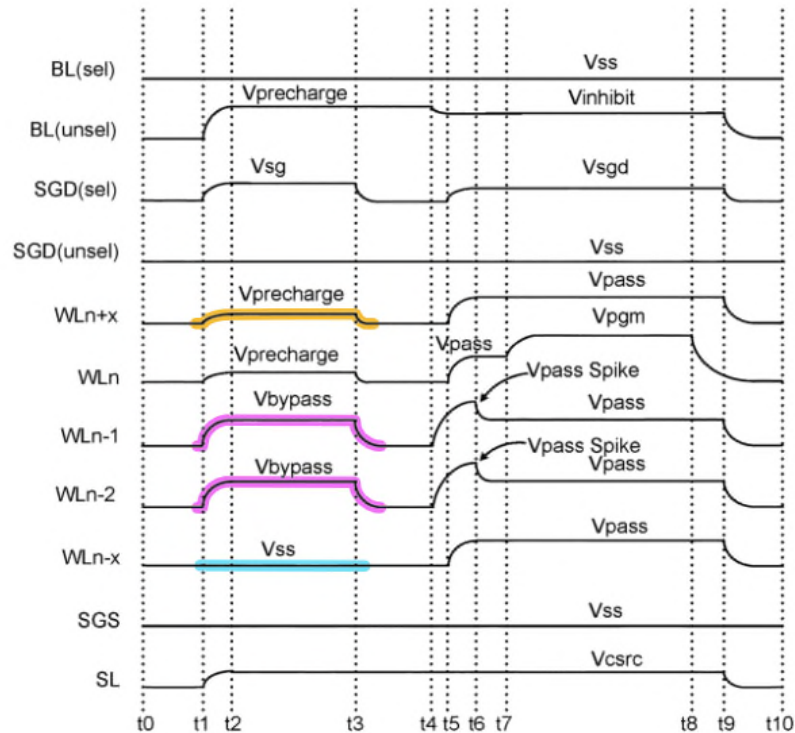
During programming, the word lines are selected one at a time in “order” from the source- to drain-side: “WL0, WL1, WL2, ... WL95.” Zhao, 17:27-29. “To assist in ... boosting[,]” Zhao’s “control circuit” “pre-charge[s]” the “channels of ... NAND strings” before programming. *Id.*, 13:65-14:1, 14:35-40; 16:65-67. Different groups of word lines are supplied with different pre-charge voltages. *See id.*, Fig. 13. Unprogrammed word lines on the “drain side” of the selected word line receive a “pre-charge” voltage $V_{precharge}$. *Id.*, 19:19-22; 19:57-58; 22:45-48. Multiple “already programmed (e.g. source side) unselected word line[s] ... adjacent to the selected word line” are supplied with a higher “bypass voltage” V_{bypass} . *Id.*, 19:32-50; 22:50-53. The remainder of the source-side word lines receive a “low” pre-charge voltage V_{ss} . *Id.*, 19:22-23; 23:7-9. According to Zhao, using these different pre-charge voltages “equalizes the charge between the source side ... and the drain side of the channel” assisting in the avoidance of “program disturb.” *Id.*, 19:50-56; 22:65-23:5.

Figure 4G depicts one “sub-block” of memory. Zhao, 12:6-7. The general locations of the word line groups receiving Zhao’s different pre-charge voltages are shown below:



Id., Fig. 4G. Figure 13 is “a signal diagram” showing the signals applied to Zhao’s lines, including those applied to the word lines “during pre-charge” “time period” “t1-t3[.]” *Id.*, 22:18-20, 22:39-23:5.

Figure 13



Id., Fig. 13; Liu, ¶¶ 120-132.

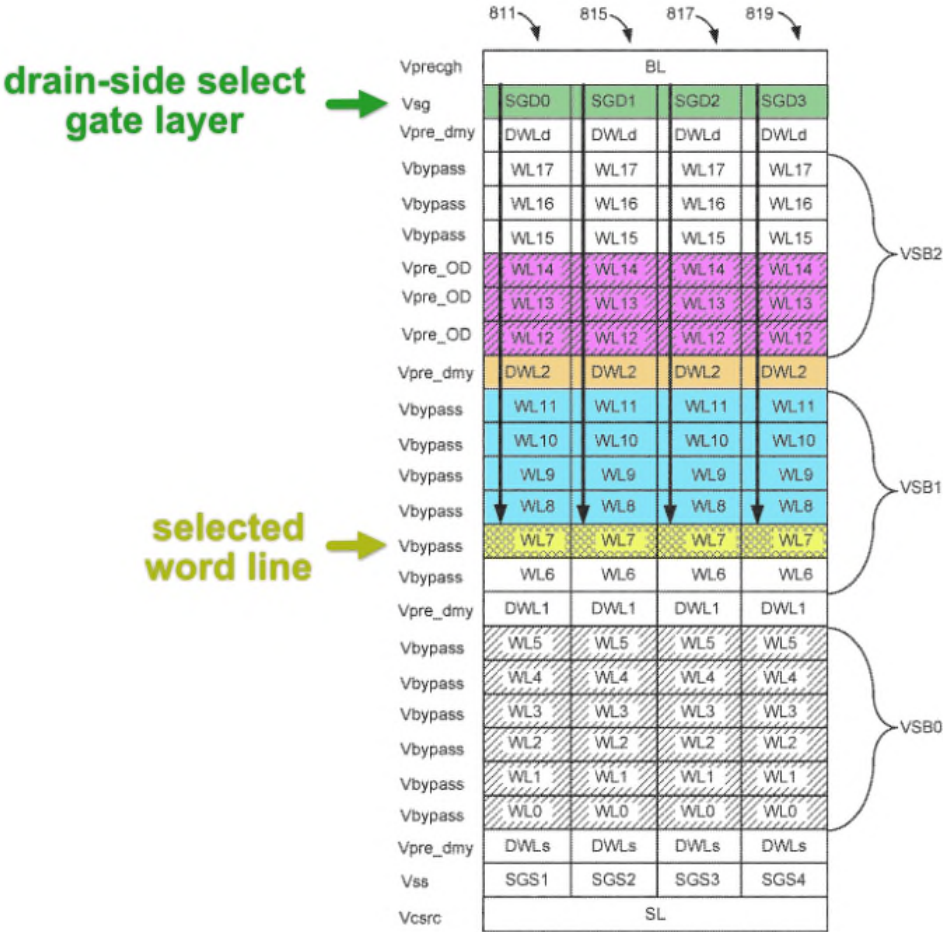
C. Yang

Yang was filed November 26, 2018. *See* Yang, Cover. It is prior art under AIA § 102(a)(2). Yang is also directed to a “three-dimensional memory array of non-volatile memory cells” arranged into “vertical NAND strings.” *Id.*, 5:4-14. Although Yang’s memory structure is similar to Zhao’s (*see, e.g., id.*, Fig. 4G), Yang groups its word lines differently and applies different pre-charge voltages.

According to Yang, “[i]f the channel of [an] unselected NAND string is not adequately pre-charged during the pre-charge phase, the NAND channel may fail to boost to a sufficient voltage during the programming phase to adequately prevent

program disturb.” *Id.*, 2:58-62. Yang goes on to explain that a string may not be adequately pre-charged if there is “valid data” from a previous programming step in memory cells. *Id.*, 3:20-27. To avoid this problem, Yang applies a high “over-drive voltage” (Vpre_OD) during pre-charging to previously “programmed data word lines” located above a selected word line. *Id.*, 22:4-11; 24:28-33. A lower “bypass voltage” (Vbypass) is applied to any “not programmed” word lines. *Id.*, 22:31-37, 24:11-17. And a different “dummy pre-charge voltage” (Vpre_dmy) is “applied to all dummy word lines.” *Id.*, 24:18-27.

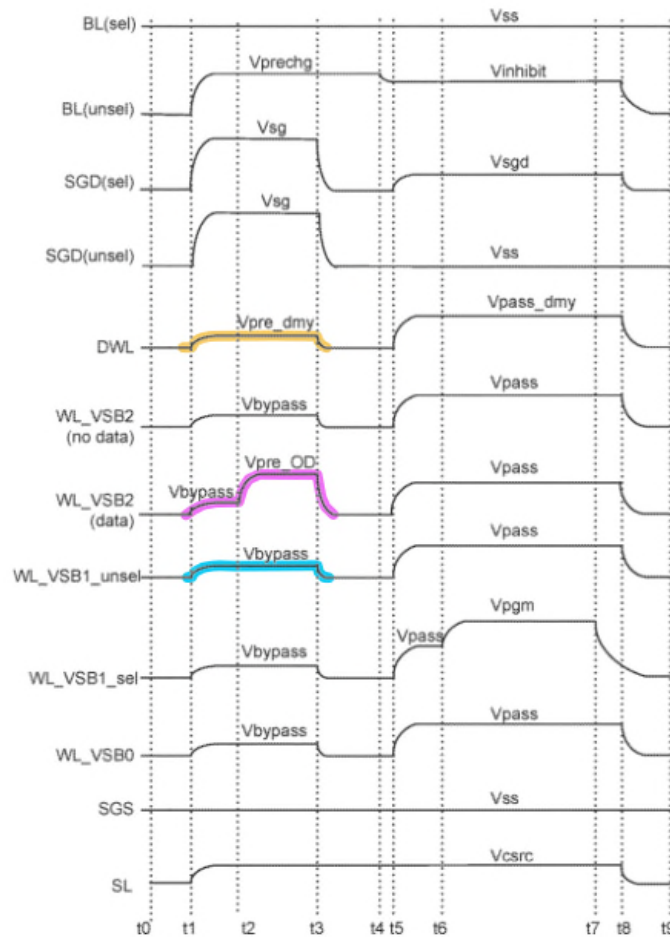
Figure 8C shows an example arrangement of word lines, along with the different applied pre-charge voltages. Yang, 25:29-33. In the figure, WL7 is currently “selected.” *Id.*, 25:18-19. WL8-WL11 do not include data (so are supplied with Vbypass), while WL12-WL14 were previously “programmed” (and are thus supplied with Vpre_OD). *Id.*, 22:4-11; 24:28-33. DWL2 (which is supplied with Vpre_dmy) separates the word lines into “sub-block[s]” that “are treated as separate units for erase/program[ing] purposes....” *Id.*, 9:49-51, 12:22-23.



Id., Fig. 8C.

Figure 8B is a “timing diagram” showing when Yang applies different pre-charge voltage pulses to its word lines. Yang, 23:20-22. “[T]imes t1-t4 correspond to ... [the] pre-charge phase.” *Id.*, 23:23-25.

FIG. 8B



Id., Fig. 8B; Liu, ¶¶ 133-145.

IX. The '822 Patent's Claims Are Obvious

A. *Ground 1: Obviousness Over Lee*

Claims 1-3, 6, and 11-13 are all obvious over Lee when considered in view of the knowledge possessed by a POSITA.

1. Independent Claims 1 and 11

Because they include many of the same limitations, independent claims 1 and 11 will be addressed together.

[1.Pre]/[11.Pre] “A [method of controlling a memory device, the] memory device, comprising”³

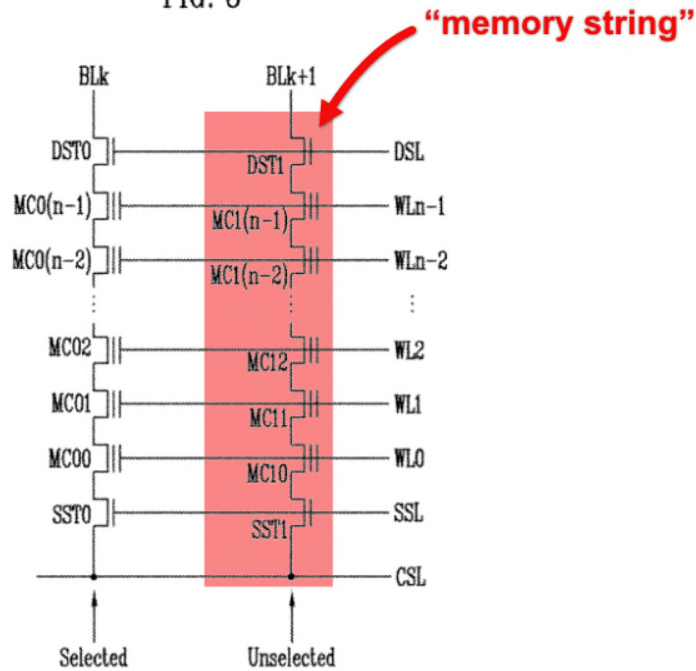
To the extent limiting, Lee teaches the preamble. Lee relates to “a semiconductor memory device” and “a method of operating the semiconductor memory device” with “control logic.” Lee, 1:52-2:3; *see also id.*, Abstract; 1:16-18; *see also* Liu, ¶¶ 150-151.

[1.A]/[11.A] “a plurality of memory strings”

Lee’s “semiconductor memory device 100 includes a memory cell array 110.” Lee, 5:60-61. The memory cells are arranged in a “plurality of cell strings[.]” *Id.*, 6:12-15; *see also id.*, 1:36-48 (similarly discussing “three-dimensional” NAND memory with “a plurality of strings”). “Each of the cell strings includes a drain select transistor, a plurality of memory cells[,], and a source select transistor, which are coupled between a bit line BL and a common source line SL.” *Id.*, 6:1-18. Figure 3 below provides an example. The figure depicts two “*memory strings*”: a “selected cell string” “targeted for a program operation” and an “unselected cell string” (annotated red). *Id.*, 7:28-36.

³ [Bracketed] text is present only in claim 11.

FIG. 3

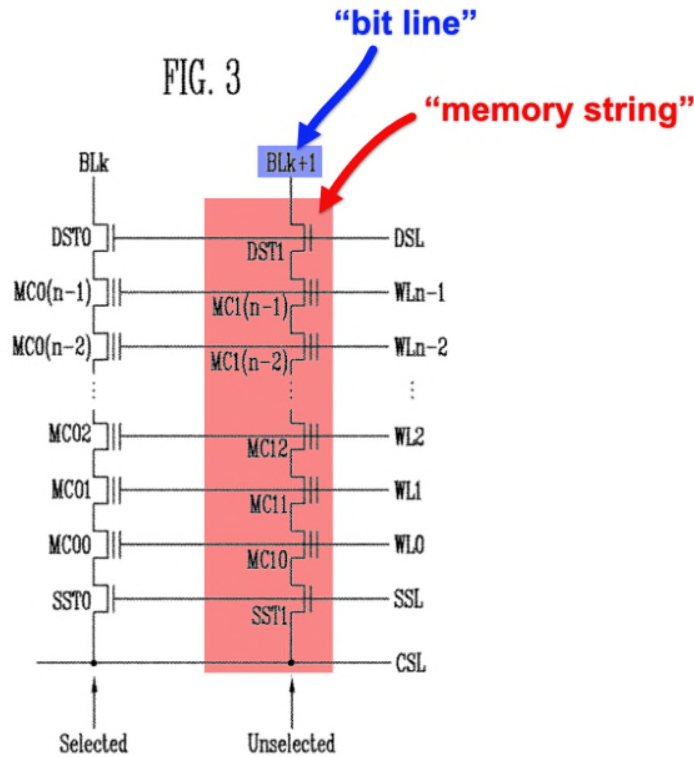


Id., Fig. 3; *see also id.*, Fig. 4B; Liu, ¶¶ 152-157.

[1.B]/[11.B] “a bit line connected to a first memory string of the plurality of memory strings”

Lee teaches the claimed *“bit line connected to a first memory string.”*

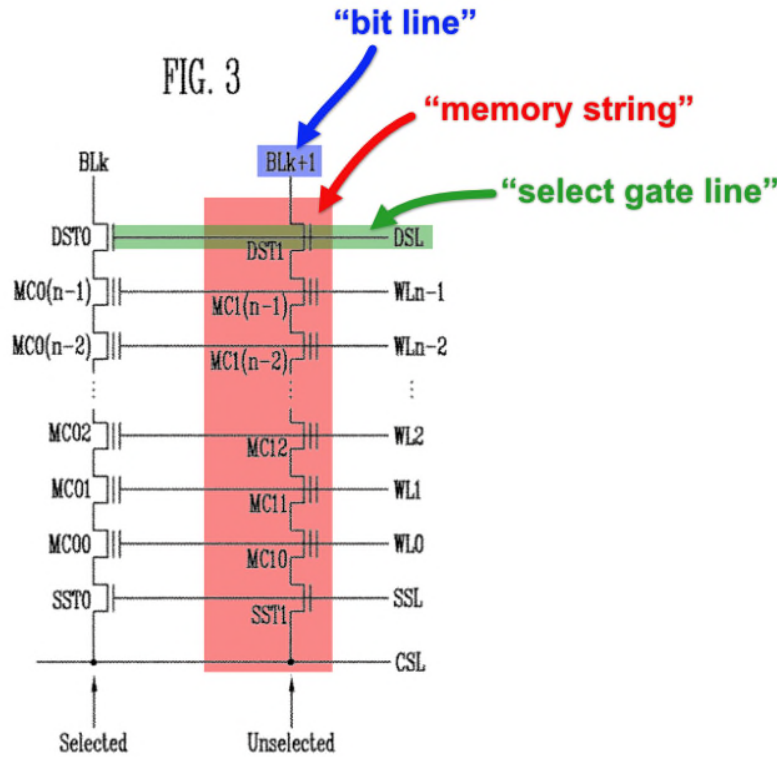
According to Lee, each of “cell string” in its “memory cell array” is “coupled to a bit line.” Lee, 7:28-36. In Figure 3, the depicted “unselected string” (red) is “coupled to a bit line BLk+1” (blue). *Id.*; *see also id.*, 6:15-18.



Id., Fig. 3; *see also id.*, Fig. 4B; Liu, ¶¶ 158-160.

[1.C]/[11.C] “a select gate line connected to the first memory string of the plurality of memory strings”

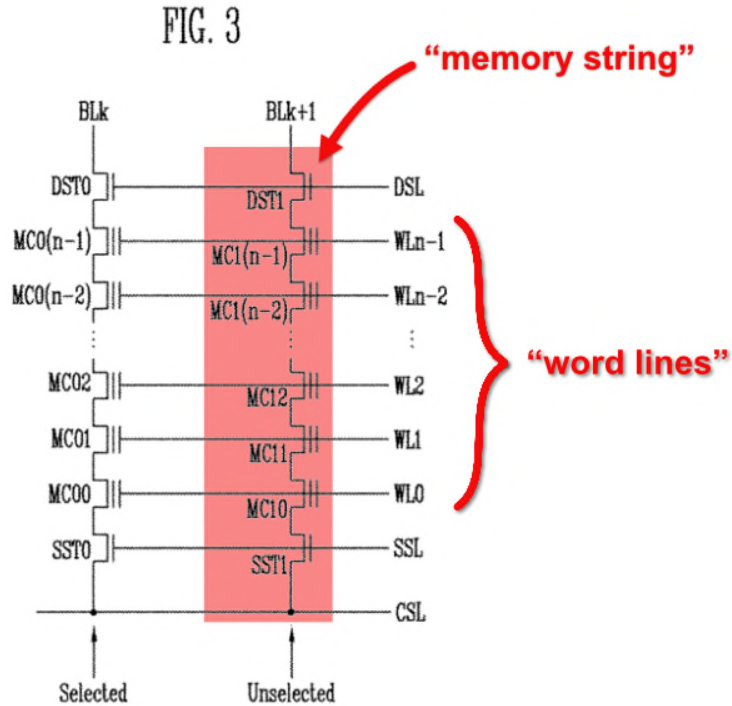
According to Lee, each “cell string” in its memory array includes an upper “drain select transistor” (DST) that is “coupled to a ... drain select line DSL.” Lee, 7:37-43; *see also id.*, 6:15-18. Lee’s DSL—the claimed “*select gate line*” that is “*connected to the first memory string*”—is annotated green in Figure 3 below:



Id., Fig. 3; see also *id.*, Fig. 4B; Liu, ¶¶ 161-163.

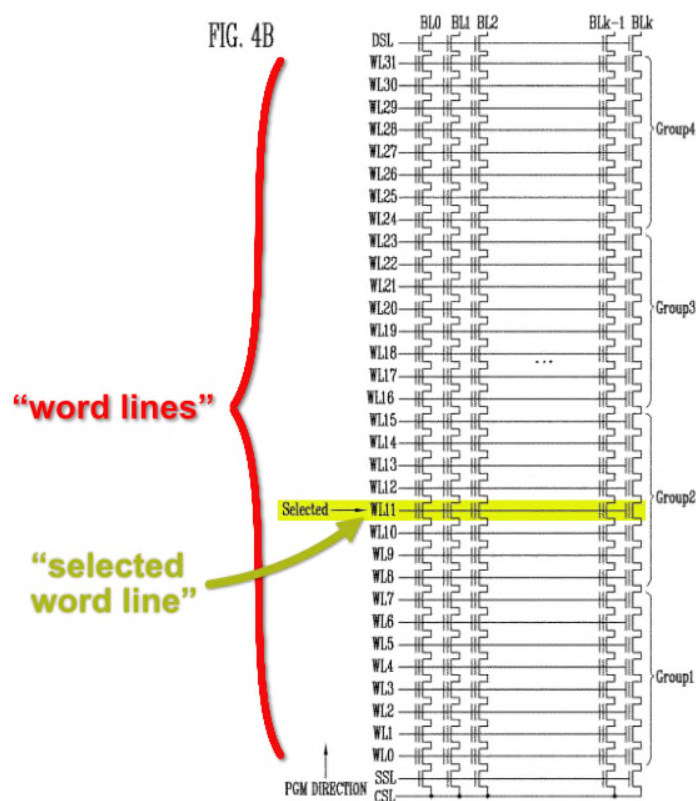
[1.D]/[11.D] “a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string”

Lee includes a *“plurality of word lines ... connected to the first memory string.”* According to Lee, the memory cells making up its array’s “memory blocks BLK1 to BLKz” are arranged into “pages” and are “coupled in common to a single word line.” Lee, 5:64-6:7. There are a “plurality of pages” (and associated “word lines”) in Lee’s memory cell array. *Id.* In Figure 3, the “memory cells” in each “cell string” are “coupled to the word lines WL0 to WLn-1. *Id.*, 7:30-45.



Id., Fig. 3.

Next, Lee explains that individual word lines are “*selected*” during operation of its memory. In one example, the memory array may include “thirty-two word lines WL0 to WL31.” Lee, 8:6-7. During programming, both the “bit line” associated with a particular “target” cell’s “string” and the cell’s “word line” are “selected.” *Id.*, 7:28-34, 8:18-25. The word lines are selected sequentially following a “program direction.” *Id.*, 8:23-25. The “program direction is a direction from ... word line WL0 toward ... word line WL31.” *Id.*; see also *id.*, 2:11-12. In Figure 4B below, the “word line WL11 is selected[.]” *Id.*, 9:15-17, 39-40.



Id., Fig. 4B; *see also* Liu, ¶¶ 164-171 .

[1.E] “a control circuit configured to” / [11.E] “[the method comprising]”

Lee includes the claimed “*control circuit*” “*configured*” to perform the claimed “*method.*” Lee’s “semiconductor memory device 100 includes[,]” among other components, “a control logic 140[.]” Lee, 5:60-63. The “control logic” is “coupled” to both an “address decoder” and “voltage generation unit[,]” and is “configured to control the overall operation of the semiconductor memory device 100.” *Id.*, 7:5-7. This includes, for instance, controlling the “appl[ication] of pre-bias voltages to the word lines during a program operation” via the voltage generation unit and address decoder. *Id.*, 7:8-19; *see also id.*, Abstract (referencing

a “semiconductor memory device” with a “control logic”; Fig. 1 (showing “control logic 140” controlling the “voltage generation unit 150” and “address decoder 120” for purposes of applying voltages to word lines WL); Liu, ¶¶ 172-176.

[11.E.0] “[applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period]”

[1.E.1]/[11.E.1] “apply[ing] a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a [the] pre-charge period”

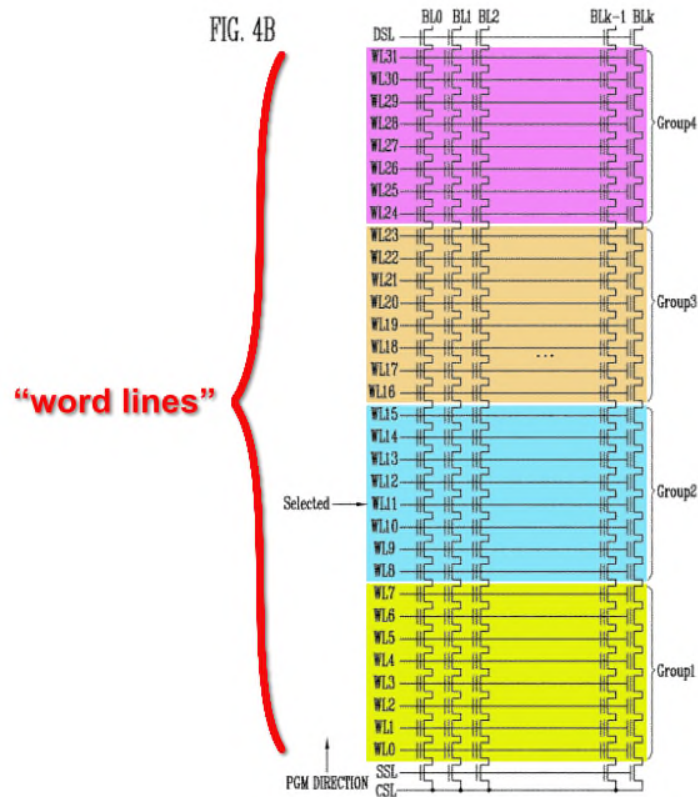
[1.E.2]/[11.E.2] “apply[ing] a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and”

[1.E.3]/[11.E.3] “apply[ing] a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period”

These limitations collectively require application of “*first*,” “*second*,” and “*third*” “*word line pre-pulse signal[s]*” to “*first*,” “*second*,” and “*third*” “*group[s]*” of “*word lines*” during a “*pre-charge period*.” Claim 11 additionally requires application of a “*word line signal to the selected word line*” during this same “*pre-charge period*[.]” Lee renders all this obvious.

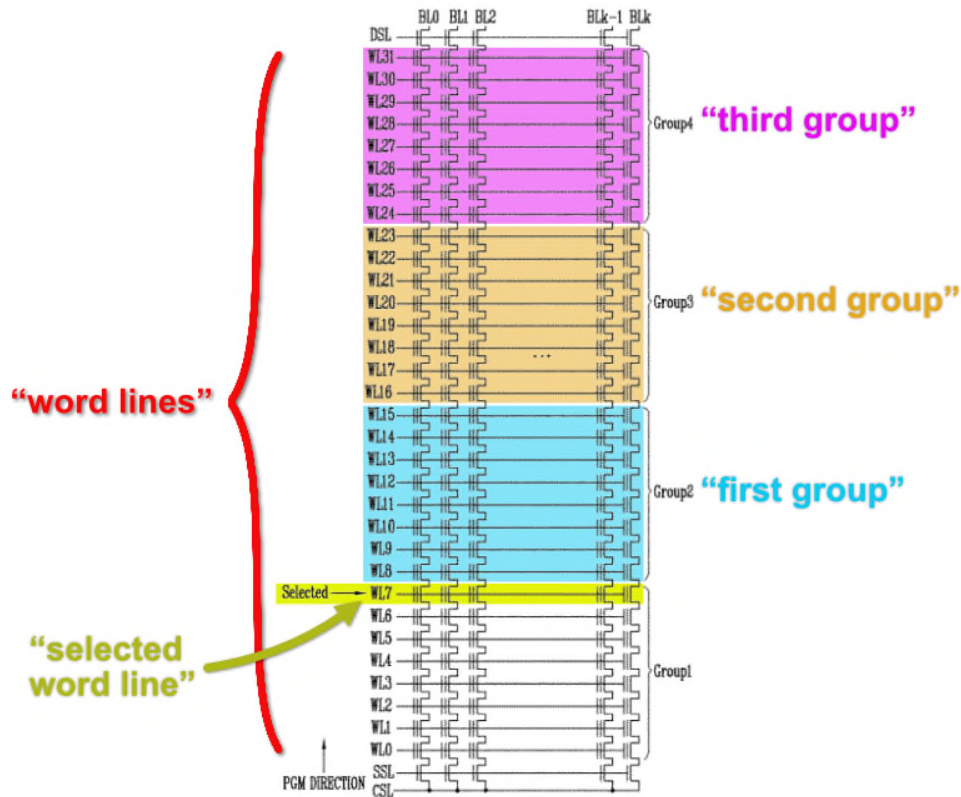
To begin, Lee arranges its word lines into multiple “*group[s]*.” Lee explains that “the word lines coupled to a memory string in a memory block may be grouped ... during a precharge operation of the cell string.” Lee, 7:58-61; *see also id.*, 2:4-5. For example, in Figure 4B, “the control logic may group the thirty-two word lines into four word line groups. Each of the first to fourth word line groups Group1 to

Group4 includes eight word lines.” *Id.*, 9:36-40. These “group[s]” are annotated purple, orange, blue, and yellow below:



Id., Fig. 4B.

The cells in this Figure are programmed in sequence starting at the source side. Lee, Fig. 4B. “[W]ord line WL11” is currently “selected[.]” *Id.*, 9:39-40. The below demonstrative provides an example where another word line—WL7 in Group1—is selected. As shown, there is a “**first group**” (WL8-WL15 in Group2, blue), “**second group**” (WL16-WL23 in Group 3, orange), and “**third group**” (WL24-WL31 in Group4, purple) in the “**plurality of word lines**”:



Lee, Fig. 4B (modified to show WL7 selected), *see also* Liu, ¶¶ 177-184.

Next, Lee teaches use of a “*plurality*” of “*word line pre-pulse signal[s]*” during a “*pre-charge period.*” According to Lee, “different pre-bias voltages may be applied to the respective groups during a precharge operation of the cell string.” Lee, 7:58-61; *see also* Abstract; 1:62-2:3. The “pre-bias voltages ... applied to the plurality of word lines” vary by group, and change “depending on the respective position of the word lines” for purposes of “precharg[ing the] channel regions of the plurality of memory cells” coupled to the word lines. *Id.*, 1:65-2:3. The closer “a word line group to which a word line belongs is to the” upper “drain select transistor, the higher a pre-bias voltage ... applied to the word line may be.” *Id.*, 8:32-37; *see*

also id., 2:5-9.

In the specific example of Figure 4B, because “WL11” is “selected,” Lee provides its “Group2” word lines with “[a] pre-bias voltage having a default value.” *Id.*, 9:52-55. The “Group3” word lines are provided with a “higher” “pre-bias voltage” than that provided to “Group2.” *Id.*, 9:44-48. And the “Group4” word lines are provided with a “higher” “pre-bias voltage” than that provided to “Group3.” *Id.*, 9:48-52. Likewise, when WL7 in Group1 is selected, Group1 will be provided with the “default value,” while the word lines in Group2, Group3, and Group4 will be provided with increasingly higher “pre-bias voltages.” *See id.*, 1:65-2:9, 8:32-37, 9:36-59.

The demonstrative below provides an example. As shown, the claimed ***“first word line pre-pulse signal”*** is applied ***“first group of the plurality of word lines”*** (the pre-bias voltage applied to WL8-WL15 in Lee’s Group2, blue), a ***“second word line pre-pulse signal”*** is applied to a ***“second group of the plurality of word lines”*** (the higher pre-bias voltage applied to WL16-WL23 in Lee’s Group3, orange), and a ***“third word line pre-pulse signal”*** is applied to a ***“third group of the plurality of word lines”*** (the even higher pre-bias voltage applied to WL24-WL31 in Lee’s Group4, purple):



Lee, Fig. 4B (modified to show WL7 selected), *see also* Liu, ¶¶ 185-192.

A POSITA also would have understood that Lee's pre-bias voltages are ***“pre-pulse[s]”*** applied during a ***“pre-charge period[.]”*** According to the '822 patent, the “pre-charge period” occurs “before programming.” Ex. 1001, 3:43. This is what Lee teaches. Lee repeatedly refers to these voltages as “precharge voltage[s]” that are applied for purposes of “precharg[ing the] channel regions” of its memory cells. Lee, 1:62-2:1; 2:30-32. Further, these voltages are applied during a separate “precharge operation” that occurs prior to application of “a program voltage” to the memory's word lines. *Id.*, 9:7-11; *see also id.*, 2:59-62 (“application of the pre-bias voltages” occurs before “a program loop for a selected program cell”); 11:19-22

(referencing a separate “step S205” during which “precharging” occurs, followed by a “step S207 of performing a program loop”); Fig. 7 (showing separate steps S205 and S207). The ’822 patent explains that the “pre-charge period” occurs “before programming.” Ex. 1001, 3:43-44. This is what Lee teaches: its pre-bias voltages are applied in a separate step before program voltages are applied. *See* Liu, ¶¶ 193-196.

A POSITA also would have understood (or considered it obvious) that Lee’s pre-bias voltages are supplied in the form of a “*pulse*.” According to Lee, there are two different periods of operation during programming of its memory array. First, the “pre-bias voltages” are applied during a “precharge operation” period. Lee, 7:58-67; *see also id.*, 8:15-17 (“pre-bias voltages” are “applied to the ... word lines ... in a precharging step”). Then, when the “precharge operation is completed, a program voltage may be applied to the selected word line” and “a pass voltage may be applied to the unselected word lines” in a separate “program loop” step. *Id.*, 9:7-13; *see also id.*, 6:29-32 (explaining that “program voltages V_{pgm} ” are applied to cells that are being programmed, while “pass voltages V_{pass} ” are applied to non-programmed cells); 9:10-13 (explaining that voltage application is not continuous but is instead “repeatedly performed” in a “program loop”). Because Lee (1) supplies its pre-bias voltages in a separate and distinct-in-time step, and (2) the pre-bias voltages differ from the later V_{pgm} and V_{pass} voltages, a POSITA would have understood the pre-

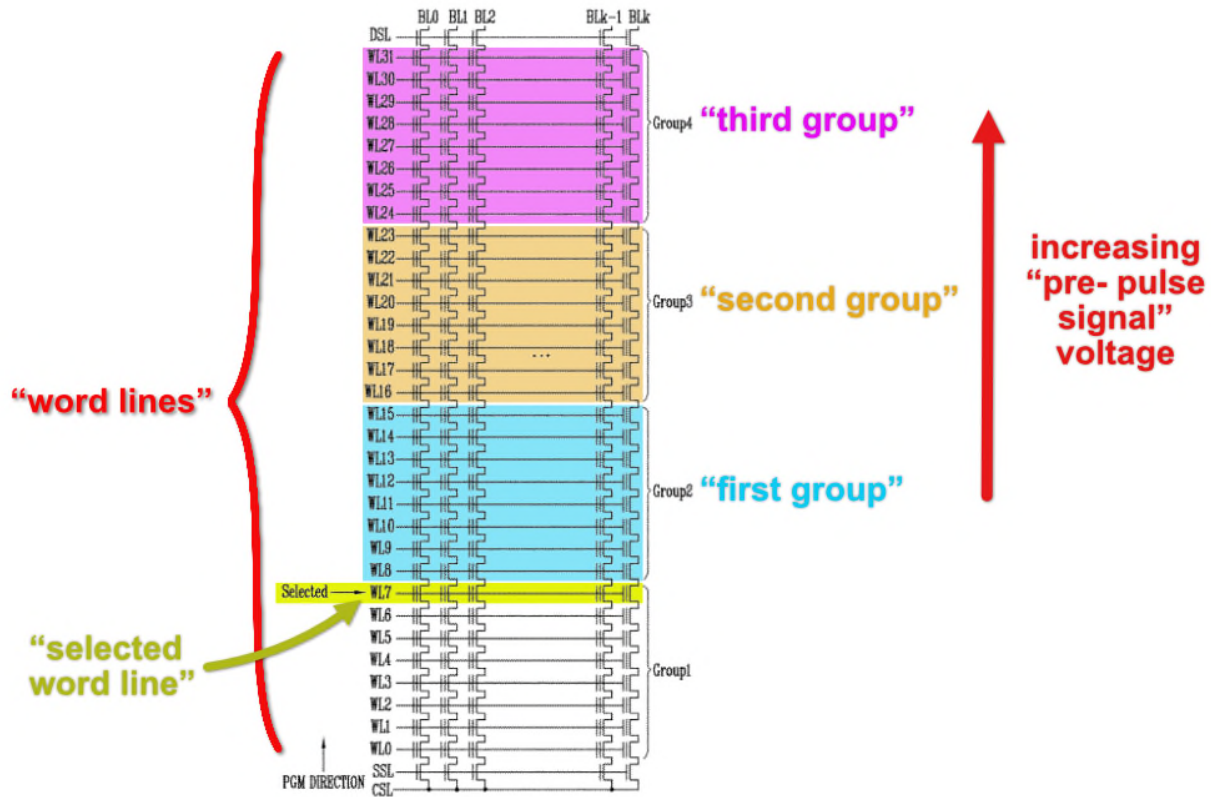
bias voltages to be supplied as “*pulse[s]*.” See Liu, ¶¶ 197-203.

Moreover, when the '822 patent was filed, programming voltages were conventionally provided in the form of a “pulse.” Ex. 1006, 44; *see also id.*, 116-117 (providing examples of various “conventional programming pulse[s]”); Ex. 1007, 142-143 (explaining that “pulses” are applied to a “cell” during “programming”); Ex. 1008, 354 (explaining that “program voltages are provided to ... selected cells for the desired amount of time” as a “pulse”); *id.*, 338 (referencing the use of various program “pulses”). A POSITA would have understood Lee to operate in the same way. See Liu, ¶¶ 204-205. All of the voltages supplied during programming—including both the pre-bias voltages and the later program and pass voltages—obviously would be supplied as pulses. *Id.*; *see also* Zhao, Fig. 13 (supplying pre-charge voltages as pulses); Yang, Fig. 8B (similar).

Lee also teaches the application of a “*word line signal to the selected word line*” during its “*pre-charge period*” as claim 11 requires. According to Lee, the “word line group” that includes “a word line coupled to a program cell”—the “*selected word line*”—is provided with a “default value” “[p]re-bias voltage[]” during precharge. Lee, 2:23-29. Thus, in the example shown in Figure 4B, “[a] pre-bias voltage having [the] default value is applied to the word lines WL8 to WL15 included in the second Group2, including a word line WL11 that is coupled to a selected transistor” during pre-charging. *Id.*, 9:52-55; Liu, ¶¶ 206-209.

[1.E.4]/[11.E.4] “wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal”

Lee also renders this obvious. Lee explains that “different pre-bias voltages” are applied to its word line “groups during a precharge operation....” Lee, 7:58-61; *see also* Abstract; 1:62-2:3. And in Figure 4B, “higher ... pre-bias voltage[s]” are applied to “word line group[s]” that are closer to the “drain select transistor....” *Id.*, 8:32-37; 9:44-51; *see also id.*, 1:65-2:9. Thus, when WL7 in Group1 is selected, the “*third*” “*pre- pulse signal*” applied to Lee’s “*third group*” of word lines (WL24-WL31, purple) exceeds the “*second*” “*pre-pulse signal*” applied to the “*second group*” of word lines (WL16-WL23, orange). And this “*second*” “*pre-pulse signal*” exceeds the “*first*” “*pre-pulse signal*” applied to the “*first group*” of word lines (WL8-WL15, blue):



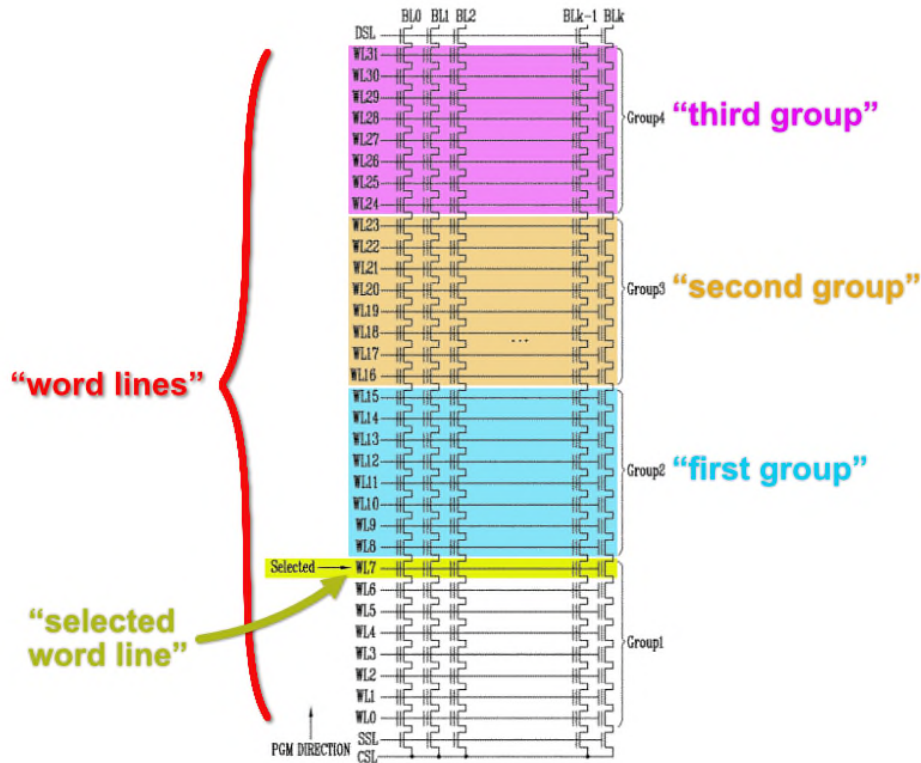
Lee, Fig. 4B (modified to show WL7 selected); *see also* Liu, ¶¶ 210-213.

2. Claims 2 and 12

Claim 2 depends on claim 1. Claim 12 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines”

As shown below, Lee’s *“first group ... of word lines”* (WL8-WL15), *“second group ... of word lines”* (WL16-WL23), and *“third group ... of word lines”* (WL24-WL31) are *“disposed in an order of distance”* from the *“selected word line”* (WL7):



Lee, Fig. 4B (modified to show WL7 selected), *see also, id.*, 9:35-5; Liu, ¶¶ 214-216.

3. Claims 3 and 13

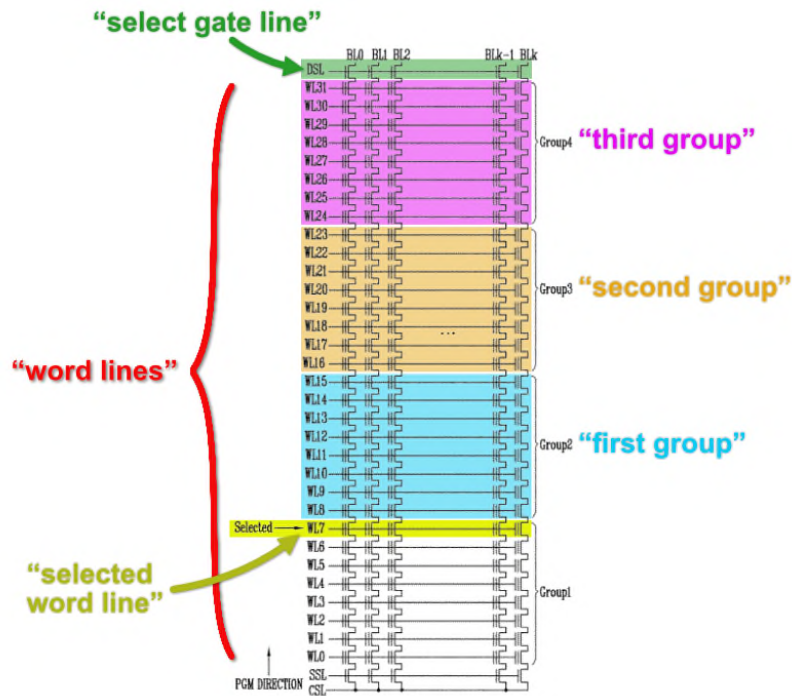
Claim 3 depends on claim 1. Claim 13 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line”

Lee teaches that its memory array includes an upper “drain select line DSL.”

Lee, 7:37-43; *see also id.*, 6:15-18; *supra* discussion of limits [1.C]/[11.C]. As shown below, an example “*selected word line*” (WL7, yellow), “*first group ... of*

word lines” (WL8-WL15, blue), “*second group ... of word lines*” (WL16-WL23, orange), “*third group ... of word lines*” (WL24-WL31, purple), and “*select gate line*” (DSL, green) are also arranged in order as this claim requires:



Lee, Fig. 4B (modified to show WL7 selected); *see also* Liu, ¶¶ 217-220.

4. Claim 6

Claim 6 depends on claim 1 and further requires that:

“the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines”

This is taught by Lee for the same reasons explained in connection with claim 1: Lee’s control unit causes the “selected” word line to be supplied with a “default value” “[p]re-bias voltage[]” during pre-charge. Lee, 2:23-29; 9:52-55; *see also supra* discussion of limit [11.E.0]. Moreover, Lee also applies a “program voltage

Vpgm” to the selected word line during programming. Lee, 6:29-36, 9:7-14; Liu, ¶¶ 221-225.

B. Ground 2: Obviousness Over Zhao

Claims 1, 4-7, 9, 11, 14-16, and 18-19 are all obvious over Zhao when considered in view of the knowledge possessed by a POSITA.

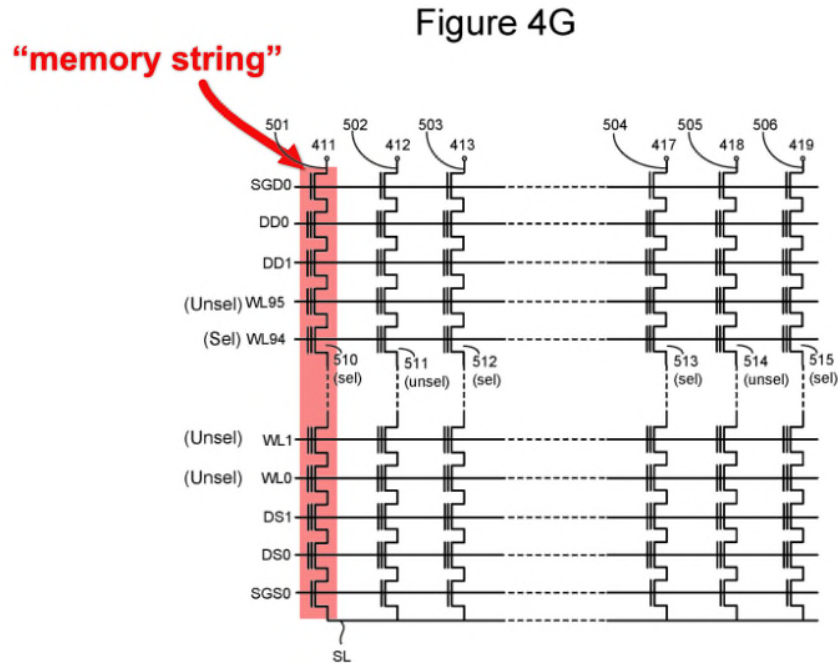
1. Independent Claims 1 and 11

[1.Pre]/[11.Pre] “A [method of controlling a memory device, the] memory device, comprising”

To the extent limiting, Zhao teaches the preamble. Zhao teaches a “memory system 100” that “implements” various “countermeasures for avoiding program disturb.” Zhao, 4:7-10; Liu, ¶¶ 228-230.

[1.A]/[11.A] “a plurality of memory strings”

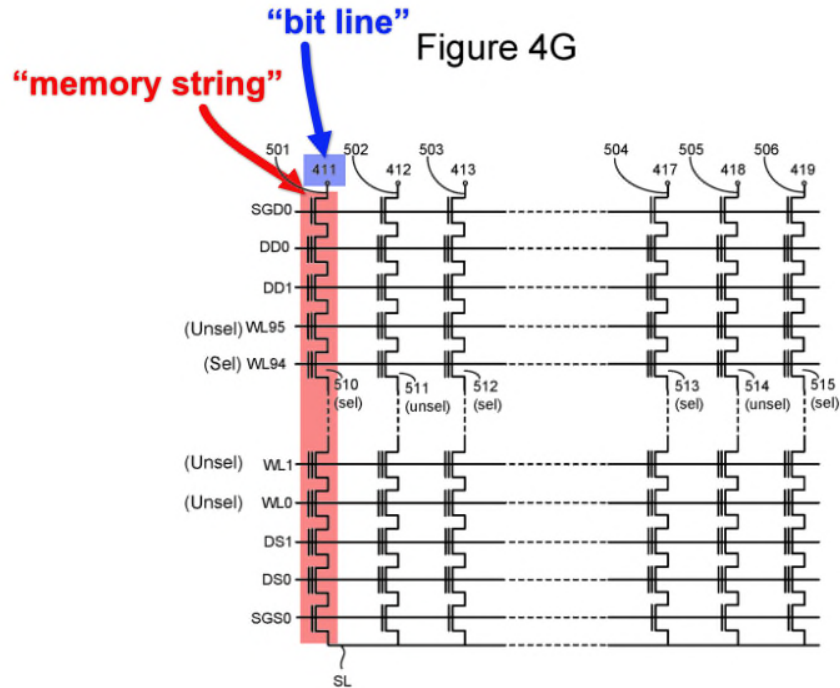
Zhao includes the claimed “*plurality of memory strings.*” According to Zhao, its “three dimensional (‘3D’) NAND structure” includes a “plurality of ... vertical columns[,]” where “each vertical column implements a NAND string.” Zhao, 8:31-44; *see also id.*, 6:41-43 (explaining that Zhao’s “memory structure” includes multiple “vertical NAND strings”). Each of these “NAND strings” includes a series of “non-volatile memory cells.” *Id.*, 10:6-9. Figure 4G—which depicts a “sub-block” of Zhao’s memory—provides an example. *Id.*, 12:6-7. This figure depicts “six NAND strings 501, 502, 503, 504, 505, and 506” of the “thousands of NAND strings” making up the sub-block. *Id.*, 12:9-13.



Id., Fig. 4G; *see also* Fig. 4F; Liu, ¶¶ 231-235.

[1.B]/[11.B] “a bit line connected to a first memory string of the plurality of memory strings”

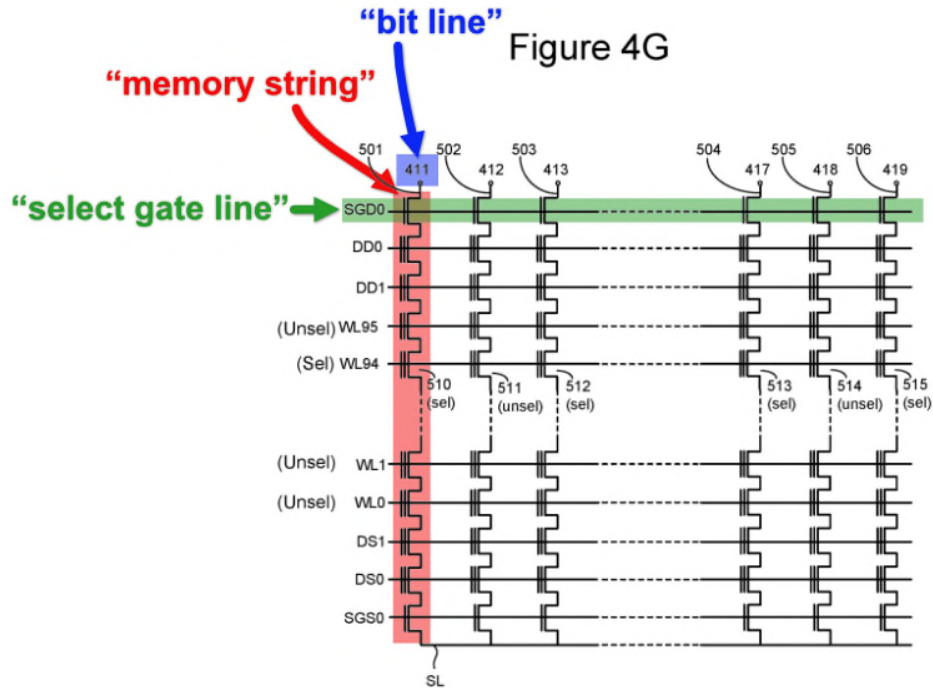
Zhao teaches *“a bit line”* that is *“connected to a first memory string.”* Each of Zhao’s “NAND strings” is connected to a “bit line.” Zhao, 11:53-61; *see also id.*, 8:54-61. One such bit line 411 is annotated blue below:



Id., Fig. 4G; *see also* Fig. 4F; Liu, ¶¶ 236-238.

[1.C]/[11.C] “a select gate line connected to the first memory string of the plurality of memory strings”

Zhao also teaches the claimed “*select gate line connected to the first memory string.*” According to Zeng, its “memory array” can include “8 select layers.” Zhao, 7:64-66; *see also id.*, 9:34-38. This includes upper “[d]rain side select layers SGD0, SGD1, SGD2, and SGD3” that “electrically connect and disconnect NAND strings from bit lines.” *Id.*, 10:19-21; *see also id.*, 11:59-60. All the “NAND strings” in each “[s]ub-block” are “connected” to the same SGD. *Id.*, 12:6-10. One such SGD is annotated green below:



Id., Fig. 4G; *see also* Fig. 4F; Liu, ¶¶ 239-243.

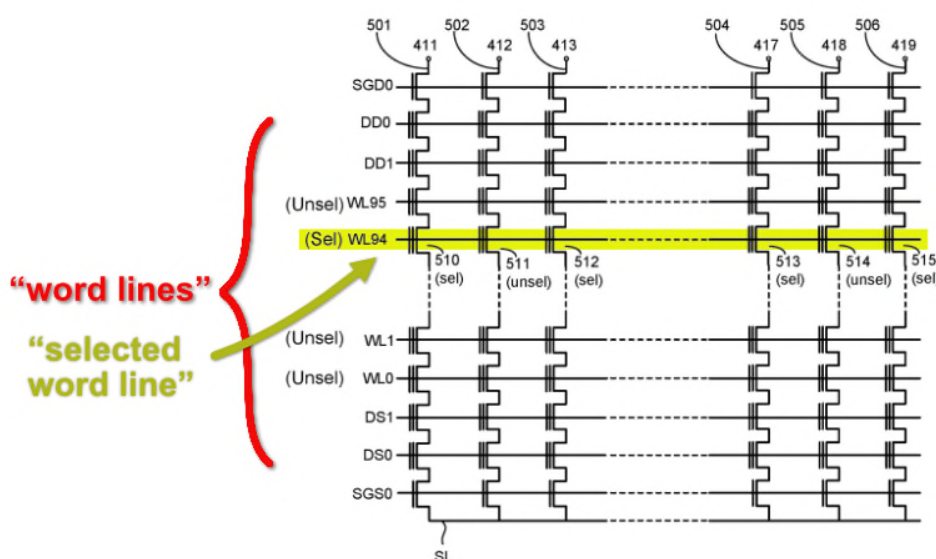
[1.D]/[11.D] “a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string”

Zhao teaches the claimed *“plurality of word lines is connected to the first memory string.”* Zhao’s memory can include “96 data word line layers” and “6 dummy word line layers.” Zhao, 7:64-66; *see also id.*, 9:34-38. These “word line layers WLL0-WLL95 connect to” the “memory cells” making up Zhao’s “NAND strings.” *Id.*, 10:8-13; *see also id.*, 12:6-9. The “[d]ummy word line layers DD0, DD1, DS0, DS1, WLDL, and WLDU connect to dummy memory cells” in the strings. *Id.*, 10:11-13.

Zhao also teaches the claimed *“selected word line.”* According to Zhao, during “a programming process[,]” certain memory cells are “selected” “to take on

a new electric characteristic ... to reflect a changed programming state.” Zhao, 3:30-49. To facilitate this, the memory’s word lines are selected one at a time in “order WL0, WL1, WL2, ... WL95.” *Id.*, 17:27-30; *see also id.*, 17:13-45. In Figure 4G below, “word line WL94” is “selected for programming.” *Id.*, 12:14-25.

Figure 4G



Id., Fig. 4G; *see also* Fig. 4F; Liu, ¶¶ 244-251.

[1.E] “a control circuit configured to” / [11.E] “[the method comprising]”

Zhao includes the claimed “*control circuit*” that performs a pre-charging “*method.*” Zhao’s memory includes “[c]ontrol circuitry 310” that “perform[s] memory operations ... on memory structure 326.” Zhao, 5:64-66. Among other components, the “control circuitry” includes a “power control circuit 316” that “creat[es] voltages.” *Id.*, 5:66-6:20. This allows the “control circuit” to “perform[.]” the “process for programming.” *Id.*, 13:65-14:6. The “controller” also includes a

“pre-charge circuit 584” that is responsible for “perform[ing] the pre-charging of the channels of unselected NAND strings, including applying the pre-charge signals” at the appropriate time during the programming process. *Id.*, 16:40-67; *see also* Fig. 8; Liu, ¶¶ 252-255.

[11.E.0] “[applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period]”

[1.E.1]/[11.E.1] “apply[ing] a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a [the] pre-charge period”

[1.E.2]/[11.E.2] “apply[ing] a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and”

[1.E.3]/[11.E.3] “apply[ing] a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period”

This is all obvious over Zhao. Zhao teaches a system in which different “*word line pre-pulse signal[s]*” can be applied to a memory’s “*word lines*” “*during a pre-charge period.*” Zhao explains that “[t]o assist in ... boosting[,]” its “control circuit” can “pre-charge” the “channels of NAND strings.” Zhao, 13:65-14:1, 14:35-40; *see also id.*, 16:65-67. As shown in Figure 7, this “pre-charge” (step 542) occurs before application of a “program pulse” (step 546):

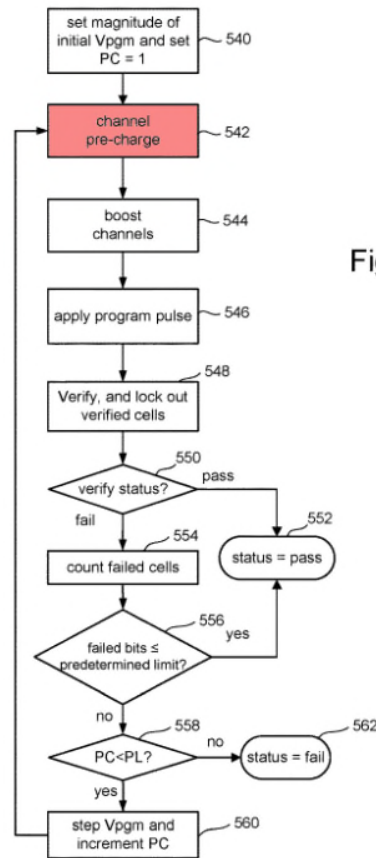


Figure 7

Id., Fig. 7; *see also id.*, 14:35-55.

Zhao goes on to explain that its “memory system pre-charges the channels of at least a subset of unselected NAND strings, ... prior to” programming “by applying one or more pre-charge voltages to the selected word line and drain side unselected word lines.” Zhao, 19:12-17. According to Zhao, “[b]y applying these pre-charge voltages, the voltage of the channel will be raised, which will improve the future boosting.” *Id.*, 19:17-19. The “voltage[s] applied to the control gates” are in the form of “pulses.” *Id.*, 14:7-16. And multiple different “pre-charge voltages” are employed. *Id.*, 19:19-60. For instance, “only” word lines on the “drain side of the

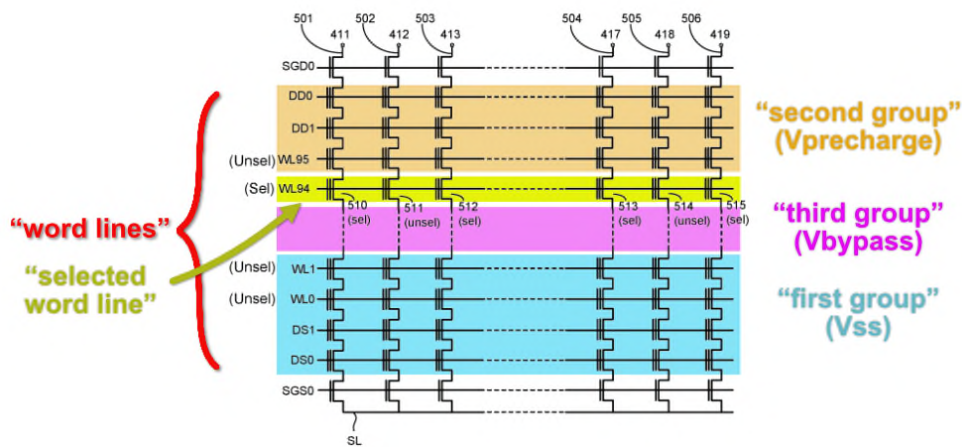
channel” (*i.e.*, those between the currently selected word line and the top select gate) can receive a “pre-charge” voltage. *Id.*, 19:19-23; 19:57-58. The majority of the “source side” word lines “receive 0 volts or one or more voltages that are too low to pre-charge.” *Id.*, 19:22-23. And “multiple already programmed (e.g., source side) unselected word line[s] ... adjacent to the selected word line” can “receive[]” a different “bypass voltage” “while pre-charging[.]” *Id.*, 19:32-50.

Annotated Figures 4G and 13 below show the application of these various “**word line pre-pulse signal[s]**” during a “**pre-charge period.**” Zhao explains that “time period ... t1-t3 corresponds to pre-charging.” Zhao, 22:39-41. Again, three different voltages are applied to different groups of word lines in this period. “Vprecharge (e.g., ~2 volts)” is applied to “selected word line WLn” and “drain side unselected word lines WLn+x.” *Id.*, 22:41-49. “Vbypass (e.g., ~6-10 volts)” is applied to “already programmed source side unselected word lines WLn-1 and WLn-2[.]” *Id.*, 22:50-53. And “[t]he remaining source side unselected word lines WLn-x remain at Vss (e.g., 0 v).” *Id.*, 23:7-9. While Vss is 0V in the Figure, Zhao explains that a “low” non-zero voltage can be supplied instead in the same t1-t3 time period as the other pre-charge voltage pulses. *Id.*, 19:22-24.

This results in what this limitation requires. A “**first word line pre-pulse signal**” (a low non-zero voltage in place of Vss, blue) is applied to a “**first group of ... word lines**” (the source-side word lines not adjacent to the selected word line,

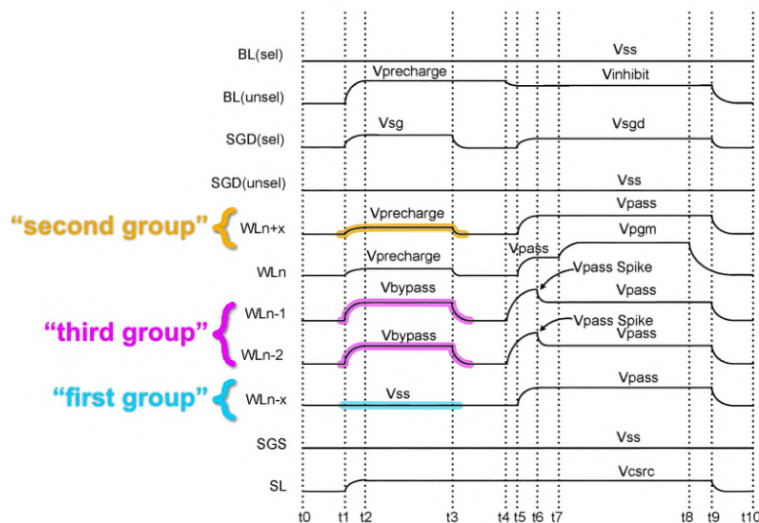
WLn-x), a “*second word line pre-pulse signal*” (Vprecharge, orange) is applied to a “*second group of ... word lines*” (the drain-side word lines, WLn+x), and a “*third word line pre-pulse signal*” (Vbypass, purple) is applied to a “*third group of ... word lines*” (the source-side word lines adjacent to the selected word line, WLn-1 and WLn-2):

Figure 4G



Zhao, Fig. 4G.

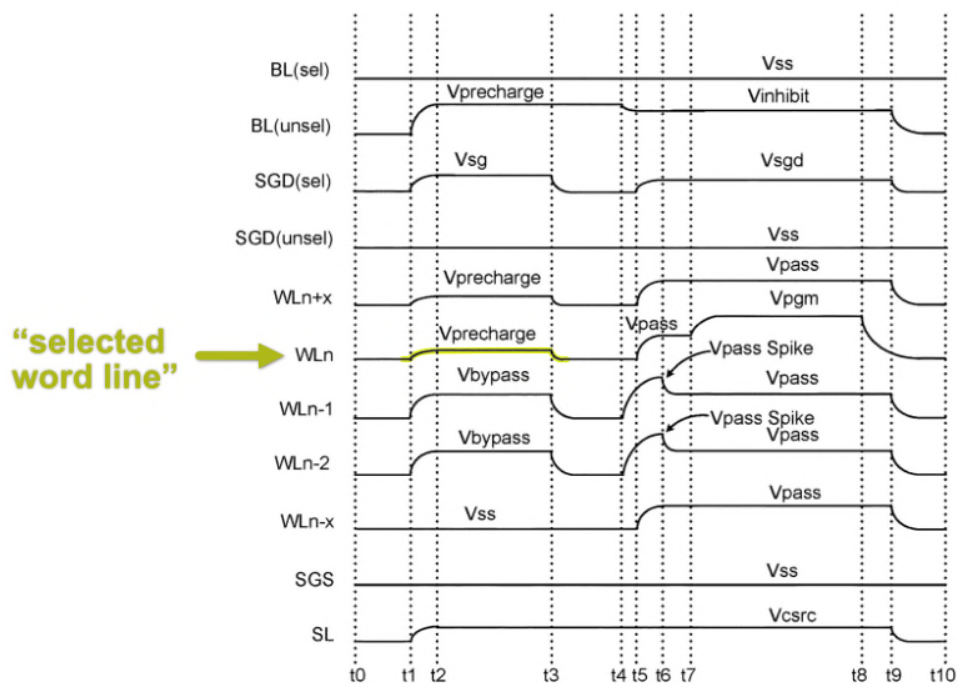
Figure 13



Id., Fig. 13; Liu, ¶¶ 256-274.

Claim 11 additionally requires application of a “*word line signal to the selected word line*” during this same “*pre-charge period[.]*” This is also taught by Zhao. In particular, Zhao explains that during “pre-charging” time period “t1-t3[.]” “the selected word line WLn is raised to the pre-charge voltage....” Zhao, 22:39-49; *see also id.*, 19:12-19. This is also shown in Figure 13:

Figure 13



Id., Fig. 13; *see also* Liu, ¶¶ 275-278.

[1.E.4]/[11.E.4] “wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal”

Zhao renders this obvious: the voltage of Zhao’s “*third word line pre-pulse signal*” (Vbypass, 6-10V) is highest, the voltage of its “*second word line pre-pulse*

signal” ($V_{\text{precharge}}$, 2V) is next highest, and the voltage of its **“first word line pre-pulse signal”** (a “low” non-zero voltage in place of V_{ss}) is lowest. Zhao, 19:19-23; 19:57-58; 22:39-23:9; Fig. 13; *see also* Liu, ¶¶ 279-280.

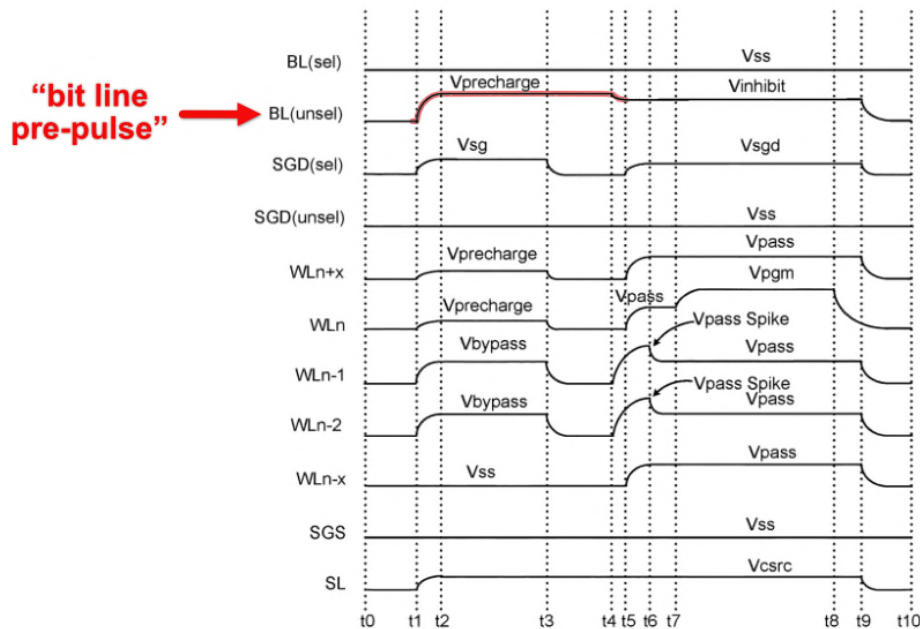
2. Claims 4 and 14

Claim 4 depends on claim 1. Claim 14 depends on claim 11. Both claims similarly require:

that “the control circuit is configured to apply” (claim 4) or “applying” (claim 14) “a bit line pre-pulse signal to the bit line during the pre-charge period”

Zhao’s **“control circuit”** applies a **“bit line pre-pulse signal” “during the pre-charge period.”** As explained in connection with claim 1, Zhao includes “control circuitry” that “performs the pre-charging of the channels of unselected NAND strings” by “applying the pre-charge signals....” Zhao, 16:53-67; *see also id.*, 5:64-6:20; 13:65-14:6. And as part of this “the unselected bit lines are raised to a pre-charge voltage $V_{\text{precharge}}$ (e.g., ~2 volts)” during the “t1-t3 ... precharging” period. *Id.*, 22:39-44. The unselected bitline is maintained at this voltage until the beginning of a later “boosting” period that begins at t4. *Id.*, 23:13-18. This is shown in Figure 13:

Figure 13



Id., Fig. 13; *see also* Liu, ¶¶ 281-287.

3. Claims 5 and 15

Claim 5 depends on claim 4. Claim 15 depends on claim 14. Both claims further require that:

“the first memory string is an unselected memory string, and the bit line is an unselected bit line”

Zhao explains that it “pre-charges the channels of ... unselected NAND strings ([i.e.] channels connected to unselected memory cells.)” Zhao, 19:10-17. And as part of this, Zhao applies a “pre-charge voltage” pulse to “unselected bit lines.” *Id.*, 22:39-45; *see also* Fig. 13; Liu, ¶¶ 288-292.

4. Claim 6

Claim 6 depends on claim 1 and further requires that:

“the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines”

This is taught by Zhao for the same reasons explained in connection with limitation [11.E.0]: during “pre-charging,” “the selected word line WL_n is raised to the pre-charge voltage....” Zhao, 22:39-49; *see also id.*, 19:11-17; Fig. 13; *supra* discussion of limit [11.E.0]. Zhao also applies a “program signal V_{pgm} ... to the selected word line” during later programming. Zhao, 14:49-51; Fig. 13; Liu, ¶¶ 293-296.

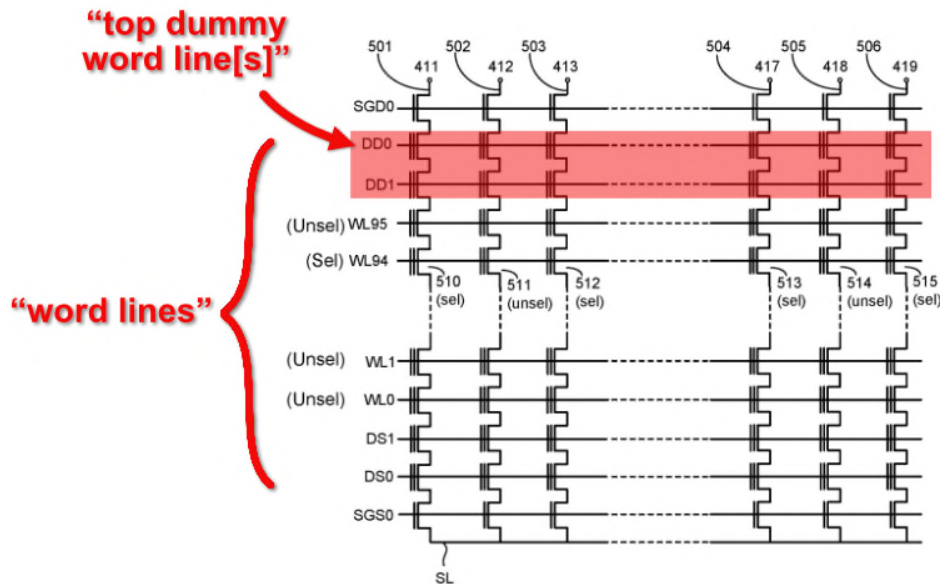
5. Claims 7 and 16

Claim 7 depends on claim 1. Claim 16 depends on claim 11. Both claims similarly require that:

“[the control circuit is configured to] apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the pre-charge period”

Zhao’s memory includes *“a top dummy word line of the plurality of word lines.”* According to Zhao, its memory can include “6 dummy word line layers.” Zhao, 7:64-66; *see also id.*, 9:34-38. Two of these—dummy word line layers DD0 and DD1—are located on the upper “drain” side of Zhao’s “memory structure.” *Id.*, 9:30-39, 9:56-61, 10:6-13. This is shown in Figure 4G below:

Figure 4G



Id., Fig. 4G.

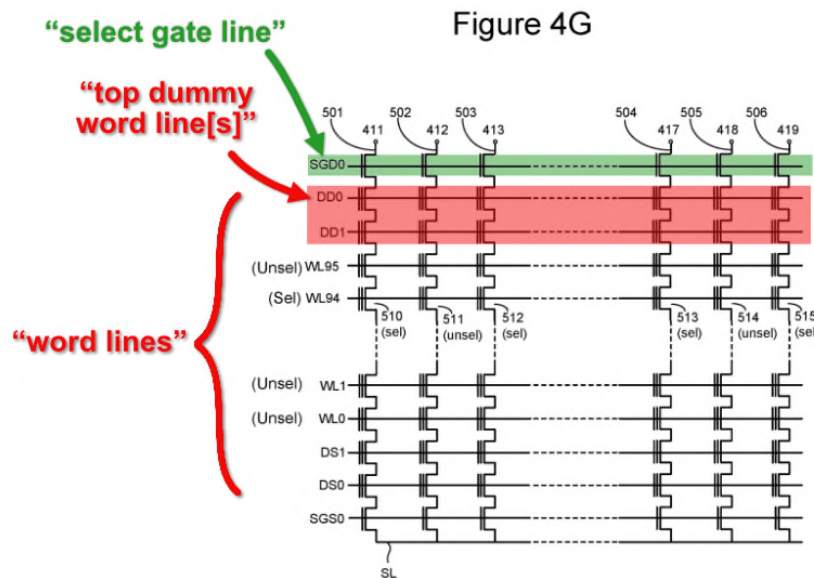
Next, Zhao explains that “the dummy word lines are operated in the same manner as unselected word lines.” Zhao, 24:11-13; *see also id.*, 25:31-32. Again, Zhao’s “drain side unselected word lines $WLn+x$ ” are supplied with the “pre-charge voltage” ($V_{precharge}$) “to cause pre-charging” during the “pre-charging” “time period.” *Id.*, 22:39-49. Because they are operated in the same manner as the unselected word lines, a POSITA would have understood that Zhao’s drain-side dummy word lines DD0-DD1 would be supplied with the same pre-charge voltage $V_{precharge}$. *See* Liu, ¶¶ 297-306. This is the claimed “**top dummy word line pre-pulse signal**” “**appl[ied]**” “**during the pre-charge period.**” *Id.*

6. Claim 18

Claim 18 depends on claim 16 and further requires that:

“the top dummy word line is disposed between the third group of the plurality of word lines and the select gate line”

Zhao teaches this. Zhao’s *“select gate line”* (SGD0) is located at the top of its memory structure. Zhao’s *“top dummy word line”* (DD0-DD1) are located immediately below the *“select gate line.”* The *“third group of the plurality of word lines”* (already programmed source-side word lines WLn-1 and WLn-2) are located below these lines and within the collection of the other *“word lines”* (WL0-WL95):



Zhao, Fig. 4G; Liu, ¶¶ 307-311.

7. Claims 9 and 19

Claim 9 depends on claim 1. Claim 19 depends on claim 11. Both claims further require that:

“the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third word line pre-pulse signal are positive”

Zhao teaches the use of *“positive” “pre-pulse signal” “voltage levels.”* In

particular, Zhao's "***third word line pre-pulse signal***" (Vbypass) can be "~6-10 volts." Zhao, 22:50-53. Zhao's "***second word line pre-pulse signal***" (Vprecharge) can be "~2 volts." *Id.*, 22:43-44. And Zhao's "***first word line pre-pulse signal***" (the voltage applied to the source-side unselected word lines) can be "0 volts or one or more voltages that are too low to pre-charge." *Id.*, 19:23-26; *see also id.*, Fig. 13 (showing the use of various positive pre-charge voltages); Liu, ¶¶ 312-317.

C. Ground 3: Obviousness over Zhao and Lee

The claims addressed in Ground 2, along with additional dependent claims 2-3, 8, 12-13, and 17, are also obvious over Zhao when modified in view of Lee's teachings and the knowledge possessed by a POSITA.

1. Claims 1, 4-7, 9, 11, 14-16, and 18-19

As explained in Ground 2, Zhao itself renders claims 1, 4-7, 9, 11, 14-16, and 18-19 obvious. Just as these claims require, Zhao applies three different "***pre-pulse signal[s]***" to "***group[s]***" of word lines during a "***pre-charge period.***" More specifically, Zhao programs its word lines one at a time starting at the source-side of its memory structure and ending at the drain-side. The word line currently being programmed is "selected" and supplied with a pre-charge voltage and later programming voltage (the claimed "***word line signal***"). Vprecharge (Zhao's "***second***" signal) is applied to the unselected word lines on the drain-side of the selected word line (the "***second***" group). Vbypass (Zhao's "***third***" signal) is applied

to the first two source-side word lines adjacent to the selected word line (the “*third*” group). And a low, non-zero voltage in place of V_{ss} (Zhao’s “*first*” signal) is applied to the remaining source-side word lines (the “*first*” group). *See supra* discussion of limitations [1.E.1]-[1.E.3].

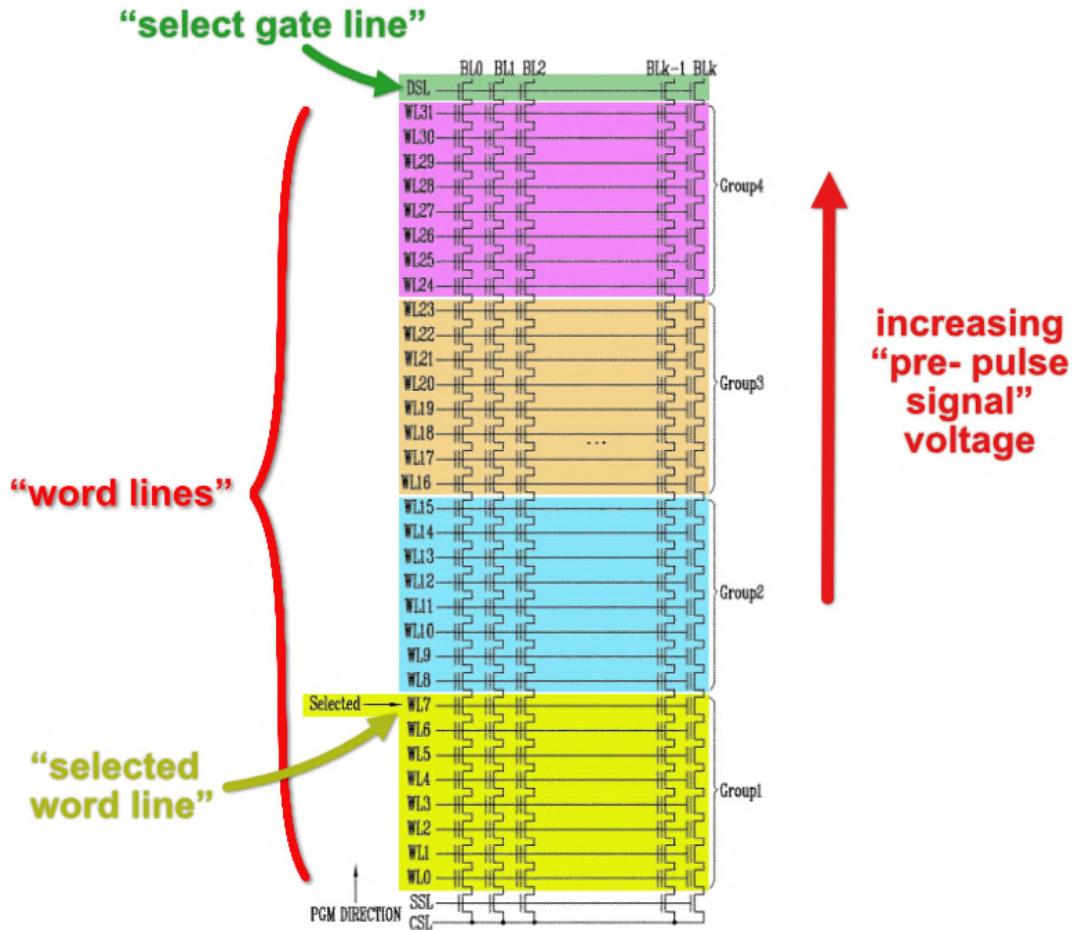
Zhao also renders these same claims obvious for additional reasons when modified following Lee’s teachings. As repeatedly explained above, Zhao applies the same “V_{precharge}” “pre-charge voltage” to all unselected word lines on drain-side of the currently selected word line. *E.g.*, Zhao, 22:39-49; *see also id.*, 14:35-39; 16:65-67; 19:9-29; Figs. 7, 13. This is intended to “[t]o assist in ... boosting” of the word lines that are “inhibited from programming.” *Id.*, 14:35-40; *see also id.*, 19:17-19 (similarly explaining that “[b]y applying these pre-charge voltages, the voltage of the channel will be raised, which will improve the future boosting.”).

Lee, however, highlights a problem with this approach. According to Lee, in a “typical ... precharge operation of an unselected memory string, a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor.” Lee, 8:25-29. This “reduce[s]” “the precharge level” such that “boosting is not effectively generated” and “program disturb occurs.” *Id.*, 8:29-32.

To account for this effect, Lee teaches that “[t]he word lines coupled to a memory string in a memory block may be grouped ... during a precharge operation

of the cell string.” Lee, 7:58-61; *see also id.*, 2:4-5. For example, in Figure 4B of Lee, thirty-two word lines are arranged into four groups of eight. *Id.*, 9:36-40. Then, according to Lee, “different pre-bias voltages may be applied to the respective groups during a precharge operation...” *Id.*, 7:58-61; *see also* Abstract; *see also id.*, 1:62-2:3. The closer “a word line group to which a word line belongs is to the” upper “drain select transistor, the higher a pre-bias voltage ... applied to the word line may be.” *Id.*, 8:32-37; *see also id.*, 2:5-9. While different voltages are applied to the drain-side word lines, the selected word line and the source-side word lines may continue to be supplied with a “default value.” *Id.*, 2:23-29; 9:36-59.

The below demonstrative—based on Figure 4G—provides an example of this. Lee’s word lines are arranged in four groups (Group1, Group2, Group3, Group4). WL7 is currently selected for programming. Thus, Group1 is provided with a “default” voltage during pre-charging. The word lines in Group2, Group3, and Group4, however, are provided with increasingly higher pre-charge voltages:



Lee, Fig. 4B (modified to show WL7 selected); Liu, ¶¶ 320-339.

Lee goes on to explain that by employing different pre-bias voltages with different groups of word lines, it “offset[s]” the “effects caused by the resistance component between the source select transistor and the drain select transistor” and allows a “uniformly formed” “precharge level” “in the entirety of the cell string.” Lee, 7:61-62; 8:47-52. This in turn further “mitigate[s] [the] program disturb phenomenon....” *Id.*, 1:52-56; 8:51-52; 15:4-7; Liu, ¶ 340.

While Zhao itself also renders the claims obvious, applying this teaching from

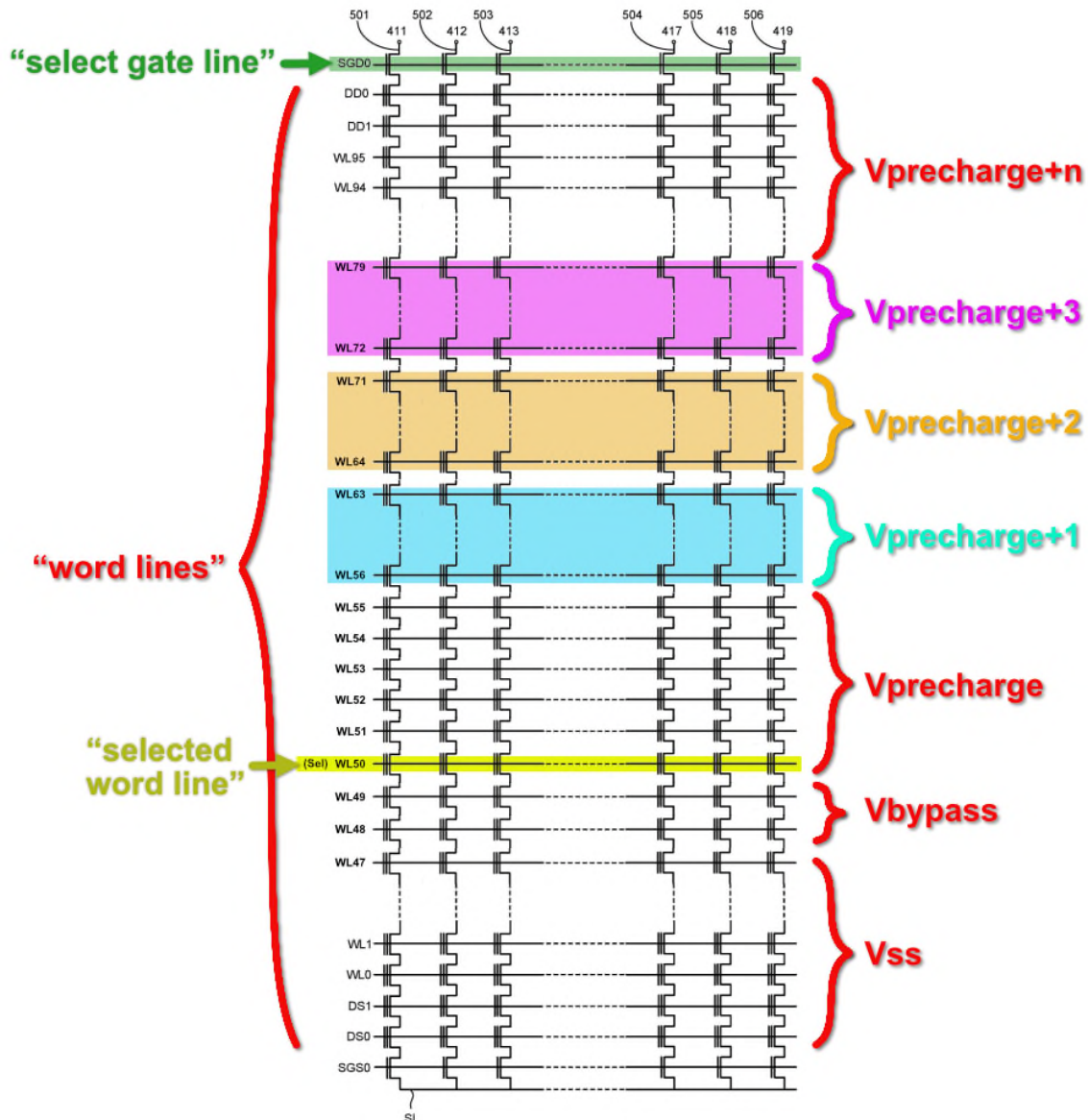
Lee to Zhao gives rise to yet another reason why the claimed subject matter would have been considered obvious by a POSITA. Rather than applying the same Vprecharge voltage to all Zhao's unselected drain-side word lines, Zhao's word lines would be evenly grouped and different, increasing pre-charge voltages would be applied to the different groups of drain-side word lines based on their location relative to the drain select transistor. Liu, ¶¶ 341-343. The following discussion provides an example.

Zhao explains that its memory may employ "six dummy word line layers DD0, DD1, DS0, SD1, WLDL, WLDU" and "ninety six data word line layers WLL0-WLL95." Zhao, 9:34-39. Following Lee's example, the word lines can be divided into twelve groups of eight: WL0-WL07, WL08-WL15, WL16-WL23, WL24-WL31, WL32-WL39, WL40-WL47, WL48-WL55, WL56-WL63, WL64-WL71, WL72-WL79, WL80-WL87, and WL88-WL95. *See* Liu, ¶¶ 344-346. Per Zhao, the "dummy word lines are operated in the same manner as unselected word lines." Zhao, 24:12-14, 25:31-33. So, the lower dummies would be grouped with WL0-WL07, while the upper dummies would be grouped with WL88-WL95. *See* Liu, ¶ 347. In Zhao, the word lines are programmed in order from WL0 to WL95. *See* Zhao, 17:27-29. Zhao also includes an example where "WL50 is the selected word line." *Id.*, 17:21-25. This selected word line is part of the group that includes WL48-WL55.

Again, Lee teaches that the group containing the “selected” word line can be supplied with “default” pre-charge value. Lee, 9:36-59. Thus, Zhao’s treatment of the word lines in this group would remain the same: both selected WL50 and drain-side unselected WL51-WL55 would continue to be supplied with $V_{precharge}$, and the two adjacent source-side unselected WL48-WL49 would continue to be supplied with V_{bypass} . See Liu, ¶¶ 348-352.

But, following Lee’s teachings, the other groups of unselected drain-side word lines are now treated differently during the pre-charge period. WL56-WL63 would now receive a higher pre-charge voltage like $V_{precharge}+1$, WL64-WL71 would receive a still higher pre-charge voltage like $V_{precharge}+2$, WL72-WL79 would receive an even higher pre-charge voltage like $V_{precharge}+3$, and so on until the last group of drain-side word lines, which would receive $V_{precharge}+n$. Liu, ¶ 352.

An example of this is shown in the demonstrative below:



Id., ¶ 353.

These collections of drain-side word lines receiving increasingly higher pre-charge voltages correspond to claimed “*groups*”: WL56-WL63 are the “*first group*” that receive a “*first ... pre-pulse signal*” ($V_{\text{precharge}+1}$); WL64-WL71 are the “*second group*” that receive a higher “*second ... pre-pulse signal*” ($V_{\text{precharge}+2}$); and WL72-WL79 are the “*third group*” that receive an even higher “*third ... pre-*

pulse signal” ($V_{\text{precharge}+3}$). Liu, ¶ 354. Moreover, these “*groups*” are now arranged sequentially between the “*selected word line*” (WL50 in this example) and Zhao’s “*top select gate line*” (SGD0). *Id.*, ¶ 355.

A POSITA would have been motivated to apply Lee’s teachings to Zhao in the manner described above. A POSITA would have recognized that while Zhao addresses some sources of program disturb, it does not fully mitigate the phenomena. For instance, it does not take channel resistance into account. Liu, ¶¶ 356-358. A POSITA also would have recognized that this would have resulted in less effective boosting and increased program disturb. *Id.*, ¶ 359. This would have been particularly the case when programming word lines closer to the source-side of a memory string. *Id.*, ¶ 360. In such circumstances, the channel length between the drain-side of the string and word line selected for programming would be quite long, resulting in a relatively high channel resistance. *Id.* A POSITA would have recognized that Lee presents a solution to this problem: it groups word lines and applies different, higher pre-charge voltages to the drain-side unselected word lines to offset the channel resistance effect. *Id.*, ¶ 361. A POSITA would have recognized that applying this approach to Zhao would allow it to achieve more uniform pre-charging, better boosting, and reduced program disturb. *Id.*, ¶ 362. Additionally, by reducing the voltage applied to certain drain-side word lines, cell endurance is increased. *Id.*, ¶ 363.

A POSITA also would have recognized that Lee furthers Zhao’s own design goals. Liu, ¶¶ 364-367. Zhao repeatedly explains that its memory employs various “countermeasures” to “prevent ... program disturb.” *E.g.*, Zhao, 2:10-26, 4:7-10, 18:52-59. As part of this, Zhao seeks to avoid “voltage differential[s]” in “the channel” of an unselected NAND string. *E.g.*, *id.*, 22:65-23:5. Lee also reduces program disturb and does so by ensuring a uniform channel voltage. Lee, 7:61-62; 8:47-52. This similarity in purpose also would have motivated a POSITA to apply Lee’s teachings to Zhao. *See* Liu, ¶ 367.

Next, a patent’s claims are obvious when they “simply arrange[] old elements with each performing the same function it had been known to perform and yield[] no more than one would expect from such an arrangement...” *KSR Int’l Co. v. Teleflex Inc.*, 550 US 398, 406 (2007). This is the case here. The combination of Zhao and Lee would continue to produce the respective benefits discussed in these two references. *See* Liu, ¶¶ 368-371. For instance, the various countermeasures discussed in Zhao—including the application of a higher “Vbypass” pre-charge voltage to source-side unselected word lines—would still be employed to “reduce[] or eliminate the voltage differential between the source side of the channel and the drain side of the channel that may later cause program disturb.” Zhao, 22:65-23:12; *see also* Liu, ¶ 370. And use of Lee’s teachings would offset the resistance effects on the drain-side of the selected word line for purposes of further reducing program

disturb. *See id.*, ¶ 371.

A POSITA also would have had a reasonable expectation of success. Zhao's memory is already able to apply different pre-charge voltages to different groups of word lines. Liu, ¶¶ 372-374. Further, Zhao already expressly contemplates that "one or more pre-charge voltages" can be applied "to the selected word line and drain side unselected word lines" during pre-charging. *E.g.*, Zhao, 19:9-17. Given this, a POSITA would have considered the application of Lee to Zhao to amount to nothing more than a straightforward extension of Zhao's existing teachings. Liu, ¶¶ 373-375.

2. Claims 2 and 12

Claim 2 depends on claim 1. Claim 12 depends on claim 11. Both claims further require that:

"the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines"

This is obvious in view of Zhao and Lee. As explained, Lee teaches that the closer "a word line group to which a word line belongs is to the" upper "drain select transistor, the higher a pre-bias voltage ... applied to the word line may be." Lee, 8:32-37; *see also id.*, 2:5-9. When this teaching is applied to Zhao, this claim is satisfied. Zhao's "*first*," "*second*," and "*third*" "*group[s] ... of word lines*" (WL56-WL63, WL64-WL71, and WL72-WL79) are "*disposed in an order of*

distance from the selected word line” (WL50). See Liu, ¶¶ 376-383.

3. Claims 3 and 13

Claim 3 depends on claim 1. Claim 13 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line”

This is also obvious in view of Zhao and Lee. As explained, Zhao’s memory includes upper “[d]rain side select layers[,]” including a layer SGD0 shown in Figure 4G. Zhao, 7:64-66; see also *id.*, 9:34-38; 10:19-21; 11:59-60; Fig. 4G. This is the claimed **“select gate line.”** See *supra* discussion of limitation [1.C]. Because this **“select gate line”** is located at the top of Zhao’s memory, the **“first,” “second,”** and **“third” “group[s] ... of word lines”** (WL56-WL63, WL64-WL71, and WL72-WL79) are arranged in order between the **“selected word line”** (WL50) and the **“select gate line”** (SGD0) as required. See Liu, ¶¶ 384-388.

4. Claims 8 and 17

Claim 8 depends on claim 7. Claim 17 depends on claim 16. Both claims further require:

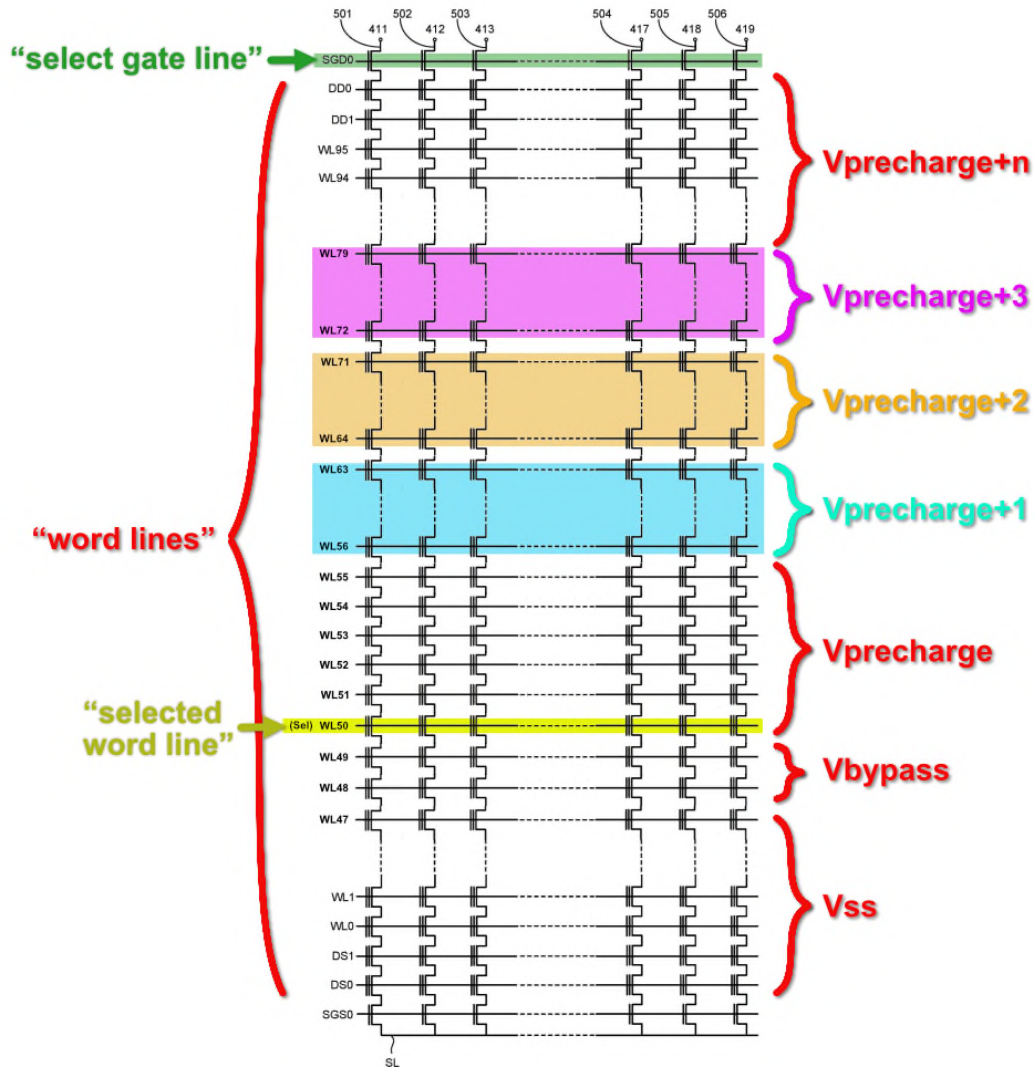
“a voltage level of the top dummy word line pre-pulse signal is greater than that of the third word line pre-pulse signal”

This is also obvious in view of Zhao and Lee. Again, Zhao’s memory includes

multiple top dummy lines. *See* Zhao, Fig. 4G (showing top dummy lines DD0-DD1 adjacent to WL95). Zhao also teaches that these “dummy word lines are” to be “operated in the same manner as unselected word lines.” *Id.*, 24:12-13; *see also id.*, 25:31-32.

As explained, a POSITA would have understood that Zhao’s top dummy word lines should be supplied with the same pre-charging voltage as the adjacent active word lines. *See supra* discussion of claims 7/16 in Ground 2. And following Lee’s teachings, Zhao’s drain-side unselected word lines will have increasingly higher pre-charge voltages the closer they are to the drain-side select gate. *See supra* Section IX.C.1. Zhao’s dummy word lines DD0-DD1 are much closer to the drain-side select gate than its “third” group of word lines (WL72-WL79). *See* Zhao, Fig. 4G; *see also* Liu, ¶¶ 391-395. Thus, following Lee’s teachings, a POSITA would have understood that these dummy word lines would be supplied with a “**top dummy word line pre-pulse signal**” with a “**voltage level**” that is higher than that of the “**third word line pre-pulse signal**” supplied to the “**third**” group of word lines. *See id.*, ¶ 396.

The demonstrative below provides an example. Top dummy lines DD0-DD1 receive $V_{precharge}+n$, which exceeds $V_{precharge}+3$:



Liu, ¶ 397.

D. *Ground 4: Obviousness Over Yang*

Claims 1-7, 9, 11-17, and 18-19 are all obvious over Yang when considered in view of the knowledge of a POSITA.

1. *Independent Claims 1 and 11*

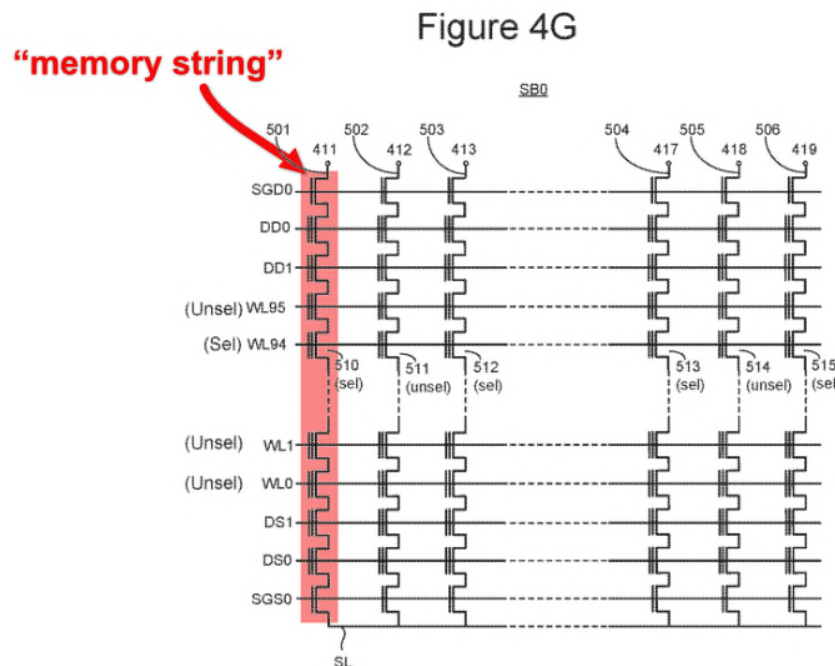
[1.Pre]/[11.Pre] “A [method of controlling a memory device, the] memory device, comprising”

To the extent limiting, Yang teaches this. Yang teaches a “memory system

100” with a “memory structure 126.” Yang, 3:52-61. The memory also employs certain “[t]echniques ... for pre-charging NAND strings during a programming operation.” *Id.*, 2:23-25; *see also* Liu, ¶¶ 400-403.

[1.A]/[11.A] “a plurality of memory strings”

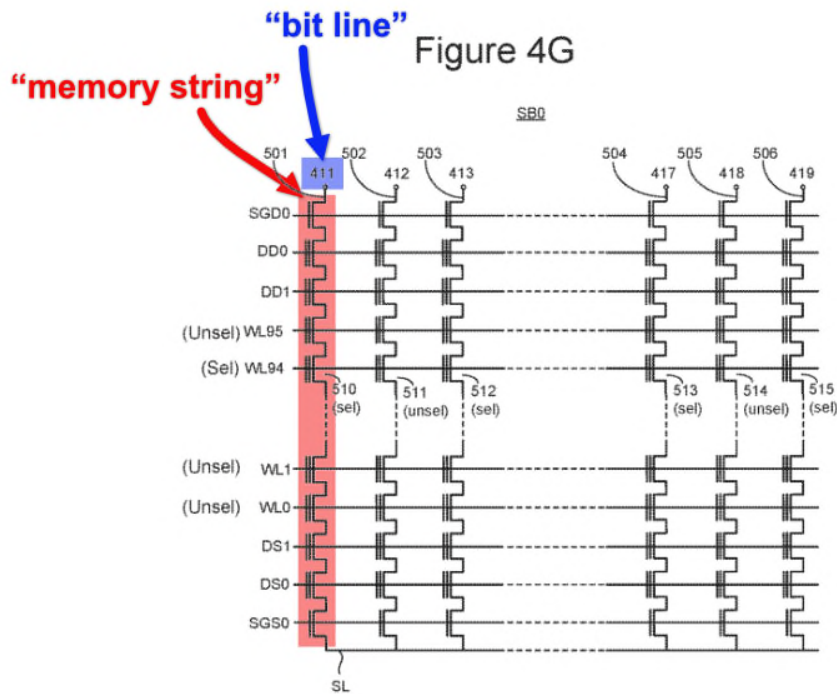
Yang teaches a memory with “*a plurality of memory strings.*” Yang’s memory structure, like all NAND memory, “has strings of non-volatile memory cells that have a select transistor at each end. Typically, such strings are referred to as NAND strings.” Yang, 1:16-19; *see also id.*, 2:24-30. Figure 4G depicts an example “sub-block” of Yang’s memory. *Id.*, 14:35. While the block “will have thousands of NAND strings[,]” “six NAND strings 501, 502, 503, 504, 505, and 506” are depicted. *Id.*, 14:38-42. One example string is annotated red:



Id., Fig. 4G; *see also* Liu, ¶¶ 404-408.

[1.B]/[11.B] “a bit line connected to a first memory string of the plurality of memory strings”

Yang teaches the claimed *“bit line connected to a first memory string.”* According to Yang, each “NAND string” in its memory structure “may have a drain side select transistor at one end that connects the string to a bit line.” Yang, 1:19-20; *see also id.*, 2:23-30. Figure 4G “depicts a set of bit lines ... 411, 412, 413, 414, ... 419.” *Id.*, 11:18-28; 14:14-20. Bit line 411 is connected to NAND string 501:

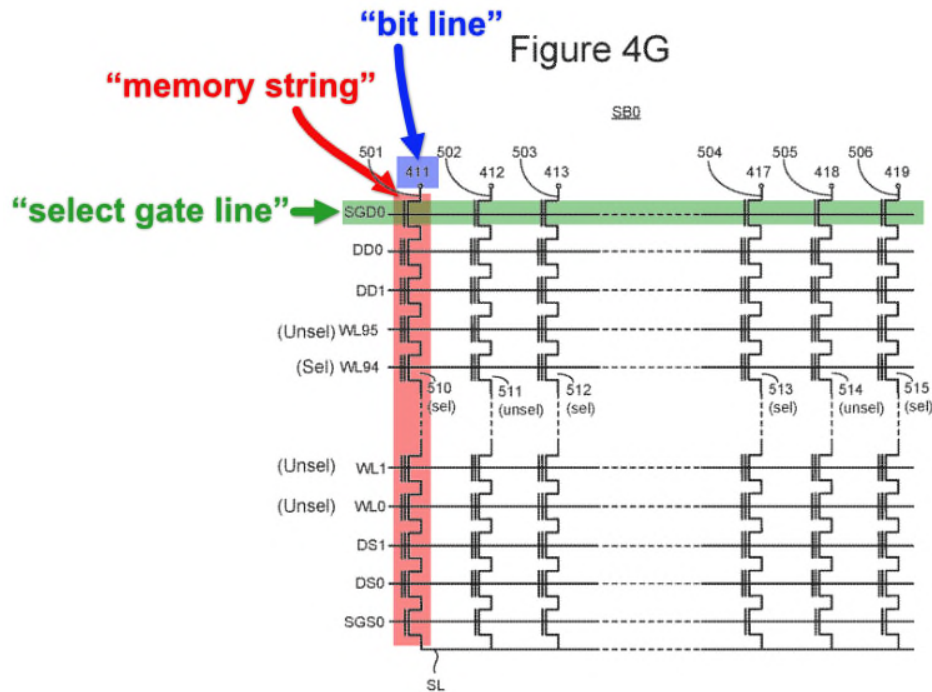


Id., Fig. 4G; *see also* Liu, ¶¶ 409-412.

[1.C]/[11.C] “a select gate line connected to the first memory string of the plurality of memory strings”

Yang teaches a *“select gate line connected to the first memory string.”* According to Yang, its memory structure includes multiple “select layers.” Yang, 8:67-9:2. This includes an upper “drain-side SG layers” that are “associated with

the drain side of a set of NAND strings.” *Id.*, 13:1-5. The “[d]rain side selection lines” “are used to determine which ... NAND strings connect to the associated bit lines.” *Id.*, 14:20-25. Drain-side select gate layer SGD0 is annotated green below:

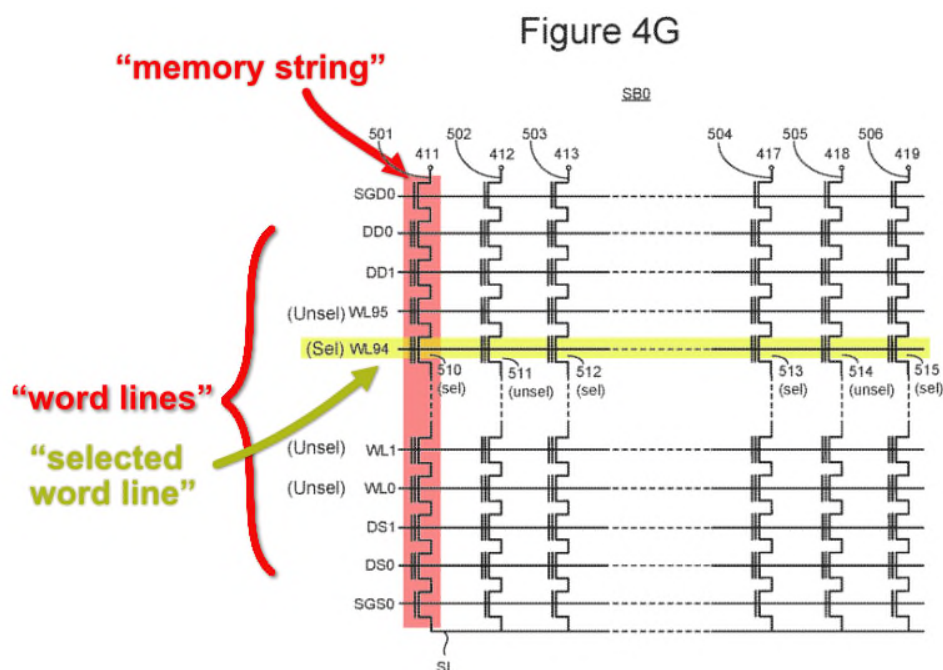


Id., Fig. 4G; see also Liu, ¶¶ 413-417.

[1.D]/[11.D] “a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string”

Yang teaches a memory with “*a plurality of word lines*” that are “*connected to the first memory string.*” In one example, Yang’s memory structure includes “96 data word line layers” and “6 dummy word line layers.” Yang, 8:67-9:2. And as shown in Figure 4G, “WL0-WL95 run[] across the entire sub-block” and connect to the various “NAND strings.” *Id.*, 14:35-42. Yang also explains that certain of its “word line[s]” are “selected” during memory operation “to receive programming.”

Id., 2:35-38; *see also id.*, 14:50-54. In Figure 4G, “word line WL94” has been “selected.” *Id.*, 15:7-16. This is the claimed “*selected word line*”:



Id., Fig. 4G; *see also* Liu, ¶¶ 418-422.

[1.E] “a control circuit configured to” / [11.E] “[the method comprising]”

Yang teaches a “*control circuit*” that performs the claimed “*method.*” Yang includes “[c]ontrol circuitry 110” with, among other components, “a power control circuit 116.” Yang, 4:14-18. The “[p]ower control circuit 116 controls the power and voltages applied to the word lines, bit lines, and select lines during memory operations.” *Id.*, 4:25-27. This allows Yang’s control circuitry to engage in “programming” of “NAND strings.” *Id.*, 16:31-37; Liu, ¶¶ 423-426.

[11.E.0] “[applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period]”

[1.E.1]/[11.E.1] “apply[ing] a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a [the] pre-charge period”

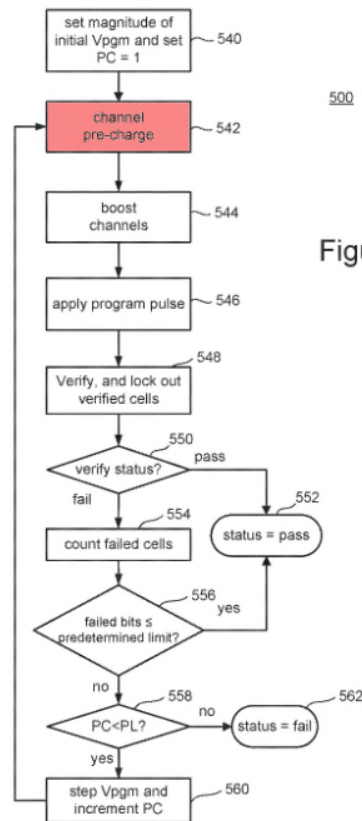
[1.E.2]/[11.E.2] “apply[ing] a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and”

[1.E.3]/[11.E.3] “apply[ing] a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period”

Yang’s memory obviously organizes its word lines into the various “*group[s]*” and applies the different “*signal[s]*” these limitations collectively require.

As an initial matter, Yang renders obvious the application of “*pre-pulse signals*” to a memory structure’s “*word lines*” “*during a pre-charge period.*” According to Yang, its “programming operation has a channel pre-charge phase.” Yang, 2:42-46. This “pre-charge phase” occurs before a later “program phase.” *Id.*, 21:40-50. During the “pre-charge phase[,]” “channels of unselected NAND strings ... are pre-charged to a desired voltage level.” *Id.*, 21:46-50. Then, during the “program phase ... selected memory cells connected to the selected word line are programmed” while “unselected memory cells connected to the selected word line are inhibited from programming.” *Id.*, 21:50-54. Figure 5 shows this initial “pre-charge” step 542, along with the later step 546 where “a program pulse” is applied.

Id., 17:7-41.



Id., Fig. 5.

Yang also renders obvious the application of different “*pre-pulse signals*” to different “*group[s]*” of its word lines. According to Yang, “[i]f the channel of the unselected NAND string is not adequately pre-charged during the pre-charge phase, the NAND channel may fail to boost to a sufficient voltage during the programming phase to adequately prevent program disturb.” Yang, 2:58-62. The string may not be adequately pre-charged if, for instance, there is “valid data” in memory cells above or below a cell currently selected for programming. *Id.*, 3:20-27.

To avoid this problem, Yang applies different pre-charge voltages to different sets of word lines. This includes an “overdrive voltage,” “bypass voltage[,]” and “dummy voltage.” Yang, 3:28-39; 24:1-46; *see also id.*, 9:65-10:18; 17:24-28. The applied voltages are in the form of “pulses.” *Id.*, 16:50-53.

Yang also explains which of the various word lines in its memory structure receive the different pre-charge voltages. Yang’s word lines are arranged in “different vertical sub-blocks VSB0, VSB1, VSB2 that are treated as separate units for erase/programming purposes....” Yang, 9:49-61, 12:22-23. Each “sub-block” includes multiple word lines. When the memory structure includes 96 total word lines, “VSB0” can include “WLL0-WLL31,” “VSB1” can include “WLL32-WLL63[,]” and “VSB2” can include “WLL64-WLL95.” *Id.*, 12:23-29. There are also “[d]ummy word line layer[s]” between the sub-blocks. *Id.*, 12:32-35.

Yang applies pre-charge voltages to these various word lines depending on both the sub-block where the line is located and whether it was programmed in prior programming steps (and thus already contains data). In one example shown, “[o]ne of the word lines (WL7) in vertical sub-block VSB1 is selected for programming.” Yang, 25:18-19. Then, the “over-drive voltage” (Vpre_OD) is applied to the “programmed data word lines” in the “upper vertical sub-block VSB2” of the memory structure. *Id.*, 22:4-11; 24:28-33. The “bypass voltage” (Vbypass) is applied to the “word lines in VSB2 that are not programmed” and all the “data word

lines” in VSB1 and VSB0. *Id.*, 22:31-37, 24:11-17. The “dummy pre-charge voltage” (Vpre_dmy) is “applied to all dummy word lines” in the same pre-charge period. *Id.*, 24:18-27.

Figure 8B is a “timing diagram” showing when Yang applies different pre-charge voltage pulses to its word lines, dummy lines, select gates, bit lines, and other lines. *See* Yang, 23:20-23. “[T]imes t1-t4 correspond to ... a pre-charge phase.” *Id.*, 23:23-25. Figure 8C shows an example arrangement of the various word lines, dummy lines, and sub-blocks, along with the different applied pre-charge voltages. *See id.*, 25:29-33. While Figure 8C depicts each sub-block as including only a single dummy word line layer and six data word line layers, Yang explains that “[m]ore or less ... layers can also be used.” *Id.*, 9:2-5. Thus, a POSITA would have understood that Yang also teaches embodiments with more dummy word lines. *See, e.g., id.*, Fig. 4C (showing 96 data word lines, and 2 layers of upper dummy word lines); *see also* Liu, ¶¶ 427-445.

As summarized by the below annotated versions of these figures, Yang renders obvious what claims 1 and 11 require. A “**word line signal**” (Vbypass, yellow in Figure 8B) is applied to “**the selected word line**” (WL7, yellow in Figure 8C). A “**first word line pre-pulse signal**” (Vbypass, blue in Figure 8B) is applied to “**a first group ... of word lines**” (non-data containing WL8-WL11 in VBS1, blue in Figure 8C). A “**second word line pre-pulse signal**” (Vpre_dmy, orange in Figure

8B) is applied to ***“a second group ... of word lines”*** (the dummy word lines between VBS1 and VBS2, orange in Figure 8C). And a ***“third word line pre-pulse signal”*** (Vpre_OD, purple in Figure 8B) is applied to ***“a third group ... of word lines”*** (previously programmed and data-containing WL12-WL14 in VSB2, purple in Figure 8C). All of these signals are applied during the same ***“pre-charge period”*** (t1-t3):

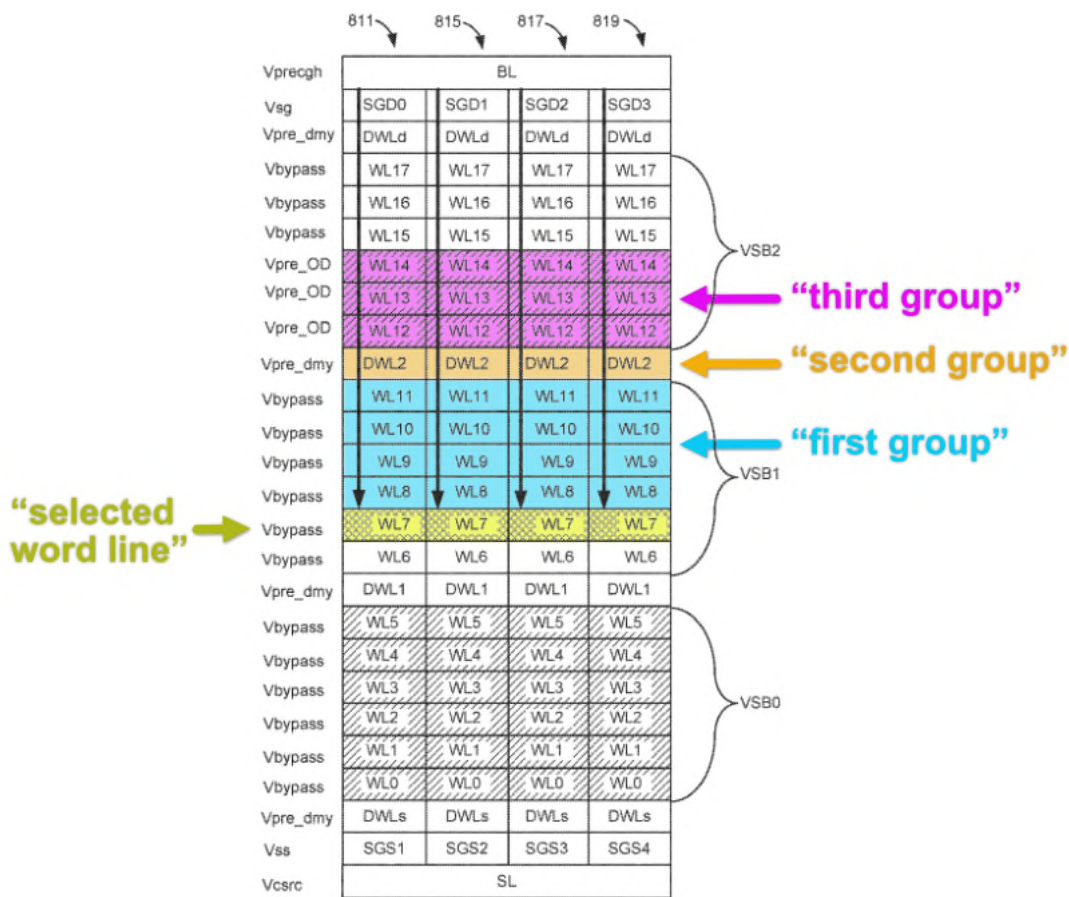
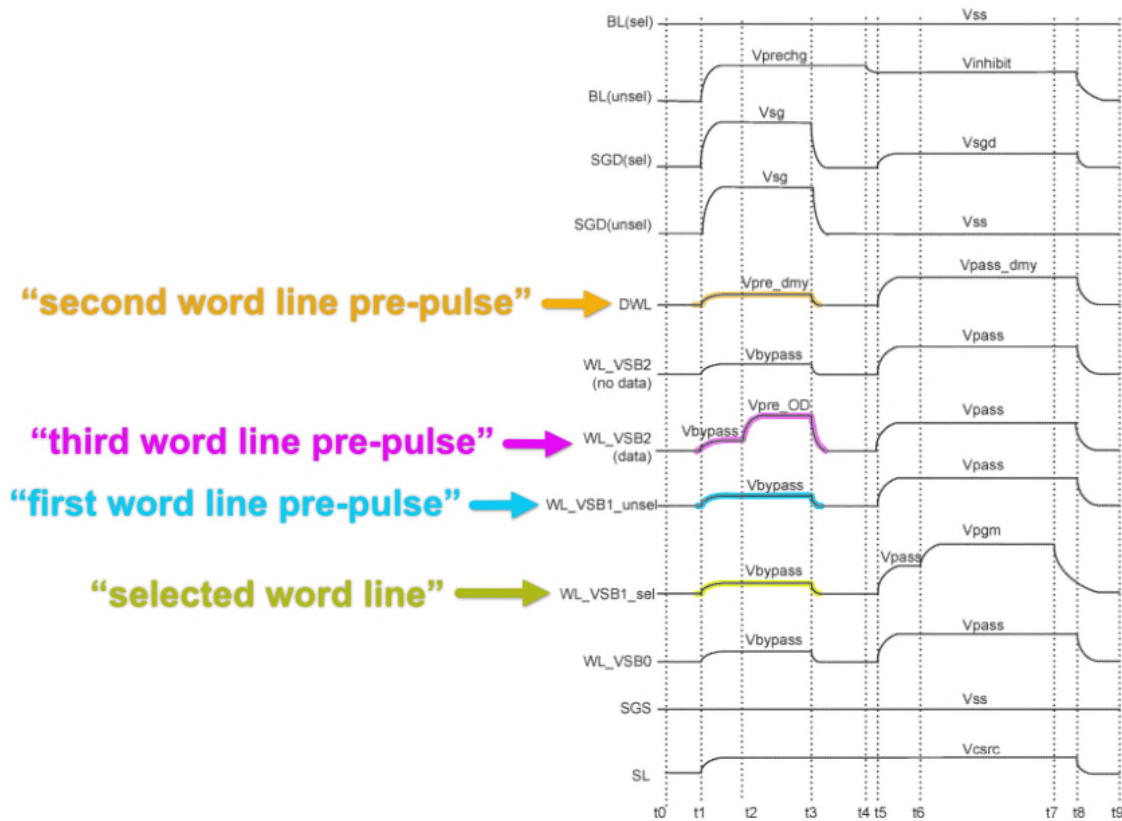


FIG. 8C

Yang, Fig. 8C.

FIG. 8B



Yang, Fig. 8B; *see also* Liu, ¶¶ 446-454.

[1.E.4]/[11.E.4] “wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal”

While Yang does not provide numerical examples for all of its different pre-charge voltages, a POSITA would nonetheless have understood Yang to render what this limitation requires obvious. Again, Yang applies three different voltage pulses to its various word lines during a pre-charge period: a “*first ... pre-pulse signal*” (Vbypass), a “*second ... pre-pulse signal*” (Vpre_dmy), and a “*third ... pre-pulse signal*” (Vpre_OD). *See supra* discussion of limits [1.E.1]-[1.E.3]. Yang explains

that “overdrive voltage Vpre_OD” is a high voltage “above all the data states” of the memory cells. Yang, 20:53-55. The “bypass voltage” Vbypass can be a low voltage: it can be lower than all the various memory cell read states and is only required to be higher than Vev (the “voltage level to test whether a memory cell has been properly erased”). *Id.*, 19:23-44; 20:64-21:5. The “dummy pre-charge voltage” Vpre_dmy can be an intermediate voltage like 5V that is lower than Vpre_OD. *Id.*, 24:18-27; Fig. 6; *see also* Liu, ¶¶ 455-460.

2. Claims 2 and 12

Claim 2 depends on claim 1. Claim 12 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines”

This is taught by Yang. As shown in Figure 8C below, Yang’s “*first group*” (WL8-WL11, blue), “*second group*” (DWL2, orange), and “*third group*” (WL12-WL14, purple) of “*word lines*” are “*disposed in an order distance*” from the “*selected word line*” (WL7, yellow):

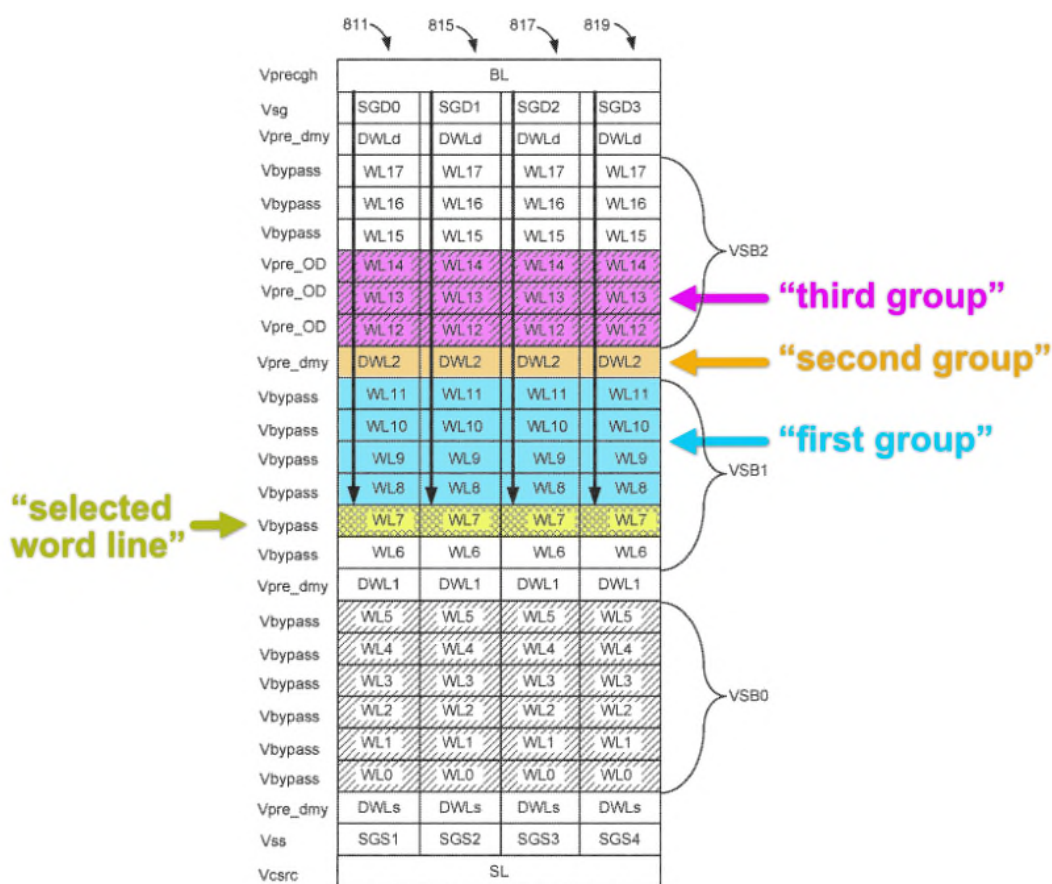


FIG. 8C

Yang, Fig. 8C; *see also* Liu, ¶¶ 461-463.

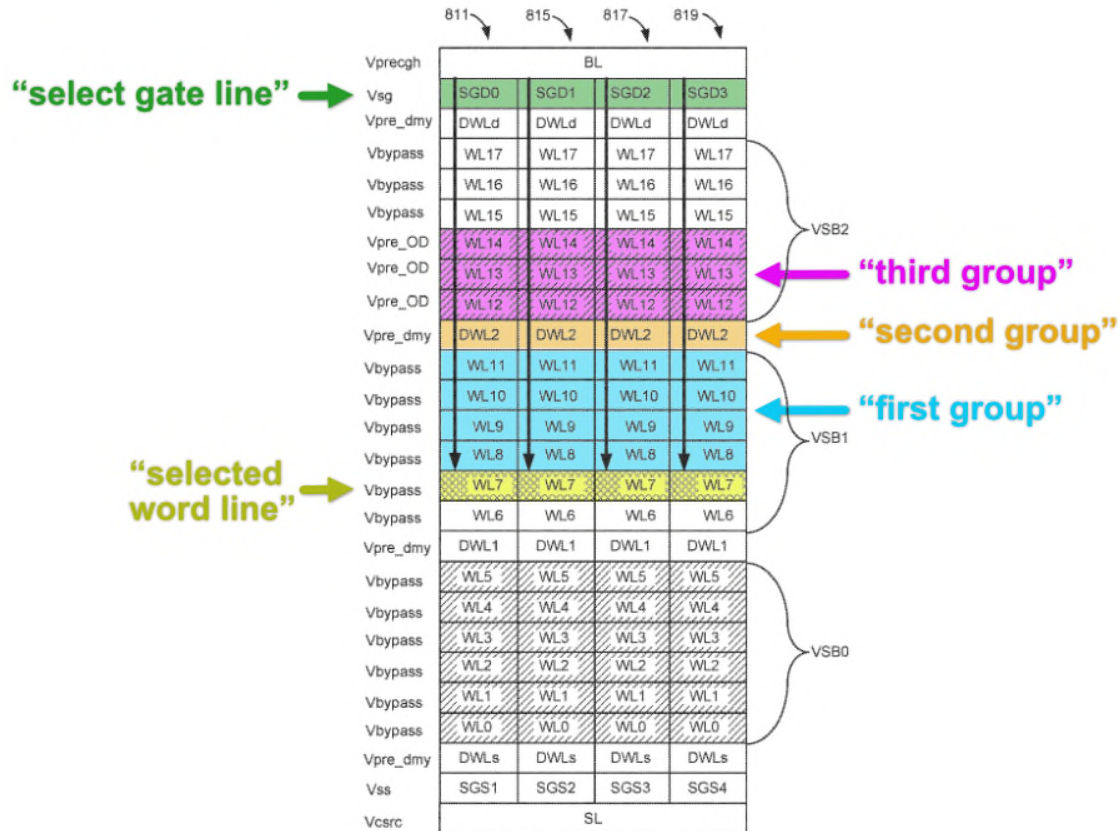
3. Claims 3 and 13

Claim 3 depends on claim 1. Claim 13 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line”

This is also taught by Yang. As shown in Figure 8C below, Yang’s “*first group*” (WL8-WL11, blue), “*second group*” (DWL2, orange), and “*third group*”

(WL12-WL14, purple) of “*word lines*” are “*disposed adjacent to*” the “*selected word line*” (WL7, yellow) and between this word line and the “*select gate line*” (SGD0-SGD3, green) in the manner this claim requires:



Yang, Fig. 8C; *see also* Liu, ¶¶ 464-466.

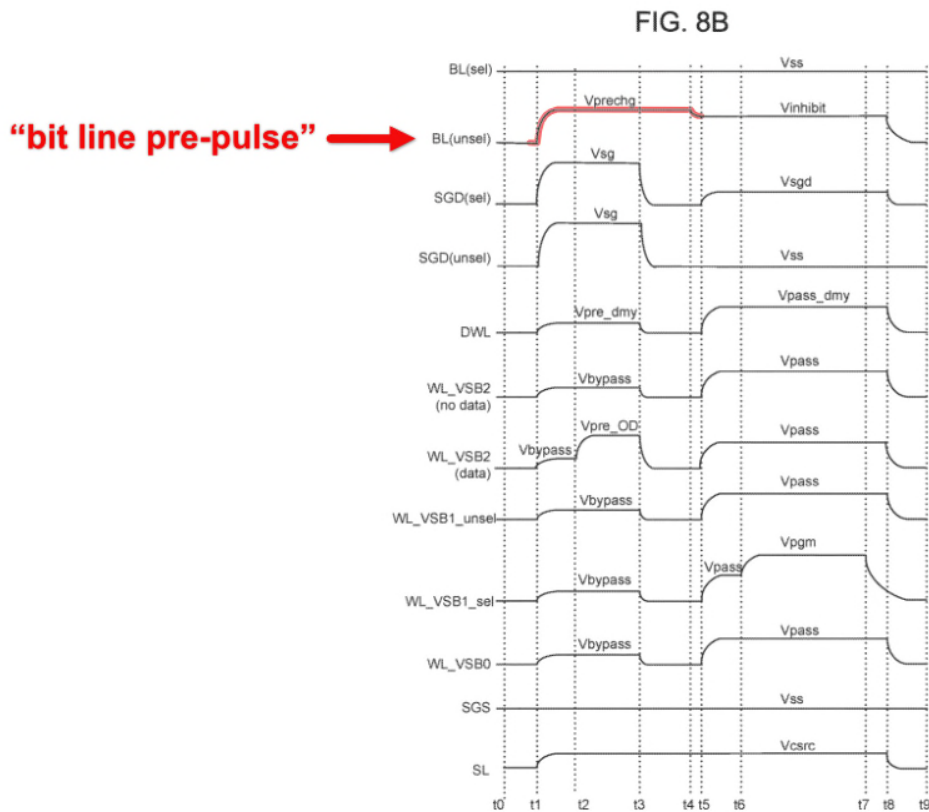
4. Claims 4 and 14

Claim 4 depends on claim 1. Claim 14 depends on claim 11. Both claims similarly require:

that “the control circuit is configured to apply” (claim 4) or “applying” (claim 14) “a bit line pre-pulse signal to the bit line during the pre-charge period”

Yang’s “*control circuit*” applies the claimed “*bit line pre-pulse signal*”

“during the pre-charge period.” According to Yang, “during a pre-charge phase of a programming operation[,]” its controller applies “a pre-charge voltage” “to a bit line (BL) connected to an unselected NAND string.” Yang, 9:65-10:5; *see also id.*, 21:61-64 (a “pre-charge voltage is applied to a bit line connected to a drain side select transistor at one end of the unselected NAND string”); 23:37-44 (during the pre-charge period “the voltage on the unselected bit line (BL(unsel)) is raised towards the pre-charge voltage (Vprechg).” This is shown in Figure 8B:



Id., Fig. 8B; *see also* Liu, ¶¶ 467-471.

5. Claims 5 and 15

Claim 5 depends on claim 4. Claim 15 depends on claim 14. Both claims

further require that:

“the first memory string is an unselected memory string, and the bit line is an unselected bit line”

Yang explains that during its “pre-charge phase[,]” “channels of unselected NAND strings ... are pre-charged to a desired voltage level.” Yang, 21:46-50. As part of this, pre-charge voltages are applied to the “unselected bit line[s.]” *Id.*, 23:37-44; *see also* Liu, ¶¶ 472-475.

6. Claim 6

Claim 6 depends on claim 1 and further requires that:

“the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines”

This is taught by Yang for the same reasons explained in connection with limitation [11.E.0]: the “bypass voltage” (V_{bypass}) is applied to the selected word line during pre-charging. Yang, 22:31-37, 24:11-17; Figs 8B-C; *see also supra* discussion of limit [11.E.0]; Liu, ¶¶ 476-477.

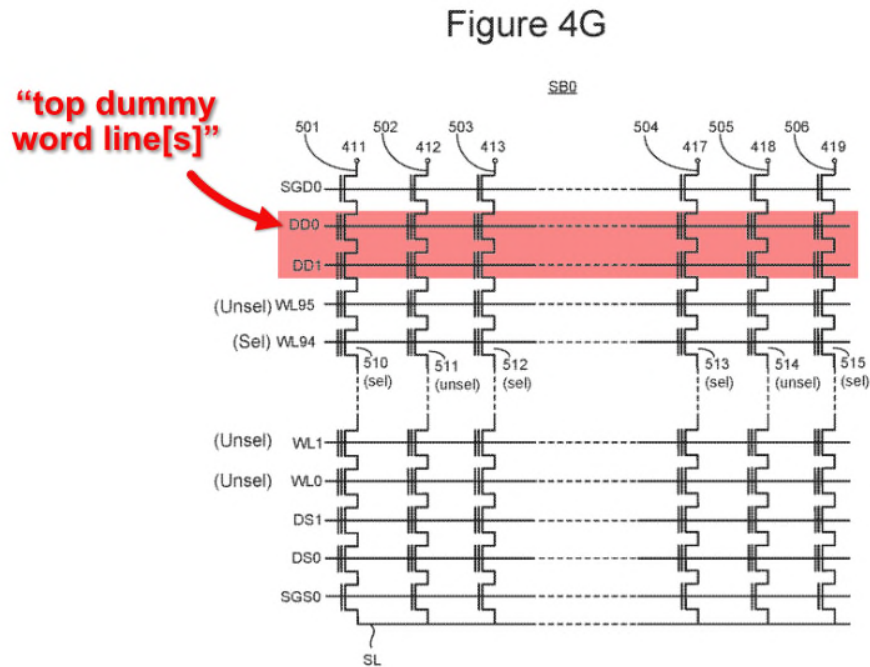
7. Claims 7 and 16

Claim 7 depends on claim 1. Claim 16 depends on claim 11. Both claims similarly require that:

“[the control circuit is configured to] apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the pre-charge period”

Yang’s memory structure includes *“a top dummy word line.”* Per Yang, its memory includes multiple “dummy word lines.” Yang, 8:67-9:2. These includes

“drain side dummy word line layers” that are located “[b]elow the SGD layers.” *Id.*, 13:8-9. Example dummy word line layers DD0-DD1 are annotated red in Figure 4G below:



Id., Fig. 4G; *see also id.*, Fig. 8C (similarly showing a top dummy word line layer DWLd).

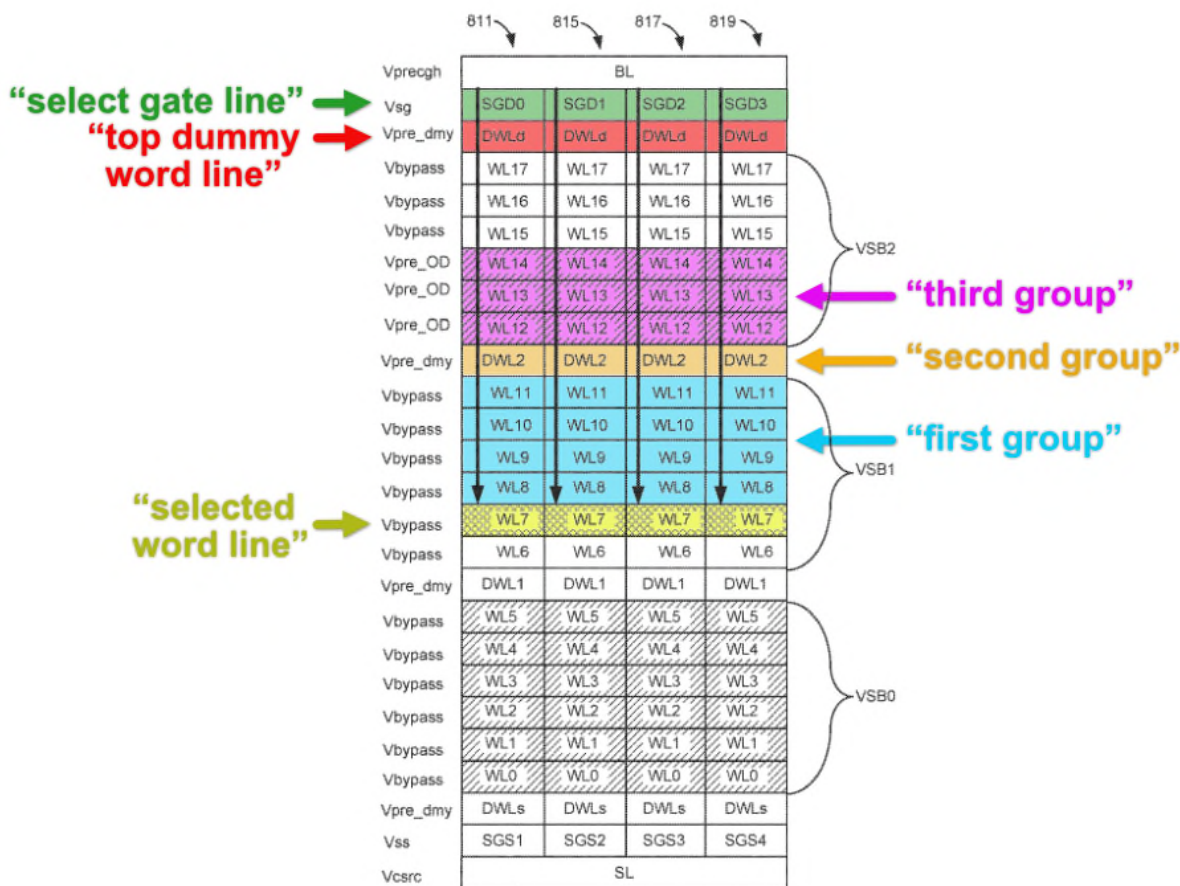
Yang also teaches application of a “*a top dummy word line pre-pulse*” to its dummy word lines during the “*pre-charge period.*” In particular, a “dummy pre-charge voltage” (V_{pre_dmy}) is “applied to all dummy word lines” during pre-charge period t_1 - t_3 . Yang, 24:18-27; Fig. 8B-C; *see also* Liu, ¶¶ 478-484.

8. Claim 18

Claim 18 depends on claim 16 and further requires that:

“the top dummy word line is disposed between the third group of the plurality of word lines and the select gate line”

As shown in Figure 8C below, Yang’s **“top dummy word line”** (DWLd, red) is **“between”** its **“third group of ... word lines”** (WL12-WL14, purple) and the **“select gate line”** (SGD0-SGD3):



Yang, Fig. 8C; *see also* Liu, ¶¶ 485-487.

9. Claims 9 and 19

Claim 9 depends on claim 1. Claim 19 depends on claim 11. Both claims further require that:

“the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third word line pre-pulse signal are positive”

All of the pre-pulse voltages employed by Yang are positive. *See, e.g.,* Yang, Fig. 8B; *see also* Liu, ¶¶ 488-490.

E. Secondary Considerations

There is no evidence in the '822 patent's prosecution history of any pertinent secondary considerations of nonobviousness.

X. Conclusion

For the foregoing reasons, Petitioner respectfully requests institution of IPR and cancellation of claims 1-9 and 11-19.

Petition for *Inter Partes* Review of U.S. Patent No. 11,501,822

Respectfully submitted,

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Dated: April 11, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,930 words.

Dated: April 11, 2024

By: /s/ K. Patrick Herman

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on April 11, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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