

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00795
U.S. Patent No. 11,501,822
Issue Date: November 15, 2022

Title: NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD

DECLARATION OF DAVID KUAN-YU LIU, PH.D.

TABLE OF CONTENTS

I. INTRODUCTION	5
II. BACKGROUND AND EXPERT QUALIFICATIONS.....	5
III. ASSIGNMENT AND MATERIALS CONSIDERED	8
IV. UNDERSTANDING OF THE LAW	9
V. LEVEL OF SKILL IN THE ART	13
VI. TECHNOLOGY BACKGROUND.....	15
VII. THE '822 PATENT.....	22
A. Effective Filing Date	22
B. Overview	23
C. Prosecution History	26
D. Claims.....	27
VIII. CLAIM CONSTRUCTION	33
IX. UNPATENTABILITY ANALYSIS	34
A. Overview of the Prior Art.....	34
1. Lee.....	34
2. Zhao.....	36
3. Yang	40
B. <i>Ground 1</i> : Claims 1-3, 6, and 11-13 Are Obvious Over Lee.....	43
1. Independent Claims 1 and 11.....	44
2. Claims 2 and 12.....	62
3. Claims 3 and 13.....	63
4. Claim 6.....	65

Petition for *Inter Partes* Review of U.S. Patent No. 11,501,822
Declaration of David Kuan-Yu Liu, Ph.D.

C.	<i>Ground 2: Claims 1, 4-7, 9, 11, 14-16, and 18-19 Are Obvious Over Zhao</i>	66
1.	Independent Claims 1 and 11.....	66
2.	Claims 4 and 14.....	79
3.	Claims 5 and 15.....	80
4.	Claim 6.....	81
5.	Claims 7 and 16.....	82
6.	Claim 18.....	84
7.	Claims 9 and 19.....	85
D.	<i>Ground 3: Claims 1-9 and 11-19 Are Obvious Over Zhao when Modified in View of Lee</i>	86
1.	Claims 1, 4-7, 9, 11, 14-16, and 18-19	86
2.	Claims 2 and 12.....	97
3.	Claims 3 and 13.....	98
4.	Claims 8 and 17.....	99
E.	<i>Ground 4: Claims 1-7, 9, 11-17, and 18-19 Are Obvious Over Yang</i>	101
1.	Independent Claims 1 and 11.....	102
2.	Claims 2 and 12.....	115
3.	Claims 3 and 13.....	116
4.	Claims 4 and 14.....	118
5.	Claims 5 and 15.....	119
6.	Claim 6.....	120
7.	Claims 7 and 16.....	120

Petition for *Inter Partes* Review of U.S. Patent No. 11,501,822
Declaration of David Kuan-Yu Liu, Ph.D.

8.	Claim 18.....	121
9.	Claims 9 and 19.....	123
F.	Secondary Considerations of Non-Obviousness.....	123

I, David Kuan-Yu Liu, Ph.D. declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in the claims of U.S. Patent No. 11,501,822, which I refer to herein as the ’822 patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$550 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My curriculum vitae (“CV”) is attached hereto as Ex. 1017 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

6. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D.

degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

7. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

8. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating a novel source-side injection mechanism for flash EPROM channel hot-electron programming. A source-side injection mechanism is one particular form of a hot carrier injection (HCI) mechanism.

9. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing flash cell and periphery devices in AMD's CMOS-based 0.5 μm and 0.35 μm flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology to accommodate x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

10. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices. This included various different types of memory, including NAND flash memory and embedded flash memory.

11. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

12. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75 nm CMOS technology node, a half node version between 90 nm and 65 nm).

13. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing embedded non-volatile memory process technology for power management product applications.

14. Since 2007, I have served as a technical consultant where I have provided expert advice regarding flash memory technology, CMOS process technology, and semiconductor device physics. As part of this, I have considered,

assessed, and assisted with the design of various different memory devices, including NAND flash and monolithic 3D memory structures.

III. ASSIGNMENT AND MATERIALS CONSIDERED

15. I have been asked to provide analysis and explain the subject matter of the '822 patent, including the state of the art when the application underlying the '822 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '822 patent including how that art relates to the challenged claims of the '822 patent and to provide my opinions regarding whether that art invalidates the claimed subject matter.

16. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the claims of the '822 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any applicable rule.

17. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '822 patent.

18. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and

Petition for *Inter Partes* Review of U.S. Patent No. 11,501,822
Declaration of David Kuan-Yu Liu, Ph.D.

considered the '822 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1004	U.S. Patent No. 10,121,529 B2 to Lee
1005	U.S. Patent No. 10,643,718 B2 to Zhao et al.
1006	Aritome, “NAND Flash Memory Technologies” (2016)
1007	Brown et al., “Nonvolatile Semiconductor Memory Technology” (1998)
1008	Cappelletti, et al., “Flash Memories” (1999)
1009	U.S. Patent No. 9,589,978 to Yip
1010	U.S. Patent No. 10,726,920 B2 to Yang
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1015	File History of U.S. Patent No. 11,081,164 (Appl 16-709,944) to Jia et al.
1016	File History of U.S. Patent No. 11,862,230 (Appl 17-965,527) to Jia et al.

IV. UNDERSTANDING OF THE LAW

19. I am not an attorney, but have been instructed in and applied the law as described in this section.

20. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary

skill in the art (POSITA) would have understood the claims of the alleged invention in Section V below.

21. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

22. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

23. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to

ascertain whether the disclosures in those references render the combination obvious to such a person.

24. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

25. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

26. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

27. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

28. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

29. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

30. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

31. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but

unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

32. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention.

33. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

34. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

35. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

36. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of

the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

37. In my opinion, a POSITA in the field of the '822 patent would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

38. In my opinion, this POSITA would have been aware of and generally knowledgeable about NAND memory's structure, its component parts, how it operates, and how it is controlled.

39. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile NAND flash memory—I was a person of more than the ordinary level of skill in the art as of October 2019. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGY BACKGROUND

40. This section provides technology background to the '822 patent.

41. The '822 patent and the prior art discussed in this petition relate generally to NAND flash memory.

42. “Flash memory” represents an example of “non-volatile memory.” Ex. 1009, 1:24-26.

43. “Non-volatile memory is memory that can retain its data values for some extended period without the application of power.” *Id.*, 1:26-28.

44. NAND flash has been known and in use for quite some time, having been first developed in 1987. *See* Ex. 1006, 22.

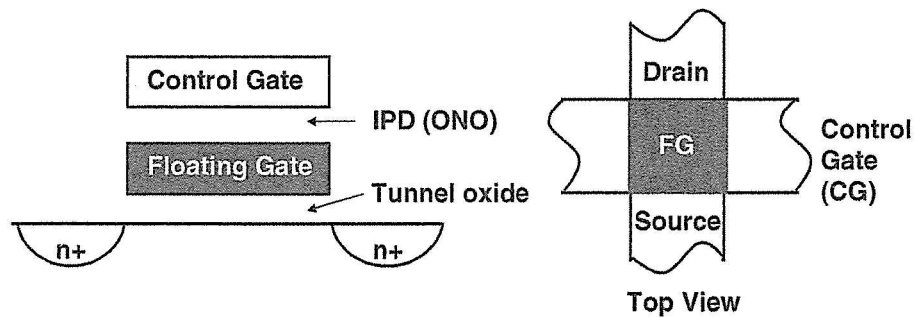
45. Like all semiconductor memory, NAND flash includes memory “cells.” In NAND flash, data is stored in a “cell” formed from a single transistor that is the logical equivalent of what a POSITA would have understood to be a “NOT AND” circuit. Ex. 1006, 38-39. This is why this type of memory is referred to as “NAND.”

46. A NAND memory cell can be formed from a “Nch MOS transistor with [a] poly-silicon floating gate (FG).” Ex. 1006, 38-39. “Charge is stored in [the] FG” and the “potential of [the] FG is controlled by a control gate (CG) voltage with capacitive coupling between [the] CG and FG.” *Id.*

47. The presence and the amount of the charge on the floating gate of this type of cell will determine how well the memory cell transistor conducts current

under a given control gate voltage. For an Nch memory cell, the more electrons that are stored on the floating gate, the higher the control gate voltage will need to be to turn on the transistor. This control gate voltage that turns on the transistor is known as the threshold voltage.

48. The below figure provides an example of one type of flash memory cell:



Ex. 1006, 39.

49. Other NAND flash employs a transistor with a “charge trap.” *See* Ex. 1012, 109.

50. In this type of transistor, charge is stored in “non-conducting dielectric layer”—like silicon nitride—instead of a floating gate. *See* Ex. 1012, 109.

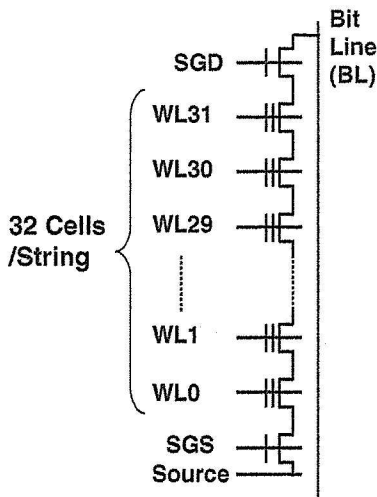
51. NAND flash memory cells are arranged in “strings” with multiple cells “connected in series.” Ex. 1006, 38.

52. The cells are surrounded by “two select transistors (SGD, SGS).” Ex. 1006, 38. The “SGD connects” at the string’s drain side “to isolate it from the bit

line (BL),” and the “SGS connects at” the string’s source side “to isolate it from a source line (SL).” *Id.*

53. Word lines are connected to the control gate of each memory cell. Ex. 1006, 38-39.

54. An example of one NAND memory string with memory cells arranged in series along the string is shown below:

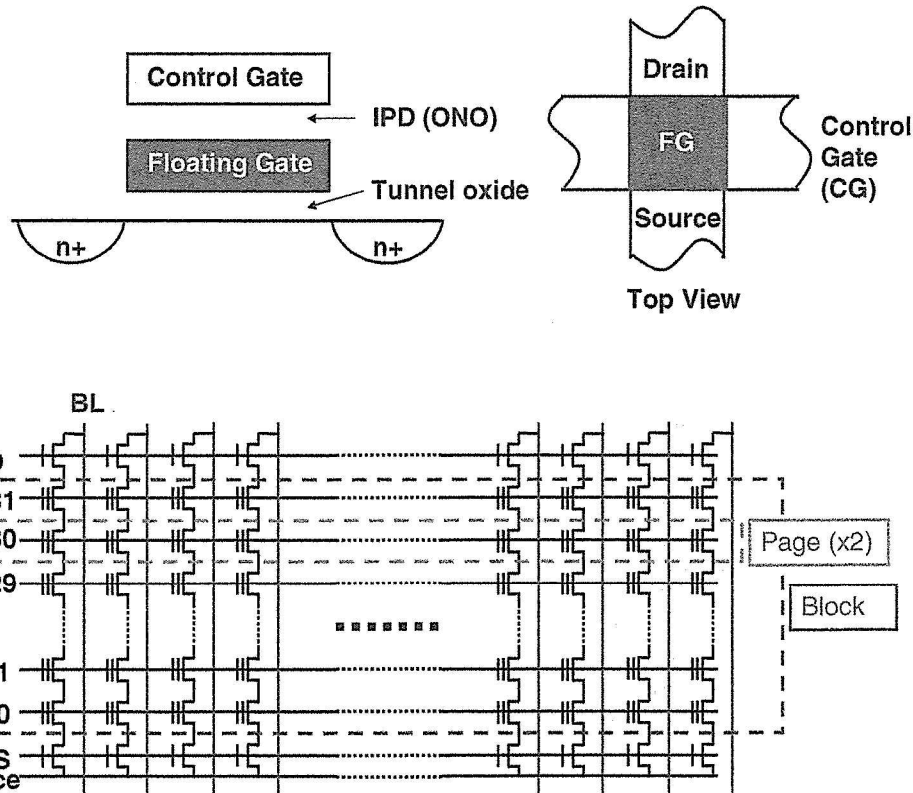


Ex. 1006, 39.

55. Early NAND flash devices were formed as two-dimensional arrays on a substrate surface.

56. Here, the “memory array is formed by straight active area lines ... and straight gate lines” located on a substrate surface. Ex. 1006, 38. Memory cells are located at the “intersection[s]” of the lines. *Id.*

57. An example of this is shown below, with an example memory cell again shown in the top figure, and a two dimensional array of such cells shown in the figure below:



Ex. 1006, 40.

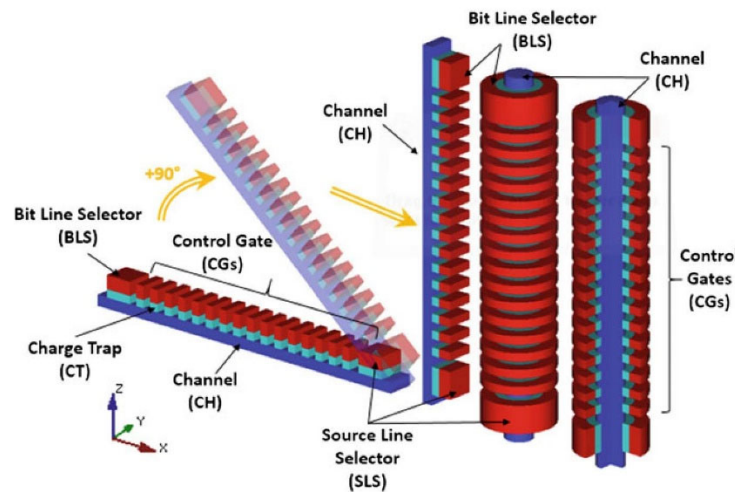
58. As also shown, the cells are grouped into “page[s]” extending along the word lines and “block[s].” Ex. 1006, 40. “[R]ead and program operations are performed per page” while “the erase operation is performed per block.” *Id.*, 39.

59. “In order to further scale down the memory cell size of NAND flash memory,” the art developed so-called “three-dimensional (3D) NAND flash cells” starting in about 2006. Ex. 1006, 292.

60. In 3D NAND, rather than arranging memory cells in a two-dimensional array, 3D NAND arranges cells in a three-dimensional array that is built up in layers.

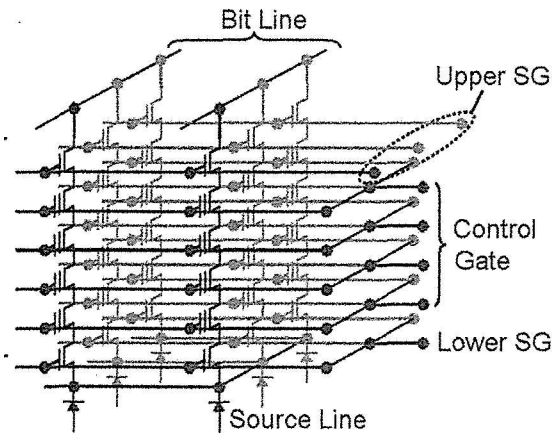
61. A POSITA would have known that “[c]onceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1011, 3.

62. The following image provides a demonstrative example of the relationship between the structure of a 2D NAND string and a 3D NAND string:



Ex. 1012, 122.

63. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1006, 296.

64. “Production of 3D NAND flash memory ... started in August 2013.”

Ex. 1006, 393.

65. To program a particular NAND memory cell in a memory string, a “high-voltage V_{pgm} ” is applied to the word line connected to the cell, which is often referred to as the “selected” word line, while “keeping” the string’s bit line at “0V.”

Ex. 1006, 44. The other unselected cells in this selected memory string will have a passing voltage, V_{pass} , lower in value than the programming voltage V_{pgm} , being applied to their word lines to allow the 0V to be passed to the channel of the selected memory cell. Application of this program voltage causes electron movement into the cell and raises the cell’s threshold voltage to a value within a specific range (or one of several different specific ranges) for purposes of storing data. *Id.*, 45.

66. Because the selected word line to which this program voltage is applied also passes through cells in many other strings, an “inhibit” voltage is applied to these strings’ bit lines to prevent undesired programming. Ex. 1006, 46.

67. As mentioned earlier, a lower “ V_{pass} ” voltage is also applied to all unselected word lines (Ex. 1006, 44-46) to pass the 0V from the bit line to facilitate the programming of the selected cell.

68. Due to the close proximity of memory cells, along with the application of these various different voltages during the programming operation, NAND is subject to a well-known “phenomenon” referred to as “[p]rogram disturb.” Ex. 1006, 52.

69. “Program disturb” involves “the threshold voltage ... of unselected cells” undesirably “increas[ing] during program operation.” Ex. 1006, 52-53. This is problematic, as cells not identified for programming modification may nonetheless enter a different/unintended programmed state due to the voltages applied to the other, adjacent lines. *Id.*

70. “Program disturb” can occur both in the NAND string that includes the programmed cell and in adjacent strings. Ex. 1006, 52-53.

71. It was known that applied voltages can be tailored to either avoid or minimize program disturb. Ex. 1006, 52-53.

72. For instance, increasing the V_{pass} voltage applied to unselected word lines increases the so-called “boosting” voltage in adjacent NAND strings—a voltage that is induced in part by word line voltage—thereby reducing program disturb in those strings. Ex. 1006, 52-53. But this also has the effect of increasing program disturb in the string that includes the programmed cell. *Id.*

73. A lower V_{pass} has the opposite effect, reducing program disturb in the string that includes the programmed cell, but increasing it in adjacent strings. Ex. 1006, 52-53.

VII. THE '822 PATENT

A. Effective Filing Date

74. I understand that the application leading to the '822 patent was filed on June 21, 2021.

75. Based on my review of the '822 patent, I note that it also references a PCT application on its face, which was filed October 22, 2019.

76. For purposes of this declaration, I have been instructed to use October 22, 2019 as the effective filing date of the '822 patent. My opinions in this declaration were formed from the perspective of a POSITA as of October 22, 2019, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

B. Overview

77. The '822 patent relates to a “non-volatile memory device”—such as a “three-dimensional (3D) NAND flash memory”—and an associated “control method....” Ex. 1001, 1:15-19.

78. The patent explains that typical “3D NAND memory architecture stacks memory cells vertically in multiple layers, achieving a higher density....” Ex. 1001, 1:29-32.

79. “As more layers are added, the bit density increases, thus increasing ... storage capacity.” Ex. 1001, 1:32-33. But “[w]ith the layer increases, ... program disturb becomes worse.” *Id.*, 1:34-35.

80. One way to address this, according to the patent, is to apply “[a] pre-pulse signal ... to an unselected bit line....” Ex. 1001, 1:34-37. The patent notes that this, however, also presents issues as longer channels “reduce[]” “[t]he effect” of such a “bit line pre-charge.” *Id.*, 1:39-41.

81. The patent goes on to explain that “[a] traditional method for improving the bit line pre-charge effect is to extend the bit line pre-pulse time.” Ex. 1001, 1:41-44. But according to the patent, this results in slower programming. *Id.*

82. Another “traditional method” identified in the patent entails “increas[ing] the voltage level of the bit line pre-pulse.” Ex. 1001, 1:44-48. This “increase[s] the risk of the breakdown” of the “bit line transistor.” *Id.*

83. In an effort to address these identified problems, the '822 patent “appl[ies] word line pre-pulse signals with different voltage levels” for purposes of “reducing programming disturb.” Ex. 1001, 1:17-19. The further a word line is “away from the selected word line, the larger voltage level of the” applied “word line pre-pulse signal[.]” *Id.*, 4:39-43.

84. According to the patent, this “enhance[s]” “the channel potential gradient” in the unselected NAND strings, which in turn “enhance[es] the pre-charge effect” and “reduc[es] programming disturb.” Ex. 1001, 4:54-59.

85. Figures 3 and 4, both of which are reproduced below in annotated form with color added, provide an example.

86. Figure 3 shows a single “memory string.” Ex. 1001, 5:7-11.

87. Connection of the “memory string” to an “unselected bit line BL” is controlled by a “top select gate line TSG” (green). Ex. 1001, 5:11-15.

88. “[W]ord lines WL0 to WLn” pass through the memory string. Ex. 1001, 5:14-16.

89. One of these—“WL0” (yellow)—is “the selected word line” the figure’s example. Ex. 1001, 5:18-20.

90. The remaining word lines are divided into a “first group” (blue “Bottom WL”), “second group” (orange “Middle WL”), and “third group” (purple “Top WL”). Ex. 1001, 5:19-34.

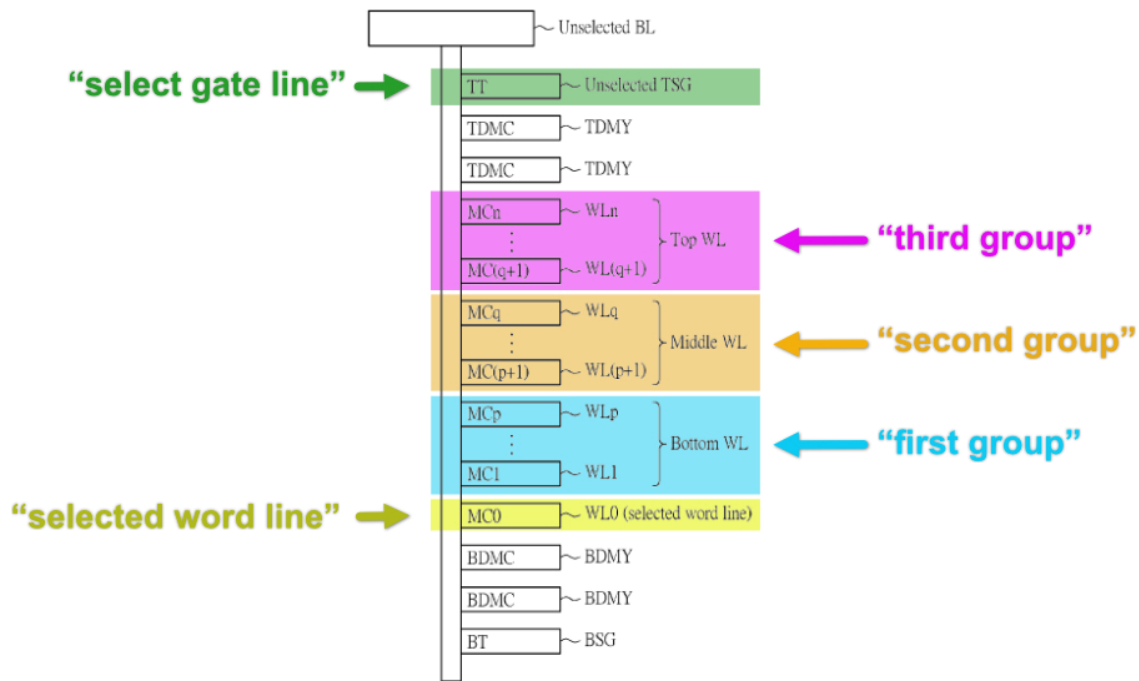


FIG. 3

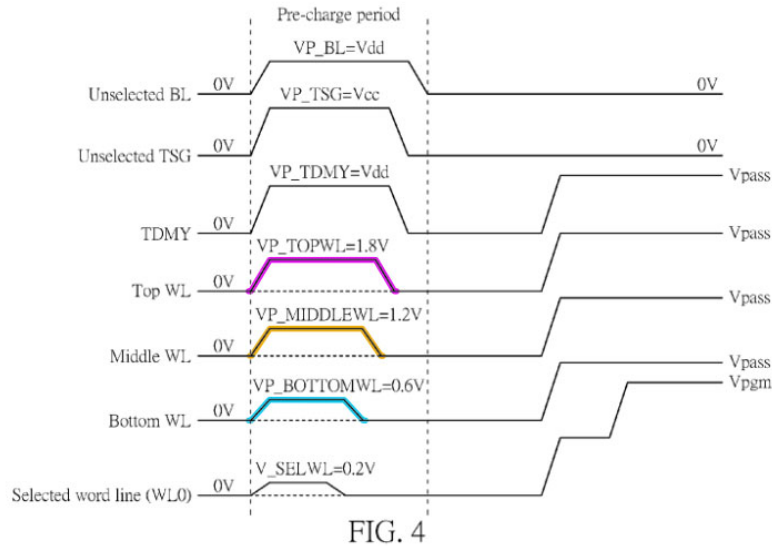
Ex. 1001, Fig. 3.

91. Figure 4 is a “signal timing diagram of” Figure 3’s “memory string[.]”

Ex. 1001, 5:35-38.

92. The '822 patent explains that to improve the potential in the string's channel and reduce program disturb, three different “word line pre-pulse signals”—labeled VP_BOTTOMWL (blue), VP_MIDDLEWL (orange), and VP_TOPWL (purple)—are applied to the three groups of word lines. Ex. 1001, 5:50-55.

93. The voltage level of these signals increases with distance from the “selected word line”:



Ex. 1001, Fig. 4.

C. Prosecution History

94. As noted above, I have reviewed the '822 patent's prosecution history.

95. The Examiner rejected the '822 patent only on double patenting grounds. *See generally* Ex. 1002.

96. I have also reviewed the '822 patent's parent application (U.S. App. 16/709,944, Ex. 1015.)

97. The claims in this parent application were rejected by the Examiner over U.S. Patent No. 10,283,202 ("Chen") and U.S. Pub. 2011/0194351 ("Kim). *See* Ex. 1015, pp. 79-87.

98. The parent application's broader claims, in contrast to those of the '822 patent, required only a "plurality of word line pre-pulse signals" at the time of the

rejection. The broadest claims did not yet mention a “first,” “second,” and “third” signal. Ex. 1015, p. 35.

99. Because of this, the Examiner based the rejection on Chen’s teaching of two different word line pre-pulse voltages (0 or 2V). Ex. 1015, p. 83-84.

100. Kim similarly applied two different pre-pulse voltages (V2 or V3) to various word lines. Ex. 1015, p. 85.

101. Applicant responded to these rejections by amending the claims to require (1) “first,” “second,” and “third,” “pre-pulse signal” voltages, (2) that “first,” “second[,]” and “third” groups of word lines be arranged in order between the “selected word line and the select gate line[,]” and (3) that the “voltage level” of the “pre-pulse signal” increase from the “first” to the “second” and then to the “third” “group[.]” Ex. 1015, pp. 115-116.

102. This resulted in allowance of the claims. *See* Ex. 1015, pp. 131-134.

D. Claims

103. For reference, claims 1-9 and 11-19 of the ’822 patent are reproduced below:

1. A memory device, comprising:
 - a plurality of memory strings;
 - a bit line connected to a first memory string of the plurality of memory strings;

a select gate line connected to the first memory string
of the plurality of memory strings;

a selected word line of a plurality of word lines,
wherein the plurality of word lines is connected to
the first memory string; and

a control circuit configured to:

apply a first word line pre-pulse signal of a plurality
of word line pre-pulse signals to a first group of
the plurality of word lines during a pre-charge
period;

apply a second word line pre-pulse signal of the
plurality of word line pre-pulse signals to a
second group of the plurality of word lines
during the pre-charge period; and

apply a third word line pre-pulse signal of the
plurality of word lines pre-pulse signals to a third
group of the plurality of word lines during the
pre-charge period,

wherein a voltage level of the second word line pre-
pulse signal is greater than that of the first word
line pre-pulse signal, and a voltage level of the
third word line pre-pulse signal is greater than
that of the second word line pre-pulse signal.

2. The memory device of claim 1, wherein the first
group of the plurality of word lines, the second group of

the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines.

3. The memory device of claim 1, wherein the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.

4. The memory device of claim 1, wherein the control circuit is configured to apply a bit line pre-pulse signal to the bit line during the pre-charge period.

5. The memory device of claim 4, wherein the first memory string is an unselected memory string, and the bit line is an unselected bit line.

6. The memory device of claim 1, wherein the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines.

7. The memory device of claim 1, wherein the control circuit is configured to apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the pre-charge period.

8. The memory device of claim 7, wherein a voltage level of the top dummy word line pre-pulse signal is greater than that of the third word line pre-pulse signal.

9. The memory device of claim 1, wherein the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third word line pre-pulse signal are positive.

11. A method of controlling a memory device, the memory device comprising a plurality of memory strings, a bit line connected to a first memory string of the plurality of memory strings, a select gate line connected the first memory string of the plurality of memory strings, a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string, the method comprising:

applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period;

applying a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during the pre-charge period;

applying a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second

group of the plurality of word lines during the pre-charge period; and

applying a third word line pre-pulse signal of the plurality of word line pre-pulse signals to a third group of the plurality of word lines during the pre-charge period;

wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

12. The method of claim **11**, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines.

13. The method of claim **11**, wherein the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.

14. The method of claim **11**, further comprising applying a bit line pre-pulse signal to the bit line during the pre-charge period.

15. The method of claim **14**, wherein the first memory string is an unselected memory string, and the bit line is an unselected bit line.

16. The method of claim **11**, further comprising apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the pre-charge period.

17. The method of claim **16**, wherein a voltage level of the top dummy word line pre-pulse signal is greater than that of the third word line pre-pulse signal.

18. The method of claim **16**, wherein the top dummy word line is disposed between the third group of the plurality of word lines and the select gate line.

19. The method of claim **11**, wherein the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third word line pre-pulse signal are positive.

VIII. CLAIM CONSTRUCTION

104. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

105. I have been informed that the words of a claim are generally given the ordinary and customary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

106. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

107. In my opinion, the terms of the ’822 patent’s claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

IX. UNPATENTABILITY ANALYSIS

108. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '822 patent, a POSITA would have considered claims 1-9 and 11-19 of the '822 patent to be unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art

109. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

1. Lee

110. Lee states on its face that it issued November 6, 2018. *See* Ex. 1004, Cover. In view of this date of issuance, which is before the '822 patent's own October 22, 2019 effective filing date, I understand that Lee is prior art under 35 U.S.C. § 102(a)(1)

111. Lee describes a “semiconductor memory device”—with “a three-dimensional structure”—that “mitigate[s] a program disturb phenomenon.” Ex. 1004, 1:52-56, 7:23-24.

112. To facilitate this, Lee arranges its memory's “word lines” into “a plurality of word line groups.” Ex. 1004, 2:4-5.

113. Then, “different pre-bias voltages are applied” to the different groups of word lines during a “precharge” step “depending on the respective positions of the word lines.” Ex. 1004, 1:62-2:3. “[T]he closer a word line group ... is to a drain

select transistor in the memory cell array, the higher a pre-bias voltage to be applied to the word line may be.” Ex. 1004, 2:13-16.

114. According to Lee, the application of different pre-bias voltages to the different groups in this manner accounts for “the resistance component” along a memory string’s channel and allows “the precharge level in the channel” to be “uniformly formed.” Ex. 1004, 8:47-51. This in turn “mitigate[s]” the “program disturb phenomenon.” *Id.*, 8:51-52.

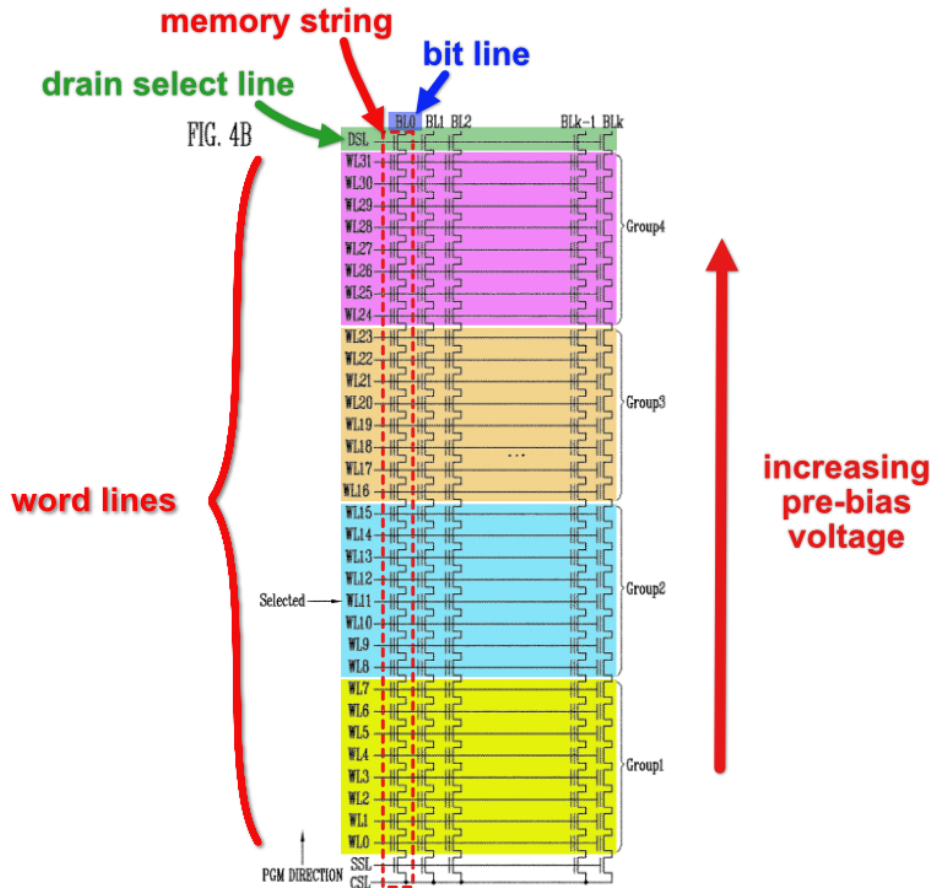
115. Lee also includes examples. In these examples, multiple vertical memory “strings” are connected to a lower “source select line SSL[,]” “word lines” WL0-WL31, and upper “drain select line DSL.” Ex. 1004, 7:37-43. Each string also connects to a “corresponding bit line.” *Id.*

116. In the more specific example shown in Figure 4B, the memory’s word lines WL0-WL31 are arranged, through the control logic, into “first to fourth word line groups Group1 to Group4....” Ex. 1004, 9:36-40.

117. The word lines are selected for programming one at a time beginning at “WL0” and moving “toward ... WL31.” Ex. 1004, 8:22-25.

118. And “the closer a group is to the drain select transistor, the higher” the “applied” “pre-bias voltage....” for the corresponding word lines. Ex. 1004, 9:41-55.

119. The below annotated version of Figure 4B (with color added for emphasis) shows these different word line groups and indicates the direction in which the pre-bias voltage increases:



Ex. 1004, Fig. 4B.

2. Zhao

120. Zhao shows that it was filed June 7, 2018. *See* Ex. 1005, Cover. This filing pre-dates the '822 patent's own October 22, 2019 filing date. In view of this, I understand that Zhao is prior art under 35 U.S.C. § 102(a)(2).

121. Zhao relates to a “memory system 100” that “implements” various “countermeasures for avoiding program disturb.” Ex. 1005, 4:7-10.

122. According to Zhao, this memory can be “a three dimensional memory array” with multiple vertical “NAND strings.” Ex. 1005, 6:34-44.

123. The “NAND strings”—like most typical NAND strings—are connected to lower source-side and upper drain-side “selection lines” multiple intervening dummy and data word lines, and “associated bit line(s).” *Id.*, 11:53-61; 12:6-13.

124. During programming, the word lines are selected one at a time in “order” from the source- to drain-side: “WL0, WL1, WL2, ... WL95.” Ex. 1005, 17:27-29.

125. Zhao explains that “[t]o assist in ... boosting” of its channels, its “control circuit” “pre-charge[s]” the “channels of ... NAND strings” before programming. Ex. 1005, 13:65-14:1, 14:35-40; 16:65-67.

126. Zhao also explains that different groups of word lines are supplied with different pre-charge voltages. Ex. 1005, Fig. 13.

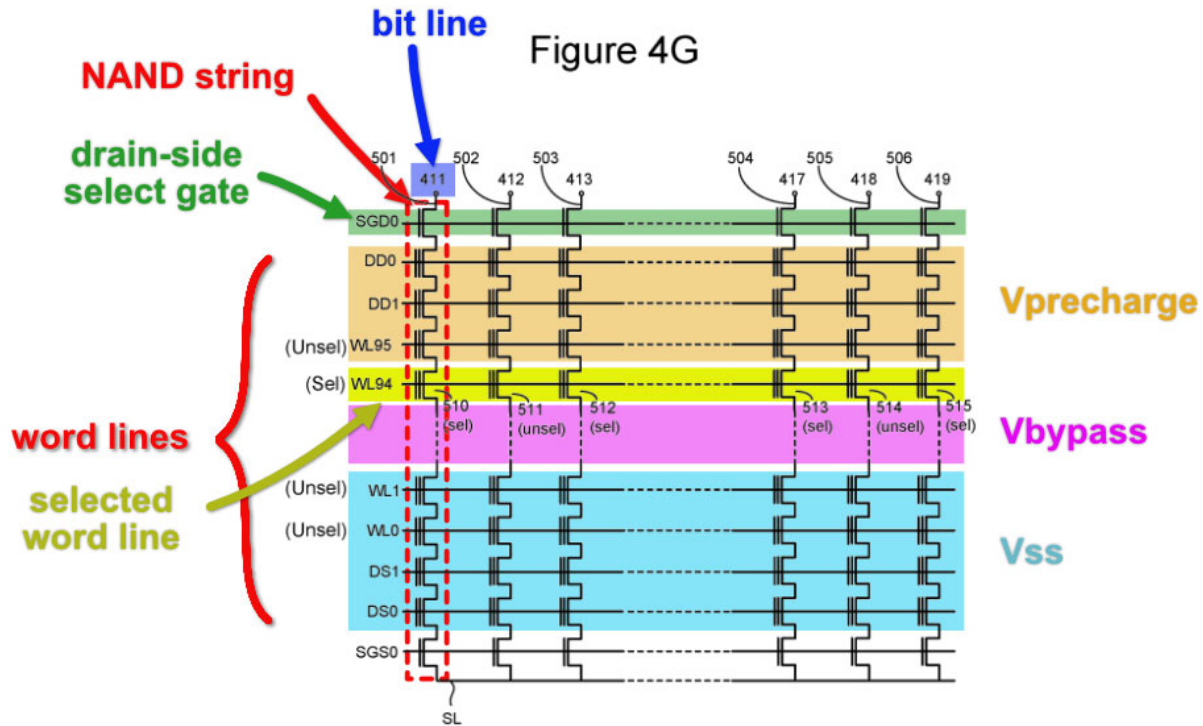
127. In particular, unprogrammed word lines on the “drain side” of the selected word line receive a “pre-charge” voltage $V_{precharge}$. Ex. 1005, 19:19-22; 19:57-58; 22:45-48.

128. Multiple “already programmed (e.g. source side) unselected word line[s] ... adjacent to the selected word line” are supplied with a higher “bypass voltage” V_{bypass} . Ex. 1005, 19:32-50; 22:50-53.

129. The remainder of the source-side word lines receive a “low” pre-charge voltage V_{ss} . Ex. 1005, 19:22-23; 23:7-9.

130. According to Zhao, applying these different pre-charge voltages to these different word line groups “equalizes the charge between the source side ... and the drain side of the channel” assisting in the avoidance of “program disturb.” Ex. 1005, 19:50-56; 22:65-23:5.

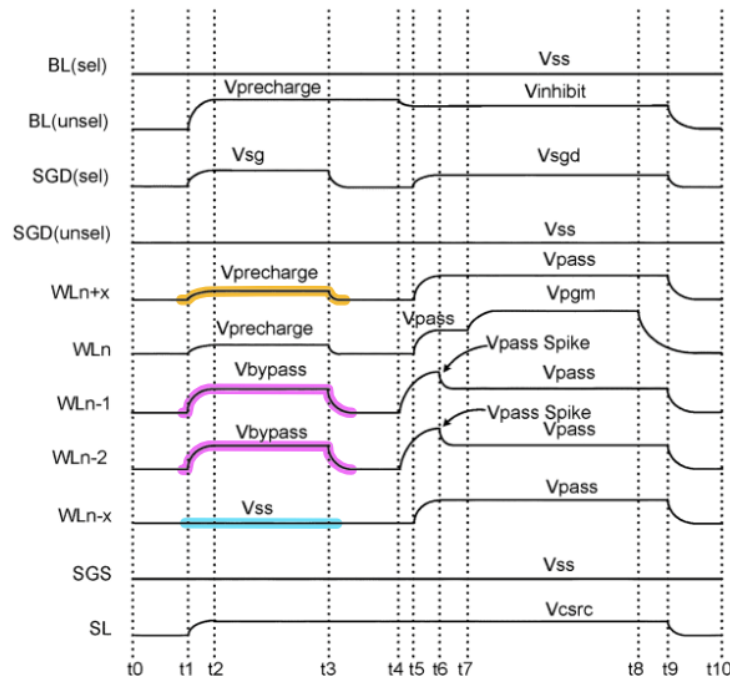
131. Figure 4G depicts one “sub-block” of memory. Ex. 1005, 12:6-7. An annotated version of this figure—again with color added for emphasis—is reproduced below. The general locations of the word line groups receiving Zhao’s different pre-charge voltages are shown by these colored annotations. The matching colored text to the right indicates the applied pre-charge voltages:



Ex. 1005, Fig. 4G.

132. Figure 13, reproduced and annotated below, is “a signal diagram” showing the signals applied to Zhao’s lines, including those applied to the different groups of word lines “during pre-charge” “time period” “t1-t3[.]” Ex. 1005, 22:18-20, 22:39-23:5.

Figure 13



Ex. 1005, Fig. 13.

3. Yang

133. Yang states that it was filed November 26, 2018. *See* Ex. 1010, Cover. This filing date pre-dates the '822 patent's October 22, 2019 filing date. In view of this, I understand that Yang is prior art under 35 U.S.C. § 102(a)(2).

134. Yang is also directed to a “three-dimensional memory array of non-volatile memory cells” arranged into “vertical NAND strings.” Ex. 1010, 5:4-14.

135. Yang's memory structure is similar to, and includes the same basic NAND components as, Zhao's memory. *See, e.g.*, Ex. 1010, Fig. 4G.

136. Yang, however, groups its word lines differently than Zhao and applies different pre-charge voltages to these different groups.

137. According to Yang, “[i]f the channel of [an] unselected NAND string is not adequately pre-charged during the pre-charge phase, the NAND channel may fail to boost to a sufficient voltage during the programming phase to adequately prevent program disturb.” Ex. 1010, 2:58-62.

138. Yang explains that a string may not be adequately protected from program disturb, presumably due to being inadequately pre-charged, if there is “valid data” from a previous programming step in memory cells. Ex. 1010, 3:20-27.

139. To avoid this problem, Yang applies a high “over-drive voltage” (V_{pre_OD}) during pre-charging to previously “programmed data word lines” located above a selected word line. Ex. 1010, 22:4-11; 24:28-33.

140. A lower “bypass voltage” (V_{bypass}) is applied to any “not programmed” word lines. Ex. 1010, 22:31-37, 24:11-17.

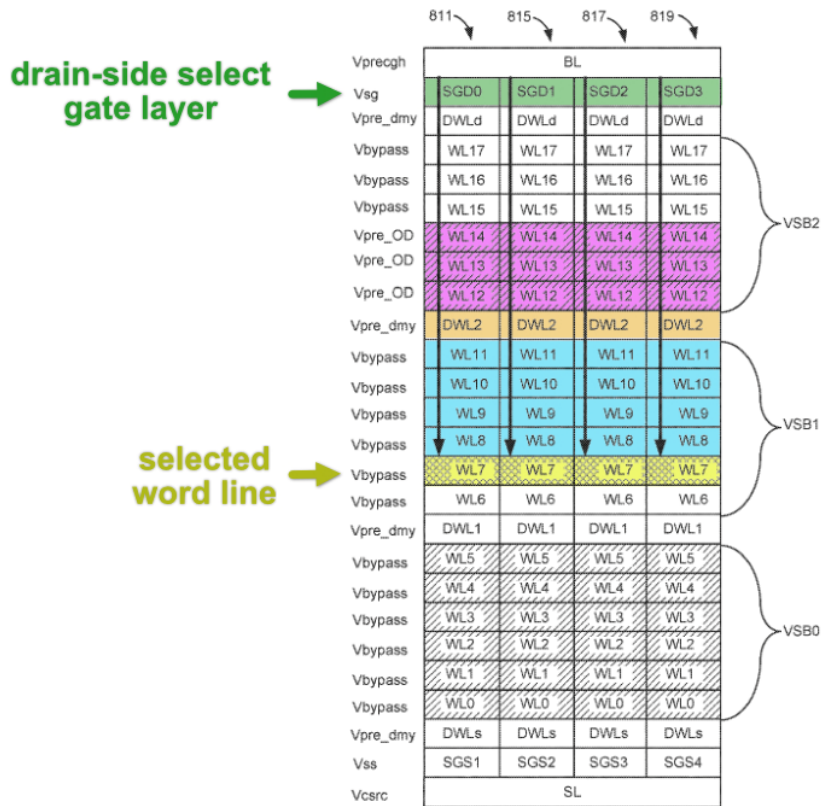
141. And a different “dummy pre-charge voltage” (V_{pre_dmy}) is “applied to all dummy word lines.” Ex. 1010, 24:18-27.

142. Figure 8C—which is reproduced in annotated form below with color added for emphasis—shows an example arrangement of word lines along with the different applied pre-charge voltages. *See* Ex. 1010, 25:29-33.

143. In the figure, WL7 is currently “selected.” Ex. 1010, 25:18-19. WL8-WL11 do not include data (so are supplied with V_{bypass}), while WL12-WL14 were

previously “programmed” (and are thus supplied with Vpre_OD). *Id.*, 22:4-11; 24:28-33.

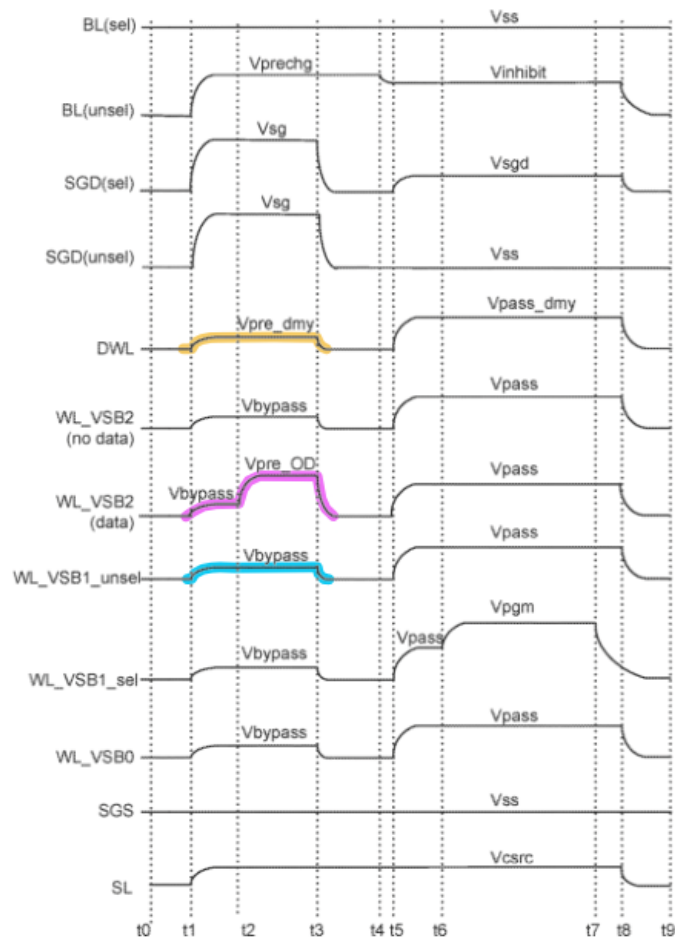
144. DWL2 (which is supplied with Vpre_dmy) separates the word lines into “sub-block[s]” that “are treated as separate units for erase/programming purposes....” Ex. 1010, 9:49-51, 12:22-23.



Ex. 1010, Fig. 8C.

145. Yang explains that Figure 8B—also reproduced below with added color annotations—is a “timing diagram” showing when Yang applies different pre-charge voltage pulses to its word lines. *See* Ex. 1010, 23:20-22. According to Yang, “times t1-t4 correspond to ... [the] pre-charge phase.” *Id.*, 23:23-25.

FIG. 8B



Ex. 1010, Fig. 8B.

B. Ground 1: Claims 1-3, 6, and 11-13 Are Obvious Over Lee

146. In my opinion, a POSITA would have considered Lee to be within the scope of the prior art and highly relevant to the patentability of the '822 patent's claims.

147. In my opinion, when viewed and considered in light of the knowledge possessed by a POSITA at the time of the alleged invention, Lee renders claims 1-3, 6, and 11-13 of the '822 patent obvious.

1. Independent Claims 1 and 11

148. Due to their similarity, I will analyze claims 1 and 11 together.

149. Prior to discussing a particular claim limitation, I have reproduced the language of the limitation. In doing so, I [bracketed] text that is present in only one of the two claims. The non-bracketed text is shared.

[1.Pre]/[11.Pre] “A [method of controlling a memory device, the] memory device, comprising”¹

150. In my opinion, to the extent this preamble language is limiting, it is taught by Lee.

151. Lee teaches that it relates to “a semiconductor memory device” and “a method of operating the semiconductor memory device” with “control logic.” Ex. 1004, 1:52-2:3; *see also id.*, Abstract; 1:16-18.

[1.A]/[11.A] “a plurality of memory strings”

152. This, in my opinion, is taught by Lee.

¹ Claim language is identified throughout this declaration using text that is ***bolded and in italics***.

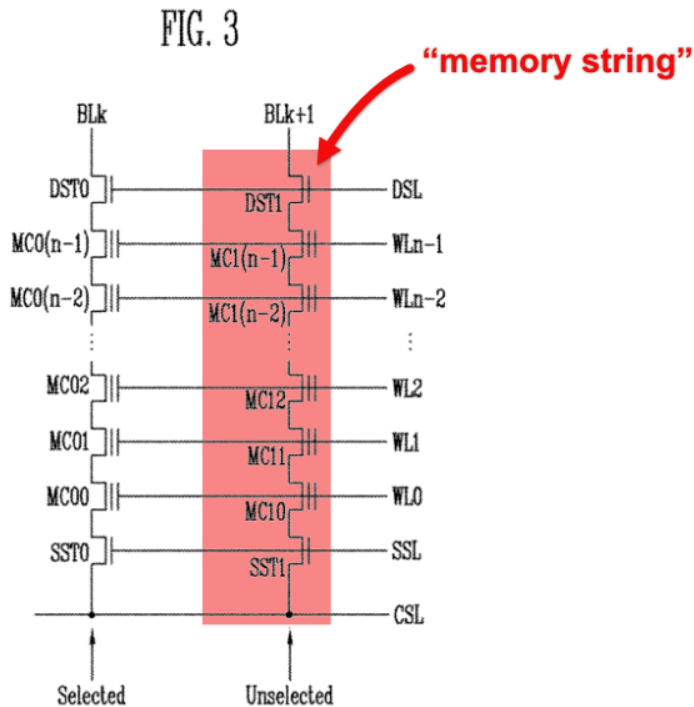
153. Lee explains that its “semiconductor memory device 100 includes a memory cell array 110.” Ex. 1004, 5:60-61.

154. This array “includes a plurality of memory blocks BLK1 to BLKz.” Ex. 1004, 5:64-65. “Each of the memory blocks BLK1 to BLKz includes a plurality of memory cells.” *Id.*, 6:1-3.

155. The memory cells are arranged in a “plurality of cell strings” formed from “memory cells stacked on the semiconductor substrate.” Ex. 1004, 6:12-15; *see also id.*, 1:36-48 (similarly discussing “three-dimensional” NAND memory with “a plurality of strings that are vertically formed on a semiconductor substrate”).

156. “Each of the cell strings includes a drain select transistor, a plurality of memory cells[,] and a source select transistor, which are coupled between a bit line BL and a common source line SL.” Ex. 1004, 6:1-18.

157. Figure 3, which is reproduced below, provides an example of this. The figure depicts two “**memory strings**”—a “selected cell string” that is “targeted for a program operation” and is “coupled to bit line BL_k” and an “unselected cell string” (annotated red below) that is “coupled to bit line BL_{k+1}.” Ex. 1004, 7:28-36.



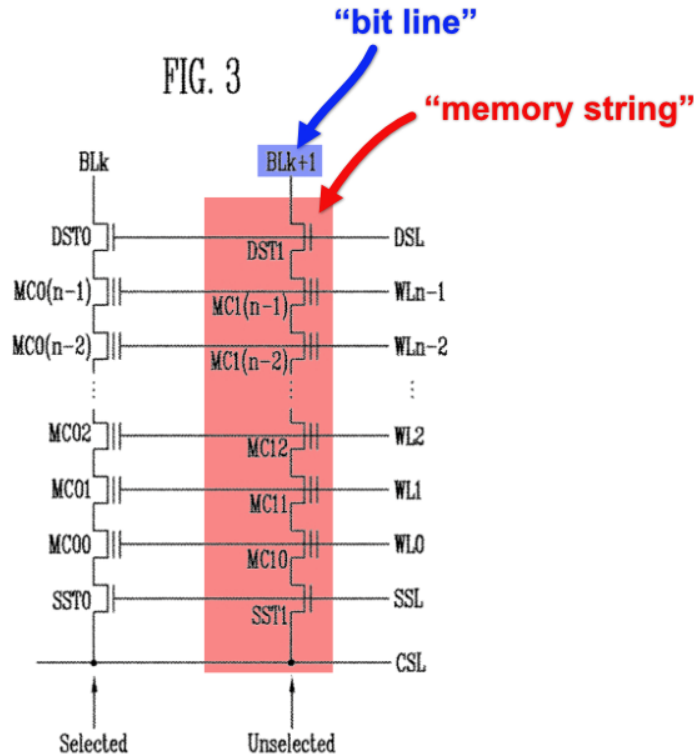
Ex. 1004, Fig. 3; *see also id.*, Fig. 4B (similarly showing multiple cell strings).

[1.B]/[11.B] “a bit line connected to a first memory string of the plurality of memory strings”

158. In my opinion, Lee teaches the claimed **“bit line connected to a first memory string.”**

159. According to Lee, each of “cell string” in its “memory cell array” is “coupled to a bit line.” Ex. 1004, 7:28-36.

160. For example, in Figure 3, the depicted “unselected string” (annotated red) is “coupled to a bit line BLk+1” (annotated blue). Ex. 1004, 7:28-36; *see also id.*, 6:15-18 (explaining that “[e]ach of the cell strings” is “coupled” to a “bit line BL”).



Ex. 1004, Fig. 3; *see also id.*, Fig. 4B (similarly showing bit lines BL0-BLk).

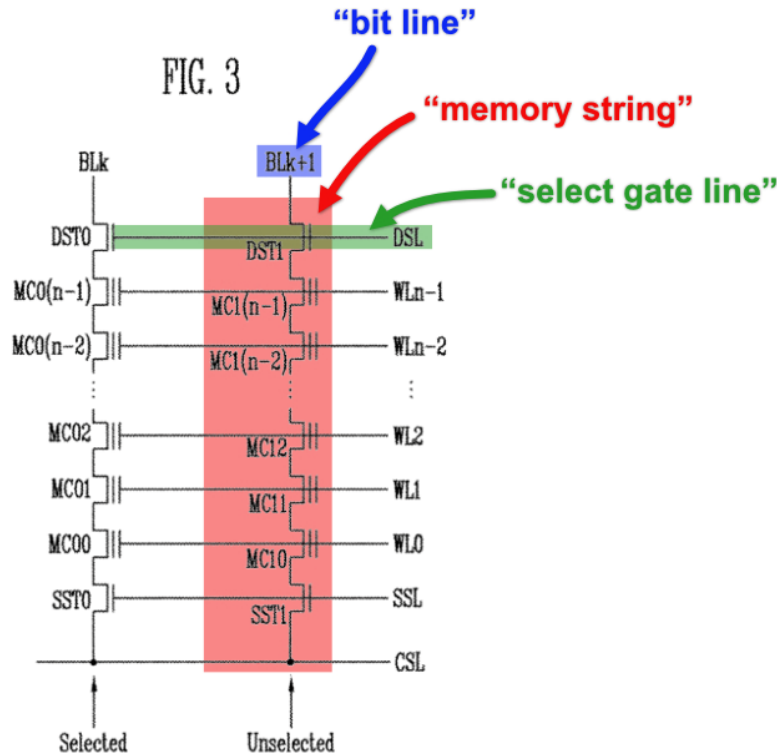
[1.C]/[11.C] “a select gate line connected to the first memory string of the plurality of memory strings”

161. This, in my opinion, is taught by Lee.

162. According to Lee, each “cell string” in its memory array includes an upper “drain select transistor” (DST) that is “coupled to a ... drain select line DSL.”

Ex. 1004, 7:37-43; *see also id.*, 6:15-18 (similarly explaining that “[e]ach of the cell strings includes a drain select transistor”).

163. Lee’s DSL is the claimed “*select gate line*” that is “*connected to the first memory string.*” This DSL is annotated green in Figure 3 below:



Ex. 1004, Fig. 3; *see also id.*, Fig. 4B (similarly showing an upper “DSL”).

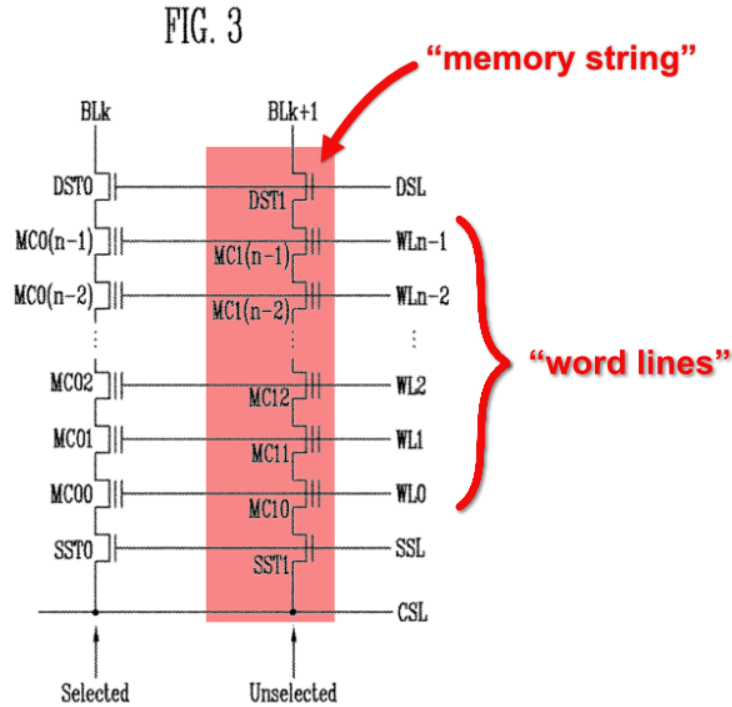
[1.D]/[11.D] “a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string”

164. In my opinion, Lee includes a *“plurality of word lines ... connected to the first memory string.”*

165. According to Lee, the memory cells making up its array’s “memory blocks BLK1 to BLKz” are arranged into “pages” and are “coupled in common to a single word line.” Ex. 1004, 5:64-6:7.

166. There are a “plurality of pages” (and associated “word lines”) in Lee’s memory cell array. Ex. 1004, 5:64-6:7. For instance, in Figure 3, the “memory

cells” in each “cell string” are “coupled to the word lines WL0 to WLn-1. Ex. 1004, 7:30-45.



Ex. 1004, Fig. 3.

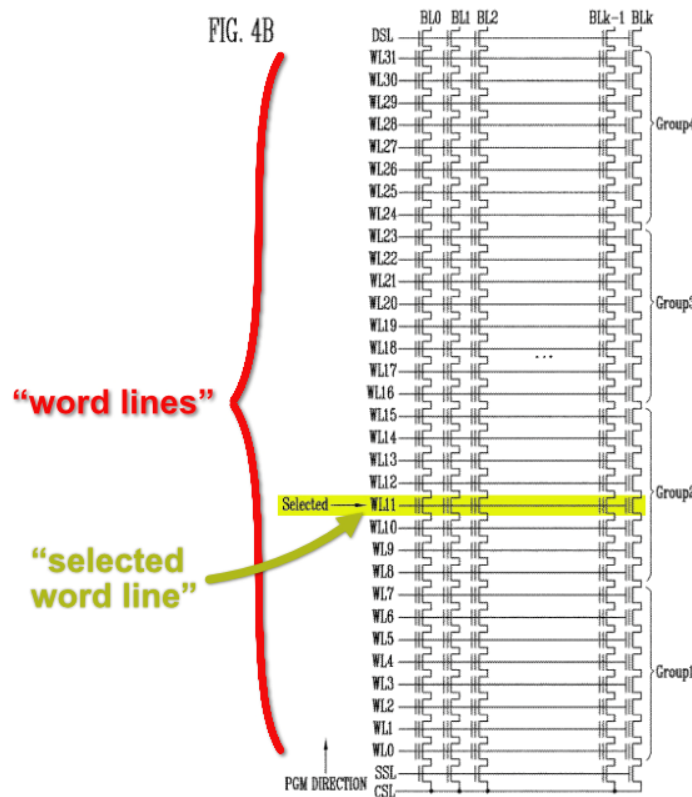
167. Next, Lee explains that individual word lines are “*selected*” during operation of its memory.

168. In one example discussed in Lee, the memory array may include “thirty-two word lines WL0 to WL31.” Ex. 1004, 8:6-7.

169. During programming, both the “bit line” associated with a particular “target” cell’s “string” and the cell’s “word line” are “selected.” Ex. 1004, 7:28-34, 8:18-25. The word lines are selected sequentially following a “program direction.” Ex. 1004, 8:23-25.

170. For instance, the “program direction is a direction from a zeroth word line WL0 toward a thirty-first word line WL31.” Ex. 1004, 8:23-25; *see also id.*, 2:11-12 (“the memory cells may be programmed in a sequence from a memory cell adjacent to a source select transistor”).

171. In Figure 4B below, the “eleventh word line WL11 is selected” and includes “the program cell.” Ex. 1004, 9:15-17, 39-40. The cells are programmed in a “PGM DIRECTION” starting from WL0 and proceeding to WL31:



Ex. 1004, Fig. 4B.

[1.E] “a control circuit configured to” / [11.E] “the method comprising”

172. In my opinion, Lee includes the claimed “**control circuit**” that is “**configured**” to perform the claimed “**method.**”

173. Lee’s “semiconductor memory device 100 includes[,]” among other components, “a control logic 140[.]” Ex. 1004, 5:60-63.

174. The “control logic” is “coupled” to both an “address decoder” and “voltage generation unit[,]” and is “configured to control the overall operation of the semiconductor memory device 100.” Ex. 1004, 7:5-7.

175. This control can entail controlling the “appl[ication] of pre-bias voltages to the word lines during a program operation” via the voltage generation unit and address decoder. Ex. 1004, 7:8-10.

176. More specifically, “the voltage generation unit 150 generates and outputs” different voltages. Ex. 1004, 7:14-19. These output voltages are then applied to the appropriate portions of the “memory cell array 110” by the “address decoder 120.” *Id.*, 6:29-35; *see also id.*, Abstract (referencing a “semiconductor memory device” with a “control logic”; Fig. 1 (showing “control logic 140” controlling the “voltage generation unit 150” and “address decoder 120” for purposes of applying voltages to word lines WL).

[11.E.0] “applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period”

[1.E.1]/[11.E.1] “apply[ing] a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a [the] pre-charge period”

[1.E.2]/[11.E.2] “apply[ing] a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and”

[1.E.3]/[11.E.3] “apply[ing] a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period”

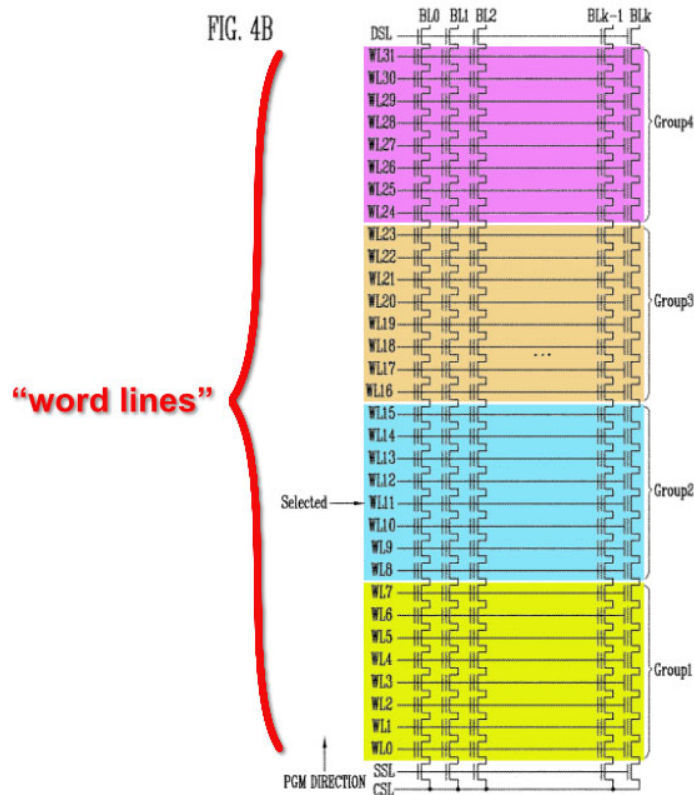
177. This, in my opinion, is rendered obvious by Lee.

178. These limitations require arrangement of word lines into “*first*,” “*second*,” and “*third*” “*group[s]*” of “*word lines*.” They also require application of “*first*,” “*second*,” and “*third*” “*word line pre-pulse signal[s]*” to “*first*,” “*second*,” and “*third*” “*group[s]*” of “*word lines*” during a “*pre-charge period*.” Claim 11 additionally requires application of a “*word line signal to the selected word line*” during this same “*pre-charge period[.]*” This, in my opinion, is what Lee teaches.

179. Lee arranges its word lines into multiple “*group[s]*.”

180. Lee explains that “the word lines coupled to a memory string in a memory block may be grouped ... during a precharge operation of the cell string.” Ex. 1004, 7:58-61; *see also id.*, 2:4-5 (explaining that the various word lines can be “grouped into a plurality of word line groups”).

181. For example, in Figure 4B, “the control logic may group the thirty-two word lines into four word line groups. Each of the first to fourth word line groups Group1 to Group4 includes eight word lines.” Ex. 1004, 9:36-40. These “group[s]” are annotated in purple, orange, blue, and yellow below:



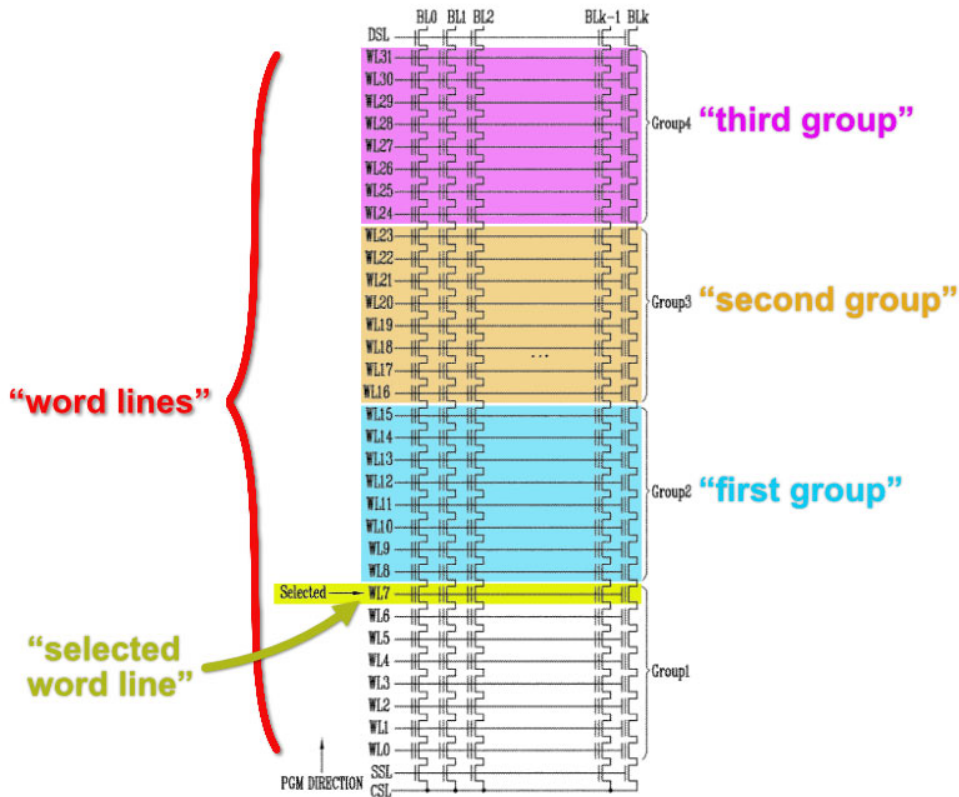
Ex. 1004, Fig. 4B.

182. Again, in this Figure’s example, the cells are programmed in sequence starting at the source side and “word line WL11” is shown as “selected[.]” Ex. 1004, 9:39-40.

183. The below demonstrative provides an example where another word line—this time WL7 in Group1—is now the selected word line. Because the word

lines are programmed from WL0 to WL31 (*see* “PGM DIRECTION” in Fig. 4B),

184. As shown, there is a **“first group”** (WL8-WL15 in Group2, annotated blue), **“second group”** (WL16-WL23 in Group 3, annotated orange), and **“third**



See Ex. 1004, Fig. 4B (modified to show WL7 as selected).

185. Next, in my opinion Lee teaches use of a “*plurality*” of “*word line pre-pulse signal/s*” during a “*pre-charge period.*”

186. According to Lee, “different pre-bias voltages may be applied to the respective groups during a precharge operation of the cell string.” Ex. 1004, 7:58-61; *see also* Abstract (“different pre-bias voltages are applied to the plurality of word lines depending on the relative positions of the word lines”); *see also id.*, 1:62-2:3 (similar).

187. Lee explains that the “pre-bias voltages ... applied to the plurality of word lines” vary by group, and change “depending on the respective position of the word lines” for purposes of “precharg[ing the] channel regions of the plurality of memory cells” coupled to the word lines. Ex. 1004, 1:65-2:3.

188. The closer “a word line group to which a word line belongs is to the” upper “drain select transistor, the higher a pre-bias voltage ... applied to the word line may be.” Ex. 1004, 8:32-37; *see also id.*, 2:5-9.

189. In the specific example of Figure 4B, because “WL11” is “selected,” Lee provides its “Group2” word lines with “[a] pre-bias voltage having a default value.” Ex. 1004, 9:52-55. The “Group3” word lines are provided with a “higher” “pre-bias voltage” than that provided to “Group2.” *Id.*, 9:44-48. And the “Group4” word lines are provided with a “higher” “pre-bias voltage” than that provided to “Group3.” *Id.*, 9:48-52.

190. Likewise, when WL7 in Group1 is selected, Group1 will be provided with the “default value” (because it includes the selected word line) while the word

lines in Group2, Group3, and Group4 will be provided with increasingly higher “pre-bias voltages” the further away they are from the selected word line. Ex. 1004, 1:65-2:9, 8:32-37, 9:36-59.

191. The demonstrative below provides an example.

192. As shown, the claimed ***“first word line pre-pulse signal”*** is applied to a ***“first group of the plurality of word lines”*** (the pre-bias voltage applied to WL8-WL15 in Lee’s Group2, annotated blue below), a ***“second word line pre-pulse signal”*** is applied to a ***“second group of the plurality of word lines”*** (the higher pre-bias voltage applied to WL16-WL23 in Lee’s Group3, annotated orange), and a ***“third word line pre-pulse signal”*** is applied to a ***“third group of the plurality of word lines”*** (the even higher pre-bias voltage applied to WL24-WL31 in Lee’s Group4, annotated purple):



See Ex. 1004, Fig. 4B (modified to show WL7 as selected).

193. In my opinion, a POSITA would have understood that Lee's pre-bias voltages to be *"pre-pulse signal[s]"* applied during a *"pre-charge period[.]"*

194. The '822 patent explains that the "pre-charge period" occurs "before programming" voltages are applied to selected memory cells. Ex. 1001, 3:43.

195. This, in my opinion, is when Lee applies its pre-bias voltages.

196. Lee repeatedly refers to these voltages as "precharge voltage[s]" that are applied for purposes of "precharge[ing the] channel regions" of its memory cells. Ex. 1004, 1:62-2:1; 2:30-32. These voltages are applied during a separate "precharge operation" that occurs prior to application of "a program voltage" to the

memory's word lines. *Id.*, 9:7-11; *see also id.*, 2:59-62 (“application of the pre-bias voltages” occurs before “a program loop for a selected program cell”); 11:19-22 (referencing a separate “step S205” during which “precharging” occurs, followed by a “step S207 of performing a program loop”); Fig. 7 (showing separate steps S205 and S207).

197. In my opinion, a POSITA also would have understood (or considered it obvious) that the Lee's pre-bias voltages are supplied in the form of a “*pulse*.”

198. According to Lee, there are two different periods of operation during programming of its memory array.

199. The programming operation commences by grouping of the word lines coupled to the memory cells. As discussed in Paragraphs 185-190, this grouping is for the purpose of applying different pre-bias voltages.

200. The “pre-bias voltages” are applied during a “precharge operation” period. Ex. 1004, 7:58-61; *see also id.*, 7:63-67 (discussing the “appl[ication] of different pre-bias voltages to word lines at a precharging step during a programming operation”); 8:15-17 (“pre-bias voltages” are “applied to the ... word lines ... in a precharging step”).

201. Then, when the “precharge operation is completed, a program loop operation is subsequently performed. During the program loop operation, a different set of voltages will be applied to the memory array: a program voltage may be

applied to the selected word line” and “a pass voltage may be applied to the unselected word lines” in this separate “program loop” step. Ex. 1004, 9:7-13; *see also id.*, 6:29-32 (explaining that “program voltages V_{pgm} ” are applied to cells that are being programmed, while “pass voltages V_{pass} ” are applied to non-programmed cells).

202. Further, Lee explains that its programming voltage application is not continuous but is instead “repeatedly performed” in a “program loop.” Ex. 1004, 9:10-13.

203. Because Lee (1) supplies its pre-bias voltages in a separate and distinct in time step, and (2) the pre-bias voltages differ from the later V_{pgm} and V_{pass} voltages, a POSITA would have understood the pre-bias voltages to be supplied for only the precharging period, and then removed prior to commencing the program loop where a different set of programming voltages will be supplied to the memory cells. A POSITA would have known that these on-off pre-bias voltages during the precharging period are the very definitions of “*pulse[s]*.”

204. Moreover, when the ’822 patent was filed, programming voltages were conventionally provided in the form of a “pulse.” Ex. 1006, 44; *see also id.*, 116-117 (providing examples of various “conventional programming pulse[s]”); Ex. 1007, 142-143 (explaining that “pulses of predetermined duration are repeatedly applied” to a “cell” during “programming”); Ex. 1008, 354 (explaining that

“program voltages are provided to ... selected cells for the desired amount of time” as a “pulse”); Ex. 1008, 338 (referencing the use of various program “pulses”).

205. In my opinion, a POSITA would have understood Lee to operate in the same way. All of the voltages Lee supplies during its precharge/programming process, including both the pre-bias voltages and the later program and pass voltages, would obviously be supplied as pulses.

206. In my opinion, Lee also teaches the application of a “*word line signal to the selected word line*” during its “*pre-charge period[.]*”

207. Here, Lee explains that the “word line group” that includes “a word line coupled to a program cell”—the selected word line—is provided with a “default value” “[p]re-bias voltage[.]” during precharge. Ex. 1004, 2:23-29.

208. Thus, in the example shown in Figure 4B where WL11 is selected, “[a] pre-bias voltage having [the] default value is applied to the word lines WL8 to WL15 included in the second Group2, including a word line WL11 that is coupled to a selected transistor.” Ex. 1004, 9:52-55.

209. Again, as explained, when the “selected” word line is in Lee’s Group1, it will be supplied with a different pre-bias voltage than that supplied to the word lines in Lee’s Group2, Group3, and Group4. See Ex. 1004, 2:5-9 (“[T]he closer a word line group ... is to a first-programmed memory cell ..., the lower a pre-bias voltage ... applied to the word line may be.”); see also *id.*, 9:36-59.

[1.E.4]/[11.E.4] “wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal”

210. This, in my opinion, is rendered obvious by Lee.

211. Again, Lee explains that “different pre-bias voltages” are applied to its word line “groups during a precharge operation....” Ex. 1004, 7:58-61; *see also* Abstract; 1:62-2:3.

212. And in Figure 4B, “higher ... pre-bias voltage[s]” are applied to “word line group[s]” that are closer to the “drain select transistor....” Ex. 1004, 8:32-37; 9:44-51; *see also id.*, 1:65-2:9.

213. Thus, when WL7 in Group1 is selected as shown in the demonstrative below (which is the same demonstrative I discuss above), the ***“third” “pre-pulse signal”*** applied to Lee’s ***“third group”*** of word lines (WL24-WL31, annotated purple) exceeds the ***“second” “pre-pulse signal”*** applied to the ***“second group”*** of word lines (WL16-WL23, annotated orange). And this ***“second” “pre-pulse signal”*** exceeds the ***“first” “pre-pulse signal”*** applied to the ***“first group”*** of word lines (WL8-WL15, annotated blue):



See Ex. 1004, Fig. 4B (modified to show WL7 as selected).

2. Claims 2 and 12

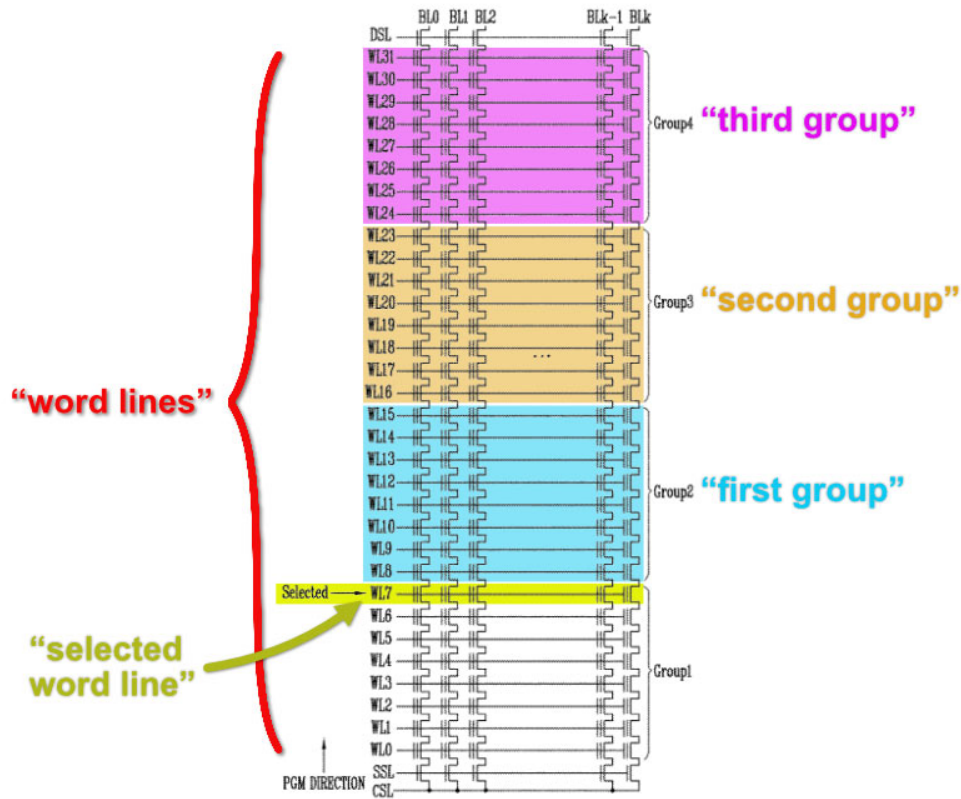
214. Claim 2 depends on claim 1. Claim 12 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines”

215. This, in my opinion, is taught by Lee.

216. As shown in the demonstrative below (which is the same demonstrative employed when discussing claims 1 and 11), Lee’s *“first group ... of word lines”* (WL8-WL15), *“second group ... of word lines”* (WL16-WL23), and *“third*

group ... of word lines” (WL24-WL31) are “*disposed in an order of distance*” from the “*selected word line*” (WL7):



See Ex. 1004, Fig. 4B (modified to show WL7 as selected); 9:35-55.

3. Claims 3 and 13

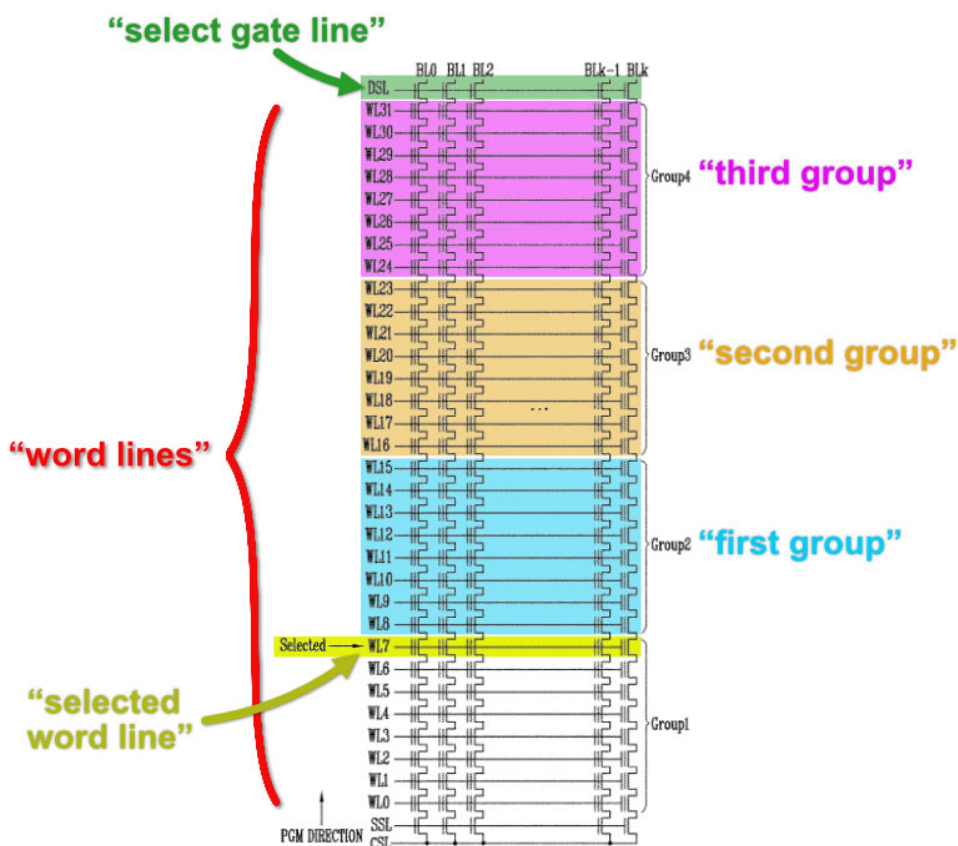
217. Claim 3 depends on claim 1. Claim 13 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line”

218. This, in my opinion, is taught by Lee.

219. Again, as I have explained, Lee teaches that its memory array includes an upper “drain select line DSL.” Ex. 1004, 7:37-43; *see also id.*, 6:15-18; *supra* discussion of limits [1.C]/[11.C].

220. As shown in the demonstrative below, an example “*selected word line*” (WL7, annotated yellow), “*first group ... of word lines*” (WL8-WL15, annotated blue), “*second group ... of word lines*” (WL16-WL23, annotated orange), “*third group ... of word lines*” (WL24-WL31, annotated purple), and “*select gate line*” (DSL, annotated green) are also arranged in order as this claim requires:



See Ex. 1004, Fig. 4B (modified to show WL7 as selected).

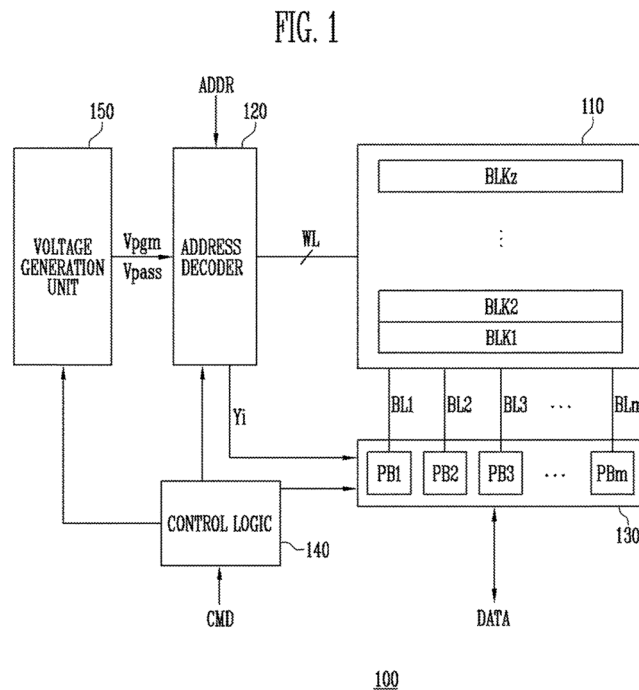
4. Claim 6

221. Claim 6 depends on claim 1 and further requires that:

“the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines”

222. This, in my opinion, is taught by Lee for the same reasons explained in connection with claim 1.

223. FIG. 1 in Lee, shown below, illustrates the control circuit, in the form of the control logic, and its interaction with the word line signals.



Ex. 1004, Fig. 1.

224. “The address decoder 120 is coupled to the memory cell array 110 through the word lines WL. The address decoder 120 is configured to operate in

response to control of the control logic 140.” Ex. 1004, 6:22-25. “The address decoder 120 applies, during a program operation, program voltages V_{pgm} , pass voltages V_{pass} , and operating voltages which are generated from the voltage generation unit 150, to a plurality of memory cells,” *Id.*, 6:29-33.

225. Additionally, Lee’s control unit causes the “selected” word line to be supplied with a “default value” “[p]re-bias voltage[.]” during precharge. Ex. 1004, 2:23-29; 9:52-55; *see also supra* discussion of limit [11.E.0].

C. Ground 2: Claims 1, 4-7, 9, 11, 14-16, and 18-19 Are Obvious Over Zhao

226. In my opinion, a POSITA would have considered Zhao to be within the scope of the prior art and highly relevant to the patentability of the ’822 patent’s claims.

227. In my opinion, when viewed and considered in light of the knowledge possessed by a POSITA, Zhao renders claims 1, 4-7, 9, 11, 14-16, and 18-19 of the ’822 patent obvious.

1. Independent Claims 1 and 11

[1.Pre]/[11.Pre] “A [method of controlling a memory device, the] memory device, comprising”

228. In my opinion, to the extent this preamble language is limiting, it is taught by Zhao.

229. Zhao teaches a “memory system 100” that “implements” various “countermeasures for avoiding program disturb.” Ex. 1005, 4:7-10.

230. The memory can include “a three dimensional memory array” with multiple “NAND strings.” Ex. 1005, 6:34-44.

[1.A]/[11.A] “a plurality of memory strings”

231. In my opinion, Zhao includes the claimed “*plurality of memory strings.*”

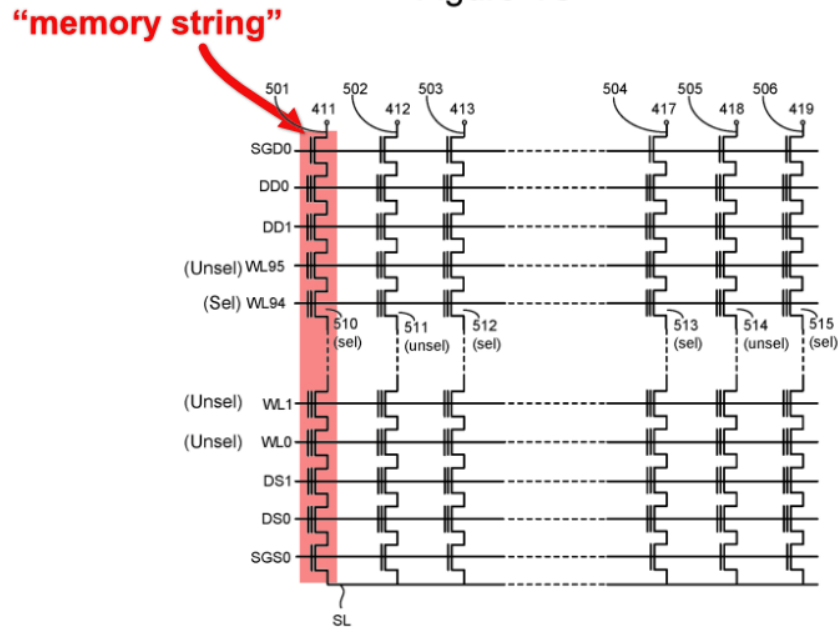
232. According to Zhao, a “three dimensional (‘3D’) NAND structure” includes a “plurality of ... vertical columns[,]” where “each vertical column implements a NAND string.” Ex. 1005, 8:31-44; *see also id.*, 6:41-43 (explaining that Zhao’s “memory structure” includes multiple “vertical NAND strings”).

233. Each of these “NAND strings” includes a series of “non-volatile memory cells.” Ex. 1005, 10:6-9.

234. Figure 4G—which depicts a “sub-block” of Zhao’s memory—provides an example. Ex. 1005, 12:6-7.

235. This figure, which is reproduced in annotated form below, depicts “six NAND strings 501, 502, 503, 504, 505, and 506” of the “thousands of NAND strings” making up the sub-block. Ex. 1005, 12:9-13. One of these strings is shown in red for emphasis:

Figure 4G



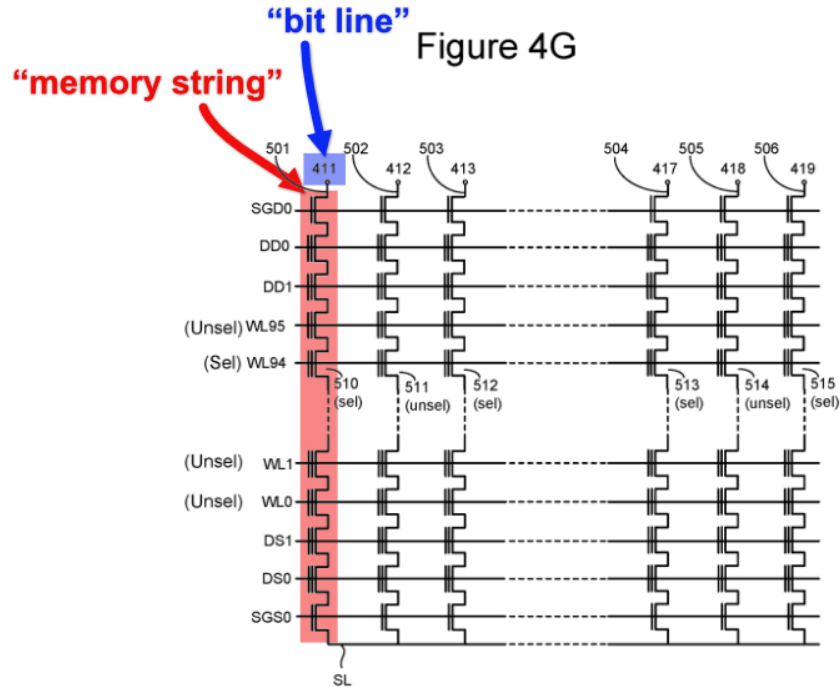
Ex. 1005, Fig. 4G; *see also* Fig. 4F.

[1.B]/[11.B] “a bit line connected to a first memory string of the plurality of memory strings”

236. In my opinion, Zhao teaches “a bit line” that is “connected to a first memory string.”

237. Each of Zhao’s “NAND strings” is connected to a “bit line.” Ex. 1005, 11:53-61; *see also id.*, 8:54-61 (explaining that the memory includes a “set of bit lines 415, including bit lines 411, 412, 413, 414, ... 419” connected to the strings).

238. One such bit line 411 is annotated blue in Figure 4G below:



Ex. 1005, Fig. 4G; *see also* Fig. 4F.

[1.C]/[11.C] “a select gate line connected to the first memory string of the plurality of memory strings”

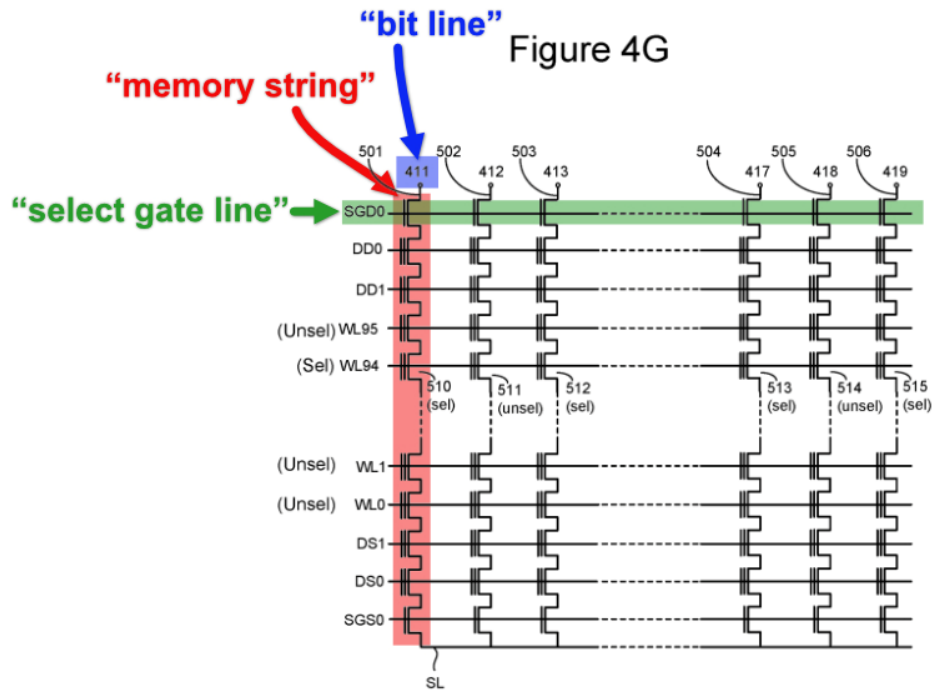
239. In my opinion, Zhao also teaches the claimed ***“select gate line connected to the first memory string.”***

240. According to Zhao, its “three dimensional memory array” can include, for instance, “8 select layers.” Ex. 1005, 7:64-66; *see also id.*, 9:34-38.

241. This includes upper “[d]rain side select layers SGD0, SGD1, SGD2, and SGD3” that “are used to electrically connect and disconnect NAND strings from bit lines.” Ex. 1005, 10:19-21; *see also id.*, 11:59-60 (similarly referencing “[d]rain side selection lines” that “connect” the “NAND strings ... to the associated bit line(s)”.

242. According to Zhao, all the “NAND strings” in each “[s]ub-block” are “connected” to the same SGD. Ex. 1005, 12:6-10.

243. One such SGD is annotated green in Figure 4G below:



Ex. 1005, Fig. 4G; *see also* Fig. 4F.

[1.D]/[11.D] “a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string”

244. In my opinion, Zhao teaches the claimed “***plurality of word lines is connected to the first memory string.***”

245. Zhao explains that its memory can include “96 data word line layers” and “6 dummy word line layers.” Ex. 1005, 7:64-66; *see also id.*, 9:34-38.

246. The “word line layers WLL0-WLL95 connect to” the “memory cells” making up Zhao’s NAND strings.” Ex. 1005, 10:8-13; *see also id.*, 12:6-9.

247. The “[d]ummy word line layers DD0, DD1, DS0, DS1, WLDL, and WLDU connect to dummy memory cells” in the strings. Ex. 1005, 10:11-13.

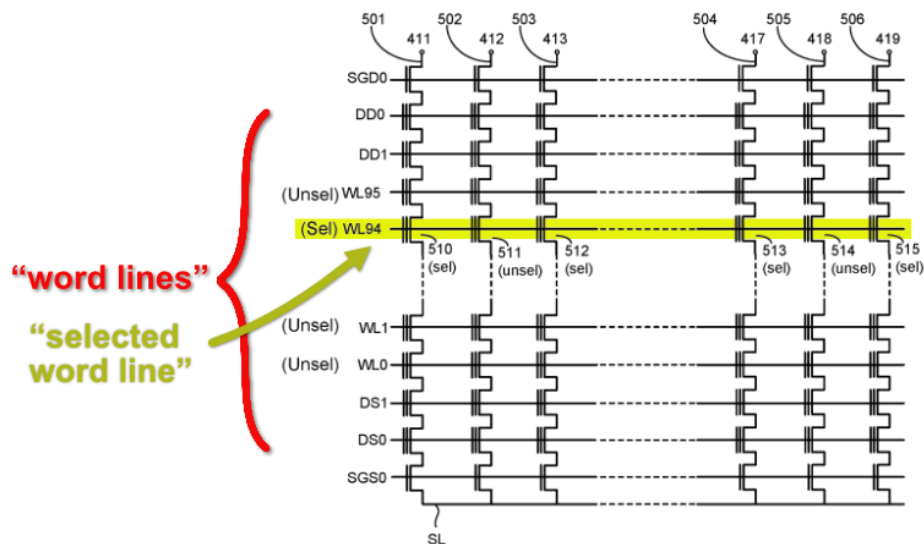
248. Next, in my opinion Zhao also teaches the claimed “*selected word line.*”

249. According to Zhao, during “a programming process[,]” certain memory cells are “selected” “to take on a new electric characteristic ... to reflect a changed programming state.” Ex. 1005, 3:30-49.

250. As part of this, the memory’s word lines are selected one at a time in “order WL0, WL1, WL2, ... WL95.” Ex. 1005, 17:27-30; *see also id.*, 17:13-45 (discussing various “selected” and “unselected” word lines during programming.)

251. In Figure 4G below, “word line WL94” is shown as “selected for programming.” Ex. 1005, 12:14-25.

Figure 4G



Ex. 1005, Fig. 4G; *see also* Fig. 4F.

[1.E] “a control circuit configured to” / [11.E] “the method comprising”

252. In my opinion, Zhao includes the claimed “*control circuit*” that performs a pre-charging “*method.*”

253. Zhao’s memory includes “[c]ontrol circuitry 310” that “perform[s] memory operations ... on memory structure 326.” Ex. 1005, 5:64-66. Similarly, Zhao explains that the “control circuit” is responsible for “perform[ing]” the “process for programming.” *Id.*, 13:65-14:6.

254. The “control circuitry” includes a “power control circuit 316” that “creat[es] voltages.” Ex. 1005, 5:66-6:20.

255. The “controller” can also include a “pre-charge circuit 584” that is responsible for “perform[ing] the pre-charging of the channels of unselected NAND

strings, including applying the pre-charge signals” at the appropriate time during the programming process. Ex. 1005, 16:40-67; *see also* Fig. 8.

[11.E.0] “applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period”

[1.E.1]/[11.E.1] “apply[ing] a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period”

[1.E.2]/[11.E.2] “apply[ing] a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and”

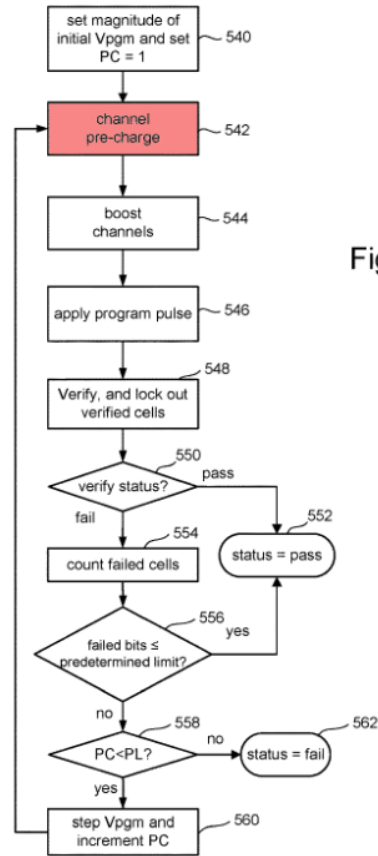
[1.E.3]/[11.E.3] “apply[ing] a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period”

256. This, in my opinion, is all rendered obvious by Zhao.

257. In particular, Zhao renders obvious a system in which different “***word line pre-pulse signal[s]***” are applied to a memory’s “***word lines***” “***during a pre-charge period.***”

258. Zhao explains that “[t]o assist in ... boosting[,]” its “control circuit” can “pre-charge” the “channels of NAND strings.” Ex. 1005, 13:65-14:1, 14:35-40; *see also id.*, 16:65-67 (similarly discussing “pre-charging of the channels of unselected NAND strings”).

259. As shown in Figure 7, this “pre-charge” (step 542) occurs before application of a “program pulse” (step 546):



Ex. 1005, Fig. 7; *see also id.*, 14:35-55 (explaining that “pre-charge” occurs before application of the “program signal Vpgm ... to the selected word line”).

260. Zhao goes on to explain that its “memory system pre-charges the channels of at least a subset of unselected NAND strings ... prior to” programming “by applying one or more pre-charge voltages to the selected word line and drain side unselected word lines.” Ex. 1005, 19:12-17.

261. According to Zhao, “[b]y applying these pre-charge voltages, the voltage of the channel will be raised, which will improve the future boosting.” Ex. 1005, 19:17-19.

262. The “voltage[s] applied to the control gates” by Zhao are in the form of “pulses.” Ex. 1005, 14:7-16.

263. Further, Zhao also teaches that multiple different “pre-charge voltages” can be employed. Ex. 1005, 19:19-60.

264. For instance, the “only” word lines on the “drain side of the channel” (*i.e.*, those between the currently selected word line and the top select gate) can receive a “pre-charge” voltage. Ex. 1005, 19:19-23; 19:57-58.

265. The majority of the “source side” word lines “receive 0 volts or one or more voltages that are too low to pre-charge.” Ex. 1005, 19:22-23.

266. And “multiple already programmed (e.g. source side) unselected word line[s] ... adjacent to the selected word line” can “receive[]” a different “bypass voltage” “while pre-charging[.]” Ex. 1005, 19:32-50.

267. Annotated Figures 4G and 13 below shows the application of these various “***word line pre-pulse signal[s]***” during a “***pre-charge period.***”

268. Zhao explains that “time period ... t1-t3 corresponds to pre-charging.” Ex. 1005, 22:39-41.

269. As shown, three different voltages are applied to different groups of word lines in this period.

270. First, “Vprecharge (e.g., ~2 volts)” is applied to “selected word line WLn” and “drain side unselected word lines WLn+x.” Ex. 1005, 22:41-49.

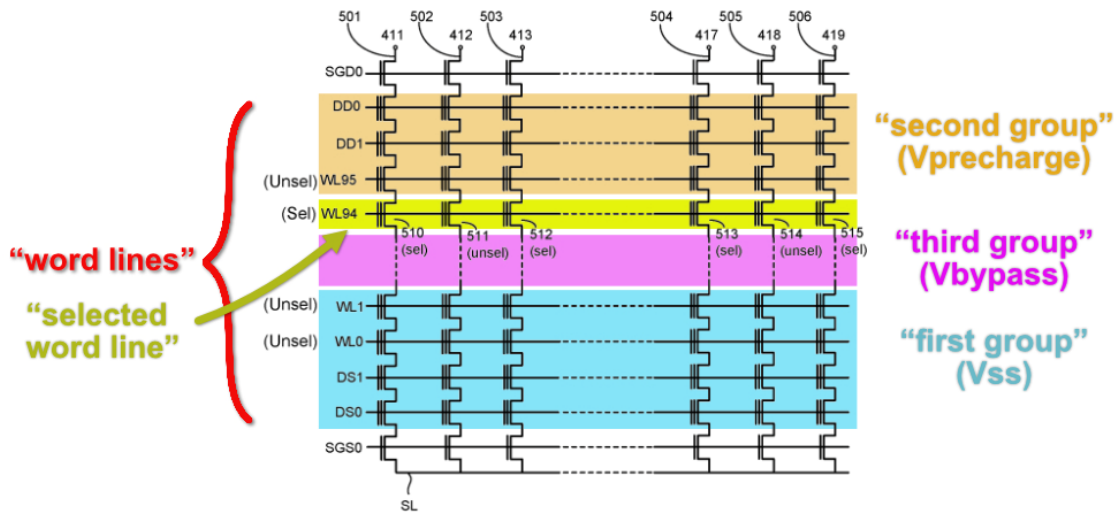
271. Second, “Vbypass (e.g., ~6-10 volts)” is applied to “already programmed source side unselected word lines WLn-1 and WLn-2[.]” Ex. 1005, 22:50-53.

272. And third, “[t]he remaining source side unselected word lines WLn-x remain at Vss (e.g., 0 v).” Ex. 1005, 23:7-9. Again, while Vss is 0V in the Figure, Zhao explains that a “low” non-zero voltage signal can be applied instead in the same t1-t3 time period as the other pre-charge pulses. *Id.*, 19:22-24. This applied voltage is greater than zero, but not as high as the other pre-charge voltages. *See id.*

273. In my opinion, application of these different pre-charge voltages to these different groups of word lines results in what this limitation requires.

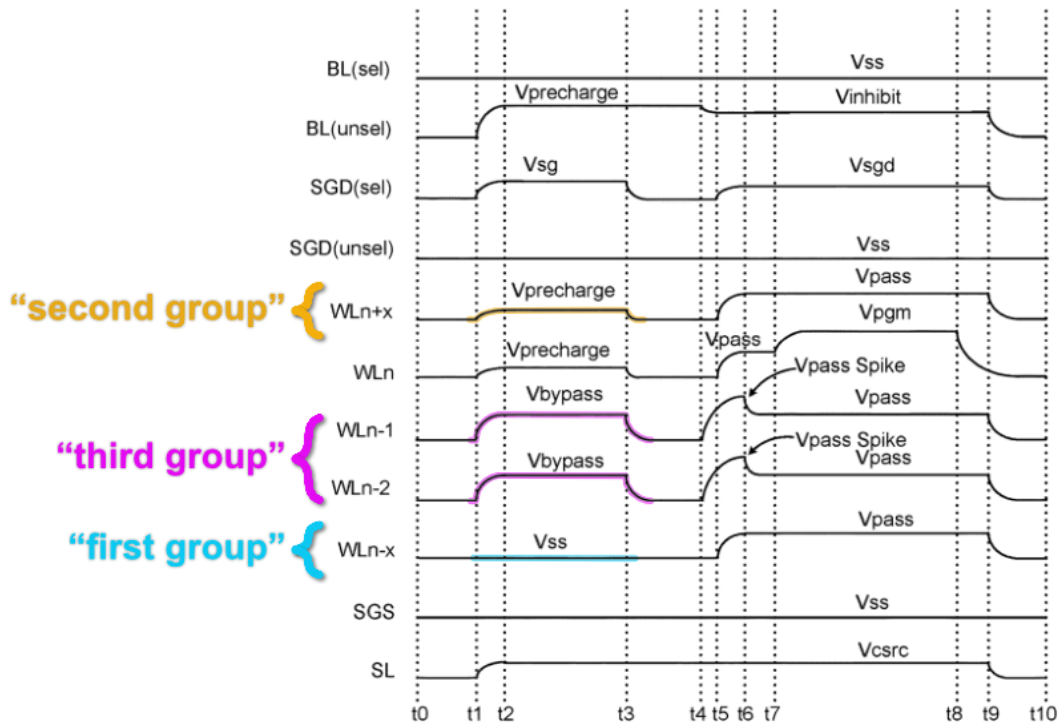
274. More particularly, a “***first word line pre-pulse signal***” (a low non-zero voltage in place of Vss, annotated blue) is applied to a “***first group of ... word lines***” (source side word lines WLn-x), a “***second word line pre-pulse signal***” (Vprecharge, annotated orange) is applied to a “***second group of ... word lines***” (drain side word lines WLn+x), and a “***third word line pre-pulse signal***” (Vbypass, annotated purple) is applied to a “***third group of ... word lines***” (source side word lines WLn-1 and WLn-2):

Figure 4G



Ex. 1005, Fig. 4G.

Figure 13



Ex. 1005, Fig. 13.

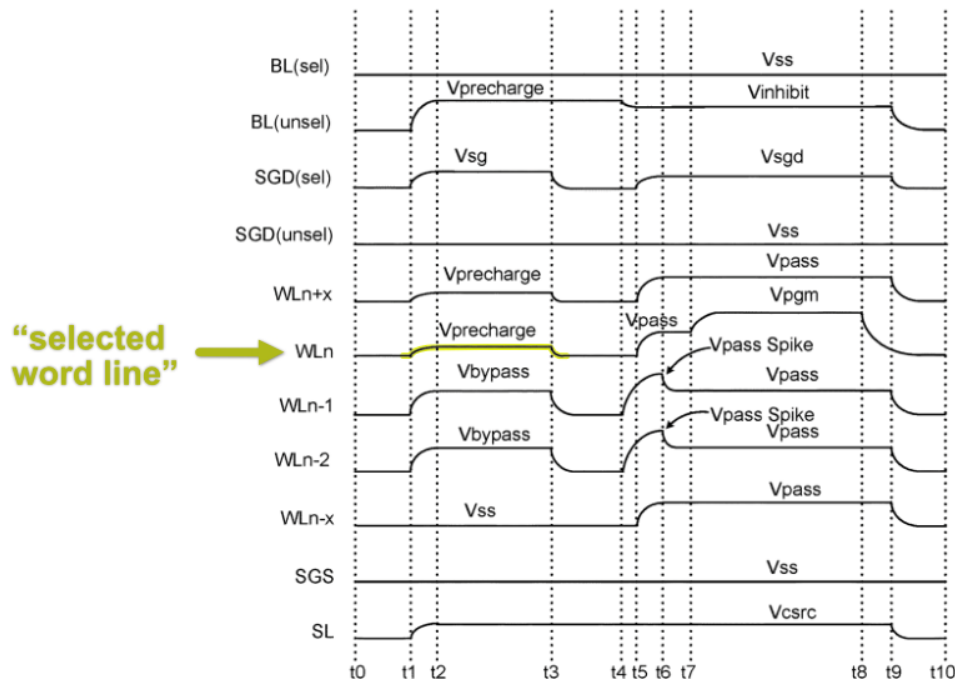
275. Claim 11 additionally requires application of a “**word line signal to the selected word line**” during this same “**pre-charge period[,]**”

276. This, in my opinion, is also taught by Zhao.

277. In particular, Zhao explains that during “pre-charging” time period “t1-t3[,]” “the selected word line WLn is raised to the pre-charge voltage....” Ex. 1005, 22:39-49; *see also id.*, 19:12-19 (explaining that during the “pre-charge” step, a “pre-charge voltage[.]” is “appl[ied] ... to the selected word line”).

278. The signal applied to the selected word line WLn shown in Figure 13:

Figure 13



Ex. 1005, Fig. 13.

[1.E.4]/[11.E.4] “wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal”

279. This, in my opinion, is also rendered obvious by Zhao.

280. In particular, the voltage of Zhao’s ***“third word line pre-pulse signal”*** (Vbypass, 6-10 volts) is highest, the voltage of its ***“second word line pre-pulse signal”*** (Vprecharge, 2 volts) is next highest, and the voltage of its ***“first word line pre-pulse signal”*** (a “low” non-zero voltage in place of Vss). See Ex. 1005, 19:19-24; 19:57-58; 22:39-23:9; Fig. 13.

2. Claims 4 and 14

281. Claim 4 depends on claim 1. Claim 14 depends on claim 11. Both claims similarly require:

that “the control circuit is configured to apply” (claim 4) or “applying” (claim 14) “a bit line pre-pulse signal to the bit line during the pre-charge period”

282. This, in my opinion, is taught by Zhao.

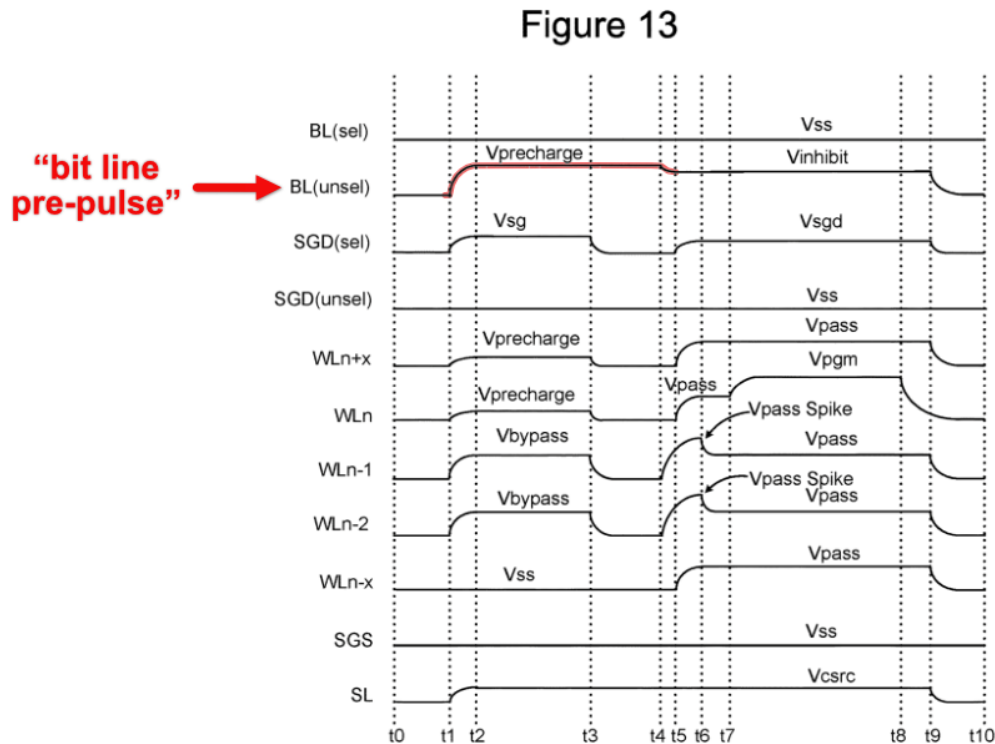
283. Zhao’s ***“control circuit”*** applies a ***“bit line pre-pulse signal”*** ***“during the pre-charge period.”***

284. As I explained in connection with claim 1, Zhao includes “control circuitry” that “performs the pre-charging of the channels of unselected NAND strings” by “applying the pre-charge signals....” Ex. 1005, 16:53-67; see also *id.*, 5:64-6:20; 13:65-14:6.

285. And as part of this, “the unselected bit lines are raised to a pre-charge voltage $V_{precharge}$ (e.g., ~2 volts)” during the “t1-t3 ... precharging” period. Ex. 1005, 22:39-44.

286. The unselected bitline is maintained at this voltage until beginning of a later “boosting” period that begins at t4. Ex. 1005, 23:13-18.

287. This bit-line pre-pulse signal is shown in Figure 13 below:



Ex. 1005, Fig. 13.

3. Claims 5 and 15

288. Claim 5 depends on claim 4. Claim 15 depends on claim 14. Both claims further require that:

“the first memory string is an unselected memory string, and the bit line is an unselected bit line”

289. This, in my opinion, is also taught by Zhao.

290. As I have explained, Zhao applies various pre-pulse signals to its memory’s word lines for purposes of pre-charging the channels of the memory’s strings. *See* Ex. 1005, 13:65-14:1, 14:35-40; 16:65-67.

291. Further, according to Zhao, its system operates to “pre-charge[] the channels of ... unselected NAND strings ([i.e.] channels connected to unselected memory cells.” *Id.*, 19:10-17. So, just as this claim requires, the ***“first memory string”*** whose channel is pre-charged during the ***“pre-charge period”*** is an ***“unselected memory string.”***

292. Moreover, as part of this, Zhao applies a “pre-charge voltage” pulse to “unselected bitlines.” *Id.*, 22:39-45; *see also* Fig. 13. As a result, the bit line connected to the channel subject to pre-charging is ***“an unselected bitline”*** as this claim requires.

4. Claim 6

293. Claim 6 depends on claim 1 and further requires that:

“the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines”

294. This, in my opinion, is taught by Zhao for the same reasons explained in connection with limitation [11.E.0].

295. In particular, during “pre-charging,” “the selected word line WLn is raised to the pre-charge voltage....” Ex. 1005, 22:39-49; *see also id.*, 19:11-17; Fig. 13; *supra* discussion of limit [11.E.0].

296. Zhao also applies a “program signal Vpgm ... to the selected word line” during later programming. Ex. 1005, 14:49-51; Fig. 13.

5. Claims 7 and 16

297. Claim 7 depends on claim 1. Claim 16 depends on claim 11. Both claims similarly require that:

“[the control circuit is configured to] apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the pre-charge period”

298. This, in my opinion, is rendered obvious by Zhao.

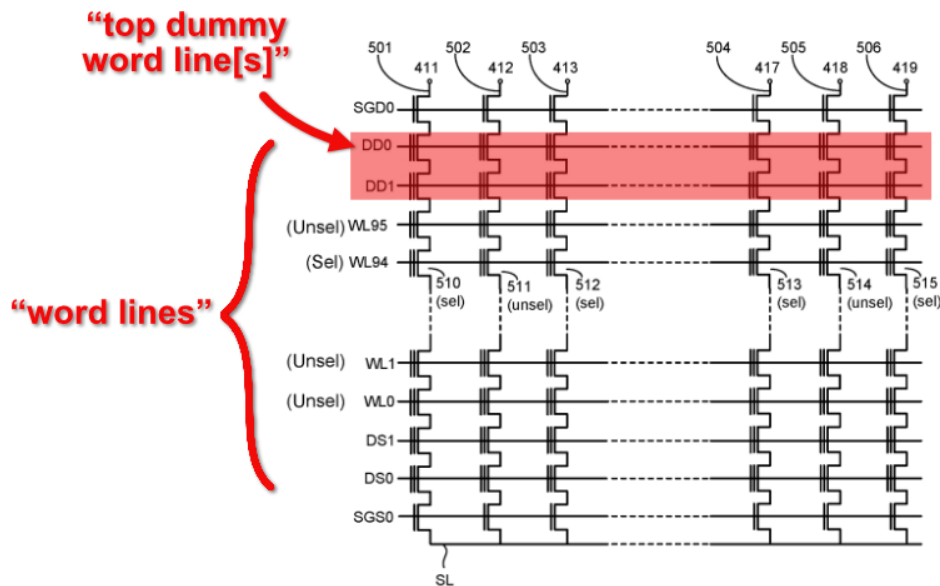
299. In particular, Zhao’s memory includes ***“a top dummy word line of the plurality of word lines.”***

300. According to Zhao, its memory can include “6 dummy word line layers.” Ex. 1005, 7:64-66; *see also id.*, 9:34-38.

301. Two of these—dummy word line layers DD0 and DD1—are located on the upper “drain” side of Zhao’s “three dimensional memory structure.” Ex. 1005, 9:30-39, 9:56-61, 10:6-13.

302. These dummy word lines are shown in Figure 4G below:

Figure 4G



Ex. 1005, Fig. 4G.

303. Next, Zhao explains that “the dummy word lines are operated in the same manner as unselected word lines.” Ex. 1005, 24:11-13; *see also id.*, 25:31-32. This is consistent with the understanding of a POSITA in terms of how the dummy word lines are operated.

304. As I have explained, Zhao’s “drain side unselected word lines $WLn+x$ ” are supplied with the “pre-charge voltage” ($V_{precharge}$) “to cause pre-charging” during the “pre-charging” “time period.” Ex. 1005, 22:39-49.

305. Because they are operated in the same manner as the unselected word lines, in my opinion a POSITA would have understood that Zhao’s drain-side dummy word lines DD0-DD1 would also be supplied with the same pre-charge voltage $V_{precharge}$.

306. This is the claimed *“top dummy word line pre-pulse signal”*
“appl[ied]” “during the pre-charge period.”

6. Claim 18

307. Claim 18 depends on claim 16 and further requires that:

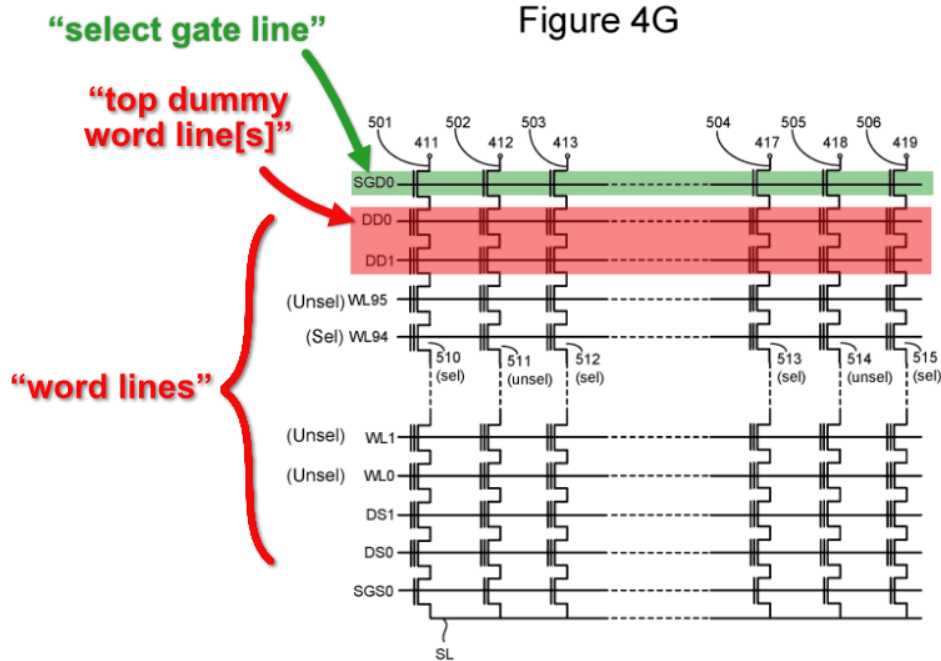
“the top dummy word line is disposed between the third group of the plurality of word lines and the select gate line”

308. This, in my opinion, is taught by Zhao.

309. Zhao’s *“select gate line”* (SGD0) is located at the top of its three-dimensional memory structure.

310. Zhao’s *“top dummy word line”* (DD0-DD1) are located immediately below the *“select gate line.”*

311. The *“third group of the plurality of word lines”* (already programmed source-side word lines WLn-1 and WLn-2) are located below these lines and within the collection of the other *“word lines”* (WL0-WL95):



Ex. 1005, Fig. 4G.

7. Claims 9 and 19

312. Claim 9 depends on claim 1. Claim 19 depends on claim 11. Both claims further require that:

“the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third word line pre-pulse signal are positive”

313. This, in my opinion, is taught by Zhao.

314. In particular, Zhao teaches the use of ***“positive” “pre-pulse signal” “voltage levels.”***

315. Zhao’s ***“third word line pre-pulse signal”*** (Vbypass) can be “~6-10 volts.” Ex. 1005, 22:50-53.

316. Zhao's "*second word line pre-pulse signal*" ($V_{precharge}$) can be " ~ 2 volts." Ex. 1005, 22:43-44.

317. And Zhao's "*first word line pre-pulse signal*" (the voltage applied to the source-side unselected word lines) can be "one or more voltages that are too low to pre-charge." Ex. 1005, 19:23-26; *see also id.*, Fig. 13 (showing the use of various positive pre-charge voltages).

D. Ground 3: Claims 1-9 and 11-19 Are Obvious Over Zhao when Modified in View of Lee

318. In my opinion, a POSITA would have considered both Zhao and Lee to be within the scope of the prior art and highly relevant to the patentability of the '822 patent's claims.

319. In my opinion, when Zhao is modified in view of Lee's teachings and the knowledge possessed by a POSITA, claims 1-9 and 11-19 of the '822 patent are all rendered obvious.

1. Claims 1, 4-7, 9, 11, 14-16, and 18-19

320. As I explained in Ground 2, Zhao itself renders claims 1, 4-7, 9, 11, 14-16, and 18-19 obvious.

321. Again, Zhao applies three different "*pre-pulse signal[s]*" to "*group[s]*" of word lines during a "*pre-charge period.*"

322. Zhao programs its word lines one at a time starting at the source-side of its memory structure and ending at the drain-side. The word line currently being

programmed is “***selected***” and supplied with a pre-charge voltage and later programming voltage (the claimed “***word line signal***”).

323. Vprecharge (Zhao’s “***second***” signal) is applied to the unselected word lines on the drain-side of the selected word line (the “***second***” group).

324. Vbypass (Zhao’s “***third***” signal) is applied to the first two source-side word lines adjacent to the selected word line (the “***third***” group).

325. And a low, non-zero voltage in place of Vss (Zhao’s “***first***” signal) is applied to the remaining source-side word lines (the “***first***” group). (*See supra* discussion of limitations [1.E.1]-[1.E.3].)

326. As repeatedly explained above, Zhao applies the same “Vprecharge” “pre-charge voltage” to all unselected word lines on the drain-side of the currently selected word line during a “pre-charging” “time period.” *E.g.*, Ex. 1005, 22:39-49; *see also id.*, 14:35-39; 16:65-67; 19:9-29; Figs. 7, 13.

327. Zhao explains that this is intended to “[t]o assist in ... boosting” the word lines that are “inhibited from programming.” Ex. 1005, 14:35-40; *see also id.*, 19:17-19 (similarly explaining that “[b]y applying these pre-charge voltages, the voltage of the channel will be raised, which will improve the future boosting”).

328. Lee, however, highlights a potential problem with this approach.

329. According to Lee, during a “typical program operation, during a precharge operation of an unselected memory string, a threshold voltage of a

memory cell is increased by a resistance component between the source select transistor and the drain select transistor.” Ex. 1004, 8:25-29.

330. This “reduce[s]” “the precharge level in a source select side channel” such that “boosting is not effectively generated” and “program disturb occurs.” Ex. 1004, 8:29-32.

331. To account for this effect, Lee teaches that “[t]he word lines coupled to a memory string in a memory block may be grouped ... during a precharge operation of the cell string.” Ex. 1004, 7:58-61; *see also id.*, 2:4-5 (explaining that the various word lines can be “grouped into a plurality of word line groups”).

332. For example, in Figure 4B of Lee, “the control logic may group the thirty-two word lines into four word line groups. Each of [the] first to fourth word line groups Group1 to Group4 includes eight word lines.” Ex. 1004, 9:36-40.

333. Then, according to Lee, “different pre-bias voltages may be applied to the respective groups during a precharge operation of the cell string.” Ex. 1004, 7:58-61; *see also* Abstract (“different pre-bias voltages are applied to the plurality of word lines depending on the relative positions of the word lines”); *see also id.*, 1:62-2:3 (similar).

334. Lee explains that the “pre-bias voltages ... applied to a plurality of word lines” vary by group, and change “depending on the respective position of the word

lines” for purposes of “precharg[ing the] channel regions of the plurality of memory cells” coupled to the word lines. Ex. 1004, 1:65-2:3.

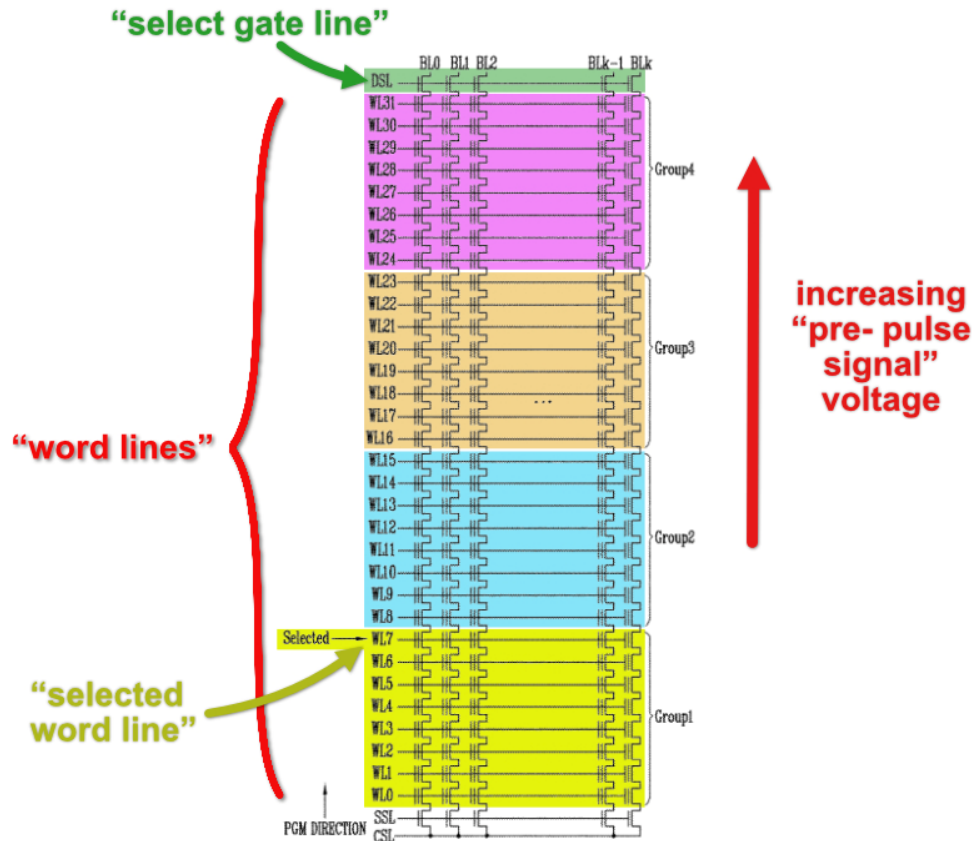
335. The closer “a word line group to which a word line belongs is to the” upper “drain select transistor, the higher a pre-bias voltage ... applied to the word line may be.” Ex. 1004, 8:32-37; *see also id.*, 2:5-9.

336. While different voltages are applied to the drain-side word lines, the selected word line and the source-side word lines may continue to be supplied with a “default value.” Ex. 1004, 2:23-29; 9:36-59.

337. The below demonstrative—based on Figure 4G in Lee—provides an example of this.

338. Lee’s word lines are arranged in four groups (Group1, Group2, Group3, Group4). WL7 is currently selected for programming.

339. Thus, as specified in Lee, Group1 is provided with a “default” voltage during pre-charging. The word lines in Group2, Group3, and Group4, however, are provided with increasingly higher pre-charge voltages as the distance from the selected word line increases:



Ex. 1004, Fig. 4B (modified to show WL7 as selected).

340. Lee goes on to explain that by employing different pre-bias voltages with different groups of word lines, it “offset[s]” the “effects caused by the resistance component between the source select transistor and the drain select transistor” and allows a “uniformly formed” “precharge level” “in the entirety of the cell string.” Ex. 1004, 7:61-62; 8:47-52. This in turn further “mitigate[s] [the] program disturb phenomenon....” *Id.*, 1:52-56; 8:51-52; 15:4-7.

341. While Zhao itself also renders the claims obvious, in my opinion the combination that results from applying this teaching from Lee to Zhao gives rise to

yet another reason why the claimed subject matter of claims 1, 4-7, 9, 11, 14-16, and 18-19 would have been considered obvious by a POSITA.

342. Rather than applying the same Vprecharge voltage to all Zhao's unselected drain-side word lines, Zhao's word lines would be evenly grouped into word line groups following Lee's teachings.

343. Then, following Lee, different, increasing pre-charge voltages would be applied to the different groups of drain-side word lines based on their location relative to the drain select transistor.

344. The following discussion provides one example of how a POSITA would have applied Lee's teachings to Zhao.

345. Zhao explains that its memory may employ "six dummy word line layers DD0, DD1, DS0, SD1, WLDL, WLDU" and "ninety six data word line layers WLL0-WLL95." Ex. 1005, 9:34-39.

346. Following Lee's example, the word lines can be divided into 12 groups of 8: WL0-WL07, WL08-WL15, WL16-WL23, WL24-WL31, WL32-WL39, WL40-WL47, WL48-WL55, WL56-WL63, WL64-WL71, WL72-WL79, WL80-WL87, and WL88-WL95.

347. Zhao's "dummy word lines are operated in the same manner as unselected word lines." Ex. 1005, 24:12-14, 25:31-33. So, the lower dummies

would be grouped with WL0-WL07, while the upper dummies would be grouped with WL88-WL95.

348. In Zhao, the word lines are programmed in order from WL0 to WL95. *See* Ex. 1005, 17:27-29. Zhao also includes an example where “WL50 is the selected word line.” *Id.*, 17:21-25. This selected word line is part of the group that includes WL48-WL55.

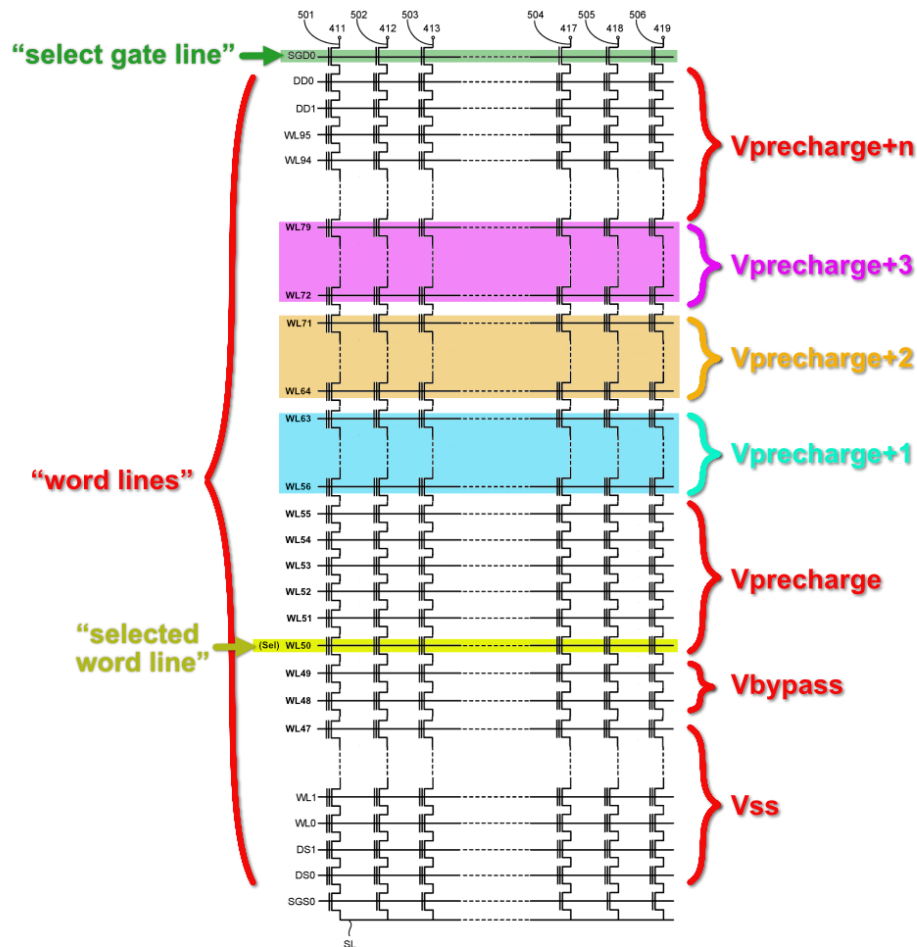
349. Again, Lee teaches that the group containing the “selected” word line can be supplied with “default” pre-charge value. Ex. 1004, 9:36-59.

350. Thus, Zhao’s treatment of the word lines in this group would remain the same: both selected WL50 and drain-side unselected WL51-WL55 would continue to be supplied with $V_{precharge}$ and source-side unselected WL48-WL49 would continue to be supplied with V_{bypass} .

351. But following Lee’s teachings, the other groups of unselected drain-side word lines would now be treated differently during the pre-charge period.

352. WL56-WL63 would now receive a higher pre-charge voltage like $V_{precharge+1}$, WL64-WL71 would receive a still higher pre-charge voltage like $V_{precharge+2}$, WL72-WL79 would receive an even higher pre-charge voltage like $V_{precharge+3}$, and so on until the last group of drain-side word lines, which would receive $V_{precharge+n}$.

353. An example of this is shown in the demonstrative below. Here, Zhao's Figure 4G has been modified to show additional word lines between WL94 and WL1. And color has been added to show one way that the word lines would obviously be grouped:



Ex. 1005, Fig. 4G (modified to show additional word lines between WL 94 and WL1).

354. In my opinion, the collections of drain-side word lines receiving increasingly higher pre-charge voltages correspond to claimed "*groups*": WL56-WL63 are the "*first group*" that receive a "*first ... pre-pulse signal*"

(Vprecharge+1); WL64-WL71 are the “*second group*” that receive a higher “*second ... pre-pulse signal*” (Vprecharge+2); and WL72-WL79 are the “*third group*” that receive an even higher “*third ... pre-pulse signal*” (Vprecharge+3).

355. Moreover, these “*groups*” are now arranged sequentially between the “*selected word line*” (WL50 in this example) and Zhao’s “*top select gate line*” (SGD0).

356. In my opinion, a POSITA would have been motivated to apply Lee’s teachings to Zhao in the manner described above.

357. A POSITA would have recognized that while Zhao addresses some sources of program disturb, it does not fully mitigate the phenomena. For instance, it does not take channel resistance into account.

358. As such, Zhao’s original implementation would result in using a single precharging voltage of Vprecharge on the drain side of the selected memory cell. Due to the channel resistance effect, the full Vprecharge on the bitline would be attenuated greatly at the WL that is closest to the top select gate line.

359. A POSITA also would have recognized that this would have resulted in less effective boosting and increased program disturb.

360. This would have been particularly the case when programming word lines closer to source-side. In such circumstances, the channel length between drain-

side and word line selected for programming would be quite long, resulting in a relatively high channel resistance.

361. A POSITA would have recognized that Lee presents a solution to this problem: it groups word lines and applies different pre-charge voltages to the drain-side unselected word lines to offset the channel resistance effect.

362. A POSITA would have recognized that applying this approach to Zhao would allow it to achieve more uniform pre-charging, better boosting, and reduced program disturb.

363. Additionally, applying unnecessarily high voltage, which could occur if the same voltage is applied to all the drain-side word lines, has the potential to reduce cell endurance. As a result, a POSITA would have understood that by relatively reducing the voltage applied to certain drain-side word lines, cell endurance would be increased.

364. A POSITA also would have recognized that Lee furthers Zhao's design goals. Zhao repeatedly explains that its memory employs various "countermeasures" to "prevent ... program disturb." *E.g.*, Ex. 1005, 2:10-26, 4:7-10, 18:52-59.

365. To avoid program disturb, Zhao seeks to avoid "voltage differential[s]" in "the channel" of an unselected NAND string, during the process of precharging to facilitate the future boosting of the channel to inhibit program disturb. *E.g.*, Ex. 1005, 22:65-23:5.

366. Lee also reduces program disturb and does so by ensuring a uniform channel voltage during the precharging period. Ex. 1004, 7:61-62; 8:47-52.

367. In my opinion, this similarity in purpose of optimizing the biasing conditions during the precharging period also would have motivated a POSITA to apply Lee's teachings to Zhao.

368. Next, a patent's claims are obvious when they simply arrange old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement.

369. This is the case here. A POSITA also would have recognized that the combination of Zhao and Lee would continue to produce the respective benefits discussed in these two references.

370. For instance, the various countermeasures discussed in Zhao, including the application of a higher "Vbypass" pre-charge voltage to source-side unselected word lines, would still be employed to "reduce[] or eliminate the voltage differential between the source side of the channel and the drain side of the channel that may later cause program disturb." Ex. 1005, 22:65-23:12.

371. And use of Lee's teachings would offset the resistance effects on the drain-side of the selected word line for purposes of further reducing program disturb.

372. In my opinion, a POSITA also would have had a reasonable expectation of success.

373. Zhao's memory is already structured and is able to apply different pre-charge voltages to different groups of word lines.

374. Further, Zhao also already expressly contemplates that "one or more pre-charge voltages" can be applied "to the selected word line and drain side unselected word line" during pre-charging. *E.g.*, Ex. 1005, 19:9-17.

375. Given this, a POSITA would have considered the application of Lee to Zhao to amount to nothing more than a straightforward extension of Zhao's existing teachings.

2. Claims 2 and 12

376. Claim 2 depends on claim 1. Claim 12 depends on claim 11. Both claims further require that:

"the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines"

377. This, in my opinion, is obvious in view of Zhao and Lee.

378. As I explained, Lee teaches that the closer "a word line group to which a word line belongs is to the" upper "drain select transistor, the higher a pre-bias voltage ... applied to the word line may be." Ex. 1004, 8:32-37; *see also id.*, 2:5-9.

379. When this teaching is applied to Zhao, a POSITA would have understood this claim to be satisfied.

380. Zhao's "*first*," "*second*," and "*third*" "*group[s] ... of word lines*" (WL56-WL63, WL64-WL71, and WL72-WL79) would be "*disposed in an order of distance from the selected word line*" (WL50).

381. These word line groups also received different pre-pulse signals.

382. WL56-WL63 are the "*first group*" that receive a "*first ... pre-pulse signal*" ($V_{\text{precharge}+1}$); WL64-WL71 are the "*second group*" that receive a higher "*second ... pre-pulse signal*" ($V_{\text{precharge}+2}$); and WL72-WL79 are the "*third group*" that receive an even higher "*third ... pre-pulse signal*" ($V_{\text{precharge}+3}$).

383. Moreover, these "*groups*" of word lines are now arranged sequentially between the "*selected word line*" (WL50 in this example) and Zhao's "*top select gate line*" (SGD0).

3. Claims 3 and 13

384. Claim 3 depends on claim 1. Claim 13 depends on claim 11. Both claims further require that:

"the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line"

385. This, in my opinion, is also obvious in view of Zhao and Lee.

386. As I have already explained, Zhao’s memory includes upper “[d]rain side select layers[,]” including a layer SGD0 shown in Figure 4G. Ex. 1005, 7:64-66; *see also id.*, 9:34-38; 10:19-21; 11:59-60; Fig. 4G.

387. This is the claimed “*select gate line.*” (*See supra* discussion of limitation [1.C].)

388. Because this “*select gate line*” is located at the top of Zhao’s memory, the “*first,*” “*second,*” and “*third*” “*group[s] ... of word lines*” (WL56-WL63, WL64-WL71, and WL72-WL79) are arranged in order between the “*selected word line*” (WL50) and the “*select gate line*” (SGD0) as required.

4. Claims 8 and 17

389. Claim 8 depends on claim 7. Claim 17 depends on claim 16. Both claims further require:

“a voltage level of the top dummy word line pre-pulse signal is greater than that of the third word line pre-pulse signal”

390. This, in my opinion, is also obvious in view of Zhao and Lee.

391. Again, Zhao’s memory includes multiple top dummy lines. *See* Ex. 1005, Fig. 4G (showing top dummy lines DD0-DD1 adjacent to WL95).

392. Zhao also teaches that these “dummy word lines are” to be “operated in the same manner as unselected word lines.” Ex. 1005, 24:12-13; *see also id.*, 25:31-32.

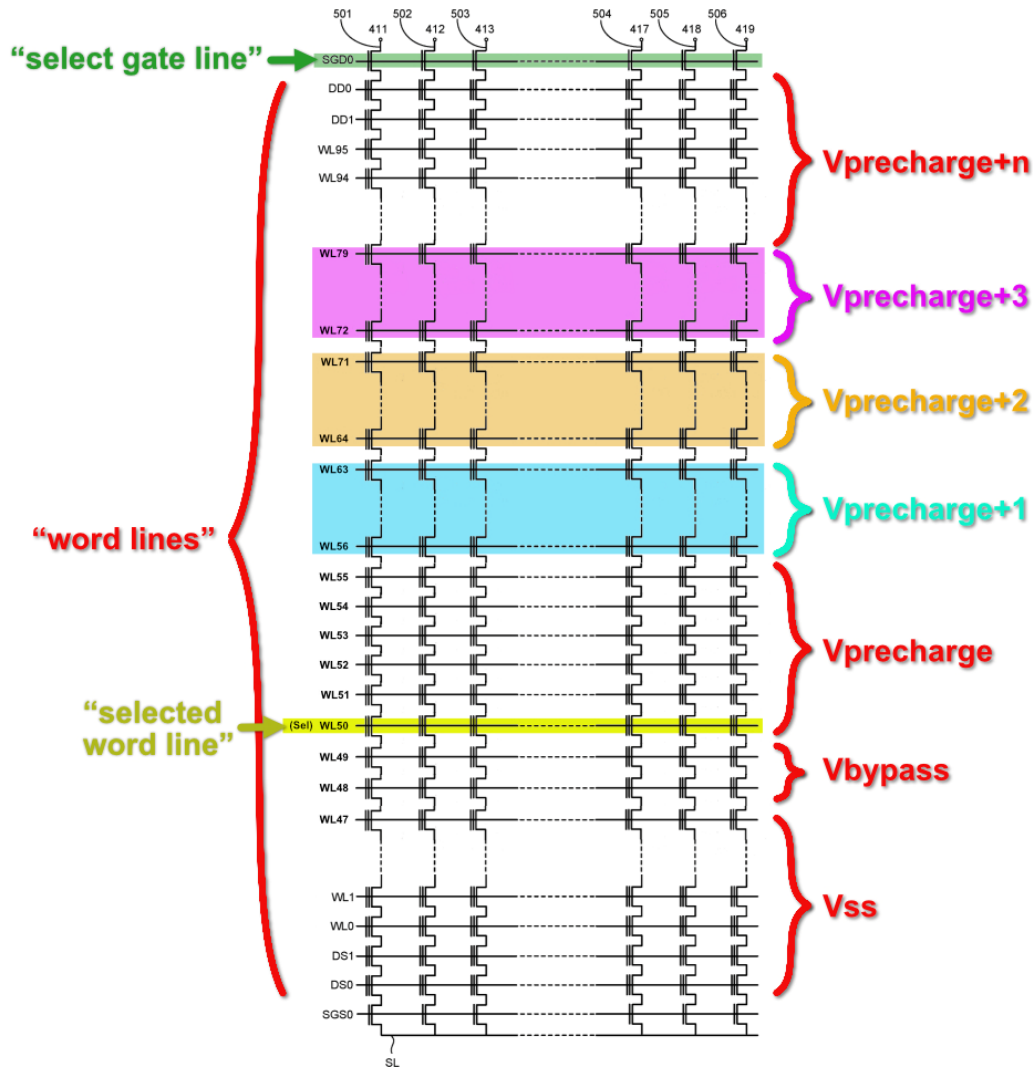
393. As I explained, a POSITA would have understood that Zhao's top dummy word lines should be supplied with the same pre-charging voltage as the adjacent active word lines. *See supra* discussion of claims 7/16 in Ground 2.

394. And following Lee's teachings, Zhao's drain-side unselected word lines will have increasingly higher pre-charge voltages the closer they are to the drain-side select gate. *See supra* Section IX.D.1.

395. Zhao's dummy word lines DD0-DD1 are much closer to the drain-side select gate than its "third" group of word lines (WL72-WL79). *See* Ex. 1005, Fig. 4G.

396. It follows that per Lee, a POSITA would have understood that these dummy word lines in Zhao would be supplied with a "***top dummy word line pre-pulse signal***" with a "***voltage level***" that is higher than that of the "***third word line pre-pulse signal***" supplied to the "***third***" group of word lines.

397. The demonstrative below provides an example. Top dummy lines DD0-DD1 receive $V_{precharge}+n$, which exceeds $V_{precharge}+3$:



Ex. 1005, Fig. 4G (modified to show additional word lines between WL 94 and WL1).

E. Ground 4: Claims 1-7, 9, 11-17, and 18-19 Are Obvious Over Yang

398. In my opinion, a POSITA would have considered Yang to be within the scope of the prior art and highly relevant to the patentability of the '822 patent's claims.

399. In my opinion, when viewed and considered in light of the knowledge possessed by a POSITA, Yang renders claims 1-7, 9, 11-17, and 18-19 of the '822 patent obvious.

1. Independent Claims 1 and 11

[1.Pre]/[11.Pre] “A [method of controlling a memory device, the] memory device, comprising”

400. In my opinion, to the extent this preamble language is limiting, it is taught by Yang.

401. Yang teaches a “memory system 100” with a “memory structure 126.” Ex. 1010, 3:52-61.

402. Yang’s memory structure can be “a three-dimensional memory array of non-volatile memory cells” arranged into “vertical NAND strings.” Ex. 1010, 5:4-14.

403. The memory also employs certain “[t]echniques ... for pre-charging NAND strings during a programming operation.” Ex. 1010, 2:23-25.

[1.A]/[11.A] “a plurality of memory strings”

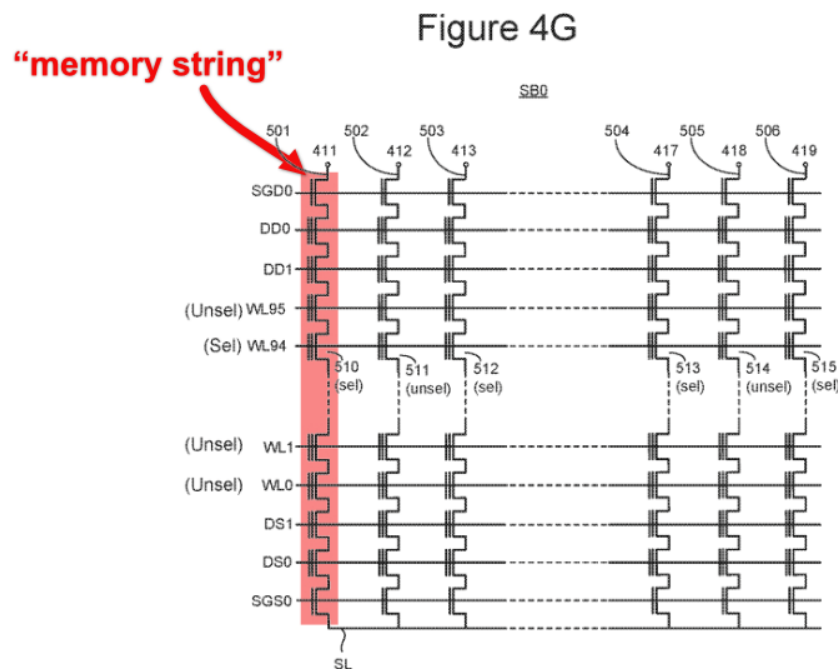
404. In my opinion, Yang teaches a memory with ***“a plurality of memory strings.”***

405. Yang explains that its memory structure, like all NAND flash memory, “has strings of non-volatile memory cells that have a select transistor at each end.

406. Typically, such strings are referred to as NAND strings.” Ex. 1010, 1:16-19; *see also id.*, 2:24-30 (explaining that “[a] NAND string comprises a number of memory cells connected in series”).

407. Figure 4G of Yang, which is reproduced in annotated form below, depicts an example “sub-block” of Yang’s memory. Ex. 1010, 14:35. While the block “will have thousands of NAND strings[,]” Yang explains that “six NAND strings 501, 502, 503, 504, 505, and 506” are depicted. Ex. 1010, 14:38-42.

408. One example string is annotated red:



Ex. 1010, Fig. 4G.

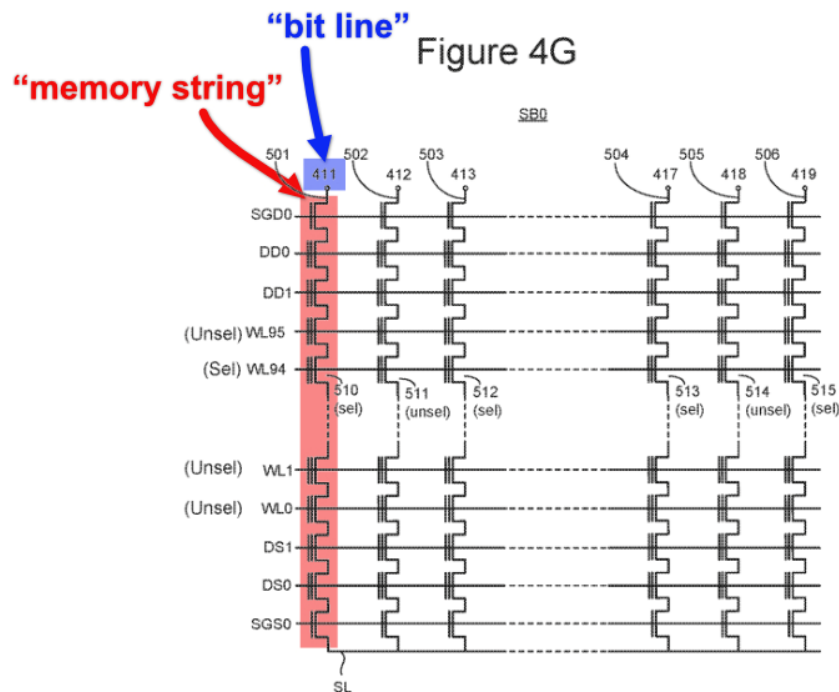
[1.B]/[11.B] “a bit line connected to a first memory string of the plurality of memory strings”

409. In my opinion, Yang teaches the claimed **“bit line connected to a first memory string.”**

410. According to Yang, each “NAND string” in its memory structure “may have a drain side select transistor at one end that connects the string to a bit line.”
Ex. 1010, 1:19-20; *see also id.*, 2:23-30 (similar).

411. Figure 4G “depicts a set of bit lines ... 411, 412, 413, 414, ... 419.”
Ex. 1010, 11:18-28; 14:14-20.

412. As shown in the below annotated version of this figure, blue annotated bit line 411 is connected to NAND string 501:



Ex. 1010, Fig. 4G.

[1.C]/[11.C] “a select gate line connected to the first memory string of the plurality of memory strings”

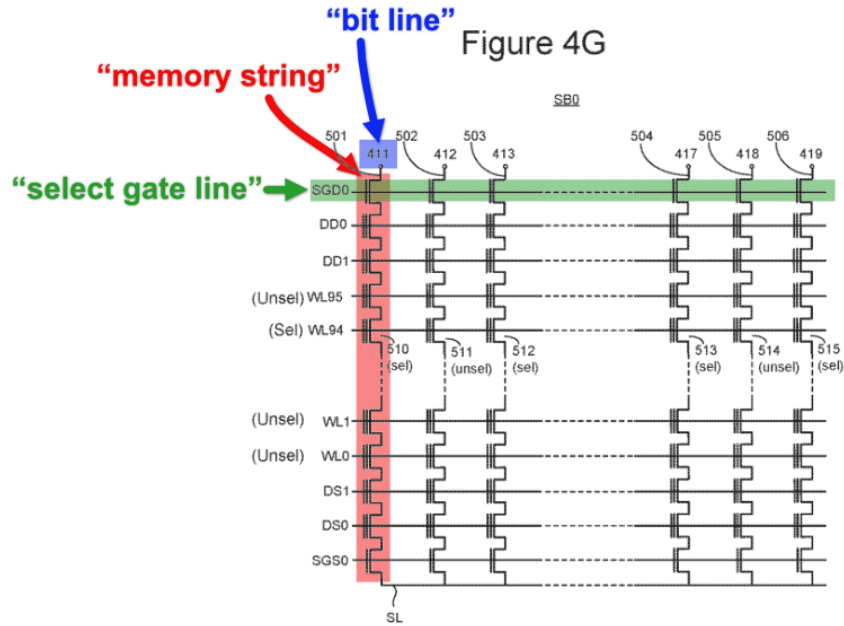
413. In my opinion, Yang teaches a ***“select gate line connected to the first memory string.”***

414. According to Yang, its memory structure includes multiple “select layers.” Ex. 1010, 8:67-9:2.

415. This includes an upper “drain-side SG layers” that are “associated with the drain side of a set of NAND strings.” Ex. 1010, 13:1-5.

416. Yang explains that the “[d]rain side selection lines” “are used to determine which ... NAND strings connect to the associated bit lines.” Ex. 1010, 14:20-25.

417. Drain-side select gate layer SGD0 is annotated green in Figure 4G below:



Ex. 1010, Fig. 4G.

[1.D]/[11.D] “a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string”

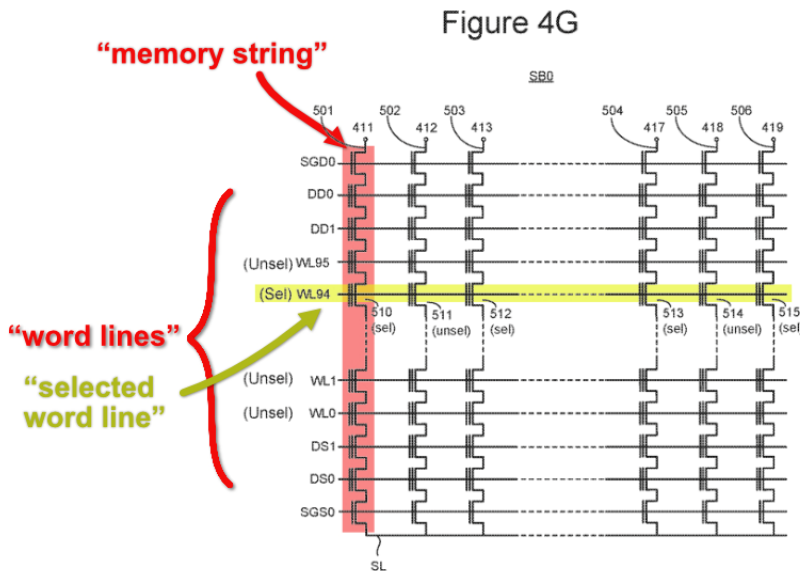
418. In my opinion, Yang teaches a memory with *“a plurality of word lines”* that are *“connected to the first memory string.”*

419. Yang explains that in one example, its memory structure includes “96 data word line layers” and “6 dummy word line layers.” Ex. 1010, 8:67-9:2.

420. And as shown in Figure 4G, “WL0-WL95 run[] across the entire sub-block” and connect to the various “NAND strings.” Ex. 1010, 14:35-42.

421. Yang also explains that certain of its “word line[s]” are “selected” during memory operation “to receive programming.” Ex. 1010, 2:35-38; *see also id.*, 14:50-54.

16. This is the claimed “*selected word line*”:



Ex. 1010, Fig. 4G.

[1.E] “a control circuit configured to” / [11.E] “the method comprising”

423. In my opinion, Yang teaches a “*control circuit*” that performs the claimed “*method.*”

424. Yang includes “[c]ontrol circuitry 110” with, among other components, “a power control circuit 116.” Ex. 1010, 4:14-18.

425. The “[p]ower control circuit 116 controls the power and voltages applied to the word lines, bit lines, and select lines during memory operations.” Ex. 1010, 4:25-27.

426. This allows Yang’s control circuitry to engage in “programming” of “NAND strings.” Ex. 1010, 16:31-37.

[11.E.0] “applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period”

[1.E.1]/[11.E.1] “apply[ing] a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period”

[1.E.2]/[11.E.2] “apply[ing] a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and”

[1.E.3]/[11.E.3] “apply[ing] a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period”

427. Yang renders all of this obvious: a POSITA would have understood that Yang organizes its memory’s word lines into the various ***“group[s]”*** and applies the different ***“signal[s]”*** these limitations require.

428. To start, Yang teaches applying ***“pre-pulse signals”*** to its memory structure’s ***“word lines”*** ***“during a pre-charge period.”***

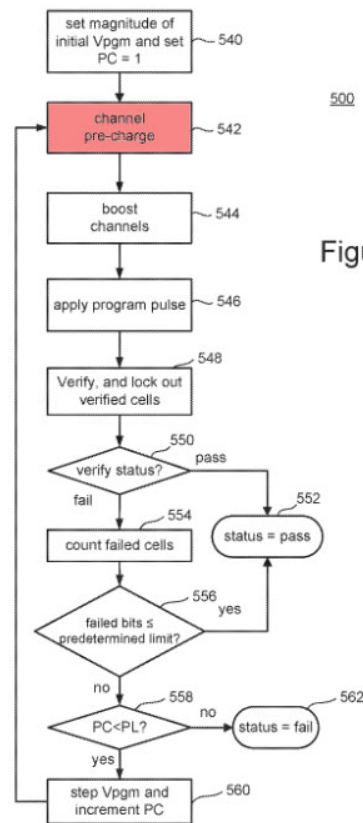
429. According to Yang, its “programming operation has a channel pre-charge phase.” Ex. 1010, 2:42-46. This “pre-charge phase” occurs before a later “program phase.” *Id.*, 21:40-50.

430. During the “pre-charge phase[,]” “channels of unselected NAND strings ... are pre-charged to a desired voltage level.” Ex. 1010, 21:46-50.

431. Then, during the “program phase ... selected memory cells connected to the selected word line are programmed” while “unselected memory cells

connected to the selected word line are inhibited from programming.” Ex. 1010, 21:50-54.

432. Figure 5, reproduced below, shows this initial “pre-charge” step 542, along with the later step 546 where “a program pulse” is applied. Ex. 1010, 17:7-41.



Ex. 1010, Fig. 5.

433. Next, Yang also renders obvious the application of different “*pre-pulse signals*” to different “*group[s]*” of its word lines.

434. Yang explains that “[i]f the channel of the unselected NAND string is not adequately pre-charged during the pre-charge phase, the NAND channel may fail to boost to a sufficient voltage during the programming phase to adequately prevent program disturb.” Ex. 1010, 2:58-62.

435. According to Yang, the string may not be adequately pre-charged if, for instance, there is “valid data” in memory cells above or below a cell currently selected for programming. Ex. 1010, 3:20-27.

436. To avoid this problem, Yang applies different pre-charge voltages to different sets of word lines. This includes an “overdrive voltage,” “bypass voltage[,]” and “dummy voltage.” Ex. 1010, 3:28-39 (referencing application of an “overdrive voltage” and different “bypass voltage”); 24:1-46 (referencing “bypass,” “overdrive,” and “dummy” pre-charge voltages); *see also id.*, 9:65-10:18 (similarly referencing application of both an “overdrive voltage” and “bypass voltage” to different portions of the memory during a “pre-charge phase”); 17:24-28 (similar). The applied voltages are in the form of “pulses.” *Id.*, 16:50-53.

437. Yang also explains which of the various word lines in its memory structure receive the different pre-charge voltages.

438. Yang’s word lines are arranged in “different vertical sub-blocks VSB0, VSB1, VSB2 that are treated as separate units for erase/programming purposes....” Ex. 1010, 9:49-61, 12:22-23.

439. Each “sub-block” includes multiple active word lines. For instance, when the memory structure includes 96 total word lines, “VBS0” can include “WLL0-WLL31,” “VSB1” can include “WLL32-WLL63[,]” and “VBS2” can include “WLL64-WLL95.” Ex. 1010, 12:23-29.

440. There are “[d]ummy word line layer[s]” between the sub-blocks. Ex. 1010, 12:32-35.

441. Yang applies pre-charge voltages to these various word lines depending on both the sub-block where the line is located and its current program state.

442. In one example in Yang, “[o]ne of the word lines (WL7) in vertical sub-block VSB1 is selected for programming.” Ex. 1010, 25:18-19.

443. Then, the “over-drive voltage” (V_{pre_OD}) is applied to the “programmed data word lines” in the “upper vertical sub-block VSB2” of the memory structure. Ex. 1010, 22:4-11; 24:28-33.

444. The “bypass voltage” (V_{bypass}) is applied to the “word lines in VSB2 that are not programmed” and all the “data word lines” in VSB1 and VSB0. Ex. 1010, 22:31-37, 24:11-17.

445. The “dummy pre-charge voltage” (V_{pre_dmy}) is “applied to all dummy word lines” in the same pre-charge period. Ex. 1010, 24:18-27. This is shown in multiple figures.

446. Figure 8B is a “timing diagram” showing when Yang applies different pre-charge voltage pulses to its word lines, dummy lines, select gates, bit lines, and other lines. *See* Ex. 1010, 23:20-23. “[T]imes t1-t4 correspond to ... a pre-charge phase.” Ex. 1010, 23:23-25.

447. Figure 8C shows the arrangement of the various word lines, dummy lines, and sub-blocks, along with the different pre-charge voltages applied to the different lines. *See* Ex. 1010, 25:29-33.

448. While Figure 8C depicts each sub-block as including only a single dummy word line layer and six data word line layers, Yang explains that “[m]ore or less ... layers can also be used.” Ex. 1010, 9:2-5. Thus, in my opinion, a POSITA would have understood that Yang also obviously teaches embodiments where more data and dummy word lines are used. *See, e.g., id.*, Fig. 4C (showing 96 data word lines, and 2 layers of upper dummy word lines.)

449. As summarized by the below annotated versions of these figures, Yang teaches what claims 1 and 11 require.

450. A “**word line signal**” (Vbypass, yellow in Figure 8B) is applied to “**the selected word line**” (WL7, yellow in Figure 8C).

451. A “**first word line pre-pulse signal**” (Vbypass, blue in Figure 8B) is applied to “**a first group ... of word lines**” (non-programmed WL8-WL11 in VBS1, blue in Figure 8C).

452. A “*second word line pre-pulse signal*” (Vpre_dmy, orange in Figure 8B) is applied to “*a second group ... of word lines*” (the dummy word lines between VBS1 and VBS2, orange in Figure 8C).

453. And a ***“third word line pre-pulse signal”*** (Vpre_OD, purple in Figure 8B) is applied to ***“a third group ... of word lines”*** (previously programmed WL12-WL14 in VSB2, purple in Figure 8C).

454. All of these signals are applied during the same “*pre-charge period*” (t1-t3):

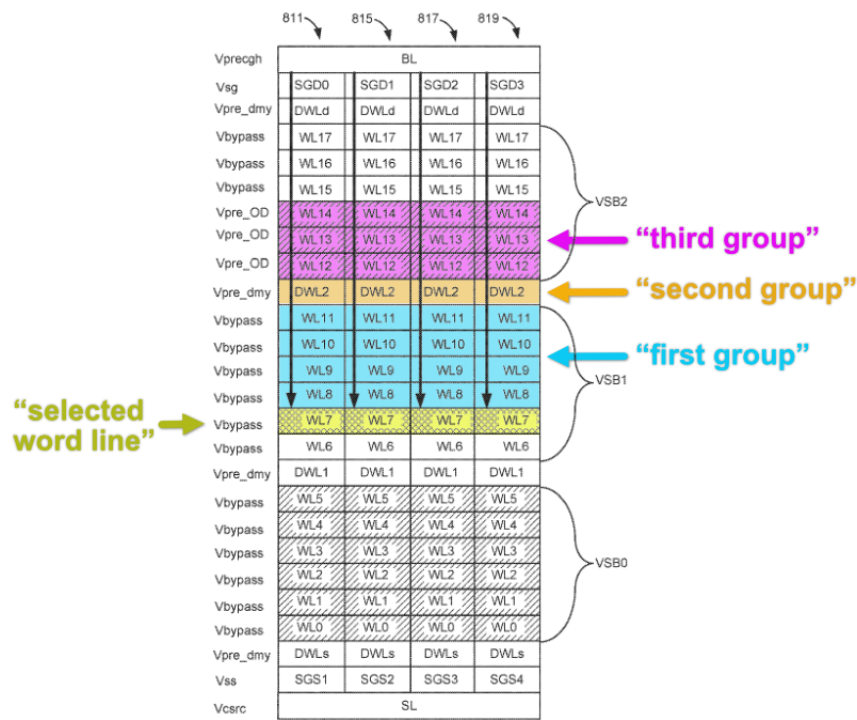
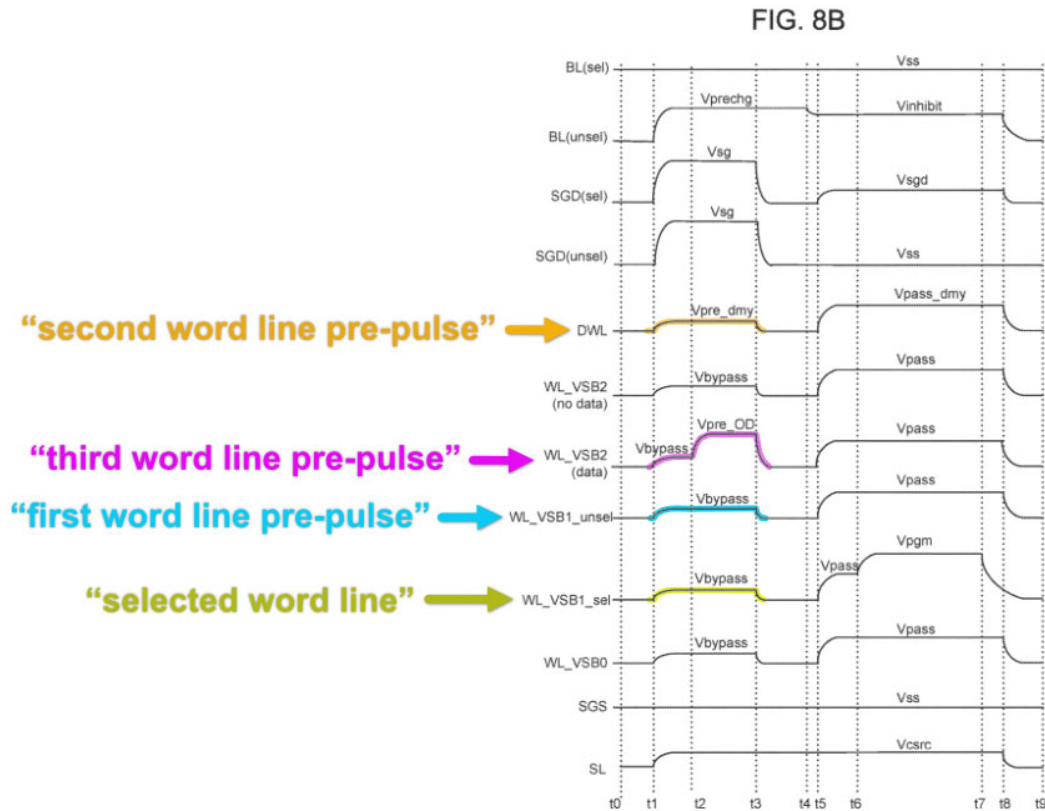


FIG. 8C

Ex. 1010, Fig. 8C.



Ex. 1010, Fig. 8B.

[1.E.4]/[11.E.4] “wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal”

455. This is also, in my opinion, obvious in view of Yang.

456. While Yang does not provide numerical examples for all of its different pre-charge voltages, in my opinion, a POSITA would nonetheless understand Yang to render this limitation obvious.

457. Again, Yang applies three different voltage pulses to its various word lines during a pre-charge period: a **“first ... pre-pulse signal”** (Vbypass), a

“second ... pre-pulse signal” (Vpre_dmy), and a *“third ... pre-pulse signal”* (Vpre_OD). (*See supra* discussion of limits [1.E.1]-[1.E.3].)

458. Yang explains that “overdrive voltage Vpre_OD” is a high voltage “above all the data states” of the memory cells. Ex. 1010, 20:53-55.

459. The “bypass voltage” Vbypass can be a low voltage: it can be lower than all the various memory cell read states, and is only required to be higher than Vev (the “voltage level to test whether a memory cell has been properly erased”). and not higher than at least that of the Vv7. Ex. 1010, 19:23-44; 20:64-21:5. A POSITA would have recognized that a typical range of Vev and Vv7 would obviously have been, for instance, a non-zero voltage between 0V to 4V. *See, e.g.*, Ex. 1006, 117 (providing example “program state” voltages for a “MLC” of approximately 0.5V, 1.75V, and 3V). Given this, a POSITA would have known that Vbypass would be somewhere below 5V.

460. The “dummy pre-charge voltage” Vpre_dmy can be an intermediate voltage like 5V that is lower than Vpre_OD. Ex. 1010, 24:18-27; *see also id.*, Fig. 6.

2. Claims 2 and 12

461. Claim 2 depends on claim 1. Claim 12 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines”

462. This, in my opinion, is taught by Yang.

463. As shown in annotated Figure 8C below, Yang’s ***“first group”*** (WL8-WL11, blue), ***“second group”*** (DWL2, orange), and ***“third group”*** (WL12-WL14, purple) of ***“word lines”*** are ***“disposed in an order distance”*** from the ***“selected word line”*** (WL7, yellow):

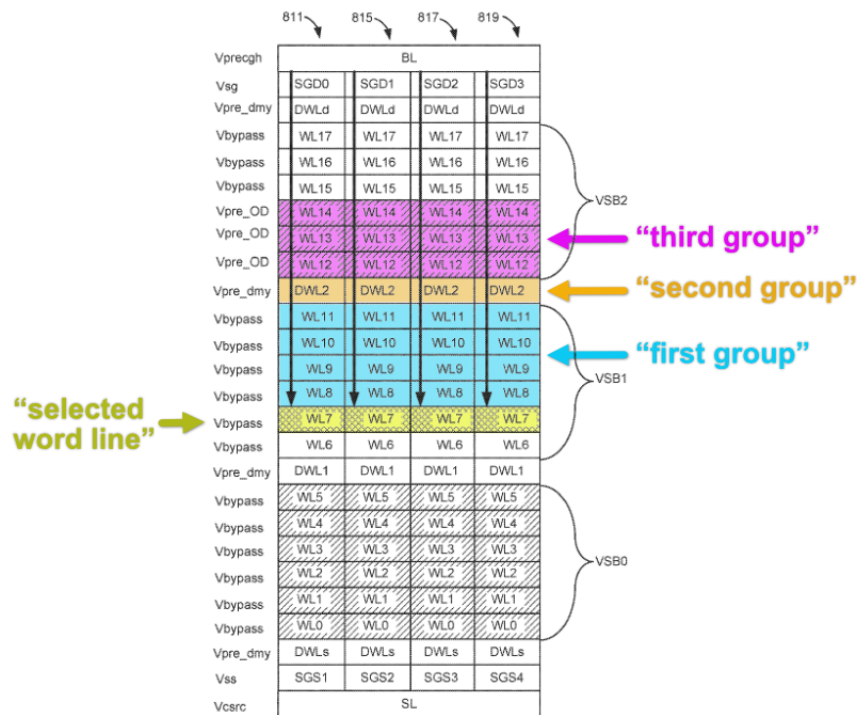


FIG. 8C

Ex. 1010, Fig. 8C.

3. Claims 3 and 13

464. Claim 3 depends on claim 1. Claim 13 depends on claim 11. Both claims further require that:

“the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line”

465. This, in my opinion, is also taught by Yang.

466. As shown in annotated Figure 8C below, Yang’s ***“first group”*** (WL8-WL11, blue), ***“second group”*** (DWL2, orange), and ***“third group”*** (WL12-WL14, purple) of ***“word lines”*** are ***“disposed adjacent to”*** the ***“selected word line”*** (WL7, yellow) and between this word line and the ***“select gate line”*** (SGD0-SGD3, green) in the manner this claim requires:

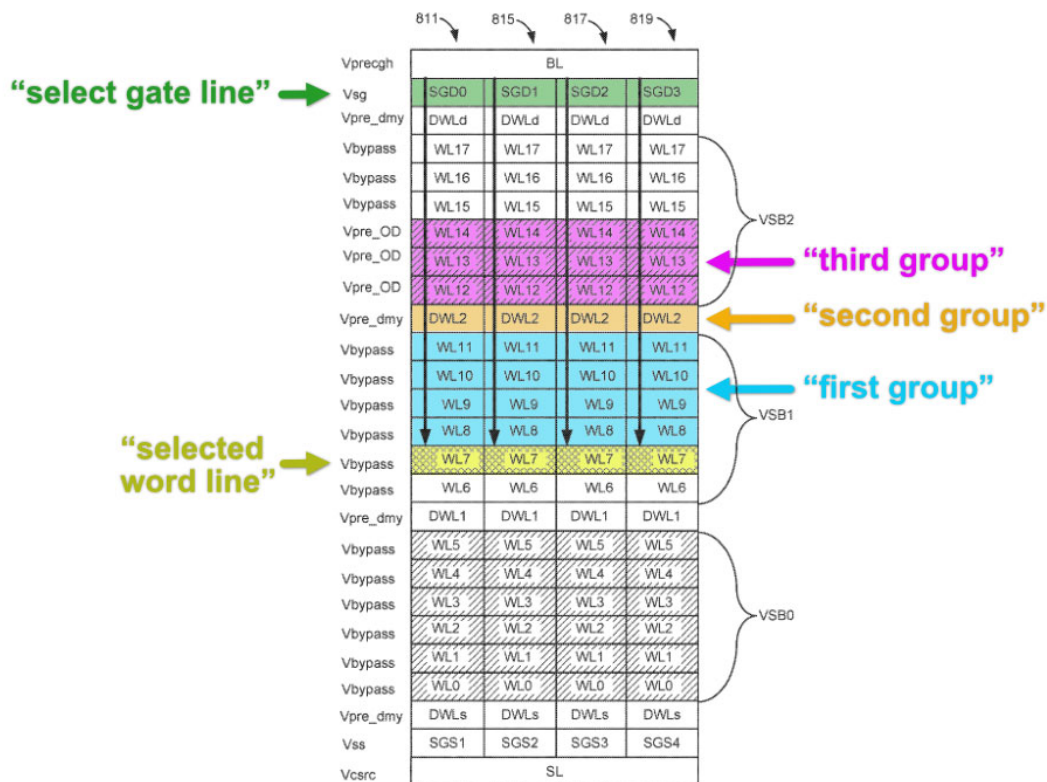


FIG. 8C

Ex. 1010, Fig. 8C.

4. Claims 4 and 14

467. Claim 4 depends on claim 1. Claim 14 depends on claim 11. Both claims similarly require:

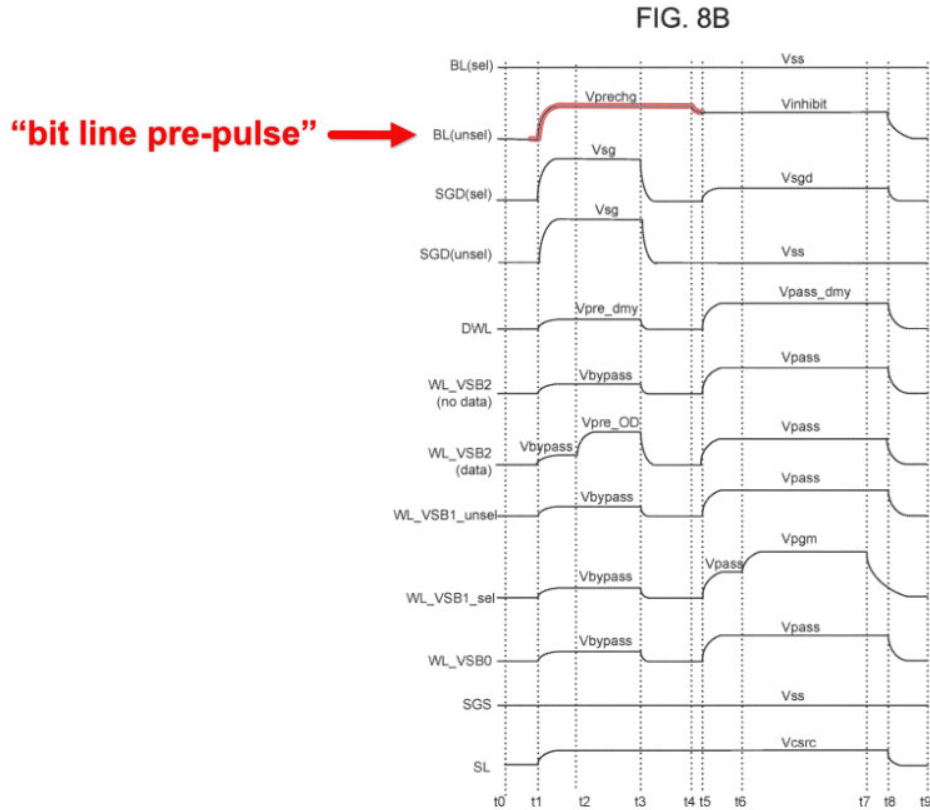
that “the control circuit is configured to apply” (claim 4) or “applying” (claim 14) “a bit line pre-pulse signal to the bit line during the pre-charge period”

468. This, in my opinion, is taught by Yang.

469. Yang’s “*control circuit*” applies the claimed “*bit line pre-pulse signal*” “*during the pre-charge period.*”

470. According to Yang, “during a pre-charge phase of a programming operation[,]” its controller applies “a pre-charge voltage” “to a bit line (BL) connected to an unselected NAND string.” Ex. 1010, 9:65-10:5; *see also id.*, 21:61-64 (a “pre-charge voltage is applied to a bit line connected to a drain side select transistor at one end of the unselected NAND string”); 23:37-44 (during the pre-charge period “the voltage on the unselected bit line (BL(unsel)) is raised towards the precharge voltage (Vprechg).”

471. This is shown in Figure 8B:



Ex. 1010, Fig. 8B.

5. Claims 5 and 15

472. Claim 5 depends on claim 4. Claim 15 depends on claim 14. Both claims further require that:

“the first memory string is an unselected memory string, and the bit line is an unselected bit line”

473. This, in my opinion, is taught by Yang.

474. Yang explains that during its “pre-charge phase[,]” “channels of unselected NAND strings ... are pre-charged to a desired voltage level.” Ex. 1010, 21:46-50.

475. As part of this, pre-charge voltages are applied to the “unselected bit line[s.]” Ex. 1010, 23:37-44.

6. Claim 6

476. Claim 6 depends on claim 1 and further requires that:

“the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines”

477. This, in my opinion, is taught by Yang for the same reasons explained in connection with limitation [11.E.0]: the “bypass voltage” (V_{bypass}) is applied to the selected word line during pre-charging. Ex. 1010, 22:31-37, 24:11-17; Figs 8B-C; *see also supra* discussion of limit [11.E.0].

7. Claims 7 and 16

478. Claim 7 depends on claim 1. Claim 16 depends on claim 11. Both claims similarly require that:

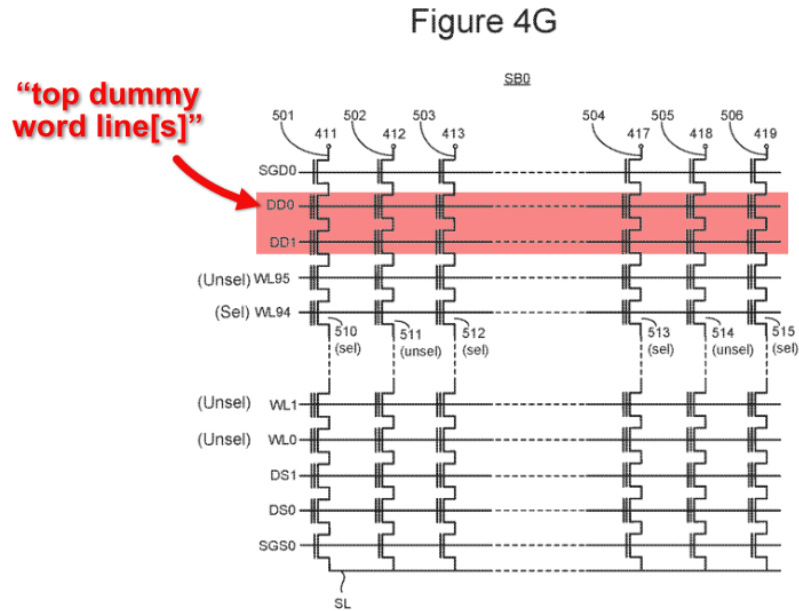
“[the control circuit is configured to] apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the pre-charge period”

479. In my opinion, Yang’s memory structure includes ***“a top dummy word line.”***

480. Yang’s memory includes multiple “dummy word lines.” Ex. 1010, 8:67-9:2.

481. These includes “drain side dummy word line layers” that are located “[b]elow the SGD layers.” Ex. 1010, 13:8-9.

482. Example dummy word line layers DD0-DD1 are annotated red in Figure 4G below:



Ex. 1010, Fig. 4G; *see also id.*, Fig. 8C (similarly showing a top dummy word line layer DWLd).

483. Yang also teaches application of a *“a top dummy word line pre-pulse”* to its dummy word lines during the *“pre-charge period.”*

484. In particular, a “dummy pre-charge voltage” (Vpre_dmy) is “applied to all dummy word lines” during pre-charge period t1-t3. Ex. 1010, 24:18-27; Fig. 8B-C.

8. Claim 18

485. Claim 18 depends on claim 16 and further requires that:

487. As shown in annotated Figure 8C below, Yang’s “*top dummy word line*” (DWLd, red) is “*between*” its “*third group of ... word lines*” (WL12-WL14, purple) and the “*select gate line*” (SGD0-SGD3):



Micron Ex. 1003, p. 122
Micron v. YMTC
IPR2024-00795

9. Claims 9 and 19

488. Claim 9 depends on claim 1. Claim 19 depends on claim 11. Both claims further require that:

“the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third word line pre-pulse signal are positive”

489. This, in my opinion, is taught by Yang.

490. All of the pre-pulse voltages employed by Yang are positive. *See, e.g.,* Ex. 1010, Fig. 8B.

F. Secondary Considerations of Non-Obviousness

491. Based on my review of the '822 patent's prosecution history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims.

492. I am not separately aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like. Instead, as discussed above, it is my opinion that the subject matter embraced by the '822 patent's claims was known in and obvious over the prior art. Moreover, it is also my opinion the teachings of the prior art would have been expected to successfully function as or be usable with working NAND memory devices.

Petition for *Inter Partes* Review of U.S. Patent No. 11,501,822
Declaration of David Kuan-Yu Liu, Ph.D.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: April 9th, 2024

Location: Fremont, California

Signature: 
David Kuan-Yu Liu