

**Reliability and NVSM
Reliability****6.0. INTRODUCTION**

Reliability is a measure of a product's performance consistency. A reasonable quantitative definition of reliability is the probability that the product item remains effective in performing its designated function as required in an operating environment for a specific period of time. However, at the component level, in view of the necessary high measure of reliability to support system product reliability, the reliability metric is often given by the device's rate of failure to meet performance requirements within the expected (or specified) operating environment. For example, to specify component reliability, we may define a failure rate unit (FIT), in which

$$1 \text{ Failure UnIT} \equiv 1 \text{ FIT} \equiv 1 \text{ failure}/10^9 \text{ device-hours}$$

A commonly accepted set of assumptions, generally found to be representative of the failure behavior of electronic components and other complex systems, has been systematized as the reliability "bathtub" curve shown in Fig. 6.1.

The early failure or the so-called infant mortality period represents high failure rates attributable to manufacturing defects. Screening, testing, and burn-in procedures implemented by the manufacturer and user alike are traditional primary means of quality control and assurance with which enhancement of reliability is attempted. Fig. 6.2 illustrates the expected impact of burn-in on the failure rate during infant mortality.

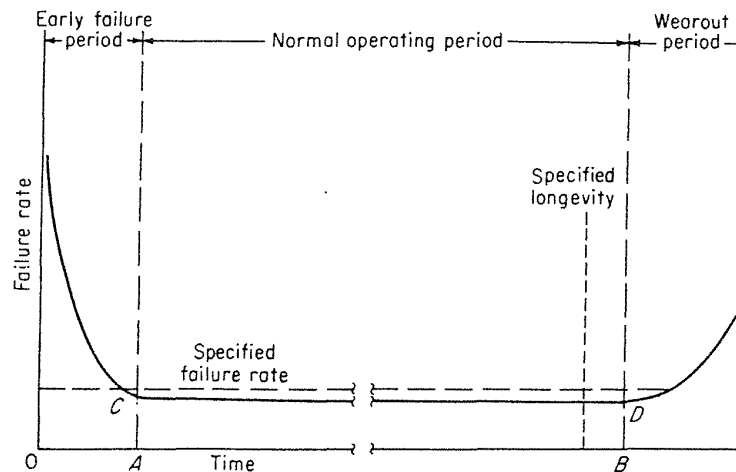


Figure 6.1 The reliability lifetime “bathtub” curve (after Grant and Leavenworth [6.1] from “Reliability of Military Electronics Equipment [6.2]).

The failure rate attained during the normal operating period defines quantitatively the quality of the component. Proper design, with sufficient design margins to exclude failure modes from the operating regime of the component, ensures a low failure rate during the product lifetime. Similarly, good engineering design practices increase the longevity of the component and the postponement of the onset of the wearout period or end-of-life of the product.

An alternative view of reliability is presented in Fig. 6.3 in which the utility of reliability, effected through design and manufacturing, is emphasized. Reliability is designed into a product through the elimination of failure modes in the use of the component, the incorporation of margins in the component circuits, the application of redundancy, fault tolerance, and other reliability enhancement techniques, and the implementation and monitoring of the manufacturing processes to minimize the introduction of latent defects to the manufactured component. Thus, reliability is incorporated at all levels of design, in the manufacturing process, in the device, in the circuit, and in the system component design. Reliability is assured through screen

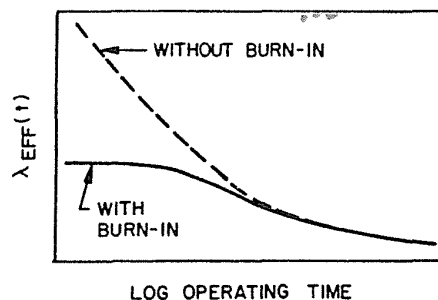


Figure 6.2 Failure rate versus time in use for devices with and without burn-in (after Sze [6.3]).

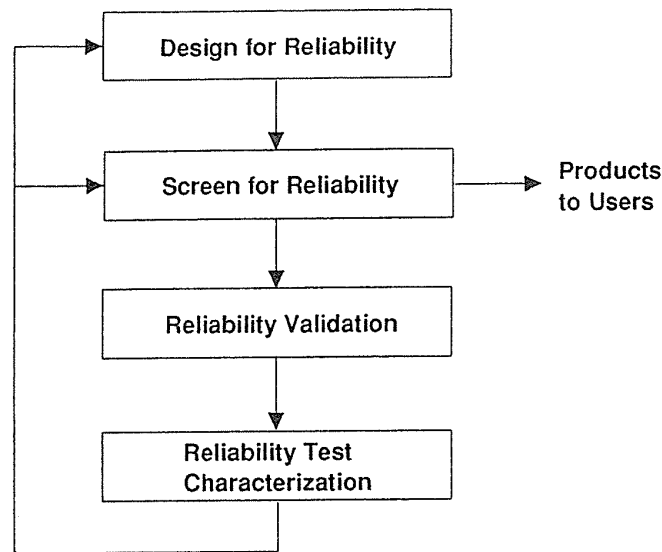


Figure 6.3 An alternative view of product reliability.

testing, sampling for failures, life testing, and application of field use data. In addition, reliability test characterization is performed to provide for design and screening methodology.

NVSM is a subset of MOS/semiconductor integrated circuit technology. Therefore, NVSM reliability failure considerations include all those of MOS devices. It should also incorporate the NVSM unique definition of reliability failure: “the retrieval of incorrect data from memory as it is accessed within the specified operating conditions” [6.4]. This definition of reliability is inclusive of NVSM failures, such as retention failures, because of reduced operating margins, as well as failures due to catastrophic endurance wearout. This chapter discusses unique NVSM reliability issues. For completeness, Table 6.1 is provided to summarize some of the known semiconductor integrated circuit (IC) reliability failure mechanisms that are not unique to NVSM [6.5]. As a result of NVSM’s inherently higher operating electric fields, if not properly considered, some of the known MOS failure mechanisms can unnecessarily become prominent contributors to device failures. Examples of some applicable failure modes include contaminants in dielectrics, electromigration of interconnect metallization, as well as dielectric breakdowns from high-field effects.

Not unlike other VLSI semiconductor technologies, NVSM reliability has a significant impact on yield, and consequently, on cost. A high infant mortality failure rate often manifests itself as a low yield in the process line. Worse yet, a high infant mortality failure rate leads to a high return rate as failures occurring within the product warranty period. A more complex relationship between reliability, yield, and cost can be exemplified by the consideration of incorporating testability and redundancy to improve reliability, which may increase circuit com-

TABLE 6.1 TIME-DEPENDENT FAILURE MECHANISMS IN SILICON SEMICONDUCTOR DEVICES (AFTER SZE AND PECK [6.5] PER [6.3]).

Device association	Failure mechanism	Relevant factors	Accelerating factors	Acceleration (E_a = apparent activation energy for temp.)
Silicon oxide and silicon-silicon oxide interface	Surface charge accumulation	Mobile ions, V, T	T	$E_a = 1.0\text{--}1.05\text{ eV}$ (depends upon ion density)
	Dielectric breakdown	$\mathcal{E}$, T	$\mathcal{E}$, T	$E_a = 0.2\text{--}1.0\text{ eV } \mathcal{E}^\gamma$, $\gamma(T) = 1\text{--}4.4$
	Charge injection	$\mathcal{E}$, T, Q_f	$\mathcal{E}$, T	$E_a = 1.3\text{ eV}$ (slow trapping) $E_a \approx -1\text{ eV}$ (hot electron injection)
Metallization	Electromigration	T, J, A, gradients of T and J, grain size	T, J	$E_a = 0.5\text{--}1.2\text{ eV}$ J^γ , $\gamma(T) = 1\text{--}4$
	Corrosion (chemical, galvanic, electrolytic)	Contamination, H, V, T	H, V, T	Strong H effect $E_a \approx 0.3\text{--}1.1\text{ eV}$ (for electrolysis) V may have thresholds
	Contact degradation	T, metals, impurities	Varied	
Bonds and other mechanical interfaces	Intermetallic growth	T, impurities, bond strength	T	Al-Au: $E_a = 1.0\text{--}1.05\text{ eV}$
	Fatigue	Bond strength, temperature cycling	Temp. extremes in cycling	
Hermeticity	Seal leaks	Pressure differential, atmosphere	Pressure	

Note: V—voltage; T—temperature; $\mathcal{E}$ —electric field; J—current density; A—area; H—humidity.

plexity and die size. Both of these factors determine the yield of a semiconductor process, as well as being direct contributors to product cost. Yet, as has been verified by many effective early product introductions, use of redundancy and fault-tolerant techniques can affect yield and cost performance competitiveness in an otherwise noneconomical process. This important complex relationship between reliability and yield is noted herein, for the purpose of encouraging future research studies and analyses.

6.1. PRIMARY RELIABILITY CONCERNS

Both floating gate and floating trap NVSM devices are dependent on the integrity of the memory device dielectrics for reliable device performance. Failures in the gate dielectrics contribute to both retention and endurance failures. In addition, since NVSM devices are MOS integrated circuit devices, they suffer reliability failures in a similar fashion as MOS devices. Furthermore, because of the high electric field needed to write or erase NVSM devices, higher than typical MOS integrated circuit V_{DD} voltages are usually routed through some of the integrated circuit elements. Therefore, NVSM IC devices typically can be expected to experience higher electrical field stresses under normal operating conditions. These devices would exhibit higher than typical failure rates if the design was not appropriately executed with those considerations carefully incorporated in the manufacturing process, device structure, or circuit configuration.

Table 6.2 lists the common EPROM failure mechanisms that have been observed [6.6]. Of the many failure modes listed, a significant number are related to typical MOS IC device failure mechanisms. The table also shows the region of the reliability lifetime “bathtub” curve affected by the failure mechanism, as well as the corresponding thermal activation energy and the primary detection methods for failure. In Sections 6.1.1 and 6.1.2, detailed discussions on failures uniquely related

TABLE 6.2 EPROM FAILURE MECHANISMS (AFTER ROSENBERG [6.6]).

Mode	Lifetime Region Affected	Thermal Activation Energy (eV)	Primary Detection Method
Slow trapping	Wearout	1.0	High-temp bias
Surface charge	Wearout	0.5–1.0	High-temp bias
Contamination	Infant/wearout	1.0–1.4	High-temp bias
Polarization	Wearout	1.0	High-temp bias
Electromigration	Wearout	1.0	High-temp operating life
Microcracks	Random	—	Temperature cycling
Contacts	Wearout/infant	—	High-temp operating life
Silicon defects	Infant/random	0.3	High-temp operating life
Oxide breakdown/leakage	Infant/random	0.3	High-temp operating life
Hot-electron injection	Wearout	—	Low-temp operating life
Fabrication defects	Infant	—	High-temp burn-in
Charge loss	Infant/random/wearout	1.4	High-temp storage
Oxide-hopping conduction	Infant/random	0.6	High-temp storage/burn-in

to NVSM are presented. It suffices here to note that, in the case of the EPROM, for example, charge loss, oxide trapping, and hot-electron injection are primarily responsible for EPROM device failures. Charge traps typically result in EPROM wearout failures. For EEPROMs (E²PROMs) and flash E²PROMs, the buildup leading to end-of-lifetime dependent dielectric breakdown and dielectric charge trapping contribute similarly to retention and endurance reliability failures. For floating trap NVSM devices such as the MNOS, SONOS, and other equivalent memory devices, the behavior of traps in the gate dielectric is the primary contributor to the reliability performance of NVSM devices vis-à-vis their retention and endurance features.

Not unnoticed by many device technologists is a possibly significant difference in reliability failure related to pinhole defects between floating gate and floating trap NVSM devices. A conductive pinhole defect in the thin oxide dielectric of the floating gate NVSM device destroys the charge storage capability of the floating electrode. On the other hand, such a defect may not result in catastrophic failure of the floating trap NVSM device. Therefore, it is reasonable to assume, given that other factors are equivalent, that the reliability of floating trap NVSM devices can be expected to be superior to floating gate NVSM devices.

6.1.1 Physics of Traps

In the context of NVSM, we will review the physics of traps. Traps are the storage sites for MNOS-type floating trap NVSM devices. They constitute the very means that lead to reliability failures in EEPROM-type floating gate NVSM devices. Therefore, the fundamental understanding of traps is very important to the NVSM technology.

6.1.1.1 Charge and Traps in SiO₂. Charge and traps in SiO₂ have been studied extensively because of their technological importance in MOS technology. Following Deal and the recommendations of an IEEE-sponsored committee [6.7], the charges in the Si-SiO₂ and SiO₂ systems, applicable also to the floating gate NVSM technology, are categorized below and illustrated in Fig. 6.4. They are:

1. Interface trapped charge, located at the Si-SiO₂ interface, in electrical communication with the silicon, readily charged or discharged dependent on the surface potential. They are attributed to intrinsic dangling bonds at the interface, other structural or oxidation-induced defects, metal impurities, and other physically induced defects, such as by radiation. In the literature, this category of charge is also known as surface states, fast states, interface states, Q_{ss}, and so on.
2. Fixed oxide charge, located in the oxide in close proximity to the interface, not in direct electrical communication with the silicon, and primarily positively charged. The charge originates with the oxidation process in which ionized silicon is not satisfied with an oxygen bond.
3. Oxide trapped charge, in the bulk of the oxide, with either negative or positive polarity, dependent on the nature of the charge trapped. Particularly in the case

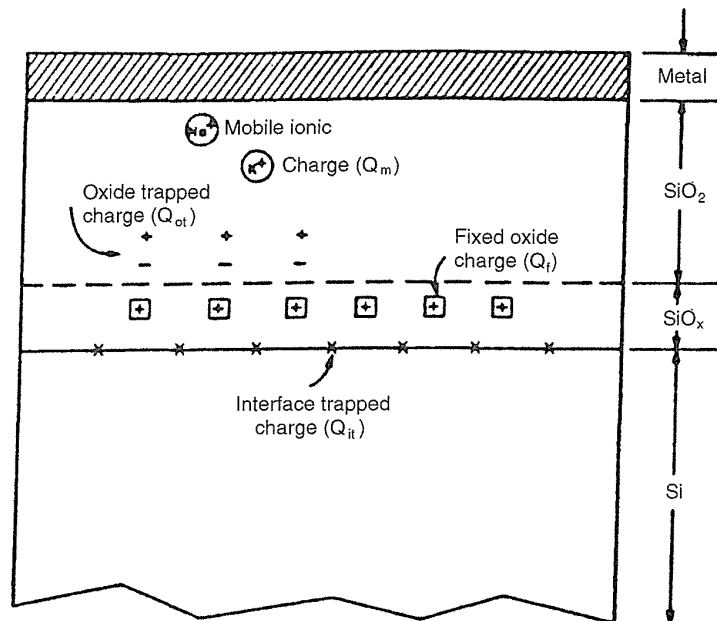


Figure 6.4 Terminology for charges associated with thermally oxidized silicon (after Deal [6.7]).

of floating gate NVSM, these trapped charges are dependent on the endurance cycling of the device, with a reliability failure mode dependent on the fluence or the cumulative transport of charge through the oxide.

4. Mobile ionic charge, primarily due to ionic contaminants, such as Na^+ , and to a lesser degree, ions such as Li^+ and K^+ .

Table 6.3 summarizes the recommended symbols for these categories' charge. The interface trap density further reflects the quantification of the interface trapped charges both spatially (per unit area) and energetically (per eV in the energy band gap of SiO_2).

The primary failure mechanism of the oxide pertains to dielectric breakdown due to high field/current stressing, modifying the physical properties dominated by the traps, and trapped charge in the oxide. Conceptually, the breakdown process can be viewed in stages: (1) localized high-field regions form as a result of charge trapping, (2) these localized regions cause positive feedback effects and trapping of more charge, and (3) eventually, the local high-field region generates sufficient current density to result in dielectric failure due to electrical runaway processes. A physical model that clearly describes all the various known factors of breakdown in SiO_2 is still being pursued by researchers in the field. The following discussion presents a generic model suitable for elaboration on some of the physical concepts for a better understanding of NVSM reliability [6.8].

TABLE 6.3 OXIDE CHARGES (AFTER DEAL [6.7]).

Interface trapped charge	Q_{it}, N_{it}
Fixed oxide charge	Q_f, N_f
Oxide trapped charge	Q_{ot}, N_{ot}
Mobile ionic charge	Q_m, N_m
Interface trap density	D_{it} (number/cm ² · eV)

Notes: Q = Net effective charge per unit area
N = Net number of charges per unit area

Under high-field bias, electrons are injected from the substrate silicon into the gate dielectric, SiO₂, via Fowler–Nordheim tunneling. (Hot holes injected from the gate into the oxide are also possible.) In the oxide, some of the electrons can gain sufficient energy to cause impact-ionization, creating hole-electron pairs. Some of the holes, instead of being driven by the channel field to be collected by the substrate silicon, are trapped in localized weak spots, resulting in localized field enhancement and further increasing the Fowler–Nordheim tunnel current. A positive regenerative process is initiated, leading to dielectric breakdown or endurance failure. Figure 6.5 illustrates the process just described with energy band diagrams.

In the case of thin gate MOS and tunnel oxide NVSM devices, it has been shown experimentally that the endurance of the oxide is dependent on the time required for the total hole fluence, Q_p, to reach some critical value, where

$$Q_p \propto J \alpha t \tag{6.1}$$

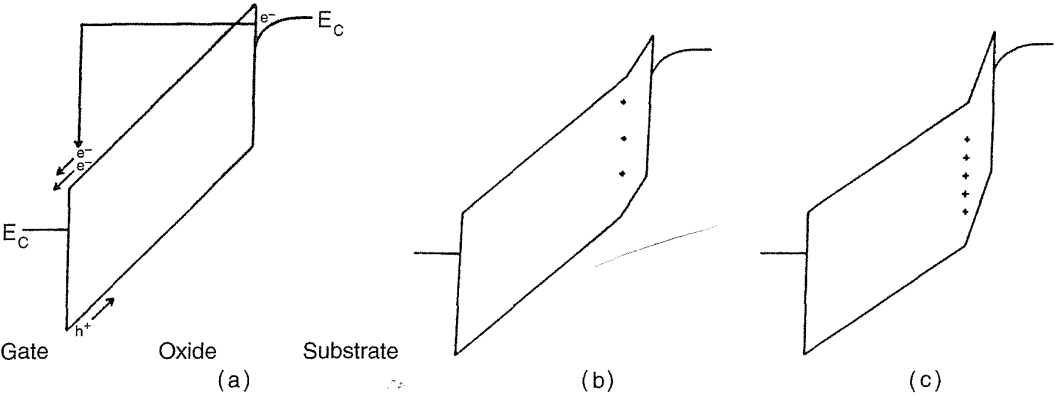


Figure 6.5 Breakdown in SiO₂ due to high-field current injection. (a) Electron injection from the cathode results in some of the electrons gaining sufficient energy to create hole-electron pairs in the SiO₂. Some of the generated holes are driven to the cathode. (b) Hole trapping in local areas at the cathode increases the cathode field. (c) Localized high densities of trapped holes result in the formation of localized high-field/current density regions, causing positive feedback eventually resulting in breakdown (after Chen et al. [6.8]).

in which

$(J \propto \exp -(B/E_{ox}) = \text{the Fowler-Nordheim tunnel current density}$

$\alpha \propto \exp -(H/E_{ox}) = \text{the hole-generation coefficient}$

and thus, t_{BD} , time to endurance breakdown, can be given as

$$t_{BD} \propto \exp(B + H)/E_{ox} \quad (6.2)$$

As seen from this equation, a linear relationship exists between $\log t_{BD}$ and $1/E_{ox}$, as is illustrated in Fig. 6.6, which compares the model with experimental data.

From this equation, the “electric field acceleration factor,” β , can be derived as

$$\beta \equiv \frac{d[\log(t_{BD})]}{d E_{ox}} = \frac{-(B + H)}{2.30 \cdot E_{ox}^2} \left[\frac{\text{decade}}{\text{mv/cm}} \right] \quad (6.3)$$

which predicts, from the model, that β is proportional to $1/E_{ox}^2$. Figure 6.7 compares the model-based β factor with results reported in the literature, showing the agreement between experiment and theory.

The β factor, though widely used to extrapolate oxide lifetime from accelerated stress testing, exhibits a wide spread in measured values and thus requires more accurate modeling to take into consideration the defect-related, statistical features of failure. A simple concept of “effective oxide thinning,” ΔX_{ox} , describing a defect density as D (ΔX_{ox}), has been introduced [6.9], which yields

$$t_{BD} \propto e^{(B+H)(X_{ox}-\Delta X_{ox})/V_{ox}} \quad (6.4)$$

where the ΔX_{ox} term, with a corresponding defect density D (ΔX_{ox}), represents effects such as localized weak spots, surface aspirates (regions of effective high E_{ox}), and localized defects where increased trap generation occurs. Figure 6.8 illustrates the effect of ΔX_{ox} on β and concurrently references the calculated β factor to experimental results.

The temperature dependency of both the acceleration factor and the effective activation energy for oxide breakdown can be obtained from Eq. (6.2) by substituting

$$B + H = (B_0 + H_0)(c + E_a/kT) \quad (6.5)$$

from which

$$\beta \propto 1/T \quad (6.6)$$

can be derived.

The inverse β and temperature relationship was found to be representative of oxides of different thicknesses, as seen in Fig. 6.9.

The temperature dependency of the effective activation energy for oxide failure can be derived from Eqs. (6.2) and (6.5) as

$$\begin{aligned} E_{a\text{eff}} &\equiv k \frac{d \ln(t_{BD})}{d (1/T)} \\ &= \frac{(B_0 + H_0)(X_{ox} - \Delta X_{ox})E_a}{V_{ox}} - E_b \end{aligned} \quad (6.7)$$

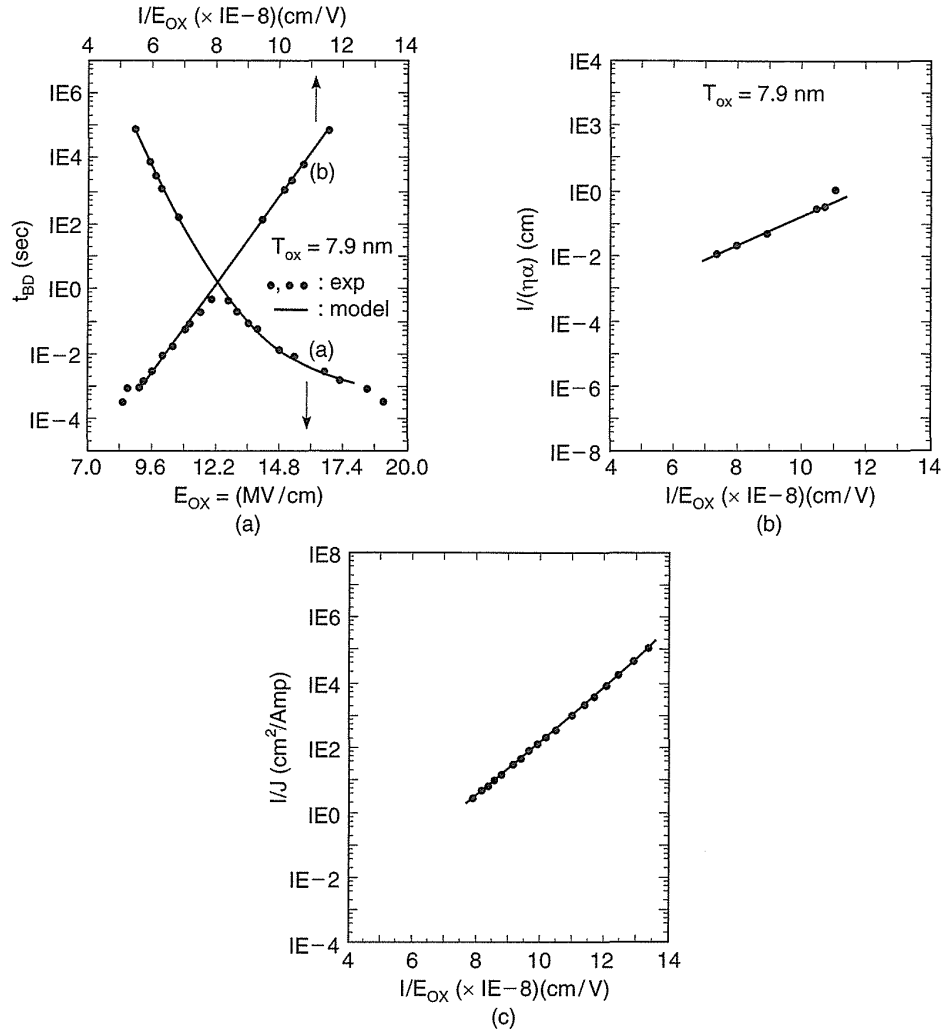


Figure 6.6 Experimental data on dielectric breakdown. (a) Log t_{BD} versus E_{ox} and $1/E_{ox}$ for the 7.9 nm tunneling oxide. Log t_{BD} follows a linear relationship with $1/E_{ox}$, not E_{ox} as hitherto assumed. (b) Log $1/\alpha$ versus $1/E_{ox}$ for the 7.9 nm tunneling oxide. The slope corresponds to the H factor of α ($\alpha = \alpha_0 e^{-H/E}$). (c) Log $1/J_{total}$ versus $1/E_{ox}$ for the same tunneling oxide. The slope in the figure is approximately equal to the B factor of the Fowler-Nordheim current ($J = AE^2 e^{-B/E}$) (after Chen et al. [6.8]).

An alternative and frequently used model for time-dependent dielectric breakdown of silicon dioxide is given as follows [6.11–6.13]:

$$t_f(F) = A \exp \left\{ \beta [V_{BO}(F) - V] + \frac{\Delta H}{kT} \right\} \quad (6.8)$$

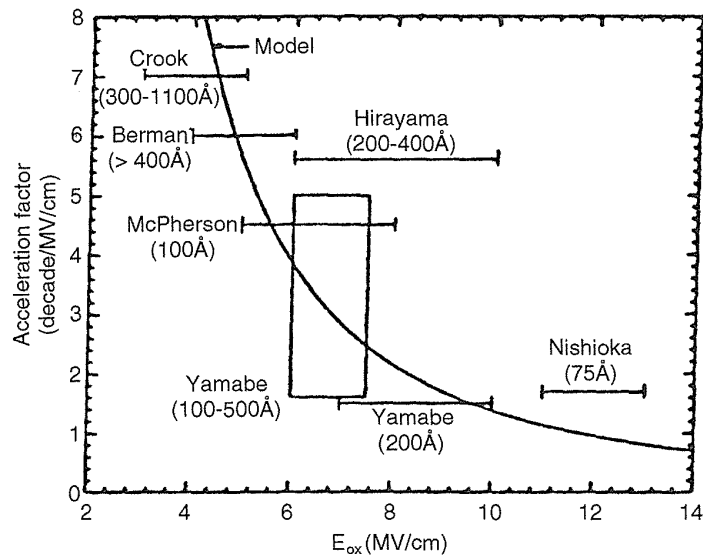


Figure 6.7 Theoretical field acceleration factor compared with reported results. The solid curve is derived from $\log(t_{BD})(B+H)/E_{ox}$ (after Lee et al. [6.9]).

where $t_f(F)$ = time-to-fail associated with the population percent F
 β = a voltage parameter
 $V_{BO}(F)$ = a limiting breakdown voltage
 ΔH = the activation energy of the failure mechanism
 A = a pre-exponential term that has the units of time

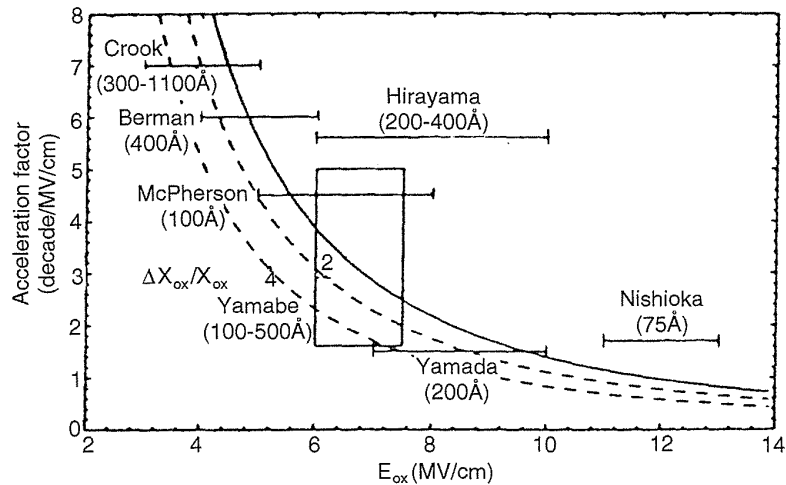


Figure 6.8 Field acceleration factor β versus E_{ox} as a function of $\Delta X_{ox}/X_{ox}$. β decreases with increasing ΔX_{ox} (after Lee et al. [6.9]).

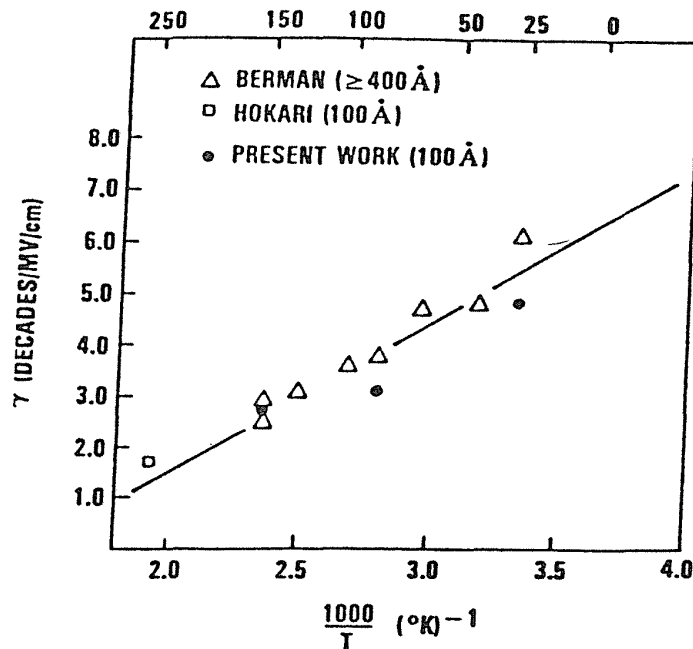


Figure 6.9 Dependence of the electric-field acceleration parameter on temperature (after McPherson and Baglee [6.10]).

This model is primarily derived empirically and predicts a linear dependency on the electric field, even though it could be argued that, for high electric fields typically experienced by EEPROM erase/write operations, both experimental data and theory point to the reciprocal field model. Contradictory data found in recent literature [6.14] indicate the need for caution in the use of one generic model for failure prediction. Table 6.4 illustrates the orders of magnitude difference in calculated reliability parameters in time-dependent dielectric breakdown data for 210 Å oxide films, based on differences of the two models in question.

6.1.1.2 Charge and Traps in Si_3N_4 . In floating trap NVSM devices such as MNOS and its various derivatives, including SNOS, MONOS, and SONOS, the spatially distributed traps in the silicon nitride replace the floating gate as the storage element, or more correctly, medium. Unlike the study of traps in SiO_2 , there has been much less in the literature regarding the nature of traps in Si_3N_4 .

A microscopic physical model of Si_3N_4 traps has been proposed [6.15] based on known attributes of traps in silicon nitride, including:

1. Electron and hole traps as being equal in number
2. Traps spatially distributed in the entire dielectric

TABLE 6.4 LINEAR AND RECIPROCAL MODEL ACCELERATION PARAMETERS AND FIT RATES FOR HIGH- AND LOW-FIELD REGIONS (AFTER BOYKO AND GERLACH [6.14]).

Temp. (C)	Model, Regime	Acceleration Parameter*			FIT Rate		
		Median	Lower 95%	Upper 95%	Median	Lower 95%	Upper 95%
150	Linear, high-E	1.7	1.3	2.2	140,000	63,000	320,000
	Linear, low-E	5.4	4.4	6.4	250	140	430
	Recip., high-E	84	62	105	.006	.00006	.5
	Recip., low-E	83	68	99	.04	.02	.09
60	Linear, high-E	3.2	2.5	3.8	1300	610	2900
	Linear, low-E	4.7	3.0	6.4	100	43	240
	Recip., high-E	150	82	180	< 1e-6		
	Recip., low-E	94	61	130	.0006	.0001	.004

*Units Linear = decades/MV/cm Reciprocal = decades/cm/MV

3. A large electron capture cross section for electron traps, and similarly, a large capture cross section for hole traps, indicating that both types of traps are charged
4. Spectroscopic evidence of excess silicon, equivalently dangling Si bonds, as well as Si–H and N–H bonds in the microscopic model of silicon nitride

In the model, the memory traps are attributed to unsatisfied silicon bonds, or dangling bonds, originating from silicon nitride film formation (see Fig. 6.10). A silicon dangling bond that has an electron in it is electrically neutral. The energy level for this electron is inside the energy gap of Si, at an energy D_0 , slightly below the midgap position, as illustrated by the electron energy diagram of a MNOS structure in Fig. 6.11. However, this neutral configuration of the dangling bond is not the lowest energy state. Instead, either of the two charge configurations—one with the dangling bond possessing two electrons, or the other, possessing none (i.e., two holes)—is lower in energy. Hence, the system of Si dangling bonds cooperatively

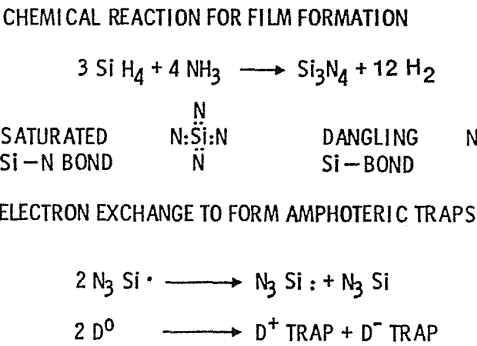


Figure 6.10 Microscopic model of memory traps (after Hsia and Ngai [6.15]).

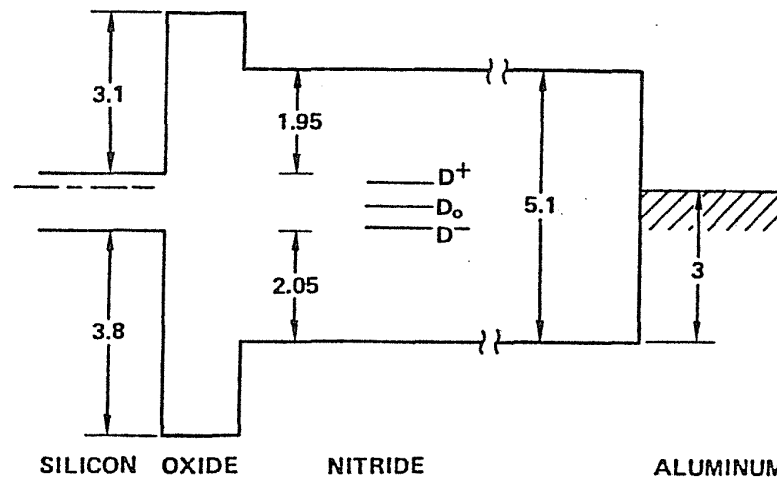


Figure 6.11 Electron-energy diagram of MNOS structure (all energy values in eV) (after Hsia and Ngai [6.15]).

lowers its total energy by electron charge transfer from one dangling bond to the other. Such charge transfers are accompanied by bond distortions. The result is the formation of positively and negatively charged dangling bonds replacing the original neutral ones. The negatively charged dangling bond state D^- , with two electrons, lies in energy below D_0 , near the Si valence band edge. D^- is a hole memory trap. The positively charged dangling bond state D^+ , with two holes, lies in energy above D_0 , near the Si conduction band edge. D^+ is an electron memory trap. If the initial charge state of the silicon nitride film is neutral, then we must have equal numbers of D^+ and D^- states compensating each other, consistent with empirical results [6.16, 6.17]. Since these memory traps, D^+ and D^- , are charged, the large observed capture cross section of $5 \times 10^{-13} \text{ cm}^2$ for both holes and electrons is congruous with the model [6.16, 6.17]. The trap center is amphoteric; that is, the dangling bond can possess either of the two charge states, D^+ or D^- .

Subsequent empirical evaluation of electron and hole injection and trapping in MONOS NVSM devices has provided evidence of the amphoteric nature of silicon nitride charge traps [6.18].

Figure 6.12 depicts n-channel MNOS memory operations as represented by the energy diagram of the nitride–oxide–silicon system. In the write operation, an electron, available at the Si–SiO₂ interface, tunnels through the SiO₂ barrier to the nitride conduction band. The electron then drops to the D^+ level, converting D^+ to D^0 . By a similar process, D^0 is converted to D^- in accordance with



To erase, one electron in the D^- state tunnels across to the silicon conduction band via the large tunnel barrier comprised of the spatial silicon nitride region and the silicon dioxide barrier. Then, the remaining electron in the D^0 state similarly

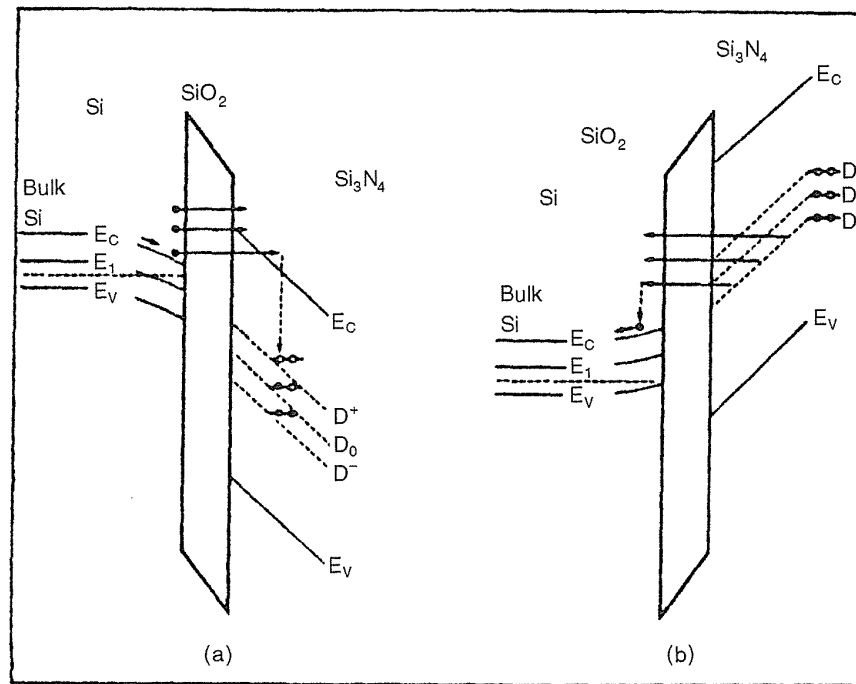


Figure 6.12 Energy-level diagrams describing MNOS memory operations: (a) write; (b) erase (after Hsia and Ngai [6.19]).

tunnels across the barrier. The asymmetry of the tunnel barrier leads to asymmetry in the memory erase write operation.

For p-channel MONOS NVSM devices, hole injection from the semiconductor has been demonstrated as the dominant mechanism for writing, and the traps in the nitride can undergo a similar reaction:



For a given injection condition, one of the capture processes involves a charged state and is characterized by a larger capture cross section compared with the capture process by the neutral state, D^0 .

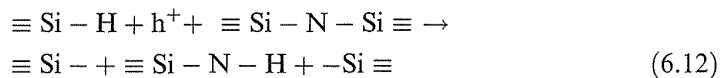
Silicon nitride, prepared by chemical vapor deposition from ammonia-silane mixtures at elevated temperatures, has a significant concentration of hydrogen. The hydrogen contained in the film is bonded to either silicon or nitrogen. The hydrogen content increases with decreasing deposition temperature, indicating more complete Si-N bonding in the nitride at higher deposition temperatures [6.17, 6.20]. Results [6.21] from combining nuclear reaction and infrared absorption studies have indicated hydrogen concentrations of 8.1 and 6.5% for deposition temperatures of 750°C (with NH_3/SiH_4 ratio of 200:1) and 900°C (with NH_3/SiH_4 ratio of 300:1), respectively.

It is expected that there will be more complete Si–N bonding at higher growth temperatures and larger NH_3/SiH_4 ratios. Indeed, for films deposited at 900°C and 950°C, no Si–H bonds are observed [6.21] and H is bonded only to N. A chemical vapor deposition (CVD) nitride grown at a relatively low temperature (around 600°C) will have more incomplete silicon–nitrogen bonding. In addition to existing silicon dangling bonds D^+ and D^- , there are also the hydrogen-decorated silicon dangling bonds, that is, Si–H bonds. Si–H is not a strong bond. Upon annealing [6.17,6.21] at a higher temperature, say 950°C, the Si–H bonds in the low-temperature film will break and H can diffuse out of the film. Indeed, it has been shown that annealing [6.21] a 750°C film for five hours at 950°C removed 50% of H bonded to N and 65% of H bonded to Si. The process of high-temperature annealing of a film grown at a low temperature has the effect of increasing the Si and N dangling bonds, the strained Si–N and Si–Si bonds, as well as D^+ and D^- . All these species can be candidates for memory traps in the silicon nitride bulk. Si dangling bonds and strained Si–Si bonds have been identified [6.22] as the origins of interface states and charges at the Si– SiO_2 interface of Si MOS devices.

On erase/write cycling the MNOS device, electrons or holes of large energy are injected into the nitride. For example, the injected hole makes the following electro-mechanical reactions possible:



and



Here, $\equiv \text{Si}$ denotes the Si bonded to three N atoms, and $\equiv \text{Si}-$ denotes a Si dangling bond, D^0 , which will eventually lower its energy by conversion to D^+ and D^- . Thus, memory traps are created by Si–H bond breaking, and in addition, cause the movement of stored charges away from the silicon.

The microscopic model of memory traps can be considered in connection with a macroscopic model to predict the logarithmic retention behavior of the MNOS devices, as well as increased dielectric conduction after endurance exercise [6.23].

The spatially distributed traps can be viewed as localized regions of the memory dielectric. With high-field stress, delocalization increases, with structural adjustment shifting the local energy levels in the regions of highest applied field, increasing the partial coherence of the nearby site waveforms, and thus enhancing site-to-site (as trap-to-trap) carrier mobility between these sites. With continuing erase/write or endurance cycling, intersections of delocalized states can result in the formation of a “weak link” network in the dielectric, which anticipates the device failing in the end-of-life “conductive” mode.

The macroscopic model can be considered as the generalization of the Boltzmann Principle via-à-vis the localized trap sites. The number of sites, N, available for activation in the range E to E + dE can be written as

$$N = f(E)dE \quad (6.13)$$

If we assume that the activation of N for a generalized parameter ξ is proportional to N , then,

$$\frac{dN}{d\xi} = \lambda N \quad (6.14)$$

Now, if we also assume

$$\frac{d\lambda}{dE} = \frac{\lambda}{E_o} \quad (6.15)$$

Then,

$$\begin{aligned} N &= N_o \exp[-\lambda\xi] \\ &= f_o(E)dE \exp[-\lambda\xi] \end{aligned} \quad (6.16)$$

and

$$\lambda = C \exp[-E/E_o] \quad (6.17)$$

If q is defined to be the average charge of the parameter of interest Q per activation, then

$$\begin{aligned} \frac{dQ}{d\xi} &= \int_{E_1}^{E_2} q \frac{dN}{d\xi} \\ &= q \frac{E_o}{\xi} \int_{E_1}^{E_2} f_o(E) \exp[-\lambda\xi] \exp[-E/E_o] dE \end{aligned} \quad (6.18)$$

and, assuming $f_o(E) = \text{constant} = r$, then

$$\frac{dQ}{d\xi} = \frac{qrE_o}{\xi} * [\exp(-\lambda\xi)] \Big|_{\lambda = C \exp[-E_1/E_o]}^{\lambda = C \exp[-E_2/E_o]}$$

or

$$\frac{dQ}{d\xi} = \frac{qrE_o}{\xi} * [\exp(-C\xi \exp(-E_1/E_o)) \{1 - \exp(-\Delta E/E_o)\}] \quad (6.19)$$

where E_1 = lowest site energy
 E_o = highest site energy
 ΔE = $E_2 - E_1$,
 r = $N/\Delta E$

for

$$\Delta E \gg E_o \text{ and } E_2 < E_o$$

Therefore, the generic form of the macroscopic behavior is

$$\Delta Q = \frac{qNE_o}{\Delta E} * \log \xi + \text{constant} \quad (6.20)$$

predicting a logarithmic behavior for MNOS retention and endurance.

For example, in the case of a thermally activated system, such as retention and endurance, $E_o = kT$ and the generalized parameter can be taken to be time, that is, $\xi = t$ (time). Then, the generic form is given as Eq. (6.21), representing MNOS retention behavior over extended time.

$$\Delta Q = \frac{qNkT}{\Delta E} * \log t + \text{constant} \quad (6.21)$$

6.1.2 NVSM failure modes

Both types of NVSM memory devices have been considered together as similar technologies having very similar operational properties and limitations; however, their failure modes are quite dissimilar. This is due largely to the significantly different roles the traps played in each corresponding device types. Thus, the failure modes of the floating gate NVSM devices are studied separately from that of the floating trap NVSM devices.

6.1.2.1 Floating Gate NVSM Devices Two distinct contributors to EPROM retention, with different activation energies, have been determined [6.24]. (1) Charge leakage due to oxide-hopping conduction between the floating gate and the silicon substrate is dependent on the oxide dielectric quality. Manufacturing and substrate defects are random and have low activation energies, 0.3 eV for catastrophic defect failures and 0.6 eV for oxide-hopping leakage failures. Both failures manifest themselves as infant mortality and random lifetime failures. (2) Charge loss due to thermal emission has a thermal activation energy of 1.4 eV. This high-activation energy contributes to the nonvolatile retention properties of the EPROM. A plot of initial discharge rate versus storage temperature for the worst case bit of a typical programmed EPROM part is shown in Fig. 6.13.

This figure can be compared with a corresponding plot, Fig. 6.14, of a defective bit of another EPROM. The difference in activation energy of the two should be noted. The screening of the defective EPROM for reliability can be effectively implemented based on an understanding of the failure mechanism of the device, taking advantage of the activation energy differences.

Repeated stress of erase-program operations of the EPROM leads to another major failure mode of the EPROM, namely, the endurance limits and failures. Two types of failure phenomena have been reported—loss of memory window and shift of operating margin. The window collapse can be attributed to field or charge current fluence generation of oxide traps leading to increased leakage discharge of the floating gate. During cycling, the electrons can also become trapped in the oxide. The resulting negative oxide charge can be observed as a shift of threshold window center with endurance. The trapped charge also inhibits further injection charging of the floating gate, causing the memory cell to require a higher program voltage or a

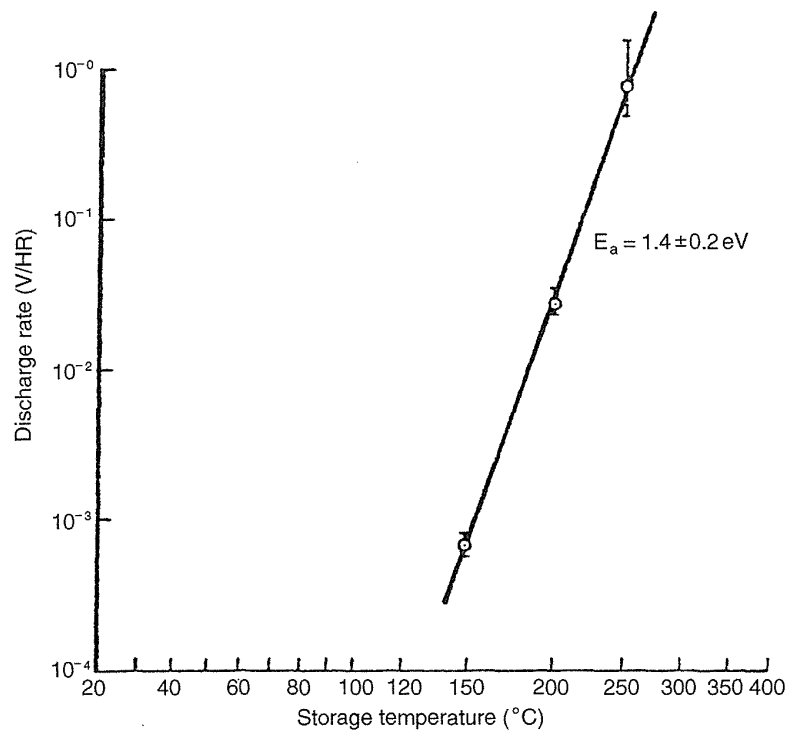


Figure 6.13 Plot of initial discharge rate versus storage temperature for the worst case bit on typical programmed parts (after Shiner et al. [6.24]).

longer program time. For the same program pulse, the memory cell exhibits a narrowing of the threshold window.

There are several approaches for Flash EEPROM. They are generically derived from EPROM technology. The programming, identical to EPROM, is accomplished with channel hot-electron injection. Different from UV erase in EPROM, the Flash EEPROM erase is accomplished with Fowler–Nordheim tunneling through the oxide gate dielectric. Therefore, bipolarity electric stress is experienced by the oxide gate dielectric in the case of Flash EEPROM endurance.

Even as it is generally acceptable to assume that Flash EEPROMs, being based on EPROM technology, have similar reliability characteristics, reliability performance is different. The thin gate oxide in use in EEPROMs is often exposed to a significantly increased level of operating stress since supply voltage scaling is not practiced as other aspects of the device process technology are scaled. Table 6.5 illustrates the relationship between process/device technology and the time-dependent oxide failure acceleration factor that must be used to accommodate the differences in oxide thickness.

The reliability characteristics of the floating gate tunnel oxide EEPROM (FLOTOX), with its thin tunnel oxide of less than 200 Å (typically 100 Å), are expected to be dominated by the properties of the tunnel oxide. In tunnel oxide

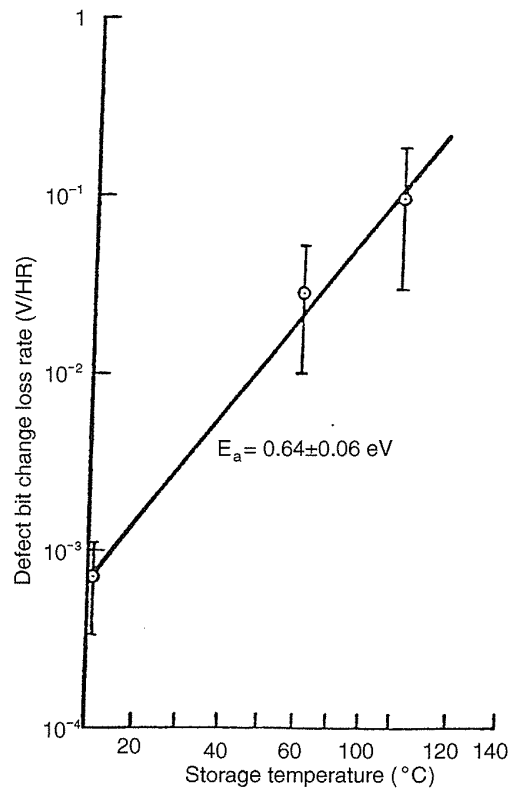


Figure 6.14 Plot of discharge rate versus storage temperature for erased defect bits in the programmed state (after Shiner et al. [6.24]).

TABLE 6.5 TIME-DEPENDENT OXIDE FAILURE ACCELERATION
(PER INTEL REPORT [6.25]). [REPRINTED BY PERMISSION OF INTEL CORPORATION,
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Type	Supply Voltage (Volts)	Oxide Thickness (Å)	Operating Stress (MV/CM)	Acceleration Factor at _% Over Stress				
				10%	20%	30%	50%	100%
HMOS E	5	700	0.714	3.2	10	32	100	1.0E + 5
HMOS II E	5	400	1.25	7.5	55	422	3162	5.6E + 8
ETOX™	5	400	1.25	7.5	13.4	422	3162	5.6E + 8
ETOX 11	5	235	2.13	3.7	13.4	49.1	658	4.3E + 5

Assumes:

1. No bias generators.
2. Depletion loads.
3. Failure rate calculations use the appropriate acceleration factor for stress voltage and maximum operating voltage (conservative).

EEPROMs (some EEPROMs use nitride as the tunnel dielectric structure, making them similar in properties to the generic MNOS NVSM devices to be discussed later in this section), typically the oxide dielectric is thermally grown. The tunnel oxide is expected to be limited in endurance performance, with electron and hole traps dynamically modified, filled and emptied, and new traps generated, by the tunneling current during erase and write cycling. Figure 6.15 shows the typical endurance plots of a FLOTOX EEPROM illustrating some aspects of the device's charge-trapping properties.

Initially, with erase/write cycling, the threshold window is widened. The generation of additional positive charges in the silicon dioxide near either interface of the metal-insulator semiconductor (MIS) structure with each corresponding erase or write cycle, during endurance exercising, results in an additional electric field at the injection interface for electrons to increase charge storage at the electrode and a corresponding field at the anode, that is, the poly-SiO₂ interface, for write threshold increase. Figure 6.16 illustrates the influence of positive charges in the SiO₂ on the EEPROM threshold window. The dominant endurance characteristic of the EEPROM is the collapse of the threshold window with increasing erase/write cycles. This phenomenon has been referred to as trap-up. The tunneling electrons, or fluence through the oxide, can be captured by electron traps. In addition, electron traps are generated by the tunneling current.

The trapped charge in the oxide reduces the effective injection field at the tunneling interface, decreasing the tunneling current and thus narrowing the threshold window of the device until it becomes nonoperative as a circuit element. A single-cell endurance is compared against measured array endurance features in Fig. 6.15. It dramatizes the importance and necessity of designing for worst case margins to ensure the performance of the product which, in this example, is an array of 16,384

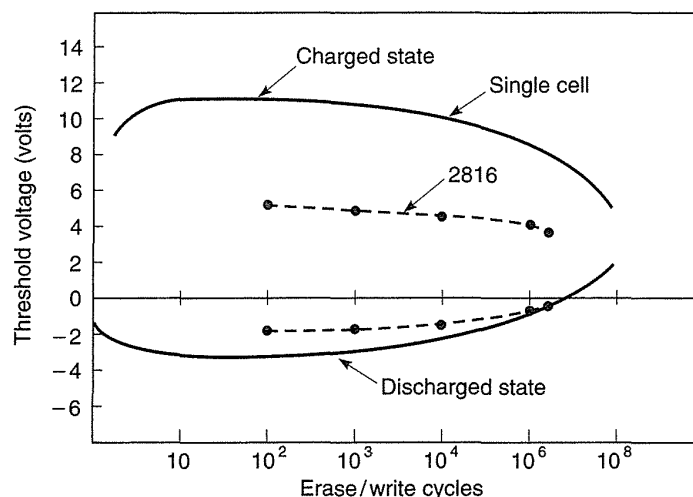


Figure 6.15 Typical cell and device window versus log cycles (after Euzent et al. [6.26]).

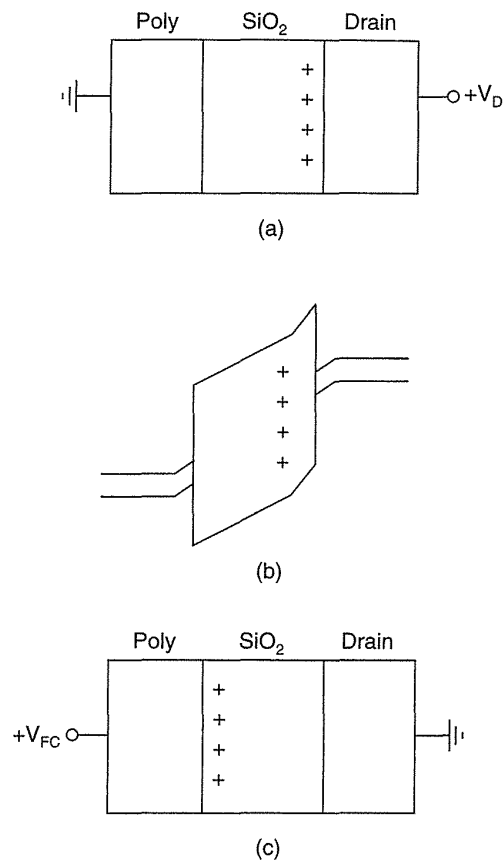


Figure 6.16 Threshold window widening (after Euzent et al. [6.26]). (a) Positive charge included at the SiO₂-Si interface at the end of the operation. (b) Band diagram of subsequent erase showing lowering of the tunneling barrier by the trapped positive charge. (c) Positive charge near polysilicon-SiO₂ interface at the end of the erase operation.

individual EEPROM cells. Figure 6.17 is a threshold window endurance plot of a 1Mbit Flash EEPROM memory illustrating not only the design margins needed to ensure product quality, but also excellent endurance properties of $> 10^6$ erase/write cycles, reflecting the improvement made in the gate dielectric endurance properties through the 1980s. Intrinsic charge loss of EEPROMs is expected to be equivalent to that of EPROMs. However, EEPROMs can be assumed to exhibit a higher rate of data retention failure than EPROMs due to defect-related failures of the oxide dielectric. The EEPROM tunnel oxide typically is thinner, and in addition, the number of erase/write cycles, which is usually specified several orders of magnitude higher for recent EEPROMs, contribute to higher defect charge losses than EPROM devices of the equivalent technology stage (i.e., defect levels of the process as well as lithographic dimensions). The activation energy of this EEPROM failure mechanism has been measured [6.26] at 0.62 ± 0.4 eV.

Other than tunnel oxide floating gate EEPROMs, the other floating gate EEPROM technology is the textured-poly gate cell. Based on much thicker interpoly tunnel oxides than the tunnel oxide typical of FLOTOX EEPROMs, textured-poly devices exhibit excellent reliability in failures due to random defects that contribute

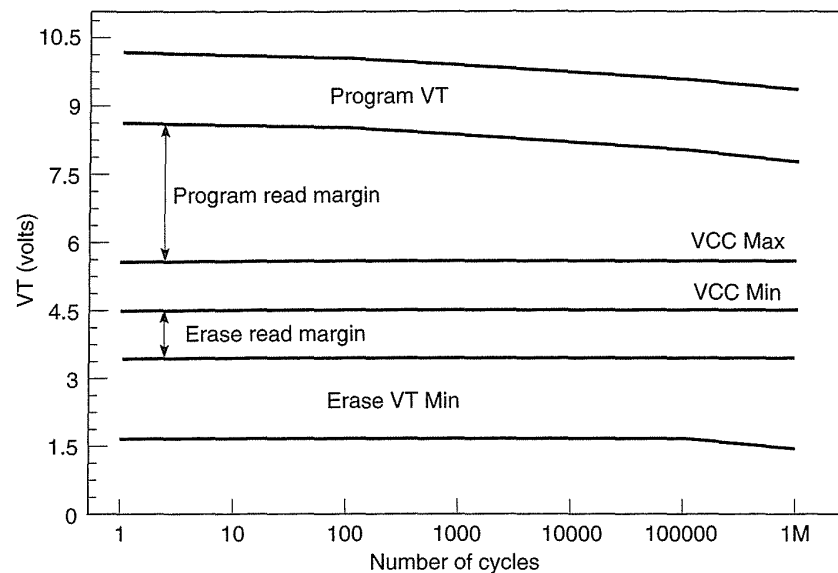


Figure 6.17 Array V_t versus cycles (after Kynett et al. [6.27]).

to intrinsic charge loss causing retention failures with endurance cycling. On the other hand, the textured-poly cells typically suffer from charge-trapping endurance failure at much lower levels of endurance cycling than FLOTOX devices [6.28]. Figure 6.18 compares the trap-up properties of the two floating gate EEPROM devices.

6.1.2.2 Floating Trap NVSM Devices. With spatially distributed traps in the dielectric as the storage means, MNOS retention differs markedly from that of the floating gate NVSM. MNOS thresholds continuously decay as trapped charges in the dielectric are detrapped. A logarithmic threshold decay was established and reported in the literature [6.29]. The end of data retention, typically represented by the closure of the threshold memory window, has also been investigated in terms of temperature; that is, activation energy, derived from Arrhenius plots, ranges from ≈ 0.6 eV to 1.8 eV without considering endurance effects. The deleterious effect of endurance exercising on the MNOS device can be presented as a continuous reduction of retention lifetime activation energy with erase/write cycling of the device. Table 6.6 and Fig. 6.19 present a set of such data on MNOS retention and endurance reliability.

6.2. NVSM RELIABILITY AND APPLICATIONS

Current trends in microcomputer chips will lead to chips that have more than 100 million transistors and a required failure rate of 10 FIT [6.30]. Data from Intel Corporation (see Fig. 6.20) clearly support this FIT rate trend along with the asso-

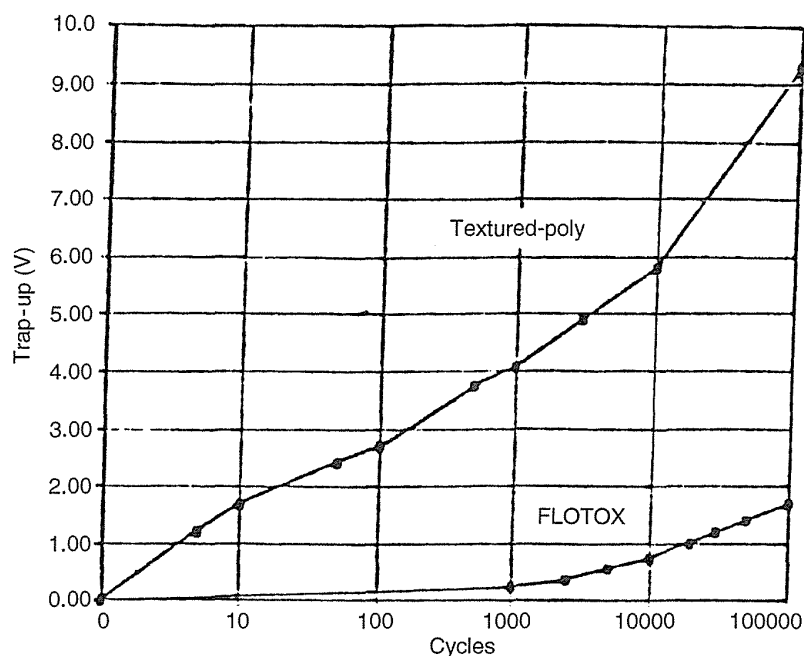


Figure 6.18 Trap-up comparison. Trap-up is measured as the increase in programming voltage required to program the cell as a result of cycling (after Mielke et al. [6.28]).

ciated improved infant mortality goals targeted for the end of this century. This trend will carry over into memory chips as well.

In order to reach these transistor count goals, the feature sizes of CMOS technology will be scaled to a $0.2\ \mu\text{m}$ channel length, a $50\ \text{\AA}$ gate oxide thickness, and a metal pitch of $0.8\ \mu\text{m}$ as indicated by Intel trends in Figs. 6.21 and 6.22.

These dimensional trends have a profound effect on the requirements for reliability assessment and process control. Chips will be operating with many orders of magnitude less intrinsic reliability margin than was available in the early 1970s. Assuming that existing relationships between time-to-fail and device parameters are valid for electromigration, hot-carrier degradation, and oxide wearout, it can

TABLE 6.6 ACTIVATION ENERGIES AT VARIOUS ERASE/WRITE CYCLES (AFTER AJIKI ET AL. [6.29]).

Erase/Write Cycles	Activation Energy (eV)
10	0.67
10^3	0.60
10^4	0.50
10^5	0.25

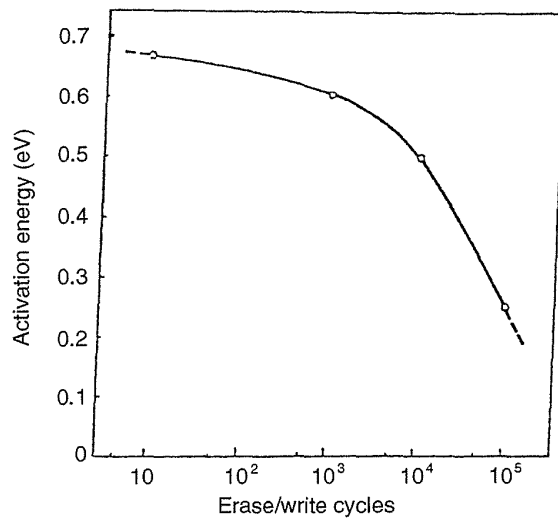


Figure 6.19 Activation energies at various erase/write cycles (after Ajiki et al. [6.29]).

be shown in Fig. 6.23 that relative median time-to-fail has been reduced by the scaling process.

This reduced reliability margin means that the processing line monitoring requirements must grow to offset the smaller latitude. Material quality variations that were acceptable in the past can no longer be tolerated in the future. As new processes and new materials are introduced in submicron fabrication, it will be

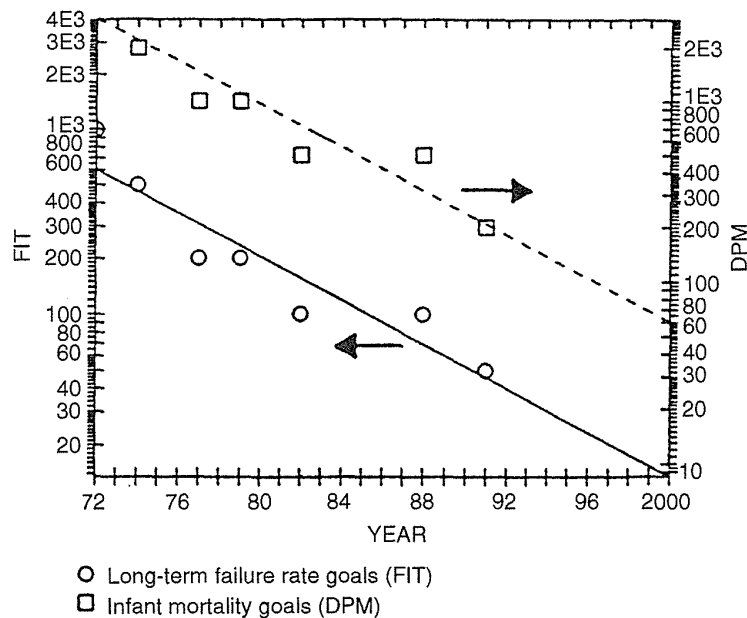


Figure 6.20 Infant mortality and long-term failure rate goals at Intel versus time (after Crook [6.30]).

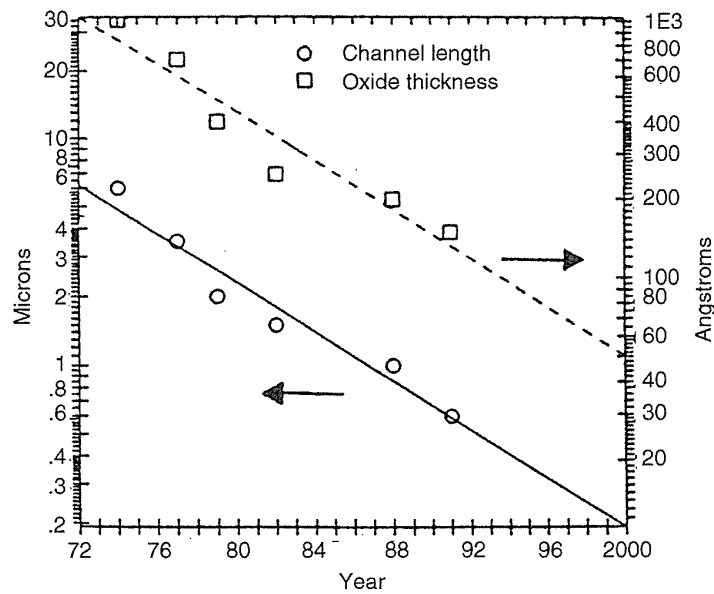


Figure 6.21 VLSI channel length and gate oxide thickness trends (after Crook [6.30]).

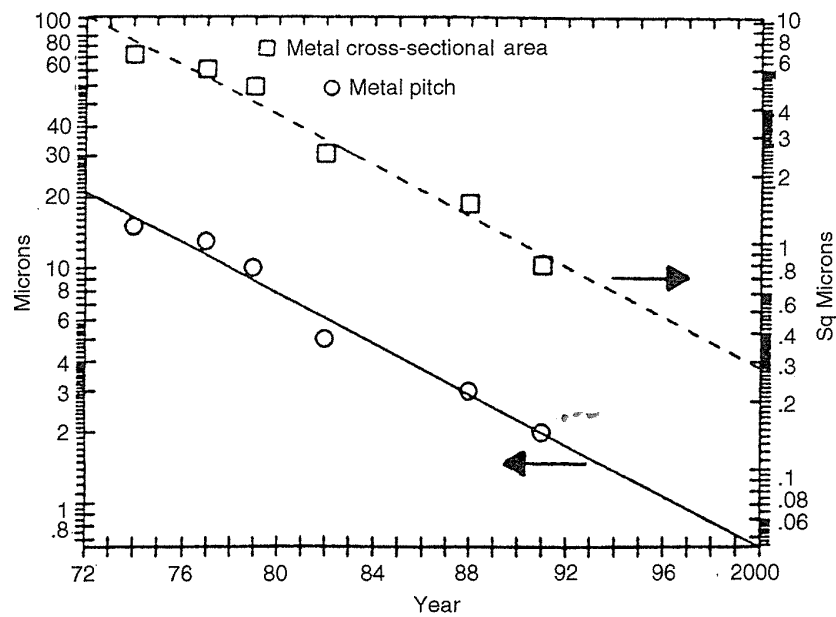


Figure 6.22 VLSI metal pitch and minimum line cross-sectional trends after Crook [6.30]).

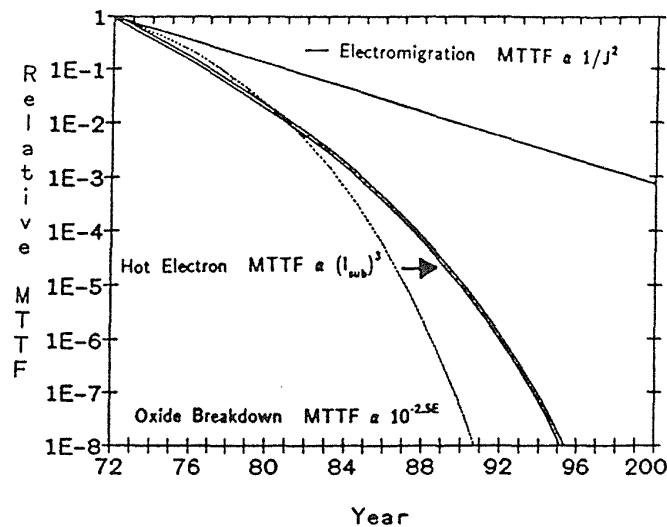


Figure 6.23 Over the years, impact of the effects of device and metallization scaling on time-to-failure margins for electromigration, hot electrons, and oxide wearout failure mechanisms (after Crook [6.30]).

necessary to update or completely change reliability models to accommodate new mechanisms. Test structures must be developed to characterize the reliability limiting processes and provide monitors for process control. It is necessary to monitor the individual mechanisms at the wafer level, at the end of processing, and also to extend wafer-level monitors further back into the processing line. Tighter process controls within an aggressive statistical process control (SPC) regime is critical.

Among the main considerations in reliability of NVSM devices is the fact that normal operation of the devices requires high operating voltages in order to erase or write data. The high voltages result in high-stress fields across the gate oxides of not only the storage devices, but also the MOS circuitry that supports the operation of the storage device. The insulator quality becomes the most serious concern for the fabricator of NVSM devices. Even relatively small insulator defects, which may be of little concern to standard MOS circuits, are of major concern in NVSM devices because of the higher operating fields. This is compounded by the fact that floating gate devices must use ultra-thin insulators to be able to program the storage devices quickly.

In addition to the high-field stress in insulators, another stress factor is caused by the high-peak current required to charge and discharge circuit capacitances to the elevated voltages required in the chip. This places interconnect metalization in jeopardy of early failure due to electromigration. The high-peak current densities result in high-peak temperature and can place more stringent requirements on the current density limit rules that designers must use in designs. Because one of the design goals is to produce the highest circuit density possible, the current density design rules are commonly pushed to the limit permitted by the fabrication process.

Beyond the hard fail aspects of the materials are the issues of retention and endurance failure modes in NVSM devices as outlined in Section 6.1. These mechanisms cause slow degradation in performance. Retention failure is caused by repeated interrogation of the device, resulting in a small amount of charge being changed, which limits the time period within which data can be accessed without error to a time less than is acceptable for an application. Endurance failure is a result of changes in the characteristics of the storage transistor so that the device can no longer meet performance criteria (usually retention time). Changes in device characteristics occur with accumulated erase/write cycles.

The above reliability limiting mechanisms must be understood individually, modeled, and monitored in order to maintain a prescribed level of NVSM reliability. The following discussion addresses the failure mechanisms in terms of intrinsic and extrinsic, or defect-related causes. In order to be able to monitor the reliability of NVSM devices (or any other MOS device), models must be created for the rates of failure due to each mechanism. This enables the development of well-characterized test structures and will lead to more accurate statistical process control in manufacturing.

With appropriate models in place that allow the extrapolation of individual mechanism-accelerated test data to use conditions, additional effort is needed to understand the point in the fabrication process where the reliability hazard is introduced. It is also necessary to be aware that fabrication testing is not, by itself, sufficient to guarantee a flow of highest quality product.

6.2.1 Reliability Modeling

The authors endorse a global perspective of NVSM reliability—the reliability of the NVSM represents the quality of the product and its improvement that can be addressed in all stages of product design and manufacturing, ranging from processing to reliability testing. However, it must be understood that existing insulator reliability models, as described in Section 6.1, are empirical and may be changed as more research is done to understand the physical processes of stress-induced insulator damages. At this time, there are two widely debated models for insulator reliability. One is described in [6.31] and is referred to as the “E” model, indicating the electric field dependency of acceleration factor. The other is included in the paper by Chen et al. [6.8], which has fit data from numerous papers to an equation for time-to-fail that varies as $1/E$. Since both models appear to fit available data, the actual physical model will likely have other variables involved in a more complex relationship with electric field and temperature. For purposes of assessing the oxide reliability of NVSM devices, the $1/E$ model fits experimental results best when the oxide is exposed to high electric fields in the range used to write data into a NVSM chip.

In addition to the insulator failure models, there are models for the other mechanisms that determine chip reliability. This section discusses a number of other models for mechanisms that are of interest to NVSM reliability. A top-down approach is appropriate to gain perspective in the problem of creating models

to measure and track reliability on a fabrication line. The familiar “bathtub” failure rate curve has three regions of interest: early life (often called infant mortality), useful life, and wearout. The early-life hazard rate has always been a major concern for manufacturers because it directly impacts product warranties and company reputation.

There is a simplified method for expressing the overall early-life hazard rate of a chip by defining an expression that contains the aggregate effects of all mechanisms involved in limiting the lifetime of a NVSM chip. It is most common to choose an exponential distribution for early failure rates because it generally fits measured early failure data very well, and it also has the property of being mathematically tractable. This expression takes the classical time-dependent hazard rate form:

$$\lambda(t) = \lambda_b * \exp(-\tau * t) \quad (6.22)$$

where λ_b = base failure rate
 τ = rate time constant
 t = time

The equation assumes that all temperature-dependent mechanisms are referenced to 25°C (room temperature). The failure rate obtained from samples life-tested at other temperatures is obtained by multiplying each time-to-fail by the Arrhenius relationship to correct it to the reference temperature.

$$A(T) = \exp\{[-E_a/k] * [(1/T) - (1/T_o)]\} \quad (6.23)$$

where $A(T)$ = temperature acceleration factor
 T = temperature (Kelvin)
 T_o = reference temperature (Kelvin)
 k = Boltzmann’s constant = 8.62310^{-5} (eV/K)
 E_a = activation energy (eV)

The failure rate at the new temperature then becomes

$$\lambda(t) = \lambda_b * A(T) * \exp[-\tau * A(T) * t] \quad (6.24)$$

which is the basic temperature acceleration model for failure rates of any CMOS device by any known mechanism. Tables 6.1 and 6.2 in Sections 6.0 and 6.1, respectively, contain activation energies that have been measured for many mechanisms of concern to semiconductor device manufacturers. The actual value of activation energy for early-life failures may vary from the values stated in the tables because the tabulated activation energies are measured for the wearout process. Early failures may contain multiple contributing mechanisms that lead to activation energy values that differ significantly from the tabulated values given here. Table 6.7 summarizes typical values for coefficients for Eq. 6.24 for a range of mechanisms that govern failure rates in IC devices.

The failure rate during the early failure period is also governed by other acceleration factors that relate to the specific mechanism. In this case, it is necessary to understand the physics of the mechanism well enough to at least derive an empirical

TABLE 6.7 EARLY-LIFE FAILURE RATE PARAMETERS

Mechanism	Lambda_b (F/10 ⁶ hrs.)	Tau (1/hrs.)	Ea (eV/deg K)
Metal	0.00102	1.18	0.55
Oxide	0.0788	7.70	0.30
Contamination	0.000022	0.0028	1.0
Miscellaneous	0.010	2.2	0.43

model for the mechanism. Even though the previous discussion relates to early failure, it must be understood that these physical mechanisms are generally responsible for all aspects of the life curve because the presence or absence of small defects in the materials results in local conditions that manifest themselves as early failures (e.g., Eq. 6.4, Section 6.1). For the mechanisms of greatest interest to NVSM designers and users (i.e., time-dependent dielectric breakdown, hot-carrier damage, and electromigration), acceptable empirical models already exist and are a reasonably good fit to a large amount of experimental data.

6.2.1.1 Oxide Failure Models. Section 6.1 discussed one of two models that are commonly found in the literature. In particular, one model discussed is referred to as the 1/E model, as is clear from the form of the field acceleration factor equation (Eq. 6.3 in Section 6.1). There is still considerable discussion in the reliability research community over whether the 1/E model applies over the entire field stress range to which oxides are commonly exposed. As extensive data sets show, the 1/E model fits well for high-field cases, which is precisely the case for NVSM applications. However, existing data at the lower fields experienced by support circuitry on NVSM chips suggest that the earlier field acceleration factor model by Crook [6.12] fits data at more moderate field levels. This is referred to as the “E” model:

$$A_{ef:oxide} = \exp[(E_{ref} - E_s)/E_o] \quad (6.25)$$

where E_{ref} = reference electric field
 E_s = stress electric field (operating field)
 E_o = normalizing electric field

Extensive experimental data collected by Domangue et al. [6.33] yielded a value for E_o of 0.134 MV/cm.

In the case of the 1/E model, the field acceleration factor experimentally determined by Lee, Chen, and Hu [6.9] for 1% failure was found to be 192 MV/cm. Based on this observation, the field acceleration factor most appropriate for NVSM devices is given as

$$A_{ef:oxide} = \exp[-192(1/E_s - 1/E_{ref})] \quad (6.26)$$

Field acceleration factors are significantly influenced by the assumptions made relative to the defect population that is of interest. In the case of early failure, time to

1% fail, the slope of the $1/E_s$ versus time-to-fail curve, is significantly less than is observed at around 50% failures, as shown in Fig. 6.24. This graph clearly shows the degradation effects of oxide defects on the useful life of MOS devices. NVSM devices are particularly susceptible to random defects because of the necessarily thin oxides and high operating fields during write. As was indicated in Section 6.1, the development of oxide lifetime models is based primarily on experimental data and curve fitting to intuitively reasonable model equations. There is not yet a fully physical model that describes all aspects of TDDDB life-limiting characteristics that account for the highly complex effects of various defects (including contamination). It is possible that, when routine oxide growth techniques approach defect-free quality, a more refined theoretical model will be published and experimentally verified.

In addition to a field acceleration factor for oxides, experimental results have suggested that an acceleration factor exists for scaling oxide thickness. Yamabe and Taniguchi [6.34] have described experimental data that suggest the existence of a relationship between oxide thickness and oxide thickness at constant electric field. It is apparent that this relationship is second order to the effects of electric field. Also, it is not clear whether this relationship is more a function of the significance of defect size compared to the oxide thickness. If this observation proves to be related to a mechanism other than defects, then it will have a significant bearing on NVSM reliability because the oxide thickness is so small in storage devices.

The models discussed previously for field-accelerated oxide failure assume that the oxide is exposed to a uniform stress level resulting from a roughly equipotential surface on both sides of the oxide. In NVSM devices, stress conditions are far from

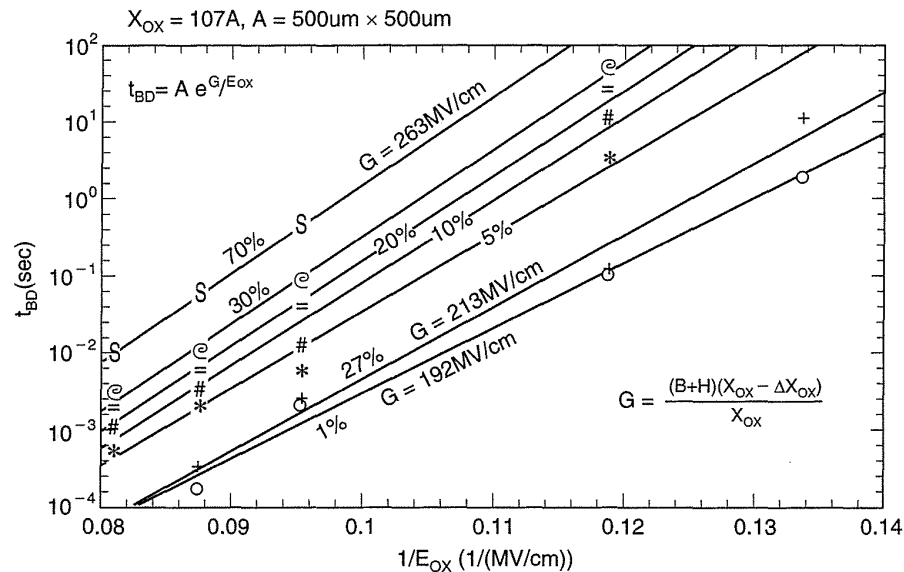


Figure 6.24 t_{BD} versus $1/E_s$, for different percentage failure levels for TDDDB data (after Lee et al. [6.35]).

uniform because the method for writing and erasing the contents of the memory involves the use of hot-carrier injection along with Fowler–Nordheim tunneling current. In addition, high-drain voltages can be present along with low gate voltages in NVSM devices and bias transistors close to the snapback region, which is favorable to hot-hole injection into the oxide. Several studies [6.35–6.37] have shown that these bias conditions lead to nonuniform stress conditions in the drain region. In particular, Chen et al. [6.35] have shown a sharp drop in Q_{bd} in transistors that have been biased to inject significant hole current into the oxide. At present, there is no model for predicting oxide failure under these conditions against a general background of uniform field stress. The main concern in this situation is that existing uniform field stress models may underestimate the oxide lifetime.

6.2.1.2 Hot-Carrier Damage Models. Hot-carrier damage to transistors is of considerable concern to circuit designers of MOS circuits. As hot-carrier-induced damage occurs, the transistor transconductance and threshold voltage shift, causing circuitry eventually to fail to perform to the level required for proper operation of the circuit. It is ironic to be concerned about hot-carrier damage in a treatment on NVSM reliability because hot-carrier injection is one of the important mechanisms used for writing into NVSM cells. However, the concern applies to the MOS support circuitry present on the same chip that contains the nonvolatile memory array. If the support circuitry fails to perform its intended task, then the entire chip is considered useless even if the storage array is fully functional.

For short-channel MOS transistors, hot-carrier degradation can be expressed empirically in a simple parameter shift relationship [6.32]:

$$\text{Transistor parameter shift} = Phc * t^n \quad (6.27)$$

where t = stress time

n = power factor, which changes with injection mode

Phc = magnitude of degradation

Phc varies with bias conditions and has been experimentally shown to be related to drain voltage. This constant has an exponential relationship with drain voltage (V_d) [6.32]:

$$Phc = \beta * \exp(-\alpha/V_d) \quad (6.28)$$

The proportionality constants, α and β , are found experimentally for transistors produced on a specific processing line. These constants are extremely sensitive to processing variations and also depend on manufacturing methods that have been devised to reduce hot-carrier damage rates on short-channel transistors. In particular, various lightly doped drain (LDD) structures are implemented by several manufacturing techniques that have a profound effect on the parameters in these equations.

Combining Eqs. 6.27 and 6.28, we can solve for the amount of time required for a specified shift in a parameter. This is useful for cases where a designer intends to implement circuits that are tolerant of selected parameter shifts caused by hot-carrier damage. From a manufacturing point of view, it is valuable to have a method that

can be used to relate easily measured electrical quantities to expected time to unacceptable parameter change. One easily measured electrical quantity is the amount of substrate current that flows at specific bias conditions known to cause high rates of parameter shift. As experimentally determined, the substrate current is strongly correlated with the transistor parameter degradation rates [6.45, 6.46]. Substrate current generation is modeled by [6.46]:

$$I_{\text{sub}} = C * I_d * \exp(-\phi(i)/q * \lambda * E_m) \quad (6.29)$$

where C = process determined constant

I_d = drain current

$\phi(i)$ = impact-ionization energy

λ = mean-free path of electrons in the channel

q = electron charge

E_m = maximum electric field in the channel

An expression that relates substrate current and drain current to transistor lifetime, t , was developed [6.47] and requires relatively simple calibration procedures for parameter shift:

$$t = (A/I_d) * (I_{\text{sub}}/I_d)^{-m} \quad (6.30)$$

where A and m (typically m is about 2.5 to 2.9) are determined experimentally for a particular wafer fabrication process. This relationship assumes no temperature-related factors. Since it is widely recognized that a thermal effect is to be accounted for in hot-carrier damage, the following thermal acceleration relationship was defined [6.50], which corrects the constant A for temperature:

$$A_{\text{hc}}(T) = A_o * \exp(-0.039/kT)$$

which leads to the following revision of Eq. 6.30:

$$t = (C/A_{\text{hc}}(T) * I_d) * (I_{\text{sub}}/I_d)^{-m} \quad (6.31)$$

where C is an experimentally determined constant.

Conspicuously absent in the above discussion is an early-life failure rate relationship. This is because hot-carrier damage is strictly a wearout mechanism that affects all transistors at roughly the same rate for the same level of stress. There may, however, be some local structural differences in LDD technology transistors, introduced during manufacture, that would affect the damage rate at different locations on a wafer, which would be treated as a process control issue.

6.2.1.3 Electromigration Models. Electromigration of interconnects is one of the most common life-limiting mechanisms found in VLSI devices. There have been many examples of documented field failures in which this mechanism was found. Its presence as a lifetime limiter is not confined to any one technology, but is most commonly observed whenever there is either a requirement for high DC current in a chip or there is a persistent high-peak pulse current of the type commonly found in memory devices. NVSM chips are among the most vulnerable to

pulse-current-driven electromigration failure because high-peak current flows whenever write or erase operations occur.

The early-life failure model for electromigration assumes a form described in [6.32]:

$$\lambda(t) = 1.02E - 3 * A(T) * [\exp(-1.18 * t_0)] * \exp[-1.18 * A(T) * t] \quad (6.32)$$

where $A(T)$ = temperature acceleration factor

t_0 , t in hours

This empirically derived failure rate was extracted from a large database described in reference [6.32] and tries to deal with all factors that cause early failure in metal interconnects. This expression, along with an expression describing the wearout aspects of interconnects, provides NVSM designers with a means of analyzing life-limiting factors in a chip.

Given a manufacturing facility that is well controlled with respect to random point defects in the metallization, the lifetime of the metal interconnects is well described by the classic “Black’s Model” that relates the combined effects of current density and temperature on the lifetime of the metal [6.91]. Cumulative failures are lognormally distributed.

$$t_{50} = A * ((1/J)^n) * \exp(E_a/kT) \quad (6.33)$$

where A = pre-exponential constant

J = current density (A/cm^2)

E_a = metal thermal activation energy (eV)

n = current density exponent

k = Boltzmann’s constant = $8.62 \text{ E-}5 \text{ eV/K}$

T = metal temperature (K)

Constants E_a and n are determined experimentally in accelerated tests involving ASTM standard test methods [6.38–6.40], and generally result in constants that span a relatively narrow range depending on the type of metal system in use for interconnects. The pre-exponential constant contains the effects of the metal deposition environment and alloy composition, metal thickness, width, and length. The constant A (and for that matter, all of the other constants) must be determined experimentally on a specific test structure (e.g., the ASTM structure) in order to have a reference point for metal quality that can be extrapolated to normal use conditions.

Activation energy, E_a , ranges from about 0.43 eV to about 0.8 eV, with a typical value of about 0.55 eV. Factors controlling the actual value of the activation energy include alloy composition, annealing conditions, contamination, and the presence or absence of passivation. In addition, special metal systems that utilize composite structuring with a refractory barrier material below (or above and below) the aluminum alloy layer will exhibit different activation energies depending on the criteria defined as failure. These composite, or layered, metal systems typically do not fail in the open-circuit mode observed with aluminum alloys. They experience a resistance increase with time as the aluminum alloy layer migrates, leaving only the barrier

material to conduct current. Electromigration testing of these composite materials uses a fractional resistance increase (e.g., 1.30 times initial resistance at the test temperature) as a failure criterion. The choice of magnitude of this fractional change of resistance will affect the value of the activation energy extracted.

The current density exponent, n , has a typical value of 2.0 for metal subjected to nominal design limit current densities. Other values of n are reported in [6.32] for some alloys and composites, depending on the current density used in the electromigration test. It is particularly important that the material being tested be carefully characterized at various ranges of current density in order to be able to extract a value of n that is consistent with the test conditions and that will make extrapolation to at-use conditions meaningful. Extraction of n for extreme acceleration factor conditions is also desirable, as will be discussed later in this chapter.

Black's Model for electromigration assumes that a direct current flows in the interconnect. As a result, there will be an equilibrium mass flow condition which eventually results in open failure. If the current flow is pulsed or bipolar, there may not be an equilibrium mass flow condition in the interconnect. Towner et al. [6.41] have empirically derived a duty cycle correction relationship that translates DC t_{50} test results to pulsed DC operating conditions. Generally, a frequency dependency does not exist as long as the pulse period is shorter than the vacancy relaxation time of the interconnect metal. Suehle [6.42] and others [6.43, 6.44] have shown experimentally that, when the pulse frequency is greater than about 200 Hz, the relationship between t_{50} :pulse and t_{50} :DC is

$$(t_{50}:\text{pulse})/(t_{50}:\text{DC}) = 1/r^2 \quad (6.34)$$

where

$$r = \text{pulse duty cycle.}$$

In the case of complete symmetry of current flow direction (fully bipolar, assuming short periods) [6.43], the electromigration lifetime is greatly increased, yielding an MTF:AC/MTF:DC ratio of about 1000. This ratio was experimentally shown to be independent of current density and is of considerable importance in the case where a metal interconnect is supplying current to charge and discharge a large capacitive load.

6.2.2 NVSM Application — Device Design Examples

An accurate understanding of device performance limitations and reliability failure mechanisms points to device design innovations that can enhance product manufacturability and reliability. As devices are scaled for storage density, drain-source leakages and gate dielectric defects become significant performance, reliability, and manufacturability issues. Recent EPROMs and Flash EEPROMs have incorporated changes in the memory cell to minimize the impact of these failure modes [6.49, 6.50, 6.51]. A series-enhancement MOS transistor is added to the floating gate structure to form a split gate memory cell, as seen in Fig. 6.25. The series transistor eliminates the depletion leakage current of electrically erased memory

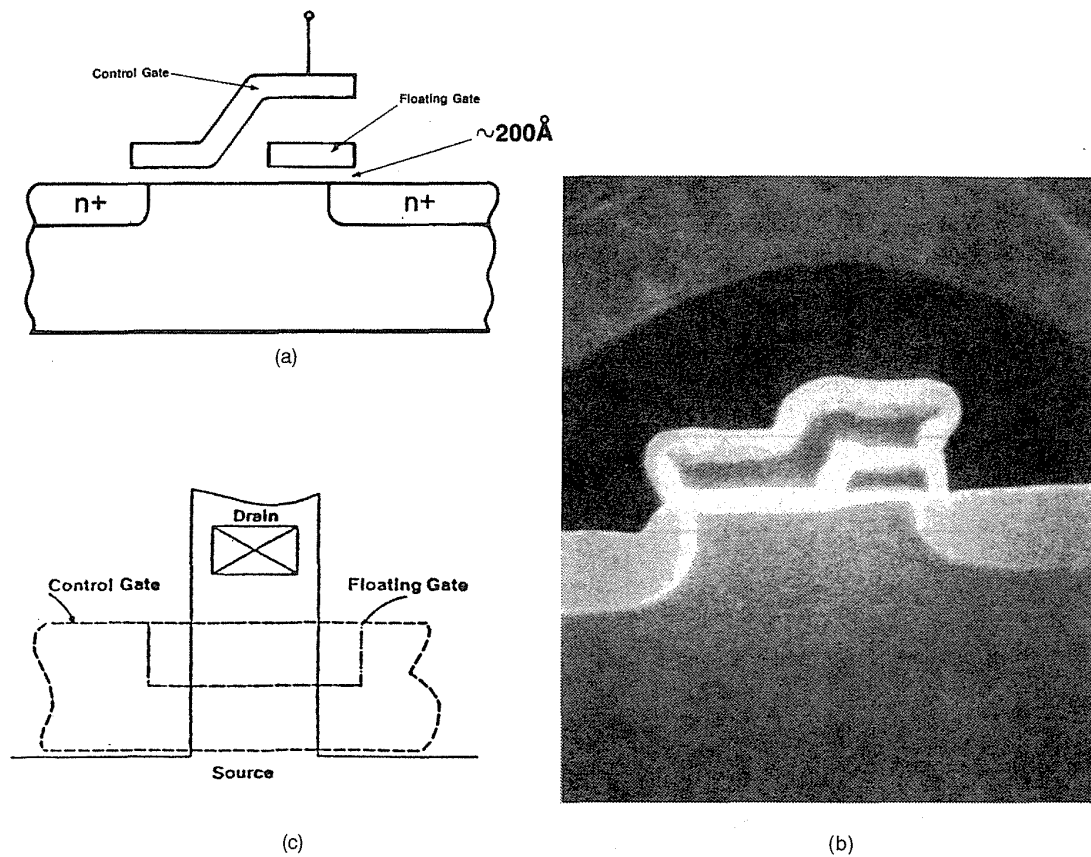


Figure 6.25 (a) Crosssection of the Flash EEPROM cell, (b) SEM cross section, and (c) layout of the Flash EEPROM cell (after Samachisa [6.49]).

devices in the EEPROM array. It also provides immunity to drain-source punch-through, regardless of the effective channel length of the floating gate memory region. Therefore, with the series transistor as part of the memory cell structure, the yield-limiting memory channel area can be minimized to improve manufacturability. The split gate EEPROM cell size is larger ($\simeq 20\%$) than a similar cell using the same set of design rules, but without the series transistor. The increase in area must be evaluated against the smaller memory channel length that can be utilized and the reduction of erase and read circuit complexity because of the improved memory cell characteristics. To reduce the gate dielectric defect level and, concurrently, to enhance capacitive-coupling of the control gate and the floating gate, an interpoly dielectric sandwich of a $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ stacked structure [6.51] has been used (see Fig. 6.26). A higher breakdown voltage and lower defect density than a SiO_2 monolayer dielectric for this structure have been reported in the literature [6.53, 6.54]. To obtain better

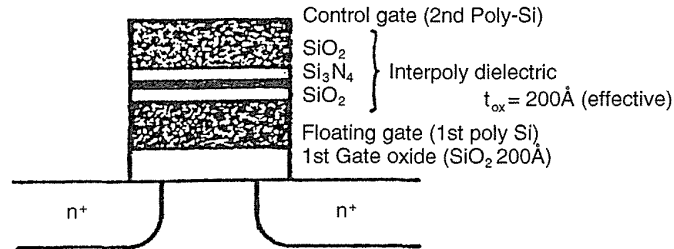


Figure 6.26 Cross-sectional view of the memory cell transistor (after Ohtsuka [6.51]).

endurance characteristics, the FLOTOX EEPROM tunnel insulator utilizing nitrided oxide thin films has been suggested [6.55, 6.56].

The importance of the role of reliability physics and engineering is evident in the device design of floating trap NVSM cells. To eliminate charge injection from the polysilicon gate electrode into the nitride, a blocking oxide is introduced, forming the silicon–oxynitride–nitride–oxide–silicon (SONOS) memory gate structure. Typical cross-sectional views of the SNOS and SONOS are compared in Fig. 6.27. In Fig. 6.28, typical capacitance-voltage (C-V) plots of these structures are illustrated showing the “0” and “1” states of the devices, set/programmed with ± 25 V, 5-second programming pulses. The location of the “0” and “1” states, vis-à-vis the initial C-V plots in SONOS structures, indicates that charge injection is from the substrate, validating the successful blocking of the undesirable gate electrode injection [6.59].

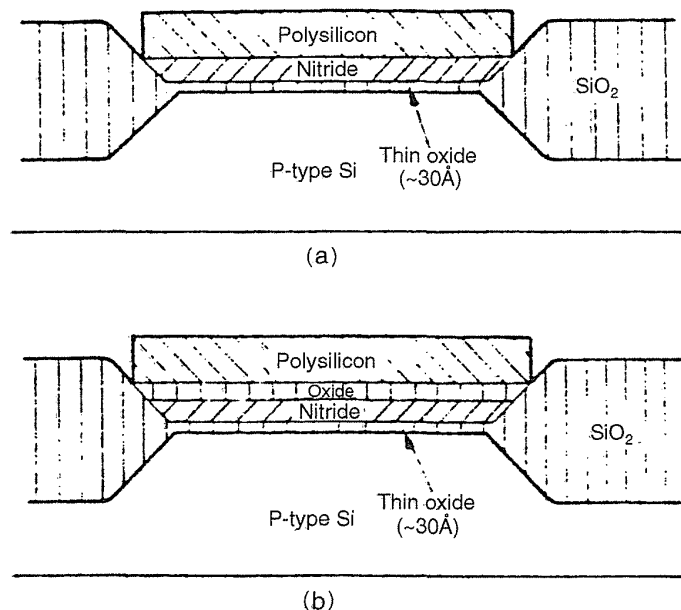


Figure 6.27 Cross-sectional views of (a) SNOS and (b) SONOS capacitors (after Chen [6.57]).

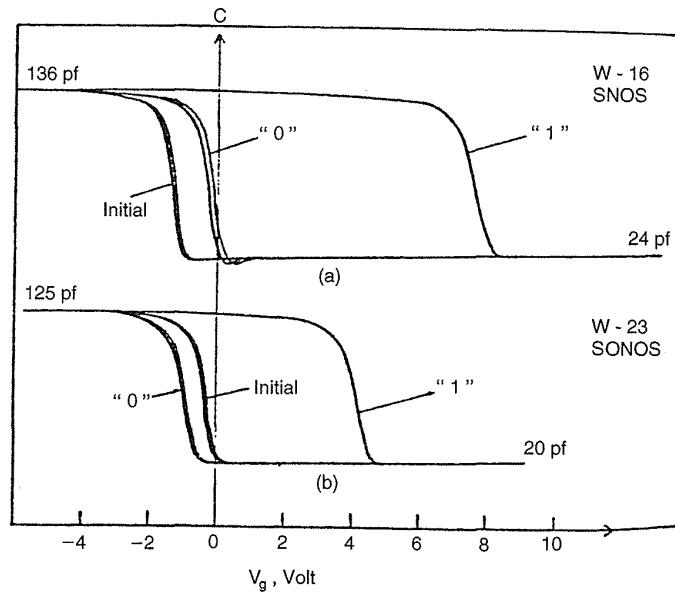


Figure 6.28 C-V plots of SNOS and SONOS capacitors after application of negative- and positive-voltage pulses (after Chen [6.57]).

The nitride trap density, conductivity, and composition can also be tailored vertically in the MNOS memory gate to improve NVSM retention and endurance. By adjusting fabrication process parameters, a two-layer silicon nitride memory dielectric can be formed in which the layer immediate to the tunnel oxide is to be maximized for memory charge traps, and the second layer formed, minimized for trap defects. The charge traps are thus restricted to a region that is most effective for memory threshold shifts. Retention and endurance of the device are improved as charge leakage and charge centroid migration are bounded by the “trap-free” second nitride layer preceding the gate electrode [6.58].

Series MOS structures merged with the MNOS memory transistor (see Fig. 6.29) are used to eliminate depletion-mode operation of the MNOS, as well as to reduce yield and reliability failures due to memory dielectric pinholes over heavily doped source and drain diffusions [6.59]. Such structures also have increased drain-source breakdown voltages, as well as greatly reduced soft turn-on leakages. To eliminate “sidewalk” parasitic leakage currents, cross gate MNOS memory structures have been effective [6.60]. Figure 6.30 shows the center cross-sectional view along the width direction in the gate region of a typical step gate MNOS transistor. The transistor region between the thick gate oxide and thin memory oxide region functions as an MNOS device with gradually increasing oxide thickness. This region has been termed the sidewalk and causes parasitic leakage currents, as is illustrated in Fig. 6.31. Figure 6.32 is a composite schematic of the cross gate MNOS memory structure. Along the width of the gate channel, the sidewalks are removed, with the gate extending beyond the metal electrode. The field oxide at the edge of the MNOS gate width prevents the formation of any parasitic conductive path due to fringing

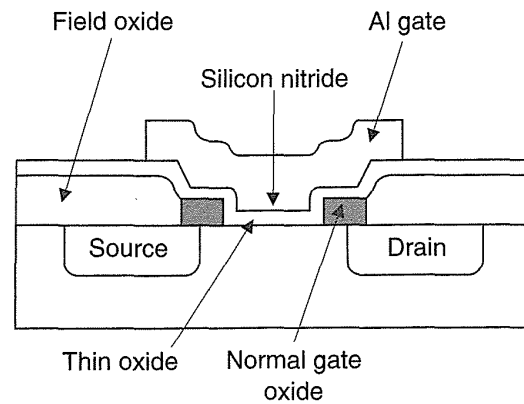


Figure 6.29 Schematic showing representative section through MNOS memory transistor (after Hsia [6.59]).

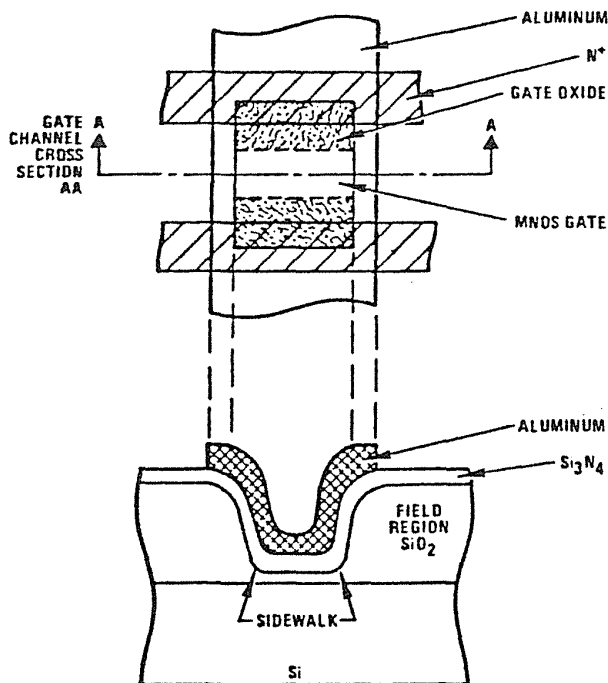


Figure 6.30 Typical MNOS device structure with cross section AA showing the "sidewalk" region (after Hsia [6.60]).

fields. Figure 6.33 shows the transfer characteristics of the cross gate MNOS memory device without the parasitic sidewalk leakage current. The improved margins that resulted from eliminating the "sidewalk" parasitic leakage currents permit single-transistor memory arrays and improved MNOS memory array density, since the more conservative two elements per lot storage/sense techniques are no longer needed, even though the cross gate memory cell is larger in area.

The use of an on-chip program voltage so that a single low-level V_{DD} supply (i.e., 5 V) can be used for EEPROM operation imposes additional design considerations on the memory cell [6.61]. In a conventional, fully aligned MNOS (SNOS) memory transistor, a large program current flows as a result of drain breakdown due

Figure 6.31 Typical MNOS transistor characteristics with parasitic leakage current problems (after Hsia [6.60]).

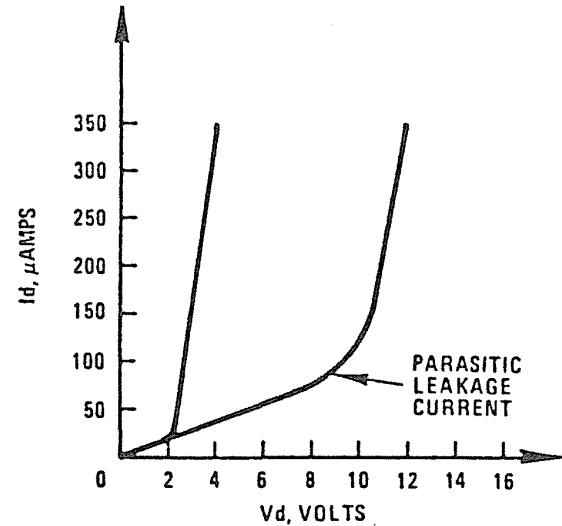


Figure 6.32 The cross-gate MNOS memory device (after Hsia [6.60]).

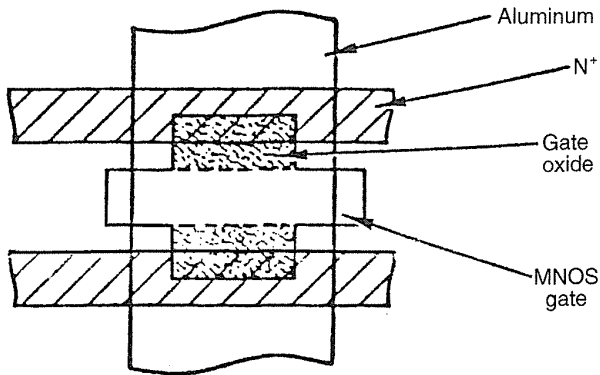
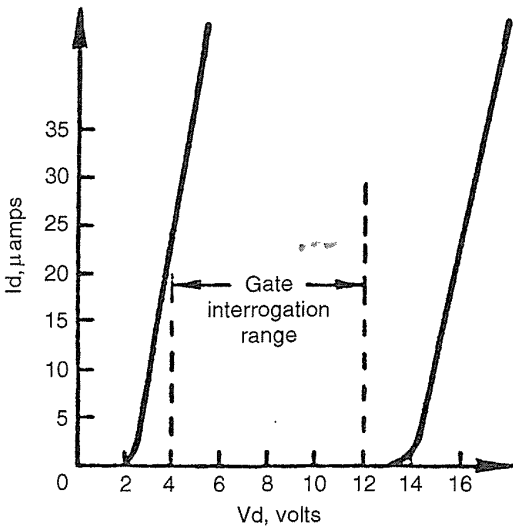


Figure 6.33 Typical device transistor characteristics obtained with the cross gate MNOS memory device (after Hsia [6.60]).



to hard ground biases on gate and substrate. The on-chip program voltage supply current cannot readily sustain such a large programming current to reduce the breakdown voltage. Therefore, an off-set MNOS memory cell structure is utilized, as shown in Fig. 6.34. The $N - N^+$ off-set drain (and source) structure, together with the step polysilicon gate, results in two field-strength regions under the gate electrode (see Fig. 6.35). With the off-set, the breakdown voltage is dependent on impurity concentration. In addition, optimization of the breakdown voltage must be determined in connection with the relationship of concentration and voltage drop through the channel region. Figure 6.36 shows these two relationships and the selection of an N implant dosage of $3 \times 10^{12} \text{ cm}^{-2}$ to $10 \times 10^{12} \text{ cm}^{-2}$ for optimal results.

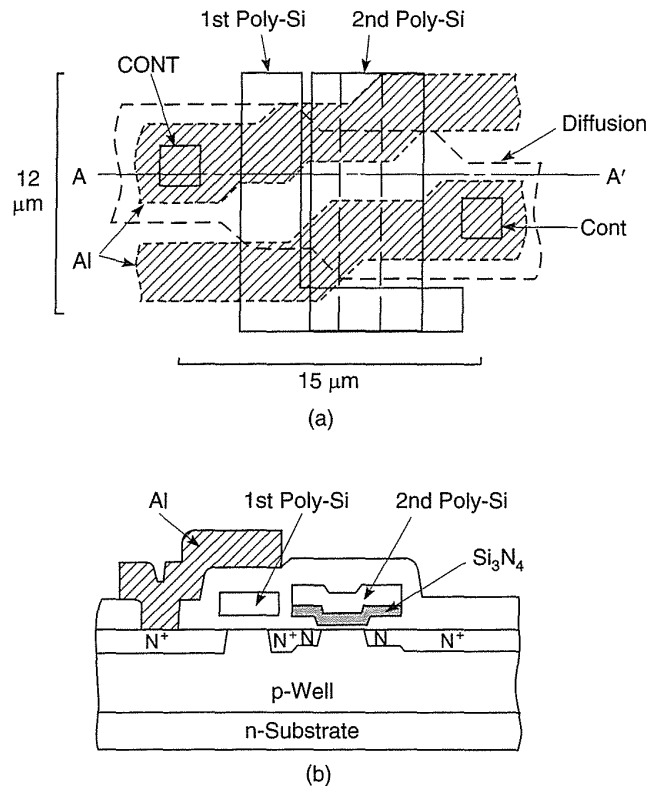


Figure 6.34 Memory cell (a) layout pattern and (b) cross section for 64Kbit EEPROM (after Yasude [6.61]).

6.2.3 NVSM Application — Circuit Design Examples

Attention to design margins through circuit design enhances circuit performance and improves reliability. First-generation MNOS NVSM products, for example, used two-element-per-bit storage and differential sensing to provide for the necessary margins to achieve performance and reliability [6.62]. In Fig. 6.37, note

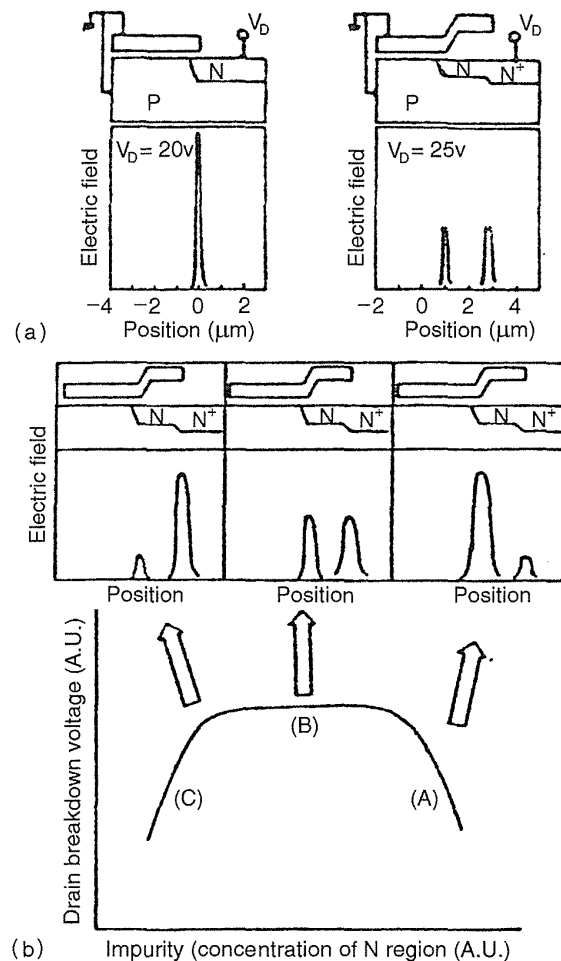


Figure 6.35 Electric-field strength under gate electrode. (a) Comparison between conventional MNOS device and high-voltage-structure MNOS device. (b) Drain breakdown voltage versus impurity concentration of N-region, in conjunction with electric-field strength (after Yasuda [6.61]).

that the memory data bit is stored as the difference in threshold voltage between the two MNOS transistors in the two legs of the flip-flop load. The load control transistors are bypass elements which ensure that the flip-flop latching current is determined by the high-conductance state memory transistor. The latching sense flip-flop is the difference sensing circuit for data output. Improvement in device technology and the continuing pressure to achieve high-density storage per unit area in silicon provided the incentive for single-element storage. That is accomplished with the use of a reference storage element plus a balanced bitline (see Fig. 6.38), in which a reference bitline is used for each of the two MNOS storage arrays shared by the differential sense flip-flop circuit in common [6.64]. Figures 6.39 and 6.40 are similar sensing schemes using high noise-immunity circuit design techniques to achieve reliable high-speed sensing of floating gate NVSM devices. In Fig. 6.40, the reference voltage for the flip-flop sense circuit is derived in the “dummy” memory cells, which are erased and programmed in every Flash erase cycle of the multi-megabit Flash E²PROM [6.65]. The characteristic of the “dummy” cell is the same as that of the

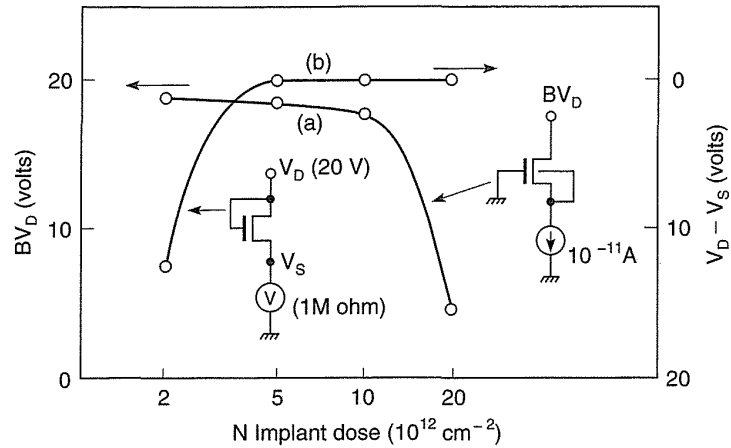


Figure 6.36 N-implant dose dependence of (a) breakdown voltage and (b) voltage drop through MNOS device (after Yasuda [6.61]).

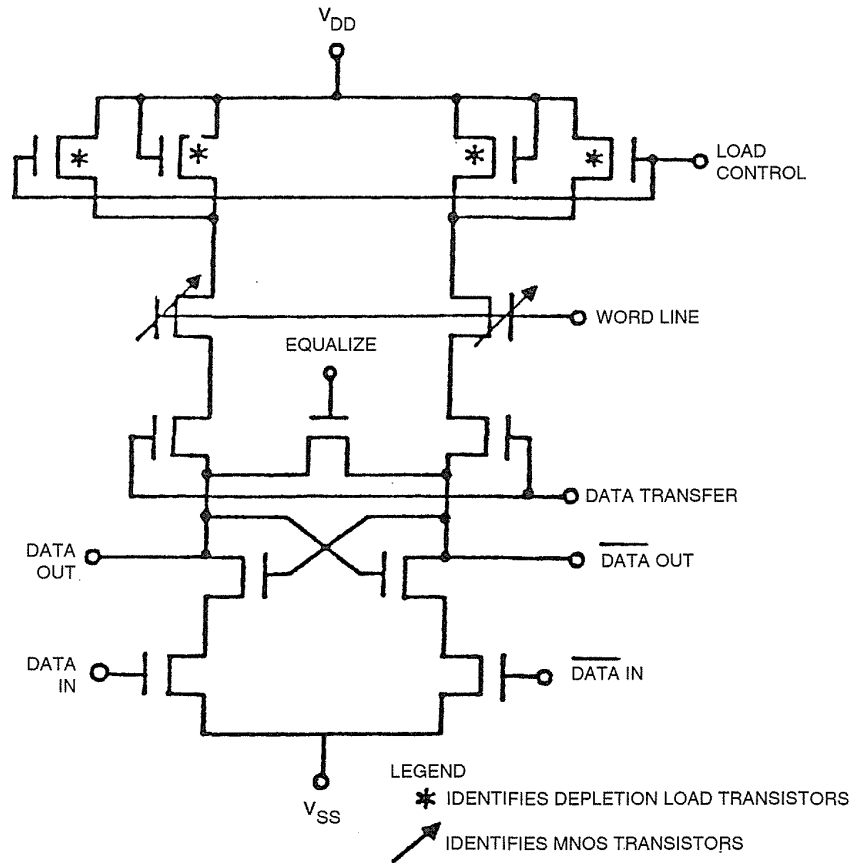


Figure 6.37 Two-element-per-bit MNOS memory cell (after Hsia [6.62]).

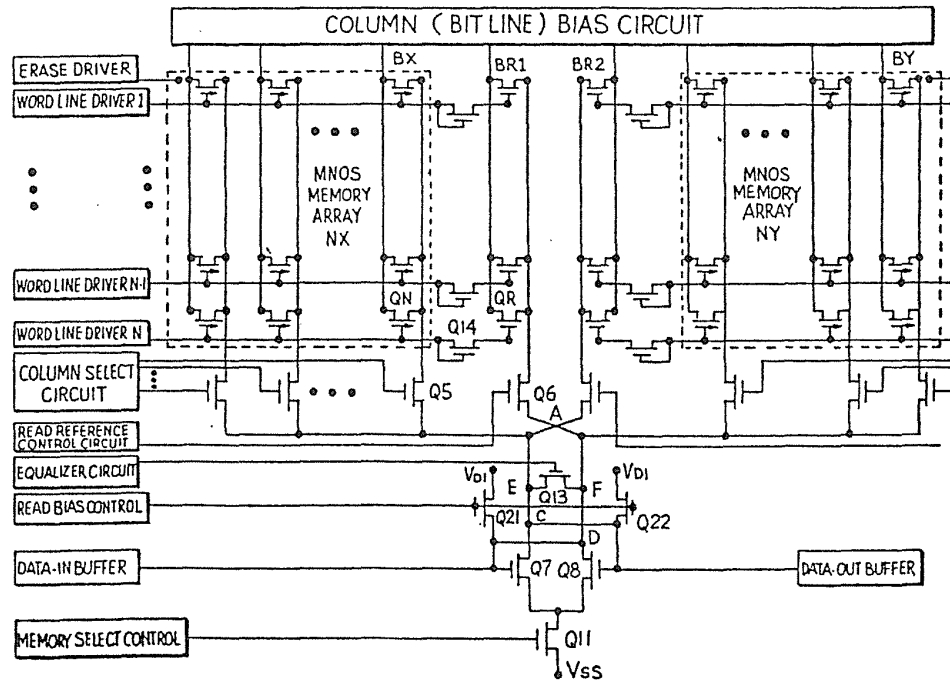


Figure 6.38 Referenced threshold, balanced bitline sensing of MNOS data storage (after Hsia [6.63]).

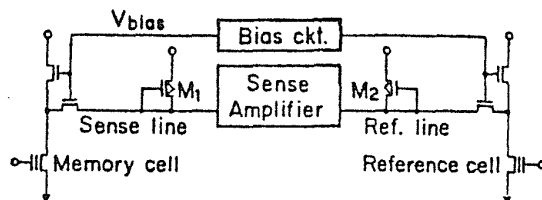


Figure 6.39 EPROM sensing scheme (after Imamiya et al. [6.64]).

data cell. However, the capacitances in the array are such that the reference level is loaded so that it is at a value between a “zero” (programmed state) and a “one” (erased state).

For many EEPROM applications, single-bit endurance failures have been the limiting reliability constraint. To improve endurance reliability, many circuit techniques are utilized, such as redundancy of data storage so that the stored data can be retrieved correctly even if one of the memory devices in a two-element-per-bit storage scheme fails. Figure 6.41 illustrates the schematic of a redundant storage cell concept designated as the “Q” cell [6.66]. The cell is composed of two identical EEPROM memory transistors, which are programmed identically with the same data through adjacent bitlines BL_1 and BL_2 . The memory read operation is accomplished separately from both transistors with separate sense amplifiers. The data are, in turn, combined through a logic NOR operation. The correct datum is read out as

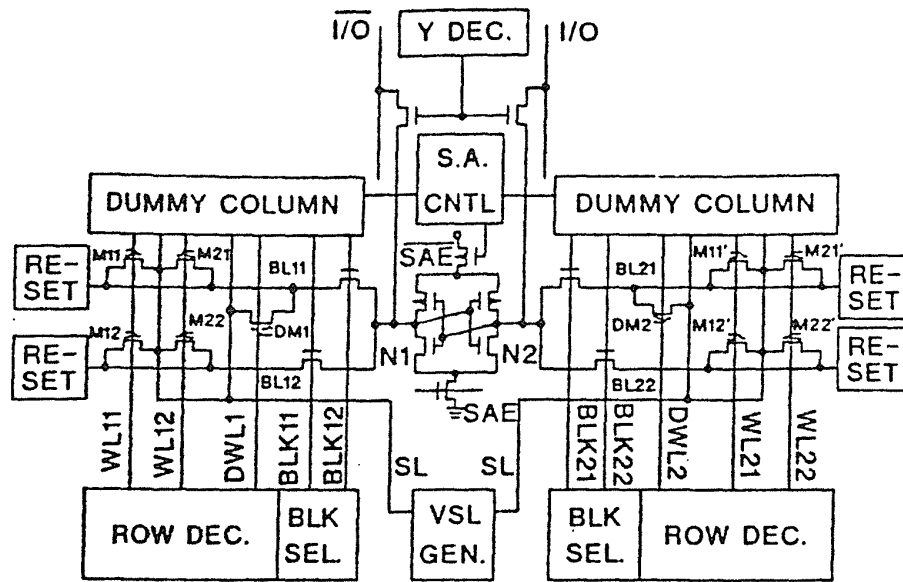


Figure 6.40 Block diagram of sense circuit (after Kobayaski et al. [6.65]).

long as one of the two EEPROM transistors and its corresponding data path is not defective. Assuming an initial 100% goodness screening for parts acceptance, the reliability of parts in use is greatly enhanced by the application of the redundant storage, because the probability of an adjacent cell wearing out (or failing endurance) at the same time is exceedingly low.

To realize high-density EEPROMs with high reliability, error correction circuits (ECCs) are often utilized [6.67–6.70]. ECCs are effective in improving EEPROM reliability failures due to random bit failure caused by tunnel oxide breakdown in erase/write endurance. We can derive the first-order improvement in product reliability as follows. The chip failure probability without ECC, P_o , is simply

$$P_o = 1 - (1 - q)^{1M} \quad (6.35)$$

in which q is the bit failure probability.

In the case of the use of 4 parity bits generated from 8 data bits, that is, ECC (8,4), the byte failure probability, q_A , is given as the probability of more than 2 bits out of 12 bits failing, since ECC corrects for single-bit errors,

$$q_A = 1 - (1 - q)^{12} - {}_{12}C_2 q (1 - q)^{11} \quad (6.36)$$

and the megabit (or 128 KB) chip failure probability, P_A , is given as

$$P_A = 1 - (1 - q_A)^{128K} \quad (6.37)$$

Figure 6.42 illustrates the calculated result of the use of EEC techniques to improve product reliability, in the case of a megabit EEPROM, using three alternative EEC choices [6.69]. The orders of magnitude improvement in reliability with ECC is very impressive.

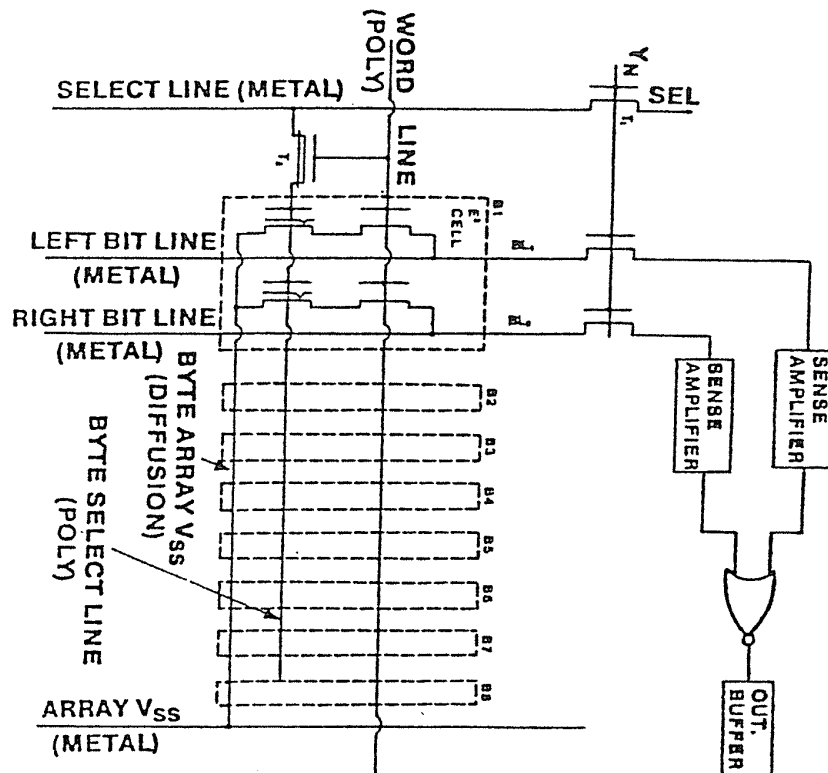


Figure 6.41 Schematic of the byte organization using the Q-cell concept (after Cioaca et al. [6.66]).

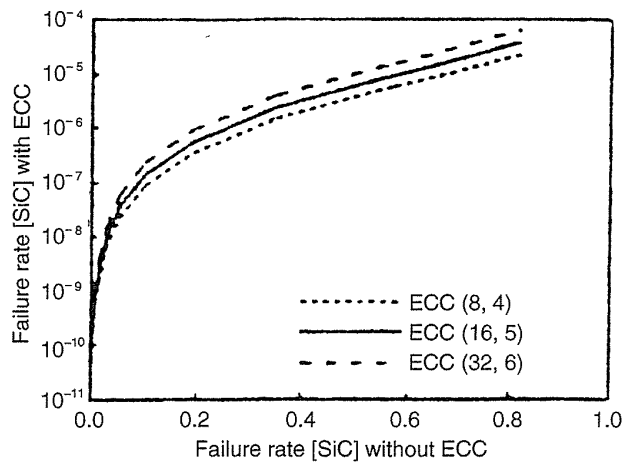


Figure 6.42 Calculated failure rate of 1Mbit EEPROM caused by random bit failure (after Terada et al. [6.69]).

6.3. RELIABILITY TESTING AND YIELD

All semiconductor devices are manufactured with numerous controls in place to guarantee that the manufacturing parameters are stable and are on the process design target. In general, these controls are re-checked by measuring test structures on the final product wafer plus various performance tests conducted on the product itself. Parametric test devices provide information about how well the process achieved the goal of meeting parametric specifications. Assuming that parametric targets are achieved, functional tests conducted on the product will supply data that relate to the yield of the product, which, in turn, reveal faulty parts due to design-related sensitivities to process variations along with faulty parts caused by random defects. Yield is defined as the ratio of functional parts to the total number of parts manufactured in a wafer lot or specified period of time.

$$Y = \text{Number of good chips} / \text{Total chips fabricated} \quad (6.38)$$

A basic process yield can be computed based on the number of initially functional parts from the wafer lot. This yield number rarely is representative of the final yield because further parts fallout after burn-in.

Before IC devices can be installed into systems, additional testing is usually performed after the parts are subjected to burn-in in an attempt to remove marginally reliable devices that would fail in a short period of time after being placed into service. Burn-in testing is a mildly accelerated life test that is intended to cause devices with reliability defects to fail, effectively removing most of the devices that fail in the infant mortality (early-life) failure region of the “bathtub” curve.” The number of infant mortality failures is generally kept in the production line database along with the number of initially nonfunctional parts detected at initial functional test. A yield figure that accounts for all functional parts after burn-in is the true production yield.

Reliability testing beyond burn-in is typically performed on individual part types using procedures prescribed by either the manufacturer’s standard procedures or by military procedures. In general, life testing involves two broad categories of data gathering: failed part field return and accelerated life testing. Gathering reliability data by tracking the failures of parts in the field is an effective, though very expensive, method, even if it is possible to have a complete environmental history of the part while in service. The most common method of assessing parts reliability is to run accelerated life tests on a randomly selected set of parts from one or more wafer lots. Unfortunately, trends in failure rate requirements are becoming more demanding as VLSI technology progresses. As Crook¹ [6.30] has noted, trends in infant mortality and long-term life goals have been projected through the year 2000. Based on this projection, it will be necessary to achieve a long-term life failure rate of 10 FIT by the end of the century.

The reduction in failure rate goals has profound implications for life testing as is commonly described in various military and commercial testing procedures. As

¹This paper by D. L. Crook is recommended to the reader for projecting testing into a framework of future technology.

mentioned above, life testing is performed on a sample of parts from the production line. The sample size is dictated by requirements for FIT rate and confidence limits needed to have an acceptable assurance of reliability. Typical life tests are performed at 125°C for 1,000 hours. If we assume that the failure distribution is Poisson statistics, then the number of samples required for a life test is easily calculated. Table 6.8 illustrates the sample-size requirements based on some example failure rates and confidence limits. Clearly, in order to achieve the failure rate goals projected for the end of the century, sample size for life testing will have to be very large.

We may add to this the fact that chip complexity is increasing at a rate that would result in 100 million transistor chips by the end of the century as seen in Fig. 6.43. Unfortunately, as chip complexity increases over the next decade, the cost of each chip will be on the order of several hundred to a few thousand dollars. At this cost level, life testing of the scale dictated by these projections will not be cost-

TABLE 6.8 THE EFFECT OF FAILURE RATE GOAL ON THE MINIMUM SAMPLE SIZE REQUIREMENTS, ASSUMING POISSON STATISTICS (AFTER CROOK [6.30]).

Failure Rate Goal (FIT)	No. of Devices 90% UCL		No. of Devices 60% UCL	
	0 Fails	2 Fails	0 Fails	2 Fails
1000	355	835	143	463
100	3550	8350	1437	4630
10	35,500	83,500	14,370	46,300

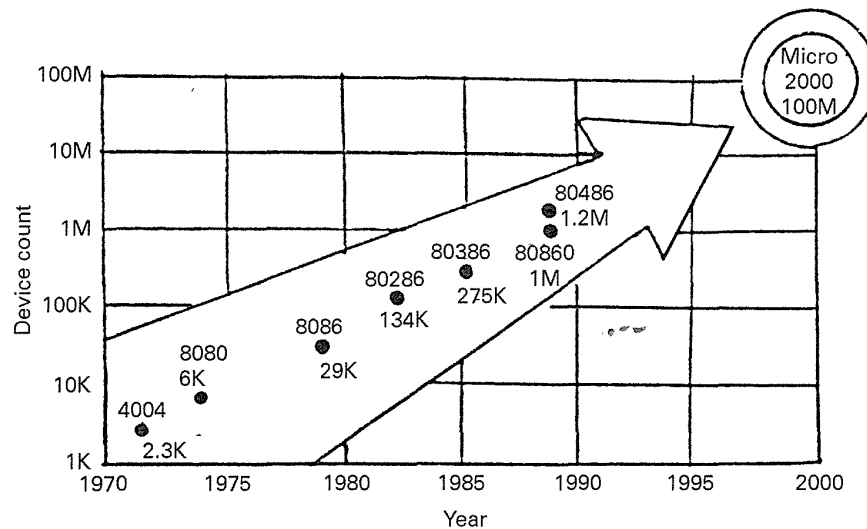


Figure 6.43 Microcomputer transistor count per chip versus time (after Crook [6.30]).

effective. It is very clear that some method other than product life testing is required to assess chip reliability.

During the past 15 years or so, a number of research efforts have been initiated to provide a means by which manufacturers can effectively predict the wearout lifetime of IC devices by using information about physical failure mechanisms. This research effort has produced the well-understood physical failure models that were discussed in Section 6.2.1. Given these physical models, we can construct test structures and test procedures that will enable routine wafer-level monitoring of lifetime limiting mechanisms. Wafer-level reliability testing is a highly effective tool for both in-line and end-of-line reliability monitoring on current technologies. JEDEC Standards are being defined for the three reliability limiting failure modes (electromigration, hot-carrier damage, and oxide wearout) and will soon be in widespread use.

Section 6.3.2 describes the proposed standard reliability test methods in sufficient detail that they can be implemented on a wafer fabrication line. It must be understood that the monitoring and process control required for production of high-reliability integrated circuits is very complex and is becoming more so as the minimum fabricated geometry decreases in size. No single method of monitoring will completely guarantee reliable chips. However, a combination of in-line monitoring, along with end-of-line wafer-level reliability monitoring, will provide both the necessary feedback needed for good statistical process control and valuable “disaster alarms” that will minimize the chances of installing chips containing known global reliability hazards into critical systems.

Before discussing the wafer-level reliability testing procedures mentioned above, it is necessary to point out the limitations that future chip complexity will place on the use of wafer-level reliability testing as a tool for process control. Current technologies are at a level of complexity that permit effective use of wafer-level reliability testing as an end-of-line reliability monitor. However, based on projections of future technologies [6.30], end-of-line wafer-level testing will not be sufficient to address the 10 FIT failure rate requirements of the future.

First, we must realize that, as device geometries scale, the intrinsic reliability margin becomes progressively smaller. This point was discussed earlier and illustrated in Fig. 6.23. Scaling to current technologies necessitated major improvements in contamination control to compensate for the shrinking intrinsic reliability margin.

The continual improvement in processing technology, which has reduced the number of defect-related failures (infant mortality), has a dramatic effect on the ability to detect any remaining defects. Crook uses oxide reliability as an example of a traditional reliability limiter in MOS technology and points out that statistics on oxide failure (Fig. 6.44) indicate that the defect tail of the cumulative failure distribution is becoming a significantly smaller percentage of the total population. This leaves a cumulative failure distribution that is controlled primarily by intrinsic behavior. Monitoring the defect tail with test structures will become a statistical problem similar to the problem of life testing an entire functional device. By the end of the century, it will at best be possible for test structures to monitor one-twentieth of the active gate area of the chip if the test capacitors are confined to the scribe lines. The only way to be able to monitor the defect failure of the oxide is to assign 100% more

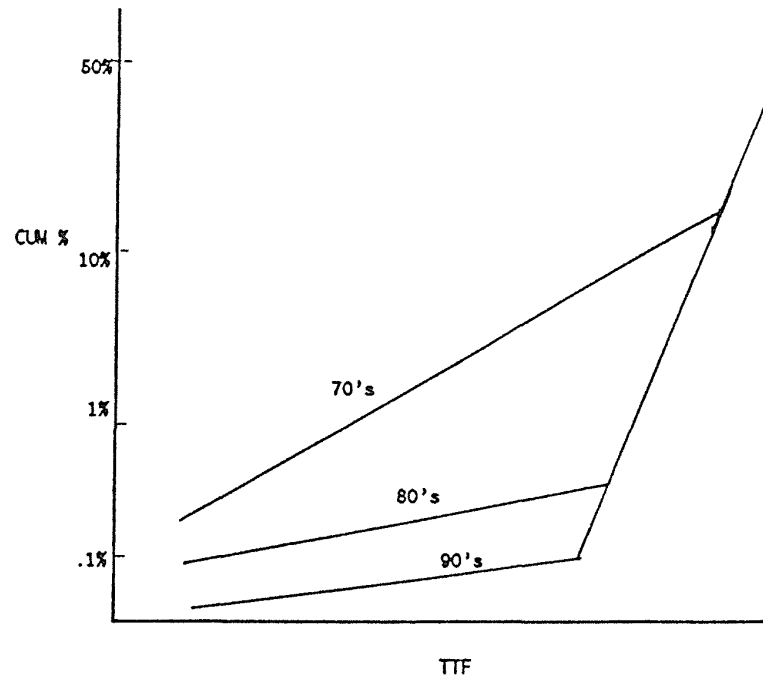


Figure 6.44 Examples of typical distributions for oxide defects in the past, present, and future (after Crook [6.30]).

area to the test structures. This option is surely unacceptable to any manufacturer who produces chips to sell for profit.

A similar argument involving test structure scale could be made for the other failure mechanisms, which leads to the conclusion that wafer-level reliability monitors are not useful as the primary process control monitor. Wafer-level reliability testing must be augmented with monitors that are closer to the processes that control the production of reliable materials. Crook suggests that the most promising place to install reliability monitors is far up the processing fishbone, as illustrated in Fig. 6.45. Each step in the process must have monitors in order to ensure that each step contributes its part to the overall reliability of the product. This, in turn, implies that reliability assurance must depend on a high level of confidence in these processing step monitors. End-of-line wafer-level reliability testing will continue to provide a check for reliability disasters, much as parametric tests on a small number of transistors within the PCM serve to provide an assurance that all of the transistors in a wafer are performing within the designed limits.

The testing technology required for monitoring well into the fishbone of each processing sequence is beyond the scope of this chapter. We will supply some guidelines for end-of-line and in-line wafer-level reliability testing that will serve existing technology well, while providing a model for methods that will be useful in the future.

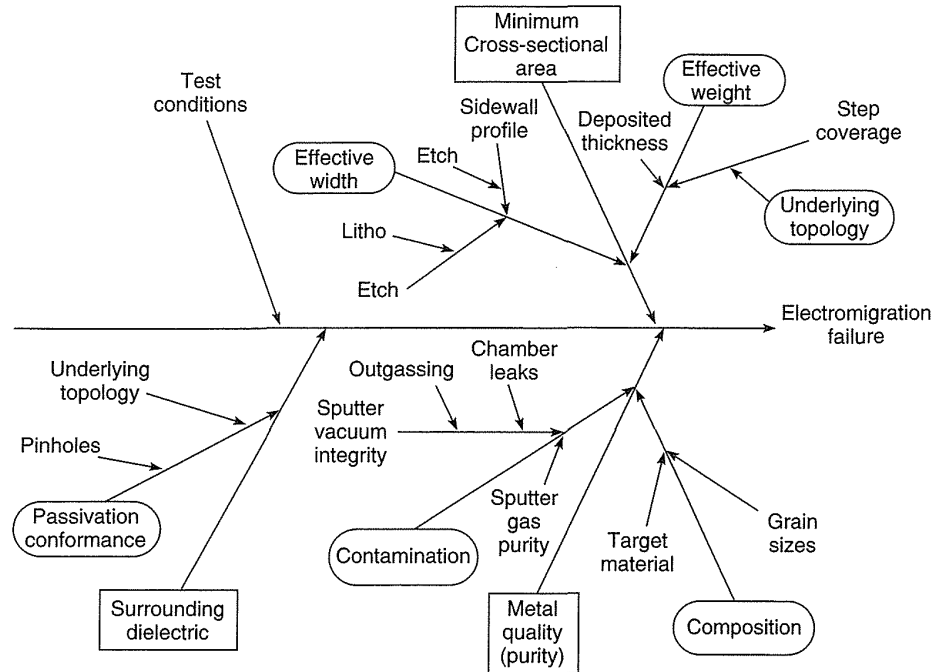


Figure 6.45 Fishbone diagram showing input variables that affect electromigration time-to-fail (after Crook [6.30]).

6.3.1 Validation Testing : Reliability Assurance in Manufacturing²

Life test reliability data validate accelerated tests used by manufacturers and consumers alike. Additional reliability data on the breakdown of defect mechanisms and failure modes provide the feedback data necessary not only to improve the manufacturing process, but also to direct future efforts in the areas of process, design, and manufacturing.

Reliability testing must utilize test procedures, sampling plans, and data analysis procedures that are specified in JEDEC standard methods. As of 1992, no official standard was set out in the JEDEC files. The methods described in this section provide a snapshot of the preliminary standards at this time. It is likely that only small changes will be made in these methods when the official JEDEC Standard is published.

The lifetime models used for all the methods included herein are empirical and represent a best fit to existing data. As dimensions scale downward, there is likely to

²This section contains paraphrased and extracted material from: FINAL REPORT—Develop Quality Assurance Procedures Based on Wafer Level Testing, by Vance C. Tyree, written for Defense Advanced Research Projects Agency under Contract No. N00140-87-9263, April 10, 1991.

be some deviation in predicted lifetime if the mechanism responsible for failure changes. In this section, all efforts are made to point out the known weaknesses in the existing models.

Validation testing involves two inseparable parts which establish that the fabrication line first is not building in some fundamental reliability hazards, and second, is able to assess the degree to which the design of the part itself contributes to any excessive stress that could lead to early failure.

Wafer-level reliability testing is a powerful tool for measuring the generic quality of the fabrication process itself. Generic quality is absolutely essential to being able to produce reliable parts of any type. In the case of NVSM, in which intentional “overstress” is applied to write data into the device, a tight statistical quality control with rapid, accurate feedback of insulator quality will form the basis of long-life NVSM parts.

Waferlevel reliability testing permits monitoring reliability limiting mechanisms at the wafer level before the parts are packaged and placed into service. This test method must be performed very rapidly in order not to delay the wafer production flow. Highly accelerated stress is applied to a test structure that is designed to represent some worst case at risk structure permitted in a design. Time-to-fail data are gathered and analyzed to assess the relative quality of the wafer. These data are compared with similar data taken from a known good wafer lot and used to decide whether built-in reliability hazards are produced in the wafer lot under test. Since the basis of the quality assessment is the use of test data from highly accelerated tests, it is important to recognize the limitations of such testing relative to the extrapolated life for the product.

6.3.1.1 Accelerated Testing and Its Limitations. Accelerated testing, by definition, enhances the rate of progress of failure mechanisms in order to study their relative importance in a product. The enhancement process involves increases in temperature, voltage, current, and so on, to levels that will result in acceleration factors large enough to reduce lifetime to a manageable value for test purposes. The difficulty is that, as acceleration factors become large, reliability limiting processes that are of secondary interest interfere with the mechanism of interest. If the mechanism is isolated in a test structure, moderate to very high acceleration factors can be used to study the mechanism.

When extreme acceleration factors are used, it is dangerous to extrapolate the results of tests to at-use conditions because either secondary mechanisms may interfere with projection or statistical scatter is so great that extrapolation over many decades yields ambiguous results. Figure 6.46 illustrates an attempted extrapolation of hot-electron degradation test results to at-use conditions. A well-tested and proven model for the mechanism must exist if such extrapolations are even possible. With such a model, experimental errors and defects occur, causing data scattering that leads to inaccurate extrapolation. The scatter boxes and associated median values of test data in Fig. 6.46 illustrate the uncertainty in extrapolation of accelerated test results over several decades. Accelerated life test data must be carefully examined for potentially ambiguous circumstances that can invalidate an extrapolation to at-use

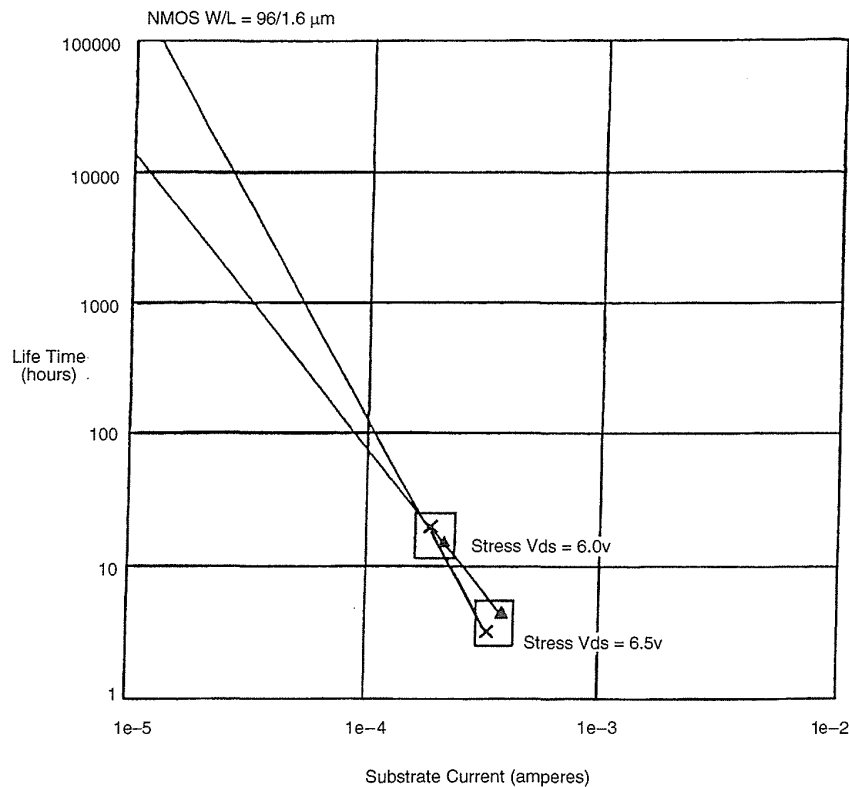


Figure 6.46 Hot-carrier lifetime extrapolation error.

conditions. The most common complicating factors in extrapolation of measured time-to-fail data are the presence of bimodal or multimodal distributions in the data and large standard deviations in the statistics. There is also considerable confusion about what statistical distributions to assume.

6.3.1.2 The Impact of Choice of Distribution. The two most common distributions in use in reliability testing are lognormal and Weibull. Many researchers in reliability have found that both distributions are useful, depending on the mechanism that is monitored or on stress conditions used in the life tests. When sample sizes are large, it may be possible to distinguish between the two distributions if the data contain relatively little scatter. However, in many instances small sample sizes are dictated, as in the case of wafer-level reliability testing. Wafer-level tests are usually confined to the space in the scribe lanes (or kerf) between chips, which represents a relatively small wafer area that must be shared with parametric monitoring test structures.

As shown in [6.71], when there is a difference in assumed distribution (e.g., lognormal versus Weibull) for a Standard Wafer-Level Electromigration Acceleration Test (SWEAT) structure unit [6.83], the ability to distinguish between

the two distributions is strongly influenced by the sample size. In the example in the reference [6.71], Fig. 6.47, a “perfect” data set shows no curvature when the SWEAT unit is assumed to be lognormally distributed and plotted on a lognormal graph. However, when the SWEAT unit is iterated, the distribution is no longer lognormal for the string of SWEAT units and shows slight curvature with a “perfect” data set. This curvature is so slight that, if the data sample size is small and contains scatter, there is no way to distinguish the deviation from lognormal. Evidently, attempting to extrapolate what may be a quasi-lognormal distribution to at-use conditions from a small sample size is going to yield a significant error in hazard rate. This error can become large when we are attempting to extrapolate highly accelerated test data to at-use conditions that are several decades longer in time than the actual test time. Noise in the data compounds an already difficult extrapolation of a distribution that is not a straight line on a lognormal graph, as was the case with the SWEAT example.

The choice of an appropriate distribution is significantly influenced by the acceleration factors used in the life testing. The distribution for failure in at-use conditions is very likely different from the distribution that appears to match data from accelerated tests. Life testing strategy must account for the fact that highly accelerated tests may not permit extrapolation to at-use conditions because multiple failure mechanisms may significantly influence the outcome.

6.3.1.3 Recognizing Bimodal Distributions. Bimodal, and in some cases multimodal, distributions in life test data are a frequent source of error in at-use condition extrapolations from accelerated test data. The best way to deal with this

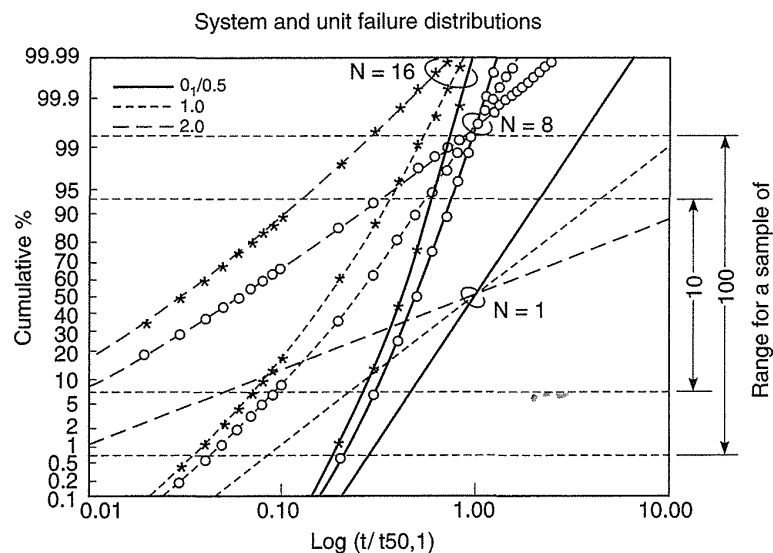


Figure 6.47 Distributions of individual SWEAT units compared with distributions of iterated SWEAT units (after Crowell et al. [6.71]).

problem is to create test conditions that do not stimulate competing reliability-limiting mechanisms. Unfortunately, only rarely can a practical test environment be created that will permit such simplification. Testing time considerations will force higher stress levels that, in turn, force the data analyst to deal with bimodal distributions.

Assuming that each mechanism has its own sigma and mean, we can express the cumulative distribution function (CDF) as

$$F(t) = \sum_{i=1}^k q_i * F_i(t) \quad (6.39)$$

where q_i is the fraction of the population that belongs to mechanism i .

Note that

$$\sum_{i=1}^k q_i = 1 \quad (6.40)$$

If we have a bimodal distribution ($k = 2$), then we can express the CDF as

$$F(t) = q_1 * F_1(t) + (1 - q_1) * F_2(t) \quad (6.41)$$

where q_1 would be an early fail population and q_2 would be the main population expressed in terms of the early population: $q_2 = 1 - q_1$. $F(t)$ could equally well be expressed in terms of the main population.

Figure 6.48 shows the general form of lognormal plots of bimodal distributions in which each population has two well-defined means and various sigmas. In this set of examples, $\ln(t_{50}) = 0$ for the freak (early) population, and $\ln(t_{50}) = 10$ for the main population. Also assume that $q_e = 0.1$ and $q_m = 0.9$. The various sigmas of both populations include 1/2, 2.0, and 5.0. The vertical scale is the normalized cumulative fail percentage, and the horizontal scale is the natural log of the lifetime. The first thing to note is that, as long as the sigmas of the two populations are relatively small, it is easy to recognize the presence of two populations simply by the fact that the lognormal plots are not linear. Also, note that the upper vertical bars indicate that 90% of the freak (early) population lies to the left of the vertical bar, and the lower vertical bars indicate that 90% of the main population lies to the right of the vertical bar. Finally, observe that it is intuitively possible to separate the mean and sigma from the plot as long as the sigmas of the two populations are not too large.

Theoretically, given knowledge of the form of the CDFs of the two populations, their mean and sigma can be extracted as long as the two populations do not overlap very much. Figure 6.49 illustrates a typical bimodal lognormal plot of life test data indicated by the circles on the graph. The squares show the lognormal plot of the extracted early population, where $q_e = 0.2$, and the triangles show the lognormal plot of the extracted main population, where $q_m = 0.8$. Clearly, any attempt to fit the set of data points to a line on the lognormal graph will lead to a grossly distorted mean and sigma.

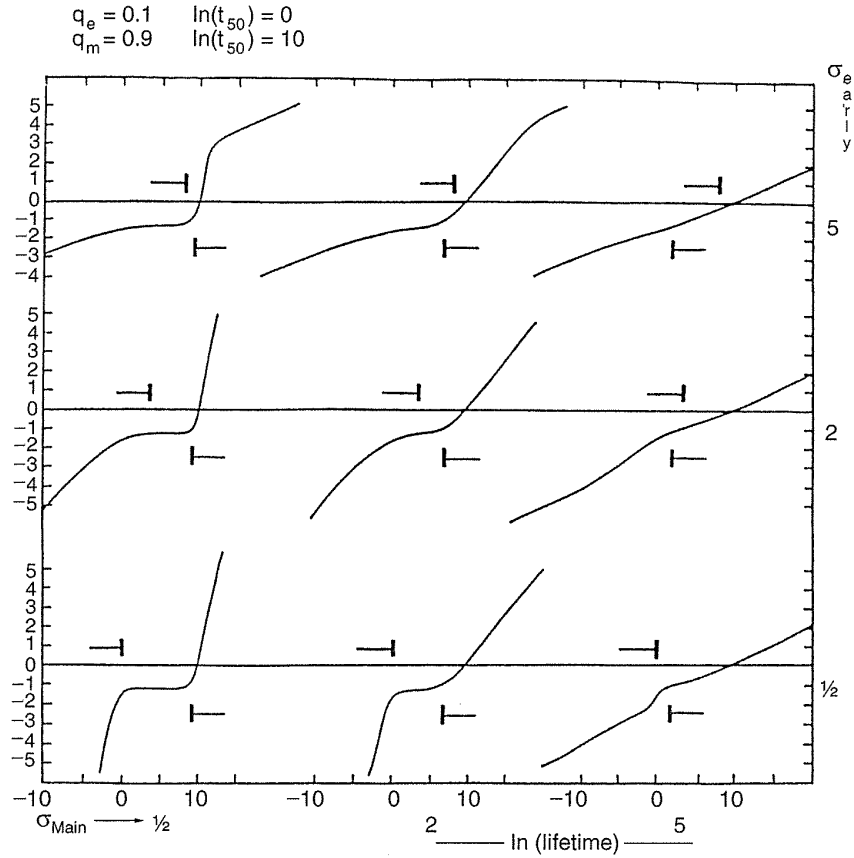


Figure 6.48 Bimodal lognormal distributions.

Mathematically, the CDF of the entire data population is represented as

$$F(t) = q_e * F_e(t) + q_m * F_m(t) \quad (6.42)$$

Solving for $F_e(t)$ yields

$$F_e(t) = \frac{F(t) - q_m * F_m(t)}{q_e} \quad (6.43)$$

Assuming that the early and main populations do not overlap much, the early part of the population can be expressed, assuming that $F_e(t)$ is approximately zero, as

$$F_e(t) = \frac{F(t)}{q_e} \quad (6.44)$$

Similarly, assuming that $F_e(t)$ is approximately one, the main population can be expressed as

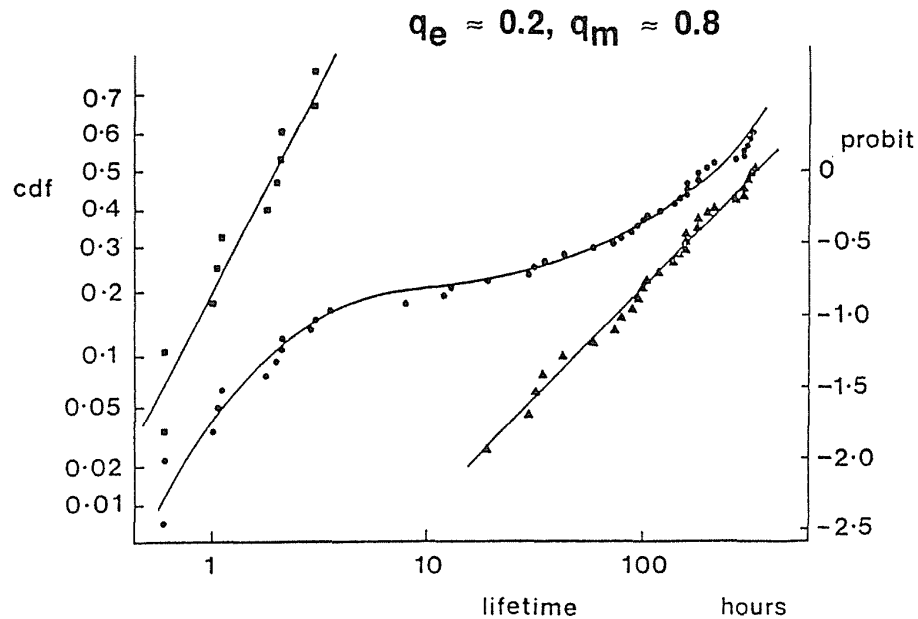


Figure 6.49 Life test data containing early and main populations.

$$F_m(t) = \frac{F(t) - q_e}{1 - q_e} \quad (6.45)$$

The early populations are usually a result of the presence of “weak” structures caused by random defects. As has been indicated, these early failures can be separated from the main population, and permit the evaluation of the global quality of the test structures. Unfortunately, when conducting wafer-level tests that are highly accelerated, the distributions become multimodal because other less dominant mechanisms become activated. The separation process becomes impossible, and some other means must be devised to relate wafer-level reliability test results to at-use conditions. A method for dealing with this additional complication is to create a test structure and test method calibration hierarchy.

6.3.1.4 Hierarchical Calibration: Dealing with Nonideal Data Sets. By recognizing the limitations that highly accelerated testing impose, it is possible to develop wafer-level test structures, test methods, and data analysis procedures that provide valuable tracking of product reliability. Highly accelerated test structures can be defined to minimize the deviation from the life models empirically derived from large sample sizes at more moderate accelerated test conditions. This allows simple representation of measured data from the highly accelerated tests for the purpose of comparison of one wafer lot with another, even though extrapolation to at-use conditions is invalid. Traceability to at-use conditions is achieved by using a database of moderate acceleration factor tests performed on test structures and product or product-like functional devices from calibration wafers that also contain the wafer-level reliability test structures.

This hierarchy of testing creates a well-controlled reliability tracking environment for wafer fabrication. It is important to realize that this hierarchy has interpretation limits. As long as wafer-level test results remain within prescribed bounds, there is no reason to be concerned that the product life expectancy has changed from the reference lot. However, if data from the wafer-level tests indicate either an increase or a decrease in accelerated test lifetime, then interpretation of the test results becomes more complex.

The simplest result to deal with is a consistent increase in wafer-level test lifetime. This indicates that the material under test is becoming more robust for some reason that hopefully is known to the fabrication manager. If this is the case, then it is necessary to re-calibrate the hierarchy and continue monitoring.

Reliability tracking to maintain quality becomes more difficult when there is a reduction in wafer-level test lifetime. If the reduction is relatively small, then the temptation is to ignore it as a statistical glitch caused by relatively small sample sizes. This can be dealt with by having a clear idea of the relationship of acceptable confidence limits (say 90% or 95%) to the calibration point in the hierarchy of test structures. It is clearly dangerous to try to extrapolate the highly accelerated test results to at-use conditions in order to assess the reliability degradation that is represented in the wafer-level test data. The correct procedure is to consult the cumulative database that exists on the wafer fabrication line in order to match the observed deviation with past experience with wafer-level tests, which have corresponding moderate acceleration factor tests, that are extrapolatable, and conclude its impact based on this comparison. In the absence of such a database, as would be the case at the start-up of wafer-level reliability testing, a database must be created.

Creation of a hierarchical reliability database involves periodically conducting moderate acceleration factor life tests (including correlation with a product or an equivalent Standard Evaluation Circuit) alongside wafer-level reliability test structures. Mechanism-specific reliability test structures on a test chip that contains wafer-level test structures for the same mechanism provide the means by which the wafer-level structures can be correlated with test results that can be extrapolated from moderate acceleration factor tests. Where possible, these test structures should be included along with every wafer lot that is fabricated. In any case, calibration wafers should be fabricated periodically to permit this tracking.

To complete the reliability correlation database, a functional device that is part of the product line should be life-tested from wafers from the same lot as the calibration wafers described above. In the absence of a large-volume product, as would be the case for a manufacturer who is involved primarily in ASIC fabrication, a Standard Evaluation Circuit (SEC) designed in the same gate array, or a standard cell library, could be used as a functional device to correlate moderate acceleration factor test structure results with a product or product-like device. An SEC should be designed to reflect the "typical" design style used for the majority of the devices produced on the fabrication line. For a fabrication line that is producing NVSM devices, a proper SEC would be a typical product chip. SEC life testing would be conducted at typical 1,000-hour life test conditions recommended for MIL testing, or at test conditions specified for the most critical application.

As the volume of reliability test data accumulates in the database, the uncertainty bounds for wafer-level test data shrink and permit definition of less ambiguous accept–reject criteria for wafer lots. This hierarchical calibration procedure is the most viable method for implementing a practical wafer-level reliability screening program on a fabrication line. The need for the calibration will remain as long as physical models cannot predict the lifetime of a material in the presence of multiple life-limiting mechanisms under highly accelerated stress testing.

6.3.1.5 Isolating Mechanisms—Models and Testing: TDDB. Time-dependent dielectric breakdown (TDDB) has gained considerable attention in recent years because, even though feature sizes of MOS devices have been steadily shrinking, the supply voltage has remained at 5.0 V. This trend is unabated to the sub-micron channel-length regime. As a result, with the thinner gate oxides, the in-use electric field has increased from 1 MV/cm to 2 MV/cm, which increases the rate of failure of gate oxides due to stress field.

The result of this scaling is that the quality of the oxide must be as close to theoretically perfect as possible. Thus, screens must be in place to catch global fabrication problems that could lead to early failure in the oxide. Stressing at moderate fields (3 to 5 MV/cm) has been used [6.12, 6.72] to study TDDB and to develop models for extrapolation to at-use conditions. Unfortunately, these tests require weeks of stressing to produce useful life data on oxides. If wafer screens are to be practical, stressing at very high fields (6 to 8 MV/cm) is necessary [6.31] to obtain results in a shorter time. Or even stressing to breakdown (8 to 10 MV/cm) must be used [6.77, 6.78] to gather data in minutes or seconds.

Test structures for oxide testing are simply capacitors constructed in various convenient configurations for either wafer probing or packaged testing. A test structure suitable for gathering statistical TDDB data on a fabrication process for purposes of calibration is given in Fig. 6.50 and fills a rather large die with a large array of capacitors in both the n-substrate and the p-well (or the reverse). This layout of capacitors allows wafer probe access to 38 capacitors in parallel for simultaneous stressing. The pad structure can be turned inside-out and converted to wire bonding pads to allow testing as packaged devices in order to eliminate the need for a probe station and to allow implementation of a large test fixture to stress large numbers of capacitor arrays simultaneously at different stress conditions. A total of 5 to 10 sites would be needed to gather data on 200 to 300 capacitors per wafer. The progress of data gathering is enhanced in such a structure by using step stressing [6.13] or a modified version of this method.

The test configuration illustrated in Fig. 6.51 allows measurement of capacitance, leakage testing to assess the condition of each capacitor, and a stress mode in which all capacitors are stressed in parallel through individual resistors to prevent a failure in one capacitor from modifying the stress to the others.

Moderate acceleration factor testing can be done using a modified-step stress testing procedure. A step stress (voltage step) time-to-fail equation [6.13] will help gather calibration data in a relatively short time. The step stress method described by Anolick [6.13] has been modified to permit convenient, moderate speed testing of

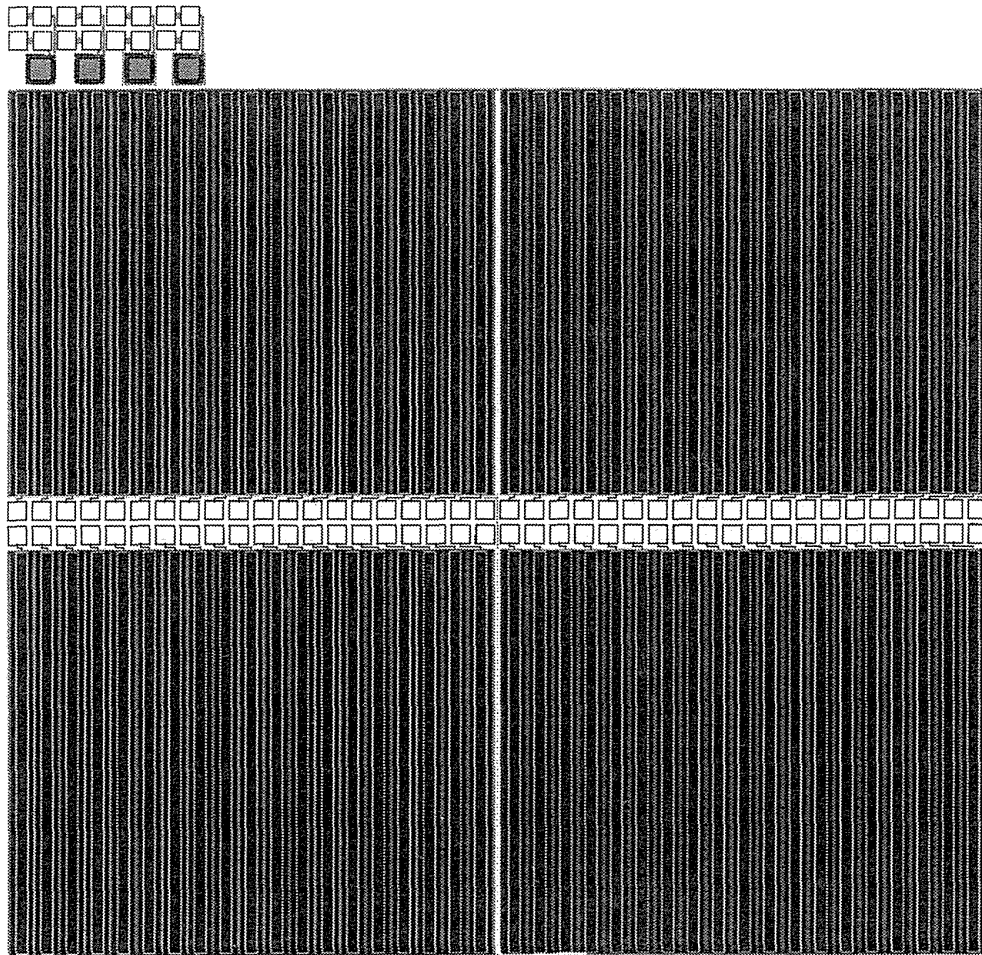


Figure 6.50 Wafer-probed TDDDB test capacitor array.

large numbers of capacitors at various fields. The test method diagrammed in Fig. 6.51 utilizes an exponential progression of stress time followed by a test for leakage at the end of each time interval. Time intervals (in seconds) are 0.01, 0.1, 1.0, 10.0, 100, and 1,000 at each stress field level.

Each sweep through the stress time intervals is done at a fixed stress field. After each sweep, the number of failures at the end of each time interval is also saved. The next sweep over the same capacitor array is performed at a higher field, and the data for that time/field are saved. Each surviving capacitor is exposed to progressively higher fields, while accumulating stress from all past stress sweeps. Test data generally must be treated as censored data because each chip may not have all capacitors failing at a particular stress condition. Extrapolation of test results to at-use conditions is done by the method given in Anolick [6.13].

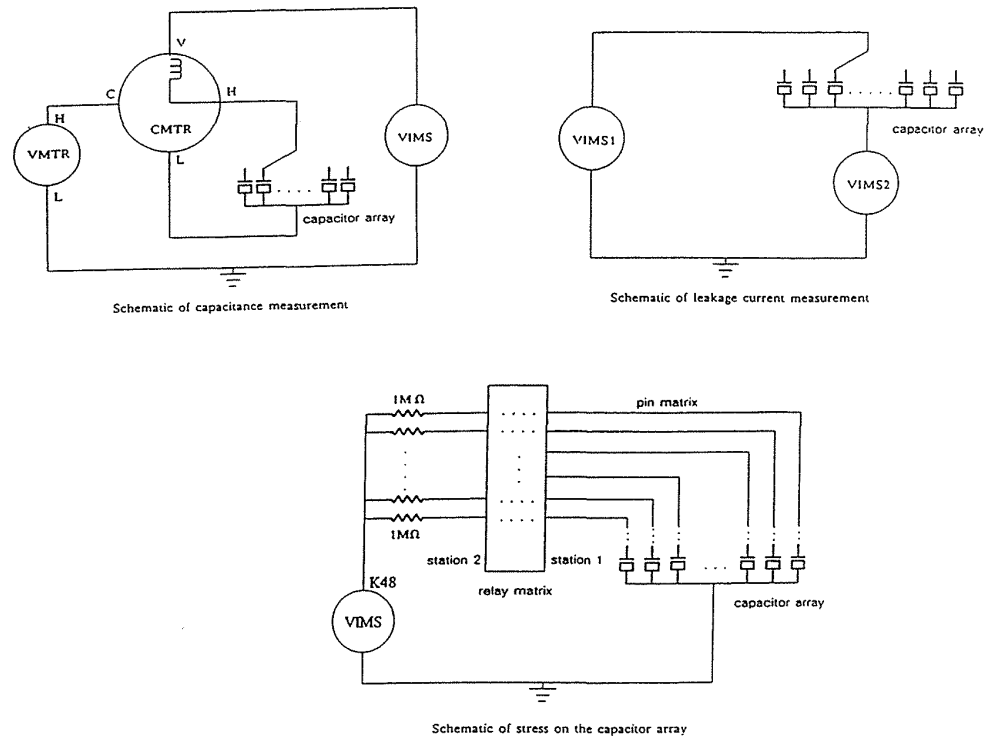


Figure 6.51 Test configuration for capacitor arrays.

This step stress method is more rapid than testing at a fixed field and can be done at wafer-level. Test times are still much longer than can be considered practical for true wafer-level testing. It can also be argued that testing is too rapid for unambiguous extrapolation to at-use conditions. It is, therefore, advisable to include package-level fixed field stress testing in the calibration procedure in order to build a solid confidence bridge with the rapid wafer-level testing used in wafer screening.

Testing at the wafer level typically implies that the testing time will be very short to avoid reducing wafer fabrication line throughput. Rapid wafer-level testing for TDDDB is most easily achieved by using a ramped stress procedure. A ramped stress procedure depends on the assumption that oxide failure occurs when a critical level of total charge fluence has been reached. It is further assumed that the time span over which this total charge fluence is reached does not change the magnitude of the total fluence to failure. This leads to two rapid testing strategies that are suitable for wafer screening. Voltage ramp testing increases the stress field in prescribed steps while monitoring the capacitor for signs of failure. Voltage ramp testing starts at stress levels near normal operating fields and progressively increases the stress to failure. The second method is current ramp testing, which forces measured quantities of charge through the capacitor. The charge magnitude is progressively increased by increasing the force current at regular time intervals until the capacitor fails.

A JEDEC Task Group, JC-14.2, whose charter enables it to generate wafer reliability testing standards, has defined a standard test method for TDDDB and was in final voting at the time this text was being written. The current version of the document, JEDEC Document No. JESD-35, "A Procedure for the Wafer-Level Testing of Thin Dielectrics," reflects the current status of the TDDDB test method standards.

Voltage ramp and current ramp testing provide two valuable quality parameters. A relatively small sample size of test capacitors can distinguish between good quality oxide and lesser quality oxide, as shown in Fig. 6.52. The histogram with single lines is from a high-quality oxide, while the double bar histogram is from one with lower quality. The test can clearly indicate a global problem that will uniformly degrade the expected lifetime of transistors.

The same test methods used on large sample sizes will permit extraction of defect density-limited oxide problems. It can also reveal differences in oxide edge effects involving field edge or poly edge. Figure 6.53 shows a comparison of oxides from two different fabrication lines. Fabricator A has no distinguishable defect tail in the cumulative distribution function (CDF) and unmeasurable differences in edge effects in the gate oxide. Fabricator B is relatively dominated by defect-limited oxide breakdown. This oxide is nominally acceptable, considering that operating fields are around 1.5 MV/cm. However, this oxide would be less desirable for IC devices to be used in a system that must operate for long periods of time without any opportunity for repair. In addition, the fabricator B oxide has no statistically distinguishable edge

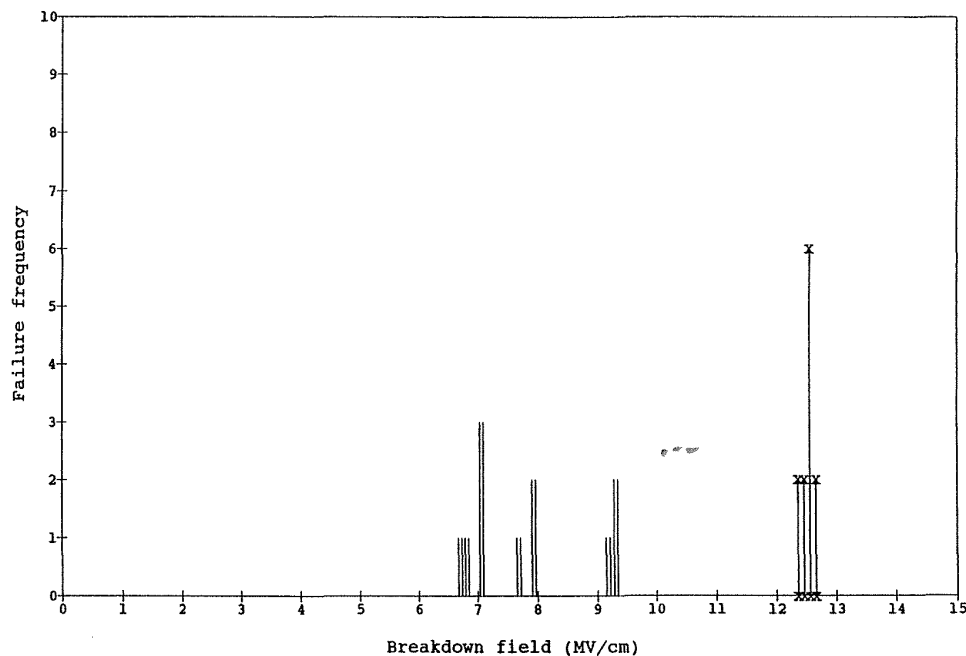


Figure 6.52 Histogram of two different oxides derived from small sample sizes.

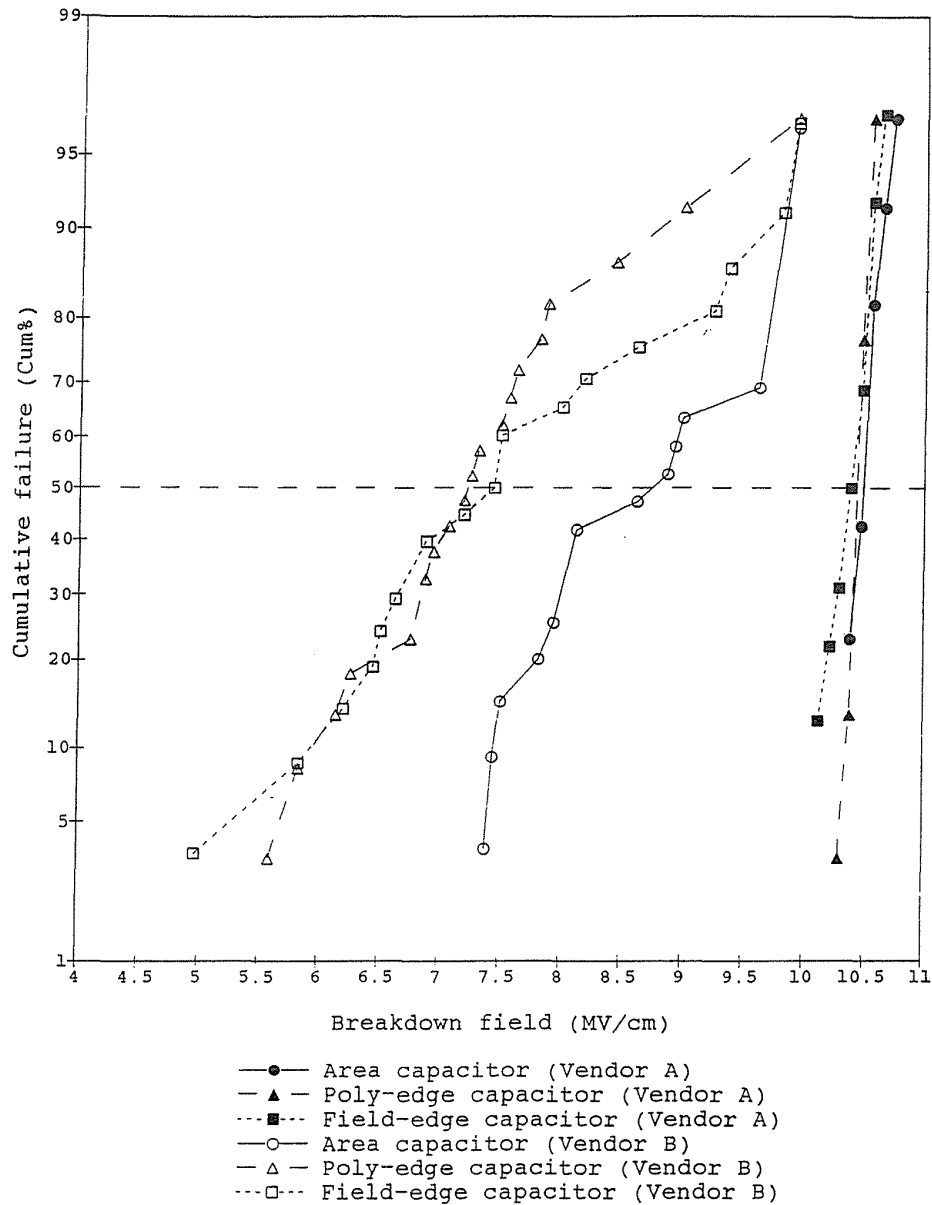


Figure 6.53 CDF plots of voltage ramp TDDDB test results from two different fabricators.

factors, largely because of the much larger sigma for this defect-dominated CDF tail. However, there is a suggestion of better performance on area capacitors, with edge factors minimized in the test structure. The JEDEC test procedure includes a description of a defect density extraction process, as well as a suggested test structure design.

6.3.1.6 Isolating Mechanisms—Models and Testing: EM. In discussing electromigration (EM), most of the literature deals with aluminum and its alloys (e.g., Al/Si and Al/Si/Cu). The models that have been developed for electromigration apply fairly well to these metal systems. However, we must not forget that most of the fine-line technologies (e.g., 1.2 μm CMOS) are using barrier metal (e.g., Al/W, Al/Ti-W, etc.) to retard metal and contact electromigration. The behavior of these metals in electromigration tests [6.76] will require some strategy changes that are yet to be defined.

Normal operating current density, by design rule, is typically 1×10^5 A/cm², which generally guarantees a 20+ year lifetime for the metal. The current density ranges commonly used in accelerated testing are 0.5×10^6 to 2.5×10^6 A/cm² for a moderate acceleration factor and 3.0×10^6 to 1.0×10^7 A/cm² for an extreme acceleration factor. Both ranges of acceleration factor are needed to establish a hierarchical electromigration test program with reasonable correlation to at-use conditions.

A widely accepted time-to-fail model for an aluminum alloy interconnect is

$$t_{50} = A * W^p * L^q * t * J^{-n} * \exp\left(\frac{E_a}{k * T}\right) \quad (6.46)$$

where E_a = activation energy, about 0.4 eV to 0.9 eV, and length and width compensation is included to handle grain mechanical stress effects [6.78–6.80]. However, since we are concerned primarily with fine-line technologies, the length, thickness, and width dependencies are negligible and are typically absorbed into the constant A. The activation energy is a function of alloy composition and thermal processes during wafer fabrication. The time-to-fail relationship that is most commonly quoted is

$$t_{50} = A * J^{-n} * \exp\left(\frac{E_a}{k * T}\right) \quad (6.47)$$

The exponent in the current density is of concern because the array of test structures that are being considered for wafer-level reliability (WLR) electromigration testing will use widely different current densities. The value of n is determined by the current density [6.77] and must be known in order to extrapolate test results to at-use conditions. Fortunately, extrapolation from extreme current densities, where n is changing rapidly, will not be required with careful calibration to test results at moderate current densities.

Electromigration in contacts is becoming a much more serious problem than it has been in the past because the junction depths and contact sizes are smaller in fine-line technologies. Testing for contact electromigration is more difficult at wafer level because forcing a larger current through contacts to obtain a large acceleration factor can cause large-voltage gradients in the junction region, which can provide alternate current paths.

Two failure modes should be considered in contacts: high resistance caused by migration of silicon into the contact region, and junction leakage caused by aluminum spikes growing into pits in the contact. A model for leakage and for resistance increase [6.81, 6.82] is useful for extrapolation to at-use conditions. Separate models are needed to deal with the two contact failure mechanisms. Both models are dis-

cussed in detail in the referenced papers. The activation energy and magnitude of n are a function of the contact metallurgy and the magnitude of current flowing, all of which make highly accelerated testing difficult.

Fortunately, the use of barrier metals in contacts moderates the contact electromigration problem enough that tests at extreme acceleration factors to screen the wafers are not necessary. Barrier materials have essentially eliminated the classic contact EM problem and have extended contact lifetime to well beyond the expected lifetime for interconnect metal. However, in the spirit of checking, which has been the intent of WLR, some method for determining correct barrier metal deposition will enable an indirect contact screening procedure.

6.3.1.7 Electromigration Testing Standards: Contact Electromigration. In the case of contact electromigration, there is no standard procedure other than using small contact strings [6.81] and testing them individually at elevated temperatures to obtain a reasonable acceleration factor. A reasonable test is to place the contact test structure at high temperature (135 to 200°C) and to apply a stress current (monitoring contact voltage drop), interrupted periodically to measure junction leakage. Failure criteria must be set for junction leakage and contact resistance.

It is doubtful that much effort will ever be needed to define wafer-level tests for contact electromigration because fabrication technology is evolving in a direction that eventually will completely eliminate any direct contact of aluminium with silicon either at junctions or to polysilicon. Currently, developments are favoring the use of barrier materials or even the use of selectively deposited refractory material within contacts.

6.3.1.8 Electromigration Testing Standards: Interconnect Electromigration. A considerable amount of effort has been directed toward creating wafer-level metal electromigration screens. The first step is to define an electromigration test that can be used for calibration of wafer-level electromigration tests. At this point in time, a rather well-exercised test structure and test method for oven-based electromigration testing has been developed at the National Institute of Standards and Technology, which is currently an ASTM standard [6.38, 6.41, 6.42]. Consistent results were obtained [6.77] when test stripes were tested in packages and at wafer probe. This test is run at a moderate current density (typically 2.5×10^6 A/cm²) and yields activation energy values that are observed by others.

With an accurate electromigration test method in place for calibration of metal systems, it is possible to pursue wafer-level tests. The structure that has received the greatest attention is the Standard Wafer-Level Electromigration Acceleration Test (SWEAT) [6.83], which can detect metalization problems with amazing accuracy. It can be tested in less than one minute (typically targeted for 30 seconds) per test structure. Test current density is in the range of 1×10^7 A/cm², which causes significant Joule heating (self-heating to 300–400°C). These two acceleration factors working together are the reason why the test is so rapid. Temperature and current density are controlled to achieve a target failure time for “normal” metal.

Even though some concern has been expressed that such extreme acceleration factors result in the domination of electromigration by some other mechanism of failure, much experimental evidence [6.92] reveals that the failures are dominated by electromigration. However, without calibration with the NIST structure, it is difficult to extrapolate results to use conditions. It is extremely useful in detecting poor step coverage when several SWEAT structures are placed over various steps.

Two other rapid electromigration test methods have been considered: the isothermal and the breakdown energy of metal (BEM) [6.84] tests. The isothermal test involves using Joule heating to raise the temperature of a metal stripe to a very high temperature (near 400°C) and maintaining it there by controlling the current. This is done in a controlled manner by monitoring the resistance of the metal stripe while under stress. The BEM test is a current ramp test to failure in which the total integrated energy dissipated in the test stripe to cause open-circuit failure is a measure of the metal resistance to electromigration. The median energy to fail in the stripe (in units of energy per unit length) becomes the measure of metal quality.

The main focus of this section is on the SWEAT structure because the SWEAT method is rapidly becoming a de facto industry standard. A layout for the standard SWEAT structure unit is presented in Fig. 6.54, with several candidate voltage tap configurations indicated. The configuration labeled "C" is the proposed standard configuration. The most pressing concern about the SWEAT test procedure is the lack of knowledge of the thermal environment along the test structure. The approximate temperature assessment described in the Root and Turner paper [6.83] used geometric arguments that were at best one-dimensional approximations.

A test method suggested in Root [6.92] uses a rather simple geometrical argument for translating average temperature measured, employing resistometric methods to peak temperature of the test link. However, a fairly broad distribution

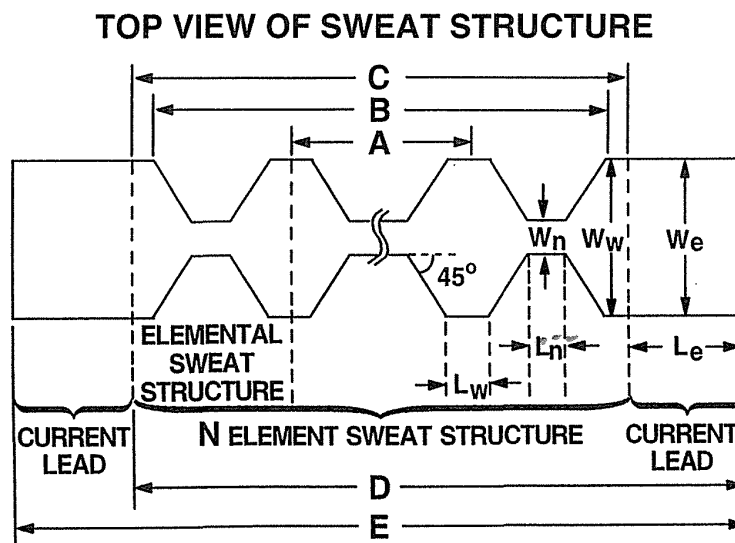


Figure 6.54 SWEAT structure unit and various voltage tap configurations (after Crowell et al. [6.85]).

in the data suggests that the temperature was not very well controlled or even known (see Fig. 6.55). Even though the method implemented was being considered for use as the JEDEC standard SWEAT procedure, a mathematical model of the SWEAT thermal environment (TEARS model) [6.81, 6.85] greatly improves the estimate of the peak temperature, with an observable improvement in test stability.

Evidence of the lower accuracy of temperature assessment is indicated in Fig. 6.55, which shows three different implementations of temperature computation. Figures 6.55a,b show the two most common methods of temperature calculation. Figure 6.55a, labeled “Historical,” shows controller stability when the system uses a geometrically calculated temperature, which is the basic method described in the Root and Turner paper. An improvement is achieved by incorporating a local heat-sinking concept in the heat flow through the SWEAT structure. Both methods show evidence of temperature drift that the system must periodically correct. This correction can be seen as a “sawtooth” correction to the calculated time-to-fail graph in Figures 6.55a,b during the early part of the test.

The TEARS model is sufficiently general that it can be used for other test structure geometries that are tested by using at least partial Joule heating as part of the thermal acceleration process. In addition, it can account for thermal gradient effects in the SWEAT structure that are responsible for causing thermoelectric potentials within the test structure, which, in turn, cause a modification of the temperature profile symmetry (Fig. 6.56).

SWEAT TEST FOR APPARENT t_{50} versus TIME :

(A) "Historical"; (B) Local-Heat-Sinking; (C) TEARS.

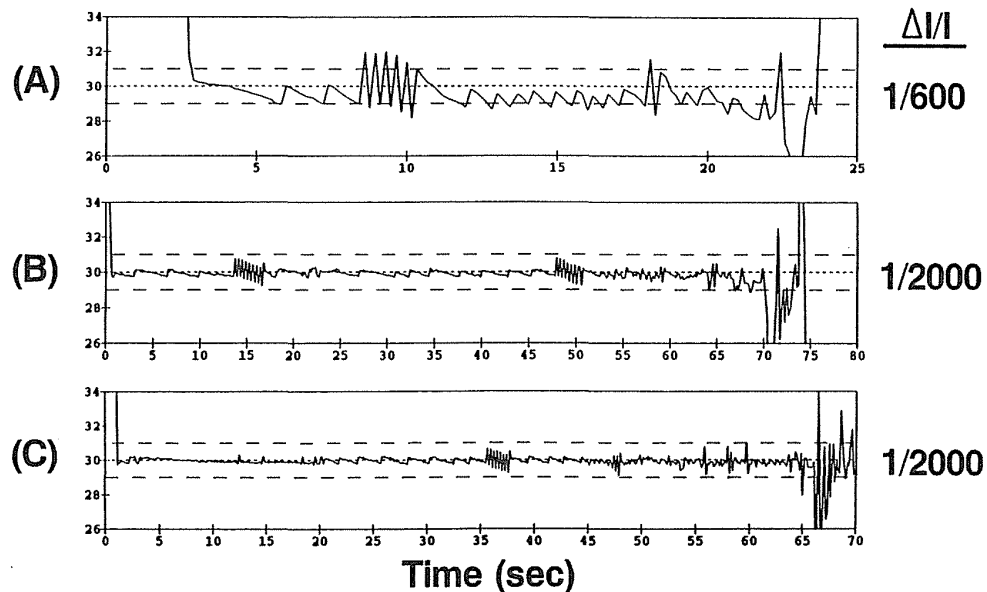


Figure 6.55 Test data showing computed time-to-fail control for three thermal models.

TEMPERATURE RISE PROFILE FOR METAL-2

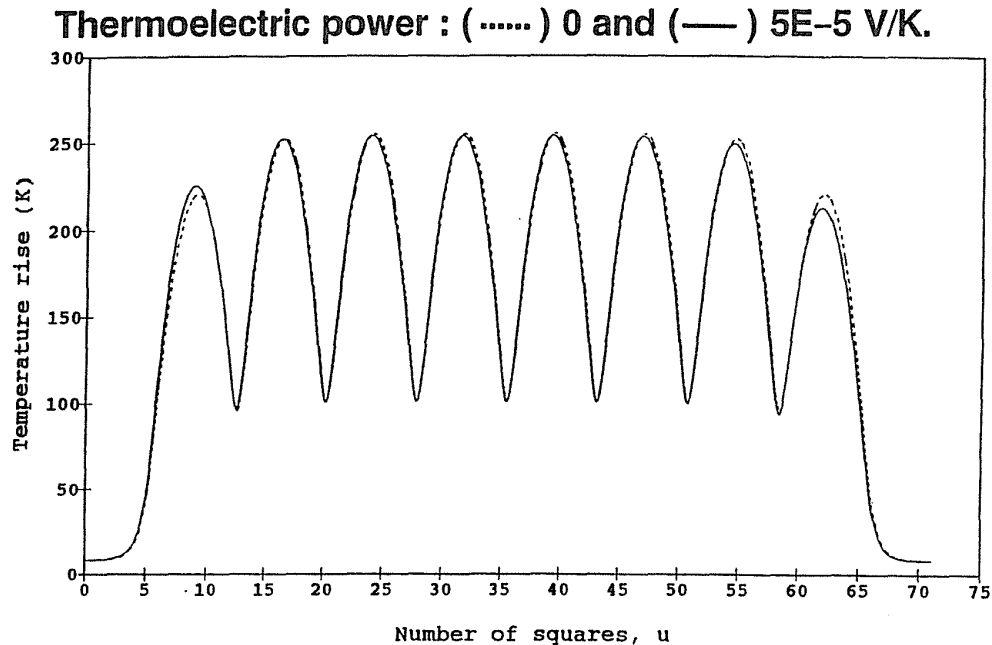


Figure 6.56 SWEAT thermal profile: with and without the thermoelectric term.

Programs for wafer-level monitoring of electromigration in metal interconnects can be implemented with existing test structures and time-to-fail models, but a good thermal model for estimating temperature during testing with substantial Joule heating is essential.

6.3.1.9 Isolating Mechanisms—Models and Testing: HCD. Hot-carrier-induced MOS transistor degradation (HCD) becomes a concern as channel lengths become less than about $2.0\ \mu\text{m}$. Since normal operating voltages have not been scaling with channel length, this problem will become increasingly important to monitor. Methods for reducing the rate of degradation through fabrication process changes (LDD, etc.) involve delicate fabrication procedures that can get out of control and must be monitored. Accelerated testing is certainly in order, but the danger of extrapolation error is great because most simple testing methods are indirect and extrapolation models are empirically derived.

Generally, stress conditions use an elevated drain voltage to enhance the rate of degradation. Tests generally monitor changes in drain current, in threshold, and in transconductance, G_m . A model for time-to-fail based on threshold change [6.48] is a typical example of an empirical model that uses the ratio of drain current to substrate current as an indicator of damage rate. Thus,

$$t_{50} = H * W * \frac{I_{ds}^{1.9}}{I_b^{2.9}} * \Delta V_{th}^{1.5} \quad (6.48)$$

where H = dielectric dependent constant and W = channel length. However, the observed ratio of changes in drain current versus initial drain current suggests a more complex model [6.86]. Much more experimentation is needed to define a good extrapolation model that will relate the measurements at wafer-level to the shift in parameters that concern the circuit designer.

Currently, hot-carrier testing is typically done at high stress levels to cause changes in threshold and transconductance (hence, drain saturation current) and requires many hours of stress time to detect significant changes in transistor characteristics. These tests are frequently done at wafer level, but the length of stress time required makes them unsuitable for wafer screening. Since substrate current is directly related to the electron hole pair generation rate, monitoring substrate current is a practical method of estimating the hot-carrier damage rate, as was assumed in the above extrapolation model.

The most direct wafer-level test method to use is a four-terminal field-effect transistor (FET) connected to measure drain current and substrate current. A stress drain voltage greater than at-use conditions is applied, and the gate voltage is swept to find the peak in the substrate current. The measured values of drain current and substrate current are used to assess the hot-carrier sensitivity of the transistor. Test transistors should be minimum design rule channel length by a width of at least 20 times the channel length. A pass/fail criterion is based on the ratio of the drain current at the peak substrate current to the peak substrate current. The exact pass/fail threshold is experimentally developed by calibration with long-term stress tests that compare changes in threshold, transconductance, and saturation current with initial tested drain current to substrate current ratio.

Clearly, new wafer-level hot-carrier tests are needed that can measure the actual damage process at the early stages of hot-carrier injection before damage reaches a level that begins to change transconductance. One promising method uses charge pumping to measure the increase in interface states caused by hot-carrier injection [6.87, 6.88]. Figure 6.57 shows the test configuration used to gather data for correlation with long-term test data. Data gathered from this system are illustrated in Fig. 6.58 and show large shifts in charge-pumping current after only a moderate amount of conventional stress time of three hours.

Charge-pumping current tests are compared with test results of transconductance changes in Table 6.9. These data show how many seconds of stressing are required to cause a 10% shift in charge-pumping current and a 10% shift in transconductance at various stress bias conditions. The stress conditions range from moderate stress bias ($V_{ds} = 6.5$ V, $V_{gs} = 3.0$ V) to just above at-use bias ($V_{ds} = 5.5$ V, $V_{gs} = 1.5$ V). In all cases, the reduction in test time is dramatic. Typically, charge-pumping tests show a 10% shift in 1/1,000 the stress time. The only smaller ratio is at $V_{ds} = 5.5$ V, which required less than six minutes to change the charge-pumping current by 10%, while available data for transconductance indicate more than 28 hours for an estimated 10% change in transconductance. The trans-

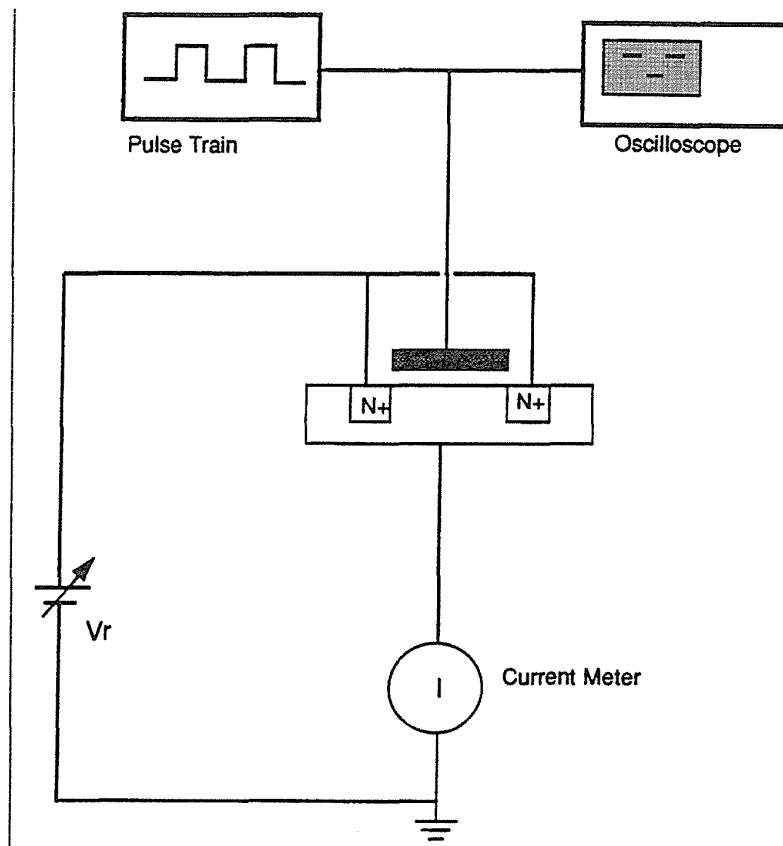


Figure 6.57 Charge-pumping measurement configuration.

conductance test at a drain stress of $V_{ds} = 5.5 \text{ V}$ was actually terminated after 28 hours before a transconductance change of 10% was logged.

Charge-pumping measurements are clearly capable of rapid assessment of hot-carrier damage rate at the wafer level. It not only is rapid, but it actually measures the transconductance degradation mechanism directly by measuring the accumulation of surface states. One limitation imposed by charge pumping is that, with the very low current measured (picoampere range), it is almost impossible to conduct the tests in the automated wafer probe environment found in a wafer fabrication line. More research is needed to solve this problem.

6.3.2 Typical Reliability Data

With the diversity of NVSM technology, and the progress and maturity of technology through the years, in addition to the different metrics used by various manufacturers and users to quantify the several aspects of NVSM reliability, a meaningful comparative study of reliability is not practical or desirable. Nevertheless, a quantitative feel for NVSM reliability can be obtained with some

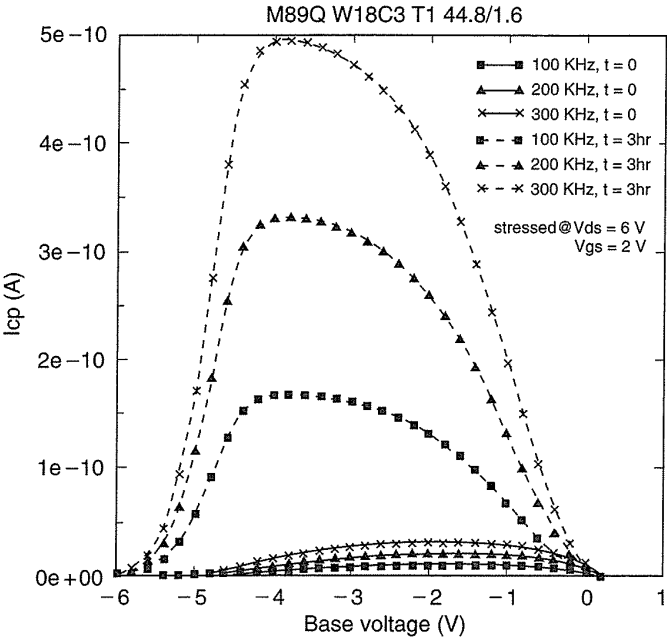


Figure 6.58 Charge-pumping current before and after stress.

reliability data from the literature. Readers are advised (1) to note the date of publication of data compiled in this section, (2) to consult the cited literature for measurement methods and techniques used, and (3) to develop their own data through their supplier or their own reliability test programs.

Table 6.10 compares the defect-limited memory data retention of several NVSM devices, published in 1987 [6.28]. These failure rates can be compared with typical < 100 FIT data established for SRAM and DRAM of that time. For memory applications, data-loss failures (i.e., soft errors from alpha particle, etc.) should be included as overall retention failure considerations, if ECC is not used in the application. Table 6.11 compares retention data-loss failure rates of floating gate EPROM and E²PROM technology against the other semiconductor memory technologies of

TABLE 6.9 COMPARISON OF TESTING TIME FOR DIFFERENT EVALUATION TECHNIQUES IN HCD ASSESSMENT

Method \ HCD indicator		Time-to-10% change (sec)					
		$V_{ds} = 6.5$ $V_{gs} = 2.0$	$V_{ds} = 6.5$ $V_{gs} = 3.0$	$V_{ds} = 6.25$ $V_{gs} = 2.0$	$V_{ds} = 6.26$ $V_{gs} = 3.0$	$V_{ds} = 6.0$ $V_{gs} = 2.0$	$V_{ds} = 5.5$ $V_{gs} = 1.5$
Charge-pumping technique		2.0	6.3	4.5	7.9	25	316
DC transistor parameter characterization technique (gm in linear region)		1920	12,600	7311	15,300	18,026	> 100,800

TABLE 6.10 NONVOLATILE MEMORY DATA RETENTION
(AFTER MIELKE ET AL. [6.28]).

Sample				%Fail vs. # Hours				
Product	Type	Size	Temp.	48	168	500	1000	FITS
64 KB	EPROM	1800	250°C	0.9%	1.1%	2.0%	n.a.	15
16 KB	FLOTOX	550	150°C	0.0%	0.0%	0/2%	0.2%	31
64 KB	Tex-Poly	350	250°C	0.0%	0.0%	0.0%	0.3%	1

TABLE 6.11 TYPICAL RETENTION FAILURE RATES (FIT)
(AFTER MIELKE ET AL. [6.28]).

Technology	Soft Errors	Total
EPROM/E ² PROM	< 1	1–50
DRAM	50–1000	50–1000
Poly-load SRAM	20–1000	20–1000
Full-CMOS SRAM	10–50	10–50

interest. Table 6.12 further compares these technologies in terms of lifetime catastrophic failure mechanisms, such as oxide breakdowns and data loss from gate leakage. From Table 6.12, it can be noted that floating gate NVSM devices have superior oxide breakdown properties—primarily a consequence of attention to silicon dioxide dielectric integrity necessitated by high-voltage requirements of the floating gate operations. Table 6.13 summarizes some representative values for endurance failure rates of Flash EEPROM and other floating gate NVSM devices. The limited erase/write endurance performance of floating gate devices must be carefully evaluated in terms of end-use memory system erase/write cycle requirements.

Floating trap NVSM devices, such as MNOS memories, have been reported to have superior data retention failure rates as compared to floating gate NVSM devices, such as FLOTOX and textured-poly EEPROMs [6.89]. The spatially distributed traps in MNOS memories are less subject to data loss from electrical charge

TABLE 6.12 LIFE TEST FAILURE RATES (FIT) (AFTER MIELKE ET AL. [6.28]).

Product(s)	Technology	Oxide Breakdown	Data Loss	All Causes
64 KB	Tex-Poly	< 48	< 15	129
16 KB	FLOTOX	< 21	17	43
64 KB–512 KB	EPROM	11	52	100
General Logic	Non-FG	91	0	120

TABLE 6.13 FLASH MEMORY RELIABILITY DATA SUMMARY (PER INTEL DATA BOOK [6.89]). [REPRINTED BY PERMISSION OF INTEL CORPORATION, COPYRIGHT 1988, INTEL CORPORATION]

- Flash memory life test reliability is equivalent to EPROM (64 vs. 103 FITS)
 - Flash memory reprogrammability failure rate lower than EPROM/EEPROM
- Reprogrammability failure specifications
- | | |
|--------------|-----------------------------|
| Flash memory | < .1% AT 10 K-cycles (goal) |
| EPROM | 2% |
| EEPROM | 5% AT 10 K-cycles |

- Flash memory cycling test results to date

Product	Cycles	Fail/unit
27F64	20,000	0/1000
28F256	60,000	0/2

- Data retention equivalent to EPROM (~100 years)

leaks through latent failures in the memory oxide film. Figure 6.59 shows the retention failure characteristics of MNOS (measured at accumulated 1% failure) against temperature (Arrhenius plot) and against floating gate NVSM devices A, B, and C. Accumulated failures from erase/write endurance cycling typical of a MNOS EEPROM product is given in Fig. 6.60. The failure rate was within the 10^5 erase/write cycle endurance specification of the product as of November 1987. Other data included in the figure are for floating gate NVSM devices measured in a similar manner.

As has been discussed, the limited endurance of NVSM products precludes their application as random access memories in traditional design or architecture. On the other hand, for applications or designs in which the device is accessed infrequently, such as N times per day (where N is less than 100, for example), the endurance reliability of the NVSM can be calculated and can be shown to be similar to that of other semiconductor IC memory devices such as DRAMs and SRAMs.

From Fig. 6.60, after 10^5 erase/write cycles, the cumulative chip failure rate is about 0.7%. This particular device is organized architecturally as 256 pages of 32 bytes so that each erase/write access is, in effect, an erase/write cycle for 32 bytes. Therefore, failure rate/page is $0.7 \times (1/256)\%$, and the failure rate dependence on N is given as follows:

$$\begin{aligned}
 \text{Failure Rate} &= (0.7\%/256 \text{ pages}/10^5) * (N \text{ times}/24 \text{ hours}) \\
 &= N \times 10^{-11} / \text{hours} \\
 &= N \times 10^{-2} \text{ FIT}
 \end{aligned}$$

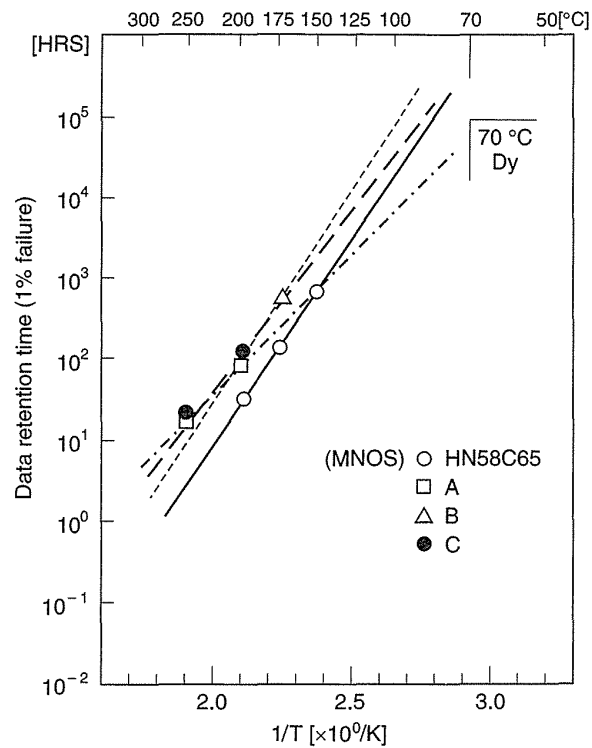


Figure 6.59 Data retention characteristics (Arrhenius plot) (after Hagiwara et al. [6.90]).

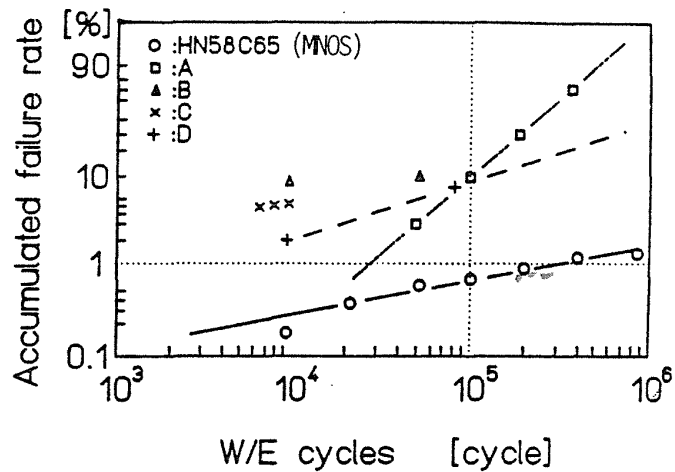


Figure 6.60 Reliability on write/erase cycles (accumulated failure rate) (after Hagiwara et al. [6.90]).

Typical DRAM and SRAM ICs have failure rates in the range of 10 to 100 FIT. Thus, the NVSM endurance reliability for some applications can be treated much like other IC components in the system. In fact, in many applications where $N \simeq 1$, the endurance reliability of NVSM products does not contribute to system reliability concerns.

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Radiation Tolerance

7.0. INTRODUCTION

This chapter considers the very important topic of radiation response of nonvolatile semiconductor memories. Modern electronic systems must perform properly in hostile radiation environments created by nuclear explosions for most Department of Defense (DOD) applications. In addition, all space systems are exposed to electrons and protons in or near the Van Allen belts and to cosmic rays [7.1].

7.1. BASIC RADIATION CONSIDERATIONS

First, a brief summary of basic radiation effects is presented as a foundation for considering the radiation response of floating gate and SNOS memory devices.

7.1.1 Radiation Environments

It is important to establish quantitatively the types of radiation environments and the appropriate range of intensities that are of interest to system designers contemplating the use of SNOS and floating gate memories.

7.1.1.1 Nuclear Weapon Environments. Nuclear explosions generate neutrons, gamma rays, and X rays [7.2]. Endo-atmospheric explosions create a radiation threat primarily from neutrons and gamma rays. The X rays are converted to a blast wave and thermal radiation from the fireball by interaction with the atmosphere in the immediate vicinity of the explosion. Balanced hardness considerations dictate the nuclear radiation specification. If the equipment is manned, human survival (approximately 500 Rads), or near instantaneous human incapacitation (approximately 3,000 Rads), defines the ionizing dose specification level [7.3]. The ionizing dose specification for these applications is, therefore, usually less than 3,000 Rads(Si). The accompanying neutron specification, determined in the same manner, is usually less than 10^{12} n/cm² (1 Mev Equivalent). This explanation is greatly oversimplified for purposes of clarity and brevity. Factors involved in this determination are the relative biological effectiveness (RBE) to relate Rads(Si) for neutrons and gamma rays to radiation equivalent man (REMs). The actual size of the nuclear weapon is also an extremely important factor. For weapons larger than 20 kilotons (KTs), blast and thermal effects are usually dominant. It is only for scenarios that involve nuclear weapons smaller than 20 KT that neutron and gamma specifications are normally encountered.

For unmanned electronic equipment, the radiation specification is normally balanced to the capability of the system to survive the nuclear blast. A blast survival capability of approximately 2 psi (pounds per square inch) is typical for most electronic equipment. Determining the neutron and gamma ray exposure coradius with 2 psi coincidentally usually results in gamma specifications less than 3,000 Rads(Si) and neutron levels less than 10^{12} n/cm² (1 Mev Equivalent). Finally, fallout is an important factor. The radioactive fission fragments are thrust high into the atmosphere and fall back to earth in a complex pattern dominated by wind and weather. It should be recognized that some special military requirements may be encountered with higher radiation specifications. It is frequently required that components meet a higher radiation specification than the electronic system. This is done to provide a hardness design margin; such design margins usually range from 3 to 10.

Exo-atmospheric systems such as satellites and ballistic missiles operate in the hard vacuum of space. Here, the X rays travel unattenuated and interact directly with the system. The neutrons and gamma rays also arrive at the system with no attenuation. The radiation requirements are established for balanced hardness by determining the system survivability to the thermomechanical effects of X rays. This limit is approximately 1 cal/cm² for many satellites. The most vulnerable components tend to be polished optical lenses or sensors that are, by necessity, directly exposed to the unattenuated X-ray flux. The neutron, X-ray, and gamma ray intensities at the 1 cal/cm² radius are easily determined for typical nuclear weapons. A neutron fluence of 3×10^{11} n/cm² is typical, and a gamma dose of 50 Rads(Si) is usually encountered. However, the total ionizing dose is usually dominated by shine-through X rays and electrons that have been attenuated by the satellite skin, the electronic box, and the component package. The shine-through dose is usually between 500 and 50,000 Rads(Si). Often, high atomic number shielding materials, such as lead, are used to attenuate the X rays. In the practical limit, X-ray shine-through can be reduced to the same level as the gamma exposure, or about 50 Rads(Si).

Tactical and avionic specification considerations are summarized in Table 7.1. The lower limits are levels below which semiconductor devices show no significant degradation in nearly all applications. The upper limits are radiation levels that result in nearly instantaneous human incapacitation and severe blast damage.

A design margin at the component level is used to ensure high system survival probability without the necessity of component radiation lot sample testing. Some military requirements, such as strategic weapon systems, require much higher radiation specifications. These requirements are system specific and are always classified; therefore, they cannot be discussed here.

TABLE 7.1 TACTICAL AND AVIONIC RADIATION REQUIREMENTS

	Typical	Range		Components with Design Margin
		Lower Limit	Upper Limit	
Neutron fluence n/cm**2	10exp12	10exp11	2*10exp12	5*10exp12
1 Mev Equivalent				
Ionizing dose Rads (Si)	3,000	50	5,000	10,000
Dose rate Rads (Si)/s	10exp8	10exp6	10exp9	3*10exp9
Overpressure Psi	2	—	5	—

7.1.1.2 The Natural Space Radiation Environment. The natural space radiation environment is dominated by protons and electrons from the Van Allen belts. These belts contain high levels of ionizing radiation, and therefore, nearly all space satellites are established in orbits either below or above the belts. Low earth orbits (LEOs) are substantially below the inner belt as exemplified by the various shuttle orbits. Synchronous altitude satellites are in an orbit substantially above the outer belt. The National Aeronautics and Space Administration (NASA) has done extensive mapping of electron and proton fluxes in the entire operational space around the earth, and computer programs are available to define proton and electron fluences and spectra of any desired orbit for any mission life. However, these mappings still contain considerable uncertainties. A typical worst case mission electron fluence is 10^{15} e/cm² with an average energy of 1 MeV.

For all but a few orbits close to the inner belt, the proton fluence contributes a negligible amount of ionizing dose compared to electrons. However, proton fluences are defined in the same manner as electron fluences for desired orbits and mission life. The range of protons is relatively small, and the satellite skin, the box thickness, and the component package combine to reduce the ionizing dose from protons. When a nuclear weapon explodes in space, it produces a very high density of electrons that are trapped by the earth's magnetic field in a manner similar to the natural belts. These are referred to as pumped-up belts, and the electrons are known as Argus electrons after the first test blast that led to their discovery. These electrons decay as a function of time, and the decay time depends strongly on the location of the burst. A large number of bursts can build the electron density up to a saturation

value in the pumped-up belts. Worst case mission electron fluences can be an order of magnitude higher than the natural fluence under these circumstances.

The ionizing radiation reaching electronic components is attenuated by the satellite skin, the walls of the electronic box, the walls of the package, and any other structures through which the radiation must pass. This typically amounts to 1 to 3 g/cm² and provides attenuation of two to three orders of magnitude. This results in ionizing dose levels in electronics varying from 10³ to 10⁵ Rads(Si) for most applications. Figure 7.1 shows the attenuation characteristics and can be used to calculate the dose reaching electronic devices.

Cosmic radiation is the final major constituent of the space environment that can damage electronic components. The contribution to total ionizing dose is negligible. The satellite and other material surrounding the electronic components provide no significant shielding due to the extremely high energy of cosmic ray components. Some

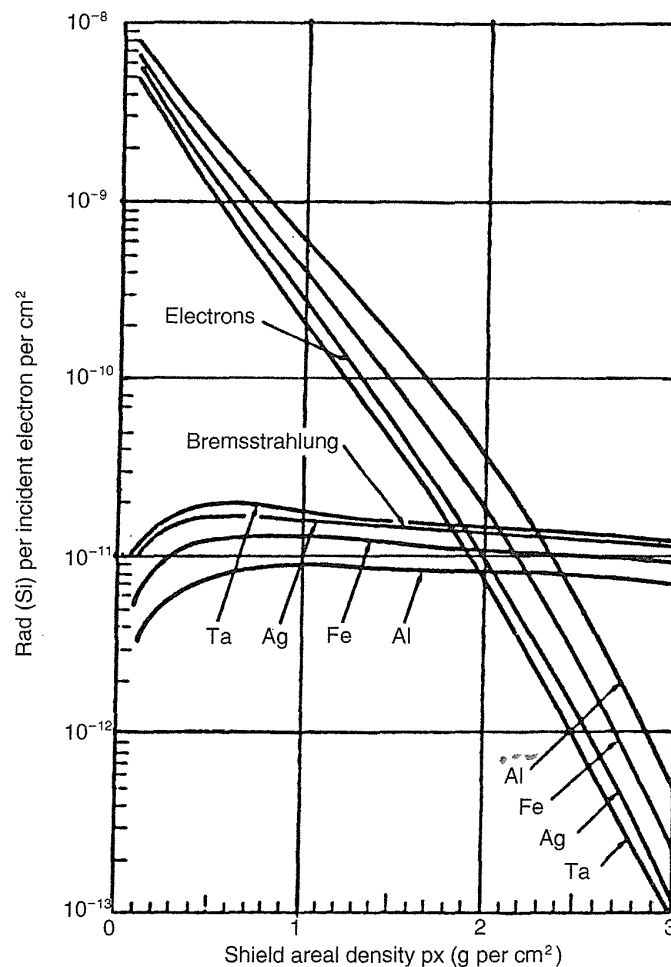


Figure 7.1 Isotropic fission electron dose as a function of shielding thickness for a family of shielding materials.

cosmic rays originate in the sun, and their fluxes are tied into the solar cycle. Again, NASA has mapped cosmic ray behavior in the space around the earth, and estimates of cosmic ray activity can be obtained for anticipated orbits and mission duration. Cosmic rays cause single-event phenomena (SEP) in semiconductor components, which primarily cause only a change of state in a logic cell. Subsequently, the entire component functions properly. This is referred to as single-event upset (SEU). Occasionally, however, the passage of a cosmic ray through the active volume of a semiconductor component can trigger latchup or burnout; these incidents usually result in catastrophic failure. The cosmic ray environment is described by the Heinrich curves shown in Fig. 7.2, which are plots of particle flux as a function of linear energy transfer (LET) [7.5]. These curves reflect various amounts of solar activity, allowing the designer to select his own worst case condition.

7.1.1.3 Nuclear Power Reactors. There is a small usage of semiconductor components in commercial power reactors. For example, pressure and temperature

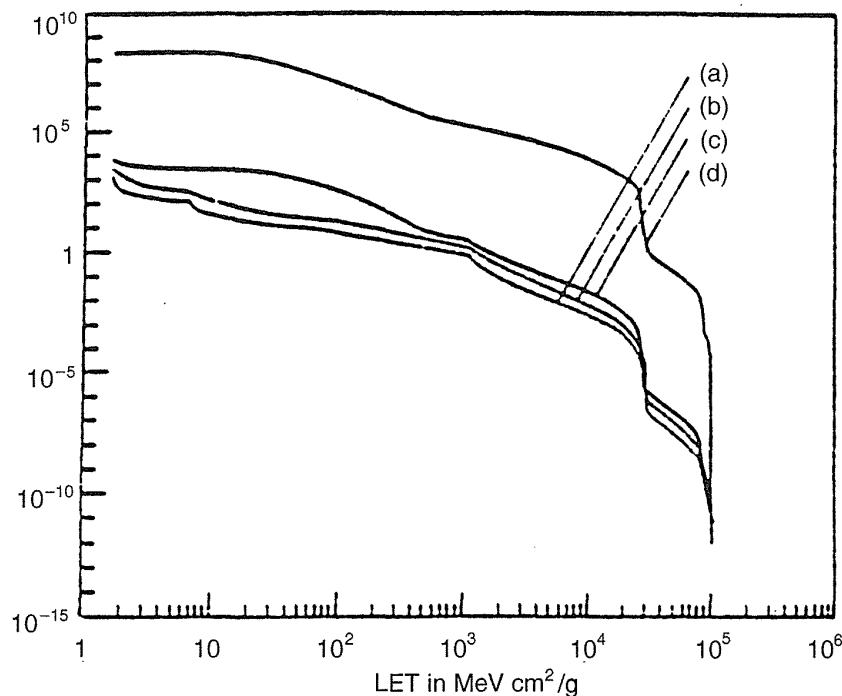


Figure 7.2 Integral LET spectra in the interplanetary medium, inside a spacecraft with 0.064 cm aluminum walls. These spectra include the contribution of all the elements. (a) Pure galactic cosmic rays at solar maximum; (b) pure galactic cosmic rays at solar minimum; (c) an environment so severe that it is exceeded only 10% of the time; (d) an extremely large solar flare at its peak.

transducers are used to monitor the reactor core. These components are specified to survive 2×10^8 Rads(Si), reflecting a loss of coolant accident (LOCA) [7.6].

7.1.1.4 Radiation Simulations. Radiation testing of semiconductor components is routinely accomplished in a variety of simulators [7.1]. The most commonly used simulators include: (1) fast burst reactors and training-research-isotopes-general-atomic (TRIGA) reactors for neutron exposure, (2) Cobalt-60 cells for ionizing dose exposure, (3) linear accelerators (LINACs) and Flash X rays for dose-rate testing, (4) Aracor machines for in-line ionizing dose hardness assurance testing of semiconductor components, and (5) cyclotrons for simulating high-energy cosmic rays. It should be noted that simulators do not accurately reproduce the environments for which the equipment is being designed. Extrapolation or interpolation is usually required.

For example, the ionizing dose environment in space is usually caused by shine-through electrons delivered at a very low rate (0.0001 to 1 Rad(Si)/s), and the standard test is in a Co⁶⁰ cell at 300 Rad(Si)/s. This can be very misleading, for ionizing dose effects are strongly dependent on dose-rate. On the other hand, the ionizing dose from a nuclear weapon is usually delivered very rapidly and is strongly scenario dependent. The prompt dose is delivered at rates ranging from 10^6 to 10^{12} Rads(Si)/s, with a pulse width of approximately 10 ns. Almost all of the dose is accumulated within one minute. The ionizing dose simulation in the Co⁶⁰ cell is thus at too low a rate to properly simulate nuclear weapon effects. Most LINACs and Flash X rays cannot exactly simulate the very short nuclear prompt pulse. This is not a serious problem since obtainable simulator pulse widths vary from approximately 10 ns to 100 ns.

Dosimetry can also be a problem, but with good technique, it can be accomplished with 25% repeatability and 50% absolute accuracy [7.1,7.3]. Radiation testing should be carefully planned in advance, with close cooperation between test engineers, facility engineers who usually take responsibility for dosimetry, and health service personnel who ensure that the testing being carried out is consistent with safety and minimum radiation exposure to personnel.

Ionizing dose is usually monitored with thermoluminescent dosimeters (TLDs), and, if the pulse shape requires monitoring, it is often done with a personal identification number (PIN) diode. Neutron dose is usually monitored with sulfur pellets. The facility personnel then convert the sulfur reading to a 1 Mev Equivalent neutron fluence using a factor obtained by using a complex unfolding procedure generic to their facility in its present test configuration. All dosimetry calibrations should be traceable to national standards maintained by the National Institute of Standards and Technology (NIST).

7.1.2 Displacement Damage

Displacement damage is caused by all high-energy radiation and describes the disorder in the single-crystal silicon lattice resulting from collisions between the radiation particles and individual silicon atoms. However, neutron fluence is the

primary cause of displacement damage in the environments discussed previously. The predominant source is nuclear explosions.

Occasionally, it is necessary to evaluate displacement damage from protons or electrons. Since charged particles transfer nearly all of their energy to the silicon lattice by ionizing interactions, ionizing dose damage usually exceeds displacement damage by a large factor. When a neutron collides with a silicon atom, the silicon atom is highly energized. It becomes a recoil primary and subsequently dislodges many more silicon atoms before it loses all of its energy and comes to rest in the lattice. The immediate consequence of this process is the formation of a large number of Frenkel defects (vacancy interstitial pairs). The vacancy is an effective recombination and trapping center. Both the vacancy and interstitial are mobile at room temperature. The vacancy diffuses until it forms a more complex defect, which is stable. The vacancy might encounter an interstitial atom, in which case an immediate repair of the lattice occurs at that location. Other, less benign possibilities include: (1) formation of an E center by complexing with a donor atom, (2) formation of an A center by binding to an oxygen impurity atom, or (3) formation of a divacancy by tying up another vacancy. These defects are all effective recombination and trapping centers. They cause a reduction in minority carrier lifetime and an increase in silicon resistivity. The increase in resistivity is a result of majority carrier trapping and mobility reduction of the remaining majority carriers.

7.1.2.1 Lifetime Degradation. The amount of lattice damage is directly proportional to neutron fluence. The recombination rate of minority carriers is directly proportional to the amount of lattice damage, and finally, the minority carrier lifetime is inversely proportional to the recombination rate. Thus,

$$1/\tau = 1/\tau_0 + K\phi \quad (7.1)$$

where τ is the minority carrier lifetime, τ_0 is the initial unirradiated lifetime, K is a proportionality constant, and ϕ is the 1 Mev Equivalent neutron fluence. The derivation of this equation is beyond the scope of this book. The equation holds for values of neutron fluence up to 10^{16} n/cm². Minority-carrier lifetime is a function of injection level that translates to a dependence on bias currents in semiconductor devices. The Shockley–Read formalism can be used to introduce this dependence into Eq. (7.1). The major effect of lifetime degradation is a reduction in current gain in bipolar devices. Lifetime degradation also causes an increase in junction leakage currents. Ionizing dose also increases leakage currents, and these effects are usually dominant in MOS devices. Figure 7.3 shows the dependence of lifetime damage constant on doping density and injection level for silicon [7.1].

7.1.2.2 Carrier Removal. The trapping of majority carriers in silicon devices is directly proportional to neutron fluence. However, as the trapping continues, each carrier removed is a bigger proportion of the remaining carriers. This results in the following expression for carrier density as a function of neutron fluence.

$$n = N_{di}(1 - k\phi)/(1 + k\phi) \quad (7.2)$$

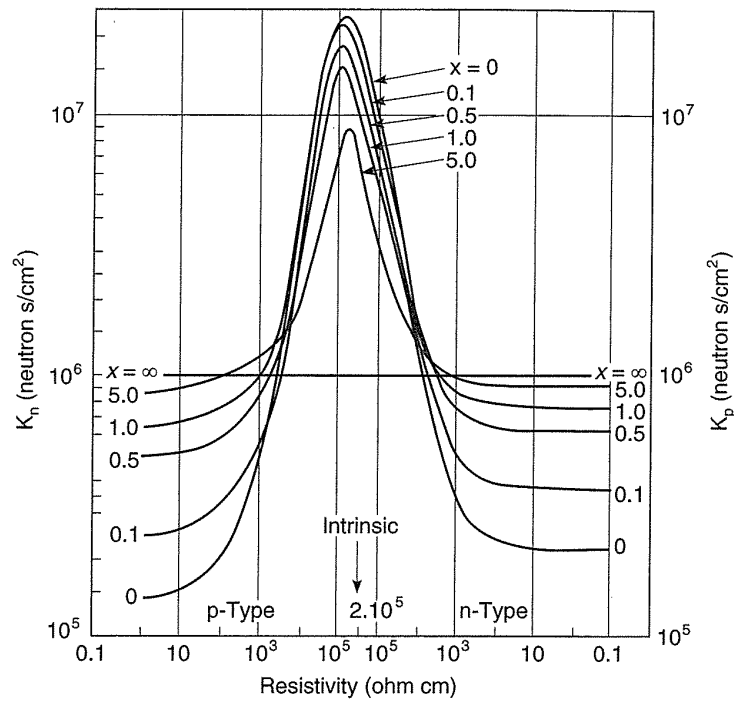


Figure 7.3 Damage constants versus resistivity for various injection ratios (proportional to bias currents).

where N_{di} is the initial donor density assumed to be equal to the initial electron carrier density, k is a constant, and ϕ is the neutron fluence. This approximation assumes that the removal process is dominated by the donor vacancy trapping centers, and it neglects small contributions from oxygen vacancy centers and divacancies. When $k\phi$ reaches one, the material becomes intrinsic. The divacancy has trapping levels at the middle of the band gap, and all silicon material asymptotically approaches intrinsic at high levels of neutron irradiation. The expression for carrier density is often approximated by the exponential relationship

$$n = N_{di} \exp(-k_1 \phi) \quad (7.3)$$

where k_1 is a constant. The carrier removal rate is then

$$dn/d\phi = -N_{di}k_1 \quad k_1 \phi \ll 1 \quad (7.4)$$

Figure 7.4 shows carrier removal data in N- and P-type silicon for a 10% change in resistivity [7.7]. Figure 7.5 shows the change in resistivity as a function of neutron fluence [7.7].

7.1.2.3 Mobility Degradation. Each carrier removed is trapped at a defect center, becomes charged, and is therefore an effective scattering center for the remaining mobile carriers. The Conwell-Weisskopf formula relates carrier mobility

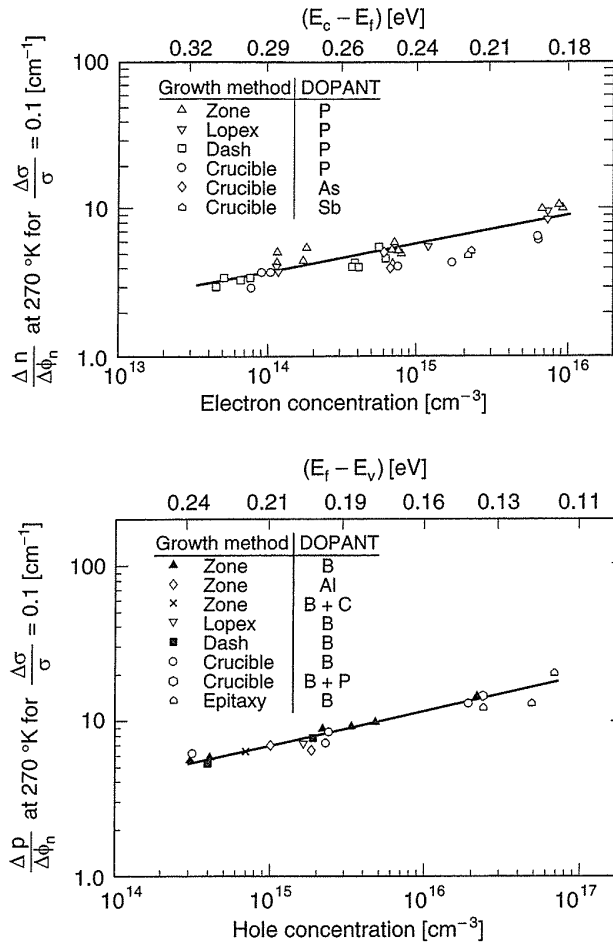


Figure 7.4 Neutron-induced carrier removal rates at 270 K for silicon, evaluated for a 10% shift in resistivity.

to the density of charged scattering centers. Therefore, this formula can be modified by adding $N_{di}k_1\phi$ directly to the density of scattering centers. The resulting mobility decreases monotonically with neutron fluence in a power law fashion [7.1] as $\mu_n = 65 + 1,265\{1 + 6.47 \cdot 10 \exp(-13) \cdot N_{di}(1 + k_1\phi)^{0.72}\}^{-1}$. A similar expression is available for hole mobility.

7.1.2.4 Particle Equivalence. All high-energy nuclear radiation produces displacement damage. The majority of the radiation damage database has been obtained with reactor neutrons and normalized to 1 Mev Equivalent n/cm². Therefore, it is useful to relate displacement damage from other high-energy radiation to neutron damage. It has been conclusively shown that displacement damage is proportional to the energy that goes into atomic displacements, regardless of the type of irradiation. Thus, it is possible to relate the displacement damage for any given type of high-energy radiation to 1 Mev Equivalent neutron damage by a simple proportionality constant.

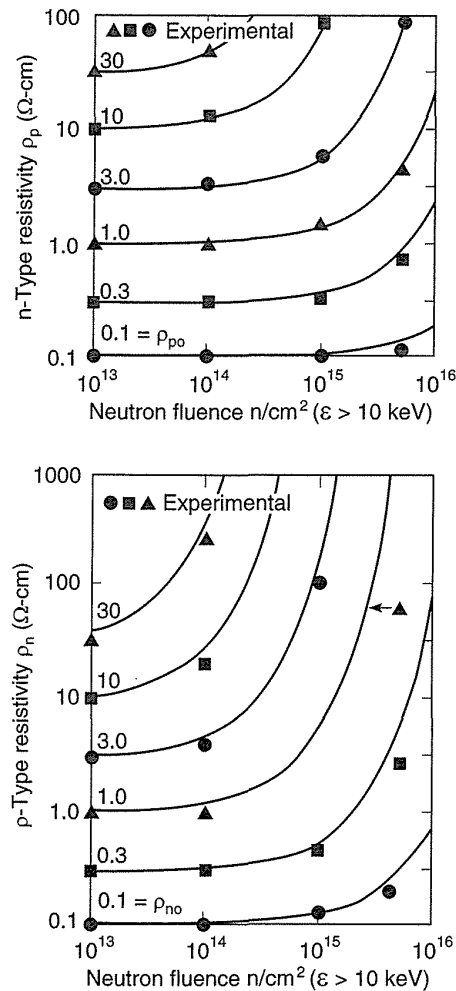


Figure 7.5 Dependence of resistivity on neutron fluence for silicon.

The radiation types of primary interest include protons, electrons, and gammas. Protons and electrons are charged particles that convert most of their energy to ionization in semiconductor materials. Therefore, damage to electron devices is usually dominated by ionizing dose effects. The production of displacements by gamma radiation is a two-stage process: first, a Compton electron is produced, and then the Compton electron can produce displacement damage. Consequently, device damage from gamma radiation is almost always dominated by ionizing dose effects.

7.1.2.5 Device Effects. The dominant effect of displacement damage is the reduction of common emitter current gain in bipolar devices, which is a direct result of the reduction in minority carrier lifetime [7.1]. This effect is proportional to radiation fluence and is given by the Messenger-Spratt equation,

$$\Delta 1/\beta = \phi/2\pi f_t K \quad (7.5)$$

where β is the common emitter current gain, ϕ is neutron fluence, f_t is the common emitter gain-bandwidth product, and K is a constant (approximately 1.6×10^6 for silicon). For bipolar ICs, this shows up as a reduction in parameters such as fanout in digital circuits and open loop gain in op-amps. Second-order effects include increases in resistance, leakage current, and breakdown voltage. Figure 7.6 shows typical current gain data as a function of bias current and neutron fluence.

The dominant effect of displacement damage in MOS devices is an increase in channel resistance and a reduction of transconductance. These effects are a direct consequence of carrier trapping, which reduces carrier density and mobility, and increases device resistivity. Neutron irradiation produces a relatively small ionizing dose due to ionization effects associated with the stopping of recoil silicon atoms. This ionizing dose is sufficient to cause failure in unhardened MOS devices at moderate to high levels of neutron exposure. The ionizing dose depends strongly on the nature of the materials that are shielding the silicon device from the neutrons and the materials in the immediate vicinity of the device.

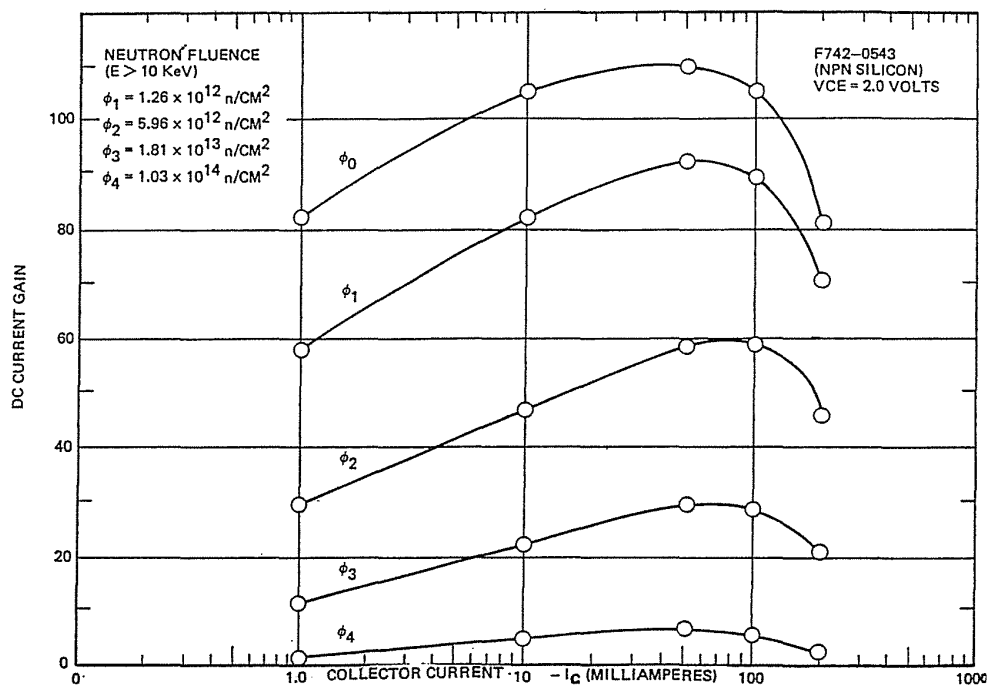


Figure 7.6 DC current gain for a small-signal NPN silicon transistor as a function of bias current for various values of neutron fluence.

7.1.3 Ionizing Dose Damage

Ionizing radiation produces hole-electron pairs in semiconductors and insulators. When these carriers recombine or are swept out of the semiconductor, the effect is transient and no permanent damage can result. However, if some of these carriers are trapped, they can produce significant changes in electrical properties and result in permanent damage. The energy levels of the trapping centers vary from shallow to deep with respect to conduction and valence bands. This leads to a wide variation in annealing properties.

The trapping states at the silicon-silicon dioxide interface exhibit a complex time-dependent buildup. The interplay between time-dependent buildup and annealing processes makes ionizing dose damage in semiconductor devices a complex phenomenon [7.8]. There is no such thing as a unique “total dose” response for semiconductor devices. Ionizing dose quasi-permanent damage is a function of the dose-rate time history, the total dose, and the time after irradiation at which the device is measured. Other important variables include the bias voltage applied and the temperature. The existing ionizing dose database must be used very cautiously. It can only be legitimately extrapolated to environments that closely approximate the dose rate at which the data were taken, as well as the total dose. Often, the dose-rate information is not available; most of the available data are from Co^{60} irradiations done at approximately 300 Rads(Si)/s. The accumulation rate of ionizing dose in space is roughly four orders of magnitude lower, making it virtually impossible to extrapolate the existing data and necessary to obtain additional test data applicable to space dose rates.

A similar problem exists for extrapolation to weapon environments where the prompt dose is delivered in microseconds and the accumulation rate is six to twelve orders of magnitude greater than typical Co^{60} test data. This problem is further exacerbated since some semiconductor devices damage more at Co^{60} rates than at lower dose rates, whereas others damage less. A similar statement holds for higher dose rates compared to Co^{60} rates. A considerable research effort is currently ongoing to improve this situation, with support from the major using agencies, including DOD, DOE, and NASA. At this time, a revision of Mil. Std. 883, Method 1019.4 is planned, which will contain an added anneal step to ensure that the Co^{60} test will yield data that are always more conservative than exposure to either much lower or much higher dose rates.

7.1.3.1 Trapping in Bulk SiO_2 . Most silicon dioxide layers encountered in modern silicon semiconductor devices trap substantially all of the photo generated holes, whereas, nearly all the photogenerated electrons are swept out by the field in the oxide. The net result is an accumulation of trapped holes. In N-channel transistors, this accumulation occurs close to the silicon-silicon dioxide interface where it causes a substantial negative shift in threshold voltage and an increase in leakage current. In p-channel devices, the accumulation of trapped holes occurs close to the gate electrode-silicon dioxide interface where it produces a much smaller negative shift in threshold voltage.

Hole trapping in field oxides produces large voltage shifts that cause leakage current increases. The substrate oxide in silicon-on-insulator (SOI) material is believed to trap both holes and electrons. The majority of hole traps are shallow and are characterized by a distribution of energy levels. As a result, substantial annealing occurs even at room temperature and can be accelerated at elevated temperatures. The accumulation of holes is proportional to the ionizing dose, and the annealing rate is proportional to the density of trapped holes. Therefore, the density of holes at any time after the start of irradiation can be obtained as the linear convolution of the dose rate and the unit impulse response. The unit impulse for threshold voltage shift, which is proportional to trapped hole density, is

$$-\gamma_o \Delta V_{to} = -C_1 \ln t/t_a + C_2 \quad (7.6)$$

where γ_o is the impulse dose, ΔV_{to} is the threshold voltage shift, t is time in minutes, t_a is one minute, and C_1 and C_2 are constants that depend on the manufacturing process [7.1].

7.1.3.2 Trapping at the SiO_2 -Si Interface. Many modern MOS devices also exhibit a buildup of electrons trapped in interface states. This buildup is a complex two-stage phenomenon that leads to a time-dependent buildup, as well as time-dependent annealing behavior. The electron traps are significantly deeper than the hole traps, so that annealing effects at ordinary device application temperatures are dominated by annealing of trapped holes. The trapped holes and electrons tend to cancel each other in terms of their effect on threshold voltage shift.

Interface states tend to be amphoteric, and p-channel devices usually exhibit a buildup of trapped holes. These traps add to the effect of the holes trapped in the silicon dioxide.

Interface state charge, either holes or electrons, is effective in reducing channel mobility, transconductance, switching speed, and increasing channel resistance [7.8].

7.1.3.3 Device Effects. The degrading effects of ionizing dose on semiconductor devices are extremely complex and poorly understood. The radiation effects community continues to utilize a “total dose” terminology that is almost completely incorrect for describing ionizing dose damage. The majority of ionizing dose damage measurements have been made in Co^{60} at approximately 300 Rads(Si)/s. These data can be used to make relative hardness comparisons between devices where the damage is caused primarily by hole storage in the oxide. Linear convolution can usually be relied on for extrapolation to much higher and much lower dose rates for devices where hole storage is the dominant failure mechanism. For devices where hole storage in the oxide and interface charge storage make significant contributions, both effects must be measured and the Co^{60} data cannot be used either to make relative hardness assessments or to extrapolate to other dose rates.

Hole storage and interface charge effects can be measured using special techniques. The damaging effects of hole storage on devices can be determined by a technique that rapidly irradiates the device and then measures the affected parameters before the interface charge buildup occurs. The damage caused by interface

states can be determined by irradiating the device and then storing the device at elevated temperatures. The storage temperature and time are selected to anneal substantially all of the oxide charge and allow the buildup of interface states to go to completion. This selection is tricky because too long a time or too high a temperature can also anneal part of the interface states. A storage of 24 hours at 125°C has been used successfully. The best high temperature storage procedure is probably different for different manufacturing processes.

Ionizing radiation effects are poorly understood. There is still no combination of measurements (electrical, chemical, or physical) which can be made on a semiconductor device and used to predict its response in an ionizing radiation environment. This is in marked contrast to neutron, SEU, and dose-rate effects, where our understanding allows reasonable predictions based on device measurements. The microscopic nature of the hole traps and the interface traps is unknown, although a number of models have been proposed in the literature. A quantitative relationship between the density of traps and the manufacturing process is needed, and this must be supplemented by a quantitative relationship between the ionizing dose, density of traps, and trapped charge. The totality of data available suggests that “pure silicon oxide” contains a negligible trap density and that the traps actually observed are crystalline defects, which are strongly affected by the high-temperature processing steps, and chemical defects, which can be inadvertently introduced at many of the process steps. Today, radiation hard processes combine reduced high-temperature processing steps with ultra-clean manufacturing processes to reduce trap densities at the interface and in the oxide. Some success has also been reported by introducing dopants to neutralize interface states.

The effects of ionizing radiation on devices must be obtained by lot sample testing units from a production process and the use of statistical techniques to extrapolate the behavior to be expected from the rest of the lot.

Bipolar devices are relatively unaffected by ionizing radiation. At high levels, however, the current gain is reduced because charge trapping increases the surface recombination velocity at the emitter periphery. Leakage current increases are also experienced in some bipolar structures. Finally, the introduction of oxides as isolating regions in modern bipolar ICs introduces leakage problems; SOI devices are a good example.

MOS devices suffer increased leakage, negative threshold voltage shifts, decreased transconductance, reduced speed, and increased channel resistance. These are the most important failure mechanisms, but it should be remembered that all of the specified electrical parameters will show changes. Figure 7.7 shows threshold voltage changes as a function of ionizing dose for various bias conditions [7.8].

Two insidious results of the complex damage phenomena will now be highlighted. First, the dose-rate dependence makes the total dose failure threshold a strong function of the dose-rate used to test the device. Second, some devices show a failure window. That is, they do not fail until a critical dose level is reached; then they remain in a failed state until a second higher critical dose level is reached; then they again become operative; and finally, they fail again at a third critical dose level. Ionizing dose tests must consider both of these problems to ensure that the test

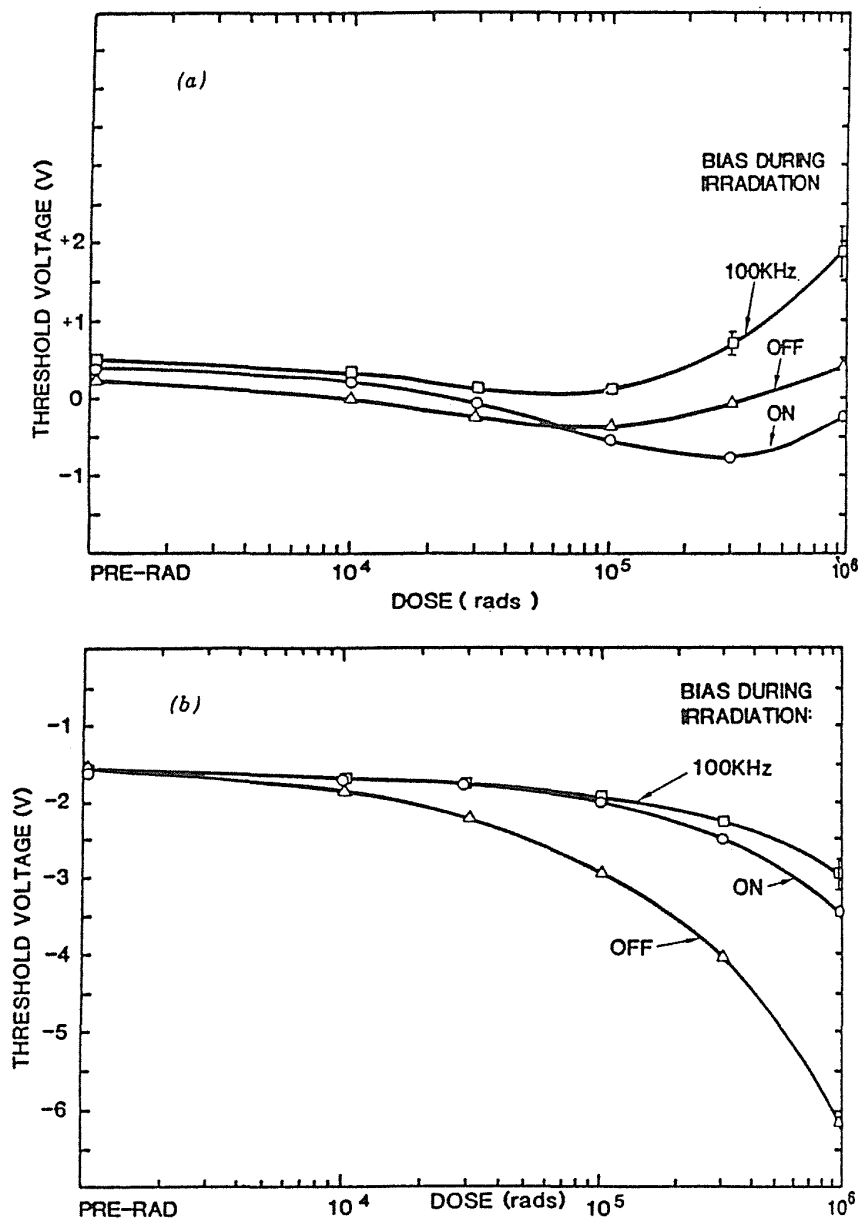


Figure 7.7 Threshold voltage shifts as a function of ionizing dose for transistors biased on and off and switched at a 100 kHz rate.

results are truly applicable to the specified scenario. Figure 7.8 shows ionizing dose failure threshold as a function of exposure rate for a typical unhardened silicon IC [7.8].

Unhardened MOS devices have failure thresholds that range from 500 Rads(Si) to about 50,000 Rads(Si), with PMOS devices about 10 times as hard as comparable

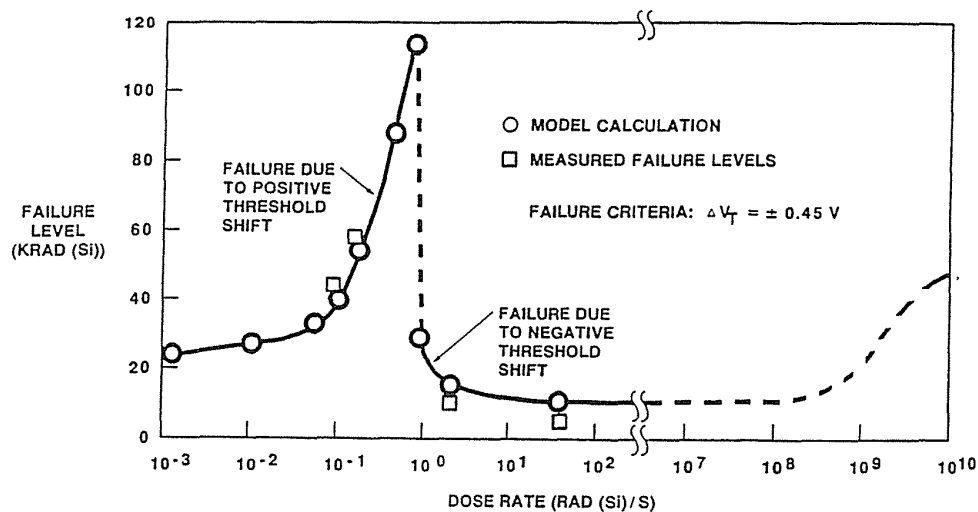


Figure 7.8 Ionizing dose required to produce failure as a function of the dose rate at which the radiation is delivered.

NMOS devices. Most unhardened MOS devices can be used in tactical and avionic applications, although they often require hardness assurance tests. They can also be used in moderate space environments, especially when sufficient shielding is available and hardness assurance tests are incorporated.

Hardened MOS devices are available at ionizing dose levels up to about 1×10^6 Rads(Si). Research programs have yielded operable devices up to 100×10^6 Rads(Si).

7.1.4 Dose-Rate Effects

Dose-rate effects describe the transients excited in devices by bursts of ionizing radiation from nuclear explosions or from simulators such as LINACs and Flash X rays. Photocarriers (hole-electron pairs) are generated in semiconductors and insulators by the ionizing radiation. These carriers are immediately accelerated by the built-in fields and the applied fields resulting in photocurrents. Usually, the magnitude of these photocurrents is well within safe operating limits for semiconductor devices, and no permanent damage results. Frequently, however, these currents exceed the levels required to switch logic devices, and logic errors result in digital circuits. At very high dose-rate levels, for devices biased at high-voltage levels, burnout can occur. This is usually not a problem at tactical and avionic levels but can be a very important problem for space applications with a nuclear weapon specification. At dose-rate levels above 1×10^8 Rads(Si)/s, ICs with parasitic NPNP or PNP parasitic paths can be caused to latch up. Latchup can be catastrophic if the product of the holding current and the applied voltage exceeds the device power-handling capability. In any case, the device, when in the latched condition, will not respond to input signals.

7.1.4.1 Generation Rates. The generation energies for photocarriers in silicon, silicon dioxide, and silicon nitride are 3.6 eV, 18 eV, and 10.8 eV, respectively. The generation constants are silicon— 4.2×10^{13} , silicon dioxide— 8.4×10^{12} , and silicon nitride— 1.4×10^{13} photocarriers per cm^3 per Rad. When photocarriers are created in the vicinity of a P–N junction, a photocurrent is generated, which behaves in the same manner as junction leakage current. The equilibrium photocurrents are proportional to the dose rate, the generation constant, and the effective volume [7.1]. The effective volume is the junction area times the sum of the junction width and the effective diffusion lengths on both sides of the junction. Thus,

$$I_{pp} = qg\gamma A(w + L_p + L_n) \quad (7.7)$$

where q is electron charge, g is the generation constant, γ is the dose-rate, w is the junction width, L_p is the hole diffusion length on the N side of the junction, and L_n is the electron diffusion length on the P side of the junction. For short pulses of radiation (pulse width, t_p , less than the minority carrier lifetime, τ), the photocurrent is given by

$$I_p = I_{pp}(t_p/\tau)^{1/2} \quad (7.8)$$

where I_p is the prompt photocurrent [7.1].

7.1.4.2 IEMP. Internal electromagnetic pulse (IEMP) is created by radiation pulses when they penetrate the walls of an electronic system and the package surrounding an electronic device [7.1]. The EMP is created by Compton electrons and photoelectrons accelerated across cavities in the electronics. The magnitude of the effect depends on the energy, magnitude, and type of incident radiation flux, the thickness and composition of the walls and packaging materials traversed, and the dimensions of the cavity. A thorough discussion of these effects is beyond the scope of this work and can be found in referenced literature. IEMP effects are usually insignificant in tactical and avionic applications (although they cannot be completely neglected), but they are extremely important in space applications that have a nuclear weapons survivability requirement. IEMP effects can be minimized by emphasizing good electromagnetic design practices such as minimizing ground loops, keeping all components close to ground planes, and using dense layout designs to minimize volume and void regions.

7.1.4.3 Burnout. Radiation pulses can cause burnout in electronic devices when they are in a powered-up or biased condition. If the pulse energy is high enough, burnout can occur in unpowered electronics. However, the required levels are above those normally encountered in nearly all applications. Radiation pulses of interest are so short that the energy has a very limited time to be diffused by thermal conduction. In the adiabatic limit, all of the energy goes into a temperature rise in the affected volume. Failure usually occurs in metallization runs, vias, or p–n junctions. The energy dissipated during the pulse can be estimated as the product of the resistance, pulse width, and photocurrent squared for resistive elements such as metallization stripes and vias. The resulting temperature rise is the product of the

energy dissipated and the mass involved, divided by the specific heat. For p–n junctions, the energy dissipated is the product of the bias voltage, pulse width, and junction photocurrent. If the bias voltage is not “stiff,” it may sag or collapse during the pulse, and under these circumstances, the dissipated energy is reduced. The temperature rise is again approximated as the product of the energy dissipated and the mass of the junction, divided by the specific heat. Device failure threshold can be estimated by comparing the temperature rise to maximum device temperature specifications, the intrinsic temperature for the semiconductor resistivities involved, or the melting temperature for the regions involved.

Many modern semiconductor devices exhibit a photoresponse that follows the prompt pulse, whereas others produce photocurrents that persist long after the pulse is over. The extended response comes from the lifetime of photocarriers in extended bulk silicon or substrate regions. Devices that show this response, such as monolithic CMOS ICs, are much more susceptible to burnout than are devices such as CMOS-SOI or CMOS-SOS ICs. The pulse widths encountered are often sufficiently long, especially considering the extended response, so that thermal conduction is possible in one dimension. In this case, a solution to the thermal continuity equation results in a temperature rise proportional to the product of the power per unit area (P/A) and the square root of the pulse width, t_p [7.1]. This result has been applied to semiconductor devices, and measured values of the Wunsch–Bell constant are available in several industry data bases. Thus,

$$\Delta T_f = K t_p^{1/2} P_f / A \quad (7.9)$$

where ΔT_f is the temperature rise at failure, K is the Wunsch–Bell constant, P_f is the power at failure, and A is the junction area. Values of ΔT which result in device failure range from about 100°C to 1400°C. The values of K tabulated in databases are usually worst case measurements and can be used to estimate survivable levels of P/A .

7.1.4.4 Latchup. Some modern IC families are subject to latchup. Latchup is caused when a radiation pulse or an electrical transient turns on a PNP or an NPN parasitic path within the monolithic structure [7.1, 7.8]. Bulk CMOS ICs are particularly susceptible, whereas CMOS-SOS, CMOS-SOI, PMOS and NMOS ICs cannot latchup. Latchup can be suppressed on bulk CMOS ICs by utilizing lightly doped epitaxial silicon on heavily doped starting wafers. This approach is coupled with frequent body and substrate ties to reduce parasitic resistance enough to eliminate latchup. Other logic families, such as low power Schottky TTL ICs, have a low probability of latchup. Latchup can be catastrophic if the power dissipated in the latch up path is sufficient to cause failure. Otherwise, the applied bias can be removed, thus breaking the latchup path. Subsequently, the bias can be reapplied and the device will function normally. While a device is latched, it will not respond to input signals to the affected regions.

The electrical requirement for latchup is that the product of the common emitter current gains in the interconnected parasitic PNP and NPN transistors be greater than unity. Current gain increases with bias current, so that any transient, electrical

or radiation, that increases the current through the parasitic latchup path may cause latchup. Current gain also increases with temperature, so that it is possible for a device which will not latch at room temperature to exhibit latchup at elevated temperatures. The internal biases on the latchup path are affected by series and parallel resistances that can shift as a function of radiation and temperature. Thus, devices may exhibit latchup windows as the dose rate increases. These devices show no latchup up to a threshold value; then they exhibit latchup up to a higher value of dose-rate, and they do not latch up at even higher dose rates. These complexities make it virtually impossible to design a cost-effective, but highly reliable, hardness assurance screen.

The latchup problem can be most effectively resolved by using a combination of the following proven techniques: (1) use only ICs from families that cannot latch up, (2) use a power-sequencing scheme to immediately remove bias after a prompt radiation pulse and restore the bias no sooner than 100 microseconds later, and (3) place a resistor or inductor in series with the IC to ensure that the current is restricted to a value significantly less than the measured holding current of the latchup path.

7.1.4.5 Upset. Upset usually refers to a logic change produced in a digital device. Frequently, the term is extended to include an output transient that exceeds the device noise margin. There is no general definition of upset for analog circuits, although, for unique applications, an output transient that is large enough to cause functional degradation is often referred to as upset. For the great majority of cases, the transient produced in analog circuits by a short burst of radiation does not cause significant functional degradation and acts much like a large noise pulse. Industry data banks contain upset thresholds for nearly all IC families and a large amount of data on individual devices. The usual hardening techniques are to design the circuitry so that it is fail safe when upset and to go through an appropriate reset procedure to mitigate the effects of the data loss caused by the upset. For serious problems, such as autonomous computer systems in ICBMs, a circumvention subsystem is used. A radiation detector disables the computer logic and clamps the I/Os, and a software program reinitializes the computer to the last valid data set stored in hard memory. The normal computer program then takes over. Upset thresholds vary from approximately 10^7 Rads(Si)/s in unhardened logic families to 10^{11} Rads(Si)/s in hardened CMOS-SOS and CMOS-SOI families [7.1].

7.1.5 Single-Event Phenomena

The trend to higher and higher densities in modern ICs has reached the point at which the ionization produced by the passage of a single cosmic ray, or α particle, through the active volume of a logic device can deposit a charge significantly greater than the charge that maintains the logic state. Under these conditions, the device can be upset. In some cases, the resulting photocurrents can trigger latchup or second breakdown, leading to catastrophic failure [7.1,7.8].

7.1.5.1 Single-Event Latchup/Burnout. Latchup has been observed in some monolithic CMOS ICs after the passage of a high-energy ion through the device. This would obviously be catastrophic in the space environment. Therefore, susceptible devices must be eliminated in the design phase, or the system level fixes discussed in Section 7.1.4.4 must be employed [7.8]. Burnout has been observed in MNOS and SNOS memory devices from a high-energy ion when in a relatively high-gate bias condition typical of the write cycle. The burnout path has been identified through the gate dielectric by subsequent failure analysis. Burnout has also been observed in n-channel power MOS transistors. The high-energy ion triggers a second breakdown, or possibly, a parasitic latchup path leading to burnout. Since n-channel devices are significantly more susceptible than p-channel devices, the second breakdown explanation is probably correct. Power MOS transistors such as HEXFETs are actually composed of thousands of transistors in parallel. The ion track from a cosmic ray particle is capable of triggering the burnout in a single transistor, which then spreads to produce a large burnout area involving many of the neighboring transistors. Hardened n-channel power transistors have been designed which virtually eliminate this failure mode.

7.1.5.2 Single-Event Upset. Single-event upset is of concern in microprocessors and memories. Upsets in a microprocessor invalidate the calculation currently underway, and the only effective mitigating techniques are to use redundancy with recalculation when indicated, or triple redundancy and voting. Upsets in a memory can be detected and corrected using error detection and correction (EDAC) software, with only a small penalty in overhead. The basic technique requires that the bits in a word be separated so that the probability of the same cosmic ray causing multiple bit errors in the same word is vanishingly small. This is readily accomplished, for example, by using sixteen $256\text{ K} \times 1$ memory chips in parallel to form a $256\text{ K} \times 16$ memory. Each 16-bit word then has one bit in each chip. The simplest EDAC technique detects two bit errors and corrects one. Because the SEU rate in space is low for even the most sensitive memory chips, presently this technique is completely adequate.

CMOS-SOS and CMOS-SOI memories show much lower SEU rates than monolithic CMOS ICs. An effective hardening technique has been developed which consists of adding cross-coupled resistors to SRAM cells. These resistors, in combination with the cell capacitance, act as a low-pass filter and prevent the high-frequency transient caused by the cosmic ray particle from upsetting the cell. Cross-coupled capacitors can also be used to lower SEU error rates. The Miller effect multiplies the effective capacitance by the voltage gain of the cell, and the enhanced capacitance filters the cosmic ray transient, preventing cell upset. Transistor feature size must be below 10 microns before SEU rates become significant. Therefore, many older generation IC memories are intrinsically hard with respect to SEU. This is an attractive hardening possibility if the amount of data that must be protected is relatively small. The transient photocurrents generated by a cosmic ray track are essentially over in less than a nanosecond for small particles, such as α particles, and can persist for several nanoseconds for larger particles, such as iron ions.

7.2. FLOATING GATE RADIATION EFFECTS

Several significant hardening efforts have been directed toward EPROMs or EEPROMs, and hardened devices may soon become commercially available [7.10, 7.11]. EPROMs are normally erased by exposure to ultraviolet light, whereas EEPROMs can be erased electrically. However, both device types use a similar gate structure so that their radiation response is similar. The failure threshold in an ionizing dose environment is approximately 5 KRads(Si) and may be extended up to approximately 100 KRads(Si) by use of special circuit design and device-hardening approaches. The ionizing dose environment is the most critical problem for floating gate devices, and so, it will not be necessary to evaluate neutron, dose rate, and SEU response in detail. Unhardened floating gate devices are suitable for use in most tactical and avionic applications, as long as a hardness assurance program is in place to ensure adequate survivability. It should also be possible to use them in low to moderate ionizing dose environments in space by using appropriate shielding in combination with a hardness assurance program. These devices are unsuitable for use in severe radiation environments.

The floating gate contains a polysilicon layer insulated from both the gate and the silicon channel by silicon dioxide layers. A “one” is stored in the memory cell by increasing the electron charge in the polysilicon layer, thereby establishing a relatively high positive threshold voltage for the n-channel transistor. A “zero” is stored by removing the electrons or adding holes, thereby establishing a negative threshold voltage for the transistor. Ionizing radiation tends to reduce the electron charge on the floating gate when a one is stored and to increase the electron charge when a zero is stored. This drives the transistor to an intermediate value of threshold voltage and destroys the stored information.

7.2.1 Basic Effects

MOS transistor threshold voltage is a function of the charge on the floating gate and is given by

$$V_t = V_{t0} + \sigma d / \epsilon \quad (7.10)$$

where V_t is threshold voltage, V_{t0} is the initial threshold of the transistor, σ is the charge density on the gate, d is the oxide thickness between the control gate and the floating gate, and ϵ is the oxide dielectric constant. Three processes contribute to the net loss in electronic charge produced by ionizing radiation on the floating gate; (1) hole injection from the oxides on both sides of the floating gate, (2) hole trapping in the oxides, and (3) electron emission from the floating gate. For the relatively low values of field normally encountered in floating gate memory devices, hole injection and hole trapping are proportional to the field, E .

$$f(E) = 1 - \exp(-kE) \approx kE \text{ for } E \leq 0.5 \text{ MV/cm} \quad (7.11)$$

At high levels of ionizing radiation, the three processes reach an equilibrium characterized by an equilibrium threshold voltage, V_{te} . The continuity equation can be solved for the threshold voltage as a function of ionizing radiation for these

conditions [7.12]. The combined effects of endurance and radiation have also been analyzed and measured [7.13].

7.2.2 Response to Ionizing Radiation

Ionizing radiation reduces the threshold voltage of the transistor in the “one” state toward the equilibrium state value and increases the value of the threshold voltage in the “zero” state toward the equilibrium state value. Radiation therefore closes the window between the two states of the memory. Thus,

$$V_t(D) = V_{te} + (V_{to} - V_{te}) \exp(-AD) \quad (7.12)$$

where D is the ionizing dose in Rads(SiO_2) and A is a constant of proportionality that depends on the specific manufacturing process. This relatively simple result gives excellent agreement between measured and predicted results using only the fitting parameter A , as is shown in Fig. 7.9. The basic process at work is simply the change in charge on the floating gate which can be accurately modeled as a one-dimensional capacitor. The charge is proportional to radiation dose, and its subsequent motion is closely approximated as being proportional to the field. However, the process-dependent constant A reflects the type, quantity, and energy levels of the traps in the oxide regions. Very little is known about these traps, and it is their mitigation that is essential to hardening floating gate memory devices. It is noted in passing that the ultraviolet radiation used to erase EPROMs is really a massive dose of ionizing radiation that creates the equilibrium threshold voltage, V_{te} , without damaging the device in any permanent fashion.

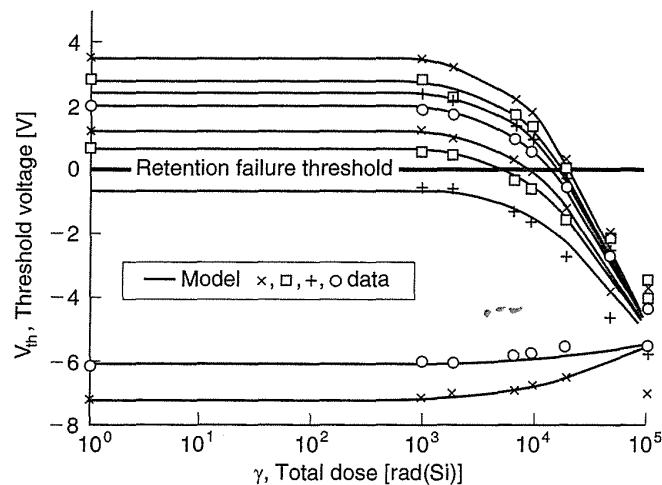


Figure 7.9 Agreement between predicted and measured shifts in threshold voltage as a function of ionizing dose for a floating gate memory device.

7.2.3 Hardening of Floating Gate Devices

Normally, reading the floating gate memory devices is accomplished by comparison with a reference level. Above this level, read “one”; below this level, read “zero.” Obviously, a differential sensing scheme could be used to read the memories, and the radiation failure threshold could be significantly increased. However, this would substantially complicate the memory design and the read circuitry. The memories could be set to a significantly higher “one” threshold by increasing the write cycle drive, thus widening the initial window. This could produce a substantial improvement in radiation failure threshold. Perhaps hardened oxide technology can be applied to the oxides on both sides of the floating gate, but this would require major process modifications. For the foreseeable future, it may be possible to increase the radiation failure threshold by a factor of ten.

7.2.4 Dose-Rate Response

The radiation-induced changes in charge on the floating gate occur extremely fast and will, therefore, follow the radiation pulses normally encountered. The change in threshold voltage will therefore depend on the total ionizing dose in the pulse and will be independent of the dose rate. The dose per pulse is approximately equal to the product of the maximum dose rate and the pulse width (full width-half maximum). For nearly all applications, floating gate memory devices will be limited by the ionizing dose failure threshold and not by dose-rate effects. In most applications, the logic device composing the rest of the digital system will upset at relatively low dose-rates. Therefore, from a system standpoint, dose-rate effects will be very important, even though they will not directly erase the floating gate memories.

7.2.5 Other Radiation Effects

The present relatively low ionizing dose failure threshold for floating gate devices makes it unnecessary to evaluate the neutron failure threshold in detail. For any practical exposure scenario, the ionizing dose failure threshold would be reached while the neutron fluence was below the level that would produce any measurable changes. A semiquantitative neutron failure threshold can be estimated as approximately 10^{14} n/cm², at which level the accompanying ionizing dose would be approaching the failure threshold. At 10^{15} n/cm², the transconductance and channel resistance would also show significant degradation. Floating gate memories are not directly susceptible to SEU since the ionizing charge released by even the highest energy cosmic rays in the vicinity of the floating gate will not cause a significant change in threshold voltage. Again, however, it must be noted that SEU in the controlling logic could result in an erroneous write.

7.2.6 System Considerations

Floating gate memories have a long-term retention problem in that the charge tends to leak off the floating gate under normal operating conditions. This is not a problem for most applications. Radiation also causes charge to leak off the gate. Both of these problems can be mitigated by using a refresh cycle similar to that used for dynamic memories. In fact, it is probably necessary for space applications in which the ionizing radiation accumulates over time. Ionizing radiation effects are known to be strong functions of temperature. The radiation analysis and characterization of floating gate devices have primarily been considered at room temperature. This is probably adequate for many applications, but it should be noted that elevated temperatures will significantly enhance both normal and radiation-induced leakage.

7.3. SNOS RADIATION EFFECTS

Silicon–nitride–oxide–silicon (SNOS) memories have been the traditional devices used where a programmable radiation-hardened nonvolatile memory is required. The silicon–nitride–silicon dioxide gate dielectric sandwich has been effectively used to harden some MOS devices. Adjustment of the oxide and nitride region thicknesses makes the device an effective EPROM. The device is similar to a floating gate device. However, the charge that controls the memory state is a sheet at the nitride–oxide interface. SNOS memories have achieved ionizing dose failure thresholds in excess of 1 MRad(Si).

7.3.1 Basic Effects

Again, the effect of ionizing radiation is to create hole-electron pairs in the gate oxide and nitride. This charge drifts to the oxide–nitride interface where it reduces the threshold voltage if the gate is initially in the “one” state and increases the threshold voltage if the gate is initially in the “zero” state, thus reducing the window. At very large values of ionizing radiation, the threshold voltage reaches an equilibrium value and the stored information is lost. Charge storage must occur in a sheet at the interface between two insulators of different dielectric constants to satisfy the fundamental laws of electrostatics. The problem of dominant radiation effects comes from ionizing dose, and so a detailed discussion of dose-rate, neutron, and SEU effects will not be necessary. Write voltages of 10 to 20 V are used in SNOS memories. Memory gate dielectric burnout from some high-energy ions (typically ions with LETs of Argon or greater) will occur for SNOS memories when a write voltage is applied to the gate. This limits the safe memory cycling specification for SNOS memories in space. For typical applications with less than 10^4 cycles, failure probabilities are very low, with expected error rates less than 10^{-13} errors per bit day.

7.3.2 Response to Ionizing Radiation

The continuity equation can be solved in the gate region (see Fig. 7.10), as a function of ionizing dose and leads to a relationship similar to Eq. (7.12). However, for SNOS devices, a composite solution that combines the effects of normal charge leakage and the effects of radiation-induced leakage has been obtained [7.14] and is given as

$$V_t(D, t) = (V_{t0} - V_v)(t/t_0)^a \exp(-AD) - Bt^a \exp(-AD) \int_{t_0}^t D(t') t'^a \exp(AD) dt' + V_v \quad (7.13)$$

where a is a tunneling constant, V_v is the threshold voltage before the device has been written, erased, or irradiated, V_{t0} is the initial threshold voltage, t_0 is the time immediately after a write pulse when V_{t0} is measured (typically several seconds), A is a process-dependent constant that reflects the type and density of the trapping states in the gate, and B is a constant reflecting the normal charge leakage from the gate. In the absence of radiation, Eq. (7.13) simplifies to

$$a = \ln\{[V(t) - V_v]/[V_{t0} - V_v]\}/\ln(t/t_0) \quad (7.14)$$

from which the value of a can be determined by measuring $V(t)$ at two different times, for example, 5 and 50 seconds. A simple expression for a device irradiated in the virgin state is

$$V_t(D) = B\{\exp(-AD) - 1\} + V_v \quad (7.15)$$

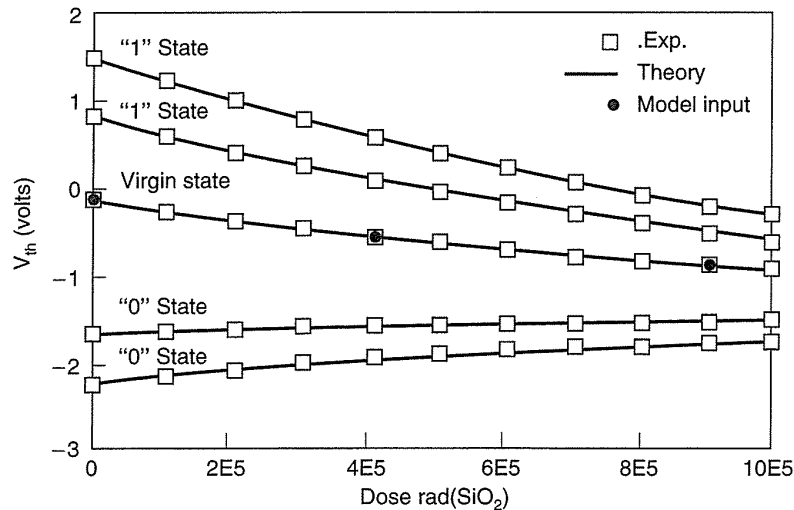


Figure 7.10 Agreement between modeled and experimental changes in threshold voltage for an SNOS memory device.

Irradiating a device at two radiation levels, such as 250 KRads and 1 MRad, allows the constants A and B to be obtained. At this point, Eq. (7.13) can be used to accurately model the time and radiation performance of a SNOS memory device. Unfortunately, the integral is not available in closed form, and a numerical integration must be performed. Again, excellent agreement between this model and the experimental results is obtained, as shown in Fig. 7.10 [7.15].

7.3.3 Response to Dose Rate

The SNOS memory device stores such a large amount of charge at the nitride-oxide interface that the ionization in most prompt pulses of interest cannot degrade the memory. However, the dose-rate upset threshold of a SNOS memory will be determined by the associated read and write circuitry.

When SNOS devices are properly designed into computer systems, they provide EEPROMs with excellent radiation hardness characteristics. The design must provide circumvention to protect the memory from invalid write or erase commands during a prompt radiation pulse, and software to identify and ignore misreads during a radiation pulse. These two requirements are often simultaneously met by the circumvention subsystem.

7.3.4 Response to Neutron Fluence

SNOS memories have a high degree of inherent hardness to ionizing radiation, and so their response to neutrons usually depends only on displacement damage effects. Since they are majority carrier devices, the only effect of lifetime degradation is a small increase in leakage currents. The displacement damage effects of concern are an increase in resistivity and a decrease in channel mobility. These effects were discussed in Section 7.1.2, and the data provided can be used to predict the degradation in transconductance and switching speed, as well as the increase in channel resistance. The failure threshold is usually between 10^{14} and 10^{15} n/cm². The response of the transconductance, g_m , can be obtained as

$$g_m = g_{mo} \exp -(\phi/K) \approx g_{mo}(1 - K\phi) \quad (7.16)$$

where K is a function of the SNOS channel resistivity [7.1]. The increase in channel resistance is obtained in a similar fashion, as is the reduction in cutoff frequency, $f_c = g_m/2\pi C_g$,

$$f_c \approx f_{co}(1 - K'\phi) \quad (7.17)$$

where K' is the sum of K and the mobility degradation constant for the appropriate channel resistivity. Although the radiation effects can be approximately calculated from Eqs. (7.16) and (7.17), K and K' are often obtained as fitted constants from a simple radiation experiment [7.1].

7.3.5 Hardening of SNOS Memories

The hardening of SNOS memories has proceeded by optimizing the manufacturing process to improve the inherent hardness of the nitride–oxide gate dielectric. Since these devices are used in hardened processors and computers, a large effort has been required to harden the associated microcircuits to a level consistent with the SNOS devices. A circumvention procedure is usually required. A detector is used to sense the dose rate at a level substantially below that which would cause an upset. This activates circuits that clamp the memory to prevent miswrites or erasures and activates a software procedure that identifies and ignores any misreads that might have occurred during the pulse. It then restores normal function from a valid start point. This provides continuous operation with only a very short interrupt. For most tactical applications, circumvention is probably not necessary.

7.4. OTHER NONVOLATILE RAMs

EEPROM requirements in radiation environments have also been satisfied using magnetic memories and hardened RAMs with battery backup. Recently, ferroelectric memories have been proposed for hardened nonvolatile applications.

7.4.1 Magnetic RAMs

Magnetic memories include core memories, which have received extensive application, and plated wire memories which so far have received limited application due to their relatively high cost. Bubble memories have also been used in some applications. All of these magneto-inductive devices are inherently hard for the normally encountered range of radiation environments. However, all of these memories must also be protected from invalid write commands and cannot be read in the presence of dose-rate environments approaching the upset level of the associated circuitry. Another type of memory based on the magneto-resistive effect has recently been proposed and is under development.

7.4.2 Static RAMs with Battery Backup

Perhaps the most formidable competitors for radiation-hardened nonvolatile applications are the new state-of-the-art CMOS-SOS and CMOS-SOI RAMs. These devices are not truly nonvolatile but can be designed with battery backup to handle temporary power supply failures. They have the same density, speed, and power requirements as the associated ICs.

7.4.3 Ferroelectric RAMs

Recently, ferroelectric memories have appeared as candidates for radiation-hard nonvolatile memories. The basic cell promises to be inherently hard for environ-

ments of practical interest, but so far the problems of integrating their manufacture with the process for silicon ICs has not been completely solved. However, useful hardened devices are expected in the foreseeable future [7.16].

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Procurement Considerations

8.0. INTRODUCTION

When procuring a microcircuit, many considerations are important. These may be divided into two categories: administrative and technical. Administrative issues, such as price, delivery, service, and product assurance, are not discussed here; instead, technical issues, such as performance, quality, and reliability, are addressed.

In order to ensure that the manufacturer properly executes technical considerations, the customer should verify the existence and adequacy of the manufacturer's product assurance system. Recognized industry standards for quality systems, such as ISO-9001 or EIA-599, can be used for evaluation. With the reduction of the DOD's microcircuit standardization program and the emphasis on purchasing commercial products, there is no longer an independent body to develop or assess microcircuit standards and performance. The user is therefore cautioned to carefully assess any given microcircuit's data sheet and actual performance for compliance with application requirements. There are neither formal industry standards nor documented best commercial practices that clearly define or assess device specifications or performance. Although ISO-9001 registration will assure the adequacy of a company's quality systems, there is no assurance of the adequacy of either the commercial data sheet or device performance to meet application requirements. "Best commercial practices" are perfectly adequate for many applications; however, application requirements, for example, temperature range, endurance, and data retention,

for reprogrammable nonvolatile memories often necessitate that the user clearly specify and review device conformance.

The performance of a microcircuit is evaluated on the basis of parameters specified in a data sheet. Quality is a measure of conformance to specification, typically expressed in parts per million (PPM) nonconforming, reference EIA Standard 554. Quality levels, as maximum PPM lot acceptance guarantees, are usually provided in manufacturers' warranty policies. Reliability is an expectation of quality over time, typically expressed as a failure rate in %/1000 hours or failures in time (FITs), or as a mean time to failures (MTTF). Reliability expectations are usually provided in manufacturers' reliability reports for device or process families.

Reprogrammable nonvolatile semiconductor memories have performance values, data sheets, and quality levels similar to other microcircuits. Reliability expectations are complicated by considerations of endurance and data retention, which have failure mode characteristics that are not applicable to other microcircuits. Thus, reprogrammable nonvolatile memories have additional procurement considerations that affect manufacturing methods, data sheet specifications, quality levels, and reliability.

The following sections discuss the elements necessary for a complete data sheet, critical parameters for evaluating the quality of a device, and a reliability evaluation methodology.

8.1. COMMERCIAL SPECIFICATION PRACTICES

The industry uses three primary documents to specify microcircuits: data sheets, reliability documents, and warranty policies. The following sections describe the desired contents of each of these documents.

8.1.1 Data Sheets

Microcircuit electrical performance is specified by a data sheet. Data sheets may be very simple expressions of "nominal" performance levels or an extensive listing of minimum and maximum performance levels under all allowed conditions. The magnitude of testing by the manufacturer usually correlates with the stringency of the specification. The most thorough and detailed device specifications were the Standardized Microcircuit Drawings (SMDs) provided by the U.S. government. Currently, no industry body generates or validates device specifications, that is, data sheet format, specifications, or criteria.

The device data sheet contains a description of how the device performs its intended function, for example, how to write to and read from a memory; and a list of parameters with performance limits and conditions that define and specify how each function is implemented. Testing validates that the circuit performs as specified. Data sheet limits and values are based on considerations of device performance, system requirements, and test capability. The ability to test parameter performance is critical in understanding various data sheet limits and values.

Reprogrammable nonvolatile memories have more complicated features and functions than most memories, due to the complexities and limitations of the technologies used to erase and program the memory cell. The wide variety of technologies used to implement the various features and functions can be confusing or conflicting. Although some features, for example, pin-out, page-write, and Software Data Protection, have been standardized according to reference JEDEC Standard 21-C, there still may be significant differences in performance (e.g., endurance) between manufacturers for supposedly the same device type. In addition, major functional differences exist between devices depending on the intended application. For example, interfacing the memory to the system may be serial or parallel; the number of power supplies required may be one or more; the duration of time to erase and program may take nanoseconds to minutes; and the minimum erase/program element size may be bits, bytes, pages, sectors, or the entire chip. The user must carefully consider the performance of all features and functions when designing with reprogrammable nonvolatile memories.

Device performance will predictably change as a function of environmental parameters. For example, with MOS devices, read speed will be slower at high temperatures, and power supply current will be higher at low temperatures. Therefore, the environment is specified. Device testing by the manufacturer is performed at worst case conditions to assure the user of device conformance to the data sheet under all allowable conditions. The power supply level directly affects the performance of the device; a lower value is worst case for most parameters because of the poorer conductivity of the MOS transistor at lower voltages. This is most evident for read access times, which are generally slower at low V_{cc} and high temperature.

The temperature range is typically specified as commercial, 0 to 70°C; industrial, -40 to 85°C; or military, -55 to 125°C, reflecting the severity of the expected application. Commercial and industrial temperatures are ambient temperatures; therefore, the junction temperature of an operating device will be higher than the ambient, and the device must be tested at other than the specified limits. The test temperature can be calculated as a function of the specified temperature, the device power dissipation at the temperature limit, and the thermal resistance of the package. Military temperatures are case temperatures; therefore, the junction temperature will be the same as the case test temperature. For example, the test temperature, and the specified case temperature are the same, excluding guardbands. Ambient humidity is a test concern because, at low temperatures, frozen condensation can lock the equipment or cause leakage paths.

Devices are typically specified with $\pm 10\%$ power supplies; however, both extremes need not be tested for all parameters. A worst case power supply condition, based on characterization, can be stipulated for most parameters. Thus, the worst case is the only condition that would be tested in production.

Reprogrammable nonvolatile memory test parameters fall into three categories: AC or timing, DC or parametric, and functional. AC parameters are the maximum or minimum timing conditions needed for the device to function, for example, address setup times, data hold times, as well as the minimum/maximum responses from the device, such as read access times. DC parameters are the static levels on

each pin in the various operational modes, including power supply current, input levels, and output leakage. Functional parameters include those timing and static conditions (i.e., AC and DC parameters) necessary for the device to function in a given mode. Specific parameter conditions are usually included in the data sheet and should reflect how the device is tested.

Conventions for measuring parameters should be clearly stated, because device performance can change significantly for apparently minor differences in measuring methods. The most critical reference points are for AC or timing measurements. Timing limits are minimum or maximum timing values for each parameter. Input requirements for the device are specified from the external system point of view, that is, what the system must provide to the device. Responses from the device are specified from the device point of view, that is, what the device provides to the system. Timing edge reference points are required to differentiate between the provided input pulse levels or output levels and their respective (as recognized by the device) valid trip points. Edge reference points must be specified relative to where the device recognizes a valid signal level. Actual test specification edge reference points generally indicate those points that the tester recognizes as the beginning of a transition for timing measurement, not where the device recognizes a valid signal. The difference provides a built-in guardband between test conditions and actual performance requirements. The levels specified for DC or static performance may not be the same levels specified for AC or timing performance.

Integral to the testing of an integrated circuit is the test philosophy utilized to determine the parameters that are tested and in what manner. Included in the philosophy are guardbanding methodologies, interface hardware design rules, test routine algorithms, and characterization requirements.

Guardbanding is the off-setting of a parameter, condition, or attribute acceptance level from the specified value. Guardbanding is done to account for variability in equipment and device performance or to make test programs more efficient and effective. Machine guardbands, implemented in the forcing, measured, or external conditions, are required to account for the accuracy and precision capabilities of testers, interface hardware, and handlers. Device guardbands are implemented where device performance greatly exceeds the parameter limit; thus, an early warning of a change in performance is available. Test program guardbands are implemented to speed up device testing, where worst case conditions can be applied based on predictable device behavior, for example, for pattern sensitivities.

Parameter conformance to specification can be measured in a variety of ways. In variate testing, which is generally used only for characterization, the actual value of the parameter is determined. For DC parameters, this is relatively simple because the measurement is effectively the output of a voltmeter or ammeter. For AC parameters, this can be very complex, depending on the timing signal measured, because a narrow strobe must be continuously repositioned until the desired transition is detected or the reference edge must be continuously repositioned until the desired output is obtained. Various addressing and data patterns can be utilized, which can significantly affect test time, for example, a galpat versus an address increment addressing pattern. Traditional RAM read/write patterns are not usually employed because most reprogrammable nonvolatile memories have much longer write times

compared with their read times. Variate testing, whether on an automated tester or a bench setup, is used primarily to validate the design and performance models for initial device release or after design changes.

Attribute testing is the comparison of a measured parameter under given conditions to a specified limit. The tested parameter then either passes or fails—go/no-go. Some parameters are directly compared with the limit, whereas others must be “tested by inference” or “tested by the application of specified signals and conditions.” Tested by inference is the validation of the performance of a parameter by the measurement of the correct performance of a correlated parameter or function. Tested by inference also applies when testing a worst case condition; therefore, all other conditions need not be tested. Tested by the application of specified signals and conditions is the applying of input parameters at their specified minimum or maximum and measuring the correct performance of a dependent parameter or function. Parameters that are outputs from the device are measured or compared with standards. Inputs to the device are tested by inference or application of specified signals and conditions.

Data sheets usually reference mechanical specifications for the packages containing the microcircuits. Most packages conform with JEDEC Publication 95. Otherwise, the manufacturer should have a similar type of specification that provides all dimensional and material requirements. Visual and mechanical quality characteristics are usually inspected for compliance to the applicable specification by the manufacturer before shipment of the devices. Dimensions, such as package thickness and lead spacing, may be critical for automatic insertion equipment operation. Composition, such as lead finish, may be critical for solderability. Explicit methodology and criteria for validating mechanical and visual performance are contained in JEDEC Standard 22 or MIL-STD-883 for plastic and hermetic devices, respectively.

Data sheets are typically divided into several sections. The following lists and describes appropriate sections for reprogrammable nonvolatile memories:

Product Description: A prose description of each device function and feature.

Package Pinouts: A drawing of each offered package, with pin assignments.

Block Diagram: A drawing of the overall logical architecture of the device, identifying external control signals and major logic blocks.

Pin Description: A tabular description of each pin assignment, including symbol, name, and function.

Operation Mode Tables: A tabular description of each functional mode of the device, including the status of each externally applied signal and internally generated signal.

Reliability Characteristics: A tabular listing of reliability parameters, including endurance, data retention, electrostatic discharge (ESD) immunity, and latchup that identifies the specification limit, units, and test method.

Absolute Maximum Stress Ratings: A list of those parameters and limits, which if exceeded, could cause permanent damage to the device.

Operating Range: A table of the temperature and voltage operating range limits.

DC Operating Characteristics: A table listing DC parameters, limits, units, and test conditions. Note: “Typicals” should not be listed in this table, but provided in the form of a plot of the parameter as a function of key external variables, that is, voltage, temperature.

AC Characteristics: A table listing AC parameters, limits, units, and test conditions. Often, separate tables will be provided for the read and write functions. Note: “Typicals” should not be listed in this table, but provided in the form of a plot of the parameter as a function of key external variables, that is, voltage, temperature.

AC Conditions of Test: A table and drawing defining the input and output conditions and loading during AC measurements.

Timing Diagrams: A graphical description of each function, showing the level and sequence of all signals.

Flowcharts: A graphical flowchart of the sequence of steps to perform each device function.

Device Ordering Information: A table listing the information necessary to generate the applicable part number for each device option, for example, package, speed, temperature range, and voltage.

8.1.2 Reliability Parameters

Reliability evaluation may be divided into two categories: mechanical and electrical. Reprogrammable nonvolatile semiconductor memories are assembled in packages using similar materials and processes as other microcircuits; thus, the mechanical reliability of the package is the same. Package stresses can be used to evaluate thermal and mechanical stress effects on the reprogrammable nonvolatile memory die. Of particular concern is data retention, which can be adversely affected by thermal or mechanical stresses induced during the package assembly or board assembly processes. Adherence to recommended soldering profiles is very important to avoid potential adverse effects on data retention. Mechanical reliability evaluations typically use JEDEC Standard 22 or MIL-STD-883 for test methods.

Electrical reliability for reprogrammable nonvolatile semiconductor memories is different from reliability for other microcircuits. Reprogrammable nonvolatile memory reliability is the summation of the factors of operating life (read), data retention, and endurance [see Eq. (8.1)]; see reference JEDEC Standards 29, 34, and 47. The specific failure modes and mechanisms are described in Chapter 6. The manufacturer’s reliability assurance program for screening, qualification, and product monitoring must address the specific concerns for each technology, for example, floating gate, floating trap.

$$\text{Failure Rate (FR) device} = \text{FR read} + \text{FR endurance} + \text{FR data retention} \quad (8.1)$$

The read, endurance, and data retention failure rates are thermally accelerated; therefore, failure rates must be given stating the temperature, confidence interval,

and apparent activation energy (Arrhenius acceleration) or alternative deceleration technique.

Endurance is the most important failure rate because the actual endurance is a direct function of the application, that is, the number of times the device is rewritten during system operation. In other words, the total system life can be compromised by the endurance capability of the reprogrammable nonvolatile memory. Some device technologies have known endurance wearout mechanisms, which is not a factor in normal operation, but can affect system performance if the specified number of endurance cycles is greatly exceeded.

Endurance is defined as “The measure of the ability of a nonvolatile memory device to meet its data sheet specifications as a function of accumulated nonvolatile data changes,” per IEEE Std 1005-1991, Definitions and Characterization of Floating Gate Semiconductor Arrays. The data sheet specifications include write functionality, data retention, and read access time. Typically, a nonvolatile data change is the completion of an erase/program cycle for each byte, that is, transferring charge to and from the storage node in the memory cell.

Endurance, in floating gate or floating trap MOS technologies, has two primary failure mechanisms: charge trapping or oxide damage. Three failure modes can result—data retention degradation, access time degradation, or loss of write functionality (including various “disturb” mechanisms). The charge is transferred to and from the storage node through an oxide, resulting in the failure mechanisms of oxide damage and charge trapping. These mechanisms are caused by the cumulative effects of passing a current through a nominal insulator and placing a high electric field across an oxide. Thicker oxides have a greater likelihood of measurable charge trapping. Thinner oxides require greater care in processing to reduce initial oxide defects, which cause yield loss. Endurance cycling over the lifetime of the system will cause random oxide damage and charge trapping at some constant low level. Design and processing by the manufacturer must be such as to minimize initial defects and reduce generated defects to the lowest possible level. Stressing and testing must be performed to separate devices with various levels of endurance performance.

When a high number of endurance cycles (before the onset of wearout) or a very low endurance cycle failure rate is desired, error correction is suitable for random failures. Bit or byte error correction methods may be used to improve the endurance of devices whose dominant failure mode is random damage to the oxides which insulate the storage node. Error correction is not practical for uniform charge degradation mechanisms, for example, charge-trapping induced failures. Note that low failure rates during the stipulated useful life region, suitable for most applications, are achieved by proper design, processing, and screening without the use of error correction.

Endurance follows the “bathtub” curve, with an infant mortality region governed by latent defects, a useful life region governed by the intrinsic integrity of the design and process (assuming infant mortality has been eliminated by screening), and a predictable wearout region governed by the cumulative effects of transferring charge through an oxide. The manufacturer eliminates infant mortality during screening and testing. The failure rate level in the useful life region is assessed by way of product monitors. The onset of wearout is determined by extended endurance

cycling, including stressing devices past the initial failure. Endurance cycling, as a periodic qualification test, has historically been considered the preferred means of verifying capability because cycling can be performed in real time and is the actual operating mode of the device.

Data retention has infant mortality, which must be screened in the manufacturing flow. There is a useful life region that is governed by the intrinsic integrity of the design and process. Wearout does not occur (in the sense that permanent, nonreversible degradation is present) because the storage node may be refreshed. Intrinsic data retention, the time the storage node is capable of retaining charge independent of the application, may vary by device design and process technology, but for most technologies it is essentially very long compared with real-world operating conditions. The extrinsic data retention is a function of endurance—that is, data retention degradation introduced by erase/program cycling. Endurance failure rate expectations should contain the extrinsic data retention failure rate induced by endurance. The intrinsic data retention failure rate should be considered independent of endurance.

Test Method 1033 of MIL-STD-883 describes the procedures to be used when performing endurance cycling for screening or endurance performance verification. Various methods exist to eliminate infant mortality. These methods are a function of product design and the dominant failure mechanisms of the process. For example, some devices use endurance cycling, and others use a margin test to screen out infant mortality. Most device manufacturing flows contain an infant mortality data retention unbiased bake screen, for example, per JESD-22-A103 High Temperature Storage Life. Military requirements contain a periodic Quality Conformance Inspection (QCI) that must be performed on SMD or 883 compliant byte-alterable EEPROMs to verify operating life, data retention, and endurance. A similar requirement could be added for other reprogrammable nonvolatile devices in the applicable procurement specification or in the manufacturer's internal manufacturing documentation.

Random defects, which occur naturally in the wafer fabrication process, cause infant mortality endurance or data retention failures. In neither case is there an explicit relationship that correlates infant mortality with device performance in the useful life or wearout regions. To improve yields, manufacturers may include redundant memory in the device which is used to repair initial or infant mortality failures. For large and complex memory arrays, for example, RAMs, EPROMs, or EEPROMs, few device types are shipped that do not include some level of redundancy repair. Due to the localized nature of the random defects that cause initial or infant mortality failures, the reliability of repaired and nonrepaired devices is equivalent.

The endurance failure rate of the reprogrammable nonvolatile memories in a system increases in importance as a function of the number of times the system rewrites the memory during the system's life. System reliability is a function of the failure rate in the specified useful life region of the device, not of the time when the onset of wearout occurs. Given that the operating life failure rate of an MOS memory is on the order of 100 FITs (0.01%/1000 hours) or less, the endurance and intrinsic data retention failure rate contributions to the total failure rate should

be an order of magnitude or more lower than 100 FITs, that is, 10 FITs or less [see Eq. (8.1)].

8.1.3 Warranty Policies

All microcircuit manufacturers provide warranty policies or terms and conditions of sale. These documents are typically divided into three categories: the warranty, the guaranty, and the applicable conditions.

The warranty typically states that any nonconforming device may be returned to the manufacturer for credit or replacement. Conformance is to the data sheet or other applicable procurement specification and is usually for a term of one year from date of shipment.

The guaranty is for lot acceptance and typically states that any lot that fails the lot acceptance sampling plan per the applicable specification may be returned to the manufacturer for credit or replacement, within one year from shipment.

The warranty policy defines those conditions under which devices may be returned, including administrative and technical requirements. Administrative requirements define the logistics and methodology of documenting and returning the affected devices, so that credit may be applied to the correct purchase order. Technical requirements include: defining the condition of returned devices (e.g., must be testable) and the amount of correlation needed to validate nonconformance.

Lot acceptance guarantees, specified per the applicable lot acceptance sampling plan, define guaranteed quality levels. Typically, the quality level applies to all data sheet electrical parameters and the applicable mechanical/visual parameters, but does not apply to reliability expectations. Data retention and endurance may be treated as quality parameters; thus, they often have lot acceptance guaranty. These parameters are conventionally considered reliability expectations; however, the number of years for data retention and the number of cycles for endurance are typically specified in the data sheet. The relatively quick and simple measurement of these parameters allows specific lot acceptance requirements to be stipulated.

Quality levels, measured in PPM nonconforming, are estimates of the average outgoing quality (AOQ) of the manufacturers' production line, after all screening, testing, and acceptance sampling have been performed. EIA Standard 554 defines how to assess AOQ in PPM for microcircuit manufacturing. Transformation of acceptable quality level (AQL) or lot tolerant percent defective (LTPD) sampling plans and lot guaranty levels to AOQ values is treated in standard texts on acceptance sampling.

The warranty policy should contain a definition and statement of guaranty for endurance and data retention. An example is as follows:

Endurance is the measure of the ability of a reprogrammable nonvolatile memory device to meet its data sheet specifications as a function of accumulated erase/program cycles. An erase/program cycle is the act of changing data from original (e.g., erased) to opposite (e.g., programmed) back to original for all bits of the memory array.

The memory shall be capable of the specified number of erase/program cycles per specified memory element, e.g., byte, sector, page, independent of the erase or program method, e.g., byte, page, sector, chip.

Data retention is the measure of the integrity of the stored data as a function of time. Data retention time is the time from data storage to the time at which a repeatable data error is detected.

The device shall be capable of the specified number of years of data retention. This applies across the operating temperature range and after the specified minimum number of endurance cycles.

The memory has a lot acceptance guaranty of a 1% AOQL (LTPD 5/1) for the specified number of endurance cycles and data retention years, as verified by the specified test methodology (see section 8.4.2).

8.2. CRITICAL DEVICE PARAMETERS

Some device characteristics are more important for the operation of the user's system than others. The following sections describe those parameters that are deemed most critical and require careful evaluation.

8.2.1 Electrical

All electrical parameters are important for the correct functioning of a device in an application; however, a few parameters tend to be more visible because they are the ones that most often appear to fail.

Critical DC parameters are input/output leakage, for example, I_{il} , I_{ih} , and power supply currents, for example, I_{cc} , I_{pp} , I_{sb} . High input/output leakage levels, typically caused by electro-static discharge (ESD) or electrical over-stress (EOS) will cause nonfunctionality by address lines, control pins, or outputs being unable to go to correct levels. High power supply currents, either active or standby, typically caused by EOS, may overload supply lines and damage other components. Logic test methods such as I_{ddq} and built-in self test (BIST) are generally not applicable to large memory arrays because these test methods are not sensitive or complete enough to detect subtle memory cell defects or variations.

Critical AC parameters are access timing values (e.g., T_{aa} , T_{ce}), and input/output level conditions (e.g., V_{ih}/V_{il} , V_{oh}/V_{ol}). Access times are sensitive to data patterns, including checkerboard, diagonal, and address patterns, such as address complement and diagonal galpat. If the device is inadequately tested by the manufacturer (i.e., not using worst case data and address patterns), it may occasionally read incorrectly in the application. Input/output level test conditions differ widely from device to device and from manufacturer to manufacturer. Timing values are extremely sensitive to the applied input/output levels. Thus, devices with supposedly the same timing value may function differently in the application because of different levels used during manufacturers' testing.

All parameters should be controlled by the manufacturer's internal documentation for how they are tested. Some parameters, such as capacitance, are only tested initially and after a design change that affects the parameter. Others should indicate whether testing is by inference (e.g., V_{ih-max}), or by application of specified signals and conditions (e.g., setup/hold times). The address and data patterns used for verifying write and read functionality, as well as appropriate machine, test, or device guardbands, should be included in the manufacturer's internal documentation.

8.2.2 Mechanical/Visual

Critical mechanical parameters are the package dimensions of thickness and lead spacing, which can affect how devices interact with automatic insertion equipment or the dimensions of the application; and solderability, which affects the mechanical, thermal, and electrical connection of the device to the application.

Critical visual parameters are the marking of the device and the marking permanency. These clearly and permanently identify the device, as to part number, date code, orientation, and the like.

8.2.3 Reliability

Critical reliability parameters include endurance, data retention, and package integrity. Endurance is application dependent (i.e., how often the device is rewritten) and affects the overall system failure rate. Data retention is application sensitive (i.e., the intrinsic or extrinsic data retention failure rate of some devices or technologies may preclude some applications). Standard package integrity may be application sensitive (i.e., concerns with hermeticity, especially for glass-sealed packages, and concerns with cumulative exposure to temperature and humidity for plastic packages). Plastic package recommended soldering profiles must be carefully adhered to in order to prevent thermal or mechanical stress-induced data retention degradation.

Two other issues, though not exactly normal application reliability concerns, may be of concern when using nonvolatile memories: radiation tolerance and declassification ability. Radiation tolerance is a measure of how much radiation a device may receive and continue to function. In some cases, for similar technologies, radiation tolerance correlates with reliability performance but is not always a means for comparing different reprogrammable nonvolatile technologies for reliability. Declassification ability is a measure of the difficulty or possibility of recovering information that has been supposedly removed (i.e., erased) from the device.

8.3. MANUFACTURER'S SCREENING

The manufacturer of microcircuits must include, as part of the test and inspection flow, various screens to eliminate latent or generated defects that could cause the device to become nonconforming to specification. The following sections describe

some of the more common screening practices for reprogrammable nonvolatile memories.

8.3.1 Electrical

The manufacturing of microcircuits consists of four major steps: fabrication, assembly, screening/test, and quality assurance. Fabrication consists of various physical, chemical, photolithography, and inspection operations to form die on the microcircuit wafer; assembly consists of placing microcircuit die in a package for connection to other elements; screening/test consists of applicable stressing of devices, then identification of the conformance level of each microcircuit (and removing nonconforming devices); and quality assurance of regular sampling to verify quality and reliability performance.

Normal microcircuit manufacturing practices include one or more 100% electrical tests; for example, each device is tested for DC, AC, and functional parameters, separating passing devices by performance level. For complex microcircuits such as reprogrammable nonvolatile memories, electrical testing before assembly (e.g., wafer sort) is done at room temperature, and electrical testing post assembly is performed at high or cold temperature or both. Military devices require testing at high, low, and room temperatures. Commercial devices usually have a single insertion at high temperature and are guardbanded for parameters that are adversely affected by lower temperatures. For example, MOS devices are worst case at high temperature for speed; however, I_{cc} is worst case at low temperature. Therefore, I_{cc} is guardbanded in the high-temperature test.

Complex devices are tested using automated testers (automated test equipment—ATE) and test handlers with suitable interface hardware. The ATE is controlled by software, called a test program, which contains the various algorithms for testing a device. These include the forced and measured values, guardbands, data patterns, and address patterns in a sequence sufficient to exercise all functions at applicable data sheet limits. In addition, manufacturer's test programs typically include special modes that allow operation of the device in a nondata sheet specified manner to improve test effectiveness or efficiency, for example, apply an accelerating stress for reduced test time. Handlers control the ambient temperature for test and segregate devices into various bins by test results.

Users should verify that the manufacturer has fully documented the test program, the interface hardware, the accuracy and precision of the test setup, and the operating procedures for performing tests.

8.3.2 Reliability

Although microcircuits are designed for reliability, variability in manufacturing processes could result in degradation of performance sooner than expected. This infant mortality is usually the result of random latent defects in manufacturing material or processes and may be detected by accelerated stresses.

Reprogrammable nonvolatile memories have two major reliability parameters, endurance and data retention, both of which require evaluation and possible additional screening to remove infant mortalities. Screening of other reliability parameters should be consistent with that of other microcircuits fabricated with similar processes and assembled in similar packages. Test methods should reference MIL-STD-883 for hermetic devices or JEDEC Standards for plastic devices.

The manufacturer's test flow should include screens for endurance and data retention. Typical endurance screening is the performance of some number of endurance (erase/program) cycles or other oxide stress procedure to accelerate latent defects in the charge transmission oxide. Endurance stressing also is used to accelerate defects that can cause various disturb failures—for example, read-disturb and program-disturb. The number and type of disturbs is a function of the process technology and circuit design. Endurance screening is usually followed by a data retention stress, such as a high temperature unbiased bake, for accelerating latent data retention failures. The manufacturer should be able to provide a methodology and data to support whatever endurance and data retention screens are used. Test Method 1033 of MIL-STD-883 provides a format for defining the requirements for an endurance and data retention screen.

8.4. QUALIFICATION TESTING

In order to transfer a microcircuit to production or ship to a customer, manufacturers perform some level of qualification activities. The following sections describe some of these basic qualification activities.

8.4.1 Characterization

Upon identifying a potential device for an application, the device's adequacy for the application must be verified. Given that the application constraints are known, this usually consists of characterizing the electrical and reliability performance of the proposed device. Before embarking on the very expensive effort of device characterization, several other activities should be performed.

The manufacturer should be audited by the user or users' representative, for example, the National Supervising Inspectorate for the ISO-9000 series Quality Systems (NSI) for general capability to consistently manufacture a device that conforms to all applicable specifications. This includes system capability as well as specific technical abilities. The manufacturer may provide information to the user that details the manufacturing technology, device performance specifications, and reliability expectations.

Once the user is satisfied that the manufacturer's quality system and the device's performance comply with the application requirements, the user should obtain some devices for validation of expected results. Testing performed by the user should verify device performance to the data sheet or other applicable specification. This testing can be used as the basis for establishing a correlation between the manufac-

turer's inspection and the user's application. Critical electrical and mechanical/visual parameters may require extra attention to assure consistency in measurement and repeatability in results.

Reliability parameters should receive characterization, especially endurance and data retention. Erase/program cycling and data retention bake should continue until the onset of endurance wearout, that is, where the endurance failure rate increases with additional cycles. Verification of the intrinsic data retention failure rate should establish, using standard deceleration techniques, that the MTTF of the reprogrammable nonvolatile memory is greater than the application's required storage time. Other reliability parameters, such as life test and package stresses, may use data provided by the manufacturer.

Typical endurance and data retention characterization tests consist of choosing two samples. Subject the first sample to the number of endurance cycles at the temperature used in the application, followed by a data retention bake that correlates to the storage time required of the application. Subject the second sample to increasing numbers of erase/program cycles, interweaved periodically with short data retention bakes, until a statistically significant fraction, for example, 20%, of the devices have failed two or more bits. Analysis of these data in conjunction with the manufacturer's supplied data should validate the feasibility of the proposed device in the application.

8.4.2 Verification

After characterization verifies that the microcircuit is capable of meeting the application requirements, some ongoing testing may be required to assure that production deliveries continue to conform to specification. Commonly used methods include source inspection, incoming inspection, regular audits, and periodic monitors.

Source inspection requires the user or designate to witness critical manufacturing or quality assurance operations in order to verify that the shipped product conforms to the applicable specification. Incoming inspection accomplishes a similar purpose by having the user inspect production material upon receipt.

In regular audits, the user periodically assesses the manufacturer to ensure that manufacturing methods, systems, procedures, and specifications are adhered to in the ongoing production of the purchased microcircuits. Periodic monitoring subjects a sample to an incoming test or a characterization evaluation.

Incoming inspection is probably the least productive of the various verification methodologies. Regular audits, combined with periodic monitors, are likely the most effective, but require a skilled and trained audit and evaluation team for implementation. Source inspection is the simplest method for the user to directly verify product conformance to specification. The method that is most appropriate to a given application depends on the relationship of manufacturer and user, the manufacturing and quality system capabilities of both parties, and any other overriding considerations, for example, government requirements. In all cases, regular commu-

nication between manufacturer and user is vital to ensure ongoing performance improvement.

The user should monitor reliability parameters by periodically reviewing the manufacturer's reliability reports, using the following methodology:

An endurance test, reference Method 1033 of MIL-STD-883, shall be added before performing the steady state life test and extended data retention test. Cycling may be chip, sector, block, byte, or page on finished devices. The following conditions shall be met:

- (1) All bytes shall be cycled for a minimum of the specified number of cycles at equipment room ambient.
- (2) Perform parametric, functional, and timing tests at room (high) temperature, after cycling. Devices having bits not in the proper state after functional testing shall constitute a device failure. Separate the devices into two groups for extended data retention and steady state life test, then write correct data patterns.
- (3) Perform extended data retention, consisting of high temperature unbiased storage for 1000 hours minimum at 150°C minimum. The storage time may be accelerated by using a higher temperature according to the Arrhenius relationship and an apparent activation energy of 0.6 eV. The maximum storage temperature in a nitrogen environment shall not exceed 175°C for hermetic or 160°C for plastic devices. All devices shall be written with a charge on all memory cells in each device, such that a loss of charge can be detected (e.g., worst case pattern).
- (4) Read the data retention pattern and perform parametric, functional, and timing tests at room (high) temperature, after cycling and bake. Devices having bits not in the proper state after functional testing shall constitute a device failure.
- (5) Perform steady state life, reference method 1005 condition D of MIL-STD-883, for 1000 hours at 125°C in a nitrogen environment. The steady state life time may be accelerated by using an Arrhenius relationship and an apparent activation energy of 0.4 eV. The maximum operating junction temperature shall not exceed 160°C. All devices shall be written with a checkerboard or equivalent topological alternating bit pattern.
- (6) Read the steady state life pattern and perform parametric, functional, and timing tests at room (high) temperature, after cycling and steady state life. Devices having bits not in the proper state after functional testing shall constitute a device failure.
- (7) The endurance, data retention, and steady state life tests shall individually pass a sample plan to an LTPD of 5/1 (sample size = 77, accept = 1), equivalent to an AOQL = 1%.

8.5. SUMMARY

Reprogrammable nonvolatile memories should be procured with the same care as other microcircuits. The additional application-dependent reliability parameters of endurance and data retention require careful consideration of device design, manufacturing methodology, reliability criteria, and documented performance. The features and functions of various technology and device alternatives require careful consideration before final system design approval.

The preceding sections have outlined major areas in which microcircuits, in general, and reprogrammable nonvolatile memories, in particular, require special procurement considerations.

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- [8.23] IEEE Std-1005-1991, IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays.
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- [8.25] JEP-95, Registered and Standard Outlines for Solid State and Related Products.

Note: A wide variety of MIL-STD-883 and JESD-22-XX Test Methods are applicable to the specification, qualification, and reliability monitoring of reprogrammable nonvolatile memories. Some of particular interest are:

MIL-STD-883, Test Method 1033, Endurance Life.

JESD-22-A103, High Temperature Storage Life.

JESD-22-A112, Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices.

JESD-22-A113, Preconditioning of Plastic Surface-Mount Devices Prior to Reliability Testing.

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William D. Brown is a university professor and head of the Department of Electrical Engineering at the University of Arkansas. As a Member of the Technical Staff at Sandia Laboratories in Albuquerque, NM, from 1969–1977, Dr. Brown initiated Sandia's research and development effort on metal-nitride-oxide-silicon (MNOS) device technology. After joining the faculty at the University of Arkansas in 1977, his nonvolatile semiconductor memory research concentrated on the synthesis and characterization of plasma-enhanced chemical vapor deposited (PECVD) silicon nitride for application in MNOS and SNOS memory devices. Dr. Brown has served on IEEE NVM standards committees, and he is an organizer and participant in the IEEE International Nonvolatile Memory Technology Conference and its precursor conferences.

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