

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	N/A
Filing Date	N/A
First Named Inventor	Jianquan Jia
Title	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	YMTP0261USA3

SIGNATURE of Applicant or Patent Practitioner

Signature	/Roger Chen/	Date (Optional)	12/11/2019
Name	Roger Chen	Registration Number	67314
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
☐ *Total of _____ forms are submitted.			

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

27765

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	AUG 21 2018
Name	SIMON SHI-NING YANG		
Title	CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner or Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Atty. Docket No. YMTP0261USA3

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☒ The attached application, or
☐ United States application or PCT international application number
_____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is Room 7018, No.18, Huaguang Boulevard, Guandong Tech. Industrial Park, Donghu Development Area, Hongshan District, Wuhan City, Hubei Province 430074, P.R.C. (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions,

renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 27765** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Jianquan Jia Date: 2019.11.07

Signature of Inventor: Jianquan Jia

LEGAL NAME OF INVENTOR

Inventor: Ying Cui Date: 2019.11.07

Signature of Inventor: Ying Cui

LEGAL NAME OF INVENTOR

Inventor: Kaikai You Date: 2019.11.07

Signature of Inventor: Kai Kai You

Doc Code: ECOMM.AUTH/ECOMM.WTDW

Doc Description: Internet Communications Authorized/Internet Communications Authorization Withdrawn

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS	Application No.	N/A
	Filing Date	N/A
	First Named Inventor	Jianquan Jia
	Art Unit	N/A
	Examiner Name	N/A
	Practitioner Docket No.	YMTP0261USA3

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. To authorize permission for Internet Communications.

☒ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

II. To withdraw authorization for Internet Communications.

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☒ attorney or agent of record. Registration number 67314

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____

/Roger Chen/
Signature

12/11/2019
Date

Roger Chen
Typed or printed name

3027291562
Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	YMTP0261USA3
		Application Number	
Title of Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1		Remove	
Legal Name			
Prefix	Given Name	Middle Name	Family Name
	Jianquan		Jia
Residence Information (Select One) US Residency • Non US Residency Active US Military Service			
City	Wuhan City, Hubei Province	Country of Residence ⁱ	CN
Mailing Address of Inventor:			
Address 1	Room 7018, No.18, Huaguang Boulevard, Guandong Tech. Industrial Park,		
Address 2	Donghu Development Area, Hongshan District		
City	Wuhan City, Hubei Province	State/Province	
Postal Code		Country ⁱ	CN
Inventor 2		Remove	
Legal Name			
Prefix	Given Name	Middle Name	Family Name
	Ying		Cui
Residence Information (Select One) US Residency • Non US Residency Active US Military Service			
City	Wuhan City, Hubei Province	Country of Residence ⁱ	CN
Mailing Address of Inventor:			
Address 1	Room 7018, No.18, Huaguang Boulevard, Guandong Tech. Industrial Park,		
Address 2	Donghu Development Area, Hongshan District		
City	Wuhan City, Hubei Province	State/Province	
Postal Code		Country ⁱ	CN
Inventor 3		Remove	
Legal Name			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	YMTP0261USA3
		Application Number	
Title of Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kaikai		You	

Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service

City	Wuhan City, Hubei Province	Country of Residence ⁱ	CN
------	----------------------------	-----------------------------------	----

Mailing Address of Inventor:

Address 1	Room 7018, No.18, Huaguang Boulevard, Guangdong Tech. Industrial Park,		
Address 2	Donghu Development Area, Hongshan District		
City	Wuhan City, Hubei Province	State/Province	
Postal Code		Country ⁱ	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Add

Correspondence Information:Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).☐ An Address is being provided for the correspondence information of this application.

Customer Number	27765		
Email Address	rogerchen@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		
Attorney Docket Number	YMTP0261USA3	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	YMTP0261USA3
		Application Number	
Title of Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		

Publication Information:
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2019/112409	2019-10-22
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)¹ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	YMTP0261USA3
		Application Number	
Title of Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Remove Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	YMTP0261USA3
		Application Number	
Title of Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	YMTP0261USA3
		Application Number	
Title of Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Applicant	1	Remove		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.				
Clear				
☒ Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor		
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:				
Name of the Deceased or Legally Incapacitated Inventor:				
If the Applicant is an Organization check here. ☒				
Organization Name	Yangtze Memory Technologies Co., Ltd.			
Mailing Address Information For Applicant:				
Address 1	Room 7018, No.18, Huaguang Boulevard, Guandong Tech. Industrial Park,			
Address 2	Donghu Development Area, Hongshan District			
City	Wuhan City, Hubei Province	State/Province		
Country	CN	Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Applicant Data may be generated within this form by selecting the Add button.				
Add				

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	YMTP0261USA3
		Application Number	
Title of Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		

Assignee	1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
Remove				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add				

Signature:					Remove
NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).					
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	YMTP0261USA3
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Title of Invention	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		

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Title of Invention:		NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		
First Named Inventor/Applicant Name:		Jianquan Jia		
Filer:		Winston Hsu/Krystal Pan		
Attorney Docket Number:		YMTP0261USA3		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
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Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1720

Electronic Acknowledgement Receipt	
EFS ID:	37991555
Application Number:	16709944
International Application Number:	
Confirmation Number:	7658
Title of Invention:	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD
First Named Inventor/Applicant Name:	Jianquan Jia
Customer Number:	27765
Filer:	Winston Hsu/Kate Yeh
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	YMTP0261USA3
Receipt Date:	11-DEC-2019
Filing Date:	
Time Stamp:	04:03:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1720
RAM confirmation Number	E2019BA505094464
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7	Internet Communications Authorized	3673813.PDF	415108	no	2
			3cd8c4f274543c5cb859f90a1b5b73b04b997472		
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8	Application Data Sheet	3673821.PDF	1782380	no	9
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9	Fee Worksheet (SB06)	fee-info.pdf	34679	no	2
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Title

NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD

Cross Reference To Related Applications

[0001] This application is a continuation of PCT Application No. PCT/CN2019/112409, filed on Oct. 22, 2019, the entire contents of which are incorporated herein by reference.

Background of the Invention

1. Field of the Invention

[0002] The present invention is related to a non-volatile memory device and a control method, and more particularly to a non-volatile memory device and a control method capable of applying word line pre-pulse signals with different voltage levels and reducing programming disturb.

2. Description of the Prior Art

[0003] Non-volatile memory devices, such as flash memory, have become the storage of choice in various electrical products, such as personal computers, flash drives, digital cameras, and mobile phones. Flash memory devices have undergone rapid development. The flash memory can store data for a considerably long time without powering, and have advantages such as high integration level, fast access, easy erasing, and rewriting. To further improve the bit density and reduce cost of the flash memory device, a three-dimensional (3D) NAND flash memory has been developed. A 3D NAND memory architecture stacks memory cells vertically in multiple layers, achieving a higher density than traditional NAND memory. As more layers are added, the bit density increases, thus increasing more storage capacity. With the layer increases, the program disturb becomes worse. A pre-pulse signal may be applied to an unselected bit line connect to an unselected memory string so as to remove boosting charges (electrons) of the unselected memory string. However, as the layer increases, the channel length increases accordingly. The effect of bit line pre-charge for electrons remained in the bottom channel will be reduced because of the increased

channel length. A traditional method for improving the bit line pre-charge effect is to extend the bit line pre-pulse time, but this would sacrifice and influence the data programming time. Another traditional method for improving the bit line pre-charge effect is to increase the voltage level of the bit line pre-pulse, but this would increase the risk of the breakdown phenomenon of the bit line transistor. Thus, there is a need for improvement.

Summary of the Invention

[0004] It is therefore an objective of the present invention to provide a non-volatile memory device and a control method capable of applying word line pre-pulse signals with different voltage levels and reducing programming disturb.

[0005] An embodiment provides a non-volatile memory device. The non-volatile memory device includes a memory array including a plurality of memory strings, each memory string including a select gate transistor and a plurality of memory cells connected in series with the select gate transistor; a bit line connected to a first memory string of the plurality of memory strings; a select gate line connected to the select gate transistor of the first memory string of the plurality of memory strings; a plurality of word lines connected to the plurality of memory cells of the first memory string of the plurality of memory strings, each word line connected to a respective memory cell of the first memory string; a first control circuit configured to apply a bit line pre-pulse signal to the bit line during a pre-charge period; and a second control circuit configured to apply a word line signal to a selected word line of the plurality of word lines and apply a plurality of word line pre-pulse signals to word lines disposed between the select gate line and the selected word line during the pre-charge period, wherein voltage levels of the plurality of word line pre-pulse signals are incremental.

[0006] Another embodiment provides a control method of non-volatile memory device. The non-volatile memory device includes a memory array

including a plurality of memory strings and each memory string includes a select gate transistor and a plurality of memory cells connected in series with the select gate transistor. The control method includes applying a bit line pre-pulse signal to a bit line connected to a first memory string of the plurality of memory strings during a pre-charge period; applying a word line signal to a selected word line connected to a selected memory cell of the plurality of memory cells of the first memory string during the pre-charge period; and applying a plurality of word line pre-pulse signals to a plurality of word lines connected to the plurality of memory cells of the first memory string and disposed between the select gate line and the selected word line during the pre-charge period, wherein voltage levels of the plurality of word line pre-pulse signals are different.

[0007] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0008] FIG. 1 is a schematic diagram of a non-volatile memory device according to an embodiment of the present invention.

[0009] FIG. 2 is a schematic diagram illustrating a memory string and related connection lines of the non-volatile memory device shown in FIG. 1 according to an embodiment of the present invention.

[0010] FIG. 3 is a schematic diagram illustrating an unselected memory string and related connection lines of the non-volatile memory device shown in FIG. 1 according to an embodiment of the present invention.

[0011] FIG. 4 and FIG. 5 are signal timing diagrams of the memory string shown in FIG. 3 according to embodiments of the present invention.

Detailed Description

[0012] Please refer to FIG. 1, which is a schematic diagram of a non-volatile memory device 1 according to an embodiment of the present invention. The non-volatile memory device 1 may be an NAND flash memory.

For example, the non-volatile memory device 1 may be a three-dimensional (3D) NAND flash memory. The non-volatile memory device 1 includes a memory array 10 and control circuits 20 and 30. The memory array 10 includes a plurality of memory strings. Each memory string includes a plurality of memory cells. The memory cells of each string are connected together in series. The intersection of a word line and a semiconductor channel forms a memory cell. Top select gate lines TSGs, word lines WLs, top dummy word lines TDMYs, bottom dummy word lines BDMYs and bottom gate lines BSGs are connected between the memory array 10 and the control circuit 20. Bit lines BLs are connected between the memory array 10 and the control circuit 30.

[0013] FIG. 2 is a schematic diagram illustrating a memory string and related connection lines of the non-volatile memory device 1 shown in FIG. 1 according to an embodiment of the present invention. The memory string of the memory array 10 includes, but not limited thereto, a top select gate transistor, at least one top dummy memory cell, a plurality of memory cells, at least one bottom dummy memory cell and a bottom select gate transistor. A bit line BL is coupled to the memory string. A top select gate line TSG is connected to the top select gate transistor of the memory string. The at least one top dummy memory cell is connected in series with the top select gate transistor. At least one top dummy word line TDMY is connected to the at least one top dummy memory cell of the memory string. Each top dummy word line is separately connected to a top dummy memory cell. The plurality of memory cells can be configured to store data. The plurality of memory cells can be connected in series with the at least one top dummy memory cell. Word lines WL are connected to the memory cells of the memory string. Each word line WL is separately connected to a memory cell. Further, the memory cells of the memory string of the memory array 10 are disposed sequentially along a first direction between the top dummy memory cell and the bottom dummy memory cell and accordingly the word lines WL are disposed sequentially along the first direction between the top dummy word line TDMY and the bottom dummy word line BDMY.

[0014] Moreover, the at least one bottom dummy memory cell is connected in series with the plurality of memory cells. At least one bottom dummy word line BDMY is connected to the at least one bottom dummy memory cell of the memory string. Each bottom dummy word line BDMY is separately connected to a bottom dummy memory cell. The bottom select gate transistor is connected in series with the at least one bottom dummy memory cell. A bottom select gate line BSG is connected to the bottom select gate transistor of the memory string. Writing and erasing data in the memory cells can be controlled from the control circuits and external circuits through the connection lines of the non-volatile memory device 1.

[0015] During a pre-charge period (before programming), the control circuit 30 is configured to apply a bit line pre-pulse signal to unselected bit lines BL of unselected memory strings of the memory array 10. For example, for each unselected memory string, the control circuit 30 is configured to apply a bit line pre-pulse signal to an unselected bit line BL of the each unselected memory string during the pre-charge period. The control circuit 20 is configured to apply a top select gate pre-pulse signal to the top select gate line TSG and apply a bottom select gate pre-pulse signal to the bottom select gate line BSG. Moreover, the control circuit 20 is configured to apply a word line signal to a selected word line of the unselected memory string. The control circuit 20 is configured to apply a plurality of word line pre-pulse signals to word lines which are disposed between the selected word line and the top dummy word line TDMY (or the top select gate TSG). The control circuit 20 is also configured to apply a top dummy word line pre-pulse signal to the top dummy word lines TDMY disposed between the word lines and the top select gate TSG and apply a bottom dummy word line pre-pulse signal to the bottom dummy word lines BDMY disposed between the word lines and the bottom select gate BSG.

[0016] Moreover, voltage levels of the plurality of word line

pre-pulse signals applied to the word lines disposed between the selected word line and the top dummy word line TDMY may be different. For example, the voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the selected word line and the top dummy word line TDMY may be incremental. For example, the voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the selected word line and the top dummy word line TDMY are incremental sequentially from a word line disposed adjacent to the selected word line. For example, a first word line pre-pulse signal of the plurality of word line pre-pulse signals can be applied to a first word line of the plurality of word lines, and the first word line is disposed adjacent to the selected word line and between the selected word line and the top dummy word line TDMY. A second word line pre-pulse signal of the plurality of word line pre-pulse signals can be applied to a second word line of the plurality of word lines, and the second word line is disposed adjacent to the first word line and between the first word line and the top dummy word line TDMY. In an embodiment, the voltage level of the second word line pre-pulse signal is greater than the voltage level of the first word line pre-pulse signal.

[0017] A third word line pre-pulse signal of the plurality of word line pre-pulse signals can be applied to a third word line of the plurality of word lines, and the third word line is disposed adjacent to the second word line and between the second word line and the top dummy word line TDMY. In an embodiment, the voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal. A fourth word line pre-pulse signal of the plurality of word line pre-pulse signals can be applied to a fourth word line, and the fourth word line is disposed adjacent to the third word line and between the third word line and the top dummy word line TDMY, and so on. In an embodiment, the voltage level of the fourth word line pre-pulse signal is greater than the voltage level of the third word line pre-pulse signal, and so on.

[0018] In other words, the farther away from the selected word line, the larger voltage level of the word line pre-pulse signal can be applied since the word line pre-pulse signals are applied to word lines disposed between the top select gate TSG and the selected word line. The voltage level of the word line pre-pulse signal applied to the word line located farthest from the selected word line may be the largest among the voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the selected word line and the top dummy word line TDMY. The voltage level of the word line pre-pulse signal applied to the word line located closest from the selected word line may be the smallest among the voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the selected word line and the top dummy word line TDMY. Since the word line pre-pulse signals with different voltage levels are applied to the word lines between the top select gate line and selected word line, the channel potential gradient is therefore enhanced, and thus enhancing the pre-charge effect of the unselected bit line and reducing programming disturb.

[0019] In addition, a voltage level of the top dummy word line pre-pulse signal applied to the top dummy word lines TDMY is greater than the voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the selected word line and the top dummy word line TDMY.

[0020] Moreover, the word lines disposed between the selected word line and the top select gate TSG can be divided into multiple groups of the word lines. Each divided group of word lines may include at least one word line. Note that, the amount of the word lines of each group of the word lines is not limited, and may be varied and designed in accordance with practical system demands and requirements. Each group of the word lines may include at least one word line. For example, please refer to FIG. 3. FIG. 3 is a schematic diagram illustrating an unselected memory string and related connection lines of the non-volatile memory device 1 shown in FIG. 1 according to an embodiment

of the present invention. A top select gate transistor TT, top dummy memory cells TDMY, memory cells MC0 to MCn, bottom dummy memory cells BDMC and a bottom select gate transistor BT are connected in series. FIG. 3 shows the unselected bit line BL, the top select gate line TSG, the top dummy word lines TDMY, the word lines WL0 to WLn, the bottom dummy word lines BDMY and the bottom select gate line BSG. As shown in FIG. 3, suppose the word line WL0 is the selected word line, the word lines WL1 to WLn are divided into a first group of word lines (Bottom WL), a second group of word lines (Middle WL) and a third group of word lines (Top WL). From the bottom to top, the first group of word lines (Bottom WL) includes the word lines WL1 to WLp. The first group of word lines (Bottom WL) is between the selected word line (word line WL0) and the second group of word lines (Middle WL). The second group of word lines (Middle WL) includes the word lines WL(p+1) to WLq. The second group of word lines (Middle WL) is between the first group of word lines (Bottom WL) and the third group of word lines (Top WL). The third group of word lines (Top WL) includes the word lines WL(q+1) to WLn. The third group of word lines (Top WL) is between the second group of word lines (Middle WL) and the top dummy word lines TDMY.

[0021] Please further refer to FIG. 3 and FIG. 4. FIG. 4 is a signal timing diagram of the memory string shown in FIG. 3 according to an embodiment of the present invention. Sequentially from the top of FIG. 4, the signal waveforms in a pre-charge period are: a bit line pre-pulse signal VP_BL, a top select gate pre-pulse signal VP_TSG, a top dummy word line pre-pulse signal VP_TDMY, word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL and a word line signal V_SELWL. During a pre-charge period, the bit line pre-pulse signal VP_BL is applied to the unselected bit line BL of the unselected memory string of the memory array 10. The top select gate pre-pulse signal VP_TSG is applied to the top select gate line TSG. The top dummy word line pre-pulse signal VP_TDMY is applied to the top dummy word lines TDMY. The word line pre-pulse signals VP_TOPWL is applied to the third group of word lines (Top WL). The word line pre-pulse signals

VP_MIDDLEWL is applied to the second group of word lines (Middle WL). The word line pre-pulse signals VP_BOTTOMWL is applied to the first group of word lines (Bottom WL). The bit line pre-pulse signal VP_BL applied to the unselected bit line BL may be a first power supply voltage Vdd. The top select gate pre-pulse signal VP_TSG applied to the top select gate line TSG may be a second power supply voltage Vcc. The top dummy word line pre-pulse signal VP_TDMY applied to the top dummy word lines TDMY may also be the first power supply voltage Vdd. The word line signal V_SELWL applied to the selected word line (WL0) can be a programming voltage.

[0022] In an embodiment, as shown in FIG. 4, the voltage level (1.2 volts) of the word line pre-pulse signal VP_MIDDLEWL is greater than the voltage level (0.6 volts) of the word line pre-pulse signal VP_BOTTOMWL. The voltage level (1.8 volts) of the word line pre-pulse signal VP_TOPWL is greater than the voltage level (1.2 volts) of the word line pre-pulse signal VP_MIDDLEWL. The voltage level (Vdd) of top dummy word line pre-pulse signal VP_TDMY is greater than the voltage levels of the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL. In another embodiment, Please further refer to FIG. 5. FIG. 5 is a signal timing diagram of the memory string shown in FIG. 3 according to an alternative embodiment of the present invention. Sequentially from the top of FIG. 5, the signal waveforms in a pre-charge period are: a bit line pre-pulse signal VP_BL, a top select gate pre-pulse signal VP_TSG, a top dummy word line pre-pulse signal VP_TDMY, word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL and a word line signal V_SELWL. The word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL and the word line signal V_SELWL are negative pulse signals. As shown in FIG. 5, the voltage level (-1.2 volts) of the word line pre-pulse signal VP_MIDDLEWL is greater than the voltage level (-1.8 volts) of the word line pre-pulse signal VP_BOTTOMWL. The voltage level (-0.6 volts) of the word line pre-pulse signal VP_TOPWL is greater than the voltage level (-1.2 volts) of the word line pre-pulse signal VP_MIDDLEWL. The voltage level (Vdd) of top dummy word line pre-pulse signal VP_TDMY is greater

than the voltage levels of the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL.

[0023] In an embodiment, please further refer to FIGs. 3-5. During the pre-charge period, the ending of the word line pre-pulse signal VP_MIDDLEWL applied to the second group of word lines (Middle WL) occurs after the ending of the word line pre-pulse signal VP_BOTTOMWL applied to the first group of word lines (Bottom WL). The ending of the word line pre-pulse signal VP_TOPWL applied to the third group of word lines (Top WL) occurs after the ending of the word line pre-pulse signal VP_MIDDLEWL applied to the second group of word lines (Middle WL). The ending of the top dummy word line pre-pulse signal VP_TDMY applied to the top dummy word lines TDMY occurs after the endings of the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL. As shown in FIG. 4 and FIG. 5, the end point of the word line pre-pulse signal VP_MIDDLEWL applied to the second group of word lines (Middle WL) is after the end point of the word line pre-pulse signal VP_BOTTOMWL applied to the first group of word lines (Bottom WL) during the pre-charge period. The end point of the word line pre-pulse signal VP_TOPWL applied to the third group of word lines (Top WL) is after the end point of the word line pre-pulse signal VP_MIDDLEWL applied to the second group of word lines (Middle WL) during the pre-charge period. The end point of the top dummy word line pre-pulse signal VP_TDMY applied to the top dummy word lines TDMY is after the end points of the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL. Since the word line pre-pulse signals with different ending timing are applied to the word lines between the top select gate line and selected word line, the whole programming speed can be improved effectively.

[0024] Moreover, as shown in FIG. 4, since the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL are positive pulse signals, the falling edge of the word line pre-pulse signal VP_MIDDLEWL is after the falling edge of the word line pre-pulse signal VP_BOTTOMWL during the pre-charge period. The falling edge of the

word line pre-pulse signal VP_TOPWL is after the falling edge of the word line pre-pulse signal VP_MIDDLEWL during the pre-charge period. The falling edge of the top dummy word line pre-pulse signal VP_TDMY applied to the top dummy word lines TDMY is after the falling edges of the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL. As shown in FIG. 5, since the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL are negative pulse signals, the rising edge of the word line pre-pulse signal VP_MIDDLEWL is after the rising edge of the word line pre-pulse signal VP_BOTTOMWL during the pre-charge period. The rising edge of the word line pre-pulse signal VP_TOPWL is after the rising edge of the word line pre-pulse signal VP_MIDDLEWL during the pre-charge period. The rising edge of the top dummy word line pre-pulse signal VP_TDMY is after the rising edges of the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL.

[0025] In an embodiment, please further refer to FIGs. 4-5. During the pre-charge period, the pulse durations (signal lengths) of the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL are incremental. The pulse duration of the word line pre-pulse signal VP_MIDDLEWL applied to the second group of word lines (Middle WL) is greater than the pulse duration of the word line pre-pulse signal VP_BOTTOMWL applied to the first group of word lines (Bottom WL). The pulse duration of the word line pre-pulse signal VP_TOPWL applied to the third group of word lines (Top WL) is greater than the ending of the word line pre-pulse signal VP_MIDDLEWL applied to the second group of word lines (Middle WL). The pulse duration of the top dummy word line pre-pulse signal VP_TDMY applied to the top dummy word lines TDMY is greater than the pulse durations of the word line pre-pulse signals VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL.

[0026] In summary, the embodiments of the present invention provide word line pre-pulse signals with different to drive the word lines between the top select gate line and selected word line so as to enhance channel potential gradient, and thus enhancing the pre-charge effect

of the unselected bit line and reducing programming disturb. Moreover, the embodiments of the present invention provide word line pre-pulse signals with different ending timing to the word lines between the top select gate line and selected word line, and thus improving the whole programming speed effectively.

[0027] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims

What is claimed is:

1. A non-volatile memory device, comprising:
 - a memory array comprising a plurality of memory strings, each memory string comprising a select gate transistor and a plurality of memory cells connected in series with the select gate transistor;
 - a bit line connected to a first memory string of the plurality of memory strings;
 - a select gate line connected to the select gate transistor of the first memory string of the plurality of memory strings;
 - a plurality of word lines connected to the plurality of memory cells of the first memory string of the plurality of memory strings, each word line connected to a respective memory cell of the first memory string;
 - a first control circuit configured to apply a bit line pre-pulse signal to the bit line during a pre-charge period; and
 - a second control circuit configured to apply a word line signal to a selected word line of the plurality of word lines and apply a plurality of word line pre-pulse signals to word lines disposed between the select gate line and the selected word line during the pre-charge period, wherein voltage levels of the plurality of word line pre-pulse signals are incremental.
2. The non-volatile memory device of claim 1, wherein the second control circuit is configured to apply a first word line pre-pulse signal of the plurality of word line pre-pulse signal to a first group of the plurality of word lines disposed adjacent to the selected word line and disposed between the selected word line and the select gate line during the pre-charge period, apply a second word line pre-pulse signal of the plurality of word line pre-pulse signal to a second group of the plurality of word lines disposed adjacent to the first group of the plurality of word lines and disposed between the first group of the plurality of word line and the select gate line during the pre-charge period, and apply a third

word line pre-pulse signal of the plurality of word line pre-pulse signal to a third second group of the plurality of word lines disposed adjacent to the second group of the plurality of word lines and between the second group of the plurality of word lines and the select gate line during the pre-charge period.

3. The non-volatile memory device of claim 2, wherein a voltage level of the second word line pre-pulse signal is greater than a voltage level of the first word line pre-pulse signal and a voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal.
4. The non-volatile memory device of claim 2, wherein an ending of the second word line pre-pulse signal is after an ending of the first word line pre-pulse signal and an ending of the third word line pre-pulse signal is after the ending of the second word line pre-pulse signal.
5. The non-volatile memory device of claim 2, wherein a pulse duration of the second word line pre-pulse signal is greater than a pulse duration of the first word line pre-pulse signal and a pulse duration of the third word line pre-pulse signal is greater than the pulse duration of the second word line pre-pulse signal.
6. The non-volatile memory device of claim 1, wherein the memory array further comprises at least one dummy memory cell, the at least one dummy memory cell is disposed between the select gate transistor and the plurality of memory cells and connected in series with the select gate transistor and the plurality of memory cells, and the non-volatile memory device further comprises at least one dummy word line and each dummy word line is connected to a respective dummy memory cell, wherein the second control circuit is configured to apply a dummy word line pre-pulse signal to the at least one dummy word line.

7. The non-volatile memory device of claim 6, wherein a voltage level of the dummy word line pre-pulse signal is greater than voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
8. The non-volatile memory device of claim 6, wherein an ending of the dummy word line pre-pulse signal is after endings of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
9. The non-volatile memory device of claim 6, wherein a pulse duration of the dummy word line pre-pulse signal is greater than pulse durations of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
10. The non-volatile memory device of claim 1, wherein the first string of the plurality of memory strings is an unselected string and the bit line is an unselected bit line during the pre-charge period.
11. A control method of non-volatile memory device, the non-volatile memory device comprising a memory array comprising a plurality of memory strings, each memory string comprising a select gate transistor and a plurality of memory cells connected in series with the select gate transistor, the control method comprising:
applying a bit line pre-pulse signal to a bit line connected to a first memory string of the plurality of memory strings during a pre-charge period;
applying a word line signal to a selected word line connected to a selected memory cell of the plurality of memory cells of the first memory string during the pre-charge period; and
applying a plurality of word line pre-pulse signals to a plurality of word lines connected to the plurality of memory cells of the

first memory string and disposed between the select gate line and the selected word line during the pre-charge period, wherein voltage levels of the plurality of word line pre-pulse signals are incremental.

12. The control method of claim 11, wherein the step of applying the plurality of word line pre-pulse signals to the word lines connected to the plurality of memory cells of the first memory string and disposed between the select gate line and the selected word line during the pre-charge period comprises:

apply a first word line pre-pulse signal of the plurality of word line pre-pulse signal to a first group of the plurality of word lines disposed adjacent to the selected word line and disposed between the selected word line and the select gate line during the pre-charge period;

applying a second word line pre-pulse signal of the plurality of word line pre-pulse signal to a second group of the plurality of word lines disposed adjacent to the first group of the plurality of word lines and disposed between the first group of the plurality of word line and the select gate line during the pre-charge period; and

applying a third word line pre-pulse signal of the plurality of word line pre-pulse signal to a third second group of the plurality of word lines disposed adjacent to the second group of the plurality of word lines and between the second group of the plurality of word lines and the select gate line during the pre-charge period.

13. The control method of claim 12, wherein a voltage level of the second word line pre-pulse signal is greater than a voltage level of the first word line pre-pulse signal and a voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal.

14. The control method of claim 12, wherein an ending of the second

word line pre-pulse signal is after an ending of the first word line pre-pulse signal and an ending of the third word line pre-pulse signal is after the ending of the second word line pre-pulse signal.

15. The control method of claim 12, wherein a pulse duration of the second word line pre-pulse signal is greater than a pulse duration of the first word line pre-pulse signal and a pulse duration of the third word line pre-pulse signal is greater than the pulse duration of the second word line pre-pulse signal.
16. The control method of claim 11, wherein the memory array further comprises at least one dummy memory cell, the at least one dummy memory cell is disposed between the select gate transistor and the plurality of memory cells and connected in series with the select gate transistor and the plurality of memory cells, and the non-volatile memory device further comprises at least one dummy word line and each dummy word line is connected to a respective dummy memory cell, wherein the second control circuit is configured to apply a dummy word line pre-pulse signal to the at least one dummy word line.
17. The control method of claim 16, wherein a voltage level of the dummy word line pre-pulse signal is greater than voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
18. The control method of claim 16, wherein an ending of the dummy word line pre-pulse signal is after endings of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
19. The control method of claim 16, wherein a pulse duration of the dummy word line pre-pulse signal is greater than pulse durations

of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.

20. The control method of claim 11, wherein the first string of the plurality of memory strings is an unselected string and the bit line is an unselected bit line during the pre-charge period.

Abstract of Disclosure

A non-volatile memory device and a control method are provided and disclosed. The non-volatile memory device includes a memory array, a bit line, a plurality of word lines, a first control circuit, and a second control circuit. The bit line is connected to a first memory string of the memory array. The plurality of word lines are connected to memory cells of the first memory string and each word line is connected to a respective memory cell. The first control circuit is configured to apply a bit line pre-pulse signal to the bit line during a pre-charge period. The second control circuit is configured to apply a word line signal to a selected word line and apply a plurality of word line pre-pulse signals to word lines disposed between a select gate line and the selected word line. Voltage levels of the plurality of word line pre-pulse signals are incremental.

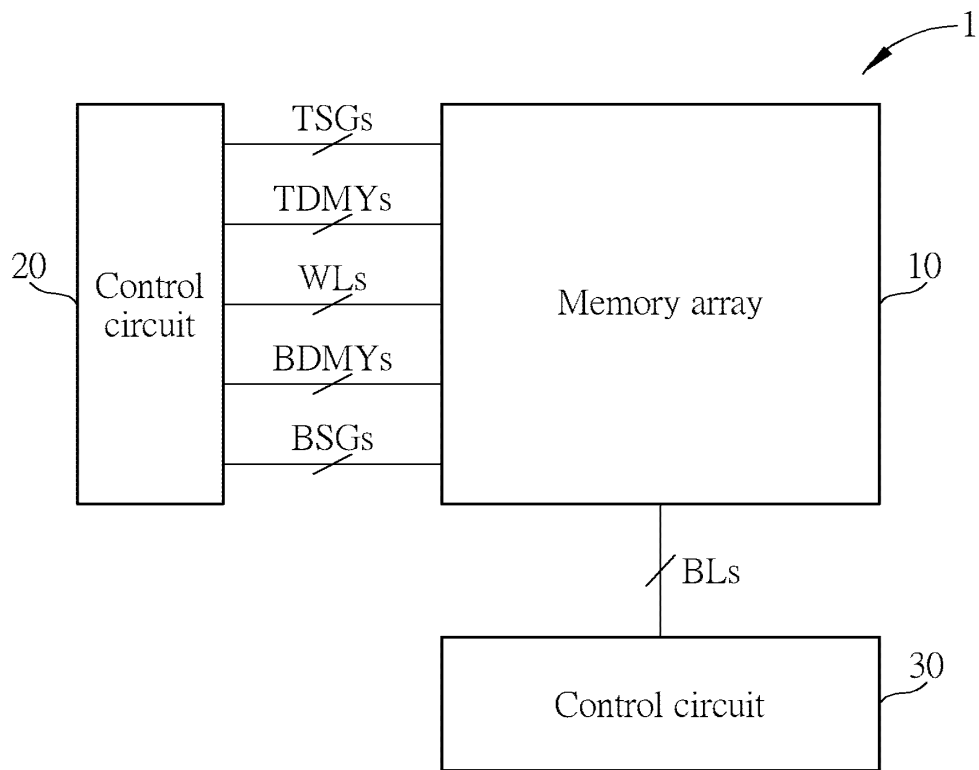


FIG. 1

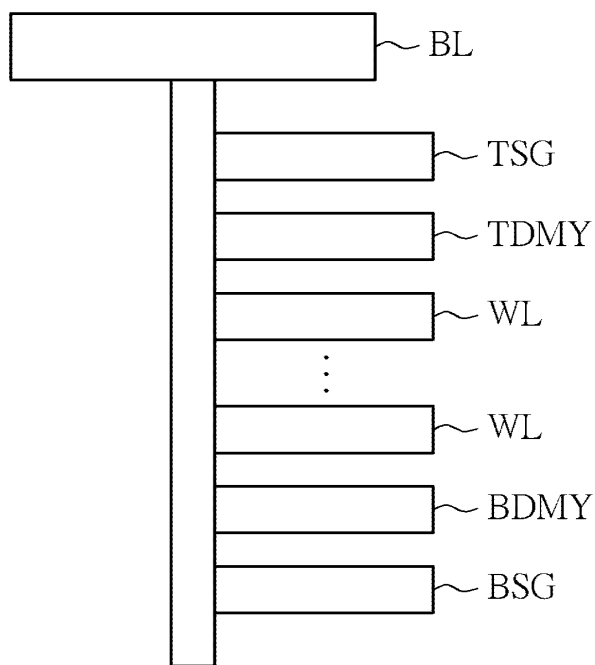


FIG. 2

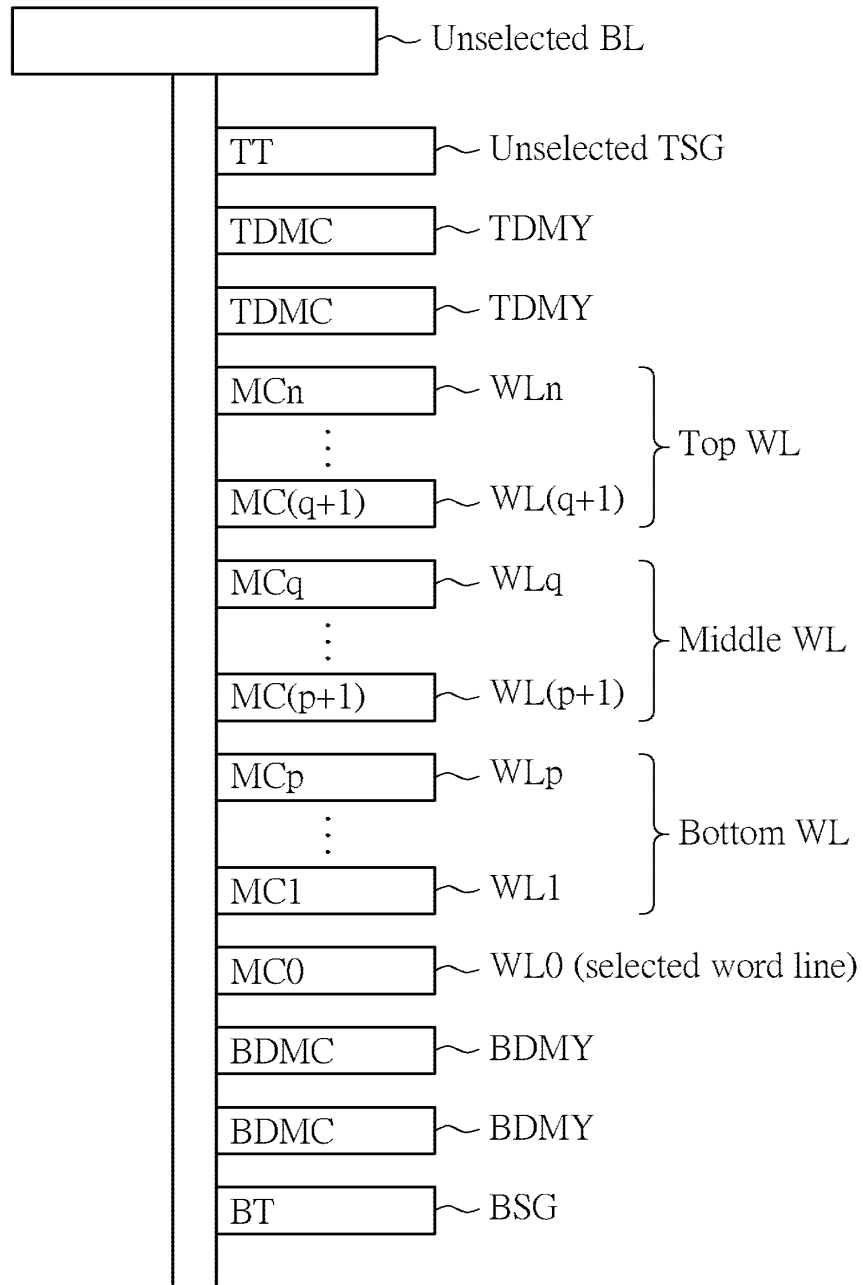


FIG. 3

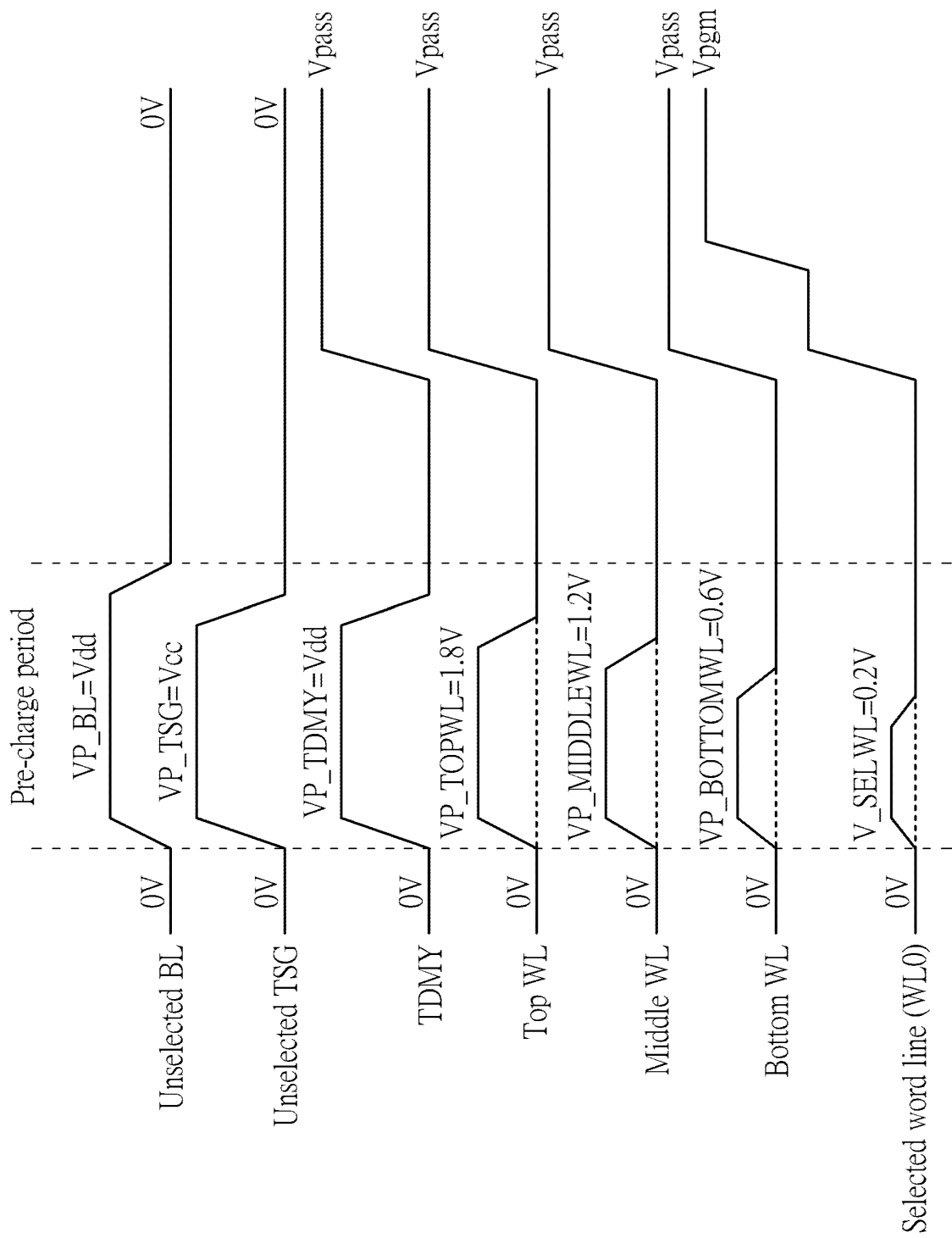


FIG. 4

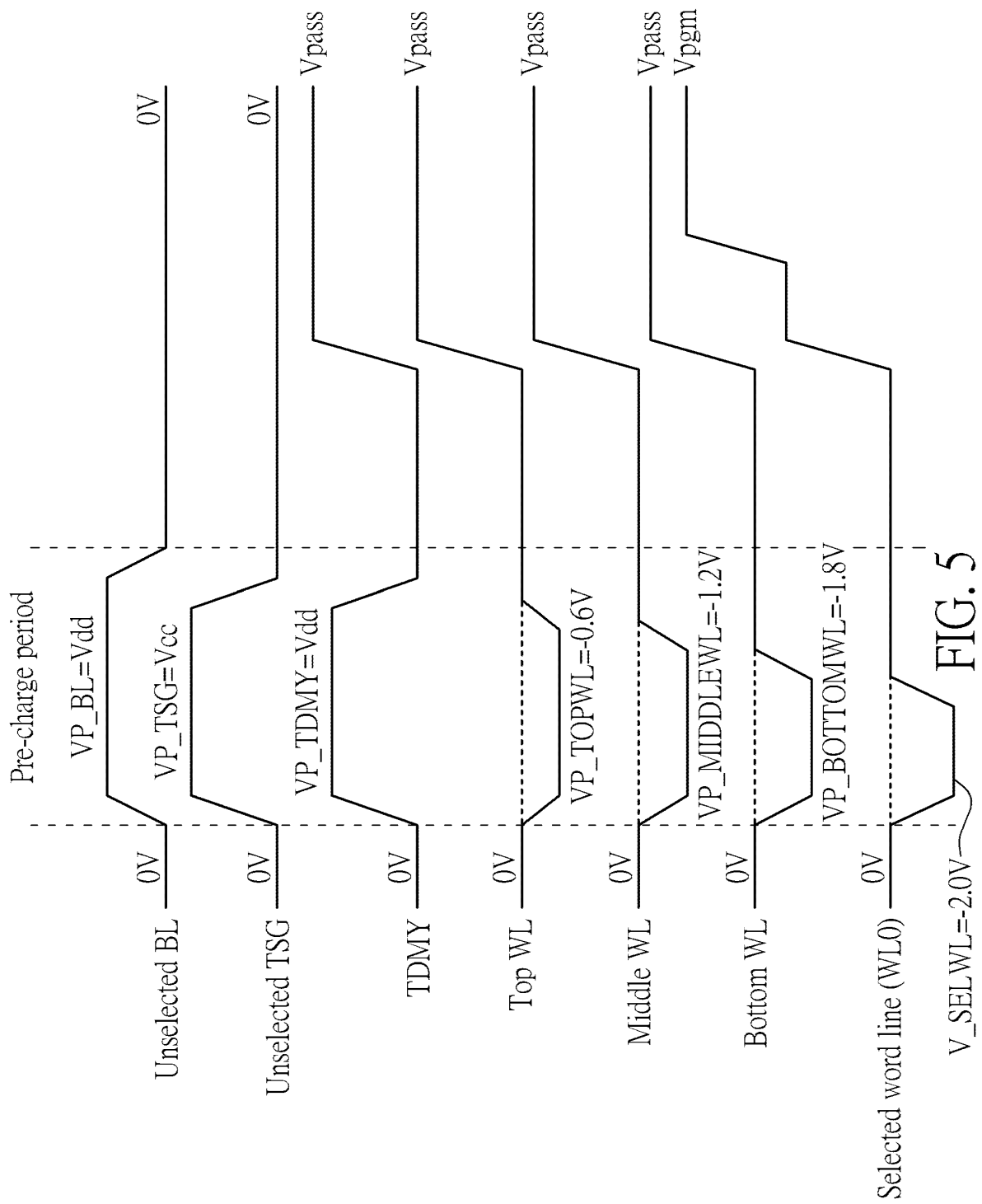


FIG. 5

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/709,944	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/709,944	12/11/2019	2827	1720	YMTP0261USA3	20	2

CONFIRMATION NO. 7658

27765

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

FILING RECEIPT



0000000113698336

Date Mailed: 01/03/2020

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Inventor(s)

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Kaikai You, Wuhan City, CHINA;

Applicant(s)

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Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2019/112409 10/22/2019

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/709,944**

Projected Publication Date: 04/22/2021

Non-Publication Request: No

Early Publication Request: No
Title

NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

U.S.PATENTS								
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
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U.S.PATENT APPLICATION PUBLICATIONS								
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	20110194351	A1	2011-08-11	KIM			
	2	20190108883	A1	2019-04-11	Yu			
	3	20190156901	A1	2019-05-23	Chen			
FOREIGN PATENT DOCUMENTS								
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**INFORMATION DISCLOSURE
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(Not for submission under 37 CFR 1.99)

Application Number	16709944
Filing Date	2019-12-11
First Named Inventor	Jianquan Jia
Art Unit	2827
Examiner Name	NGUYEN, VIET Q
Attorney Docket Number	YMTP0261USA3

NON-PATENT LITERATURE DOCUMENTS

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	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

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Name/Print	Roger Chen	Registration Number	67314

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EFS ID:	40370669
Application Number:	16709944
International Application Number:	
Confirmation Number:	7658
Title of Invention:	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD
First Named Inventor/Applicant Name:	Jianquan Jia
Customer Number:	27765
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Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0261USA3
Receipt Date:	27-AUG-2020
Filing Date:	11-DEC-2019
Time Stamp:	03:45:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3936164.PDF	26299	no	3
			738aadd18e510c9f7d9fc6480965247d86210f0b		
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16709944
	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10283202	B1	2019-05-07	Chen	

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190147955	A1	2019-05-16	Chen	

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	110289034	CN	A	2019-09-27			Abstract

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16709944
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Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2020-10-29
Name/Print	Winston Hsu	Registration Number	41526

abstract of CN110289034A

The present invention relates to a kind of nonvolatile memory and its operating method, which includes: memory cell array, including multiple storage string groups, and each storage string group includes multiple storage strings; common source end is connected to the other end of each storage string via the first string selecting pipe; a plurality of first string selecting pipe wordline, every first string selecting pipe wordline are connected to the grid of the first string selecting pipe of corresponding storage string group; And controller, it is configured that in the pre-conducting phase before the reading stage, the first string selecting pipe of the first string selecting pipe for choosing storage string and non-selected storage string in the multiple storage string is connected, and apply the first lasting pre-charge pressure to the common source end. Nonvolatile memory according to the present invention and its operating method can reduce by the groove potential of the non-selected storage string of increase and read interference.



(21)申请号 201910576900.3

(22)申请日 2019.06.28

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(51)Int.Cl.

G11C 16/08(2006.01)

G11C 16/24(2006.01)

G11C 16/26(2006.01)

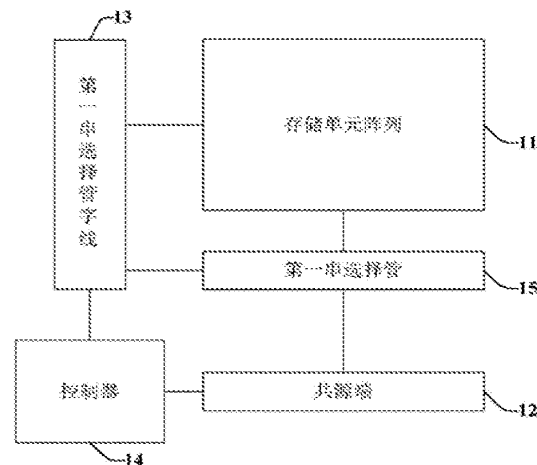
权利要求书2页 说明书10页 附图6页

(54)发明名称

非易失性存储器及其操作方法

(57)摘要

本发明涉及一种非易失性存储器及其操作方法,该非易失性存储器包括:存储单元阵列,包括多个存储串组,每个存储串组包括多个存储串;共源端,经由第一串选择管连接到每个存储串的另一端;多条第一串选择管字线,每条第一串选择管字线连接到对应的存储串组的第一串选择管的栅极;以及控制器,配置为:在读取阶段之前的预导通阶段中,导通所述多个存储串中的选中存储串的第一串选择管和非选中存储串的第一串选择管,且对所述共源端施加持续的第一预充电电压。根据本发明的非易失性存储器及其操作方法,可以通过增加非选中存储串的沟道电势,降低读干扰。



1. 一种非易失性存储器,包括:

存储单元阵列,包括多个存储串组,每个存储串组包括多个存储串;

共源端,经由第一串选择管连接到每个存储串的另一端;

多条第一串选择管字线,每条第一串选择管字线连接到对应的存储串组的第一串选择管的栅极;以及

控制器,配置为:在读取阶段之前的预导通阶段中,导通所述多个存储串中的选中存储串的第一串选择管和非选中存储串的第一串选择管,且对所述共源端施加持续的第一预充电电压。

2. 如权利要求1所述的非易失性存储器,其特征在于,还包括:

多条位线,每条位线经由第二串选择管连接到每个存储串的一端;

多条第二串选择管字线,每条第二串选择管字线连接到对应的存储串组的第一串选择管的栅极;

所述控制器配置为在所述读取阶段对所述多条位线施加驱动电压,所述第一预充电电压大于所述驱动电压。

3. 如权利要求1所述的非易失性存储器,其特征在于,所述控制器配置为在所述预导通阶段结束之前,关断所述非选中存储串的第一串选择管,且保持所述第一预充电电压直至所述预导通阶段结束。

4. 如权利要求1所述的非易失性存储器,其特征在于,所述控制器还配置为在所述预导通阶段中,导通所述选中存储串的存储单元和非选中存储串的存储单元的沟道。

5. 如权利要求2所述的非易失性存储器,其特征在于,所述控制器配置为在所述预导通阶段中,关断所述选中存储串的第二串选择管和所述非选中存储串的第二串选择管。

6. 如权利要求2所述的非易失性存储器,其特征在于,所述控制器还配置为:在所述预导通阶段中,导通所述多个存储串中的选中存储串的第二串选择管和非选中存储串的第二串选择管,且对所述多条位线施加持续的第二预充电电压。

7. 如权利要求6所述的非易失性存储器,其特征在于,所述控制器配置为在所述预导通阶段结束之前,关断所述非选中存储串的第二串选择管,且保持所述第二预充电电压直至所述预导通阶段结束。

8. 如权利要求6所述的非易失性存储器,其特征在于,所述第二预充电电压大于所述驱动电压。

9. 如权利要求6所述的非易失性存储器,其特征在于,所述第一预充电电压和所述第二预充电电压相等。

10. 一种非易失性存储器的操作方法,所述非易失性存储器包括存储单元阵列、共源端和多条第一串选择管字线,所述存储单元阵列包括多个存储串组,每个存储串组包括多个存储串;所述共源端经由第一串选择管连接到每个存储串的另一端;所述多条第一串选择管字线的每条第一串选择管字线连接到对应的存储串组的第一串选择管的栅极;其中所述方法包括:

在读取阶段之前的预导通阶段中,导通所述多个存储串中的选中存储串的第一串选择管和非选中存储串的第一串选择管,且对所述共源端施加持续的第一预充电电压。

11. 如权利要求10所述的方法,其特征在于,所述非易失性存储器还包括多条位线和多

条第二串选择管字线,每条位线经由第二串选择管连接到每个存储串的一端,每条第二串选择管字线连接到对应的存储串组的第一串选择管的栅极;

所述方法还包括在所述读取阶段对所述多条位线施加驱动电压,所述第一预充电压大于所述驱动电压。

12. 如权利要求10所述的方法,其特征在于,在所述预导通阶段结束之前,关断所述非选中存储串的第一串选择管,且保持所述第一预充电压直至所述预导通阶段结束。

13. 如权利要求10所述的方法,其特征在于,还包括在所述预导通阶段中,导通所述选中存储串的存储单元和非选中存储串的存储单元的沟道。

14. 如权利要求11所述的方法,其特征在于,还包括在所述预导通阶段中,关断所述选中存储串的第二串选择管和所述非选中存储串的第二串选择管。

15. 如权利要求11所述的方法,其特征在于,还包括在所述预导通阶段中,导通所述多个存储串中的选中存储串的第二串选择管和非选中存储串的第二串选择管,且对所述多条位线施加持续的第二预充电压。

16. 如权利要求15所述的方法,其特征在于,在所述预导通阶段结束之前,关断所述非选中存储串的第二串选择管,且保持所述第二预充电压直至所述预导通阶段结束。

17. 如权利要求15所述的方法,其特征在于,所述第二预充电压大于所述驱动电压。

18. 如权利要求15所述的方法,其特征在于,所述第一预充电压和所述第二预充电压相等。

非易失性存储器及其操作方法

技术领域

[0001] 本发明涉及半导体器件的技术领域,尤其涉及一种非易失性存储器及其操作方法。

背景技术

[0002] 半导体存储器可以包括易失性存储器(volatile memory,VM)和非易失性存储器(nonvolatile memory,NVM)。易失性存储器通常可以作为操作系统或其他正在运行程序的临时存储介质,如内存。当电源关闭时,易失性存储器不能保留数据。非易失性存储器则用于存储需长期保留的数据,如硬盘。在突然断电或关闭电源的时候,非易失性存储器仍会保留数据。非易失性存储器的示例包括闪存(Flash memory)、只读存储器ROM或电可擦出可编程只读EEPROM等。闪存包括NAND型、NOR型等。

[0003] 对NAND型闪存进行读操作时,施加在选中存储单元上的导通电压需要大于该存储单元的最大阈值。以多级存储单元(MLC)技术为例,导通电压需要大于第四个态的最大阈值。该导通电压会对非选中字线上的存储单元产生读干扰,尤其是对第一个态(L1)的影响最大,会使存储单元阈值向右移动,造成读干扰。在实际的读操作中,考虑到功耗问题,位线上的驱动电压不会太高,远小于导通电压。由于非选中串的沟道没有耦合电势,其沟道电势等于位线上的驱动电压。这样,对于非选中串上的非选中存储单元来说,其沟道电势远小于导通电压,每次读操作都会受到导通电压与沟道电势之差所带来的读干扰。

发明内容

[0004] 本发明所要解决的技术问题是提供一种降低非选中存储单元读干扰的非易失性存储器及其操作方法。

[0005] 本发明的一个方面提出一种非易失性存储器,包括:存储单元阵列,包括多个存储串组,每个存储串组包括多个存储串;共源端,经由第一串选择管连接到每个存储串的另一端;多条第一串选择管字线,每条第一串选择管字线连接到对应的存储串组的第一串选择管的栅极;以及控制器,配置为:在读取阶段之前的预导通阶段中,导通所述多个存储串中的选中存储串的第一串选择管和非选中存储串的第一串选择管,且对所述共源端施加持续的第一预充电电压。

[0006] 在本发明的一实施例中,所述非易失性存储器还包括:多条位线,每条位线经由第二串选择管连接到每个存储串的一端;多条第二串选择管字线,每条第二串选择管字线连接到对应的存储串组的第一串选择管的栅极;所述控制器配置为在所述读取阶段对所述多条位线施加驱动电压,所述第一预充电电压大于所述驱动电压。

[0007] 在本发明的一实施例中,所述控制器配置为在所述预导通阶段结束之前,关断所述非选中存储串的第一串选择管,且保持所述第一预充电电压直至所述预导通阶段结束。

[0008] 在本发明的一实施例中,所述控制器还配置为在所述预导通阶段中,导通所述选中存储串的存储单元和非选中存储串的存储单元的沟道。

[0009] 在本发明的一实施例中,所述控制器配置为在所述预导通阶段中,关断所述选中存储串的第二串选择管和所述非选中存储串的第二串选择管。

[0010] 在本发明的一实施例中,所述控制器还配置为:在所述预导通阶段中,导通所述多个存储串中的选中存储串的第二串选择管和非选中存储串的第二串选择管,且对所述多条位线施加持续的第二预充电电压。

[0011] 在本发明的一实施例中,所述控制器配置为在所述预导通阶段结束之前,关断所述非选中存储串的第二串选择管,且保持所述第二预充电电压直至所述预导通阶段结束。

[0012] 在本发明的一实施例中,所述第二预充电电压大于所述驱动电压。

[0013] 在本发明的一实施例中,所述第一预充电电压和所述第二预充电电压相等。

[0014] 本发明还提出一种非易失性存储器的操作方法,所述非易失性存储器包括存储单元阵列、共源端和多条第一串选择管字线,所述存储单元阵列包括多个存储串组,每个存储串组包括多个存储串;所述共源端经由第一串选择管连接到每个存储串的另一端;所述多条第一串选择管字线的每条第一串选择管字线连接到对应的存储串组的第一串选择管的栅极;其中所述方法包括:在读取阶段之前的预导通阶段中,导通所述多个存储串中的选中存储串的第一串选择管和非选中存储串的第一串选择管,且对所述共源端施加持续的第一预充电电压。

[0015] 在本发明的一实施例中,所述非易失性存储器还包括多条位线和多条第二串选择管字线,每条位线经由第二串选择管连接到每个存储串的一端,每条第二串选择管字线连接到对应的存储串组的第一串选择管的栅极;所述方法还包括在所述读取阶段对所述多条位线施加驱动电压,所述第一预充电电压大于所述驱动电压。

[0016] 在本发明的一实施例中,在所述预导通阶段结束之前,关断所述非选中存储串的第一串选择管,且保持所述第一预充电电压直至所述预导通阶段结束。

[0017] 在本发明的一实施例中,还包括在所述预导通阶段中,导通所述选中存储串的存储单元和非选中存储串的存储单元的沟道。

[0018] 在本发明的一实施例中,还包括在所述预导通阶段中,关断所述选中存储串的第二串选择管和所述非选中存储串的第二串选择管。

[0019] 在本发明的一实施例中,还包括在所述预导通阶段中,导通所述多个存储串中的选中存储串的第二串选择管和非选中存储串的第二串选择管,且对所述多条位线施加持续的第二预充电电压。

[0020] 在本发明的一实施例中,在所述预导通阶段结束之前,关断所述非选中存储串的第二串选择管,且保持所述第二预充电电压直至所述预导通阶段结束。

[0021] 在本发明的一实施例中,所述第二预充电电压大于所述驱动电压。

[0022] 在本发明的一实施例中,所述第一预充电电压和所述第二预充电电压相等。

[0023] 本发明在对非易失性存储器进行读写操作时,通过在读写阶段之前的预导通阶段,对非易失性存储器的共源端施加第一预充电电压,或同时对位线施加第二预充电电压,增加了非选中存储串的沟道电势,减少了非选中存储单元的沟道电势和读取阶段的导通电压之间的电势差,从而降低了读干扰。

附图说明

[0024] 为了让本发明的上述目的、特征和优点能更明显易懂,以下结合附图对本发明的具体实施方式作详细说明,其中:

[0025] 图1是本发明一实施例的非易失性存储器的结构示意图;

[0026] 图2是本发明一实施例的非易失性存储器的部分结构示意图;

[0027] 图3是对图2中所示的存储单元进行读取的时序图;

[0028] 图4是读干扰所带来的存储单元阈值变化示意图;

[0029] 图5是本发明一实施例的非易失性存储器中对存储单元进行读取操作的时序图;

[0030] 图6是本发明另一实施例的非易失性存储器中对存储单元进行读取操作的时序图;

[0031] 图7是本发明一实施例的非易失性存储器的操作方法的示例性流程图。

具体实施方式

[0032] 为了让本发明的上述目的、特征和优点能更明显易懂,以下结合附图对本发明的具体实施方式作详细说明。

[0033] 在下面的描述中阐述了很多具体细节以便于充分理解本发明,但是本发明还可以采用其它不同于在此描述的其它方式来实施,因此本发明不受下面公开的具体实施例的限制。

[0034] 如本申请和权利要求书所示,除非上下文明确提示例外情形,“一”、“一个”、“一种”和/或“该”等词并非特指单数,也可包括复数。一般说来,术语“包括”与“包含”仅提示包括已明确标识的步骤和元素,而这些步骤和元素不构成一个排它性的罗列,方法或者设备也可能包含其他的步骤或元素。

[0035] 在详述本发明实施例时,为便于说明,表示器件结构的剖面图会不依一般比例作局部放大,而且所述示意图只是示例,其在此不应限制本发明保护的范围。此外,在实际制作中应包含长度、宽度及深度的三维空间尺寸。

[0036] 为了方便描述,此处可能使用诸如“之下”、“下方”、“低于”、“下面”、“上方”、“上”等等的空间关系词语来描述附图中所示的一个元件或特征与其他元件或特征的关系。将理解到,这些空间关系词语意图包含使用中或操作中的器件的、除了附图中描绘的方向之外的其他方向。例如,如果翻转附图中的器件,则被描述为在其他元件或特征“下方”或“之下”或“下面”的元件的方向将改为在所述其他元件或特征的“上方”。因而,示例性的词语“下方”和“下面”能够包含上和下两个方向。器件也可能具有其他朝向(旋转90度或处于其他方向),因此应相应地解释此处使用的空间关系描述词。此外,还将理解,当一层被称为在两层“之间”时,它可以是所述两层之间仅有的层,或者也可以存在一个或多个介于其间的层。

[0037] 在本申请的上下文中,所描述的第一特征在第二特征之“上”的结构可以包括第一和第二特征形成直接接触的实施例,也可以包括另外的特征形成在第一和第二特征之间的实施例,这样第一和第二特征可能不是直接接触。

[0038] 应当理解,当一个部件被称为“在另一个部件上”、“连接到另一个部件”、“耦合于另一个部件”或“接触另一个部件”时,它可以直接在该另一个部件之上、连接于或耦合于、或接触该另一个部件,或者可以存在插入部件。相比之下,当一个部件被称为“直接在另一

个部件上”、“直接连接于”、“直接耦合于”或“直接接触”另一个部件时,不存在插入部件。同样的,当第一个部件被称为“电接触”或“电耦合于”第二个部件,在该第一部件和该第二部件之间存在允许电流流动的电路路径。该电路路径可以包括电容器、耦合的电感器和/或允许电流流动的其它部件,甚至在导电部件之间没有直接接触。

[0039] 图1是本发明一实施例的非易失性存储器的结构示意图。参考图1所示,该非易失性存储器包括存储单元阵列11、共源端12、多条第一串选择管字线13和控制器14。其中,存储单元阵列11中包括多个存储串组,每个存储串组包括多个存储串;共源端12经由第一串选择管15连接到每个存储串的另一端;多条第一串选择管字线13中的每条第一串选择管字线13连接到对应的存储串组的第一串选择管的栅极;控制器14配置为在读取阶段之前的预导通阶段中,导通该多个存储串中的选中存储串的第一串选择管和非选中存储串的第一串选择管,且对共源端12施加持续的第一预充电压。

[0040] 图2是本发明一实施例的非易失性存储器的部分结构示意图。图2以3D NAND存储器为例对本发明的非易失性存储器进行说明。但是图2并不用于限制本发明的非易失性存储器的范围。在其他的实施例中,本发明的非易失性存储器可以是2D NAND类型。

[0041] 参考图2所示,以具有垂直沟道结构的3D NAND类型存储器的块结构为例。图1中所示的存储单元阵列11可以包括若干个该块结构。在该块结构中具有多个呈垂直状的存储串210,每个存储串210中包括若干个串接在一起的存储单元,在图2中用黑色圆点表示存储单元。例如,存储串211中具有三个存储单元201。每个存储串210的一端与第二串选择管240相连接,另一端与第一串选择管230相连接。在图2中用黑色圆点表示第一串选择管230和第二串选择管240。例如,存储串211的一端与第二串选择管241相连接,另一端与第一串选择管231相连接。

[0042] 每条第一串选择管字线250连接到属于同一个存储串组的第一串选择管230的栅极。参考图2所示,第一串选择管字线251与多个第一串选择管231的栅极相连接,与该多个第一串选择管231相连的多个存储串211属于同一个存储串组,可以称之为第一存储串组。参考图2所示,与多个第一串选择管232相连的多个存储串212属于另一个存储串组,可以称之为第二存储串组。

[0043] 参考图2所示,第一存储串组中的存储串211的另一端经过第一串选择管231与共源端220相连接。该共源端220即图1中所示的共源端12。同理,第二存储串组中的存储串212的另一端经过第一串选择管232与共源端220相连接。不同存储串组的第一串选择管231、232都与共源端220相连接。

[0044] 尽管本发明的实施例示出包括两个存储串组的器件,但是可以理解的是该实施例仅为本发明的非易失性存储器的部分结构示意图,不用于限定本发明的非易失性存储器中存储串组的数目、存储串中的存储单元的数目以及第一串选择管230、第一串选择管字线250等的数目。

[0045] 对于3D NAND类型的非易失性存储器来说,第一串选择管230位于存储串210的下方,也称为下选择管;第二串选择管240位于存储串210的上方,也称为上选择管。共源端220即3D NAND型存储器中的公共源极线CSL。

[0046] 参考图2所示,在一些实施例中,本发明的非易失性存储器还包括多条位线270,每条位线270经由第二串选择管240连接到每个存储串的一端。例如,位线271、272都经由第二

串选择管241连接到多个存储串211的一端;位线271、272都经由第二串选择管242连接到多个存储串212的一端。对于3D NAND类型的非易失性存储器来说,一条位线270在每个存储串组里连接一个存储串。

[0047] 每条第二串选择管字线260连接到属于同一个存储串组的第二串选择管240的栅极。例如,第二串选择管字线261连接到属于第一存储串组的第二串选择管241的栅极;第二串选择管字线262连接到属于第二存储串组的第二串选择管242的栅极。

[0048] 参考图2所示,在该块结构中,存储单元在三维空间内按照阵列方式排布,位于同一层内的多个存储单元组成存储行,位于不同存储串但位于同一存储行内的存储单元的栅极在物理上相连接,并且都连接至同一字线280。如图2所示,字线281、字线282和字线283分别将位于不同存储行的存储单元连接起来。

[0049] 图2及其所示的实施例不用于限定本发明的非易失性存储器中第二串选择管240、第二串选择管字线260、字线280等的数目。

[0050] 在这些实施例中,控制器14配置为在读取阶段对多条位线270施加驱动电压,并且控制器14施加到共源端220的第一预充电压大于该驱动电压。

[0051] 在对图2所示的存储器块结构中的某一存储单元进行读取操作时,需要确定选中的存储单元所在的存储串和存储行,该存储行可以通过与选中的存储单元相连接的字线来确定。例如,以图2中用圆圈圈出的存储单元201为所要进行读取操作的存储单元。存储单元201所在的存储串211为选中存储串,与存储单元201所在的选中存储行相连接的字线为字线282,称之为选中字线282。

[0052] 图3是对图2中所示的存储单元进行读取的时序图。参考图3所示,通常在对存储单元201进行读取之前,有一个预导通阶段,用来打开选中存储串和非选中存储串的沟道;在对存储单元201进行读取完成之后,有一个预关断过程。其中,在预导通阶段和预关断阶段中,所有字线(包括字线280、第一串选择管字线250和第二串选择管字线260)上所加的电压都称为预导通电压,该预导通电压可以大于或等于导通电压,从而保证沟道的导通。这样做的目的是抑制非选中存储串的热载流子注入串扰。

[0053] 具体地,结合图2和图3所示,在预导通阶段,对选中存储单元字线282和非选中存储单元字线281、283均施加预导通电压,以打开选中存储串和非选中存储串的沟道。在选中存储单元字线282和非选中存储单元字线281、283电压的上升时期,非选中存储串的第一串选择管和第二串选择管上施加的电压也跟随上升,使得非选中存储串的第一串选择管和第二串选择管均打开;对选中存储串的第一串选择管字线250和第二串选择管字线260也施加预导通电压,使选中存储串的第一串选择管和第二串选择管均打开;同时,位线和共源端都保持低电位。

[0054] 在本发明的实施例中,低电位均为0V。在其他的实施例中,低电位也可以为其他电压值。

[0055] 在读取阶段,对位线271、272施加驱动电压;对选中存储串的第一串选择管字线251和第二串选择管字线261施加导通电压,打开该存储单元201所在的选中存储串的第一串选择管231和第二串选择管241;对非选中存储串的第一串选择管字线232和第二串选择管字线242施加关断电压,关断非选中存储串的第一串选择管232和第二串选择管242,使非选中存储串的沟道与位线断开,非选中存储串的沟道电势被锁定为低电位,避免非选中存

储串的沟道被导通;对选中存储串中的选中存储单元201所在存储行以外的非选中存储单元字线281、283施加导通电压,使选中存储串的沟道导通;在选中存储单元字线282上加读取电压,即可对存储单元201内的信息进行读取。

[0056] 在读取阶段,共源端220始终处于接地状态。

[0057] 在预导通阶段,选中存储串和非选中存储串的沟道分别与其所对应的位线导通,因此,选中存储串和非选中存储串的沟道电势保持和位线相同的低电位,使选中存储串和非选中存储串的沟道不会因为字线电压的变化而耦合出电压,从而避免在对非选中存储单元的字线施加导通电压时造成热载流子注入串扰的问题。

[0058] 在读取阶段,对于位于非选中存储串上的非选中行的存储单元来说,例如图2中的存储单元202,由于这一类存储单元的沟道电势本来为低电压,在读取阶段受到非选中存储单元字线283上的导通电压的影响,沟道电势和导通电压之间具有电势差,从而引起读干扰;对于位于非选中存储串上的选中行的存储单元来说,例如图2中的存储单元203,这一类存储单元的沟道电势本来为低电压,在读取阶段受到选中存储单元字线282上的读取电压的影响,沟道电势和读取电压之间具有电势差,从而引起读干扰;对于位于选中存储串上的非选中存储单元来说,例如图2中的存储单元204,在读取阶段则会承受由于导通电压和驱动电压之间的电势差所引起的读干扰。

[0059] 上述的读干扰与引起该读干扰的电势差正相关,该电势差越大,则读干扰越强。因此,在读取阶段所施加的导通电压越大,则对存储单元造成的读干扰越大。对于上述的三种非选中存储单元202、203、204来说,位于选中存储串上的非选中存储单元204所承受的读干扰小于另外两种存储单元202、203所受到的读干扰。

[0060] 图4是读干扰所带来的存储单元阈值变化示意图。图4以多级存储单元(MLC)技术为例,存储单元可以具有四种不同的数据格式,包括00、01、10和11,则施加给存储单元的阈值电压应具有四种不同的状态,也就是四种阈值态。对应阈值电压从低到高分别用L1、L2、L3和L4表示该四种阈值态。其中L1所对应的阈值电压最低。

[0061] 参考图4所示,在对选中的存储单元进行读操作时,为了使选中的存储单元打开,所加导通电压需要大于存储单元的最大阈值。由于非选中字线上的存储单元的沟道电势本来为低电压,由于导通电压和该沟道电势产生的电压差,使非选中字线上的存储单元阈值向右移动,如图4中的虚线所示,从而产生读干扰。具有不同阈值态的存储单元的阈值向右移动的量不同,对处于L1阈值态的存储单元影响最大。

[0062] 在实际的NAND读取操作中,考虑到功耗问题,驱动电压不会太高,甚至远小于导通电压。因此,会导致非选中存储串上的非选中行的存储单元在每次读操作时都会受到沟道电势和导通电压之差所带来的读干扰。

[0063] 为了进一步的克服上述技术方案中的读干扰现象,本发明的非易失性存储器对控制器14进行了配置,通过在读写阶段之前的预导通阶段,对非易失性存储器的共源端施加第一预充电电压,或同时对位线施加第二预充电电压,增加了非选中存储串的沟道电势,减少了非选中存储单元的沟道电势和读取阶段的导通电压之间的电势差,从而降低了读干扰。具体包括两种对存储单元进行读取操作的方式,以下结合图5和图6对该两种方式进行说明。

[0064] 图5是本发明一实施例的非易失性存储器中对存储单元进行读取操作的时序图。参考图5所示,该读取操作的时序图与图3所示的时序图所不同的是,本发明的非易失性存

储器的控制器14配置为在预导通阶段中,对共源端220施加持续的第一预充电电压510。此时,选中存储串的第一串选择管和非选中存储串的第一串选择管都被打开,处于导通状态。如图5所示,可以通过在选中存储串的第一串选择管字线施加预导通电压使选中存储串的第一串选择管导通,以及在非选中存储串的第一串选择管字线施加预导通电压使非选中存储串的第一串选择管导通。

[0065] 参考图5所示,在本发明的非易失性存储器的控制器14还配置为在预导通阶段中,关断选中存储串的第二串选择管和非选中存储串的第二串选择管。参考图5所示的时序图,在预导通阶段中,控制器14可以通过给选中存储串的第二串选择管字线施加关断电压来关断选中存储串的第二串选择管,并且通过给非选中存储串的第二串选择管字线施加关断电压来关断非选中存储串的第二串选择管。并且,在预导通阶段,多条位线270保持低电位。

[0066] 在图5所示的实施例中,控制器14在预导通阶段在共源端220施加第一预充电电压510,直到预导通阶段结束,才将共源端220接地。同时,控制器14在预导通阶段在选中存储串的第一串选择管字线施加预导通电压使选中存储串的第一串选择管导通,以及在非选中存储串的第一串选择管字线施加预导通电压使非选中存储串的第一串选择管导通。并且在预导通阶段结束之前,关断非选中存储串的第一串选择管,还将施加在选中存储串的第一串选择管字线上的预导通电压变为导通电压。

[0067] 在这些实施例中,控制器14可以是同时开始对字线和共源端220施加其各自所对应的电压。

[0068] 图5所示的实施例在读取阶段和预关断阶段的时序关系和图3所示的实施例相同。

[0069] 图6是本发明另一实施例的非易失性存储器中对存储单元进行读取操作的时序图。参考图6所示,该读取操作的时序图与图5所示的时序图所不同的是,本发明的非易失性存储器的控制器14配置为在预导通阶段中,导通多个存储串中的选中存储串的第二串选择管和非选中存储串的第二串选择管,且对多条位线施加持续的第二预充电电压610。

[0070] 参考图6所示,在一些实施例中,控制器14还可以配置为在预导通阶段结束之前,关断非选中存储串的第二串选择管,且保持第二预充电电压610直至该预导通阶段结束。参考图6所示的时序图,在预导通阶段尚未结束之前,控制器14即将施加在非选中存储串的第二串选择管字线上的预导通电压关断,同时保持施加在多条位线270上的第二预充电电压610,直到预导通阶段结束,位线270上的电压才变为驱动电压。并且,控制器14在预导通阶段结束之前,还将施加在选中存储串的第二串选择管字线上的预导通电压变为导通电压。

[0071] 在这些实施例中,控制器14可以是同时开始对字线、位线270和共源端220施加其各自所对应的电压。

[0072] 在这些实施例中,控制器14施加在多条位线270上的第二预充电电压610的时间长于施加在非选中存储串的第二串选择管字线上的预导通电压的时间和施加在选中存储串的第二串选择管字线上的预导通电压的时间。

[0073] 参考图6所示,在一些实施例中,控制器14还可以配置为在预导通阶段结束之前,关断非选中存储串的第一串选择管。参考图6所示的时序图,在预导通阶段尚未结束之前,控制器14即将施加在非选中存储串的第一串选择管字线上的预导通电压关断,同时保持施加在共源端220上的第一预充电电压510,直到预导通阶段结束,共源端220才变为接地。并且,控制器14在预导通阶段结束之前,还将施加在选中存储串的第一串选择管字线上的预导通

电压变为导通电压。

[0074] 参考图6所示,在一些实施例中,控制器14同时在共源端220施加第一预充电压510和在多条位线270上施加第二预充电压610的时间,并且第一预充电压510和第二预充电压610的持续时间相同。

[0075] 参考图6所示,在一些实施例中,第二预充电压610大于驱动电压。

[0076] 参考图6所示,在一些实施例中,第一预充电压510和第二预充电压610可以不相等。

[0077] 参考图6所示,在一些实施例中,施加在共源端220的第一预充电压510和施加在多条位线270上的第二预充电压610可以相等。在这种情况下可以避免由于电压差而产生电流,可以降低存储器的功耗,并且使整个存储器中的沟道预充的比较均匀。

[0078] 参考图5-6所示,在一些实施例中,在读取阶段,施加在选中存储单元字线上的读取电压呈阶梯上升状,并且该读取电压始终小于导通电压。

[0079] 图7是本发明一实施例的非易失性存储器的操作方法的示例性流程图。与图1和图2所示的实施例类似地,这里所述的非易失性存储器包括存储单元阵列11、共源端12和多条第一串选择管字线13,该存储单元阵列11包括多个存储串组,每个存储串组包括多个存储串;该共源端12经由第一串选择管15连接到每个存储串的另一端;该多条第一串选择管字线13的每条第一串选择管字线连接到对应的存储串组的第一串选择管15的栅极。在本说明书中关于图1-6所示的实施例的说明内容都适用于图7所示的实施例中的非易失性存储器。

[0080] 参考图7所示,该操作方法包括:

[0081] 步骤710,在读取阶段之前的预导通阶段中,导通多个存储串中的选中存储串的第一串选择管和非选中存储串的第一串选择管,且对共源端施加持续的第一预充电压。

[0082] 参考图5-6所示,在预导通阶段中,可以通过在选中存储串的第一串选择管字线施加预导通电压使选中存储串的第一串选择管导通,以及在非选中存储串的第一串选择管字线施加预导通电压使非选中存储串的第一串选择管导通。可以通过控制器14对共源端220施加持续的第一预充电压510。

[0083] 在一些实施例中,在预导通阶段结束之前,还包括关断非选中存储串的第一串选择管,且保持第一预充电压510直至预导通阶段结束。参考图5-6所示,在预导通阶段尚未结束之前,控制器14即将施加在非选中存储串的第一串选择管字线上的预导通电压关断,同时保持施加在共源端220上的第一预充电压510,直到预导通阶段结束,共源端220才变为接地。并且,控制器14在预导通阶段结束之前,还将施加在选中存储串的第一串选择管字线上的预导通电压变为导通电压。也就是说,在这些实施例中,控制器14施加在共源端220的第一预充电压510的时间长于施加在非选中存储串的第一串选择管字线上的预导通电压的时间和施加在选中存储串的第一串选择管字线上的预导通电压的时间。

[0084] 在一些实施例中,本发明操作方法中所用到的非易失性存储器还包括多条位线和多条第二串选择管字线,每条位线经由第二串选择管连接到每个存储串的一端,每条第二串选择管字线连接到对应的存储串组的第一串选择管的栅极。与图1和图2所示的实施例类似地,相关的说明书内容都适用于这些实施例中的非易失性存储器。

[0085] 在这些实施例中,对该非易失性存储器的操作方法还可以包括:

[0086] 步骤720,在读取阶段对多条位线施加驱动电压。并且,对共源端220施加的持续的

第一预充电电压510大于该驱动电压。

[0087] 进一步地,本发明的非易失性存储器的操作方法还可以包括以下的步骤:

[0088] 步骤730,在预导通阶段中,导通选中存储串的存储单元和非选中存储串的存储单元的沟道。

[0089] 参考图5-6所示,在这些实施例中,可以通过给选中存储串的存储单元字线和非选中存储串的存储单元字线施加预导通电压来使选中存储串的存储单元和非选中存储串的存储单元的沟道导通。并且,在预导通阶段中,该预导通电压持续的施加在选中存储串的存储单元字线和非选中存储串的存储单元字线,直到预导通阶段结束。当读取阶段开始时,非选中存储单元字线上施加的电压变为导通电压,选中存储单元字线上施加的电压变为读取电压。

[0090] 步骤740,在预导通阶段中,关断选中存储串的第二串选择管和非选中存储串的第二串选择管。

[0091] 参考图5所示,在这些实施例中,可以通过给选中存储串的第二串选择管字线施加关断电压来关断选中存储串的第二串选择管,并且通过给非选中存储串的第二串选择管字线施加关断电压来关断非选中存储串的第二串选择管。并且,在预导通阶段,多条位线270保持低电位。

[0092] 步骤750,在预导通阶段中,导通多个存储串中的选中存储串的第二串选择管和非选中存储串的第二串选择管,且对多条位线施加持续的第二预充电电压。

[0093] 参考图6所示,在这些实施例中,可以通过给选中存储串的第二串选择管字线施加预导通电压来导通选中存储串的第二串选择管,并且通过给非选中存储串的第二串选择管字线施加预导通电压来导通非选中存储串的第二串选择管。可以通过控制器14对多条位线270施加持续的第二预充电电压610。

[0094] 在一些实施例中,本发明的非易失性存储器的操作方法还包括在预导通阶段结束之前,关断非选中存储串的第二串选择管,且保持第二预充电电压直至预导通阶段结束。

[0095] 参考图6所示,在这些实施例中,在预导通阶段结束之前,控制器14即将施加在非选中存储串的第二串选择管字线上的预导通电压关断,同时保持施加在多条位线270上的第二预充电电压610,直到预导通阶段结束,位线270上的电压才变为驱动电压。并且,控制器14在预导通阶段结束之前,还将施加在选中存储串的第二串选择管字线上的预导通电压变为导通电压。

[0096] 在这些实施例中,控制器14施加在多条位线270上的第二预充电电压610的时间长于施加在非选中存储串的第二串选择管字线上的预导通电压的时间和施加在选中存储串的第二串选择管字线上的预导通电压的时间。

[0097] 在本发明的非易失性存储器的操作方法的一些实施例中,第二预充电电压610大于驱动电压。

[0098] 在本发明的非易失性存储器的操作方法的一些实施例中,第一预充电电压510和第二预充电电压610可以不相等。

[0099] 在本发明的非易失性存储器的操作方法的一些实施例中,施加在共源端220的第一预充电电压510和施加在多条位线270上的第二预充电电压610可以相等。在这种情况下可以避免由于电压差而产生电流,可以降低存储器的功耗,并且使整个存储器中的沟道预充的

比较均匀。

[0100] 在本发明的非易失性存储器的操作方法的实施例中,在预导通阶段所施加的预导通电压均大于或等于在读取阶段所施加的导通电压。在一些实施例中,控制器14可以是同时开始对字线、位线270和共源端220施加其各自所对应的电压。

[0101] 图7使用了流程图用来说明根据本发明实施例的操作方法所执行的操作。应当理解的是,前面的操作不一定按照顺序来精确地执行。相反,可以按照倒序或同时处理各种步骤。同时,或将其他操作添加到这些过程中,或从这些过程移除某一步或数步操作。

[0102] 虽然本发明已参照当前的具体实施例来描述,但是本技术领域中的普通技术人员应当认识到,以上的实施例仅是用来说明本发明,在没有脱离本发明精神的情况下还可做出各种等效的变化或替换,因此,只要在本发明的实质精神范围内对上述实施例的变化、变型都将落在本申请的权利要求书的范围内。

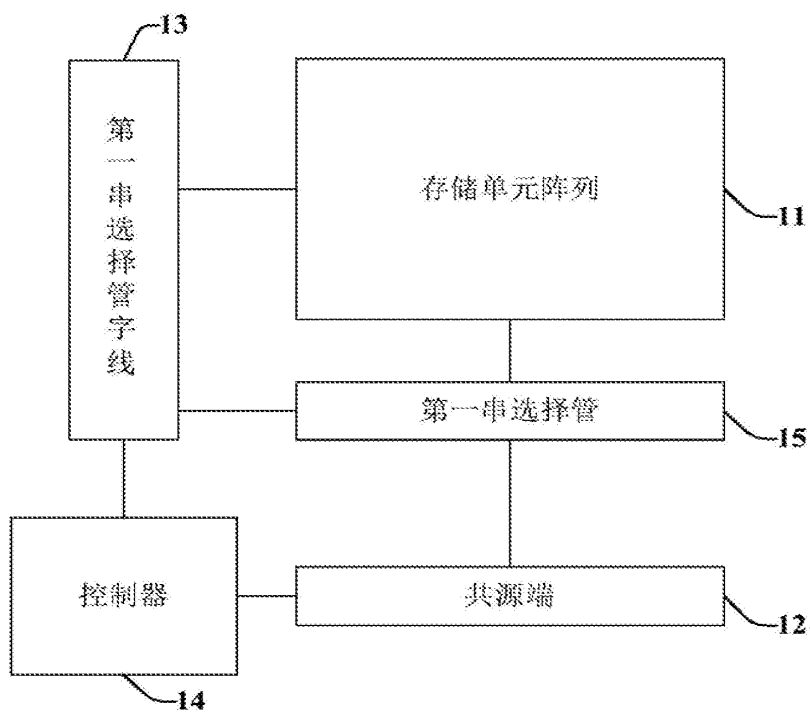


图1

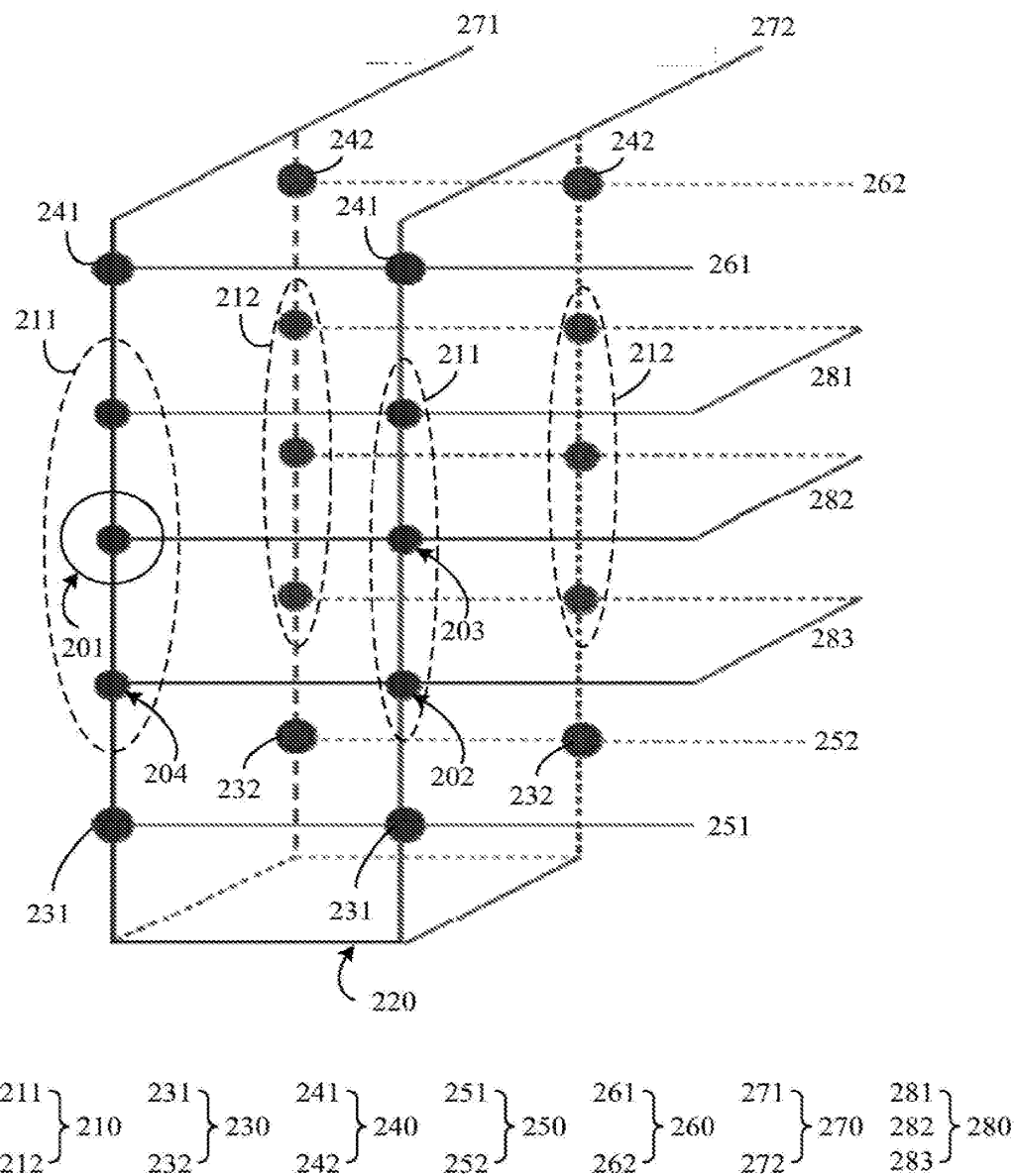


图2

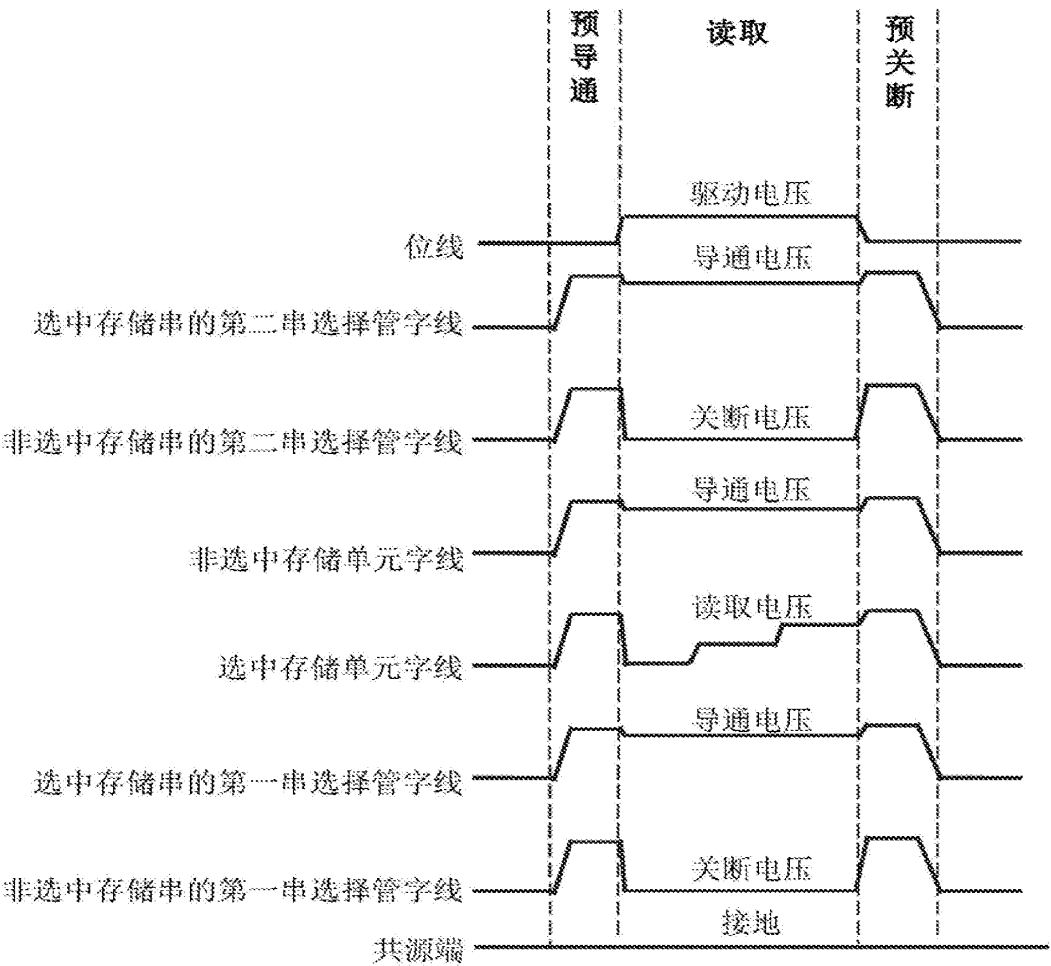


图3

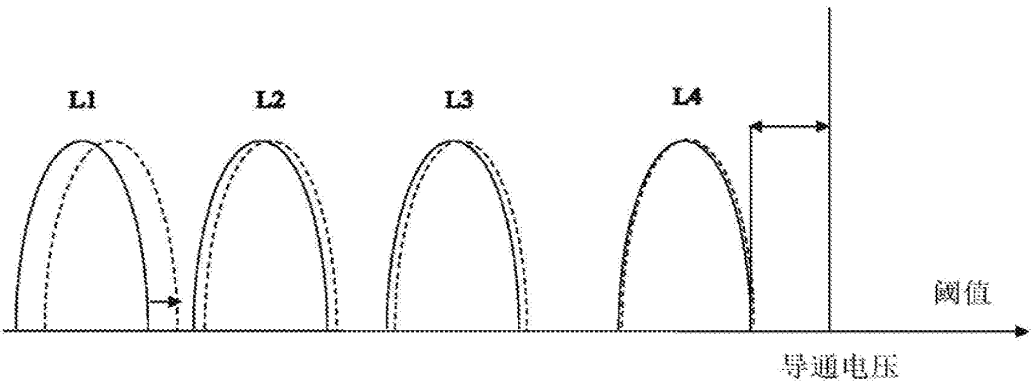


图4

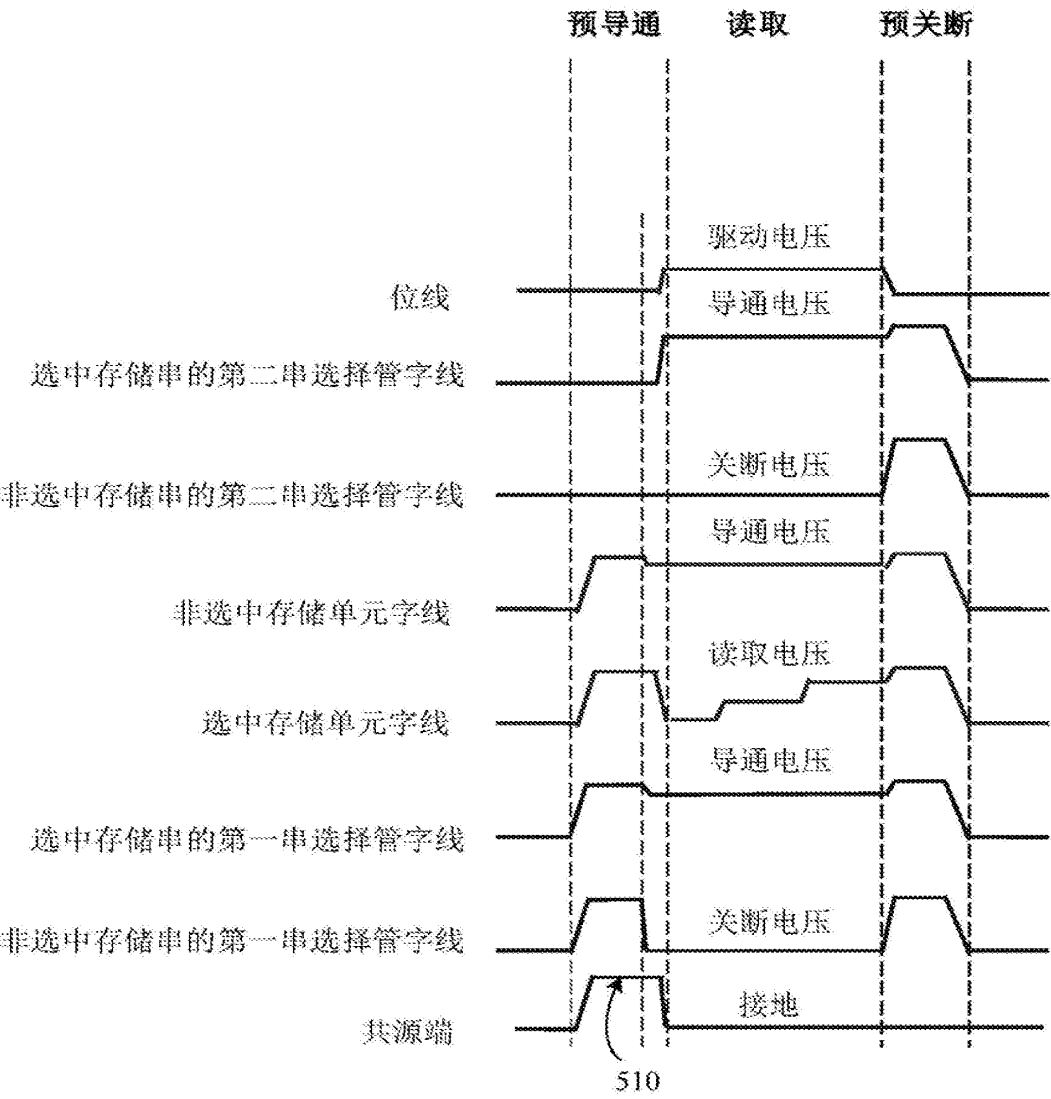


图5

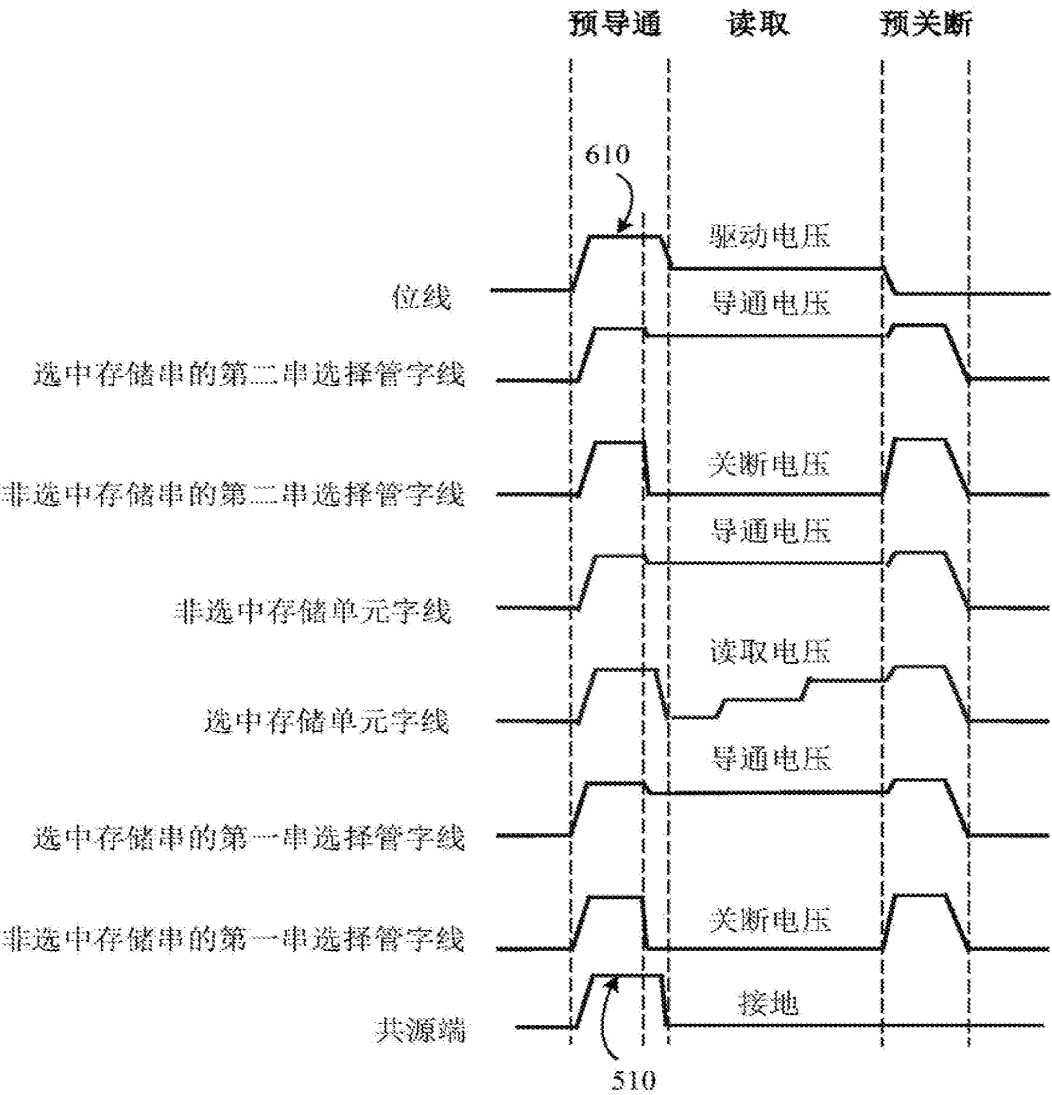


图6

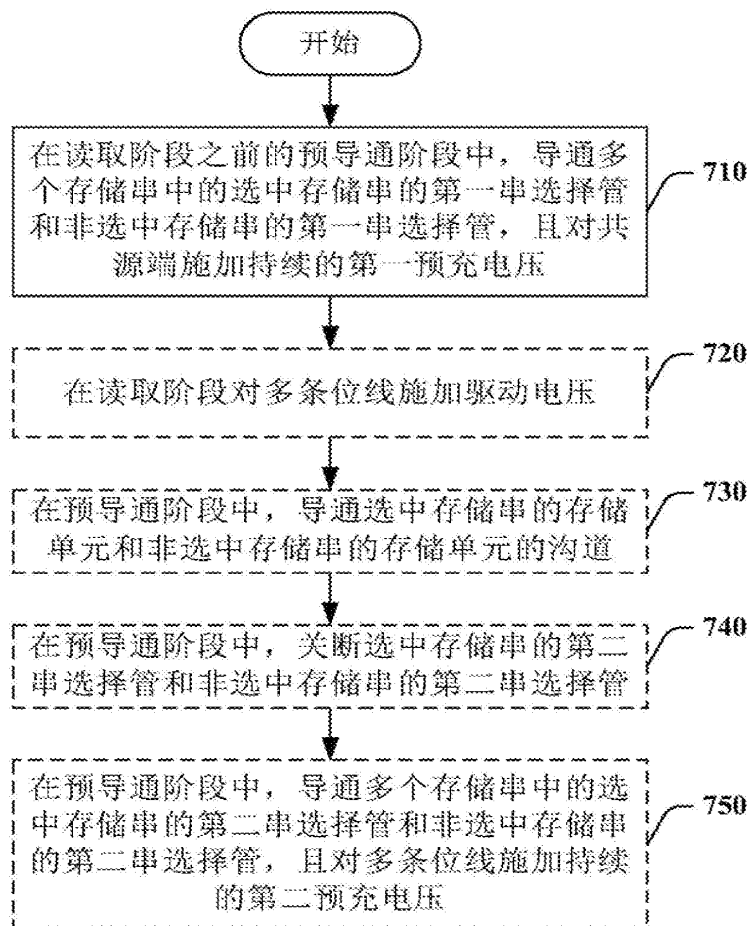


图7

Electronic Acknowledgement Receipt	
EFS ID:	40990846
Application Number:	16709944
International Application Number:	
Confirmation Number:	7658
Title of Invention:	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD
First Named Inventor/Applicant Name:	Jianquan Jia
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Edie Hung
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0261USA3
Receipt Date:	02-NOV-2020
Filing Date:	11-DEC-2019
Time Stamp:	03:41:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	4005907.PDF	26445	no	3
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2	Foreign Reference	CHN_110289034.pdf	3614692	no	20
			5c7dc8ff9b7f34203905c904e277af54cdedf58d		
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/709,944	12/11/2019	Jianquan Jia	YMTP0261USA3	7658
27765	7590	01/15/2021	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION 5F., NO.389, FUHE RD., YONGHE DIST. NEW TAIPEI CITY, TAIWAN			NGUYEN, VIET Q	
			ART UNIT	PAPER NUMBER
			2827	
			NOTIFICATION DATE	DELIVERY MODE
			01/15/2021	ELECTRONIC

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DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

1. Claims **1-20** are present for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

2. Claims **1-2, 6, 10-12, 16 & 20** are rejected under 35 U.S.C. 102(a)(2) as being anticipated by **Chen et al (US 10,770,157)**.

Claims 1 & 11, **Chen et al (see Figs. 1 & 7)** shows a memory device comprising a plurality of NAND strings SB0-SB7, each string has consecutive word lines WL0-WL95, with at least a select gate transistor (see either SGD/716 or SGS/701 at both end of each string). Fig. 13A-13C shows a method for precharging & programming a particular cell string with precharging phase (step 1301) first following by a programming phase (see steps 1302-1304) later, and particularly Fig. 13C show that during any precharge period/phase, the bit line of that string will be applied with the bit line pre-

pulse signals to both unselected & selected bit lines (i.e., see $V_{bl_unsel}=2V$ & $V_{bl_sel}=0V$) during mini-steps 1321-1322, then following by applying other word line pre-pulse signals (i.e., see $V_{pch_ds}=1$ to $2V$, $V_{pch_n}=1$ to $2V$ & $V_{pch_ss}=0$ to $2V$, etc.) during mini-steps 1323-1325 as well.

It is further noted that Fig. 11A-12A shows that such plurality of word lines siting between a selected word line W_{ln} , with a pre-charge (or pre-pulse signal = $2V$) is applied to selected word line W_{ln} , while other different precharge/pre-pulse signals (from $0V$ to $2V$) are also applied to a plurality of other word lines coupled to other cells on same string and these cells are disposed in between the selected gate line and the selected word line W_{ln} during this precharge period/step, wherein these pre-pulse/pre-charge signals are also capable of increasing or incremental pulse steps if desired. For example, Fig. 12A shows the pulses 1230 ($=0V$) increased to pulses 1231 ($=2V$), while these word lines (from W_{l0} to W_{ln-1}) are also sit in between the selected word line W_{ln} and at least one of the selected gate (see the select gate line SGS next to the W_{l0} line as shown in Fig. 7 as one example) as claimed.

Claims 2 & 12, Fig. 10A-12A show that during the precharge period, a plurality of groups of adjacent word lines (see group 1230, 1231, 1232, and 1031 in Fig. 12A as example) are further divided into groups with separate pre-pulse signals from 1st pre-pulse level to the 3rd pre-pulse level (i.e., see $0V$ level applied to 1st WL group 1230, then $2V$ applied to 2nd WL group 1231, then $0V$ to 3rd WL group 1232, and so on in Fig. 12A as example). Thus, any other possible divided WL group/configuration could have been possibly carried out as well without complexity.

Claims 6 & 16, Fig. 7 shows the use of at least one dummy word line with its corresponding pre-pulse signal applied to its gate line (WLDD or WLDS) as well-known in this art.

Claims 10 & 20, Fig. 7 shows that any string can be selected by the user for programming/precharging as the “selected bit line”, while other strings remained unselected (or floated) as “unselected bit line” as this is also well-known to one skilled in this art of NAND cell programming technique.

3. Claims **1-2, 6, 10-12, 16 & 20** are rejected under 35 U.S.C. 102(a)(2) as being anticipated by **Chen et al (US 10,283,202)**.

Claims 1 & 11, **Chen et al (see Figs. 1 & 7)** shows a memory device comprising a plurality of NAND strings SB0-SB3, each string has consecutive word lines WL0-WL31, with at least a select gate transistor (see either SGD/718 or SGS/702 at both end of each string). Fig. 10A shows a method for precharging & programming a particular cell string with precharging phase (step 1003) first, then following by a programming phase (steps 1004-1107) later, and particularly step (1003a) showing that two different initial voltage levels (or two different pre-pulse signals) can be applied to two to three adjacent word line groups as claimed. For example, Fig. 1B shows that one 1st group of word lines WL can be applied with V2 pulse level, while a second WL group can be applied with another but higher pre-pulse signals V3 as claimed.

It is further noted that Fig. 10B show that these WL groups are adjacent to each other and sit between the selected word line and any selected gate and designated as lower tier or upper tier as relative to the selected word line as well.

Fig. 11A-12A shows that such plurality of word lines siting between a selected word line W_{ln} , with a pre-charge (or pre-pulse signal= 2V) is applied to selected word line W_{ln} , while other different precharge/pre-pulse signals (from 0V to 2V) are also applied to a plurality of other word lines coupled to other cells on same string and these cells are disposed in between the selected gate line and the selected word line W_{ln} during this precharge period/step, wherein these pre-pulse/pre-charge signals are also capable of increasing or incremental pulse steps if desired. For example, Fig. 12A shows the pulses 1230 (=0V) increased to pulses 1231 (=2V), while these word lines (from W_{l0} to W_{ln-1}) are also sit in between the selected word line W_{ln} and at least one of the selected gate (see the select gate line SGS next to the W_{l0} line as shown in Fig. 7 as one example) as claimed.

Claims 2 & 12, Fig. 10B show that during the precharge period, a plurality of groups of adjacent word lines (see 1st group) are applied pre-pulse signals from 1st pre-pulse level V1 to V2 depending on tier locations, and next WL group (2nd & 3rd) are applied with a higher pre-pulse signals at higher levels V3 as claimed. Thus, any other possible divided WL group/configuration could have been possibly carried out as well without complexity.

Claims 6 & 16, Fig. 7 shows the use of at least one dummy word line with its corresponding pre-pulse signal applied to its gate line (WLDD or WLDS) as well-known in this art.

Claims 10 & 20, Fig. 7 shows that any string can be selected by the user for programming/precharging as the "selected bit line", while other strings remained

unselected (or floated) as “unselected bit line” as this is also well-known to one skilled in this art of NAND cell programming technique.

4. Claims **1-2, 10-12, & 20** are rejected under 35 U.S.C. 102(a)(2) as being anticipated by **KIM et al (US 2011/0194351)**.

Claims 1 & 11, **KIM et al (see Figs. 1-2)** shows a memory device comprising a plurality of NAND strings BL0 & BL1, each string has consecutive word lines WL0-WL31, with at least a select gate transistor (see either SSL or GSL lines at both end of each bit/string). Fig. 10 shows a method for precharging & programming a particular cell string with precharging phase (steps 302-304) first on two adjacent groups of WL (as upper & lower channel groups), then following by a programming phase (step 306) later, and particularly Fig. 11 show different pre-pulse signals are applied to different group of adjacent WL in incremental pulse step from 0V to V2 to V3 levels as well.

It is further noted that Fig. 11 shows that such plurality of word lines siting between a selected word line WL26, with a pre-charge (or pre-pulse signal= 0V to 2V) is applied to selected word line WL26, while other different precharge/pre-pulse signals have their incremental values (from 0V to V2 levels, or from 0V to V3 levels) are also applied to a plurality of other adjacent groups of word lines (i.e., V3 to WL group WL 27) and V2 to group WL28-WL31 as example), etc. Similarly for the lower channel groups (WL0 to WL24 below selected WL26, another pre-pulse levels V2 or V5 are applied as claimed. Thus, many other pre-pulse signal levels could have been similarly applied to other WL divided/configurations as well without complexity as claimed. See also Figs. 12-13 for other WL group configurations.

Claims 2 & 12, Fig. 11-13 show that during the precharge period, a plurality of groups of adjacent word lines are further applied with separate pre-pulse signals from 1st pre-pulse level to the 3rd pre-pulse level (i.e., see 0V level to V3 or V5 levels as example), and so on. Thus, any other possible divided WL group/configuration could have been possibly carried out as well without complexity.

Claims 10 & 20, Fig. 1-2 shows that any string can be selected by system for programming/precharging as the “selected bit line”, while other strings remained unselected (or floated) as “unselected bit line” as this is also well-known to one skilled in this art of NAND cell programming technique.

5. Other claims not mentioned are objected as being dependent upon the rejected claims above but tentatively contain allowable subject matter for other recited features not clearly suggested or seen elsewhere at this time.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIET Q NGUYEN whose telephone number is (571)272-1788. The examiner can normally be reached on M-F 7:30-3PM EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VIET Q NGUYEN/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 16/709,944		Applicant(s)/Patent Under Reexamination Jia et al.	
	Examiner VIET Q NGUYEN		Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20200353312-A1	11-2020	Smith; Cameron	A63B24/0075	1/1
*	B	US-9460805-B1	10-2016	Pang; Liang	G11C16/10	1/1
*	C	US-10283202-B1	05-2019	Chen; Hong-Yan	G11C16/08	1/1
*	D	US-10770157-B1	09-2020	Chen; Hong-Yan	G11C16/32	1/1
*	E	US-20110194351-A1	08-2011	KIM; Jin-Ki	G11C16/0483	365/185.17
	F					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)

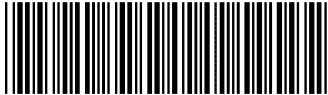
Notice of References Cited

Part of Paper No. 20210111

<i>Index of Claims</i> 	Application/Control No. 16/709,944	Applicant(s)/Patent Under Reexamination Jia et al.
	Examiner VIET Q NGUYEN	Art Unit 2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	01/12/2021								
	1	✓								
	2	✓								
	3	○								
	4	○								
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	17	○								
	18	○								
	19	○								
	20	✓								

<i>Search Notes</i> 	Application/Control No. 16/709,944	Applicant(s)/Patent Under Reexamination Jia et al.
	Examiner VIET Q NGUYEN	Art Unit 2827

CPC - Searched*		
Symbol	Date	Examiner
G11C 11/4085, 11/4074, 11/4094, 11/4099, 11/419	8/24/2020	vn

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	230.06, 185.18, 185.24	8/24/20	vn

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
G11C 11/4085, 11/4074, 11/4094, 11/4099, 11/419	8/24/2020	vn
EAST	01/12/2021	vn
Updated IDS	01/12/2021	vn

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G11C	11/4085, 11/4074, 11/4094, 11/4099, 11/419	01/12/2021	vn

/VIET Q NGUYEN/ Primary Examiner, Art Unit 2827	
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EAST Search History

EAST Search History (Prior Art)

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L1	8,655	(precharg\$4 or pre-charge\$4) near5 (wordline\$1 or word-line\$1 or (word adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:37
L2	29,527	(precharg\$4 or pre-charge\$4) near5 (bitline\$1 or bit-line\$1 or (bit adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:38
L3	34,383	"SGL" or (select adj1 gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:38
L4	44	1 with 2 with 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:39
L5	7,725	365/203.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:07
L6	51,869	3(G11C11/4085 or G11C11/4099 or G11C11/4074 or G11C11/419 or G11C11/4094).cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:11
L7	44	(5 or 6) and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:11
L8	44	(5 or 6) and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 10:20
L9	12,180	(precharg\$4 or pre-charge\$4) near9 (wordline\$1 or word-line\$1 or (word adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L10	31,140	(precharg\$4 or pre-charge\$4) near9 (bitline\$1 or bit-line\$1 or (bit adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L11	60,418	"SGL" or (select adj1 gate) or (select adj1 transistor\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L12	1,994	9 and 10 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:24
L13	1,102	9 and 10 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:24

L14	914	(program-disturb\$1 or (program\$4 near2 disturb\$1)) and (channel near3 length)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:26
L15	612	11 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:26
L16	7,590	dummy near3 (wordline\$1 or word-line\$1 or (word adj line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:27
L17	180	15 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:27

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L3	2	("10283202" "20190147955").PN.	US-PGPUB; USPAT	OR	ON	2021/01/12 12:53

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L3	2	"20200035312"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 08:53
L4	1	"20200035312" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 08:57
L5	5	"10283202" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 08:58
L6	12	"9460805" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:04
L7	2	"10636487" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:14
L8	1	"10685723" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:15
L9	2	"20200168276" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:17
L10	1	"20200152282" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:39
L11	2	"20190371406" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:41
L12	2	"10373697" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:43
L13	2	"20190355429" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:44
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L16	1	"20180233206" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:57
L17	22	"9412463" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:57
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L28	1	"10593411" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:11
L29	2	"10217518" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:11
L30	8	"9887002" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:13
L31	13	"9460805" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:15
L32	1	"20200035312" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:21
L34	5	"10283202" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:23
L35	13	"9460805" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:25

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EAST Search History**EAST Search History (Prior Art)**

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L3	62	((("YANGTZE") near3 ("MEMORY") near3 ("TECHNOLOGIES") near3 ("CO") near3 ("LTD"))).AS,AANM.	USPAT	OR	ON	2020/08/24 19:10
L4	82	((("JIA") near3 ("Jianquan")) OR (("CUI") near3 ("Ying")) OR (("YOU") near3 ("Kaikai"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:10
L8	11,841	365/230.06	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:37
L11	0	365/203.ccls	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39
L12	7,725	365/203.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39
L14	3	(1 or 12) and (pre-charg\$4 near5 pre-pulse\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39
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L6	62	((("YANGTZE") near3 ("MEMORY") near3 ("TECHNOLOGIES") near3 ("CO") near3 ("LTD"))).AS,AANM.	USPAT	OR	ON	2020/08/24 19:12
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L9	0	(2 or 7) and 5 and 6	USPAT	OR	ON	2020/08/24 19:38
L10	0	(2 or 7) and 5 and (pre-charge\$4 near5 pre-pulse\$1)	USPAT	OR	ON	2020/08/24 19:38
L13	5	("1" or "12") and (pre-charge\$4 near5 pre-pulse\$1)	USPAT	OR	ON	2020/08/24 19:39

8/24/2020 7:47:11 PM

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EAST Search History (Prior Art)

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L11	0	365/203.ccls	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39
L12	7,725	365/203.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39
L14	3	(1 or 12) and (pre-charg\$4 near5 pre-pulse\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39

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L10	0	(2 or 7) and 5 and (pre-charge\$4 near5 pre-pulse\$1)	USPAT	OR	ON	2020/08/24 19:38
L13	5	("1" or "12") and (pre-charge\$4 near5 pre-pulse\$1)	USPAT	OR	ON	2020/08/24 19:39

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17,737	(G11C11/4085 or G11C11/4099 or G11C11/4074 or G11C11/419 or G11C11/4094).cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:10
L3	62	((("YANGTZE") near3 ("MEMORY") near3 ("TECHNOLOGIES") near3 ("CO") near3 ("LTD"))).AS,AANM.	USPAT	OR	ON	2020/08/24 19:10
L4	82	((("JIA") near3 ("Jianquan")) OR (("CUI") near3 ("Ying")) OR (("YOU") near3 ("Kaikai"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:10
L8	11,841	365/230.06	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:37
L11	0	365/203.ccls	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39
L12	7,725	365/203.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39
L14	3	(1 or 12) and (pre-charg\$4 near5 pre-pulse\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:39
L15	2,450	(1 or 12) and (pre-charg\$4 near8 (bitline\$1 or (bit-line\$1) or (bit adj1 line\$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:43
L16	98	(1 or 12) and (pre-charg\$4 near8 (increas\$4 or increment\$3) near8 (bitline\$1 or (bit-line\$1) or (bit adj1 line\$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/24 19:45

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	6,090	(G11C11/4085 or G11C11/4099 or G11C11/4074 or G11C11/419 or G11C11/4094).cpc.	USPAT	OR	ON	2020/08/24 19:10
L5	30	((("JIA") near3 ("Jianquan")) OR (("CUI") near3 ("Ying")) OR (("YOU") near3 ("Kaikai"))).INV.	USPAT	OR	ON	2020/08/24 19:12

L6	62	((("YANGTZE") near3 ("MEMORY") near3 ("TECHNOLOGIES") near3 ("CO") near3 ("LTD"))).AS,AANM.	USPAT	OR	ON	2020/08/24 19:12
L7	10,482	365/230.06	USPAT	OR	ON	2020/08/24 19:37
L9	0	(2 or 7) and 5 and 6	USPAT	OR	ON	2020/08/24 19:38
L10	0	(2 or 7) and 5 and (pre-charge\$4 near5 pre-pulse\$1)	USPAT	OR	ON	2020/08/24 19:38
L13	5	("1" or "12") and (pre-charge\$4 near5 pre-pulse\$1)	USPAT	OR	ON	2020/08/24 19:39

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8,655	(precharg\$4 or pre-charge\$4) near5 (wordline\$1 or word-line\$1 or (word adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:37
L2	29,527	(precharg\$4 or pre-charge\$4) near5 (bitline\$1 or bit-line\$1 or (bit adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:38
L3	34,383	"SGL" or (select adj1 gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:38
L4	44	1 with 2 with 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:39
L5	7,725	365/203.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:07
L6	51,869	3(G11C11/4085 or G11C11/4099 or G11C11/4074 or G11C11/419 or G11C11/4094).cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:11
L7	44	(5 or 6) and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:11
L8	44	(5 or 6) and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 10:20
L9	12,180	(precharg\$4 or pre-charge\$4) near9 (wordline\$1 or word-line\$1 or (word adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L10	31,140	(precharg\$4 or pre-charge\$4) near9 (bitline\$1 or bit-line\$1 or (bit adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L11	60,418	"SGL" or (select adj1 gate) or (select adj1 transistor\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L12	1,994	9 and 10 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:24
L13	1,102	9 and 10 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:24

L14	914	(program-disturb\$1 or (program\$4 near2 disturb\$1)) and (channel near3 length)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:26
L15	612	11 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:26
L16	7,590	dummy near3 (wordline\$1 or word-line\$1 or (word adj line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:27
L17	180	15 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:27

EAST Search History (Interference)

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8/26/2020 12:17:48 PM

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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8,655	(precharg\$4 or pre-charge\$4) near5 (wordline\$1 or word-line\$1 or (word adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:37
L2	29,527	(precharg\$4 or pre-charge\$4) near5 (bitline\$1 or bit-line\$1 or (bit adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:38
L3	34,383	"SGL" or (select adj1 gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:38
L4	44	1 with 2 with 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 08:39
L5	7,725	365/203.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:07
L6	51,869	3(G11C11/4085 or G11C11/4099 or G11C11/4074 or G11C11/419 or G11C11/4094).cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:11
L7	44	(5 or 6) and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 09:11
L8	44	(5 or 6) and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 10:20
L9	12,180	(precharg\$4 or pre-charge\$4) near9 (wordline\$1 or word-line\$1 or (word adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L10	31,140	(precharg\$4 or pre-charge\$4) near9 (bitline\$1 or bit-line\$1 or (bit adj1 line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L11	60,418	"SGL" or (select adj1 gate) or (select adj1 transistor\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:23
L12	1,994	9 and 10 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:24
L13	1,102	9 and 10 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:24

L14	914	(program-disturb\$1 or (program\$4 near2 disturb\$1)) and (channel near3 length)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:26
L15	612	11 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:26
L16	7,590	dummy near3 (wordline\$1 or word-line\$1 or (word adj line\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:27
L17	180	15 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2020/08/26 11:27

EAST Search History (Interference)

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8/26/2020 12:18:03 PM

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16709944
	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

U.S.PATENTS								
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	10283202	B1	2019-05-07	Chen			

U.S.PATENT APPLICATION PUBLICATIONS								
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	20190147955	A1	2019-05-16	Chen			

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	110289034	CN	A	2019-09-27			Abstract

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.Q.N/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16709944
	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

	1		
EXAMINER SIGNATURE			
Examiner Signature	/VIET Q NGUYEN/	Date Considered	01/12/2021
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.Q.N/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16709944
	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2020-10-29
Name/Print	Winston Hsu	Registration Number	41526

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16709944
	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

U.S.PATENTS								
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1							
U.S.PATENT APPLICATION PUBLICATIONS								
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	20110194351	A1	2011-08-11	KIM			
	2	20190108883	A1	2019-04-11	Yu			
	3	20190156901	A1	2019-05-23	Chen			
FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1							

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.Q.N/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16709944
	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		
EXAMINER SIGNATURE			
Examiner Signature	/VIET Q NGUYEN/		Date Considered 01/12/2021
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.Q.N/

Micron Ex. 1015, p. 110
Micron v. YMTC
IPR2024-00795

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16709944
	Filing Date	2019-12-11
	First Named Inventor	Jianquan Jia
	Art Unit	2827
	Examiner Name	NGUYEN, VIET Q
	Attorney Docket Number	YMTP0261USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2020-08-25
Name/Print	Roger Chen	Registration Number	67314

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	"20200035312" and "pre-pulse"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 08:53
L2	0	"20200035312" and "pre-pulse1"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 08:53
L3	2	"20200035312"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 08:53
L4	1	"20200035312" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 08:57
L5	5	"10283202" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 08:58
L6	12	"9460805" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:04
L7	2	"10636487" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:14
L8	1	"10685723" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:15
L9	2	"20200168276" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:17
L10	1	"20200152282" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:39
L11	2	"20190371406" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:41
L12	2	"10373697" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:43
L13	2	"20190355429" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:44
L15	1	"10269435" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:55
L16	1	"20180233206" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:57
L17	22	"9412463" and increment\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:57
L18	3	"9412463".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 09:58
L19	2	"9286994".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:01
L20	2	"20130250690".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:02

L21	2	"20130250690" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:05
L22	2	"20130250688" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:05
L23	1	"10748627" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:06
L24	1	"10748619" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:08
L25	0	"10635501" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:09
L26	2	"10635501".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:09
L27	1	"10636501" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:10
L28	1	"10593411" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:11
L29	2	"10217518" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:11
L30	8	"9887002" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:13
L31	13	"9460805" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:15
L32	1	"20200035312" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:21
L34	5	"10283202" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:23
L35	13	"9460805" and (pre-charge or precharge)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/01/12 10:25

EAST Search History (Interference)

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1/12/2021 10:51:06 AM

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NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD

Appl. No. : 16/709,944 Confirmation No. 7658
First Named Inventor : Jianquan Jia
Filed : December 11, 2019
TC/A.U. : 2827
Examiner : NGUYEN, VIET Q
Docket No. : YMTP0261USA3
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of January 15, 2021, please amend the above-identified application as follows:

- 5 **Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 5 1. (currently amended): A non-volatile memory device, comprising:
- a memory array comprising a plurality of memory strings, each memory string comprising a select gate transistor and a plurality of memory cells connected in series with the select gate transistor;
 - a bit line connected to a first memory string of the plurality of memory strings;
 - 10 a select gate line connected to the select gate transistor of the first memory string of the plurality of memory strings;
 - a plurality of word lines connected to the plurality of memory cells of the first memory string of the plurality of memory strings, each word line connected to a respective memory cell of the first memory string;
 - 15 a first control circuit configured to apply a bit line pre-pulse signal to the bit line during a pre-charge period; and
 - a second control circuit configured to apply a word line signal to a selected word line of the plurality of word lines and apply a plurality of word line pre-pulse signals to word lines disposed between the select gate line and the selected word line during the pre-charge period, wherein voltage levels of the plurality of word line pre-pulse signals are incremental;
 - 20 wherein the second control circuit is configured to apply a first word line pre-pulse signal of the plurality of word line pre-pulse signal to a first group of the plurality of word lines disposed adjacent to the selected word line and disposed between the selected word line and the select gate line during the pre-charge period, apply a second word line pre-pulse signal of the plurality of word line pre-pulse signal to a second group of the plurality of word lines disposed adjacent to the first group of the plurality of word lines and disposed between the first group of the plurality of word line and the select gate line during the pre-charge period, and apply a third word line pre-pulse
 - 25 signal of the plurality of word line pre-pulse signal to a third group of the plurality of word lines disposed adjacent to the second group of the plurality of word lines and disposed between the second group of the plurality of word line and the select gate line during the pre-charge period, and apply a fourth word line pre-pulse signal of the plurality of word line pre-pulse signal to a fourth group of the plurality of word lines disposed adjacent to the third group of the plurality of word lines and disposed between the third group of the plurality of word line and the select gate line during the pre-charge period, and
 - 30 apply a fifth word line pre-pulse signal of the plurality of word line pre-pulse signal to a fifth group of the plurality of word lines disposed adjacent to the fourth group of the plurality of word lines and disposed between the fourth group of the plurality of word line and the select gate line during the pre-charge period, and

5 signal of the plurality of word line pre-pulse signal to a third second group of the plurality of word lines disposed adjacent to the second group of the plurality of word lines and between the second group of the plurality of word lines and the select gate line during the pre-charge period, wherein a voltage level of the second word line pre-pulse signal is greater than a voltage level of the first word line pre-pulse signal and a voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal.

10 2-3. (cancelled)

4. (currently amended): The non-volatile memory device of claim [[2]]1, wherein an ending of the second word line pre-pulse signal is after an ending of the first word line pre-pulse signal and an ending of the third word line pre-pulse signal is after
15 the ending of the second word line pre-pulse signal.

5. (currently amended): The non-volatile memory device of claim [[2]]1, wherein a pulse duration of the second word line pre-pulse signal is greater than a pulse duration of the first word line pre-pulse signal and a pulse duration of the third
20 word line pre-pulse signal is greater than the pulse duration of the second word line pre-pulse signal.

6. (original): The non-volatile memory device of claim 1, wherein the memory array further comprises at least one dummy memory cell, the at least one dummy
25 memory cell is disposed between the select gate transistor and the plurality of memory cells and connected in series with the select gate transistor and the plurality of memory cells, and the non-volatile memory device further comprises at least one dummy word line and each dummy word line is connected to a respective dummy memory cell, wherein the second control circuit is configured
30 to apply a dummy word line pre-pulse signal to the at least one dummy word line.

7. (original): The non-volatile memory device of claim 6, wherein a voltage level of the dummy word line pre-pulse signal is greater than voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
8. (original): The non-volatile memory device of claim 6, wherein an ending of the dummy word line pre-pulse signal is after endings of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
9. (original): The non-volatile memory device of claim 6, wherein a pulse duration of the dummy word line pre-pulse signal is greater than pulse durations of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
10. (original): The non-volatile memory device of claim 1, wherein the first string of the plurality of memory strings is an unselected string and the bit line is an unselected bit line during the pre-charge period.
11. (currently amended): A control method of non-volatile memory device, the non-volatile memory device comprising a memory array comprising a plurality of memory strings, each memory string comprising a select gate transistor and a plurality of memory cells connected in series with the select gate transistor, the control method comprising:
applying a bit line pre-pulse signal to a bit line connected to a first memory string of the plurality of memory strings during a pre-charge period;
applying a word line signal to a selected word line connected to a selected

memory cell of the plurality of memory cells of the first memory string during the pre-charge period; and

applying a plurality of word line pre-pulse signals to a plurality of word lines connected to the plurality of memory cells of the first memory string and disposed between the select gate line and the selected word line during the pre-charge period, wherein voltage levels of the plurality of word line pre-pulse signals are incremental, the step comprising:

applying a first word line pre-pulse signal of the plurality of word line pre-pulse signal to a first group of the plurality of word lines disposed adjacent to the selected word line and disposed between the selected word line and the select gate line during the pre-charge period;

applying a second word line pre-pulse signal of the plurality of word line pre-pulse signal to a second group of the plurality of word lines disposed adjacent to the first group of the plurality of word lines and disposed between the first group of the plurality of word line and the select gate line during the pre-charge period; and

applying a third word line pre-pulse signal of the plurality of word line pre-pulse signal to a third second group of the plurality of word lines disposed adjacent to the second group of the plurality of word lines and between the second group of the plurality of word lines and the select gate line during the pre-charge period;

wherein a voltage level of the second word line pre-pulse signal is greater than a voltage level of the first word line pre-pulse signal and a voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal.

12-13. (cancelled)

14. (currently amended): The control method of claim [[12]] 11, wherein an ending of the second word line pre-pulse signal is after an ending of the first word line

pre-pulse signal and an ending of the third word line pre-pulse signal is after the ending of the second word line pre-pulse signal.

- 5 15. (currently amended): The control method of claim [[12]] 11, wherein a pulse duration of the second word line pre-pulse signal is greater than a pulse duration of the first word line pre-pulse signal and a pulse duration of the third word line pre-pulse signal is greater than the pulse duration of the second word line pre-pulse signal.
- 10 16. (original): The control method of claim 11, wherein the memory array further comprises at least one dummy memory cell, the at least one dummy memory cell is disposed between the select gate transistor and the plurality of memory cells and connected in series with the select gate transistor and the plurality of memory cells, and the non-volatile memory device further comprises at least one dummy
- 15 word line and each dummy word line is connected to a respective dummy memory cell, wherein the second control circuit is configured to apply a dummy word line pre-pulse signal to the at least one dummy word line.
- 20 17. (original): The control method of claim 16, wherein a voltage level of the dummy word line pre-pulse signal is greater than voltage levels of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
- 25 18. (original): The control method of claim 16, wherein an ending of the dummy word line pre-pulse signal is after endings of the plurality of word line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.
- 30 19. (original): The control method of claim 16, wherein a pulse duration of the dummy word line pre-pulse signal is greater than pulse durations of the plurality of word

line pre-pulse signals applied to the word lines disposed between the at least one dummy word line and the selected word line during the pre-charge period.

20. (original): The control method of claim 11, wherein the first string of the plurality
5 of memory strings is an unselected string and the bit line is an unselected bit line during the pre-charge period.

Electronic Acknowledgement Receipt	
EFS ID:	42071315
Application Number:	16709944
International Application Number:	
Confirmation Number:	7658
Title of Invention:	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD
First Named Inventor/Applicant Name:	Jianquan Jia
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Jessie Su
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0261USA3
Receipt Date:	04-MAR-2021
Filing Date:	11-DEC-2019
Time Stamp:	02:11:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	4135156.PDF	605391	no	3
			e6e3e2ff527a6c291445a9d8ec06d754ecb9a802		
Warnings:					

Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	4135155.PDF	93395	no	1
			b094587fd9c4d8dd1c3671bd8020d18fccf63551		
Warnings:					
Information:					
3	Claims	4135154.PDF	104277	no	6
			1b8ac12436f5275842e68f70ab382f89acedf9bd		
Warnings:					
Information:					
Total Files Size (in bytes):				803063	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record
5 in the application file.

1. Claim Amendments

Claims 1, 4-5, 11 and 14-15 have been amended. Claim 1 is amended to include all the limitations of allowable claim 3, and claims 2-3 are accordingly cancelled. The
10 dependency of claims 4 and 5 is changed to depend upon base claim 1. Claim 11 is amended to include all the limitations of allowable claim 13, and claims 12-13 are accordingly cancelled. The dependency of claims 14 and 15 is changed to depend upon base claim 11. These amendments are at least supported by paragraph [0022] of the specification, FIG. 4 and claims as originally filed. No new matter is entered. Acceptation
15 of the amendments is hereby requested.

2. Claims in view of 35 U.S.C. 102

Claim 1-2, 6, 10-12, 16 and 20 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Chen (US 10,770,157); claim 1-2, 6, 10-12, 16 and 20 are rejected under
20 35 U.S.C. 102(a)(2) as being anticipated by Chen (US 10,283,202); and claim 1-2 and 10-12 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Kim (US2011/0194351).

Response:

25 In response to allowable subject matter of the Office Action, claim 1 has been amended to include all the limitations of allowable claim 3, and claims 2-3 are accordingly cancelled. Claim 11 has been amended to include all the limitations of allowable claim 13, and claims 12-13 are accordingly cancelled. Independent claims 1 and 11 now recite the features of “the second control circuit is configured to apply a first
30 word line pre-pulse signal of the plurality of word line pre-pulse signal to a first group of

the plurality of word lines disposed adjacent to the selected word line and disposed between the selected word line and the select gate line during the pre-charge period, apply a second word line pre-pulse signal of the plurality of word line pre-pulse signal to a second group of the plurality of word lines disposed adjacent to the first group of the plurality of word lines and disposed between the first group of the plurality of word line and the select gate line during the pre-charge period, and apply a third word line pre-pulse signal of the plurality of word line pre-pulse signal to a third second group of the plurality of word lines disposed adjacent to the second group of the plurality of word lines and between the second group of the plurality of word lines and the select gate line during the pre-charge period, wherein a voltage level of the second word line pre-pulse signal is greater than a voltage level of the first word line pre-pulse signal and a voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal”, which is not taught by the references.

Since claims 1 and 11 of the instant application have recited at least one distinct feature which is not taught by the references, claims 1 and 11 should be allowable. Reconsideration of claims 1 and 11 is respectfully requested. Claims 4-10 are dependent on claim 1, claims 14-20 are dependent on claim 11, and claims 4-10, 14-20 should be allowable if claims 1 and 11 are found allowable. Reconsideration of claims 4-10, 14-20 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Appl. No. 16/709,944
Reply to Office action of January 15, 2021

Sincerely yours,

/Roger Chen/

Date: 03/02/2021

Roger Chen, Patent Agent No. 67,314

5 5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan

Voice Mail: 302-729-1562

e-mail : RogerChen@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in
10 D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD				Application or Docket Number 16/709,944		Filing Date 12/11/2019		☐ To be Mailed		
Substitute for Form PTO-875										
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO										
APPLICATION AS FILED - PART I										
FOR		(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA			RATE (\$)		FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*			x \$100 =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*			x \$460 =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL				
APPLICATION AS AMENDED - PART II										
AMENDMENT	03/04/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	x \$100 =		0		
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	x \$480 =		0		
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		0		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =				
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =				
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE				
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE				
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/ANTJUAN M RIVERA/				
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 04/05/2021
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/05/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/709,944	12/11/2019	Jianquan Jia	YMTP0261USA3	7658

TITLE OF INVENTION: NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	07/06/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980.

It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
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Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

27765 7590 04/05/2021

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/709,944	12/11/2019	Jianquan Jia	YMTP0261USA3	7658

TITLE OF INVENTION: NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	07/06/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, VIET Q	2827	365-230060

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/709,944	12/11/2019	Jianquan Jia	YMTP0261USA3	7658
27765	7590	04/05/2021	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION 5F., NO.389, FUHE RD., YONGHE DIST. NEW TAIPEI CITY, TAIWAN			NGUYEN, VIET Q	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 04/05/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/709,944	Applicant(s) Jia et al.	
	Examiner VIET Q NGUYEN	Art Unit 2827	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment on 3/4/2021.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1,4-11 and 14-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material ____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other ____.
--	---

/VIET Q NGUYEN/ Primary Examiner, Art Unit 2827	
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Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Reasons for Allowance

1. The following is an examiner's statement of reasons for allowance:

The prior arts fail to teach or fairly suggest a non-volatile memory device comprising:

a memory array comprising a plurality of memory strings, each memory string comprising a select gate transistor and a plurality of memory cells connected in series with the select gate transistor; a bit line connected to a first memory string of the plurality of memory strings; a select gate line connected to the select gate transistor of the first memory string of the plurality of memory strings; a plurality of word lines connected to the plurality of memory cells of the first memory string of the plurality of memory strings, each word line connected to a respective memory cell of the first memory string; a first control circuit configured to apply a bit line pre-pulse signal to the bit line during a pre-charge period; and a second control circuit configured to apply a word line signal to a selected word line of the plurality of word lines and apply a plurality of word line pre-pulse signals to word lines disposed between the select gate line and the selected word line during the pre-charge period, wherein voltage levels of the plurality of word line pre-pulse signals are incremental, wherein the second control circuit is configured to apply a first word line pre-pulse signal of the plurality of word line

pre-pulse signal to a first group of the plurality of word lines disposed adjacent to the selected word line and disposed between the selected word line and the select gate line during the pre-charge period, apply a second word line pre-pulse signal of the plurality of word line pre-pulse signal to a second group of the plurality of word lines disposed adjacent to the first group of the plurality of word lines and disposed between the first group of the plurality of word line and the select gate line during the pre-charge period, and apply a third word line pre-pulse signal of the plurality of word line pre-pulse signal to a third second group of the plurality of word lines disposed adjacent to the second group of the plurality of word lines and between the second group of the plurality of word lines and the select gate line during the pre-charge period, wherein a voltage level of the second word line pre-pulse signal is greater than a voltage level of the first word line pre-pulse signal and a voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIET Q NGUYEN whose telephone number is (571)272-1788. The examiner can normally be reached on M-F 7:30-3PM EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

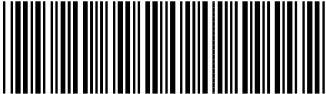
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VIET Q NGUYEN/
Primary Examiner, Art Unit 2827

<i>Index of Claims</i> 	Application/Control No. 16/709,944	Applicant(s)/Patent Under Reexamination Jia et al.
	Examiner VIET Q NGUYEN	Art Unit 2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	01/12/2021	03/31/2021							
1	1	✓	=							
	2	✓	-							
	3	○	-							
2	4	○	=							
3	5	○	=							
4	6	○	=							
5	7	○	=							
6	8	○	=							
7	9	○	=							
8	10	✓	=							
9	11	✓	=							
	12	✓	-							
	13	○	-							
10	14	○	=							
11	15	○	=							
12	16	✓	=							
13	17	○	=							
14	18	○	=							
15	19	○	=							
16	20	✓	=							

Issue Classification 	Application/Control No. 16/709,944	Applicant(s)/Patent Under Reexamination Jia et al.	
	Examiner VIET Q NGUYEN	Art Unit 2827	

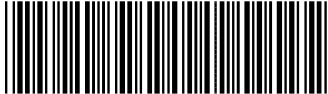
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Symbol					Type	Version
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G11C	/	11	/	4094	I	2013-01-01
G11C	/	11	/	419	I	2013-01-01
G11C	/	11	/	4099	I	2013-01-01
G11C	/	11	/	4074	I	2013-01-01

CPC Combination Sets					
Symbol				Type	Set
	/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/VIET Q NGUYEN/ Primary Examiner, Art Unit 2827	31 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

U.S. Patent and Trademark Office

Part of Paper No.: 20210331

Issue Classification 	Application/Control No. 16/709,944	Applicant(s)/Patent Under Reexamination Jia et al.
	Examiner VIET Q NGUYEN	Art Unit 2827

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G11C		8	00
NON-CLAIMED			

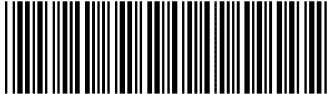
US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
365	230.06

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/VIET Q NGUYEN/ Primary Examiner, Art Unit 2827	31 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

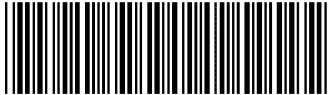
U.S. Patent and Trademark Office

Part of Paper No.: 20210331

Issue Classification 	Application/Control No. 16/709,944	Applicant(s)/Patent Under Reexamination Jia et al.
	Examiner VIET Q NGUYEN	Art Unit 2827

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	8	10	15	19										
	2	9	11	16	20										
	3		12												
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5	7	12	16												
6	8	13	17												
7	9	14	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/VIET Q NGUYEN/ Primary Examiner, Art Unit 2827	31 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

<i>Search Notes</i> 	Application/Control No. 16/709,944	Applicant(s)/Patent Under Reexamination Jia et al.
	Examiner VIET Q NGUYEN	Art Unit 2827

CPC - Searched*		
Symbol	Date	Examiner
G11C 11/4085, 11/4074, 11/4094, 11/4099, 11/419	8/24/2020	vn

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	230.06, 185.18, 185.24	8/24/20	vn

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
G11C 11/4085, 11/4074, 11/4094, 11/4099, 11/419	8/24/2020	vn
EAST	01/12/2021	vn
Updated IDS	01/12/2021	vn
Updated EAST	03/31/2021	vn

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G11C	11/4085, 11/4074, 11/4094, 11/4099, 11/419	01/12/2021	vn

/VIET Q NGUYEN/ Primary Examiner, Art Unit 2827	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	19,221	(G11C11/4085 or G11C11/4099 or G11C11/4074 or G11C11/419 or G11C11/4094).cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2021/03/31 10:01
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L4	89	((("JIA") near3 ("Jianquan")) OR (("CUI") near3 ("Ying")) OR (("YOU") near3 ("Kaikai"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2021/03/31 10:02

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L5	150	((("YANGTZE") near3 ("MEMORY") near3 ("TECHNOLOGIES") near3 ("CO") near3 ("LTD"))).AS,AANM.	USPAT	OR	ON	2021/03/31 10:02
L6	35	((("JIA") near3 ("Jianquan")) OR (("CUI") near3 ("Ying")) OR (("YOU") near3 ("Kaikai"))).INV.	USPAT	OR	ON	2021/03/31 10:02
L7	5,470	365/230.06.ccls.	USPAT	OR	ON	2021/03/31 10:03
L8	0	(2 or 7) and (5 or 6) and (pre-pulse adj1 signal\$1)	USPAT	OR	ON	2021/03/31 10:03

3/31/2021 10:03:54 AM

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 Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 7658

SERIAL NUMBER 16/709,944	FILING or 371(c) DATE 12/11/2019 RULE	CLASS 365	GROUP ART UNIT 2827	ATTORNEY DOCKET NO. YMTP0261USA3		
APPLICANTS Yangtze Memory Technologies Co., Ltd., Wuhan City, CHINA; INVENTORS Jianquan Jia, Wuhan City, CHINA; Ying Cui, Wuhan City, CHINA; Kaikai You, Wuhan City, CHINA; ** CONTINUING DATA ***** This application is a CON of PCT/CN2019/112409 10/22/2019 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 01/02/2020						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/VIET Q NGUYEN/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CHINA	SHEETS DRAWINGS 4	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION 5F., NO.389, FUHE RD., YONGHE DIST. NEW TAIPEI CITY, TAIWAN						
TITLE NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD						
FILING FEE RECEIVED 1720	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/709,944	12/11/2019	Jianquan Jia	YMTP0261USA3

CONFIRMATION NO. 7658

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

PUBLICATION NOTICE



OC000000125080521

Title:NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD

Publication No.US-2021-0118484-A1

Publication Date:04/22/2021

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PART B – FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 04/05/2021

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Hitomi Lin	(Typed or printed name)
/Hitomi Lin/	(Signature)
06/29/2021	(Date)

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.,
New Taipei City,
Taiwan

APPLICATION NO	FLING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
16/709,944	12/11/2019	Jianquan Jia	YMTPO261USA3	7658

TITLE OF INVENTION: **NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD**

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0	\$0	\$1200	07/06/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, VIET Q	2827	365-230060

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. **Winston Hsu**2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE or COUNTRY)

Yangtze Memory Technologies Co., Ltd.**Wuhan City, Hubei Province, P.R.C.**Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government4a. Fees Submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment (Please first reapply any previously paid fee shown above):

- ☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-3105

5. Change of Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27.
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Winston Hsu/

Date 06/28/2021

Typed or printed name Winston Hsu

Registration No. 41526

Electronic Patent Application Fee Transmittal				
Application Number:		16709944		
Filing Date:		11-Dec-2019		
Title of Invention:		NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD		
First Named Inventor/Applicant Name:		Jianquan Jia		
Filer:		Winston Hsu/Hitomi Lin		
Attorney Docket Number:		YMTP0261USA3		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	43100210
Application Number:	16709944
International Application Number:	
Confirmation Number:	7658
Title of Invention:	NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD
First Named Inventor/Applicant Name:	Jianquan Jia
Customer Number:	27765
Filer:	Winston Hsu/Hitomi Lin
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	YMTP0261USA3
Receipt Date:	29-JUN-2021
Filing Date:	11-DEC-2019
Time Stamp:	01:43:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E20216S243521039
Deposit Account	503105
Authorized User	Hitomi Lin
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)
37 CFR 1.20 (Post Issuance fees)
37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	4254194.PDF	762494	no	1
			5684402e11de34949329d699b2bb85690558d197		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30336	no	2
			e63772876893bc6aba9899d8479cfc9fc95455a		

Warnings:

Information:

Total Files Size (in bytes):	792830
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/709,944	08/03/2021	11081164	YMTP0261USA3	7658

27765 7590 07/14/2021
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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TAIWAN

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

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IR103 (Rev. 10/09)

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Micron v. YMTC
IPR2024-00795