

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00795
Patent 11,501,822

**DECLARATION OF STEVEN PRZYBYLSKI, PH.D. IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

Executed this 17th day of July, 2024 in Ann Arbor, Michigan.



Steven A. Przybylski, Ph.D.

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	QUALIFICATIONS	2
III.	MY ASSIGNMENT AND BASES OF OPINIONS	4
IV.	SUMMARY OF MY OPINIONS	6
V.	APPLICABLE LEGAL STANDARDS	6
	A. Ordinary Skill in the Art	6
	B. Claim Construction	8
VI.	SCOPE AND CONTENT OF THE PRIOR ART	9
	A. Zhao	9
	B. Lee	14
	C. The Combination of Zhao and Lee Described in the Petition	17
VII.	CONCLUSION	26

I, Steven Przybylski, Ph.D., hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Yangtze Memory Technologies Company, LTD (“YMTC”) in the above captioned *inter partes* review of U.S. Patent No. 11,501,822 (Ex. 1001, “’822 patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’822 patent (“Petition”) and the April 9, 2024 Declaration of Dr. David Kuan-Yu Liu (Ex. 1003, “Liu”).

2. I am being compensated for my time at my usual consulting rate of \$575 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with Patent Owner in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

3. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. QUALIFICATIONS

4. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

5. I earned a Bachelor of Applied Science from the University of Toronto in 1980. I was enrolled in the Engineering Science program, completing a course of study combining the Electrical Engineer and Computer Science options.

6. I earned a Master of Science in Electrical Engineering degree and a Ph.D. in Electrical Engineering in 1982 and 1988 respectively, both from Stanford University.

7. I also earned a Masters of Business Administration from the Haas School of Business at the University of California at Berkeley in 2000.

8. I have extensive experience with memory semiconductor integrated circuits and the memory systems constructed of them. At Stanford, my dissertation was on the optimization of single- and multi-level cache hierarchies to maximize system-level performance. Also at Stanford, I was a member of the core team that architected, designed, built, and tested the seminal MIPS processor. I was responsible for the design of the instruction decode and control units as well as architecting the virtual memory support. I assembled and debugged the entire microprocessor design and oversaw its fabrication and testing. In 1984 and 1985, I

took a leave of absence from Stanford to become a member of the founding team of MIPS Computer Systems, a startup in California that designed, built, and sold processors and computer systems. In 1989, after finishing my doctorate and brief post-doctorate at Stanford, I returned to MIPS Computer Systems. Throughout my two periods of employment at MIPS Computer Systems, I had a number of titles and worked on a variety of projects. Noteworthy were stints as processor architect, systems architect, hardware-software team liaison, and Chief Scientist of the High-End Systems group. During the second period, I also served as a Consulting Assistant Professor in the Department of Electrical Engineering at Stanford. I designed and taught an advanced graduate level course on cache and memory system design.

9. In 1991, I left MIPS to become an independent consultant. In that capacity I have provided technical, strategic, marketing, and intellectual property services to a large number of clients both domestically and internationally.

10. The technical consulting I performed was principally related to advancements in semiconductor memories and their application in systems. Specifically with respect to non-volatile memories and Flash memories in particular, I advised companies on a variety of memory types and on trends in NAND and NOR Flash memories and the processes used in their manufacture. In the 2000's, I helped develop a new NAND Flash architecture and separately a universal memory

interface that was optimized for use in heterogeneous memory systems and that was equally applicable to DRAMs and to NAND Flash devices.

11. I am a member of both the Institute of Electrical and Electronics Engineers (IEEE) and the Association of Computing Machinery (ACM). In addition, in 1997 I became a registered patent agent. I am listed as the inventor on 11 domestic patents and their foreign counterparts. The subject matters include memory devices, memory subsystems, networks, error detection and correction codes, processors and cache memories. Between 1994 and approximately 2000, I was a leading independent analyst following, writing, and teaching about both the technical and business aspects of the DRAM industry. Overall, I have written three books and over 25 articles in the areas of memory, processors, and computer systems. In particular, I wrote and revised an 850-page book entitled “New DRAM Technologies: A Comprehensive Analysis of the New Architectures.” I have presented many lectures, classes and seminars on semiconductor memories and their memory systems, processors and computer systems. I have presented full and half-day seminars on discrete and embedded DRAMs to over 2,500 engineers, marketers, managers, and financial analysts.

III. MY ASSIGNMENT AND BASES OF OPINIONS

12. I have been asked to provide my opinions as to the scope and content of the prior art presented by Petitioner and Dr. Liu in Ground 3 of the Petition.

Specifically, I have been asked to provide my opinions concerning the scope and content of the Lee (Ex. 1004) and Zhao (Ex. 1005) references as would have been understood by a person of ordinary skill in the art, and to respond to certain assertions by Petitioner and Dr. Liu regarding the combination of Lee and Zhao asserted in Ground 3 of the Petition.

13. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited herein including those listed below:

Exhibit No.	Reference
N/A	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,501,822 (IPR2024-00795, Paper 1)
Ex. 1001	U.S. Patent No. 11,501,822 B2 to Jia et al. (“the ’822 patent”)
Ex. 1002	File History of U.S. Patent No. 11,501,822 B2 to Jia et al.
Ex. 1003	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
Ex. 1004	U.S. Patent No. 10,121,529 B2 to Lee (“Lee”)
Ex. 1005	U.S. Patent No. 10,643,718 B2 to Zhao et al. (“Zhao”)
Ex. 1006	Aritome, “NAND Flash Memory Technologies” (2016)
Ex. 1007	Brown et al., “Nonvolatile Semiconductor Memory Technology” (1998)
Ex. 1008	Cappelletti, et al., “Flash Memories” (1999)
Ex. 1009	U.S. Patent No. 9,589,978 to Yip
Ex. 1010	U.S. Patent No. 10,726,920 B2 to Yang
Ex. 1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
Ex. 1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
Ex. 1015	File History of U.S. Patent No. 11,081,164 (Appl 16-709,944) to Jia et al.
Ex. 1017	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
Ex. 2002	U.S. Pat. No. 11,081,164 (“the ’164 patent”)
Ex. 2004	U.S. Pat. No. 10,700,157 (“Chen”)
Ex. 2005	U.S. Pub. 2011/0194351 (“Kim”)

14. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

15. All emphases (such as bolding, underlying, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. SUMMARY OF MY OPINIONS

16. It is my opinion that:

- Neither Lee or Zhao disclose the use of three distinct word line pre-pulse signals being applied to groups of a plurality of word lines.
- A person of ordinary skill in the art would not have been motivated have been motivated to apply Lee's purported teachings related to offsetting resistance to Zhao's system in the manner described in the Petition.

V. APPLICABLE LEGAL STANDARDS

17. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

A. Ordinary Skill in the Art

18. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an

“ordinary artisan” or by the acronyms “POSITA” (person of ordinary skill in the art) or “POSA,” as of the time of the invention.

19. I have been asked to consider the level of ordinary skill that someone in the field of technology of the '822 patent would have had at the time the claimed invention disclosed in the '822 patent was made. In determining the level of ordinary skill in the art, I considered the following: (1) the levels of education and experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology.

20. In my opinion, a person of ordinary skill in the art capable of reading and understanding the claims of the '822 patent at the time of the invention would have had at least a bachelor's degree in electrical engineering, computer engineering, or a similar discipline, along with at least 2 years of professional experience with semiconductor memory devices, or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

21. In this case, Dr. Liu has asserted in his declaration that a person of ordinary skill in the art at the time of the invention described in the '822 patent would have a:

bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices (including issues relating to the operation, e.g., programming, of said

devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

Liu ¶37.

22. In view of my educational background and years of experience, including my many years of experience developing NAND Flash architecture, I both met and exceeded the qualifications of a person of ordinary skill in the art as of the earliest possible priority date of the '822 Patent in October 2019. That is true under both my own definition of a POSITA, as well as under Dr. Liu's definition, and my opinions as set forth herein are the same regardless of which definition of a person of ordinary skill in the art is applied.

B. Claim Construction

23. I understand that Patent Owner has proposed that the term “word line pre-pulse signal” is properly construed as a “pulse signal to prepare word lines for a programming step,” and that it is the only term Patent Owner proposes for construction in its Preliminary Response. I also understand that Petitioner did not identify any proposed claim constructions in the Petition.

24. I also understand that the parties have identified proposed terms to be construed in the district court case that is proceeding in parallel with this requested IPR, but that the parties have not yet exchanged proposed claim constructions. At

this time, I have not been asked by Patent Owner to provide an opinion on claim construction in either the requested IPR or in the parallel district court proceedings.

25. Where applicable, I have been instructed to apply Patent Owner's proposed construction of the term "word line pre-pulse signal" when rendering my opinions. However, my opinions as to Ground 3 do not depend on this particular construction. For all other terms, I have applied the plain and ordinary meaning of the claims consistent with the intrinsic evidence.

VI. SCOPE AND CONTENT OF THE PRIOR ART

26. I understand that Petitioner and Dr. Liu assert that claims 1, 4-7, 9, 11, 14-16, and 18-19 of the '822 patent are obvious over the combination of Zhao (Ex. 1005) in view of Lee's purported teachings (Ex. 1004). Petition at 59; Liu, ¶¶318-319-112; *see also* Petition at 60-71; Liu at ¶¶320-397. I have been asked to opine on the scope and content of Zhao and Lee, what a person of ordinary skill in the art would have understood Zhao and Lee to disclose and teach, and whether a person of ordinary skill in the art would have been motivated to apply Lee's teachings to Zhao in the manner proposed in the Petition.

A. Zhao

27. U.S. Patent No. 10,643,718 ("Zhao") was issued on May 5, 2020. For the purposes of my present analysis, I have been asked to assume that Zhao is prior art to the '822 patent.

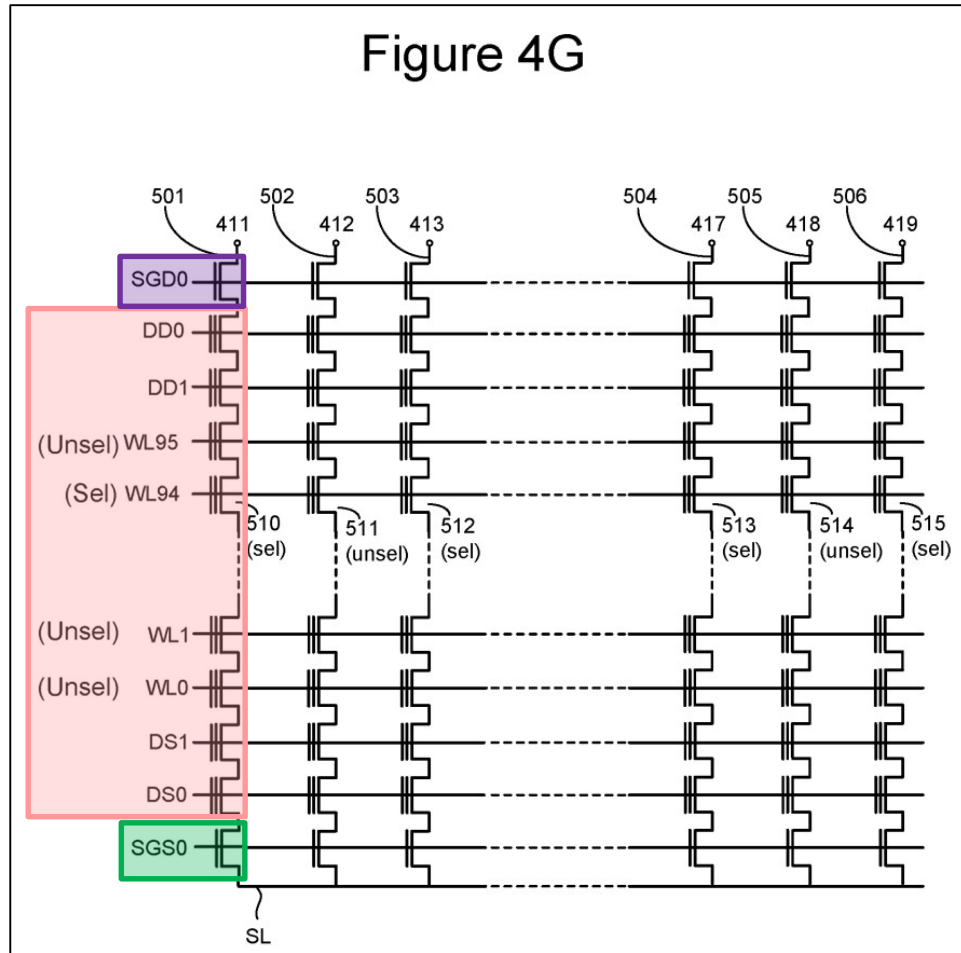
28. Zhao addresses the phenomenon of “program disturb” in memory systems, which describes “the unintended programming of one or more locations in a memory while performing a programming process for other locations in the memory.” Zhao, 2:10-14. Specifically, Zhao discusses one potential source of program disturb that “can result from electrons trapped in the channel being accelerated from one side of a selected word line to another side of the selected word line and redirected into the selected word line.” Zhao, 2:14-18.

29. To address this source of program disturb, Zhao states that “countermeasures are proposed to open the channel from one side of a selected word line to the other side of the selected word line.” Zhao, 2:10-26. In other words, Zhao’s techniques are intended to create an even distribution of charges in the area surrounding the selected word line by turning on the memory cell transistors driven by the selected word line prior to the program operation. Zhao describes three categories of possible countermeasures that take place at different points in the programming cycle. First, Zhao states that “[o]ne proposed countermeasure includes purging (cleaning/clearing the electrons from) the already programmed side of the channel during a pre-charge operation performed as part of the programming process.” Zhao, 2:27-49. Second, Zhao states that “[a]nother proposed countermeasure includes applying a voltage spike on one or more already programmed unselected word lines adjacent the selected word line during boosting

of the not yet programmed side of the channel.” Zhao, 2:50-3:4. Finally, Zhao states that “[a]nother proposed countermeasure include delaying the ramping down of voltages of one or more already programmed unselected word lines adjacent the selected word line at the conclusion of a program verify process.” Zhao, 3:5:24.

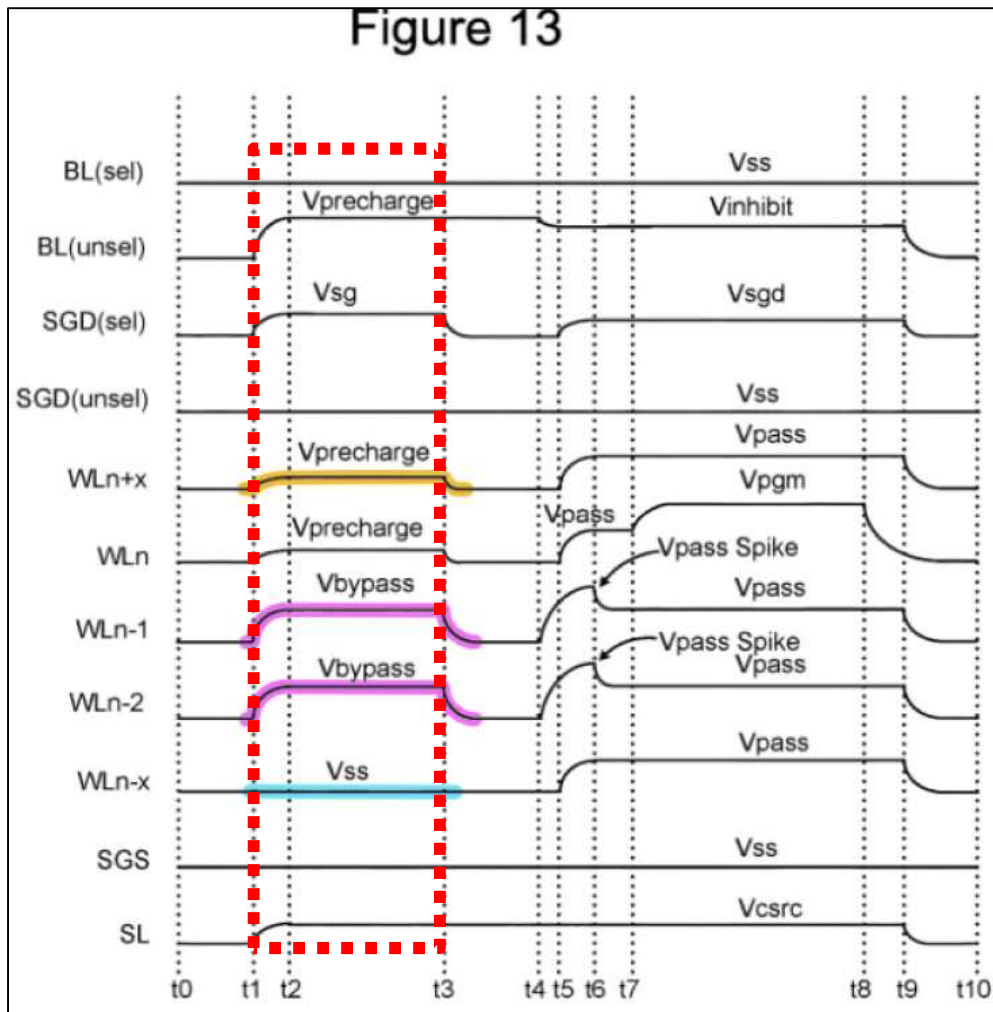
30. As illustrated in Figure 4G, the structure of Zhao’s memory is based on “vertical NAND strings with charge-trapping material” that “includes **memory cells** connected by a channel.” Zhao, 6:34-46. Each “NAND string” is made up of multiple **memory cells** connected in series between a drain side select transistor controlled by a “[d]rain side selection line” and a source side select transistor controlled by “[s]ource side selection line.” Zhao, 9:10-18, 11:53-12:13. These selection lines are used to select which of the NAND strings to interact with for memory operations. Each NAND string is connected to a bit line through its drain side selection transistor and to a source line (SL) through its source side selection transistor. Each **memory cell** in a NAND string is connected to a word line, and during a memory operation there will be a “selected memory cell” on a “selected NAND string”, “unselected memory cells” on the selected NAND string, as well as unselected NAND strings. Zhao, 12:14-41, 27:30-48.¹

¹ All emphasis and annotations have been added, unless otherwise noted.



31. Figure 13 is a signal or timing diagram illustrating the different program disturb countermeasures disclosed by Zhao starting from time t_0 when “all the depicted signals are at ... **0 volts (V_{ss})**.” Zhao, 22:34-41. As is relevant for the '822 Patent, the time period “from **t_1 - t_3 corresponds to pre-charging.**” *Id.*²

² For convenience, I have reproduced the same annotations used by the Petition and Dr. Liu for **$V_{precharge}$** , **V_{bypass}** , and **V_{ss} (e.g., 0 v)**.



32. As depicted in Fig. 13, different voltages are applied to different word lines. As explained by Zhao, a “**pre-charge voltage Vprecharge**” is applied to the “unselected bit lines,” “the selected word line WLn,” and “the drain side unselected word lines WLn+x,” in order to cause “pre-charging of the drain side channels of unselected NAND strings.” Zhao, 22:39-50.

33. At the same time, “already programmed source side unselected word lines WLn-1 and WLn-2 are raised to a **bypass voltage Vbypass**,” which “comprises a voltage of a magnitude sufficient to cause memory cells receiving the **bypass**

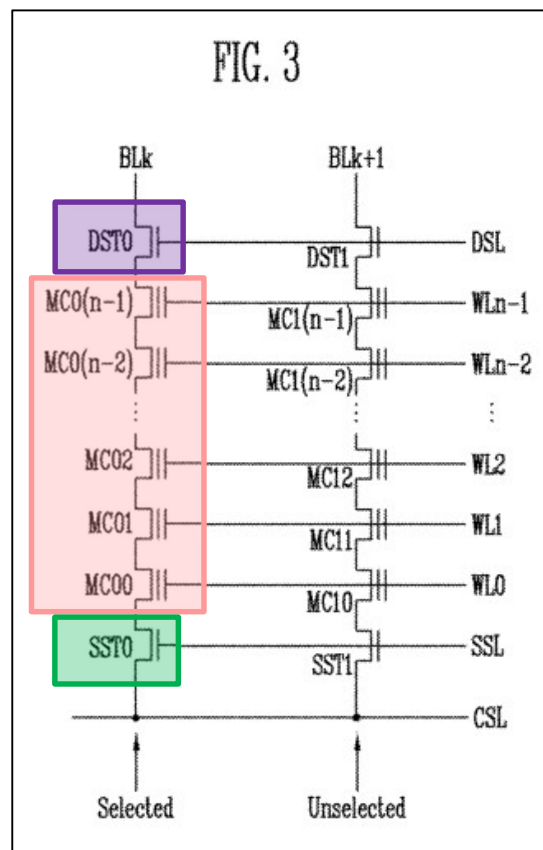
voltage to turn on, regardless of which state the memory cells are programmed (or erased) to.” Zhao, 22:50-60. As explained by Zhao, raising word lines to **Vbypass** “opens up the channel (e.g., electrically couples the two ends of the channel)” in the corresponding memory cells. Zhao, 22:65-23:5.

34. Finally, as explained by Zhao, “[t]he remaining source side unselected word lines WLn-x remain at **Vss (e.g., 0 v)**.” Zhao, 23:7-8. As explained by Zhao, the flat voltage applied to the unselected source side word lines may “0 volts” another voltage level “too low to pre-charge and/or too low to turn on the memory cells in a highest data state.” Zhao, 19:22-26. But regardless of the precise value used, Zhao teaches that the word lines “remain” at that value throughout the t1-t3 period that corresponds to pre-charging. *See* Zhao, 22:34-43, 23:7-10. Further, as illustrated in Figure 13, during the precharge period, the gate of the source select transistor (signal SGS) is held at Vss, as are the gates of the “lowest” memory cells in the string (e.g. WLn-x). Thus, these transistors in the unselected strings that are closest to the source line remain off during the precharge operation. Zhao, Fig. 13, 22:18-23:12.

B. Lee

35. U.S. Patent No. 10,121,529 (“Lee”) was issued on November 6, 2018. For the purposes of my present analysis, I have been asked to assume that Lee is prior art to the ’822 patent.

36. Lee's summary section states that it is directed to "a semiconductor memory device configured to mitigate a program disturb phenomenon, and a method of operating the semiconductor memory device." Lee, 1:53-56. As illustrated in Fig. 3, Lee's memory cell strings are structured similar to Zhao and include "a **source select transistor SST0**, **memory cells MC00 to MC0(n-1)**, and a **drain select transistor DST0**" arranged in a series. Lee, 7:37-58.



37. Lee states that it seeks to create "a uniform precharge level in the entirety of the cell string." Lee, 7:58-62. According to Lee, a "typical" pre-charge operation will cause "a threshold voltage of a memory cell is increased by a

resistance component between the source select transistor and the drain select transistor” which can reduce the pre-charge level in the memory cell. Lee, 8:25-52.

38. To address this purported problem, Lee states that it will apply “different pre-bias voltages to the respective word line groups” along the entire length of the memory string based on the relative positions of the word lines. Lee, 2:63-3:7. For example, in a “memory block” that includes “thirty-two word lines WL0 to WL31,” Lee states that the system will determine “pre-bias voltages to be applied to the respective word lines WL0 to WL31 depending on a position of a word line coupled to the target memory cell to be programmed.” Lee, 8:3-17.

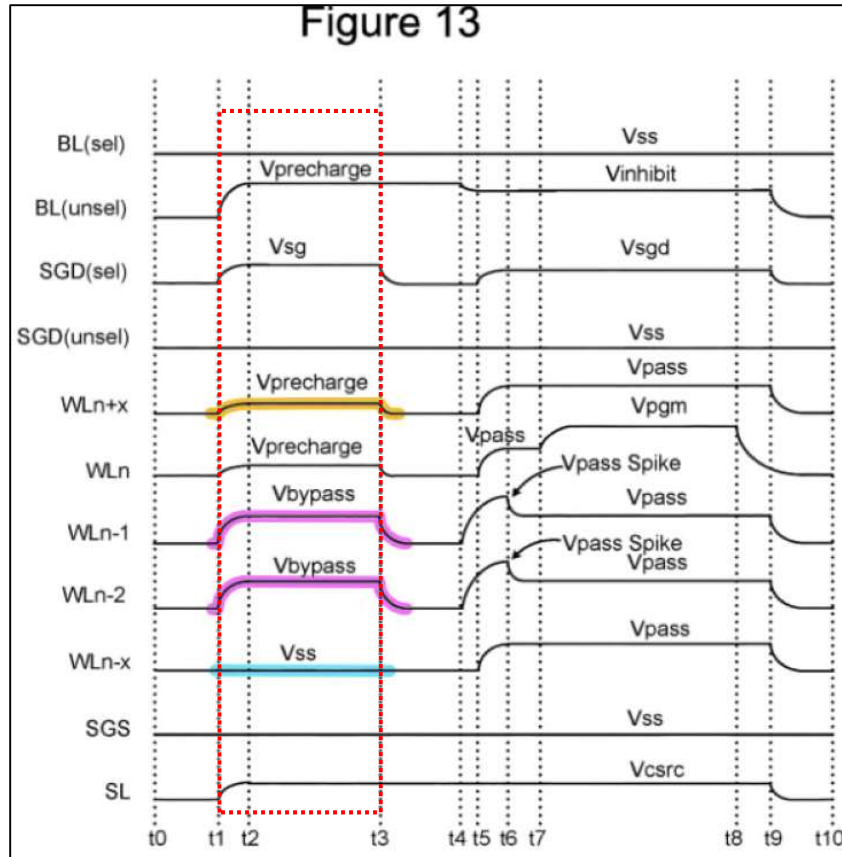
39. Specifically, Lee discloses that “during a precharge process, the closer a word line group to which a word line belongs is to the drain select transistor, the higher a pre-bias voltage to be applied to the word line may be.” Lee, 8:33-37. But Lee does not include any signal diagrams, or provide any further details regarding the shape and timing of the specific “pre-bias” voltages. The consequence of this application of different pre-bias voltages to each of the word lines according to their position in the memory block relative to the source and drain select lines if designed to ensure that all of the channels of the memory cells in the unselected NAND strings are turned on. Lee, 8:18-52.

C. The Combination of Zhao and Lee Described in the Petition

40. Petitioner and Dr. Liu argue that claims 1, 4-7, 9, 11, 14-16, and 18-19 of the '822 patent are obvious over the combination of Zhao in view of Lee's purported teachings. Petition at 59; Liu, ¶¶318-319-112; *see also* Petition at 60-71; Liu, ¶¶320-397. I disagree, and it is my opinion that a POSITA would not have been motivated to apply Lee's purported teachings to Zhao's system in the manner that Petitioner and Dr. Liu have described.

41. As explained in greater detail below, the purported benefits that Lee's purported teachings are intended to provide would not be applicable to the combined system described by the Petition. As described in Lee, the use of multiple pre-bias voltages is intended to compensate for the fact that "a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor." Lee, 8:25-52; *see also* Petition at 62 (characterizing Lee as trying to offset "effects caused by the resistance component between the source select transistor and the drain select transistor"). But those types of resistive effects that Lee seeks to compensate for are not present in the proposed combination described in the Petition. Rather, it appears that the proposed combination is driven primarily, if not exclusively, by hindsight bias and a desire to apply Lee's teachings to Zhao in a way that superficially emulates certain key features of the '822 patent.

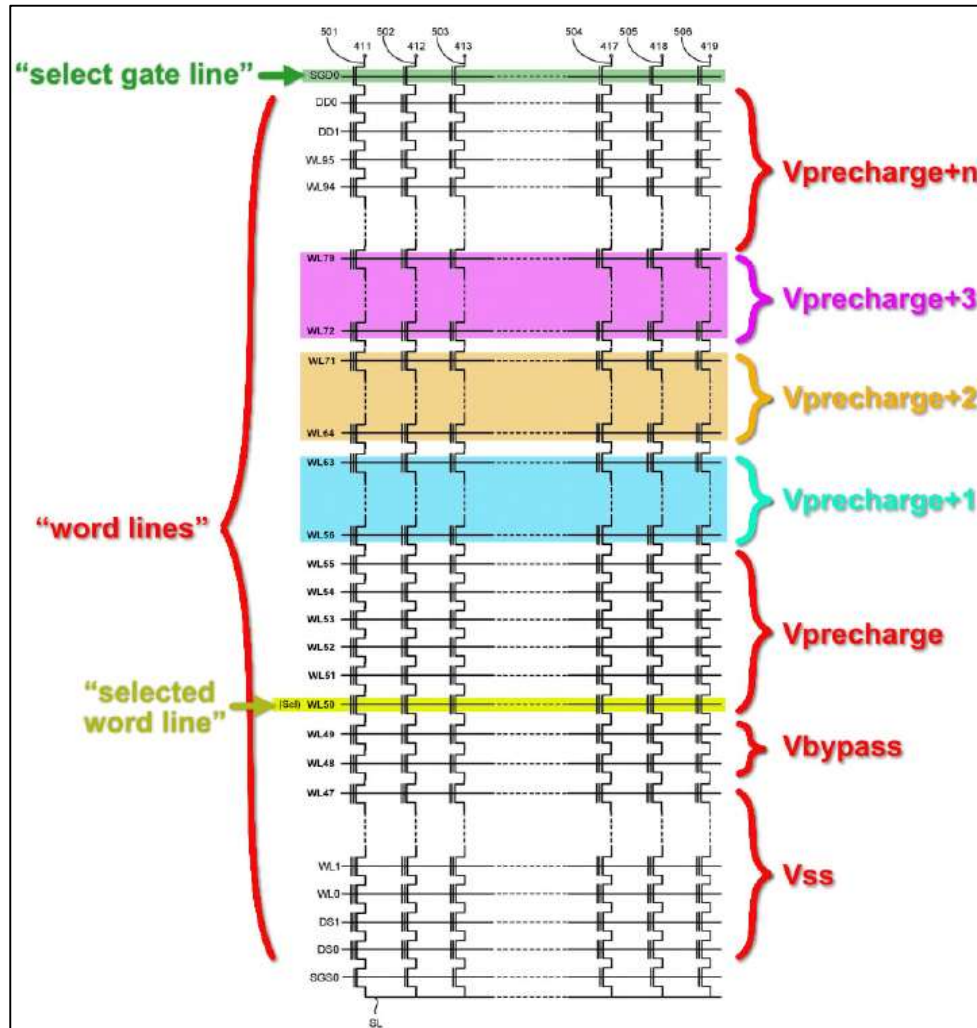
42. As I previously discussed in Section VI.A, Zhao discloses that a “**pre-charge voltage $V_{precharge}$** ” is applied to the “unselected bit lines,” “the selected word line WLn ,” and “the drain side unselected word lines $WLn+x$,” in order to cause “pre-charging of the drain side channels of unselected NAND strings.” Zhao, 22:39-50. Because the source select transistor and the memory cells closest to the source select transistor are off during precharge, no current flows at all during precharge through this portion of the string. So, as the precharge phase begins and the drain select transistor and all the memory cells in the upper portion of the unselected NAND string are turned on, the voltages in the channels of those memory cells comes to an equilibrium based on the unselected bit line voltage ($BL(unsel)$). Once this equilibrium is reached, no further current flow occurs in the unselected string during the precharge period. Zhao, Figure 13, 22:18-23:12.



Zhao Fig. 13.

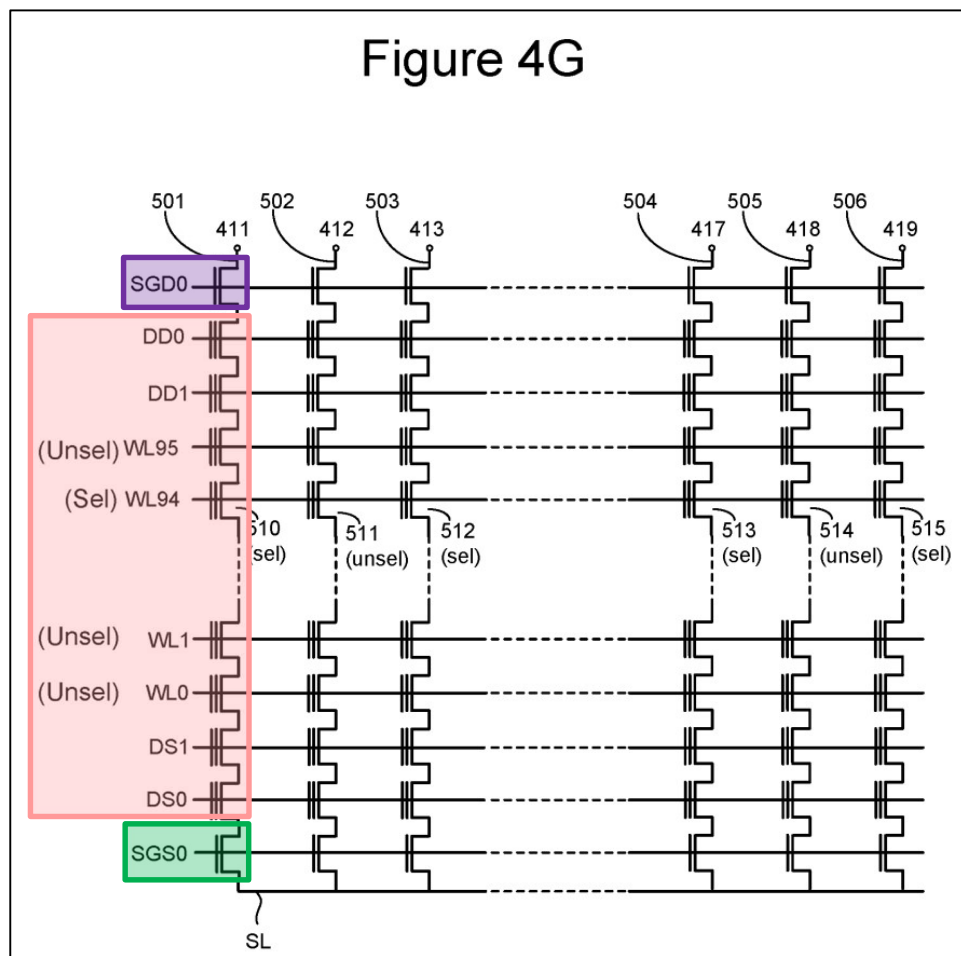
43. Petitioner and Dr. Liu argue, in effect, that a POSITA would have been motivated to apply Lee’s teachings to Zhao’s use of the **Vprecharge** signal on the drain side unselected word lines $WLn+x$. *See* Petition at 60-67. Specifically, the Petition suggests that a POSITA would have been motivated to replace **Vprecharge** with multiple different pre-charge signals, as purportedly taught by Lee, in view of Lee’s statement that this will offset “effects cause by the resistance component between the source select transistor and the drain select transistor.” Petition at 62; Liu, ¶340 (citing Lee at 1:52-56; 8:51-52; 15:4-7). Petitioner and Dr. Liu also go

further, and set forth an illustration of how the combined system would purportedly operate.



Petition at. 65 (Annotations reproduced from Petition). However, the proposed combination described in the Petition is inconsistent with the stated motivation of trying to offset a “resistance component between the source select transistor and the drain select transistor,” and attempting to apply Lee’s teachings in the manner proposed ignores the actual structure and operation of the memory cell string.

44. As I previously discussed in Sections VI.A and VI.B, both Lee and Zhao describe a “string” of “memory cells connected by a channel.” Zhao, 6:34-46; *see also* Zhao, 9:10,18, 11:53-12:13, Fig. 4G; Lee, 7:37-58, Fig. 3. For example, as shown in Figure 4G of Zhao, each memory string is made up of multiple **memory cells** connected in series between a “[d]rain side selection line” and a “[s]ource side selection line.” Zhao, 9:10,18, 11:53-12:13.



Zhao Fig. 4G. As a result of being connected in series, *all* of the **memory cells** in the string must be turned on to enable current to flow between the “[d]rain side selection line” and a “[s]ource side selection line.” *See* Zhao, 9:10,18, 11:53-12:13.

In other word, in order to form a conductive channel through the memory cell string, all of the memory cells that make up the string must be turned on. If any individual cells within the string or either of the select transistors are turned off, there is no current through the string. As a result, there are also no voltage drops across the channels of the memory cells along the length of the string, and no changes in the memory cell threshold voltages and the word line voltages necessary to form conductive channels in the memory cells as a result of their position within the string.

45. The Petition incorrectly suggests that a POSITA would have been motivated to apply Lee’s teachings to Zhao based on Lee purportedly teaching that its methods offset “effects caused by the resistance component between the source select transistor and the drain select transistor.” *See* Petition at 62 (citing Lee 8:25-52). But Petition ignores that several of memory cells within the string are *explicitly* turned off as part of the proposed combination. Specifically, Zhao’s use of **V_{ss}** (or another voltage that is “too low to pre-charge and/or too low to turn on memory cells in a highest data state”), cuts off the memory cell’s channel and precludes any current flowing along the memory string between the “[**d**]rain side selection line” (*i.e.*, the drain select transistor) and a “[**s**]ource side selection line” (*i.e.*, the source select transistor), or alternatively between the bit line at the top of the string and the source lines (SL) at the bottom of the string. *See* Zhao, 19:22-26. The purported motivation that Petitioner and Dr. Lui points to for applying Zhao’s teachings (*i.e.*, that multiple

different pre-charge voltages are needed to offset a “resistance component between the source select transistor and the drain select transistor”) is simply inapplicable in the proposed combination, as there are no voltage drops along the channels of the memory cells along the length of the string. Petition at 60. A POSITA would not have been motivated based on Lee’s disclosure to replace Zhao’s use of **Vprecharge** with multiple pre-charge signals in the manner that Petitioner has proposed, and attempting to do so would not compensate for a purported “resistance component” or otherwise help to create a more uniform charge distribution.

46. This basic inconsistency between Lee’s system and Zhao’s purported teachings that the Petition seeks to borrow is also highlighted by the distinct approaches that each reference uses for mitigating program disturb. Zhao discloses that its pre-charge operation is for “purging (cleaning/clearing the electrons from) the already programmed side of the channel” prior to the subsequent boosting and programming operations. *See Zhao*, 2:27-35; *see also id.*, 18:63-19:8 (describing a method for “purging the already programmed side of the channel during a pre-charge operation”). This act of “purging” is intended to mitigate program disturb resulting from “source side hot electron injection,” which arises from unwanted charges being accelerated from the source side of the selected word line to the drain side of the selected word line during the boosting process, and then being redirected into memory cells on the selected word line. *Zhao*, 18:36-51. To address this

phenomenon, Zhao teaches that “a bypass voltage to multiple already programmed side unselected word lines while pre-charging ... the channels of unselected NAND strings.” Zhao, 19:29-34; *see also* Zhao, 22:50-56. Applying this bypass voltage “electrically couples the two ends of the channel” in the region where the bypass voltage is applied, thereby allowing electrons to flow freely and near the selected word line and “eliminate the voltage differential between the source side of the channel and the drain side of the channel that may later cause program disturb.” Zhao, 22:65-23:5.

47. By comparison, Lee discusses a disparate approach for mitigating program disturb that would be inapplicable in Zhao’s system in the context of the proposed combination set forth in the Petition. As I discussed above, Zhao applies a localized bypass voltage to word lines adjacent to the selected word line that “electrically couples the two ends of the channel” and allows charges to be equalized, but does so without creating a conducting channel between the source select transistor and the drain select transistor at the ends of the memory string. *See* Zhao, 22:65-23:5. By comparison, Lee discloses applying a pre-charge voltage to *every* memory cell in the string in an effort to create a “uniform” charge distribution throughout the entire string. *See, e.g.*, Lee, 8:3-18 (a “memory block includes thirty-two word lines WL0 to WL31” and pre-bias voltages are “applied to the respective word lines WL0 to WL31 in a precharging step during a program operation”). Doing

so create a current through the memory string channel, and as a result, Lee (unlike Zhao) must compensate for the fact that the “pre-charge level in a source side channel is reduced and thus charge boosting is not effectively generated” because “a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor.” Lee, 8:25-31, 8:47-52.

48. A POSITA would not have been motivated to apply Lee’s teachings to Zhao in the manner suggested in the Petition. Lee and Zhao are not, as Petitioner and Dr. Liu seems to suggest, describing complementary and compatible techniques for reducing different types of program disturb. *See* Petition at 66-68. To the contrary, Lee’s use of preset bias levels for each and every word-line in the memory string (including those adjacent to the selected word line) is fundamentally different than the scheme described by Zhao. In essence, Lee is solving a problem that does not exist in Zhao. In the context of Petitioner’s proposed combination, where several memory cells in the string are cut off and there is no conductive channel along the full length of the memory string, Lee’s core teachings regarding the use of different voltages to compensate for resistance along the memory string (*i.e.*, at different locations between the source select transistor and the drain select transistor) would not provide the benefits that Lee’s teachings purport to provide.

49. Accordingly, the supposed “motivation” that Petitioner and Dr. Liu have identified for applying Lee’s teachings to Zhao’s system does not support

creating the proposed system that the Petition has put forth. Rather, Petitioner's and Dr. Liu's illustrations showing how Lee's teachings would be applied is divorced from any possible benefits to Zhao's system. The stated motivation does not match the proposed combination. Rather, the proposed combination appears to be using hindsight in an attempt to combine teachings together in a way that superficially emulates the use of different word line pre-pulse signals described in the '822 Patent.

VII. CONCLUSION

50. For at least the reasons discussed above, I disagree with the arguments raised in the Petition regarding the scope and content of Lee and Zhao as understood by a person ordinary skill in the art, and I disagree that a POSITA would have been motivated to apply Lee's teachings to Zhao's system in the manner described in Ground 3 of the Petition.

51. This declaration represents my opinions that I have formed to date on the specific issues for which I have been asked to opine and based on the material currently available to me. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also, I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

52. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are

believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

APPENDIX A

Steven A. Przybylski

President, Verdande Group, Inc.

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Professional Experience

2003 - Present **President, Verdande Group, Inc**

An inventor, registered patent agent, strong communicator and seasoned technical expert, I provide intellectual property services to a diverse set of clients across the digital electronics spectrum. I provide patent, trade secret, and contract dispute litigation support services, and have extensive experience as a testifying and non-testifying expert in matters before district courts, the PTAB, the ITC, and foreign jurisdictions. I have testified by expert report, deposition, and live testimony on matters of claim construction, infringement, and invalidity, and have assisted in evaluations of potential damages and monetization strategies. With strong written and verbal skills, I provide tutorials to those of both technical and non-technical backgrounds, including judges and attorneys. In addition, I offer pre- and post-transaction portfolio evaluations and due diligence analyses.

I have been retained for these services with regard to:

Computer Systems

Processor design
Processor architecture
Multiprocessing
Graphics systems
Graphics/CUDA processors
Cache memories
Memory systems
Memory modules
Floating point computation
Operating systems
I/O systems
System boot issues

Consumer Electronics

Infotainment systems
Video encoding and decoding
Medical equipment
Embedded systems
Portable electronic systems
User interface design
Wired and wireless networking
Power/energy management
Standards development
Display interconnects
Integrated memories
Digital signal processing
Cloud-based content navigation
and serving

Semiconductors

DRAMs
Flash
SRAMs
Other non-volatile memories
Memory controllers
High-speed interconnects
Signal integrity
2D, 2.5D and 3D packaging
Error detection and correction
Clock distribution techniques
Semiconductor processing
IC and system testing
Computer aided design
FPGAs

2000 – 2003 **Manager, SSM Technologies, LLC.**

I managed, developed and sold a significant patent portfolio relating to DRAMs. Recognizing the intrinsic value of a long-neglected portfolio, I negotiated control of the portfolio and developed a new patent prosecution strategy. I oversaw and participated in the implementation of this strategy, culminating in the issue of a new set of broad method and apparatus claims. I then worked to monetize the portfolio and to maximize return to the inventors and SSM's investors by analyzing the sell/license decision and guiding the stakeholders through the decision-making process. I gathered relevant documentation and analyses, approached likely purchasers, presented interested parties with the collected materials, actively sold the offensive and defensive utility of the portfolio, and orchestrated an auction-style final sales process.

1991 – 2000 **President and Principal Consultant, Verdande Group, Inc**

I have consulted on product strategy, comparative technical analysis, and system-level design in the areas of DRAMs, Flash, SRAMs and other semiconductor memories, computer systems and CPU architecture, and uni- and multi-processor memory hierarchy design. Technical engagements have included serving as memory system architect for Flash and DRAM memory devices and systems. In addition, I offered: general business planning and analysis services to computer and semiconductor companies; intellectual property management, including portfolio evaluation, development and brokering, and litigation support services to IP holders and legal firms; and due-diligence analyses to venture capitalists and securities firms.

My writing and analysis encompasses an extensive range of topics for trade magazines, conferences, and academic journals. As one of the leading independent analysts of the semiconductor memory industry, I wrote (1994) and substantially revised (1996) an 850-page research report entitled *New DRAM Technologies: A Comprehensive Analysis of the New Architectures*, available from the publishers of *The Microprocessor Report*. I have also taught and presented tutorials to both technical and non-technical audiences on subjects including semiconductor memory architecture, memory hierarchy design, and computer systems and CPU architecture. In particular, I have presented over 50 full- and partial-day seminars on these topics to over 2,500 managers, engineers, marketers, and analysts. I have also served on the advisory boards of high-technology start-ups, advising on processor, DRAM and Flash memory trends and general business opportunities.

- 1989 - 1991 **Chief Scientist and Systems Architect, MIPS Computer Systems.**
I played a variety of roles within MIPS, including assistant to the Senior Vice President of Engineering, technical lead for a group of designers that investigated the technical and economic feasibility of developing a companion chip to the R3000 CPU and R3010 FPU, troubleshooter within the High-End Systems Group responsible for taking on any short or long term task that was in need of additional manpower, chief scientist for the group in charge of planning and investigating options for future high-end systems, systems architect for both a new R4000 based symmetrical multi-processor and a low-cost desk-top machine.
- 1990 - 1991 **Consulting Assistant Professor, Dept. of Elect. Eng., Stanford University.**
I designed and taught an advanced graduate level course on cache and memory hierarchy design and supervised the students' research activities. Two groups of students continued their research and ultimately published their efforts under my direction.
- 1989 - 1989 **Postdoctoral Scholar, Department of Electrical Engineering, Stanford University.**
As a postdoctoral scholar, I continued my dissertation research into the analysis of cache behaviour and performance-optimal memory hierarchy design.
- 1984 - 1985 **Computer Architect and Systems Designer, MIPS Computer Systems.**
My main contribution during MIPS' first year was the specification of the architecture and micro-organization of the R2000 VLSI RISC CPU, including the CPU interface and the cache subsystem. I was integrally involved in the implementation of both the CPU and system-level design. My most important role was that of liaison between the VLSI, board-level hardware, compiler and operating system teams.
- 1981 - 1988 **Research Assistant, Department of Electrical Engineering, Stanford University.**
I was a key participant in the MIPS VLSI CPU design team, involved in the design, debugging and testing of the IC design. I also oversaw the development of a prototype CPU board, and subsequently aided in the architectural specification of the MIPS-X VLSI CPU. My dissertation research used analytical and empirical techniques to examine memory hierarchy design from the perspective of optimizing system level performance.

Education

Haas School of Business, University of California at Berkeley, M.B.A. (2000).

Coursework and final project included a combined emphasis on business strategy and financial analysis.

Stanford University, M.S.E.E. (1982), Ph.D. (1988).

Research areas: Computer systems design and VLSI integrated circuit design. Concentrated areas of study spanned the breadth of both electrical engineering and software systems. Topics of extensive coursework included digital systems design, computer architecture, semiconductor devices, error correction codes, control theory, and system software — including user interface design, operating systems, compilers, and I/O systems. Doctoral dissertation title: Performance-Directed Memory Hierarchy Design.

University of Toronto, B.A.Sc. with Honours (1980).

My unique, specially approved course of study within the Engineering Science Programme combined the computer science and electrical engineering degree programs. This provided a broad and deep background in both areas. Coursework and undergraduate thesis covered digital systems design, computer systems, control theory, network analysis, analog circuit design, semiconductor physics, human-computer interfaces, operating systems, compilers, database design, and AI.

Honors and Publications

Awards

Most Influential Paper Award, ACM/IEEE International Symposium on Computer Architecture, 1989, with Mark Horowitz and John Hennessy.

Micro Test-of-Time Award, for one of the ten most influential papers of the first 25 years of the IEEE Micro Symposium, with John Hennessy, Norman Jouppi, Christopher Rowen, Thomas Gross, Forest Baskett, and John Gill. 1994.

Books

S. Przybylski, *New DRAM Technologies*, MicroDesign Resources, 1996, 1994.

S. Przybylski. *Cache and Memory Hierarchy Design: A Performance-Directed Approach*, Morgan Kaufmann, 1990.

J. Hennessy, S. Przybylski. VLSI Processor Design Methodology. Chapter I in *VLSI Electronics, Microstructure Science*, Vol. 14, Einspruch, N. ed., Academic Press, 1986.

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Seminars, Tutorial, Session Chairs

- PC System Architecture Trends, Panel member, 1999 Microprocessor Forum, San Jose, October 1999.
- An Introduction to Semiconductor Memories, A Verdande Group presentation in cooperation with Citibank Inc, Taipei, Taiwan ROC, June 1998.
- Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar. Presented more than 10 times to corporations between September 1997 and October 1999
- The New DRAMs for Main Memory and Graphics, Full day Seminar, Verdande Group Seminar Series, Portland, Austin, San Jose, and Boston, September 1997.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar, Verdande Group Seminar Series, Portland, Austin, San Jose, and Boston, September 1997.

Sorting Out the New DRAMs, Half-Day Tutorial, Hot Chips IX, August 1997.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar, Presented at 24th Annual International Symposium on Computer Architecture, May 1997.

The New DRAMs For Main Memory and Graphics, Full day tutorial, 1997 PC Tech Forum, May 1997.

The New DRAM Architectures, DRAM Tutorial, 1996 ISSCC, February 1997.

Selecting the Best Memory Technology for PCs and Graphics, Full day tutorial, 1996 PC Tech Forum, May 1996.

The Changing DRAM and VRAM Marketplace, Full day tutorial, Presented more than 20 times to corporations between September 1995 and October 1999.

The Changing DRAM and VRAM Marketplace, Full day tutorial, Sponsored by Nikkei Microdevices, Tokyo, Japan, March 1996.

The Changing DRAM and VRAM Marketplace, Full day tutorial, 1995 Microprocessor Forum, October 1995.

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New Graphics Memories. Lecture. WinHEC, March 1995.

Emerging DRAM Architectures. Lecture. WinHEC, February 1994.

New DRAM Organizations. Session chair. Proceedings of COMPCON, Spring 1994.

Computer architecture and organization. Half-day tutorial. OCATE/Oregon State University, August 18, 1993.

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Computer Architecture. Full day tutorial with Normal Jouppi and Mark Horowitz. International Solid State Circuits Conference, February 1993.

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Patents

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C. Hansen, S. Przybylski, T. Riordan, L. Weber. *Dual Byte Order Computer Architecture*. Patent No. 4,959,779, September 25, 1990.

Foreign counterparts of the above.

Additional Information

Registered US Patent Agent, 1997 - present

Professional Societies: IEEE, ACM

Citizenship: Canadian with U.S. resident alien status