

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00795

Patent 11,501,822

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Declaration of Dr. Steven Przybylski (“Przybylski”)
Ex. 2002	U.S. Pat. No. 11,081,164 (“the ’164 patent”)
Ex. 2003	Reserved
Ex. 2004	U.S. Pat. No. 10,700,157 (“Chen”)
Ex. 2005	U.S. Pub. 2011/0194351 (“Kim”)
Exs. 2006-09	Reserved
Ex. 2010	Declaration of Jonathan Bradford

LIST OF ABBREVIATIONS

Abbreviation	Term
'144	U.S. Pat. No. 11,081,164 (Ex. 2002)
'822	U.S. Pat. No. 11,501,822 (Ex. 1001)
Challenged Claims	'822, Claims 1-9 and 11-19
Chen	U.S. Pat. No. 10,770,157 (Ex. 2004)
Kim	U.S. Pub. No. 2011/0194351 (Ex. 2005)
Liu	Declaration of Dr. David Kuan-Yu Liu (Ex. 1003)
Lee	U.S. Pat. No. 10,121,529 (Ex. 1004)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,501,822 (IPR2024-00795, Paper 1)
Parallel District Court Litigation	<i>Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Przybylski	Declaration of Dr. Steven A. Przybylski (Ex. 2001)
Yang	U.S. Pat. No. 10,726,920 (Ex. 1010)
Zhao	U.S. Pat. No. 10,643,718 (Ex. 1005)

Pursuant to §42.107,¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to any Challenged Claim. Portions of this Preliminary Response are supported by the declaration of Dr. Steven A. Przybylski. *See* Ex. 2001 ("Przybylski"), ¶¶ 1-27.

I. INTRODUCTION

U.S. Patent No. 11,501,822 ("’822," Ex. 1001) is directed to a novel pre-charging process for applying signals to word lines of a three-dimensional non-volatile flash memory device to mitigate the effects of "programming disturb," which is when the programmed state of a memory cell is inadvertently altered by a programming operation performed on adjacent memory cells, caused by electrons trapped in the vertical channels of the memory device. The prior art at the time of filing of the ’822 sought to address programming disturb by employing a pre-charging process, however methods at the time had drawbacks on memory device programming speed and increased the risk of transistor breakdown.

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

The '822 introduced a novel pre-charging process that reduced programming disturb without compromising device-level performance. The new pre-charging process taught by the '822 and recited in the claims is characterized by several features not found in or rendered obvious by the prior art, including the application of three pre-pulse signals of incrementally increasing voltages levels to three different groups of word lines during a pre-charge period. By virtue of applying incrementally increasing pulse signals, the overall duration of the pre-charging process is kept short and the voltage levels closest to the selected word line are minimized, which limits adverse effects on the programming speed of the memory device and improves the longevity of the device circuitry. Thereby, the '822 invention overcomes the drawbacks of the prior art. *See, e.g., '822, 1:20-48.*

Institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to any of the Challenged Claims.

Petitioner does not assert that any of the cited references anticipate the independent Challenged Claims, and seemingly concedes that the art does not explicitly disclose the use of three “word line pre-pulse signals” with the incrementally increasing voltage levels required by the claims. *See Pet., 6.* Instead, Petitioner raises obviousness based on a mix of unsupported assumptions, conclusory testimony from Dr. Liu, and hindsight rationalizations.

First, Petitioner’s ground based on Lee fails because Lee does not disclose or render obvious a first, second, and third “word line pre-pulse signal” as required by the Challenged Claims. As properly construed, a “word line pre-pulse signal” is a “pulse signal to prepare word lines for a programming step.” But Petitioner incorrectly relies on disclosures from Lee directed to applying different kinds of voltage signals, *i.e.*, “pre-bias voltages,” that are not disclosed to be pulses, and improperly relies on incorrect inferences and the conclusory hindsight-based testimony from Dr. Liu to suggest that it would be obvious to implement Lee’s “pre-bias voltages” as pulses.

Second, Petitioner’s arguments based on Zhao fail because Zhao does not disclose or render obvious a first, second, and third “word line pre-pulse signal” as required by the Challenged Claims. Again, the claimed “word line pre-pulse signal” must be a pulse, but Petitioner incorrectly relies on Zhao’s application of a constant, flat voltage that remains unchanged throughout the purported pre-charge period, and relies on a misreading of Zhao to incorrectly suggest that it would have been obvious to replace that flat voltage with a word line pre-pulse signal.

Third, Petitioner relies on a purported combination of Zhao and Lee, but fails to show that a POSITA would have been motivated to combine Zhao with Lee for at least the reason that the teachings Petitioner attempts to borrow from Lee would fail to provide the alleged benefits when applied to Zhao’s system. At most, the

purported combination tries to “reconstruct the applicant’s invention only with the benefit of hindsight” and thus fails to render the claims obvious. *See Netflix, Inc. v. DivX, LLC*, 80 F.4th 1352, 1359 (Fed. Cir. 2023).

Fourth, Petitioner’s arguments based on Yang fail because it does not disclose or render obvious three distinct “word line pre-pulse signals” applied to three distinct groups of word lines that have incrementally increasing “voltage levels” as required by the Challenged Claims.

II. THE CLAIMED INVENTION OF THE ’822 PATENT

The claimed invention of the ’822 is directed to an improved three-dimensional (“3D”) non-volatile flash memory device that provides a novel approach for mitigating programming disturb. ’822, 1:15-19, 2:56-58.

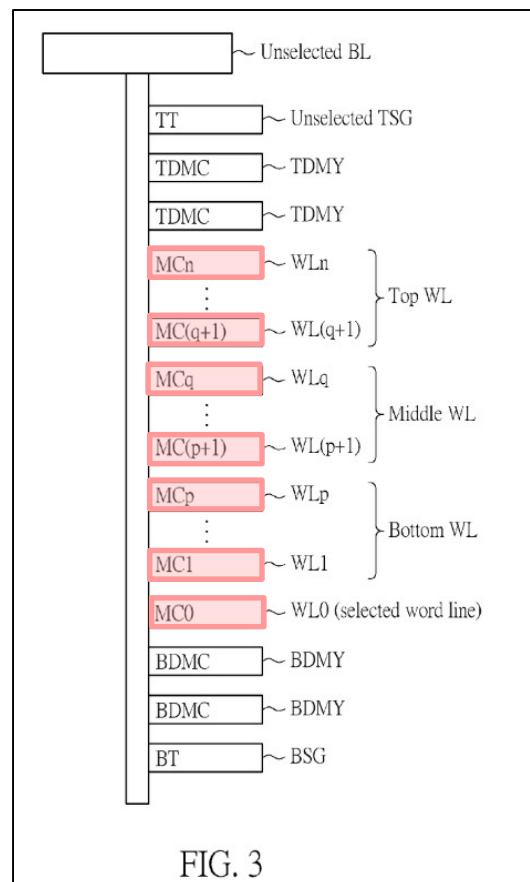
3D NAND flash memory technology architecture has been developed to vertically stack memory cells across multiple layers to increase bit density and storage capacity as compared to traditional NAND memory. ’822, 1:29-32. However, as the number of vertical layers and bit density increases, the effects of programming (or program) disturb are exacerbated. ’822, 1:32-33. As was understood in the art, programming disturb is a phenomenon in non-volatile memory devices when the programmed state of a memory cell is inadvertently altered as a result of a programming operation performed on adjacent, selected memory cells,

causing data corruption and reducing the reliability and integrity of stored data. *See, e.g.,* Yang, 2:35-41 (describing “program disturb” in general).

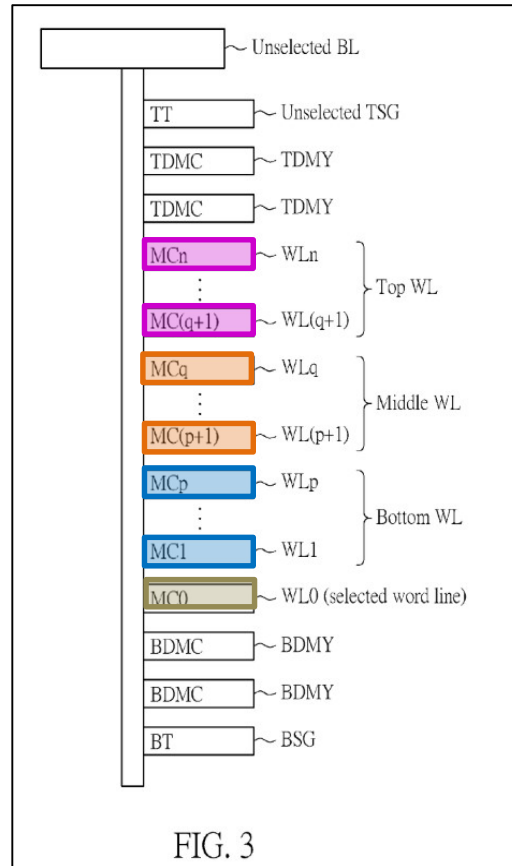
To help mitigate programming disturb, a pre-charge operation is performed to remove boosting charges (electrons) from unselected memory strings prior to a programming operation, for example, by applying an appropriate pre-pulse signal to unselected word lines. '822, 1:34-38. However, as more layers are added to the memory device architecture, it becomes increasingly difficult for pre-charge operations to remove electrons from the bottom-most layers of the device. '822, 1:39-41. Traditional systems attempted to compensate for this reduced effect by increasing the duration of pre-pulse signals applied to the unselected word lines, or by increasing the voltage levels used during pre-charge operation, but such methods have significant drawbacks that adversely effect data programming speeds and increase the risk of transistor breakdown. '822, 1:41-48. By comparison, the inventors of the '822 developed an improved pre-charging operation to mitigate the effects of programming disturb in memory devices, while avoiding the drawbacks associated with traditional methods. '822, 1:48-55.

The claimed invention of the '822 mitigates program disturb in high-layer non-volatile memory devices by introducing a novel method of applying multiple pre-pulse signals to memory device word lines, with each one having a different voltage level. Specifically, the '822 is directed to a non-voltage memory device that

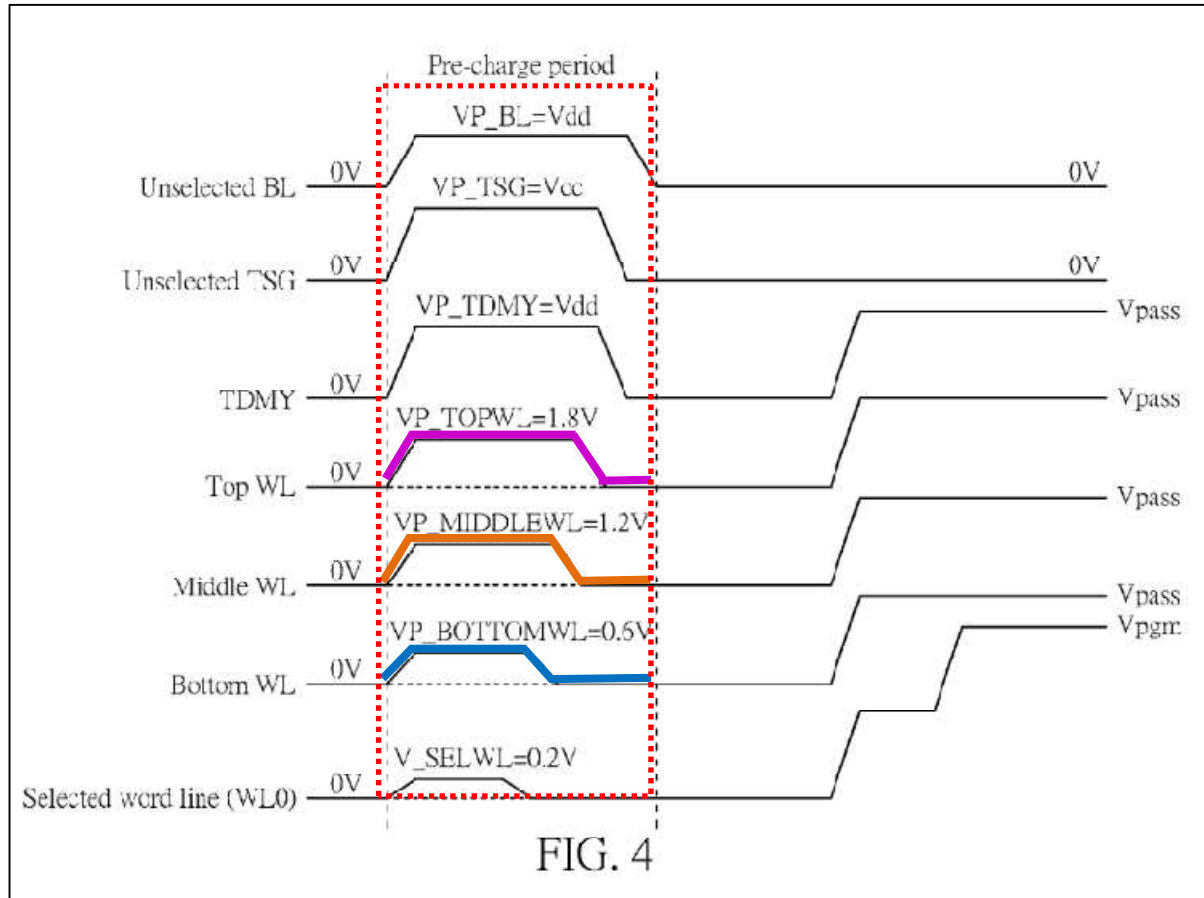
has a plurality of memory strings, each memory string including: a top select gate transistor (“TSG”), at least one top dummy memory cell (“TDMY”) and one bottom dummy memory cell (“BDMY”), a plurality of memory cells that are “configured to store data,” bottom select transistor (“BSG”), and a bit line (“BL”). ’822, 3:6-9, 3:18-19. The memory cells are “disposed sequentially ... between the top dummy memory cell and the bottom dummy memory cell.” ’822, 3:23-26. **Word lines (“WL”)** are connected to the memory cells, each with a separate connection, and “disposed sequentially ... between the top dummy word line TDMY and the bottom dummy word line BDMY.” ’822, 3:20-23, 3:26-29.



The '822 invention uses a “control circuit” to apply “word line pre-pulse signals” to the word lines “disposed between the selected word line and the top dummy word line TDMY (or the top select gate TSG)” “during a pre-charge period” that occurs “before programming.” '822, 3:43-46, 3:55-59. That is, the '822 teaches applying the pre-charging operation to word lines *above* the selected word line, closer to the TDMY or TSG. In a separate step, the control circuitry applies a “dummy word line pre-pulse signal” to “top dummy word lines TDMY” and “bottom dummy word lines BDMY.” '822, 3:59-65. For example, as shown in Fig. 3 below, word lines disposed between the **selected word line** and TDMY (or TSG) may be “divided into multiple groups of ... word lines,” with each group including “at least one word line”: a “**first group of word lines**” including word line WL1 through word line WLp, a “**second group of word lines**” including word line WL(p+1) through word line WLq, and a “**third group of word lines**” including word line WL(q+1) through word line WLn. '822, 4:66-5:2, 5:18-34.



During the “pre-charge period,” three different word line pre-pulse signals with different voltage levels are applied to these three groups of word lines. For example, in the embodiment illustrated in Fig. 4, a **first word line pre-pulse signal** VP_BOTTOMWL is applied to the first group of word lines (“Bottom WL”), a **second word line pre-pulse signal** VP_MIDDLEWL is applied to the second group of word lines (“Middle WL”), and a **third word line pre-pulse signal** VP_TOPWL is applied to the third group of word lines (“Top WL”) during the **pre-charge period**. ’822, 5:50-55.



As shown in Fig. 4, the voltage level of the word line pre-pulse signals is incremental, with the VP_BOTTOMWL signal having the lowest voltage level (0.6 volts), VP_MIDDLEWL having an intermediary voltage level (1.2 volts), and VP_TOPWL having the highest voltage level (1.8 volts). '822, 5:65-6:4. In this embodiment, a top dummy word line pre-pulse signal, VP_TDMY, applied to dummy word lines is a separate voltage level (Vdd) that is greater than the voltage levels for VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL. '822, 6:4-8. Similarly, the pre-pulse signal for the selected word line, V_SELWL, is a voltage level (0.2 volts) that is

lower than the voltage levels for VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL. '822, Fig. 4, 5:62-64.

By supplying different pre-pulse voltages to the word lines disposed between the selected word line and the top select gate, the channel potential gradient is enhanced, which favorably influences the distribution and movement of channel-trapped electrons and prevents electrons from accelerating into unselected memory cells during a programming operation. *See* '822, 7:37-47. And by using multiple pre-pulse signals to create a channel potential gradient, the '822 invention limits the overall duration of the pre-charge period and reduce the voltage levels applied during the pre-charge period, resulting in a faster programming time and less risk of transistor breakdown phenomenon as compared to conventional systems. *See* '822, 1:41-48. Accordingly, the claimed pre-charging process of the '822 improved over the prior pre-charging methods.

Independent Claim 1 of the '822 is an apparatus claim directed to aspects of the above-described invention:

[1.pre] A memory device, comprising:

[1.a] a plurality of memory strings;

[1.b] a bit line connected to a first memory string of the plurality of memory strings;

[1.c] a select gate line connected to the first memory string of the plurality of memory strings;

[1.d] a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string; and

[1.e] a control circuit configured to:

[1.e.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period;

[1.e.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[1.e.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,

[1.e.4] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

Independent Claim 11 of the '822 is a method claim directed to the same aspects of the above-described invention:

[11.pre] A method of controlling a memory device, the memory device comprising a plurality of memory strings, a bit line connected to a first memory string of the plurality of memory strings, a select gate line connected the first memory string of the plurality of memory strings, a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string, the method comprising:

[11.a] applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period;

[11.b] applying a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during the pre-charge period;

[11.c] applying a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[11.d] applying a third word line pre-pulse signal of the plurality of word line pre-pulse signals to a third group of the plurality of word lines during the pre-charge period;

[11.e] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

III. FILE HISTORY

The '822 claims remain patentable over the prior art for at least the same reason identified during prosecution of the '822 and its parent application. As discussed further below in Section VI, the prior art does not disclose or render obvious the claimed process of the '822 entailing “apply[ing] a [first/second/third] word line pre-pulse signal ... to a [first/second/third] group of the plurality of word lines during a pre-charge period,” wherein each signal has an incrementally increasing “voltage level” such that the “voltage level” of the “first word line pre-pulse signal” is the lowest and the “voltage level” on the “third word line pre-pulse signal” is the greatest. Claims directed to this and substantively similar limitations were allowed in the '822 family after extensive prosecution and consideration of numerous prior art references.

A. '164 (Parent) File History

The '822, corresponding to U.S. App. 16/709,944, is a continuation of and terminally disclaimed over U.S. Pat. No. 11,081,164 (“the '164 patent,” Ex. 2003). Ex. 1002 (the '822 File History (“'822FH”)), 12, 82-83. The claims of the '164, like the claims of the '822, require the step of “apply[ing] a [first/second/third] word line pre-pulse signal ... to a [first/second/third] group of the plurality of word lines” “during a pre-charge period,” where the “voltage level” of the “pre-pulse signal[s]” incrementally increase from that applied on the “first group” (lowest “voltage level”) to the “second group,” and from the “second group” to the “third group” (greatest “voltage level”), as shown in the table below.

'822 Claim 1	'164 Claim 1
1. A memory device, comprising: ... a control circuit configured to:	1. A non-volatile memory device, comprising: ... a second control circuit configured to apply a word line signal to a selected word line of the plurality of word lines and apply a plurality of word line pre-pulse signals to word lines disposed between the select gate line and the selected word line during the pre-charge period, wherein voltage levels of the plurality of word line pre-pulse signals are incremental;
apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the	wherein the second control circuit is configured to apply a first word line pre-pulse signal of the plurality of word line pre-pulse signal to a first

<p>plurality of word lines during a pre-charge period;</p>	<p>group of the plurality of word lines disposed adjacent to the selected word line and disposed between the selected word line and the select gate line during the pre-charge period,</p>
<p>apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and</p>	<p>apply a second word line pre-pulse signal of the plurality of word line pre-pulse signal to a second group of the plurality of word lines disposed adjacent to the first group of the plurality of word lines and disposed between the first group of the plurality of word line and the select gate line during the pre-charge period, and</p>
<p>apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,</p>	<p>apply a third word line pre-pulse signal of the plurality of word line pre-pulse signal to a third second group of the plurality of word lines disposed adjacent to the second group of the plurality of word lines and between the second group of the plurality of word lines and the select gate line during the pre-charge period,</p>
<p>wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and</p>	<p>wherein a voltage level of the second word line pre-pulse signal is greater than a voltage level of the first word line pre-pulse signal and</p>
<p>a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.</p>	<p>a voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal.</p>

Applicant attained allowance of the '164 after explaining in response to an Office Action dated January 15, 2021 that the cited references of record—U.S. Pat. No. 10,700,157 (“Chen,” Ex. 2004) and U.S. Pub. 2011/0194351 (“Kim,” Ex. 2005)—failed to disclose the newly-added limitation reciting: “apply[ing] a [first/second/third] word line pre-pulse signal ... to a [first/second/third] group of the plurality of word lines ... during the pre-charge period,” “wherein a voltage level of the second word line pre-pulse signal is greater than a voltage level of the first word line pre-pulse signal and a voltage level of the third word line pre-pulse signal is greater than the voltage level of the second word line pre-pulse signal.” Ex. 1015 ('164 File History (“'164FH”)), 123-124.

In a Notice of Allowance dated April 5, 2021, the Examiner found all pending claims allowable. *Id.*, 131. In the statement for the reasons for allowance, the Examiner found that the claim limitations taken as a whole were allowable over the prior art of record, stating that “[t]he prior arts fail to teach or fairly suggest” claim 1 of the '164 patent. *Id.*, 131-133.

B. '822 File History

The '822 is a continuation of the '164 and, as noted above, the '822 claims recite similar limitations to those that formed the basis for the '164 allowance.

In an Office Action dated December 30, 2021, the Examiner rejected prosecution claims 2 and 12 on the ground of obviousness-type double patenting

over claims 1 and 9 of the '164 parent patent. Ex. 1002 ('822FH), 62-65. The Applicant overcame the rejection by filing a terminal disclaimer over the '164, and the Examiner subsequently allowed all pending claims. *See id.*, 82-83, 107, 174.

In the statement for the reasons for allowance, the Examiner identified several key limitations, stating that “[t]he prior arts fail to teach or fairly suggest” claim 1 of the '822 patent. *Id.*, 276.

IV. CLAIM CONSTRUCTION

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” §42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art (“POSITA”). *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A POSITA ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant extrinsic evidence, although the claims and patent specification are the primary sources for construing claims. *Id.*, 1314-16.

Petitioner has not identified any terms for construction, and the parties have not yet exchanged proposed claim constructions in the parallel district court proceeding. *See Pet.*, 18. Other than the term “word line pre-pulse signal,” Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the challenged claims for the purposes of institution.

Patent Owner, however, reserves the right to modify its proposed construction and to raise further claim construction issues if the Board institutes IPR, and to raise claim construction issues in the underlying district court proceedings.

A. “Word Line Pre-Pulse Signal”

The term “word line pre-pulse signal” should be construed as a “pulse signal to prepare word lines for a programming step.” That construction is supported by the intrinsic record, including the ’822 claims and specification.

First, the claims support Patent Owner’s construction. For example, claim 1 recites applying a “word line pre-pulse signal” during a “pre-charge period,” which the specification explains is “before programming.” ’822, 3:43 (“[d]uring a pre-charge period (before programming)”). Thus, the pre-pulse signal prepares the word line before the programming step. In addition, the claims confirm that the “pre-pulse signal” is in the form of a pulse. For example, claim 20 recites that the “pulse duration of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal,” and that the “pulse duration of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.” *Id.*, 10:20-24.

The specification further confirms that a “word line pre-pulse signal” refers to a pulse signal applied to word lines in preparation for a programming step. For example, the specification describes “word line pre-pulse signals” as either “positive pulse signals” (*id.*, 6:61-66) or “negative pulse signals” (*id.*, 6:11-19) that each have

an associated “pulse duration” within the pre-charge period (*id.*, 7:19-36). *See also id.*, 1:15-19 (“applying word line pre-pulse signals” is for “reducing programming disturb”), 3:43-46 (the “pre-charge period” is “before programming”), Figs. 4-5 (depicting the word line pre-pulse signals as pulses).

Petitioner seemingly agrees with Patent Owner’s construction, recognizing that the claimed “word-line pre-pulse signal” must be a “pulse” applied to word lines in preparation for a subsequent programming step. *See, e.g.*, Pet., 2 (arguing that the art, “just like the ’822 patent,” teaches “memories that apply three different voltage pulses to three different groups of word lines during a pre-charge period”), 38-39 (arguing why it would have been obvious for the signals Petitioner maps to the claimed “word-line pre-pulse signal” to be implemented in the form of pulses), 51 (characterizing the signals Petitioner maps to the claimed “word line pre-pulse signal[s]” as “pre-charge voltage pulses”).

Thus, as supported by the claims and the specification, and confirmed by Petitioner, the term “word line pre-pulse signal” should be construed as a “pulse signal to prepare word lines for a programming step.”

Furthermore, a “pulse” as used in the ’822 patent does not encompass a flat voltage signal, nor has the Petitioner suggested that it would. Indeed, the ’822 specification and the claims confirm that each “word line pre-pulse signal” has at least a “voltage level” and a “pulse duration.” *See* ’822 Claims 1, 11 (describing “a

voltage level of the ... word line pre-pulse signal”), Claim 20 (describing “a pulse duration of the third word line pre-pulse signal”); *see also id.*, 3:66-4:22 (describing “voltage levels” of the “word line pre-pulse signals”), 7:19-36 (describing “pulse durations (signal lengths) of the word line pre-pulse signals”), Figs. 4-5 (depicting word line pre-pulse signals). Thus, as confirmed by the claims and specification, a “pulse” does not include a flat voltage, for which the “pulse duration” and “voltage level” would be undefined. For purposes of resolving the arguments raised in this Preliminary Response, the Board need not determine the full scope of a “pulse.” The Board is required to construe terms “only to the extent necessary to resolve the controversy.” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

V. BACKGROUND OF THE ASSERTED PRIOR ART

A. U.S. Pat. No. 10,121,529 (“Lee”) (Ex. 1004)

Petitioner does not contend that Lee anticipates the Challenged Claims, and instead argues only that it renders obvious certain claims, including the independent Challenged Claims. Pet., 6, 26-41. Lee is purportedly directed to “a semiconductor memory device configured to mitigate a program disturb phenomenon, and a method of operating the semiconductor memory device.” Lee, 1:53-56; *see also* Lee 7:37-58. However, the ’822 and Lee employ disparate techniques for addressing program disturb. The ’822 mitigates program disturb resulting from “boosting charges” by using pre-pulse signals to create a “channel potential gradient” during a pre-charge

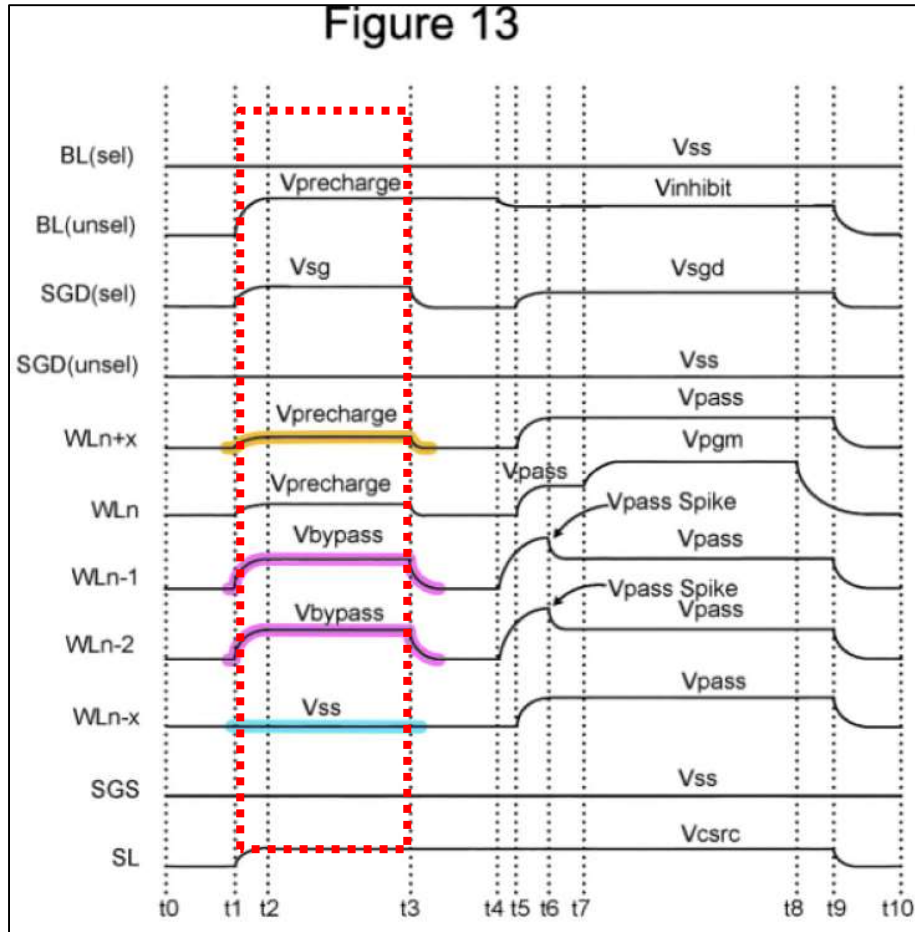
period, thus removing unwanted charge. *See* '822, 1:20-48. By comparison, Lee seeks to create a more “uniformly formed” charge throughout the device by compensating the “resistance component between the source select transistor and the drain select transistor.” Lee, 7:58-62, 8:25-52. *See* Przybylski, ¶¶ 35-37.

To create a uniform level of charge, Lee describes applying “different pre-bias voltages to the respective word line groups” along the entire length of the memory string based on their relative positions within the string. *See* Lee, 2:63-3:7, 8:3-17. Specifically, Lee discloses that “the closer a word line group to which a word line belongs is to the drain select transistor, the higher a pre-bias voltage to be applied to the word line may be,” turning on all the memory cells in the memory string in the process. Lee, 8:18-52. But Lee does not disclose any details regarding the “pre-bias voltages” beyond its statements that “different” voltages are used with some “higher” than others. Lee, 7:58-62, 8:65-9:6. Indeed, Lee does not disclose any waveform or timing characteristics of the voltages applied within its system, does not disclose that the “pre-bias” voltage (or any voltage) would be implemented as a “pulse,” and does not otherwise render obvious that the “pre-bias” voltage would be implemented as “word line pulse signal” as required by the Challenged Claims. *See* Przybylski, ¶¶ 38-39.

B. U.S. Pat. No. 10,643,718 (“Zhao”) (Ex. 1005)

Petitioner does not contend that Zhao anticipates the Challenged Claims, and instead argues only that that Zhao (Ground 2), or alternately the combination of Zhao and Lee (Ground 3), renders obvious certain claims, including the independent Challenged Claims. Pet., 44-71. Zhao describes “strings” of memory cells, each of which is connected to a corresponding word line. Zhao, 6:34-46; *see also id.* 9:10-18, 11:53-12:13, Fig. 4G. At any given time, one memory cell is “selected” for programing. *See id.* 12:14-41, 27:30-48. Zhao discloses three different possible “countermeasures ... to open the channel from one side of a selected word line to the other side of the selected word line” in order to combat certain types of program disturb. *Id.*, 2:10-26. Zhao describes these as “purging ... the already programmed side of the channel” (*id.* 2:27-49), “applying a voltage spike one or more already programmed unselected word lines” (*id.* 2:50-3:4), and “delaying the ramping down of the voltages ... at the conclusion of a program verify process” (*id.* 3:5:24). *See* Przybylski, ¶¶ 28-30.

As depicted in Fig. 13, Zhao illustrates these countermeasures using different voltages applied to different wordlines. Starting at time t_0 , “all the depicted signals are at ... 0 volts (V_{ss}),” and the time period “from **t_1 - t_3 corresponds to pre-charging.**” Zhao 22:34-41. *See* Przybylski, ¶ 31.



Like Lee, Zhao fails to teach or otherwise render obvious the use of three “pre-pulse signals” during a “pre-charge period” as required by the independent claims of the ’822. Petitioner incorrectly attempts to characterize portions of **Vss**, **Vprecharge**, and **Vbypass** waveforms as equivalent to the claimed “pre-pulse signals ... during a pre-charge period” recited by the independent claims of the ’822.² See Pet., 23. Setting aside that the waveforms identified by Petitioner

² For convenience, Petitioner’s annotations for **Vss**, **Vprecharge**, and **Vbypass** are reproduced above.

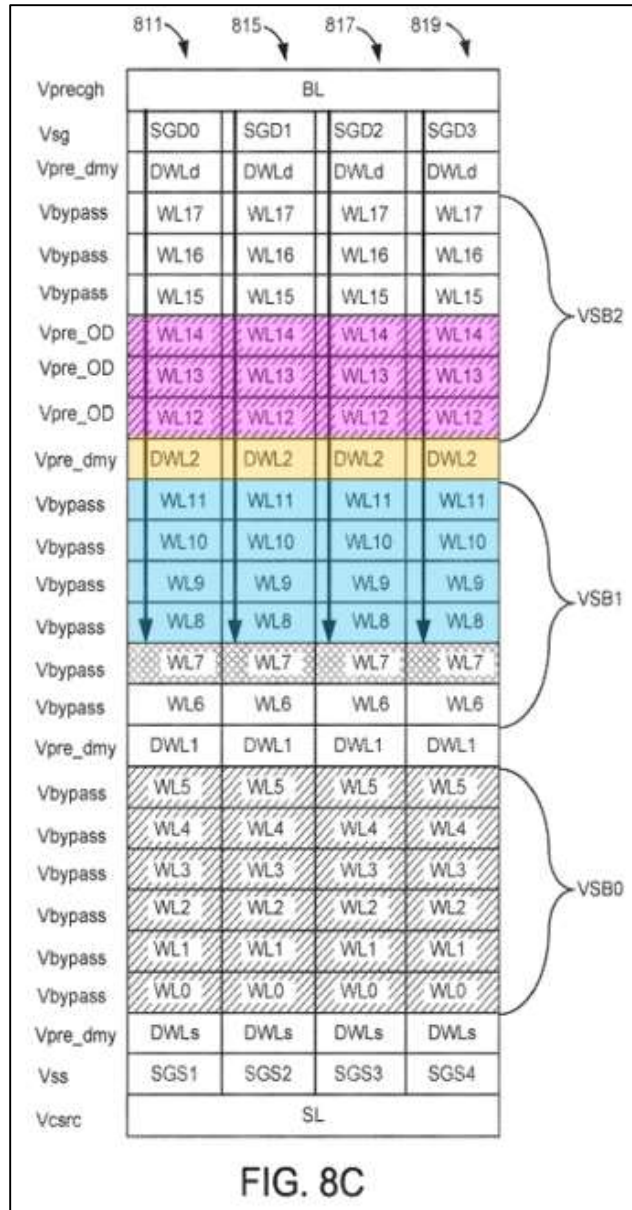
extend beyond Zhao's "pre-charging" period, the flat 0 volts (**V_{ss}**) signal identified by Petitioner as being applied to word line WLn-x does not constitute a "word line pre-pulse signal ... during a pre-charge period" as properly construed. Indeed, Petitioner seemingly concedes that a flat signal would not satisfy the claim language, and instead mischaracterizes Zhao as disclosing some other "low" voltage being applied in lieu of the flat signal shown in Figure 13. *See* Pet., 51. But Zhao does not disclose or otherwise render obvious a "word line pre-pulse signal" being applied to those word lines. Rather, Zhao explicitly teaches that the word lines "remain" at a fixed value throughout the relevant time period. *See* Zhao, 23:7-10. Accordingly, Zhao fails to disclose a "word line pre-pulse signal" being applied to word line WLn-x in the purported pre-charge period, and Petitioner has similarly failed to show that it would have been otherwise obvious to implement Zhao's system using three distinct "word line pre-pulse signals" as required by the Challenged Claims. *See* Przybylski, ¶¶ 32-34.

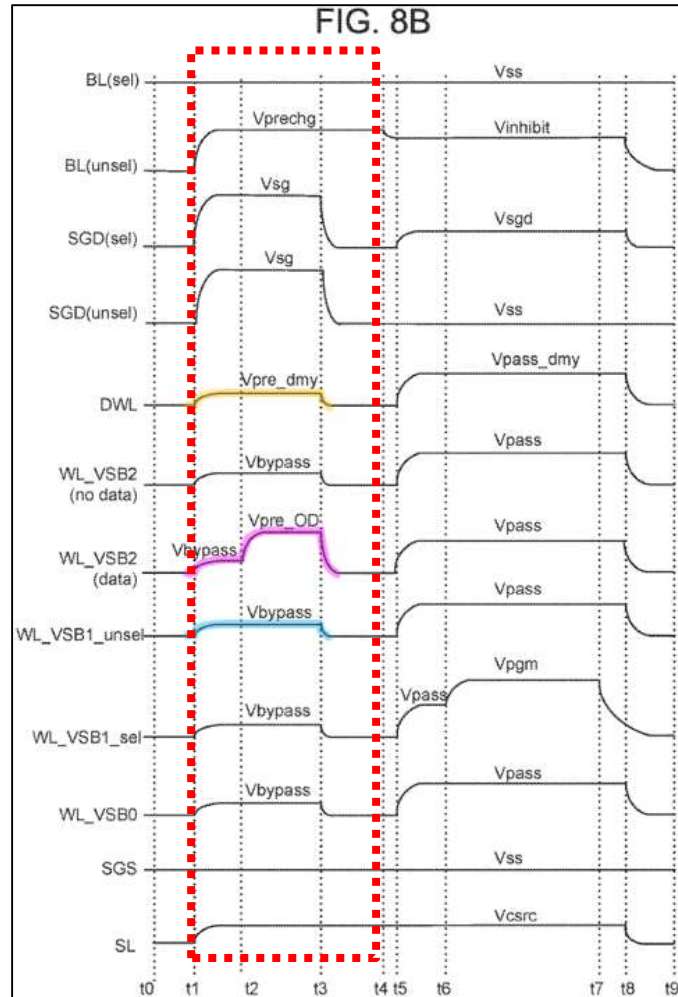
C. U.S. Pat. No. 10,726,920 ("Yang") (Ex. 1010)

Petitioner does not contend that Yang anticipates the Challenged Claims, and again argues only that Yang renders obvious certain claims, including the independent Challenged Claims. Pet., 71-89. Yang purports to address the problem of program disturb in memory cells ("unselected memory cells") surrounding other memory cells that are to receive programming ("selected memory cells"). Yang,

Abstract, 2:35-41. Yang purportedly does this by applying “boosting voltages” to the unselected memory cells before a programming operation on the selected memory cell, so that the unselected memory cell reaches “sufficient voltage during the programming phase” such that “the differential between the channel voltage (of the unselected memory cell) and the ... control gate of [the] unselected memory cell[] will be too small to allow for programming of the unselected memory cell.” Yang, 2:42-62- 25:65-26:3.

Yang describes a binary choice where “during a pre-charge phase of a programming operation, an overdrive voltage is applied to some memory cells and a bypass voltage is applied to other memory cells.” Yang 3:28-31. For example, as depicted in Figs. 8B and 8C, Yang teaches: (1) an **“overdrive voltage” (“V_{pre_OD}”)** is applied to word lines of “programmed” memory cells, and (2) a **“bypass voltage” (“V_{bypass}”)** is applied to “not yet programmed” memory cells during the **“pre-charge phase”** depicted at “times t1-t4.” Yang, Figs. 8B-C, 23:19-25, 24:1-17, 24:28-46, 25:9-28. Yang also discloses a **“dummy pre-charge voltage” (“V_{pre_dmy}”)** that is applied to a “dummy” memory cell used to “electrically isolate” sets of memory cells within the string. *See* Yang, 12:35-43, 24:18-27.





Petitioner attempts to characterize portions of **Vbypass**, **Vpre_dmy**, and **Vpre_OD** as equivalent to the claimed “[first/second/third] word line pre-pulse signals” applied to a “[first/second/third] group of plurality of word lines.” *See* Pet. at 23-26, 80-82.³ But Petitioner’s argument fails to show or otherwise render obvious three distinct “word-line pre-pulse signal” being applied to three distinct groups of word lines, or

³ For convenience, Petitioner’s annotations for **Vbypass**, **Vpre_dmy**, and **Vpre_OD** have been reproduced above.

that the relative voltage levels of the purported “word-line pre-pulse signals” are satisfied by Petitioner’s proposed claim mapping.

**VI. PETITIONER FAILS TO ESTABLISH A REASONABLE
LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO
THE CHALLENGED CLAIMS**

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claims because Petitioner has failed to show that the cited references disclose the steps recited in each of the independent Challenged Claims: “apply[ing] a [first/second/third] word line pre-pulse signal ... to a [first/second/third] group of the plurality of words lines during a pre-charge period,” wherein the “voltage level” of the “second word line pre-pulse signal is greater than that of the first word line pre-pulse signal” and the “voltage level” of the “third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.” As explained below, Petitioner cites to three references—Lee, Zhao, and Yang—and asserts that each one individually, or Zhao and Lee in combination, show these features. Each of Petitioner’s arguments fails.

First, Lee does not disclose or render obvious a “word line pre-pulse signal.” As properly construed, a “word line pre-pulse signal” is a “pulse signal to prepare word lines for a programming step,” but the Petition incorrectly relies on disclosures from Lee directed to applying different kinds of voltage signals—“pre-bias voltages”—that are nowhere disclosed to be pulses. *Second*, Zhao does not disclose

or render obvious a “first word line pre-pulse signal” because the Petition incorrectly relies on a flat voltage signal that remains fixed at a single value before, during, and throughout the relevant time period, which is not a “pulse” as properly construed, or indeed under any possible meaning of the term. *Third*, Petitioner fails to show that a POSITA would have been motivated to combine Zhao with Lee for at least the reason that the teachings that Petitioner attempts to borrow from Lee would provide no benefits when applied to Zhao’s system, leaving impermissible hindsight as the only rationale for the purported combination. *Fourth*, Yang does not disclose or render obvious three distinct “word line pre-pulse signals” applied to three distinct groups of word lines that have incrementally increasing “voltage levels” as required by the claims.

A. Ground 1: Lee Does Not Disclose or Render Obvious a “First Word Line Pre-Pulse Signal of a Plurality of Word Line Pre-Pulse Signals,” “Second Word Line Pre-Pulse Signal of a Plurality of Word Line Pre-Pulse Signals,” and “Third Word-Line Pre-Pulse Signal of a Plurality of Word Line Pre-Pulse Signals” Applied “During a Pre-Charge Period”

Lee does not disclose or otherwise render obvious limitations [1.e.1]-[1.e.3] and [11.b]-[11.d] because Lee’s “pre-bias” voltages (*i.e.*, the purported “word line pre-pulse signals” identified by Petitioner) are not “word line pulse signals” as required by the ’822 Patent. Pet., 26-44. As properly construed, a “word line pre-pulse signal” is a “pulse signal to prepare word lines for a programming step.” See §IV. Lee, however, fails to disclose that the purported “word line pre-pulse signals”

are pulses, and Petitioner’s assertion that a POSITA would have found it obvious for these voltages to be “supplied in the form of a ‘pulse’” is based on nothing more than improper inferences and conclusory expert testimony that conflates the *programming* voltages used to set memory cell values with the claimed *pre-pulse* (or *pre-charge*) signals applied during a pre-charge period. Pet., 37-38.

Claim 1 recites a control circuit configured to “**apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines** during a pre-charge period” (Element [1.e.1]); “**apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines** during the pre-charge period” (Element [1.e.2]); and “**apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines** during the pre-charge period” (Element [1.e.3]). Analogous limitations are found in Elements [11.b]-[11.d] of independent claim 11, and are common to each of the Challenged Claims. As discussed in Section IV, a “word line pre-pulse signal” is a “pulse signal to prepare word lines for a programming step.”

As explained by the ’822, the claimed approach improves over conventional approaches by using multiple pre-pulse signals to “enhance” the “channel potential gradient ... thus enhancing the pre-charge effect of the unselected bit line and reducing programming disturb.” ’822, 4:39-59, 7:37-47; *see also id.*, 1:41-44

(describing that the invention avoids the need for using increased voltages or extended data programming times). In contrast, Lee seeks to create a “uniformly formed” charge by compensating the “resistance component between the source select transistor and the drain select transistor.” Lee, 7:58-62, 8:25-52.

Petitioner incorrectly argues that the “pre-bias” voltages that Lee uses to achieve a uniform charge level render obvious the claimed “pre-pulse signals ... during a pre-charge period” recited by claims 1 and 11 of the ’822, despite Lee failing to disclose that the “pre-bias” voltages (or that any other voltages) are implemented as a “pulse” as required by the claims. Indeed, Petitioner seemingly concedes that Lee does not explicitly disclose the use of “word line pre-pulse signals,” and instead draws unsupported, incorrect inferences and relies on Dr. Liu’s conclusory testimony to argue that the use of “word line pre-pulse signals” was nonetheless obvious. Pet., 38-39.

Petitioner presents two flawed arguments for why it would have been obvious for Lee’s “pre-bias voltages” to be implemented as “word line pre-pulse signals” within the meaning of the ’822 claims. First, Petitioner asserts that “a POSITA would have understood (or considered it obvious) that Lee’s pre-bias voltages are supplied in the form of a ‘pulse’” based on the combined disclosures that “Lee (1) supplies its pre-bias voltages in a separate and distinct-in-time step, and (2) the pre-bias voltages differ from the later V_{pgm} and V_{pass} voltages.” Pet., 38-39 That

argument is misplaced. Lee does not disclose the signal, waveform, or timing characteristics of the “pre-bias voltages” (or any other voltages), and there is nothing to suggest that the “pre-bias voltages” would be applied in the form of a “pulse” in particular. Even assuming—as Petitioner and Dr. Liu contend—that Lee’s pre-bias voltages differ from the voltages applied during a subsequent programming step, that would be true for any number of arbitrary signals. “[T]he breadth of these choices and the numerous combinations indicate that these disclosures would not have rendered the claimed invention obvious.” *Leo Pharm. Prods. v. Rea*, 726 F.3d 1346, 1356 (Fed. Cir. 2013). Nothing in Lee suggests or otherwise renders obvious that pre-bias voltages would take the form of “pulses,” nor has Petitioner presented a cogent argument why Lee’s pre-bias voltages would be applied as “pulses” just because they are applied in a distinct period and differ from later voltages.

Second, Petitioner relies on conclusory, unsupported testimony of Dr. Liu to assert that “when the ’822 patent was filed, programming voltages were conventionally provided in the form of a ‘pulse,’” and suggests that Lee’s “pre-bias voltages ... obviously would be supplied as pulses” as well. *See* Pet., 39; *see also* Liu Dec. ¶¶ 204-205. That argument is equally misplaced, and conflates *programming* voltages with the claimed *pre-pulse* (or *pre-charge*) signals applied during a pre-charge period. As explained by the ’822, the purpose of the invention is to remove boosting charges during a distinct pre-charge period *before* the

subsequent programming operation. *See* '822, 3:43-46 (signals are applied in “***a pre-charge period (before programming)***”) (emphasis added); *see also id.* 3:50-65 (describing distinct signals applied in a pre-charging period and the programming period). Petitioner and Dr. Liu identify examples of programming pulses allegedly known in the art, but those pulses are not used in a “pre-charge period” as required by the claims, and are instead used to set the value of a memory cell in the subsequent programming step. *See* Pet., 39; Liu Dec. ¶¶ 204-205 (citing Aitome (Ex. 1006) at 44, 116-117, 142-143 (discussing “applying high-voltage, V_{pgm} ” for “programming pulses”); Cappelletti (Ex. 1008) at 354 (a “[p]rogram [p]ulse” is provided to program a “selected cell”)). No portion of the Aritome or Cappelletti background references cited by Petitioner and Dr. Liu discloses signals applied during a pre-charging period, nor has Dr. Liu provided any rationale why using pulses for a subsequent programming step would require or render obvious pulses to be used for pre-charge signals. As before, Petitioner and Dr. Liu have failed to show that Lee’s pre-bias voltages are supplied in a pulse form, or that it would be obvious to do so.

For at least the reasons provided above, Lee fails to teach or render obvious the claimed process of applying pre-pulse signals to word line groupings as required by each of the independent Challenged Claims. Petitioner’s cited disclosures merely pertain to Lee’s disclosure of pre-bias voltages that are neither expressly disclosed nor obviously supplied as pre-pulse signals.

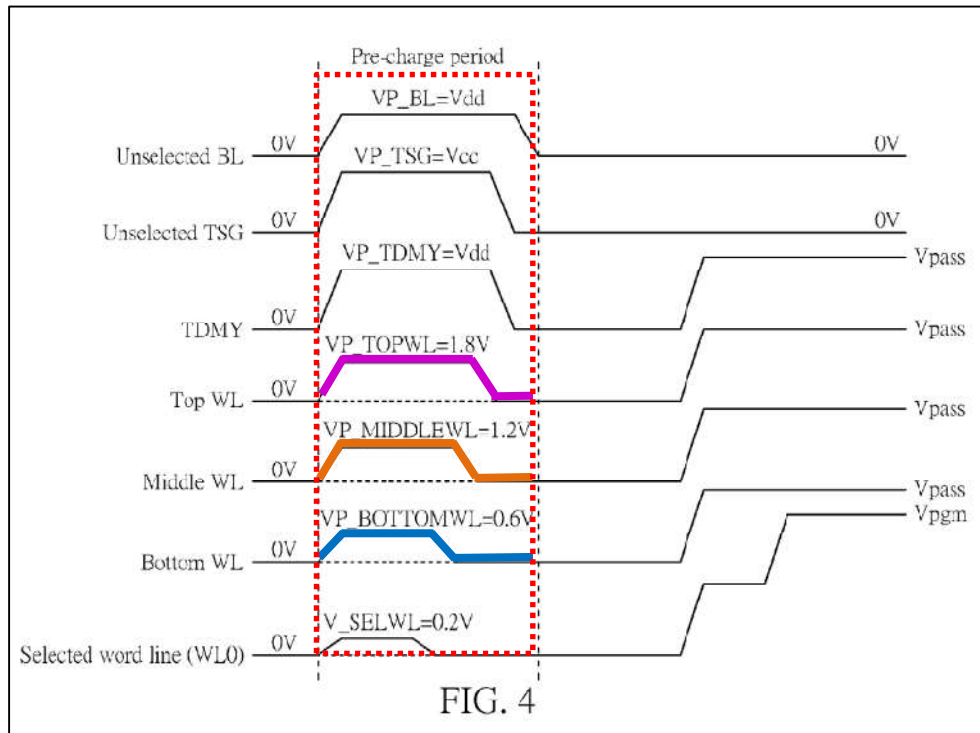
B. Ground 2: Zhao Does Not Teach or Render Obvious “a First Word Line Pre-Pulse Signal of a Plurality of Word Line Pre-Pulse Signals” Applied “to a First Group of the Plurality of Word Lines During a Pre-Charge Period”

Zhao does not disclose or otherwise render obvious limitations [1.e.1] and [11.b] because Zhao’s application of a flat, unchanging, V_{ss} voltage (*i.e.*, the purported “first pre-pulse signal” identified by Petitioner) is not a “pulse” as required by the ’822, and instead shows that no pulse is applied during the purported pre-charge period. Pet., 44-59. Moreover, Petitioner’s suggestion that Zhao discloses or otherwise renders obvious the use of a pulsed signal in lieu of V_{ss} during the relevant time period is based on incorrect inferences and mischaracterizations of Zhao’s teachings. *Id.*

Claim 1 recites a control circuit configured to “**apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines** during a pre-charge period” (Element [1.e.1]). Analogous limitations are found in Element [11.b] of independent claim 11, and are common to each of the Challenged Claims. As discussed in Section IV, a “word line pre-pulse signal” is a “pulse signal to prepare word lines for a programming step,” and a “pulse” does not encompass a flat voltage signal.

As explained in Section II, the claimed invention of the ’822 improves of conventional systems by using multiple pre-pulse signals during a pre-charge period to enhance the channel potential gradient, remove boosting charges, and mitigate the

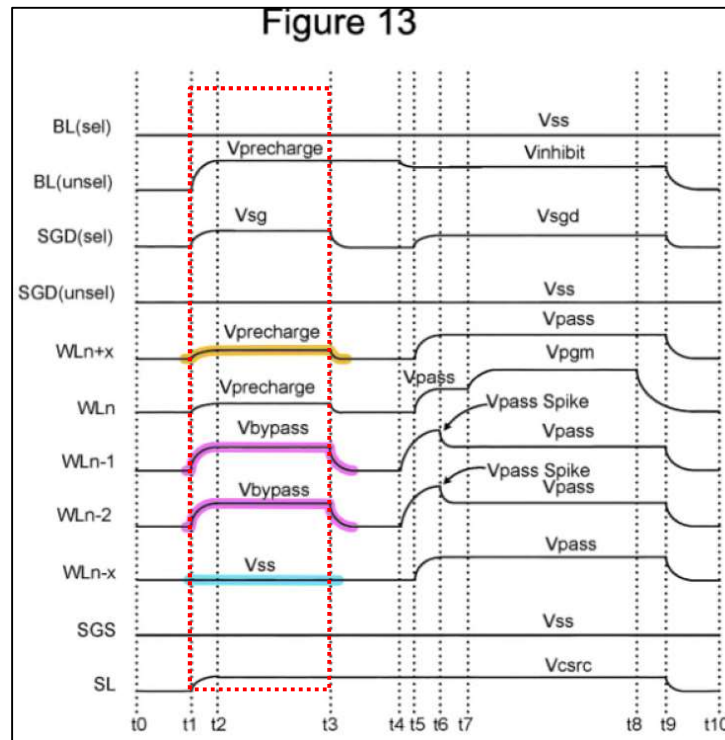
effects of programming disturb. For example, as illustrated in the embodiment of Fig. 4, a **first word line pre-pulse signal**, a **second word line pre-pulse signal**, and a **third word line pre-pulse signal** are each applied to different groups of word lines during **the pre-charge period**:



But unlike the claimed invention of the '822, Zhao does not disclose three separate word line pre-pulse signals during the pre-charge period, as required by the '822.

Zhao's approach to mitigating program disturb is illustrated by Fig. 13. Starting at time t_0 , "all the depicted signals are at ... 0 volts (V_{ss})," and the time period "from **t_1 - t_3 corresponds to pre-charging.**" Zhao, 22:34-41. But Zhao fails to disclose three distinct "pre-pulse signals" applied to groups of word lines during the pre-charging period. For example, as shown below, Petitioner incorrectly

characterizes **V_{ss}** as one of the claimed “pre-pulse signals ... during a pre-charge period” recited by the independent claims of the ’822.⁴ *See* Pet., 22-23; *see also id.*, 52.



Petitioner’s argument fails at least because the flat “**0 volt (V_{ss})**” voltage identified in the petition is not a “word line pre-pulse signal,” as it is not a “pulse.” Rather, Zhao explicitly teaches that “word lines WLn-x **remain at V_{ss}** (e.g., 0 v)” throughout the relevant time period. Zhao, 23:5-12.

Petitioner seemingly tries to address Zhao’s deficiency by asserting, incorrectly, that a different voltage may be applied to WLn-x in place of V_{ss} during

⁴ For convenience, Petitioner’s annotations have been reproduced above.

the time period t1-t3. *See* Pet., 51-52. To support this assertion, Petitioner points to Zhao's disclosure that: "To prevent the source side of the channels from being pre-charged, *unselected source side word lines receive 0 volts or one or more voltages that are too low to pre-charge* and/or too low to turn on memory cells in a highest data state." Zhao, 19:22-24. But that added disclosure does not suggest that a pulse is applied to word lines WLn-x during the pre-charge period. At most, Zhao is describing that the flat Vss signal depicted in Fig. 13 may be fixed at "0 volts," or another fixed voltage. Zhao, 19:22-26. But a flat signal, regardless of the voltage of that signal, is not a pulse. At no point does Zhao disclose a pulse being applied to WLn-x.

Thus, Petitioner has failed to show that word lines WLn-x in Zhao (*i.e.*, the purported "first group of word lines") receives a "first word line pre-pulse signal" during a pre-charge period as required by the independent Challenged Claims, nor has Petitioner provided any rationale why a POSITA would modify Zhao to do so. Rather, Zhao explicitly teaches that a flat signal rather than a pulse is applied to that group of word lines during the relevant time period. *See* Zhao, 23:5-12.

C. Ground 3: A POSITA Would Not Have Been Motivated to Combine Zhao and Lee

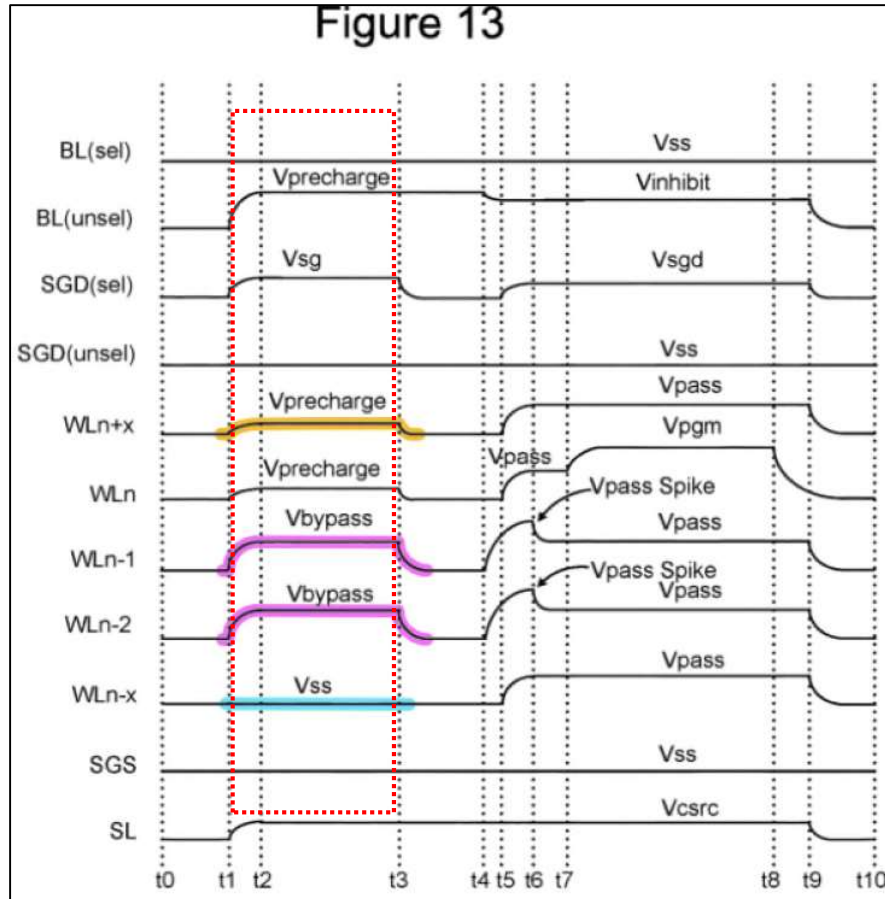
As described above in Sections VI.A and VI.B, Zhao and Lee fail to disclose or otherwise render obvious the use of a "first word line pre-pulse signal," "second word line pre-pulse signal," and "third word line pre-pulse signal," during "a pre-

charge period” as required by independent claims 1 and 11. Petitioner attempts to address these deficiencies by cobbling together disclosures from Lee (Ground 1) and Zhao (Ground 2), but has failed to show that a POSITA would have motivated to apply Lee’s teachings in the manner proposed in the Petition—*i.e.*, that the use of multiple increasing pre-bias voltages is needed to offset “effects caused by the resistance component between the source select transistor and the drain select transistor.” Pet., 62; *see also* Lee 8:25-52 (explaining that “a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor”). As explained below, these particular effects are not present in Zhao’s system, and Lee’s teachings would not provide the intended benefits purportedly described by Lee and relied upon by Petitioner as a purported motivation to combine. It is only through impermissible hindsight bias, in an effort to reconstruct the ’822 system *ex-post*, that a POSITA would attempt to apply Lee’s teachings to Zhao in the manner that Petitioner proposes. *See* Przybylski, ¶¶ 40-41.

As discussed in Sections VI.A and VI.B, Claim 1 recites a control circuit configured to “apply a [first/second/third] word line pre-pulse signal of a plurality of word line pre-pulse signals to a [first/second/third] group of the plurality of word lines during a pre-charge period” (Elements [1.e.1]-[1.e.2]), wherein “a voltage level of **the second word line pre-pulse signal** is greater than that of **the first word line**

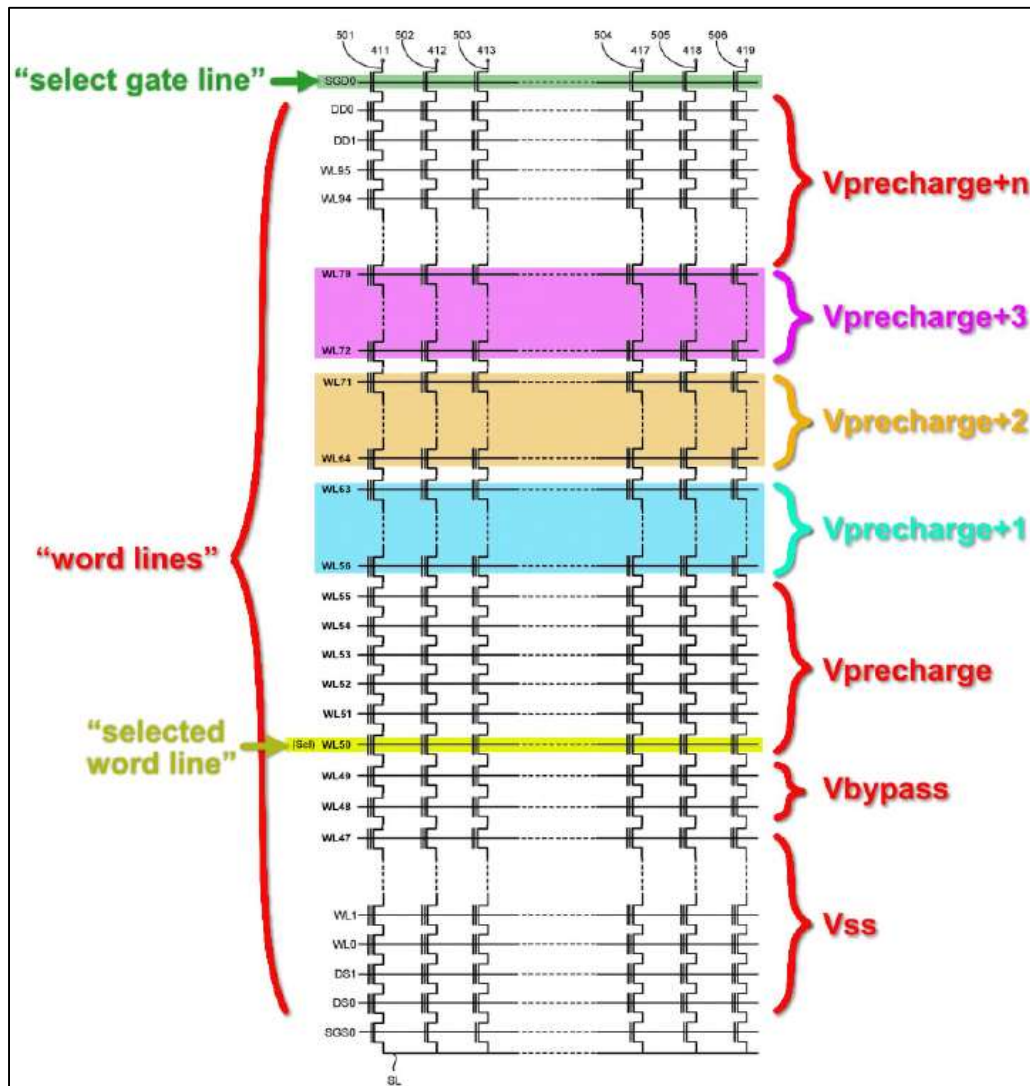
pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.” (Element [1.e.4]). Analogous limitations are found in Elements [11.b]- [11.e] of independent claim 11, and are common to each of the Challenged Claims.

As discussed in Section V.B, Zhao generally describes applying a “Vprecharge” signal to word lines $WLn+x$ located on the drain-side of the currently selected word line.



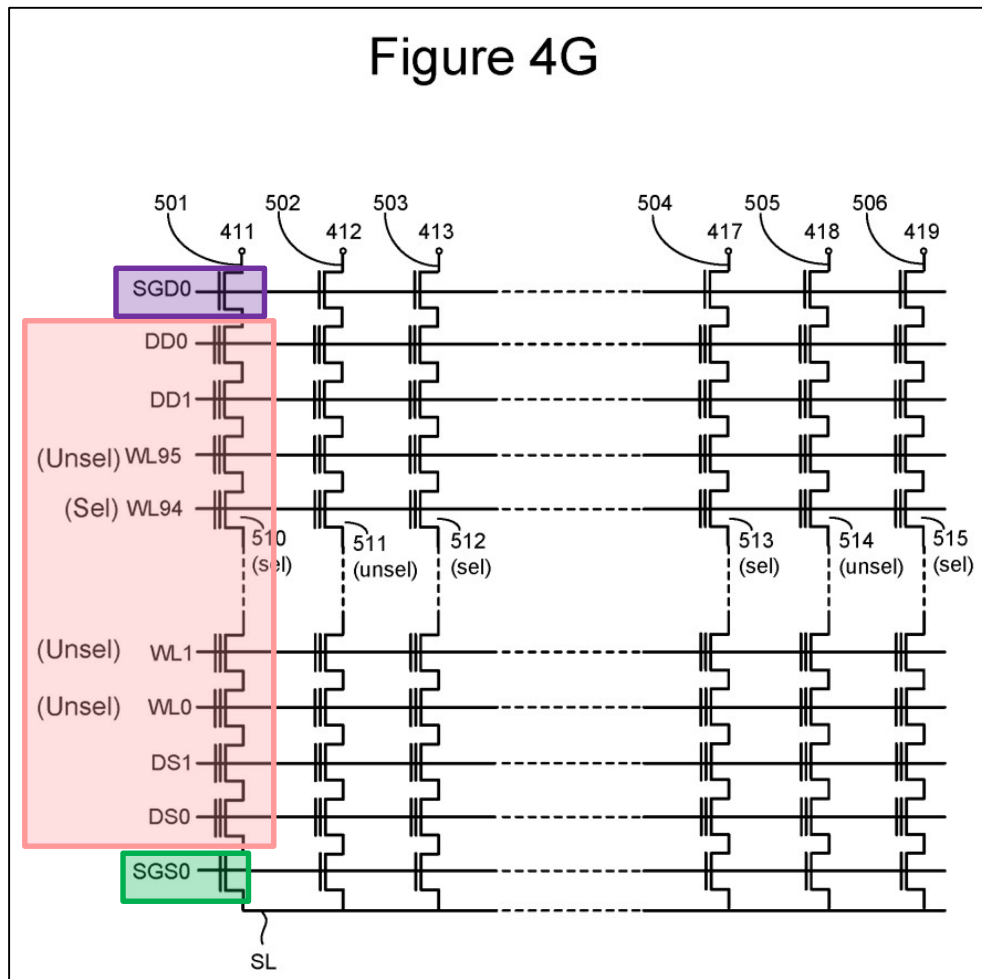
Zhao, Fig. 13. Petitioner argues that it would have been obvious to replace Zhao’s single Vprecharge signal with a series of different pre-charge signals, as allegedly

taught by Lee, in an effort to “compensate” for “effects caused by the resistance component between the source select transistor and the drain select transistor,” and that the combined system would operate as illustrated below. *See* Pet., 60-67.



Pet., 65 (Annotations reproduced from Petition). But Petitioner's proposed combination is inconsistent with the purported motivation for applying Lee's teachings, and ignores the actual structure and operation of the memory cell string. See Przybylski, ¶¶ 42-43.

Both Lee and Zhao describe typical memory strings, which are a “vertical column” of **memory cells** arranged in series between a **source side** select transistor and a **drain side** select transistor.



Zhao, Fig. 4G, 10:6-24; *see also* Lee, Fig. 3, 7:37-57 (describing the structure of the memory cell string). As shown in the figure, because memory cells are connected in series, *all* of the **memory cells** must be turned on for current to flow between the **source side** select transistor and the **drain side** select transistor (*i.e.*, all the memory cells must be turned on to form a conductive channel through the memory cell string).

If any memory cell is turned off, there is no conductive channel. As a result, no current flows through the memory string, there are no voltage drops across the channels of the memory cells along the length of the string, and there are no changes in the memory cell threshold voltages (or the corresponding word line voltages necessary to form conductive channels) in the memory cells as a result of their position within the string. *See* Przybylski, ¶ 44.

The Petition fails to address the fact that in Zhao, as well as Petitioner's proposed combination, several of the memory cells are *explicitly* turned off. Indeed, Zhao's use of **V_{ss}** (or a similar voltage "too low to pre-charge and/or too low to turn on memory cells in a highest data state"), precludes any current flowing between the **source side** select transistor and the **drain side** select transistor as well as between the bit line at the top of the NAND string and sources line at the bottom of the NAND string. *See* Zhao, 19:22-26. The purported motivation that Petitioner points to for applying Zhao's teachings (*i.e.*, that multiple different pre-charge voltages are needed to offset changes in memory cell threshold voltages due to a "resistance component between the source select transistor and the drain select transistor") is simply inapplicable. Pet., 60; Zhao 8:25-29. Contrary to what Petitioner suggests, there is no need to replace **V_{precharge}** with multiple pre-charge signals in the manner they have proposed, and attempting to do so would not compensate for a

purported “resistance component” or otherwise help to create a more uniform charge distribution. *See* Przybylski, ¶ 45.

The inconsistency between Zhao’s teachings and Lee’s system is further highlighted by their distinct approaches for mitigating program disturb. Zhao’s pre-charge operation is directed to “purging (cleaning/clearing the electrons from) the already programmed side of the channel” prior to the subsequent boosting and programming steps. *See* Zhao, 2:27-35; *see also id.* 18:63-19:8 (describing a method for “purging the already programmed side of the channel during a pre-charge operation”). Purging mitigates program disturb resulting from “source side hot electron injection,” which arises from unwanted charges being accelerated from the source side to the drain side during boosting, and then redirected into memory cells on the selected word line. Zhao, 18:36-51. To address this problem, Zhao teaches that “a bypass voltage to multiple already programmed side unselected word lines while pre-charging ... the channels of unselected NAND strings.” Zhao, 19:29-34; *see also* Zhao, 22:50-56. Doing so “electrically couples the two ends of the channel” in the region where the bypass voltage is applied, and allows electrons to flow freely near the selected word line and “eliminate the voltage differential between the source side of the channel and the drain side of the channel that may later cause program disturb.” Zhao, 22:65-23:5. *See* Przybylski, ¶ 46.

Lee discusses a wholly disparate approach for mitigating program disturb that is inapplicable in Zhao's system. Zhao applies a localized bypass voltage that "electrically couples the two ends of the channel" and allows charges to be equalized, but does so without conducting between the source select transistor and the drain select transistor at the ends of the memory string. *See* Zhao, 22:65-23:5. By comparison, Lee applies a pre-charge voltage to *every* memory cell in the string. *See, e.g.,* Lee, 8:3-18 (a "memory block includes thirty-two word lines WL0 to WL31" and pre-bias voltages are "applied to the respective word lines WL0 to WL31 in a precharging step during a program operation"). As a result, Lee, unlike Zhao, must compensate for the fact that the "pre-charge level in a source side channel is reduced and thus charge boosting is not effectively generated" because "a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor." Lee, 8:25-31, 8:47-52. *See* Przybylski, ¶ 47.

Contrary to Petitioner's assertions, a POSITA would not have been motivated to apply Lee's teachings to Zhao. They are not, as Petitioner seems to suggest, describing complementary techniques for further reducing program disturb. *See* Pet., 66-68. Rather, Lee's use of preset bias levels for each and every word-line (which would include those adjacent to the selected word line) is fundamentally different than the scheme described by Zhao, and Lee's teachings regarding the use

of different voltages to compensate for resistance along the memory string (*i.e.*, at different locations between the source select transistor and the drain select transistor) would not provide the benefits that Lee’s teachings purport to provide in the context of Petitioner’s proposed combination. *See* Przybylski, ¶ 48.

Rather, Petitioner’s and Dr. Liu’s illustrations showing how the supposed combination would operate is divorced from any possible benefits to Zhao’s system. At best, it is a naked attempt to “reconstruct the applicant’s invention only with the benefit of hindsight,” that fails to render obvious the Challenged Claims. *Netflix*, 80 F.4th at 1359. *See* Przybylski, ¶¶ 49-52.

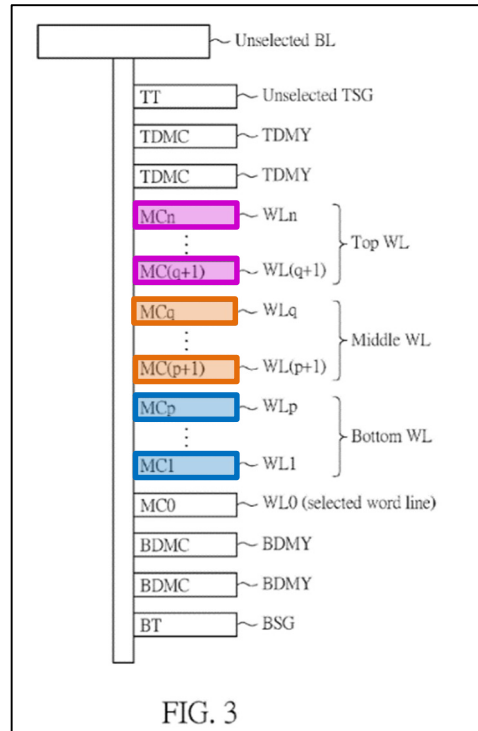
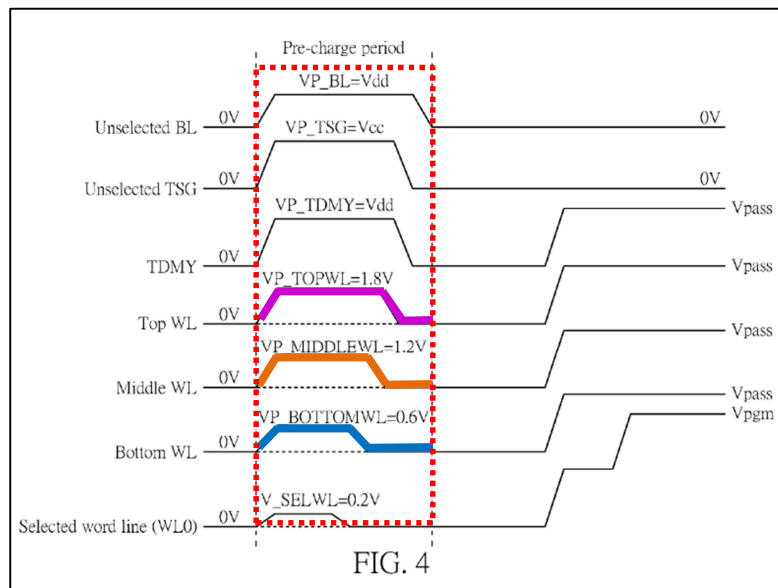
D. Ground 4: Yang Does Not Teach or Render Obvious Applying Three Distinct “Word Line Pre-Pulse Signal[s]” to Groups of Word Lines With Incrementally Increasing Voltages

Yang does not disclose or otherwise render obvious limitations [1.e.1]-[1.e.4] because Yang’s use of “Vbypass,” “Vpre_OD,” and “Vpre_dmy” voltages (*i.e.*, the purported “word line pre-pulse signals”) fails to disclose three signals applied to three groups of word lines that have incrementally increasing voltage levels. Moreover, Petitioner’s assertion that “a POSITA would nonetheless have understood Yang to render what this limitation requires obvious” is unsupported by the record and insufficient to support a finding of obviousness. *Pet.*, 76-82.

Claim 1 recites a control circuit configured to “**apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the**

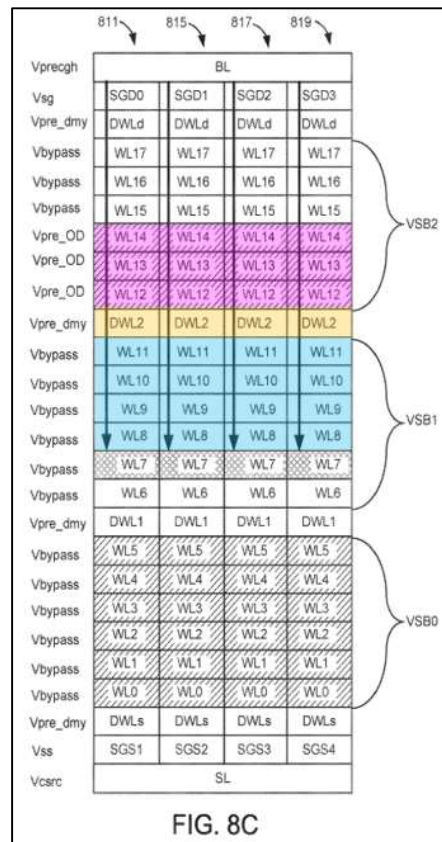
plurality of word lines during a pre-charge period” (Element [1.e.1]); “**apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines** during the pre-charge period” (Element [1.e.2]); and “**apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines** during the pre-charge period” (Element [1.e.3]) wherein “**a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.**” (Element [1.e.4]). Analogous limitations are found in Elements [11.b]-[11.e] of independent claim 11, and are common to each of the Challenged Claims.

As described in the '822, the system is “configured to apply a plurality of word line pre-pulse signals to word lines which are disposed between the selected word line and the top dummy word line TDMY,” with “incremental” voltage levels. '822, 3:55-59; 4:2-10. For example, in the embodiment illustrated in Figs. 3-4, the 1.8V voltage level of the **third word line pre-pulse signal** (VP_TOPWL) is greater than 1.2V voltage level of the **second word line pre-pulse signal** (VP_MIDDLEWL) which is greater than the 0.6V voltage level of the **first word line pre-pulse signal** (VP_BOTTOMWL). *See* '822, 5:50-55, 5:65-6:8, Figs. 3-4.

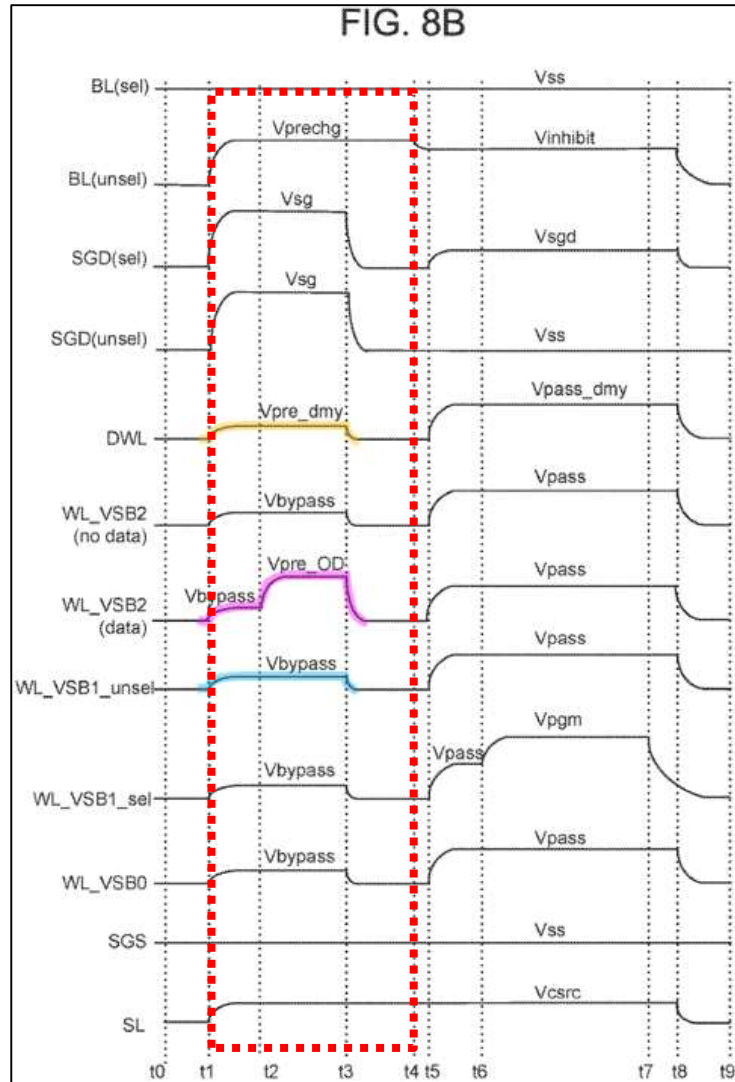


Unlike the '822, Yang does not disclose three distinct “word line pre-pulse signals” applied to groups of word lines that have incrementally increasing voltage levels. As shown in Figures 8B-8C of Yang, copied below, Petitioner improperly equates the claimed “**first**,” “**second**,” and “**third**” word line pre-pulse signals

applied to groups of word lines with Yang's disclosure of: (1) **"bypass voltage"** (**"Vbypass"**) applied to "not yet programmed" memory cells, (2) a **"dummy pre-charge voltage"** (**"Vpre_dmy"**) applied to a "dummy" memory cell,⁵ and (3) an **"overdrive voltage"** (**"Vpre_OD"**) applied to "programmed" memory cells, respectively. Pet., 73-81.



⁵ Petitioner incorrectly asserts that Yang's disclosure of using "[m]ore or less ... layers" discloses the use of multiple dummy layers in lieu of the one depicted in the figure. *See* Pet., 79; Yang 9:2-5. Incorporating more layers into the device does not imply the use of multiple dummy layers in the specific location identified.



Yang, Figs. 8B-8C.⁶ Yang does not disclose, and Petitioner has not otherwise shown, that **Vbypass**, **Vpre_dmy**, and **Vpre_OD** constitute distinct “word line pre-pulse signals” applied to different groups of word lines with the different voltage levels required by the claims.

⁶ Petitioner’s annotations for **Vbypass**, **Vpre_dmy**, and **Vpre_OD** are reproduced above.

Petitioner attempts to remedy Yang’s deficiencies by acknowledging that “Yang does not provide numerical examples” for the relevant voltage levels, and asserts in conclusory fashion that a POSITA would have “nonetheless understood Yang to render what this limitation requires obvious.” Pet., 81-82. But Petitioner’s unsupported assertions (e.g., that **Vpre_dmy** has an “intermediate” value less than **Vpre_OD**) does not establish any relationship between the relative magnitude of **Vpre_dmy** as it relates to **Vbypass**, or otherwise show that Petitioner’s proposed mapping discloses or renders obvious the limitations of the independent Challenged Claims. *See* Pet., 81-82.

VII. CONCLUSION

The Petition should be denied institution, as Petitioner has failed to establish a likelihood that it would prevail with respect to any of the Challenged Claims based on the grounds presented in the petition.

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Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(c)(1). According to the word-processing system's word count, the brief contains 9,435 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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