

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00795
Patent 11,501,822 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Micron Technology, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–9 and 11–19 of U.S. Patent No. 11,501,822 B2 (Ex. 1001, “the ’822 patent”). Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 8 (“Prelim. Resp.”). The Petition is supported by a declaration from Dr. David Kuan-Yu Liu. Ex. 1003 (“Liu Declaration”). The Preliminary Response is supported by a declaration by Dr. Steve Przybylski. Ex. 2001 (“Przybylski Declaration”).

We have authority to determine whether to institute an *inter partes* review. See 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons given below, on this record, Petitioner has established a reasonable likelihood that it would prevail in showing the unpatentability of claims 1–9 and 11–19 of the ’822 patent. Accordingly, we institute an *inter partes* review as to claims 1–9 and 11–19 of the ’822 patent on all asserted grounds of unpatentability.

B. *Real Parties in Interest*

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 4. Patent Owner identifies itself as a real party-in-interest. Paper 5, 2.

C. Related Matters

The parties represent that the '822 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 5, 2; Pet. 4.

Petitioner has also filed IPRs challenging other patents asserted in the district court case, namely U.S. Patent Nos. 10,658,378 (IPR2024-00788), 10,861,872 (IPR2024-00789), 10,868,031 (IPR2024-00790), 10,937,806 (IPR2024-00791), 10,950,623 (IPR2024-00794), 11,468,957 (IPR2024-00792), and 11,600,342 (IPR2024-00793). Pet. 4.

D. The '822 Patent

The '822 patent is titled “Non-Volatile Memory Device and Control Method.” Ex. 1001, code (54). The '822 patent issued from Application No. 16/709,944, filed on December 11, 2019, and claims priority via a continuation application to PCT/CN/2019/112409, filed on October 22, 2019. *Id.* at code (63).

The '822 patent relates to “a non-volatile memory device and a control method capable of applying word line pre-pulse signals with different voltage levels and reducing programming disturb.” *Id.* at 1:15–19.

E. Illustrative Claim

Claim 1 is illustrative, and recites as follows:¹

[1.Pre] A memory device, comprising:

[1.A] a plurality of memory strings;

[1.B] a bit line connected to a first memory string of the plurality of memory strings;

[1.C] a select gate line connected to the first memory string of the plurality of memory strings;

[1.D] a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string; and

[1.E] a control circuit configured to:

[1.E.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period;

[1.E.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[1.E.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,

[1.E.4] wherein a voltage level of the second word line prepulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

¹ Bracketed organization added as per the Petition.

F. Evidence

Petitioner relies on the following patent document evidence.

Name	Patent Document	Exhibit
Lee	US 10,121,529 B2	1004
Zhao	US 10,643,718 B2	1005
Yang	US 10,726,920 B2	1010

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–9 and 11–19 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3, 6, 11–13	103 ²	Lee
1, 4–7, 9, 11, 14–16, 18–19	103	Zhao
1–9, 11–19	103	Zhao, Lee
1–7, 9, 11–16, 18–19	103	Yang

II. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art [to which said subject matter pertains].” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level

² Petitioner asserts, and we accept for purposes of institution, that AIA 35 U.S.C. 103 applies to the ’822 patent. See Pet. 19.

of ordinary skill in the art; and (4) objective evidence of non-obviousness.³
See Graham v. John Deere Co., 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) at the critical time

would have had a bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

Pet. 18 (citing Ex. 1003 ¶¶ 35–38). Petitioner further asserts that a POSITA “would have been aware of and generally knowledgeable about NAND memory’s structure, its component parts, how it operates, and how it is controlled. *Id.* (citing Ex. 1003 ¶ 38). Patent Owner does not provide any such assessment. *See* Prelim. Resp. 16. For purposes of this Decision, we adopt Petitioner’s proposed level of ordinary skill, as it appears to be consistent with the specification of the ’822 patent and the prior art of record.

C. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person

³ Neither party presents evidence or arguments regarding objective evidence of non-obviousness at this stage.

of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Here, Petitioner states the claims can be afforded their plain and ordinary meaning and no further claim construction is required. Pet. 18. Patent Owner argues for construction only of the phrase “word line pre-pulse signal.” Prelim. Resp. 16–19. Patent Owner argues that claim 1 applies such a signal during a pre-charge period, which the Specification explains is before programming. *Id.* at 17 (citing Ex. 1001, 3:43). Patent Owner reasons that accordingly, the pre-pulse signal “prepares the word line before the programming step.” Prelim. Resp. 17. Patent Owner further argues that such a signal is in the form of a pulse, and that a pulse is described in the Specification as having an associated duration. *Id.* at 17–18 (citing Ex. 1001, 7:19–36); *see also id.* at 27 (stating “[a]s properly construed, a ‘word line pre-pulse signal’ is a ‘pulse signal to prepare word lines for a programming step’”). Patent Owner argues that Petitioner applies the same understanding of the phrase in its Petition, at least to the extent that Petitioner has not suggested that such a pulse would encompass a flat voltage signal. *Id.* at 18 (citing Pet. 2, 38–39, 51).

We agree that Petitioner applies its teachings with the same understanding of “pre-pulse signal” as Patent Owner. *See, e.g.*, Pet. 38–39 (asserting that Lee teaches, or that that Lee would make obvious, pre-bias signals applied as pulses). Because no dispute as to the meaning of this phrase exists at this time in a manner that would affect the outcome of this decision, we do not need to determine a particular construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy,

and only to the extent necessary to resolve the controversy.” (quoting *Vivid Techs., Inc. v. Am. Sci & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness over Lee

Petitioner asserts that claims 1–3, 6, and 11–13 are unpatentable under 35 U.S.C. § 103 as obvious over Lee. Pet. 26. Patent Owner argues against the assertion. Prelim. Resp.

Upon consideration of Petitioner’s explanations and the totality of evidence in this current record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in showing that claims 1–3, 6, and 11–13 are unpatentable under 35 U.S.C. § 103 as obvious over Lee.

1. Lee

Lee is titled “Semiconductor Memory Device For Applying Different Bias Voltages and Operating Method Thereof.” Ex. 1004, code (54). Lee relates to a semiconductor memory device in which pre-bias voltages are applied to a plurality of word lines to precharge channel regions of the memory cells. *Id.* at code (57). Different pre-bias voltages are applied depending on the relative positions of the word lines. *Id.* Lee applies prebias voltages during a “precharging step.” *Id.* at 8:15–18.

2. Analysis of Claim 1

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 1. Patent Owner does not specifically argue against Petitioner’s assertions for limitations [1.Pre]–[1.D]; however, we draw no inference therefrom and Petitioner bears the burden of persuasion.

[1.Pre]–[1.D] A memory device, comprising: a plurality of memory strings; a bit line connected to a first memory string of the plurality of memory strings; a select gate line connected to the first memory string of the plurality of memory strings; a selected word line of a plurality

of word lines, wherein the plurality of word lines is connected to the first memory string;

Petitioner asserts that limitations [1.Pre]–[1.D] are taught by Lee in the following manner. Petitioner points to Lee’s semiconductor memory device 100 having a memory cell array with memory cells arranged in a plurality of cell strings. Pet. 27–28 (citing Ex. 1004, 5:60–61, 6:12–15, Fig. 3). Petitioner points to Lee’s description that each of these cell strings are coupled to a bit line; for example, Lee’s bit line “BLk+1” coupled to an unselected string in Figure 3. *Id.* at 28–29 (citing Ex. 1004, 7:28–36, Fig. 3). Petitioner points to Lee’s description that each cell string is coupled to a “drain select line DSL,” which Petitioner characterizes as the claimed “select gate line.” *Id.* at 29–30 (citing Ex. 1004, 7:37–43, Fig. 3). Petitioner points to Lee’s description that its memory cells are arranged into “pages” and are “coupled in common to a single word line.” *Id.* at 30–31 (citing Ex. 1004, 5:64–6:7, 7:30–45, Fig. 3). Petitioner further asserts that during programming of a particular cell, that cell’s associated bit line and word line are “selected.” *Id.* at 31–32 (citing Ex. 1004, 7:28–34, 8:18–24, Fig. 4).

Patent Owner does not, at this stage, argue against these assertions. Upon review of Lee, we determine that Petitioner’s assertions are supported by the record in a manner sufficient for institution.

[1.E] a control circuit configured to: [1.E.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period; [1.E.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and [1.E.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to

a third group of the plurality of word lines during the pre-charge period,

Petitioner asserts that Lee teaches application of the three claimed word line pre-pulse signals during a pre-charge period. Pet. 33. Petitioner points to Lee's description of four "groups" of word lines, each group containing eight word lines. *Id.* at 33–34 (citing Ex. 1004, 7:58–61, 9:36–40). Petitioner points to Lee's statement that "different pre-bias voltages may be applied to the respective groups during a precharge operation of the cell string." *Id.* at 35 (citing Ex. 1004, 7:58–61). Petitioner asserts that these voltages are "pre-pulses" applied during a pre-charge period that occurs before programming. *Id.* at 37 (citing Ex. 1:62–2:1, 2:30–32, 2:59–62, 9:7–11).

Petitioner asserts that such voltages are supplied in the form of a "pulse" because (1) they are supplied in a distinct-in-time step and (2) differ from later-applied V_{pgm} and V_{pass} voltages. *Id.* at 38–39 (citing Ex. 1003 ¶¶ 197–203). Petitioner further asserts that programming voltages were conventionally provided in the form of a pulse such that a person having ordinary skill in the art would have understood Lee to operate by supplying all voltages during programming as pulses. *Id.* at 39 (citing Ex. 1006, 44, 116–117; Ex. 1007, 142–143; Ex. 1008, 338, 354; Ex. 1003 ¶¶ 204–205).

Patent Owner argues that Lee does not disclose the claimed "word line pre-pulse signals" because Lee does not provide its pre-pulse signals in the form of pulses. Prelim. Resp. 28–31. Patent Owner argues that merely because Lee's signal is applied over a distinct period for a distinct voltage does not mean that the signal is a "pulse" as claimed. *Id.* at 31. However, Dr. Liu testifies that a POSITA would have understood that Lee's "on-off pre-bias voltages," which are supplied during the precharging period and

then removed before the programming voltages are supplied, are by definition a pulse. Ex. 1003 ¶ 203. Moreover, the '822 patent illustrates its precharge signal pulses as signals applied for a period of time at a certain voltage. See Ex. 1001, Fig. 4. The '822 patent describes a variety of different periods of time for the voltage application, including a period that extends over the entire precharge period. Ex. 1001, Fig. 5 (top line), 7:19–36. Thus, we have concerns about Patent Owner's argument that the current record distinguishes between the claimed "pulse" and Lee's signal applied for a distinct period of time for a distinct voltage; during trial, the parties may clarify the scope of the claimed "pre-pulse signal."⁴ For purposes of institution, we determine that Petitioner has provided sufficient argument and evidence that Lee's application of a distinct voltage over the pre-charge period teaches the pulse of claim 1.

Patent Owner also argues against Petitioner's assertion that pre-charge voltages would have been applied as a pulse in Lee because programming voltages were conventionally provided as a pulse. Prelim. Resp. 31–32 (citing Pet. 39; Ex. 1003 ¶¶ 204–205). Because we determine that Lee teaches applying precharge voltages as a pulse, for purposes of institution we need not reach the question of whether it would have been obvious for Lee to have provided its pre-charge voltages as a pulse. However, based on the preliminary record, it appears Patent Owner's arguments may have merit and we have concerns as to whether Petitioner has adequately shown that methods of applying programming voltages would have been obvious for applying precharge voltages.

⁴ We note that Dr. Przybylski has "not been asked by Patent Owner to provide an opinion on claim construction" at this stage. Ex. 2001 ¶ 24.

Patent Owner further argues that Lee’s signals are used for a different purpose than discussed in the ’822 patent. *Id.* at 29–30. Patent Owner argues that Lee’s signals are to produce a “uniformly formed charge” to compensate the resistance between source select transistor and drain selector, whereas the claimed ’822 patent pulses are to enhance the channel potential gradient and reduce programming disturb.” *Id.* at 29–30 (citing Ex. 1001, 4:39–59, 7:37–47; Ex. 1004, 7:58–62), 8:25–52. However, Lee also applies its signals to “mitigate a program disturb phenomenon.” Ex. 1004, 1:52–56. It is unclear at this stage how the purported differences pointed out by Patent Owner support any distinction related to a pulse. Consequently, we do not find such argument availing at this stage of the proceeding.

[1.E.4] wherein a voltage level of the second word line prepulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

Petitioner asserts that Lee teaches limitation [1.E.4] through its description that “different pre-bias voltages” are applied to its word line “groups during a precharge operation” and that “higher ... pre-bias voltage[s]” are applied to “word line group[s]” that are closer to the “drain select transistor.” Pet. 40 (citing Ex. 1004, 7:58-61, Abstr., 1:62–2:9, Fig. 4B, 8:32–37; 9:44–51). Patent Owner does not specifically contest this assertion.

We agree that Petitioner’s assertion is supported by the record in a manner sufficient for institution. Lee describes that the voltage applied to group 4 is greater than that for group 3, which in turn is greater than that for group 2. Ex. 1004, 9:41–52. Accordingly, Petitioner has sufficiently shown that Lee teaches limitation [1.E.4] for purposes of institution.

Conclusion

For the foregoing reasons, Petitioner has demonstrated a reasonable likelihood that it will prevail on showing that claim 1 would have been obvious over Lee.

3. *Analysis of Claims 2, 3, 6, and 11–13*

Petitioner’s assertions for independent claim 11, having similar limitations to those of claim 1, rest essentially on the same showing, which we also find persuasive at this stage for the aforementioned reasons. Pet. 26–41.

With respect to the word line groups being disposed “in an order of distance,” as set forth for claims 2 and 12, we agree with Petitioner’s uncontested assertion that Lee shows such an order in its Figure 4B. *Id.* at 41–42.

With respect to the further ordering set forth in claims 3 and 13, we agree with Petitioner’s uncontested assertion that Lee’s Figure 4B shows a select gate line, then a third group, then a second group, then a first group, and then the selected word line in its order of word and gate lines. *Id.* at 42–43 (citing Ex. 1004, 7:37–43, 6:15–18; Ex. 1003 ¶¶ 217–220).

With respect to the application of a word line signal to the selected word line as set forth in claim 6, we agree with Petitioner’s uncontested assertion that “Lee’s control unit causes the ‘selected’ word line to be supplied with a ‘default value’ ‘[p]re-bias voltage[.]’ during pre-charge,” and a “program voltage *V*_{pgm}” during programming. *Id.* at 44–45 (citing Ex. 1004, 2:23–29, 6:29–36, 9:7–14, 9:52–55; Ex. 1003 ¶¶ 221–225).

Conclusion

For the foregoing reasons, Petitioner has demonstrated a reasonable likelihood that it will prevail on showing that claims 2, 3, 6, and 11–13 would have been obvious over Lee.

E. Obviousness over Zhao

Petitioner asserts that claims 1, 4–7, 9, 11, 14–16, and 18–19 would have been obvious over Zhao. Pet. 44–59. Because we have determined that the Lee-based ground supports institution of trial, we institute for all claims and grounds, and we need not further determine whether the Zhao-based ground would also support institution. For purposes of focusing the issues for trial, we have considered Petitioner’s explanations and the totality of evidence in this current record, and we provide the following analysis.

1. Zhao

Zhao is titled “Non-Volatile Memory with Countermeasure for Program Disturb Including Purge During Precharge.” Ex. 1005, code (54). Zhao relates to a semiconductor memory device in which it is proposed to address program disturb during memory cell programming by “open[ing] the channel from one side of a selected word line to the other side of the selected word line after a sensing operation for program verify and prior to a subsequent programming voltage being applied.” *Id.* at code (57). Unselected NAND strings are pre-charged prior to applying the program voltage to the selected word line. *Id.* at Fig. 11, [702]. Different pre-bias voltages are applied depending on the relative positions of the word lines. *Id.* During programming, unselected cells are maintained at a voltage V_{dd} to inhibit programming while selected cells have a program pulse applied thereto. *Id.* at 14:43–64. In one embodiment, a time period t_1 – t_3 corresponds to precharging, during which unselected bit lines are raised to a

pre-charge voltage. *Id.* at 22:39–49, Fig. 13. During the next time period t4–t10 corresponding to programming, the unselected NAND strings have their voltage lowered from Vpre-charge to Vinhibit. *Id.* at 23:13–17.

2. Analysis of Claim 1

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 1. Patent Owner does not specifically argue against Petitioner’s assertions for limitations [1.Pre]–[1.D]; however, we draw no inference therefrom and Petitioner bears the burden of persuasion.

[1.Pre]–[1.D] A memory device, comprising: a plurality of memory strings; a bit line connected to a first memory string of the plurality of memory strings; a select gate line connected to the first memory string of the plurality of memory strings; a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string;

Petitioner asserts that limitations [1.Pre]–[1.D] are taught by Zhao in the following manner. Petitioner points to Zhao’s memory system 100 having a three dimensional NAND structure having columns implementing NAND strings, in which each NAND string includes a series of non-volatile memory cells. Pet. 44–45 (citing Ex. 1005 4:7–10, 8:31–44, 6:41–43, 10:6–9; 12:6–7, 12:9–13, Figs. 4F, 4G). Petitioner further points to Zhao’s bit line 411 and select gate line SGD0 connected to a NAND string as exemplary of teaching a bit line and a select gate line that are connected to a first memory string. *Id.* at 45–47 (citing Ex. 1005, 7:64–66, 10:19–21, 11:53–61, 12:6–10, Fig. 4G). Petitioner further points to Zhao as teaching a plurality of word line layers WLL0–WLL95 as connecting to the memory cells that make up Zhao’s NAND strings, and that at least one word line, for example,

word line 94, is “selected for programming.” *Id.* at 47–48 (citing Ex. 1005, 7:64–66, 10:8–13, 3:30–49, 17:27–30, 12:14–25, Fig. 4G).

Patent Owner does not, at this stage, argue against these assertions. Upon review of Zhao, we determine that Petitioner’s assertions are supported by the record in a manner sufficient for institution.

[1.E] a control circuit configured to: [1.E.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period; [1.E.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and [1.E.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,

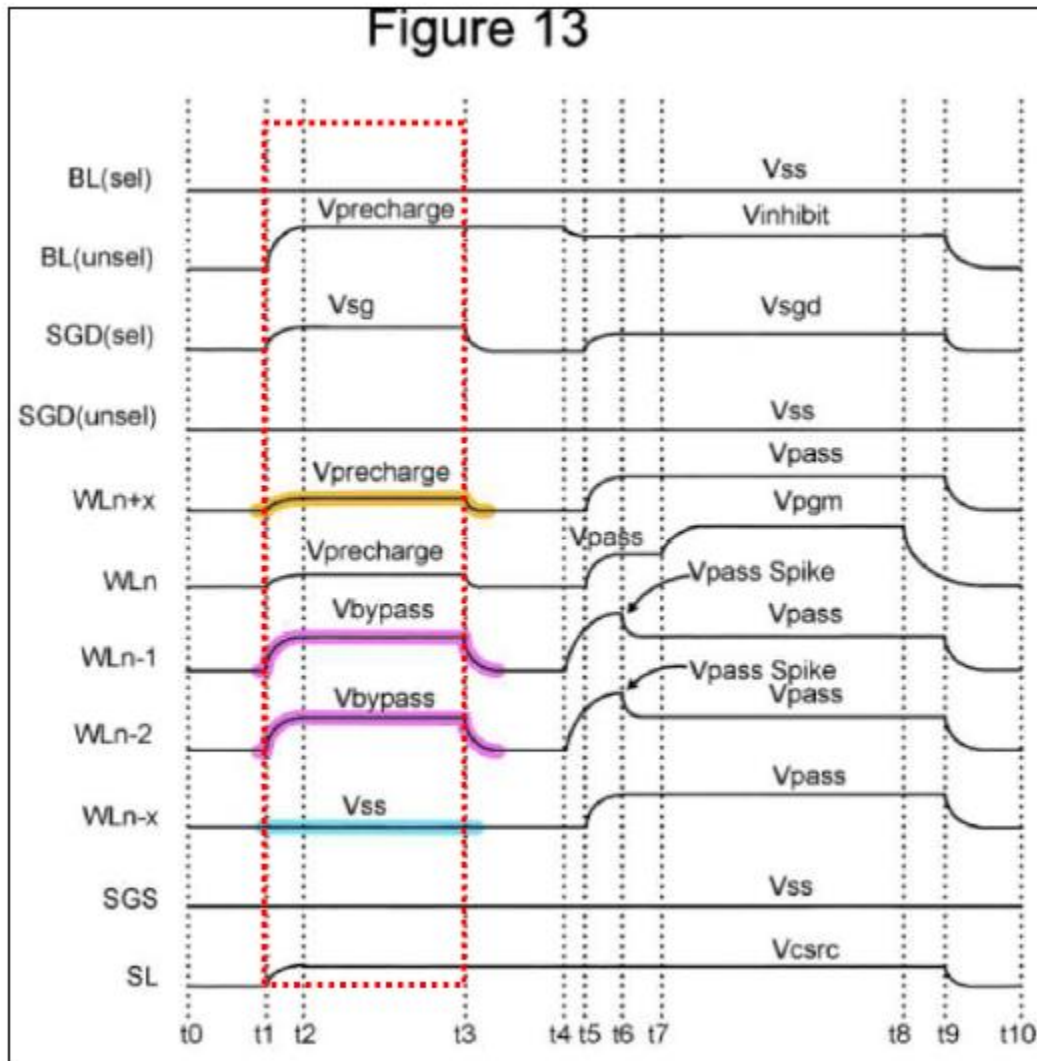
Petitioner asserts that Zhao describes a control circuit 310 that performs memory operations on memory structure 326, including a process for programming and a pre-charge circuit 584 that applies pre-charge signals to channels of unselected NAND strings. Pet. 48–49 (citing Ex. 1005, 5:64–6:20, 13:65–14:6, 16:40–67, Fig. 8). Petitioner further asserts that Zhao teaches that the pre-charge in step 542 occurs before the application of a program pulse in step 546. *Id.* at 49–50 (citing Ex. 1005, Fig. 7, 14:35–55, 19:12–19). Petitioner asserts that Zhao describes these pre-charge voltages to be in the form of “pulses.” *Id.* at 50 (citing Ex. 1005, 14:7–16).

Petitioner further points to Zhao’s description that “multiple already programmed (e.g., source side) unselected word line[s] ... adjacent to the selected word line” can “receive[]” a different “bypass voltage” “while pre-charging[.]” *Id.* at 50–51 (citing Ex. 1005, 19:19–60). Petitioner further points to Zhao’s description at Figures 4G and 13 of a pre-charge period corresponding to time period t_1 – t_3 , in which three different voltages are

applied to different word line groups. *Id.* at 51 (citing Ex. 1005, 22:39–53). Petitioner specifically points to unselected word lines $WLn-1$ and $WLn-2$ as having a V_{bypass} voltage of 6-10 V and a “low” V_{ss} voltage for the remaining source side unselected wordlines $WLn-x$. *Id.* (citing Ex. 1005, 22:41–53, 19:22–24).

Petitioner asserts that the claimed “first” pre-pulse signal is taught by Zhao’s low-voltage V_{ss} applied to nonadjacent source-side word lines $WLn-x$, the “second” pre-pulse signal is taught by Zhao’s $V_{precharge}$ applied to the drain-side word lines $WLn+x$, and the “third” pre-pulse signal is taught by Zhao’s V_{bypass} applied to the source-side word lines adjacent source-side word lines $WLn-1$ and $WLn-2$. *Id.* at 51–52. Petitioner states that although V_{ss} is 0V in the Figure, Zhao explains that a “low” non-zero voltage can be supplied instead in the same $t1-t3$ time period as the other pre-charge voltage pulses. *Id.* at 51 (citing Ex. 1005, 19:22–24). Petitioner contends that when a “low” non-zero voltage is supplied instead of 0V in the same $t1-t3$ time period, this results in a “first word line pre-pulse signal” (a low non-zero voltage in place of V_{ss} , blue) applied to a “first group of . . . word lines” (the source-side word lines not adjacent to the selected word line, $WLn-x$). *Id.* at 51–52.

Patent Owner argues that the V_{ss} voltage is not a pulse because it is a “flat, unchanging” voltage and thus, Zhao does not disclose or suggest the claimed first pre-pulse signal. Prelim. Resp. 33; *see also id.* at 36 (stating Zhao explicitly teaches that a flat signal, rather than a pulse, is applied to word lines $WLn-x$ during the relevant time period). Patent Owner annotates Figure 13 to illustrate:



Id. Annotated Figure 13 of Zhao illustrates timing regions t0 through t10 and the voltages applied to different regions. *Id.* at 35. Patent Owner highlights how Vss stays level during timing region t1–t3 in contrast to the voltage increases for Vprecharge and Vbypass over the same period. *Id.* Patent Owner interprets Zhao’s statement that Vss may instead receive “one or more voltages that are too low to pre-charge” as describing that a *fixed* non-zero voltage may be applied rather than a fixed zero voltage. *Id.* (citing Ex. 1005, 19:22–26). Patent Owner asserts that regardless of whether the Vss signal is fixed at 0 volts or another fixed voltage, that the signal will

remain flat, regardless of the voltage of that signal, and that a flat signal is not a pulse. *Id.* at 36.

At this stage, Patent Owner’s argument appears to have merit. Zhao describes its Vbypass voltage as a certain voltage; i.e., 6-10 volts, applied over a set timespan; e.g., t1–t3, and Patent Owner does not dispute that this voltage is a pulse. Figure 13 of Zhao illustrates that Vss is applied over that same timespan and not over the later t4–t9 timespan. Ex. 1005, Fig. 13; Prelim. Resp. 35–36 (Patent Owner’s annotated version of Figure 13). However, Zhao states that lines WLn-x “remain” at either Vss or a low voltage. Ex. 1005, 23:7–8. Although the voltages of WLn-x are later “raised” at period t4–t10, Zhao does not indicate that the application of the nonzero Vss voltage occurs over a discrete time period that would be consistent with the claimed pre-pulse signal. We invite the parties to develop these arguments further at trial, to the extent permitted by our rules. In particular, we invite the parties address the scope of the claimed pre-pulse signal, including whether a pre-pulse signal is any signal that occurs during the pre-charge period and prior to the programming pulse, and what is required for a signal to be considered a “pulse.”

[1.E.4] wherein a voltage level of the second word line prepulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

Petitioner asserts that Zhao teaches the claimed order, by describing that the “third” signal, Vbypass, is at 6-10V, the “second” signal, Vprecharge, is at 2V, and the “first” signal is a “low” non-zero voltage for WLn-x. Pet. 53–53 (citing Ex. 1005, 19:19–23, 19:57–58, 22:39–23:9, Fig. 13; Ex. 1003 ¶¶ 279–280). Patent Owner does not specifically contest this assertion, which we find supported by the record for purposes of

institution. Accordingly, Petitioner has sufficiently shown that Lee teaches limitation [1.E.4] for purposes of institution.

3. *Analysis of Claims 4–7, 9, 11, 14–16, and 18–19*

Petitioner’s assertions for independent claim 11, having similar limitations to those of claim 1, rest essentially on the same showing, and we reach the same conclusions at this stage for the aforementioned reasons. Pet. 44–53.

With respect to applying a bit line pre-pulse signal during the pre-charge signal, as set forth for claims 4 and 14, we agree with Petitioner’s uncontested assertion that Zhao teaches this as discussed above with respect to Figure 13. Pet. 54–55.

With respect to the first memory string and bit line both being unselected as set forth for claims 5 and 15, we agree with Petitioner’s uncontested assertion that Zhao teaches this through its description of precharging unselected NAND strings and unselected bit lines. Pet. 55 (citing Ex. 1005, 19:10–17, 22:39–45; Ex. 1003 ¶¶ 288–292).

With respect to the word line signal being applied to the selected word line as set forth for claim 6, we agree with Petitioner’s uncontested assertion that Zhao teaches this through its description of precharging unselected NAND strings and unselected bit lines. *Id.* at 55–56 (citing Ex. 1005, 22:39–49, 14:49–51).

With respect to the top dummy word line pre-pulse signal during the pre-charge period as set forth for claims 7 and 16, we agree with Petitioner’s uncontested assertion that Zhao teaches this through its description of dummy word line layers DD0 and DD1 at the upper drain side of Zhao’s memory structure that are “operated in the same manner as unselected word lines”; i.e., supplied with $V_{precharge}$ during the precharging time period.

Id. at 56–57 (citing Ex. 1005, 7:64–66, 9:30–39, 9:56–61, 10:6–13, 24:11–13, 25:31–32, 22:39–49, Fig. 4G; Ex. 1003 ¶¶ 297–306).

With respect to the top dummy word line being between the third word line group and the select gate line as recited for claim 18, we agree with Petitioner’s uncontested assertion that Figure 4G illustrates top dummy lines DD0 and DD1 below the select gate line SGD0 and above the already-programmed (and therefore currently unselected) word lines WLn-1 and WLn-2. *Id.* at 57–58 (citing Ex. 1005, Fig. 4G; Ex. 1003 ¶¶ 307–311).

With respect to the three word line voltage levels being positive, as set forth for claims 9 and 19, we agree with Petitioner’s uncontested assertion that Zhao teaches positive pre-pulse signal voltage levels because Zhao refers to positive voltage values. *Id.* at 58–59 (citing Ex. 1005, 22:50–53, 22:43–44, 19:23–26, Fig. 13).

F. Obviousness over Zhao and Lee

Petitioner asserts that claims 1–9 and 11–19 would have been obvious over Zhao in view of Lee. Pet. 59–68. Because we have determined that Petitioner’s showing based on Lee alone is sufficient to support institution, we institute for all claims and grounds, and we need not determine whether Zhao in view of Lee also supports institution. However, because claims 8 and 17 are only addressed in the Zhao-Lee combination, we provide the following additional analysis of claims 8 and 17, and further address Patent Owner’s arguments against the Zhao-Lee combination.

For its Zhao-Lee combination, Petitioner applies the teachings of Zhao for limitations [1.Pre]–[1.E.3]. Pet. 59–60. Petitioner applies the teachings of Lee to satisfy the relative voltage level limitations of [1.E.4]. Pet. 60–68. Petitioner also asserts that claims 8 and 17 would have been obvious over Zhao in view of Lee, relying on its contentions that the top

dummy lines are operated in the same manner as unselected word lines (as expressed for claims 7 and 16) and Lee's teaching that unselected word lines will have increasingly higher pre-charge voltages. Pet. 69–71. As discussed in the prior sections of this Decision, we find for purposes of institution that the limitations of claims 1, 7, 11, and 16, from which claims 8 and 17 depend directly or indirectly, are taught by Zhao except for limitation 1.E.4, which we find to be taught by Lee. We further find for purposes of institution that Petitioner's assertions for the additional limitations of claims 8 and 17, which are uncontested by Patent Owner at this stage, are supported by the current record.

With respect to the reasons to combine the teachings of Lee and Zhao, Petitioner asserts that a person having ordinary skill in the art would add Lee's teaching to that of Zhao for claims 1–9 and 11–19 to result in collections of drain-side word lines receiving increasingly higher pre-charge voltages corresponding to their distance from the selected word line because it would result in a more effective mitigation of program disturb through Lee's grouping of word lines to offset the relatively high *channel* resistance of when programming word lines closer to the source-side of a memory string. *Id.* at 65–66 (citing Ex. 1003 ¶¶ 356–363). Petitioner also asserts that Lee furthers Zhao's goal of avoiding voltage differentials in the channel of an unselected NAND string because Lee ensures a uniform channel voltage; moreover, that this represents arranging old elements with each performing their known function. *Id.* at 67 (citing Ex. 1005, 2:10–26, 4:7–10, 18:52–59, 22:65–23:12; Ex. 1004, 7:61–62, 8:47–52; Ex. 1003 ¶¶ 364–371).

Patent Owner argues that Petitioner's reasons to combine Lee and Zhao with respect to claims 1–9 and 11–19 are deficient. Prelim. Resp. 36–

37. Specifically, Patent Owner argues that there is no need to replace $V_{precharge}$ with multiple pre-charge signals in the manner proposed. *Id.* at 41–42 (citing Ex. 2001 ¶ 45). Patent Owner further argues that because Zhao sets a voltage too low to turn on memory cells, current between source side select transistor and drain side select transistor is precluded, and therefore, Petitioner’s reasoning based on offsetting a resistance component between the transistors is precluded. *Id.* at 39–41 (citing Ex. 1005, 19:22–26, 8:25–29; Ex. 2001 ¶¶ 42–44). Patent Owner further argues that Lee uses preset bias levels for every word line and applies a pre-charge voltage to every memory cell in the string, which is distinct from Zhao’s technique of electrically coupling the ends of the channel but not conducting between the transistors at the ends of the memory string. *Id.* at 42–44.

In furtherance of advancing this issue for trial, we note that at this stage, the declarants disagree on technical aspects of the combination. Dr. Lui attests that Lee’s different pre-bias voltages would offset effects caused by the resistance component to allow a uniform precharge level in the entirety of the cell string, which occurs because “Zhao’s original implementation would result in using a single precharging voltage of $V_{precharge}$ on the drain side of the selected memory cell[, and d]ue to the channel resistance effect, the full $V_{precharge}$ on the bitline would be attenuated greatly at the WL that is closest to the top select gate line.” Ex. 1003 ¶¶ 340, 358. However, Dr. Przybylski attests that Zhao’s V_{ss} (either zero or nonzero) cuts off the memory cell’s channel and precludes any current flow between source select transistor and drain select transistor, resulting in no voltage drops along the length of the string, and thereby negates the need for replacing $V_{precharge}$ with multiple signals as per Lee. Ex. 2001 ¶ 45. These competing factual attestations appear irreconcilable

on the current record, except to the extent that they indicate that Petitioner's asserted combination is not a simple arrangement of old elements that "yield no more than one would expect from such an arrangement." *See KSR v. Teleflex*, 550 US 398, 406. Accordingly, we invite the parties to further develop these arguments at trial, to the extent permitted by our rules.

G. Obviousness over Yang

Petitioner asserts that claims 1–7, 9, 11–17, and 18–19 would have been obvious over Yang. Pet. 71–89. Because we have determined that institution is appropriate for at least one claim, we institute for all claims and all grounds, and we need not further determine whether Petitioner has shown that institution is proper for its assertions based upon Yang. In furtherance of the record for trial, we address Petitioner's assertion that Yang renders obvious three signals applied to three groups of word lines that have incrementally increasing voltage levels in view of Patent Owner's counter-arguments.

With respect to the limitation ([1.E.4]) at issue, Petitioner admits that "Yang does not provide numerical examples for all of its different pre-charge voltages." Pet. 81. However, Petitioner asserts that a person having ordinary skill in the art would have understood Yang to render this obvious. *Id.* In applying Yang, Petitioner asserts that the claimed first signal is taught by Yang's Vbypass signal, the claimed second signal is taught by Yang's Vpre_dmy signal, and the claimed third signal is taught by Yang's Vpre_OD signal. *Id.* Petitioner further asserts that Yang teaches that:

"overdrive voltage Vpre_OD" is a high voltage "above all the data states" of the memory cells. The "bypass voltage" Vbypass can be a low voltage: it can be lower than all the various memory cell read states and is only required to be higher than Vev (the "voltage level to test whether a memory cell has been properly

erased”). The “dummy pre-charge voltage” V_{pre_dmy} can be an intermediate voltage like 5V that is lower than V_{pre_OD} .

Pet. 82 (citing Ex. 1010, 20:53–55, 19:23–44, 20:64–21:5, 24:18–27).

Patent Owner argues that Petitioner’s assertions are unsupported and do not establish any relationship of the relative magnitude of V_{pre_dmy} as it relates to V_{bypass} . Prelim. Resp. 47–49. In particular, Patent Owner contends that Petitioner has insufficiently explained the basis for its asserted relationship, because Petitioner does not clearly show support in the record for its assertions that V_{pre_OD} need be higher than 5V, and that V_{ev} is smaller than 5V, during precharge. Patent Owner’s arguments appear to have merit, and we invite the parties to further develop these arguments at trial, to the extent permitted by our rules.

III. CONCLUSION

For the reasons discussed above, we conclude Petitioner has shown a reasonable likelihood of prevailing with respect to at least one of claims 1–9 and 11–19. We determine that the record supports institution. Accordingly, we institute an *inter partes* review of all challenged claims under all grounds set forth in the Petition. 37 C.F.R. § 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”); see *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (noting that the language of 35 U.S.C. § 314(b) “indicates a binary choice—either institute review or don’t”); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute as requiring “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

Our determination at this stage of the proceeding is based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which an *inter partes* review has been instituted. Our final decision will be based on the full record developed during trial.

IV. ORDER

For the foregoing reasons, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted for all asserted grounds on all asserted claims, i.e.:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3, 6, 11–13	103	Lee
1, 4–7, 9, 11, 14–16, 18–19	103	Zhao
1–9, 11–19	103	Zhao, Lee
1–7, 9, 11–16, 18–19	103	Yang

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

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