

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00795

Patent 11,501,822

PATENT OWNER'S RESPONSE

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LIST OF EXHIBITS

Exhibit ("Ex.")	Description
2001	July 17, 2024, Declaration of Dr. Steven Przybylski ("Przybylski")
2002	U.S. Pat. No. 11,081,164 ("the '164 patent")
2003	Reserved
2004	U.S. Pat. No. 10,700,157 ("Chen")
2005	U.S. Pub. 2011/0194351 ("Kim")
2006-09	Reserved
2010	July 17, 2024, Declaration of Jonathan Bradford
2011	January 3, 2025, Declaration of Dr. Steven Przybylski ("PrzyblyskiII")
2012	Pulse, Wiley Electrical and Electronics Engineering Dictionary (2004)
2013	Pulse, IEEE Standard Dictionary (1996)
2014	Pulse, Webster's II New College Dictionary (2001)
2015	Micron's Preliminary Claim Constructions and Extrinsic Evidence Pursuant to Patent Local Rule 4-2, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , N.D. Cal. 3:23-cv-05792-RFL (Aug. 5, 2024) ("Micron's Preliminary Claim Constructions")
2016	Dispose, Merriam-Webster's Dictionary and Thesaurus (2014)
2017	Dispose, Merriam-Webster's Collegiate Dictionary (2012)
2018	Dispose, American Heritage Dictionary of the English Language (2011)
2019	Dispose, New Oxford American Dictionary (2010)
2020	Series of Images, Stamped as Ex. 2020 in the December 17, 2024, Deposition of Dr. David Kuan-Yu Liu

2021	Transcript of the December 17, 2024, Deposition of Dr. David Kuan-Yu Liu (“Liu Tr.”)
2022	Hambley, “Electrical Engineering Principles and Applications, Fourth Edition” (2008) (“Hambley”)
2023-2029	Reserved
2030	January 3, 2025, Declaration of Jonathan Bradford

LIST OF ABBREVIATIONS

Abbreviation	Term
'822	U.S. Pat. No. 11,501,822 (Ex. 1001)
Aritome	Aritome, “NAND Flash Memory Technologies” (2016) (Ex. 1006)
Brown	Brown et al., “Nonvolatile Semiconductor Memory Technology” (1998) (Ex. 1007)
Cappalleti	Cappelletti, et al., “Flash Memories” (1999) (Ex. 1008)
Challenged Claims	'822, Claims 1-9 and 11-19
Chen	U.S. Pat. No. 10,770,157 (Ex. 2004)
Hambley	Hambley, “Electrical Engineering Principles and Applications, Fourth Edition” (2008) (ex. 2008)
Kim	U.S. Pub. No. 2011/0194351 (Ex. 2005)
Liu	Declaration of Dr. David Kuan-Yu Liu (Ex. 1003)
Lee	U.S. Pat. No. 10,121,529 (Ex. 1004)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,501,822 (IPR2024-00795, Paper 1)
Parallel District Court Litigation	<i>Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.

POSITA Person of ordinary skill in the art

Przybylski I	July 17, 2024, Declaration of Dr. Steven Przybylski (Ex. 2001)
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PrzybylskiII	January 3, 2025, Declaration of Dr. Steven Przybylski (Ex. 2011)
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Yang	U.S. Pat. No. 10,726,920 (Ex. 1010)
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Zhao	U.S. Pat. No. 10,643,718 (Ex. 1005)
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I. INTRODUCTION

The references in Petitioner’s Grounds, either alone (Grounds 1, 2, 4) or in combination (Ground 3), fail to disclose or render obvious the Challenged Claims of U.S. Patent No. 11,501,822 (“’822,” Ex. 1001). For example, the art fails to disclose or render obvious the use of three distinct “word line pre-pulse signal[s]” with incrementally increasing voltages being applied to groups of word lines during a pre-charge period as recited in the independent claims 1 and 11. Further, Petitioner fails to present evidence that the modifications necessary for its proposed Grounds were suggested or otherwise motivated at the time of the invention, or that there was at the time a reasonable expectation that the modifications would succeed. Instead, Petitioner relies on conclusory expert testimony, misrepresentations, and pure hindsight. As set forth herein, the Grounds presented in the Petition fail to make the required showing of obviousness. This Patent Owner Response is supported by the declaration of Dr. Steven Przybylski. See Ex. 2010 (“PrzybylskiII”), ¶¶1-26.

II. THE ’822 PATENT

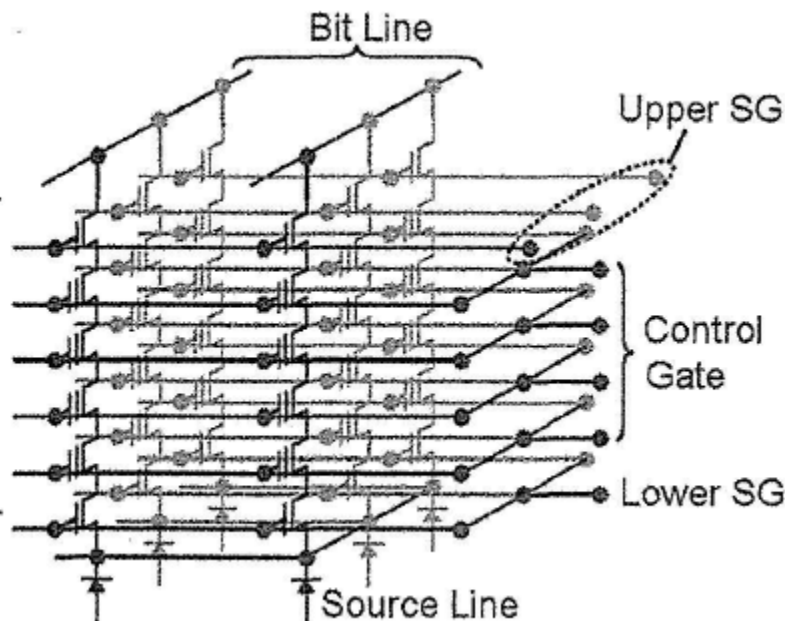
The ’822 discloses a novel pre-charging process for applying signals to word lines of a three-dimensional non-volatile flash memory device to mitigate the effects of “programming disturb,” which is when the programmed state of a memory cell is inadvertently altered by a programming operation performed on adjacent memory cells, caused by electrons trapped in the vertical channels of the memory

device. '822, 1:52-55; *see also* Ex. 1006 (“Aritome”) at 52; Ex. 1007 (“Brown”) at 239; Ex. 1008 (“Cappelletti”) at 32 (describing program disturb generally). The prior art at the time of the '822 sought to address programming disturb by employing a pre-charging process, however methods at the time had drawbacks on memory device programming speed and increased the risk of transistor breakdown. '822, 1:41-48. PrzybylskiII, ¶¶27-28.

The '822 introduced a novel pre-charging process that reduced programming disturb without compromising device-level performance. '822, 1:53-55. The new pre-charging process taught by the '822 and recited in the claims is characterized by several features not found in or rendered obvious by the prior art, including the application of three pre-pulse signals of incrementally increasing voltages levels to three different groups of word lines during a pre-charge period. *See* '822, 1:56-2:27, claims 1, 11. By virtue of applying incrementally increasing pulse signals, the overall duration of the pre-charging process is kept short and voltage levels are minimized, which limits adverse effects on the programming speed of the memory device and improves the longevity of the device circuitry. '822, 1:41-48. Thereby, the '822 invention overcomes the drawbacks of the prior art. *See, e.g.*, '822, 1:20-48. PrzybylskiII, ¶29.

3D NAND flash memory technology architecture has been developed to vertically stack memory cells across multiple layers to increase bit density and

storage capacity as compared to traditional NAND memory. '822, 1:29-32. In general, 3D NAND flash memory organizes memory cells into vertically stacked “strings” of memory, which intersect with horizontally arranged “word lines” that can be used to apply voltages onto each of the individual memory cells. See '822, 2:43-3:2. These vertically stacked “memory strings” are then placed together to form a full three-dimensional array.



Ex. 1006, 296. Each memory cell is transistor with a variable “threshold voltage” (i.e., the voltage that, when applied to the gate terminal of the memory cell, will cause the transistor to turn on) corresponding to the stored state of the memory cell. See, e.g., Ex. 1007 (“Brown”) at 30-32 (describing basic transistor operation); Ex. 1008 (“Cappelletti”) at 14-17 (same). Voltages can be applied to the gate terminal of each memory cell using the corresponding “word line,” and the voltages can be

applied to the channel formed between the source and drain of each memory cell (which collectively form a long channel that runs along the entire length of the memory string) using the bit line and source line that are connected on either end of the memory string. See Ex. 1006 (“Aritome”), 42-49. At the top and the bottom of each memory string are also “select gate” transistors that can be used to selectively control which of the memory strings is connected to the bit line and source line at any given time. *Id.* 295-296. PrzybylskiII, ¶30.

During a typical programming operation, a high programming voltage (V_{pgm}) is applied to the word line connected to the memory cell that is being programmed—also known as the “selected” word line—while 0V (or another low voltage) is applied to the bit line of the memory string containing the memory cell being programmed. Ex. 1006, 42-46. The large voltage difference between the programming voltage and the 0V bit line voltage causes electrons to be injected into the storage layer of the memory cell, thus changing the threshold voltage of that memory cell. *Id.*, 45-46. To ensure that the voltage being applied to the bit line reaches the memory cell being programmed, a “ V_{pass} ” voltage large enough to turn on the memory cell transistors, but not large enough to cause unwanted programming, is applied to all unselected word lines during the programming operation. *Id.*, 44-46. Additionally, because the selected word line also intersects many other unselected memory strings that are not being programmed, an “inhibit”

voltage is applied to these strings' bit lines (as compared to the 0V applied on the selected memory string that contains the memory cell being programmed) that prevents undesired programming by reducing the voltage difference between V_{pgm} and the bit line voltage on the unselected memory strings. *Id.*, 46. PrzybylskiII, ¶¶31-32.

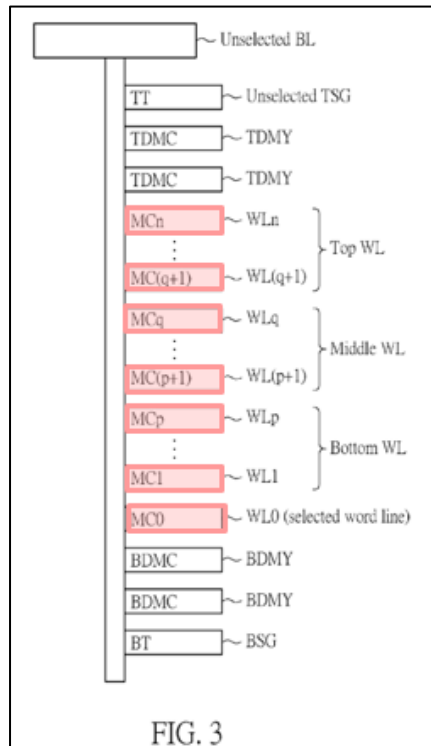
However, as the number of vertical layers and bit density increases, the effects of programming (or program) disturb are exacerbated. '822, 1:32-33. As was understood in the art, programming disturb is a phenomenon in non-volatile memory devices when the programmed state of a memory cell is inadvertently altered due to a programming operation performed on adjacent, selected memory cells, causing data corruption and reducing the reliability and integrity of stored data. *See, e.g.*, Aritome, 52; Brown, 239; Cappelletti, 32-33 (describing program disturb in general). PrzybylskiII, ¶33.

To help mitigate programming disturb, a pre-charge operation is performed to remove boosting charges (electrons) from unselected memory strings prior to a programming operation. '822, 1:34-38. However, as more layers are added to the memory device architecture, it becomes increasingly difficult for pre-charge operations to remove electrons from the bottom-most layers of the device. '822, 1:38-41. Traditional systems attempted to compensate for this reduced effect by, for example, increasing the duration of the pre-charging period—thus increasing the

overall programming time of the device—or by increasing the voltage levels used during the pre-charge operation, but such methods have significant drawbacks that adversely effect data programming speeds and increase the risk of transistor breakdown. '822, 1:38-48. By comparison, the inventors of the '822 developed an improved pre-charging operation to mitigate the effects of programming disturb in memory devices, while avoiding the drawbacks associated with traditional methods. '822, 1:48-55. PrzybylskiII, ¶34.

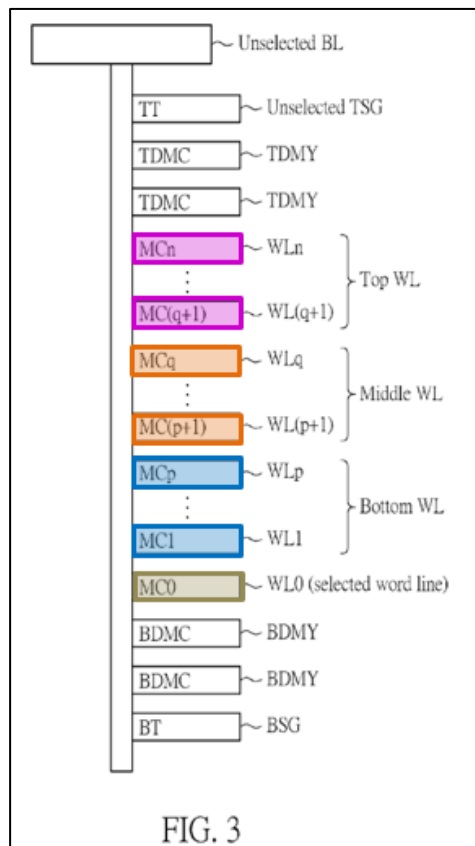
The '822 mitigates program disturb in non-volatile memory devices by introducing a novel method of applying multiple pre-pulse signals to memory device word lines, with each signal having a different voltage level. This is done by grouping the word lines within the memory string, and then applying different pre-pulse signals to each group, with the voltage level of each pre-pulse signal being larger than the last one. For example, as shown in Figure 3 below, a memory device may have a plurality of memory strings that each includes: a top select gate transistor (“TSG”) that controls when the memory string is connected to the bit line (“BL”), at least one top dummy memory cell (“TDMY”) and one bottom dummy memory cell (“BDMY”) that do not store data but which may electrically isolate portions of the memory string from the rest of the device, a plurality of memory cells that are “configured to store data,” and a bottom select transistor (“BSG”) that control when the memory string is connected to a source line. '822, 3:6-9, 3:18-19. The memory

cells are then placed in series “between the top dummy memory cell and the bottom dummy memory cell” with a **word line (“WL”)** being connected to the gate terminal of each memory cell that is used to control the voltages applied to each memory cell within the string. ’822, 3:20-23, 3:26-29. PrzybylskiII, ¶35.



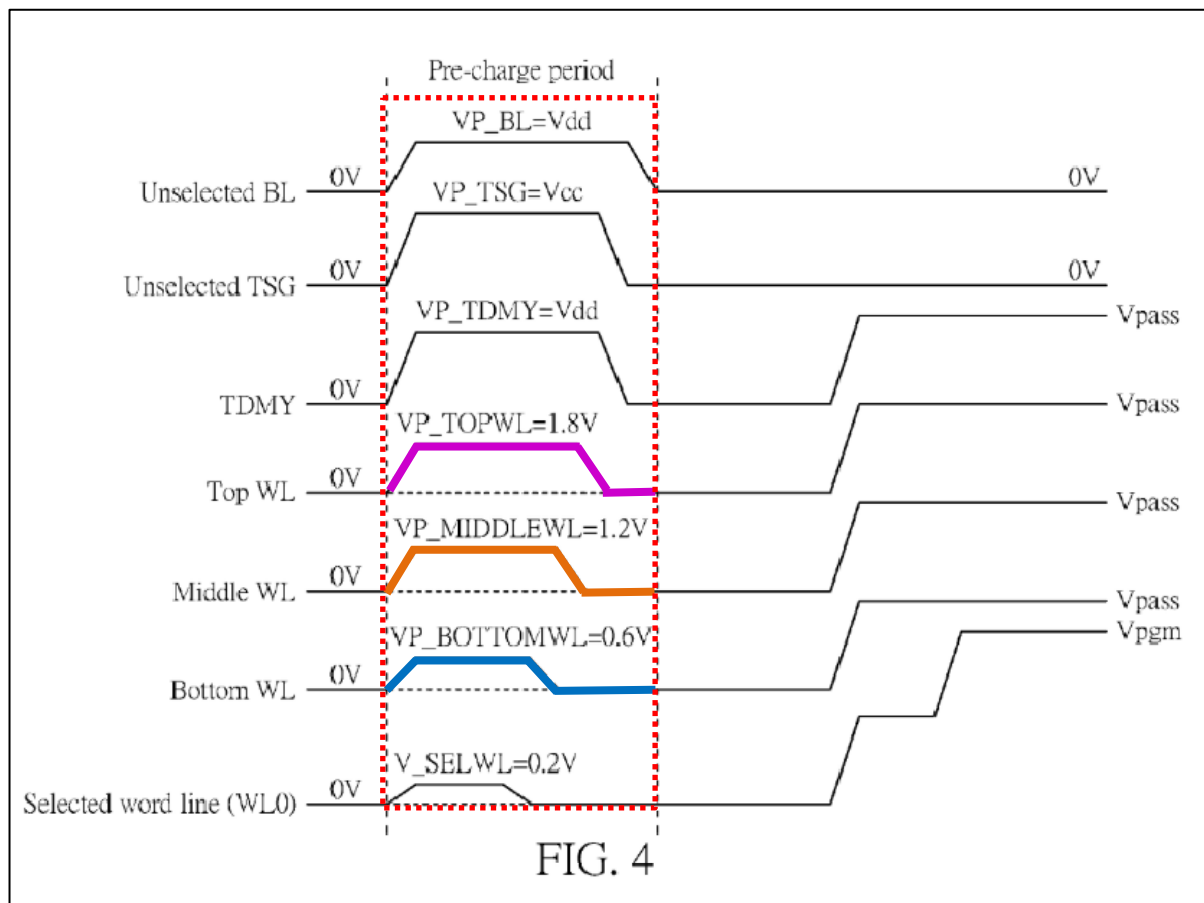
The ’822 teaches using a “control circuit” to apply “word line pre-pulse signals” to the word lines “disposed between the selected word line and the top dummy word line TDMY (or the top select gate TSG)” “during a pre-charge period” that occurs “before programming.” ’822, 3:43-46, 3:55-59. That is, in this arrangement, the ’822 teaches applying the pre-charging operation to word lines **above** the selected word line, on the drain side of the selected memory cell closer to the TDMY or TSG. In some embodiments, the control circuitry also applies a

“dummy word line pre-pulse signal” to “top dummy word lines TDMY” and “bottom dummy word lines BDMY.” ’822, 3:59-65. For example, as shown in Fig. 3 below, word lines disposed between the **selected word line** and TDMY (or TSG) may be “divided into multiple groups of ... word lines”: a “**first group of word lines**” including word line WL1 through word line WLp, a “**second group of word lines**” including word line WL(p+1) through word line WLq, and a “**third group of word lines**” including word line WL(q+1) through word line WLn. ’822, 4:66-5:2, 5:18-34. PrzybylskiII, ¶36.



During the “pre-charge period,” three different word line pre-pulse signals with different voltage levels are applied to these three groups of word lines. For example,

in the embodiment illustrated in Fig. 4, a **first word line pre-pulse signal** VP_BOTTOMWL is applied to the first group of word lines (“Bottom WL”), a **second word line pre-pulse signal** VP_MIDDLEWL is applied to the second group of word lines (“Middle WL”), and a **third word line pre-pulse signal** VP_TOPWL is applied to the third group of word lines (“Top WL”) during the **pre-charge period**. ’822, 5:50-55. PrzybylskiII, ¶37.



As shown in Fig. 4, the voltage level of the word line pre-pulse signals is incremental, with the VP_BOTTOMWL signal having the lowest voltage level (0.6 volts), VP_MIDDLEWL having an intermediary voltage level (1.2 volts), and VP_TOPWL

having the highest voltage level (1.8 volts). '822, 5:65-6:4. In this embodiment, a top dummy word line pre-pulse signal, VP_TDMY, applied to dummy word lines has a separate voltage level (Vdd) that is greater than the voltage levels for VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL. '822, 6:4-8. Similarly, the pre-pulse signal for the selected word line, V_SELWL, has a voltage level (0.2 volts) that is lower than the voltage levels for VP_TOPWL, VP_MIDDLEWL and VP_BOTTOMWL. '822, Fig. 4, 5:62-64. PrzybylskiII, ¶38.

By supplying different pre-pulse voltages to the word lines disposed between the selected word line and the top select gate, the channel potential gradient is enhanced, which favorably influences the distribution and movement of channel-trapped electrons and prevents electrons from accelerating into unselected memory cells during a programming operation. See '822, 7:37-47. And by using multiple pre-pulse signals to create a channel potential gradient, the overall duration of the pre-charge period and the voltage levels applied during the pre-charge period are reduced, resulting in a faster programming time and less risk of transistor breakdown phenomenon as compared to conventional systems. See '822, 1:38-48. Accordingly, the claimed pre-charging process of the '822 improved over the prior pre-charging methods. PrzybylskiII, ¶¶39-40.

Independent Claim 1 of the '822 is an apparatus claim directed to aspects of the above-described invention:

[1.pre] A memory device, comprising:

[1.a] a plurality of memory strings;

[1.b] a bit line connected to a first memory string of the plurality of memory strings;

[1.c] a select gate line connected to the first memory string of the plurality of memory strings;

[1.d] a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string; and

[1.e] a control circuit configured to:

[1.e.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period;

[1.e.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[1.e.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,

[1.e.4] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

Independent Claim 11 of the '822 is a method claim directed to aspects of the above-described invention:

[11.pre] A method of controlling a memory device, the memory device comprising a plurality of memory strings, a bit line connected to a first memory string of the plurality of memory strings, a select

gate line connected the first memory string of the plurality of memory strings, a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string, the method comprising:

[11.a] applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period;

[11.b] applying a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during the pre-charge period;

[11.c] applying a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[11.d] applying a third word line pre-pulse signal of the plurality of word line pre-pulse signals to a third group of the plurality of word lines during the pre-charge period;

[11.e] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

III. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this proceeding only, Patent Owner does not object to the definition of a person of ordinary skill in the art (“POSITA”) proffered by Petitioner and adopted by the Board at institution—i.e., a person with “a bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND memory devices (including issues relating to the operation, e.g., programming, of said

devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 18. The Challenged Claims are valid regardless of the precise definition used for a POSITA. PrzybylskiII, ¶¶41-45.

IV. CLAIM CONSTRUCTION

Other than the terms identified below, Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of the *inter partes* review. Patent Owner, however, reserves the right to modify or elaborate on its proposed constructions and to raise further claim construction issues in the parallel district court proceedings. PrzybylskiII, ¶46.

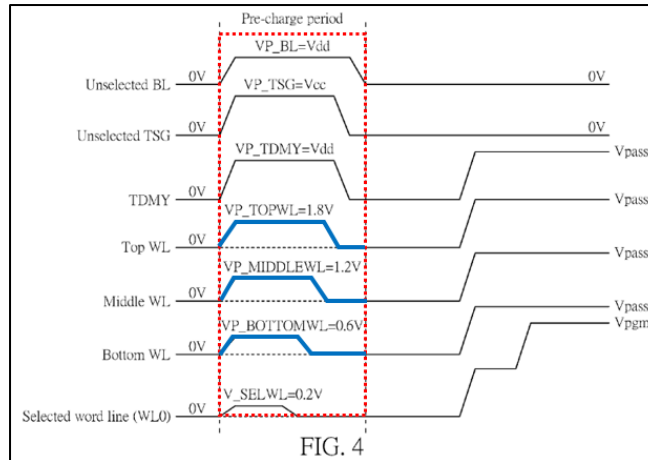
A. “Word Line Pre-Pulse Signal”

For purposes of this proceeding, Patent Owner agrees with Petitioner that the term “word line pre-pulse signal” should be construed as a “pulse signal to prepare word lines for a programming step” wherein a “pulse” is a “signal that must increase in value and then decrease in value (or vice versa).” That construction is supported by the intrinsic record. First, the ’822 claims support the construction. For example, claim 1 recites applying a “word line pre-pulse signal” during a “pre-charge period,” which the specification explains is “before programming.” ’822, 3:43 (“[d]uring a pre-charge period (before programming)”). Thus, the pre-pulse signal prepares the

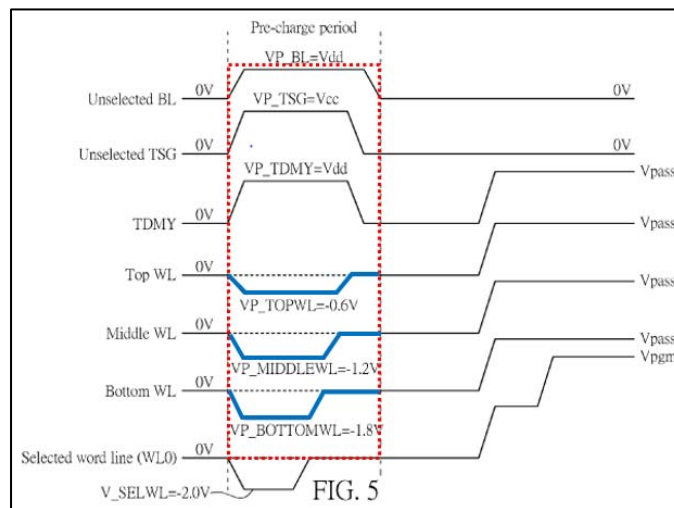
word line before the programming step. In addition, the claims confirm that the “pre-pulse signal” is in the form of a pulse, which has a “duration” and thus a beginning and an end. For example, claim 20 recites that the “pulse duration of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal,” and that the “pulse duration of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.” *Id.*, 10:20-24. PrzybylskiII, ¶¶47-48.

The specification further confirms that a “word line pre-pulse signal” refers to a pulse signal applied to word lines in preparation for a programming step. For example, the specification describes “word line pre-pulse signals” as either “positive pulse signals” (*id.*, 6:61-66) or “negative pulse signals” (*id.*, 6:11-19) that each have an associated “pulse duration” within the pre-charge period (*id.*, 7:19-36). *See also id.*, 1:15-19 (“applying word line pre-pulse signals” is for “reducing programming disturb”), 3:43-46 (the “pre-charge period” is “before programming”), Figs. 4-5 (depicting the word line pre-pulse signals as pulses during the pre-charging period). PrzybylskiII, ¶49.

The specification further confirms that a “pulse” must increase in value and then decrease in value (or vice-versa). For example, as shown in Fig. 4, each of the illustrated “word line pre-pulse signals” is a “positive pulse” that increases in value to a fixed level before decreasing in value during the pre-charge period.



'822, 6:61-7:6, Fig. 4. Similarly, in the preferred embodiments illustrated in Fig. 5, each of the illustrated “word line pre-pulse signals” is a “negative pulse” that decreases in value to a fixed level before increasing in value during the pre-charge period.



'822, 7:6-18, Fig. 5. The specification also further confirms that a “pulse” has a “duration” and thus must be denoted by a beginning and an end. '822, 7:19-36. PrzybylskiII, ¶50.

Increasing in value and then decreasing in value (or vice-versa) is also consistent with the plain and ordinary meaning of the term pulse. Indeed, dictionary definitions of the term “pulse” that were cited by Micron in the parallel district court proceeding require at least some type of rise and fall as part of a “pulse.” *See e.g.*, Ex. 2012 (Pulse, Wiley Electrical and Electronics Engineering Dictionary (2004)) (“a well defined variation which increases from a steady value to a maximum, **then back to or near the original value**, all in a comparatively short time); Ex. 2013 (Pulse, IEEE Standard Dictionary (1996)) (“[a] wave that departs from an initial level for a limited duration of time **and ultimately returns** to the original level”); Ex. 2014 (Pulse, Webster's II New College Dictionary (2001)) (“A transient amplification or intensification of a characterization ... of a wave characteristic, **followed by return** to equilibrium or steady state”); *see also* Ex. 2015 (Micron’s Preliminary Claim Constructions) at 4-5 (listing Petitioner’s evidence regarding its proposed construction of “word line pre-pulse signal”). PrzybylskiII, ¶51.

Additionally, as recognized by the Board in the Decision to Institute (“DI”), both parties interpret the term “word line pre-pulse signal” to at least require a pulse signal that is used to prepare word lines for a programming step. *See* DI 7 (“Petitioner applies the same understanding of the phrase in its Petition, at least to the extent that Petitioner has not suggested that such a pulse would encompass a flat voltage signal.”). The fact that a “word line pre-pulse signal” is itself a pulse is

further confirmed by Petitioner’s proposed construction in the parallel district court proceeding: “***a signal that increases in value and then decreases in value (or vice versa)*** before a programming step.” Ex. 2015 at 4. Thus, according to Petitioner’s construction: (1) the word line pre-pulse signal is itself a pulse; and (2) at minimum a pulse signal must increase in value and then decrease in value (or vice-versa). *Id.*¹ PrzybylskiII, ¶52.

¹ Notably, during deposition Petitioner’s expert Dr. Liu was unable and unwilling to define the term “pulse,” or to say with any certainty whether example waveforms would or would not qualify as a “pulse”: “Q. What is a pulse? I don’t know. I’m not here to define the pulse....” Ex. 2021 (Liu Tr.) at 25:19-25; *see also id.*, 39:7-25 (refusing to comment on whether example waveforms in Ex. 2020 constitute a pulse), 41:3-44:25. Indeed, Dr. Liu could not tell whether any waveform shown in Ex. 2020 (charting voltage compared to time) constitutes a pulse. *Id.* 29:14-62:3 (generally refusing to answer questions concerning Ex. 2020 regardless of context); *see, e.g., id.* 44:7-25 (refusing to answer any questions concerning Ex. 2020; “...are you willing to answer any of my questions about this document? No”), 45:1-46:2 (refusing to answer outside the context of the ’822), 57:23-62:3 (refusing to answer whether a waveform would constitute a pulse if the waveform appeared as part of Figure 4 of the ’822). PrzybylskiII, ¶53.

It is not necessary for the Board to construe the term further to resolve the arguments presented. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (The Board is required to construe terms “only to the extent necessary to resolve the controversy.”). Even under Petitioner’s proposed construction, the Grounds presented in the Petition fail to render obvious the Challenged Claims. PrzybylskiII, ¶54.

**B. “Disposed in an Order of Distance from the Selected Word Line”
/ “Disposed Adjacent to the Selected Word Line”**

Because the Grounds raised in the Petition fail to disclose or render obvious the limitations of independent claims 1 and 11, the Board does not need to construe any terms in the remaining dependent claims. But if the Board reaches the issue of whether the added limitations of dependent claims 2 and 12 are disclosed or rendered obvious by the prior art, the plain and ordinary meaning of the term “disposed in an order of distance from the selected word line” requires that the word line groups be disposed in order based on the location of the selected word line. Similarly, as used in claims 3 and 13, the plain and ordinary meaning of the term “the first group of the plurality of word lines are disposed adjacent to the selected word line” requires that group to be disposed adjacent to the location of the selected word line. As discussed further below in Sections VI.B, VI.C, IX.B, and IX.C, those limitations are not satisfied by predetermined groups, such as those disclosed by Lee and Yang, that remain the same regardless of where the selected word line is located. That

interpretation, which is implicit in Petitioner’s mappings for at least Grounds 1 and 4, ignores the plain meaning of the word “disposed.” PrzybylskiII, ¶55.

Patent Owner’s construction is confirmed by the ’822 specification. As described by the ’822, once a word line (e.g., WL0) is chosen as the selected word line, “the word lines WL1 to WLn are divided into a first group of word lines (Bottom WL), a second group of word lines (Middle WL) and a third group of word lines (Top WL).” ’822, 5:18-22. *See also* ’822, 5:24-34 (“The first group of word lines (Bottom WL) is between the selected word line (word line WL0) and the second group of word lines (Middle WL)”). PrzybylskiII, ¶56.

That understanding is also confirmed by the plain meaning of “disposed.” Indeed, the dictionary definition of “disposed” requires objects to be “arrange[d] in a particular position” or to be “put in place,” further confirming that groups “disposed in an order of distance from the selected word line” must be arranged into position based on the location of that word line. *See e.g.*, Ex. 2016 (Dispose, Merriam-Webster’s Dictionary and Thesaurus (2014)) (“to put in place”); Ex. 2017 (Dispose, Merriam-Webster’s Collegiate Dictionary (2012)) (same); Ex. 2018 (Dispose, American Heritage Dictionary of the English Language (2011)) (“To place or set in a particular order; arrange”); Ex. 2019 (Dispose, New Oxford American Dictionary (2010)) (“arrange in a particular position”). PrzybylskiII, ¶57.

Moreover, Petitioner also recognizes that in “dependent claims 2-3 and 12-13,” the claimed “groups” will be chosen based on the location of the “currently selected” word line that has been chosen for programming. Pet. 2. PrzybylskiII, ¶58.

Thus, as confirmed by plain meaning of the claims and the specification, claims 2-3 and 12-13 require that the word line groups be disposed in order based on the location of the selected word line. PrzybylskiII, ¶59.

V. THE PRIOR ART REFERENCES RELIED UPON²

A. U.S. Pat. No. 10,121,529 (“Lee”) (Ex. 1004)

Petitioner does not contend that Lee anticipates the Challenged Claims, and instead argues that it only renders obvious certain claims, including the independent Challenged Claims. Pet., 6, 26-41. Lee is purportedly directed to “a semiconductor memory device configured to mitigate a program disturb phenomenon, and a method of operating the semiconductor memory device.” Lee, 1:53-56; *see also* Lee 7:37-58. However, the ’822 and Lee employ disparate techniques for addressing program disturb. The ’822 mitigates program disturb resulting from “boosting charges” by using pre-pulse signals to create a “*channel potential gradient*” during a pre-charge period, thus removing unwanted charge. *See* ’822, 1:20-48, 4:54-59, 7:37-42. By

² For the purposes of the present IPR proceeding only, Patent Owner does not contest that the Lee, Zhao, and Yang references qualify as prior art to the ’822.

comparison, Lee seeks to create a more “**uniformly formed**” **charge** throughout the device by compensating the “**resistance component** between the source select transistor and the drain select transistor.” Lee, 7:58-62, 8:25-52. PrzybylskiII, ¶¶60-61.

Specifically, Lee states that during a “typical” precharge operation, “a threshold voltage of a memory cell is increased by a **resistance component** between the source select transistor and the drain select transistor” meaning that “the precharge level in a source select side channel is reduced.” Lee, 8:25-32. In general, when there is current running from the drain select transistor to the source select transistor along the length of the memory string, any resistance along the length of the memory string will create voltage drops which, in turn, may result in a “precharge level” being reduced on the “source select side” of the memory string. See Lee, 8:25-32. To compensate for this and create a uniform level of charge, Lee describes applying “different pre-bias voltages to the respective word line groups” along the entire length of the memory string based on their relative positions within the string. See Lee, 2:63-3:7, 8:3-17. Specifically, Lee discloses that “the closer a word line group to which a word line belongs is to the drain select transistor, the higher a pre-bias voltage to be applied to the word line may be,” turning on all the memory cells in the memory string in the process. Lee, 8:18-52. PrzybylskiII, ¶62.

But Lee does not disclose any details regarding the “pre-bias voltages” beyond its statements that “different” voltages are used, with some “higher” than others. Lee, 7:58-62, 8:65-9:6. Indeed, Lee does not disclose any waveform or timing characteristics of the voltages applied within its system, does not disclose that the “pre-bias” voltage (or any voltage) would be implemented as a “pulse,” and does not otherwise render obvious that the “pre-bias” voltage would be implemented as a “word line pulse signal” as required by the Challenged Claims. PrzybylskiII, ¶63.

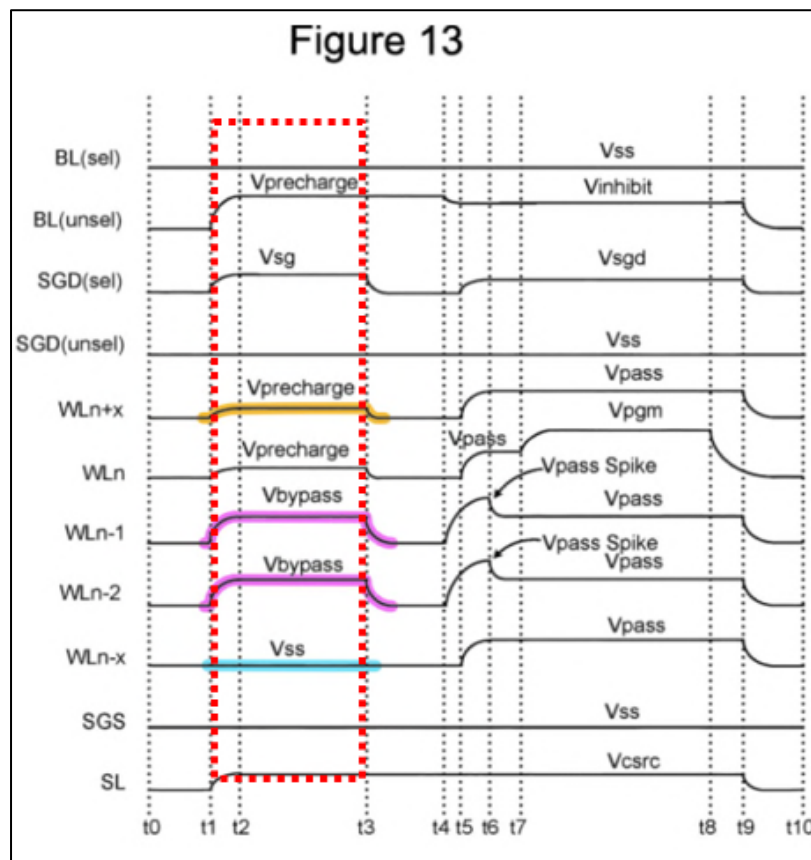
B. U.S. Pat. No. 10,643,718 (“Zhao”) (Ex. 1005)

Petitioner does not contend that Zhao anticipates the Challenged Claims, and instead argues only that that Zhao (Ground 2), or alternately the combination of Zhao and Lee (Ground 3), renders obvious certain claims, including the independent Challenged Claims. Pet., 44-71. Zhao describes “strings” of memory cells, each of which is connected to a corresponding word line. Zhao, 6:34-46; *see also id.* 9:10-18, 11:53-12:13, Fig. 4G. At any given time, one memory cell is “selected” for programing. *See id.* 12:14-41, 27:30-48. Zhao discloses three different possible “countermeasures ... to open the channel from one side of a selected word line to the other side of the selected word line” in order to combat certain types of program disturb. *Id.*, 2:10-26. Zhao describes these as “purging ... the already programmed side of the channel” (*id.* 2:27-49), “applying a voltage spike on one or more already programmed unselected word lines” (*id.* 2:50-3:4), and “delaying the ramping down

of the voltages ... at the conclusion of a program verify process” (*id.* 3:5:24).

PrzybylskiII, ¶¶64-67.

As depicted in Fig. 13, Zhao illustrates these countermeasures using different voltages applied to different wordlines. Starting at time t_0 , “all the depicted signals are at ... 0 volts (V_{ss}),” and the time period “from **t1-t3 corresponds to pre-charging.**” Zhao 22:34-41. PrzybylskiII, ¶68.



Like Lee, Zhao fails to teach or otherwise render obvious the use of three “pre-pulse signals” during a “pre-charge period” as required by the independent claims of the ’822. As previously recognized in the Decision to Institute, Petitioner incorrectly attempts to characterize portions of **Vss**, **Vprecharge**, and **Vbypass**

waveforms as equivalent to the claimed “pre-pulse signals ... during a pre-charge period” recited by the independent claims of the ’822.³ See Pet., 49-52; DI 19. Not only do the purported pre-charging waveforms relied on by Petitioner extend beyond Zhao’s “pre-charging” period, the flat 0 volts (**Vss**) signal identified by Petitioner as being applied to word line WLn-x does not constitute a “word line pre-pulse signal ... during a pre-charge period” even under Petitioner’s own proposed construction as it does not “increase[] in value and then decrease[] in value (or vice versa) before a programming step.” See Section IV.A (Claim Construction); see also Zhao 22:39-23:9 (describing the applied voltages). PrzybylskiII, ¶69.

Indeed, Petitioner seemingly concedes that a flat signal would not satisfy the claim language, and instead mischaracterizes Zhao as disclosing some other “low” voltage being applied in lieu of the flat signal shown in Figure 13. See Pet., 51. But Zhao does not disclose or otherwise render obvious a “word line pre-pulse signal” being applied to those word lines. Rather, Zhao explicitly teaches that the word lines “remain” at a fixed value throughout the relevant time period. See Zhao, 23:7-10; see also Zhao 19:22-26, 23:7-10. Accordingly, Zhao fails to disclose a “word line pre-pulse signal” being applied to word line WLn-x in the purported pre-charge

³ For convenience, Petitioner’s annotations for **Vss**, **Vprecharge**, and **Vbypass** are reproduced above.

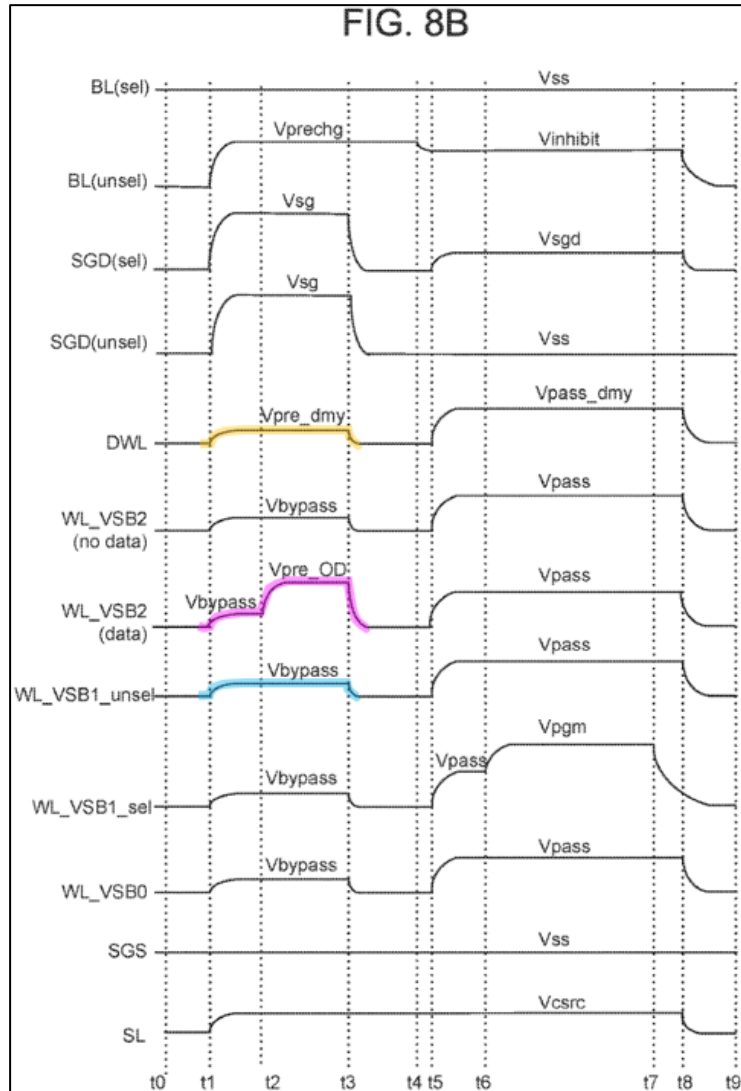
period, and Petitioner has similarly failed to show that it would have been otherwise obvious to implement Zhao's system using three distinct "word line pre-pulse signals" as required by the Challenged Claims. PrzybylskiII, ¶70.

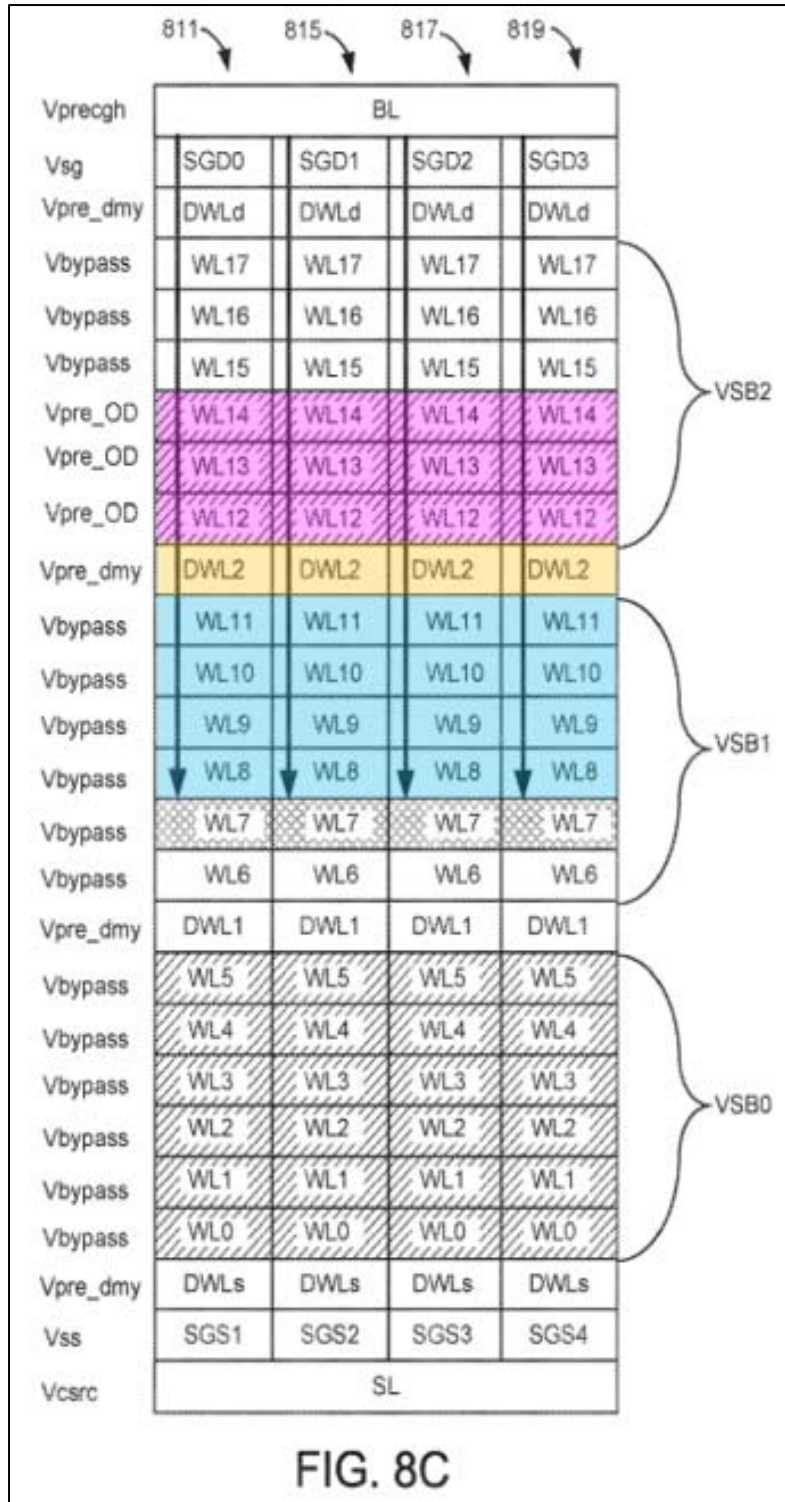
C. U.S. Pat. No. 10,726,920 ("Yang") (Ex. 1010)

Petitioner does not contend that Yang anticipates the Challenged Claims, and again argues that Yang only renders obvious certain claims, including the independent Challenged Claims. Pet., 71-89. Yang purports to address the problem of program disturb in memory cells ("unselected memory cells") surrounding other memory cells that are to receive programming ("selected memory cells"). Yang, Abstract, 2:35-41. Yang purportedly does this by applying voltages to "pre-charge" the channel of unselected memory strings prior to a programming operation, so that the subsequent "boosting voltages" will cause the unselected memory strings to reach a "sufficient voltage during the programming phase" such that "the differential between the channel voltage (of the unselected memory cell) and the ... control gate of [the] unselected memory cell[] will be too small to allow for programming of the unselected memory cell." Yang, 2:42-62, 25:65-26:3. PrzybylskiII, ¶¶71-72.

Yang describes a binary choice where "during a pre-charge phase of a programming operation, an overdrive voltage is applied to some memory cells and a bypass voltage is applied to other memory cells." Yang 3:28-31. For example, as depicted in Figs. 8B and 8C (below), Yang teaches: (1) an **"overdrive voltage"**

(“**Vpre_OD**”) is applied to word lines of “programmed” memory cells, and (2) a “bypass voltage” (“**Vbypass**”) is applied to “not yet programmed” memory cells during the “**pre-charge phase**” depicted at “times t1-t4.” Yang, Figs. 8B-C, 23:19-25, 24:1-17, 24:28-46, 25:9-28. Yang also discloses a “**dummy pre-charge voltage**” (“**Vpre_dmy**”) that is applied to a “dummy” memory cell used to “electrically isolate” sets of memory cells within the string. See Yang, 12:35-43, 24:18-27. PrzybylskiII, ¶73.





Petitioner erroneously attempts to characterize portions of **Vbypass**, **Vpre_dmy**, and **Vpre_OD** as equivalent to the claimed “[first/second/third] word

line pre-pulse signals” applied to a “[first/second/third] group of the plurality of word lines.” See Pet. 23-26, 80-82.⁴ But as recognized in the Decision to Institute, Petitioner’s argument fails to show or otherwise render obvious three distinct “word-line pre-pulse signals” being applied to three distinct groups of word lines, or that the relative voltage levels of the purported “word-line pre-pulse signals” are satisfied by Petitioner’s proposed claim mapping. DI 25. To the contrary, a POSITA would expect the value of **Vbypass** to be the same as the value chosen for **Vpre_dmy** as shown in Fig. 8B. PrzybylskiII, ¶74.

VI. GROUND 1: LEE DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-3, 6, 11-13

Petitioner has failed to show that Lee alone discloses or renders obvious at least limitations [1.e.1]-[1.e.3] and [11.b]-[11.d], or the added limitations of dependent claims 2-3, and 12-13. Regarding limitations [1.e.1]-[1.e.3] and [11.b]-[11.d], Lee does not disclose or render obvious the use of “word line pre-pulse signals.” Specifically, Lee’s “pre-bias” voltages are not applied in the form of pulses, nor has Petitioner shown that a POSITA would have been motivated to modify Lee’s disclosed “pre-bias” voltages to be applied as pulses. As for the added limitations of dependent claims 2-3 and 12-13, Lee does not disclose or render obvious that

⁴ For convenience, Petitioner’s annotations for **Vbypass**, **Vpre_dmy**, and **Vpre_OD** have been reproduced above.

groups are “disposed” based on the locations of the selected word line. PrzybylskiII, ¶¶75-77.

A. Independent Claims: Lee Does Not Disclose or Render Obvious a “[First/ Second/ Third] Word Line Pre-Pulse Signal” Applied “During a Pre-Charge Period” (Limitations [1.e.1]-[1.e.3] and [11.b]-[11.d])

Lee does not disclose or otherwise render obvious limitations [1.e.1]-[1.e.3] and [11.b]-[11.d] at least because Lee’s “pre-bias” voltages (*i.e.*, the purported “word line pre-pulse signals” identified by Petitioner) are not “word line pulse signals” as required by the ’822 Patent. Pet., 26-44. Even under Petitioner’s proposed construction, the term “word line pre-pulse signal” requires—at bare minimum—a signal that “increases in value and then decreases in value (or vice versa).” See §IV.A (Claim Construction). Lee, however, fails to disclose that the purported “word line pre-pulse signals” increase and then decrease in value, and Petitioner’s assertion that a POSITA would have found it obvious for these voltages to be “supplied in the form of a ‘pulse’” is based on nothing more than improper inferences and conclusory expert testimony that conflates the *programming* voltages used to set memory cell values with the claimed *pre-pulse* (or *pre-charge*) signals applied during a pre-charge period. Pet., 37-38. Worse yet, it serves no purpose given Lee’s disclosed desire to obtain a “uniform” pre-charge level in the memory string and needlessly extends programming times, which is why Lee applies a

consistent pre-bias voltage to the word lines and not a pulse. Lee, 7:58-62, 9:7-13, Fig. 7. PrzybylskiII, ¶¶78-79.

Claim 1 recites a control circuit configured to “**apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines** during a pre-charge period” (Element [1.e.1]); “**apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines** during the pre-charge period” (Element [1.e.2]); and “**apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines** during the pre-charge period” (Element [1.e.3]). Analogous limitations are found in Elements [11.b]-[11.d] of independent claim 11, and are common to each of the Challenged Claims. PrzybylskiII, ¶80.

As explained in Section II, the ’822 improves over conventional approaches by using multiple pre-pulse signals to “**enhance**” the “**channel potential gradient ...** thus enhancing the pre-charge effect of the unselected bit line and reducing programming disturb.” ’822, 4:39-59, 7:37-47; *see also id.*, 1:41-44 (describing that the invention avoids the need for using increased voltages or extended data programming times). In contrast, Lee seeks to create a “**uniformly formed**” charge by compensating the “resistance component between the source select transistor and the drain select transistor.” Lee, 7:58-62, 8:25-52. PrzybylskiII, ¶81.

Petitioner incorrectly argues that the “pre-bias” voltages that Lee uses to achieve a uniform charge level render obvious the claimed “pre-pulse signals ... during a pre-charge period” recited by claims 1 and 11 of the ’822. Contrary to what Petitioner asserts, Lee does not disclose that the “pre-bias” voltages are implemented as a “pulse” (or otherwise increase and then decrease in value) as required by the claims. In fact, Lee does not disclose any waveforms or timing characteristics for the voltages applied within its system, and Lee’s stated goal of creating a “uniform” pre-charge level would suggest that pre-bias voltages are applied as a single, flat, value followed immediately by programming voltages, rather than using a pulse. *See* Lee 7:58-62, 9:7-13, Fig. 7. PrzybylskiII, ¶¶82.

Petitioner presents two flawed arguments for why it would have been obvious for Lee’s “pre-bias voltages” to be implemented as “word line pre-pulse signals” within the meaning of the ’822 claims. First, Petitioner asserts that “a POSITA would have understood (or considered it obvious) that Lee’s pre-bias voltages are supplied in the form of a ‘pulse’” based on the combined disclosures that “Lee (1) supplies its pre-bias voltages in a separate and distinct-in-time step, and (2) the pre-bias voltages differ from the later Vp_{gm} and V_{pass} voltages.” Pet., 38-39. That argument is misplaced. Lee does not disclose the signal, waveform, or timing characteristics of the “pre-bias voltages” (or any other voltages), and there is nothing to suggest that the “pre-bias voltages” would be applied in the form of a “pulse” in

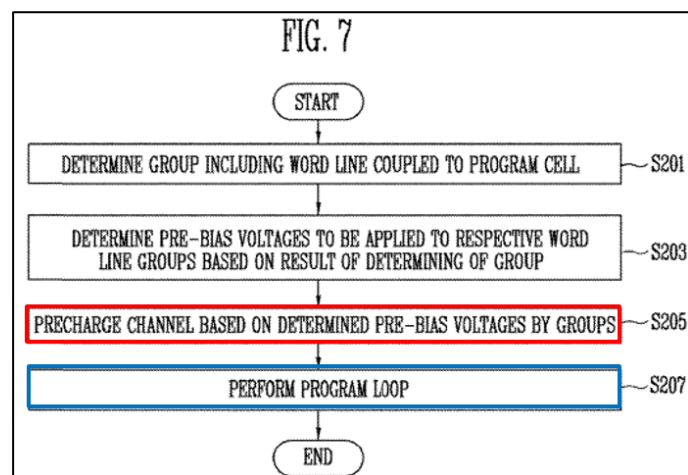
particular. Even assuming—as Petitioner and Dr. Liu contend—that Lee’s pre-bias voltages differ from the voltages applied during a subsequent programming step, that would be true for any number of arbitrary signals. “[T]he breadth of these choices and the numerous combinations indicate that these disclosures would not have rendered the claimed invention obvious.” *Leo Pharm. Prods. v. Rea*, 726 F.3d 1346, 1356 (Fed. Cir. 2013). Nothing in Lee suggests or otherwise renders obvious that pre-bias voltages would take the form of “pulses,” nor has Petitioner presented a cogent argument as to why Lee’s pre-bias voltages would be applied as “pulses” just because they are applied in a distinct period and differ from later voltages. Indeed, Lee is concerned with creating a “uniform precharge level in the entirety of the cell string” followed immediately by programming voltages. See Lee 7:58-62, 9:7-13, Fig. 7. In the context of Lee’s system, using a transient pulse disadvantageously reduces device throughput and slows down the device by extending the total time needed for programming operations. PrzybylskiII, ¶¶83-84.

In the Decision to Institute, the Board credited Dr. Liu’s testimony that Lee’s pre-bias voltages are in the form of “on-off pre-bias voltages” that are cycled on and off, but Dr. Liu’s testimony is unsupported by the record and contradicts Lee’s disclosure. See DI 10-11, citing Liu ¶203. Specifically, Dr. Liu asserts—without any citation to Lee itself—that the pre-bias voltages are “removed prior to commencing the program loop,” and are thus “on-off” voltages that form a pulse. See Liu ¶203.

But Lee says no such thing, and there is nothing to suggest the pre-bias voltages cycled off prior to programming. Indeed, the Petition does not articulate an advantage to applying precharge voltages as pulses in the context of Lee's system. It does not serve Lee's goal of creating a "uniform pre-charge level in the entirety of the cell string" prior to programming, and would slow the device by extending the time required for programming operations. See Lee 7:58-62, 9:7-13, Fig. 7. Rather, Lee teaches that pre-charge voltages are followed immediately by the programming voltages, stating:

After the pre-bias voltage is applied to the respective word lines and the precharge operation is completed, a program voltage may be applied to the selected word line WL10, and a pass voltage may be applied to unselected word lines WL0 to WL9 and WL11 to WL31. The above-mentioned operation is a program loop for memory cells, and the program loop may be repeatedly performed.

Lee, 9:7-13; see also Lee Fig. 7 (showing the "**Program Loop**" immediately following the "**Precharge Channel**" step). PrzybylskiII, ¶85.



Lee, Fig. 7.

At no point does Lee disclose that the bias voltages being used to pre-charge the channel are being raised and then lowered (or vice-versa) before the programming step, as would be required by Petitioner's own construction of the term "word line pre-pulse signal," which Petitioner did not include in its Petition. See §IV.A (Claim Construction). PrzybylskiII, ¶86.

Second, Petitioner also relies on Dr. Liu's conclusory, unsupported testimony to assert that "when the '822 patent was filed, programming voltages were conventionally provided in the form of a 'pulse,'" and suggest that Lee's "pre-bias voltages ... obviously would be supplied as pulses" as well. See Pet., 39; see also Liu Dec. ¶¶ 204-205. That argument is equally misplaced, and conflates **programming voltages** with the claimed **pre-pulse** (or **pre-charge**) signals applied during a pre-charge period. As explained by the '822, the purpose of the invention is to remove boosting charges during a distinct pre-charge period **before** the subsequent programming operation. See '822, 3:43-46 (signals are applied in "**a pre-charge period (before programming)**") (emphasis added); see also *id.* 3:50-65 (describing distinct signals applied in a pre-charging period and the programming period). Petitioner and Dr. Liu identify examples of programming pulses allegedly known in the art, but those pulses are not used in a "pre-charge period" as required by the Claims, and are instead used to set the value of a memory cell in the subsequent programming step. See Pet., 39; Liu Dec. ¶¶ 204-205 (citing Aitome (Ex.

1006) at 44, 116-117, 142-143 (discussing “applying high-voltage, V_{pgm} ” for “programming pulses”); Cappelletti (Ex. 1008) at 354 (a “[p]rogram [p]ulse” is provided to program a “selected cell”)). No portion of the Aritome or Cappelletti background references cited by Petitioner and Dr. Liu discloses signals applied during a pre-charging period, nor has Dr. Liu provided any rationale why using pulses for a subsequent programming step would require or render obvious pulses to be used for pre-charge signals. Indeed, doing so would not serve Lee’s stated goal of “uniformity,” and would slow down the device and reduce throughput by extending the total time needed to perform programming operations as discussed above. *See* Lee 7:58-62, 9:7-13, Fig. 7. As before, Petitioner and Dr. Liu have failed to show that Lee’s pre-bias voltages are supplied in a pulse form, or that it would have been obvious to do so. PrzybylskiII, ¶87.

For at least the reasons provided above, Lee fails to teach or render obvious the claimed process of applying pre-pulse signals to word line groupings as required by each of the independent Challenged Claims. Petitioner’s cited disclosures merely pertain to Lee’s disclosure of pre-bias voltages that are neither expressly disclosed nor obviously supplied as “word line pre-pulse signals” in the sense of the ’822. PrzybylskiII, ¶88.

Lee does not disclose or render obvious dependent claims 2-3, 6, and 12-13 for at least the same reasons. PrzybylskiII, ¶88.

B. Claims 2 and 12: Lee Does Not Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line”

In addition, Lee does not disclose or render obvious the added limitations of dependent claims 2 and 12 requiring that groups of word lines are “disposed in an order of distance from the selected word line.” Rather, Lee teaches that groups are fixed in predetermined locations that do not change based on the position of the selected word line. PrzybylskiII, ¶89.

The added limitations of dependent claim 2 recite, “wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines *are disposed in an order of distance from the selected word line* of the plurality of word lines.” Analogous limitations are found in dependent claim 12. PrzybylskiII, ¶90.

As discussed in Section IV.B (Claim Construction), the plain and ordinary meaning of the term “disposed in an order of distance from the selected word line” requires that the groups be disposed in order based on the location of the selected word line. By comparison, Lee fails to disclose or render obvious that the location of the selected word line has any bearing on how word lines are grouped together. PrzybylskiII, ¶91.

Lee discloses various ways to divide word lines into groups, but in each case, the groups are determined without any regard given to the location of the selected

word line. For example, the embodiment of Fig. 4A divides word lines into “two word line groups” of “sixteen word lines” each, the embodiment of Fig. 4B divides word lines into “four word line groups” of “eight word lines” each, and Fig. 4C divided word lines into groups where the “closer a word line group is to the drain select transistor, the fewer the number of word lines included.” Lee, 8:4-10, 9:36-40, 10:4-12, Figs. 4A-4C. Indeed, Lee discloses that groups are determined **before** a word line is selected for programming, and the pre-bias voltages are determined after the fact based on which group contains the selected word line. See Lee, 10:63-11:9, Fig. 6. At no point does Lee disclose or otherwise render obvious that groups are disposed based on distance to a selected word line, nor has the Petitioner provided any argument to suggest that Lee could be modified to do so. PrzybylskiII, ¶92.

The fact that Lee’s groups are not disposed in an order of distance from the selected word line was further confirmed by Petitioner’s expert. Indeed, Petitioner’s expert was questioned about Fig. 4B of Lee during his deposition. Liu Tr. 23:3-18. When asked directly if the groups were “disposed in an order of distance from the selected word line 11,” Petitioner’s expert instead stated that they were “disposed in order either from the ... bi[t] line or from the source line,” rather than the selected word line. Liu Tr. 25:2-15. PrzybylskiII, ¶93.

For at least the reasons provided above, Lee fails to teach or render obvious that groups “disposed in an order of distance from the selected word line of the plurality of word lines” as required by claims 2 and 12. PrzybylskiII, ¶94.

C. Claims 3 and 13: Lee Does Not Disclose or Render the “First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line”

In addition, Lee does not disclose or render obvious the added limitations of dependent claims 3 and 13 requiring that “the first group of the plurality of word lines are disposed adjacent to the selected word line.” Rather, as discussed above in Section VI.B, Lee teaches that groups are fixed in predetermined locations that do not change based on the position of the selected word line. PrzybylskiII, ¶95.

The added limitations of dependent claim 3 recite, “wherein *the first group of the plurality of word lines are disposed adjacent to the selected word line*, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.” Analogous limitations are found in dependent claim 13. PrzybylskiII, ¶96.

As discussed in Section IV.B (Claim Construction), the plain and ordinary meaning of the term “the first group of the plurality of word lines are disposed adjacent to the selected word line” requires the first group to be disposed adjacent to

the location of the selected word line. By comparison, Lee fails to disclose or render obvious that the location of the selected word line has any bearing on how word lines are grouped together. Lee discloses various ways to divide word lines into groups, but in each case, the groups are determined without any regard given to the location of the selected word line. See Lee, 8:4-10, 9:36-40, 10:4-12. At no point does Lee disclose or otherwise render obvious that a first group is disposed adjacent to a selected word line, nor has the Petitioner provided any argument to suggest that Lee could be modified to do so. PrzybylskiII, ¶97.

For at least the reasons provided above, Lee fails to teach or render obvious “wherein the first group of the plurality of word lines are disposed adjacent to the selected word line” as required by claims 3 and 13. PrzybylskiII, ¶98.

VII. GROUND 2: ZHAO DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1, 4-7, 9, 11, 14-16, 18-19

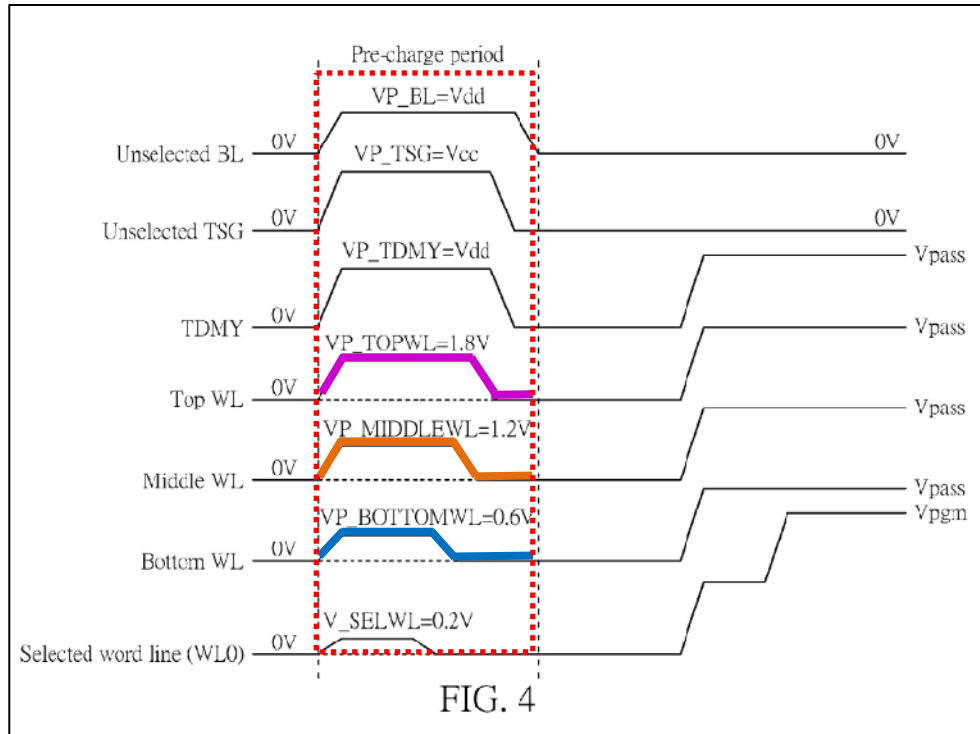
Petitioner has failed to show that Zhao alone discloses or renders obvious limitations [1.e.1] and [11.b] of the ’822. Regarding limitations [1.e.1] and [11.b], Zhao does not disclose or render obvious applying a “first word line pre-pulse signal” because Zhao’s application of a flat, unchanging, V_{ss} voltage (*i.e.*, the purported “first word line pre-pulse signal” identified by Petitioner) is not a “pulse” as required by the ’822, nor has Petitioner shown that a POSITA would have been motivated to modify Zhao to replace V_{ss} with a pulse. PrzybylskiII, ¶¶99-100.

A. Independent Claims: Zhao Does Not Disclose or Render Obvious Applying a “First Word Line Pre-Pulse Signal ... During a Pre-Charge Period” (Limitations [1.e.1] and [11.b])

Zhao does not disclose or otherwise render obvious at least limitations [1.e.1] and [11.b] because Zhao’s application of a flat, unchanging, Vss voltage (*i.e.*, the purported “first pre-pulse signal” identified by Petitioner) is not a “pulse” as required by the ’822, and instead shows that no pulse is applied during the purported pre-charge period. Pet., 44-59. Even under Petitioner’s proposed construction, the term “word line pre-pulse signal” requires—at minimum—a signal that “increases in value and then decreases in value (or vice versa) before a programming step,” which is not satisfied by Zhao’s flat Vss signal. *See* §IV.A (Claim Construction). Moreover, Petitioner’s suggestion that Zhao discloses or otherwise renders obvious the use of a pulsed signal in lieu of Vss during the relevant time period is based on incorrect inferences and mischaracterizations of Zhao’s teachings. Pet. 44-59. PrzybylskiII, ¶¶101-102.

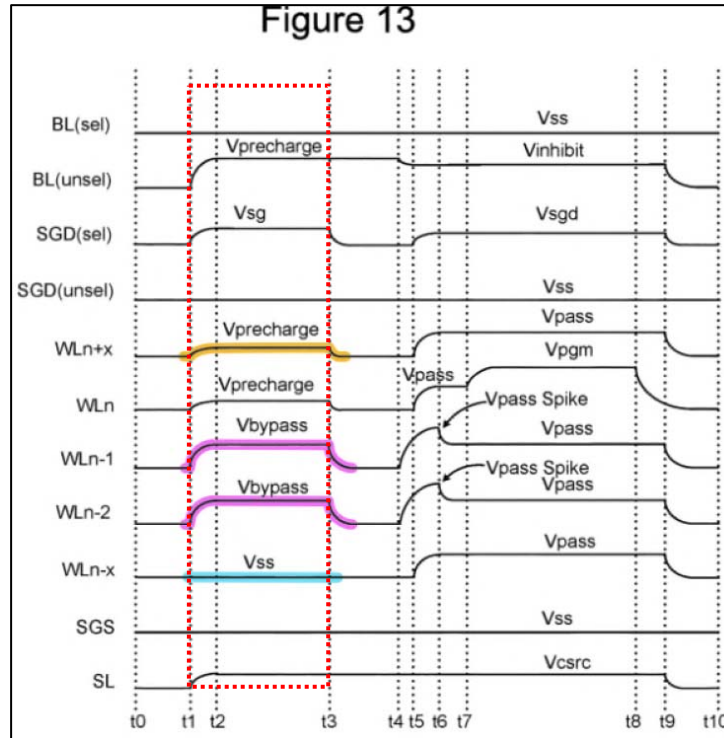
Claim 1 recites a control circuit configured to “**apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines** during a pre-charge period” (Element [1.e.1]). An analogous limitation is found in Element [11.b] of independent claim 11, and is common to each of the Challenged Claims. PrzybylskiII, ¶103.

As explained in Section II, the '822 improves conventional systems by using multiple pre-pulse signals during a pre-charge period to enhance the channel potential gradient, remove boosting charges, and mitigate the effects of programming disturb. See '822, 4:39-59. For example, as illustrated in the embodiment of Fig. 4, a **first word line pre-pulse signal**, a **second word line pre-pulse signal**, and a **third word line pre-pulse signal** are each applied to different groups of word lines during **the pre-charge period**:



But unlike the claimed invention of the '822, Zhao does not disclose three separate word line pre-pulse signals during the pre-charge period, as required by the '822. PrzybylskiII, ¶104.

Zhao's approach to mitigating program disturb is illustrated by Fig. 13. Starting at time t_0 , "all the depicted signals are at ... 0 volts (V_{ss})," and the time period "from **t_1 - t_3 corresponds to pre-charging.**" Zhao, 22:34-41. But Zhao fails to disclose three distinct "pre-pulse signals" applied to groups of word lines during the pre-charging period. For example, as shown below, Petitioner incorrectly characterizes V_{ss} as one of the claimed "pre-pulse signals ... during a pre-charge period" recited by the independent claims of the '822.⁵ See Pet., 22-23, 52.



Petitioner's argument fails at least because the flat "**0 volt (V_{ss})**" voltage identified in the Petition is not a "word line pre-pulse signal," as it is not a "pulse," and would

⁵ For convenience, Petitioner's annotations have been reproduced above.

fail to qualify as a “word line pre-pulse signal” even under Petitioner’s own proposed construction of the term as it does not “increase[] in value and then decrease[] in value (or vice versa).” See §IV.A (Claim Construction). Rather, Zhao explicitly teaches that “word lines WLn-x **remain at Vss** (e.g., 0 v)” throughout the relevant time period. Zhao, 23:5-12. PrzybylskiII, ¶105.

Petitioner seemingly tries to address Zhao’s deficiency by asserting, incorrectly, that a different voltage may be applied to WLn-x in place of Vss during the time period t1-t3. See Pet., 51-52. To support this assertion, Petitioner points to Zhao’s disclosure that: “To prevent the source side of the channels from being pre-charged, **unselected source side word lines receive 0 volts or one or more voltages that are too low to pre-charge** and/or too low to turn on memory cells in a highest data state.” Zhao, 19:22-24. But that added disclosure does not suggest that a pulse is applied to word lines WLn-x during the pre-charge period. At most, Zhao is describing that the flat Vss signal depicted in Fig. 13 may be fixed at “0 volts,” or another fixed voltage. Zhao, 19:22-26. But a flat signal, regardless of the voltage of that signal, is not a pulse. At no point does Zhao disclose a pulse being applied to WLn-x. PrzybylskiII, ¶106.

Thus, Petitioner has failed to show that word lines WLn-x in Zhao (*i.e.*, the purported “first group of word lines”) receives a “first word line pre-pulse signal” during a pre-charge period as required by the independent Challenged Claims, nor

has Petitioner provided any rationale as to why a POSITA would modify Zhao to do so. Rather, Zhao explicitly teaches that a flat signal rather than a pulse is applied to that group of word lines during the relevant time period. *See* Zhao, 23:5-12. Moreover, it would not make sense to replace Vss with some other value, as Zhao teaches that the WLn-x should be remain turned off and prevented from pre-charging throughout the relevant time period. *See* Zhao, 19:2-26. PrzybylskiII, ¶107.

Zhao does not disclose or render obvious dependent claims 4-7, 9, 14-16, and 18-19 for at least the same reasons. PrzybylskiII, ¶108.

VIII. GROUND 3: ZHAO IN VIEW OF LEE DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-9, 11-19

Petitioner has failed to show that a POSITA would have been motivated to modify Zhao in view of Lee in the manner suggested in the Petition to render obvious the subject matter of limitations [1.e.1]-[1.e.3] and [11.b]-[11.d] of the '822. PrzybylskiII, ¶¶109-110.

A. Independent Claims: A POSITA Would Not Have Been Motivated to Combine Zhao and Lee in the Manner Proposed in the Petition

As described above in Sections VI.A and VII.A, Zhao and Lee fail to disclose or otherwise render obvious the use of a “first word line pre-pulse signal,” “second word line pre-pulse signal,” and “third word line pre-pulse signal,” during “a pre-charge period” as required by independent claims 1 and 11. Petitioner attempts to address these deficiencies by cobbling together disclosures from Lee (Ground 1) and

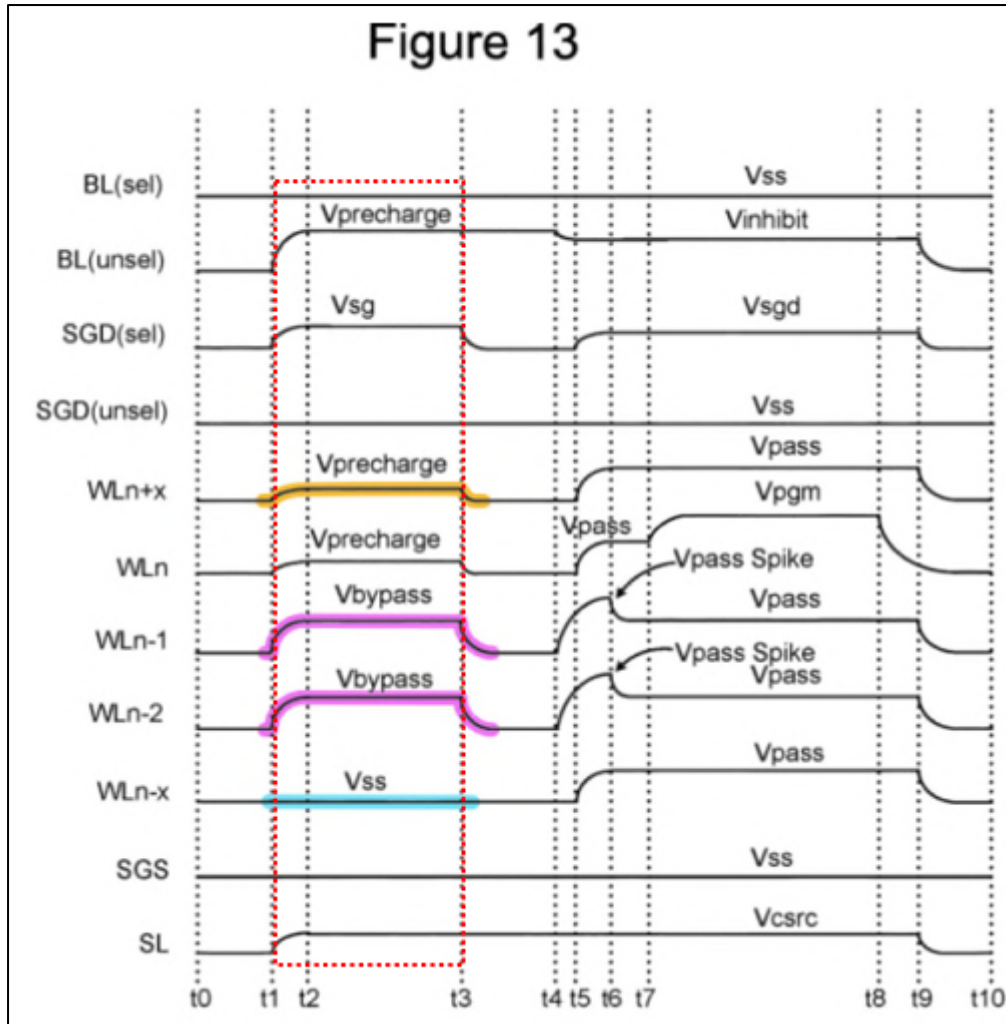
Zhao (Ground 2), but has failed to show that a POSITA would have motivated to apply Lee's teachings in the manner proposed in the Petition—*i.e.*, that the use of multiple increasing pre-bias voltages is needed to offset “effects caused by the resistance component between the source select transistor and the drain select transistor.” Pet., 62; *see also* Lee 8:25-52 (explaining that “a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor”). PrzybylskiII, ¶111.

There are at several reasons why a POSITA would not have been motivated to apply Lee's teachings to Zhao in the manner suggested in the Petition. **First**, Petitioner fails to show that a POSITA would have looked to Lee when implementing Zhao as Lee is concerned with problems arising from charging operations performed via the common source line, while Zhao instead performs charging from the bit-line. Indeed, Lee states that it is addressing issues in “typical programming operations” wherein “***the precharge level in a source select side channel is reduced*** and thus channel boosting is not effectively generated.” Lee, 8:25-37. **Second**, to the extent that Lee is concerned with compensating for the effect of a “resistance” component that appears between the source and drain, those effects are not present in Zhao's system. *See* Lee, 8:46-52. **Third**, even assuming a “resistance” component was present in Zhao's system, the proposed modification described in the Petition would not compensate for the effect. **Fourth**, the absence

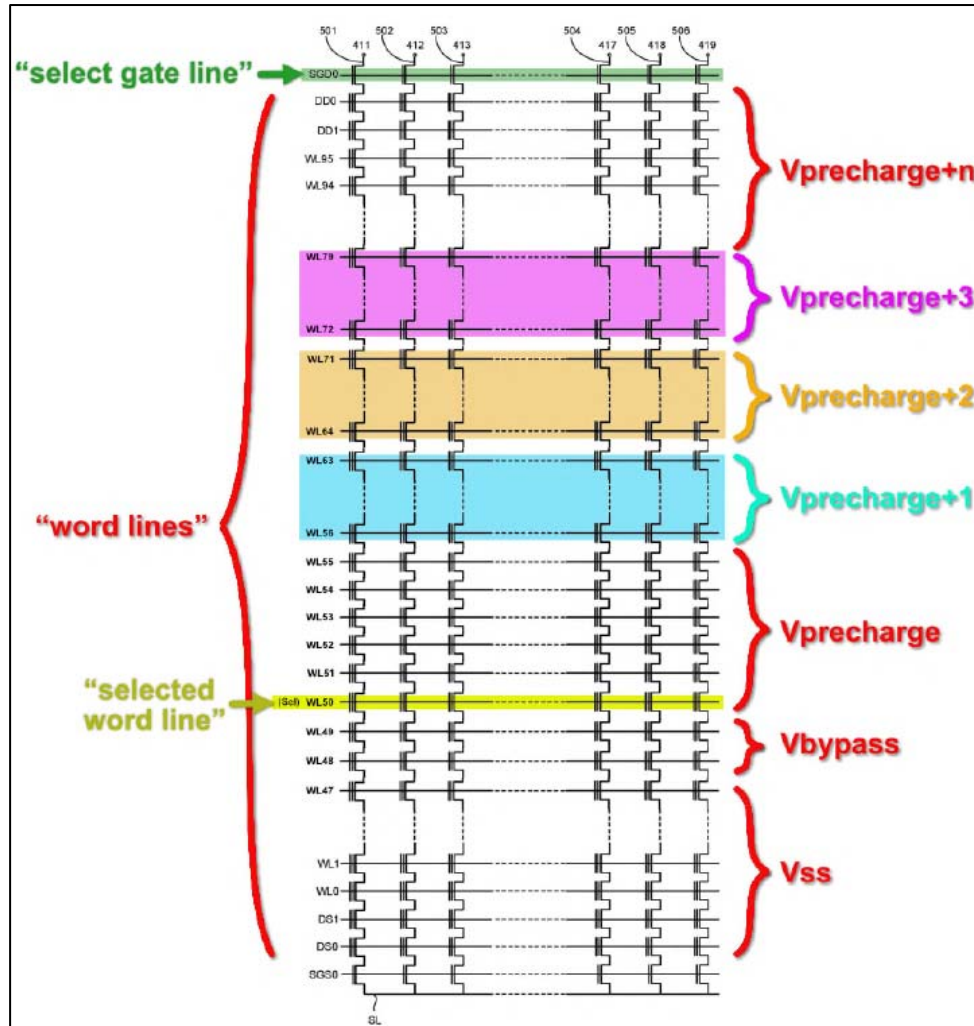
of a “resistance” component in Zhao arises because Zhao and Lee use different approaches for mitigating program disturb, and a POSITA would not achieve any benefits by applying Lee’s teachings to Zhao in the method suggested in the Petition. Accordingly, applying Lee’s teachings as proposed in the Petition would not provide the intended benefits purportedly described by Lee and relied upon by Petitioner as a purported motivation to combine. It is only through impermissible hindsight bias, in an effort to reconstruct the ’822 system *ex-post*, that Petitioner argues a POSITA would attempt to apply Lee’s teachings to Zhao. PrzybylskiII, ¶112.

Claim 1 recites a control circuit configured to “apply a [first/second/third] word line pre-pulse signal of a plurality of word line pre-pulse signals to a [first/second/third] group of the plurality of word lines during a pre-charge period” (Elements [1.e.1]-[1.e.2]), wherein “a voltage level of **the second word line pre-pulse signal** is greater than that of **the first word line pre-pulse signal**, and a voltage level of the **third word line pre-pulse signal** is greater than that of **the second word line pre-pulse signal**.” (Element [1.e.4]). Analogous limitations are found in Elements [11.b]- [11.e] of independent claim 11 and are common to each of the Challenged Claims. PrzybylskiII, ¶113.

As discussed in Section V.B, Zhao generally describes applying a “**Vprecharge**” signal to word lines $WLn+x$ located on the drain-side of the currently selected word line.



Zhao, Fig. 13. Petitioner argues that it would have been obvious to replace Zhao’s single **Vprecharge** signal with a series of different pre-charge signals with increasingly large voltage levels, as allegedly taught by Lee, in an effort to “compensate” for “effects caused by the resistance component between the source select transistor and the drain select transistor,” and that the combined system would operate as illustrated below. See Pet., 60-67.



Pet., 64-65 (annotations reproduced from Petition). But Petitioner’s proposed combination is inconsistent with the purported motivation for applying Lee’s teachings and ignores the actual structure and operation of the memory cell string. PrzybylskiII, ¶114.

First, as a preliminary matter, a POSITA would not look to Lee because Lee is concerned with problems arising from pre-charging operations performed via the common source line, while Zhao instead performs charging from the bit-line. Specifically, Lee purports to address problems arising in “typical programming

operations” where memory cell threshold voltages are “increased by a resistance component between the source select transistor and the drain select transistor,” and as a result “**the precharge level in a source select side channel is reduced** and thus channel boosting is not effectively generated.” Lee, 8:25-37. This is also apparent in the design of Lee’s system, where the “precharge voltage [is] applied **to the common source line** during a precharge operation.” Lee, 8:25-37, 8:65-:6. By comparison, in the embodiment of Fig. 13 of Zhao on which Petitioner relies, the pre-charge voltages are explicitly applied through the **bit line** (and charging is performed through the bit line side of the device) rather than the **source line**. See, e.g., Zhao 22:39-47 (“[a]t time t1 ... **the unselected bit lines are raised to a pre-charge voltage** Vprecharge”). Petitioner’s expert has overlooked this distinction, and incorrectly assumed that Lee’s teachings would be directly applicable to Zhao. But the schemes used when charging from the bit line as opposed to the common source differ substantially. See, e.g., Yang 1:59-2:19 (distinguishing Fig. 8A-8C embodiments where “pre-charge is from a bit line,” Fig. 9A-9C embodiments where “pre-charge is from a source line,” and Fig. 10A-10C embodiments where “pre-charge is from both a bit line and a source line”). PrzybylskiII, ¶115.

In general, Petitioner has ignored the differences that arise from precharging via the bit line as opposed to the source line, and has not properly explained how—if at all—Lee’s teachings would need be adapted to compensate for the change. For

example, Lee teaches that when charging from the common source, all word lines between the group containing the selected word line and the common source receive a single “**default value**.” See Lee, 8:25-37, 8:65-9:6, 9:41-59, Fig. 4. Applying that teaching to Zhao would not result, as Petitioner suggests, in different voltages on “drain side word lines.” Pet 64. Zhao charges from the bit line, and Lee’s teaching indicates, if anything, a single **default value** of $V_{precharge}$ is used for all word lines between the selected word line and the bit line (similar to the unmodified Zhao system). See Zhao, 22:39-50. PrzybylskiII, ¶116.

Second, the purported motivation that Petitioner points to for applying Lee’s teachings (i.e., Lee’s teaching that multiple different pre-charge voltages are needed to offset a “resistance component between the source select transistor and the drain select transistor”) is simply inapplicable in Zhao. Pet., 60 (citing Lee 8:25-29). Contrary to what Petitioner suggests, there is no need to replace Zhao’s **$V_{precharge}$** with multiple pre-charge signals in the manner they have proposed, and attempting to do so would not compensate for a purported “resistance component” or otherwise help to create a more uniform charge distribution. Rather, because there is no current flowing through the memory string in Zhao (i.e., the transistors receiving a **V_{ss}** are cut off and act like open circuits), the voltage level along the conducting portion of the channel (i.e., the portion formed by the memory cells at the top of the string that

receive $V_{\text{precharge}}$ through $WLn+x$) does not vary with some “resistance component” that needs to be offset. PrzybylskiII, ¶117

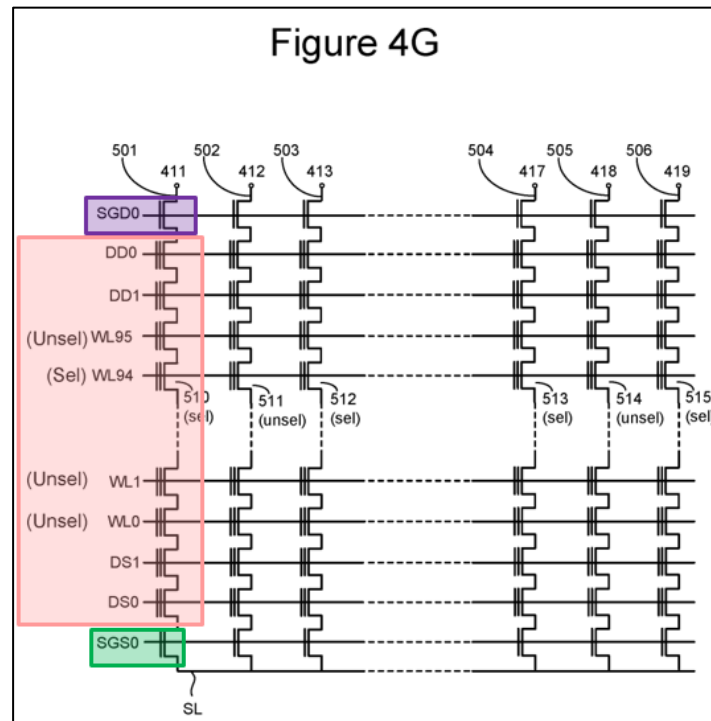
Lee states that “a threshold voltage of a memory cell is increased by a **resistance component** between the source select transistor and the drain select transistor” such that “**the precharge level in a source select side channel** is reduced.” Lee, 8:25-32. This is a result of Ohm’s law—changes in voltage are proportional to current times resistance ($V=I \times R$). See, e.g., Ex. 2022 (Hambley) at 29. When a current runs from the source select transistor and to the drain select transistor along the length of the memory string (I_{DS}), the “resistance component between the source select transistor and the drain select transistor” (R_{channel}) will create voltage drops which, in turn, may result in a “precharge level” being reduced on the “source select side” of the memory string furthest from the bit line ($\Delta V_{\text{DS}} = R_{\text{channel}} \times I_{\text{DS}}$). See Lee, 8:25-32. To compensate for this and create more uniform level of charge, Lee describes applying “different pre-bias voltages to the respective word line groups” along the entire length of the memory string based on their relative positions within the string. See Lee, 2:63-3:7, 8:3-17.⁶ But this “resistance component” referenced

⁶ During his deposition, Dr. Liu for the first time attempted to provide an alternative explanation for Lee’s system. Specifically, Dr. Liu introduced the argument that what Lee describes as a “resistance component between the source select transistor

by Lee does not matter in a system like Zhao's where there **is no current** running "between the source select transistor and the drain select transistor" in the memory string. See Lee, 8:25-32. PrzybylskiII, ¶118.

and the drain select transistor" is actually referencing a "body effect" or "source voltage effect" that causes memory cell threshold voltages to change as "a function of how many transistors [are] connected in series with it." Liu Tr. 82:12-25. But Lee makes no mention of "body effects" or "source voltage effects," and Dr. Liu's attempt to shift to new invalidity theories based on a supposed "body effect" is untimely and improper. "It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). Petitioner cannot submit "new evidence or argument" after the fact in an attempt to make out a prima facie case of unpatentability. PTAB Consolidated Patent Trial Practice Guide (Nov. 21, 2019) at 73. Nevertheless, Dr. Liu's explanation is found nowhere in Lee, let alone the Petition. Rather, Lee instead states that "a resistance component between the source select transistor and the drain select transistor" causes a "precharge level in a source select side channel" to be "reduced." Lee 8:25-31. PrzybylskiII, ¶119.

Both Lee and Zhao describe typical memory strings, which are a “vertical column” of **memory cells** arranged in series between a **source side** select transistor and a **drain side** select transistor.



Zhao, Fig. 4G, 10:6-24; *see also* Lee, Fig. 3, 7:37-57 (describing the structure of the memory cell string). As shown in the figure, because memory cells are connected in series, *all* of the **memory cells** must be turned on for current to flow between the **source side** select transistor and the **drain side** select transistor (*i.e.*, all the memory cells must be turned on to form a conductive channel through the memory cell string). If any memory cell is turned off, there is no conductive channel. As a result, no current flows through the memory string, there are no voltage drops across the channels of the memory cells along the length of the string, and there are no changes

in the memory cell threshold voltages (or the corresponding word line voltages necessary to form conductive channels) in the memory cells as a result of their position within the string. PrzybylskiII, ¶120.

The Petition fails to address the fact that in Zhao, as well as Petitioner's proposed combination, several of the memory cells are explicitly turned off. Indeed, Zhao's use of **Vss** (or a similar voltage "too low to pre-charge and/or too low to turn on memory cells in a highest data state"), precludes any current flowing between the **source side** select transistor and the **drain side** select transistor as well as between the bit line at the top of the NAND string and sources line at the bottom of the NAND string, thus precluding "resistance components" between the source select transistor and the drain select transistor from creating changes in voltage along the portion of the memory string being pre-charged. See Zhao, 19:22-26. PrzybylskiII, ¶121.

Third, even assuming that the effects of a "resistance component between the source select transistor and the drain select transistor" were present in Zhao's system, the fact that Zhao charges from the bitline would preclude Petitioner's proposed combination from working as intended. See Lee, 8:46-52. Specifically, Petitioner has proposed that "unselected drain-side word lines" are divided into groups and applied with different voltage levels, such that the word lines near the bit line are applied with higher voltages (e.g., such that $V_{\text{precharge}+3} > V_{\text{precharge}+2} > V_{\text{precharge}+1}$). Petition at 64-65. But unlike in Lee, Zhao describes the precharge

being applied through the **bitline** rather than the **common source**. Compare Lee, 8:65-9:6, with Zhao 22:39-47. If there were resistive effects present, it would be the word lines furthest from the **bitline** that require the “resistance component between the source select transistor and the drain select transistor” to be offset. See Lee 8:47-51. But in Zhao, the word lines furthest from the bit line aren’t even supposed to be precharged—they are applied with a V_{ss} voltage that is deliberately too low to precharge the memory cells. See Zhao, 19:22-26. There is no need to precharge those word lines, and increasing the bias voltages applied near the bit line as Petitioner suggests is not needed to offset any purported resistive component. See Pet. 64-65. Rather, the modification that Petitioner has proposed pointlessly drives the word lines closest to the bit line with excessive voltages ($V_{precharge+1}$, $V_{precharge+2}$, $V_{precharge+3}$, etc.) for no reason, increasing device complexity and the risk of transistor breakdown in the process. PrzybylskiII, ¶¶122-124.

Fourth, these inconsistencies between Lee and Zhao, and the lack of a “resistance” that needs to be offset in Zhao’s system, arise from the two systems using disparate and incompatible approaches for mitigating program disturb. Zhao’s pre-charge operation is directed to “purging (cleaning/clearing the electrons from) the already programmed side of the channel” prior to the subsequent boosting and programming steps. See Zhao, 2:27-35; see also *id.* 18:63-19:8 (describing a method for “purging the already programmed side of the channel during a pre-charge

operation”). Purging mitigates program disturb resulting from “source side hot electron injection,” which arises from unwanted charges being accelerated from the source side to the drain side during boosting, and then redirected into memory cells on the selected word line. Zhao, 18:36-51. To address this problem, Zhao teaches applying “a bypass voltage to multiple already programmed side unselected word lines while pre-charging ... the channels of unselected NAND strings.” Zhao, 19:29-34; *see also* Zhao, 22:50-56. Doing so “opens up the channel (e.g. electrically couples the two ends of the channel) ***so that electrons can migrate (electrical communication) from the source side of the channel to the drain side of the channel***” and thus “eliminate[] the voltage differential between the source side of the channel and the drain side of the channel.” Zhao 22:65-23:5. PrzybylskiII, ¶¶125-126.

Lee discusses a wholly disparate approach for mitigating program disturb. Zhao applies a localized bypass voltage that “electrically couples the two ends of the channel” and allows charges to be equalized, but does so without conducting current between the source select transistor and the drain select transistor at the ends of the memory string—hence why there is no need to compensate for “resistance” effects creating voltage differences along the length of the memory string channel. *See* Zhao, 22:65-23:5. By comparison, Lee applies a pre-charge voltage to every memory cell in the string. *See, e.g.,* Lee, 8:3-18 (a “memory block includes thirty-two word

lines WL0 to WL31” and pre-bias voltages are “applied to the respective word lines WL0 to WL31 in a precharging step during a program operation”). As a result, Lee, unlike Zhao, must compensate for the fact that the “pre-charge level in a source side channel is reduced and thus charge boosting is not effectively generated” because “a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor.” Lee, 8:25-31, 8:47-52. PrzybylskiII, ¶127.

Contrary to Petitioner’s assertions, a POSITA would not have been motivated to apply Lee’s teachings to Zhao. They are not, as Petitioner seems to suggest, describing complementary techniques for further reducing program disturb. See Pet.,66-68. Rather, Lee’s use of preset bias levels for each and every word-line (which would include those adjacent to the selected word line) is fundamentally different than the scheme described by Zhao, and Lee’s teachings regarding the use of different voltages to compensate for resistance along the memory string (*i.e.*, at different locations between the source select transistor and the drain select transistor) would not provide the benefits that Lee’s teachings purport to provide in the context of Petitioner’s proposed combination. PrzybylskiII, ¶¶128.

Rather, Petitioner’s and Dr. Liu’s illustrations showing how the supposed combination would operate is divorced from any possible benefits to Zhao’s system. At best, it is a naked attempt to “reconstruct the applicant’s invention only with the

benefit of hindsight,” that fails to render obvious the Challenged Claims. *Netflix, Inc. v. DivX, LLC*, 80 F.4th 1352, 1359 (Fed. Cir. 2023). PrzybylskiII, ¶129.

Zhao in view of Lee also does not disclose or render obvious dependent claims 2-9 and 12-19 for at least the same reasons. PrzybylskiII, ¶130.

IX. GROUND 4: YANG DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-7, 9, 11-16, 18-19

Petitioner has failed to show that Yang alone discloses or renders obvious at least limitations [1.e.1]-[1.e.4] and [11.b]-[11.e], or the added limitations of dependent claims 2-3, and 12-13. Regarding limitations [1.e.1]-[1.e.4] and [11.b]-[11.e], Yang fails to disclose three signals with incrementally increasing voltage levels being applied to three groups of word lines, and Petitioner’s argument that a POSITA would have nonetheless found the Challenged Claims obvious is unsupported by the record. For the added limitations of dependent claims 2-3 and 12-13, Yang does not disclose or render obvious that groups are “disposed” based on the locations of the selected word line. PrzybylskiII, ¶¶131-134.

A. Independent Claims: Yang Does Not Disclose or Render Obvious Word Line Pre-Pulse Signals with Incrementally Increasing Voltage Levels

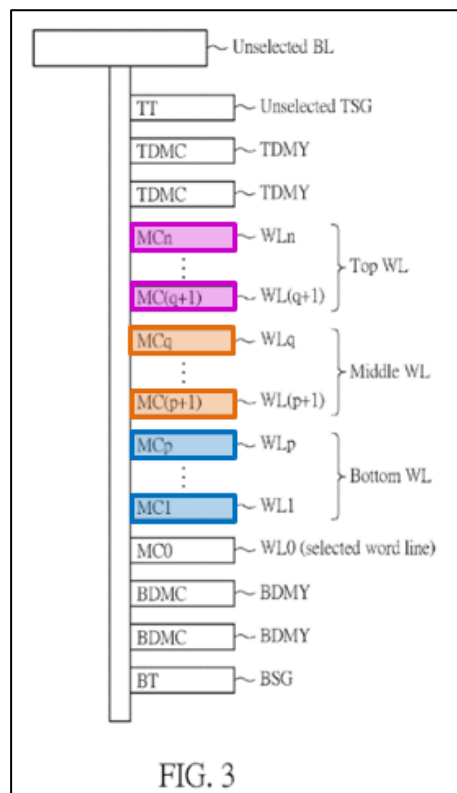
Yang does not disclose or otherwise render obvious limitations [1.e.1]-[1.e.4] and [11.b]-[11.e] because Yang’s use of “Vbypass,” “Vpre_OD,” and “Vpre_dmy” voltages (i.e., the purported “word line pre-pulse signals”) fails to disclose three signals applied to three groups of word lines that have incrementally increasing

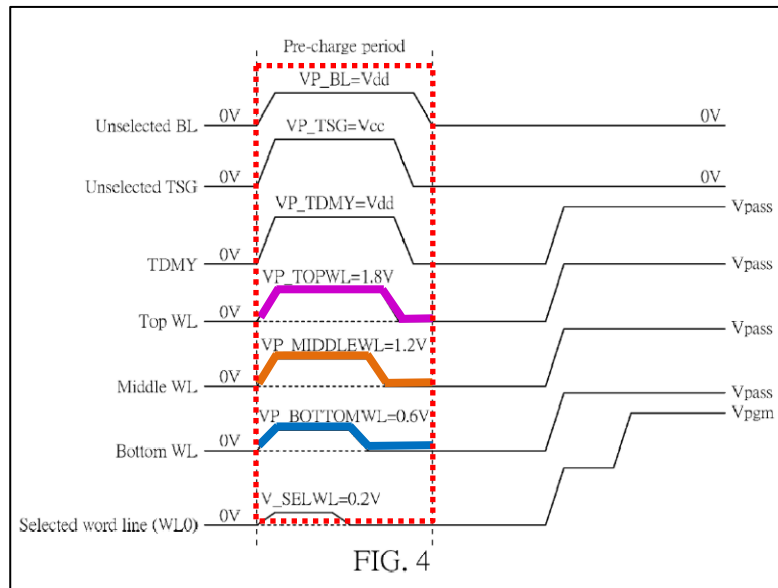
voltage levels. Moreover, Petitioner’s assertion that “a POSITA would nonetheless have understood Yang to render what this limitation requires obvious” is unsupported by the record and insufficient to support a finding of obviousness. Pet., 76-82. PrzybylskiII, ¶¶135-136.

Claim 1 recites a control circuit configured to “**apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines** during a pre-charge period” (Element [1.e.1]); “**apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines** during the pre-charge period” (Element [1.e.2]); and “**apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines** during the pre-charge period” (Element [1.e.3]) wherein “*a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.*” (Element [1.e.4]). Analogous limitations are found in Elements [11.b]-[11.e] of independent claim 11, and are common to each of the Challenged Claims. PrzybylskiII, ¶137.

As described in the ’822, the system is “configured to apply a plurality of word line pre-pulse signals to word lines which are disposed between the selected word line and the top dummy word line TDMY,” with “incremental” voltage

levels. '822, 3:55-59; 4:2-10. For example, in the embodiment illustrated in Figs. 3-4, the 1.8V voltage level of the **third word line pre-pulse signal** (VP_TOPWL) is greater than 1.2V voltage level of the **second word line pre-pulse signal** (VP_MIDDLEWL), which is greater than the 0.6V voltage level of the **first word line pre-pulse signal** (VP_BOTTOMWL). See '822, 5:50-55, 5:65-6:8, Figs. 3-4 (copied below). PrzybylskiII, ¶138.

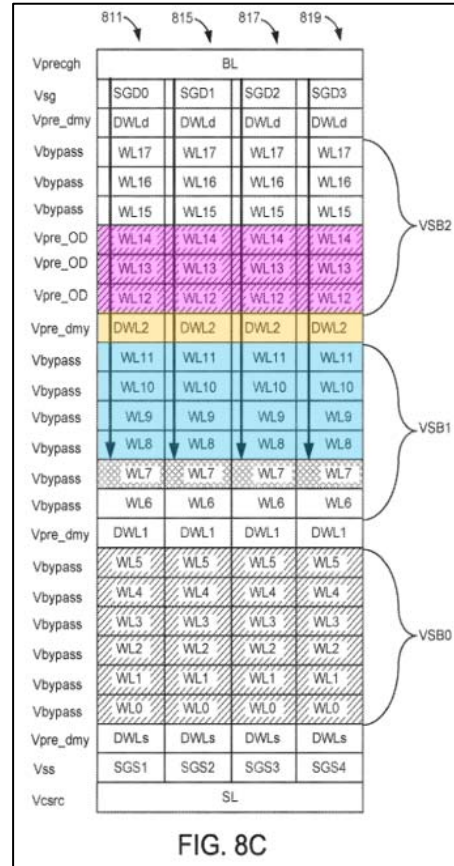




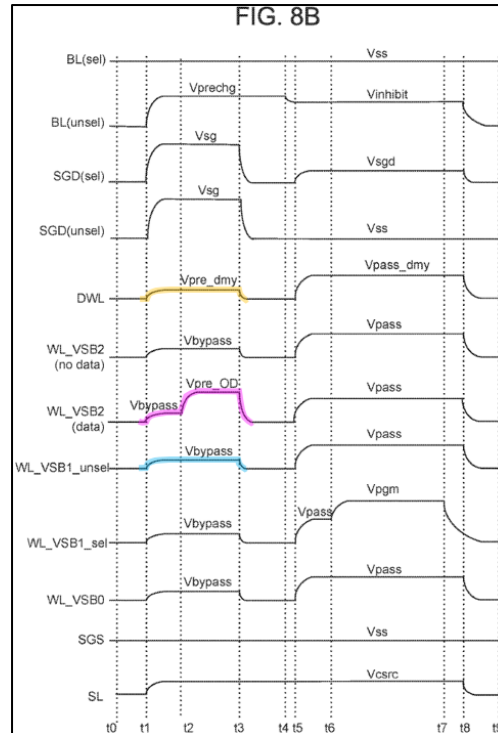
Unlike the '822, Yang does not disclose three distinct “word line pre-pulse signals” applied to groups of word lines that have incrementally increasing voltage levels. As shown in Figures 8B-8C of Yang, copied below, Petitioner improperly equates the claimed “**first**,” “**second**,” and “**third**” word line pre-pulse signals applied to groups of word lines with Yang’s disclosure of: (1) “**bypass voltage**” (“**V_{bypass}**”) applied to data word lines that are “not programmed,” (2) a “**dummy pre-charge voltage**” (“**V_{pre_dmy}**”) applied to a “dummy” word lines,⁷ and (3) an

⁷ Petitioner incorrectly asserts that Yang’s disclosure of using “[m]ore or less ... layers” discloses the use of multiple dummy layers in lieu of the one depicted in the figure. See Pet., 79; Yang 8:54-9:5. Yang states that dummy memory cells are used to “electrically isolate a first set of memory cell transistors within the memory string” by being placed between different “vertical sub-block[s]” of memory cells. Yang

“overdrive voltage” (“Vpre_OD”) applied to “programmed data word lines,” respectively. Pet., 73-81.



12:35-43. Incorporating more layers into the device (e.g., by including new sub-blocks into the stack, or increasing the size of existing sub-blocks) does not imply that dummy layers would be doubled-up so that multiple dummy layers appear in a single location. Rather, in the context of Yang, only a single layer of dummy memory cells needs to be used to isolate any given set of memory cells. PrzybylskiII, ¶140.

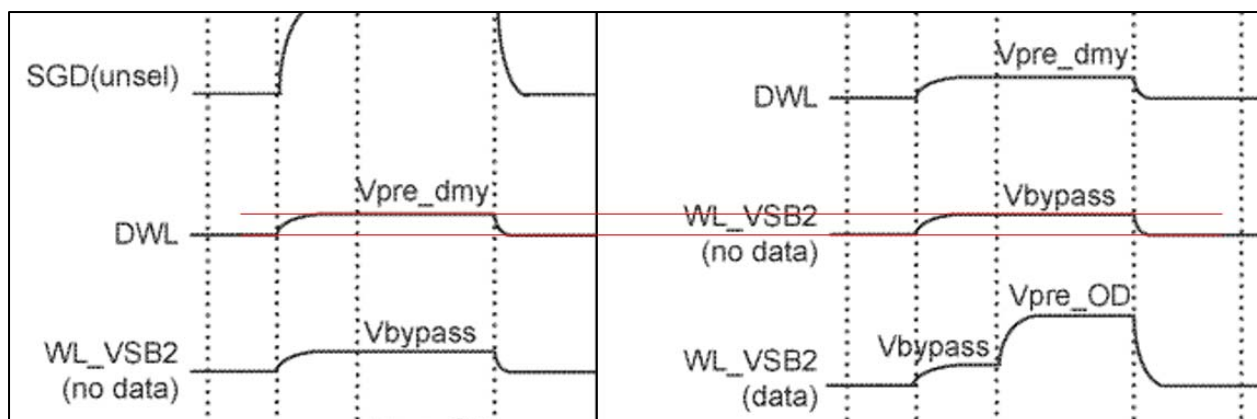


Yang, Figs. 8B-8C.⁸ Yang does not disclose, and Petitioner has not otherwise shown, that **Vbypass**, **Vpre_dmy**, and **Vpre_OD** constitute distinct “word line pre-pulse signals” applied to different groups of word lines with the different voltage levels required by the claims. PrzybylskiII, ¶139.

As recognized in the Decision to Institute, Petitioner has not shown support in the record for its assertion that the voltages identified would have the relative magnitude levels required by the Challenged Claims. See DI 24-25. Moreover, Petitioner’s failure to make the requisite showing in the Petition cannot be remedied

⁸ Petitioner’s annotations for **Vbypass**, **Vpre_dmy**, and **Vpre_OD** are reproduced above.

after the fact. *See, e.g., Intelligent Bio-Sys.*, 821 F.3d at 1369; PTAB Consolidated Patent Trial Practice Guide (Nov. 21, 2019) at 73 (“Petitioner may not submit new evidence or argument in reply that it could have presented earlier”). The Petition acknowledges that “Yang does not provide numerical examples” for the relevant voltage levels, and asserts in conclusory fashion that a POSITA would have “nonetheless understood Yang to render what this limitation requires obvious.” Pet., 81-82. But Petitioner’s unsupported assertions (e.g., that **Vpre_dmy** has an “intermediate” value less than **Vpre_OD**) does not establish any relationship between the relative magnitude of **Vpre_dmy** as it relates to **Vbypass**, or otherwise show that Petitioner’s proposed mapping discloses or renders obvious the limitations of the independent Challenged Claims. *See* Pet., 81-82. Petitioner has not identified anything in Yang to suggest that a POSITA would have been motivated to use a value for **Vpre_dmy** that is different than that of **Vbypass**. To the contrary, placing copies of the waveforms side-by-side shows that **Vpre_dmy** and **Vbypass** are illustrated in Fig. 8B as having identical values.



Yang. Fig. 8B (color annotations added). Using the same voltage for both also advantageously simplifies the design of a memory device by requiring only a single voltage generator instead of two separate voltage generators for producing the **Vpre_dmy** and **Vbypass** signals. Thus, Petitioner has failed to show that Yang discloses or renders obvious three signals applied to three groups of word lines that have incrementally increasing voltage levels, as required by the Challenged Claims. PrzybylskiII, ¶141.

Yang also does not disclose or render obvious dependent claims 2-7, 9, 12-16, and 18-19 for at least the same reasons. PrzybylskiII, ¶142.

B. Claims 2 and 12: Yang Does Not Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line”

In addition, Yang does not disclose or render obvious the added limitations of dependent claims 2 and 12 requiring that groups of word lines are “disposed in an order of distance from the selected word line.” Rather, the groups in Yang do not change based on the position of the selected word line. PrzybylskiII, ¶143.

The added limitations of dependent claim 2 recite, “wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines ***are disposed in an order of distance from the selected word line*** of the plurality of word lines.” Analogous limitations are found in dependent claim 12. PrzybylskiII, ¶144.

As discussed in Section IV.B (Claim Construction), the plain and ordinary meaning of the term “disposed in an order of distance from the selected word line” requires that the groups be disposed in order based on the location of the selected word line. By comparison, Yang fails to disclose or render obvious that the location of the selected word line has any bearing on how word lines are grouped together. *See* Yang Fig. 8C, 25:9-33. PrzybylskiII, ¶145.

Yang divides word lines into three groups, none of which depends on the location of the selected word line: (1) “data word line ... that are not programmed;” (2) data word lines that are “programmed;” and (3) “dummy word lines.” *See* Yang 24:1-17, 24:18-27, 24:28-31. At no point are the groups determined based on the location of the selected word line. Rather, “dummy” word lines are based on where dummy memory cell transistors have been placed during the manufacturing process, and the data word lines are grouped based on whether the corresponding memory cells have been programmed or not. At no point does Yang disclose or otherwise render obvious that these groups are disposed based on distance to a selected word line, nor has the Petitioner provided any argument to suggest that Yang could be modified to do so. PrzybylskiII, ¶146.

For at least the reasons provided above, Yang fails to teach or render obvious that groups “disposed in an order of distance from the selected word line of the plurality of word lines” as required by claims 2 and 12. PrzybylskiII, ¶147.

C. Claims 3 and 13: Yang Does Not Disclose or Render the “First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line”

In addition, Yang does not disclose or render obvious the added limitations of dependent claims 3 and 13 requiring that “the first group of the plurality of word lines are disposed adjacent to the selected word line.” Rather, as discussed above in Section IX.B, Yang teaches that groups do not change based on the position of the selected word line. PrzybylskiII, ¶148.

The added limitations of dependent claim 3 recite, “wherein *the first group of the plurality of word lines are disposed adjacent to the selected word line*, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.” Analogous limitations are found in dependent claim 13. PrzybylskiII, ¶149.

As discussed in Section IV.B (Claim Construction), the plain and ordinary meaning of the term “the first group of the plurality of word lines are disposed adjacent to the selected word line” requires that group to be disposed adjacent to the location of the selected word line. By comparison, Yang fails to disclose or render obvious that the location of the selected word line has any bearing on how word lines are grouped together. Instead, Yang groups word lines into “data word line ... that

are not programmed, data word lines that are “programmed,” and “dummy word lines.” See Yang 24:1-17, 24:18-27, 24:28-31. In each case, the groups are determined without any regard given to the location of the selected word line. At no point does Yang disclose or otherwise render obvious that a first group is disposed adjacent to a selected word line, nor has the Petitioner provided any argument to suggest that Yang could be modified to do so. PrzybylskiII, ¶150.

For at least the reasons provided above, Yang fails to teach or render obvious “wherein the first group of the plurality of word lines are disposed adjacent to the selected word line” as required by claims 3 and 13. PrzybylskiII, ¶151.

X. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the ’822 are anticipated or obvious. Accordingly, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(a)-(b). According to the word-processing system's word count, the brief contains 13,951 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

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The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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