

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,
v.
YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2024-00795
U.S. Patent No. 11,501,822

PETITIONER'S REPLY

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,501,822 B2 to Jia et al.
1002	File History of U.S. Patent No. 11,501,822 B2 to Jia et al.
1003	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
1004	U.S. Patent No. 10,121,529 B2 to Lee (“Lee”)
1005	U.S. Patent No. 10,643,718 B2 to Zhao et al. (“Zhao”)
1006	Aritome, “NAND Flash Memory Technologies” (2016)
1007	Brown et al., “Nonvolatile Semiconductor Memory Technology” (1998)
1008	Cappelletti, et al., “Flash Memories” (1999)
1009	U.S. Patent No. 9,589,978 to Yip
1010	U.S. Patent No. 10,726,920 B2 to Yang
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1014	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf

1015	File History of U.S. Patent No. 11,081,164 (Appl 16-709,944) to Jia et al.
1016	File History of U.S. Patent No. 11,862,230 (Appl 17-965,527) to Jia et al.
1017	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
1018	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1019	Declaration of Jared Bobrow in Support of Petitioner’s Motion for Admission Pro Hac Vice
1020	Transcript from the March 21, 2025 Deposition of Steven Przyblyski, Ph.D.
1021	Reply Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
1022	Spinelli et al., “Reliability of NAND Flash Memories: Planar Cells and Emerging Issues in 3D Devices,” <i>Computers</i> 2017, 6, 16 (2017)

I. INTRODUCTION

Petitioner submits this reply in support of its Petition (Paper 1) for IPR of the '822 patent. Patent Owner's response repeatedly fails to consider the totality of the prior art's teachings, misreads the claims, and is replete with technical and legal errors.

Patent Owner begins by arguing that the signals Lee applies to its word lines during pre-charging are not "pulses." Here, however, Patent Owner does not account for what Lee actually discloses. According to Lee, pre-charging occurs in a *distinct* step that is *completed* before programming. A POSITA would have understood this to mean that Lee's pre-charge voltages are supplied as pulses. Indeed, supplying programming voltages as distinct, controlled pulses—as was admittedly routine in the art when the '822 patent was filed—*requires* that pre-charge voltages also be supplied as pulses. Otherwise, unwanted programming would occur (either due to poor pre-charging or a disruption of the program voltages).

Next, Patent Owner attempts to distinguish Lee from certain of the '822 patent's dependent claims. But in so doing, it reads limitations into the claims that simply are not there. Per Patent Owner, the claims somehow require a memory's word lines to be *re-grouped* every time a different word line is selected. There is no such requirement. For the challenged claims that are apparatus claims, the process used to group the word lines is irrelevant. For the challenged claims that are method

claims, there is no limit on when (or how often) grouping occurs. All that is required is that there **be** word line groups. This is what Lee teaches.

Patent Owner's arguments regarding Zhao also do not account for the totality of its disclosure. According to Patent Owner, Zhao always leaves its source-side word lines at a "flat" non-pulsed ground voltage during pre-charging. It does not. Instead, Zhao explains that that these word lines—which start at 0 V—can receive a **non-zero voltage** during pre-charging period t1-t3.

Patent Owner also fails to distinguish the combination of Zhao and Lee. Patent Owner argues that a POSITA would consider these two references to be incompatible and fundamentally different. This is because Zhao—per Patent Owner—"precharg[es] via the bitline" without current flow while Lee pre-charges from the common source and employs current flow. NAND pre-charging does not work this way. Current is never applied during pre-charging. Instead, potential differences between a NAND string channel and the word lines act to purge and redistribute electrons in the channel. Because pre-charging requires only potential differences—not applied current—it does not matter whether a voltage is applied to the channel's source or drain side. A POSITA would have understood these references to be compatible, directly applicable to each other, and complementary.

Patent Owner concludes by addressing Yang. According to Patent Owner, two of Yang's three pre-charge voltages are supposedly "identical." But the only thing

Patent Owner does to arrive at this conclusion is visually compare Yang's signals in its figures. Not only does this invite legal error (patent figures do not supply precise dimensions) but it entirely ignores that Yang separately discusses and details the provision of three different voltages during pre-charging.

II. ARGUMENT

A. Ground 1: Lee Renders the Claims Obvious

Ground 1 explained why Lee renders the '822 patent's claims obvious. Patent Owner's attempts to distinguish Lee lack merit.

1. *Lee Applies "Pre-Pulse Signal[s]" to Its "Word Line[s]"*

The '822 patent's claims require application of certain "word line pre-pulse signal[s]" to different groups of word lines "during a pre-charge period." Ex. 1001, claim 1. While Patent Owner includes a lengthy section in its Response discussing the meaning of the term "pulse," there is no dispute that to be a "pulse," an applied "signal" must "increase in value and then decrease in value (or vice versa)." Response, 13.¹

¹ Patent Owner incorrectly states that "Dr. Liu was unable and unwilling to define the term 'pulse'" during his deposition. Response, 17 n.1. In fact, following the very testimony that Patent Owner quotes, Dr. Liu walked through what this term means in the '822 patent. Ex. 2021, 25:17-28:2, 28:20-29:12. While Dr. Liu did not answer questions regarding hypothetical "waveforms" shown in Ex. 2020, none

Patent Owner argues that the voltages applied to Lee's word lines during pre-charging do not necessarily "increase and then decrease." Response, 29. According to Patent Owner, because "Lee does not disclose any waveforms or timing characteristics," its "pre-charge" voltages could instead be "applied as a single, flat value followed immediately by programming voltages." *Id.*, 31. While programming voltages were routinely supplied as pulses in the prior art, Patent Owner posits that doing the same with Lee's pre-charge voltages would purportedly "serve no purpose" and would somehow be inconsistent with Lee's goal of "uniform" pre-charging. *Id.*, 29-31. These arguments fail to account for Lee's teachings and lack technical basis.

As already explained in the Petition (Petition, 37-38), Lee plainly teaches that pre-charging and programming occur in **separate, distinct steps**. For instance, as shown in Figure 7, Lee's "precharging" occurs in an earlier step S205, while a "program" operation is performed in separate later step S207. Lee, Fig. 7, 11:13-22; 11:34-40 (similarly referencing separate "precharging" and "program" steps). Lee also explains that pre-charge voltages are applied only "**during** a precharge

of these have any relevance to the prior art at issue here. Indeed, Patent Owner's expert similarly declined to offer opinions regarding the exhibit. Ex. 1020, 9:25-11:18.

operation” or “precharging step.” *Id.*, 7:58-61 (emphasis added); 7:63-65; 8:15-17; *see also* 8:25-29; 8:32-47; 8:53-64 (pre-charge voltages applied “during” specific steps or periods of operation). And according to Lee, “program” and “pass” voltages are not applied to Lee’s word lines until “***after*** ... the precharge operation is ***completed.***” *Id.*, 9:7-14 (emphasis added).

Patent Owner effectively negates all this. Rather than giving effect to Lee’s teaching that pre-charging occurs in a ***separate*** step that is ***completed*** before programming, Patent Owner improperly blends Lee’s steps together into a ***single, continuous*** operation. Patent Owner argues that Lee’s pre-charge voltage could be applied as a “single, flat value followed immediately by programming voltages.” *E.g.*, Response, p. 31. NAND memory does not operate this way. Word line potential does not instantaneously change. Ex. 1021, ¶¶ 10-12. There will necessarily be a period of ramp up as the potential moves from an original to another value. *Id.*; Ex. 1020, 53:16-54:8 (agreeing that there is a period of “ramp-up”). This operation is reflected throughout the prior art. *E.g.*, Zhao, Fig. 13 (showing word line potential gradually increasing when voltage is applied and gradually decaying when voltage is removed); Yang, Figs. 8B, 9B (similar).

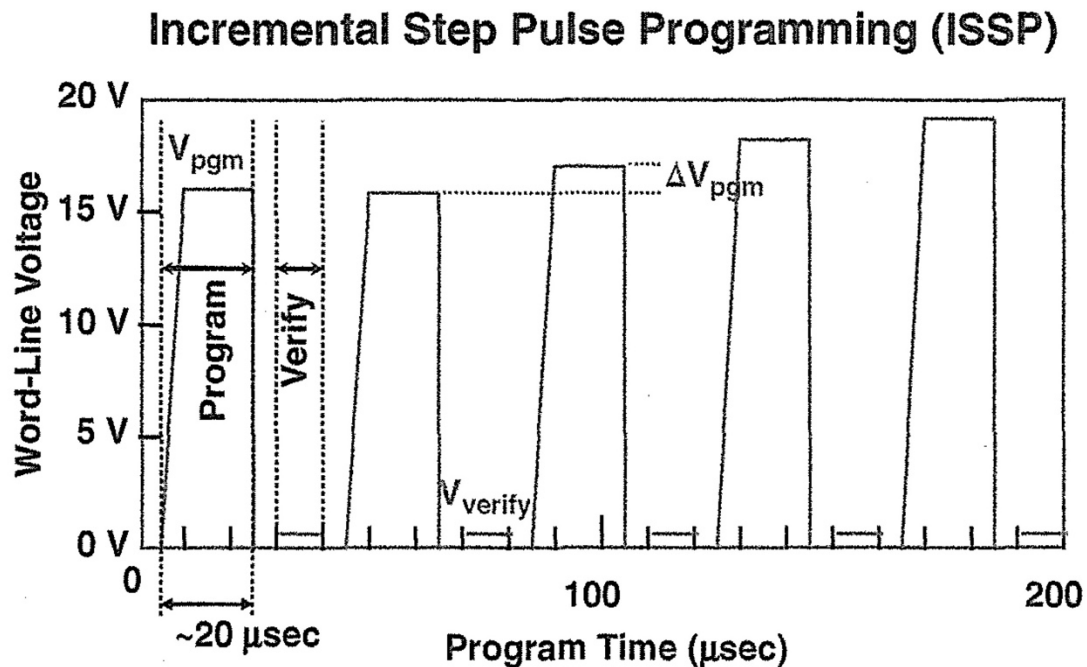
Lee teaches the use of different voltages during a pre-charging and a later programming phase. Lee, 6:29-35 (discussing the application of “pass” and “program voltages” during a programming phase); 7:58-62 (discussing the

application of “different pre-bias voltages” during pre-charging). These voltages will need to be generated—typically by a charge pump—and then supplied to the appropriate word lines. Ex. 1020, 12:6-25 (Patent Owner’s expert recognizing that charge pumps are present in most commercial NAND when ’822 patent filed); 15:2-20 (known row decoders contribute to turning word lines off/on), 33:9-16 (charge pumps “known and commonly used”). This prevents word line voltage from “immediately” transitioning from the pre-charge to the programming value. Ex. 1021, ¶¶ 21-30. Instead, there will be a period of transition as voltage switches from one value to another. *Id.*, ¶¶ 11-14, 28-29. If Lee’s different voltages are not pulsed, and were for some reason piled on top of each other, this ramp up period would cause pre-charging to continue for some indeterminate period while programming voltages are being applied. Ex. 1021, ¶¶ 13-20. Once again, this is not how Lee operates. Per Lee, programming voltages are not applied until after pre-charging is “completed.” Lee, 9:7-14; Ex. 1020, 47:14-25, 48:15-22, 49:13-17 (Patent Owner’s expert confirming that programming in Lee does not occur until pre-charge “has been set up[,] “has run its course[,]” and “achieved its desired result”). To achieve separate pre-charging and programming as Lee instructs—as opposed to blended pre-charging/programming—a POSITA would have understood that the voltages applied to Lee’s word lines would need to be (or at the very least would obviously be) pulsed. Ex. 1021, ¶¶ 15-20.

Next, Patent Owner is also wrong when it argues that there is no “rationale why using pulses for a subsequent programming step would require or render obvious pulses to be used for pre-charge signals.” Response, 35. To begin, Lee employs a standard “voltage generation unit” and “address decoder” to supply voltages to its word lines. Lee, 5:60-62, 6:19-39. These well-known components supply voltages in the form of pulses. Ex. 1021, ¶¶ 21-29, 36. Next, Patent Owner does not dispute that programming voltages were routinely supplied in the form of pulses in the prior art. Response, 34-35. Lee includes a shared “voltage generation unit 150” that outputs **both** its pre-charge and programming voltages. Lee, 7:13-19; *see also* 6:19-21, 6:28-36, Fig. 1; Ex. 1020, 40:8-41:3 (programming and pre-bias voltages “flow” to the word lines along the same path). A POSITA would plainly have understood that because Lee’s pre-charging and programming voltages are generated by the same type of unit, they would obviously have the same form. Ex. 1021, ¶¶ 21-29, 36-39.

A POSITA also would have understood that use of well-known pulsed programming voltages **requires** that the pre-charge voltages **also** be pulsed. An “incremental step pulse programming” (or ISPP) “scheme has been used in NAND flash memory products for a long time, more than 20 years, due to fast programming speed, tight V_t distribution, and excellent reliability.” Ex. 1006, 118; Ex. 1012, 82 (cell programming is “typically accomplished by” ISPP). This type of pulsed

programming entails repeated application of “program voltages to the selected cells for the desired amount of time (typically some microseconds).” Ex. 1008, 354. An example of this is shown below:



Ex. 1006, 146. As shown, to perform ISPP, the word line voltage starts at 0 V. *Id.* Then, a series of voltage pulses—each with a particular duration and magnitude—are applied to program the memory cell allowing it to reach the desired threshold voltage. *Id.*; see also Ex. 1021, ¶¶ 40-43; Ex. 1020, 18:13-19:6, 19:17-23:10 (typical ISPP programming starts at 0 V, pulses, returns to 0 V, etc.). When using ISPP, pass voltages applied to unselected word lines must also be pulsed—with the same pulse duration as the selected word line—to avoid program disturb. Ex. 1021, ¶ 44; Ex. 1020, 25:5-25 (pass and program voltages need to be applied at same time). Lee applies pre-charge voltages to all its word lines—including both the selected and

unselected lines—during the same pre-charge period. If pre-charging were not pulsed, the later programming procedure would be altered. The first pulse applied to each word line would no longer have the intended magnitude and duration. Instead, it would be combined with the pre-charge voltage (which never returned to zero), resulting in an indeterminate and undesired increase in programming. Ex. 1021, ¶¶ 45-49. This would defeat the purpose of ISPP: a “tight V_t distribution” and “excellent reliability” (Ex. 1006, 118) would no longer be achieved via specific, controlled programming pulses.

Patent Owner also is wrong that using pulses “would not serve Lee’s stated goal of ‘uniformity...’” Response, 35. It is Patent Owner’s proposed voltage provision scheme—not the use of pulses—that would reduce “uniformity.” Because word line potential is unable to instantaneously shift, applying the programming or pass voltage immediately after pre-charging without first allowing potential to return to 0 V will result in some indeterminate amount of extra unintended pre-charging that disrupts the desired pre-charge level. Ex. 1021, ¶¶ 31-35. A POSITA would have readily understood that this unwanted effect is avoided (and uniformity is maintained) by separating the pre-charge and programming periods in time. *Id.* The memory would also become inordinately complicated (requiring more voltage sources to facilitate continuous voltage supply). *Id.*

Finally, it bears noting that neither Patent Owner nor its expert points to any actual evidence supporting their assertions. No examples of prior art references employing a “single, flat value followed immediately by programming voltages” are provided. Ex. 1020, 51:5-19. And no evidence is provided showing why pulses would decrease “uniformity.” These types of bald, conclusory assertions are entitled to no weight. *E.g., Coalition for Affordable Drugs VII LLC v. Pozen Inc.*, Case IPR2015-01680, Paper 18 at 15 (Feb. 11, 2016).

2. Lee’s Groups Are “Disposed in Order of Distance from the Selected Word Line”

Claim 2 of the ’822 patent requires that the “**first**,” “**second**,” and “**third**” groups of word lines present in claim 1’s “memory device” be “**disposed in an order of distance from the selected word line of the plurality of word lines.**” Ex. 1001, claim 2. Claim 12—which depends on claim 11—includes the same limitation. Patent Owner argues that this excludes word line groups that are “predetermined” and “do not change based on the position of the selected word line.” Response, 36.

This improperly reads limitations into the claims. Claim 2 is an apparatus claim. “[A]pparatus claims cover what a device is, not what a device does.” *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469 (Fed. Cir. 1990). Thus, for purposes of claim 2, it does not matter when the word lines are divided. All that matters is that there be “first,” “second,” and “third” “groups” of word lines to which different pre-charge voltages referenced by the claim can be applied by the

claimed “control circuitry.” This is exactly what Lee discloses: its word lines are divided into groups and different pre-charge voltages are applied to those groups. Petition, 33-42.

While claim 11 is a method claim, it also includes no requirement that the claimed groups be formed at any particular time. Nor is there any requirement that the groups be re-formed and changed when a different word line is selected. Nor does the specification require reading in such a limitation. The patent explains only that “word lines disposed between the selected word line and a top select gate TSG can be divided into multiple groups....” Ex. 1001, 4:66-5:1. There is no discussion of when this division occurs. There is also no discussion of re-grouping. In the patent’s sole example, WL0 (the bottom-most word line) is selected and the remaining word lines are grouped into three groups. *Id.*, Fig. 3. Limiting the claims in the manner Patent Owner proposes finds no support in the intrinsic record. *Thorner v. Sony Computer Entertainment Am., LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (departing from ordinary meaning requires clear specification lexicography or disavowal of claim scope).

Next, even if the claims did for some reason require repeated re-grouping of word lines—they do not—this is taught by Lee. Lee explains that every time it applies a program voltage to a different selected word line, its control logic “determine[s], based on the result of the grouping, pre-bias voltages to be applied ...

depending on a position of the word line coupled to the target memory cell to be programmed.” Lee, 7:63-65. Different voltages are applied to different word line groups depending on which word line is selected. In Figure 4B, WL11 is selected. *Id.*, Fig. 4B. Per Lee, WL0-WL7 (“Group1”) and WL8-WL15 (“Group2”) all receive a “default” voltage. *Id.*, 9:41-55. WL16-WL23 (“Group3”) and WL24-WL31 (“Group4”) receive increasingly higher voltages. *Id.* So, the word lines on the source-side of selected word line WL11 are divided into three groups (WL12-WL15, WL16-WL23, and WL24-WL31) receiving three different pre-charge voltages. *Id.* Lee goes on to explain that as the selected word line shifts, different voltages are applied. When the selected word line is “included in the third Group3,” WL0-WL23 all receive a “default” voltage while only WL24-31 (“Group4”) receive a “higher” voltage. *Id.*, 9:60-66. So, now there only two groups of word lines (the word lines in Group3 above the selected word line, and WL24-31) receiving two different pre-charge voltages. *Id.* Thus, unlike the ‘822 patent, which includes no such description, Lee does include an example of word line groups that adjust—via the application of different voltages—as the selected word line changes.

3. Lee’s “First Group” Is “Disposed Adjacent to the Selected Word Line”

Claims 3 and 13 require that the **“first group of the plurality of word lines”** be **“disposed adjacent to the selected word line.”** Ex. 1001, Claim 3. Patent Owner simply repeats the same argument it made when addressing claim 2. Response at

38-39. As explained, the claims do not require continually re-dividing the word lines. And Lee teaches this in any event. *Supra* Section II.A.2.

B. Ground 2: Zhao Renders the Claims Obvious

Ground 2 explained why Zhao itself renders many of the '822 patent's claims obvious. Patent Owner does not dispute that Zhao groups its memory's word lines and applies different voltages to the different groups during pre-charging. It also does not dispute that at least some of these voltages are supplied as pulses. The only purportedly missing claim limitation is that requiring ***“first word line pre-pulse signal.”*** Patent Owner argues that Zhao lacks this ***“first”*** signal because it purportedly only applies a “flat signal”—as opposed to a pulse—to word lines WLn-x during pre-charging. Response, 39-44. This does not account for the totality of Zhao's teachings. While a flat 0V signal can be applied to these word lines throughout the pre-charge period, Zhao also discloses an alternative: a non-zero pulsed signals can be used instead.

All of Zhao's various lines start “at 0 volts” (or “Vss”) “[a]t time t0.” Zhao, 22:34-35. Then, between time periods t1-t3, different voltages can be applied to different lines for purposes of pre-charging. *Id.*, 22:39-23:12. At “time t3,” the word lines with applied, non-zero voltages are again “lowered to ground/Vss” and the “pre-charge process has completed.” *Id.*, 23:8-11.

Zhao explains that in one embodiment, the “source side unselected word lines WLn-x” can “**remain** at Vss (e.g., 0 V)” during pre-charge period t1-t3. Zhao, 23:7-9. In other words, no signal or voltage is applied to these word lines and they remain at their starting potential. But this is not all that Zhao teaches. Rather than leaving WLn-x at their starting potential, these “unselected source side word lines” can alternatively “**receive ... one or more voltages** that are too low to pre-charge and/or too low to turn on memory cells in the highest data state (e.g., data state S7).” *Id.*, 19:22-26 (emphasis added). This voltage is applied during pre-charging step 650. *Id.*, 19:9-26. So, Zhao teaches two different ways to handle word lines WLn-x: (1) the word lines can remain at the original potential of 0 V or (2) a variety of non-zero voltage can be applied during pre-charging. As all of Zhao’s voltages are applied in the form of pulses (*e.g.*, *id.*, Fig. 13), a POSITA would have understood that the voltages applied to WLn-x also would be in the form of pulses. Ex. 1021, ¶¶ 57-63.

According to Patent Owner, Zhao’s reference to the application of “one or more voltages that are too low to pre-charge” is just another “flat voltage” applied to WLn-x. Response, 43. Put another way, it appears to be Patent Owner’s position that the “one or more voltages that are too low to pre-charge” are nothing more than an alternative to the Vss/ground employed by Zhao’s various signal lines.

This is inconsistent with and fails to account for the totality of Zhao’s disclosure. Per Zhao, “all” of its signal lines are “at 0 volts (Vss)” at t0 (before pre-

charging). Zhao, 22:34-38. The lines are then “raised” to various “pre-charge voltage[s]” between t1-t3. *Id.*, 22:39-49. Period t1-t3 “corresponds to the pre-charging” “steps 650 and 622 of Fig. 10....” *Id.* Then, the lines are “all lowered to ground/Vss” after t3 when pre-charging is complete. *Id.*, 22:34-50, 23:5-12; *see also* Ex. 1020, 66:10-67:19, 68:4-25 (confirming Zhao’s operation). According to Zhao, the “one or more voltages that are too low to pre-charge” are “received” by WLn-x during “pre-charge” steps 650 and 652. Zhao, 19:12-26. This is plainly referring to a voltage that is applied to WLn-x during the same pre-charging period t1-t3 discussed throughout Zhao. Zhao does not say that the “one or more voltages that are too low to pre-charge” are applied to WLn-x at all times as a “flat” voltage or replacement for the ground voltage. Instead, these voltages are received by the lines only during pre-charge.

This is why Zhao renders the claims obvious: WLn-x start at 0 V at t0 (just like all of Zhao’s lines), are “raised” to “one or more voltages that are too low to pre-charge” during t1-t3, and then return to 0 V after t3 (once again, like all Zhao’s lines). Ex. 1021, ¶¶ 50-62. Patent Owner has not meaningfully addressed these collective teachings. Instead, it simply discusses the different portions of Zhao in isolation. This was improper: it is the “combined teachings” of the art that must be considered. *In re GPAC Inc.*, 57 F.3d 1573, 1581 (Fed. Cir. 1995). When all of Zhao’s teachings

are considered together—as they must be—it is apparent that Zhao renders the claims obvious.

C. Ground 3: Zhao and Lee Render the Claims Obvious

Ground 3 in the Petition explained why Zhao, when modified following Lee’s teachings, renders the claims obvious.

Patent Owner does not dispute that Zhao and Lee—at least separately—disclose all the ’822 patent’s claim limitations. Instead, Patent Owner argues only that a POSITA would not have been motivated to use Lee’s different pre-charge voltages with Zhao. Response, 44-58. According to Patent Owner, “Lee is concerned with problems arising from pre-charging operations performed via the common source line, while Zhao instead performs charging from the bit line.” *Id.*, 48. Patent Owner also argues that in Lee, there is “current running” through the memory string channel during pre-charging, while there is no such flow in Zhao because certain of its transistors are closed. *Id.*, 50-52. Patent Owner then posits that because of this, Zhao does not need and cannot use Lee’s teachings. *Id.*

This is wrong and misunderstands how pre-charging occurs in 3D NAND memory. There is no meaningful difference between “precharging via the bitline” versus the “source line.” Moreover, neither Lee nor Zhao applies current during pre-charging.

The purpose of pre-charging is to prepare a NAND memory string's channel for later programming. *E.g.*, Yang, 2:23-24 (discussing “pre-charging NAND strings” before a “program operation”). Pre-charging entails only the application of voltages. No current is applied because only one select gate is open during the programming phase of operation. Ex. 1021, ¶¶ 64-70; Ex. 1006, p. 45 (noting that in NAND, only one select gate is open—not both—during program operations). Indeed, any current flow during the programming phase would collapse the charge pumps applying voltages to unselected strings either for pre-charging purposes or to inhibit programming. Ex. 1021, ¶ 69. The voltages applied during pre-charging are intended only to purge and redistribute electrons already in the channel that may later cause program disturb. *E.g.*, Lee, 1:52-56 (discussing the mitigation of “program disturb”); Zhao, 17:4-12 (noting that “program disturb” can be caused by “electrons trapped in the channel”). The overall amount of channel pre-charging (*i.e.*, total electron movement and purging) is controlled by applying a voltage to the channel itself. Ex. 1021, ¶¶ 72-78. The relative amount of charging along the channel (*i.e.*, the electron distribution) is controlled by applying different voltages to the word lines associated with the channel. *Id.* A greater potential difference between the voltage applied to a particular word line and the voltage applied to the channel results in more pre-charging in the portion of the channel associated with that word line. Because its purpose is simply to create a potential difference that

facilitates electron redistribution, the channel voltage can be applied to either end of the channel (so long as there is electrical connection between the point where the voltage is applied to the channel and the portion of the channel targeted for pre-charging). *Id.*, ¶¶ 77-78; *see also* Yang, 17:16-23 (3D memory’s channel can be pre-charged from the “drain end of the NAND string” or the “source end”).

Given all this, a POSITA would have understood that Lee and Zhao are not only compatible, but provide complementary solutions to the same problem. Both address program disturb. *E.g.*, Lee, 1:52-56; 2:18-25. And both employ the same general approach: they create voltage differentials between a NAND channel and word lines to control channel charge distribution. *Id.*, 1:62-2:32; Zhao, 19:9-56. The only real difference between Lee and Zhao is the portion of the channel they address.

Lee seeks to ensure uniform pre-charging in the portion of the channel between the selected word line and the bit line when programming from source to drain. Lee, 8:36-51. According to Lee, when programming in this direction, a “resistance component between the source select transistor and the drain select transistor” operates to relatively reduce the “precharge level” of memory cells closer to the channel’s source side and further away from the bit line that will have an applied voltage during programming. *Id.*, 8:25-32. So, Lee applies lower voltages to word lines closer to the selected word line (resulting in a larger potential difference

with the channel and more pre-charging) and higher voltages to word lines located farther away (resulting in a smaller potential difference and less pre-charging). *Id.*

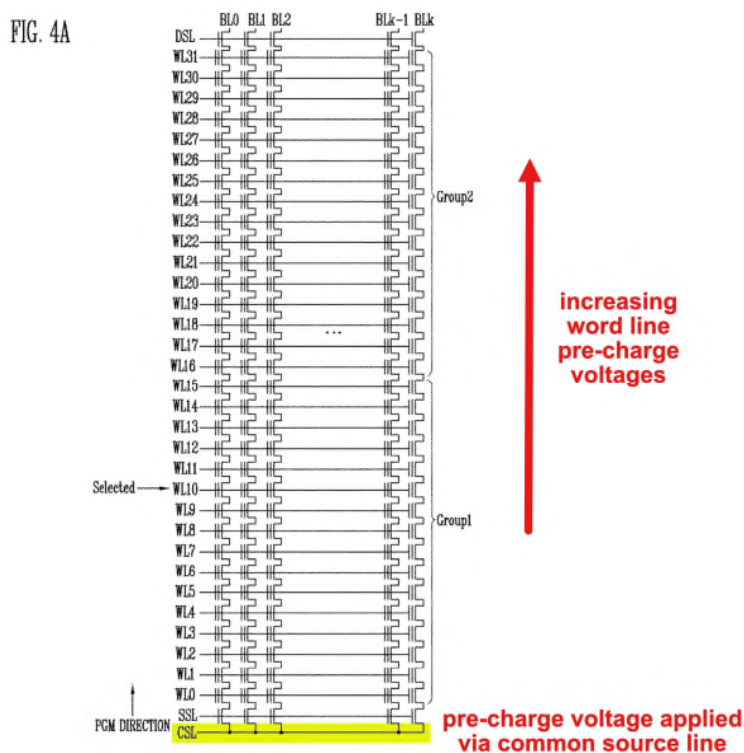
Zhao addresses pre-charging issues in the portion of the channel **crossing** the selected word line. In particular, Zhao seeks to prevent “electrons trapped in the channel [from] being accelerated from one side of a selected word line to another side of the selected word line and redirected into the selected word line” during programming. Zhao, 2:14-18. Thus, it tailors word line voltages around the selected word line to “open the channel from one side of the selected word line to the other side” so electrons can move across the selected word line to “purg[e]” the “already programmed side of the channel.” *Id.*, 2:18-30.

So, together, Zhao and Lee present a complete solution to program disturb: Lee ensures that pre-charging occurs uniformly along the not-yet-programmed portion of the channel. Zhao ensures that charge imbalances across the already programmed and not-yet-programmed portion of the channel do not result in program disturb. Ex. 1021, ¶¶ 79-92.

Next, a POSITA would **not** have considered Lee inapplicable to Zhao. Although Lee applies a “precharge voltage” to its “common source line” (Lee, 2:30-32), this voltage is only meant to create potential differences between Lee’s channel and its word lines. The **very same** effect would be achieved if Lee applied its pre-charge voltage to its bit line. The same channel-to-word line potential differences

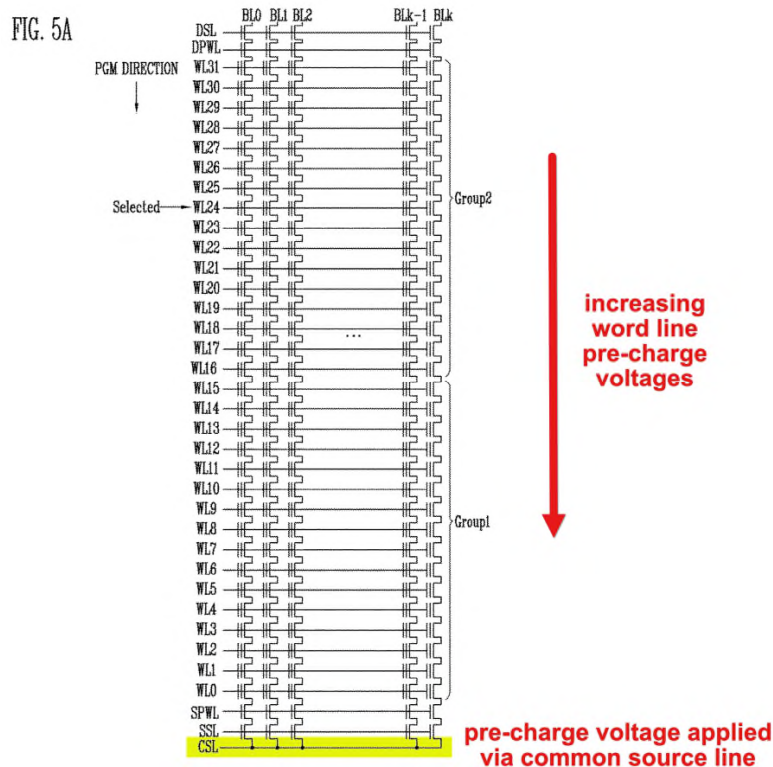
would exist, and the same uniform pre-charge would develop along the channel. Ex. 1021, ¶¶ 93-97.

Lee itself confirms that this is the case. Figure 4A of Lee depicts an embodiment in which Lee's memory array is programmed from source to drain. Lee, 8:18-20. Before programming, a "precharge voltage" is applied to the common source line. *Id.*, 4:65-67. At the same time, pre-charge voltages are also applied to the word lines. These voltages increase with distance from the selected word line in the direction of programming. *Id.*, 8:32-47.



Id., Fig. 4A (annotated). In Figure 5A, however, Lee's memory array is programmed in the opposite direction (from drain to source). *Id.*, 10:16-21. The voltages applied to the word lines still increase in the direction of programming. *Id.*, 10:28-50. This

is the case even though Lee applies voltage to the common source line (and not the bit line) during pre-charging. *Id.*, 1:30-37, 1:52-58, 8:65-67, 11:34-38, 11:45-61, Fig. 8.



Id., Fig. 5A (annotated).

If Lee were operating in the way Patent Owner argues it does—such that Lee’s different pre-charge voltage somehow relates to “current flow” with higher pre-charge voltages further along in this supposed “flow”—then Lee would have applied voltages to its word lines in Figures 4A and 5A in the same way (as a pre-charge voltage is applied to the common source line in both figures). But Lee does not do this. Instead, it **reverses** the order of the word line voltages in Figure 5A. This is because it is only potential differences that matter during pre-charging. And Lee

intends the word lines closest to the selected word line to be subject to relatively more pre-charging. Thus, it applies lower voltages to these word lines. And it does this even though this now positions the word lines receiving the highest pre-charge voltages right next to the source of channel voltage (the common source line). Ex. 1021, ¶¶ 98-107.

Patent Owner also is wrong when it argues that a POSITA would consider Lee limited to supposed problems relating to “current flowing through the memory string” during pre-charging. Response, 50. There is no “current flow” during pre-charging. Pre-charging is accomplished by creating potential differences between the memory channel and the associated word lines. Lee does state that its various pre-charge voltages are meant to “offset” a “resistance component between the source select transistor and the drain select transistor.” Lee, 8:25-29, 8:47-51. This does not mean, however, that Lee supplies current during pre-charging. Instead, as Dr. Liu explained during his deposition, Lee is referring to the fact that the threshold voltages of transistors connected in series along a channel vary in the direction of programming. Ex. 2021, 83:12-84:2 (explaining that there is a “chain effect” on transistor threshold voltages). Lee adjusts the voltages applied to each word line during pre-charging to account for this. Lee, 8:25-29, 8:47-51. Zhao will experience the same problem. Its memory also includes transistors connected in series along a channel. Zhao, Fig. 4G. And when programming from source to drain, the threshold

voltages of Zhao’s transistors will vary in the same way discussed in Lee. Ex. 1021, ¶¶ 108-115. Because Zhao applies the same pre-charge voltages to all its not yet programmed word lines, these variations in threshold voltage will result in inadequate pre-charging in the portion of the channel closest to the selected word line. *Id.*, ¶¶ 115-116. Application of Lee’s groups and word line voltages will eliminate this problem.

So, in sum, a POSITA would have applied Lee’s voltages to Zhao in the same way—and in the same increasing order—that Lee itself teaches. Because Lee achieves uniform pre-charging simply by creating potential differences, the fact that Zhao applies a potential to its channel via the bit line instead of the common source line makes no difference. Patent Owner’s arguments are technically inaccurate and are in direct conflict with what the art teaches. *Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1378 (Fed. Cir. 2017) (no weight given to arguments “plainly inconsistent with the record.”).

Finally, Patent Owner implies in its Response that any effort on the part of Petitioner to correct Patent Owner’s prior art mischaracterizations and technical errors will somehow constitutes a “new argument.” Response, 51 n.6. The Petition already explains how Zhao’s memory operates and why Lee addresses a problem with that operation. Patent Owner responded by misinterpreting and mischaracterizing the prior art. Pointing this out is not “new” argument. It is a

prototypical reply. *Apple, Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 706-07 (Fed. Cir. 2020).

D. Ground 4: Yang Renders the Claims Obvious

Ground 4 explained why yet another reference—Yang—also renders the '822 patent's claims obvious. Here Patent Owner argues that “Yang fails to disclose three signals with incrementally increasing voltages.” Response, 58. According to Patent Owner, two of Yang's pre-charge voltages—Vpre_dmy and Vbypass—would be understood to have “identical values” because their depiction in Yang's figures looks similar when viewed “side-by-side.” *Id.*, 64. “[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes....” *Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000). Yet Patent Owner improperly does just that: it attempts to draw conclusions regarding Yang's pre-charge voltages solely from figure dimensions.

When the totality of Yang's teachings are considered—and not just its figure dimensions—it is apparent that Yang teaches the use of three different pre-charge voltages: an “over-drive voltage” (Vpre_OD), a “bypass voltage” (Vbypass), and a “dummy pre-charge voltage” (Vpre_dmy). Yang, 22:4-37; 24:11-33; Fig. 8B. And it not only shows these in its figures, but it also **describes** these voltages in a way that makes plain that they have (or at least obviously could have) different

magnitudes. In particular, Vpre_OD is the highest of the pre-charge voltages “above all the data states” of the memory’s memory cells. *Id.*, 20:53-55. Vpre_dmy “has a magnitude such that the dummy memory cells will operate as a pass gate” (e.g., conduct a current). ... An example of Vpre_dmy is 5V, assuming” a memory cell “threshold voltage is less than 5V.” *Id.*, 24:18-27. In other words, while Vpre_dmy is lower than Vpre_OD, it is also intended to exceed memory cell threshold voltage. *Id.* The last pre-charge voltage—Vbypass—“is at least Vev, but no greater than Vv7....” *Id.*, 20:64-66. This voltage, unlike both Vpre_OD and Vpre-dmy, is intended to be lower than the memory cell threshold voltages. Petitioner’s expert Dr. Liu explained why this would lead a POSITA to conclude that three different voltages are employed, with Vbypass lowest, Vpre_dmy an intermediate value, and Vpre_OD highest. Ex. 1003, ¶¶ 455-460; Ex. 1021, ¶¶ 117-125. Patent Owner addresses none of this. It does not discuss—let alone dispute—Dr. Liu’s opinions. Instead, it limits itself to an improper comparison of figure dimensions.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: March 28, 2025

/K. Patrick Herman/

K. Patrick Herman, Reg. No. 75,018
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019
Telephone: (212) 506-3596
Email: P52PTABDocket@orrick.com

Attorneys for Petitioner

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing reply complies with the type volume limitation in 37 C.F.R. § 42.24(c). According to the utilized word-processing system's word count, the reply—excluding the portions referenced by § 42.24(c)—contains 5,584 words.

Dated: March 28, 2025

By: /K. Patrick Herman/

K. Patrick Herman (Reg. No. 75,018)
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019-6142
Telephone: (212) 506-3596
P52PTABDocket@orrick.com

Counsel for Petitioner.

CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing paper and associated exhibits were caused to be served via email on the following counsel of record for Patent Owner:

James L. Davis, Jr. (James.L.Davis@ropesgray.com)
Andrew T. Radsch (Andrew.Radsch@ropesgray.com)
Christopher M. Bonny (Christopher.Bonny@ropesgray.com)
Abed R. Balbaky (abed.balbaky@ropesgray.com)
YMTC-Micron-IPRs-Ropes-Service@ropesgray.com
ROPES & GRAY LLP

/K. Patrick Herman/

K. Patrick Herman (Reg. No. 75,018)
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019-6142
Telephone: (212) 506-3702
P52PTABDocket@orrick.com