

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

Civil Action No. 3:23-cv-05792-RFL

YANGTZE MEMORY TECHNOLOGIES
COMPANY, LTD.,

Plaintiff,

v.

MICRON TECHNOLOGY, INC.,

Defendant.

-----/
MICRON TECHNOLOGY, INC.,

Counterclaim Plaintiff,

v.

YANGTZE MEMORY TECHNOLOGIES
COMPANY, LTD., and YANGTZE
MEMORY TECHNOLOGIES, INC.,

Counterclaim Defendants.

-----/

REMOTE DEPOSITION OF STEVEN PRZYBYLSKI, PH.D.

March 21, 2025

Reported by:

KATHY S. KLEPFER, RMR, CRR, CLR, CS-CSR No. 14667

JOB NO. 2025-976768

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March 21, 2025

11:00 a.m. EST

REMOTE deposition of STEVEN

PRZYBYLSKI, PH.D., before before Kathy S.

Klepfer, a Registered Professional Reporter,

Registered Merit Reporter, Certified

Realtime Reporter, Certified Livenote

Reporter, and Certified Shorthand Reporter

in and for the State of Illinois (No.

084.004963) and California (No. 14667).

A P P E A R A N C E S:

(All appearing remotely)

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15	STEVEN PRZYBYLSKI, PH.D., called as a	
16	witness, having been duly sworn by a Notary	
17	Public, was examined and testified as	
18	follows:	
19	EXAMINATION BY	
20	MR. HERMAN:	
21	Q. Good morning, Doctor.	
22	Do you mind stating your name for the	
23	record, please.	
24	A. Good morning. Stephen Przybylski.	
25	MR. HERMAN: And this is Patrick	

1 Herman from Orrick, Herrington & Sutcliffe
2 here on behalf of petitioners.

3 Would patent owner's counsel like to
4 introduce themselves?

5 MR. BALBAKY: My name is Abed Balbaky
6 here representing the patent owner, Yangtze
7 Memory Technology Company.

8 BY MR. HERMAN:

9 Q. Sir, before we begin, I'd like to go
10 over a few basic ground rules to make sure we're
11 on the same page.

12 The first, have you ever been deposed
13 before, Doctor?

14 A. Yes, I have.

15 Q. How many times would you say?

16 A. Probably 25, at least. Maybe 30. I
17 don't know. I'd have to check my records.

18 Q. So you are probably familiar with the
19 procedure, but just to be sure, I'm just going
20 to go through a few things as a reminder.

21 The first is that there's a court
22 reporter here, so it's important that you
23 respond verbally so that the court reporter can
24 record your testimony. Is that okay?

25 A. Yes.

1 Q. It's also important that we not talk
2 over each other so that there is a clear record.
3 I'll do my best to wait for you to finish
4 answering before asking another question, and
5 ask that you wait until I'm done with my
6 question before answering.

7 And it's also important that neither
8 of us interject or interfere with the others
9 talking with an "uh-hum" or something like.

10 Is that okay?

11 A. I understand.

12 Q. You're also entitled to a question you
13 understand. So if anything I ask is unclear,
14 please let me know, and I'll try to clarify,
15 okay?

16 A. Okay.

17 Q. Next, I ask that you not look at
18 anything during the deposition besides documents
19 that I give you, and if you do look at anything,
20 I ask that you tell me. Is that okay?

21 A. Of course.

22 Q. Next, I ask that you not have any side
23 conversations or use technology to chat or
24 otherwise communicate with anyone during the
25 deposition. Is that okay?

1 A. Yes.

2 Q. Now, is there anything that would
3 prevent or interfere with your testimony here
4 today?

5 A. No.

6 Q. So, over the course of the deposition
7 today, I'm going to be putting exhibits that I'm
8 referring to into the chat so that you will have
9 electronic copies, and I'm going to start with
10 one that's been previously marked as Exhibit
11 2011.

12 Let me know when you have that and are
13 able to open it.

14 A. I see it in the chat. I am
15 downloading it now.

16 Okay. I have the file you just put
17 into chat downloaded and on-screen in Acrobat.

18 Q. So what is Exhibit 2011?

19 A. Correct.

20 Q. What is it?

21 A. Oh, I'm sorry. Your volume is a
22 little bit lower than the others. So I
23 apologize for that.

24 It is titled "Declaration of Steven
25 Przybylski, Ph.D., In Support of Patent Owner's

1 Response."

2 Q. And this declaration relates to an
3 IPR2024-00795; is that correct?

4 A. That's what it says on the cover
5 sheet, yes.

6 Q. And that IPR involves U.S. Patent
7 11,501,822, correct?

8 A. Correct.

9 Q. Is it okay if I refer to that patent
10 today as the "'822 patent"?

11 A. I will understand what you mean.

12 Q. And would it be okay if I refer to
13 this as either "your declaration" or your "'822
14 patent's declaration" today?

15 A. I will be clear that that's referring
16 specifically to this declaration and not the
17 POPR declaration; is that correct?

18 Q. That's right.

19 A. I understand.

20 Q. Is there anything in this declaration
21 that you believe to be inaccurate?

22 A. No, I'm not aware of anything.

23 Q. Now, if you turn to page 10 of the
24 declaration. And by "page 10," I'm referring to
25 the numbers that are following the IRP number in

1 the lower left or the lower right corner.

2 Do you see those numbers?

3 A. I do see those numbers, yes.

4 Q. So there's an IPR number and then page
5 10, which is also indicated as page 5 of your
6 document, but for purposes of the deposition
7 today, I'm going to be referring to the page
8 numbers in the lower right corner, okay?

9 A. I understand.

10 Q. So if you can turn to page 10 for me.

11 A. I'm looking at page 10.

12 Q. There is a paragraph 13 that begins on
13 page 10.

14 Do you see that?

15 A. Yes, I see paragraph 13 on page 10.

16 Q. And in that paragraph, there is a list
17 of materials that you reviewed and cited in your
18 declaration; is that correct?

19 A. Yes, it continues into page 11.

20 Q. And one of those is an exhibit that's
21 been designated as Exhibit No. 2020.

22 Do you see that?

23 A. Yes, that is the third-to-last item in
24 this list on page 11.

25 Q. So I'm going to put a copy of Exhibit

1 2020 in the chat so that you have it in front of
2 you, and let me know when you have had a chance
3 to access it and download it.

4 A. I have downloaded it and opened it in
5 Acrobat.

6 Q. So what is that exhibit?

7 A. This is an exhibit from the previous
8 deposition of Dr. Liu.

9 Q. Did you prepare this exhibit?

10 A. No, I did not.

11 Q. Do you know what it is intended to
12 show?

13 A. I don't know who prepared it or what
14 their intent was.

15 Q. So if you turn back to your
16 declaration. That's Exhibit 2011.

17 A. I'm looking at 2011.

18 Q. If you could turn to paragraph 53 of
19 your declaration, which is on page 39.

20 A. I'm on page 39.

21 Q. In paragraph 53, there is a sentence
22 that states, "Similarly, Dr. Liu refused to
23 comment on whether the example waveforms shown
24 in Exhibit 2020 (charting voltage versus time
25 for various sample waveforms) could qualify as a

1 pulse."

2 Do you see that statement?

3 A. Yes, I see that sentence.

4 Q. Now, in this declaration, you also do
5 not comment on whether the example waveforms
6 shown in Exhibit 2020, charting voltage versus
7 time, for various sample waveforms could qualify
8 as a pulse, true?

9 A. That's correct; that is not an opinion
10 that I have rendered in this declaration.

11 Q. That's an opinion that is nowhere to
12 be found in this declaration, correct?

13 A. That's correct; for this declaration,
14 I have been adopting the petitioner's proposed
15 interpretation of word line pre-pulse signal and
16 pulse, generally. So I did not concern myself
17 with anything further than that with regard to
18 what is or is not a pulse.

19 Q. Now, do you have a general
20 understanding of how NAND memory is structured
21 and operated, particularly at the time the '822
22 patent was filed?

23 A. Are you referring specifically to 3D
24 NAND or NAND, generally?

25 Q. NAND, generally.

1 A. Yes, I'm generally familiar with how
2 NAND flash operates at this time frame and
3 presently.

4 Q. How about 3D NAND?

5 A. Similarly, yes, same answer.

6 Q. Do you know what a charge pump is?

7 A. Yes, I know what a charge pump is.

8 Q. What is a charge pump?

9 A. A charge pump is a circuit board
10 generating a voltage that is not -- that is
11 different from supply voltages.

12 Q. Were charge pumps used by either NAND
13 or 3D NAND at the time the '822 patent was
14 filed?

15 A. Charge pumps are used in a wide
16 variety of semiconductor memories. They don't
17 have to be used, but, in general, for
18 commercially available products, they are
19 present.

20 Q. And was that the case when the '822
21 patent was filed?

22 A. I believe so, but I haven't actually
23 looked at any circuit diagrams or documentation
24 to confirm that specifically with regard to any
25 commercially available NAND flash devices.

1 Q. Can you briefly summarize for me how a
2 charge pump works?

3 MR. BALBAKY: Objection. Relevance.

4 THE WITNESS: I don't believe I've
5 talked about charge pumps anywhere within my
6 declaration, so I am -- if there's a
7 paragraph in my declaration you would like
8 to refer me to that talks about charge
9 pumps, I would be happy to comment on that,
10 but --

11 That's all.

12 BY MR. HERMAN:

13 Q. So, sitting here today, without
14 specifically referring to a paragraph in your
15 declaration, you're not able to provide a
16 general description about how a charge pump
17 works?

18 MR. BALBAKY: Objection to form.

19 BY MR. HERMAN:

20 Q. Fair characterization?

21 A. Since we're here today to talk about
22 my declaration in this IPR and my opinions
23 therein, I have not reviewed charge pump
24 circuits or their operation in preparation for
25 this declaration. I'm not willing to delve into

1 that unprepared territory.

2 Q. So what does a row decoder do in NAND
3 memory?

4 A. Row decoders are generally circuits
5 found within all manner of semiconductor
6 memories that decode an encoded row address into
7 a -- typically, a one-hot form to drive a
8 particular word line or set of word lines.

9 Q. And what do you mean by a "one-hot
10 form"?

11 A. So a row address at a system level is
12 a binary number between, for example, 0 and, you
13 know, 1 million. That would be a ten-digit
14 number. A one-hot form would be where there's 1
15 million lines, and one of them is a servage and
16 the others are not.

17 Q. So would it be fair to say that a row
18 decoder operates to either turn on or turn off
19 particular word lines in the NAND memory?

20 MR. BALBAKY: Objection. Relevance.

21 THE WITNESS: Row decoders are one
22 part of that overall process. You would not
23 be accurate to say that the process of
24 turning on or off a particular word line is
25 solely the responsibility of a row decoder.

1 BY MR. HERMAN:

2 Q. But row decoder contribute to the
3 process of turning on and turning off particular
4 word lines in a NAND memory, true?

5 A. Generally speaking, you will find row
6 decoders in NAND flash memories, but again, this
7 is not something that I have opined upon within
8 this declaration, and so if I did refer to row
9 decoders somewhere in here, I would appreciate
10 your pointing me at that.

11 Q. Is anything I said inaccurate? Is
12 there anything inaccurate with my statement that
13 row decoders contribute to the process of
14 turning on or turning off word lines in a NAND's
15 memory?

16 A. Generally speaking, that is an
17 accurate statement. Although, I'm sure you
18 could find counterexamples for which that's not
19 necessarily true, but I'm not familiar with any
20 sitting here today.

21 Q. So I'm going to put another exhibit in
22 the chat, and this one's been previously marked
23 as Exhibit 1012.

24 Let me know when you have got that.
25 Unfortunately, it's rather large so it may take

1 a moment.

2 A. I have textbook "Inside Solid State
3 Drive (SSDs)" by Rino Micheloni, et al., up in
4 Acrobat.

5 Q. Okay. Now, I'm going to refer once
6 again to the page numbers that are at the bottom
7 right corner as opposed to this exhibit's own
8 textbook page numbers.

9 Is that okay?

10 A. I understand.

11 Q. And I'd like to direct you to page 82,
12 which also happens to be the 82nd page of the
13 PDF that I have given you.

14 A. 82, you say?

15 Q. Yes.

16 A. The one with Figure 4.5 at the top of
17 it?

18 Q. That's right.

19 A. I'm there.

20 Q. So the last paragraph on this page
21 states with the phrase "when a floating gate
22 cell."

23 You see that?

24 A. I see that paragraph.

25 Q. And it goes on to say, "...is intended

1 to be programmed to a certain Vth state, this is
2 typically accomplished by the so-called
3 'incremental step pulse programming' (ISPP)
4 scheme."

5 You see that?

6 A. I see that sentence.

7 Q. So "Vth" in that sentence is referring
8 to the desired threshold voltage of a memory
9 cell, correct?

10 A. "Vth," as an acronym or a symbol for
11 threshold voltage, applies to all transistors,
12 not just memory cells, but in this sentence,
13 it's referring to a floating gate cell, in
14 particular.

15 Q. And that floating gate cell is one
16 memory cell within the NAND memory, correct?

17 MR. BALBAKY: Objection. Foundation.

18 THE WITNESS: This section of
19 Micheloni is referring to floating gate
20 cells, which are one type of NAND memory
21 cells that were common in the past.

22 BY MR. HERMAN:

23 Q. So the sentence that I read also
24 references "incremental step pulse programming"
25 and then uses the acronym "ISPP" for that; is

1 that right?

2 A. That is what it says on that page.

3 Q. And the sentence explains that
4 programming in NAND memory was typically
5 accomplished using ISPP at the time this
6 particular book was published, correct?

7 MR. BALBAKY: Objection. Relevance.

8 THE WITNESS: Again, that's what it
9 says, yes.

10 BY MR. HERMAN:

11 Q. What does ISPP entail?

12 MR. BALBAKY: Objection. Relevance.

13 THE WITNESS: So that paragraph goes
14 on to explain what goes on within the
15 incremental step pulse programming
16 methodology. It says, to reach a target
17 cell threshold, programming pulses with
18 durations in the range of TPP equals 100
19 microseconds are applied with increasing
20 pulse amplitude.

21 BY MR. HERMAN:

22 Q. So multiple pulses with a particular
23 length and increasing pulse and amplitude are
24 supplied, correct?

25 A. Within the construct of a floating

1 gate cell being programmed with what Micheloni
2 is calling ISPP.

3 Q. And Micheloni also states that, "Each
4 programming step is followed by a sense
5 operation to evaluate whether the target Vth has
6 already been reached," true?

7 A. That is what Micheloni says, yes.

8 Q. Now, I'm going to put yet another
9 exhibit in the chat, and this one has been
10 previously marked as Exhibit 1006.

11 And once again, it's large. This time
12 it's so large that it comes in two pieces. So
13 I'm going to send you both of the pieces so you
14 have the complete exhibit.

15 A. You want me to open one in particular,
16 or just download both and open both?

17 Q. You can download both, but we're going
18 to start with the first, Exhibit 1006.

19 A. As you said, they're large. Give me a
20 moment, please.

21 Are we done with Exhibit 1012?

22 Q. For the moment, but we'll be going
23 back to it so I would keep it handy.

24 A. Fair enough.

25 Okay. I have Exhibit 1006-1, part 1,

1 of book "NAND Flash Memory Technologies" by
2 Aritome up in Acrobat.

3 Q. And this exhibit is among the
4 materials listed in your materials considered,
5 true?

6 A. Yes, it is listed on page 10 of my
7 declaration as a reference that I reviewed in
8 preparation of my declaration.

9 Q. Now, if you could turn to page 46,
10 again referring to the page numbers in the
11 bottom right corner.

12 A. I am on page 46.

13 Q. And there's a figure at the bottom of
14 the page entitled "Incremental Step Pulse
15 Programming"?

16 A. Figure 2.13, yes.

17 Q. Which has the acronym "ISSP," for some
18 reason, after it, correct?

19 A. There seems to be some confusion about
20 how you get an acronym from an English phrase,
21 but it is consistently labeled "ISPP" in some
22 cases and "ISSP" in other cases.

23 Q. So the figure that's there is meant to
24 provide an example of incremental step pulse
25 programming, true?

1 A. That is a reasonable interpretation of
2 the bottom half of page 46 and the title and
3 caption for Figure 2.13.

4 Q. And Figure 2.13 includes both an X
5 axis that's labeled "Program Time" in
6 microsecond units, and a Y axis labeled "word
7 line-Line Voltage" that's in volts, correct?

8 A. Yes, that's correct.

9 Q. And in Figure 2.13, at time 0, the
10 word line voltage is 0, correct?

11 A. I'm sorry. Will you repeat that,
12 please? I wasn't expecting that.

13 Q. In Figure 2.13, at time 0, the word
14 line voltage is indicated to be 0, correct?

15 MR. BALBAKY: Objection. Relevance.

16 THE WITNESS: 0 volt is coincident
17 with the X axis, so it's potentially a bit
18 confusing, but a POSITA looking at this
19 would interpret the word line voltage being
20 diagrammed in this graph as being 0 volts at
21 time T equals 0.

22 BY MR. HERMAN:

23 Q. And then, at some subsequent time, the
24 voltage increases to somewhere north of 15 volts
25 for what's indicated to be a period of

1 approximately 20 microseconds, is that true?

2 A. Yeah, "north" is not really a good
3 adjective here. I would say "greater than,"
4 since we're not talking about directions, but
5 with that caveat, that is a reasonable
6 interpretation of what's shown in Figure 2.13.

7 Q. And then at some later time, the word
8 line voltage goes back to 0 volts, true?

9 A. Again, that's what a POSITA looking at
10 Figure 2.13 would interpret from this figure.

11 Q. And then, at a still yet later time,
12 the figure indicates that there is a "Verify,"
13 correct?

14 A. There is a region of time that's
15 marked as a "Verify," yes.

16 Q. And then after that region of time
17 marked as "Verify," the voltage on the word line
18 again goes from 0 to some voltage value that's
19 greater than 0 for a period of time, correct?

20 A. Yes, that's correct.

21 Q. And this process in the figure repeats
22 itself a number of times, true?

23 A. In this particular figure, there are
24 shown as five specific time periods when there
25 is an elevated voltage on the word line.

1 Q. Is what's shown in this figure
2 representative of how ISPP would have typically
3 been performed at the time the '822 patent was
4 filed?

5 MR. BALBAKY: Objection. Relevance.

6 THE WITNESS: Well, certainly that is
7 Aritome's intent here, to teach what he
8 understands the programming scheme ISPP to
9 entail. So that's what he's trying to
10 teach.

11 BY MR. HERMAN:

12 Q. And in your view, is there anything
13 inaccurate about that teaching?

14 A. There's nothing inaccurate in this
15 page that I would take exception with, but we
16 have not established any relationship between
17 this textbook and any of the subject matter in
18 my declaration or in this case generally.

19 Q. Now, in a NAND's memory, only the word
20 line that is selected receives the programming
21 voltages, correct?

22 MR. BALBAKY: Objection. Form.

23 THE WITNESS: That's an
24 oversimplification and is not strictly
25 accurate as phrased.

1 BY MR. HERMAN:

2 Q. So the unselected word lines receive
3 what is called a pass voltage, true?

4 A. When?

5 Q. During programming.

6 A. When during programming?

7 Q. So when the selected word line is
8 receiving a programming voltage.

9 A. Okay. So would you rephrase the
10 question, please, with all of its caveats?

11 Q. So maybe we'll start at the beginning.
12 During programming, the selected word
13 line will receive a programming voltage, and at
14 the same time, the unselected word lines will
15 receive a pass voltage, true?

16 A. What Aritome says in page 45 showing,
17 in Figure 2.12, the program operation of a NAND
18 flash cell array, is, as you indicated, that
19 there is one word line that receives the program
20 and the other word lines, within this fraction
21 of the overall memory array, would receive the
22 Vpass voltage of about 10 volts.

23 Q. And one of the purposes of supplying
24 the pass voltage to the unselected word lines is
25 to reduce the potential difference between the

1 selected word line and the unselected word line
2 during a program operation, true?

3 A. Does he say that specifically
4 somewhere within this text?

5 Q. I'm asking for your understanding as
6 an expert regarding how NAND is meant to
7 operate.

8 A. Well, there are many different schemes
9 for programming NAND flash memories with
10 different variations on different word line
11 voltages during the program pulses and otherwise
12 during the program operation.

13 So the purpose of the pass is
14 principally to turn on memory cells so that the
15 cell that is being -- or, the cells that are
16 being programmed are able to be properly
17 programmed.

18 Q. Right, so that pass voltage needs to
19 be supplied to the unselected word lines at the
20 time the program voltage is being supplied to
21 the selected word line, true?

22 A. Yes, that's true because, otherwise,
23 you are not going to be able to program the
24 selected memory cells as indicated by the data
25 to be programmed.

1 Q. Now, if we could go back to Exhibit
2 1012. If you could turn to page 89 for me.

3 A. 89. I'm looking at page 89.

4 Q. And the last paragraph that's on page
5 89 starts with the words, "The general effect of
6 a..."

7 Do you see that?

8 A. I see that paragraph.

9 Q. And the first sentence of that
10 paragraph reads, "The general effect of a pass
11 voltage variation on a program disturbed and a
12 pass disturbed cell..."

13 Do you see that?

14 A. I see these words, yes.

15 Q. So this paragraph is noting that both
16 applied program voltages and applied pass
17 voltages can have an effect on program
18 disturbed, correct?

19 A. I'm going to read a more significant
20 portion of this section of the book, so just
21 give me a moment, please.

22 Will you repeat the question, please?

23 Q. Yes. So this paragraph is noting that
24 both applied program voltages and applied pass
25 voltages have an effect on program disturbed,

1 correct?

2 A. This section of Micheloni's book is
3 talking about a particular programming structure
4 for floating gate NAND cells and is describing a
5 particular programming pulse sequence shown in
6 Figure 4.11 on page 88 of the textbook. And in
7 his analysis of this particular programming
8 step, he notes that if the pass voltage is too
9 high, there are consequences; and if it's too
10 low, it doesn't turn on the appropriate cells
11 that are not to be programmed.

12 So, yes, he is saying that, in the
13 extreme, both the pass voltage can disturb the
14 adjacent cells in the context of this particular
15 programming methodology.

16 Q. Now, there's a sentence that starts on
17 the bottom of page 89 that continues on to page
18 90 that reads, "In addition to the pass voltage
19 pulse amplitude value, the number of disturbing
20 pulses is very important for the disturb
21 strength."

22 Do you see that?

23 A. Yes, I see that sentence.

24 Q. And then, towards the end of the
25 paragraph, there's a sentence that reads,

1 "Finally, a NOP equals 10 results in
2 approximately 100 program pulses with the
3 highest program voltage assumed for the slowest
4 cell in programming and about 5000 pass voltage
5 pulses, because each of the 64 cells in the
6 string needs to be programmed."

7 Do you see that?

8 A. I see that sentence on page 90, yes.

9 Q. So this is referring to a program
10 operation where there are both program pulses
11 and pass voltage pulses, correct?

12 MR. BALBAKY: Objection. Relevance.

13 THE WITNESS: This paragraph does
14 refer to program pulses and pass voltage
15 pulses, again, in the context of the
16 particular programming structure that is
17 being described in this section of
18 Micheloni's text for floating gate NAND
19 cells and a particular NAND flash memory
20 array with a particular number of cells on
21 the strings and so forth.

22 So it's a very narrow statement about
23 pass voltage pulses and program pulses.

24 BY MR. HERMAN:

25 Q. Now, if you could turn to page 181 for

1 me.

2 A. Page 181, yes.

3 Q. There's a section that begins on that
4 page that's entitled "6.7, Erase," do you see
5 that?

6 A. I see the start of that section, yes.

7 Q. And the section begins by saying, "The
8 erase operation resets the information of all
9 the cells belonging to one block
10 simultaneously."

11 See that?

12 A. That's what it says there on page 181.

13 Q. Then the next paragraph references
14 Table 6.1 and 6.2. You see that?

15 A. Yes, it does reference those tables
16 there on page 181.

17 Q. And then the following sentence says,
18 "During the erase pulses."

19 Do you see that?

20 MR. BALBAKY: Objection. Relevance.

21 THE WITNESS: Yes, the next sentence
22 does begin "during the erase pulse."

23 BY MR. HERMAN:

24 Q. So this is referring to an erase
25 procedure in NAND's memory where voltages are

1 supplied in the form of a pulse, true?

2 MR. BALBAKY: Objection. Foundation.

3 THE WITNESS: Could you repeat the
4 question, please?

5 BY MR. HERMAN:

6 Q. Exhibit 1012 in the sentence I just
7 read is referring to voltages supplied during an
8 erase operation in the form of a pulse, correct?

9 A. Yes, the sentence that you have
10 outlined does use the phrase "erase pulse."
11 Chapter 6 of Micheloni's book, written
12 by Crippa and Micheloni, is describing a
13 particular NAND flash design, soup to nuts. So
14 it's describing a particular floating gate
15 device and how it is operated in its various
16 operations.

17 Erase is not an issue that has come up
18 within my declaration. I don't believe I've
19 talked about or opined about erasing at all.
20 So, other than the fact that this uses the words
21 "erase pulse," I don't have much to say about
22 it.

23 Q. Now, if you could turn to page 189 of
24 the same exhibit for me.

25 A. I'm on 189.

1 Q. And there's a section that begins with
2 6.9.3, you see that?

3 A. 6.9.3 is a section titled
4 "Double-Supply Voltage Regulator."

5 Q. And that begins with a paragraph that
6 says, "Both program and erase operations require
7 voltages higher than VDD." And then later in
8 the paragraph, the text states, "High voltages
9 are generated by a charge pump and filtered by a
10 proper voltage regulator."

11 Do you see that?

12 A. Yes, you accurately read that first
13 paragraph or characterized that first paragraph
14 of Section 6.9.3 of the Micheloni text which,
15 again, describes one particular NAND flash
16 implementation using floating gate memory cells.

17 But again, voltage regulation and
18 supply voltage generation is not something that
19 came up within my declaration, and I don't have
20 a lot to say about it in this context.

21 Q. Now, earlier today we did discuss
22 charge pumps, correct?

23 A. You asked me about charge pumps, yes.

24 Q. So is the reference to a charge pump
25 here referring to the same type of components

1 that you referred to in your testimony earlier
2 today?

3 A. Previously, you asked about charge
4 pumps in general, and I answered in the most
5 general way about what charge pumps do.

6 In this chapter of the Micheloni text,
7 he's referring to specific voltage regulator and
8 charge pump configurations. I don't know if
9 he's referring to something more narrowly than
10 my general answer previously. I'd have to study
11 this chapter more carefully to answer that.

12 Q. But he does say that high voltages are
13 generated by a charge pump, and those high
14 voltages are required for program and erase
15 operations in NAND's memory, true?

16 A. Again, you characterized that first
17 paragraph of Section 6.9.3 accurately. It is
18 referring to a particular floating gate NAND
19 flash design that is described in detail
20 throughout chapter 6.

21 Q. Do you agree that it was known at the
22 time the '822 patent was filed that a charge
23 pump is employed in NAND's memory to internally
24 generate needed voltages exceeding VDD?

25 A. I believe my testimony previously was

1 that charge pumps are used but not typically in
2 commercial products, but are not a requirement
3 of NAND flash memories, generally.

4 Q. And so typically used, but you could
5 come up with some other theoretical way to
6 supply required voltages, correct?

7 A. I'd remove the word "theoretical" from
8 that sentence.

9 Q. But you'll agree that they're
10 typically used in commercial products to supply
11 the high voltages needed for memory operation,
12 true?

13 A. Charge pumps are one of many tools in
14 the memory designer's toolkit to get the desired
15 end results. So they are a known and commonly
16 used circuit technique.

17 MR. HERMAN: I'm going to switch tacks
18 now, so it may be a good time for a brief
19 five-minute break, unless you would like to
20 keep going.

21 THE WITNESS: No, this is a good time
22 for a break.

23 MR. HERMAN: So why don't we take five
24 minutes.

25 THE WITNESS: Okay.

1 (Recess; Time Noted: 11:53 a.m.)

2 (Time Noted: 12:00 p.m.)

3 BY MR. HERMAN:

4 Q. All right. Doctor, so I'm going to
5 put what has been previously marked as Exhibit
6 1004 in the chat, and let me know when you have
7 that.

8 A. I have Patent 10,121,529 to Lee on my
9 screen in Acrobat.

10 Q. This is one of the prior art
11 references that you address in your declaration,
12 true?

13 A. Yes.

14 Q. If you could turn to column 6 of
15 Exhibit 1004 for me.

16 A. I'm looking at column 6.

17 Q. There's a paragraph in column 6 that
18 begins at line 22, and that paragraph references
19 the address decoder 120.

20 You see that?

21 A. Yes, that paragraph is referring to
22 Figure 1 and address decoder 120 there depicted.

23 Q. And that address decoder 120 is also
24 shown in Figure 1, true?

25 A. I think that's what I just said, yes.

1 Q. Now, later in that same paragraph in
2 column 6, Lee states that, "The address decoder
3 120 applies, during a program operation, program
4 voltages Vpgm, pass voltages Vpass and operating
5 voltages which are generated from the voltage
6 generation unit 150."

7 Did I get that right?

8 A. You read that accurately.

9 Q. And the same paragraph also notes that
10 "address decoder 120 is configured to operate in
11 response to control of the control logic 140,"
12 correct?

13 A. Yes. I think that sentence would have
14 been a little clearer if the word "of" was "by"
15 instead, but the idea is the same, and you
16 accurately read it.

17 Q. So this paragraph, and Figure 1 to
18 which it refers, is discussing a memory that
19 includes a voltage generation unit 150 that
20 generates voltages like Vprogram and Vpass,
21 correct?

22 A. Yes, in column 6, beginning at line
23 30, it reads -- or, 29, sorry, "The address
24 decoder 120 applies, during a program operation,
25 program voltages Vpgm, pass voltages Vpass and

1 operating voltages which are generated from the
2 voltage generator unit 150," and it goes on from
3 there.

4 Q. And this paragraph in Figure 1 are
5 also referring to a memory that includes an
6 address decoder 120 that is under control of the
7 control logic, which then, in turn, determines
8 which word lines receive those voltages
9 generated by the voltage generation unit 150,
10 correct?

11 A. Yes, that's how Lee has chosen to
12 decompose the circuitry of the memory device
13 shown in Figure 1 into particular blocks, one of
14 which he's labeled address decoder 120.

15 Q. And another of which is labeled
16 voltage generation unit 150, correct?

17 A. That's correct, but that's not the
18 only way that this circuitry can be divided into
19 blocks and named. So just so long as we're
20 clear that this is the terminology Lee has
21 chosen.

22 Q. Now, Vprogram and Vpass are two
23 different voltages that are meant to be supplied
24 to different word lines, correct?

25 MR. BALBAKY: Objection. Form.

1 THE WITNESS: It's clear from the
2 disclosure of Lee, column 6, specifically,
3 in the vicinity of line 30, that these are
4 voltages that are generated by the voltage
5 generator block and which are used in all
6 manner of locations and purposes within the
7 memory device.

8 BY MR. HERMAN:

9 Q. I was specifically referring to the
10 program and the pass voltages.

11 The program and the pass voltages are
12 two different voltages that are meant to be
13 supplied to different word lines, correct?

14 A. Is there a particular passage that
15 describes that in Lee?

16 Q. Well, I'm asking for your
17 understanding as an expert regarding NAND.

18 Do you apply the program voltages to
19 specific word lines in memory during
20 programming, or do you apply them to every
21 single word line?

22 A. Well, Lee doesn't describe that in any
23 degree that I can see. Certainly, he talks
24 about groups of word lines, but doesn't talk
25 about which voltages are applied to which.

1 Generally speaking, your statement is
2 true, but I'm not seeing a support of that idea
3 within Lee per se.

4 Q. Now, one of ordinary skill in the art
5 would understand what a program voltage is and
6 what a pass voltage is in NAND's memory, true?

7 A. Within the context specifically of
8 NAND memory, those terms are pretty
9 well-understood across the board, so I would
10 answer in the affirmative.

11 Q. Now, if you turn to column 7, there's
12 a paragraph that begins at line 8.

13 A. I'm looking at it.

14 Q. And here, Lee explains that "control
15 logic 140, in an embodiment and accordance with
16 the present invention, may apply pre-bias
17 voltages to the word lines during a program
18 operation. The control logic 140 may apply
19 different pre-bias voltages to the word lines
20 depending on the respective positions of the
21 word lines."

22 Do you see that?

23 A. You read that accurately.

24 Q. So, here, Lee is referencing another
25 set of voltages which it calls pre-bias voltages

1 that are also supplied to its word lines, true?

2 A. This sentence talks about pre-bias
3 voltages without characterizing them. So they
4 may be the same as other voltages, but they are
5 named differently.

6 Q. And there may be different pre-bias
7 voltages that are applied to different word
8 lines in Lee, correct?

9 A. Literally, it says, "The control logic
10 may apply different pre-bias voltages to word
11 lines depending on the respective positions of
12 the word lines."

13 Q. Now, will these pre-bias voltages be
14 generated by the same voltage generation unit
15 150 that's referenced in Lee?

16 A. Does it formally disclose that
17 somewhere? Because I'm not seeing that
18 particular correspondence in that portion of
19 column 7.

20 Q. Is that how you would interpret Lee,
21 that the voltage generation unit 150 will
22 generate the pre-bias voltages that are supplied
23 to the word lines?

24 A. A POSITA looking at Figure 1 and that
25 sentence in column 7 would reasonably assume

1 that a voltage generator is going to generate
2 those pre-bias voltages. It may not be the same
3 voltage generator as shown in block 150 that is
4 explicitly shown generating the program in
5 Vpass. So there may be a separate one. It's
6 unclear and not relevant specifically to the
7 principal disclosure of Lee.

8 Q. But the way that those pre-bias
9 voltages make their way to the word lines will
10 be similar to how the pass and the program
11 voltages make their way to the word lines? They
12 will be generated by a voltage generation unit,
13 they will pass through an address decoder that's
14 controlled by control logic, and they will make
15 their way to the word lines, true?

16 A. As Lee has grouped circuitry as shown
17 in Figure 1, where there is a whole lot of stuff
18 grouped together in the block named address
19 decoder -- which, to be clear, is going to
20 include more than just address decoding -- and
21 there is only one block shown driving the word
22 lines, it's clear that, however the pre-bias
23 voltages are generated, they will have to flow
24 through the block labeled address decoder in
25 Figure 1 unless there is an additional block not

1 shown that deals with word line voltages other
2 than in the program pulse phase of the program
3 operations.

4 Q. And the only component that Lee
5 discusses that generates voltages is its voltage
6 generation unit, correct?

7 A. I don't know that off the top of my
8 head.

9 Q. So, sitting here today, you don't know
10 if Lee discusses any other components for
11 generating voltages besides the voltage
12 generation unit?

13 A. Again, there may be unlabeled blocks
14 in Figure 1. I mean, Figure 1 is at a very high
15 level, and there's a great deal of circuitry
16 that's not shown.

17 It's perfectly reasonable that there
18 is a second and distinct voltage generator for
19 the voltages other than Vprogram and Vpass. Lee
20 does not address that nor hint one way or the
21 other that I'm aware of.

22 Again, if there's some passage you
23 want me to view from Lee to clarify that, by all
24 means.

25 Q. So I think what you're saying is that

1 Figure 1 includes one box that's labeled voltage
2 generation unit 150 that's responsible for
3 generating voltages, but there could be many
4 such voltage generation units, is that what
5 you're saying?

6 A. And certainly, typically, if you look
7 inside a commercial NAND flash memory, there are
8 a plurality of voltage generators which may or
9 may not, for the purposes of Lee, be grouped
10 together in one box or just remain separate and
11 undepicted.

12 Again, it's not relevant to Lee's
13 disclosure.

14 Q. Now, if we turn to column 8, at about
15 line 15, Lee explains that the pre-bias voltages
16 are voltages to be applied to the respective
17 word lines LW0 to LW31 in a pre-charging step
18 during a programming operation of the program
19 cell.

20 You see that?

21 A. I'm sorry. What line are you reading
22 from?

23 Q. Column 8, line 15. The sentence that
24 kind of begins about a third of the way through
25 line 15.

1 A. Yeah, I think you misread it. If you
2 will please read it again.

3 Q. Sure.

4 That line reads, "The pre-bias
5 voltages are voltages to be applied to the
6 respective word lines LW0 to LW31 in a
7 pre-charging step during a program operation for
8 the program cell."

9 Did I get it right that time?

10 A. No, you made the same error.

11 Q. What did I say?

12 A. It's "WL," not "LW."

13 Q. Ah, got it.

14 A. A little dyslexia going on?

15 Q. Yes.

16 Other than screwing up how the word
17 lines are labeled, did I get the rest of the
18 sentence right?

19 A. All the other words in that sentence
20 were read correctly.

21 Q. So the sentence refers to a
22 pre-charging step, correct?

23 A. Yes, that sentence includes the phrase
24 "a pre-charging step during a program operation
25 for the program cell."

1 Q. And the pre-charging step is when the
2 pre-bias voltages are applied to the word lines,
3 true?

4 A. So column 7, line 63 has a paragraph
5 beginning, "The operation of applying different
6 pre-bias voltages to word lines at a
7 pre-charging step during a program operation,"
8 etc. So that would confirm your statement.

9 Q. Now, if you could take a look at
10 Figure 7 of Lee, which is on page 11 of the PDF
11 that you have.

12 A. I'm sorry, Figure 7?

13 Q. Yes.

14 A. Yes, I'm looking at Figure 7.

15 Q. So Figure 7 provides an overview of
16 Lee's program operation, correct?

17 A. Figure 7 is characterized in column 4
18 as, "Figure 7 is a flowchart illustrating the
19 step of performing a program operation, based on
20 a result of grouping the word lines of Figure
21 6."

22 Q. So in Figure 7, that program operation
23 begins with a step labeled "S201"; is that
24 right?

25 A. Yes, the first step shown in Figure 7

1 is step S201, labeled, "determine group
2 including word line coupled to program cell."

3 Q. And there are also steps labeled as
4 step 203, step 205, and step 207, correct?

5 A. That's correct.

6 Q. Now, the pre-bias voltages will be
7 applied to the word lines only during step 205,
8 correct?

9 A. In column 11 of Lee, at line 34, it
10 talks about step 205, which is, and I quote, "At
11 step 205 of precharging channel regions of
12 memory cells based on the determined pre-bias
13 voltages, the determined pre-bias voltages are
14 applied to the respective word lines," and it
15 goes on from there.

16 So it says both in this portion of
17 column 11 and implicitly in Figure 7 that,
18 during step 205, the pre-bias voltages are
19 applied. It does not say they are applied
20 exclusively during step S205.

21 Q. But step S205 is the step in which
22 those pre-bias voltages are meant to be applied,
23 correct?

24 A. Well, as I just said, Lee is clear
25 that during step 205 they are applied. It's

1 just your presumption that they are exclusively
2 applied during step 205 is not supported either
3 by Figure 7 or by the text in column 11.

4 Q. Now, step 207 is the step where
5 program voltages are applied, correct?

6 A. So, similarly, column 11, line 38 or
7 so, it says, "At step 207 of performing the
8 program loop, a program voltage is applied to
9 the selected word line, and pass voltages are
10 applied to unselected word lines."

11 So, again, it's talking about that,
12 during that step, there is a program voltage
13 applied.

14 Q. Now, if you look at column 9 of Lee,
15 starting at line 7.

16 A. I'm looking at column 9.

17 Q. At line 7, Lee states, "After the
18 pre-bias voltage is applied to the respective
19 word lines and the precharge operation is
20 completed, a program voltage may be applied to
21 the selected word line WL0, and a pass voltage
22 may be applied to unselected word lines WL0
23 through WL9 and WL11 to WL31."

24 Do you see that?

25 A. Yes, you read that accurately.

1 Q. And I actually got the "WL" in the
2 right order that time, correct?

3 A. I did note that, yes.

4 Q. So in that passage that I read, Lee
5 uses the word "completed," true?

6 A. The word "completed" does exist there
7 on line 8.

8 Q. And the word "completed" refers to the
9 pre-charge operation, true?

10 A. It's referring to the completion of a
11 pre-charge operation. It does not clarify what
12 Lee means by the "completion of a pre-charge
13 operation" in this paragraph.

14 Q. And what Lee says here is that program
15 voltages may be applied to the word lines after
16 not only the pre-bias voltages is applied, but
17 also the pre-charge operation is completed,
18 true?

19 MR. BALBAKY: Objection to form.

20 THE WITNESS: So after the pre-charge
21 operation is complete -- in other words,
22 that the pre-charge condition that Lee wants
23 to set up has been set up and has run its
24 course -- then the algorithm moves on to the
25 next stage.

1 So you don't want to move on to the
2 next stage until you have completed the
3 pre-charge operation.

4 BY MR. HERMAN:

5 Q. So if pre-charging is still ongoing
6 for some reason, the algorithm will not yet move
7 on to the next stage and apply the program
8 voltages, true?

9 A. That's an unusual way of phrasing it.
10 It assumes there is agency there that does not
11 exist, but as the duration of the pre-charge
12 operation, generally speaking, is fixed a priori
13 based on the simulations of the designer and not
14 dynamically determined.

15 Q. But the implication of that statement
16 is you wait until pre-charging is done before
17 you apply the programming voltages, true?

18 A. The implication of this statement is
19 that you wait long enough for the pre-charge
20 operation to have run its course and achieved
21 the desired result before you move on to the
22 programming step.

23 Q. You don't move on to the programming
24 step while pre-charging is still occurring,
25 correct?

1 A. This sentence is unclear about that.
2 There are certainly many opportunities for
3 overlapping different steps of different
4 sub-operations within the general context of a
5 memory's device operation, and this particular
6 paragraph is only talking about that, after the
7 pre-charge operation is completed, however Lee
8 is defining that, a program voltage may be
9 applied. But he's not clear about what
10 "completion of the program operation" means
11 specifically other than the general intent that
12 it had achieved its desired result.

13 Q. So you wait until after the pre-charge
14 operation has achieved its desired result, and
15 then you apply the program voltages, true?

16 A. That's what a POSITA would understand
17 from this paragraph in column 9 of Lee.

18 Q. Now, if you could look back at your
19 declaration. That's Exhibit 2011.

20 A. I am looking at it.

21 Q. And if you could turn to paragraph 84
22 for me.

23 A. I am looking at paragraph 84 on page
24 61.

25 Q. There's a sentence that reads, "In

1 fact, the criteria set out on the Petition
2 (i.e., that the signal occurs in the distinct
3 time step, and that it has a value that differs
4 from some later voltages), could be satisfied by
5 any number of signals."

6 You see that?

7 A. Give me a moment to review this
8 paragraph. It's a long one.

9 Q. Are you ready?

10 A. No, I'm still reading paragraph 84.

11 Okay, would you repeat the question,
12 please?

13 Q. I was just directing your attention to
14 a particular sentence, which it seems like you
15 found, correct?

16 A. Which sentence were you specifically
17 directing me to?

18 Q. The one that begins, "In fact, the
19 criteria set out in the Petition," that
20 sentence.

21 A. Okay. I found that sentence, yes.

22 Q. There's a parenthetical in that
23 sentence that reads, "e.g., a flat signal
24 followed by a ramping voltage, a nonlinear
25 function shaped like a charging capacitor, a

1 monotonically-increasing staircase function,
2 etc."

3 Do you see that?

4 A. Yes, I see that parenthetical.

5 Q. Now, you do not cite here, or anywhere
6 else in your declaration, examples of NAND's
7 devices that apply signals to word lines that
8 are flat signals followed by a ramping voltage,
9 a nonlinear function shaped like a charging
10 capacitor, or a monotonically-increasing
11 staircase function, correct?

12 A. That's correct, I don't have provided
13 any specific examples. It's not necessary for
14 me to do so in order to rebut the petitioner's
15 argument vis-à-vis Lee.

16 Q. So no examples in your declaration,
17 true?

18 A. None called for. None necessary.
19 None provided.

20 Q. Now, further down in the paragraph,
21 you note that, "It would be advantageous to
22 apply biased voltages as flat signals that
23 remain constant throughout the entire pre-charge
24 period."

25 Do you see that?

1 A. I see that sentence, yes.

2 Q. Now, when you apply a voltage to a
3 word line, the word line's potential does not
4 immediately change to match that applied
5 voltage, true?

6 MR. BALBAKY: Objection. Relevance.

7 THE WITNESS: For the purposes of your
8 question only, you assume that the word line
9 is a single node made of metal where the
10 potential is the same across the entire
11 thing. The voltage applied to the word line
12 is the voltage at the word line. That's
13 kind of, by definition, basic EE-101.

14 In real life, there are a variety of
15 phenomena that cause localized or temporally
16 short-term deviations from that simple
17 concept, and I think that's what you're
18 getting at, but your question doesn't
19 provide enough context to give a more
20 detailed answer.

21 BY MR. HERMAN:

22 Q. So, temporally, does it take some
23 small amount of time for the word line potential
24 to ramp up to the supplied voltage?

25 A. What do you mean by "supplied voltage"

1 in that question?

2 Q. So let's say I use a charge pump to
3 apply a voltage to a word line.

4 Will it take some finite amount of
5 time for the word line's voltage to reach
6 whatever voltage is being applied by the charge
7 pump?

8 A. Well, if you treat the charge pump as
9 an idealized voltage generator, voltage source,
10 with a non-0 output impedance, there will be an
11 RC time constant between that output impedance
12 and the capacitance of the word line that causes
13 the voltage on the word line to not change
14 instantaneously and that to be a continuous
15 function over time.

16 Q. So there's some period of ramp-up; is
17 that fair to say?

18 A. Generally speaking, that's true of all
19 circuits, that we often idealized what the
20 voltage on nodes are. In practice, there are
21 various RC time constants and other effects that
22 will deviate from that idealized representation.

23 Q. And the same will occur if I attempt
24 to change the word lines's potential from one
25 value to another; there will be some period of

1 ramp as you transition from the first potential
2 to the second potential, true?

3 A. In general, the RC time constants
4 apply for any change of Delta-v for such a
5 circuit where there are resistances and
6 capacitances. So it does not just apply to a
7 change from 0 to some other voltage, but from
8 one voltage to another.

9 Q. Now, if you could turn to paragraph
10 115 of your declaration for me.

11 A. Another long one.

12 Yes, I am looking at paragraph 115.

13 Q. In this paragraph, there's a sentence
14 that notes Lee, and then there's an apostrophe
15 "S" that appears to be a typo.

16 I think what you meant to say is that,
17 "Lee states that its teachings address problems
18 arising from pre-charging operations performed
19 via the common source line (or, more
20 specifically, pre-charging operations that apply
21 pre-charging voltages via the source-line while
22 current runs through the memory string),"

23 correct?

24 A. That sentence is there and accurately
25 read.

1 Q. All right. So two questions here.
2 The first is: As you interpret Lee, current is
3 flowing through its channel during programming,
4 correct?

5 MR. BALBAKY: Objection. Form.

6 THE WITNESS: I'm going to take a
7 moment to read all of 115.

8 Okay. Would you please repeat the
9 question?

10 BY MR. HERMAN:

11 Q. So, as you interpret Lee, a current is
12 running through the channel, correct?

13 A. Yeah, I think that in Lee, column 8,
14 it talks about, during the pre-biased period,
15 that there are resistive components between the
16 source select transistor and the drain select
17 transistor that are to be offset, and that
18 implies that there is current flowing, yes.

19 Q. And Lee applies its pre-bias voltages
20 as part of its program operation, true?

21 A. And here, in particular, in column 7,
22 where it talks about, line 8, "applying pre-bias
23 voltages to word lines during a program
24 operation," a POSITA would understand "program
25 operation" in this context to mean the entirety

1 of the programming from the initial setup
2 through the plurality of pulses, if they exist,
3 and to any -- and the cleanup process that may
4 or may not exist, and I don't think is disclosed
5 within Lee, regardless.

6 Q. So, turning back to paragraph 115, you
7 also note that, "Lee states that its teachings
8 address problems arising from pre-charging
9 operations performed via the common source
10 line"; is that right?

11 A. Yes, that is what I say there in
12 paragraph 115.

13 Q. So, in your view, Lee always applies a
14 pre-charge voltage via the common source line,
15 and never via its bit line, correct?

16 A. Is there a disclosure of a bit line
17 pre-charge in Lee that you would like to point
18 me to?

19 Q. So I'm asking if it's your opinion
20 that, in all cases, Lee always applies a
21 pre-charge voltage via the source line. That
22 seems to be what you're saying in paragraph 115.

23 If that's not what you're saying,
24 please let me know.

25 A. It's certainly not one of the opinions

1 that I have listed in my summary of opinions. I
2 don't believe I have opined in my declaration
3 that it is the -- the source line pre-charging
4 is the only thing that's disclosed within Lee.

5 It is certainly the embodiment that's
6 focused on in the petition and Dr. Liu's
7 declaration, and so that is why I focused on
8 that in particular.

9 If there are other disclosures within
10 Lee that you want to point me to, I'd be happy
11 to address them.

12 Q. So it seems like you just said that,
13 in your view, Lee may also be open to
14 pre-charging via the bit line.

15 Is that what you just tried to express
16 in that answer?

17 A. What I tried to express in my last
18 answer is that I have not memorized Lee and all
19 of its embodiments.

20 It is certainly the case that in at
21 least some embodiments it talks about source
22 line pre-charging, and that is what has been
23 focused on in the petition and Dr. Liu's
24 declaration. So that is what I felt necessary
25 to rebut in light of the proposed combination

1 with Zhao.

2 Q. So paragraph 115, you state, "Lee
3 states that its teachings address problems
4 arising from pre-charging operations performed
5 via the source line."

6 So if you did not determine whether or
7 not Lee also allowed for charging via the bit
8 line, what is your basis for making that
9 statement?

10 A. My basis for that statement is that
11 it's true, Lee does state that he's treating --
12 addressing problems associated with the
13 resistance component of current flowing through
14 the strings, and it does talk about performing
15 pre-charging from the source line side.

16 This sentence does not fully
17 characterize everything that is in Lee. It's
18 just referring to those particular teachings of
19 Lee.

20 Q. All right. So one of ordinary skill
21 in the art could make reasonable inferences
22 about Lee's teachings beyond what you are
23 referring to here in paragraph 115, is that what
24 you just said?

25 A. I think that's mischaracterizing my

1 testimony. What I'm saying is that I'm
2 rebutting the arguments in the petition and Dr.
3 Liu's declaration that relate to Lee's
4 statements about common source line precharging
5 and the compensating for the resistive
6 components in the strings.

7 Q. Well, you also seem to be saying that
8 Lee may be interpreted as addressing other
9 problems besides those arising from precharging
10 operations performed via the common source line.
11 You seem to be saying that as well.

12 Are you not saying that?

13 MR. BALBAKY: Objection to form.

14 THE WITNESS: My comments about Lee
15 are in reference to particular statements of
16 Lee and particular embodiments.

17 I'm not saying anything about
18 embodiments of Lee that I have not
19 specifically cited to or that the petition
20 and Dr. Liu have not cited to.

21 BY MR. HERMAN:

22 Q. So your statements are limited to just
23 particular embodiments as opposed to addressing
24 Lee as a whole, that's what you're saying?

25 A. My statements in my declaration are

1 directed to critiquing and rebutting the
2 arguments in the petition and Dr. Liu's
3 declarations vis-à-vis what they said there
4 about Lee.

5 If there's additional things in Lee
6 that have relevance but are not referred to in
7 the petition and declaration, I have not
8 commented on those specifically.

9 Q. Now, if you turn to paragraph 62 of
10 your declaration.

11 A. I'm at 62.

12 Q. You got there faster than me. Just
13 give me a second.

14 And if you look to the portion of
15 paragraph 62 that is on page 40. It's a long
16 paragraph, so it goes on to the next page.

17 There's a sentence that begins
18 "specifically" at the top of the page. Do you
19 see that?

20 A. I see the word "specifically," yes.

21 Q. And in the middle of that sentence,
22 there's a statement that says, "current running
23 from the drain select transistor to the source
24 select transistor along the length of the memory
25 string (e.g., as a result, all of the

1 transistors within the memory string have been
2 turned on)."

3 See that statement?

4 A. Yes.

5 Q. Now, for current to flow through a
6 NAND's channel, all of the transistors along the
7 channel need to be in an "on" state, correct?

8 A. Yes, the presumption is that if any of
9 the transistors are off, its resistance is
10 essentially infinite and that there is no
11 significant current flowing through it.

12 By Kirchhoff's law, if there is no
13 current flowing through it, there is no current
14 flowing in a steady-state situation with any of
15 the memory cells in that string.

16 Q. So the select transistors at the ends
17 of the channel, so the source select transistor
18 or the drain select transistor, those would need
19 to be open for current to flow, or on for
20 current to flow, correct?

21 A. For current to flow, you need a
22 non-infinite resistance between a voltage
23 differential, and so if the source select or
24 drain select transistors are off (i.e., they
25 have a near infinite resistance), then they

1 would cut off current flow in the string, just
2 as any of the memory cells being turned off
3 would cut off current flow in the string.

4 Q. So if the drain select transistor is
5 on, but the source select transistor is off,
6 there will be no current flow in the string,
7 correct?

8 A. Not in the steady state, that's
9 correct.

10 Q. So, likewise, if the source select
11 transistor is on and the drain select transistor
12 is off, there would also be no current flow,
13 correct.

14 A. Again, in the steady state, there will
15 be no current flow if any of the transistors in
16 the string, including the select transistors,
17 are off.

18 MR. HERMAN: Now is probably a good
19 time for another short, five-minute break.

20 THE WITNESS: By all means.

21 MR. HERMAN: Is that okay?

22 THE WITNESS: Yes, by all means.

23 MR. HERMAN: Five minutes.

24 MR. BALBAKY: Works fine for me.

25 (Recess; Time Noted: 12:53 p.m.)

1 (Time Noted: 1:00 p.m.)

2 BY MR. HERMAN:

3 Q. So I'm going to put another exhibit in
4 the chat. This one has been previously marked
5 as Exhibit 1005.

6 Let me know when you have that.

7 A. I am looking at Patent 10,643,718 to
8 Zhao.

9 Q. And this is another of the prior art
10 references that you reviewed and discuss in your
11 declaration, correct?

12 A. Correct.

13 Q. If you can turn to column 22 for me.

14 A. I'm looking at 22.

15 Q. At line 18, there's the beginning of a
16 discussion of Figure 13, correct?

17 A. Yes.

18 Q. And --

19 Sorry. Go ahead.

20 A. I was just going to clarify that
21 Figure 13 is referred to in the paragraph
22 beginning on line 18 of column 22 of Zhao.

23 Q. And Zhao explains that, "Figure 13 is
24 a signal diagram depicting the behavior of
25 various signals during pre-charge, boosting, and

1 programming," right?

2 A. That's what it says there in lines 18
3 to 20.

4 Q. And if we look down to line 34, that,
5 for Zhao, references a time t_0 , right?

6 A. Yes, line 34 of column 22 at time t_0
7 of Figure 13.

8 Q. And Zhao states that, "At time t_0 of
9 Figure 13, all the depicted signals are at 0
10 volts," right?

11 A. That's what it says there, yes.

12 Q. So, according to Zhao, all of its
13 various signal lines start at 0 volts at time 0,
14 correct?

15 MR. BALBAKY: Objection. Form.

16 THE WITNESS: And later on in that
17 paragraph, there is an equivalent setup
18 between V_{ss} and 0 volts in the context of
19 Zhao -- in this paragraph of Zhao, at least.

20 BY MR. HERMAN:

21 Q. So the next paragraph, starting at
22 22:39, discusses the time period t_1 to t_3 ,
23 correct?

24 A. Yes, that next paragraph does refer to
25 time period t_1 to t_3 shown in Figure 13.

1 Q. And Zhao states that this time period
2 corresponds to pre-charging, right?

3 A. That's how Zhao characterizes that
4 time period, as pre-charging, yes.

5 Q. And during this pre-charging time
6 period, Zhao explains that certain of its word
7 lines are raised to different voltages like
8 Vprecharge and Vbypass, correct?

9 A. Let me read that paragraph.
10 Yes, so generally the paragraph
11 beginning on column 22, line 39, and then
12 continuing all the way into column 23 does
13 describe various voltages applied to different
14 signal lines, including some word lines, in the
15 period t1 through t3.

16 Q. Now, if we turn on to the next column,
17 column 23, there's a sentence that begins at
18 line 8 that says, "At time t3." See that?

19 A. I see that.

20 Q. And the sentence goes on to reference
21 a collection of different signal lines,
22 including SGD(sel), and then a number of
23 different word lines, do you see that?

24 A. Yes.

25 Q. And Zhao then goes on to say all of

1 those are lowered to ground/Vss; is that right?

2 A. Those are the words of Zhao, yes.

3 Q. Then he says, "At this point in time
4 the pre-charge process has completed and the
5 drain side of the channel of the unselected NAND
6 strings should be pre-charging to a positive
7 voltage," right?

8 A. That's what he says there in column
9 23, yes.

10 Q. So, to summarize, starting in column
11 22 at line 22 and proceeding on to that sentence
12 in column 23 I just read, Zhao describes a
13 process in which all of its signal lines start
14 at 0 volts at time 0, right?

15 A. Yes; and that's what's shown in Figure
16 3 and described in the text in columns 22 and
17 23.

18 Q. Then from time t1 to time t3, certain
19 of those lines receive voltages, correct?

20 A. Well, they all have voltages on them.
21 Nodes do have voltages units that are 0. Some
22 of the word lines and other control lines have a
23 non-0 voltage applied to them.

24 I think that's what you're trying to
25 get at, but...

1 Q. Yes, and that non-0 voltage is applied
2 to some of the word lines during period t1 to
3 t3, correct?

4 A. That is generally what's depicted in
5 column Figure 13.

6 Q. And then at t3, those lines that
7 received those non-0 voltages are returned to
8 ground/Vss, correct?

9 MR. BALBAKY: Objection to form.

10 THE WITNESS: What's illustrated in
11 Figure 13 is that, beginning at time t3,
12 those itemized word lines and select lines
13 are released, and they begin their
14 transition back down to Vss.

15 So, technically, they're not at Vss
16 until a little bit past t3, but from Zhao's
17 perspective, the pre-charged period ends at
18 t3, even if it does continue slightly beyond
19 that.

20 BY MR. HERMAN:

21 Q. So how are power signal lines
22 typically lowered to ground in NAND memory?

23 A. Well, are you referring specifically
24 to nodes, generally, or word lines,
25 specifically?

1 Q. Well, let's start with word lines.

2 A. Okay. So would you repeat the
3 question, please? I missed it.

4 Q. So how would a word line typically be
5 lowered to ground in NAND's memory?

6 A. So the word lines have -- are driven
7 by word line drivers, which take the output of
8 an address decoder and outputs from the voltage
9 generator and voltage selector, and to drive it
10 to ground, you would select a Vss, or something
11 equivalent or comparable, and cause that voltage
12 to be driven on to the word lines that you're
13 trying to drive to 0.

14 Q. So let me see if I understand.

15 So the word lines that receive a non-0
16 voltage, you would select, using the circuitry
17 you described, that non-0 voltage during t1
18 through t3, correct?

19 A. Yes, that's accurate.

20 Q. And then, at t3, you would select
21 ground or Vss for those same word lines,
22 correct?

23 A. That's one way it can be done. That's
24 the typical way it can be done. It's not the
25 only way it can be done.

1 Q. All right. I'm going to put another
2 exhibit in the chat, and that's Exhibit 1010.

3 Let me know when you have that.

4 A. I will.

5 I'm looking at Exhibit 1010, Patent
6 10,726,920 to Yang.

7 Q. And Yang is another of the prior art
8 references that you reviewed and you discuss in
9 your declaration --

10 A. Yes.

11 Q. -- correct?

12 A. I'm sorry. I spoke too soon.

13 Yes.

14 Q. And if you could turn to paragraph 141
15 of your declaration for me, and that's on page
16 107, again, referring to the page numbers in the
17 lower right corner.

18 A. Okay. You want me to look at my
19 declaration, 141. Yes, I'm there.

20 Q. That paragraph 141 spans on to page
21 108, or continues on to page 108; is that right?

22 A. Actually, it continues on to 109, too.

23 Q. And on page 108, you have an annotated
24 figure, correct?

25 A. Correct.

1 Q. And that annotated figure was
2 generated using Yang's Figure 8B, true?

3 A. Yes, reading from paragraph 141, I say
4 that, "In fact, they have identical values, as
5 can be seen clearly by placing copies of the
6 Vbypass and Vpre_dmy waveforms side by side, as
7 shown in Figure 8 below."

8 Q. So there are red lines on that figure
9 that's on page 108; is that right?

10 A. Yes, those are my annotations added to
11 the copied versions of those two signals.

12 Q. All right. So the red lines are not
13 in Yang, correct?

14 A. Those are my annotations, correct.

15 Q. And there are essentially two versions
16 of Figure 8B, both of which are cropped in your
17 demonstrative; is that right?

18 A. That's correct; taken two portions of
19 8B, put them side by side, and added red lines
20 to show how they relate to each other.

21 Q. And what you are doing is you are
22 using Figure 8B and the dimensions of the
23 signals depicted in that figure to draw
24 conclusions relating to signals Vpre_dmy and
25 Vbypass, correct?

1 A. This analysis of showing that they are
2 drawn identically is part of the support for the
3 overall conclusion of this section. They are
4 not the sole support for that conclusion.

5 Q. But you don't actually cite to
6 anything in Yang besides Figure 8B anywhere in
7 paragraph 141, true?

8 A. Figure 8B is the only explicit
9 citation to Yang in paragraph 141, but I do cite
10 to at least the petition, which indirectly
11 refers to the disclosure of Yang as well. So
12 directly and indirectly.

13 Q. And you don't cite any portion of Yang
14 in this paragraph that says that Yang's figures
15 are drawn to scale, correct?

16 A. No, I don't cite to Yang saying that
17 the figures are drawn to scale.

18 MR. HERMAN: I don't have any further
19 questions.

20 MR. BALBAKY: I don't have anything
21 further either.

22 MR. HERMAN: I think, with that, we
23 are done.

24 Thank you, Doctor. We are done today.

25 THE WITNESS: Okay.

1 MR. HERMAN: Thank you for your
2 attention.

3 MR. BALBAKY: Thank you, Doctor.

4 (Whereupon, the deposition concluded
5 at 1:16 p.m.)

6 oOo

7

8

STEVEN PRZYBYLSKI, PH.D.

9

10 Subscribed and sworn to
11 before me this day
12 of 2025.

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CERTIFICATE

I, Kathy S. Klepfer, a Registered
Merit Reporter and Certified Shorthand
Reporter within and for the State of
California, CSR No. 14667, do hereby
certify:

That STEVEN PRZYBYLSKI, the witness
whose deposition is herein before set forth,
was duly sworn by me and that such
deposition is a true record of the testimony
given by such witness.

I further certify that I am not
related to any of the parties to this action
by blood or marriage and that I am in no way
interested in the outcome of this matter.

In witness whereof, I have hereunto
set my hand this 21st day of March 2025.

Kathy Klepfer

KATHY S. KLEPFER, RPR, RMR, CRR, CLR

1 NAME OF CASE: YMTC v. Micron

2 DATE OF DEPOSITION: March 21, 2025

3 NAME OF WITNESS: STEVEN PRZYBYLSKI, PH.D.

4 Reason Codes:

- 5 1. To clarify the record.
6 2. To conform to the facts.
7 3. To correct transcription errors.

7 Page _____ Line _____ Reason _____
8 From _____ to _____

8 Page _____ Line _____ Reason _____
9 From _____ to _____

10 Page _____ Line _____ Reason _____
11 From _____ to _____

11 Page _____ Line _____ Reason _____
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22 Page _____ Line _____ Reason _____
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24 _____
25 STEVEN PRZYBYLSKI, PH.D.

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