

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00795

Patent 11,501,822

PATENT OWNER'S SUR-REPLY

TABLE OF CONTENTS

I. INTRODUCTION	1
II. CLAIM CONSTRUCTION	1
A. “Word Line Pre-Pulse Signal”	1
B. “Disposed in an Order of Distance from the Selected Word Line” / “Disposed Adjacent to the Selected Word Line”	1
III. GROUND 1: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT LEE DISCLOSES OR RENDER OBVIOUS THE CHALLENGED CLAIMS	4
A. Independent Claims: Lee Still Fails to Disclose or Render Obvious a “[First/ Second/ Third] Word Line Pre-Pulse Signal” Applied “During a Pre-Charge Period”	4
B. Claims 2 and 12: Lee Still Fails to Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line”	11
C. Claims 3 and 13: Petitioner’s New Arguments Still Fail to Show that Lee Discloses or Render Obvious the “First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line”	13
IV. GROUND 2: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT ZHAO DISCLOSES OR RENDER OBVIOUS APPLYING A “FIRST WORD LINE PRE-PULSE SIGNAL ... DURING A PRE- CHARGE PERIOD”	14
V. GROUND 3: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW A POSITA WOULD HAVE BEEN MOTIVATED TO COMBINE ZHAO AND LEE AS PROPOSED IN THE PETITION	17
VI. GROUND 4: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT YANG DISCLOSES OR RENDER OBVIOUS THE CHALLENGED CLAIMS	23
A. Independent Claims: Yang Still Fails to Disclose or Render Obvious Word Line Pre-Pulse Signals with Incrementally Increasing Voltage Levels	23
B. Claims 2-3 and 12-13: Petitioner Still Fails to Show That Yang Discloses or Renders Obvious Dependent Claims 2-3 and 12-13.	27
VII. CONCLUSION	27

TABLE OF AUTHORITIES

Cases	Page(s)
<i>Ariosa Diagnostics v. Verinata Health Inc.</i> , 805 F.3d 1359 (Fed. Cir. 2015).	6
<i>Henny Penny Corp. v. Frymaster LLC</i> , 938 F.3d 1324 (Fed. Cir. 2019).	1
<i>Hewlett-Packard Co. v. Bausch & Lomb Inc.</i> , 909 F.2d 1464 (Fed. Cir. 1990).	3
<i>INVT SPE LLC v. Int'l Trade Comm'n</i> , 46 F.4th 1361 (Fed. Cir. 2022).	3
<i>Omega Eng'g, Inc. v. Raytek Corp.</i> , 334 F.3d 1314 (Fed. Cir. 2003).	8
<i>ParkerVision, Inc. v. Qualcomm Inc.</i> , 903 F.3d 1354, 1361-62 (Fed. Cir. 2018)	3
<i>Wasica Finance GmbH v. Continental Auto Sys.</i> , 853 F.3d 1272 (Fed. Cir. 2017).	10

LIST OF EXHIBITS

Exhibit ("Ex.")	Description
2001	July 17, 2024, Declaration of Dr. Steven Przybylski ("PrzybylskiI")
2002	U.S. Pat. No. 11,081,164 ("the '164 patent")
2003	Reserved
2004	U.S. Pat. No. 10,700,157 ("Chen")
2005	U.S. Pub. 2011/0194351 ("Kim")
2006-09	Reserved
2010	July 17, 2024, Declaration of Jonathan Bradford
2011	January 3, 2025, Declaration of Dr. Steven Przybylski ("PrzyblyskiII")
2012	Pulse, Wiley Electrical and Electronics Engineering Dictionary (2004)
2013	Pulse, IEEE Standard Dictionary (1996)
2014	Pulse, Webster's II New College Dictionary (2001)
2015	Micron's Preliminary Claim Constructions and Extrinsic Evidence Pursuant to Patent Local Rule 4-2, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , N.D. Cal. 3:23-cv-05792-RFL (Aug. 5, 2024) ("Micron's Preliminary Claim Constructions")
2016	Dispose, Merriam-Webster's Dictionary and Thesaurus (2014)
2017	Dispose, Merriam-Webster's Collegiate Dictionary (2012)
2018	Dispose, American Heritage Dictionary of the English Language (2011)
2019	Dispose, New Oxford American Dictionary (2010)
2020	Series of Images, Stamped as Ex. 2020 in the December 17, 2024, Deposition of Dr. David Kuan-Yu Liu

2021	Transcript of the December 17, 2024, Deposition of Dr. David Kuan-Yu Liu (“Liu Tr.”)
2022	Hambley, “Electrical Engineering Principles and Applications, Fourth Edition” (2008) (“Hambley”)
2023-2029	Reserved
2030	January 3, 2025, Declaration of Jonathan Bradford

LIST OF ABBREVIATIONS

Abbreviation	Term
'822	U.S. Pat. No. 11,501,822 (Ex. 1001)
Aritome	Aritome, “NAND Flash Memory Technologies” (2016) (Ex. 1006)
Brown	Brown et al., “Nonvolatile Semiconductor Memory Technology” (1998) (Ex. 1007)
Cappalleti	Cappelletti, et al., “Flash Memories” (1999) (Ex. 1008)
Challenged Claims	'822, Claims 1-9 and 11-19
Chen	U.S. Pat. No. 10,770,157 (Ex. 2004)
Hambley	Hambley, “Electrical Engineering Principles and Applications, Fourth Edition” (2008) (Ex. 2022)
Kim	U.S. Pub. No. 2011/0194351 (Ex. 2005)
Liu	Declaration of Dr. David Kuan-Yu Liu (Ex. 1003)
LiuII	Reply Declaration of Dr. David Kuan-Yu Liu (Ex. 1021)
Lee	U.S. Pat. No. 10,121,529 (Ex. 1004)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,501,822 (IPR2024-00795, Paper 1)
Parallel District Court Litigation	<i>Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner	Yangtze Memory Technologies Co. Ltd.

Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
POR	Patent Owner's Response
Przybylski	July 17, 2024, Declaration of Dr. Steven Przybylski (Ex. 2001)
PrzybylskiII	January 3, 2025, Declaration of Dr. Steven Przybylski (Ex. 2011)
Reply	Petitioner's Reply
Yang	U.S. Pat. No. 10,726,920 (Ex. 1010)
Zhao	U.S. Pat. No. 10,643,718 (Ex. 1005)

I. INTRODUCTION

Unable to dispute the Petition's numerous failings, Petitioner's Reply introduces new arguments and distorts the record. The Board should disregard the Reply's new arguments as Petitioner needed to make its case in the Petition. 37 C.F.R. § 42.23(b); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330-31 (Fed. Cir. 2019) (rejecting attempts to broaden the petition's ground in its reply). Nevertheless, Petitioner's new arguments fail to address the deficiencies in the Petition and similarly fail to meet Petitioner's burden of proving unpatentability. The Challenged Claims should be upheld as patentable.

II. CLAIM CONSTRUCTION

A. "Word Line Pre-Pulse Signal"

The parties agree that the term "word line pre-pulse signal" is a form of pulse that will, at minimum, "increase in value and then decrease in value (or vice versa)." POR, 13-14; Reply, 3. That definition is supported by both intrinsic and extrinsic evidence. POR, 13-18; PrzybylskiII, ¶¶47-54. It is not necessary for the Board to construe the term further.

B. "Disposed in an Order of Distance from the Selected Word Line" / "Disposed Adjacent to the Selected Word Line"

As explained in the POR, the plain and ordinary meaning of the term "disposed in an order of distance from the selected word line" as recited by claims 2 and 12 requires the word line groups be disposed in order based on the location of

the selected word line. Similarly, the term “the first group of the plurality of word lines are disposed adjacent to the selected word line” as used in claims 3 and 13 requires that group to be disposed adjacent to the location of the selected word line. That interpretation is confirmed by the ’822 specification, and the well understood meaning of the term “disposed.” POR, 18-20; PrzybylskiII, ¶¶56-59.

The Reply disagrees, but fails to propose alternative constructions or provide any evidence of how a POSITA would have understood the claims differently. Instead, the Reply attempts to read out the claim limitations.

First, Petitioner suggests that the claims do not require “groups be formed at any particular time” and are instead satisfied when “word lines are divided into groups and different pre-charge voltages are applied to those groups” (Reply 10-11), but a POSITA would have understood claims 2-3 and 12-13 to mean what they say: groups are “disposed in an order of distance from the selected word line” (claims 2, 12), or a first group “disposed adjacent to the selected word line” (claims 3, 13). POR, 18-20; PrzybylskiII, ¶¶55-59. Determining groups based on the location of a selected word line is well supported in the intrinsic record. POR, 18-20. As the Reply acknowledges, the ’822 states that once a wordline is selected, “word lines disposed between the selected word line and a top select gate TSG can be divided into multiple groups.” Reply, 11 (citing ’802, 4:66-5:1).

Second, Petitioner tries to rewrite apparatus claims 2-3 by misapplying *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464 (Fed. Cir. 1990). Petitioner argues that apparatus claims cover “what a device is, not what a device does,” and thus “[a]ll that matters is that there be ‘first,’ ‘second,’ and ‘third’ groups of word lines to which different pre-charge voltages ... can be applied by the claimed ‘control circuitry.’” Reply, 10-12. But *Hewlett-Packard* and its progeny relate to whether “capability, as opposed to actual operation,” satisfy an apparatus claim. *ParkerVision, Inc. v. Qualcomm Inc.*, 903 F.3d 1354, 1361-62 (Fed. Cir. 2018). That distinction is not an invitation to disregard claim language. Indeed, “what the device **does** (and how it does it) is highly relevant to understanding what the device **is**, in the computer/software context.” *INVT SPE LLC v. Int’l Trade Comm’n*, 46 F.4th 1361, 1377 (Fed. Cir. 2022). Regardless of whether actual operation is necessary, the claimed device must at least be configured to apply word-line pre-pulse signals to groups “disposed in an order of distance from the selected word line” (claim 2), or a first group “disposed adjacent to the selected word line” (claim 3).

Third, Petitioner argues that Lee nonetheless satisfies the claims by having “word line groups that adjust—via the application of different voltage—as the selected word line changes” (Reply 11-12), but what the claims require is **not** merely “groups that adjust ... as the selected word line changes.” Rather, the claims require groups “disposed in an order of distance from the selected word line” (claims 2, 12),

or a first group “disposed adjacent to the selected word line” (claims 3, 13), neither of which is disclosed by Petition Grounds 1 and 4 as further discussed in §§III.B-III.C, and VI.B below. POR, 36-39, 65-68.

III. GROUND 1: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT LEE DISCLOSES OR RENDER OBVIOUS THE CHALLENGED CLAIMS

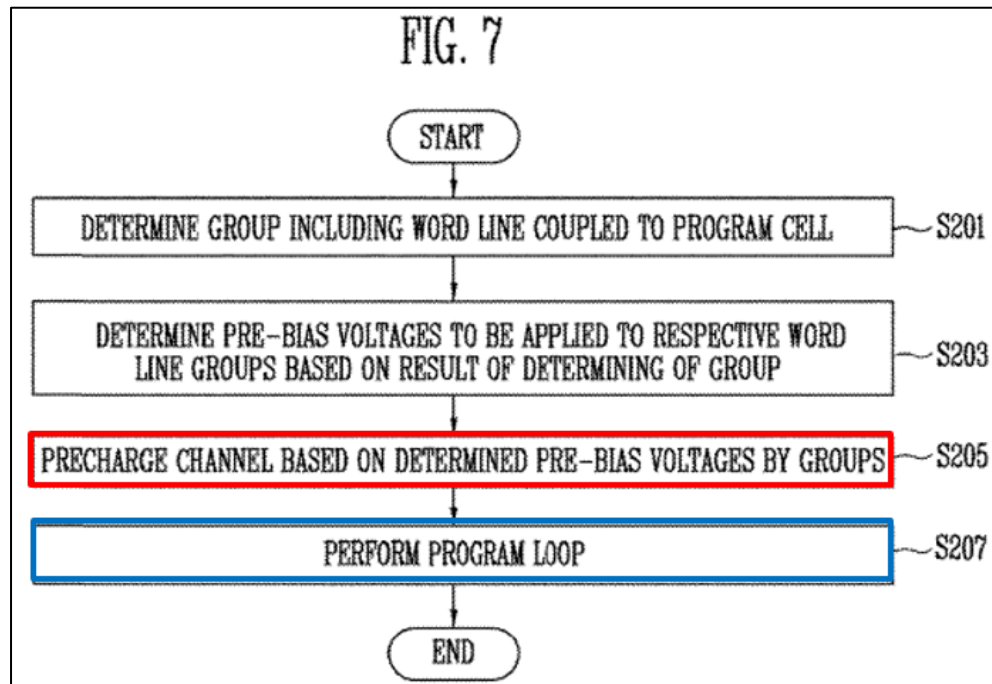
A. Independent Claims: Lee Still Fails to Disclose or Render Obvious a “[First/ Second/ Third] Word Line Pre-Pulse Signal” Applied “During a Pre-Charge Period”

Even under Petitioner’s improper new arguments, Lee does not disclose or otherwise render obvious the Challenged Claims at least because Lee’s “pre-bias” voltages are not “word line pulse signals.”

There is no dispute that the claimed “word line pre-pulse signal[s]” applied during a pre-charge period must “increase in value and then decrease in value (or vice versa).” POR, 13-14; Reply 3 (agreeing). But Lee does not disclose that the bias voltages used to pre-charge the channel (i.e., the purported “pre-pulse signal[s]”) are raised and then lowered during the pre-charge period. Rather, Lee teaches that pre-charging voltages are followed immediately by programming voltages, stating:

After the pre-bias voltage is applied to the respective word lines and the precharge operation is completed, a program voltage may be applied to the selected word line WL10, and a pass voltage may be applied to unselected word lines WL0 to WL9 and WL11 to WL31. The above-mentioned operation is a program loop for memory cells, and the program loop may be repeatedly performed.

Lee, 9:7-13, Fig. 7 (showing the “**Program Loop**” immediately following the “**Precharge Channel**” step).



The Petition fails to address this deficiency, instead asserting—without support—that the pre-bias voltages must be formed as pulses by virtue of being applied prior to the start of the programming operation. Pet., 37-38; Liu ¶203 (asserting without support that Lee uses “on-off pre-bias voltages”). Alternately, the Petition argues it was obvious to apply Lee’s pre-bias voltages as pulses because it was known for the subsequent programming voltages to be applied as “pulses.” Pet, 38-39. But Petitioner’s unsupported arguments contradict Lee’s teachings. POR, 29-35; PrzybylskiII, ¶¶78-88. Indeed, nothing in Lee suggests that pre-bias voltages are pulsed “on-off,” and Lee instead discloses that pre-bias voltages are followed immediately by programming voltages. POR, 32-34; PrzybylskiII, ¶¶85-86; Lee,

9:7-13, Fig. 7. Nor does Lee suggest that the pre-bias voltages used during pre-charging would have the same shape as voltages used during other operations (e.g., during programming). POR, 34-35; PrzybylskiII, ¶87.

The Reply improperly presents several new arguments that should have been raised in the Petition. See PTAB Consolidated Trial Practice Guide 2019, at 73 (“Petitioner may not submit new evidence or argument in reply that it could have presented earlier”); *Ariosa Diagnostics v. Verinata Health Inc.* 805 F.3d 1359, 1364 (Fed. Cir. 2015) (“Reply evidence ... must be responsive and not merely new evidence that could have been presented earlier”). Regardless, none of those arguments show that Lee discloses or renders obvious pre-bias voltages applied as pulses during a pre-charge period.

First, Petitioner incorrectly argues that pulses must be used because Lee’s pre-bias voltages are applied “during a precharge operation” that is “completed” prior to the start of the subsequent “program” operation, and there “will necessarily be a period of ramp up as the potential moves from an original to another value.” Reply 4-5. But Lee does not suggest that pre-bias voltages must be **removed** in order for the pre-charging process to be **completed**, or that the pre-bias voltages would be applied as “word line pre-pulse signals” that increase and then decrease “during the pre-charge period,” as required by the Challenged Claims. Voltages needing time to “ramp up” during Lee’s subsequent programming operation says nothing about the

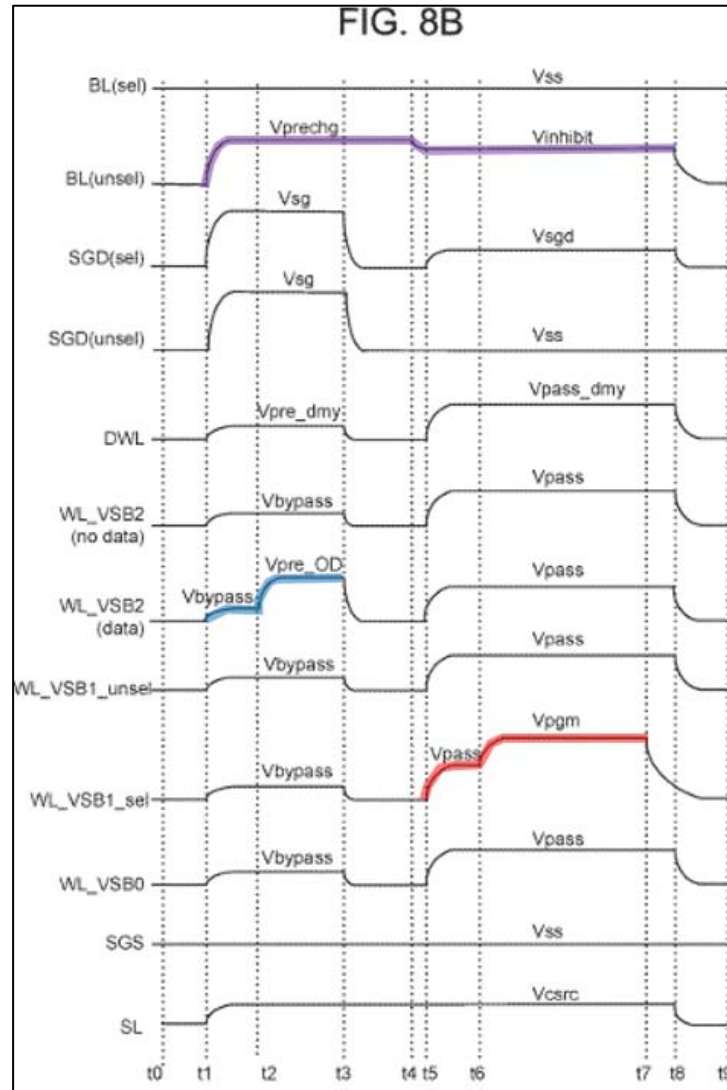
waveforms applied during the pre-charging period. Even assuming, arguendo, that Lee's pre-charging operation is followed by a "ramp up" time (or some other transition) at the start of programming, that does not suggest pre-bias voltages should be applied as "pulses" during the pre-charge operation itself. Quite the opposite, less "ramp up" is needed if the pre-charge voltage is maintained until the program operation begins as Lee indicates. Lee, 9:7-13, Fig. 7.

Petitioner's additional new argument about why "completing" pre-charging requires a pulsed signal similarly fails. Specifically, Petitioner contends that NAND devices generate voltages using a "charge pump," and applying pre-bias voltages followed directly by programming voltages will result in voltages "piled on top" of one-another that "cause pre-charging to continue for some indeterminate period while programming voltages are being applied." Reply 5-6, citing LiuII (Ex. 1021) ¶¶13-20. According to Dr. Liu, this implies that Lee's "pre-charging" cannot be "completed" until the bias voltages are returned back to their original value. LiuII ¶18. But that argument—that voltages must be returned to their original values for pre-charging to be considered "complete"—has no basis in Lee's disclosure. To the extent there is a transition period at the start of programming (e.g., as pre-charging voltages are replaced with programming voltages), that does not require or render obvious modifying Lee's pre-bias voltages to be reduced back to some initial value during the pre-charge period itself. Lee, 9:7-13, Fig. 7.

Second, Petitioner suggests Lee’s “voltage generation unit” requires all voltages to “have the same form,” or otherwise requires word line voltages to reset to 0V before outputting a new voltage (Reply 7, 9-10), but once again, nothing in Lee suggests that all applied voltages have the same form, nor does Dr. Liu’s Reply declaration provide any evidence that Lee’s “voltage generation unit” would be restricted in this way. Dr. Liu’s argument, based on Ex. 1008 (“Cappalleti”) and Ex. 1012 (“Micheloni”), is that voltage generation units are implemented in the literature using charge pumps and address decoders that generate pulses. LiuII ¶¶21-28 (*citing* Cappalleti, 259, 311, 354; Micheloni, 189, 191-192, 269). Two disclosures about charge pumps does not imply that all charge pumps work the same. More importantly, this was not part of Petitioner’s ground. Even assuming some voltage generation circuits behaved as Dr. Liu suggests, that does not alter Lee’s disclosure, which teaches applying the pre-bias voltages during the pre-charging operation, followed immediately by programming voltages. Lee, 9:7-13, Fig. 7; *see also Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1332 (Fed. Cir. 2003) (expert testimony cannot “rewrite the patent’s specification” to create a link where the language in the specification provides none).

Moreover, Dr. Liu’s ultimate conclusion—that voltages applied within NAND devices cannot “switch[] from one voltage to another without returning to ground in between” due to technical limitations—plainly contradicts the record.

LiuII ¶36. For example, the Yang reference relied on in Ground 4 illustrates several voltages transitioning between values without first returning to a starting voltage.

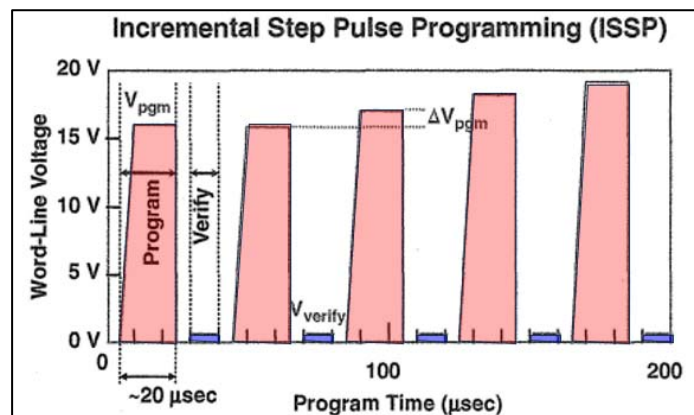


See Yang Fig. 8B (showing transitions from **Vprechg** to **Vinhibit**, **Vbypass** to **Vpre_OD**, and **Vpass** to **Vpgm** without first resetting to a starting voltage).

Finally, the Reply improperly presents a new argument based on combining Lee with “incremental step pulse programming (ISPP)” as described in Ex. 1006 (“Aritome”). This “new theory of ... obviousness absent from the petition” should

not be considered on reply. *Wasica Finance GmbH v. Continental Auto Sys.*, 853 F.3d 1272, 1286-87 (Fed. Cir. 2017). Regardless, the addition of ISPP fails to address Lee's deficiencies.

Using ISPP, a programming operation is repeated with incrementally higher programming voltages until the memory cell reaches the desired value (e.g., as shown in Aritome by multiple **programming stages** separated by **verify stages**).



Aritome, 46; see also Micheloni, 225 (describing ISPP). Petitioner and Dr. Liu mistakenly argue that ISPP requires pre-bias voltages to be applied as a pulse to avoid the “first pulse applied” from being “combined with the pre-charge voltage.” Reply 8-9, citing LiuII ¶¶40-49. But ISPP pertains to programming, not pre-charging. Regardless of how programming is performed—either using a single set of programming voltages, or a series of programming voltages—there is nothing to suggest that Lee's pre-bias voltages would be applied any differently. During any given pre-charging period, Lee applies fixed pre-bias voltages which are followed immediately by programming voltages once the pre-charging is complete. Lee, 9:7-

13, Fig. 7 (showing the “Program Loop” immediately follows the “Precharge Channel” step). Moreover, even assuming there is a transition period at the start of programming as the pre-charging voltages are replaced with an initial set of programming voltages, that does not teach or suggest modifying Lee’s pre-bias voltages to be applied as pulses during the pre-charge period itself.

B. Claims 2 and 12: Lee Still Fails to Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line”

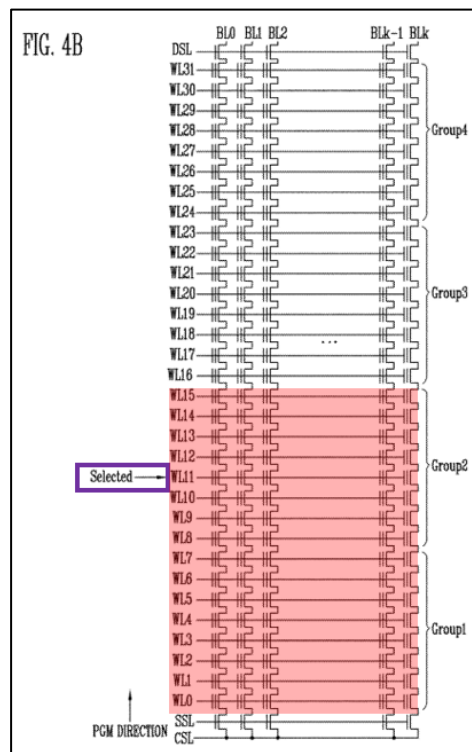
Lee does not disclose or render obvious the added limitations of dependent claims 2 and 12 requiring that the “first group,” “second group,” and “third group” of word lines are “disposed in an order of distance from the selected word line.” As explained in the POR, Lee teaches that groups are fixed in predetermined locations that do not change based on the position of the selected word line. POR, 36-38; PrzybylskiII, ¶¶89-94.

As discussed in Section IV.B (Claim Construction), the plain and ordinary meaning of the term “disposed in an order of distance from the selected word line” requires that the groups be disposed in order based on the location of the selected word line, and Petitioner’s arguments to the contrary have no basis in the record.

The Reply also misinterprets Lee as satisfying the construction set forth in the POR because multiple groups may receive the same “default” based on the location

of the selected word line. See Reply 10-12. But those new arguments still fail to show that Lee discloses or renders obvious claims 2 and 12.

In Lee, groups are fixed prior to a word-line being selected for programming, and then the “pre-bias voltages to be applied ... may be determined depending on which word line group is the group to which the selected word line belongs.” Lee, 10:63-11:9, Fig. 6. A “default” pre-bias voltage is applied to the group containing the selected word line, and all other groups “closer to the source select transistor.” Lee, 9:41-59. For example, in Fig. 4B when the **selected wordline** is inside of Group 2, “a **default value** is applied to ... **Group 2**,” and “the **default value** also is applied to ... **Group 1**” because it is closer to the source select transistor. *Id.*



Id. 9:41-59, Fig. 4B.

Even assuming, as Petitioner does, that this is equivalent to merging existing groups to form a new group, Lee still fails to satisfy the claims. At most, Lee discloses a *single* group disposed based on the location of the selected word line (i.e., the merged group containing the selected word line that receives the default voltage). The resulting system may have fewer than three groups of word lines. See Reply 12. Moreover, all word lines not receiving that default voltage remain in the same predetermined groups created *prior* to a word line being selected for programming. Accordingly, even under Petitioner's new theory, Lee fails to disclose or render obvious a "first group," "second group," and "third group" that are "disposed in an order of distance from the selected word line" as required by claims 2 and 12.

C. Claims 3 and 13: Petitioner's New Arguments Still Fail to Show that Lee Discloses or Render Obvious the "First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line"

Lee also does not disclose or render obvious dependent claims 3 and 13. POR, 38-40; PrzybylskiII, ¶¶95-98. Petitioner's Reply does not present any additional arguments for claims 3 and 13, and merely cross-references the arguments for claims 2 and 12. Reply 12-13. As discussed in Section III.B, at best Lee teaches only a *single* group disposed based on the location of the selected word line (i.e., the merged group containing the selected word line), with all other groups being predetermined irrespective of the selected word line's location. Accordingly, Lee

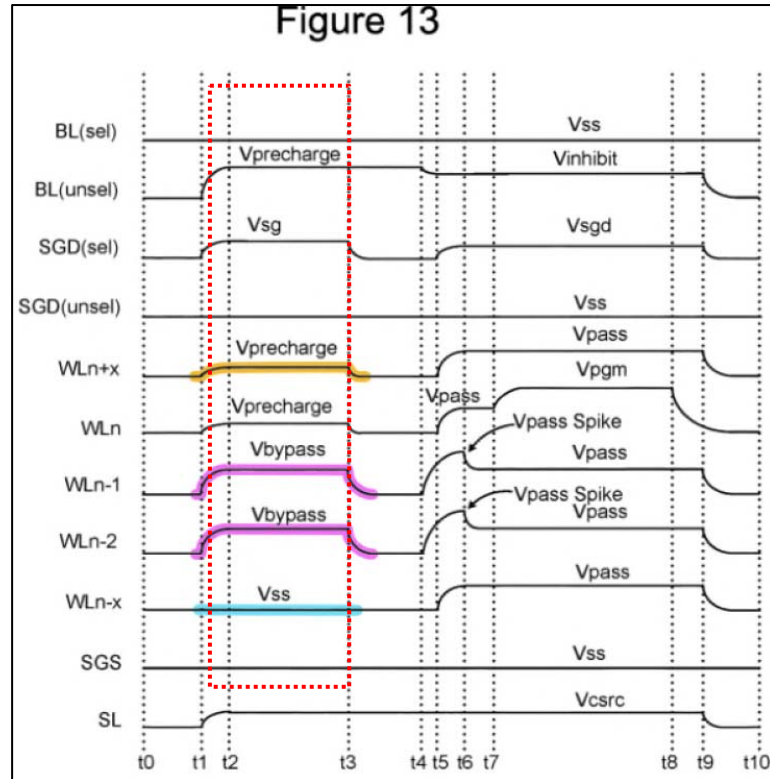
still fails to teach or suggest “the first group of the plurality of word lines are disposed adjacent to the selected word line” as required by claims 3 and 13.

IV. GROUND 2: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT ZHAO DISCLOSES OR RENDER OBVIOUS APPLYING A “FIRST WORD LINE PRE-PULSE SIGNAL ... DURING A PRE-CHARGE PERIOD”

Even under Petitioner’s new arguments, Zhao does not disclose or otherwise render obvious the independent claims because Zhao’s application of a flat V_{ss} voltage (*i.e.*, the purported “first pre-pulse signal” identified by Petitioner) is not a “pulse.” Petitioner’s new arguments fail to address this deficiency, and instead conflate Zhao’s teachings with respect to the drain side unselected word lines and source side unselected word lines.

Zhao fails to disclose applying a three “word line pre-pulse signal[s] ... during a pre-charge period” as required by the independent claims. POR, 39-44; PrzybylskiII, ¶¶99-108. In Fig. 13 of Zhao, the period “**t1-t3 corresponds to pre-charging.**” Zhao, 22:34-41. But Zhao fails to disclose three distinct “pre-pulse signals” applied during that period, and the Petition resorts to incorrectly characterizing V_{ss} as the “first ... pre-pulse signal” recited by the claims.¹ Pet., 22-23, 52.

¹ For convenience, Petitioner’s annotations for the **First**, **Second**, and **Third** groups are reproduced below.



The Petition argument fails at least because the flat “0 volt (Vss)” voltage identified is not a “word line pre-pulse signal” that increases and then decreases in value. See §II.A (Claim Construction). Rather, Zhao explicitly teaches that “*source side unselected word lines WLn-x remain at Vss (e.g., 0 v)*” throughout the relevant time period. Zhao, 23:5-12. Elsewhere, Zhao says “unselected source side word lines receive 0 volts or one or more voltages that are too low to pre-charge” during the pre-charge period. Zhao, 19:22-26. But as explained in the POR, a POSITA would have understood this to mean the flat Vss voltage applied to each source side unselected word lines WLn-x may be 0 volts, or some other value “too low to pre-charge.” POR, 43-44; PrzybylskiII, ¶¶106-108. Regardless, this is not a pulse.

The Reply disagrees, misreading Zhao as suggesting that the embodiment of Fig. 13 could be modified to replace the flat Vss signal with a pulsed signal equal to “one or more voltages that are too low to precharge.” Reply 14-15. But Petitioner’s argument conflates “source side unselected word lines” and “drain side unselected word lines,” and cherry-picks partial quotes from Zhao to suggest that “all” word lines should be “‘raised’ to various ‘pre-charge voltage[s]’ between t1-t3” before returning to their original value. Reply 14-15 (citing Zhao, 22:34-50).

Contrary to what the Reply suggests, Zhao never states that “all” word lines are “raised” to a pre-charge voltage between t1-t3. Rather, Zhao states that “[a]t time t1 ... the selected word line WLn is raised to the pre-charge voltage and the *drain side unselected word lines WLn+x* are raised to the pre-charge voltage.” Zhao, 22:41-49. Similarly, Zhao does not state that “all” word lines are returned back to ground. Rather, Zhao states that “[a]t time t3, *SGD(sel), WLn+x, WLn, WLn-1 and WLn-2* are all lowered to ground/Vss.” Zhao, 23:7-10. Zhao excludes source side word lines WLn-x from these teachings, instead disclosing that “*source side unselected word lines WLn-x remain at Vss (e.g., 0 v)*” throughout the relevant time period. Zhao, 23:5-12. Reading Zhao’s disclosures individually or in combination, word lines WLn-x start off at one or more values too low to precharge (e.g., 0V, Vss, or something similarly low), and simply remain at those values throughout the pre-charge period. POR, 39-44; PrzybylskiII, ¶¶99-108.

V. GROUND 3: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW A POSITA WOULD HAVE BEEN MOTIVATED TO COMBINE ZHAO AND LEE AS PROPOSED IN THE PETITION

Lee’s teachings are inapplicable to Zhao, and as explained in the POR, there are multiple reasons why a POSITA would not have looked to Lee to modify Zhao as illustrated in the Petition. POR 44-58; PrzybylskiII, ¶¶109-130.

The Petition incorrectly argues that a POSITA would apply Lee’s pre-bias voltages to Zhao’s drain-side word lines in view of Lee’s statement that its teachings can offset the “effects caused by the resistance component between the source select transistor and the drain select transistor.” Lee, 8:25-52; Pet. 62. As explained in the POR, those effects result from Ohm’s law ($\text{Voltage}(V) = \text{Current}(I) * \text{Resistance}(R)$) creating voltage drops due to a “resistance component between the source select transistor and the drain select transistor” when current runs through the memory string. POR 51-52, PrzybylskiII, ¶118; Lee 8:25-52. Lee’s teachings are thus inapplicable to Zhao, which has no current in the memory string. POR, 51-52; PrzybylskiII, ¶118. Moreover, even assuming Zhao suffered effects from a “resistance component,” the combination presented in the Petition ignored the differences in how Lee and Zhao perform pre-charging—with Lee applying pre-charging voltage through the source line and Zhao doing so from the bitline—which would require additional modifications that preclude combining the references as proposed in the Petition. POR, 44-58; PrzybylskiII, ¶¶109-130.

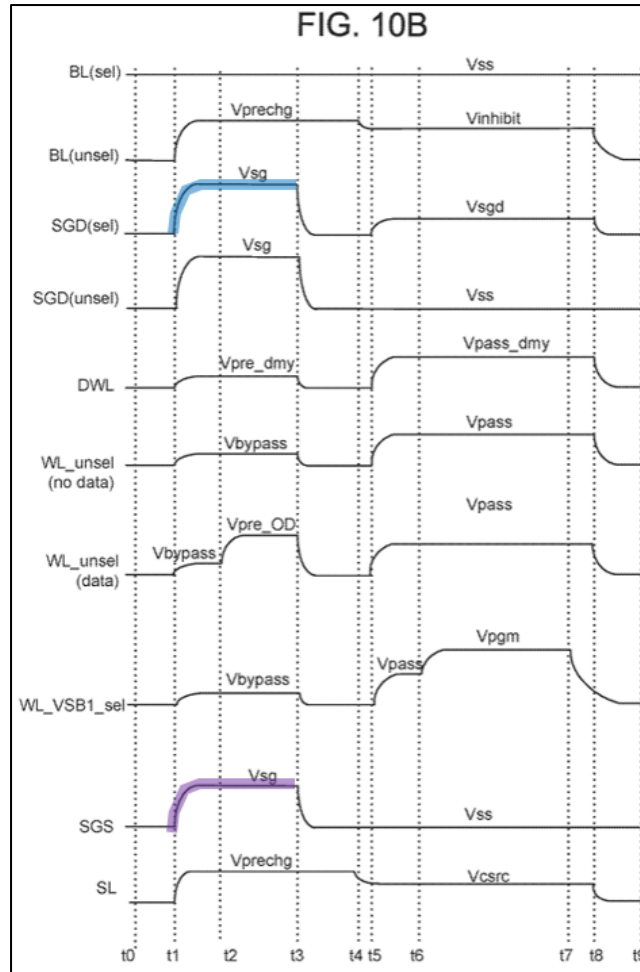
The Reply largely abandons the Petition’s motivation to combine arguments, and improperly presents several new arguments that similarly fail. These arguments urge that Lee’s statement about “effects cause by the resistance component between the source select transistor and the drain select transistor” is not describing a “resistance,” but a “chain effect” (alternately called a “body effect” or “source voltage effect” by Dr. Liu) that would exist in Zhao’s system even absent a current, and which could be addressed by applying the biasing scheme from Fig. 4 of Lee without modification. Reply 17-23; Ex. 2021 (“Liu Tr.”) 82:15-84:2. Specifically, the Reply incorrectly argues: (1) Lee’s system does not involve current in the memory string; (2) a POSITA could ignore Lee and Zhao applying pre-charging voltages from different locations; and (3) Lee’s statement about “effects caused by the resistance component” is a misnomer, and actually refers to a type of “chain effect” also present in Zhao’s system. *Id.* These new arguments fail to address the Petition’s deficiencies.

First, Petitioner incorrectly argues that the POR misinterpreted Lee as having a current running through the memory string during pre-charging. See Reply 17-18. Specifically, the Reply suggests that NAND devices can have only *one* select gate open, thus precluding current in the string. *Id.* To support this argument, Petitioner cites a statement from Ex. 1006 (“Aritome”) that “only one select gate is open during the programming phase,” and cites Yang for the proposition that a channel voltage

“can be applied to *either* end of the channel.” Reply 17-18 (emphasis in original).

Dr. Liu similarly asserts—without support—that “one of the select gates is closed” during NAND pre-charging. LiuII, ¶¶67-69.

The citations provided in the Reply have no bearing on Lee’s system, or the “effects caused by the resistance component between the source select transistor and the drain select transistor.” POR, 51-52; PrzybylskiII ¶¶118-119. How Aritome describes opening select-gates for programming says nothing about how Lee performs pre-charging. Similarly, Yang’s statement that pre-charging can be done from “either” end of the channel is irrelevant to Lee’s system. Moreover, Dr. Liu’s assertion that “one of the select gates is closed” when pre-charging (LiuII, ¶¶67, 70) is clearly contradicted by the Fig. 10 embodiment of Yang, “in which pre-charge is from *both a bit line and a source line*,” and the “**drain side select line(s) (SGD(sel))**” and “**source side select line(s) (SGS)**” are both turned on during the pre-charge phase. Yang, 2:10-19; 28:3-6; 28:26-35, Fig. 10B.



Contrary to Petitioner’s assertion that Lee and Zhao are thus presenting “compatible” and “complementary” approaches to address programming disturb (see Reply 18-19), the approaches described by Lee and Zhao remain fundamentally incompatible for the reasons explained in the POR. See POR, 55-57 PrzybylskiII, ¶¶125-129.

Second, Petitioner incorrectly argues that there would be no need to modify Lee’s teachings to account for Zhao’s applying pre-charging voltages from the bitline, rather than from the source as in Fig. 4 of Lee. Reply 19-21. Specifically, Petitioner argues that it does not matter where pre-charging voltages are applied

from, and misinterprets Fig. 5 of Lee to raise a new argument that the orientation of the pre-bias voltages (e.g., whether larger voltages are placed near the bitline or the source) depends solely on *programming direction* rather than *direction of precharging*. Reply 19-21.

Petitioner's assertion that bias voltages are identical when pre-charging from a bitline instead of the source is unsupported by the record. As explained in the POR, biasing schemes depend on where the pre-charging voltage is applied. POR, 48-50; PrzybylskiII, ¶¶115-116. Indeed, Yang uses different biasing when the “pre-charge is from a bit line” (Fig. 8 embodiments) the “pre-charge is from a source line” (Fig. 9 embodiments) or the “pre-charge is from both a bit line and a source line” (Fig. 10 embodiments). Yang 1:59-2:13, Figs. 8-10.

Petitioner's new argument based on Fig. 5 of Lee also fails. Reply 19-22. Petitioner assumes Figs. 4 and 5 of Lee both perform pre-charging from the source, and that Fig. 5 uses modified bias voltages because it has a different programming direction than Fig. 4. *Id.* But Lee does not state where the pre-charge voltage is applied in the specific embodiment of Fig. 5. Lee, 10:13-59. And even if Petitioner's interpretation of Fig. 5 were correct, it still does not address the deficiencies in the Petition. Altering bias voltages based on programming direction does not preclude the need to *also* alter the bias voltages when the location of precharging is changed, such as demonstrated by the different Yang embodiments. *See* Yang 1:59-2:13.

Finally, Petitioner improperly tries to use Dr. Liu’s testimony to rewrite Lee’s statement about offsetting the “effects caused by the resistance component between the source select transistor and the drain select transistor.” Reply 22-23; Lee, 8:25-52. The effects of the “resistance component” are only felt when a current is present in the memory string, and Zhao’s system precludes such a current. POR 51-52, PrzybylskiII, 118. Rather than address this deficiency directly, the Reply urges that Lee must not mean what it says by pointing to Dr. Liu’s deposition statements that Lee’s “resistance component” is not describing a resistance, but instead refers to “a body effect or ... source voltage effect” such that the “source voltage of one memory cell will gate the threshold voltage of that memory cell and then the subsequent memory cell ... [like] a chain effect.” Liu Tr., 82:15-84:2.

Petitioner’s new motivation argument—suggesting a POSITA would apply Lee’s teachings to offset a chain effect—was untimely and improper. It is also unsupported, and would still be inapplicable to Zhao. Indeed, there is no basis for Petitioner and Dr. Liu’s new interpretation of Lee’s teachings, as Lee does not mention any type of “body effect,” “source voltage effect,” or “chain effect.” Reply 22-23. Rather, Lee states that “a *resistance component between the source select transistor and the drain select transistor*” causes a “precharge level in a source select side channel” to be “reduced.” Lee, 8:25-31. Moreover, Petitioner’s new motivation argument fails in any case. As explained by Dr. Przybylski, the chain

effects Dr. Liu identified are also absent from Zhao. PrzybylskiII, ¶119. Such effects arise from “a voltage difference between the source and the substrate (i.e., body) of a transistor,” but “a POSITA would understand from Fig. 4E [of Zhao] that each of the memory cells is formed in the same polysilicon layer 471, and so nominally the body/substrate voltages will be identical,” implying no variation in source-substrate voltage along the string. Przybylski ¶119; Zhao, 11:1-15, Fig. 4. In short, even assuming Lee’s teachings were intended to offset a “body effect or ... source voltage effect ... [like] a chain effect” as Petitioner and Dr. Liu incorrectly suggest, Lee’s teachings would still be inapplicable in Zhao.

Accordingly, even in view of Petitioner’s new and improper Reply arguments, a POSITA would not have been motivated to apply Lee’s teachings to Zhao in the manner proposed in the Petition.

VI. GROUND 4: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT YANG DISCLOSES OR RENDER OBVIOUS THE CHALLENGED CLAIMS

A. Independent Claims: Yang Still Fails to Disclose or Render Obvious Word Line Pre-Pulse Signals with Incrementally Increasing Voltage Levels

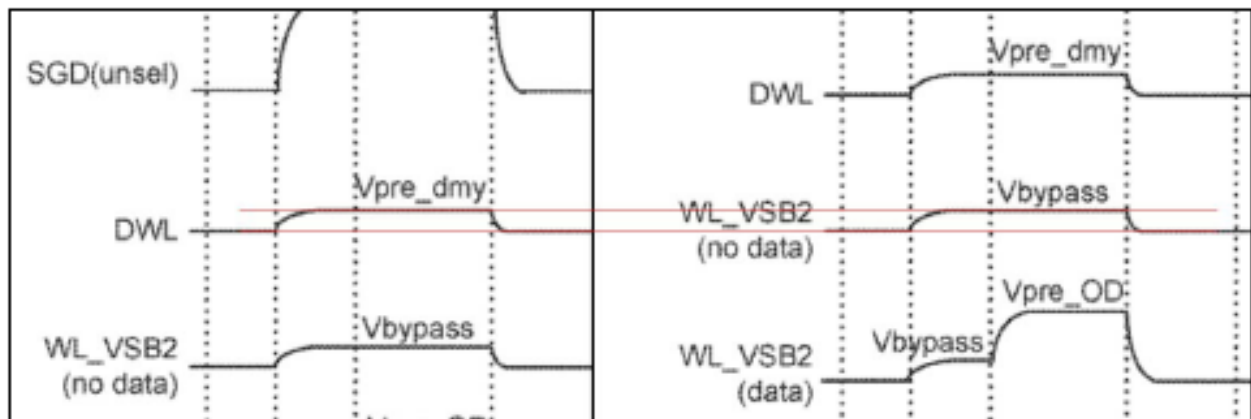
Petitioner’s new arguments fail to address the deficiencies in Yang, at least because Yang’s use of “Vbypass,” “Vpre_OD,” and “Vpre_dmy” voltages fails to disclose or render obvious three “word line pre-pulse signals” with incrementally increasing voltage levels. Moreover, Petitioner’s assertion that Fig. 8B should be set

aside and that Vpre_dmy must have some intermediate value between Vbypass and Vpre_OD is unsupported, and overlooks Vpre_dmy being applied exclusively to dummy memory cells.

As discussed in the POR, Yang does not disclose or render obvious the relative magnitudes of the purported “first” signal (Vbypass), “second” signal (Vpre_dmy), and “third” signal (Vpre_OD). POR, 58-65. Yang states that Vpre_dmy could be 5V but gives no numerical values for Vbypass or Vpre_OD, making it impossible to determine whether “a voltage level of the second word line pre-pulse signal [Vpre_dmy] is greater than that of the first word line prepulse signal [Vbypass], and a voltage level of the third word line pre-pulse signal [Vpre_OD] is greater than that of the second word line pre-pulse signal [Vpre_dmy],” as required by the Challenged Claims. Nor does Yang’s disclosure support Petitioner’s assumption that Vpre_OD must be higher than Vpre_dmy, or that Vbypass must be less than Vpre_dmy, during the pre-charging period. POR, 58-65; PrzybylskiII, ¶¶131-142.

The Petition improperly equates the claimed “**first**,” “**second**,” and “**third**” word line pre-pulse signals with Yang’s disclosure of: (1) a “**bypass voltage**” (“**Vbypass**”) applied to data word lines that are “not programmed,” (2) a “**dummy pre-charge voltage**” (“**Vpre_dmy**”) applied to a “dummy” word lines, and (3) an “**overdrive voltage**” (“**Vpre_OD**”) applied to “programmed data word lines,” respectively. Pet., 73-81. But Yang does not disclose, and the Petition fails to

otherwise show, that Vbypass, Vpre_dmy, and Vpre_OD are “word line pre-pulse signals” with the different voltage levels required by the claims. POR, 58-65; PrzybylskiII, ¶139. Indeed, the text of Yang does not describe Vpre_dmy’s magnitude relative to the other voltages, other than Vpre_dmy being illustrated identically to Vbypass in Fig. 8B in a manner that would advantageously simplify the device’s design. POR 64-65, PrzybylskiII, ¶141.



Petitioner’s new Reply arguments fail to address these deficiencies. Rather, Petitioner and Dr. Liu argue that Fig. 8B is not reliable, and incorrectly assert that Vpre_dmy has an “intermediate” value in between Vpre_OD and Vbypass based on how it is described in Yang. Reply 24-25. Specifically, Petitioner and Dr. Liu mistakenly argue that: (1) Vpre_dmy will be larger than a “threshold voltage;” (2) Vpre_OD will “exceed memory threshold voltage;” and (3) Vbypass is “lower than the memory cell threshold voltages,” and thus Vpre_dmy must have some intermediate value between the other two. *Id.* That argument ignores that Vpre_dmy

is being applied to *dummy* memory cells, and fails to establish the necessary relationship between Vpre_dmy and the other voltages.

As stated in Yang, “[t]he dummy pre-charge voltage has a magnitude such that the *dummy memory cells will operate as a pass gate*,” and “an example of Vpre_dmy is 5V, assuming that the threshold voltage is less than 5V.” Yang 24:18-27. The “threshold voltage” being described is for a dummy memory cell, which is a special structure used to “electrically isolate” different portions of the memory device. Yang, 12:35-40. By comparison, Vbypass and Vpre_OD are defined with respect to the different *programmed threshold voltages levels* found in data memory cells. See Yang 20:53-63 (“the overdrive voltage Vpre_OD will be above the threshold voltage of a data memory cell that is in any of the data states”), 20:64-21:5 (“bypass voltage is at least Vev, but no greater than Vv7”), Fig. 6.

The “threshold” described with respect Vpre_dmy has no inherent relationship with those described for Vpre_OD and Vbypass, nor have Petitioner and Dr. Liu provided any evidence establishing what that relationship would be, or why the value Vpre_dmy—even if it were somehow defined relative to programmed threshold voltages—would necessarily be between Vbypass and Vpre_OD. At most, Dr. Liu has provided the bare assertion that Vpre_dmy is “intended to exceed the programmed threshold voltage” while Vbypass must “not exceed the programmed threshold voltage.” LiuII ¶125 (emphasis in original); Reply 25. But that

unsupported statement should be afforded no weight, as it makes the same mistake as the Reply by misinterpreting Yang as defining Vpre_dmy in relation to a “programmed threshold voltage.” LiuII ¶125.

Accordingly, similar to the Petition, the Reply fails to show that Yang discloses or renders obvious three signals applied to three groups of word lines that have incrementally increasing voltage levels, as required by the Challenged Claims.

B. Claims 2-3 and 12-13: Petitioner Still Fails to Show That Yang Discloses or Renders Obvious Dependent Claims 2-3 and 12-13.

The Reply is silent on Yang’s disclosure as it relates to claim 2-3 and 12-13. As discussed in Section IV.B (Claim Construction), Petitioner incorrectly suggests those claims are satisfied any time “word lines are divided into groups and different pre-charge voltages are applied to those groups.” Reply 10-11. Properly construed, Yang does not disclose or render obvious claims 2-3 and 12-13, nor does Petitioner present any arguments suggesting Yang does. POR, 65-68; PrzybylskiII, ¶¶143-151.

VII. CONCLUSION

For at least the reasons above and in the POR, the Board should uphold all Challenged Claims as patentable.

Dated: May 9, 2025

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The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY complies with the type-volume limitation in 37 C.F.R. § 42.24(c). According to the word-processing system's word count, the brief contains 5,599 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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