

***MICRON TECHNOLOGY, INC.***  
***Petitioner***  
***v.***  
***YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.***  
***Patent Owner***

**Case No. IPR2024-00795**  
**U.S. Patent No. 11,501,822**

**Micron's Hearing Demonstratives**

**July 14, 2025**

# Overview of the '822 Patent

The present disclosure is related to a non-volatile memory device and a control method, and more particularly to a non-volatile memory device and a control method capable of applying word line pre-pulse signals with different voltage levels and reducing programming disturb.

*Ex. 1001 ('822 Patent), 1:15-19;  
See also Paper 1 (Petition), 14-15.*

# The '822 Patent's Claims

1. A memory device, comprising:
    - a plurality of memory strings;
    - a bit line connected to a first memory string of the plurality of memory strings;
    - a select gate line connected to the first memory string of the plurality of memory strings;
    - a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string; and
    - a control circuit configured to:
      - apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period;
      - apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and
      - apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,
- wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

*Ex. 1001 ('822 Patent), Claim 1*

# The '822 Patent's Claims

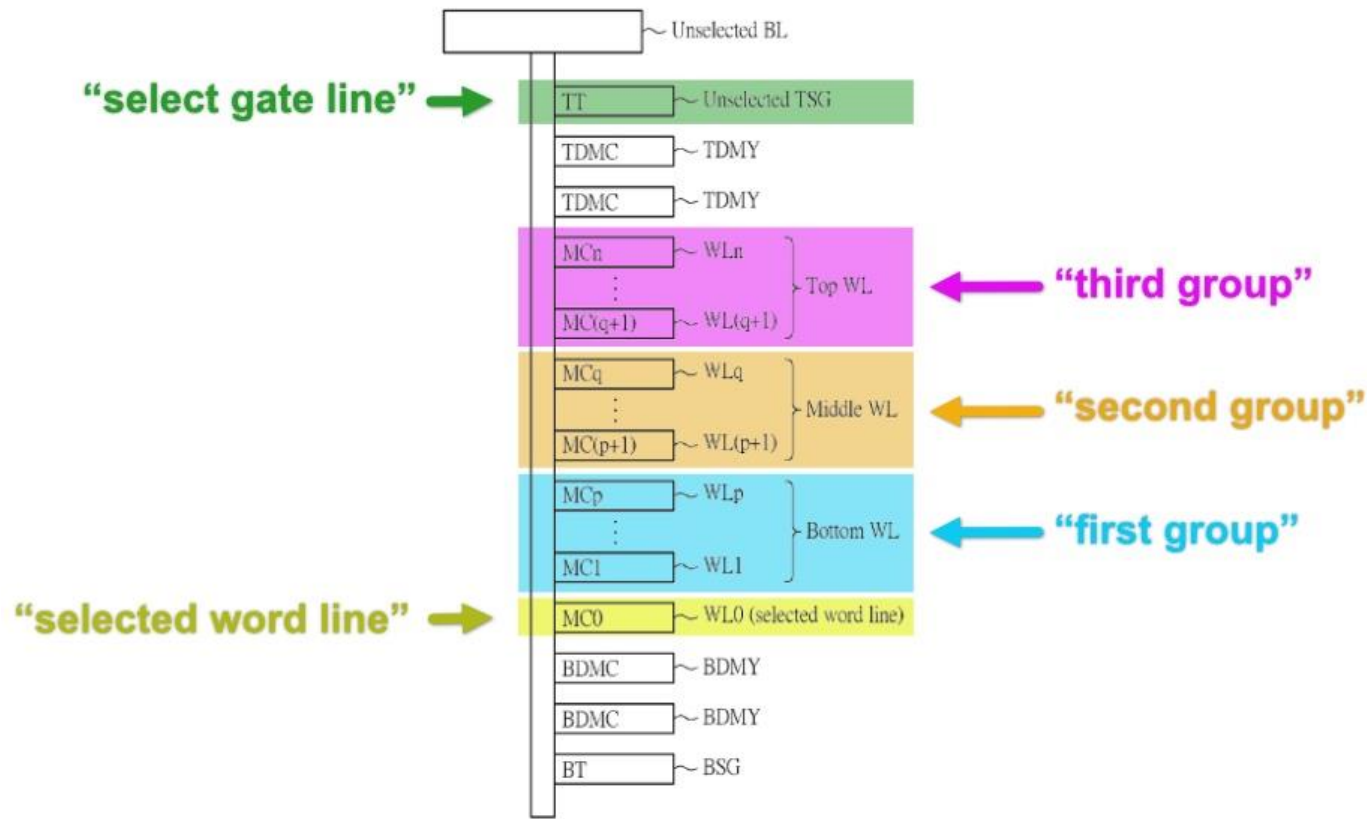
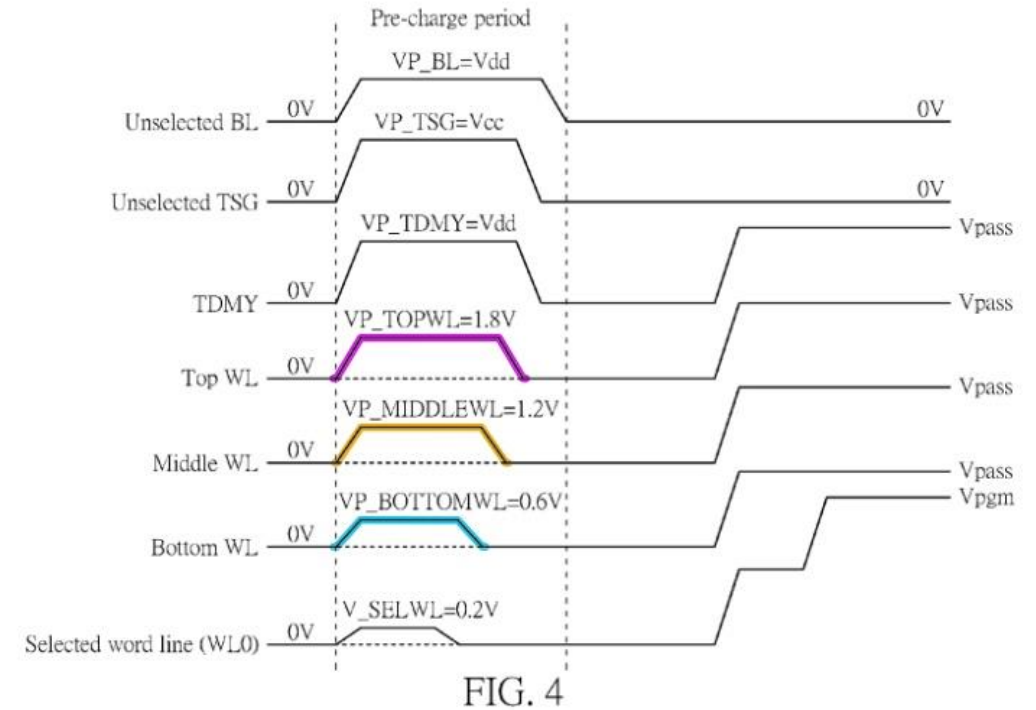


FIG. 3



Ex. 1001 ('822 Patent), Figs. 3-4;  
see also Paper 1 (Petition), 16-17.

# THE PETITION'S GROUNDS

# Instituted Grounds

| Ground | Prior Art  | Claims                                  |
|--------|------------|-----------------------------------------|
| 1      | Lee        | 1-3, 6, and 11-13 obvious               |
| 2      | Zhao       | 1, 4-7, 9, 11, 14-16, and 18-19 obvious |
| 3      | Zhao + Lee | 1-9 and 11-19 obvious                   |
| 4      | Yang       | 1-7, 9, 11-16, and 18-19 obvious        |

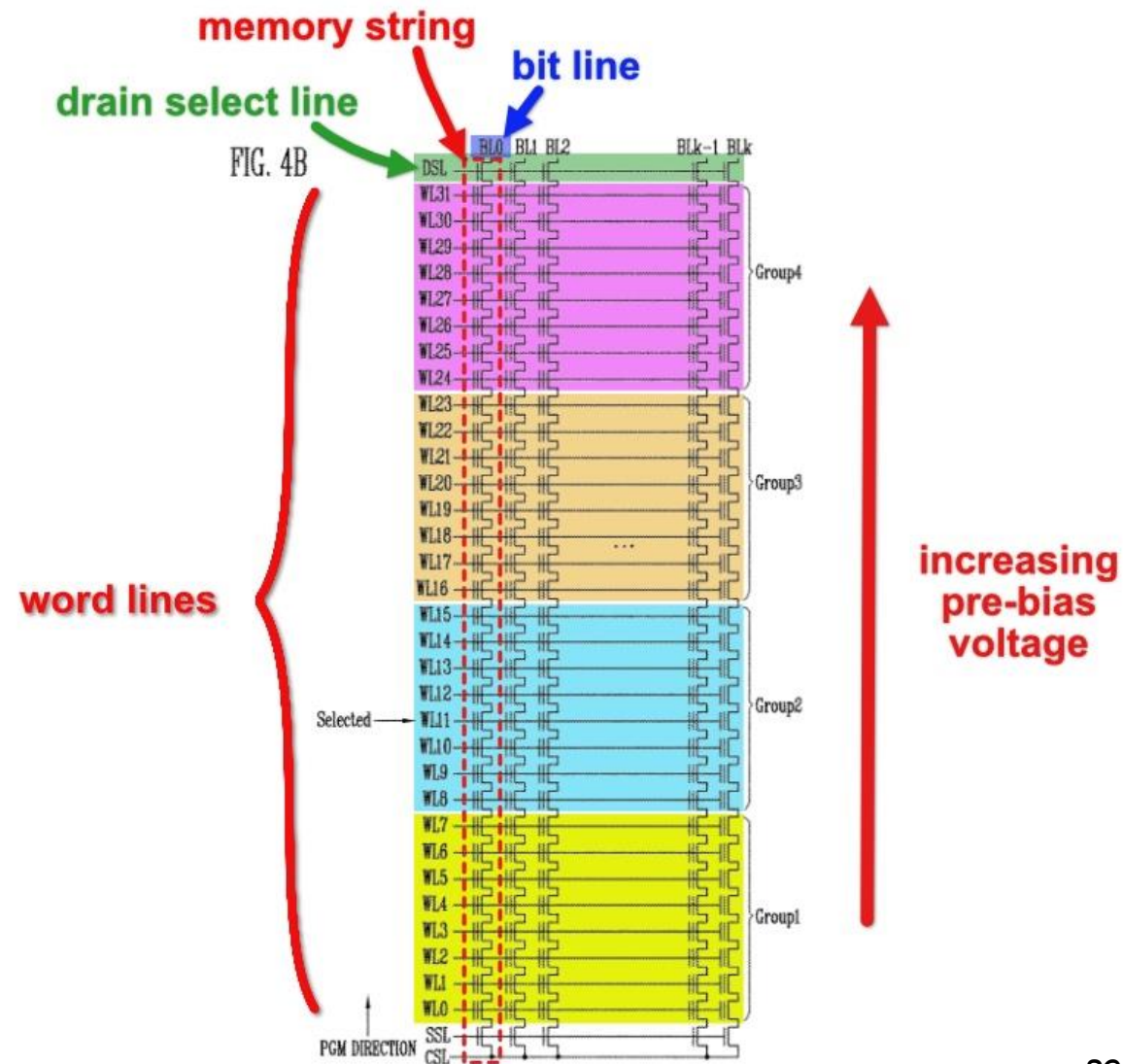
*Paper 1 (Petition), 6.*

Various embodiments in accordance with the present invention are directed toward a semiconductor memory device configured to mitigate a program disturb phenomenon, and a method of operating the semiconductor memory device.

plurality of memory cells in the memory cell array. The control logic controls the peripheral circuit and the memory cell array such that, during the program operation for the plurality of memory cells, pre-bias voltages are applied to a plurality of word lines coupled to the plurality of memory cells to precharge channel regions of the plurality of memory cells. Furthermore, different pre-bias voltages are applied to the plurality of word lines depending on the respective positions of the word lines.

*Ex. 1004 (Lee), 1:52-56, 1:62-2:3;  
see also Paper 1 (Petition), 19-20.*

# Overview of Lee



*Ex. 1004 (Lee), Fig. 4B;  
see also Paper 1 (Petition), 19-20.*

# Overview of Zhao

FIG. 1 is a block diagram of one embodiment of a memory system 100 that implements the proposed technology, including the countermeasures for avoiding program disturb discussed herein. In one embodiment, storage system

programming process of FIG. 7. In step 650, the memory system pre-charges channels of at least a subset of unselected NAND strings (ie channels connected to unselected memory cells), prior to the boosting of step 544 of FIG. 7, by applying one or more pre-charge voltages to the selected word line and drain side unselected word lines. By applying these pre-charge voltages, the voltage of the channel will be raised, which will improve the future boosting. In one

*Ex. 1005 (Zhao), 4:7-10, 19:12-19  
see also Paper 1 (Petition), 20-21.*

# Overview of Zhao

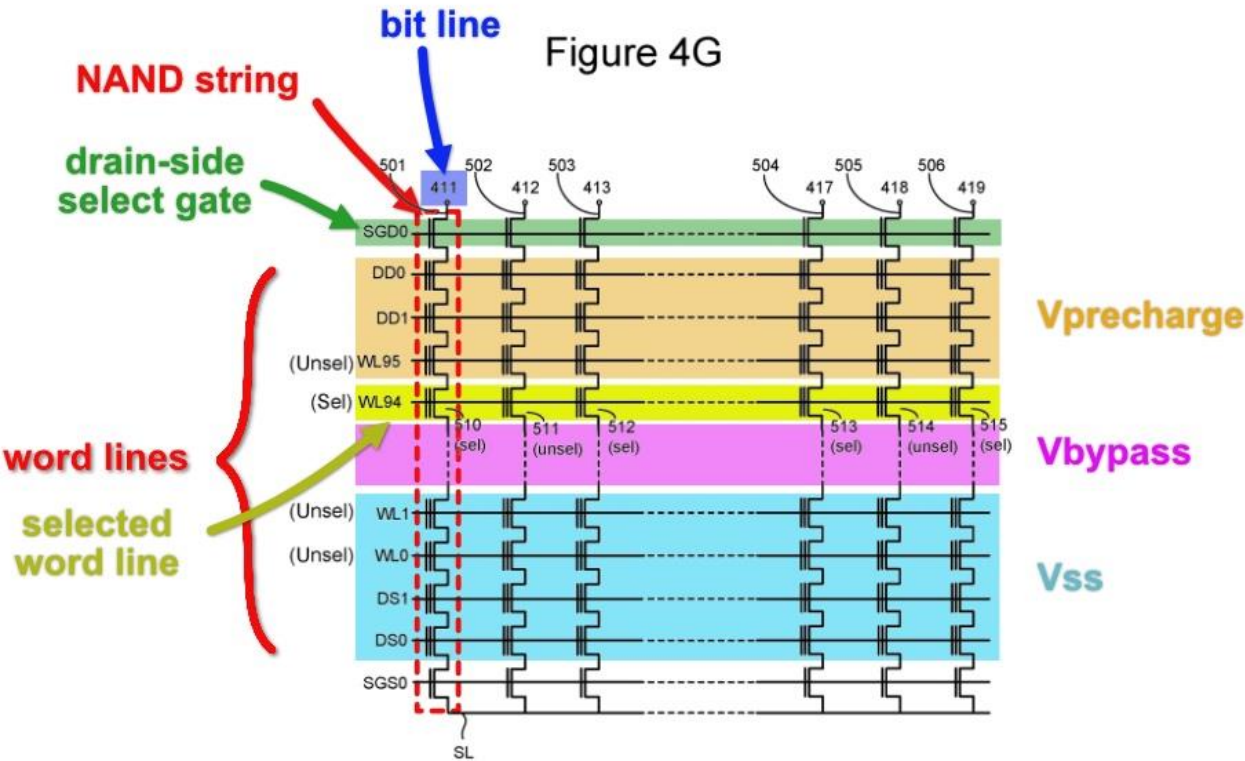
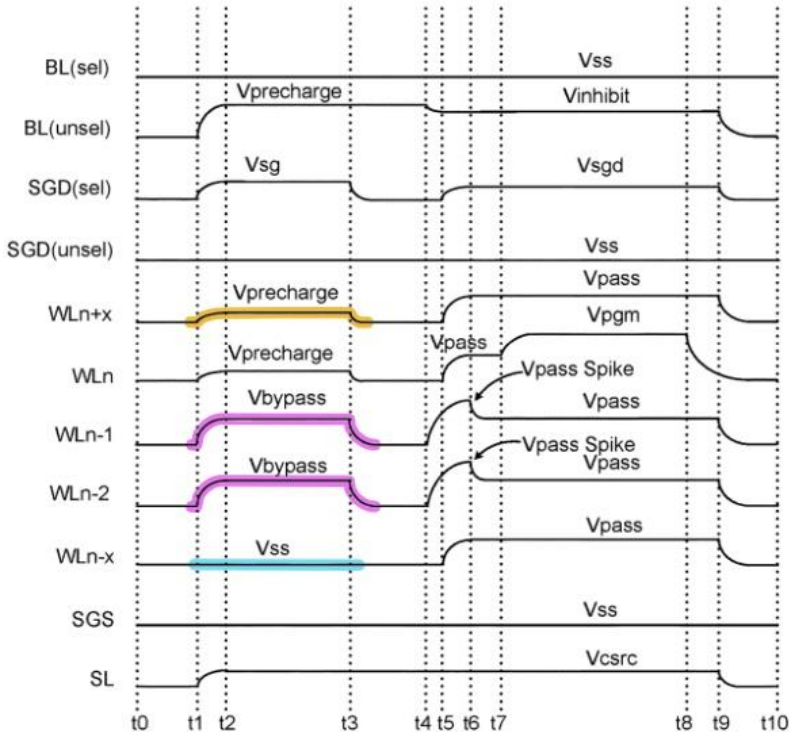


Figure 13



Ex. 1005 (Zhao), Figs. 4G, 13;  
see also Paper 1 (Petition), 21-23.

# Overview of Yang

Techniques are provided for pre-charging NAND strings during a programming operation. A NAND string comprises

In one embodiment, during the channel pre-charge phase, an overdrive voltage is applied to some memory cells and a bypass voltage is applied to other memory cells while a pre-charge voltage is applied to one or both ends of an unselected NAND string. The overdrive voltage helps to assure that the pre-charge voltage is passed to the channel of the unselected NAND string. Therefore, channel boosting (at step 544) is more effective, and program disturb is reduced or prevented.

In step 812, a dummy pre-charge voltage is applied to dummy word lines. The dummy pre-charge voltage may be

*Ex. 1010 (Yang), 2:23-25, 17:24-32, 24:18-20;  
see also Paper 1 (Petition), 23-24, 72, 78.*

# Overview of Yang

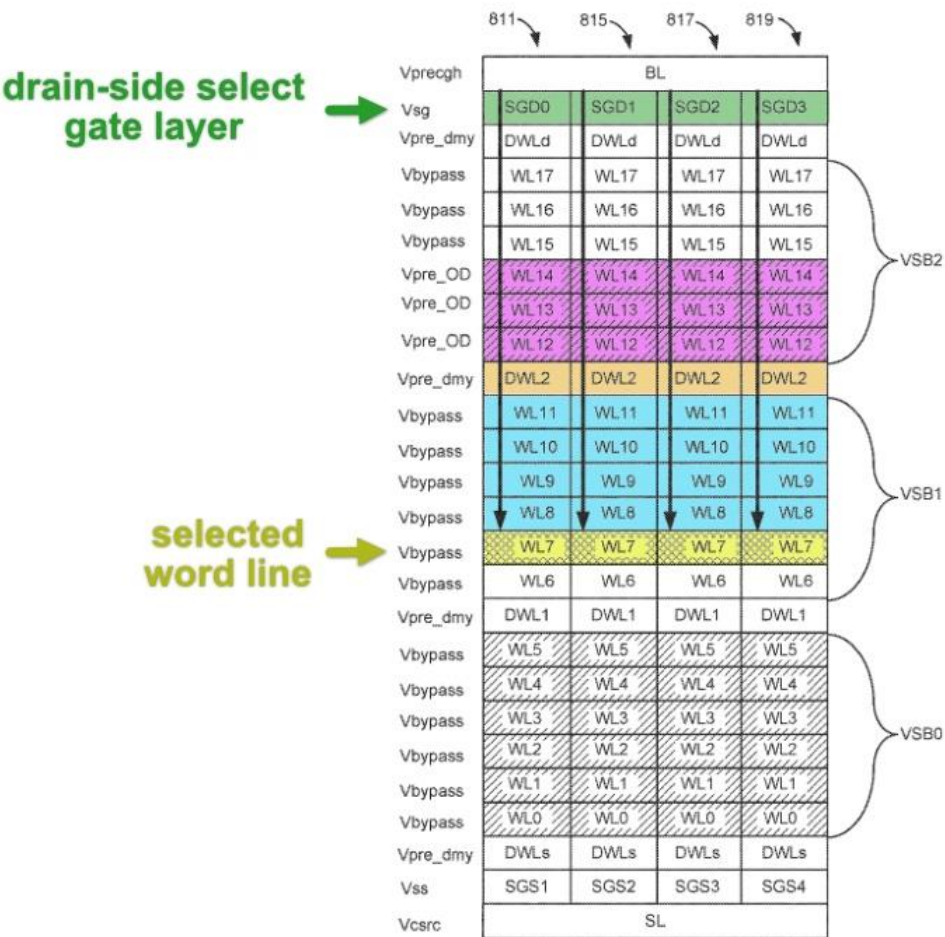
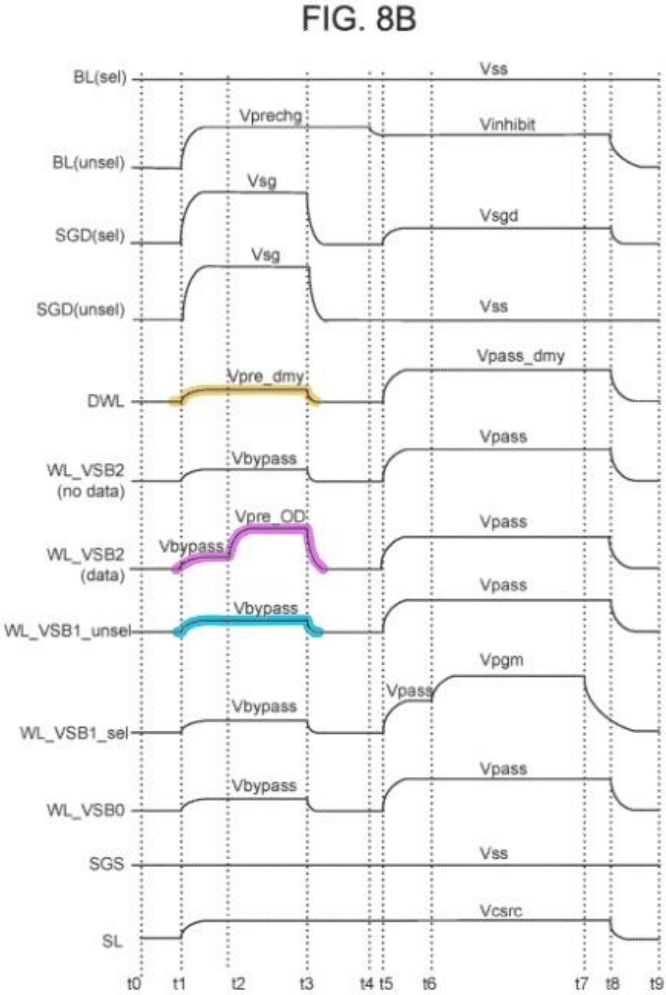


FIG. 8C



Ex. 1010 (Yang), Figs. 8B, 8C;  
see also Paper 1 (Petition), 25-26.

# THE PARTIES' REMAINING DISPUTES

# Overview of Remaining Disputes

- Does Lee supply pre-charge voltages as “pulses”? (*Ground 1*)
- Do claims 2-3 and 12-13 require word line re-grouping every time a different word line is selected for programming? (*Ground 1*)
- Does Zhao teach the supply of a non-zero, pulsed pre-charge voltage to word lines WLn-x? (*Ground 2*)
- Would it have been obvious to apply Lee to Zhao? (*Ground 3*)
- Does Yang teach three different pre-charge voltages? (*Ground 4*)

# LEE TEACHES THE CLAIMED “PULSES”

# Patent Owner's Interpretation of Lee is Technologically Infeasible and Contrary to the Prior Art

## *Patent Owner's Position:*

“Lee does not disclose any waveforms or timing characteristics for the voltages applied within its system, and Lee’s stated goal of creating a ‘uniform’ pre-charge level would suggest that pre-bias voltages are applied as a single, flat, value followed immediately by programming voltages, rather than using a pulse.”

*Paper 12 (Response), 31.*

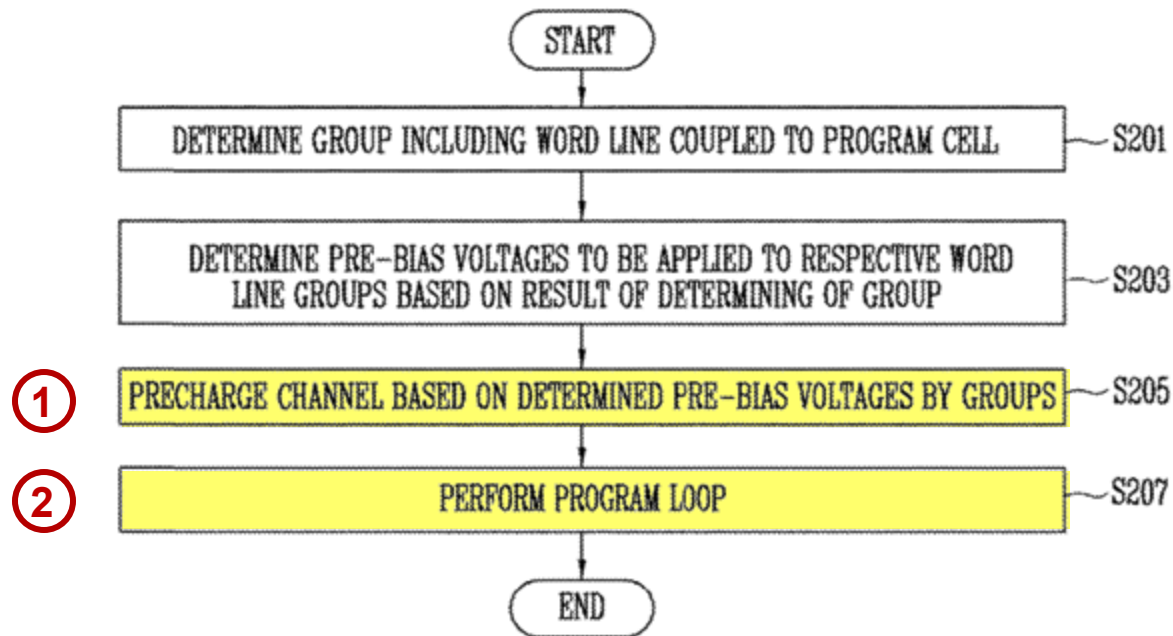
## *Patent Owner Is Incorrect:*

- Lee obviously applies pre-charge and programming voltages in **separate, distinct** steps.
- Voltages do not transition “immediately”: Patent Owner erroneously **blends** Lee’s separate pre-charging and programming steps together.
- A “voltage generation unit” like that used by Lee was known to supply voltages in the **form of pulses**.
- Programming voltages were **routinely supplied** as pulses (which requires that pre-charge voltages also be pulsed).

*Paper 14 (Reply), 3-10.*

# Lee Applies Pre-Charge Voltages Only During a Separate, Distinct Step

FIG. 7



①

The word lines coupled to a memory string in a memory block may be grouped, and different pre-bias voltages may be applied to the respective groups during a precharge operation of the cell string. Consequently, a uniform pre-charge level in the entirety of the cell string may be formed.

②

After the pre-bias voltage is applied to the respective word lines and the precharge operation is completed, a program voltage may be applied to the selected word line WL10, and a pass voltage may be applied to unselected word lines WL0 to WL9 and WL11 to WL31. The above-

*Ex. 1004 (Lee), 7:58-61, 9:7-14; Fig. 7;  
see also Paper 1 (Petition), 37-38; Paper 14 (Reply), 4-5.*

# Patent Owner's Expert Agreed that Lee Does Not Apply Program Voltages Until Pre-Charging Is Complete

Q. But the implication of that statement is you wait until pre-charging is done before you apply the programming voltages, true?

A. The implication of this statement is that you wait long enough for the pre-charge operation to have run its course and achieved the desired result before you move on to the programming step.

*Ex. 1020 (Depo. Tr.), 48:15-22, 49:13-17;  
see also Paper 14 (Reply), 6.*

# Patent Owner's Expert Also Agreed that Word Line Voltage Does Not Instantaneously Change

Q. So there's some period of ramp-up; is that fair to say?

A. Generally speaking, that's true of all circuits, that we often idealized what the voltage on nodes are. In practice, there are various RC time constants and other effects that will deviate from that idealized representation.

Q. And the same will occur if I attempt to change the word lines's potential from one value to another; there will be some period of ramp as you transition from the first potential to the second potential, true?

A. In general, the RC time constants apply for any change of Delta-v for such a circuit where there are resistances and capacitances. So it does not just apply to a change from 0 to some other voltage, but from one voltage to another.

*Ex. 1020 (Depo. Tr.), 53:16-54:8;  
see also Paper 14 (Reply), 5.*

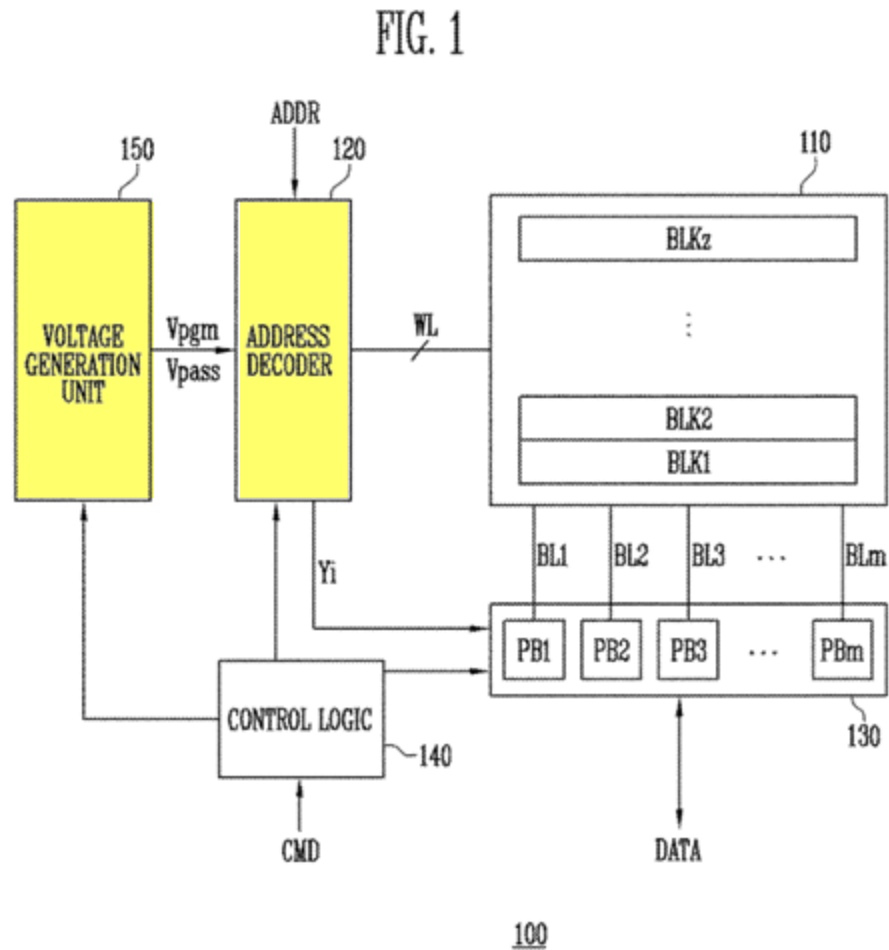
# Petitioner's Expert Dr. Liu Explained the Problem With Patent Owner's Interpretation of Lee

13. Because word line potential does not immediately change, if Lee's pre-charge voltages were not pulsed and were instead applied in the way Dr. Pryzbylski argues, word line potential would not "immediately" transition from the pre-charge to the programming value.

14. Instead, there would be a period of transition that would cause pre-charging and programming to effectively blend together: pre-charging would continue into the period where programming is meant to occur. And programming would extend back into the period when pre-charging is meant to occur. This would in turn cause pre-charging to continue for some indeterminate period while programming voltages are being applied. And it would cause programming to begin earlier than intended.

*Ex. 1021 (Liu Reply), ¶¶ 13-14;  
see also Paper 14 (Reply), 6.*

# Lee Employs a Standard “Voltage Generation Unit” and “Address Decoder”



Ex. 1004 (Lee), Fig. 1

- NAND typically employs charge pumps to generate required voltages.

Ex. 1020, 12:6-25, 33:9-16 (Przybylski Depo);  
Ex. 1008 (Cappelletti Text), 259

- Charge pumps (1) only supply voltages for discrete periods of time and (2) require time to prepare when switching from one voltage to another.

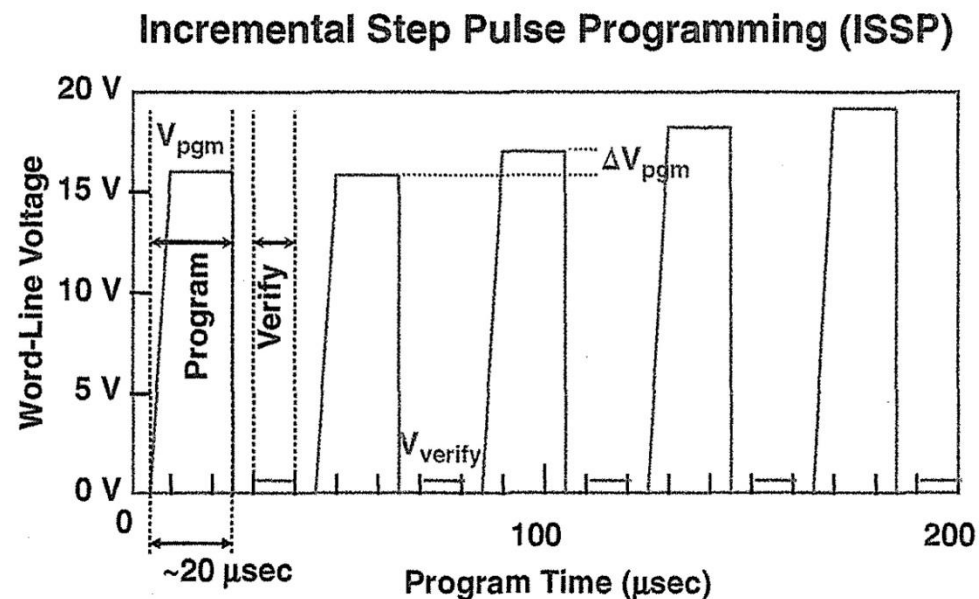
Ex. 1008 (Cappelletti Text), 311, 354

- Address decoders switch selected word lines on to supply a voltage to that line. They return the word line to 0 V when switched off.

Ex. 1020, 15:2-20 (Przybylski Depo);  
Ex. 1008 (Cappelletti Text), 269; Ex. 1012 (Micheloni Text), 191-192

see also Ex. 1021 (Liu Reply), ¶¶ 21-30  
Paper 1 (Petition), 32-33; Paper 14 (Reply), 7.

# Pulsed Programming Schemes—Which Were in Routine Use Decades Before the '822 Patent—Start at 0V, Not the Higher Pre-charge Voltage



The ISSP scheme has been used in NAND flash memory products for a long time, more than 20 years, due to fast programming speed, tight  $V_t$  distribution, and excellent reliability.

*Ex. 1006 (Aritome Text), 46, 118;  
see also Paper 1 (Petition), 39; Paper 14 (Reply), 7-8.*

**CLAIMS 2-3 AND 12-13 DO NOT REQUIRE REPEATED  
WORDLINE REGROUPING**

# Claims 2-3 and 12-13 Do Not Require Word Line Regrouping

## ***Patent Owner's Position:***

“As explained in the POR, Lee teaches that groups are fixed in predetermined locations that do not change based on the position of the selected word line.”

*Paper 15 (Sur-Reply), 11.*

## ***Patent Owner Is Incorrect:***

- The claims do not require that groups “change.”
- Even under Patent Owner's incorrect interpretation, Lee does apply different voltages to different groups of word lines as programming proceeds.

*Paper 14 (Reply), 10-12.*

# The Claims Require Only that There Be Groups: Changing Groups is Not Required

2. The memory device of claim 1, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines.

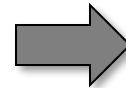
*Ex. 1001 ('822 Patent), Claim 2;  
See also Paper 14 (Reply), 10*

# Lee Applies Different Voltages to Different Groups of Word Lines as the Selected Word Line Changes

**3x groups (WL0-15, WL16-23, WL24-31),  
3x voltages:**

eight word lines. Here, there will be described the case where **eleventh word line WL11** is selected.

As described with reference to FIG. 4A, based on a group in which a selected word line is included, the closer a group is to the drain select transistor, the higher a pre-bias voltage to be applied to corresponding word lines is. That is, a pre-bias voltage that is applied to word lines WL16 to WL23 included in a third group Group3 may be higher than a pre-bias voltage that is applied to word lines WL8 to WL15 included in a second group Group2. Furthermore, a pre-bias voltage that is applied to word lines WL24 to WL31 included in a fourth group Group4 may be higher than a pre-bias voltage that is applied to word lines WL16 to WL23 included in the third group Group3. A pre-bias voltage having a default value is applied to the word lines WL8 to WL15 included in the second group Group2, including a word line WL11 that is coupled to a selected transistor. In addition, the pre-bias voltage having the default value also is applied to word lines WL0 to WL7 included in a first group, Group1, that is closer to the source select transistor than is the second group.



**2x groups (WL0-23, WL24-31),  
2x voltages:**

In another embodiment, in the case where **the selected transistor is coupled to a word line included in the third group Group3**, a pre-bias voltage having the default value may be applied to the word lines WL0 to WL23 included in the first to third groups Group1 to Group3, and a pre-bias voltage having a value higher than the default value may be applied to the word lines WL24 to WL31 included in the fourth group, Group4.

*Ex. 1004 (Lee), 9:39-55, 9:60-66;  
see also Paper 14 (Reply), 11-12.*

# ZHAO TEACHES APPLICATION OF A PULSED, NON-ZERO VOLTAGE TO ITS $WL_{N-X}$

# Zhao Teaches the Use of Non-Zero, Pulsed Pre-Charge Voltages

## ***Patent Owner's Position:***

“Zhao does not disclose or render obvious applying a ‘first word line pre-pulse signal’ because Zhao’s application of a flat, unchanging, Vss voltage ... is not a ‘pulse’ as required by the ‘822....”

*Paper 12 (Response), 39.*

## ***Patent Owner Is Incorrect:***

- Zhao teaches that a non-zero pulsed voltage can be applied to its WLn-x instead of Vss during pre-charging.

*Paper 14 (Reply), 13-16.*

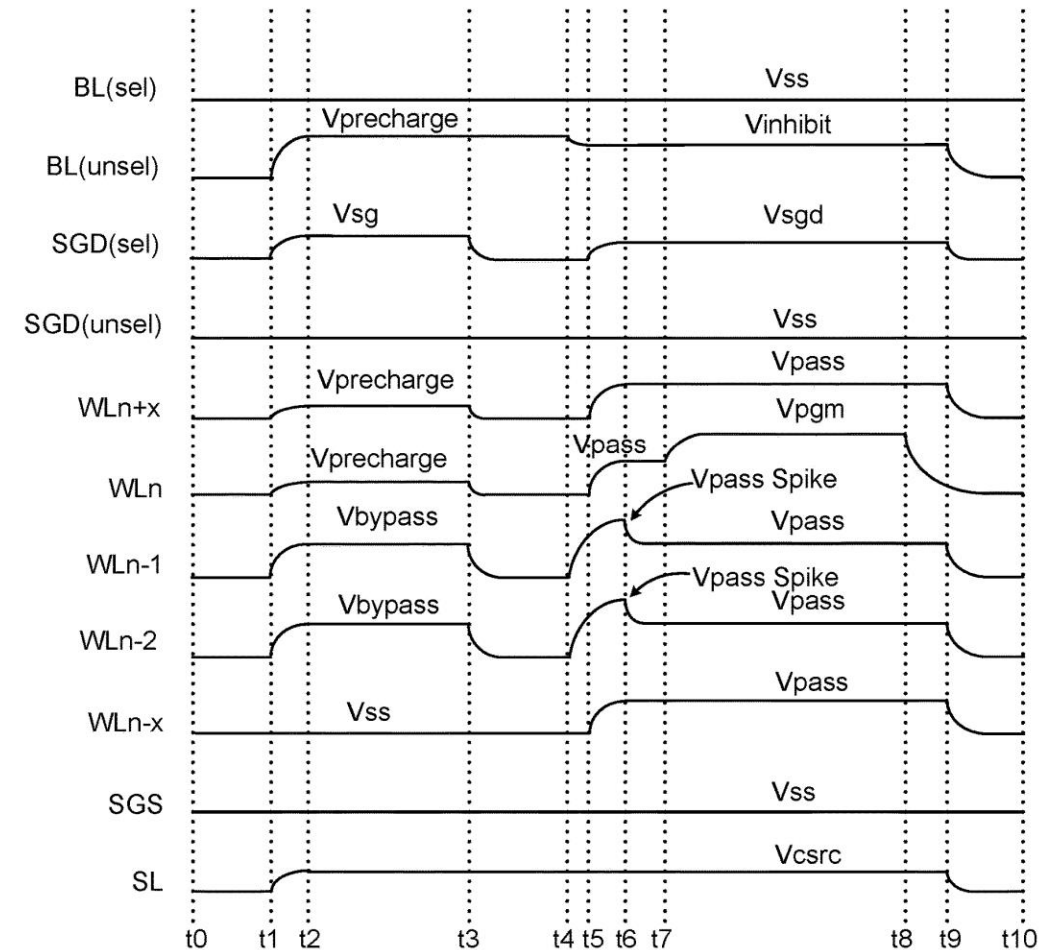
# Zhao's Lines All Start at 0V, Are Raised to a Designated Voltage During Pre-Charging, and then Return to 0V

At time  $t_0$  of FIG. 13, all the depicted signals are at 0 volts. The selected bit line BL(sel), drain side selection line

The time period of FIG. 13 from  $t_1$ - $t_3$  corresponds to pre-charging (see step 542 of FIG. 7, steps 650 and 652 of FIG. 10, and step 702 of FIG. 11). At time  $t_1$ , the source line SL is raised to  $V_{src}$  (e.g., ~2.5-3.5 volts), the unselected bit lines are raised to a pre-charge voltage  $V_{precharge}$  (e.g., ~2 volts), the drain side select line SGD(sel) connected to selected sub-blocks is raised to  $V_{sg}$  (e.g., ~6 volts), the selected word line  $WLn$  is raised to the pre-charge voltage and the drain side unselected word lines  $WLn+x$  are raised to the pre-charge voltage to cause pre-charging of the drain side channels of unselected NAND strings. This corresponds to step 650 of FIG. 10 and step 702 of FIG. 11. Also at time  $t_1$ , already programmed source side unselected word lines  $WLn-1$  and  $WLn-2$  are raised to a bypass voltage  $V_{bypass}$  (e.g., ~6-10 volts), as per step 652 of FIG. 10. The bypass

lines  $WLn-x$  remain at  $V_{ss}$  (e.g., 0 v). At time  $t_3$ , SGD(sel),  $WLn+x$ ,  $WLn$ ,  $WLn-1$  and  $WLn-2$  are all lowered to ground/ $V_{ss}$ . At this point in time the pre-charge process has completed and the drain side of channel of the unselected

Figure 13



Ex. 1005 (Zhao), 22:34-35, 22:39-53, 23:8-11, Fig. 13;  
see also Paper 1 (Petition), 51; Paper 14 (Reply), 11-12.

# Zhao Teaches That Word Lines WLn-x Can Either “Remain” at 0 V or Alternatively “Receive” a Non-Zero Voltage During Pre-Charging

bypass voltages. The remaining source side unselected word lines WLn-x remain at Vss (e.g., 0 v). At time t3, SGD(sel),

The process of FIG. 10 is performed during the programming process. For example, steps 650 and 652 of FIG. 10 are performed as part of step 542 (channel pre-charge) of the programming process of FIG. 7. In step 650, the memory system pre-charges channels of at least a subset of unselected NAND strings (ie channels connected to unselected memory cells), prior to the boosting of step 544 of FIG. 7,

...

raised, which will improve the future boosting. In one embodiment, only the drain side of the channel is pre-charged and the source side of the channel is not pre-charged. To prevent the source side of the channels from being pre-charged, unselected source side word lines receive 0 volts or one or more voltages that are too low to pre-charge and/or too low to turn on memory cells in a highest data state (e.g., data state S7). In other embodiments both the source

*Ex. 1005 (Zhao), 23:7-9, 19:9-26  
see also Paper 1 (Petition), 50-51; Paper 14 (Reply), 13-14.*

**IT WOULD HAVE BEEN OBVIOUS TO APPLY LEE'S  
TEACHINGS TO ZHAO**

# Patent Owner Misunderstands How 3D NAND Pre-Charging Occurs

## *Patent Owner's Position:*

“Lee is concerned with problems arising from charging operations performed via the common source line, while Zhao instead performs charging from the bit-line. ... Lee is concerned with compensating for the effect of a ‘resistance’ component that appears between the source and drain, those effects are not present in Zhao’s system. ... [T]here is no current flowing through the memory string in Zhao.”

*Paper 12 (Response), 45, 50.*

## *Patent Owner Is Incorrect:*

- It does not matter whether voltage is applied to the source or drain end of the channel: pre-charging results from ***potential differences***.
- Current ***never flows*** from the channel source to drain during pre-charging.
- Zhao and Lee provide ***complementary solutions*** to the same problem.

*Paper 14 (Reply), 16-24.*

# Pre-charging Results from Potential Differences, Not Current Flow

71. The purpose of applying voltages during pre-charging is to purge and redistribute electrons already in the channel that may later cause program disturb.

This is explained in both Lee (*e.g.*, Lee, 1:52-56 (discussing the mitigation of “program disturb”)) and Zhao (Zhao, 17:4-12 (noting that “program disturb” can be caused by “electrons trapped in the channel”). Indeed, Dr. Przybylski noted this himself, explaining that in Zhao pre-charging “allow[s] electrons to flow freely” for purposes of “eliminat[ing]” unwanted “voltage differential.” Ex. 2001, ¶ 46.

72. During pre-charging, a voltage is applied to both the channel and the word lines.

73. The overall amount of channel pre-charging (*i.e.*, total electron movement and purging) is controlled by the voltage applied to the channel itself.

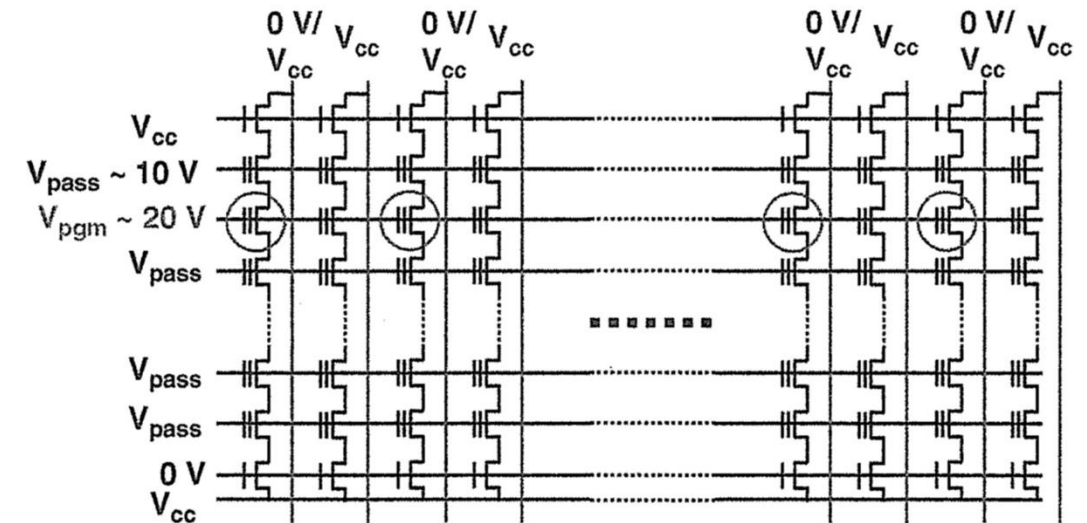
74. The relative amount of charging along the channel (*i.e.*, the electron distribution) is controlled by the application of different voltages to the word lines intersecting the channel.

75. A greater potential difference between the voltage applied to a particular word line and the voltage applied to the channel results in more pre-charging in the portion of the channel associated with that word line.

*Ex. 1021 (Liu Reply), ¶¶ 71-75  
see also Paper 14 (Reply), 17.*

## Pre-charging Results from Potential Differences, Not Current Flow

69. The only period during NAND operation when channel current flows between bitline and the source is during a read. During this phase of operation, only the low power supply voltage is applied across the channel of the string. The charge pumps are not employed, so there is no risk to this componentry. Channel current between bitline and the source does not flow during any other period of operation. One reason for this is that during other phases of operation, including program and erase, high voltages are supplied from the charge pumps. Flowing current through the channel during the precharging and programming operations would cause the charge pumps supplying the bitline voltage to collapse, adversely impacting memory operation.



*Ex. 1021 (Liu Reply)*, ¶ 69; *Ex. 1006*, 45;  
see also *Paper 14 (Reply)*, 17.

# Lee References a “Resistance Component,” Not Current Flow

WL31. In the case of the typical program operation, during a precharge operation of an unselected memory string, a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor. Consequently, the precharge level in a source select side channel is reduced and thus channel boosting is not effectively generated. Therefore, a program disturb occurs. In the case of the semiconductor memory device according to the embodiment of the present disclosure, during a precharge process, the closer a word line group to which a word line belongs is to the drain select transistor, the higher a pre-bias voltage to be applied to the word line may be. In other words, in the semiconductor

. . .

may be applied to the corresponding word line. Therefore, effects caused by the resistance component between the source select transistor and the drain select transistor are offset, whereby the precharge level in the channel may be uniformly formed. Consequently, a program disturb phenomenon is mitigated.

*Ex. 1004 (Lee), 8:25-51;  
see also Paper 1 (Petition), 19; Paper 14 (Reply), 22-23.*

# Lee's "Resistance Component" Does Not Relate to Current Flow

Q. What does it mean to have a resistance component between the source select transistor and the drain select transistor?

A. Okay. In the context of Lee -- I want to make sure that there is no disconnect in understanding. In the context of Lee, what it means by resistor component is this: It simply means the threshold voltage of a transistor is a function of how many transistor was connected in series with it.

This has to do -- some people call this a body effect or source voltage --

(Court Reporter clarification.)

THE WITNESS: Body effect or source re -- source voltage effect.

110. I explained this to Patent Owner during my deposition. Here, Lee is referring the fact that the threshold voltages of transistors connected in series along a channel vary in the direction of programming. See Ex. 2021, 83:12-84:2

111. Lee simply adjusts the voltages applied to each word line during pre-charging to account for these transistor threshold voltage differences, so that there is a gradient in the channel potential to facilitate uniform precharging, for eventual uniform channel boosting. See Lee, 8:25-29, 8:47-51. Moreover, Lee is plainly tailoring its applied word line voltages to not only account for any channel resistance, but also to prepare the array's cells using the minimum necessary voltage.

*Ex. 2021 (Liu Depo), 82:12-25; Ex. 1021 (Liu Reply), ¶¶ 110-111 see also Paper 14 (Reply), 22-23.*

# Lee's Pre-Charge Voltages Are Not Meant to Account for Current Flow (as No Current Is Flowing in Lee)

FIG. 4A

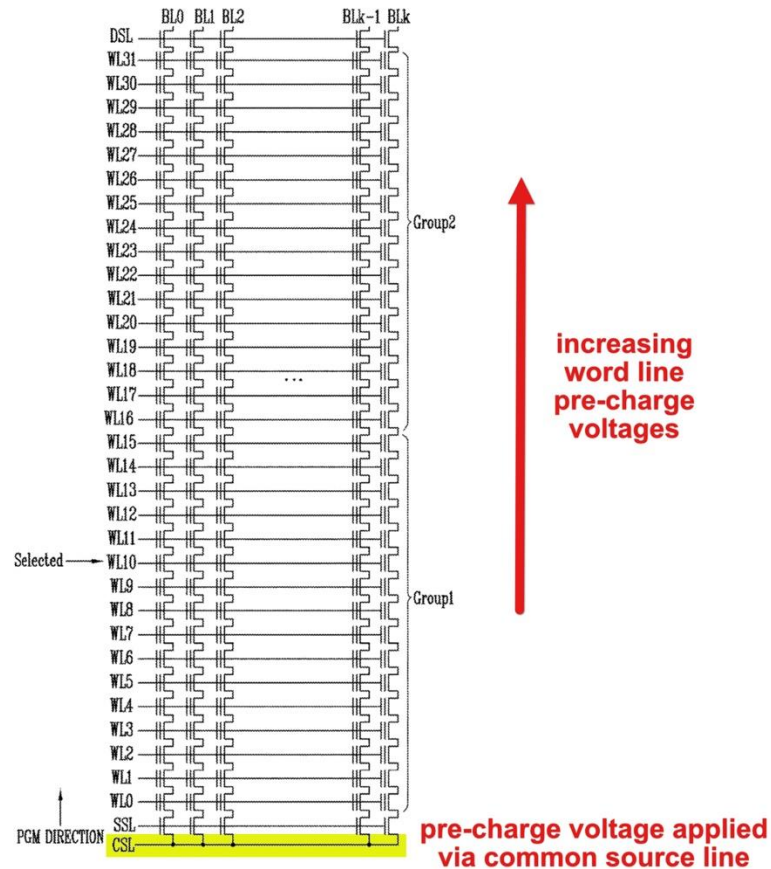
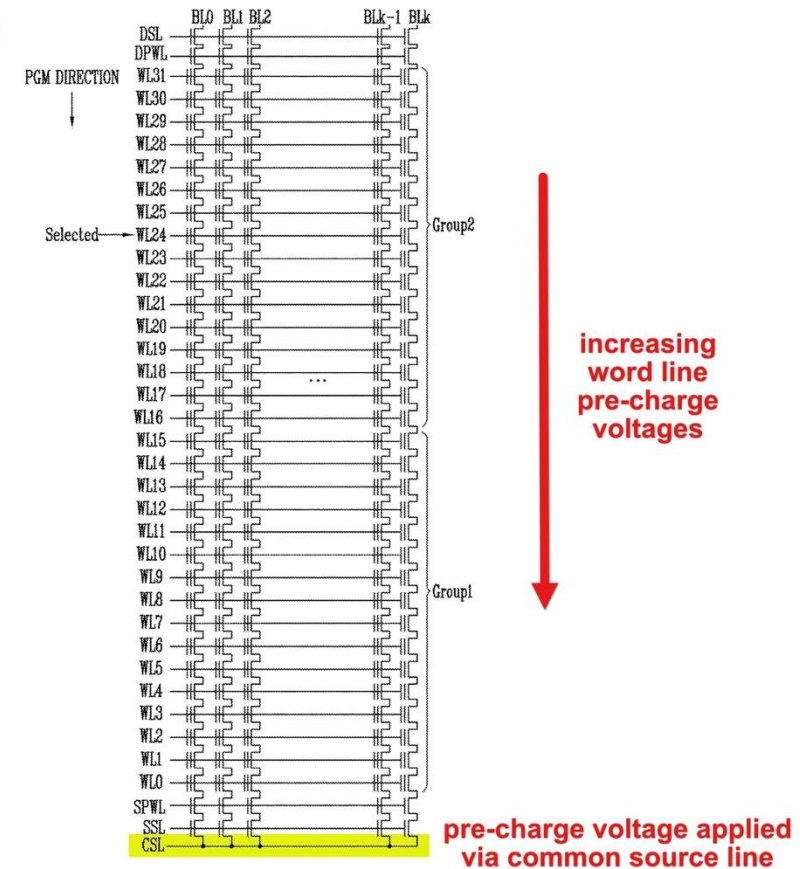


FIG. 5A



Ex. 1004 (Lee), Figs. 4A, 5A;  
see also Paper 14 (Reply), 20-21.

# Zhao and Lee Provide Complementary Solutions to the Same Problem

## Zhao:

error in the data being stored. In some cases, program disturb can result from electrons trapped in the channel being accelerated from one side of a selected word line to another side of the selected word line and redirected into the selected word line. To prevent such program disturb, countermeasures are proposed to open the channel from one side of a selected word line to the other side of the selected word line (e.g., from the source side of the selected word line to the drain side of the selected word line or from the already programmed side of the selected word line to the not yet programmed side of the selected word line) after a sensing operation for program verify and prior to a subsequent programming signal being applied.

## Lee:

WL31. In the case of the typical program operation, during a precharge operation of an unselected memory string, a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor. Consequently, the precharge level in a source select side channel is reduced and thus channel boosting is not effectively generated. Therefore, a program disturb occurs. In the case of the semiconductor memory device according to the embodiment of the present disclosure, during a precharge process, the closer a word line group to which a word line belongs is to the drain select transistor, the higher a pre-bias voltage to be applied to the word line may be. In other words, in the semiconductor

...

may be applied to the corresponding word line. Therefore, effects caused by the resistance component between the source select transistor and the drain select transistor are offset, whereby the precharge level in the channel may be uniformly formed. Consequently, a program disturb phenomenon is mitigated.

*Ex. 1005 (Zhao), 2:14-26; Ex. 1004 (Lee), 8:25-32;  
see also Paper 1 (Petition), 60-61, 66-67; Paper 14 (Reply), 218-19.*

# **YANG TEACHES THREE DIFFERENT PRE-CHARGE VOLTAGES**

# Patent Owner Relies Exclusively On How Yang's Figures Are Drawn

## ***Patent Owner's Position:***

“Petitioner has not identified anything in Yang to suggest that a POSITA would have been motivated to use a value for  $V_{pre\_dmy}$  that is different than that of  $V_{bypass}$ . To the contrary, placing copies of the waveforms side-by-side shows that  $V_{pre\_dmy}$  and  $V_{bypass}$  are illustrated in Fig. 8B as having identical values.”

*Paper 12 (Response), 64.*

## ***Patent Owner Is Incorrect:***

- Yang's figures are not drawn to scale.
- Yang repeatedly teaches that three different voltages are to be applied to its word lines during pre-charging.

*Paper 14 (Reply), 24-25.*

# Yang Explains the Differences Among Its Pre-Charge Voltages

The system uses a “bypass voltage” during the pre-charge phase of step 542, in one embodiment. The bypass voltage is at least  $V_{ev}$ , but no greater than  $V_{v7}$ , in one embodiment. For example, the bypass voltage could be  $V_{r1}$ ,  $V_{v1}$ ,  $V_{v2}$ , etc. Thus, the bypass voltage, when applied to a control gate of a data memory cell during a pre-charge phase of a programming operation, will cause the memory cell to operate as a pass gate if the memory cell is in an erased state, but not act as a pass gate for at least one programmed state.

dummy word lines. The dummy pre-charge voltage may be applied to all dummy word lines. The dummy pre-charge voltage has a magnitude such that the dummy memory cells will operate as a pass gate (e.g., conduct a current). The magnitude can differ for the different dummy word lines. With reference to FIG. 8B, the voltage on the dummy word lines (WDL) is raised to  $V_{pre\_dmy}$  at time  $t1$  and maintained until time  $t3$ . An example of  $V_{pre\_dmy}$  is 5V, assuming that the threshold voltage is less than 5V.

FIG. 6 also shows an overdrive voltage  $V_{pre\_OD}$ , which may be applied to control gates of data memory cells in step 542. The overdrive voltage is above all of the data states.

*Ex. 1010 (Yang), 24:18-27, 20:64-21:5, 20:53-55; see also Paper 1 (Petition), 81-82; Paper 14 (Reply), 24-25.*

