

Patent Owner's Demonstrative Slides

Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.
Inter Partes Review of
U.S. Patent No. 11,501,822
July 14, 2025

IPR2024-00795
Patent Trial and Appeal Board
United States Patent and Trademark Office

YMTC Ex. 2031
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I. Introduction

Table of Abbreviations

Abbreviation	Description
'822	U.S. Pat. No. 11,501,822 (Ex. 1001)
Aritome	Aritome, "NAND Flash Memory Technologies" (2016) (Ex. 1006)
Brown	Brown et al., "Nonvolatile Semiconductor Memory Technology" (1998) (Ex. 1007)
Cappalleti	Cappalleti, et al., "Flash Memories" (1999) (Ex. 1008)
Challenged Claims	'822, Claims 1-9 and 11-19
Chen	U.S. Pat. No. 10,770,157 (Ex. 2004)
Hambley	Hambley, "Electrical Engineering Principles and Applications, Fourth Edition" (2008) (Ex. 2022)
Kim	U.S. Pub. No. 2011/0194351 (Ex. 2005)
Lee	U.S. Pat. No. 10,121,529 (Ex. 1004)
Liu	Declaration of Dr. David Kuan-Yu Liu (Ex. 1003)
Liull	Reply Declaration of Dr. David Kuan-Yu Liu (Ex. 1021)
Micheloni	Micheloni et al., "Inside Solid State Drives (SSDs)" (2nd Ed. 2018) (Ex. 1012)
Office	U.S. Patent and Trademark Office
Parallel District Court Litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petition or Pet.	Petition (Pap. 1)
Petitioner	Micron Technology, Inc.
POR	Patent Owner's Response (Pap. 12)
POSITA	Person of ordinary skill in the art
POSR	Patent Owner's Sur-reply (Pap. 15)
Przybylski	July 17, 2024, Declaration of Dr. Steven Przybylski (Ex. 2001)
Przybylskill	January 3, 2025, Declaration of Dr. Steven Przybylski (Ex. 2011)
Reply	Petitioner's Reply (Pap. 14)
Yang	U.S. Pat. No. 10,726,920 (Ex. 1010)
Zhao	U.S. Pat. No. 10,643,718 (Ex. 1005)

All citations within quotations omitted herein, and emphasis added unless otherwise indicated

'822 Claim 1

- Claim 1 of the '822 recites:

[1.Pre] 1. A memory device, comprising:

[1.A] a plurality of memory strings;

[1.B] a bit line connected to a first memory string of the plurality of memory strings;

[1.C] a select gate line connected to the first memory string of the plurality of memory strings;

[1.D] a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string; and

[1.E] a control circuit configured to:

[1.E.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period;

[1.E.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[1.E.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,

[1.E.4] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

'822 Claims 2-3

- Claim 2 of the '822 recites:

The memory device of claim 1, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines.

- Claim 3 of the '822 recites:

The memory device of claim 1, wherein the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.

'822 Claim 11

- Claim 11 of the '822 recites:

[11.Pre] 11. A method of controlling a memory device, the memory device comprising a plurality of memory strings, a bit line connected to a first memory string of the plurality of memory strings, a select gate line connected the first memory string of the plurality of memory strings, a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string, the method comprising:

[11.A] applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period;

[11.B] applying a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during the pre-charge period;

[11.C] applying a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[11.D] applying a third word line pre-pulse signal of the plurality of word line pre-pulse signals to a third group of the plurality of word lines during the pre-charge period;

[11.E] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

'822 Claims 12-13

- Claim 12 of the '822 recites:

The method of claim 11, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines.

- Claim 13 of the '822 recites:

The method of claim 11, wherein the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.

Grounds

Claims	Ground
'822, claims 1-3, 6, and 11-13	Lee Obviousness
'822, claim 1, 4-7, 9, 11, 14-16, and 18-19	Zhao Obviousness
'822, claims 1-9 and 11-19	Zhao in view of Lee Obviousness
'822, claims 1-7, 9, 11-16, and 18-19	Yang Obviousness

Pet. at 12.

Disputed Issues

Issue	Slides
Pre-Pulse Signal Limitations (all Challenged Claims) • Ground 1 (Lee): Lee Does Not Disclose or Render Obvious a “[First/ Second/ Third] Word Line Pre-Pulse Signal” Applied “During a Pre-Charge Period” (Limitations [1.e.1]-[1.e.3] and [11.b]-[11.d]) • Ground 2 (Zhao): Zhao Does Not Disclose or Render Obvious Applying a “First Word Line Pre-Pulse Signal ... During a Pre-Charge Period” (Limitations [1.e.1] and [11.b]) • Ground 3 (Zhao in view of Lee): A POSITA Would Not Have Been Motivated to Combine Zhao and Lee in the Manner Proposed in the Petition • Ground 4 (Yang): Yang Does Not Disclose or Render Obvious Word Line Pre-Pulse Signals with Incrementally Increasing Voltage Levels	Slides 10-30
“Disposed in an Order of Distance from” and “Disposed Adjacent to” the Selected Word Line Limitations (Claims 2-3 and 12-13) • Claim Construction • Ground 1 (Lee): Lee Does Not Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line” (claims 2 and 12) • Ground 1 (Lee): Lee Does Not Disclose or Render the “First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line” (claims 3 and 13) • Ground 4 (Yang): Yang Does Not Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line” (claims 2 and 12) • Ground 4 (Yang): Yang Does Not Disclose or Render the “First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line” (claims 3 and 13)	Slides 31-43

II. Pre-Pulse Signal Limitations

Limitations [1.E.1]-[1.E.4] and [11.B]-[11.E] Require the Application of Three Separate Pre-Pulse Signals to Three Separate Groups of Word Lines During a Pre-Charge Period Where the Third Signal's Voltage Level Is Greater than the Second's, which is Greater than the First's

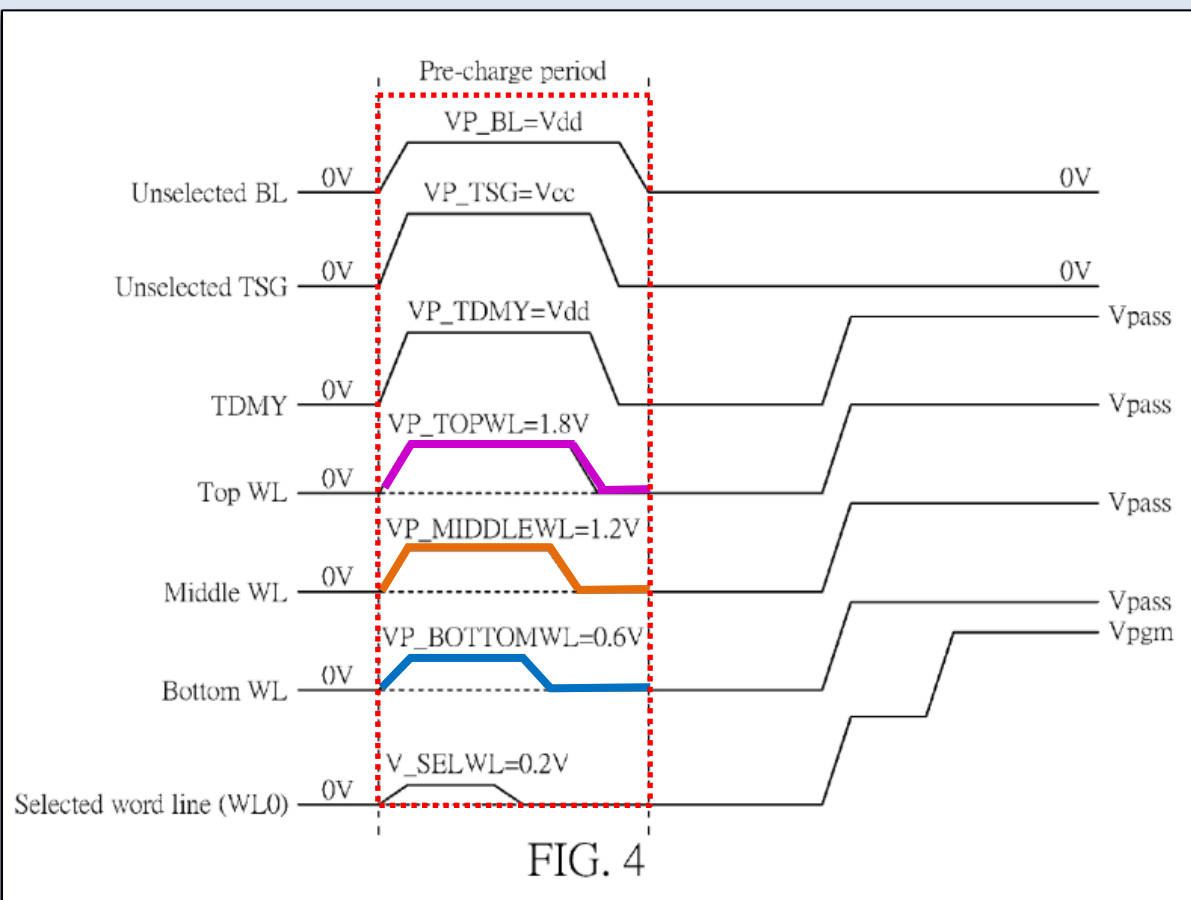
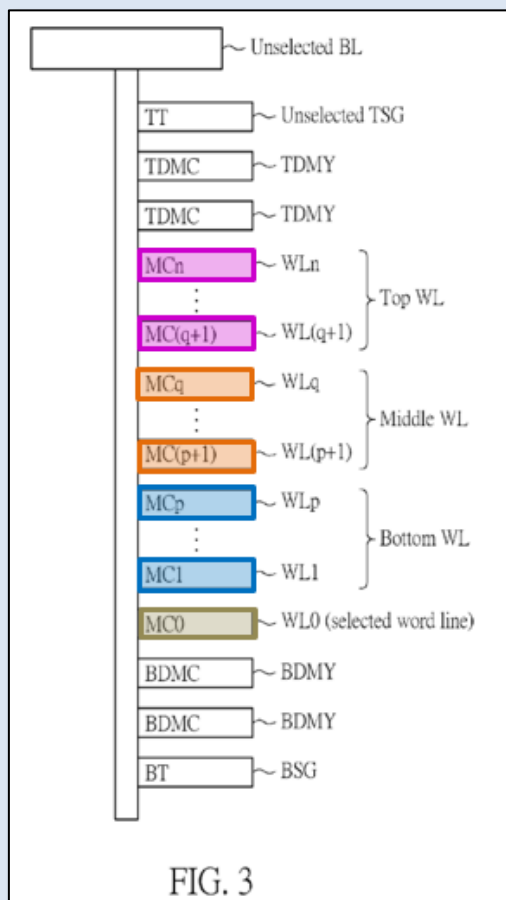
[1.E.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period;

[1.E.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[1.E.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,

[1.E.4] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

To Be a Pre-Pulse Signal During the Pre-Charge Period, the Voltage Level Must at Least Go Up and then Down (or Vice-Versa)



'822 Figs. 3-4.

- The Parties **agree** that a “word line pre-pulse signal” is a form of pulse that will, at minimum, “increase in value and then decrease in value (or vice versa).”

POR, 13-14; Reply, 3.

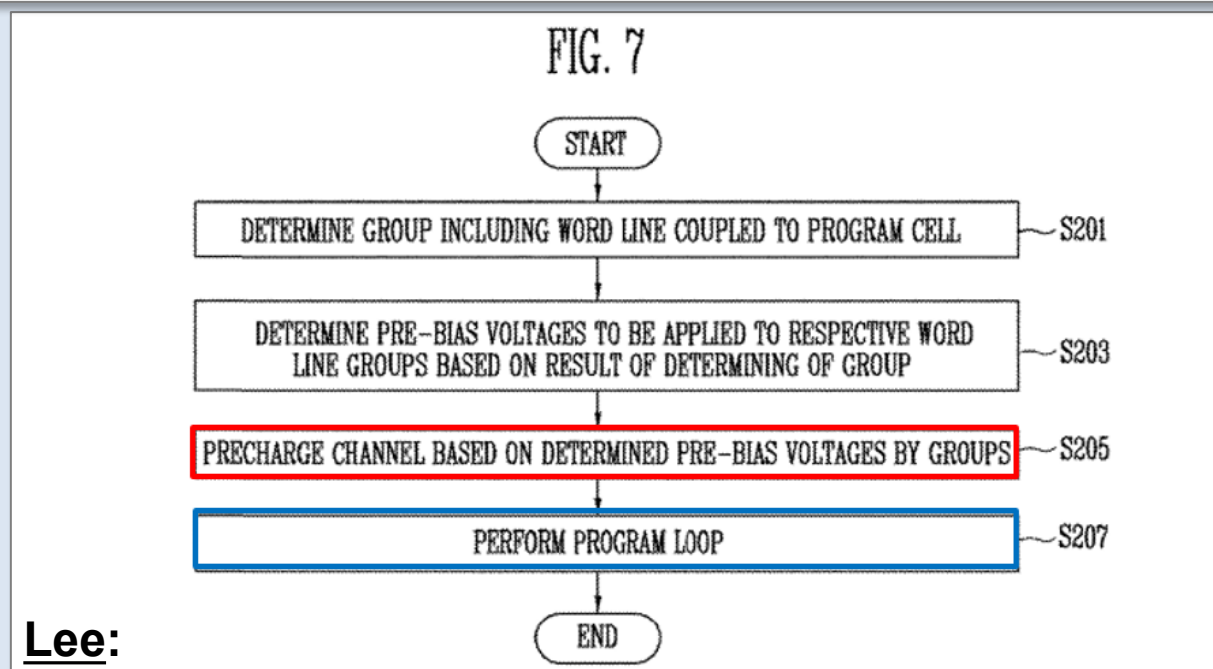
Ground 1: Lee Fails to Disclose or Render Obvious Pre-Pulse Signals During the Pre-Charge Period

Petitioner argues: “A POSITA also would have understood (or considered it obvious) that *Lee’s pre-bias voltages are* supplied in the form of *a ‘pulse.’*”

Pet. 38.

- But Lee discloses applying a single voltage during this time period—not applying a pulse:

Lee: “**After the pre-bias voltage is applied to the respective word lines and the precharge operation is completed, a program voltage may be applied** to the selected word line WL10, and a pass voltage may be applied to unselected word lines WL0 to WL9 and WL11 to WL31. The above-mentioned operation is a program loop for memory cells, and the program loop may be repeatedly performed.”



Lee, 9:7-13, Fig. 7 (showing the “Program Loop” immediately following the “Precharge Channel” step);
POR 31-35; Przybylski, ¶¶82-88; POSR 4-5.

Ground 1: Lee Fails to Disclose or Render Obvious Pre-Pulse Signals During the Pre-Charge Period

Petitioner argues: “[W]hen the ’822 patent was filed, *programming voltages were conventionally provided in the form of a “pulse.”* ... All of the voltages supplied during programming—including both the pre-bias voltages and the later program and pass voltages—*obviously would be supplied as pulses.*”

Pet. 39.

- But “programming voltages” are not “pre-programming” voltages (and thus, not pre-pulse voltages)

Dr. Przybylski: “The *Petition identifies examples of various programming pulses supposedly known in the art, but those identified voltages have no relationship to the waveforms that would be used in a ‘pre-charging’ operation, and serve a different purpose entirely.* See Pet., 39; Liu Dec. ¶¶ 204-205 (citing Aitome (Ex. 1006) at 44, 116-117, 142-143 (discussing ‘applying high-voltage, Vpgm’ for ‘programming pulses’); Cappelletti (Ex. 1008) at 354 (a ‘[p]rogram [p]ulse’ is provided to program a ‘selected cell’)).”

Przybylski ¶87; POR 34-35; POSR 6; see also Przybylski, ¶27 (discussing the difference between pre-charging and programming).

Dr. Przybylski: “The ’822 Patent discusses a novel *pre-charging* process for applying signals to word lines of a three-dimensional non-volatile flash memory device to *mitigate the effects of ‘programming disturb.’* ’822 Patent, 1:52-55. In general, ‘programming disturb’ (or ‘program disturb’) occurs when performing a *program operation on a selected memory cell inadvertently changes the programmed state of adjacent memory cells* that share the same word line or the same bit line as the selected memory cell.”

Przybylski, ¶27 (citing Ex. 1006 at 52, Ex. 1007 at 239, Ex. 1008 at 32-33); POR 1-2.

Ground 1: Lee Fails to Disclose or Render Obvious Pre-Pulse Signals During the Pre-Charge Period

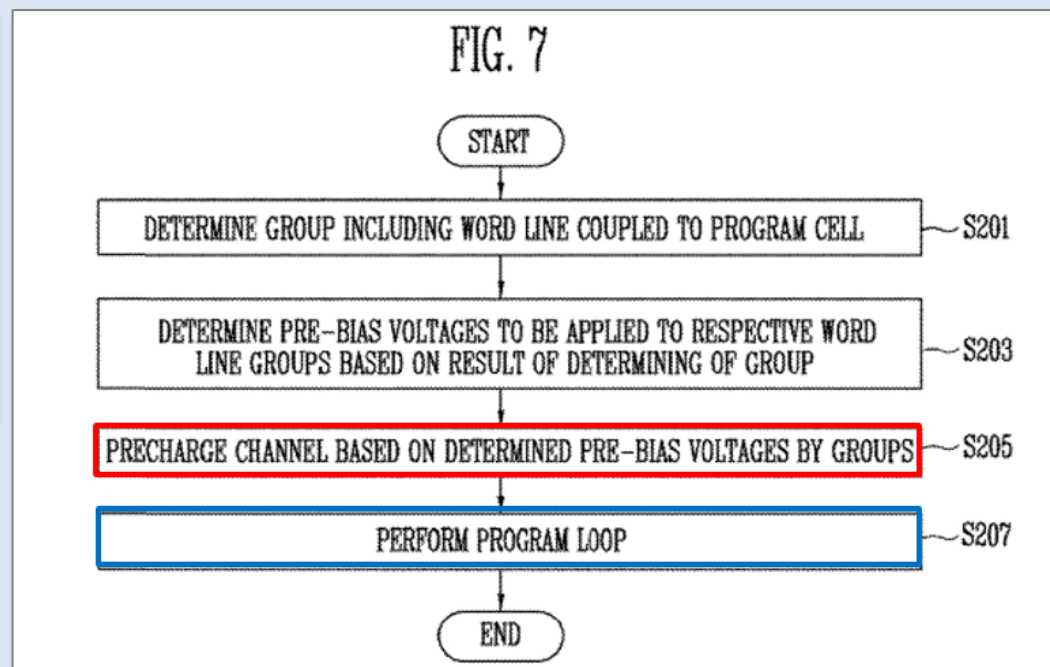
Petitioner argues: “Because Lee (1) supplies its pre-bias voltages in a separate and distinct-in-time step, and (2) the pre-bias voltages differ from the later Vpgm and Vpass voltages, *a POSITA would have understood the pre-bias voltages to be supplied as ‘pulse[s].’*”

Pet. 38-39.

- Lee does not disclose any waveforms or timing characteristics for the pre-bias voltages applied within its system
- Instead, Lee discloses applying one voltage immediately after another

Lee: “**After the pre-bias voltage is applied to the respective word lines and the precharge operation is completed, a program voltage may be applied** to the selected word line WL10, and a pass voltage may be applied to unselected word lines WL0 to WL9 and WL11 to WL31. The above-mentioned operation is a program loop for memory cells, and the program loop may be repeatedly performed.”

Lee, 9:7-13, Fig. 7 (showing the “Program Loop” immediately following the “Precharge Channel” step); POR 31-35; POSR 4-5.



Ground 1: Lee Fails to Disclose or Render Obvious Pre-Pulse Signals During the Pre-Charge Period

- Removing the pre-bias voltage before applying the program voltage is not taught in or suggested by Lee—instead it is contrary to Lee’s teachings of obtaining a “uniform” pre-voltage level

Lee: “Consequently, a **uniform pre-voltage** that is applied to the word lines included in the charge level in the entirety of the cell string may be formed.”

Lee, 7:58-62, 8:25-52, 9:7-13. Przybylski, ¶81; POR 30-35; POSR 5-6.

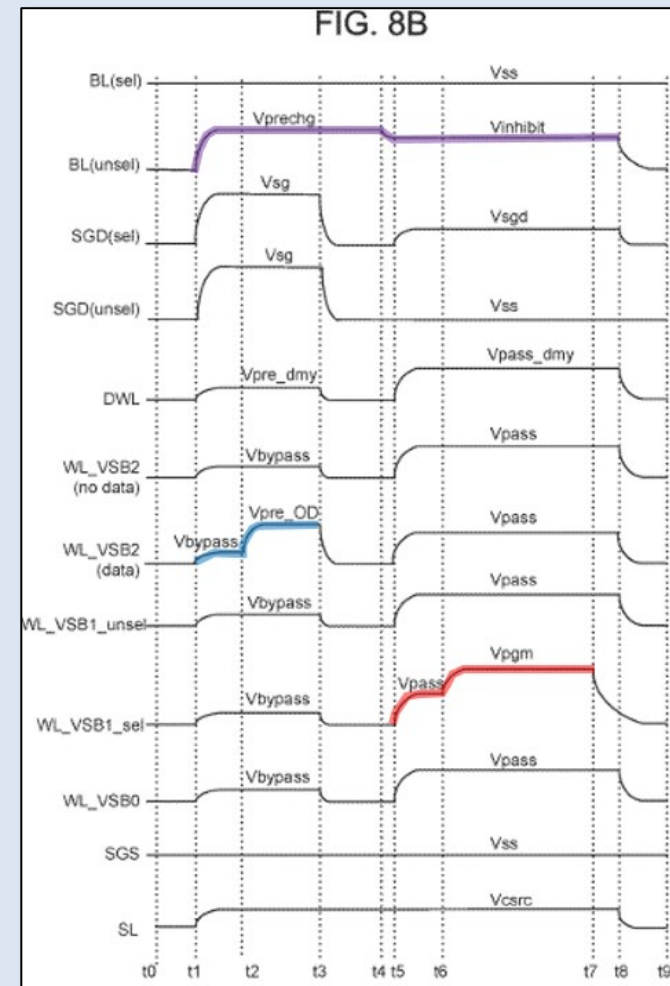
Dr. Przybylski: “The most efficient approach is applying flat signals that remain constant throughout the entire precharge period, followed directly by programming pulses. **Using transient pulses does not create a more “uniform precharge level” in the context of Lees system, and would, at best, introduce time inefficiencies by requiring a longer total time to perform the programming operation.** Accordingly, even assuming that “pulses” were commonly used for subsequent programming operations (e.g., to set the value of a selected memory cell), a POSITA would not have been motivated to modify Lee to use similarly shaped “pulses” for the bias voltages used during a recharging operation.”

Przybylski, ¶87; POR 35; POSR 5-6.

Ground 1: Petitioner's New Reply Arguments Are Improper

Petitioner argues in Reply: “These **voltages will need to be generated—typically by a charge pump**—and then supplied to the appropriate word lines. ... To achieve separate pre-charging and programming as Lee instructs—as opposed to blended pre-charging/programming—a **POSITA would have understood that the voltages applied to Lee's word lines would need to be (or at the very least would obviously be) pulsed.**”

- But Lee does not discuss using a charge pump or specify how it would operate
- The art is replete with examples where no pulse is used to transition from one voltage to another, e.g., Yang:



Reply 6.

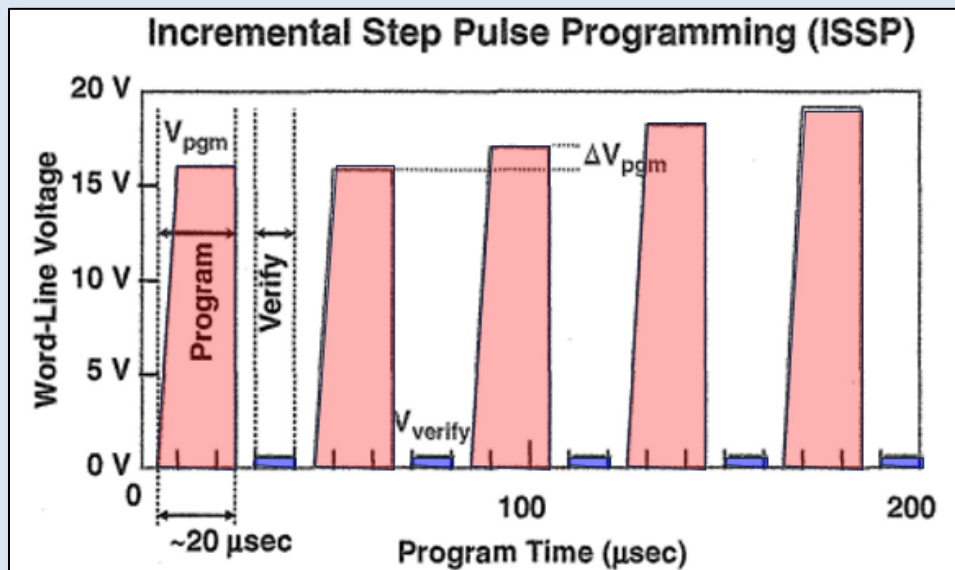
Yang, Fig. 8B; POSR 6-9.

Ground 1: Petitioner's New Reply Arguments Are Improper

Petitioner argues in Reply: “A POSITA also would have understood that *use of well-known pulsed programming voltages requires that the pre-charge voltages also be pulsed.*”

Reply 7-8.

- The new art on which Petitioner relies is about “**programming**” and “**verif[ication]**”—not preprogramming (and thus, not pre-pulse operation):



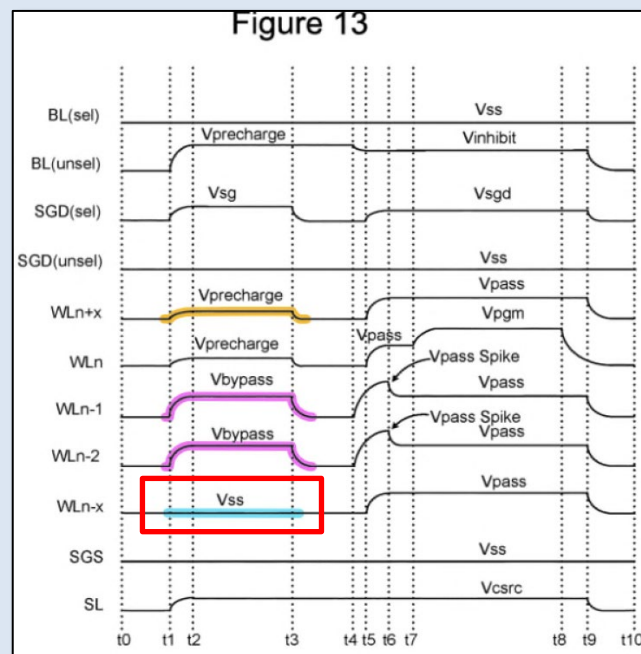
Aritome, 46; see also Micheloni, 225 (describing ISPP); POSR 9-11.

Ground 2: Zhao Does Not Disclose or Render Obvious Applying a “First Word Line Pre-Pulse Signal” (Limitations [1.E.1] and [11.B])

Petitioner argues: “A “first word line pre-pulse signal” (a low non-zero voltage in place of Vss, blue) is applied to a “first group of ... word lines” (the source-side word lines not adjacent to the selected word line, WL_n-x),....”

Reply 7-8.

- Zhao’s flat, unchanging, Vss voltage during the purported precharge period (i.e., the purported “first word line pre-pulse signal” identified by Petitioner) is not a “pulse”:



Zhao: “To prevent the source side of the channels from being pre-charged, *unselected source side word lines receive 0 volts or one or more voltages that are too low to pre-charge* and/or too low to turn on memory cells in a highest data state.”

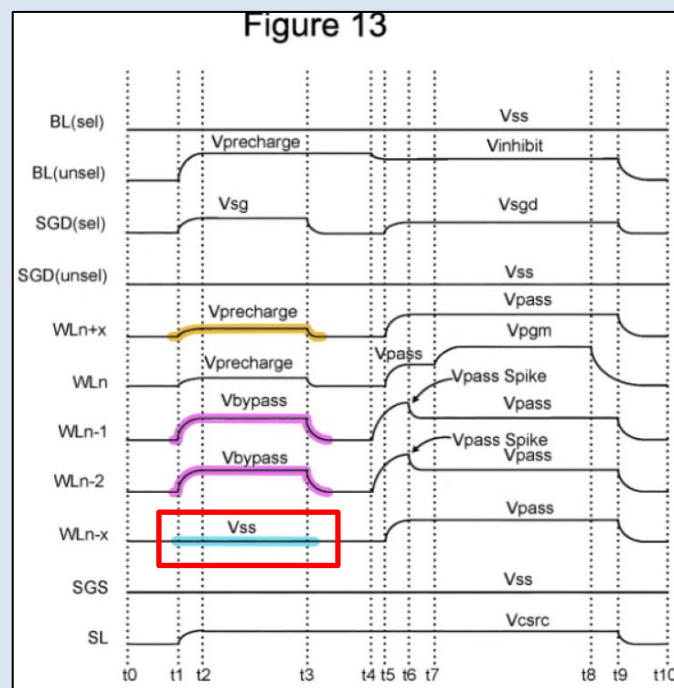
Zhao: “The *remaining source side unselected word lines WL_n-x remain at Vss (e.g., 0 v)*. At time t3, SGD(sel), WL_n+x, WL_n, WL_n-1 and WL_n-2 are all lowered to ground/Vss.”

Ground 2: Petitioner's New Reply Arguments Mischaracterize Zhao

Petitioner argues on Reply: “Per Zhao, ‘*all*’ of its signal lines are ‘at 0 volts (Vss)’ at t0 (before precharging). Zhao, 22:34-38. The lines *are then ‘raised’ to various ‘pre-charge voltage[s]’* between t1-t3. *Id.*, 22:39-49. Period t1-t3 ‘corresponds to the precharging’ ‘steps 650 and 622 of Fig. 10....’ *Id.* **Then, the lines are ‘all lowered to ground/Vss’** after t3 when pre-charging is complete. *Id.*, 22:34-50, 23:5-12; see also Ex. 1020, 66:10-67:19, 68:4-25 (confirming Zhao’s operation).”

Reply 14-15.

- But these teachings expressly exclude **WLn-x** (the alleged first group of word lines), which stays at ground/Vss during the alleged precharge period (e.g., 0 v):



Zhao: “The *remaining source side unselected word lines WLn-x remain at Vss (e.g., 0 v)*. At time t3, SGD(sel), WLn+x, WLn, WLn-1 and WLn-2 are all lowered to ground/Vss.”

Ground 3: POSITA Would Not Have Been Motivated to Combine Zhao and Lee

Petitioner argues: “Zhao applies the same ‘Vprecharge’ ‘pre-charge voltage’ to all unselected word lines on drainside of the currently selected word line. *E.g.*, Zhao, 22:39-49; **Lee, however, highlights a problem with this approach.** According to Lee, in a ‘typical ... precharge operation of an unselected memory string, **a threshold voltage of a memory cell is increased by a resistance component** between the source select transistor and the drain select transistor.’ Lee, 8:25-29.”

Pet 60.

Petitioner argues: “Lee goes on to explain that by **employing different pre-bias voltages with different groups of word lines, it ‘offset[s]’ the ‘effects caused by the resistance component** between the source select transistor and the drain select transistor’ and allows a ‘uniformly formed’ ‘precharge level’ ‘in the entirety of the cell string. Lee, 7:61-62; 8:47-52. This in turn further ‘mitigate[s] [the] program disturb phenomenon....’ *Id.*, 1:52-56; 8:51-52; 15:4-7; Liu, ¶ 340.”

Pet 62.

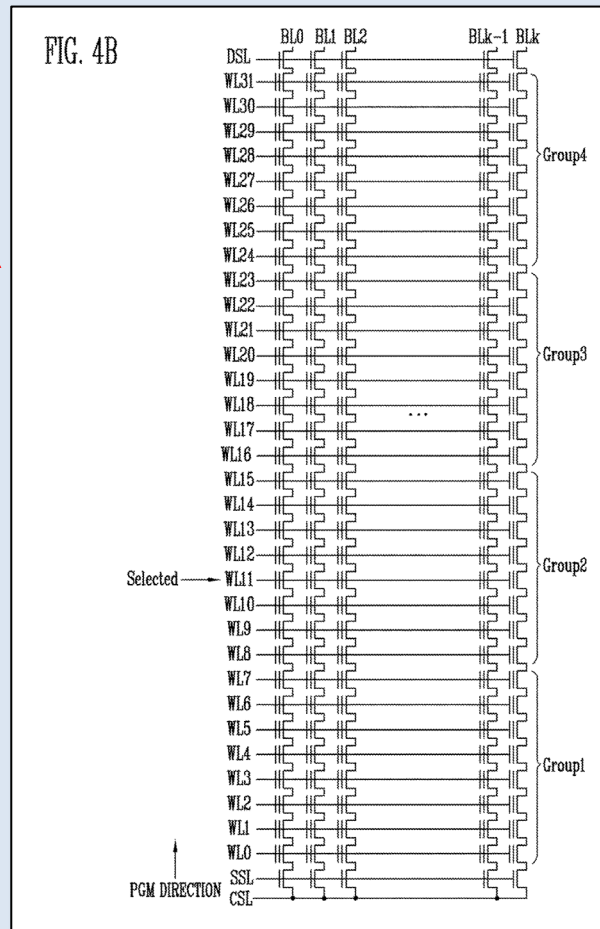
- But Lee does not highlight a problem with Zhao’s approach for multiple reasons
- **First**, Lee is concerned with problems arising from charging operations performed via the common source line, while Zhao instead performs charging from the bit-line (in the opposite direction)
- **Second**, Zhao’s memory cells are not conducting during pre-charge and thus there is no “resistance component” for which to account
- **Third**, even assuming a “resistance” component was present in Zhao’s system during precharge, the proposed modification described in the Petition would not compensate for the effect
- **Fourth**, the absence of a “resistance” component in Zhao arises because Zhao and Lee use different approaches for mitigating program disturb, and a POSITA would not achieve any benefits by applying Lee’s teachings to Zhao in the method suggested in the Petition

POR 44-58; Przybylski, ¶¶111-130; POSR 17-23.

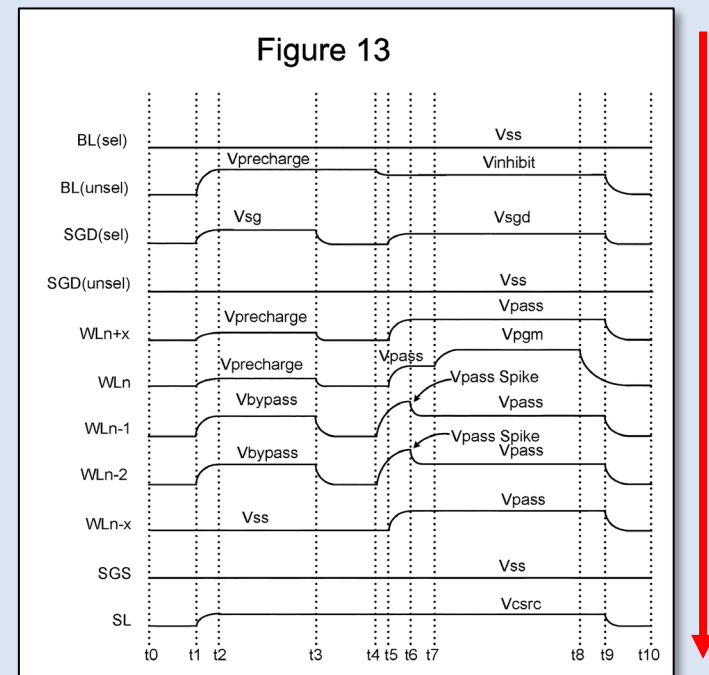
Ground 3: POSITA Would Not Have Been Motivated to Combine Zhao and Lee

- First, Lee is concerned with problems arising from charging operations performed via the common source line, while Zhao instead performs charging from the bit-line (in the opposite direction)

Lee Pre-Charges from the Source Line



Zhao Pre-Charges from the Bit Line



Lee, Fig. 4B, 8:25-37, 8:65-9:3, 9:41-59.
 Zhao, Fig. 13, 19:22-24, 22:39-47.
 POR 48-50; Przybylski, ¶¶115-116.

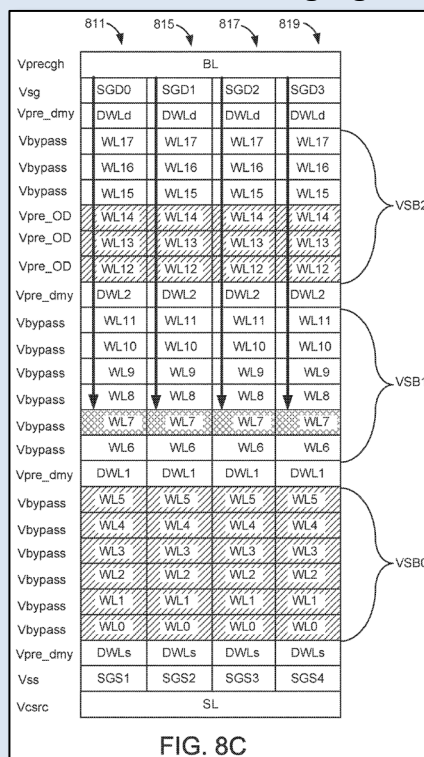
Ground 3: POSITA Would Not Have Been Motivated to Combine Zhao and Lee

- As noted by Yang and Dr. Przybylski, pre-charging from the bit line, source line, or both, involves different approaches with different biasing:

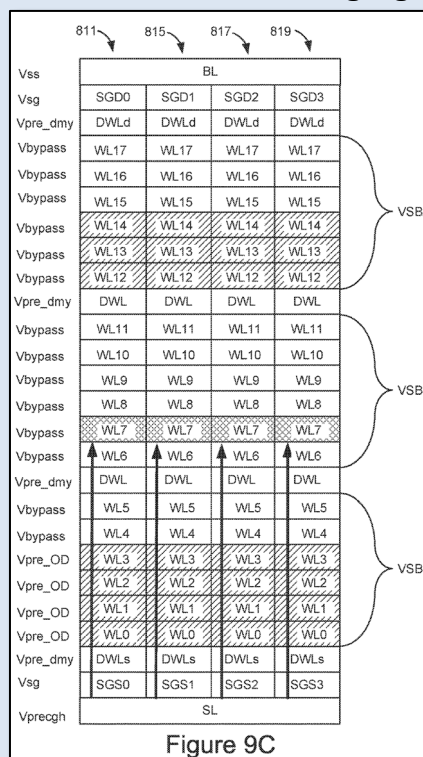
Dr. Przybylski: ***“But the schemes used when charging from the bit line as opposed to the common source can differ substantially, and cannot be ported from one situation to the other without accounting for the effects of applying the pre-charge voltage through a different location and the placement of the memory cells being pre-charged.”*** See, e.g., Yang 1:59-2:19 (distinguishing Fig. 8A-8C embodiments where “pre-charge is from a bit line,” Fig. 9A-9C embodiments where “pre-charge is from a source line,” and Fig. 10A-10C embodiments where “pre-charge is from both a bit line and a source line”).”

Przybylski, ¶¶115; POR 49-50.

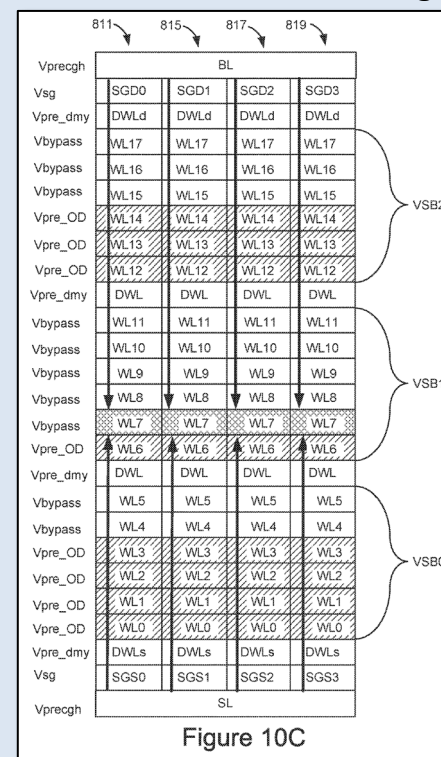
Bit Line Pre-Charging



Source Line Pre-Charging



Bit and Source Line Pre-Charging



Ground 3: POSITA Would Not Have Been Motivated to Combine Zhao and Lee

- **Second**, Zhao’s memory cells are not conducting during pre-charge and thus there is no “resistance component” for which to account
- Lee specifically targets the problem caused by a “resistance component” resulting in a lower voltage on the source select side channel

Lee: “In the case of the typical program operation, **during a precharge operation of an unselected memory string, a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor.** Consequently, the precharge level in a source select side channel is reduced and thus channel boosting is not effectively generated. Therefore, a program disturb occurs.”

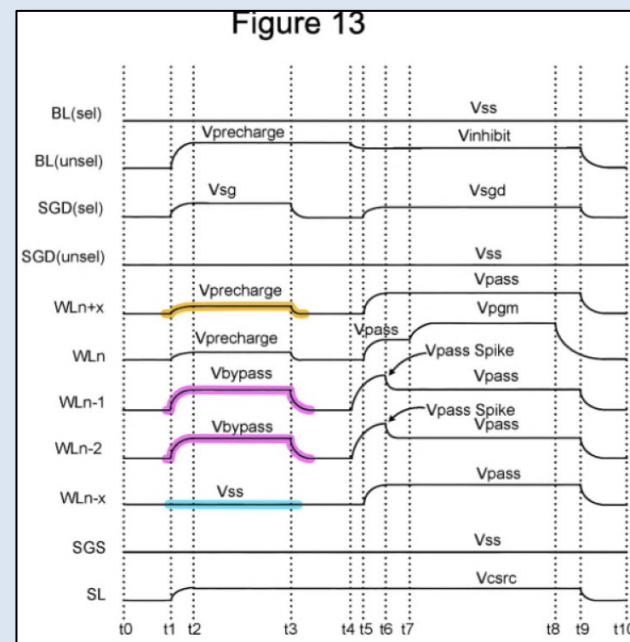
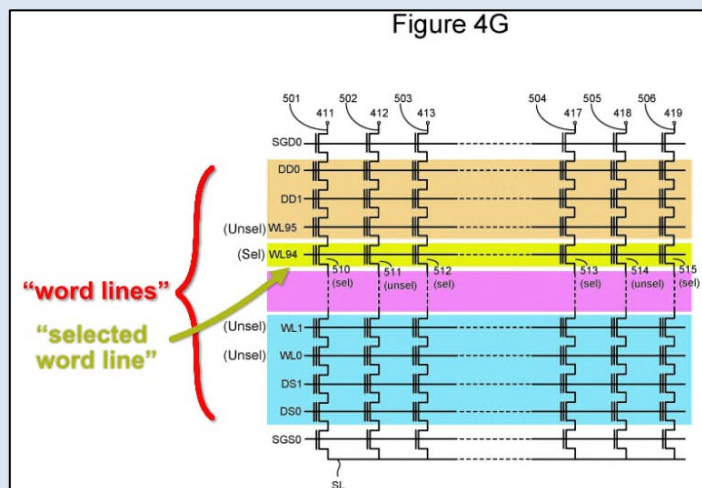
Lee, 8:25-31; POR 50-52; Przybylskill, ¶¶117-119.

- Petitioner cannot rewrite Lee’s disclosures to instead refer to a “chain effect,” which is also absent from Zhao

POR 51-52 n.6; Przybylskill, ¶119; POSR 18, 22-23; Zhao, 11:1-15, Fig. 4.

Ground 3: POSITA Would Not Have Been Motivated to Combine Zhao and Lee

- There is no “resistance component” to account for in Zhao because unlike Lee, the current in $WLn-x$ is off—thus turning off the chain of memory cells and preventing any current flow during the precharge period:



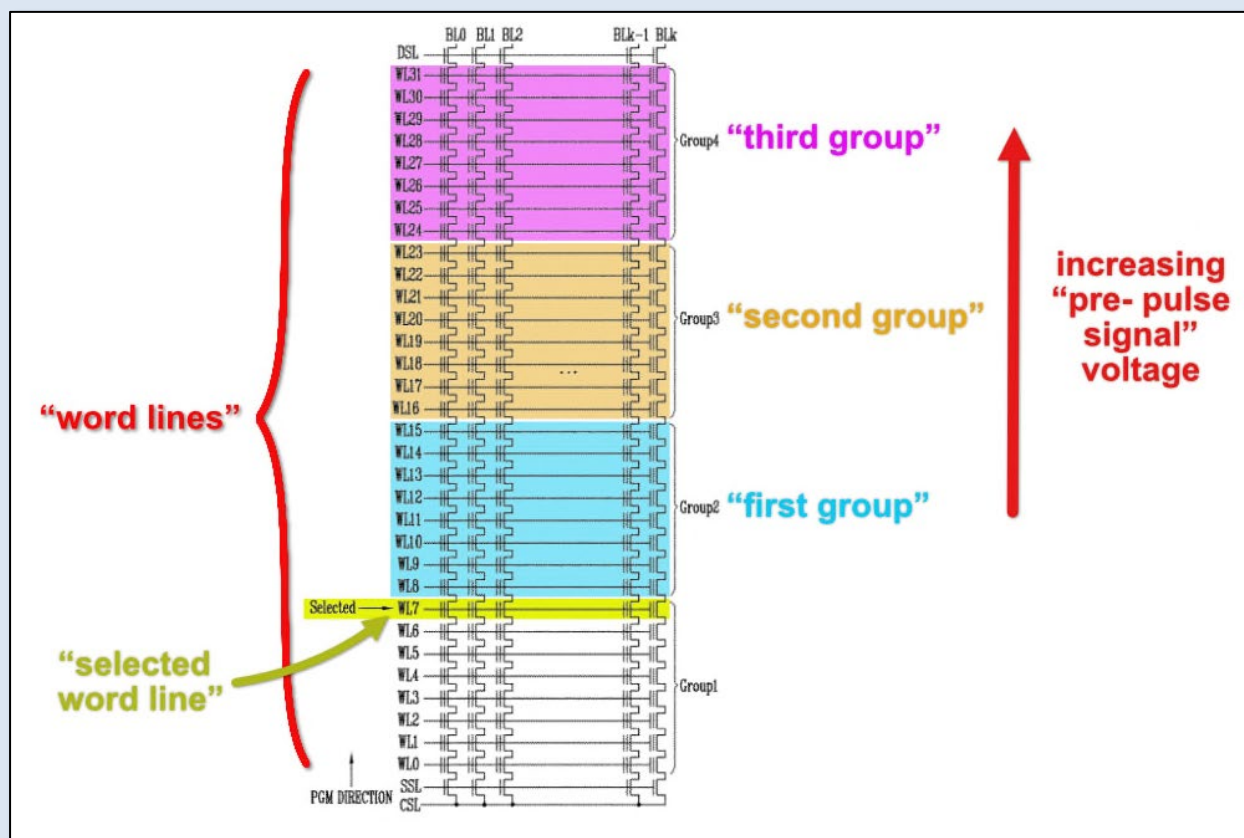
Zhao: “To prevent the source side of the channels from being pre-charged, **unselected source side word lines receive 0 volts or one or more voltages that are too low to pre-charge** and/or too low to turn on memory cells in a highest data state.”

Zhao, Fig. 13, 19:22-24; POR 50-52; Przybylski, ¶¶117-119.

Dr. Przybylski: “But Zhao’s system has several transistors cut off (e.g., **the transistors applied with Vss are turned off and act like open circuits**), thus precluding any current from flowing in the memory string. As a result, the voltage level along the conducting portion of the channel (i.e., the portion of the string formed by the memory cells near the drain select transistor that receive Vprecharge through $WLn+x$) does not vary with a “resistance component” that needs to be offset.”

Ground 3: POSITA Would Not Have Been Motivated to Combine Zhao and Lee

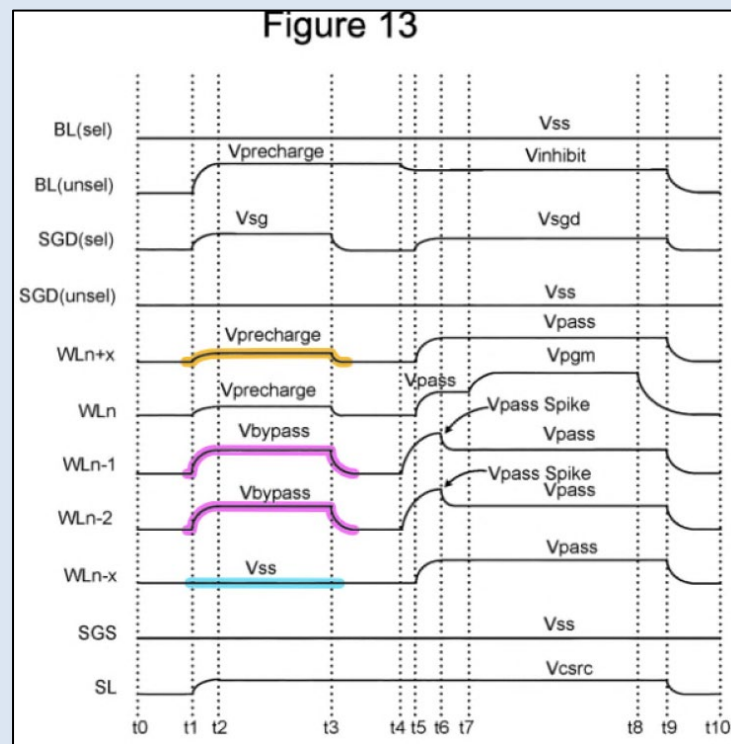
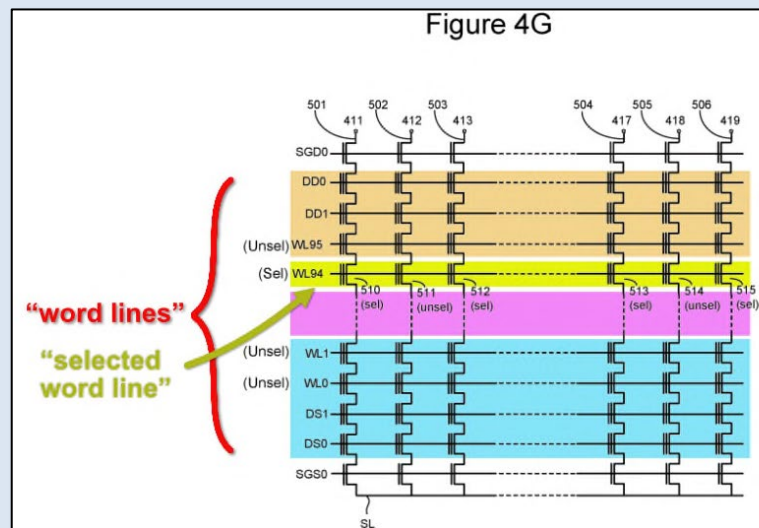
- **Third**, even assuming a “resistance” component was present in Zhao’s system, the proposed modification described in the Petition would not compensate for the effect
- Petitioner alleges that Lee teaches increasing voltages the further away the WLs are from the Source Line (**the further the WLs are from the direction of precharging**):



Pet. 41 (Lee, Fig. 4B).

Ground 3: POSITA Would Not Have Been Motivated to Combine Zhao and Lee

- Applying this concept to Zhao would mean that the voltages farther away from **the bit line** should be increased, but Zhao teaches those voltages should instead be zero or something else “too low to pre-charge”



Pet. 52 (Zhao, Figs. 4G, 13).

Zhao: “To prevent the source side of the channels from being pre-charged, **unselected source side word lines receive 0 volts or one or more voltages that are too low to pre-charge** and/or too low to turn on memory cells in a highest data state.”

Ground 3: POSITA Would Not Have Been Motivated to Combine Zhao and Lee

- **Fourth**, the absence of a “resistance” component in Zhao arises because Zhao and Lee use different approaches for mitigating program disturb, and a POSITA would not achieve any benefits by applying Lee’s teachings to Zhao in the method suggested in the Petition
- **Zhao applies a bypass voltage** to balance out the two sides of the channel and solve for program disturb:

Zhao: “Raising the source side word lines to the **bypass voltage** opens up the channel (e.g. electrically couples the two ends of the channel) so that electrons can migrate (electrical communication) from the source side of the channel to the drain side of the channel, which **reduces or eliminates the voltage differential between the source side** of the channel **and the drain side** of the channel **that may later cause program disturb**.”

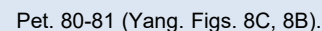
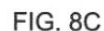
Zhao, 22:65-23:5; POR 55-58; Przybylskill, ¶¶125-130.

- **Lee instead applies a pre-charge voltage to every word line** in the string and increases the voltage the further away from the bit line (the source of pre-charging in Lee)

See Slide 26; Lee, 8:25-52; Przybylskill, ¶127; POR 55-58.

Ground 4: Yang Does Not Disclose or Render Obvious Word Line Pre-Pulse Signals with Incrementally Increasing Voltage Levels (Limitations [1.E.1]-[1.E.4] and [11.B]-[11.E])

Pet. 81-82.

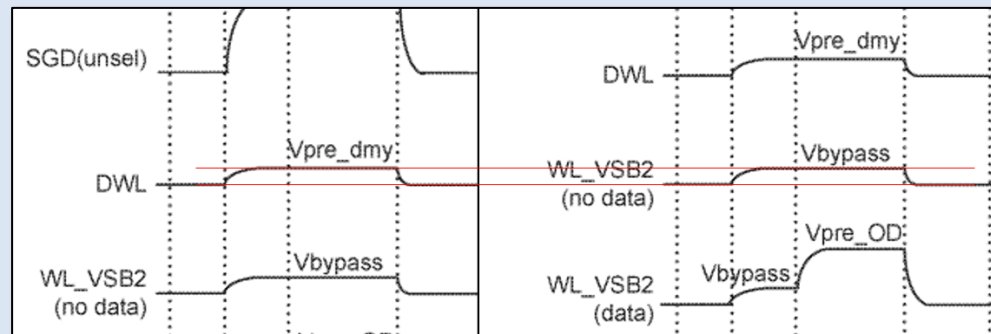


Ground 4: Yang Does Not Disclose or Render Obvious Word Line Pre-Pulse Signals with Incrementally Increasing Voltage Levels (Limitations [1.E.1]-[1.E.4] and [11.B]-[11.E])

Petitioner argues: “Yang applies three different voltage pulses to its various word lines during a pre-charge period: a **“first ... pre-pulse signal”** (Vbypass), a **“second ... pre-pulse signal”** (Vpre_dmy), and a **“third ... pre-pulse signal”** (Vpre_OD). ...”

Pet. 81-82.

- But Yang does not discuss or render obvious that Vpre_dmy is larger or smaller than Vpre_OD and Vbypass
- A specific example voltage (5V) is provided for Vpre_dmy, but not for the other two
- If anything, Vbypass and Vpre_dmy are depicted as the same:



Yang, Fig. 8B.

- And unlike Vpre_OD and Vbypass, Vpre-dmy is applied to “dummy” memory cells, which are used to operate as a pass gate:

Yang: “The **dummy pre-charge voltage** has a magnitude such that the **dummy memory cells will operate as a pass gate.**”

Yang 24:18-27, 12:35-40; POR 63-65; Przybylski, ¶141; POSR 25-26.

III. “Disposed in an Order of Distance from” and “Disposed Adjacent to” the Selected Word Line Limitations

Claims 2 and 12 Require the Three Groups of Word Lines Are “Disposed in an Order of Distance From” the Selected Word Line, and Claims 3 and 13 Require the First Group of Word Lines Are “Disposed Adjacent to” the Selected Word Line

Claim 2: The memory device of claim 1, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are **disposed in an order of distance from the selected word line** of the plurality of word lines.

Claim 12: The method of claim 11, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are **disposed in an order of distance from the selected word line** of the plurality of word lines.

Claim 3: The memory device of claim 1, wherein the first group of the plurality of word lines are **disposed adjacent to the selected word line**, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.

Claim 13: The method of claim 11, wherein the first group of the plurality of word lines are **disposed adjacent to the selected word line**, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.

The Plain Language Requires That the Word Line Groups Be Disposed in Order Based on the Location of the Selected Word Line (Claims 2/12) or Disposed Adjacent to the Location of the Selected Word Line (Claims 3/13)

- The plain language of claims 2 and 12 requires that the word line groups be **disposed** in an order based on the location of the selected word line:

Claims 2/12: “wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are ***disposed in an order of distance from the selected word line*** of the plurality of word lines”

POR 18; Przybylskill, ¶55.

- The plain language of claims 3 and 13 requires the group of word lines to be **disposed** adjacent to the location of the selected word line:

Claims 3/13: “wherein the first group of the plurality of word lines are ***disposed adjacent to the selected word line***”

POR 18; Przybylskill, ¶55.

The Specification Confirms That the Word Line Groups Must Be Disposed in Order Based on the Location of the Selected Word Line (Claims 2/12) or Disposed Adjacent to the Location of the Selected Word Line (Claims 3/13)

- The '822 specification confirms that the word line groups must be *disposed based on the location of the selected word line*

'822 Patent: “As shown in FIG. 3, *suppose the word line WL0 is the selected word line, the word lines WL1 to WLn are divided* into a first group of word lines (Bottom WL), a second group of word lines (Middle WL) and a third group of word lines (Top WL).”

'822, 5:18-22; POR 19; Przybylskill, ¶56.

'822 Patent: “The first group of word lines (Bottom WL) is *between the selected word line* (word line WL0) *and the second group of word lines* (Middle WL).”

'822, 5:24-34; POR 19; Przybylskill, ¶56.

The Extrinsic Evidence Confirms That the Word Line Groups Must Be Disposed in Order Based on the Location of the Selected Word Line (Claims 2/12) or Disposed Adjacent to the Location of the Selected Word Line (Claims 3/13)

- The plain meaning of “disposed” supports the interpretation that the word line groups must be disposed based on the location of the selected word line:

Dictionary: Dispose – “to put in place”

Ex. 2016 (Merriam-Webster’s Dictionary and Thesaurus (2014)); POR 19; Przybylskill, ¶57.

Dictionary: Dispose – “to put in place”

Ex. 2017 (Merriam-Webster’s Collegiate Dictionary (2012)); POR 19; Przybylskill, ¶57.

Dictionary: Dispose – “to place or set in a particular order; arrange”

Ex. 2018 (American Heritage Dictionary of the English Language (2011)); POR 19; Przybylskill, ¶57.

Dictionary: Dispose – “arrange in a particular position”

Ex. 2019 (New Oxford American Dictionary (2010)); POR 19; Przybylskill, ¶57.

- Petitioner correctly recognized that the claimed “groups” will be chosen based on the location of the “currently selected” word line that has been chosen for programming

Petitioner: “The patent’s narrower claims—like dependent claims 2-3 and 12-13—require that the pre-charge voltage applied to a group must increase the further the group is away from the word line currently selected for programming.”

Pet., 2; POR 20; Przybylskill, ¶58.

The Word Line Groups Must Be Disposed in Order Based on the Location of the Selected Word Line (Claims 2/12) or Disposed Adjacent to the Location of the Selected Word Line (Claims 3/13)

Petitioner argues: “[F]or purposes of claim 2, it does not matter when the word lines are divided. *All that matters is that there be “first,” “second,” and “third” “groups” of word lines to which different pre-charge voltages referenced by the claim can be applied* by the claimed ‘control circuitry.’ This is exactly what [the prior art] discloses: its word lines are divided into groups and different pre-charge voltages are applied to those groups.”

Reply 10-11.

- But a POSITA would have understood the claims to mean what they say:

Claims 2/12: “**disposed in an order of distance from the selected word line** of the plurality of word lines”

POSR 2; POR 18; Przybylskill, ¶¶55-59.

Claims 3/13: “**disposed adjacent to the selected word line**”

POSR 2; POR 18; Przybylskill, ¶¶55-59.

- Patent Owner’s construction is also supported by the specification, which Petitioner ignores (*see* Slide 34)

The Word Line Groups Must Be Disposed in Order Based on the Location of the Selected Word Line (Claims 2/12) or Disposed Adjacent to the Location of the Selected Word Line (Claims 3/13)

Petitioner argues: “Claim 2 is an apparatus claim. ‘*[A]pparatus claims cover what a device is, not what a device does.*’ *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469 (Fed. Cir. 1990).”

Reply 10-11.

- But *Hewlett-Packard* and its progeny relate to whether “capability, as opposed to actual operation,” satisfy an apparatus claim:

Federal Circuit: “[W]here claim language recites ‘capability, as opposed to actual operation,’ an apparatus that is ‘reasonably capable’ of performing the claimed functions ‘without significant alterations’ can infringe those claims.”

ParkerVision, Inc. v. Qualcomm Inc., 903 F.3d 1354, 1361-62 (Fed. Cir. 2018) (citation omitted); POSR 3.

- That distinction is not an invitation to disregard claim language:

Federal Circuit: “[W]hat the device **does** (and how it does it) **is highly relevant** to understanding what the device **is**, in the computer/software context.”

INVT SPE LLC v. Int’l Trade Comm’n, 46 F.4th 1361, 1377 (Fed. Cir. 2022); POSR 3.

- Thus, regardless of whether actual operation is necessary, the claimed device must at least be configured to apply word-line pre-pulse signals to groups that are:

“**disposed in an order of distance from the selected word line** of the plurality of word lines” (claims 2/12), or
“**disposed adjacent to the selected word line**” (claims 3/13)

POSR 3.

The Word Line Groups Must Be Disposed in Order Based on the Location of the Selected Word Line (Claims 2/12) or Disposed Adjacent to the Location of the Selected Word Line (Claims 3/13)

Petitioner argues: “[The prior art] does include an example of word line *groups that adjust—via the application of different voltages—as the selected word line changes*.”

Reply 12.

- But the claims do not merely require “groups that adjust ... as the selected word line changes”
- Rather, the claims require groups that are:

POSR 3.

“**disposed in an order of distance from the selected word line** of the plurality of word lines” (claims 2/12), or
“**disposed adjacent to the selected word line**” (claims 3/13)

POSR 3-4.

Ground 1 (Lee): Lee Fails to Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line” (Claims 2 and 12)

Petitioner argues: “Different voltages are applied to different word line groups depending on which word line is selected. ... [A]s the selected word line shifts, different voltages are applied.”

Reply 11-12.

- But Lee’s groups are determined without regard to the location of the selected word line:

Lee: “The control logic in FIG. 4A may *group the thirty-two word lines into two word line groups*. Each of a first word line group Group1 and a second word line group Group2 includes sixteen word lines.”

Lee, 8:4-10, Fig. 4A; POR 37; Przybylskill, ¶92.

Lee: “Referring to FIG. 4B, the control logic may *group the thirty-two word lines into four word line groups*. Each of first to fourth word line groups Group1 to Group4 includes eight word lines.”

Lee, 9:36-40, Fig. 4B; POR 37; Przybylskill, ¶92.

Lee: “For example, as shown in FIG. 4C, *the closer a word line group is to the drain select transistor, the fewer the number of word lines included therein may be.*”

Lee, 10:4-12, Fig. 4C; POR 37; Przybylskill, ¶92.

- Lee discloses that groups are determined *before* a word line is selected for programming—and thus are not “disposed” as required:

Lee: “Referring to FIG. 6, the method of programming the semiconductor memory device according to an embodiment includes *a step S101 of grouping word lines* coupled to memory cells into a plurality of word line groups, and *a step S103 of performing a program operation based on a result of the grouping of the word lines*. At step S101, the number of groups of word lines to be grouped and the number of word lines to be included in each of the word line groups may be determined. *At step S103, based on the determined result of the grouping of the word lines, pre-bias voltages ... may be determined depending on which word line group is the group to which the selected word line belongs*, and then a program operation may be performed.”

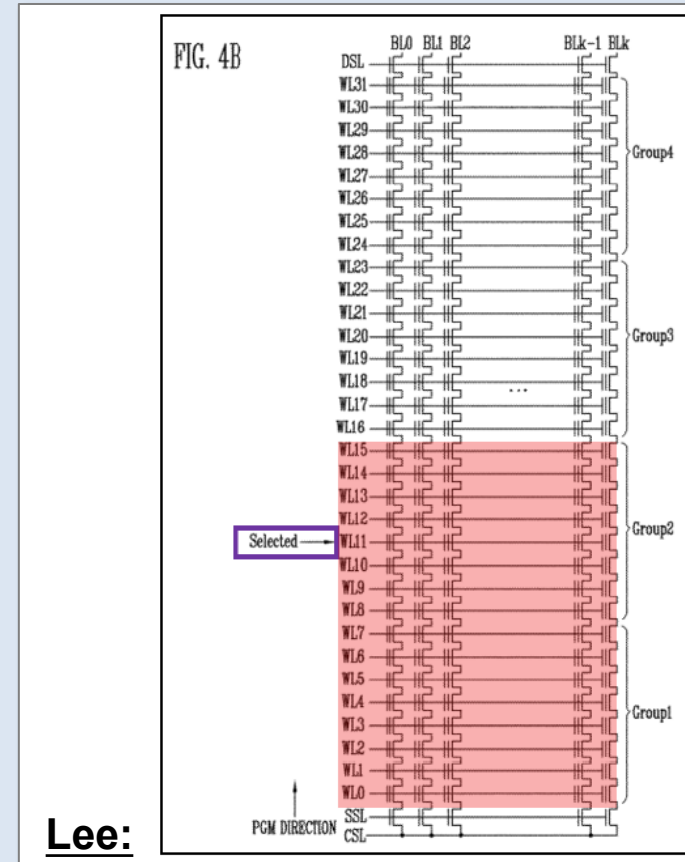
Lee, 10:63-11:9, Fig. 6; POSR 12; POR 37; Przybylskill, ¶92.

Ground 1 (Lee): Lee Fails to Disclose or Render Obvious Groups "Disposed in an Order of Distance from the Selected Word Line" (Claims 2 and 12)

Petitioner argues: "When the selected word line is 'included in the third Group3,' **WL0-WL23 all receive a 'default' voltage** while only WL24-31 ('Group4') receive a 'higher' voltage. ... So, now there only two groups of word lines (the word lines in Group3 above the selected word line, and WL24-31) receiving two different pre-charge voltages."

Reply 12 (discussing Figure 4B of Lee).

- But Lee determines groups **before** selecting a word line and setting voltages (see slide 39)
- Even assuming that this is equivalent to merging existing groups to form a new group, Lee still fails to satisfy the claims:
 - At most, Lee discloses a **single** group disposed based on the location of the selected word line (i.e., the merged group containing the selected word line that receives the default voltage) POSR 13.
 - The resulting system may have fewer than three groups of word lines POSR 13.
 - Moreover, all word lines not receiving that default voltage remain in the same predetermined groups created **prior** to a word line being selected for programming POSR 13.



Lee, Fig. 4B, 9:41-59 (showing that when the selected wordline is inside of Group 2, "a default value is applied to ... Group 2," and "the default value also is applied to ... Group 1" because it is closer to the source select transistor); POSR 12.

Ground 1 (Lee): Lee Fails to Disclose or Render Obvious the “First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line” (Claims 3 and 13)

Petitioner argues: “As explained, the claims do not require continually re-dividing the word lines. And Lee teaches this in any event. *Supra* Section II.A.2.”

Reply 12-13.

- But, again, Lee determines groups *before* selecting a word line and setting voltages (*see* slide 39)
- And as explained for claims 2 and 12, at best Lee teaches only a *single* group disposed based on the location of the selected word line (i.e., *the merged group containing the selected word line*), with **all other groups being predetermined** irrespective of the selected word line’s location
- Accordingly, Lee still fails to teach or suggest “the first group of the plurality of word lines are *disposed adjacent to the selected word line*”
- Petitioner’s Reply does not present any additional arguments for claims 3 and 13, and merely cross-references the arguments for claims 2 and 12

POSR 13.

POSR 13-14.

POSR 13.

Ground 4 (Yang): Yang Fails to Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line” (Claims 2 and 12)

- Yang divides word lines into three groups, none of which depends on the location of the selected word line: (1) “data word line ... that are not programmed;” (2) data word lines that are “programmed;” and (3) “dummy word lines”

Yang: “In step 810, a bypass voltage is applied to data word lines. The bypass voltage may be applied to all data word lines. ... FIG. 8B shows voltages for data word lines ... **that are not programmed**..., data word lines ... **that are programmed**...,”

Yang, 24:1-17; POR 66; Przybylskill, ¶146.

Yang: “In step 812, a dummy pre-charge voltage is applied to **dummy word lines**.”

Yang, 24:18-27; POR 66; Przybylskill, ¶146.

Yang: “In step 814, the voltage on **programmed word lines** in the upper vertical sub-block VSB2 is increased from the bypass voltage to an overdrive voltage after the pre-charge voltage on the bit line stabilizes.”

Yang, 24:28-31; POR 66; Przybylskill, ¶146.

- “Dummy” word lines are based on where dummy memory cell transistors have been placed during the manufacturing process

POR 66; Przybylskill, ¶146.

- As shown above, data word lines are grouped based on whether the corresponding memory cells have been programmed or not

POR 66; Przybylskill, ¶146.

- Petitioner’s Reply fails to address this limitation, conceding that Yang fails***

POSR 27.

Ground 4 (Yang): Yang Fails to Disclose or Render Obvious the “First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line” (Claims 3 and 13)

- Again, Yang divides word lines into three groups, none of which depends on the location of the selected word line: (1) “data word line ... that are not programmed;” (2) data word lines that are “programmed;” and (3) “dummy word lines”

Yang, 24:1-31; POR 66, 68; Przybylskill, ¶¶146, 150.

- Yang does not disclose or render obvious that a first group is disposed adjacent to a selected word line

POR 68; Przybylskill, ¶150.

- *Petitioner’s Reply fails to address this limitation, conceding that Yang fails*

POSR 27.