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Paper 27
Date: October 7, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00795
Patent 11,501,822 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Micron Technology, Inc. ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1–9 and 11–19 of U.S. Patent No. 11,501,822 B2 (Ex. 1001, "the '822 patent"). Paper 1 ("Pet."). Yangtze Memory Technologies Company, Ltd. ("Patent Owner") filed a Preliminary Response to the Petition. Paper 8 ("Prelim. Resp."). The Petition is supported by a declaration from Dr. David Kuan-Yu Liu. Ex. 1003 ("Liu Dec."). The Preliminary Response is supported by a declaration by Dr. Steven A. Przybylski. Ex. 2001 ("Przybylski Dec."). We instituted *inter partes* review on all asserted claims and grounds. Paper 9 (Inst. Dec.).

Patent Owner filed a Response, accompanied by a declaration of Dr. Przybylski. Paper 12 ("PO Resp."); Ex. 2011 ("Przybylski Supp. Dec."). Petitioner filed a Reply, accompanied by a Supplemental Declaration of Dr. Liu and a transcript of a deposition of Dr. Przybylski. Paper 14 ("Pet. Reply"), Ex. 1021 ("Liu Supp. Dec."); Ex. 1020 ("Przybylski Dep."). Patent Owner filed a Sur-reply. Paper 15 ("PO Sur-reply"). We held an Oral Hearing with the parties on July 14, 2025, and a transcript was entered into the record. Paper 23 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner has shown by a preponderance of the evidence that claims 1–9 and 11–19 of the '822 patent are unpatentable.

B. Real Parties in Interest

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 4. Patent Owner identifies itself as a real party-in-interest. Paper 5, 2.

C. Related Matters

The parties represent that the ’822 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 5, 2; Pet. 4.

Petitioner also filed IPRs challenging other patents asserted in the district court case, namely U.S. Patent Nos. 10,658,378 (IPR2024-00788), 10,861,872 (IPR2024-00789), 10,868,031 (IPR2024-00790), 10,937,806 (IPR2024-00791), 10,950,623 (IPR2024-00794), 11,468,957 (IPR2024–00792), and 11,600,342 (IPR2024-00793). Pet. 4.

D. The ’822 Patent

The ’822 patent is titled “Non-Volatile Memory Device and Control Method.” Ex. 1001, code (54). The ’822 patent issued from Application No. 16/709,944, filed on December 11, 2019, and claims priority via a continuation application to PCT/CN/2019/112409, filed on October 22, 2019. *Id.* at code (63).

The ’822 patent relates to “a non-volatile memory device and a control method capable of applying word line pre-pulse signals with different voltage levels and reducing programming disturb.” *Id.* at 1:15–19.

E. Illustrative Claim

Claim 1 is illustrative, and recites as follows:[1]

[1.Pre] A memory device, comprising:

[1.A] a plurality of memory strings;

[1.B] a bit line connected to a first memory string of the plurality of memory strings;

[1.C] a select gate line connected to the first memory string of the plurality of memory strings;

[1.D] a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string; and

[1.E] a control circuit configured to:

[1.E.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period;

[1.E.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[1.E.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,

[1.E.4] wherein a voltage level of the second word line prepulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

[1] Bracketed organization added as per the Petition.

F. Evidence

Petitioner relies on the following patent document evidence.

Name	Patent Document	Exhibit
Lee	US 10,121,529 B2	1004
Zhao et al. ("Zhao")	US 10,643,718 B2	1005
Yang	US 10,726,920 B2	1010

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–9 and 11–19 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3, 6, 11–13	103[2]	Lee
1, 4–7, 9, 11, 14–16, 18–19	103	Zhao
1–9, 11–19	103	Zhao, Lee
1–7, 9, 11–16, 18–19	103	Yang

II. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, "would have been obvious at the time the invention was made to a person having ordinary skill in the art [to which said subject matter pertains]." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level

[2] Petitioner asserts, and we accept based on the complete trial record, that AIA 35 U.S.C. 103 applies to the '822 patent. *See* Pet. 19.

of ordinary skill in the art; and (4) objective evidence of non-obviousness.[3] *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art ("POSITA") at the critical time

> would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

Pet. 18 (citing Ex. 1003 ¶¶ 35–38). Petitioner further asserts that a POSITA "would have been aware of and generally knowledgeable about NAND memory's structure, its component parts, how it operates, and how it is controlled. *Id.* (citing Ex. 1003 ¶ 38). Patent Owner does not object to this assertion. PO Resp. 12. We adopt Petitioner's proposed level of ordinary skill, as it appears to be consistent with the specification of the '822 patent and the prior art of record.

C. Claim Construction

In an *inter partes* review, we construe a patent claim "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)." 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their "ordinary and customary meaning," which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire

[3] Neither party presented evidence or arguments regarding objective evidence of non-obviousness during trial.

patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Here, Petitioner states the claims can be afforded their plain and ordinary meaning and no further claim construction is required. Pet. 18. Patent Owner argues for construction of the following terms: (1) "word line pre-pulse signal" and (2) "disposed in an order of distance from the selected word line"/"disposed adjacent to the selected word line." PO Resp. 13–20.

1. Word line pre-pulse signal

Patent Owner argues that such a signal "must increase in value and then decrease in value (or vice versa)." PO Resp. 13; PO Sur-Reply 1. Petitioner agrees with this construction. Pet. Reply. 3. Patent Owner further argues that the pre-pulse signal "prepares the word line before the programming step." PO Resp. 13. We agree that Petitioner applies its teachings with the same understanding of "pre-pulse signal" as Patent Owner. *See, e.g.*, Pet. 38–39 (asserting that Lee teaches, or that that Lee would make obvious, pre-bias signals applied as pulses).

Because both parties agree that a pre-pulse signal "must increase in value and then decrease in value (or vice versa)," and apply this construction in their assertions and arguments, no dispute as to the meaning of this phrase exists in a manner that would affect the outcome of this decision. Therefore, we do not need to determine a particular construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.,* 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

2. are disposed in an order of distance from the selected word line/disposed adjacent to the selected word line

With respect to claims 2, 3, 12, and 13, Patent Owner argues that the "disposed . . . [from/to] the selected word line" limitations require a disposed object to be "put in place" or "arranged in a particular position" based on the selected word line. PO Resp. 18–19 (citing dictionary definitions of "disposed" in Exs. 2016–2019); PO Sur-Reply 1–2. Patent Owner argues that the '822 patent states that once a wordline is selected, "word lines disposed between the selected word line and a top select gate TSG can be divided into multiple groups." *Id.* at 2.

Petitioner argues that claims 2 and 3 are apparatus claims that cover what the claims are, not what the claims do. Pet. Reply 10 (citing *Hewlett-Packard Co. v. Bausch & Lomb Inc,* 909 F.2d 1464, 1469 (Fed. Cir. 1990)), 12–13. With that understanding, Petitioner argues that the claims require only that there "***be*** 'first,' second,' and 'third' groups of word lines." *Id.* at 10–11. Petitioner further argues that method claims 12 and 13 do not require that the claimed groups be formed at any particular time, or that they be re-formed when a different word line is selected. *Id.* at 11–13. Petitioner argues that the '822 patent's sole example has no discussion of the initial grouping or mention of any regrouping. *Id.* at 11 (citing Ex. 1001, 4:66–5:1, Fig. 3). Petitioner further argues that it is unnecessary to resolve this construction because Lee teaches these limitations.

Regardless of Lee's teachings, we must resolve this construction to determine the patentability of claims 2, 3, 12, and 13 over the Yang ground that does not include Lee. Neither party advanced construction of these terms prior to institution, and we did not construe them in our Decision on Institution. *See* Inst. Dec. 6–8.

We agree with Patent Owner's construction of "disposed." Beginning with the plain language of the claims, each claim states "disposed." Patent Owner provides dictionary definitions for "disposed," which is described as a verb. *See, e.g.*, Ex. 2016, 3. When described as a verb in these definitions, "disposed" is the action of the actor; i.e., "the chief disposed his attendants in a circle" (Ex. 2019, 3); "She disposed of her estate among her heirs" (Ex. 2018, 3); "disposed of the matter efficiently" (Ex. 2017, 3); "troops disposed for withdrawal" (Ex. 2016, 3). Petitioner offers no contrary definition from either the Specification or any extrinsic source for that term. We agree with Patent Owner's construction of "disposed" as "put in place" or "arranged in a particular position."

Nevertheless, the construction of "disposed" does not resolve the controversy over the language of claims 2, 3, 12, and 13. The claims recite "are disposed." For example, claim 2 recites, "wherein the [first through third groups] of the plurality of word lines are disposed in an order of distance from the selected word line." Under Patent Owner's construction, this reads as, "wherein the [first through third groups] of the plurality of word lines *are arranged in a particular position* in an order of distance from the selected word line." But claim 2 does not recite that the word lines are arranged "based on" the selected word line, or that the arrangement occurs only after a word line is selected, as argued by Patent Owner. We agree with Petitioner that the express language of claim 2 does not recite any limitation as to how or when the groups of word lines are disposed.

Both parties point to the same language in the '822 patent Specification in support of their position: "the word lines disposed between the selected word line and the top select gate TSG can be divided into multiple groups of the word lines." PO Sur-Reply 2 (citing Pet. Reply 11

(citing Ex. 1001, 4:66–5:1)). We agree with both parties that the claim requires the recited arrangement to exist, at some point. But we determine that none of claims 2, 3, 12, or 13 require a step of arrangement, or an action to change the arrangement of grouped word lines.

D. Obviousness over Lee

Petitioner asserts that claims 1–3, 6, and 11–13 are unpatentable under 35 U.S.C. § 103 as obvious over Lee. Pet. 26. Patent Owner argues against the assertion. PO Resp. 28–39.

Upon consideration of Petitioner's explanations and the totality of evidence in this current record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3, 6, and 11–13 are unpatentable under 35 U.S.C. § 103 as obvious over Lee.

1. Lee

Lee is titled "Semiconductor Memory Device For Applying Different Bias Voltages and Operating Method Thereof." Ex. 1004, code (54). Lee relates to a semiconductor memory device in which pre-bias voltages are applied to a plurality of word lines to precharge channel regions of the memory cells. *Id.* at code (57). Different pre-bias voltages are applied depending on the relative positions of the word lines. *Id.* Lee applies pre-bias voltages during a "precharging step." *Id.* at 8:15–18.

2. Analysis of Claim 1

We begin our analysis of Petitioner's obviousness contentions with Petitioner's assertions as to claim 1. Patent Owner does not specifically argue against Petitioner's assertions for limitations [1.Pre]–[1.D]. PO Resp. 28. However, we draw no inference therefrom and Petitioner bears the burden of persuasion.

> *[1.Pre]–[1.D] A memory device, comprising: a plurality of memory strings; a bit line connected to a first memory string of the plurality of memory strings; a select gate line connected to the first memory string of the plurality of memory strings; a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string;*

Petitioner asserts that limitations [1.Pre]–[1.D] are taught by Lee in the following manner. Petitioner points to Lee's semiconductor memory device 100 having a memory cell array with memory cells arranged in a plurality of cell strings. Pet. 27–28 (citing Ex. 1004, 5:60–61, 6:12–15, Fig. 3). Petitioner points to Lee's description that each of these cell strings are coupled to a bit line; for example, Lee's bit line "BLk+1" coupled to an unselected string in Figure 3. *Id.* at 28–29 (citing Ex. 1004, 7:28–36, Fig. 3). Petitioner points to Lee's description that each cell string is coupled to a "drain select line DSL," which Petitioner characterizes as the claimed "select gate line." *Id.* at 29–30 (citing Ex. 1004, 7:37–43, Fig. 3). Petitioner points to Lee's description that its memory cells are arranged into "pages" and are "coupled in common to a single word line." *Id.* at 30–31 (citing Ex. 1004, 5:64–6:7, 7:30–45, Fig. 3). Petitioner further asserts that during programming of a particular cell, that cell's associated bit line and word line are "selected." *Id.* at 31–32 (citing Ex. 1004, 7:28–34, 8:18–24, Fig .4).

Upon review of Lee, we determine that Petitioner's uncontested assertions are supported by the record.

> *[1.E] a control circuit configured to: [1.E.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period; [1.E.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and [1.E.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to*

a third group of the plurality of word lines during the pre-charge period,

Petitioner asserts that Lee teaches application of the three claimed word line pre-pulse signals during a pre-charge period. Pet. 33. Petitioner points to Lee's description of four "groups" of word lines, each group containing eight word lines. *Id.* at 33–34 (citing Ex. 1004, 7:58–61, 9:36–40). Petitioner points to Lee's statement that "different pre-bias voltages may be applied to the respective groups during a precharge operation of the cell string." *Id.* at 35 (citing Ex. 1004, 7:58–61). Petitioner asserts that these voltages are "pre-pulses" applied during a pre-charge period that occurs before programming. *Id.* at 37 (citing Ex. 1:62–2:1, 2:30–32, 2:59–62, 9:7–11).

a) Does Lee describe pre-charging in the form of a pulse?

Petitioner first asserts that Lee supplies such voltages in the form of a "pulse" because (1) they are supplied in a distinct-in-time step and (2) differ from later-applied Vpgm and Vpass voltages. Pet. 38–39 (citing Ex. 1003 ¶¶ 197–203).

Patent Owner argues that Lee does not disclose the claimed "word line pre-pulse signals" because Lee does not provide its pre-pulse signals in the form of pulses because Lee's signal does not increase and then decrease in value. PO Resp. 28–34. Patent Owner argues that "Lee does not disclose any waveforms or timing characteristics for the voltages applied within its system, and Lee's stated goal of creating a 'uniform' pre-charge level would suggest that pre-bias voltages are applied as a single, flat, value followed immediately by programming voltages, rather than using a pulse." *Id.* at 31–32 (citing Ex. 1004, 7:58–62, 9:7–13, Fig. 7; Ex. 2001 ¶ 82).

Dr. Liu testifies that a POSITA would have understood that Lee's "on-off pre-bias voltages," which are supplied during the pre-charging period and then removed before the programming voltages are supplied, are by definition a pulse. Ex. 1003 ¶ 203 (explaining that "Lee (1) supplies its pre-bias voltages in a separate and distinct in time step, and (2) the pre-bias voltages differ from the later Vpgm and Vpass voltages"). Dr. Liu further attests that a pulse is a necessary form of voltage application because voltages do not change instantaneously. Ex. 1021 ¶¶ 11–13. Dr. Liu adds, "Lee even explains that 'program' and 'pass' voltages are not applied to Lee's word lines until 'after … the precharge operation is completed.'" Ex. 1021 ¶ 18 (citing Ex. 1004, 9:7–14). Dr. Liu attests that Lee "is plainly referring to pulsed operation: pre-charge is not 'completed' until the word lines are permitted to return to their original value (i.e., ground)." *Id.* Dr. Liu explains that word lines would return to an original value at the end of its step to avoid blending the separate steps. *Id.*

Although Petitioner argues that Lee's pre-charging operation is "complete" prior to the programming operation, Lee does not indicate that the pre-charging operation includes any period of decreased voltage between the two operations. Dr. Przybylski states that any requirement that the pre-charging and programming operations be distinct does not necessitate that the voltage be lowered to the original value between the two operations. Ex. 2001 ¶ 84. Dr. Przybylski points to the lack of any support in Lee for Dr. Liu's statement that Lee's pre-bias voltages are removed prior to commencing the program loop. *Id.* ¶ 85. Dr. Przybylski points to Lee's depiction, in Figure 7, that the channel pre-charging step occurs immediately prior to the programming period; i.e., without an interval in which voltages are removed. *Id.*

Dr. Przybylski further points to Lee's silence on the shape of the voltages in the pre-charging operation as permitting a range of applied voltage shapes. Ex. 2011 ¶ 82. For example, Dr. Przybylski states that many other non-pulse signals (e.g., a flat signal followed by a ramping voltage or a staircase function) may occur in a distinct time step and have a value that differs from a later voltage. *Id.* Patent Owner points to successive voltages being applied in a non-pulsed, staircase form in Yang as illustrating that a pulse is not the only way of applying successive voltages in analogous systems. PO Sur-Reply 8–9 (citing Ex. 1010, Fig. 8). Dr. Przybylski further points to Lee's statement that the purpose of Lee's pre-charging is to create a "uniform precharge level." *Id.* In Dr. Przybylski's view, applying a uniform precharge level would be inconsistent with using a pulse for pre-charging. *Id.* Petitioner's argument that Dr. Przybylski's attestation of non-pulse-shaped operations must be disregarded as unsupported by evidence is not persuasive because Patent Owner presents some support for non-pulse shaped operations in Figure 8 of Yang, and because Petitioner (who bears the burden of persuasion) also lacks supporting evidence of the shape of pre-charging voltages. Pet. Reply 10.

Based upon the above evidence and in light of the complete trial record, we determine that the distinct nature of Lee's pre-charging operation does not indicate that Lee applies a pulse during that operation. Although Dr. Liu attests that a pre-charging operation requires an on-off pulse to be a complete operation, Dr. Przybylski attests to non-pulse operations that would also provide a complete pre-charging operation. In the absence of any detail in Lee on the shapes of its applied voltages, Dr. Przybylski's non-pulse operations reasonably explain how Lee's pre-charging may occur.

Therefore, Petitioner has not shown that Lee's pre-charging operation would be understood by a person having ordinary skill in the art as being in the form of a pulse because it is a distinct operation.

Petitioner also argues that NAND memory necessarily has a "ramp-up" period when voltage is applied, and a decay when voltage is removed because applied potentials do not instantaneously change. Pet. Reply 5. However, the rate at which voltages change is not in question. Whether instantaneous or slow, Petitioner has not shown that Lee's transition from pre-charging to programming involves a decrease at the end of the pre-charging period so as to form a pulse. *See* Sur-reply 7. As Petitioner admits:

> In all cases, the pre-charge voltage is significantly lower than the programming voltage. The programming voltage is significantly higher than the pre-charge voltage. That's the case in all of the prior art that has signal timing diagrams in it. It's the case in Zhao, it's the case in Yang.

Tr. 26:4–7. Patent Owner points out that "less 'ramp-up' is needed if the pre-charge voltage is maintained until the program operation begins." PO Sur-reply 7. Because Petitioner admits that the voltage must increase "significantly" at the transition from pre-charging to programming, we are not persuaded that such a transition must first involve a decrease in voltage before increasing to the higher programming voltage.

Petitioner also argues that if a pre-charge operation is not supplied as a pulse, unwanted programming would occur due either to poor pre-charging or disruption of program voltages. Pet. Reply 1. Relying on Dr. Liu's testimony, Petitioner argues that "pre-charging [would] continue for some indeterminant period while programming voltages were applied." *Id.* at 6 (citing Ex. 1021 ¶¶ 13–20). Again, Petitioner's admission that programming

voltages are significantly higher than pre-charging voltages undermines its argument. Lee describes sequential pre-charging and programming operations. PO Sur-reply 5–6 (stating, "pre-bias voltages are followed immediately by programming voltages," citing Ex. 2011 ¶¶ 85–86; Ex. 1004, 9:7–13). Petitioner does not explain persuasively why proceeding directly from precharge voltage to programming voltage would be more disruptive than detouring to zero voltage in the midst of that transition.

Petitioner further argues that Lee's components would be understood to supply voltages in the form of pulses. Pet. Reply 7. Petitioner points to Lee's "shared voltage generation unit 150" as generating both its pre-charge and its programming voltages. *Id.* (citing Ex. 1004, 7:13–19). Petitioner argues that Lee's voltage generation unit and its address components supply voltages to its word lines, and that these components are known to supply voltages in the form of pulses. *Id.* (citing Ex. 1021 ¶¶ 21–29, 36). Dr. Liu attests that both a voltage generation unit and an address component use charge pumps for supplying voltages. Ex. 1021 ¶ 23 (citing Ex. 1008 ("Cappalletti"), 259). Petitioner argues that because Lee uses the same type of unit to generate its pre-charging and programming voltages, they would obviously have the same form. Pet. Reply 7 (citing Ex. 1021 ¶¶ 21–29, 36–39).

Patent Owner argues that Petitioner's ground did not rely on properties of Lee's voltage generation unit. PO Sur-reply 8. Although we agree that the Petition did not rely on the inherent properties of Lee's voltage generation unit, the Petition did argue that Lee would have been understood to operate by supplying all of its voltages as pulses. Pet. 39 (citing Ex. 1003 ¶ 205). We consider Petitioner's evidence of the voltage generation unit as supporting its position first raised in the Petition, and thus, not barred as a

new argument. *Chamberlain Grp., Inc. v. One World Techs., Inc.*, 944 F.3d 919, 925 (Fed. Cir. 2019) ("Parties are not barred from elaborating on their arguments on issues previously raised.").

Patent Owner also argues that the two references relied upon by Dr. Liu insufficiently establish that a person having ordinary skill in the art would recognize that Lee's circuitry includes a charge pump circuit. PO Sur-reply 8. We agree. As cited by Dr. Liu, Cappalletti states that Program and Erase voltages in a flash memory array may be generated from a low V_{CC} voltage using a capacitor-containing charge pump. Ex. 1008, 259. However, Cappalletti describes that there are two options for supplying program voltage. Cappalletti states that programming voltage V_{PP} may be "available on input pin" or if not available, "an internal circuit will generate it." *Id.* at 266. Contrary to Petitioner's reliance on Cappalletti describing that NAND program operations require a charge pump using pulsed voltage, Cappalletti describes that program voltages need not be generated by a charge pump if a dedicated high voltage supply is present. Ex. 1008, 266.

Further, Cappalletti describes row decoders having "V_{PC}," but contrary to Dr. Liu's characterization of V_{PC} necessarily representing a charge pump, Cappalletti describes V_{PC} as a "supply line" that is "at programming voltage V_{PP}." *Id.* at 269. Cappalletti further indicates that different voltage sources may be used for different voltage operations. Cappalletti distinguishes the generation of "very high" Program voltages, requiring a "very high" V_{PP}, from use of supply voltage V_{CC} for the relatively lower Read voltages. *Id.* at 252–253 (20 V Program and 5 V Read voltages on the gate), 255 ("V_{PP}" pin dedicated for Program/Erase voltage), 259, 267 ("the read voltage normally coincides with the supply voltage" which may be V_{CC}). Thus, contrary to Petitioner's argument that NAND

circuitry would use the same voltage supply, in the form of a charge pump, for all of its voltage operations, Cappalletti describes that even where a program voltage may be generated by a charge pump, a lower voltage such as a read voltage may be generated by the V_{CC} supply voltage without the use of a charge pump. *Id.* at 276.

We further note that the portion cited by Dr. Liu regarding NAND memory employing a voltage generation unit instead discusses "NOR" memory. *Compare* Ex. 1021 ¶ 23 (citing Ex. 1008, 259) *with* Ex. 1008, 252–259 ("5.1.2 NOR Cell Operation and Array Organization"). Because Cappalletti does not clearly support either of Petitioner's assertions for which it is relied, Cappalletti insufficiently supports Petitioner's assertion that a charge pump is described in Lee to provide a pre-charge pulse voltage.

Similarly, Micheloni does not support Petitioner's charge pump assertions. Like Cappalletti, Micheloni describes the use of a charge pump for program and erase operations only. Ex. 1012, 189. Thus, Micheloni does not show support for a single voltage source for all high and low voltage operations, undermining Petitioner's assertion that Lee's power source would be understood to power all of its operations in the same manner.

Further, we agree with Patent Owner that the portions of Cappalletti and Micheloni relied upon by Petitioner and Dr. Liu do not necessarily represent a broad view of the knowledge in the art. PO Sur-reply 8. Both portions have an author in common, Rino Micheloni. Ex. 1008, 250 (Chapter 5); Ex. 1012, 149 ("Chapter 6"). Micheloni cites to their own article for the use of charge pumps in a voltage regulator. Ex. 1012, 189 (stating "it is possible to design a voltage regulator [37] . . . supplied by a charge pump"), 194 (listing the authors of [37], including Rino Micheloni).

Thus, to the extent that Cappalletti and Micheloni would show that Lee uses a charge pump as a part of its precharge operation, they essentially provide a single viewpoint on such charge pumps. *See also* Ex. 1020, 32:21–33:16 (attesting to charge pumps as "one of many tools in the memory designer's toolkit to get the desired end results"), 31:5–16 (stating that Micheloni "describes one particular NAND flash implementation"). Petitioner's focus on Micheloni's views and Micheloni's voltage regulator design does not strongly show how a person of ordinary skill in the art would have understood Lee's voltage supply.

Petitioner further argues that "the use of well-known-pulsed programming voltages ***requires*** that the pre-charge voltages ***also*** be pulsed." Pet. Reply 7. Petitioner argues that if pre-charged voltages are not pulsed, they would not return to zero volts at the end of the pre-charge period. *Id.* at 9. Petitioner argues that this would result in the first pulse applied to the programming phase lacking the intended magnitude and duration because it is combined with the pre-charge voltage. *Id.* Petitioner argues this would defeat the purpose of incremental step pulse programming ("ISPP"), which it describes as being typically used for programming. *Id.* at 7 (citing Ex. 1012, 82; Ex. 1006, 118).

However, Petitioner does not show that Lee would have been understood to have used ISPP. Petitioner only shows that ISPP was typically used for cell programming, not that ISPP was the sole choice for programming such that a person having ordinary skill would have recognized Lee's cell programming to have definitively used ISPP. Further, Petitioner acknowledges that "ISPP programming starts at 0V." *Id.* at 8 (citing Ex. 1020, 19:17–23:10). Thus, even if the pre-charge voltage is nonzero at the end of the pre-charging operation, the programming phase

starts at 0V. Thus, Petitioner has not shown that Lee describes a pulsed programming operation using ISPP, or that Lee would end its pre-charging operation by returning to 0V.

Finally, we note the statements of Petitioner during oral argument. Petitioner initially asserted that Lee's pre-charging operation must return to zero volts. Tr. 15:9–21. Yet Petitioner agreed that "you could select another voltage as your ground voltage." *Id.* at 7:6–10. Petitioner stated that having a different voltage as a ground voltage would "still be pulsing, you would still be starting and ending in the same place." *Id.* at 23:5–18. The acknowledged possibility of a non-zero ending pre-charge voltage further undermines Petitioner's arguments that a pre-charge phase must end at zero volts.

For the above-described reasons, Petitioner has not persuasively shown that a person having ordinary skill in the art would have understood Lee to describe its pre-charging voltage as a pulse.

b) Would it have been obvious for Lee's pre-charging to be a pulse?

Petitioner further asserts that programming voltages were conventionally provided in the form of a pulse such that a person having ordinary skill in the art would have understood Lee to operate by supplying all voltages during programming as pulses. Pet. 39 (citing Ex. 1006, 44, 116–117; Ex. 1007, 142–143; Ex. 1008, 338, 354; Ex. 1003 ¶¶ 204–205). Dr. Liu lists several examples of programming pulses, attesting that all of Lee's voltages, including its pre-bias voltages, would obviously have been supplied as pulses. Ex. 1003 ¶ 204. Petitioner points to Figure 13 of Zhao and Figure 8B of Yang as illustrating pulsed pre-charge voltages. *Id.* (citing Ex. 1005, Fig. 13; Ex. 1010, Fig. 8B; Ex. 1003 ¶¶ 204–205).

Patent Owner argues that the programming pulses described by Dr. Liu are distinct from pulses used in a pre-charge period. PO Resp. 34. Patent Owner does not directly address Petitioner's reliance on Zhao and Yang for showing pulses in a pre-charge period, but argues that using pulses for pre-charge signals "would not serve Lee's stated goal of 'uniformity,' and would slow down the device and reduce throughput by extending the total time needed to perform programming operations." *Id.* (citing Ex. 1004, 7:58–62, 9:7–13, Fig. 7; Ex. 2011 ¶ 87). Patent Owner concludes that Petitioner has not shown that it would have been obvious for Lee's pre-bias voltages to be supplied in a pulse form. *Id.* (citing Ex. 2011 ¶ 87).

We determine that the evidence of record establishes the use of pulses to deliver voltage signals as a well-known option. Patent Owner does not contest that programming voltage signals are typically shaped as pulses. PO Resp. 34; Ex. 2011 ¶¶ 204–205. Nor does Patent Owner contest that Zhao and Yang describe both programming and pre-programming voltage signals in pulse form. PO Sur-reply 8–9 (arguing that Yang's Vprechg voltage does not return to a starting voltage, but not contesting that its voltage increases in value and then decreases in value). Although the evidence of record does not establish that Lee describes its pre-charge voltages as pulses, that evidence does indicate that voltages, including those in a pre-charging operation, were known to be delivered as a pulse.

We do not agree with Patent Owner that Lee's discussion of a uniform precharge level would indicate that a pulsed precharge voltage would not have been an obvious alternative. Patent Owner and Dr. Przybylski point to the following language in Lee relating to creating a uniform precharge level:

> The word lines coupled to a memory string in a memory block may be grouped, and different pre-bias voltages may be

> applied to the respective groups during a precharge operation of the cell string. Consequently, a uniform precharge level in the entirety of the cell string may be formed.

Ex. 1004, 7:58–62 (cited by Dr. Przybylski at Ex. 2001 ¶ 37, Ex. 2011 ¶ 87). Lee indicates that the uniformity of its precharge level results from applying different pre-bias voltages to respective groups during pre-charging. This does not support Patent Owner's argument that Lee's uniformity results from a flat, unpulsed signal. Lee does not relate the uniformity of the precharge to the shape of its pre-charging signals. Lee merely requires that different pre-bias voltages be applied to different groups during the precharge operation. *See* Ex. 1004, 7:63–64 ("[t]he operation of applying different pre-bias voltages to word lines at a pre-charging step during a program operation"), 9:7–9 ("After the pre-bias voltage is applied to the respective word lines and the precharge operation is completed, a program voltage may be applied.").

Patent Owner argues that Lee creates a "***uniformly formed***" charge by compensating the resistance component between source and drain transistors, but does not explain why such compensation disfavors a pulsed pre-charging signal. PO Resp. 30 (citing Ex. 1004, 7:58–62, 8:25–52). Despite Patent Owner's argument that using a pulse in Lee would "disadvantageously . . . extend[] the total time needed for programming operations," Patent Owner explains that its invention "avoids the need for . . . extended data programming times" by using "multiple pre-pulse signals to '***enhance***' the '***channel potential gradient***.'" PO Resp. 30 (citing Ex. 1001, 4:39–59, 7:37–47), 32 (citing Ex. 2011 ¶¶ 83–84). In contrasting the advantages of its invention with those of Lee, Patent Owner focuses on the creation of "resistance" versus the creation of a "potential gradient" of

the structures, not on the shape of the signals in either. Pet. Reply 9 ("It is Patent Owner's proposed voltage provision scheme—not the use of pulses—that would reduce "uniformity.").

Thus, neither party has shown any description in Lee, express or implied, concerning the shape of its pre-bias voltage signals. On that blank slate of Lee, we determine that Petitioner has shown that using pulsed signals would have been obvious. Petitioner has presented evidence of pulsed programming schemes as being known in the art, and evidence of individual cases of pulsed pre-programming signals. Ex. 1006, 44, 116–117; Ex. 1007, 142–143; Ex. 1008, 338, 354; Ex. 1005, Fig. 13; Ex. 1010, Fig. 8B; Ex. 1003 ¶¶ 204–205.

Consequently, we determine that Petitioner has shown, by a preponderance of the evidence, that a person having ordinary skill in the art would have considered it obvious to supply pre-charge voltages, as taught by Lee, in the form of a pulse.

> *[1.E.4] wherein a voltage level of the second word line prepulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.*

Petitioner asserts that Lee teaches limitation [1.E.4] through its description that "different pre-bias voltages" are applied to its word line "groups during a precharge operation" and that "higher … pre-bias voltage[s]" are applied to "word line group[s]" that are closer to the "drain select transistor." Pet. 40 (citing Ex. 1004, 7:58–61, Abstr., 1:62–2:9, Fig. 4B, 8:32–37, 9:44–51). Patent Owner does not specifically contest this assertion. PO Resp. 28–35.

We agree that Petitioner's assertion is supported by the complete trial record. Lee describes that the voltage applied to group 4 is greater than that

for group 3, which in turn is greater than that for group 2. Ex. 1004, 9:41–52. Accordingly, Petitioner has sufficiently shown that Lee teaches limitation [1.E.4].

Conclusion

For the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claim 1 would have been obvious over Lee.

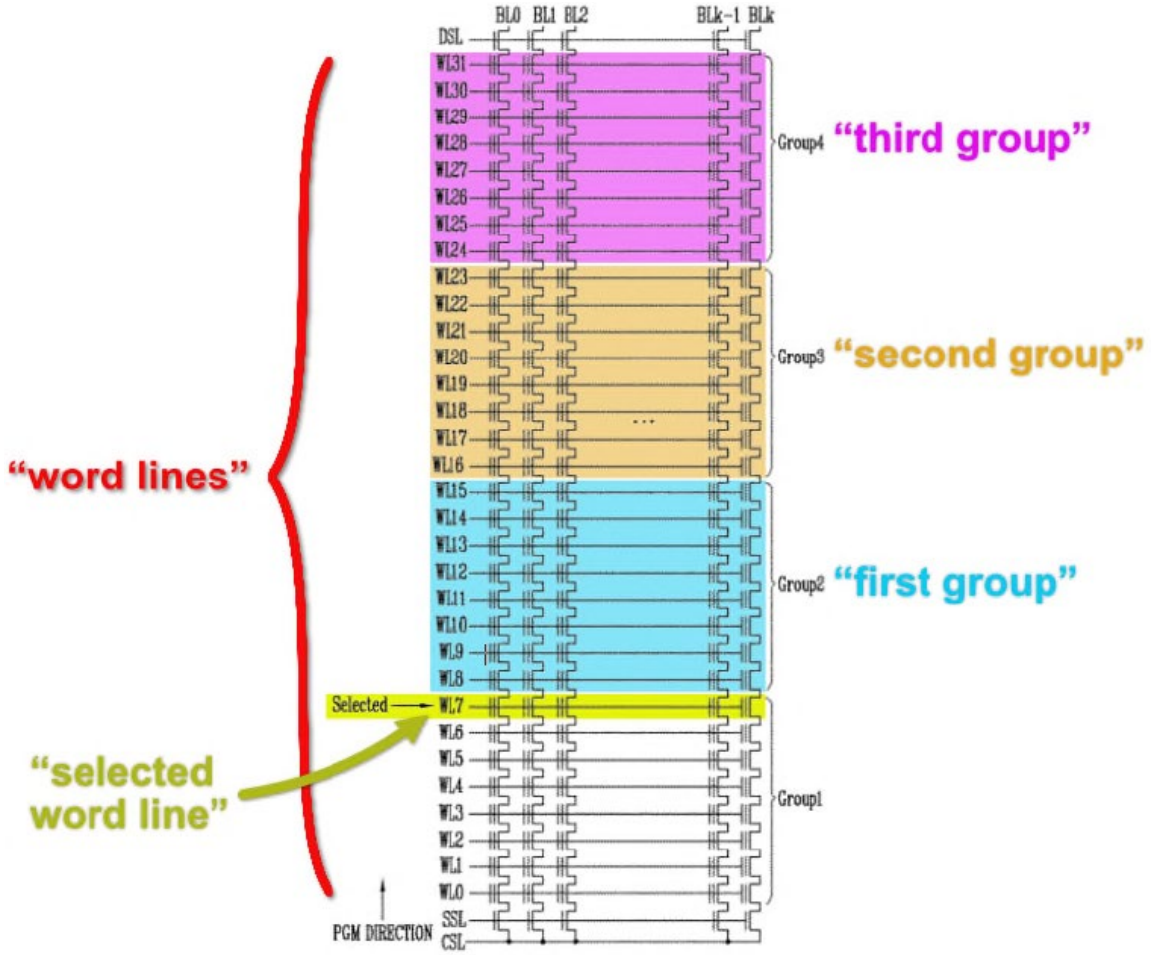
3. Analysis of Claims 2, 3, 6, and 11–13

a) Claim 11

Petitioner's assertions for independent claim 11, having similar limitations to those of claim 1, rest essentially on the same showing. Pet. 26–41. Consequently, Petitioner has shown, by a preponderance of the evidence, that claim 11 would have been obvious over Lee.

b) Claims 2 and 12

With respect to each of the word line groups being "disposed in an order of distance" from the "selected word line," as set forth for claims 2 and 12, Petitioner asserts that Lee shows such an order in its Figure 4B. Pet. 41–42. Specifically, Petitioner asserts that when Lee's word line WL7 is selected, Lee shows three groups (first group, WL8–WL15; second group, WL16–WL23; third group, WL24–WL31) progressively further from selected word line WL7, depicted in a modified version of Lee's Figure 4B:



Modified Figure 4B depicts word lines WL0 through WL31 extending from source select line SSL to drain select line DSL, with the selected word line WL7 highlighted in green, word lines WL0 through WL7 labeled "Group1," word lines WL8 through WL15 labeled "Group2," word lines WL16 through WL23 labeled "Group3," word lines WL24 through WL31 labeled "Group4," and bit lines BLs that couple the selected string to a common source line CSL. Pet. 42 (citing Ex. 1004, Fig. 4B); Ex. 1004, 7:37–38.

Patent Owner argues that Lee's groups are disposed relative to the bit line or the source line, rather than the selected word line, because Lee describes that groups are determined before a word line is selected for programming. PO Resp. 36–37. Petitioner's declarant, Dr. Liu, confirms this upon deposition. Ex. 2021, 25:2–15.

Nevertheless, Petitioner points to a configuration in Lee that teaches the groups being disposed relative to the selected word line, as claimed. When word line WL7 (or any of word lines WL0–WL6) is "selected," Lee's "Group2" word lines are disposed nearest (in the direction towards the bit line), with "Group3" and "Group4" word lines disposed successively further from WL7. In this configuration, word line groups 2, 3, and 4 are disposed an order of distance from the source line and an order of distance from the selected word line WL7. Under our construction (§II.C.2), this is sufficient.

Patent Owner argues that Lee does not teach that word lines "remain in the same predetermined groups" and that Lee's groups are "fixed prior to a word-line being selected for programming" and "do not change based on the position of the selected word line." PO Sur-reply 11–13. As noted, claims 2 and 12 do not require groups to be changed or to be changeable, because these claims recite that the groups "are disposed" at the claimed distances. *Supra* §II.C.2. Because Petitioner has pointed to one configuration of Lee that teaches the groups disposed in the claimed manner, Petitioner has shown Lee to teach the claimed disposition of groups from the selected word line.

In this manner, Petitioner has shown, by a preponderance of the evidence, that claims 2 and 12 would have been obvious over Lee.

c) Claims 3 and 13

Claims 3 and 13 further require:

> the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.

Ex. 1001, 8:19–25, 9:19–25.

Petitioner asserts that Lee's Figure 4B shows a select gate line DSL, then a third group ("Group4"), then a second group ("Group3"), then a first group ("Group2") adjacent to the selected word line (WL7) in the claimed order of word and gate lines. Pet. 42–43 (citing Ex. 1004, 7:37–43, 6:15–18; Ex. 1003 ¶¶ 217–220).

Patent Owner argues that the groups are predetermined irrespective of the selective word line's location. PO Resp. 38–39 (citing Ex. 2011 ¶ 97); PO Sur-reply 13–14. However, as discussed with respect to claims 2 and 12, claims 3 and 13 do not require "predetermined" groups. Consequently, Petitioner has shown, by a preponderance of the evidence, that claims 3 and 13 would have been obvious over Lee.

d) Claim 6

With respect to the application of a word line signal to the selected word line as set forth in claim 6, we agree with Petitioner's uncontested assertion that "Lee's control unit causes the 'selected' word line to be supplied with a 'default value' '[p]re-bias voltage[]" during pre-charge," and a "program voltage Vpgm" during programming. *Id.* at 44–45 (citing Ex. 1004, 2:23–29, 6:29–36, 9:7–14, 9:52–55; Ex. 1003 ¶¶ 221–225). Accordingly, Petitioner has shown, by a preponderance of the evidence, that claim 6 would have been obvious over Lee.

4. Conclusion

For the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claims 1–3, 6, and 11–13 would have been obvious over Lee.

E. Obviousness over Zhao

Petitioner asserts that claims 1, 4–7, 9, 11, 14–16, 18, and 19 would have been obvious over Zhao. Pet. 44–59. Patent Owner disputes that Zhao teaches three "pre-pulse signals" during a "pre-charge period." PO Resp. 23–24.

1. Zhao

Zhao is titled "Non-Volatile Memory with Countermeasure for Program Disturb Including Purge During Precharge." Ex. 1005, code (54). Zhao relates to a semiconductor memory device in which it is proposed to address program disturb during memory cell programming by "open[ing] the channel from one side of a selected word line to the other side of the selected word line after a sensing operation for program verify and prior to a subsequent programming voltage being applied." *Id.* at code (57). Unselected NAND strings are pre-charged prior to applying the program voltage to the selected word line. *Id.* at Fig. 11, [702]. Different pre-bias voltages are applied depending on the relative positions of the word lines. *Id.* During programming, unselected cells are maintained at a voltage Vdd to inhibit programming while selected cells have a program pulse applied thereto. *Id.* at 14:43–64. In one embodiment, a time period t1–t3 corresponds to pre-charging, during which unselected bit lines are raised to a pre-charge voltage. *Id.* at 22:39–49, Fig. 13. During the next time period t4–t10 corresponding to programming, the unselected NAND strings have their voltage lowered from Vpre-charge to Vinhibit. *Id.* at 23:13–17.

2. Analysis of Claim 1

We begin our analysis of Petitioner's obviousness contentions with Petitioner's assertions as to claim 1. Patent Owner does not specifically argue against Petitioner's assertions for limitations [1.Pre]–[1.D]; however,

we draw no inference therefrom and Petitioner bears the burden of persuasion.

> *[1.Pre]–[1.D] A memory device, comprising: a plurality of memory strings; a bit line connected to a first memory string of the plurality of memory strings; a select gate line connected to the first memory string of the plurality of memory strings; a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string;*

Petitioner asserts that limitations [1.Pre]–[1.D] are taught by Zhao in the following manner. Petitioner points to Zhao's memory system 100 having a three dimensional NAND structure having columns implementing NAND strings, in which each NAND string includes a series of non-volatile memory cells. Pet. 44–45 (citing Ex. 1005 4:7–10, 8:31–44, 6:41–43, 10:6–9; 12:6–7, 12:9–13, Figs. 4F, 4G). Petitioner further points to Zhao's bit line 411 and select gate line SGD0 connected to a NAND string as exemplary of teaching a bit line and a select gate line that are connected to a first memory string. *Id.* at 45–47 (citing Ex. 1005, 7:64–66, 10:19–21, 11:53–61, 12:6–10, Fig. 4G). Petitioner further points to Zhao as teaching a plurality of word line layers WLL0–WLL95 as connecting to the memory cells that make up Zhao's NAND strings, and that at least one word line, for example, word line 94, is "selected for programming." *Id.* at 47–48 (citing Ex. 1005, 7:64–66, 10:8–13, 3:30–49, 17:27–30, 12:14–25, Fig. 4G).

Patent Owner does not argue against these assertions. Upon review of Zhao, we determine that Petitioner's assertions are supported by the record.

> *[1.E] a control circuit configured to: [1.E.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period; [1.E.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and [1.E.3] apply a third word*

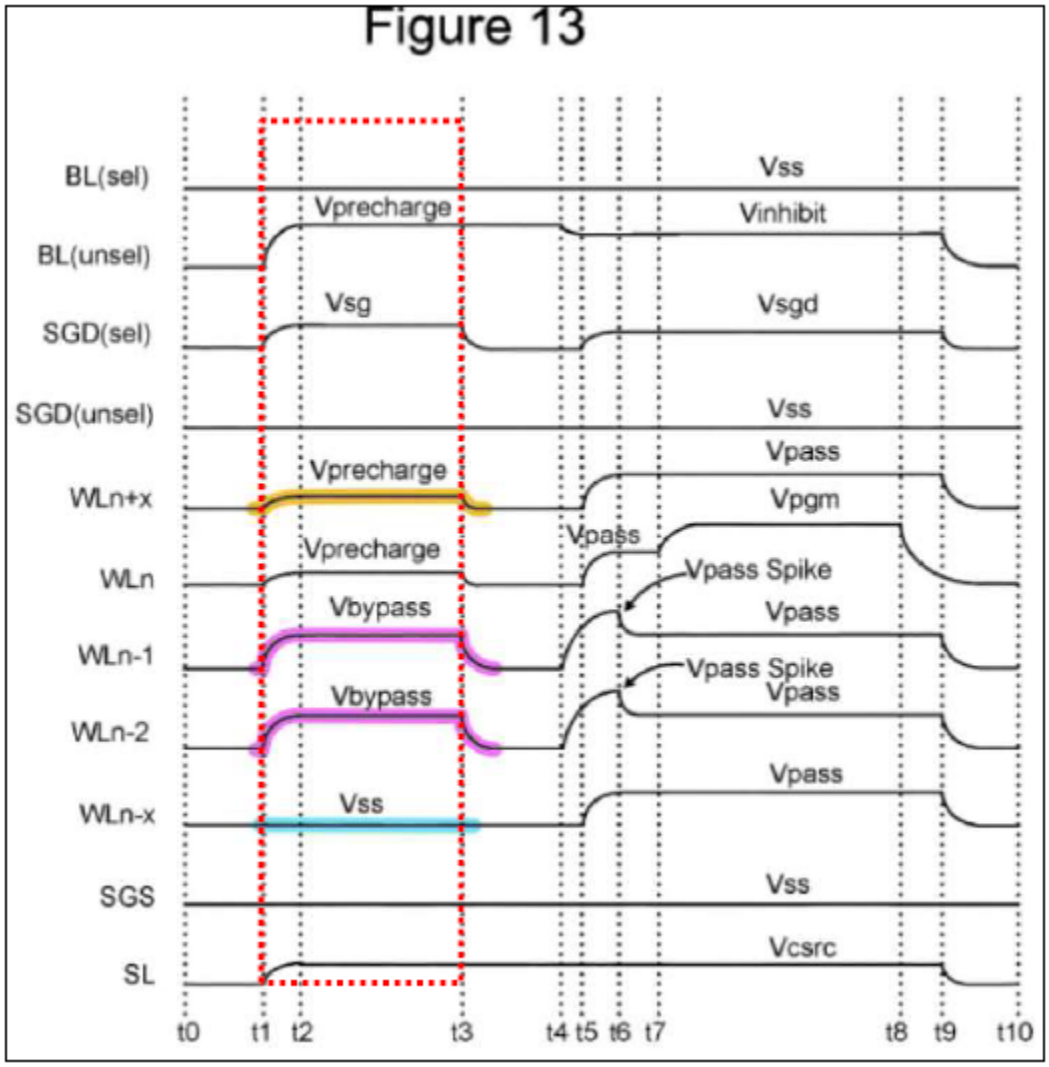
> *line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,*

Petitioner asserts that Zhao describes a control circuit 310 that performs memory operations on memory structure 326, including a process for programming and a pre-charge circuit 584 that applies pre-charge signals to channels of unselected NAND strings. Pet. 48–49 (citing Ex. 1005, 5:64–6:20, 13:65–14:6, 16:40–67, Fig. 8). Petitioner further asserts that Zhao teaches that the pre-charge in step 542 occurs before the application of a program pulse in step 546. *Id.* at 49–50 (citing Ex. 1005, Fig. 7, 14:35–55, 19:12–19). Petitioner asserts that Zhao describes these pre-charge voltages to be in the form of "pulses." *Id.* at 50 (citing Ex. 1005, 14:7–16). Petitioner further points to Zhao's description that "multiple already programmed (e.g., source side) unselected word line[s] … adjacent to the selected word line" can "receive[]" a different "bypass voltage" "while pre-charging[.]" *Id.* at 50–51 (citing Ex. 1005, 19:19–60). Petitioner further points to Zhao's description at Figures 4G and 13 of a pre-charge period corresponding to time period t1–t3, in which three different voltages are applied to different word line groups. *Id.* at 51 (citing Ex. 1005, 22:39–53). Petitioner specifically points to unselected word lines WLn-1 and WLn-2 as having a Vbypass voltage of 6-10 V and a "low" V_{SS} voltage for the remaining source side unselected wordlines WLn-x. *Id.* (citing Ex. 1005, 22:41–53, 19:22–24).

Petitioner asserts that the claimed "first" pre-pulse signal is taught by Zhao's low-voltage V_{SS} applied to nonadjacent source-side word lines WLn-x, the "second" pre-pulse signal is taught by Zhao's Vprecharge applied to the drain-side word lines WLn+x, and the "third" pre-pulse signal

is taught by Zhao's Vbypass applied to the source-side word lines adjacent source-side word lines WLn-1 and WLn-2. *Id.* at 51–52. Petitioner states that although V_{SS} is 0V in the Figure, Zhao explains that a "low" non-zero voltage can be supplied instead in the same t1-t3 time period as the other pre-charge voltage pulses. *Id*. at 51 (citing Ex. 1005, 19:22–24). Petitioner contends that when a "low" non-zero voltage is supplied instead of 0V in the same t1-t3 time period, this results in a "first word line pre-pulse signal" (a low non-zero voltage in place of V_{SS}, blue) applied to a "first group of . . . word lines" (the source-side word lines not adjacent to the selected word line, WLn-x). *Id.* at 51–52.

Patent Owner argues that the V_{SS} voltage is not a pulse because it is a "flat, unchanging" voltage and thus Zhao does not disclose or suggest the claimed first pre-pulse signal. PO Resp. 39. Patent Owner argues that because V_{SS} is not a pulse, Zhao does not teach the claimed "first word line pre-pulse signal." *Id.* at 40. Patent Owner annotates Figure 13 to illustrate:



Id. at 42. Annotated Figure 13 of Zhao illustrates timing regions t0 through t10 and the voltages applied to different regions. *Id.* Patent Owner highlights how Vss stays level during timing region t1–t3 in contrast to the voltage increases for Vprecharge and Vbypass over the same period. *Id.* Patent Owner interprets Zhao's statement that Vss may instead receive "one or more voltages that are too low to pre-charge" as describing that a *fixed* non-zero voltage may be applied rather than a fixed zero voltage. *Id.* (citing Ex. 1005, 19:22–26). Patent Owner asserts that regardless of whether the

Vss signal is fixed at 0 volts or another fixed voltage, the signal will remain flat, and that a flat signal is not a pulse. *Id.* at 42–43.

We agree with Patent Owner. Zhao states that unselected word lines WLn-x "remain" at either V_{SS} or a low voltage. Ex. 1005, 23:7–8. Zhao's "remain" language for the unselected word lines contrasts with its other word lines that "are raised to" different voltages and then "all lowered to ground/V_{SS}." *Id.* at 23:5–10. The section of Zhao cited by Petitioner states that the unselected source side word lines "receive 0 volts or one or more voltages." *Id.* at 19:23–24. The "receive" language is consistent with the "remain" language, and does not indicate that receiving a nonzero voltage causes a raising and lowering of the voltage. Rather "receive . . . one or more voltages" is consistent with the unselected lines remaining at a low voltage.

Petitioner's declarant Dr. Liu merely states that a low non-zero voltage "can be applied" "in place of V_{SS}" Ex. 1003 ¶¶ 272, 280. Dr. Liu states that Zhao's nonzero voltage that is "received" by WLn-x is not V_{SS} because V_{SS} is not a "received" voltage. Ex. 1021 ¶ 63. However, Dr. Przybylski attests that even where the low voltage is applied to the unselected word lines, the word lines "remain" at that value throughout the pre-charging period. Ex. 2001 ¶ 34. Dr. Przybylski attests that "there would be seemingly no purpose in replacing **Vss** with *another* low voltage 'too low to precharge and/or too low to turn on the memory cells' because **Vss** is *already* low enough to keep the memory cells WLn-x turned off and prevent pre-charging." Ex. 2011 ¶ 70.

Dr. Przybylski's interpretation is consistent with Figure 13, which illustrates that V_{SS}, which may be a nonzero low voltage, is a flat signal for at least four different lines. Ex. 1005, Fig. 13 (showing flat, unpulsed V_{SS}

signals for BL(sel), SGD(unsel), WLn-x, and SGS), Ex. 1005, 22:35–38 ("The selected bit line BL(sel), drain side selection line SGD (unsel) for unselected sub-blocks, and the source side select lines SGS are all at 0 volts (V_{SS}) during the entire timeframe depicted in FIG. 13."); *see* Pet Reply 13 ("All of Zhao's lines start 'at 0 volts' (or 'V_{SS}')"). Petitioner has not shown sufficient support for an interpretation in which WLn-x is raised to a low non-zero voltage and subsequently lowered to zero volts. Thus, Petitioner has not shown, by a preponderance of the evidence, that claim 1 would have been obvious over Zhao.

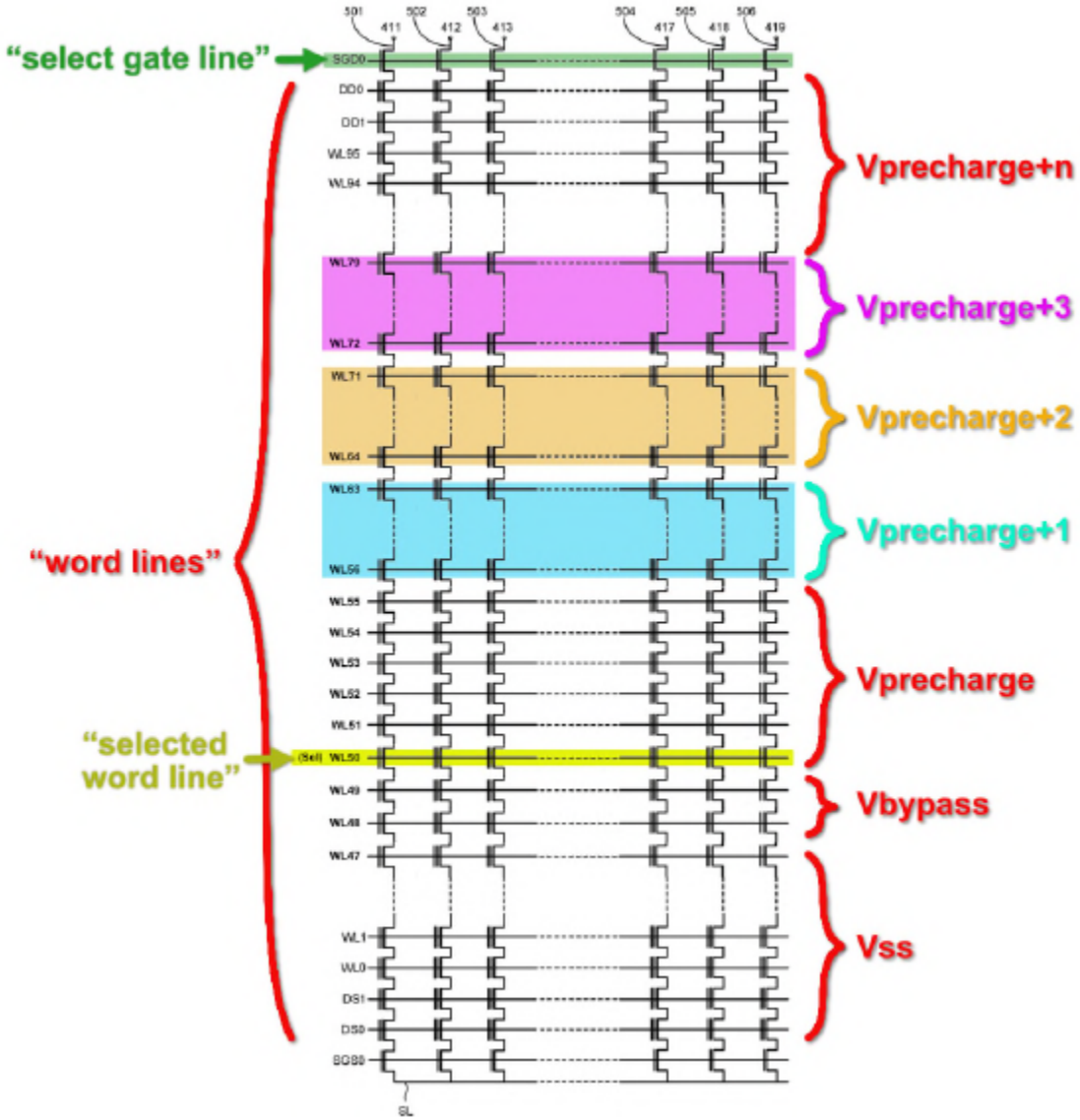
3. Analysis of Claims 4–7, 9, 11, 14–16, 18, and 19

Petitioner's assertions for independent claim 11, having similar limitations to those of claim 1, rest essentially on the same showing, and we reach the same conclusions at this stage for the aforementioned reasons. Pet. 44–53. Dependent claims 4–7, 9, 14–16, 18, and 19 depend from claims 1 or 11, and Petitioner does not present further reasons why Zhao teaches the first word line pre-pulse signal in claims 1 and 11. Consequently, we determine that Petitioner has not shown, by a preponderance of the evidence, that Zhao teaches claims 4–7, 9, 14–16, 18, and 19.

F. Obviousness over Zhao and Lee

Petitioner asserts that claims 1–9 and 11–19 would have been obvious over Zhao in view of Lee. Pet. 59–68. For its Zhao-Lee combination, Petitioner applies the teachings of Zhao for limitations [1.Pre]–[1.E.3]. Pet. 59–60. Petitioner applies the teachings of Lee to satisfy the relative voltage level limitations of [1.E.4]. Pet. 60–68. As discussed in the prior sections of this Decision, we have determined that Zhao teaches limitations [1.Pre]–[1.D] and [11.Pre]–[11.D] but not limitation 1.E, which we have determined to be taught by Lee. *Supra* §§ II.D.2, II.E.2.

In its combination, Petitioner applies the word line groups of Lee with the programmed voltages of Zhao. Petitioner argues that it would have been obvious to replace Zhao's single Vprecharge prepulse signal with Lee's multiple signals having increasingly large voltage levels. Pet. 59–60. Zhao's Vprecharge signal is uncontestedly a pulse. *See* PO Resp. 46–47; Ex. 1005, Fig. 13. Petitioner's resulting arrangement is illustrated below:



Pet. 65. In this combination, Lee's selected word line WL50 is supplied with a pre-charge value, with additional groups WL50–WL63, WL64–WL71, WL72–79 having pre-charge values that increase with each group's

distance from the selected word line WL 50. *Id.* at 64. Beyond the last group of word lines is select gate line SGD0. *Id.* at 65. Below the selected word lines, groups are applied either a bypass voltage or VSS, with SGS0 and SL at the bottom-most lines of the illustration. *Id.*

1. Rationale to Combine Zhao and Lee

Petitioner asserts that such a combination would have been obvious to address sources of program disturb, such as channel resistance, which are not mitigated by Zhao. Pet. 66 (citing Ex. 1003 ¶¶ 356–58). Petitioner asserts that Zhao applies the same Vprecharge voltage to all unselected word lines on the drain side of the currently selected word line. *Id.* at 60 (citing Ex. 1005, 22:39–49). Petitioner asserts that a person having ordinary skill in the art would have recognized that Lee's application of higher pre-charge voltages to groups of the drain-side unselected word lines offset channel resistance, providing more uniform pre-charging, better boosting, reduced program disturb, and increased cell endurance. *Id.* at 60, 66 (citing Ex. 1003 ¶¶ 361–63). Petitioner asserts that the combination applies complementary teachings of Lee and Zhao; i.e., Lee's drain-side countermeasures and Zhao's source side countermeasures. *Id.* at 67; Pet. Reply 19.

With respect to the reasons to combine the teachings of Lee and Zhao, Petitioner asserts that a person having ordinary skill in the art would add Lee's teaching to that of Zhao for claims 1–9 and 11–19 to result in collections of drain-side word lines receiving increasingly higher pre-charge voltages corresponding to their distance from the selected word line because it would result in a more effective mitigation of program disturb through Lee's grouping of word lines to offset the relatively high channel resistance when programming word lines closer to the source-side of a memory string. *Id.* at 65–66 (citing Ex. 1003 ¶¶ 356–363). Petitioner also asserts that cell

endurance is increased by reducing the voltage applied to certain drain-side word lines. *Id.* at 66 (citing Ex. 1003 ¶ 363). Petitioner also asserts that Lee furthers Zhao's goal of avoiding voltage differentials in the channel of an unselected NAND string because Lee ensures a uniform channel voltage; moreover, that this represents arranging old elements with each performing their known function. *Id.* at 67 (citing Ex. 1005, 2:10–26, 4:7–10, 18:52–59, 22:65–23:12; Ex. 1004, 7:61–62, 8:47–52; Ex. 1003 ¶¶ 364–371).

a) Bit line vs. common source line pre-charging

Patent Owner argues that Petitioner's reasons to combine Lee and Zhao with respect to claims 1–9 and 11–19 are deficient. PO Resp. 44–58. First, Patent Owner argues that Lee applies pre-charge voltage to the common source line whereas Zhao applies pre-charge voltage to the bit line. *Id.* at 45, 48–50. Patent Owner argues that there are substantial differences between such charging schemes, citing three separate embodiments in Yang for pre-charging (bit line, source line, and bit and source line) having distinct biasing schemes. *Id.* at 49 (citing Ex. 1010, 1:59–2:19; Ex. 2011 ¶ 115); PO Sur-reply 20–21 (citing Ex. 2011 ¶¶ 115–116). Patent Owner further argues that Lee, unlike Zhao, passes current through the memory string. PO Resp. 51–52; PO Sur-reply 17–20 (citing Ex. 2011 ¶ 118). Patent Owner argues that Petitioner does not explain how Lee's teachings would need to be adapted for the distinct technology of Zhao without additional modifications. PO Resp. 49–50 (citing Ex. 2011 ¶ 116).

Petitioner asserts that the teachings of Lee and Zhao are compatible because there is no meaningful difference between pre-charging via the bit line (as in Zhao) or via the source line (as in Lee). Pet. 68; Pet. Reply 16. Petitioner further asserts that neither Lee nor Zhao applies current during pre-charging because "the voltages applied during precharging are intended

only to purge and redistribute electrons already in the channel that may later cause program disturb." Pet. Reply 16–17 (citing Ex. 1021 ¶¶ 64–70; Ex. 1004, 1:52–56; Ex. 1005, 17:4–12). Petitioner argues that the lack of current flow permits channel voltage to be applied at either end of the channel. *Id.* at 17–18 (citing Ex. 1021 ¶¶ 77–78). Petitioner points to Yang's statement that the "3D memory's channel can be pre-charged from the 'drain end of the NAND string' or the 'source end.'" *Id.* (citing Ex. 1010, 17:16–23).

Although both declarants differ on the technological hurdles and issues involved in applying a charge via the bit line and/or the source line, there is one clear point of agreement. Both declarants, and both parties, agree that Yang has bit line, source line, and combined bit and source line pre-charging embodiments. PO Resp. 49 (citing Ex. 1010, 1:59–2:19); Pet. Reply 17–18 (citing Ex. 1010, 17:16–23). Because obviousness is determined from the perspective of one having ordinary skill in the art, it is telling that despite any technological hurdles, Yang treats bit line and source line charging both as alternatives and as complementary techniques that may be used in the same pre-charging operation. *See* Ex. 1010, 1:59–2:19, 27:60–63. To the extent that modifications are needed for Petitioner's combination, Yang shows the ability in the art to address pre-charging through any combination of bit line and source line charging. The record further shows that Lee is not limited to source line pre-charging. Dr. Przybylski attests that he has not opined that "the source line pre-charging is the only thing that's disclosed within Lee." Ex. 1020, 56:19–57:4. Patent Owner admits that "Lee does not state where the pre-charge voltage is applied in the specific embodiment of Fig. 5." PO Sur-reply 21. Consequently, we are persuaded on the record evidence that a person having

ordinary skill would have found it obvious to use either or both methods in a pre-charging operation of a NAND string.

b) Lee's resistance component

Patent Owner further argues that Petitioner's motivation for applying Lee's teachings to Zhao is inapplicable. PO Resp. 50. Patent Owner argues that Petitioner applies Lee's teachings to offset a resistance component between source and drain, but that this would only apply to a system like Lee having current flowing in the memory string. *Id.* Patent Owner argues that Zhao does not have current flowing in the memory string, because several of its memory cells are turned off, and consequently, has no such resistance component that would be compensated for by Lee's teachings. *Id.* at 50–54 (citing Ex. 1004, 8:25–32; Ex. 1005, 19:22–26; Ex. 2011 ¶¶ 118–121).

(1) Whether Lee's pre-charging involves current flow

Petitioner first argues that Lee's drain-side teachings are applicable to Zhao because neither Lee nor Zhao apply current during pre-charging. Pet. Reply 16. Petitioner argues that the pre-charging voltages are "intended only to purge and redistribute electrons already in the channel that may later cause program disturb." *Id.* at 17. Petitioner points to Zhao as noting that program disturb can be caused by electrons trapped in the channel, which would also be applicable to the program disturb in Lee. *Id.* (citing Ex. 1004, 1:52–56; Ex. 1005, 17:4–12).

Dr. Liu and Dr. Przybylski disagree on the factual question of whether current flows in Lee. Both experts focus on current flow through the NAND strings. Dr. Liu states that Lee applies source voltage "to shut off that string," whereas Dr. Przybylski states that Lee's pre-bias voltage causes "the

unselected NAND strings [to be] fully turned on." Ex. 2021, 84:8–18; Ex. 2011 ¶ 62.

We determine that Petitioner has not shown sufficient support for its assertion that Lee may be combined with Zhao because Lee (like Zhao) does not have current flow during pre-charging. Pet. Reply 17. Dr. Przybylski attests that Lee implies that current is flowing during its pre-bias period due to "resistive components between the source select transistor and the drain select transistor." Ex. 1020 (Przybylski Dep.), 55:13–18. Dr. Przybylski states that "if any of the transistors [in a NAND's channel] are off, its resistance is essentially infinite and that there is no significant current flowing through it." *Id.* at 61:5–11. Dr. Przybylski clarifies that there would be no current "if the source select or drain select transistors are off . . . just as any of the memory cells being turned off would cut off current flow in the string." *Id.* at 61:23–62:3. Dr. Przybylski further clarifies that this testimony relates to "the steady state." *Id.* at 63:8–17. Dr. Przybylski states that when all of the transistors within a particular memory string are turned on, the resistance along the length of the memory string creates a voltage drop across each of the memory cell transistors having deleterious effects. Ex. 2011 ¶ 62. Dr. Przybylski states that Lee, by "applying pre-bias voltages to each of the word lines, . . . ensures that all of the channels of the memory cells in the unselected NAND strings are fully turned on and development of the precharge is not inhibited." *Id.* (citing Ex. 1004, 8:18–52).

We agree with Patent Owner that Petitioner has not shown Lee's pre-charging to involve no current flow. As Dr. Przybylski attests, Lee's pre-charging applies pre-bias voltages to all word lines WL0 to WL30.

Ex. 1004, 8:11–17. Dr. Liu relies on aspects of charge pumps to support its contention that no current may flow during pre-charging or programming. Pet. Reply 17. However, we have determined that Lee does not require charge pumps. *Supra* § II.D.2.a.

Petitioner also argues that no current is applied during pre-charging because of the state of the channel during programming. Pet. Reply 17. This argument is not persuasive because Petitioner has not explained why the channel would be in the same state during both operations. *See* PO Sur-reply 19. We note that Yang, on which Petitioner relies for its similarities (*see* Pet. Reply 18), does not maintain its gates in the same state during pre-charging and programming operations. Ex. 1010, Figs. 8B, 9B, 10B; PO Sur-reply 19. We further note that Dr. Liu's general statement that no current flows during pre-charging conflicts with a description of a self-boosted program inhibit scheme for NAND technology provided by Petitioner:

> *During this pre-charge of the string* the channel side of the select transistor acts as the source. Accordingly, *a charging current flows* until the gate-to-source voltage equals the threshold voltage of the select transistor. In the second time step t2, all word lines are raised to the program pass voltage Vpass (Fig. 4.11b, c) and the channel inhibit potential is increased by capacitive coupling. This can be done because *the select transistor is closed since the pre-charge was finished*.

Ex. 1012, 88–89 (emphasis added). Although neither Lee nor Zhao explicitly state the use of a self-boosted program inhibit scheme,[4]

[4] As to its relevance, we note that under deposition, Dr. Liu discussed boosting the channel voltage in connection with inhibiting the memory cell (Ex. 2021, 84:24–85:11), and that Dr. Przybylski characterizes Zhao as providing boosting after its pre-charging operation. Ex. 1020, 63:23–64:3 (citing Ex. 1005, 22:18–20).

Petitioner's provision of a document describing a scheme in which some current may flow during a pre-charging step but not in a programming step indicates that Dr. Liu's statement may not be as broadly applicable as he attests, and undercuts the persuasiveness of his testimony on this point. Based upon the complete trial record, Petitioner has not sufficiently supported its contention that a lack of current during programming shows a lack of current during Lee's pre-charging. However, Petitioner has advanced a "chain resistance" explanation of Lee that does not require current to be passed in the steady state, which we address next.

(2) Chain resistance

Dr. Liu provides an alternative explanation as to why a lack of current during Zhao's pre-charging is not an impediment to the combination. Dr. Liu states that in both Lee and Zhao, resistance is based on a "chain effect" on the threshold voltages of transistors connected in series along a channel. Pet. 22; Ex. 2021, 83:12–84:2. Dr. Liu attests that Lee's resistance component is a function of how many transistors are connected in series with it. Ex. 2021, 83:17–21. Dr. Liu explains that due to the chain of transistors, "the source voltage of one memory cell will gate the threshold voltage of that memory cell and then the subsequent memory cell" such that "by the time you get to the drain, the threshold voltage is the highest." *Id.* at 83:22–84:2. Dr. Liu attests that this resistance occurs even during pre-charging when the transistor is off. *Id.* at 84:8–18 ("the only reason you apply the source voltage is to shut off that transistor, to shut off that string.").

Dr. Przybylski states that there are no chain effects in Zhao because Zhao's memory cells are each formed in the same polysilicon layer, and therefore would have identical body/substrate voltages. PO Sur-reply 23

(citing Ex. 2001 ¶ 119). However, whether each cell has the same voltages does not address Dr. Liu's statement that there is a cumulative effect of the threshold voltages along the chain. Dr. Liu's attestation that resistance is a function of the threshold voltages of the transistors in a string is supported by other documentation submitted by Petitioner. Ex. 1012, 168–169 (stating that the series resistance of a memory cell in a string is a function of the threshold values of the cells in the series).

Although Patent Owner argues that Dr. Liu's chain resistance is a new argument, Patent Owner does not provide any explanation in support of that conclusion. PO Sur-reply 18–23. For example, Patent Owner does not explain why Dr. Liu is precluded from further explaining that Lee's "resistance component," discussed in his original declaration, is comprised of a cumulative effect of threshold voltages along the chain. *See* PO Resp. 51 n.6; Ex. 1003 ¶ 360 ("the channel length between drain-side and word line selected for programming would be quite long, resulting in a relatively high channel resistance."). Instead, Patent Owner provides counter-arguments on the merits of Dr. Liu's statements. PO Sur-reply 22. We note that Petitioner provided its chain resistance theory in response to Patent Owner's explanation of how pre-charging occurs in 3D NAND memory. Pet. Reply 16 ("Patent Owner then posits . . . . This is wrong and misunderstands how pre-charging occurs in 3D NAND memory"), 22–23. Consequently, we do not exclude Dr. Liu's chain resistance statements or Petitioner's arguments based thereon.

c) Purported advantages

Having determine that Dr. Liu's chain resistance theory is sufficiently supported in the record, we next address whether Petitioner has sufficiently shown that such resistance would provide reason to use Lee's multiple

voltage pre-charging in the drain-side lines of Zhao. Petitioner asserts that applying Lee's increasing pre-charge voltages to the different groups of drain-side word lines based on their location relative to the drain select transistor would provide certain advantages. Pet. 62–64 (citing Ex. 1003 ¶¶ 341–343).

Dr. Liu states that Zhao would benefit from Lee's pre-charging voltages because those voltages better "prepare the array's cells using the minimum necessary voltage." Ex. 1021 ¶ 111–112. Dr. Liu's testimony is supported by Zhao, which states, "[b]y applying these pre-charge voltages, the voltage of the channel will be raised, which will improve the future boosting." Ex. 1005, 19:17–19. Dr. Liu states that Zhao's programming passes current, and the threshold voltages of Zhao's transistors will vary in the same way discussed in Lee. Ex. 1021 ¶ 114. Dr. Liu states that because Zhao applies the same pre-charge voltages to all of its not-yet-programmed drain-side word lines, those varied threshold voltages will result in inadequate pre-charging. *Id.* ¶ 115. Dr. Liu states that the application of Lee's varied pre-charging voltages to Zhao will provide Zhao with the uniform pre-charging taught by Lee. *Id.* ¶ 116.

Patent Owner argues that changing where the pre-charging voltage is applied will change the biasing scheme, and therefore, not result in claimed voltages. PO Resp. 54–55; PO Sur-reply 20–21. Patent Owner points to Yang as using different biasing depending upon whether the pre-charging is from a bit line, a source line, or both. PO Sur-reply 21 (citing Ex. 1010, Figs. 8–10, 1:59–2:13; Ex. 2011 ¶¶ 115–116). Patent Owner does not explain how the biasing of Yang affects the specific combination of Lee and Zhao asserted by Petitioner; i.e., Lee's progressive biasing of drain-side

word lines as a replacement for Zhao's single biasing of drain-side word lines.

Unlike Petitioner's focus on altering the drain-side word lines in both Lee and Zhao, Patent Owner focuses on Lee's altering the word lines furthest from the pre-charging source. Patent Owner argues that Lee applies higher voltages the nearer the word lines are to the bit line. PO Resp. 54 (citing Pet. 64–65). Patent Owner argues that "in Zhao, the word lines furthest from the bit line aren't even supposed to be precharged—they are applied with a Vss voltage that is deliberately too low to precharge the memory cells." *Id.* at 55 (citing Ex. 1005, 19:22–26).

However, Petitioner's reasoning for its combination of teachings is not based on the location of the source or bit lines. Instead, Petitioner relies upon the distance from the selected word line and the drain-side of the string. *See* Pet. 66 ("the channel length between the drain-side of the string and word line selected for programming would be quite long, resulting in a relatively high channel resistance" (citing Ex. 1003 ¶ 360)). Petitioner asserts that Lee's application of higher pre-charge voltages to the drain-side word lines "offset the channel resistance effect." *Id.* (citing Ex. 1003 ¶ 361). Lee and Zhao both admittedly have "typical memory strings, which are a 'vertical column' of memory cells arranged in series between a source side select transistor and a drain side transistor." PO Resp. 53 (emphasis omitted). Petitioner asserts that applying pre-charging to mitigate program disturb (sought by both Lee and Zhao) relies on the creation of a potential difference to facilitate electron redistribution. Pet. Reply 17–18 (citing Ex. 1004, 1:52–56; Ex. 1005, 17:4–12; Ex. 1021 ¶¶ 72–78). Petitioner asserts that the application of voltage can be performed from either end of the channel so long as it targets the portion of the channel desired to be pre-

charged. *Id.* at 18 (citing Ex. 1021 ¶¶ 77–78; Ex. 1010, 17:16–23). Although Patent Owner points to Yang as showing different "biasing schemes" based upon whether the bit line, source line, or both are used for pre-charging, each of the cited Figures 8–10 of Yang indicates that Vbypass (Yang's uncontested pre-pulse signal) is applied to at least some word lines between the selected word line and the drain-side SGD0. Ex. 1010, Figs. 8C, 9C, 10C; *see* PO Resp. 25–28 ("a 'bypass voltage' ('Vbypass') is applied to 'not yet programmed' memory cells during the 'pre-charge phase'" (citing Fig. 8C) (emphasis omitted)). We do not discern in Patent Owner's arguments, or in the evidence provided during trial, sufficient reasons why applying voltage from either source or bit line disturbs Petitioner's asserted advantage of offsetting the resistance of the channel between a selected word line and the drain side of the string.

Patent Owner further argues that Lee discusses a "wholly disparate approach" for mitigating program disturb than Zhao and that a POSITA would not have been motivated to apply Lee's teaching to Zhao. PO Resp. 56–58. Patent Owner contends that because Zhao does not conduct current when applying its bypass voltage to equalize charges, but Lee does conduct current when doing so, Lee need only compensate for insufficient charge boosting due to the increased resistance component between source and drain and does not need to compensate for "resistance" effects creating voltage differences along the length of the memory string channel. *Id.* at 56. Dr. Przybylski's supporting testimony is based upon such differences in the resistance components. *See, e.g.*, Ex. 2011 ¶ 128. However, we have credited Dr. Liu's testimony that a chain of transistors in both systems creates a resistance effect regardless of current flow in the steady state. *Supra* § II.F.1.b.2. We further agree with Petitioner that applying pre-

charging to mitigate program disturb (sought by both Lee and Zhao) relies on the creation of a potential difference to facilitate electron redistribution. Pet. Reply 17–18 (citing Ex. 1004, 1:52–56; Ex. 1005, 17:4–12; Ex. 1021 ¶¶ 72–78). We further credit Dr. Liu's testimony that Zhao's use of the same pre-charge voltages to not-yet-programmed word lines presents an issue of inadequate pre-charging that Lee addresses. Ex. 1021 ¶¶ 55–56; Pet. Reply 22–23. Consequently, we are persuaded by Petitioner that the chain resistance effects in Zhao and Lee permit the application of Lee's method of pre-charging to mitigate program disturb to be applicable and desirable in Zhao's method of applying pre-charging to mitigate program disturb.

Consequently, we determine that Petitioner has shown persuasive motivation for its combination.

2. Claims 1 and 11

In view of the foregoing, we determine that Petitioner has shown by a preponderance of the evidence, that claim 1 would have been obvious over the combined teachings of Zhao and Lee. Because claim 11 is asserted to be obvious over Zhao and Lee for essentially the same reasons as claim 1, with the same arguments presented in opposition, we further determine that claim 11 would have been obvious over the combined teachings of Zhao and Lee.

3. Claims 2, 3, 12, and 13

With respect to claims 2 and 12, Petitioner relies upon Lee's teachings of word line groups near the drain select transistor, with higher pre-bias voltage for closer groups. Pet. 68 (citing Ex. 1004, 8:32–37). Petitioner asserts that, when combined with Zhao's teachings, this results in Zhao's "first," "second," and "third" "group[s] … of word lines" (WL56-WL63,

WL64-WL71, and WL72-WL79) being "disposed in an order of distance from the selected word line" (WL50). *Id.* (citing Ex. 1003 ¶¶ 376–383).

With respect to claims 3 and 13, Petitioner further points to Zhao's drain side select layer SGD0 as the claimed select line, and SL50 as the selected word line, and three groups of word lines located therebetween. *Id.* at 69. Petitioner further points to its contentions for Lee. *Id.*

Petitioner's assertions for claims 2, 3, 12, and 13 are not disputed for any reason beyond those offered with respect to claims 1 and 11. PO Resp. 58. For the reasons expressed *supra* §§ II.D.3.b–c, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 2, 3, 12, and 13 would have been obvious over Zhao and Lee.

4. Claims 4 and 14

Claims 4 and 14 further limit the application of a bit line pre-pulse signal to the bit line during the pre-charge period. Petitioner asserts that Zhao teaches this by describing that "the unselected bit lines are raised to a pre-charge voltage Vprecharge (e.g., ~2 volts)" during the "t1-t3 . . . precharging" period." Pet. 54 (citing Ex. 1005, 22:39–44). Based on this uncontested evidence, Petitioner has shown by a preponderance of the evidence that claims 4 and 14 would have been obvious over Zhao and Lee.

5. Claims 5 and 15

Claims 5 and 15 further require that the first memory string and bit line are unselected. Petitioner asserts that Zhao teaches this by describing that it "pre-charges the channels of … unselected NAND strings ([i.e.] channels connected to unselected memory cells.)" Ex. 1005, 19:10-17. Petitioner further asserts that as part of this, Zhao applies a "pre-charge voltage" pulse to "unselected bit lines." Ex. 1005, 22:39–45; *see also* Fig. 13; Ex. 1003 ¶¶ 288-292. Based on this uncontested evidence,

Petitioner has shown by a preponderance of the evidence that claims 5 and 15 would have been obvious over Zhao and Lee.

6. Claim 6

Claim 6 further recites, "the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines." Petitioner asserts that this is taught by Zhao's description that during "pre-charging," "the selected word line WLn is raised to the pre-charge voltage…." Ex. 1005, 22:39–49. Petitioner further points to Zhao's description of a "program signal Vpgm … to the selected word line" during later programming. *Id. at* 14:49-51; Fig. 13; Ex. 1003 ¶¶ 293–296. Based on this uncontested evidence, Petitioner has shown by a preponderance of the evidence that claim 6 would have been obvious over Zhao and Lee.

7. Claims 7 and 16

Claims 7 and 16 further recite, "[the control circuit is configured to] apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the precharge period." Petitioner asserts that Zhao's memory includes "a top dummy word line of the plurality of word lines" because Zhao describes dummy word line layers DD0 and DD1 on the drain side. Pet. 56–57 (citing Ex. 1005, Fig. 4G). Petitioner further asserts that Zhao's description of dummy lines being operated in the same manner as unselected word lines indicates that the dummy lines also receive Vprecharge during the pre-charging time period. *Id.* at 57 (citing Ex. 1005, 24:11–13, 22:39–49; Ex. 1003 ¶¶ 297–306). Based on this uncontested evidence, Petitioner has shown by a preponderance of the evidence that claims 7 and 16 would have been obvious over Zhao and Lee.

8. Claims 8 and 17

Claims 8 and 17 further recite, "a voltage level of the top dummy word line pre-pulse signal is greater than that of the third word line pre-pulse signal." Petitioner asserts that Zhao's memory includes "a top dummy word line of the plurality of word lines" because Zhao describes dummy word line layers DD0 and DD1 on the drain side. Pet. 69–70 (citing Ex. 1005, Fig. 4G). Petitioner further asserts that Zhao's description of dummy lines being operated in the same manner as unselected word lines indicates that the dummy lines, located closest to the drain side select gate, receive an even higher voltage than the closest unselected word lines during the pre-charging time period. *Id.* at 70–72 (citing Ex. 1005, Fig. 4G; Ex. 1003 ¶¶ 391–395). Based on this uncontested evidence, Petitioner has shown by a preponderance of the evidence that claims 8 and 17 would have been obvious over Zhao and Lee.

9. Claim 18

Claim 18 further recites, "the top dummy word line is disposed between the third group of the plurality of word lines and the select gate line." Petitioner asserts that Zhao's "select gate line" (SGD0) is located at the top of its memory structure, and Zhao's "top dummy word lines" (DD0-DD1) are located immediately below the "select gate line" and above the third group of the plurality of word lines. Pet. 58 (citing Ex. 1005, Fig. 4G). Based on this uncontested evidence, Petitioner has shown by a preponderance of the evidence that claim 18 would have been obvious over Zhao and Lee.

10. Claims 9 and 19

Claims 9 and 19 further recite, "the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third

word line pre-pulse signal are positive." Petitioner asserts that Zhao teaches positive voltage levels by describing the voltage levels at positive values. Pet. 58–59. Based on this uncontested evidence, Petitioner has shown by a preponderance of the evidence that claims 9 and 19 would have been obvious over Zhao and Lee.

G. Obviousness over Yang

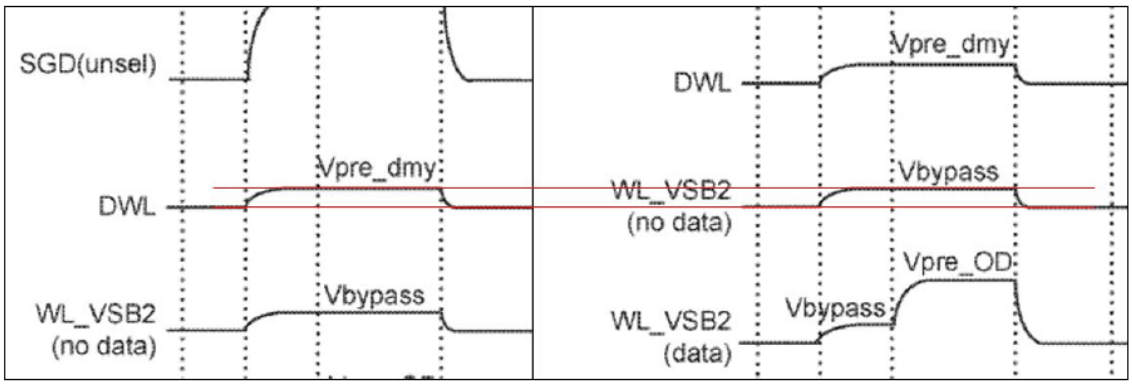
Petitioner asserts that claims 1–7, 9, 11–16, 18, and 19 would have been obvious over Yang. Pet. 71–89.

With respect to the limitation [1.E.4] at issue, Petitioner admits that "Yang does not provide numerical examples for all of its different pre-charge voltages." Pet. 81. However, Petitioner asserts that a person having ordinary skill in the art would have understood Yang to render this obvious. *Id.* In applying Yang, Petitioner asserts that the claimed first signal is taught by Yang's Vbypass signal, the claimed second signal is taught by Yang's Vpre_dmy signal, and the claimed third signal is taught by Yang's Vpre_OD signal. *Id.* Petitioner further asserts that Yang teaches that:

> "overdrive voltage Vpre_OD" is a high voltage "above all the data states" of the memory cells. The "bypass voltage" Vbypass can be a low voltage: it can be lower than all the various memory cell read states and is only required to be higher than Vev (the "voltage level to test whether a memory cell has been properly erased"). The "dummy pre-charge voltage" Vpre_dmy can be an intermediate voltage like 5V that is lower than Vpre_OD.

Pet. 82 (citing Ex. 1010, 20:53–55, 19:23–44, 20:64–21:5, 24:18–27; Ex. 1003 ¶¶ 455–460).

Patent Owner argues that Petitioner's assertions are unsupported and do not establish any relationship of the relative magnitude of Vpre_dmy as it relates to Vbypass. PO Resp. 58–64. Patent Owner contends that Yang illustrates these as having identical values:



PO Resp. 64 (citing Yang Fig. 8B). Patent Owner's annotated Figure 8B of Yang portrays Vpre_dmy and Vbypass pulses side-by-side with essentially parallel red lines spanning the top and bottom of each pulse. *Id.* Patent Owner contends that Petitioner has insufficiently explained the basis for its asserted relationship, because Petitioner does not clearly show support in the record for its assertions that Vpre_dmy have an intermediate value less than Vpre_OD, or that Vpre_dmy have any value different than that of Vbypass. *Id.* at 64. Patent Owner argues that having identical values for Vpre_dmy and Vbypass pulses conserves system resources. *Id.* at 65. Patent Owner further argues that Vpre_dmy is "applied exclusively to dummy memory cells," and thus, "has no inherent relationship with those described for Vpre_OD and Vbypass." PO Sur-reply 24.

Petitioner argues that Yang's figures may not be relied upon to show exact dimensions. Pet. Reply 24. Petitioner argues that Yang describes its three voltages, Vpre_OD, Vpre_dmy, and Vbypass, "in a way that makes plain that they have (or obviously could have) different magnitudes." *Id.* at 24–25. With respect to the relative values of Vpre_dmy and Vbypass, Petitioner argues that Yang describes Vpre_dmy as operable as a pass gate, meaning that it will conduct a current. *Id.* at 25. Petitioner asserts that because the threshold voltage to pass a current in Yang's memory cells is

"less than 5V," Vpre_dmy may be 5V. *Id.* (citing Ex. 1010, 24:18–27). Petitioner asserts that Yang describes Vbypass as "no greater than Vv7," and is intended to be ***lower*** than the memory cell threshold voltages. *Id.* (citing Ex. 1010, 20:64–66). Petitioner argues that Patent Owner has not disputed Dr. Liu's testimony that a person having ordinary skill in the art would conclude that Vpre_dmy has an intermediate value to that of Vpre_OD and Vbypass. *Id.*

We agree with Patent Owner that Petitioner has not persuasively shown a relationship of Vpre_dmy and Vbypass. Yang does not provide values for Vbypass, and although Yang describes Vv7 as its upper limit, Yang does not describe values for Vv7 either. *See* Ex. 1010, 20:15–21:5; Ex. 1003 ¶ 459. Dr. Liu describes Vv7 as the "memory's highest programmed state threshold voltage," but does not explain this conclusion. Ex. 2011 ¶ 124. Although Dr. Liu stated that Vv7 would be below 5V, Dr. Liu relies on sample *program state* voltages for a multilevel NAND cell. *Id.* (citing Ex. 1006, 117). However, Dr. Liu does not explain how these program voltages relate to Yang's *bypass* voltages. Consequently, Dr. Liu's testimony does not sufficiently support Petitioner's assertions.

Because Petitioner has not shown the claimed relationship of voltage levels for Yang's first, second, and third word lines, Petitioner has not shown that claim 1 would have been obvious over Yang. Petitioner's obviousness assertions for claims 2–7, 9, 11–16, 18, and 19 rely on the same flawed assertions, and accordingly, Petitioner has not shown that claims 1–7, 9, 11–16, 18, and 19 would have been obvious over Yang.

III. CONCLUSION

After reviewing the record and weighing the evidence offered by both parties, we determine that Petitioner shows by a preponderance of the evidence that claims 1–9 and 11–19 are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3, 6, 11–13	103	Lee	1–3, 6, 11–13	
1, 4–7, 9, 11, 14–16, 18, 19	103	Zhao		1, 4–7, 9, 11, 14–16, 18, 19
1–9, 11–19	103	Zhao, Lee	1–9, 11–19	
1–7, 9, 11–16, 18, 19	103	Yang		1–7, 9, 11–16, 18, 19
Overall Outcome			1–9, 11–19	

IV. ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner has established by a preponderance of the evidence that claims 1–9 and 11–19 are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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