22654 U.S. PTO 102704

PTO/SB/05 (09-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	1744.0330003
First Inventor	David F. SORRELLS
Title	Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology
Express Mail Label No.	

10/973917 22264 U.S. PTO 102704

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] **Fee Transmittal Form** (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. [ ] **Applicant claims small entity status.** See 37 CFR 1.27.
3. [X] **Specification** [*Total Pages* 96]
   Both the claims and abstract must start on a new page
   (For information on the preferred arrangement, see MPEP 608.01(a))
4. [X] **Drawing(s)** (*35 U.S.C. 113*) [*Total Sheets* 92]
5. **Oath or Declaration** [*Total Sheets* 5]
   a. [ ] Newly executed (original or copy)
   b. [X] A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [X] **Application Data Sheet.** See 37 CFR 1.76
7. [ ] **CD-ROM or CD-R** in duplicate, large table or Computer Program *(Appendix)*
   [ ] Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
   (if applicable, items a. – c. are required)
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

ADDRESS TO:
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. [X] **Assignment Papers** (cover sheet & document(s))
   Name of Assignee ParkerVision, Inc.
10. [X] **37 CFR 3.73(b) Statement** *(when there is an assignee)* [X] **Power of Attorney**
11. [ ] **English Translation Document** *(if applicable)*
12. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
13. [X] **Preliminary Amendment**
14. [X] **Return Receipt Postcard** (MPEP 503)
    (Should be specifically itemized)
15. [ ] **Certified Copy of Priority Document(s)**
    (if foreign priority is claimed)
16. [ ] **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
17. [X] Other: **Authorization under 37CFR 1.136(a)(3)**

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

[X] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: 09/569,044

Prior application information: *Examiner* Trinh, S. *Art Unit:* 2685

19. CORRESPONDENCE ADDRESS

[X] The address associated with Customer Number: 26111 *OR* [ ] Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

Signature		Date	10/27/04
Name (Print/Type)	Michael Q. Lee	Registration No. (Attorney/Agent)	35,239

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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U.S. PTO

PTO/SB/17 (10-03)
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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FEE TRANSMITTAL for FY 2005

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **$830.00**

Complete if Known	
Application Number	(to be assigned)
Filing Date	(herewith)
First Named Inventor	David F. SORRELLS
Examiner Name	(to be assigned)
Art Unit	(to be assigned)
Attorney Docket No.	1744.0330003

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☒ Credit card ☐ Money Order ☒ Other** ☐ None

☐ **Charge any deficiencies or credit any overpayments in Deposit Account: the fees to Deposit Acct. No. 19-0036.

Deposit Account Number: 19-0036

Deposit Account Name: Sterne, Kessler, Goldstein & Fox P.L.L.C.

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	$790.00
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) $790.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below	Fee Paid
Total Claims	20	- 20 **=	0	X		=
Independent Claims	3	- 3 **=	0	X		=
Multiple Dependent						=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	$40.00
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) $40.00

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Signature				Date	10/27/04

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*Admitted only in Maryland
*Admitted only in Virginia
•Practice Limited to Federal Agencies

October 27, 2004

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MLEE@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
Appl. No. (to be assigned); Filed: (herewith)
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/SB/05);

2. Fee Transmittal Form (PTO/SB/17);

3. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);

4. U.S. Utility Patent Application entitled:

Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology

and naming as inventors:

David F. SORRELLS, Michael J. BULTMAN, Robert W. COOK, Richard C. LOOKE and Charley D. MOSES, Jr.

the application consisting of:

a. An Application Data Sheet (37 C.F.R. § 1.76);

b. A copy of the executed Declaration, as originally filed in U.S. Appl. No. 09/569,044;

c. A specification containing:

i. 94 pages of description prior to the claims;

ii. 1 pages of claims (4 claims);

iii. a one (1) page abstract;

d. 92 sheets of drawings: (Figures 1A-1B-1C-1D, 2-5, 6A-6B-6C-6D-6E-6F-6G-6H-6I, 7-14, 15A-15B-15C-15D-15E-15F, 16-19, 20A-20B-20C-20D-20E-20F, 21, 22A-22B-22C-22D-22E-22F, 23A-23B-23C-23D-23E-23F, 24A-24B-24C-24D-24E-24F-24G-24H-24I-24J, 25A-25B-25C, 26A-26B-26C, 27A-27B-27C, 28-29, 30A-30B-30C, 31-44, 45A-45B-45C-45D, 46A-46B-46C-46D-46E, 47-48, 49A-49B-49C, 50, 51A-51B, 52A-52B-52C, 53-59, 60A-60B-60C, 61-63, 64A-64B-64C-64D-64E-64F, 65-68, 69A-69B, 70A-70B, 71A-71B-71C-71D-71E-71F, and 72);

5. Recordation Form Cover Sheet;

6. A copy of the executed Assignment to ParkerVision, Inc., recordation of which is hereby respectfully requested;

7. A copy of the executed Power of Attorney from Assignee as filed in U.S. Appl. No. 09/569,044;

8. A copy of the executed Statement under 37 C.F.R. § 3.73(b) from Assignee with a copy of the Assignment attached;

9. A Preliminary Amendment under 37 C.F.R. § 1.115;

10. Credit Card Payment Form (PTO-2038) for $830.00 to cover:

$790.00 Patent Application fee;
$ 40.00 Assignment Recordation fee; and

11. Two (2) return postcards.

It is respectfully requested that, of the two attached postcards, one be stamped with the filing date of these documents and returned to our courier, and the other, prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/NDD/sjc
Enclosures

323095_1.DOC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: (to be assigned)
SORRELLS *et al.*	Art Unit: (to be assigned)
Appl. No.: (to be assigned)	Examiner: (to be assigned)
Filed: (herewith)	Atty. Docket: 1744.0330003
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**	

Authorization to Treat a Reply as Incorporating an Extension of Time Under 37 C.F.R. § 1.136(a)(3)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 10/27/09

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

323075_1.doc

Certificate Under 37 C.F.R. § 3.73(b)

Applicant/Patent Owner: **David F. SORRELLS *et al.***

Application No./Patent No.: **09/569,044** Filed/Issue Date: **May 10, 2000**

Entitled: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**

ParkerVision, Inc., a **Corporation**,
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency,etc.)

states that it is:

1. [X] **the assignee of the entire right, title, and interest, or**

2. [ ] an assignee of an undivided part interest

in the patent application/patent identified above by virtue of either:

A. [X] **An Assignment from the inventor(s) of the patent application/patent identified above, for which a copy thereof is attached.**

OR

B. [ ] A chain of title from the inventor(s) of the patent application/patent identified above to the current assignee as shown below:

1. From: _____ To: _____
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Reel _____, Frame _____, or for which a copy thereof is attached.

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[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[X] Copies of assignments or other documents in the chain of title are attached.

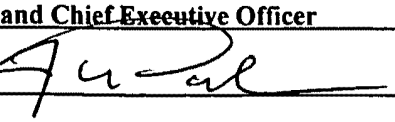
[**NOTE:** A separate copy (*i.e.*, the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the PTO. See MPEP 302-302.8]

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

Date: X 10-28-00

Name: **Jeffrey L. Parker**

Title: **Chairman and Chief Executive Officer**

Signature: X 

Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology

Inventors: **David F. Sorrells**
Michael J. Bultman
Robert W. Cook
Richard C. Looke
Charley D. Moses, Jr.

Cross-Reference to Other Applications

This is a continuation-in-part application of the following pending U.S. applications, all of which are herein incorporated by reference in their entireties:

"Additional Applications of Frequency Translation," Ser. No. 09/261,129, filed March 3, 1999, Attorney Docket No. 1744.0140001.

"Universal Frequency Translation and Applications of Same," Ser. No. 09/514,004, filed February 25, 2000, Attorney Docket No. 1744.0140004.

"Family Radio System with Multi-Mode and Multi-Band Functionality," Ser. No. 09/476,093, filed January 3, 2000, Attorney Docket No. 1744.0260001.

"Multi-Mode, Multi-Band Communications System," Ser. No. 09/476,330, filed January 3, 2000, Attorney Docket No. 1744.0330001.

"Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, filed March 14, 2000, Attorney Docket No. 1744.0450003.

"DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Ser. No. 09/526,041, filed March 14, 2000, Attorney Docket No. 1744.0880000.

This application also claims the benefit of U.S. Provisional Application "Wireless Telephone Using Universal Frequency and Translation," Ser. No. 60/195,328, filed April 10, 2000, Attorney Docket No. 1744.0070000, and U.S. Provisional Application "Wireless Local Area Network (LAN) Using Universal Frequency Translation Technology," Ser. No. 60/147,129 filed August 4, 1999, Attorney Docket No. 1744.0630000, both of which are herein incorporated by reference in their entireties.

The following patents and patent applications of common assignee are related to the present application, and are all herein incorporated by reference in their entireties:

"Method and System for Down-Converting an Electromagnetic Signal," Ser. No. 09/176,022, filed October 21, 1998, Attorney Docket No. 1744.0010000, now U.S. Patent No. 6,061,551, issued May 9, 2000.

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, Attorney Docket No. 1744.0020000.

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998, Attorney Docket No. 1744.0030000, now U.S. Patent No. 6,061,555, issued May 9, 2000.

"Integrated Frequency Translation and Selectivity," Ser. No. 09/175,966, filed October 21, 1998, Attorney Docket No. 1744.0130000, now U.S Patent No. 6,049,706, issued April 11, 2000.

"Integrated Frequency Translation And Selectivity With a Variety of Filter Embodiments," Ser. No. 09/293,283, filed April 16, 1999, Attorney Docket No. 1744.0130001.

"Matched Filter Characterization and Implementation of Universal Frequency Translation Method and Apparatus," Ser. No. 09/521,879, filed March 9, 2000, Attorney Docket No. 1744.0010003.

"Method and System for Down-Converting an Electromagnetic Signal, Transforms for Same, and Aperture Relationships," Ser. No. To Be Assigned, filed April 14, 2000, Attorney Docket No. 1744.0010009.

Background of the Invention

Field of the Invention

The present invention is generally related to multi-mode communications devices, and more particularly, to multi-mode communications devices implemented using universal frequency translation technology.

Related Art

Recent developments in computing and communications systems seek to enhance the performance and interoperability of devices. These devices, which include personal digital assistants (PDAs), mobile phones, set-top boxes, handheld personal computers, pagers, laptop personal computers, as well as home and office appliances, are being constructed to handle the tasks of traditional systems. These systems are currently constructed for receiving information signals for only a few platforms. Typically, the platforms available for a given device are predetermined. These systems can suffer from the disadvantage of being obsolete within a year or so of production, as well as being relatively expensive in terms of cost and power consumption. Conventional wireless communications circuitry is complex and has a large number of circuit parts. This complexity and high parts count increases overall cost. Additionally, higher part counts result in higher power consumption, which is undesirable, particularly in battery powered units.

Consequently, it is desirable to provide a method and apparatus for a universal platform module (UPM) for devices.

Summary of the Invention

The present invention is directed to a universal platform module (UPM). The UPM includes at least one universal frequency translation (UFT) module implemented for signal reception, transmission and/or processing. In one embodiment, the UMP also includes a control module for operating the UFT module for any selected platform or combination of platforms.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings.

Brief Description of the Figures

The invention shall be described with reference to the accompanying figures, wherein:

FIG. 1A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention;

FIG. 1D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 2 is a block diagram of a universal frequency translation (UFT) module according to an alternative embodiment of the invention;

FIG. 3 is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 4 is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 5 is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention;

FIGS. 6A-6I illustrate example waveforms used to describe the operation of the UFU module;

FIG. 7 illustrates a UFT module used in a receiver according to an embodiment of the invention;

FIG. 8 illustrates a UFT module used in a transmitter according to an embodiment of the invention;

FIG. 9 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using a UFT module of the invention;

FIG. 10 illustrates a transceiver according to an embodiment of the invention;

FIG. 11 illustrates a transceiver according to an alternative embodiment of the invention;

FIG. 12 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention;

FIG. 13 illustrates a UFT module used in a unified down-conversion and filtering (UDF) module according to an embodiment of the invention;

FIG. 14 illustrates an example receiver implemented using a UDF module according to an embodiment of the invention;

FIGS. 15A-15F illustrate example applications of the UDF module according to embodiments of the invention;

FIG. 16 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR)

components of the invention, wherein the receiver may be further implemented using one or more UFD modules of the invention;

FIG. 17 illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention;

FIG. 18 is a table of example values at nodes in the UDF module of FIG. 17;

FIG. 19 is a detailed diagram of an example UDF module according to an embodiment of the invention;

FIGS. 20A and 20A-1 are example aliasing modules according to embodiments of the invention;

FIGS. 20B-20F are example waveforms used to describe the operation of the aliasing modules of FIGS. 20A and 20A-1;

FIG. 21 illustrates an enhanced signal reception system according to an embodiment of the invention;

FIGS. 22A-22F are example waveforms used to describe the system of FIG. 21;

FIG. 23A illustrates an example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23B and 23C are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 23D illustrates another example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23E and 23F are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 24A illustrates an example receiver in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 24B-24J are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 25A illustrates a high level block diagram of an example conventional multi-mode device;

FIG. 25B illustrates a detailed block diagram of a conventional receiver;

FIG. 25C illustrates a detailed block diagram of a conventional transmitter;

FIG. 26A - 26C illustrate example universal platform modules according to embodiments of the invention;

FIGS. 27A - 27C illustrate example universal platform sub-module receivers according to embodiments of the invention;

FIG. 28 illustrates an example UFD module in greater detail according to an embodiment of the invention;

FIG. 29 illustrates an exemplary I/Q modulation embodiment of a receiver, according to the invention;

FIGS. 30A-30C illustrate example universal platform sub-module transmitters according to embodiments of the invention;

FIG. 31 illustrates further detail of an example modulator of FIG. 30B, operating in a pulse modulation (PM) mode, according to an embodiment of the invention;

FIG. 32 illustrates an universal platform module according to an embodiment of the invention;

FIG. 33 illustrates an UFU module in greater detail according to an embodiment of the invention;

FIGS. 34 and 35 illustrate exemplary block diagrams of a transmitter operating in an I/Q modulation mode, according to embodiments of the invention;

FIG. 36 illustrates a block diagram of a receiver incorporating unified down-convert and filtering according to an embodiment of the invention;

FIG. 37 illustrates a high level block diagram of an universal platform sub-module transceiver implementation according to an embodiment of the invention;

FIG. 38 illustrates a high level block diagram of universal platform sub-module receiver and transmitter implementations according to an embodiment of the invention;

FIG. 39 shows some possible protocol/bearer service combinations;

FIG. 40 shows possible representative groupings of network links;

FIG. 41 illustrates a high level block diagram of an universal platform sub-module transceiver implementation according to an embodiment of the invention;

FIG. 42 shows a chart of some standards, protocols, and bearer services;

FIG. 43 illustrates a high level block diagram of a specific implementation of device employing a universal platform module;

FIG. 44 illustrates a high level block diagram of a flexible implementation of a device employing a universal platform module;

FIGS. 45A-D illustrate example implementations of a switch module according to embodiments of the invention;

FIGS. 46A-D illustrate example aperture generators;

FIG. 46E illustrates an oscillator according to an embodiment of the present invention;

FIG. 47 illustrates an energy transfer system with an optional energy transfer signal module according to an embodiment of the invention;

FIG. 48 illustrates an aliasing module with input and output impedance match according to an embodiment of the invention;

FIG. 49A illustrates an example pulse generator;

FIGS. 49B and C illustrate example waveforms related to the pulse generator of FIG. 49A;

FIG. 50 illustrates an example energy transfer module with a switch module and a reactive storage module according to an embodiment of the invention;

FIGS. 51A-B illustrate example energy transfer systems according to embodiments of the invention;

FIG. 52A illustrates an example energy transfer signal module according to an embodiment of the present invention;

FIG. 52B illustrates a flowchart of state machine operation according to an embodiment of the present invention;

FIG. 52C is an example energy transfer signal module;

FIG. 53 is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock according to an embodiment of the present invention;

FIG. 54 shows example simulation waveforms for the circuit of FIG. 53 according to embodiments of the present invention;

FIG. 55 is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101 MHZ clock according to an embodiment of the present invention;

FIG. 56 shows example simulation waveforms for the circuit of FIG. 55 according to embodiments of the present invention;

FIG. 57 is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock according to an embodiment of the present invention;

FIG. 58 shows example simulation waveforms for the circuit of FIG. 57 according to an embodiment of the present invention;

FIG. 59 shows a schematic of the circuit in FIG. 53 connected to an FSK source that alternates between 913 and 917 MHZ at a baud rate of 500 Kbaud according to an embodiment of the present invention;

FIG. 60A illustrates an example energy transfer system according to an embodiment of the invention;

FIGS. 60B-C illustrate example timing diagrams for the example system of FIG. 60A;

FIG. 61 illustrates an example bypass network according to an embodiment of the invention;

FIG. 62 illustrates an example bypass network according to an embodiment of the invention;

FIG. 63 illustrates an example embodiment of the invention;

FIG. 64A illustrates an example real time aperture control circuit according to an embodiment of the invention;

FIG. 64B illustrates a timing diagram of an example clock signal for real time aperture control, according to an embodiment of the invention;

FIG. 64C illustrates a timing diagram of an example optional enable signal for real time aperture control, according to an embodiment of the invention;

FIG. 64D illustrates a timing diagram of an inverted clock signal for real time aperture control, according to an embodiment of the invention;

FIG. 64E illustrates a timing diagram of an example delayed clock signal for real time aperture control, according to an embodiment of the invention;

FIG. 64F illustrates a timing diagram of an example energy transfer including pulses having apertures that are controlled in real time, according to an embodiment of the invention;

FIG.65 illustrates an example embodiment of the invention;

FIG.66 illustrates an example embodiment of the invention;

FIG.67 illustrates an example embodiment of the invention;

FIG.68 illustrates an example embodiment of the invention;

FIG.69A is a timing diagram for the example embodiment of FIG. 65;

FIG.69B is a timing diagram for the example embodiment of FIG. 66;

FIG.70A is a timing diagram for the example embodiment of FIG. 67;

FIG.70B is a timing diagram for the example embodiment of FIG. 68;

FIG.71A illustrates and example embodiment of the invention;

FIG.71B illustrates example equations for determining charge transfer, in accordance with the present invention;

FIG.71C illustrates relationships between capacitor charging and aperture, in accordance with an embodiment of the present invention;

FIG.71D illustrates relationships between capacitor charging and aperture, in accordance with an embodiment of the present invention;

FIG.71E illustrates power-charge relationship equations, in accordance with an embodiment of the present invention;

FIG.71F illustrates insertion loss equations, in accordance with an embodiment of the present invention; and

FIG. 72 shows the original FSK waveform 5902 and the down-converted waveform 5904;

The invention will now be described with reference to the accompanying drawings. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is generally indicated by the left-most digit(s) in the corresponding reference number.

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1. Overview of the Invention

The present invention is directed to a universal platform module (UPM) that operates for and/or within a device. Devices include, without limitation, phones, personal digital/data assistants (PDAs), smart appliances, personal computers (PCs), set-top boxes, networked outlets (printers, projectors, facsimiles), servers, gateways, other computing and/or data processing devices, etc. The UPM may include one or more receivers, transmitters, and/or transceivers, as well as other components such as local oscillators, switches, amplifiers, etc. According to embodiments of the invention, at least some of these components are implemented using universal frequency translation (UFT) modules. The UFT module performs frequency translation operations. Embodiments of the present invention incorporating various

applications of the UFT module are described below. The UPM provides new functionality, and/or optionally works alternatively to existing components. The UPM utilizes protocols and/or bearer services and/or combinations thereof to exchange and/or process information with other components on any given network or networks (or any communication medium, for that matter). Generally, protocols, such as but not limited to Wireless Application Protocol (WAP), Jini, Java Virtual Machine (JVM), Bluetooth, IEEE 802.11, TCP/IP, UDP, HAVi, Salutation, Infrared (IR, IRDA), Service Location Protocol (SLP), Universal Plug-n-Play (UPnP, Simple Service Discovery Protocol (SSDP)), etc., provide the format for the transfer of data. Other procedures, methods, protocols, and/or standards may be combined with these protocols to enable and/or support this, similar, and additional functionalities. For example, in the case of Bluetooth, the transport standard is also supplied.

Generally, protocols call upon bearer services (also known as standards), such as CDMA (IS-95, IS-707), US-TDMA (IS-136), W-CDMA, EDGE, IS-95C, SMS, GSM (900, 1800, 1900 MHz), DataTAC, iDEN (ESMR), CDPD, dDECT, Project Angel, LMDS, MMDS, ARDIS, Mobitex, AMPS, etc. These bearer services can be classified into generations (Gs), several of which are shown in FIG. 42. The bearer services are called upon to provide the communication pipeline (such as a wired or wireless pipeline) for the device to interact with the network. It is noted that, while the invention is sometimes described herein for example purposes as involving wireless communication, the invention is applicable to any communication medium, including without limitation any wireless or wired communication medium.

Generally, platforms are layers on which protocols and bearer services are implemented and/or enabled. Platforms may be implemented using hardware, software, or combinations thereof. Conventional platforms require specialized circuitry for each type of protocol and/or bearer service. According to the invention, a UPM is enabled by one or more UFT modules on a layer with logic and/or circuitry

and/or software (or combinations thereof) for any number/combination of protocols and bearer services.

In one embodiment, the UPM includes a UFT module for connecting to/interacting with any network using any protocol/bearer service combination. This embodiment provides the benefit of reduced circuitry over conventional implementations. Furthermore, the UPM can perform multi-platform operations nearly simultaneously. Such operation by the invention is sometimes referred to herein as "apparent simultaneous operation" or "virtual simultaneous operation." For example, the UFT module can switch between a wireless local area network (WLAN) and a wide area network (WAN) and thus, communicate with components on both networks.

In another embodiment, through the use of more than one UFT module, multiple protocols and multiple bearer services can be employed simultaneously. Thus, actual simultaneous multi-operation is possible. Further, components for specific protocols and/or bearer services are included in the UPM's control module which may be upgraded and/or reprogrammed to provide support for additional platforms.

Universal platform modules exhibit multiple advantages by using UFT modules. These advantages include, but are not limited to, lower power consumption, longer power source life, fewer parts, lower cost, less tuning, and more effective signal transmission and reception. The UPM of the present invention can receive and transmit signals across a broad frequency range. The structure and operation of embodiments of the UFT module, and various applications of the same are described in detail in the following sections.

2. *Universal Frequency Translation*

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

FIG. 1A illustrates a universal frequency translation (UFT) module 102 according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

As indicated by the example of FIG. 1A, some embodiments of the UFT module 102 include three ports (nodes), designated in FIG. 1A as Port 1, Port 2, and Port 3. Other UFT embodiments include other than three ports.

Generally, the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module 102 (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

An example embodiment of the UFT module 103 is generally illustrated in FIG. 1B. Generally, the UFT module 103 includes a switch 106 controlled by a control signal 108. The switch 106 is said to be a controlled switch.

As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. 2 illustrates an example UFT module 202. The example UFT module 202 includes a diode 204 having two ports, designated as Port 1 and Port 2/3. This embodiment does not include a third port, as indicated by the dotted line around the "Port 3" label.

The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

For example, a UFT module 115 can be used in a universal frequency down-conversion (UFD) module 114, an example of which is shown in FIG. 1C. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

As another example, as shown in FIG. 1D, a UFT module 117 can be used in a universal frequency up-conversion (UFU) module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal.

These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

3. Frequency Down-conversion

The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in co-pending U.S. Patent Application entitled "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551, the full disclosure of which is incorporated herein by reference, as well as other cases cited above. A relevant portion of the above mentioned patent application

is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. 20A illustrates an aliasing module 2000 for down-conversion using a universal frequency translation (UFT) module 2002 which down-converts an EM input signal 2004. In particular embodiments, aliasing module 2000 includes a switch 2008 and a capacitor 2010. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 20A-1), the capacitor 2010 is in series with the input signal 2004 and the switch 2008 is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module 2000 with UFT module 2002 can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal 2004.

In one implementation, aliasing module 2000 down-converts the input signal 2004 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 2000 down-converts the input signal 2004 to a demodulated baseband signal. In yet another implementation, the input signal 2004 is a frequency modulated (FM) signal, and the aliasing module 2000 down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal 2006 includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 2004. In this embodiment, the control signal 2006 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 2004. Preferably, the frequency of control signal 2006 is much less than the input signal 2004.

A train of pulses 2018 as shown in FIG. 20D controls the switch 2008 to alias the input signal 2004 with the control signal 2006 to generate a down-converted output signal 2012. More specifically, in an embodiment, switch 2008 closes on a first edge of each pulse 2020 of FIG. 20D and opens on a second edge of each pulse. When the switch 2008 is closed, the input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal to the capacitor 2010. The charge stored during successive pulses forms down-converted output signal 2012.

Exemplary waveforms are shown in FIGS. 20B-20F.

FIG. 20B illustrates an analog amplitude modulated (AM) carrier signal 2014 that is an example of input signal 2004. For illustrative purposes, in FIG. 20C, an analog AM carrier signal portion 2016 illustrates a portion of the analog AM carrier signal 2014 on an expanded time scale. The analog AM carrier signal portion 2016 illustrates the analog AM carrier signal 2014 from time t_0 to time t_1.

FIG. 20D illustrates an exemplary aliasing signal 2018 that is an example of control signal 2006. Aliasing signal 2018 is on approximately the same time scale as the analog AM carrier signal portion 2016. In the example shown in FIG. 20D, the aliasing signal 2018 includes a train of pulses 2020 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 2020 repeat at an aliasing rate, or pulse repetition rate of aliasing signal 2018. The aliasing rate is determined as described below, and further described in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Serial No. 09/176,022, issued as U.S. Patent No. 6,061,551.

As noted above, the train of pulses 2020 (i.e., control signal 2006) control the switch 2008 to alias the analog AM carrier signal 2016 (i.e., input signal 2004) at the aliasing rate of the aliasing signal 2018. Specifically, in this embodiment, the switch 2008 closes on a first edge of each pulse and opens on a second edge of each pulse.

When the switch 2008 is closed, input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal 2004 to the capacitor 2010. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 2022 form down-converted signal portion 2024 (FIG. 20E) that corresponds to the analog AM carrier signal portion 2016 (FIG. 20C) and the train of pulses 2020 (FIG. 20D). The charge stored during successive under-samples of AM carrier signal 2014 form the down-converted signal 2024 (FIG. 20E) that is an example of down-converted output signal 2012 (FIG. 20A). In FIG. 20F, a demodulated baseband signal 2026 represents the demodulated baseband signal 2024 after filtering on a compressed time scale. As illustrated, down-converted signal 2026 has substantially the same "amplitude envelope" as AM carrier signal 2014. Therefore, FIGS. 20B-20F illustrate down-conversion of AM carrier signal 2014.

The waveforms shown in FIGS. 20B-20F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Serial No. 09/176,022, issued as U.S. Patent No. 6,061,551.

The aliasing rate of control signal 2006 determines whether the input signal 2004 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 2004, the aliasing rate of the control signal 2006, and the down-converted output signal 2012 are illustrated below:

$$\text{(Freq. of input signal 2004)} = n\bullet\text{(Freq. of control signal 2006)} \pm \text{(Freq. of down-converted output signal 2012)}$$

For the examples contained herein, only the "+" condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal 2004 (e.g., $n = 0.5$, 1, 2, 3, . . .).

When the aliasing rate of control signal 2006 is off-set from the frequency of input signal 2004, or off-set from a harmonic or sub-harmonic thereof, input signal 2004 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 2004. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal 2006 would be calculated as follows:

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$

$$(901\ MHZ - 1\ MHZ)/n = 900/n$$

For n = 0.5, 1, 2, 3, 4, etc., the frequency of the control signal 2006 would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signals, and exemplary methods and systems thereof, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Serial No. 09/176,022, issued as U.S. Patent No. 6,061,551.

Alternatively, when the aliasing rate of the control signal 2006 is substantially equal to the frequency of the input signal 2004, or substantially equal to a harmonic or sub-harmonic thereof, input signal 2004 is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-

sampling pulses occur at the same point of subsequent cycles of the input signal 2004. As a result, the under-samples form a constant output baseband signal. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 2006 would be calculated as follows:

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$

$$(900\ MHZ - 0\ MHZ)/n = 900\ MHZ/n$$

For n = 0.5, 1, 2, 3, 4, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Serial No. 09/176,022, issued as U.S. Patent No. 6,061,551.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1 + F_2) \div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal 2006 would be calculated as follows:

Frequency of the input $= (F_1 + F_2) \div 2$

$= (899 \text{ MHZ} + 901 \text{ MHZ}) \div 2$

$= 900 \text{ MHZ}$

Frequency of the down-converted signal = 0 (i.e., baseband)

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$

$$(900 \text{ MHZ} - 0 \text{ MHZ})/n = 900 \text{ MHZ}/n$$

For n = 0.5, 1, 2, 3, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal 2006 should be substantially equal to:

(900 MHZ - 0 MHZ)/n = 900 MHZ/n, or

(901 MHZ - 0 MHZ)/n = 901 MHZ/n.

For the former case of 900 MHZ/n, and for n = 0.5, 1, 2, 3, 4, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/n, and for n = 0.5, 1, 2, 3, 4, etc., the frequency of the control signal 2006 should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The

frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Serial No. 09/176,022, issued as U.S. Patent No. 6,061,551.

In an embodiment, the pulses of the control signal 2006 have negligible apertures that tend towards zero. This makes the UFT module 2002 a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal 2006 have non-negligible apertures that tend away from zero. This makes the UFT module 2002 a lower input impedance device. This allows the lower input impedance of the UFT module 2002 to be substantially matched with a source impedance of the input signal 2004. This also improves the energy transfer from the input signal 2004 to the down-converted output signal 2012, and hence the efficiency and signal to noise (s/n) ratio of UFT module 2002.

Exemplary systems and methods for generating and optimizing the control signal 2006, and for otherwise improving energy transfer and s/n ratio, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Serial No. 09/176,022, issued as U.S. Patent No. 6,061,551.

When the pulses of the control signal 2006 have non-negligible apertures, the aliasing module 2000 is referred to interchangeably herein as an energy transfer module or a gated transfer module, and the control signal 2006 is referred to as an energy transfer signal. Exemplary systems and methods for generating and optimizing

the control signal 2006 and for otherwise improving energy transfer and/or signal to noise ratio in an energy transfer module are described below.

3.1. Optional Energy Transfer Signal Module

FIG. 47 illustrates an energy transfer system 4701 that includes an optional energy transfer signal module 4702, which can perform any of a variety of functions or combinations of functions including, but not limited to, generating the energy transfer signal 4506.

In an embodiment, the optional energy transfer signal module 4702 includes an aperture generator, an example of which is illustrated in FIG. 46C as an aperture generator 4620. The aperture generator 4620 generates non-negligible aperture pulses 4626 from an input signal 4624. The input signal 4624 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave, etc. Systems for generating the input signal 4624 are described below.

The width or aperture of the pulses 4626 is determined by delay through the branch 4622 of the aperture generator 4620. Generally, as the desired pulse width increases, the difficulty in meeting the requirements of the aperture generator 4620 decrease. In other words, to generate non-negligible aperture pulses for a given EM input frequency, the components utilized in the example aperture generator 4620 do not require as fast reaction times as those that are required in an under-sampling system operating with the same EM input frequency.

The example logic and implementation shown in the aperture generator 4620 are provided for illustrative purposes only, and are not limiting. The actual logic employed can take many forms. The example aperture generator 4620 includes an optional inverter 4628, which is shown for polarity consistency with other examples provided herein.

An example implementation of the aperture generator 4620 is illustrated in FIG. 46D. Additional examples of aperture generation logic are provided in FIGS. 46A and 46B. FIG. 46A illustrates a rising edge pulse generator 4640, which generates pulses 4626 on rising edges of the input signal 4624. FIG. 46B illustrates a falling edge pulse generator 4650, which generates pulses 4626 on falling edges of the input signal 4624.

In an embodiment, the input signal 4624 is generated externally of the energy transfer signal module 4702, as illustrated in FIG. 47. Alternatively, the input signal 4724 is generated internally by the energy transfer signal module 4702. The input signal 4624 can be generated by an oscillator, as illustrated in FIG. 46E by an oscillator 4630. The oscillator 4630 can be internal to the energy transfer signal module 4702 or external to the energy transfer signal module 4702. The oscillator 4630 can be external to the energy transfer system 4701. The output of the oscillator 4630 may be any periodic waveform.

The type of down-conversion performed by the energy transfer system 4701 depends upon the aliasing rate of the energy transfer signal 4506, which is determined by the frequency of the pulses 4626. The frequency of the pulses 4626 is determined by the frequency of the input signal 4624. For example, when the frequency of the input signal 4624 is substantially equal to a harmonic or a sub-harmonic of the EM signal 4504, the EM signal 4504 is directly down-converted to baseband (e.g. when the EM signal is an AM signal or a PM signal), or converted from FM to a non-FM signal. When the frequency of the input signal 4624 is substantially equal to a harmonic or a sub-harmonic of a difference frequency, the EM signal 4504 is down-converted to an intermediate signal.

The optional energy transfer signal module 4702 can be implemented in hardware, software, firmware, or any combination thereof.

3.2 Smoothing the Down-Converted Signal

Referring back to FIG. 20A, the down-converted output signal 2012 may be smoothed by filtering as desired.

3.3. Impedance Matching

The energy transfer module 2000 has input and output impedances generally defined by (1) the duty cycle of the switch module (i.e., UFT 2002), and (2) the impedance of the storage module (e.g., capacitor 2010), at the frequencies of interest (e.g. at the EM input, and intermediate/baseband frequencies).

Starting with an aperture width of approximately ½ the period of the EM signal being down-converted as a preferred embodiment, this aperture width (e.g. the "closed time") can be decreased. As the aperture width is decreased, the characteristic impedance at the input and the output of the energy transfer module increases. Alternatively, as the aperture width increases from ½ the period of the EM signal being down-converted, the impedance of the energy transfer module decreases.

One of the steps in determining the characteristic input impedance of the energy transfer module could be to measure its value. In an embodiment, the energy transfer module's characteristic input impedance is 300 ohms. An impedance matching circuit can be utilized to efficiently couple an input EM signal that has a source impedance of, for example, 50 ohms, with the energy transfer module's impedance of, for example, 300 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary impedance directly or the use of an impedance match circuit as described below.

Referring to FIG. 48, a specific embodiment using an RF signal as an input, assuming that the impedance 4812 is a relatively low impedance of approximately 50 Ohms, for example, and the input impedance 4816 is approximately 300 Ohms, an

initial configuration for the input impedance match module 4806 can include an inductor 5006 and a capacitor 5008, configured as shown in FIG. 50. The configuration of the inductor 5006 and the capacitor 5008 is a possible configuration when going from a low impedance to a high impedance. Inductor 5006 and the capacitor 5008 constitute an L match, the calculation of the values which is well known to those skilled in the relevant arts.

The output characteristic impedance can be impedance matched to take into consideration the desired output frequencies. One of the steps in determining the characteristic output impedance of the energy transfer module could be to measure its value. Balancing the very low impedance of the storage module at the input EM frequency, the storage module should have an impedance at the desired output frequencies that is preferably greater than or equal to the load that is intended to be driven (for example, in an embodiment, storage module impedance at a desired 1MHz output frequency is 2K ohm and the desired load to be driven is 50 ohms). An additional benefit of impedance matching is that filtering of unwanted signals can also be accomplished with the same components.

In an embodiment, the energy transfer module's characteristic output impedance is 2K ohms. An impedance matching circuit can be utilized to efficiently couple the down-converted signal with an output impedance of, for example, 2K ohms, to a load of, for example, 50 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary load impedance directly or the use of an impedance match circuit as described below.

When matching from a high impedance to a low impedance, a capacitor 5014 and an inductor 5016 can be configured as shown in FIG. 50. The capacitor 5014 and the inductor 5016 constitute an L match, the calculation of the component values being well known to those skilled in the relevant arts.

The configuration of the input impedance match module 4806 and the output impedance match module 4808 are considered to be initial starting points for

impedance matching, in accordance with the present invention. In some situations, the initial designs may be suitable without further optimization. In other situations, the initial designs can be optimized in accordance with other various design criteria and considerations.

As other optional optimizing structures and/or components are utilized, their affect on the characteristic impedance of the energy transfer module should be taken into account in the match along with their own original criteria.

3.4 Tanks and Resonant Structures

Resonant tank and other resonant structures can be used to further optimize the energy transfer characteristics of the invention. For example, resonant structures, resonant about the input frequency, can be used to store energy from the input signal when the switch is open, a period during which one may conclude that the architecture would otherwise be limited in its maximum possible efficiency. Resonant tank and other resonant structures can include, but are not limited to, surface acoustic wave (SAW) filters, dielectric resonators, diplexers, capacitors, inductors, etc.

An example embodiment is shown in FIG. 60A. Two additional embodiments are shown in FIG. 55 and FIG. 63. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention. These implementations take advantage of properties of series and parallel (tank) resonant circuits.

FIG. 60A illustrates parallel tank circuits in a differential implementation. A first parallel resonant or tank circuit consists of a capacitor 6038 and an inductor 6020 (tank1). A second tank circuit consists of a capacitor 6034 and an inductor 6036 (tank2).

As is apparent to one skilled in the relevant art(s), parallel tank circuits provide:

low impedance to frequencies below resonance;

low impedance to frequencies above resonance; and

high impedance to frequencies at and near resonance.

In the illustrated example of FIG. 60A, the first and second tank circuits resonate at approximately 920 MHz. At and near resonance, the impedance of these circuits is relatively high. Therefore, in the circuit configuration shown in FIG 60A, both tank circuits appear as relatively high impedance to the input frequency of 950 MHz, while simultaneously appearing as relatively low impedance to frequencies in the desired output range of 50 MHz.

An energy transfer signal 6042 controls a switch 6014. When the energy transfer signal 6042 controls the switch 6014 to open and close, high frequency signal components are not allowed to pass through tank1 or tank2. However, the lower signal components (50Mhz in this embodiment) generated by the system are allowed to pass through tank1 and tank2 with little attenuation. The effect of tank1 and tank2 is to further separate the input and output signals from the same node thereby producing a more stable input and output impedance. Capacitors 6018 and 6040 act to store the 50 MHz output signal energy between energy transfer pulses.

Further energy transfer optimization is provided by placing an inductor 6010 in series with a storage capacitor 6012 as shown. In the illustrated example, the series resonant frequency of this circuit arrangement is approximately 1 GHz. This circuit increases the energy transfer characteristic of the system. The ratio of the impedance of inductor 6010 and the impedance of the storage capacitor 6012 is preferably kept relatively small so that the majority of the energy available will be transferred to storage capacitor 6012 during operation. Exemplary output signals A and B are illustrated in FIGs. 60B and 60C, respectively.

In FIG. 60A, circuit components 6004 and 6006 form an input impedance match. Circuit components 6032 and 6030 form an output impedance match into a 50 ohm resistor 6028. Circuit components 6022 and 6024 form a second output impedance match into a 50 ohm resistor 6026. Capacitors 6008 and 6012 act as storage capacitors for the embodiment. Voltage source 6046 and resistor 6002 generate a 950 MHz signal with a 50 ohm output impedance, which are used as the input to the circuit. Circuit element 6016 includes a 150 MHz oscillator and a pulse generator, which are used to generate the energy transfer signal 6042.

FIG. 55 illustrates a shunt tank circuit 5510 in a single-ended to-single-ended system 5512. Similarly, FIG. 63 illustrates a shunt tank circuit 6310 in a system 6312. The tank circuits 5510 and 6310 lower driving source impedance, which improves transient response. The tank circuits 5510 and 6310 are able store the energy from the input signal and provide a low driving source impedance to transfer that energy throughout the aperture of the closed switch. The transient nature of the switch aperture can be viewed as having a response that, in addition to including the input frequency, has large component frequencies above the input frequency, (i.e. higher frequencies than the input frequency are also able to effectively pass through the aperture). Resonant circuits or structures, for example resonant tanks 5510 or 6310, can take advantage of this by being able to transfer energy throughout the switch's transient frequency response (i.e. the capacitor in the resonant tank appears as a low driving source impedance during the transient period of the aperture).

The example tank and resonant structures described above are for illustrative purposes and are not limiting. Alternate configurations can be utilized. The various resonant tanks and structures discussed can be combined or utilized independently as is now apparent.

3.5 Charge and Power Transfer Concepts

Concepts of charge transfer are now described with reference to FIGS. 71A-F. FIG. 71A illustrates a circuit 7102, including a switch S and a capacitor 7106 having a capacitance C. The switch S is controlled by a control signal 7108, which includes pulses 19010 having apertures T.

In FIG. 71B, Equation 10 illustrates that the charge q on a capacitor having a capacitance C, such as the capacitor 7106, is proportional to the voltage V across the capacitor, where:

q = Charge in Coulombs
C = Capacitance in Farads
V = Voltage in Volts
A = Input Signal Amplitude

Where the voltage V is represented by Equation 11, Equation 10 can be rewritten as Equation 12. The change in charge Δq over time t is illustrated as in Equation 13 as $\Delta q(t)$, which can be rewritten as Equation 14. Using the sum-to-product trigonometric identity of Equation 15, Equation 14 can be rewritten as Equation 16, which can be rewritten as equation 17.

Note that the sin term in Equation 11 is a function of the aperture T only. Thus, $\Delta q(t)$ is at a maximum when T is equal to an odd multiple of π (i.e., π, 3π, 5π, . . .). Therefore, the capacitor 7106 experiences the greatest change in charge when the aperture T has a value of π or a time interval representative of 180 degrees of the input sinusoid. Conversely, when T is equal to 2π, 4π, 6π, . . ., minimal charge is transferred.

Equations 18, 19, and 20 solve for q(t) by integrating Equation 10, allowing the charge on the capacitor 7106 with respect to time to be graphed on the same axis

as the input sinusoid sin(t), as illustrated in the graph of FIG. 71C. As the aperture T decreases in value or tends toward an impulse, the phase between the charge on the capacitor C or q(t) and sin(t) tend toward zero. This is illustrated in the graph of FIG. 71D, which indicates that the maximum impulse charge transfer occurs near the input voltage maxima. As this graph indicates, considerably less charge is transferred as the value of T decreases.

Power/charge relationships are illustrated in Equations 21-26 of FIG. 71E, where it is shown that power is proportional to charge, and transferred charge is inversely proportional to insertion loss.

Concepts of insertion loss are illustrated in FIG. 71F. Generally, the noise figure of a lossy passive device is numerically equal to the device insertion loss. Alternatively, the noise figure for any device cannot be less that its insertion loss. Insertion loss can be expressed by Equation 27 or 28. From the above discussion, it is observed that as the aperture T increases, more charge is transferred from the input to the capacitor 7106, which increases power transfer from the input to the output. It has been observed that it is not necessary to accurately reproduce the input voltage at the output because relative modulated amplitude and phase information is retained in the transferred power.

3.6 Optimizing and Adjusting the Non-Negligible Aperture Width/Duration

3.6.1 Varying Input and Output Impedances

In an embodiment of the invention, the energy transfer signal (i.e., control signal 2006 in FIG. 20A), is used to vary the input impedance seen by the EM Signal 2004 and to vary the output impedance driving a load. An example of this embodiment is described below using a gated transfer module 5101 shown in FIG. 51A. The method described below is not limited to the gated transfer module 5101.

In FIG. 51A, when switch 5106 is closed, the impedance looking into circuit 5102 is substantially the impedance of a storage module, illustrated here as a storage capacitance 5108, in parallel with the impedance of a load 5112. When the switch 5106 is open, the impedance at point 5114 approaches infinity. It follows that the average impedance at point 5114 can be varied from the impedance of the storage module illustrated in parallel with the load 5112, to the highest obtainable impedance when switch 5106 is open, by varying the ratio of the time that switch 5106 is open to the time switch 5106 is closed. The switch 5106 is controlled by an energy transfer signal 5110. Thus the impedance at point 5114 can be varied by controlling the aperture width of the energy transfer signal in conjunction with the aliasing rate.

An example method of altering the energy transfer signal 5106 of FIG. 51A is now described with reference to FIG. 49A, where a circuit 4902 receives an input oscillating signal 4906 and outputs a pulse train shown as doubler output signal 4904. The circuit 4902 can be used to generate the energy transfer signal 5106. Example waveforms of 4904 are shown on FIG. 49C.

It can be shown that by varying the delay of the signal propagated by the inverter 4908, the width of the pulses in the doubler output signal 4904 can be varied. Increasing the delay of the signal propagated by inverter 4908, increases the width of the pulses. The signal propagated by inverter 4908 can be delayed by introducing a R/C low pass network in the output of inverter 4908. Other means of altering the delay of the signal propagated by inverter 4908 will be well known to those skilled in the art.

3.6.2 Real Time Aperture Control

In an embodiment, the aperture width/duration is adjusted in real time. For example, referring to the timing diagrams in FIGS. 64B-F, a clock signal 6414 (FIG. 64B) is utilized to generate an energy transfer signal 6416 (FIG. 64F), which includes

energy transfer pluses 6418, having variable apertures 6420. In an embodiment, the clock signal 6414 is inverted as illustrated by inverted clock signal 6422 (FIG. 64D). The clock signal 6414 is also delayed, as illustrated by delayed clock signal 6424 (FIG. 64E). The inverted clock signal 6414 and the delayed clock signal 6424 are then ANDed together, generating an energy transfer signal 6416, which is active - energy transfer pulses 6418 - when the delayed clock signal 6424 and the inverted clock signal 6422 are both active. The amount of delay imparted to the delayed clock signal 6424 substantially determines the width or duration of the apertures 6420. By varying the delay in real time, the apertures are adjusted in real time.

In an alternative implementation, the inverted clock signal 6422 is delayed relative to the original clock signal 6414, and then ANDed with the original clock signal 6414. Alternatively, the original clock signal 6414 is delayed then inverted, and the result ANDed with the original clock signal 6414.

FIG. 64A illustrates an exemplary real time aperture control system 6402 that can be utilized to adjust apertures in real time. The example real time aperture control system 6402 includes an RC circuit 6404, which includes a voltage variable capacitor 6412 and a resistor 6426. The real time aperture control system 6402 also includes an inverter 6406 and an AND gate 6408. The AND gate 6408 optionally includes an enable input 6410 for enabling/disabling the AND gate 6408. The RC circuit 6404. The real time aperture control system 6402 optionally includes an amplifier 6428.

Operation of the real time aperture control circuit is described with reference to the timing diagrams of FIGS. 64B-F. The real time control system 6402 receives the input clock signal 6414, which is provided to both the inverter 6406 and to the RC circuit 6404. The inverter 6406 outputs the inverted clock signal 6422 and presents it to the AND gate 6408. The RC circuit 6404 delays the clock signal 6414 and outputs the delayed clock signal 6424. The delay is determined primarily by the capacitance of the voltage variable capacitor 6412. Generally, as the capacitance decreases, the delay decreases.

The delayed clock signal 6424 is optionally amplified by the optional amplifier 6428, before being presented to the AND gate 6408. Amplification is desired, for example, where the RC constant of the RC circuit 6404 attenuates the signal below the threshold of the AND gate 6408.

The AND gate 6408 ANDs the delayed clock signal 6424, the inverted clock signal 6422, and the optional Enable signal 6410, to generate the energy transfer signal 6416. The apertures 6420 are adjusted in real time by varying the voltage to the voltage variable capacitor 6412.

In an embodiment, the apertures 6420 are controlled to optimize power transfer. For example, in an embodiment, the apertures 6420 are controlled to maximize power transfer. Alternatively, the apertures 6420 are controlled for variable gain control (e.g. automatic gain control - AGC). In this embodiment, power transfer is reduced by reducing the apertures 6420.

As can now be readily seen from this disclosure, many of the aperture circuits presented, and others, can be modified as in circuits illustrated in FIGS. 46 H-K. Modification or selection of the aperture can be done at the design level to remain a fixed value in the circuit, or in an alternative embodiment, may be dynamically adjusted to compensate for, or address, various design goals such as receiving RF signals with enhanced efficiency that are in distinctively different bands of operation, e.g. RF signals at 900 MHZ and 1.8 GHz.

3.7 Adding a Bypass Network

In an embodiment of the invention, a bypass network is added to improve the efficiency of the energy transfer module. Such a bypass network can be viewed as a means of synthetic aperture widening. Components for a bypass network are selected so that the bypass network appears substantially lower impedance to transients of the switch module (i.e., frequencies greater than the received EM signal) and appears as

a moderate to high impedance to the input EM signal (e.g., greater that 100 Ohms at the RF frequency).

The time that the input signal is now connected to the opposite side of the switch module is lengthened due to the shaping caused by this network, which in simple realizations may be a capacitor or series resonant inductor-capacitor. A network that is series resonant above the input frequency would be a typical implementation. This shaping improves the conversion efficiency of an input signal that would otherwise, if one considered the aperture of the energy transfer signal only, be relatively low in frequency to be optimal.

For example, referring to FIG. 61 a bypass network 6102 (shown in this instance as capacitor 6112), is shown bypassing switch module 6104. In this embodiment the bypass network increases the efficiency of the energy transfer module when, for example, less than optimal aperture widths were chosen for a given input frequency on the energy transfer signal 6106. The bypass network 6102 could be of different configurations than shown in FIG 61. Such an alternate is illustrated in FIG.57. Similarly, FIG. 62 illustrates another example bypass network 6202, including a capacitor 6204.

The following discussion will demonstrate the effects of a minimized aperture and the benefit provided by a bypassing network. Beginning with an initial circuit having a 550ps aperture in FIG. 65, its output is seen to be 2.8mVpp applied to a 50 ohm load in FIG. 69A. Changing the aperture to 270ps as shown in FIG. 66 results in a diminished output of 2.5Vpp applied to a 50 ohm load as shown in FIG. 69B. To compensate for this loss, a bypass network may be added, a specific implementation is provided in FIG. 67. The result of this addition is that 3.2Vpp can now be applied to the 50 ohm load as shown in FIG. 70A. The circuit with the bypass network in FIG. 67 also had three values adjusted in the surrounding circuit to compensate for the impedance changes introduced by the bypass network and narrowed aperture. FIG. 68 verifies that those changes added to the circuit, but without the bypass

network, did not themselves bring about the increased efficiency demonstrated by the embodiment in FIG. 67 with the bypass network. FIG. 70B shows the result of using the circuit in FIG. 68 in which only 1.88Vpp was able to be applied to a 50 ohm load.

3.8 Modifying the Energy Transfer Signal Utilizing Feedback

FIG. 47 shows an embodiment of a system 4701 which uses down-converted Signal 4708B as feedback 4706 to control various characteristics of the energy transfer module 4704 to modify the down-converted signal 4708B.

Generally, the amplitude of the down-converted signal 4708B varies as a function of the frequency and phase differences between the EM signal 4504 and the energy transfer signal 4506. In an embodiment, the down-converted signal 4708B is used as the feedback 4706 to control the frequency and phase relationship between the EM signal 4504 and the energy transfer signal 4506. This can be accomplished using the example logic in FIG 52A. The example circuit in FIG. 52A can be included in the energy transfer signal module 4702. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention. In this embodiment a state-machine is used as an example.

In the example of FIG. 52A, a state machine 5204 reads an analog to digital converter, A/D 5202, and controls a digital to analog converter, DAC 5206. In an embodiment, the state machine 5204 includes 2 memory locations, *Previous* and *Current,* to store and recall the results of reading A/D 5202. In an embodiment, the state machine 5204 utilizes at least one memory flag.

The DAC 5206 controls an input to a voltage controlled oscillator, VCO 5208. VCO 5208 controls a frequency input of a pulse generator 5210, which, in an embodiment, is substantially similar to the pulse generator shown in FIG. 46C. The pulse generator 5210 generates energy transfer signal 4506.

In an embodiment, the state machine 5204 operates in accordance with a state machine flowchart 5219 in FIG. 52B. The result of this operation is to modify the frequency and phase relationship between the energy transfer signal 4506 and the EM signal 4504, to substantially maintain the amplitude of the down-converted signal 4708B at an optimum level.

The amplitude of the down-converted signal 4708B can be made to vary with the amplitude of the energy transfer signal 4506. In an embodiment where the switch module 6502 is a FET as shown in FIG 45A, wherein the gate 4518 receives the energy transfer signal 4506, the amplitude of the energy transfer signal 4506 can determine the "on" resistance of the FET, which affects the amplitude of the down-converted signal 4708B. The energy transfer signal module 4702, as shown in FIG. 52C, can be an analog circuit that enables an automatic gain control function. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention.

3.9 Other Implementations

The implementations described above are provided for purposes of illustration. These implementations are not intended to limit the invention. Alternate implementations, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

3.10 Example Energy Transfer Down-Converters

Example implementations are described below for illustrative purposes. The invention is not limited to these examples.

FIG. 53 is a schematic diagram of an exemplary circuit to down convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock.

FIG. 54 shows example simulation waveforms for the circuit of figure 53. Waveform 5302 is the input to the circuit showing the distortions caused by the switch closure. Waveform 5304 is the unfiltered output at the storage unit. Waveform 5306 is the impedance matched output of the down-converter on a different time scale.

FIG. 55 is a schematic diagram of an exemplary circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock. The circuit has additional tank circuitry to improve conversion efficiency.

FIG. 56 shows example simulation waveforms for the circuit of figure 55. Waveform 5502 is the input to the circuit showing the distortions caused by the switch closure. Waveform 5504 is the unfiltered output at the storage unit. Waveform 5506 is the output of the down-converter after the impedance match circuit.

FIG. 57 is a schematic diagram of an exemplary circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock. The circuit has switch bypass circuitry to improve conversion efficiency.

FIG. 58 shows example simulation waveforms for the circuit of figure 57. Waveform 5702 is the input to the circuit showing the distortions caused by the switch closure. Waveform 5704 is the unfiltered output at the storage unit. Waveform 5706 is the output of the down-converter after the impedance match circuit.

FIG. 59 shows a schematic of the example circuit in FIG. 53 connected to an FSK source that alternates between 913 and 917 MHZ, at a baud rate of 500 Kbaud. FIG. 72 shows the original FSK waveform 5902 and the down-converted waveform 5904 at the output of the load impedance match circuit.

4. Frequency Up-conversion

The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

An example frequency up-conversion system 300 is illustrated in FIG. 3. The frequency up-conversion system 300 is now described.

An input signal 302 (designated as "Control Signal" in FIG. 3) is accepted by a switch module 304. For purposes of example only, assume that the input signal 302 is a FM input signal 606, an example of which is shown in FIG. 6C. FM input signal 606 may have been generated by modulating information signal 602 onto oscillating signal 604 (FIGS. 6A and 6B). It should be understood that the invention is not limited to this embodiment. The information signal 602 can be analog, digital, or any combination thereof, and any modulation scheme can be used.

The output of switch module 304 is a harmonically rich signal 306, shown for example in FIG. 6D as a harmonically rich signal 608. The harmonically rich signal 608 has a continuous and periodic waveform.

FIG. 6E is an expanded view of two sections of harmonically rich signal 608, section 610 and section 612. The harmonically rich signal 608 may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

Harmonically rich signal 608 is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal 608. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. 6F and FIG. 6G show separately the sinusoidal components making up the first, third, and fifth harmonics of section 610 and section 612. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal 608 is shown as a square wave, there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. 6H.

The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal 306 and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal 306. According to an embodiment of the invention, the input signal 606 may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

A filter 308 filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal 310, shown for example as a filtered output signal 614 in FIG. 6I.

FIG. 4 illustrates an example universal frequency up-conversion (UFU) module 401. The UFU module 401 includes an example switch module 304, which comprises a bias signal 402, a resistor or impedance 404, a universal frequency translator (UFT) 450, and a ground 408. The UFT 450 includes a switch 406. The input signal 302 (designated as "Control Signal" in FIG. 4) controls the switch 406 in the UFT 450, and causes it to close and open. Harmonically rich signal 306 is generated at a node 405 located between the resistor or impedance 404 and the switch 406.

Also in FIG. 4, it can be seen that an example filter 308 is comprised of a capacitor 410 and an inductor 412 shunted to a ground 414. The filter is designed to filter out the undesired harmonics of harmonically rich signal 306.

The invention is not limited to the UFU embodiment shown in FIG. 4.

For example, in an alternate embodiment shown in FIG. 5, an unshaped input signal 501 is routed to a pulse shaping module 502. The pulse shaping module 502 modifies the unshaped input signal 501 to generate a (modified) input signal 302 (designated as the "Control Signal" in FIG. 5). The input signal 302 is routed to the switch module 304, which operates in the manner described above. Also, the filter 308 of FIG. 5 operates in the manner described above.

The purpose of the pulse shaping module 502 is to define the pulse width of the input signal 302. Recall that the input signal 302 controls the opening and closing of the switch 406 in switch module 304. During such operation, the pulse width of the input signal 302 establishes the pulse width of the harmonically rich signal 306. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal 306 are a function of at least the pulse width of the harmonically rich signal 306. As such, the pulse width of the input signal 302 contributes to setting the relative amplitudes of the harmonics of harmonically rich signal 306.

Further details of up-conversion as described in this section are presented in pending U.S. application "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, incorporated herein by reference in its entirety.

5. Enhanced Signal Reception

The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same.

Referring to FIG. 21, transmitter 2104 accepts a modulating baseband signal 2102 and generates (transmitted) redundant spectrums 2106a-n, which are sent over communications medium 2108. Receiver 2112 recovers a demodulated baseband signal 2114 from (received) redundant spectrums 2110a-n. Demodulated baseband signal 2114 is representative of the modulating baseband signal 2102, where the level of similarity between the modulating baseband signal 2114 and the modulating baseband signal 2102 is application dependent.

Modulating baseband signal 2102 is preferably any information signal desired for transmission and/or reception. An example modulating baseband signal 2202 is illustrated in FIG. 22A, and has an associated modulating baseband spectrum 2204 and image spectrum 2203 that are illustrated in FIG. 22B. Modulating baseband signal 2202 is illustrated as an analog signal in FIG. 22a, but could also be a digital signal, or combination thereof. Modulating baseband signal 2202 could be a voltage (or current) characterization of any number of real world occurrences, including for example and without limitation, the voltage (or current) representation for a voice signal.

Each transmitted redundant spectrum 2106a-n contains the necessary information to substantially reconstruct the modulating baseband signal 2102. In other words, each redundant spectrum 2106a-n contains the necessary amplitude, phase, and frequency information to reconstruct the modulating baseband signal 2102.

FIG. 22C illustrates example transmitted redundant spectrums 2206b-d. Transmitted redundant spectrums 2206b-d are illustrated to contain three redundant spectrums for illustration purposes only. Any number of redundant spectrums could be generated and transmitted as will be explained in following discussions.

Transmitted redundant spectrums 2206b-d are centered at f_1, with a frequency spacing f_2 between adjacent spectrums. Frequencies f_1 and f_2 are dynamically adjustable in real-time as will be shown below. FIG. 22D illustrates an alternate embodiment, where redundant spectrums 2208c,d are centered on unmodulated

oscillating signal 2209 at f_1(Hz). Oscillating signal 2209 may be suppressed if desired using, for example, phasing techniques or filtering techniques. Transmitted redundant spectrums are preferably above baseband frequencies as is represented by break 2205 in the frequency axis of FIGS. 22C and 22D.

Received redundant spectrums 2110a-n are substantially similar to transmitted redundant spectrums 2106a-n, except for the changes introduced by the communications medium 2108. Such changes can include but are not limited to signal attenuation, and signal interference. FIG. 22E illustrates example received redundant spectrums 2210b-d. Received redundant spectrums 2210b-d are substantially similar to transmitted redundant spectrums 2206b-d, except that redundant spectrum 2210c includes an undesired jamming signal spectrum 2211 in order to illustrate some advantages of the present invention. Jamming signal spectrum 2211 is a frequency spectrum associated with a jamming signal. For purposes of this invention, a "jamming signal" refers to any unwanted signal, regardless of origin, that may interfere with the proper reception and reconstruction of an intended signal. Furthermore, the jamming signal is not limited to tones as depicted by spectrum 2211, and can have any spectral shape, as will be understood by those skilled in the art(s).

As stated above, demodulated baseband signal 2114 is extracted from one or more of received redundant spectrums 2210b-d. FIG. 22F illustrates example demodulated baseband signal 2212 that is, in this example, substantially similar to modulating baseband signal 2202 (FIG. 22A); where in practice, the degree of similarity is application dependent.

An advantage of the present invention should now be apparent. The recovery of modulating baseband signal 2202 can be accomplished by receiver 2112 in spite of the fact that high strength jamming signal(s) (e.g. jamming signal spectrum 2211) exist on the communications medium. The intended baseband signal can be recovered because multiple redundant spectrums are transmitted, where each redundant spectrum carries the necessary information to reconstruct the baseband signal. At the

destination, the redundant spectrums are isolated from each other so that the baseband signal can be recovered even if one or more of the redundant spectrums are corrupted by a jamming signal.

Transmitter 2104 will now be explored in greater detail. FIG. 23A illustrates transmitter 2301, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2206b-d. Transmitter 2301 includes generator 2303, optional spectrum processing module 2304, and optional medium interface module 2320. Generator 2303 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

Transmitter 2301 operates as follows. First oscillator 2302 and second oscillator 2309 generate a first oscillating signal 2305 and second oscillating signal 2312, respectively. First stage modulator 2306 modulates first oscillating signal 2305 with modulating baseband signal 2202, resulting in modulated signal 2308. First stage modulator 2306 may implement any type of modulation including but not limited to: amplitude modulation, frequency modulation, phase modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates modulated signal 2308 with second oscillating signal 2312, resulting in multiple redundant spectrums 2206a-n shown in FIG. 23B. Second stage modulator 2310 is preferably a phase modulator, or a frequency modulator, although other types of modulation may be implemented including but not limited to amplitude modulation. Each redundant spectrum 2206a-n contains the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal 2202.

Redundant spectrums 2206a-n are substantially centered around f_1, which is the characteristic frequency of first oscillating signal 2305. Also, each redundant spectrum 2206a-n (except for 2206c) is offset from f_1 by approximately a multiple of f_2 (Hz), where f_2 is the frequency of the second oscillating signal 2312. Thus, each

redundant spectrum 2206a-n is offset from an adjacent redundant spectrum by f_2 (Hz). This allows the spacing between adjacent redundant spectrums to be adjusted (or tuned) by changing f_2 that is associated with second oscillator 2309. Adjusting the spacing between adjacent redundant spectrums allows for dynamic real-time tuning of the bandwidth occupied by redundant spectrums 2206a-n.

In one embodiment, the number of redundant spectrums 2206a-n generated by transmitter 2301 is arbitrary and may be unlimited as indicated by the "a-n" designation for redundant spectrums 2206a-n. However, a typical communications medium will have a physical and/or administrative limitations (i.e. FCC regulations) that restrict the number of redundant spectrums that can be practically transmitted over the communications medium. Also, there may be other reasons to limit the number of redundant spectrums transmitted. Therefore, preferably, the transmitter 2301 will include an optional spectrum processing module 2304 to process the redundant spectrums 2206a-n prior to transmission over communications medium 2108.

In one embodiment, spectrum processing module 2304 includes a filter with a passband 2207 (FIG. 23C) to select redundant spectrums 2206b-d for transmission. This will substantially limit the frequency bandwidth occupied by the redundant spectrums to the passband 2207. In one embodiment, spectrum processing module 2304 also up converts redundant spectrums and/or amplifies redundant spectrums prior to transmission over the communications medium 2108. Finally, medium interface module 2320 transmits redundant spectrums over the communications medium 2108. In one embodiment, communications medium 2108 is an over-the-air link and medium interface module 2320 is an antenna. Other embodiments for communications medium 2108 and medium interface module 2320 will be understood based on the teachings contained herein.

FIG. 23D illustrates transmitter 2321, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums

2208c-d and unmodulated spectrum 2209. Transmitter 2321 includes generator 2311, spectrum processing module 2304, and (optional) medium interface module 2320. Generator 2311 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

As shown in FIG. 23D, many of the components in transmitter 2321 are similar to those in transmitter 2301. However, in this embodiment, modulating baseband signal 2202 modulates second oscillating signal 2312. Transmitter 2321 operates as follows. First stage modulator 2306 modulates second oscillating signal 2312 with modulating baseband signal 2202, resulting in modulated signal 2322. As described earlier, first stage modulator 2306 can effect any type of modulation including but not limited to: amplitude modulation frequency modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates first oscillating signal 2304 with modulated signal 2322, resulting in redundant spectrums 2208a-n, as shown in FIG. 23E. Second stage modulator 2310 is preferably a phase or frequency modulator, although other modulators could used including but not limited to an amplitude modulator.

Redundant spectrums 2208a-n are centered on unmodulated spectrum 2209 (at f_1 Hz), and adjacent spectrums are separated by f_2 Hz. The number of redundant spectrums 2208a-n generated by generator 2311 is arbitrary and unlimited, similar to spectrums 2206a-n discussed above. Therefore, optional spectrum processing module 2304 may also include a filter with passband 2325 to select, for example, spectrums 2208c,d for transmission over communications medium 2108. In addition, optional spectrum processing module 2304 may also include a filter (such as a bandstop filter) to attenuate unmodulated spectrum 2209. Alternatively, unmodulated spectrum 2209 may be attenuated by using phasing techniques during redundant spectrum generation. Finally, (optional) medium interface module 2320 transmits redundant spectrums 2208c,d over communications medium 2108.

Receiver 2112 will now be explored in greater detail to illustrate recovery of a demodulated baseband signal from received redundant spectrums. FIG. 24A illustrates receiver 2430, which is one embodiment of receiver 2112. Receiver 2430 includes optional medium interface module 2402, down-converter 2404, spectrum isolation module 2408, and data extraction module 2414. Spectrum isolation module 2408 includes filters 2410a-c. Data extraction module 2414 includes demodulators 2416a-c, error check modules 2420a-c, and arbitration module 2424. Receiver 2430 will be discussed in relation to the signal diagrams in FIGS. 24B-24J.

In one embodiment, optional medium interface module 2402 receives redundant spectrums 2210b-d (FIG. 22E, and FIG. 24B). Each redundant spectrum 2210b-d includes the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal used to generated the redundant spectrums. However, in the present example, spectrum 2210c also contains jamming signal 2211, which may interfere with the recovery of a baseband signal from spectrum 2210c. Down-converter 2404 down-converts received redundant spectrums 2210b-d to lower intermediate frequencies, resulting in redundant spectrums 2406a-c (FIG. 24C). Jamming signal 2211 is also down-converted to jamming signal 2407, as it is contained within redundant spectrum 2406b. Spectrum isolation module 2408 includes filters 2410a-c that isolate redundant spectrums 2406a-c from each other (FIGS. 24D-24F, respectively). Demodulators 2416a-c independently demodulate spectrums 2406a-c, resulting in demodulated baseband signals 2418a-c, respectively (FIGS. 24G-24I). Error check modules 2420a-c analyze demodulate baseband signal 2418a-c to detect any errors. In one embodiment, each error check module 2420a-c sets an error flag 2422a-c whenever an error is detected in a demodulated baseband signal. Arbitration module 2424 accepts the demodulated baseband signals and associated error flags, and selects a substantially error-free demodulated baseband signal (FIG. 24J). In one embodiment, the substantially error-free demodulated baseband signal will be substantially similar to the modulating baseband signal used

to generate the received redundant spectrums, where the degree of similarity is application dependent.

Referring to FIGS. 24G-I, arbitration module 2424 will select either demodulated baseband signal 2418a or 2418c, because error check module 2420b will set the error flag 2422b that is associated with demodulated baseband signal 2418b.

The error detection schemes implemented by the error detection modules include but are not limited to: cyclic redundancy check (CRC) and parity check for digital signals, and various error detections schemes for analog signal.

Further details of enhanced signal reception as described in this section are presented in pending U.S. application "Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998, incorporated herein by reference in its entirety.

6. Unified Down-conversion and Filtering

The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

FIG. 17 is a conceptual block diagram of a UDF module 1702 according to an embodiment of the present invention. The UDF module 1702 performs at least frequency translation and frequency selectivity.

The effect achieved by the UDF module 1702 is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module 1702 effectively performs input filtering.

According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals 1704 received by the UDF module 1702 are at radio frequencies. The UDF module 1702 effectively operates to input filter these RF input signals 1704. Specifically, in these embodiments, the UDF module 1702 effectively performs input, channel select filtering of the RF input signal 1704. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module 1702 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module 1702 includes a frequency translator 1708. The frequency translator 1708 conceptually represents that portion of the UDF module 1702 that performs frequency translation (down conversion).

The UDF module 1702 also conceptually includes an apparent input filter 1706 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1706 represents that portion of the UDF module 1702 that performs input filtering.

In practice, the input filtering operation performed by the UDF module 1702 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter 1706 is herein referred to as an "apparent" input filter 1706.

The UDF module 1702 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1702. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1702 can be designed with a filter center frequency f_C on the order of 900 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_C of the UDF module 1702 can be electrically adjusted, either statically or dynamically.

Also, the UDF module 1702 can be designed to amplify input signals.

Further, the UDF module 1702 can be implemented without large resistors, capacitors, or inductors. Also, the UDF module 1702 does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1702 is friendly to integrated circuit design techniques and processes.

The features and advantages exhibited by the UDF module 1702 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF

module 1702 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and samples/instances of the output signal.

More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

Next, the input sample is held (that is, delayed).

Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

FIG. 19 illustrates an example implementation of the unified down-converting and filtering (UDF) module 1922. The UDF module 1922 performs the frequency translation operation and the frequency selectivity operation in an integrated, unified manner as described above, and as further described below.

In the example of FIG. 19, the frequency selectivity operation performed by the UDF module 1922 comprises a band-pass filtering operation according to EQ. 1, below, which is an example representation of a band-pass filtering transfer function.

$$VO = \alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \qquad \text{EQ. 1}$$

It should be noted, however, that the invention is not limited to band-pass filtering. Instead, the invention effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof. As will be appreciated, there are many representations of any given filter type. The invention is applicable to these filter representations. Thus, EQ. 1 is referred to herein for illustrative purposes only, and is not limiting.

The UDF module 1922 includes a down-convert and delay module 1924, first and second delay modules 1928 and 1930, first and second scaling modules 1932 and 1934, an output sample and hold module 1936, and an (optional) output smoothing module 1938. Other embodiments of the UDF module will have these components in different configurations, and/or a subset of these components, and/or additional components. For example, and without limitation, in the configuration shown in FIG. 19, the output smoothing module 1938 is optional.

As further described below, in the example of FIG. 19, the down-convert and delay module 1924 and the first and second delay modules 1928 and 1930 include switches that are controlled by a clock having two phases, φ_1 and φ_2. φ_1 and φ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low.

Preferably, each of these switches closes on a rising edge of φ_1 or φ_2, and opens on the next corresponding falling edge of φ_1 or φ_2. However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. 19, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module 1924 is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The example UDF module 1922 has a filter center frequency of 900.2 MHZ and a filter bandwidth of 570 KHz. The pass band of the UDF module 1922 is on the order of 899.915 MHZ to 900.485 MHZ. The Q factor of the UDF module 1922 is approximately 1879 (i.e., 900.2 MHZ divided by 570 KHz).

The operation of the UDF module 1922 shall now be described with reference to a Table 1802 (FIG. 18) that indicates example values at nodes in the UDF module 1922 at a number of consecutive time increments. It is assumed in Table 1802 that the UDF module 1922 begins operating at time t-1. As indicated below, the UDF module 1922 reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

At the rising edge of φ_1 at time t-1, a switch 1950 in the down-convert and delay module 1924 closes. This allows a capacitor 1952 to charge to the current value of an input signal, VI_{t-1}, such that node 1902 is at VI_{t-1}. This is indicated by cell 1804 in FIG. 18. In effect, the combination of the switch 1950 and the capacitor 1952 in the down-convert and delay module 1924 operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor 1952 represents an instance of a down-converted image of the input signal VI.

The manner in which the down-convert and delay module 1924 performs frequency down-conversion is further described elsewhere in this application, and is additionally described in pending U.S. application "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, issued as U.S. Patent No. 6,061,551, which is herein incorporated by reference in its entirety.

Also at the rising edge of φ_1 at time t-1, a switch 1958 in the first delay module 1928 closes, allowing a capacitor 1960 to charge to VO_{t-1}, such that node 1906 is at VO_{t-1}. This is indicated by cell 1806 in Table 1802. (In practice, VO_{t-1} is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

Also at the rising edge of φ_1 at time t-1, a switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to a value stored in a capacitor 1964. At this time, however, the value in capacitor 1964 is undefined, so the value in capacitor 1968 is undefined. This is indicated by cell 1807 in table 1802.

At the rising edge of φ_2 at time t-1, a switch 1954 in the down-convert and delay module 1924 closes, allowing a capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_{t-1}, such that node 1904 is at VI_{t-1}. This is indicated by cell 1810 in Table 1802.

The UDF module 1922 may optionally include a unity gain module 1990A between capacitors 1952 and 1956. The unity gain module 1990A operates as a current source to enable capacitor 1956 to charge without draining the charge from capacitor 1952. For a similar reason, the UDF module 1922 may include other unity gain modules 1990B-1990G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules 1990A-1990G are optional. The structure and operation of the unity gain modules 1990 will be apparent to persons skilled in the relevant art(s).

Also at the rising edge of φ_2 at time t-1, a switch 1962 in the first delay module 1928 closes, allowing a capacitor 1964 to charge to the level of the capacitor 1960. Accordingly, the capacitor 1964 charges to VO_{t-1}, such that node 1908 is at VO_{t-1}. This is indicated by cell 1814 in Table 1802.

Also at the rising edge of φ_2 at time t-1, a switch 1970 in the second delay module 1930 closes, allowing a capacitor 1972 to charge to a value stored in a capacitor 1968. At this time, however, the value in capacitor 1968 is undefined, so the value in capacitor 1972 is undefined. This is indicated by cell 1815 in table 1802.

At time t, at the rising edge of φ_1, the switch 1950 in the down-convert and delay module 1924 closes. This allows the capacitor 1952 to charge to VI_t, such that node 1902 is at VI_t. This is indicated in cell 1816 of Table 1802.

Also at the rising edge of φ_1 at time t, the switch 1958 in the first delay module 1928 closes, thereby allowing the capacitor 1960 to charge to VO_t. Accordingly, node 1906 is at VO_t. This is indicated in cell 1820 in Table 1802.

Further at the rising edge of φ_1 at time t, the switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to the level of the capacitor 1964. Therefore, the capacitor 1968 charges to VO_{t-1}, such that node 1910 is at VO_{t-1}. This is indicated by cell 1824 in Table 1802.

At the rising edge of φ_2 at time t, the switch 1954 in the down-convert and delay module 1924 closes, allowing the capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_t, such that node 1904 is at VI_t. This is indicated by cell 1828 in Table 1802.

Also at the rising edge of φ_2 at time t, the switch 1962 in the first delay module 1928 closes, allowing the capacitor 1964 to charge to the level in the capacitor 1960. Therefore, the capacitor 1964 charges to VO_t, such that node 1908 is at VO_t. This is indicated by cell 1832 in Table 1802.

Further at the rising edge of φ_2 at time t, the switch 1970 in the second delay module 1930 closes, allowing the capacitor 1972 in the second delay module 1930 to

charge to the level of the capacitor 1968 in the second delay module 1930. Therefore, the capacitor 1972 charges to VO_{t-1}, such that node 1912 is at VO_{t-1}. This is indicated in cell 1836 of FIG. 18.

At time t+1, at the rising edge of φ_1, the switch 1950 in the down-convert and delay module 1924 closes, allowing the capacitor 1952 to charge to VI_{t+1}. Therefore, node 1902 is at VI_{t+1}, as indicated by cell 1838 of Table 1802.

Also at the rising edge of φ_1 at time t+1, the switch 1958 in the first delay module 1928 closes, allowing the capacitor 1960 to charge to VO_{t+1}. Accordingly, node 1906 is at VO_{t+1}, as indicated by cell 1842 in Table 1802.

Further at the rising edge of φ_1 at time t+1, the switch 1966 in the second delay module 1930 closes, allowing the capacitor 1968 to charge to the level of the capacitor 1964. Accordingly, the capacitor 1968 charges to VO_t, as indicated by cell 1846 of Table 1802.

In the example of FIG. 19, the first scaling module 1932 scales the value at node 1908 (i.e., the output of the first delay module 1928) by a scaling factor of -0.1. Accordingly, the value present at node 1914 at time t+1 is $-0.1 * VO_t$. Similarly, the second scaling module 1934 scales the value present at node 1912 (i.e., the output of the second scaling module 1930) by a scaling factor of -0.8. Accordingly, the value present at node 1916 is $-0.8 * VO_{t-1}$ at time t+1.

At time t+1, the values at the inputs of the summer 1926 are: VI_t at node 1904, $-0.1 * VO_t$ at node 1914, and $-0.8 * VO_{t-1}$ at node 1916 (in the example of FIG. 19, the values at nodes 1914 and 1916 are summed by a second summer 1925, and this sum is presented to the summer 1926). Accordingly, at time t+1, the summer generates a signal equal to $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$.

At the rising edge of φ_1 at time t+1, a switch 1991 in the output sample and hold module 1936 closes, thereby allowing a capacitor 1992 to charge to VO_{t+1}. Accordingly, the capacitor 1992 charges to VO_{t+1}, which is equal to the sum generated by the adder 1926. As just noted, this value is equal to: $VI_t - 0.1 * VO_t$

$- 0.8 * VO_{t-1}$. This is indicated in cell 1850 of Table 1802. This value is presented to the optional output smoothing module 1938, which smooths the signal to thereby generate the instance of the output signal VO_{t+1}. It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. 1.

Further details of unified down-conversion and filtering as described in this section are presented in pending U.S. application "Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed October 21, 1998, incorporated herein by reference in its entirety.

7. Example Application Embodiments of the Invention

As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

Example applications of the UFT module were described above. In particular, frequency down-conversion, frequency up-conversion, enhanced signal reception, and unified down-conversion and filtering applications of the UFT module were summarized above, and are further described below. These applications of the UFT module are discussed herein for illustrative purposes. The invention is not limited to these example applications. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s), based on the teachings contained herein.

For example, the present invention can be used in applications that involve frequency down-conversion. This is shown in FIG. 1C, for example, where an example UFT module 115 is used in a down-conversion module 114. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

This is also shown in FIG. 7, for example, where an example UFT module 706 is part of a down-conversion module 704, which is part of a receiver 702.

The present invention can be used in applications that involve frequency up-conversion. This is shown in FIG. 1D, for example, where an example UFT module 117 is used in a frequency up-conversion module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal. This is also shown in FIG. 8, for example, where an example UFT module 806 is part of up-conversion module 804, which is part of a transmitter 802.

The present invention can be used in environments having one or more transmitters 902 and one or more receivers 906, as illustrated in FIG. 9. In such environments, one or more of the transmitters 902 may be implemented using a UFT module, as shown for example in FIG. 8. Also, one or more of the receivers 906 may be implemented using a UFT module, as shown for example in FIG. 7.

The invention can be used to implement a transceiver. An example transceiver 1002 is illustrated in FIG. 10. The transceiver 1002 includes a transmitter 1004 and a receiver 1008. Either the transmitter 1004 or the receiver 1008 can be implemented using a UFT module. Alternatively, the transmitter 1004 can be implemented using a UFT module 1006, and the receiver 1008 can be implemented using a UFT module 1010. This embodiment is shown in FIG. 10.

Another transceiver embodiment according to the invention is shown in FIG. 11. In this transceiver 1102, the transmitter 1104 and the receiver 1108 are implemented using a single UFT module 1106. In other words, the transmitter 1104 and the receiver 1108 share a UFT module 1106.

As described elsewhere in this application, the invention is directed to methods and systems for enhanced signal reception (ESR). Various ESR embodiments include an ESR module (transmit) in a transmitter 1202, and an ESR module (receive) in a receiver 1210. An example ESR embodiment configured in this manner is illustrated in FIG. 12.

The ESR module (transmit) 1204 includes a frequency up-conversion module 1206. Some embodiments of this frequency up-conversion module 1206 may be implemented using a UFT module, such as that shown in FIG. 1D.

The ESR module (receive) 1212 includes a frequency down-conversion module 1214. Some embodiments of this frequency down-conversion module 1214 may be implemented using a UFT module, such as that shown in FIG. 1C.

As described elsewhere in this application, the invention is directed to methods and systems for unified down-conversion and filtering (UDF). An example unified down-conversion and filtering module 1302 is illustrated in FIG. 13. The unified down-conversion and filtering module 1302 includes a frequency down-conversion module 1304 and a filtering module 1306. According to the invention, the frequency down-conversion module 1304 and the filtering module 1306 are implemented using a UFT module 1308, as indicated in FIG. 13.

Unified down-conversion and filtering according to the invention is useful in applications involving filtering and/or frequency down-conversion. This is depicted, for example, in FIGS. 15A-15F. FIGS. 15A-15C indicate that unified down-conversion and filtering according to the invention is useful in applications where filtering precedes, follows, or both precedes and follows frequency down-conversion. FIG. 15D indicates that a unified down-conversion and filtering module 1524 according to the invention can be utilized as a filter 1522 (i.e., where the extent of frequency down-conversion by the down-converter in the unified down-conversion and filtering module 1524 is minimized). FIG. 15E indicates that a unified down-conversion and filtering module 1528 according to the invention can be utilized as a down-converter 1526 (i.e., where the filter in the unified down-conversion and filtering module 1528 passes substantially all frequencies). FIG. 15F illustrates that the unified down-conversion and filtering module 1532 can be used as an amplifier. It is noted that one or more UDF modules can be used in applications that involve at least one or more of filtering, frequency translation, and amplification.

For example, receivers, which typically perform filtering, down-conversion, and filtering operations, can be implemented using one or more unified down-conversion and filtering modules. This is illustrated, for example, in FIG. 14.

The methods and systems of unified down-conversion and filtering of the invention have many other applications. For example, as discussed herein, the enhanced signal reception (ESR) module (receive) operates to down-convert a signal containing a plurality of spectrums. The ESR module (receive) also operates to isolate the spectrums in the down-converted signal, where such isolation is implemented via filtering in some embodiments. According to embodiments of the invention, the ESR module (receive) is implemented using one or more unified down-conversion and filtering (UDF) modules. This is illustrated, for example, in FIG. 16. In the example of FIG. 16, one or more of the UDF modules 1610, 1612, 1614 operates to down-convert a received signal. The UDF modules 1610, 1612, 1614 also operate to filter the down-converted signal so as to isolate the spectrum(s) contained therein. As noted above, the UDF modules 1610, 1612, 1614 are implemented using the universal frequency translation (UFT) modules of the invention.

The invention is not limited to the applications of the UFT module described above. For example, and without limitation, subsets of the applications (methods and/or structures) described herein (and others that would be apparent to persons skilled in the relevant art(s) based on the herein teachings) can be associated to form useful combinations.

For example, transmitters and receivers are two applications of the UFT module. FIG. 10 illustrates a transceiver 1002 that is formed by combining these two applications of the UFT module, i.e., by combining a transmitter 1004 with a receiver 1008.

Also, ESR (enhanced signal reception) and unified down-conversion and filtering are two other applications of the UFT module. FIG. 16 illustrates an example

where ESR and unified down-conversion and filtering are combined to form a modified enhanced signal reception system.

The invention is not limited to the example applications of the UFT module discussed herein. Also, the invention is not limited to the example combinations of applications of the UFT module discussed herein. These examples were provided for illustrative purposes only, and are not limiting. Other applications and combinations of such applications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion; (4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals.

Additional examples are set forth below describing applications of the UFT module in the area of universal platform modules.

8. Universal Platform Module (UPM)

The invention is directed to devices which, generally, provide some information technology and communicate on a network or over any other communication medium (such as wireless and wired communication mediums). In order to communicate, the devices receive a signal, optionally modify the signal or otherwise process the signal in an application specific manner, display the information, allow modification of the information, and then transmit a modified signal at the same or different frequency or frequencies. As will be appreciated, at least some of these operations are optional. A device is often used in an off-line manner where it is disconnected from the network or networks (or, more generally, when the device is not in communication with other devices/external entities).

A device 2602 is illustrated, for example, in FIG. 32, where an example UPM 2606 enables communication with networks using cellular 3210, wireless local loop (WLL) 3215, wireless local area network (WLAN) 3220, wireline (LAN, WAN, etc.) 3230, and analog 3225 network links. These network links and/or topologies are described herein for example purposes only, although it should be understood that the invention is applicable to any communication medium. Device 2602 communicates using these links to any of the components (PCs, servers, other devices) which are available on the respective networks 3212, 3217, 3222, 3227, and 3232. Such communication may be simultaneous, either actual or apparent.

The UPM 2606 may include a receiver, transmitter, and/or transceiver. Such components employ one or more UFT modules for performing frequency translation operations. See, for example, FIGS. 10 and 11 in the case of transceivers. See, for example, FIGS. 7 and 8 for receivers and transmitters.

8.1 Conventional Multi-Mode Usage Model

FIG. 25A illustrates a high level block diagram of an example conventional multi-mode device 2502. Multi-mode device 2502 includes device resources 2504, a CDMA platform module 2508, and a Bluetooth platform module 2506. CDMA platform module 2508 is constructed to perform cellular telephone operations with the cellular CDMA network 2510. Bluetooth platform module 2506 is constructed to perform WLAN operations with other Bluetooth devices on the Bluetooth Network 2512.

FIG. 25B illustrates a more detailed block diagram of a platform module 2508a employing a conventional receiver implemented with heterodyne components. Platform module 2508a frequency down-converts and demodulates a first EM signal 2514 received by first antenna 2515. First EM signal 2514 generally comprises a

electromagnetic (EM) signal broadcast at a carrier frequency modulated by a baseband information signal.

FIG. 25C illustrates a more detailed block diagram of a platform module 2508b employing a conventional transmitter implemented with heterodyne components. Platform module 2508b operates similarly to platform module 2508a. Platform module 2508b modulates and frequency up-converts baseband signal 2518, and outputs an EM signal 2542 that is transmitted by an antenna 2540.

Conventional platform module 2508, whether implemented as a receiver or transmitter (and/or transceiver (not shown)), suffers from the disadvantages of conventional wireless communication methods and systems. For instance, receivers and transmitters are conventionally implemented with heterodyne components. As previously described, heterodyne implementations are complex, are expensive to design, manufacture, and tune, and suffer from additional deficiencies well known in the art.

8.2 Universal Platform Module of the Present Invention

FIG. 26 illustrates a high level block diagram embodiment of an exemplary universal platform enabled device 2602 according to an embodiment of the present invention.

Universal platform enabled device 2602 includes device resources 2604 and a UPM 2606. UPM 2606 comprises at least one UFT module 2620 (as shown in FIG. 26B). UPM 2606 is shown linking to various network types: cellular network 2610, WLAN network 2612, WLL network 2614, and other networks 2616. Other networks 2616 include personal area networks (PANs), other non-IP networks, and any network resulting without limitation from the connection of devices through any communication medium, wired or wireless.

UPM 2606 receives signals and transmits signals using the UFT module 2620 as described herein.

In another embodiment, additional UFT modules 2620 may be employed, as shown in FIG. 26C. Persons skilled in the relevant art(s) will recognize after reading this disclosure that in particular applications, additional UFT modules may be used.

Furthermore, FIG 26C illustrates another embodiment where universal platform sub-modules (UPSM) 2622, each containing a UFT module 2620, are employed. Each UPSM 2622 would be capable of maintaining one or more links to the various networks/communication mediums disclosed herein.

The UPM 2606 of the present invention is also directed to digital signal applications. In a further embodiment, optional signal conditioning module 2523 comprises an analog-to-digital converter (A/D), a digital signal processor (DSP), a digital-to-analog (D/A) converter, and storage. Optional signal conditioning module 2523 inputs down-converted baseband signal 2518 to A/D. A/D converts down-converted baseband signal 2518 to a digital signal on interconnection. DSP can perform any digital signal processing function on the digital signal for signal amplification, filtering, error correction, etc. DSP may comprise a digital signal processing chip, a computer, hardware, software, firmware, or any combination thereof, or any other applicable technology known to persons skilled in the relevant art(s). Storage provides for storing digital signals at any stage prior to digital-to-analog conversion by D/A. These digital signals include the digital signal received from A/D, the digital signal to be output to D/A, or any intermediate signal provided by DSP. The interconnection may be configured between the components of optional signal conditioning module 2523 in a variety of ways as required by the present application, as would be understood by persons skilled in the relevant art(s).

D/A inputs the digital signal to be transmitted from interconnection, and converts it to analog, outputting baseband signal 2518. Optional signal conditioning module 2523 provides for digital signal processing and conditioning of a received

signal prior to its re-transmission. Persons skilled in the relevant art(s) will recognize that a variety of digital signal conditioning configurations exist for optional signal conditioning module 2523. Any other digital signal conditioning function may be performed by optional signal conditioning module 2523, as would be known to persons skilled in the relevant art(s).

Furthermore, persons skilled in the relevant art(s) will recognize that optional signal conditioning module 2523 can be configured to handle a combination of analog and digital signal conditioning functions.

Exemplary embodiments of the UPM 2606 and UPSM 2622 of the present invention are described below. However, it should be understood that these examples are provided for illustrative purposes only. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

8.2.1 Universal Platform Module Embodiments

The universal platform module of the present invention is directed to applications of universal platform modules and sub-modules. The universal platform module of the present invention may be implemented in devices which are land-based, and air- and space-based, or based anywhere else applicable. For example, the universal platform module of the present invention may be implemented in devices employed in ground stations, satellites, spacecraft, watercraft, and aircraft. The universal platform module of the present invention is applicable to any number of common household consumer appliances and goods, including phones and wireless modems. The universal platform module of the present invention may be implemented in any applicable manner known to persons skilled in the relevant art(s).

The universal platform module of the present invention is preferably directed to analog signal applications, although the invention is also applicable to digital applications. UPSM 3802 in the example embodiment shown in FIG. 38 is specific to a particular protocol and a particular bearer combination. The UPSM 3802 includes a receiver 3804 and a transmitter 3808 each including one or more UFT modules (as indicated by 3806 and 3810) as described herein and in the cited patent applications. Alternatively, the UPSM 3802 includes a transceiver having one or more UFT modules as described herein (as shown in FIG. 37 and discussed below).

The UPSM 3802 also includes a control module 3812 that enables the UPSM 3802 to operate in conformance with the particular protocol/bearer service combination. In particular, the control module 3812 includes hardware, software, or combinations thereof to cause the UPSM 3802 to receive, transmit, process, and otherwise interact with signals according to the particular protocol/bearer service combination. Implementation of the control module 3812 will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein.

Examples of the UPSM 3802 include ones that operate according to the example protocol/bearer service combinations shown in FIG. 39. It should be understood that the examples shown in FIG. 39 are provided for illustrative purposes only, and are not limiting. The invention is intended and adapted to operate with other protocol/bearer service combinations, and these will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein.

Also, FIG. 40 is a representation of groups of communication links or types. The control module 3812 of the UPSM 3802 enables the UPSM 3802 to operate in conformance with any such communication link/type. In particular, the control module 3812 includes hardware, software, or combinations thereof to cause the UPSM 3802 to receive, transmit, process, and otherwise interact with signals according to the communication link/type. Implementation of the control module 3812 will be apparent to persons skilled in the relevant art(s) based on at least the

teachings contained herein. It should be understood that the examples shown in FIG. 40 are provided for illustrative purposes only, and are not limiting. The invention is intended and adapted to operate with other communication links/types, and these will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein.

An example embodiment of a USPM 3802 that operates according to the WLAN communication type/link is described in greater detail in U.S. provisional application Ser. No. 60/147,129 filed August 4, 1999, which is herein incorporated by reference in its entirety. It should be understood that this description is provided for illustrative purposes only are is not limiting. In particular, the invention is not limited to this combination.

An example embodiment of a USPM 3802 that operates according to the CDMA communication type/link is described in greater detail in U.S. patent applications Ser. Nos. 09/525,185 filed 3/14/00 and 09/525,615 filed 3/14/00, which are herein incorporated by reference in its entirety. Another example embodiment of a USPM 3802 that operates according to the CDMA communication type/link is described in greater detail in U.S. patent application "Wireless Telephone Using Universal Frequency Translation," filed April 10, 2000, Attorney Docket Number 1744.0070000, incorporated herein by reference in its entirety. It should be understood that this description is provided for illustrative purposes only and is not limiting. In particular, the invention is not limited to this combination.

The UPSM 3802, and in particular the control module 3812, for the WAP/Bluetooth combination, shall now be described in greater detail. It should be understood that this description is provided for illustrative purposes only are is not limiting. In particular, the invention is not limited to this combination.

FIG. 43 illustrates an embodiment of the invention for the UPSM 3802 and control module 3812. Control module 3812 includes sub-modules which contain implementation and operational instructions for UPSM 3802. In one embodiment,

WAP sub-module 4304 and Bluetooth sub-module 4306 are employed such that the UPSM may operate using either Bluetooth or one of the number of bearer services available to WAP.

In an embodiment, WAP sub-module 4304 contains the WAP protocol stack and specification information about the WAP architecture. For instance, the wireless application environment (WAE) or application layer, session layer (WSP), transaction layer (WTP), security layer (WTLS), and transport layer (WDP). This information would enable control module 3812 to operate the components of UPSM 3802 in a manner that conforms to both the requirements of the protocol, but also to the requirements of the operating environment. The operating environment includes, but is not limited to, the available bearer services, content encoders and decoders employed, available protocol gateways, etc.

In an embodiment, Bluetooth sub-module 4306 contains the Bluetooth protocol stack and specification information about the Bluetooth architecture. For instance, Bluetooth sub-module 4306 includes: 1) the link manager protocol (LMP), which is responsible for link setup between Bluetooth-enabled devices, including authentication and encryption; 2) the logical link control and adaptation protocol (L2CAP), which serves as an adapter between the upper layer protocols and the Bluetooth baseband protocol and permits the higher level protocols to transmit and receive L2CAP data packets; 3) the service discovery protocol (SDP), which discovers information about the devices and services available in the local Bluetooth network, and then enables a connection between two or more Bluetooth-enabled devices; 4) the cable replacement protocol (RFCOMM); 5) the telephony control protocol (TCS BIN); and 6) the telephony control-AT commands.

The Bluetooth sub-module 4306 is not limited to these protocols. Additional protocol and specification information can be included to enhance the functionality of the UPSM 3802. Implementation of the sub-modules of control module 3812 will be apparent to persons skilled in the relevant art(s) based on at least the teachings

contained herein. It should be understood that the examples shown in FIGS. 39 and 40 are provided for illustrative purposes only, and are not limiting. The invention is intended and adapted to operate with other communication links/types, and these will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein.

A device containing at least one UPM, which contains at least one UPSM 3802 of FIG. 43, is capable of linking to wireless networks using any of the bearer services available for the protocols for which it is programmed and/or encoded. In one example, the device is communicating point-of-sale information by operating the receiver 3804 and transmitter 3808 components of UPSM 3802 for Bluetooth. In a nearly simultaneous fashion, the same device is switching the same receiver 3804 and transmitter 3808 components of UPSM 3802 using the wireless application protocol (WAP) to link the device to a cellular network using a CDMA standard bearer service.

In an additional embodiment, a device is able to employ WAP sub-module 4304 to maintain two or more nearly simultaneous links to the same or different bearer services using the same or different standards. For instance, a device is using AMPS to send and receive facsimiles, while a voice call is being maintained over GSM.

UPSM 4102 in the example embodiment shown in FIG. 41 contains a control module 4112 to enable the UPSM 4102 to operate according to multiple protocol/bearer service combinations (FIG. 39) and/or multiple communication link/types (FIG. 40).

In an embodiment, the UPSM 4102 operates according to one such protocol/bearer service combination or communication link/type at any given time. In this embodiment, the UPSM 4102 may operate in a multi-threaded manner so that it switches between protocol/bearer service combination or communication link/type over time. This enables the UPSM 4102 to effectively perform virtual or apparent

simultaneous processing of multiple protocol/bearer service combinations and/or communication link/types.

Thus, the control module 4112 enables the UPSM 4102 to operate in conformance with any combination of protocol/bearer service combinations and communication link/types. In particular, the control module 4112 includes hardware, software, or combinations thereof to cause the UPSM 4102 to receive, transmit, process, and otherwise interact with signals according to any such protocol/bearer service combination or communication link/type. Implementation of the control module 4112 will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein.

In the example shown in FIG. 41, the UPSM 4102 includes a transceiver 4104 having one or more UFT 4106 modules. Alternatively, the UPSM 4102 could have one or more receivers and one or more transmitters each having one or more UFT modules. In some of such embodiments, the UPSM 4102 operates according to one or more protocol/bearer service combinations and/or communication link/types simultaneously at any given time. This enables the UPSM 4102 to perform simultaneous processing of multiple protocol/bearer service combinations and/or communication link/types.

Examples of the UPSM include ones that operate according to the example protocol/bearer service combinations shown in FIG. 39. It should be understood that the examples shown in FIG. 39 are provided for illustrative purposes only, and are not limiting. The invention is intended and adapted to operate with other protocol/bearer service combinations, and these will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein.

Also, FIG. 40 is a representation of groups of communication links or types. The control module 4112 of the UPSM 4102 enables the UPSM 4102 to operate in conformance with any such communication link/type. In particular, the control module 4112 includes hardware, software, or combinations thereof to cause the

UPSM 4102 to receive, transmit, process, and otherwise interact with signals according to the communication link/type. Implementation of the control module 4112 will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein. It should be understood that the examples shown in FIG. 40 are provided for illustrative purposes only, and are not limiting. The invention is intended and adapted to operate with other communication links/types, and these will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein.

An example embodiment of a USPM 4102 that operates according to the WLAN communication type/link is described in greater detail in U.S. provisional application Ser. No. 60/147,129 filed August 4, 1999, which is herein incorporated by reference in its entirety. It should be understood that this description is provided for illustrative purposes only are is not limiting. In particular, the invention is not limited to this combination.

An example embodiment of a USPM 4102 that operates according to the CDMA communication type/link is described in greater detail in U.S. patent applications Ser. Nos. 09/525,185 filed 3/14/00 and 09/525,615 filed 3/14/00, which are herein incorporated by reference in its entirety. Another example embodiment of a USPM 3802 that operates according to the CDMA communication type/link is described in greater detail in U.S. patent application "Wireless Telephone Using Universal Frequency Translation," filed April 10, 2000, Attorney Docket Number 1744.0070000, incorporated herein by reference in its entirety. It should be understood that this description is provided for illustrative purposes only are is not limiting. In particular, the invention is not limited to this combination.

UPSM 4102, and in particular the control module 4112, for the CDMA/GSM combination, shall now be described in greater detail. It should be understood that this description is provided for illustrative purposes only are is not limiting. In particular, the invention is not limited to this combination.

FIG. 44 illustrates an embodiment of the invention for the UPSM 4102 and control module 4112. Control module 4112 includes protocol/bearer service sub-modules (P/BSSM) 4404 which contain implementation and operational instructions for UPSM 4102. In one embodiment, any number of P/BSSM 4404 are employed such that the UPSM may operate using any number of networks.

In an embodiment, P/BSSM 4404 contains the WAP protocol stack and specification information about the WAP architecture. For instance, the wireless application environment (WAE) or application layer, session layer (WSP), transaction layer (WTP), security layer (WTLS), and transport layer (WDP). This information would enable control module 4112 to operate the components of UPSM 4102 in a manner that conforms to both the requirements of the protocol, but also to the requirements of the operating environment. The operating environment includes, but is not limited to, the available bearer services, content encoders and decoders employed, available protocol gateways, etc.

In an embodiment, P/BSSM 4404 contains the Bluetooth protocol stack and specification information about the Bluetooth architecture. For instance, P/BSSM 4404 includes: 1) the link manager protocol (LMP), which is responsible for link setup between Bluetooth-enabled devices, including authentication and encryption; 2) the logical link control and adaptation protocol (L2CAP), which serves as an adapter between the upper layer protocols and the Bluetooth baseband protocol and permits the higher level protocols to transmit and receive L2CAP data packets; 3) the service discovery protocol (SDP), which discovers information about the devices and services available in the local Bluetooth network, and then enables a connection between two or more Bluetooth-enabled devices; 4) the cable replacement protocol (RFCOMM); 5) the telephony control protocol (TCS BIN); and 6) the telephony control-AT commands.

The P/BSSM 4404 is not limited to these protocols. Additional protocol and specification information can be included to enhance the functionality of the UPSM

4102. Implementation of the sub-modules of control module 4112 will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein. It should be understood that the examples shown in FIGS. 39 and 40 are provided for illustrative purposes only, and are not limiting. The invention is intended and adapted to operate with other communication links/types, and these will be apparent to persons skilled in the relevant art(s) based on at least the teachings contained herein.

A device containing at least one UPM, which contains at least one UPSM 4102 of FIG. 44, is capable of linking to networks using any of the bearer services available for the protocols for which it is programmed and/or encoded. In one example, the device is communicating point-of-sale information by operating the transceiver 4104 component of UPSM 4102. Simultaneously, the same device is switching another of the transceiver 4104 components of UPSM 4102 using the wireless application protocol (WAP) to link the device to a cellular network using a CDMA standard bearer service.

In an additional embodiment, a device is able to employ P/BSSM 4404 to maintain two or more simultaneous links to the same or different bearer services using the same or different standards. For instance, a device is using AMPS to send and receive facsimiles, while a voice call is being maintained over GSM.

It is noted that in the embodiments of FIGS. 43 and 44 the instructions programmed and/or encoded into the sub-modules of the control modules may be update, upgraded, replaced, and/or modified in order to provide additional and/or new functionality. The functionality may take the form of new network availability, altered performance characteristics, changes in information exchange formats, etc.

These example embodiments and other alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the example embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the referenced teachings and the teachings contained herein, and are within the scope and

spirit of the present invention. The invention is intended and adapted to include such alternate embodiments.

8.2.2 Universal Platform Module Receiver

The following discussion describes down-converting signals using a Universal Frequency Down-conversion (UFD) Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is described above, and is more fully described in co-pending U.S. Patent Application entitled "Method and System for Down-converting an Electromagnetic Signal," Serial No. 09/176,022, issued as U.S. Patent No. 6,061,551, which is incorporated herein by reference in its entirety.

Exemplary embodiments of the UPM receiver are described below. However, it should be understood that these examples are provided for illustrative purposes only. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

8.2.2.1 Universal Platform Module Receiver Embodiments

FIG. 27A illustrates an embodiment of the receiving UPSM 2706. Receiving UPSM 2706 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiving UPSM 2706 of FIG. 27A comprises at least one UFD module 2702. UFD module 2702 comprises at least one UFT module 2620. Numerous embodiments for receiving UPSM 2706 will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention.

FIG. 27B illustrates an embodiment of the receiving UPSM 2706, in greater detail. Receiving UPSM 2706 comprises a UFD module 2702, an optional amplifier 2705, and an optional filter 2707. UFD module 2702 comprises at least one UFT module 2620.

UFD module 2702 inputs received signal 2704. UFD module 2702 frequency down-converts received signal 2704 to UFD module output signal 2708.

UFD module output signal 2708 is optionally amplified by optional amplifier 2705 and optionally filtered by optional filter 2707, and a down-converted baseband signal 2516 results. The amplifying and filtering functions may instead be provided for in optional signal conditioning module 2523, when present.

Received signals of a variety of modulation types may be down-converted directly to a baseband signal by receiving UPSM 2706 of FIG. 27B. These modulation types include, but are not limited to phase modulation (PM), phase shift keying (PSK), amplitude modulation (AM), amplitude shift keying (ASK), and quadrature amplitude modulation (QAM), and combinations thereof.

In embodiments, UFD module 2702 frequency down-converts received signal 2704 to a baseband signal. In alternative embodiments, UFD module 2702 down-converts received signal 2704 to an intermediate frequency.

FIG. 27C illustrates an alternative embodiment of receiving UPSM 2706 comprising a UFD module 2702 that down-converts received signal 2704 to an intermediate frequency. Receiving UPSM 2706 of FIG. 27C comprises an intermediate frequency (IF) down-converter 2712. IF down-converter 2712 may comprise a UFD module and/or a UFT module, or may comprise a conventional down-converter. In this embodiment, UFD module output signal 2708 is output by

UFD module 2702 at an intermediate frequency. This is an offset frequency, not at baseband. IF down-converter 2712 inputs UFD module output signal 2708, and frequency down-converts it to baseband signal 2710.

Baseband signal 2710 is optionally amplified by optional amplifier 2705 and optionally filtered by optional filter 2707, and a down-converted baseband signal 2516 results.

Receiving UPSM 2706 may further comprise a third stage IF down-converter, and subsequent IF down-converters, as would be required or preferred by some applications. It will be apparent to persons skilled in the relevant art(s) how to design and configure such further IF down-converters from the teachings contained herein. Such implementations are within the scope of the present invention.

8.2.2.1.1 Detailed UFD Module Block Diagram

FIG. 28 illustrates an embodiment of UFD module 2702 of FIG. 27 in greater detail. This embodiment is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

UFD module 2702 comprises a storage device 2802, an oscillator 2804, a pulse-shaping circuit 2806, a reference potential 2808, and a UFT module 2620. As described above, many embodiments exist for UFD module 2702. For instance, in embodiments, oscillator 2804, or both oscillator 2804 and pulse-shaping circuit 2806, may be external to UFD module 2702.

Oscillator 2804 outputs oscillating signal 2810, which is input by pulse-shaping circuit 2806. The output of pulse-shaping circuit 2806 is a control signal

2812, which preferably comprises a string of pulses. Pulse-shaping circuit 2806 controls the pulse width of control signal 2812.

In embodiments, UFT module 2620 comprises a switch. Other embodiments for UFT module 2620 are within the scope of the present invention, such as those described above. One terminal of UFT module 2620 is coupled to a received signal 2704, and a second terminal of UFT module 2620 is coupled to a first terminal of storage device 2802. A second terminal of storage device 2802 is coupled to a reference potential 2808 such as a ground, or some other potential. In a preferred embodiment, storage device 2802 is a capacitor. In an embodiment, the switch contained within UFT module 2620 opens and closes as a function of control signal 2812. As a result of the opening and closing of this switch, a down-converted signal, referred to as UFD module output signal 2708, results. Additional details pertaining to UFD module 2702 are contained in co-pending U.S. Patent Application entitled "Method and System for Down-Converting an Electromagnetic Signal," Serial No. 09/176,022, issued as U.S. Patent No. 6,061,551, which is incorporated herein by reference in its entirety.

8.2.2.2 In-phase/Quadrature-phase (I/Q) Modulation Mode Receiver Embodiments

FIG. 29 illustrates an exemplary I/Q modulation mode embodiment of a receiving UPSM 2706, according to the present invention. This I/Q modulation mode embodiment is described herein for purposes of illustration, and not limitation. Alternate I/Q modulation mode embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiving UPSM 2706 comprises an I/Q modulation mode receiver 2934, a first optional amplifier 2912, a first filter 2914, a second optional amplifier 2916, and a second filter 2918.

I/Q modulation mode receiver 2934 comprises an oscillator 2902, a first UFD module 2904, a second UFD module 2906, a first UFT module 2908, a second UFT module 2910, and a phase shifter 2920.

Oscillator 2902 provides an oscillating signal used by both first UFD module 2904 and second UFD module 2906 via the phase shifter 2920. Oscillator 2902 generates an "I" oscillating signal 2922.

"I" oscillating signal 2922 is input to first UFD module 2904. First UFD module 2904 comprises at least one UFT module 2908. In an embodiment, first UFD module 2904 is structured similarly to UFD module 2702 of FIG. 28, with oscillator 2902 substituting for oscillator 2804, and "I" oscillating signal 2922 substituting for oscillating signal 2810. First UFD module 2904 frequency down-converts and demodulates received signal 2514 to down-converted "I" signal 2926 according to "I" oscillating signal 2922.

Phase shifter 2920 receives "I" oscillating signal 2922, and outputs "Q" oscillating signal 2924, which is a replica of "I" oscillating signal 2922 shifted preferably by 90°.

Second UFD module 2906 inputs "Q" oscillating signal 2924. Second UFD module 2906 comprises at least one UFT module 2910. In an embodiment, second UFD module 2906 is structured similarly to UFD module 2702 of FIG. 28, with "Q" oscillating signal 2924 substituting for oscillating signal 2810. Second UFD module 2906 frequency down-converts and demodulates received signal 2514 to down-converted "Q" signal 2928 according to "Q" oscillating signal 2924.

Down-converted "I" signal 2926 is optionally amplified by first optional amplifier 2912 and optionally filtered by first optional filter 2914, and a first information output signal 2930 is output.

Down-converted "Q" signal 2928 is optionally amplified by second optional amplifier 2916 and optionally filtered by second optional filter 2918, and a second information output signal 2932 is output.

In the embodiment depicted in FIG. 29, first information output signal 2930 and second information output signal 2932 comprise down-converted baseband signal 2516 of FIGS. 27A - 27C. In an embodiment, optional signal conditioning module 2523 receives first information output signal 2930 and second information output signal 2932. These signals may be separately amplified/conditioned by optional signal conditioning module 2523. Optionally amplified and conditioned first information output signal 2930 and second information output signal 2932 may then be individually modulated and up-converted, and subsequently individually transmitted by one or more transmitters. Alternatively, optionally amplified and conditioned first information output signal 2930 and second information output signal 2932 may be modulated, up-converted, recombined into a single signal, and transmitted by a single transmitting UPSM 3006 as shown in FIG. 30 and discussed herein. For example, optionally amplified and conditioned first information output signal 2930 and second information output signal 2932 may be recombined into an I/Q modulated signal for re-transmission, as further described below. In embodiments, optionally amplified and conditioned first information output signal 2930 and second information output signal 2932 may be modulated by the same or different modulation schemes before retransmission, or before recombination and retransmission.

Alternate configurations for I/Q modulation mode receiver 2934 will be apparent to persons skilled in the relevant art(s) from the teachings herein. For instance, an alternate embodiment exists wherein phase shifter 2920 is coupled between received signal 2704 and UFD module 2906, instead of the configuration described above. This and other such I/Q modulation mode receiver embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Reference is made to pending U.S. application Ser. No. "Method, System, and Apparatus for Balanced Frequency Up-conversion of a Baseband Signal," Ser. No. 09/525,615, filed March 14, 2000, for other teachings relating to this I/Q embodiment, which is herein incorporated by reference in its entirety.

8.2.2.3 Unified Down-convert and Filter Receiver Embodiments

As described above, the invention is directed to unified down-conversion and filtering (UDF). UDF according to the invention can be used to perform filtering and/or down-conversion operations.

Many if not all of the applications described herein involve frequency translation operations. Accordingly, the applications described above can be enhanced by using any of the UDF embodiments described herein.

Many if not all of the applications described above involve filtering operations. Accordingly, any of the applications described above can be enhanced by using any of the UDF embodiments described herein.

Accordingly, the invention is directed to any of the applications described herein in combination with any of the UDF embodiments described herein.

For example, a block diagram of a receiving UPSM 2706 incorporating unified down-convert in filtering according to an embodiment of the present invention is illustrated in FIG. 36. Receiving UPSM 2706 comprises a UDF module 3602 and an optional amplifier 3604. UDF Module 3602 both down-converts and filters received signal 3610 and outputs UDF module output signal 3606. UDF module output signal 3606 is optionally amplified by optional amplifier 3604, outputting down-converted baseband signal 2516.

The unified down-conversion and filtering of a signal is described above, and is more fully described in co-pending U.S. Patent Application entitled "Integrated

Frequency Translation And Selectivity," Serial No. 09/175,966, issued as U.S. Patent No. 6,049,706, which is incorporated herein by reference in its entirety.

These example embodiments and other alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the example embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the referenced teachings and the teachings contained herein, and are within the scope and spirit of the present invention. The invention is intended and adapted to include such alternate embodiments.

8.2.2.4 Other Receiver Embodiments

The UPSM receiver embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments include, but are not limited to, down-converting different combinations of modulation techniques in an "I/Q" mode. Such alternate embodiments fall within the scope and spirit of the present invention.

For example, other UPSM receiver embodiments may down-convert signals that have been modulated with other modulation techniques. These would be apparent to one skilled in the relevant art(s) based on the teachings disclosed herein, and include, but are not limited to, amplitude modulation (AM), frequency modulation (FM), quadrature amplitude modulation (QAM), time division multiple access (TDMA), frequency division multiple access (FDMA), code division multiple access (CDMA), down-converting a signal with two forms of modulation embedding thereon, and combinations thereof.

8.2.3 Universal Platform Module Transmitter Embodiments

The following discussion describes frequency up-converting signals to be transmitted by an UPSM, using a Universal Frequency Up-conversion (UFU) Module. Frequency up-conversion of an EM signal is described above, and is more fully described in co-pending U.S. Patent Application entitled "Method and System for Frequency Up-Conversion," Serial No.09/176,154, the full disclosure of which is incorporated herein by reference in its entirety.

Exemplary embodiments of the UPSM transmitter are described below, including PM and I/Q modulation modes. However, it should be understood that these examples are provided for illustrative purposes only. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

8.2.3.1 Various Modulation Mode Transmitter Embodiments, Including Phase Modulation (PM)

FIG. 30A illustrates an exemplary embodiment of the transmitting UPSM 3006. Transmitting UPSM 3006 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Transmitting UPSM 3006 of FIG. 30A comprises at least one UFU module 3004. UFU module 3004 comprises at least one UFT module 2620. Numerous

embodiments for transmitting UPSM 3006 will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention.

FIG. 30B illustrates in greater detail an exemplary embodiment of the transmitting UPSM 3006 of FIG. 30A. Transmitting UPSM 3006 comprises a modulator 3002, a UFU module 3004, and an optional amplifier 3007.

Modulator 3002 of transmitting UPSM 3006 receives a baseband signal 2518. Modulator 3002 modulates baseband signal 2518, according to any modulation scheme, such as those described above. FIG. 31 illustrates an embodiment of modulator 3002. In this exemplary embodiment, the modulation scheme implemented may be phase modulation (PM) or phase shift keying (PSK) modulation. Modulator 3002 comprises an oscillator 3102 and a phase modulator 3104. Phase modulator 3104 receives baseband signal 2518 and an oscillating signal 3106 from oscillator 3102. Phase modulator 3104 phase modulates oscillating signal 3106 using baseband signal 2518. Phase modulators are well known to persons skilled in the relevant art(s). Phase modulator outputs modulated signal 3010, according to PM or PSK modulation.

In FIG. 30B, modulated signal 3010 is received by UFU module 3004. UFU module 3004 includes at least one UFT module 2620. UFU module 3004 frequency up-converts the modulated signal, outputting UFU module output signal 3008.

When present, optional amplifier 3006 amplifies UFU module output signal 3008, outputting up-converted signal 3005.

In alternate embodiments, transmitting UPSM 3006 does not require a modulator 3002 because UFU module 3004 performs the modulation function. FIG. 30C illustrates such an alternate embodiment of transmitting UPSM 3006 of FIG. 30A. Transmitting UPSM 3006 includes a UFU module 3004 and an optional amplifier 3007. UFU module 3004 includes at least one UFT module 2620. UFU module 3004 frequency modulates and up-converts baseband signal 2518 to UFU module output signal 3008. For instance, and without limitation, UFU module 3004

may provide for frequency up-conversion and modulation in an AM modulation mode. AM modulation techniques and other modulation techniques are more fully described in co-pending U.S. Patent Application entitled "Method and System for Frequency Up-Conversion," Serial No. 09/176,154, the full disclosure of which is incorporated herein by reference in its entirety.

8.2.3.1.1 Detailed UFU Module Embodiments

FIG. 33 illustrates a more detailed exemplary circuit diagram of an embodiment of UFU module 3004 of FIG. 30A. UFU module 3004 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

UFU module 3004 comprises a pulse-shaping circuit 3302, a first reference potential 3304, a filter 3306, a second reference potential 3308, a resistor 3310, and a UFT module 2620.

In FIG. 33, pulse shaping circuit 3302 receives baseband signal 2518. Pulse shaping circuit 3302 outputs control signal 3314, which is preferably comprised of a string of pulses. Control signal 3314 controls UFT module 2620, which preferably comprises a switch. Various embodiments for UFT module 2620 are described above. One terminal of UFT module 2620 is coupled to a first reference potential 3304. The second terminal of UFT module 2620 is coupled through resistor 3310 to a second reference potential 3308. In a PM or PSK modulation embodiment, second reference potential 3308 is preferably a constant voltage level. In other embodiments, such as in an amplitude modulation (AM) mode, second reference potential 3308 may be a voltage that varies with the amplitude of the information signal.

The output of UFT module 2620 is a harmonically rich signal 3312. Harmonically rich signal 3312 has a fundamental frequency and phase substantially proportional to control signal 3314, and an amplitude substantially proportional to the amplitude of second reference potential 3308. Each of the harmonics of harmonically rich signal 3312 also have phase proportional to control signal 3314, and in an PM or PSK embodiment are thus considered to be PM or PSK modulated.

Harmonically rich signal 3312 is received by filter 3306. Filter 3306 preferably has a high Q. Filter 3306 preferably selects the harmonic of harmonically rich signal 3312 that is at the approximate frequency desired for transmission. Filter 3306 removes the undesired frequencies that exist as harmonic components of harmonically rich signal 3312. Filter 3306 outputs UFU module output signal 3008.

Further details pertaining to UFU module 3004 are provided in co-pending U.S. Patent Application entitled "Method and System for Frequency Up-Conversion," Serial No. 09/176,154, which is incorporated herein by reference in its entirety.

8.2.3.2 In-phase/Quadrature-phase (I/Q) Modulation Mode Transmitter Embodiments

In FIG. 34, an I/Q modulation mode embodiment is presented. In this embodiment, two information signals are accepted. An in-phase signal ("I") is modulated such that its phase varies as a function of one of the information signals, and a quadrature-phase signal ("Q") is modulated such that its phase varies as a function of the other information signal. The two modulated signals are combined to form an "I/Q" modulated signal and transmitted. In this manner, for instance, two separate information signals could be transmitted in a single signal simultaneously. Other uses for this type of modulation would be apparent to persons skilled in the relevant art(s).

FIG. 34 illustrates an exemplary block diagram of a transmitting UPSM 3006 operating in an I/Q modulation mode. In FIG. 34, baseband signal 2518 comprises

two signals, first information signal 3402 and second information signal 3404. Transmitting UPSM 3006 comprises an I/Q transmitter 3406 and an optional amplifier 3408. I/Q transmitter 3406 comprises at least one UFT module 2620. I/Q transmitter 3406 provides I/Q modulation to first information signal 3402 and second information signal 3404, outputting I/Q output signal 3410. Optional amplifier 3408 optionally amplifies I/Q output signal 3410, outputting up-converted signal 3005.

FIG. 35 illustrates a more detailed circuit block diagram for I/Q transmitter 3406. I/Q transmitter 3406 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

I/Q transmitter 3406 comprises a first UFU module 3502, a second UFU module 3504, an oscillator 3506, a phase shifter 3508, a summer 3510, a first UFT module 3512, a second UFT module 3514, a first phase modulator 3528, and a second phase modulator 3530.

Oscillator 3506 generates an "I"-oscillating signal 3516.

A first information signal 3402 is input to first phase modulator 3528. The "I"-oscillating signal 3516 is modulated by first information signal 3402 in the first phase modulator 3528, thereby producing an "I"-modulated signal 3520.

First UFU module 3502 inputs "I"-modulated signal 3520, and generates a harmonically rich "I" signal 3524 with a continuous and periodic wave form.

The phase of "I"-oscillating signal 3516 is shifted by phase shifter 3508 to create "Q"-oscillating signal 3518. Phase shifter 3508 preferably shifts the phase of "I"-oscillating signal 3516 by 90 degrees.

A second information signal 3404 is input to second phase modulator 3530. "Q"-oscillating signal 3518 is modulated by second information signal 3404 in second phase modulator 3530, thereby producing a "Q" modulated signal 3522.

Second UFU module 3504 inputs "Q" modulated signal 3522, and generates a harmonically rich "Q" signal 3526, with a continuous and periodic waveform.

Harmonically rich "I" signal 3524 and harmonically rich "Q" signal 3526 are preferably rectangular waves, such as square waves or pulses (although the invention is not limited to this embodiment), and are comprised of pluralities of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveforms. These sinusoidal waves are referred to as the harmonics of the underlying waveforms, and a Fourier analysis will determine the amplitude of each harmonic.

Harmonically rich "I" signal 3524 and harmonically rich "Q" signal 3526 are combined by summer 3510 to create harmonically rich "I/Q" signal 3534. Summers are well known to persons skilled in the relevant art(s).

Filter 3532 filters out the undesired harmonic frequencies, and outputs an I/Q output signal 3410 at the desired harmonic frequency or frequencies.

It will be apparent to persons skilled in the relevant art(s) that an alternative embodiment exists wherein the harmonically rich "I" signal 3524 and the harmonically rich "Q" signal 3526 may be filtered before they are summed, and further, another alternative embodiment exists wherein "I"-modulated signal 3520 and "Q"-modulated signal 3522 may be summed to create an "I/Q"-modulated signal before being routed to a switch module. Other "I/Q"-modulation embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention. Further details pertaining to an I/Q modulation mode transmitter are provided in co-pending U.S. Patent Application entitled "Method and System for Frequency Up-Conversion," Serial No. 09/176,154, which is incorporated herein by reference in its entirety.

Reference is made to pending U.S. application Ser. No. "Method, System, and Apparatus for Balanced Frequency Up-conversion of a Baseband Signal," Ser. No. 09/525,615, filed March 14, 2000, for other teachings relating to this I/Q embodiment, which is herein incorporated by reference in its entirety.

8.2.3.3 Other Transmitter Embodiments

The UPSM transmitter embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments include, but are not limited to, combinations of modulation techniques in an "I/Q" mode. Such alternate embodiments fall within the scope and spirit of the present invention.

For example, other UPSM transmitter embodiments may utilize other modulation techniques. These would be apparent to one skilled in the relevant art(s) based on the teachings disclosed herein, and include, but are not limited to, amplitude modulation (AM), frequency modulation (FM), quadrature amplitude modulation (QAM), time division multiple access (TDMA), frequency division multiple access (FDMA), code division multiple access (CDMA), embedding two forms of modulation onto a signal for up-conversion, etc., and combinations thereof.

8.2.4 Enhanced Signal Reception Universal Platform Embodiments

In additional embodiments of the present invention, enhanced signal reception (ESR) according to the present invention may be used. As discussed above, the invention is directed to methods and systems for ESR. Any of the example applications discussed above can be modified by incorporating ESR therein to enhance communication between transmitters and receivers. Accordingly, the invention is also directed to any of the applications described above, in combination with any of the ESR embodiments described above. Enhanced signal reception using redundant spectrums is described above, and is fully described in co-pending U.S. Patent Application entitled "Method and System for Ensuring Reception of a

Communications Signal," Serial No. 09/176,415, which is incorporated herein by reference in its entirety.

For example, in an embodiment, transmitting UPSM 3006 may comprise a transmitter configured to transmit redundant spectrums, and receiving UPSM 2706 may be configured to receive and process such redundant spectrums, similarly to the system shown in FIG. 21. In an alternative embodiment, UPM 2606 may include transceivers configured to transmit, and to receive and process redundant spectrums. Accordingly, the invention is directed to any of the applications described herein in combination with any of the ESR embodiments described herein.

These example embodiments and other alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the example embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the referenced teachings and the teachings contained herein, and are within the scope and spirit of the present invention. The invention is intended and adapted to include such alternate embodiments.

8.2.5 Universal Platform Transceiver Embodiments

As discussed above, in other embodiments of the present invention, UPM 2606 may include a transceiver unit, rather than a separate receiver and transmitter. Furthermore, the invention is directed to any of the applications described herein in combination with any of the transceiver embodiments described herein.

An exemplary embodiment of a transceiving UPSM 3706 of the present invention is illustrated in FIG. 37. Transceiving UPSM 3706 includes a UFT module 2620. In one embodiment, UPM 2606 includes more than one transceiver UPSM 3706.

Transceiving UPSM 3706 frequency down-converts first EM signal 2514, and outputs down-converted baseband signal 2516. In an embodiment (not shown), each

transceiving UPSM 3706 comprises one or more UFT modules 2620 at least for frequency down-conversion.

Transceiving UPSM 3706 frequency up-converts down-converted baseband signal 2518. UFT module 2620 provides at least for frequency up-conversion. In alternate embodiments, UFT module 2620 only supports frequency down-conversion, and at least one additional UFT module 2620 provides for frequency up-conversion. The up-converted signal is output by transceiving UPSM 3706.

Further example embodiments of receiver/transmitter systems applicable to the present invention may be found in co-pending U.S. Patent Application entitled "Method and System for Frequency Up-Conversion," Serial No. 09/176,154, incorporated by reference in its entirety.

These example embodiments and other alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the example embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the referenced teachings and the teachings contained herein, and are within the scope and spirit of the present invention. The invention is intended and adapted to include such alternate embodiments.

Reference is made to pending U.S. application Ser. No. "Method, System, and Apparatus for Balanced Frequency Up-conversion of a Baseband Signal," Ser. No. 09/525,615, filed March 14, 2000, for other teachings relating to this embodiment, which is herein incorporated by reference in its entirety.

8.2.6 Other Universal Platform Module Embodiments

The UPM and UPSM embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained

herein. Such alternate embodiments include, but are not limited to, receiving a signal of a first modulation type and re-transmitting the signal in a different modulation mode. Another such alternate embodiment includes receiving a signal of a first frequency and re-transmitting the signal at a different frequency. Such alternate embodiments fall within the scope and spirit of the present invention.

8.3 Multi-Mode Infrastructure

The invention is also directed to multi-mode infrastructure embodiments for interacting with the devices discussed above. Such infrastructure embodiments include, but are not limited to, servers, routers, access points, and any other components for enabling multi-mode operation as described herein.

For example, consider a scenario of a commercial airplane. The passengers traveling in the airplane may have devices where they (1) receive flight information, (2) receive telephone calls, and/or (3) receive email. There may be a number of mediums by which such information can be received. For example, such information might be received via a wireless telephone network, or via a WLAN internal to the airplane, or via a short range wireless communication medium. The airplane may have infrastructure components to receive and route such information to the passengers' devices. The infrastructure components include control modules for enabling such operation.

In an embodiment, such infrastructure embodiments include one or more receivers, transmitters, and/or transceivers that include UFTs as described herein. In embodiments, such infrastructure embodiments include UPMs and UPSMs as described herein.

8.4 Additional Multi-mode Teachings

Additional teachings relating to multi-mode methods, apparatuses, and systems according to embodiments of the invention are described in the following applications (as well as others cited above), which are all herein incorporated by reference in their entireties:

"Family Radio System with Multi-Mode and Multi-Band Functionality," Ser. No. 09/476,093, filed January 3, 2000, Attorney Docket No. 1744.0260001.

"Multi-Mode, Multi-Band Communications System," Ser. No. 09/476,330, filed January 3, 2000, Attorney Docket No. 1744.0330001.

9. Conclusion

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What Is Claimed Is:

1. A universal platform module, comprising:

at least one universal platform sub-module, comprising at least one universal frequency conversion module that frequency converts a signal; and

a control module that provides operating information for said at least one universal platform sub-module.

2. The universal platform module of claim 1, wherein said at least one universal platform sub-module represents a receiving universal platform module comprising at least one universal frequency down-conversion module that frequency down-converts a signal.

3. The universal platform module of claim 1, wherein said at least one universal platform sub-module represents a transmitting universal platform sub-module comprising at least one universal frequency up-conversion module that frequency up-converts a signal.

4. A universal multi-mode infrastructure module, comprising:

at least one universal platform module, having:

at least one universal platform sub-module, comprising at least one universal frequency conversion module that frequency converts a signal; and

a control module that provides operating information for said at least one universal platform sub-module.

Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology

Abstract

A communication system comprising a multi-protocol, multi-bearer sub-system is described herein. The sub-system is a universal platform module that can transmit and receive one or more information signals in one or more protocols using one or more bearer services. In one embodiment, the sub-system may form a portion of a transceiver that is composed of a transmitter and a receiver, and which is a gateway server between a personal area network (PAN) and the global wireless network.

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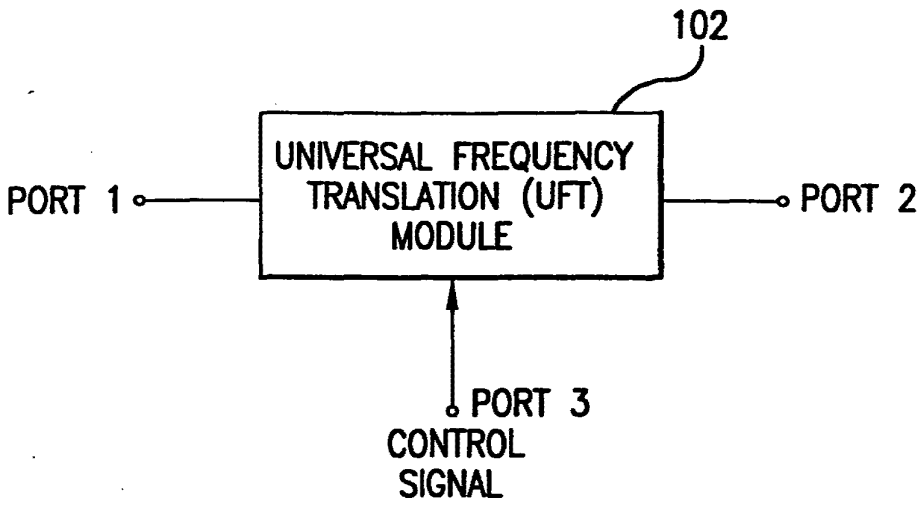

102
UNIVERSAL FREQUENCY TRANSLATION (UFT) MODULE
PORT 1
PORT 2
PORT 3
CONTROL SIGNAL

FIG. 1A

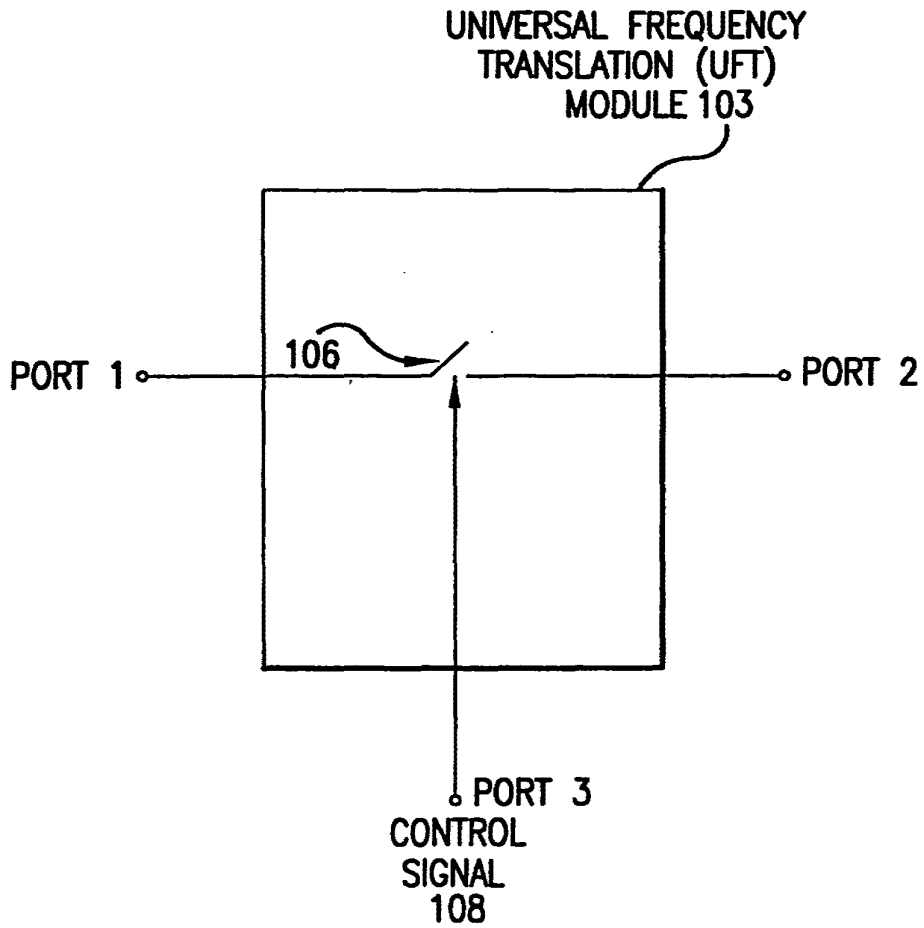

UNIVERSAL FREQUENCY TRANSLATION (UFT) MODULE 103
106
PORT 1
PORT 2
PORT 3
CONTROL SIGNAL 108

FIG. 1B

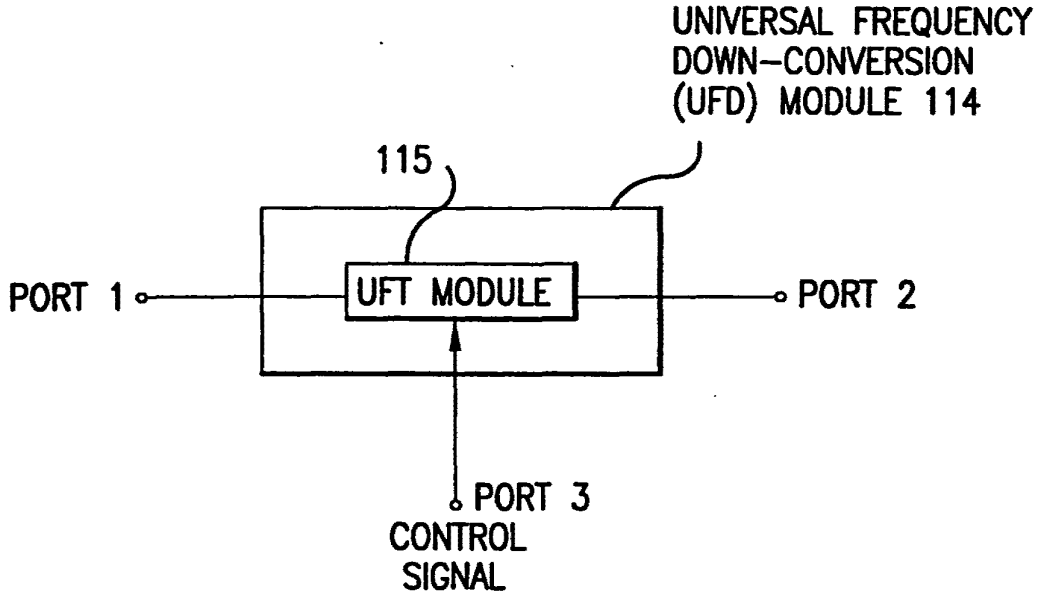

UNIVERSAL FREQUENCY
DOWN-CONVERSION
(UFD) MODULE 114
115
PORT 1
UFT MODULE
PORT 2
PORT 3
CONTROL
SIGNAL

FIG. 1C

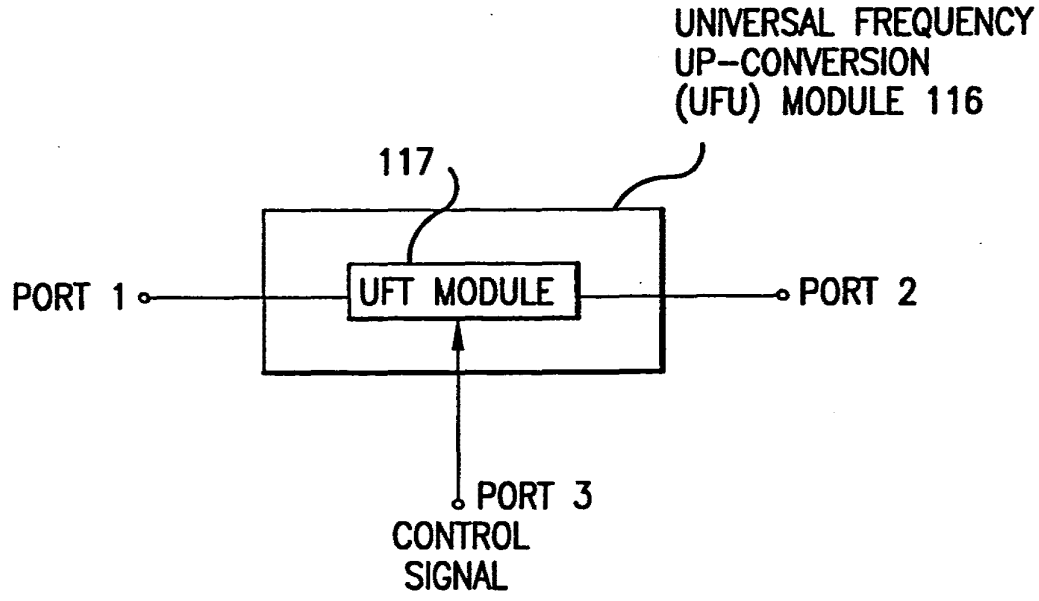

UNIVERSAL FREQUENCY
UP-CONVERSION
(UFU) MODULE 116
117
PORT 1
UFT MODULE
PORT 2
PORT 3
CONTROL
SIGNAL

FIG. 1D

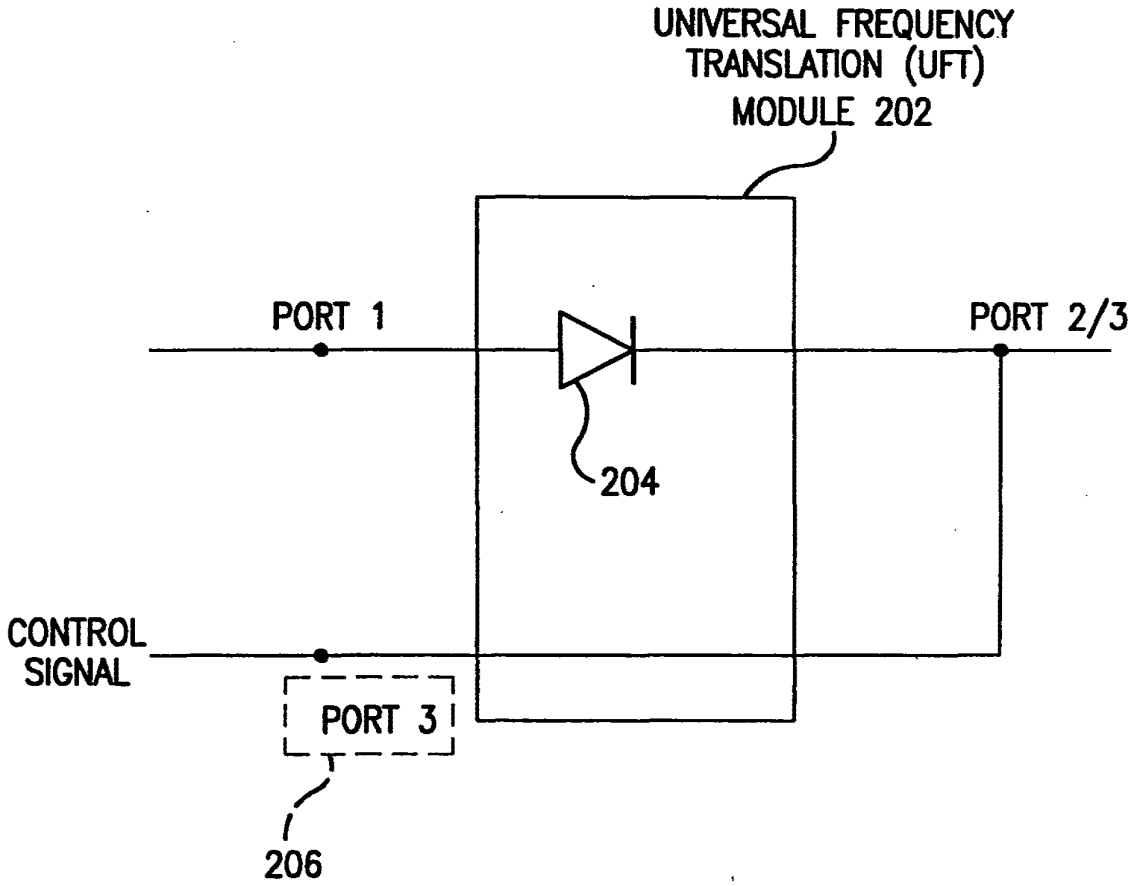

UNIVERSAL FREQUENCY
TRANSLATION (UFT)
MODULE 202
PORT 1
PORT 2/3
204
CONTROL
SIGNAL
PORT 3
206

FIG. 2

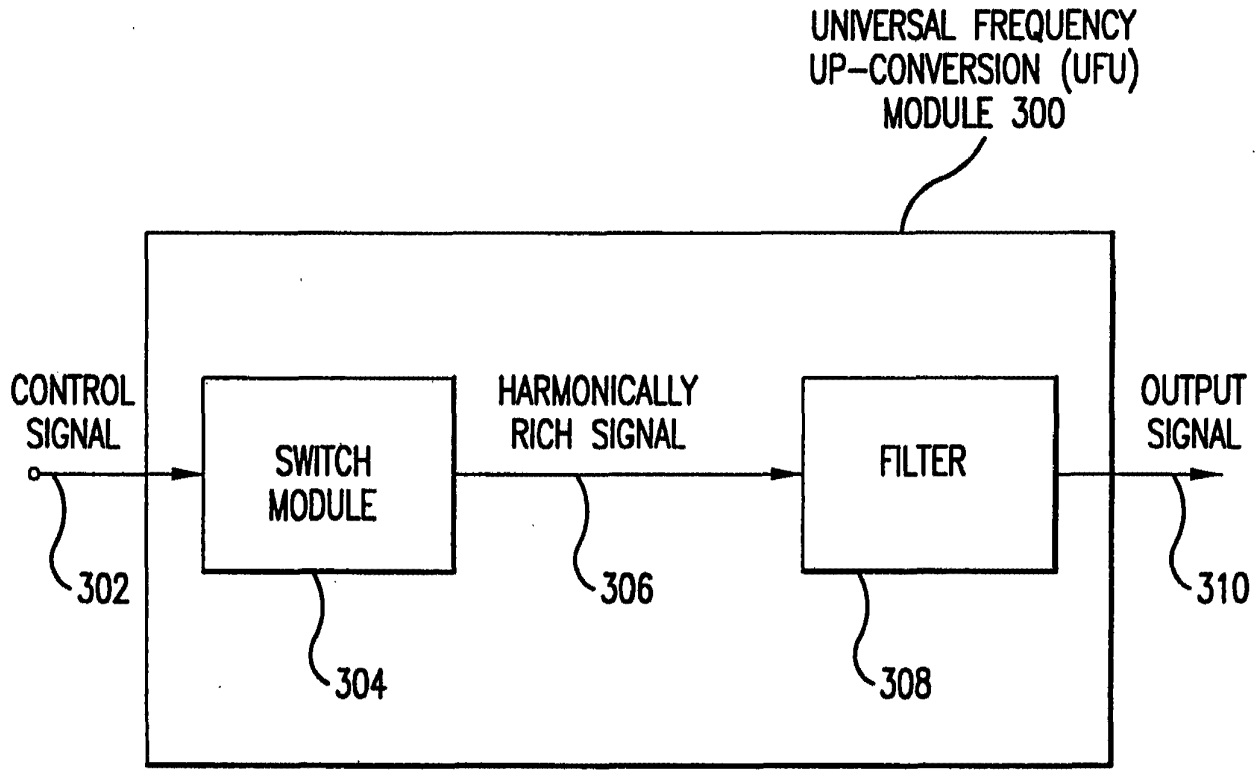

UNIVERSAL FREQUENCY
UP-CONVERSION (UFU)
MODULE 300
CONTROL
SIGNAL
SWITCH
MODULE
HARMONICALLY
RICH SIGNAL
FILTER
OUTPUT
SIGNAL
302
304
306
308
310

FIG. 3

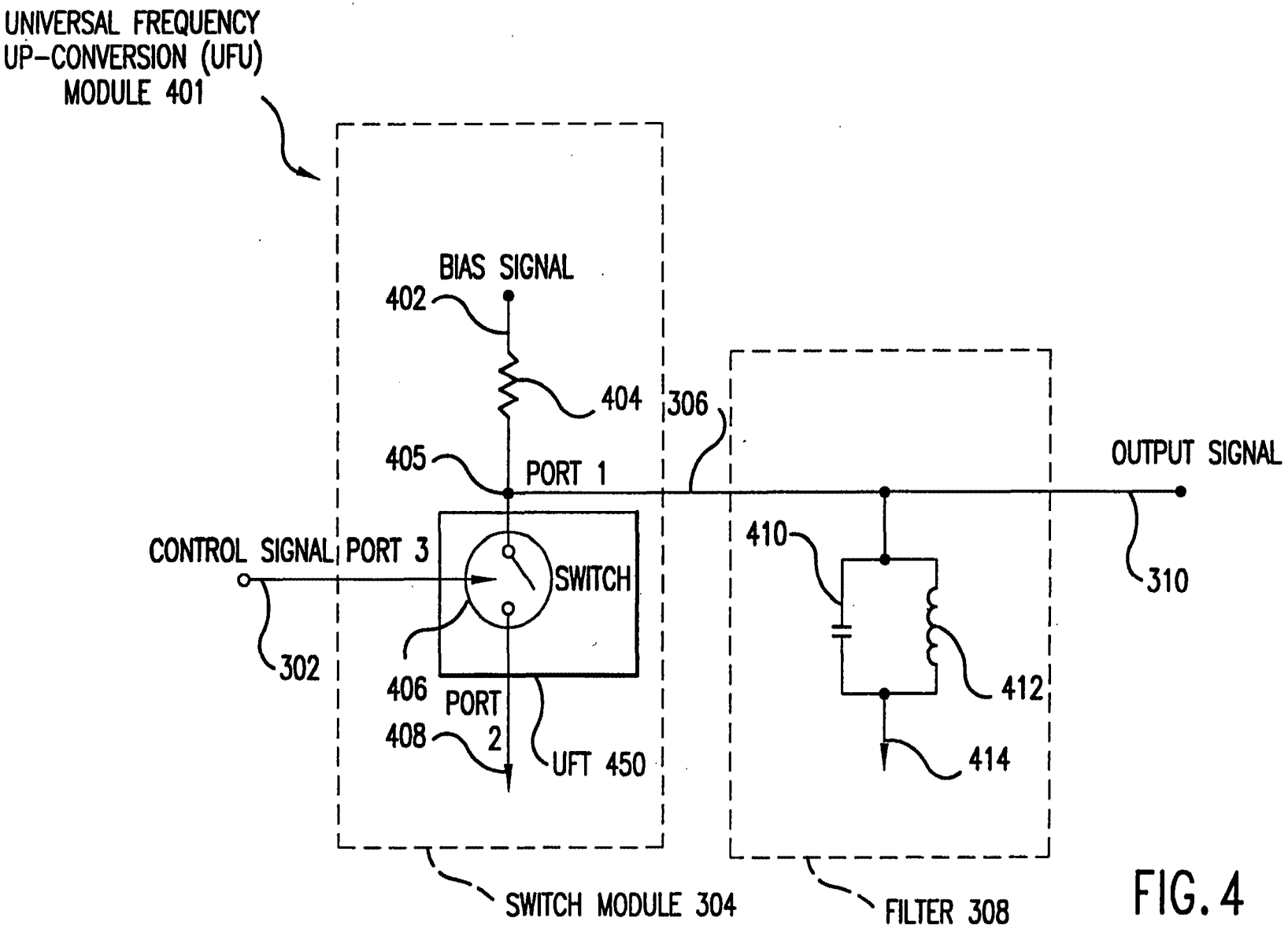

UNIVERSAL FREQUENCY
UP-CONVERSION (UFU)
MODULE 401
BIAS SIGNAL
402
404
306
405
PORT 1
OUTPUT SIGNAL
CONTROL SIGNAL
PORT 3
SWITCH
410
310
302
406
PORT
2
412
408
UFT 450
414
SWITCH MODULE 304
FILTER 308

FIG. 4

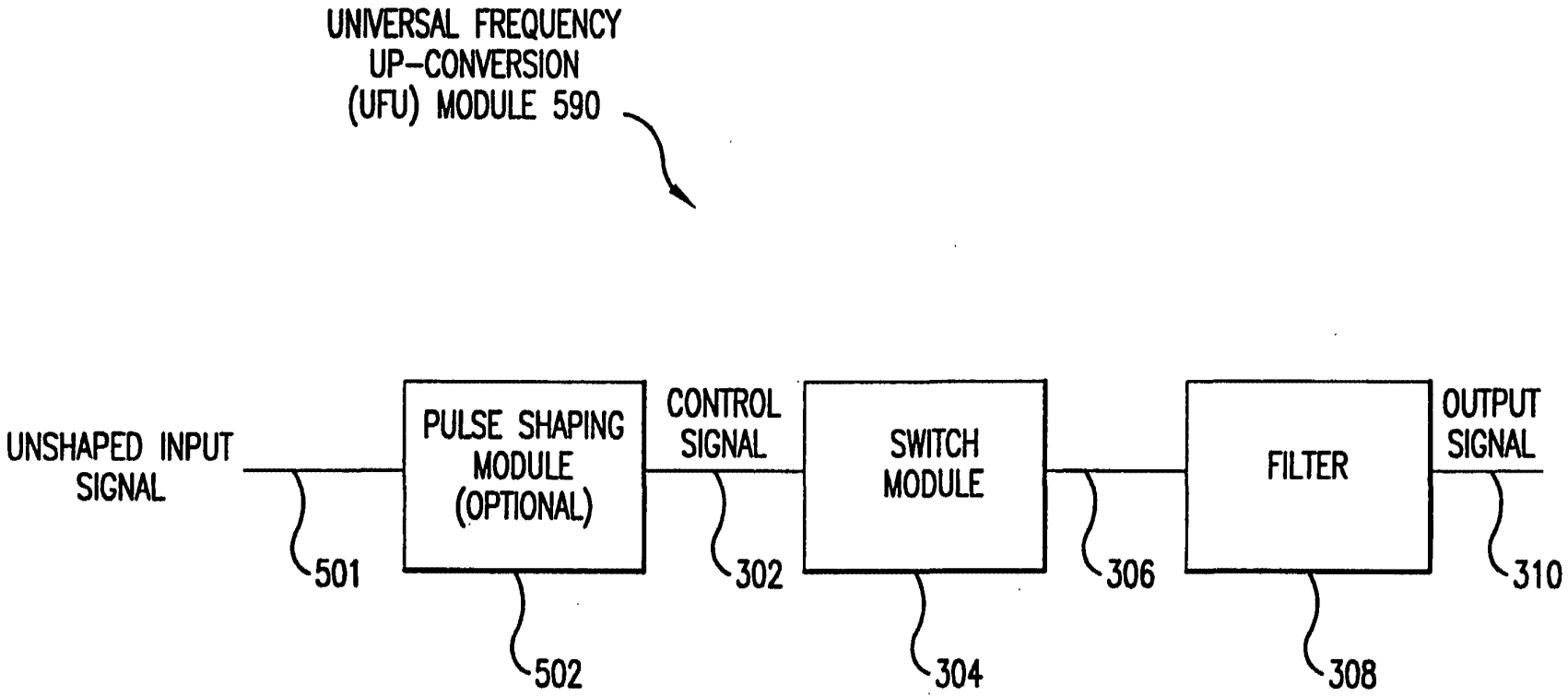

UNIVERSAL FREQUENCY
UP-CONVERSION
(UFU) MODULE 590
UNSHAPED INPUT
SIGNAL
501
PULSE SHAPING
MODULE
(OPTIONAL)
502
CONTROL
SIGNAL
302
SWITCH
MODULE
304
306
FILTER
308
OUTPUT
SIGNAL
310

FIG. 5

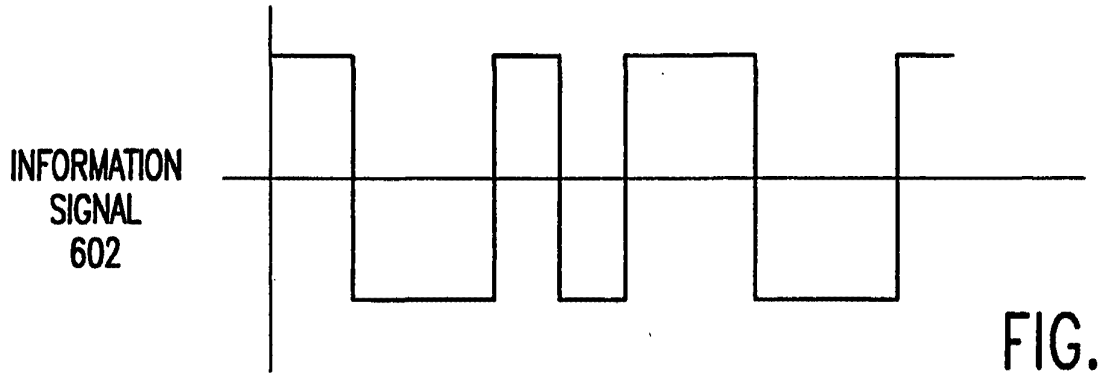


FIG. 6A

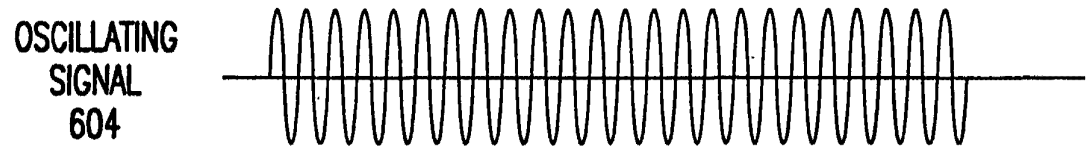


FIG. 6B

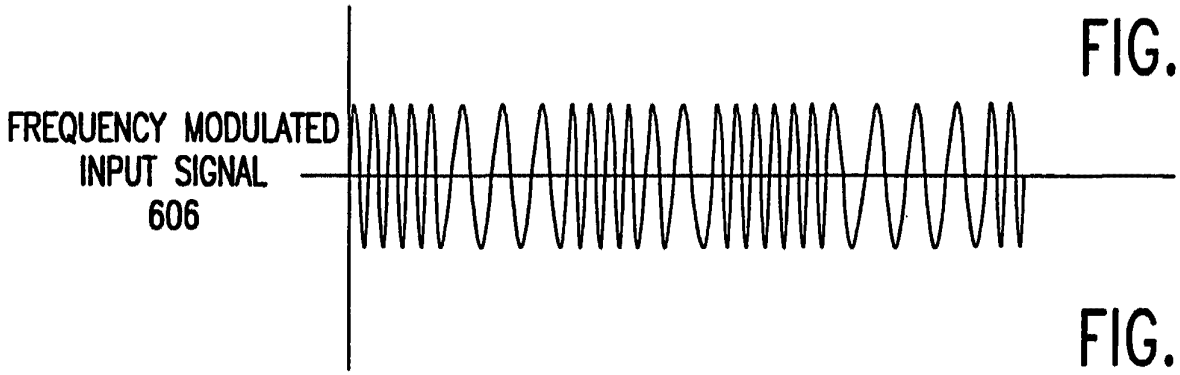


FIG. 6C

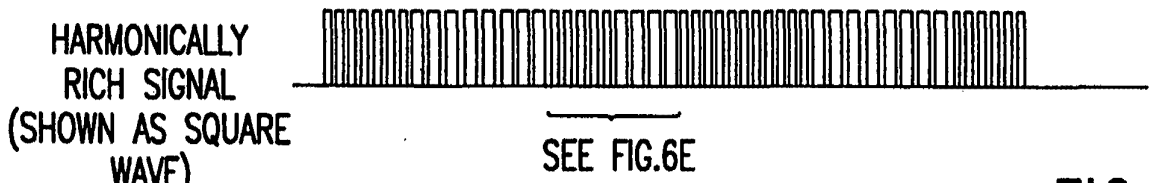


FIG. 6D

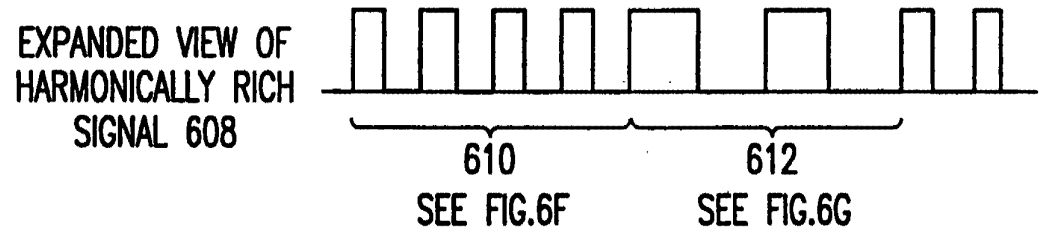


FIG. 6E

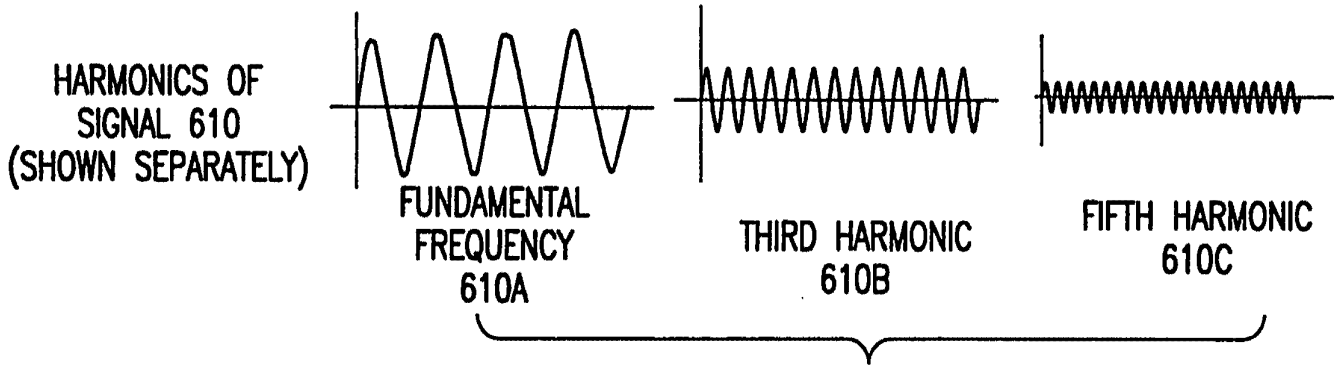


FIG. 6F

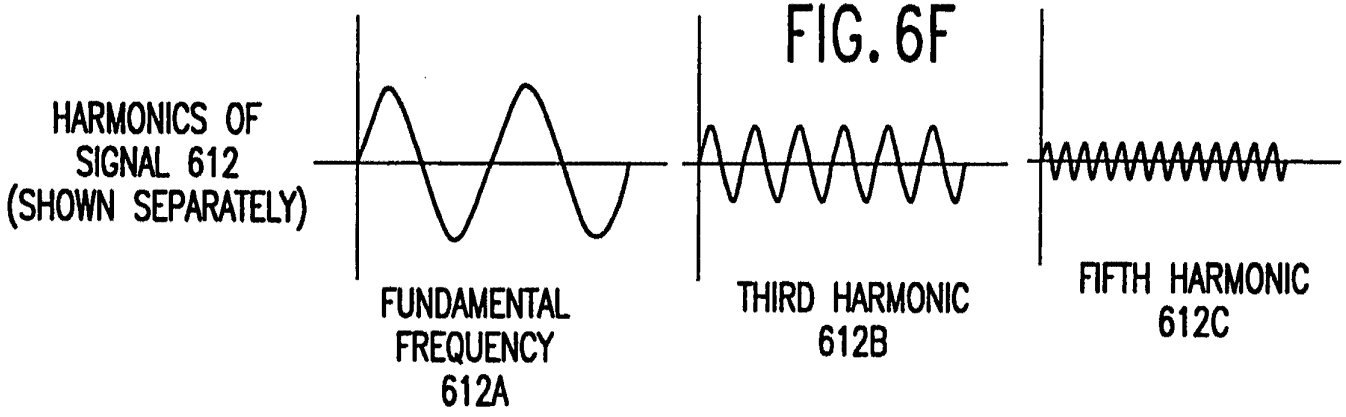


FIG. 6G

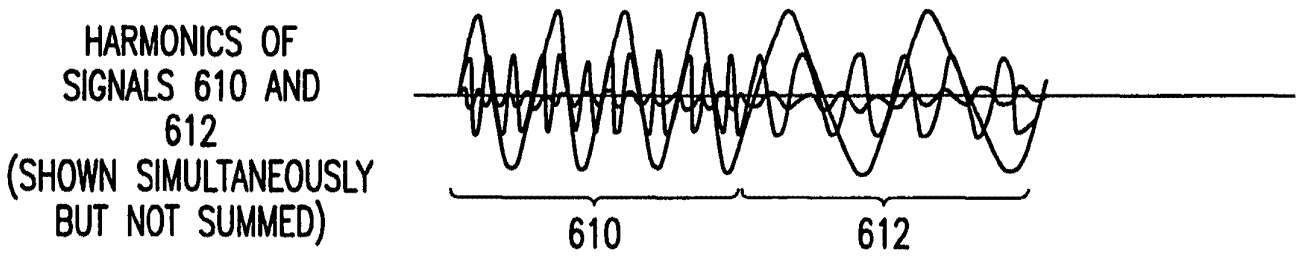

HARMONICS OF
SIGNALS 610 AND
612
(SHOWN SIMULTANEOUSLY
BUT NOT SUMMED)
610
612

FIG. 6H

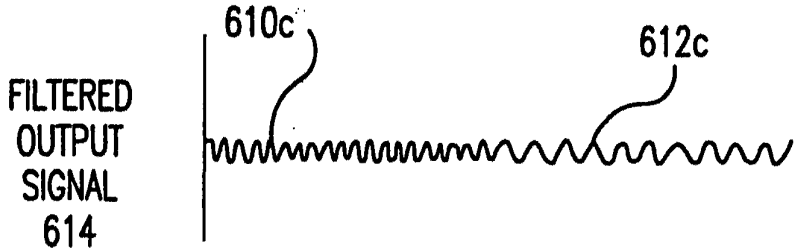

610c
612c
FILTERED
OUTPUT
SIGNAL
614

FIG. 6I

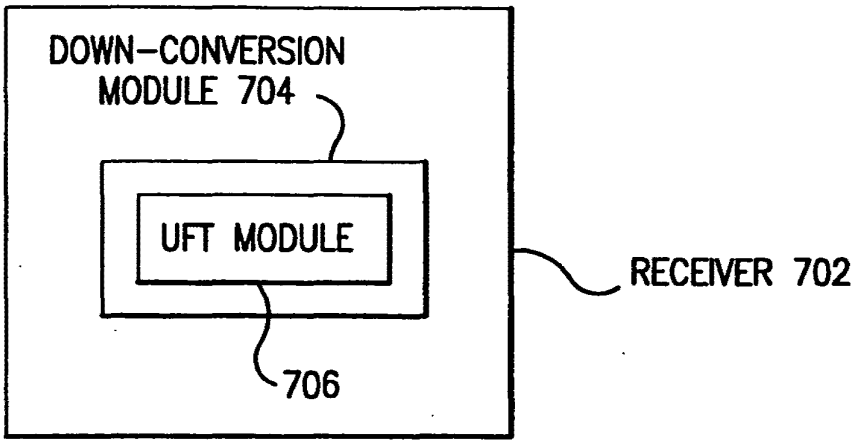

DOWN-CONVERSION
MODULE 704
UFT MODULE
706
RECEIVER 702

FIG. 7

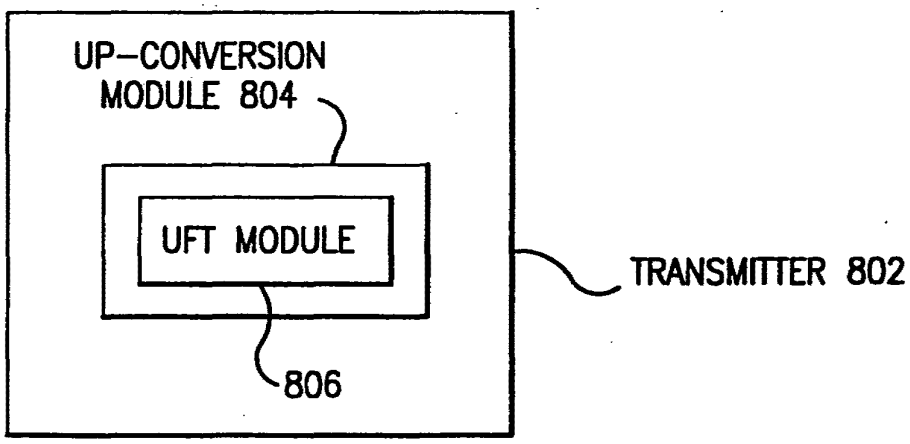

UP-CONVERSION
MODULE 804
UFT MODULE
806
TRANSMITTER 802

FIG. 8

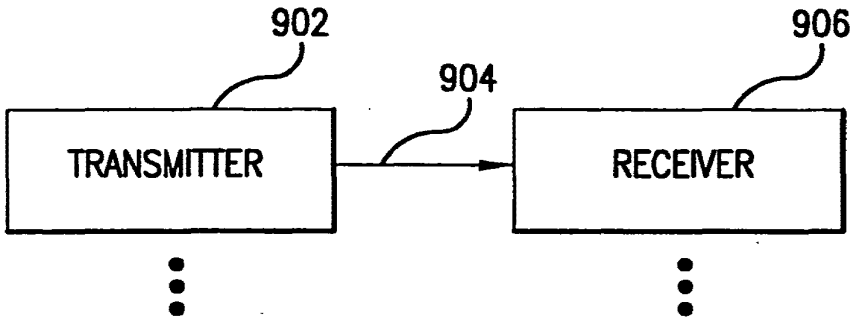

902
906
904
TRANSMITTER
RECEIVER

FIG. 9

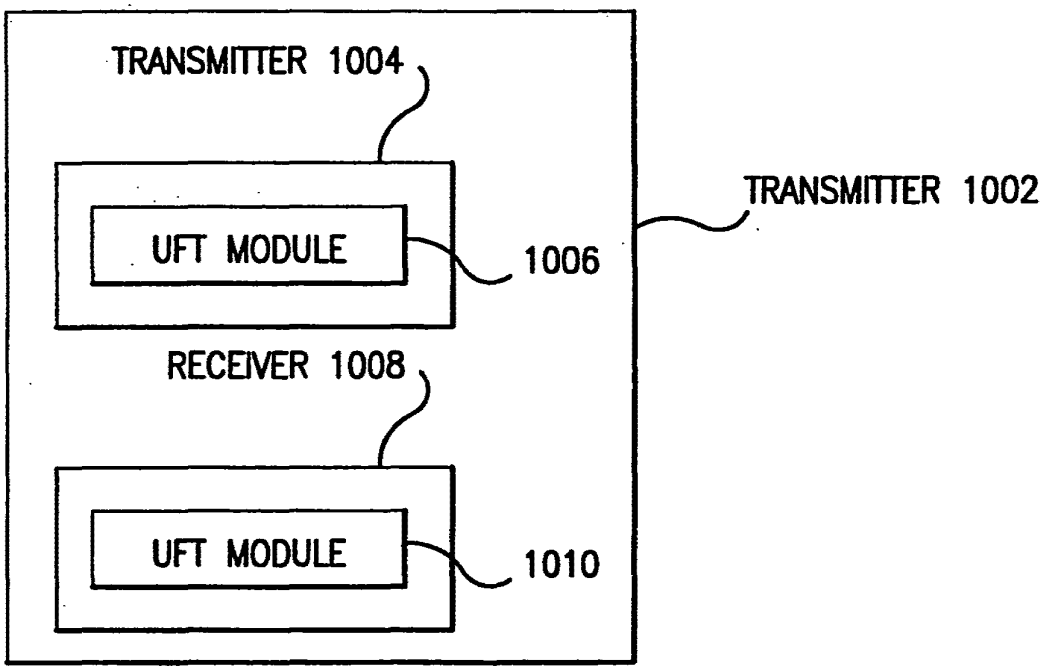

TRANSMITTER 1004
TRANSMITTER 1002
UFT MODULE
1006
RECEIVER 1008
UFT MODULE
1010

FIG. 10

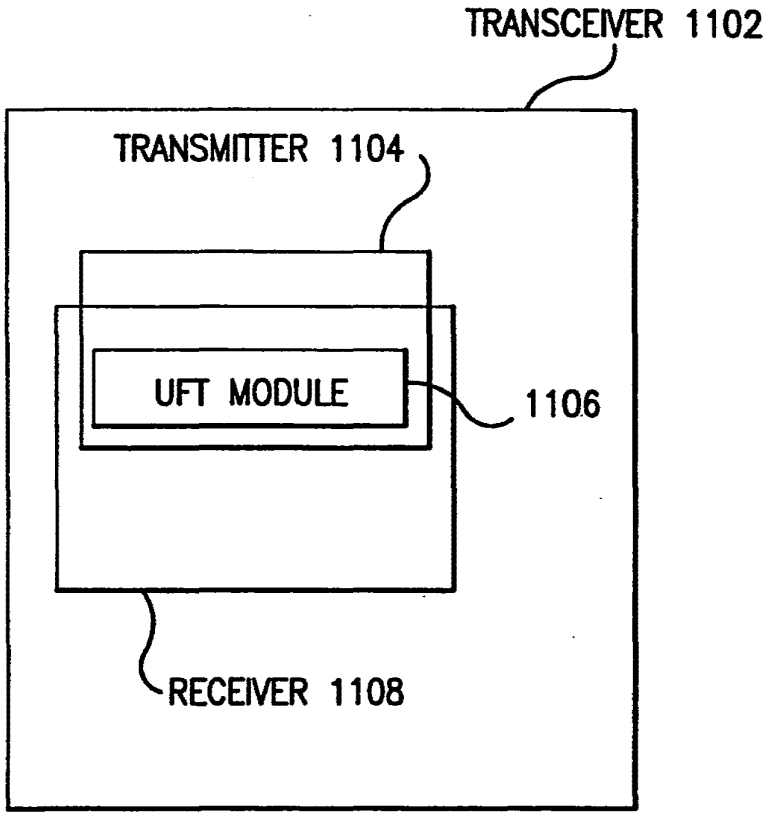

TRANSCEIVER 1102
TRANSMITTER 1104
UFT MODULE
1106
RECEIVER 1108

FIG. 11

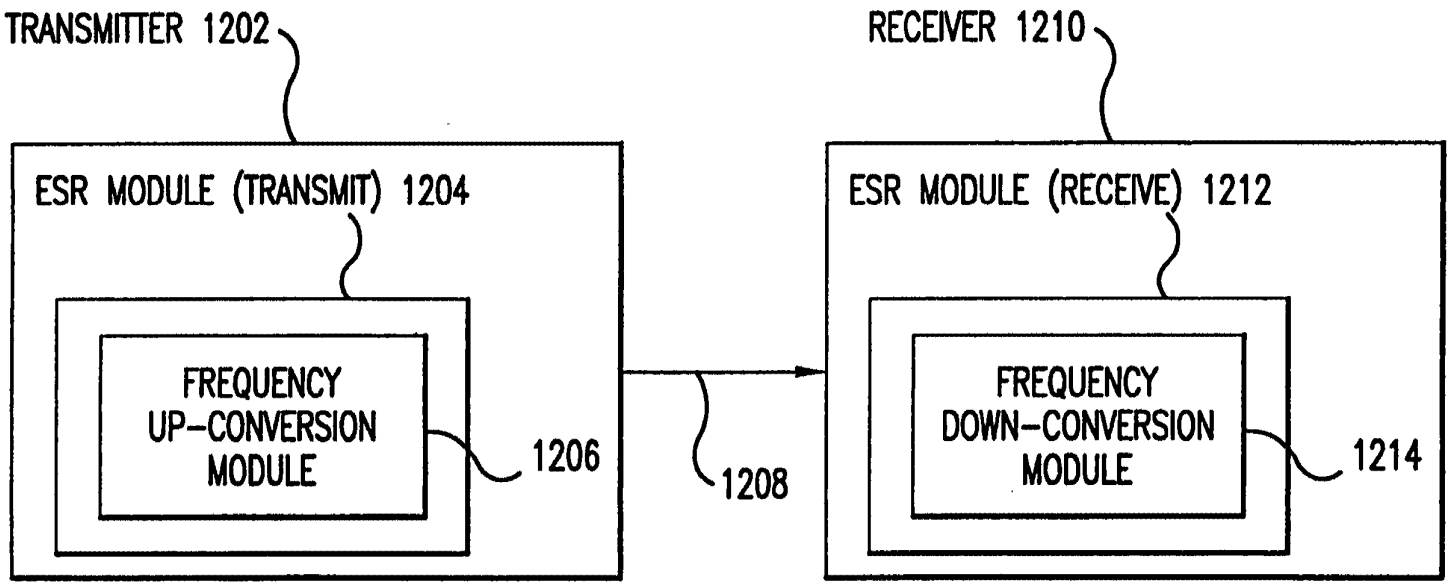

TRANSMITTER 1202
RECEIVER 1210
ESR MODULE (TRANSMIT) 1204
ESR MODULE (RECEIVE) 1212
FREQUENCY UP-CONVERSION MODULE
1206
1208
FREQUENCY DOWN-CONVERSION MODULE
1214

FIG. 12

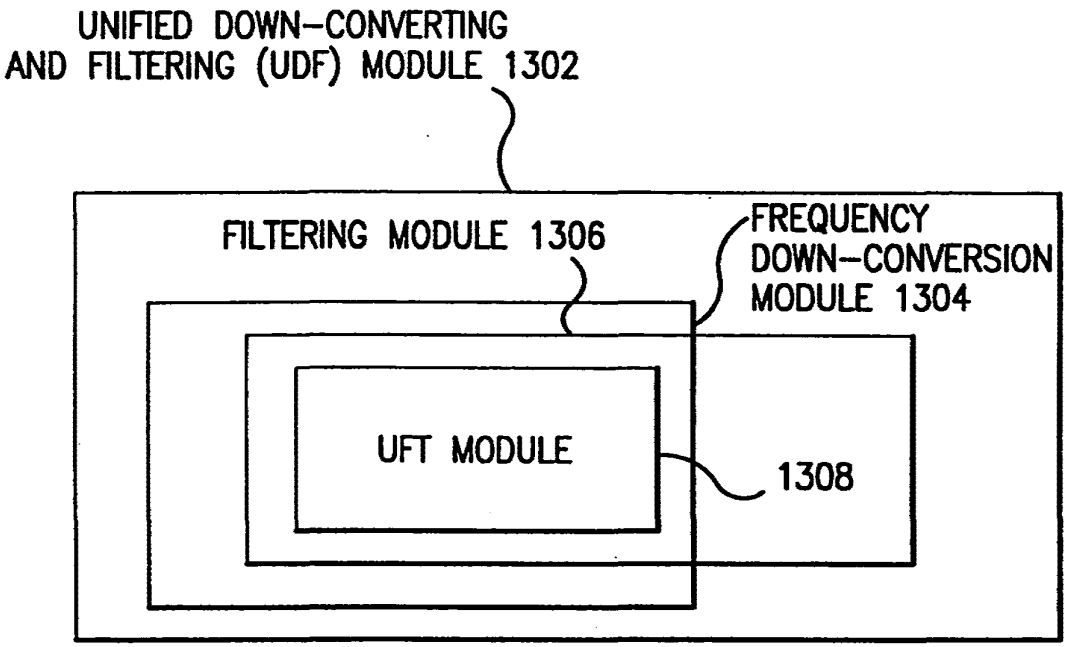

UNIFIED DOWN-CONVERTING
AND FILTERING (UDF) MODULE 1302
FILTERING MODULE 1306
FREQUENCY
DOWN-CONVERSION
MODULE 1304
UFT MODULE
1308

FIG. 13

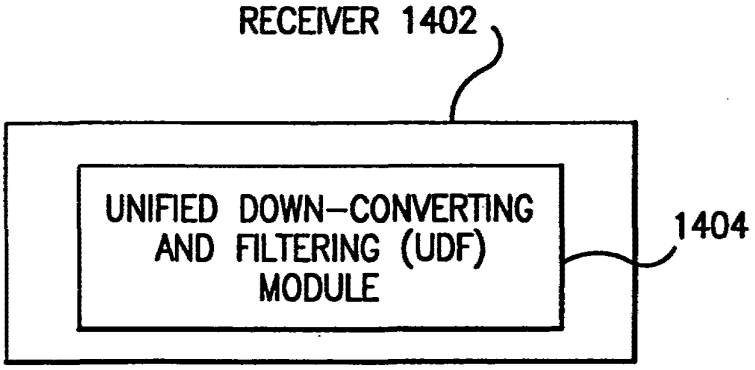

RECEIVER 1402
UNIFIED DOWN-CONVERTING
AND FILTERING (UDF)
MODULE
1404

FIG. 14

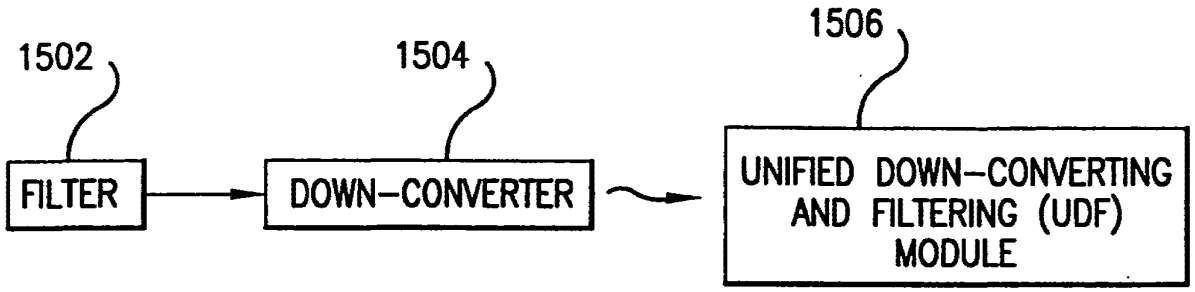


FIG. 15A

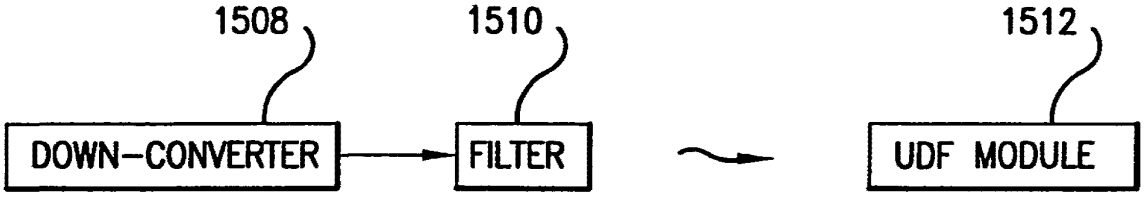


FIG. 15B

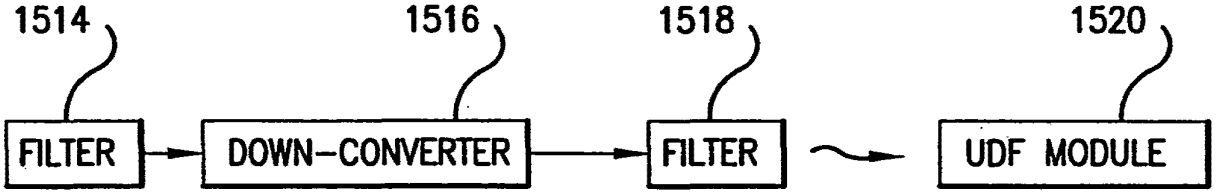


FIG. 15C

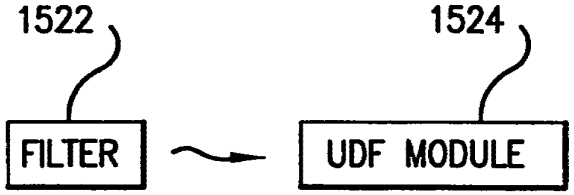


FIG. 15D

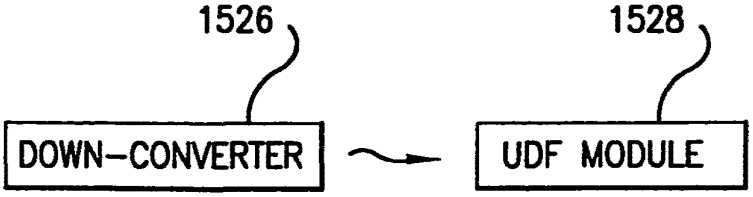


FIG. 15E

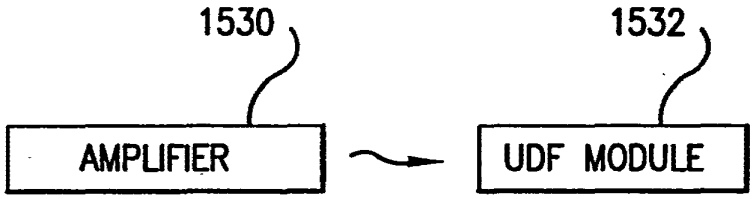


FIG. 15F

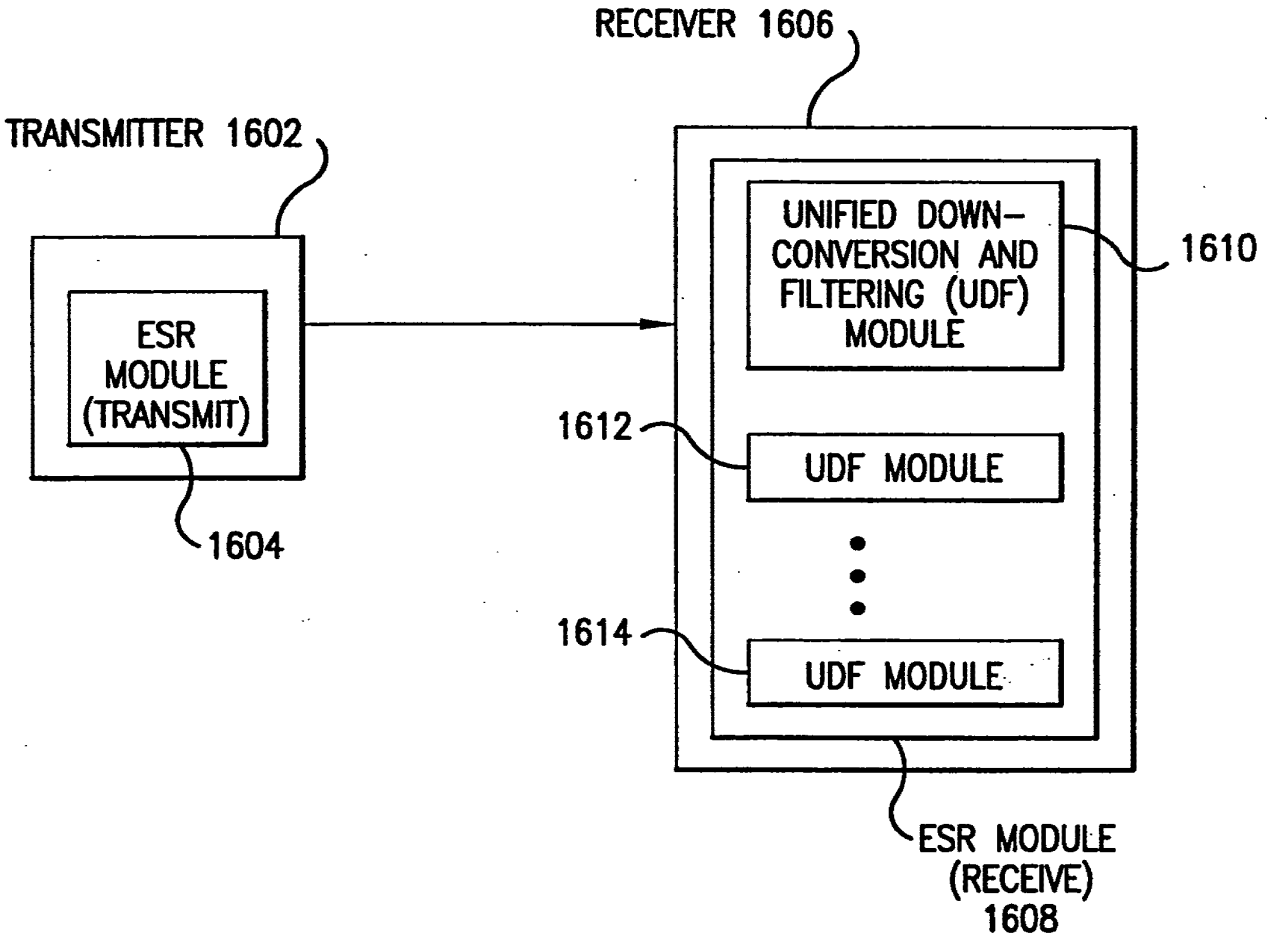

RECEIVER 1606
TRANSMITTER 1602
UNIFIED DOWN-CONVERSION AND FILTERING (UDF) MODULE
1610
ESR MODULE (TRANSMIT)
1612
UDF MODULE
1614
UDF MODULE
1604
ESR MODULE (RECEIVE) 1608

FIG. 16

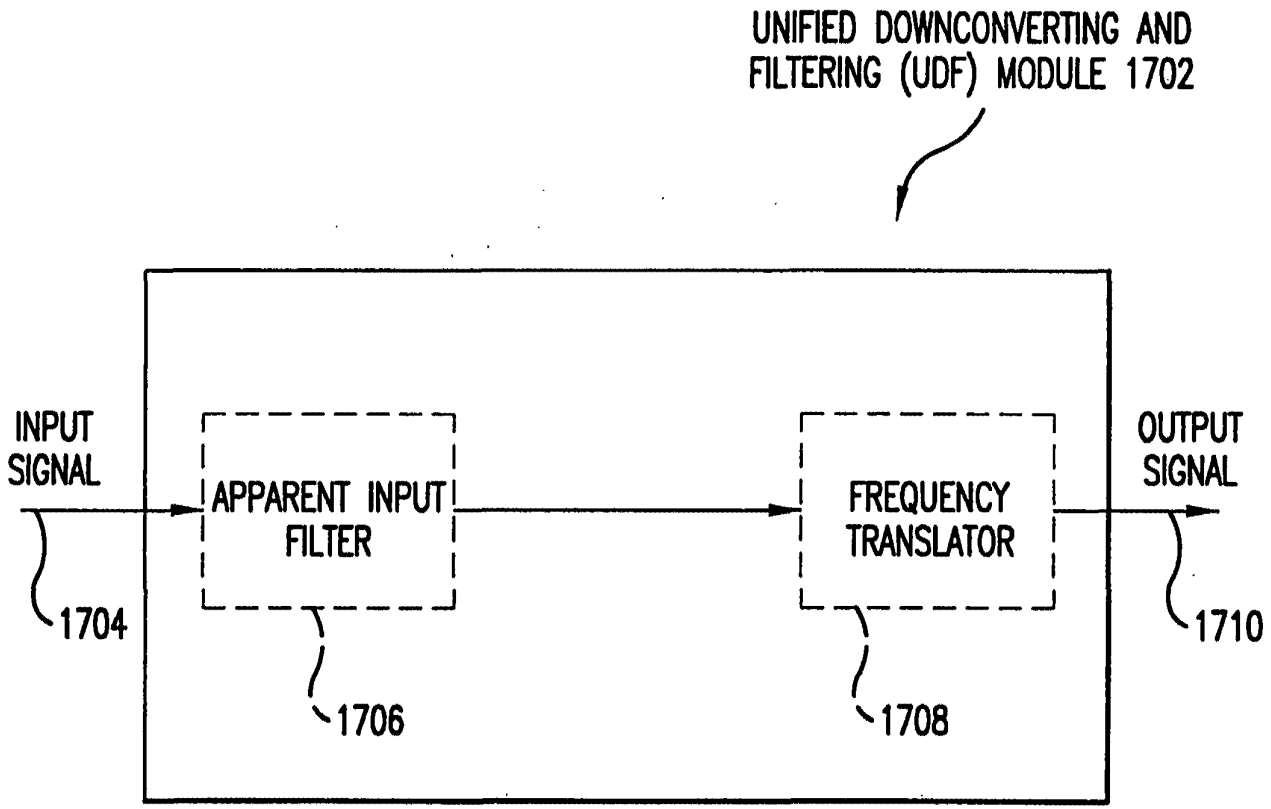

UNIFIED DOWNCONVERTING AND
FILTERING (UDF) MODULE 1702
INPUT
SIGNAL
1704
APPARENT INPUT
FILTER
1706
FREQUENCY
TRANSLATOR
1708
OUTPUT
SIGNAL
1710

FIG. 17

1802

TIME NODE	t−1 (RISING EDGE OF ϕ_1)	t−1 (RISING EDGE OF ϕ_2)	t (RISING EDGE OF ϕ_1)	t (RISING EDGE OF ϕ_2)	t+1 (RISING EDGE OF ϕ_1)
1902	VI_{t-1} 1804	VI_{t-1} 1808	VI_t 1816	VI_t 1826	VI_{t+1} 1838
1904	—	VI_{t-1} 1810	VI_{t-1} 1818	VI_t 1828	VI_t 1840
1906	VO_{t-1} 1806	VO_{t-1} 1812	VO_t 1820	VO_t 1830	VO_{t+1} 1842
1908	—	VO_{t-1} 1814	VO_{t-1} 1822	VO_t 1832	VO_t 1844
1910	— 1807	—	VO_{t-1} 1824	VO_{t-1} 1834	VO_t 1846
1912	—	— 1815	—	VO_{t-1} 1836	VO_{t-1} 1848
1918	—	—	—	—	VI_t − 1850 $0.1*VO_t$ − $0.8*VO_{t-1}$

FIG. 18

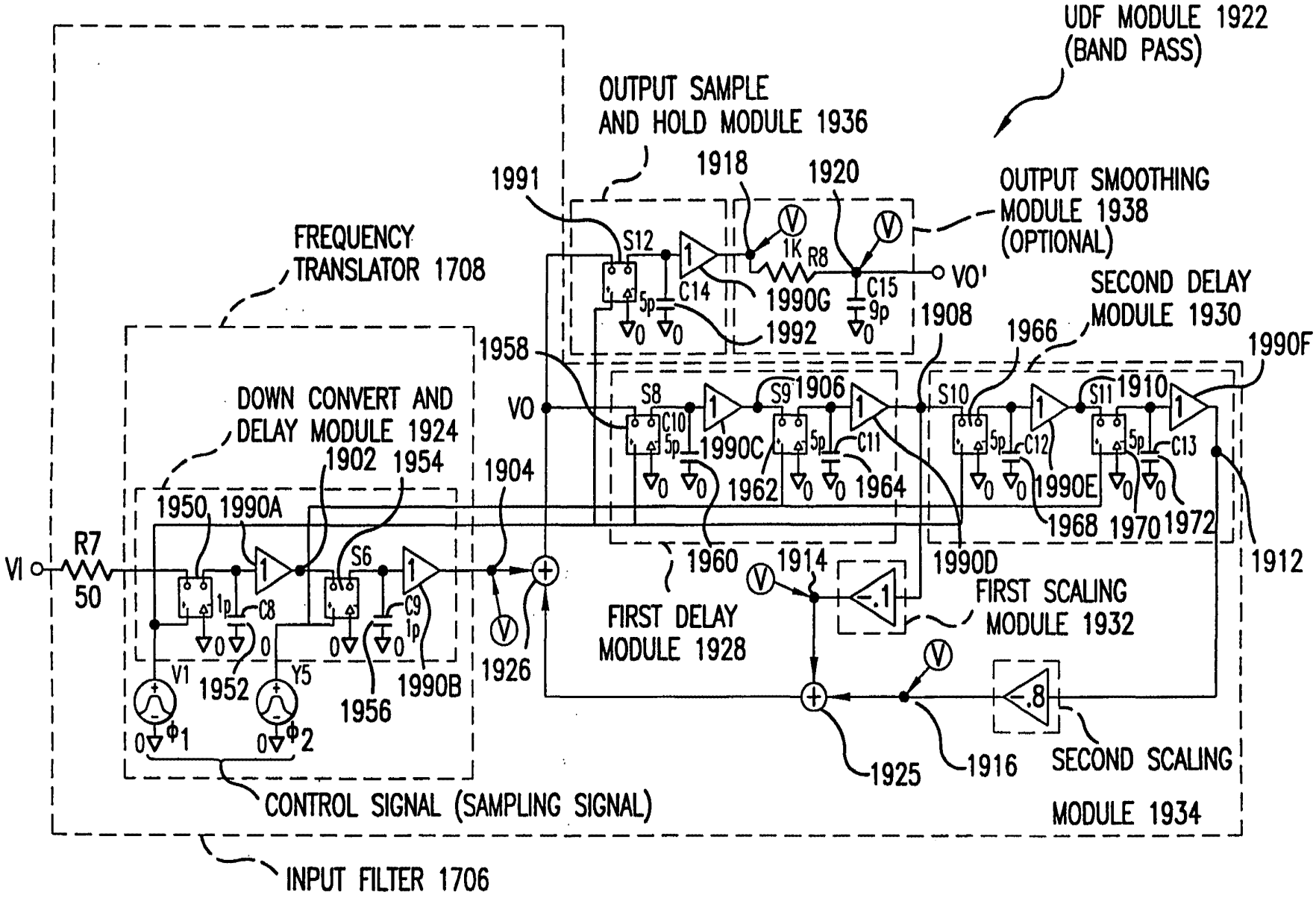

UDF MODULE 1922
(BAND PASS)
OUTPUT SAMPLE
AND HOLD MODULE 1936
1991
1918
1920
OUTPUT SMOOTHING
MODULE 1938
(OPTIONAL)
FREQUENCY
TRANSLATOR 1708
S12
1K R8
VO'
C14
1990G
C15
9p
5p
1992
SECOND DELAY
MODULE 1930
1908
1966
1990F
1958
VO
S8
S9
1906
S10
S11
1910
C10
5p
1990C
C11
C12
C13
1962
1964
1990E
1968
1970
1972
DOWN CONVERT AND
DELAY MODULE 1924
1902
1954
1904
1950
1990A
VI
R7
50
S6
1p
C8
C9
1990B
1952
1956
V1
Y5
Φ1
Φ2
1926
1960
1914
1990D
FIRST DELAY
MODULE 1928
FIRST SCALING
MODULE 1932
1912
1925
1916
SECOND SCALING
MODULE 1934
CONTROL SIGNAL (SAMPLING SIGNAL)
INPUT FILTER 1706

FIG. 19

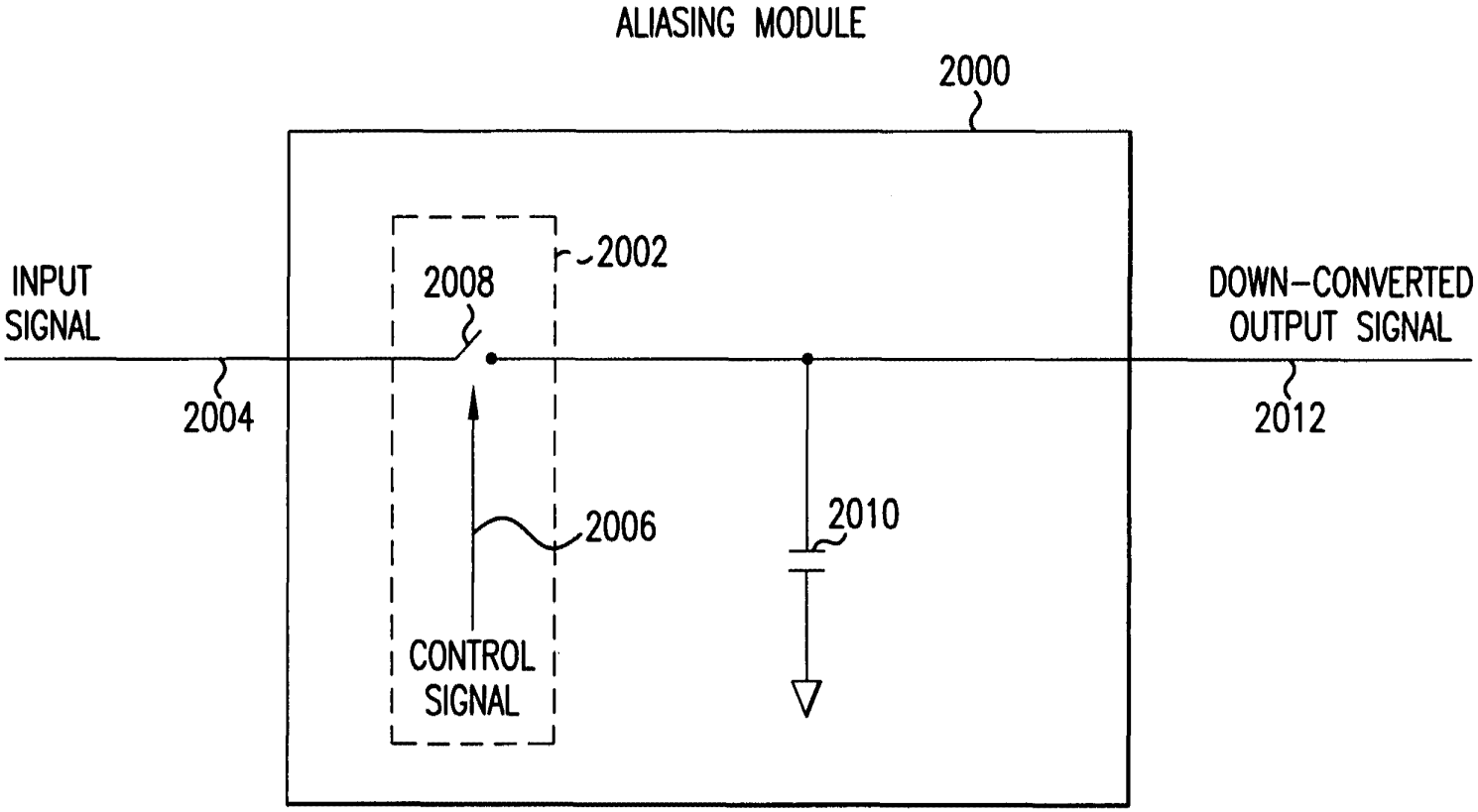

ALIASING MODULE
2000
INPUT SIGNAL
2004
2008
2002
2006
CONTROL SIGNAL
2010
DOWN-CONVERTED OUTPUT SIGNAL
2012

FIG.20A

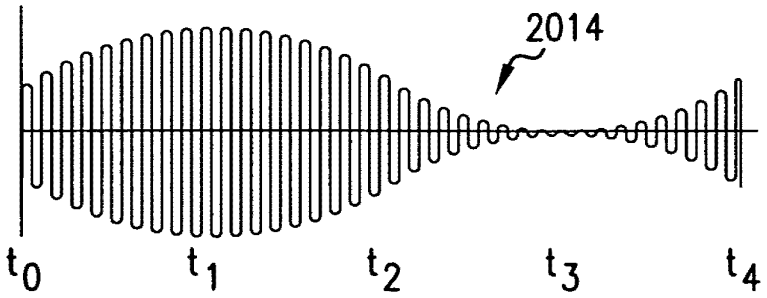


FIG.20B

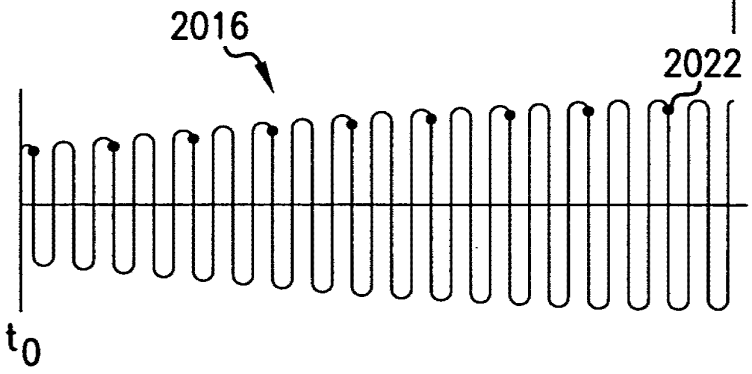


FIG.20C

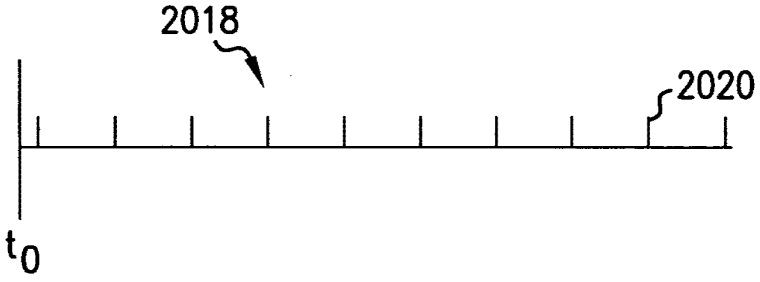


FIG.20D

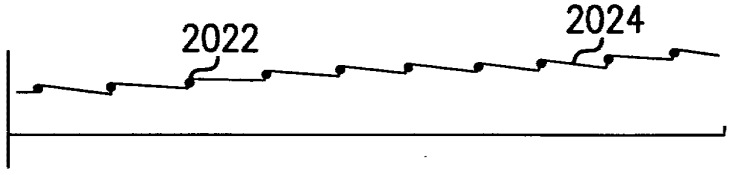


FIG.20E



FIG.20F

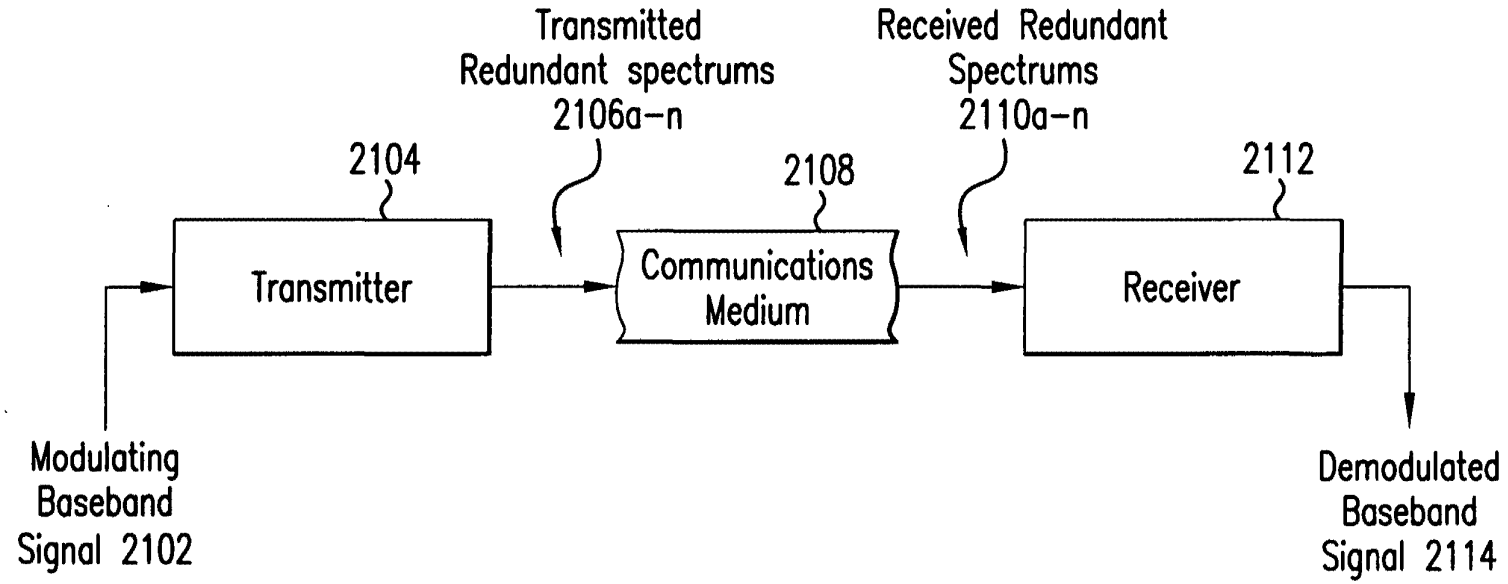

Transmitted
Redundant spectrums
2106a-n
Received Redundant
Spectrums
2110a-n
2104
2108
2112
Transmitter
Communications
Medium
Receiver
Modulating
Baseband
Signal 2102
Demodulated
Baseband
Signal 2114

FIG.21

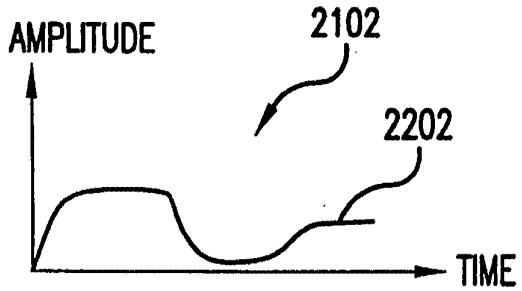


FIG. 22A

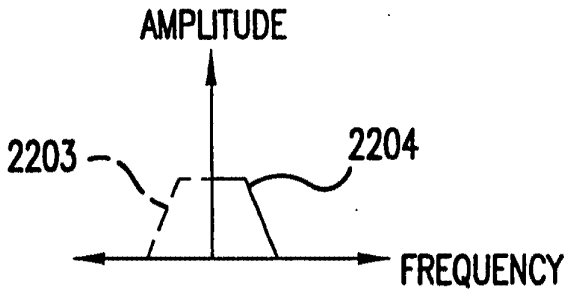


FIG. 22B

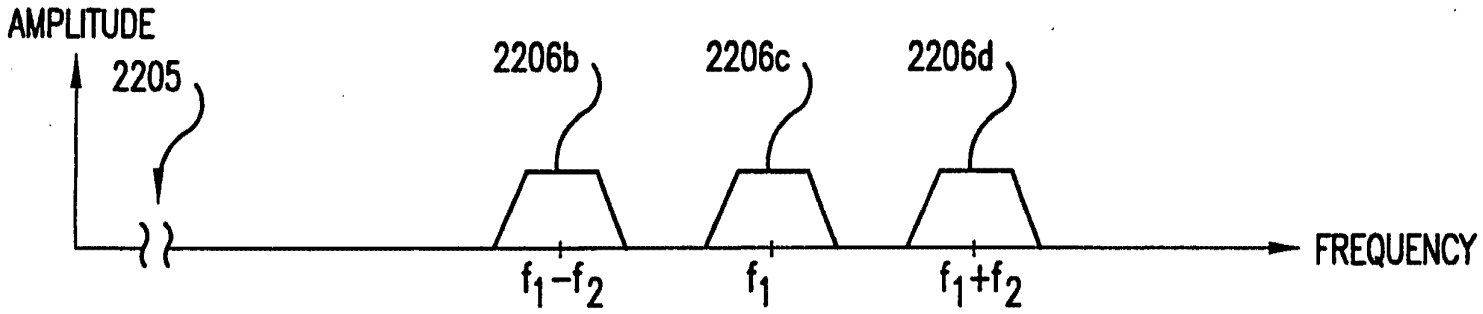


FIG. 22C

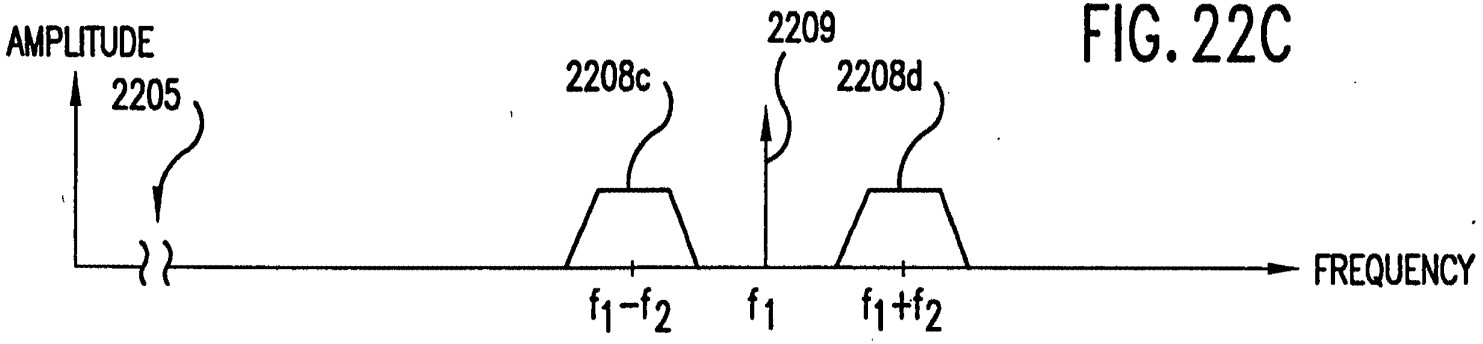


FIG. 22D

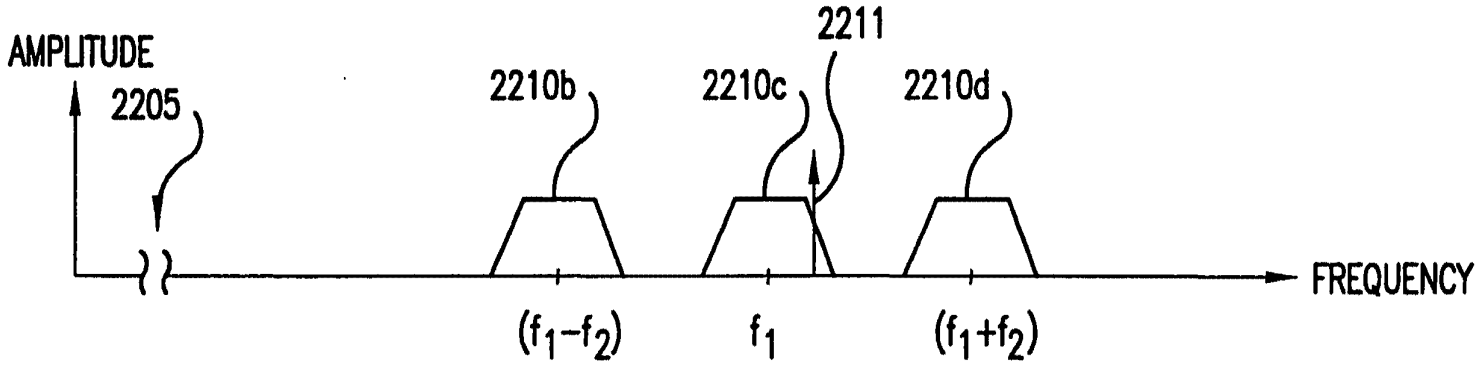


FIG. 22E

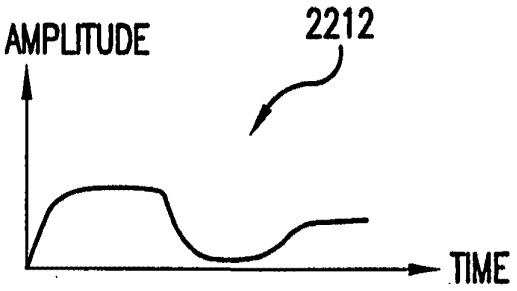


FIG. 22F

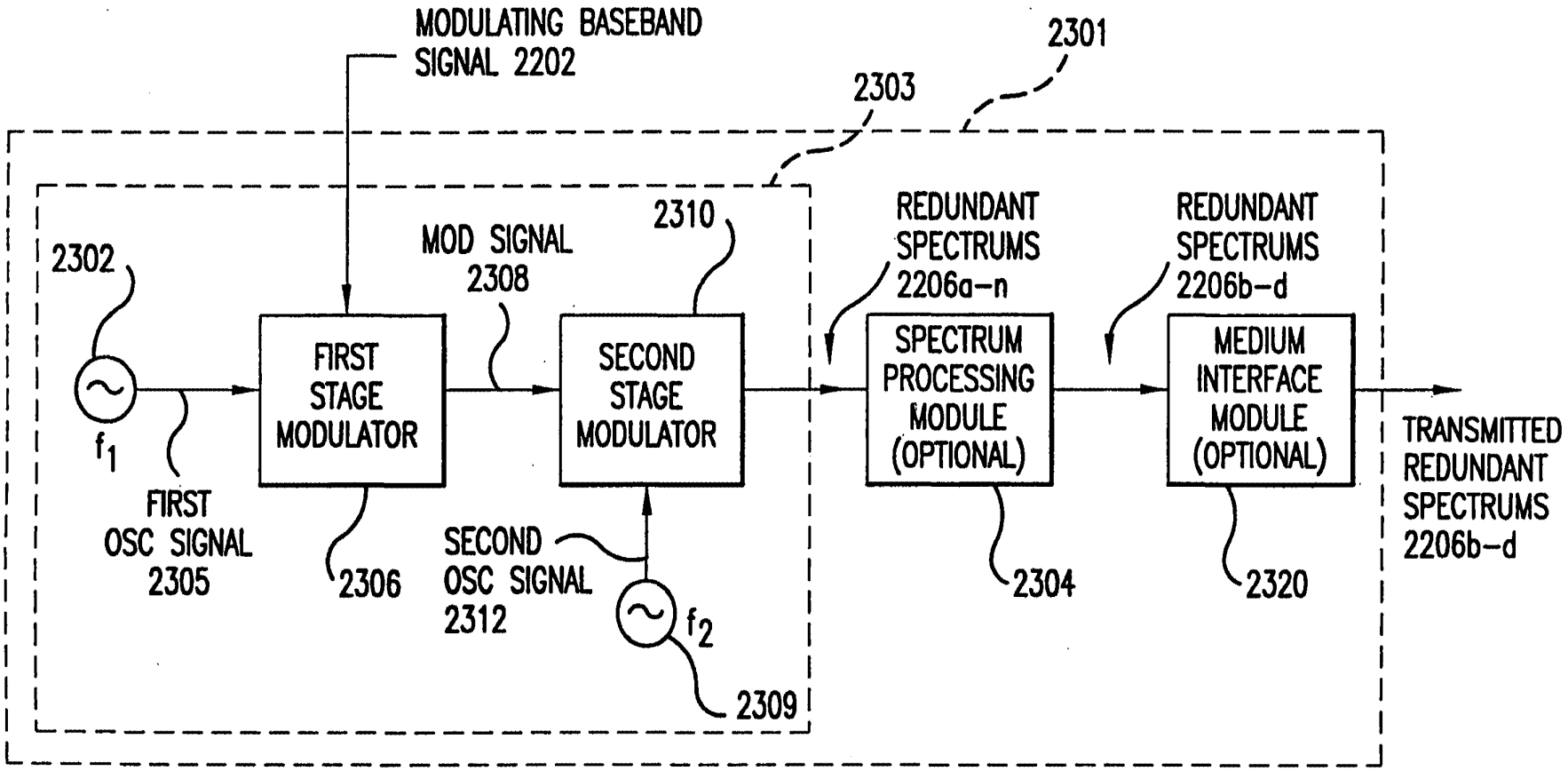

MODULATING BASEBAND SIGNAL 2202
2301
2303
2302
MOD SIGNAL 2308
2310
REDUNDANT SPECTRUMS 2206a–n
REDUNDANT SPECTRUMS 2206b–d
FIRST STAGE MODULATOR
SECOND STAGE MODULATOR
SPECTRUM PROCESSING MODULE (OPTIONAL)
MEDIUM INTERFACE MODULE (OPTIONAL)
TRANSMITTED REDUNDANT SPECTRUMS 2206b–d
f_1
FIRST OSC SIGNAL 2305
2306
SECOND OSC SIGNAL 2312
f_2
2309
2304
2320

FIG. 23A

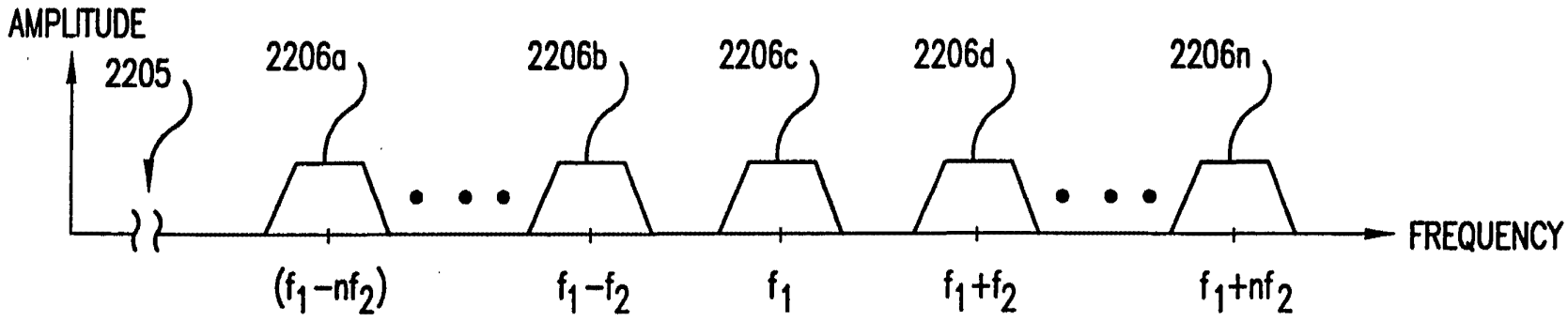


FIG. 23B

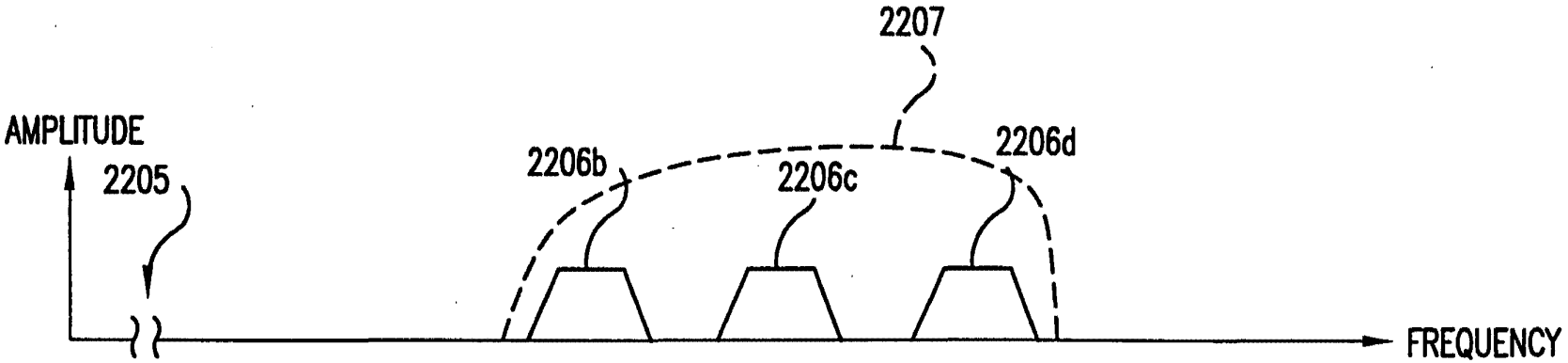


FIG. 23C

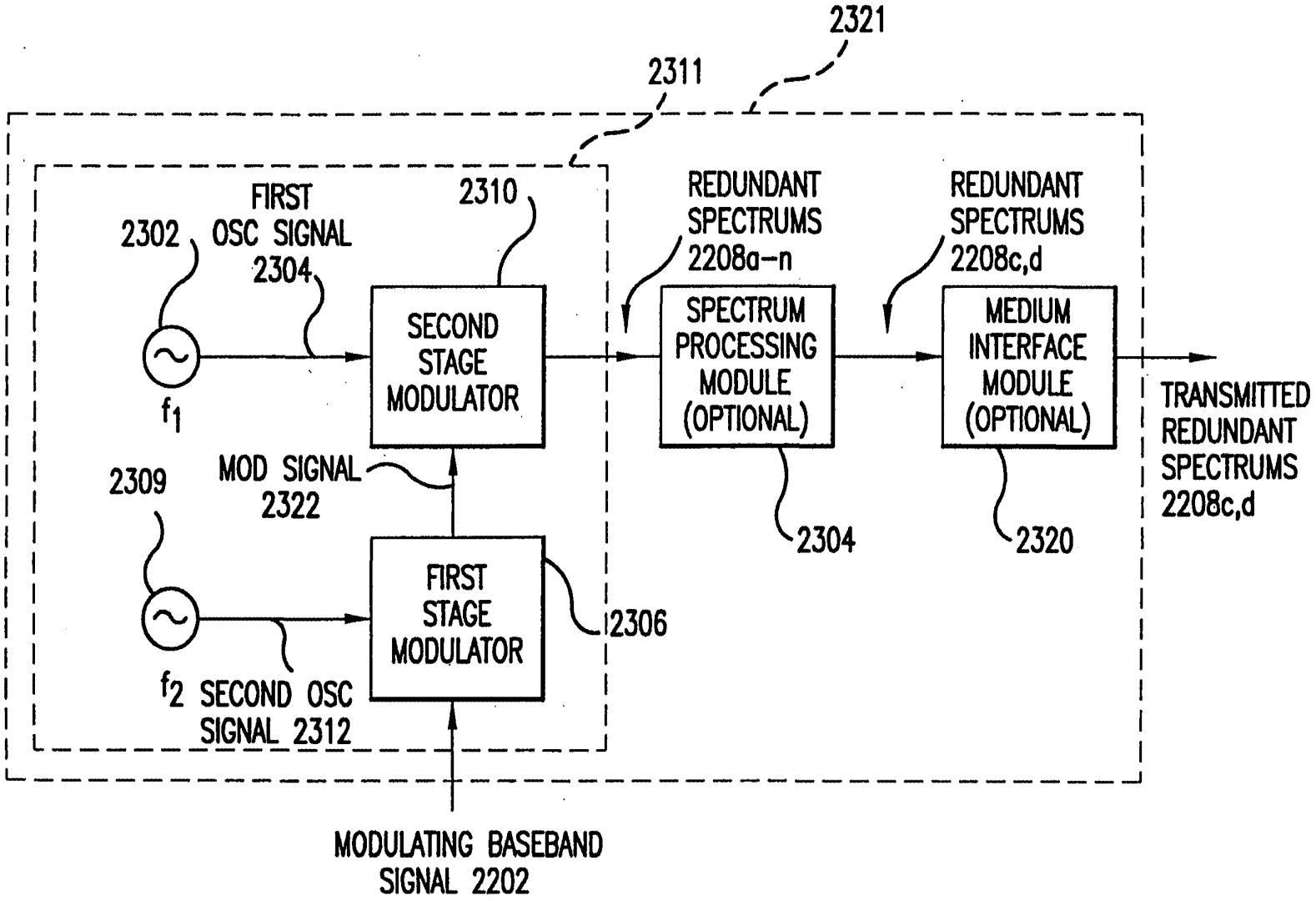

2321
2311
FIRST
OSC SIGNAL
2304
2302
2310
REDUNDANT
SPECTRUMS
2208a–n
REDUNDANT
SPECTRUMS
2208c,d
SECOND
STAGE
MODULATOR
SPECTRUM
PROCESSING
MODULE
(OPTIONAL)
MEDIUM
INTERFACE
MODULE
(OPTIONAL)
TRANSMITTED
REDUNDANT
SPECTRUMS
2208c,d
f1
MOD SIGNAL
2322
2309
2304
2320
FIRST
STAGE
MODULATOR
2306
f2 SECOND OSC
SIGNAL 2312
MODULATING BASEBAND
SIGNAL 2202

FIG. 23D

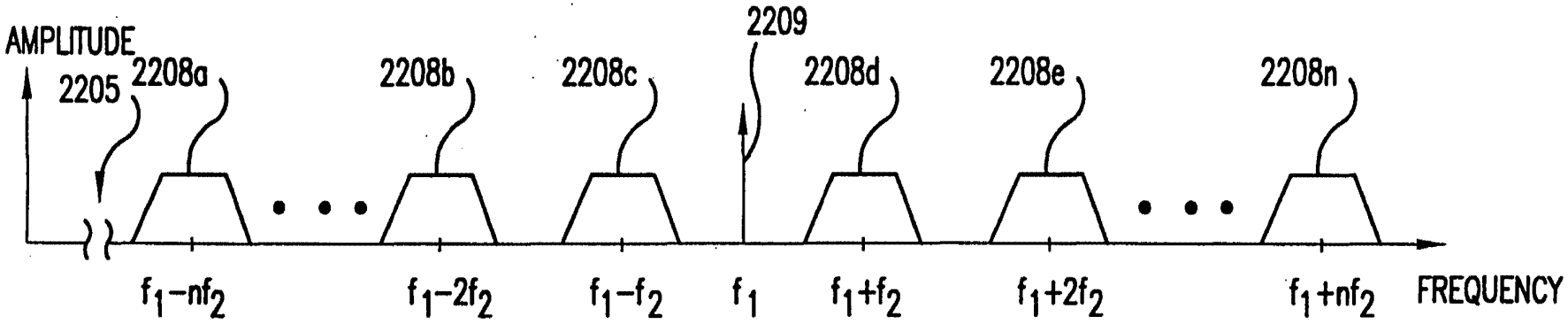


FIG. 23E

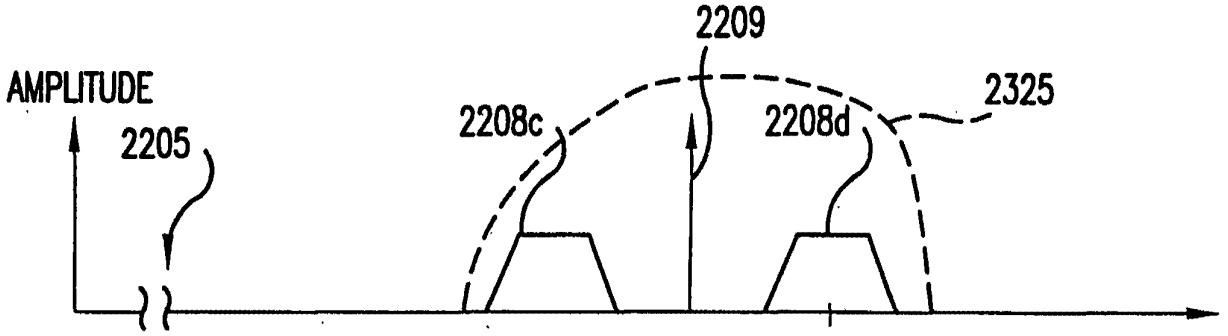


FIG. 23F

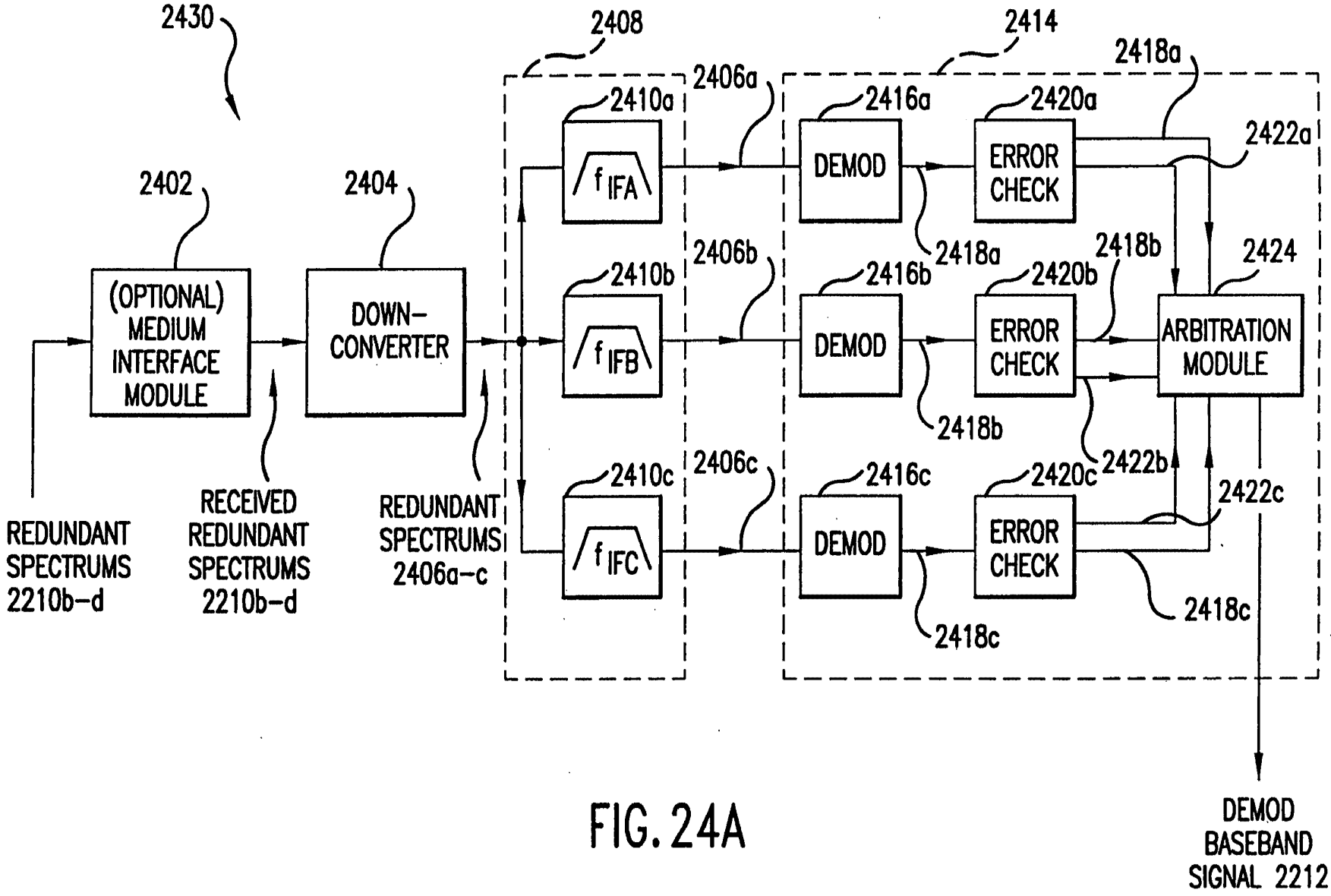

2430
2408
2414
2418a
2406a
2410a
2416a
2420a
2422a
2402
2404
DEMOD
ERROR CHECK
f IFA
2418a
2406b
2418b
2424
2410b
2416b
2420b
(OPTIONAL) MEDIUM INTERFACE MODULE
DOWN-CONVERTER
DEMOD
ERROR CHECK
ARBITRATION MODULE
f IFB
2418b
2422b
2406c
2410c
2416c
2420c
2422c
DEMOD
ERROR CHECK
f IFC
2418c
2418c
REDUNDANT SPECTRUMS 2210b-d
RECEIVED REDUNDANT SPECTRUMS 2210b-d
REDUNDANT SPECTRUMS 2406a-c
DEMOD BASEBAND SIGNAL 2212

FIG. 24A

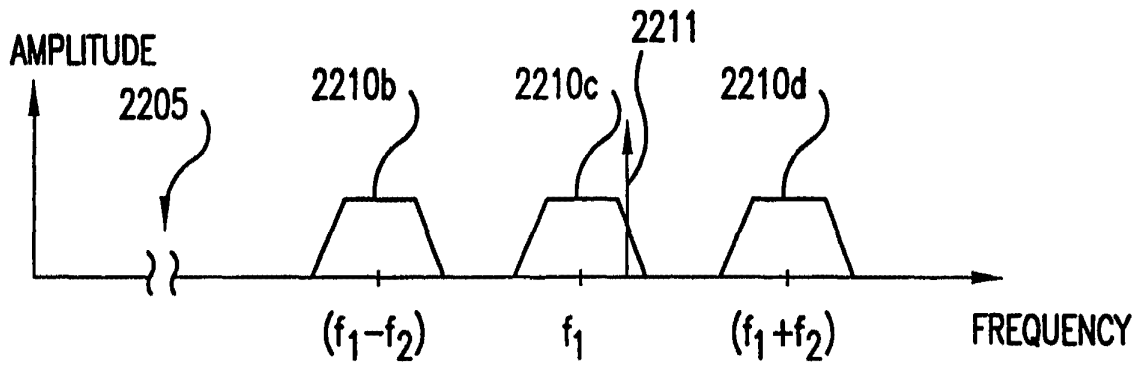


FIG. 24B

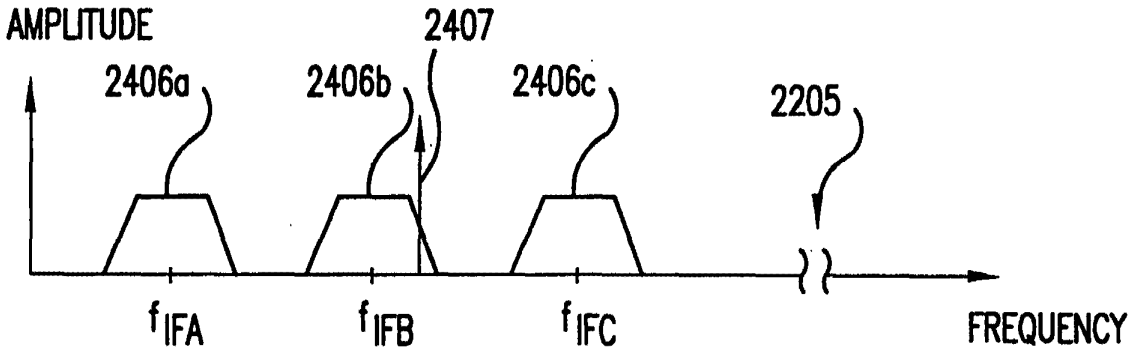


FIG. 24C

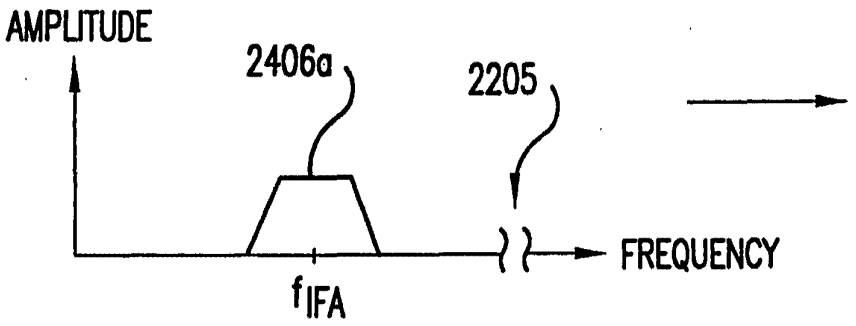


FIG. 24D

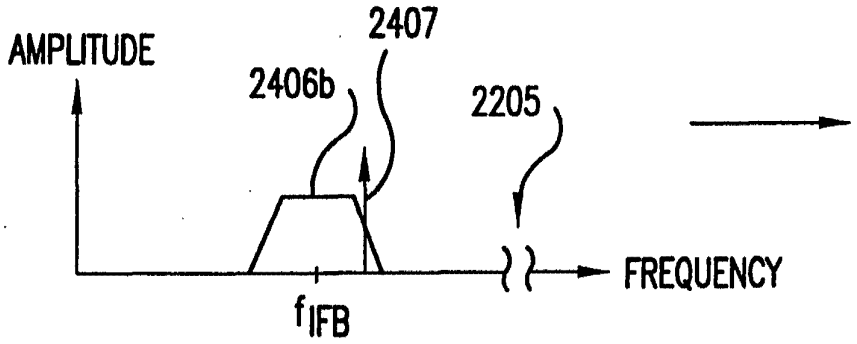


FIG. 24E

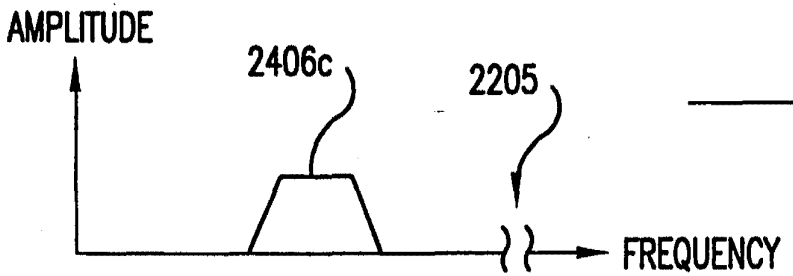


FIG. 24F

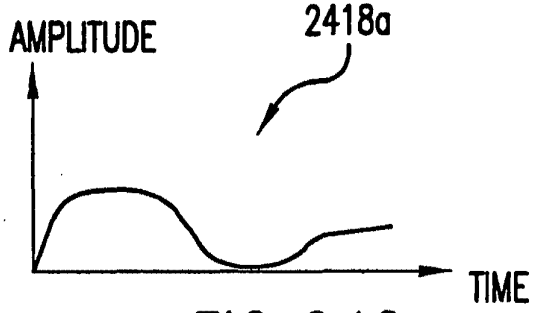


FIG. 24G

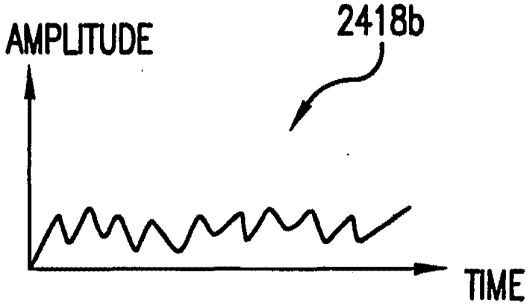


FIG. 24H

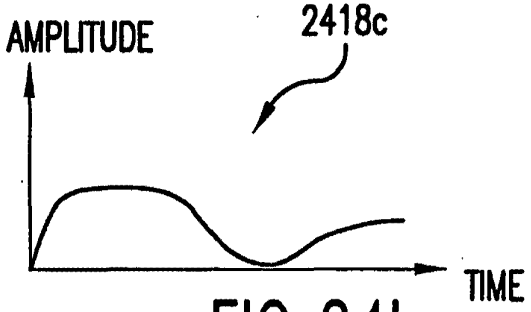


FIG. 24I

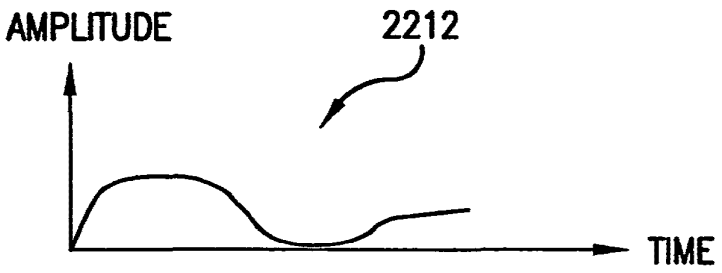


FIG. 24J

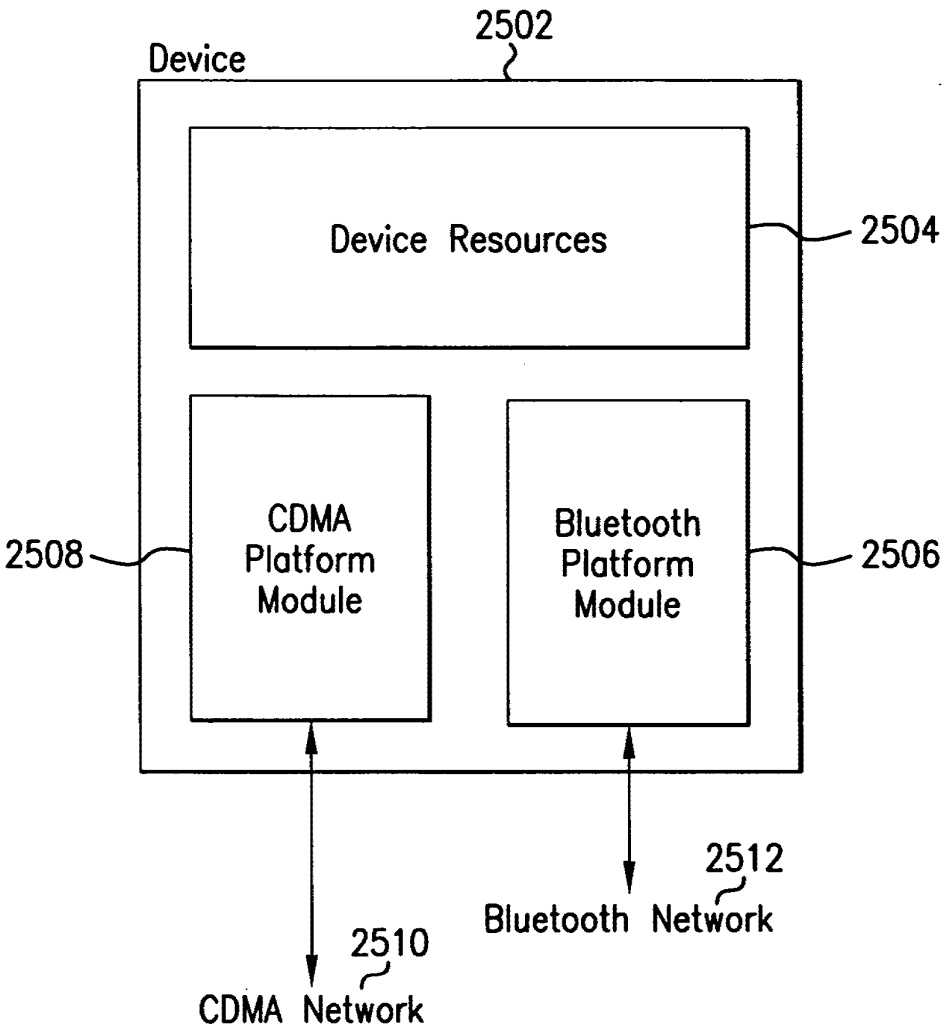

2500
2502
Device
Device Resources
2504
CDMA
Platform
Module
2508
Bluetooth
Platform
Module
2506
2512
Bluetooth Network
2510
CDMA Network

FIG.25A

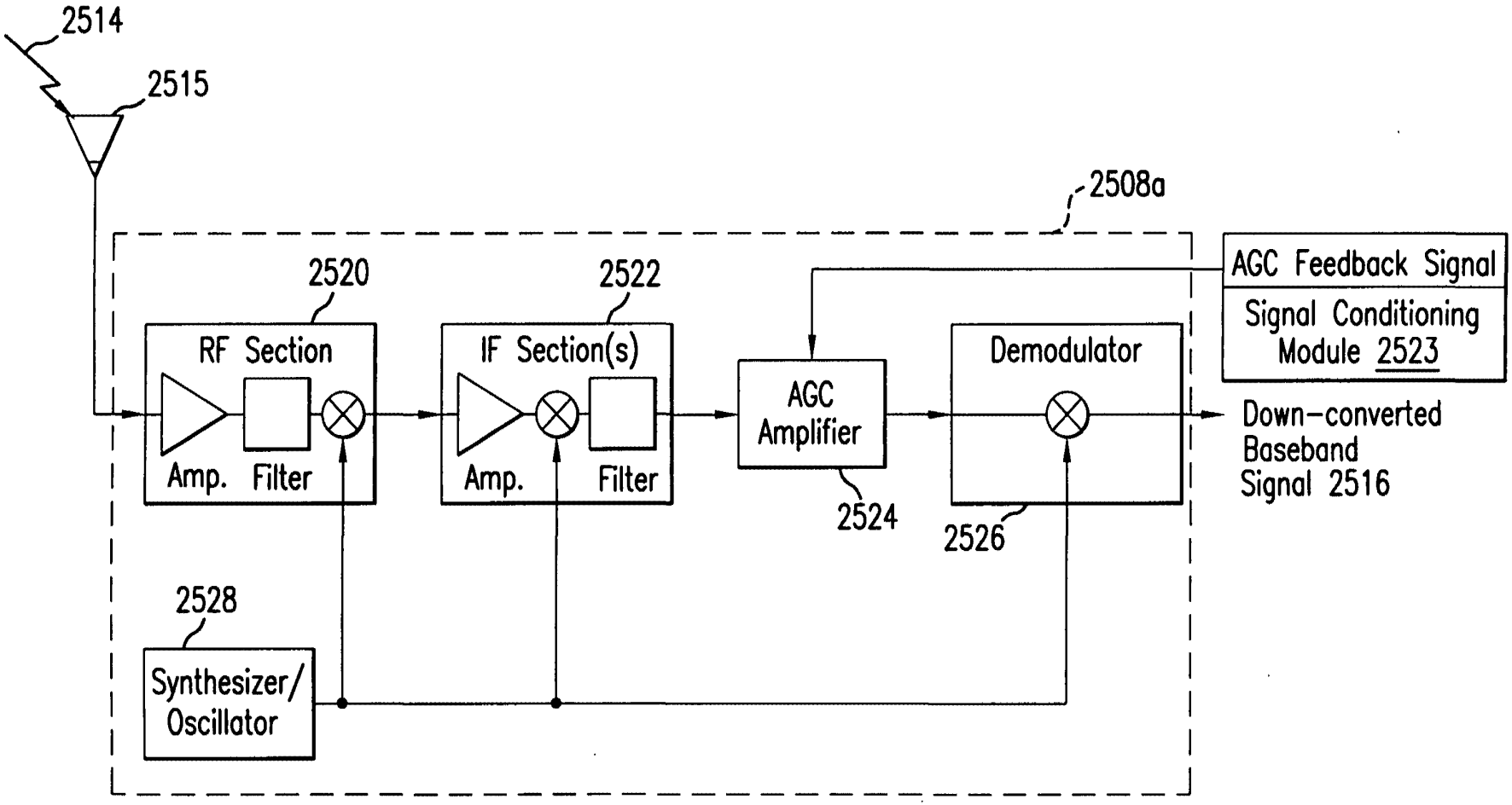

2514
2515
2508a
2520
2522
RF Section
IF Section(s)
Amp.
Filter
Amp.
Filter
AGC
Amplifier
2524
Demodulator
2526
AGC Feedback Signal
Signal Conditioning
Module 2523
Down-converted
Baseband
Signal 2516
2528
Synthesizer/
Oscillator

FIG.25B

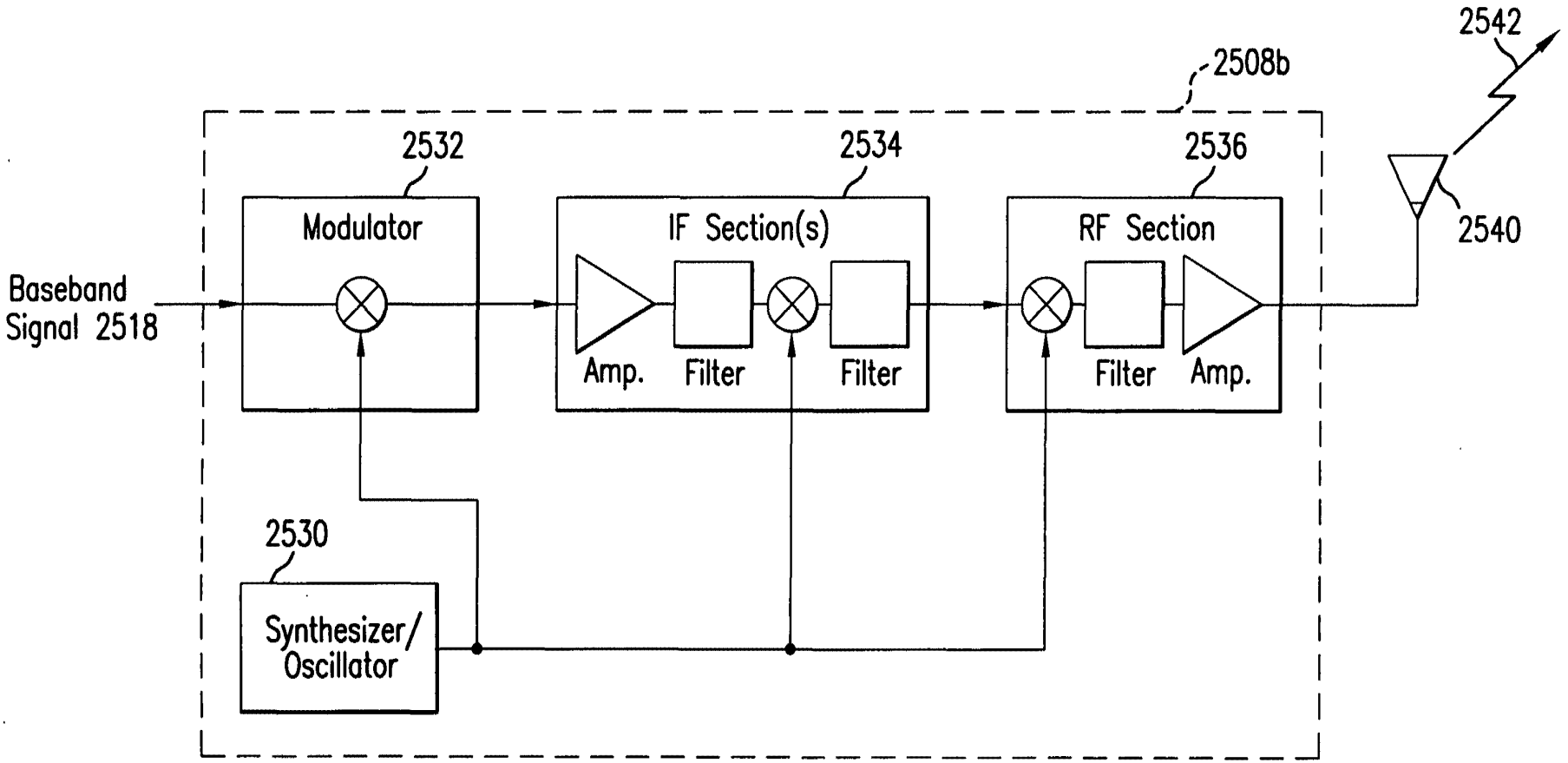

2542
2508b
2532
2534
2536
Modulator
IF Section(s)
RF Section
2540
Baseband
Signal 2518
Amp.
Filter
Filter
Filter
Amp.
2530
Synthesizer/
Oscillator

FIG.25C

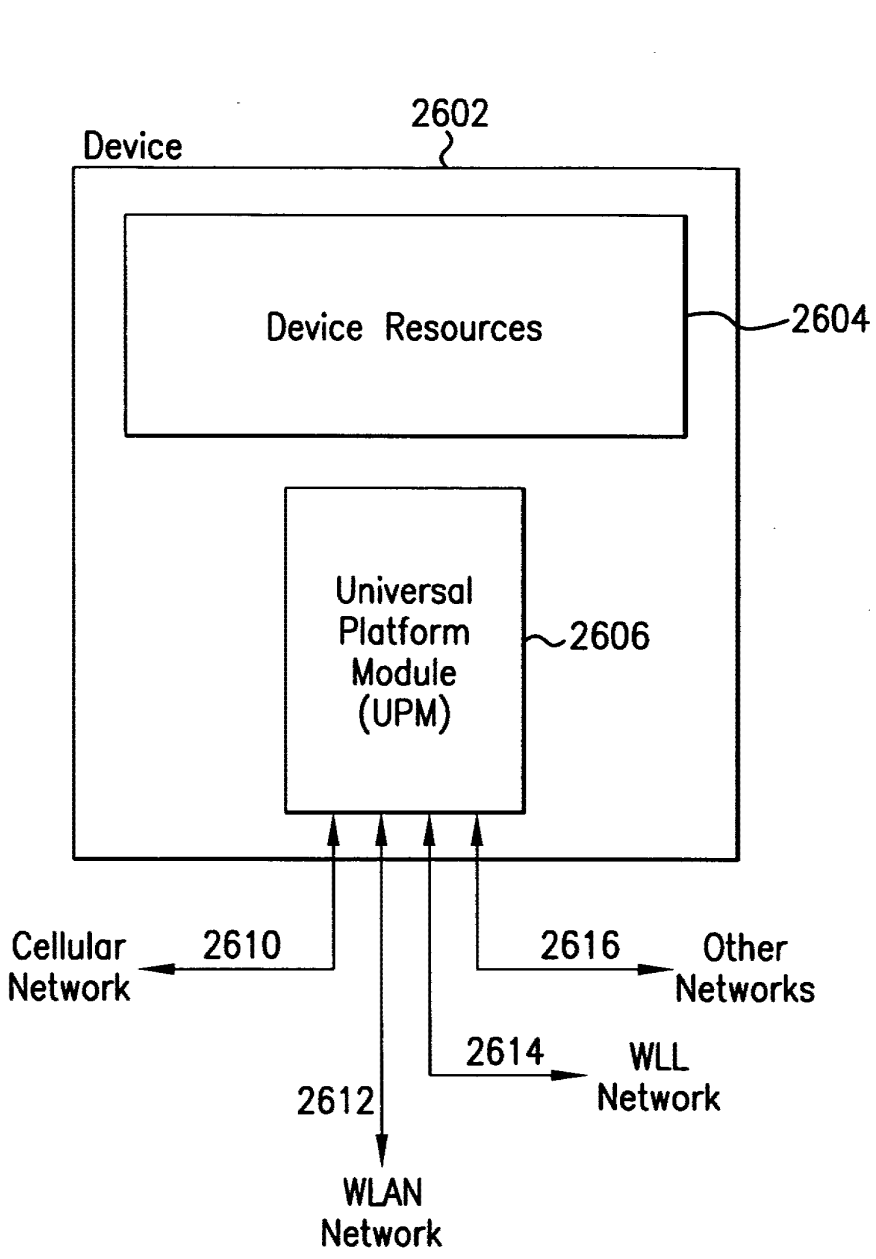

2600
2602
Device
Device Resources
2604
Universal Platform Module (UPM)
2606
Cellular Network
2610
2616
Other Networks
2614
WLL Network
2612
WLAN Network

FIG.26A

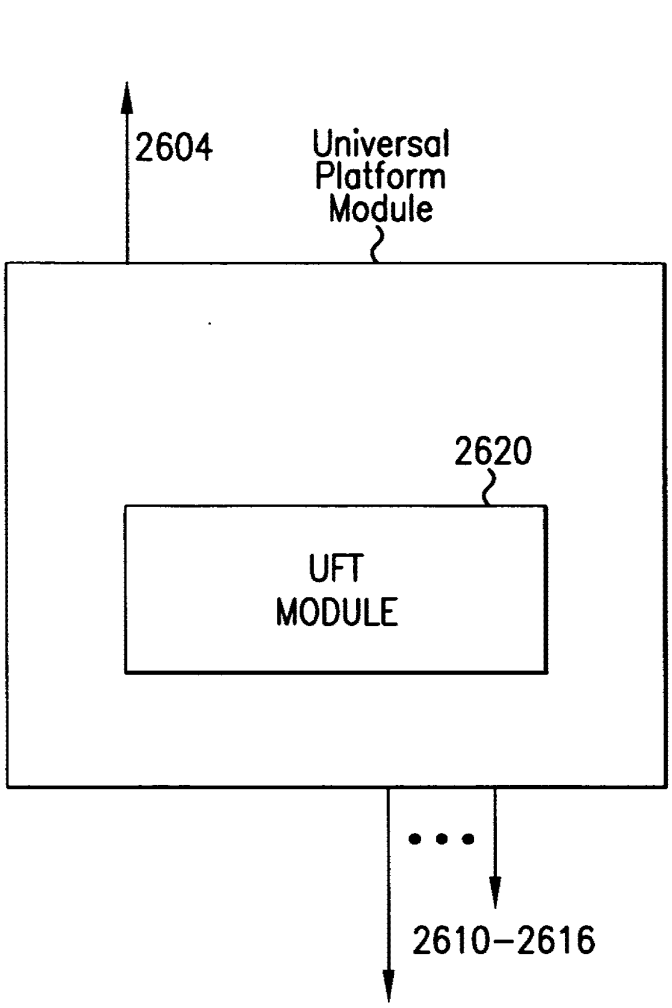

2606
2604
Universal
Platform
Module
2620
UFT
MODULE
2610–2616

FIG.26B

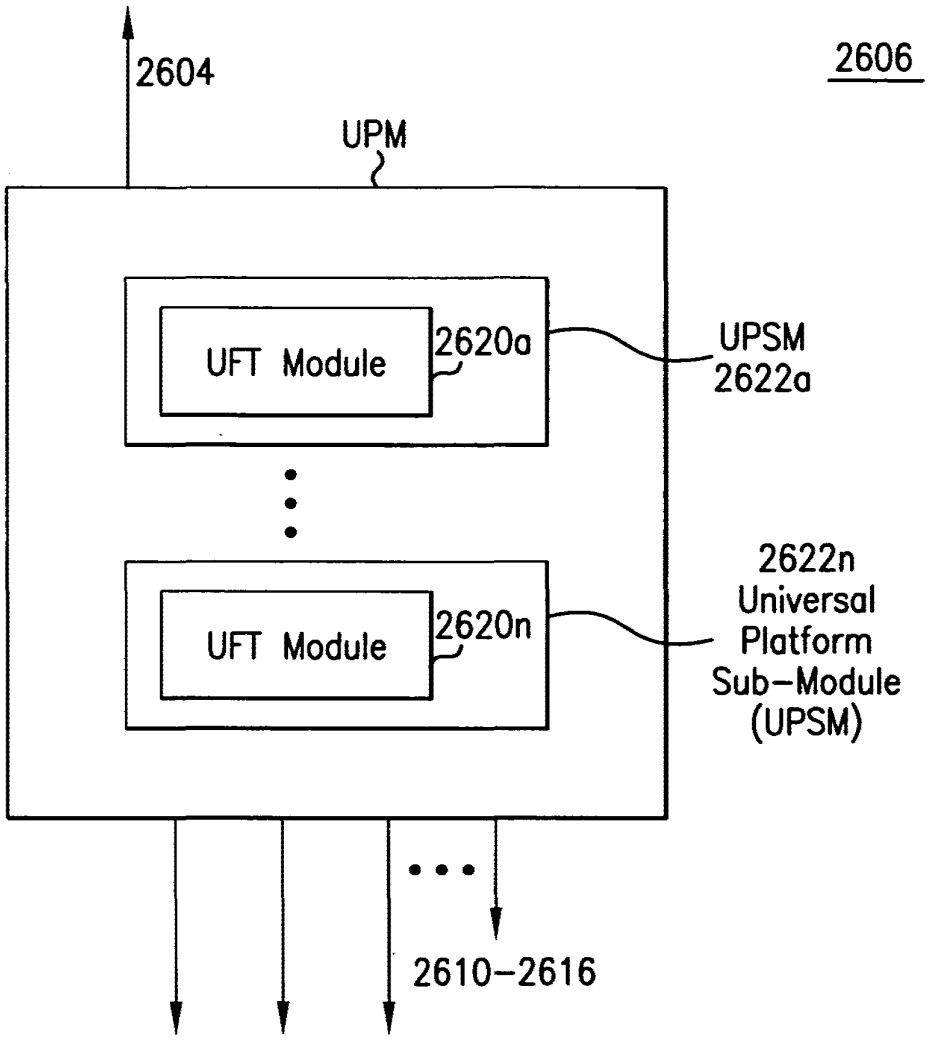

2604
2606
UPM
UFT Module
2620a
UPSM
2622a
UFT Module
2620n
2622n
Universal
Platform
Sub-Module
(UPSM)
2610-2616

FIG.26C

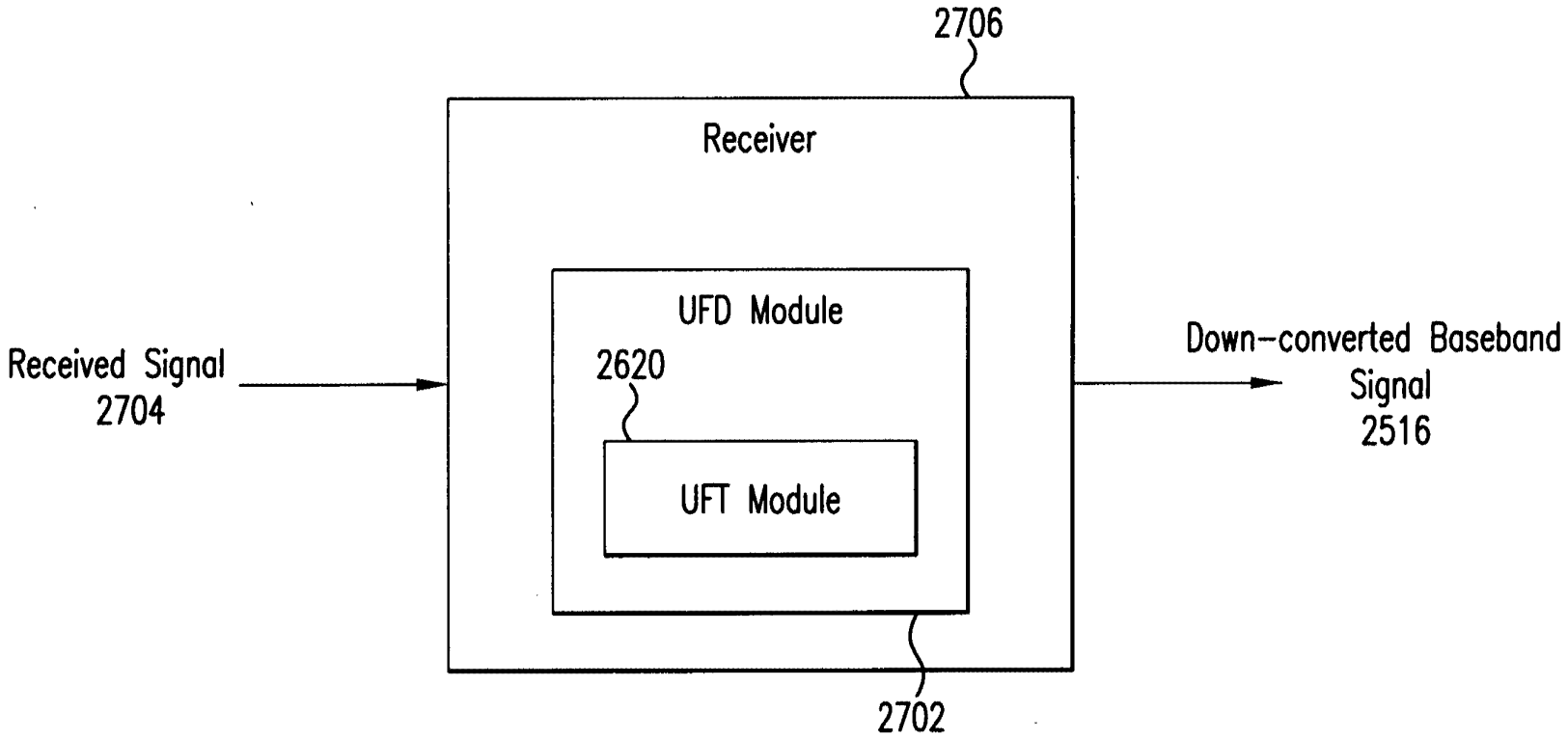

2706
Receiver
UFD Module
2620
UFT Module
Received Signal
2704
Down-converted Baseband
Signal
2516
2702

FIG.27A

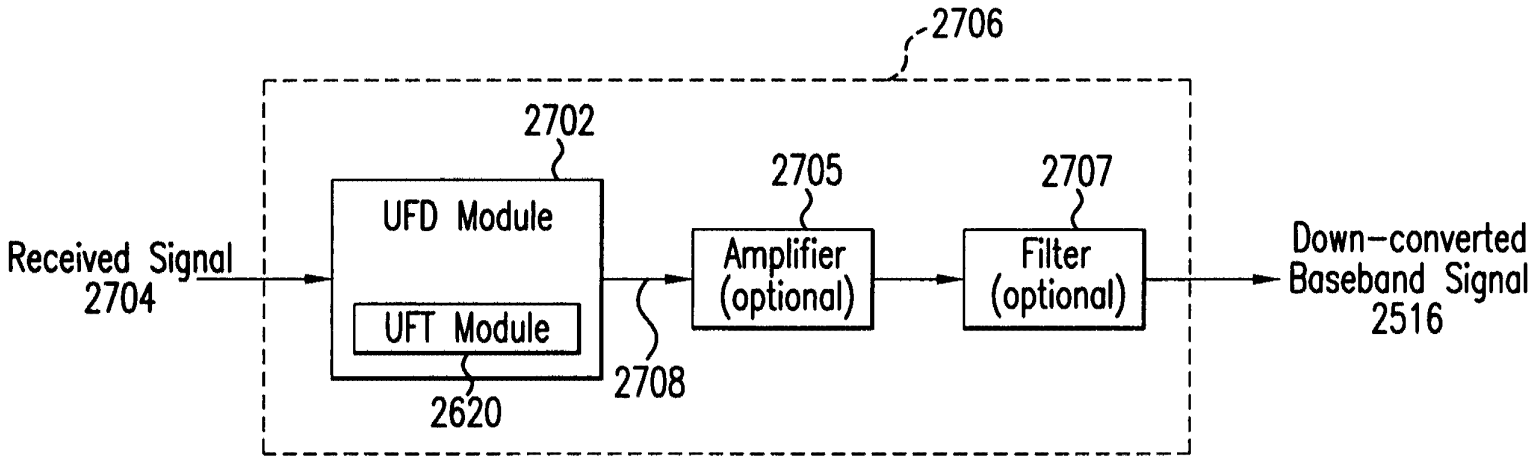


FIG.27B

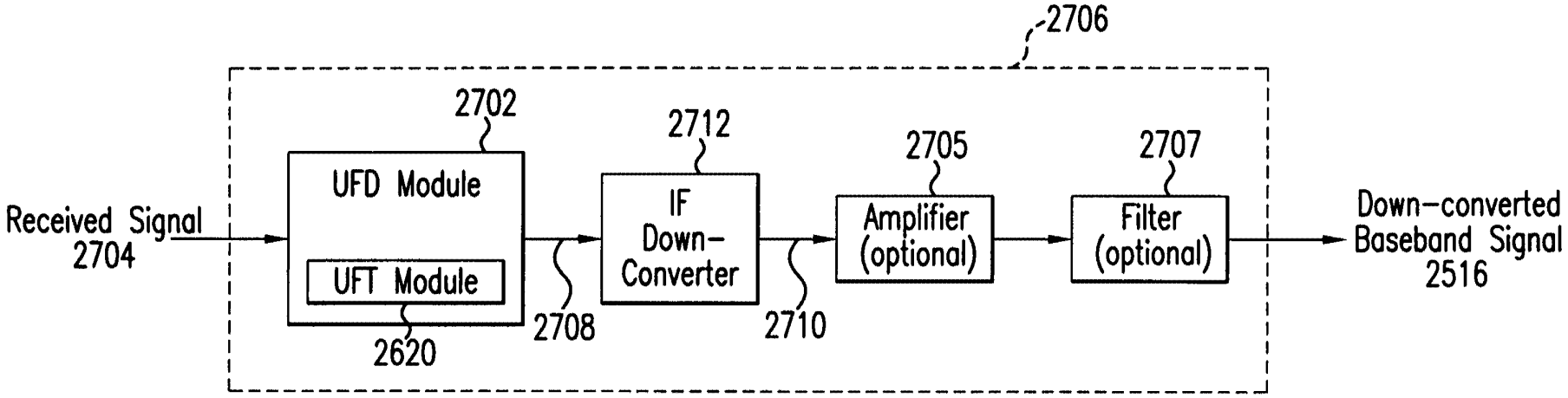


FIG.27C

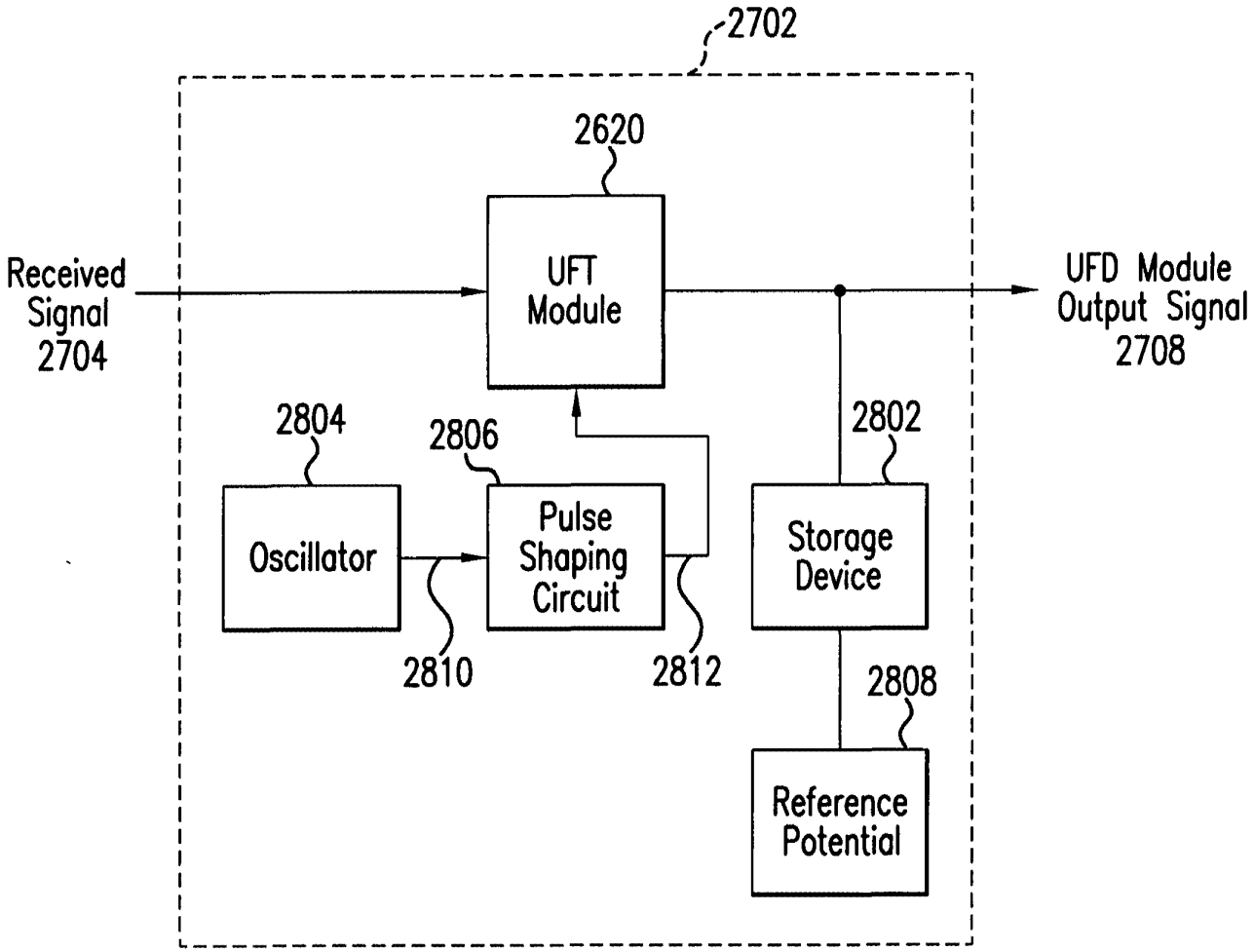

2702
2620
UFT Module
Received Signal 2704
UFD Module Output Signal 2708
2804
2806
2802
Oscillator
Pulse Shaping Circuit
Storage Device
2810
2812
2808
Reference Potential

FIG.28

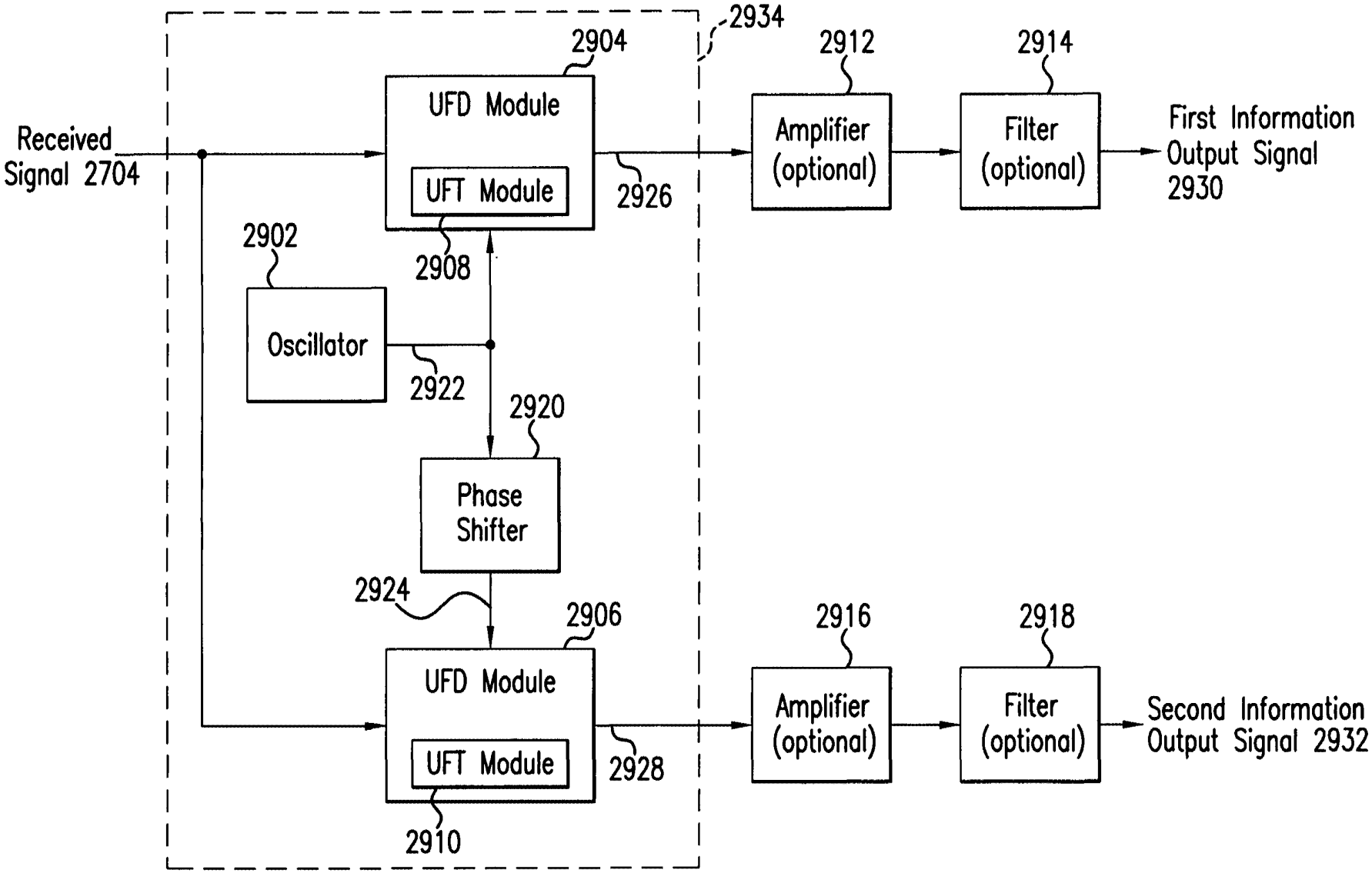

2934
2904
2912
2914
UFD Module
Amplifier (optional)
Filter (optional)
Received Signal 2704
First Information Output Signal 2930
UFT Module
2926
2902
2908
Oscillator
2922
2920
Phase Shifter
2924
2906
2916
2918
UFD Module
Amplifier (optional)
Filter (optional)
Second Information Output Signal 2932
UFT Module
2928
2910

FIG.29

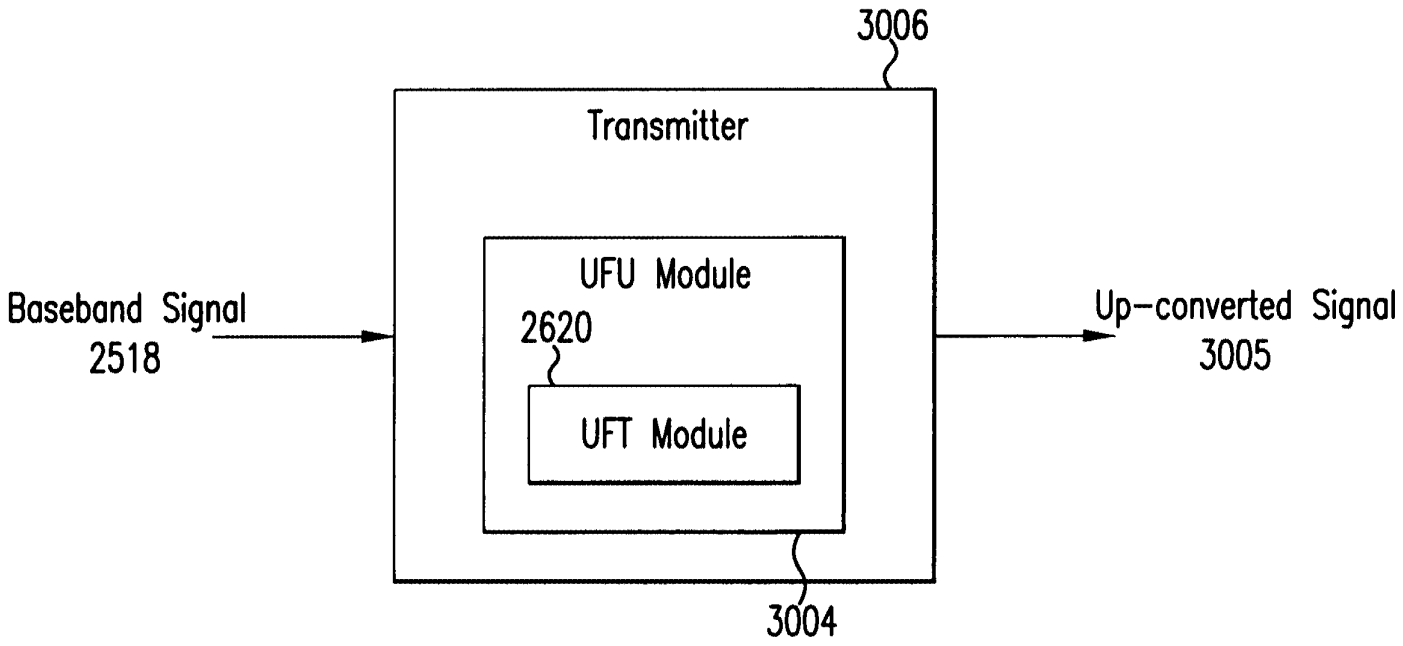

3006
Transmitter
UFU Module
2620
UFT Module
Baseband Signal
2518
Up-converted Signal
3005
3004

FIG.30A

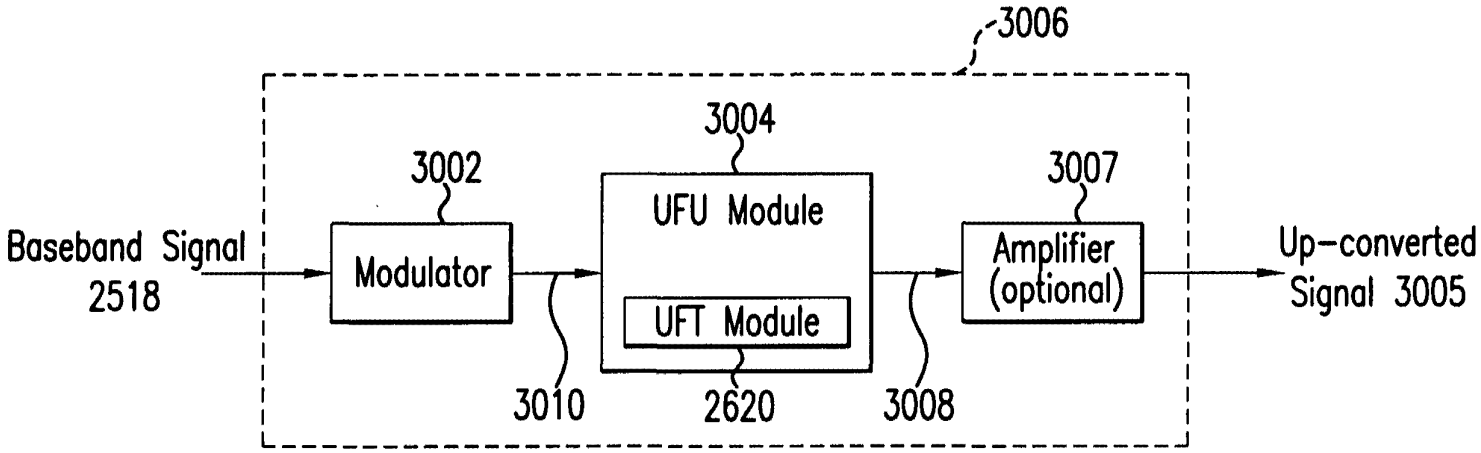


FIG.30B

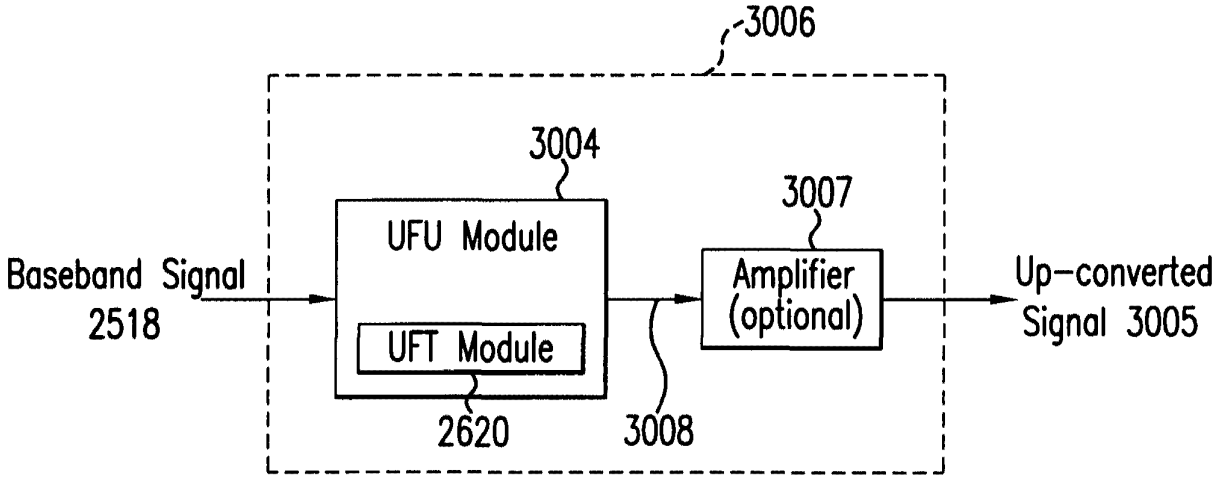


FIG.30C

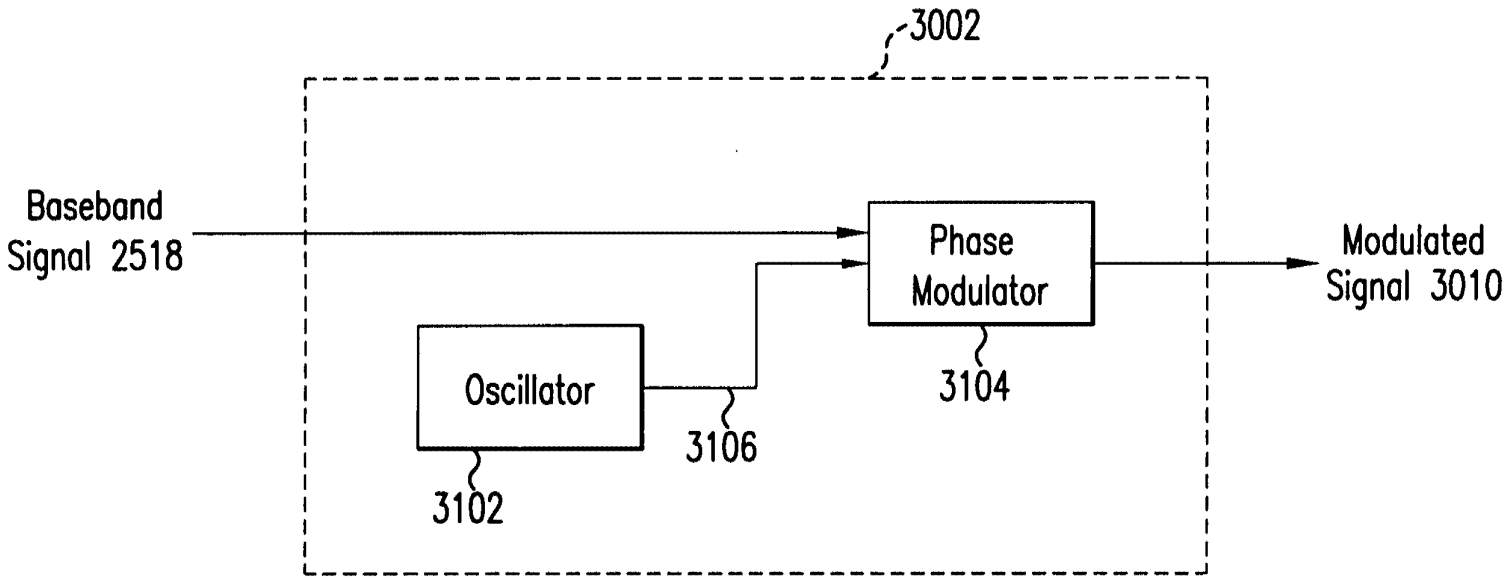

3002
Baseband
Signal 2518
Phase
Modulator
Modulated
Signal 3010
Oscillator
3104
3106
3102

FIG.31

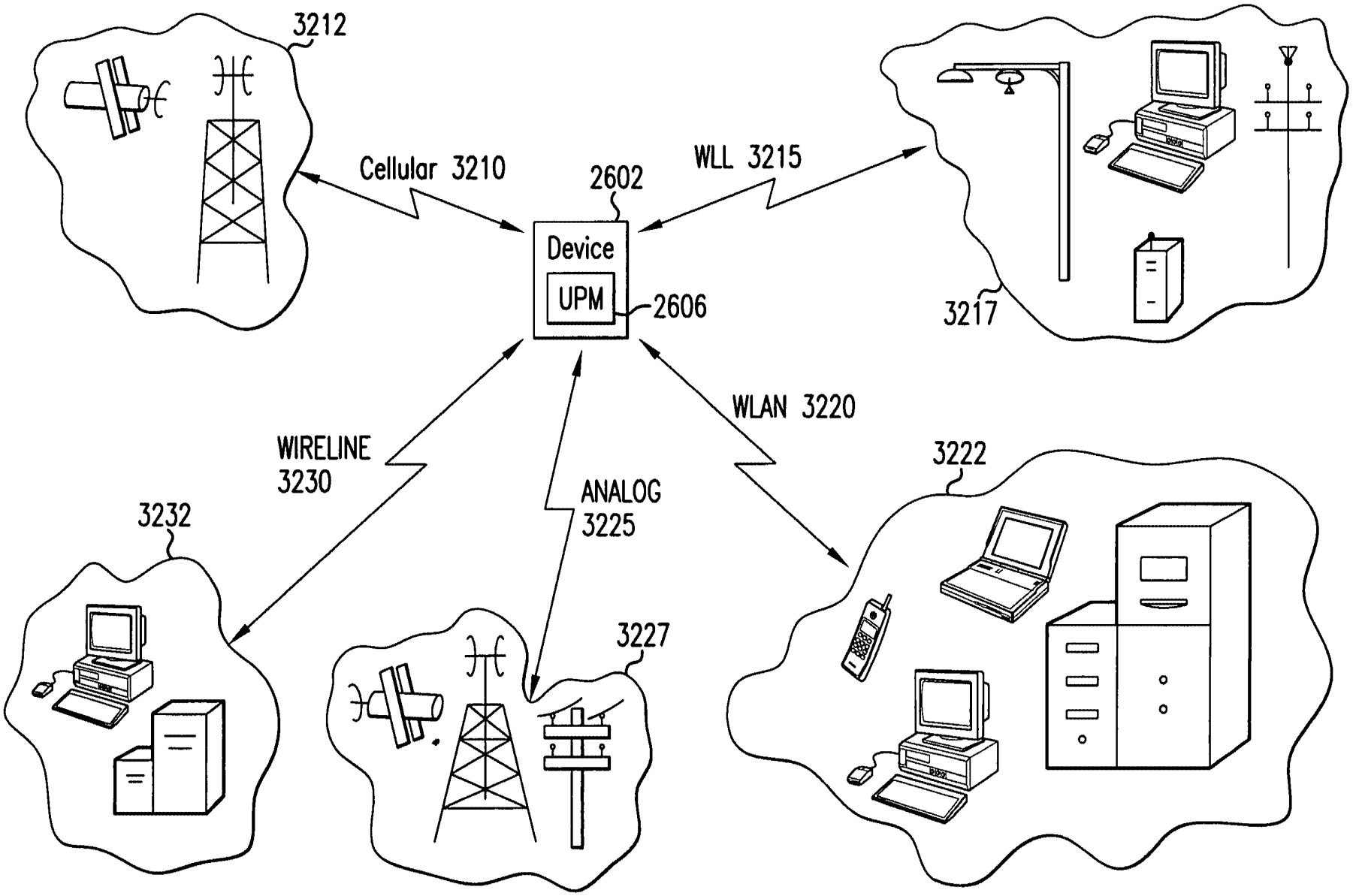

3212
Cellular 3210
2602
Device
UPM
2606
WLL 3215
3217
WIRELINE
3230
ANALOG
3225
WLAN 3220
3222
3232
3227

FIG.32

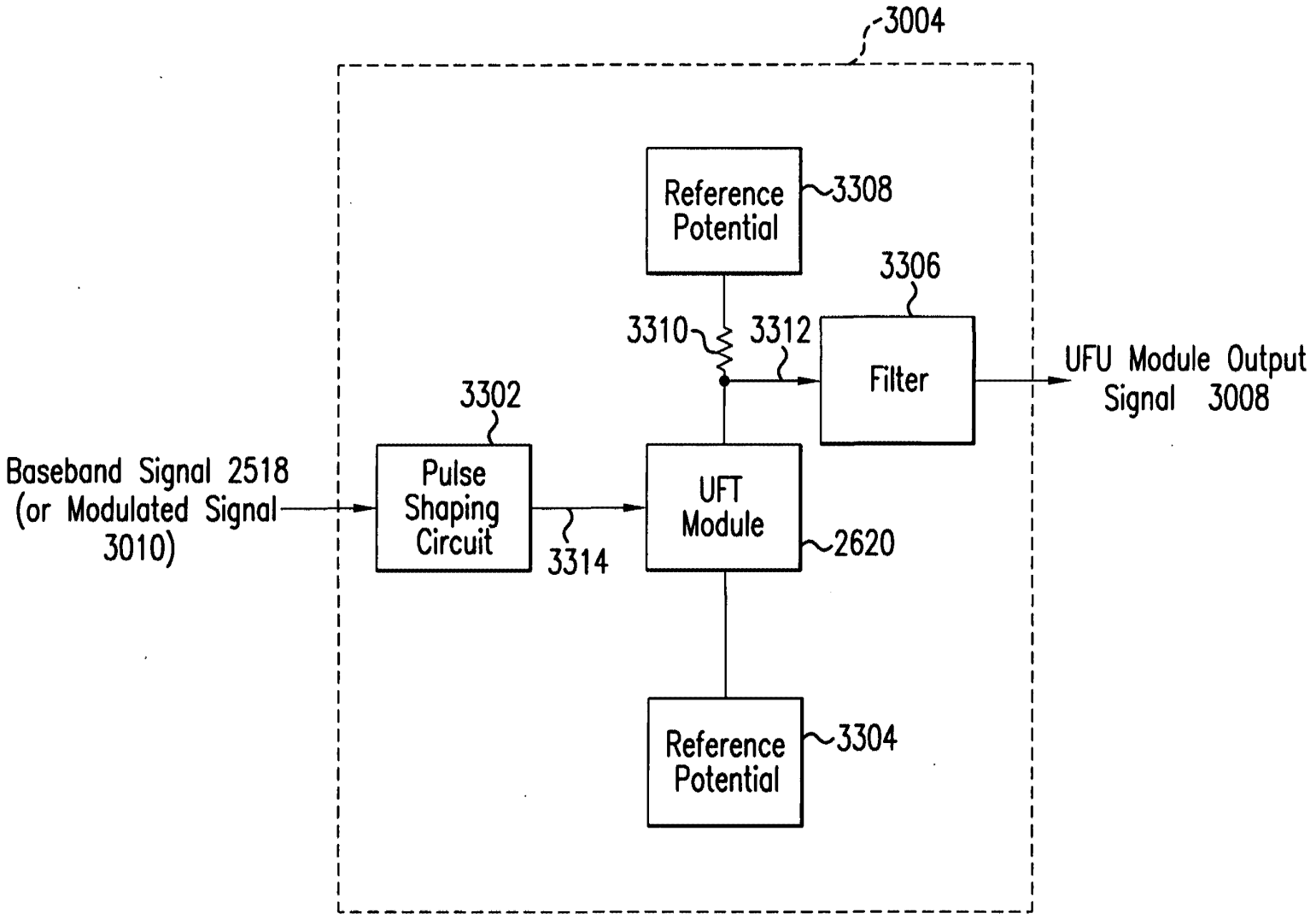

3004
Reference Potential
3308
3306
3310
3312
Filter
UFU Module Output Signal 3008
3302
Baseband Signal 2518 (or Modulated Signal 3010)
Pulse Shaping Circuit
3314
UFT Module
2620
Reference Potential
3304

FIG.33

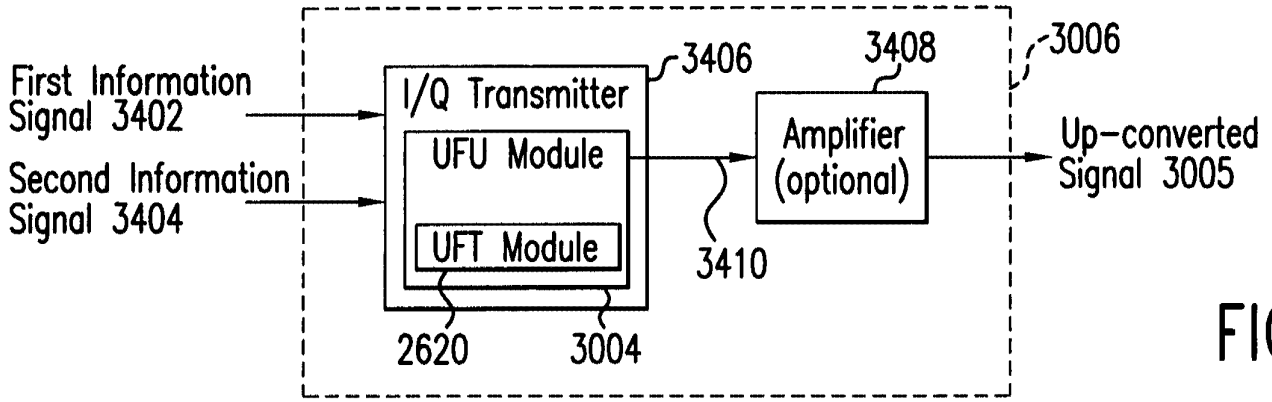

First Information Signal 3402
Second Information Signal 3404
I/Q Transmitter
UFU Module
UFT Module
3406
3408
3006
Amplifier (optional)
Up-converted Signal 3005
3410
2620
3004

FIG.34

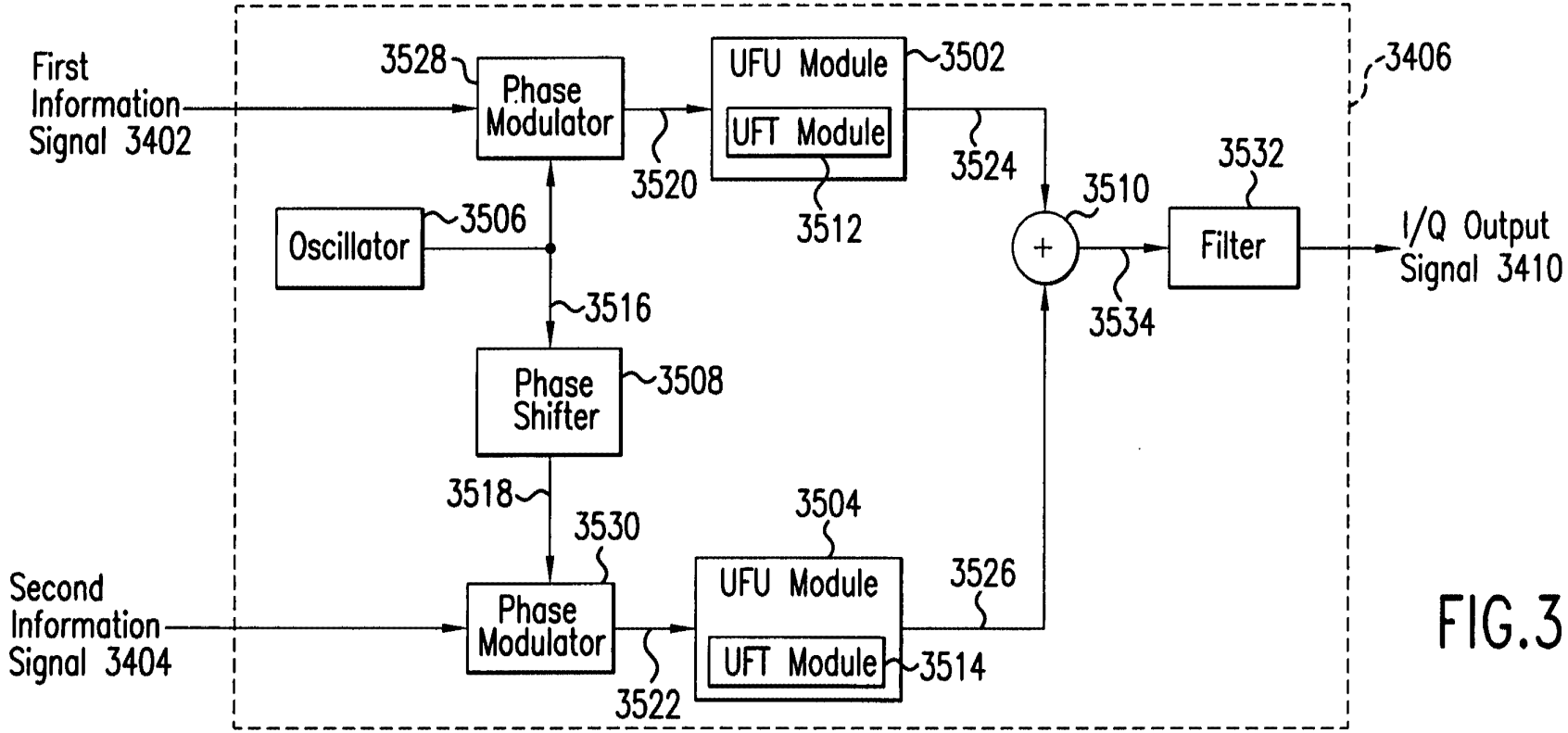

First Information Signal 3402
3528
Phase Modulator
UFU Module
UFT Module
3502
3406
3520
3512
3524
3532
3510
Oscillator
3506
Filter
I/Q Output Signal 3410
3534
3516
Phase Shifter
3508
3518
3530
3504
Second Information Signal 3404
Phase Modulator
UFU Module
UFT Module
3526
3514
3522

FIG.35

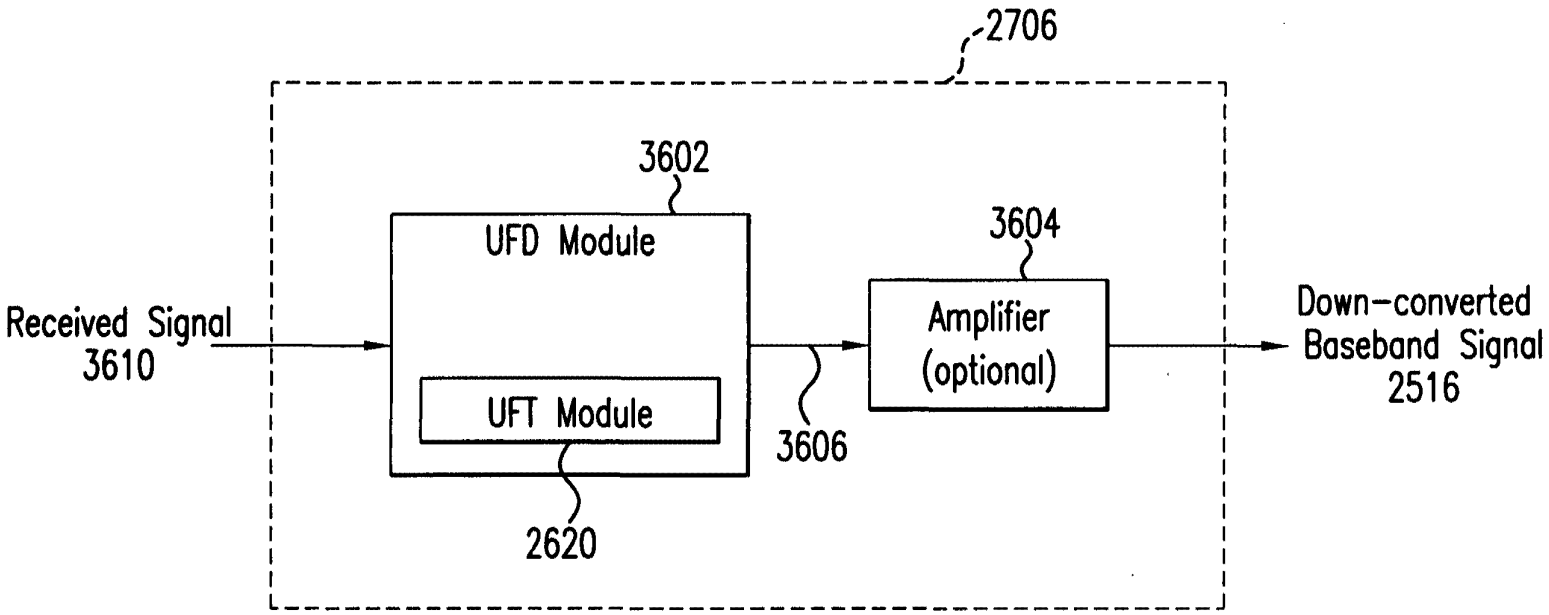

2706
3602
UFD Module
3604
Amplifier
(optional)
Received Signal
3610
UFT Module
3606
Down-converted
Baseband Signal
2516
2620

FIG.36

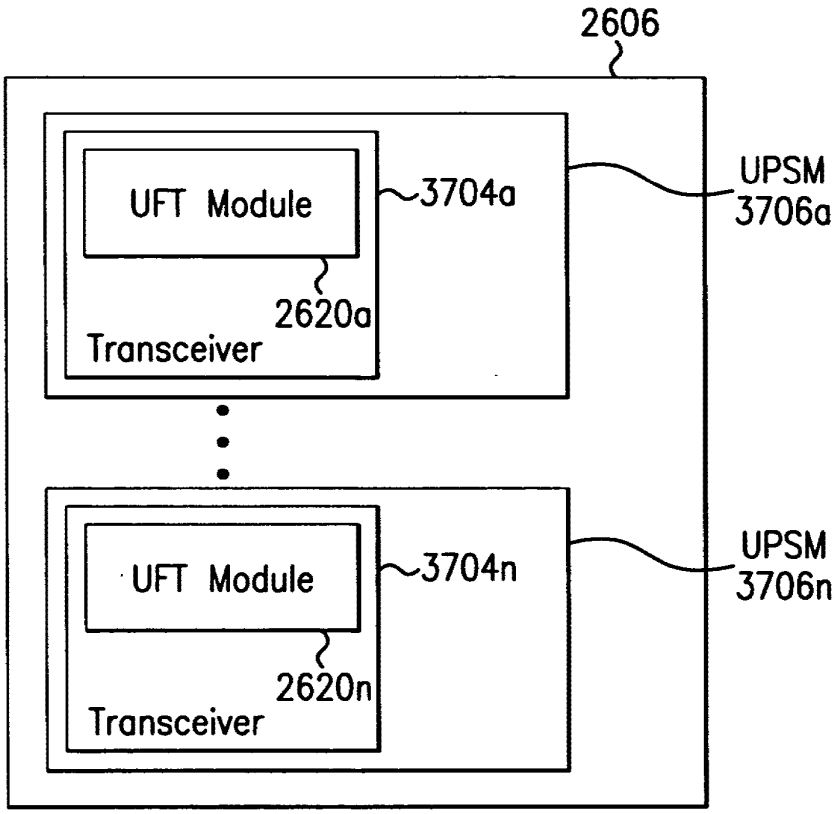

2606
UFT Module
3704a
2620a
Transceiver
UPSM
3706a
UFT Module
3704n
2620n
Transceiver
UPSM
3706n

FIG.37

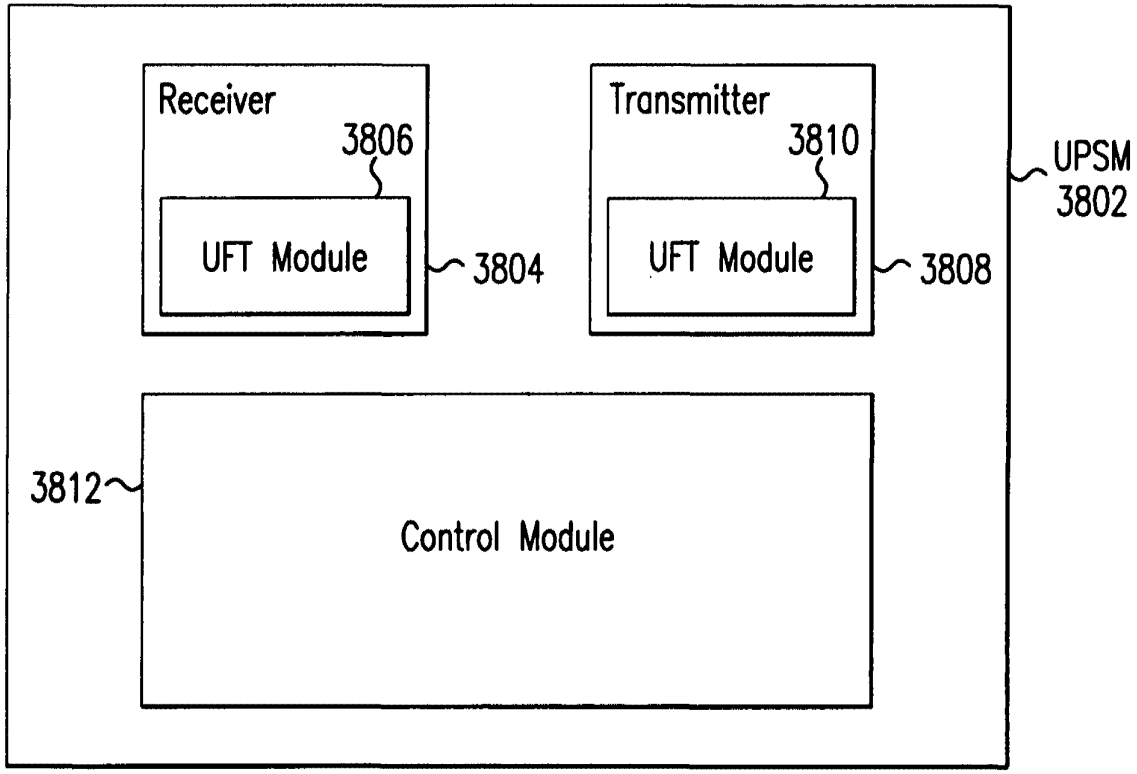

Receiver
3806
UFT Module
3804
Transmitter
3810
UFT Module
3808
UPSM
3802
3812
Control Module

FIG.38

3900

Protocol / Bearer	Bluetooth	WAP	802.11	AT Command	• • •	• • •	• • •
Bluetooth	X			X			
GSM		X					
CDMA		X					
TDMA		X					
802.11			X				
PHS		X					
CDPD		X					
PDC-P		X					
iDEN		X					
FLEX		X					
AMPS		X		X			
⋮							

FIG.39

4000

Longer-Range	Short-Range	
Wireless Local Loop (WLL) – Project Angel – LMDS – MMDS – ARDIS • • •	**Wireless LAN (WLAN)** – Bluetooth – Infrared – Home RF – 802.11 • • •	Fixed
Cellular – GSM – SMS – CDMA • • •		Mobile

FIG.40

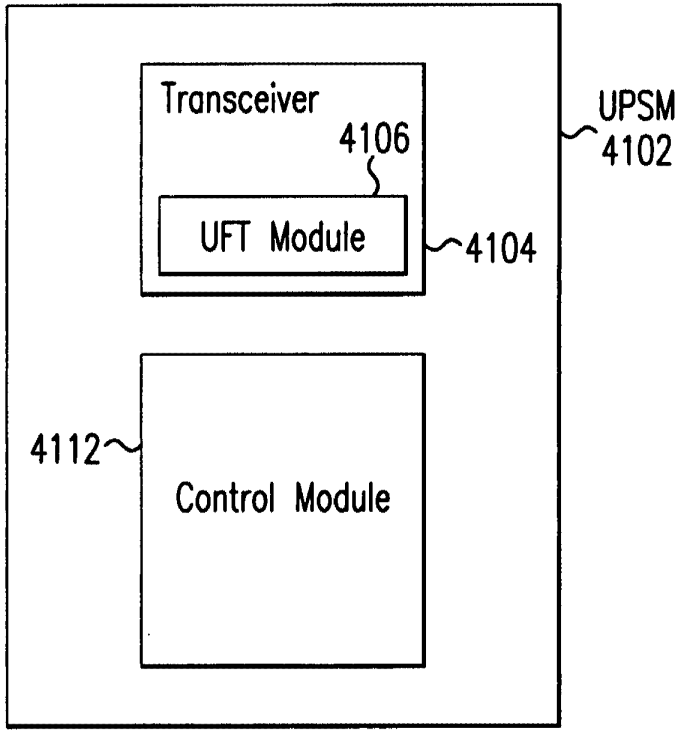

Transceiver
4106
UFT Module
4104
UPSM
4102
4112
Control Module

FIG.41

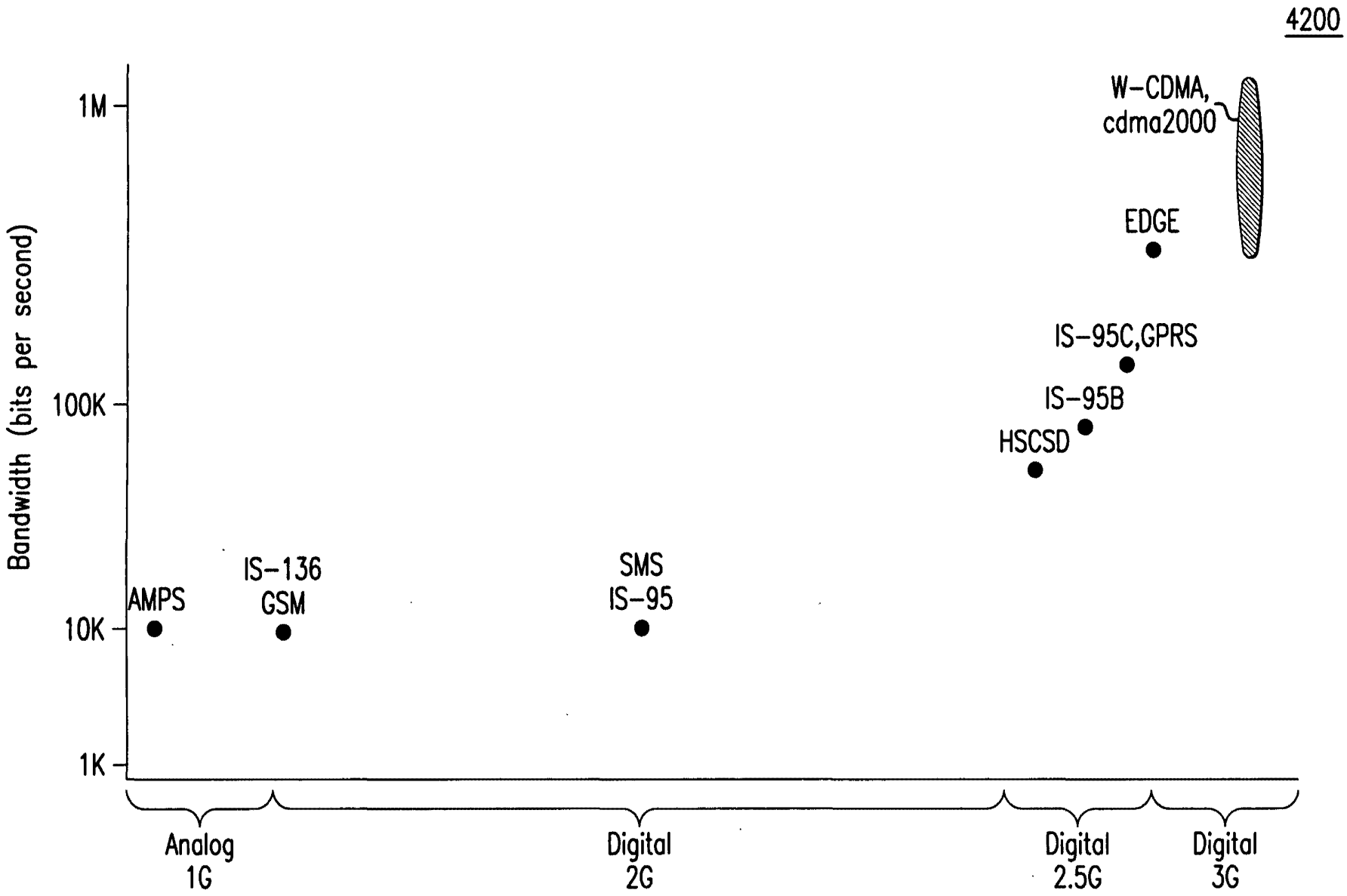

4200
1M
100K
10K
1K
Bandwidth (bits per second)
W-CDMA,
cdma2000
EDGE
IS-95C,GPRS
IS-95B
HSCSD
AMPS
IS-136
GSM
SMS
IS-95
Analog
1G
Digital
2G
Digital
2.5G
Digital
3G

FIG.42

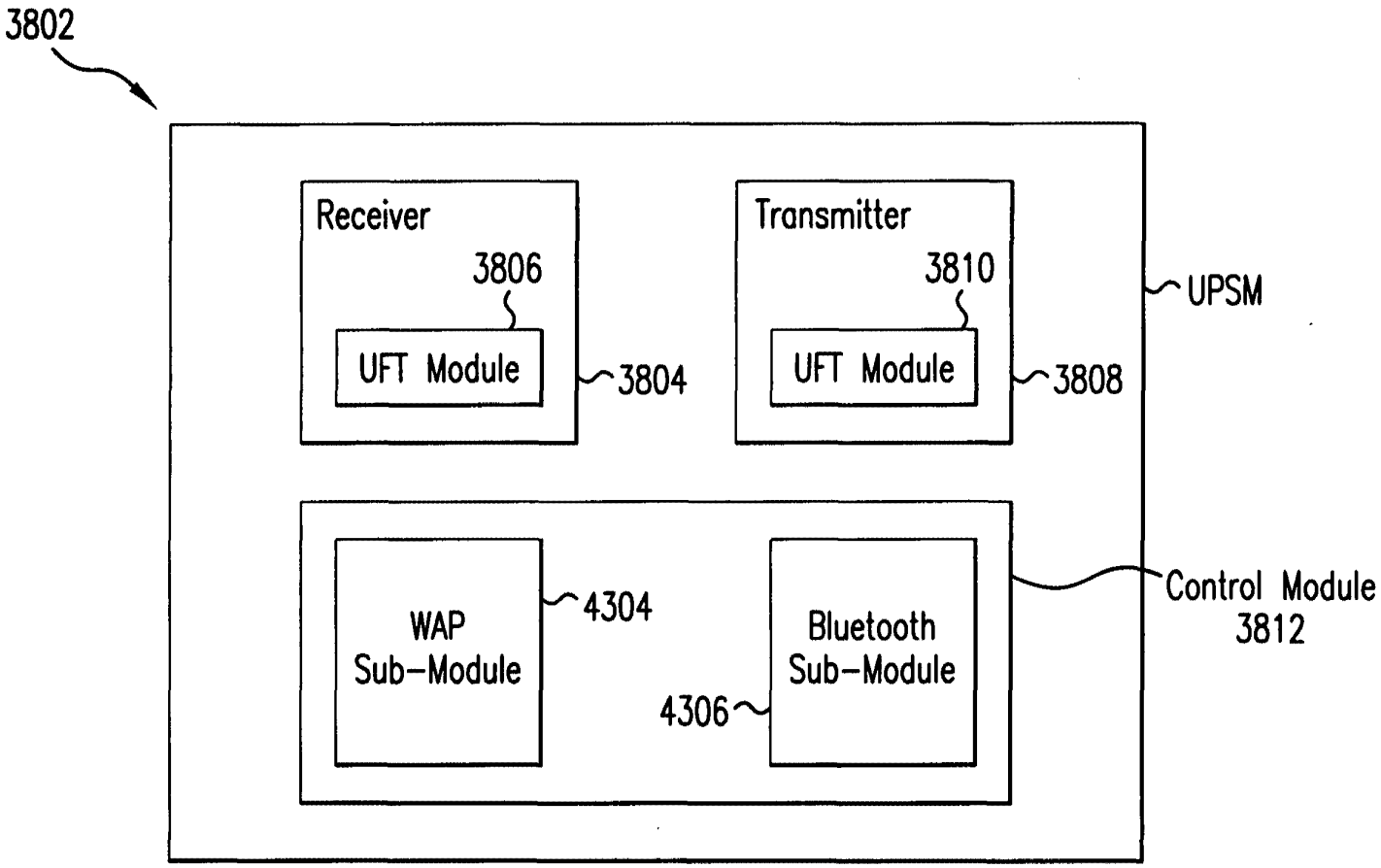

3802
Receiver
3806
UFT Module
3804
Transmitter
3810
UFT Module
3808
UPSM
WAP
Sub-Module
4304
4306
Bluetooth
Sub-Module
Control Module
3812

FIG.43

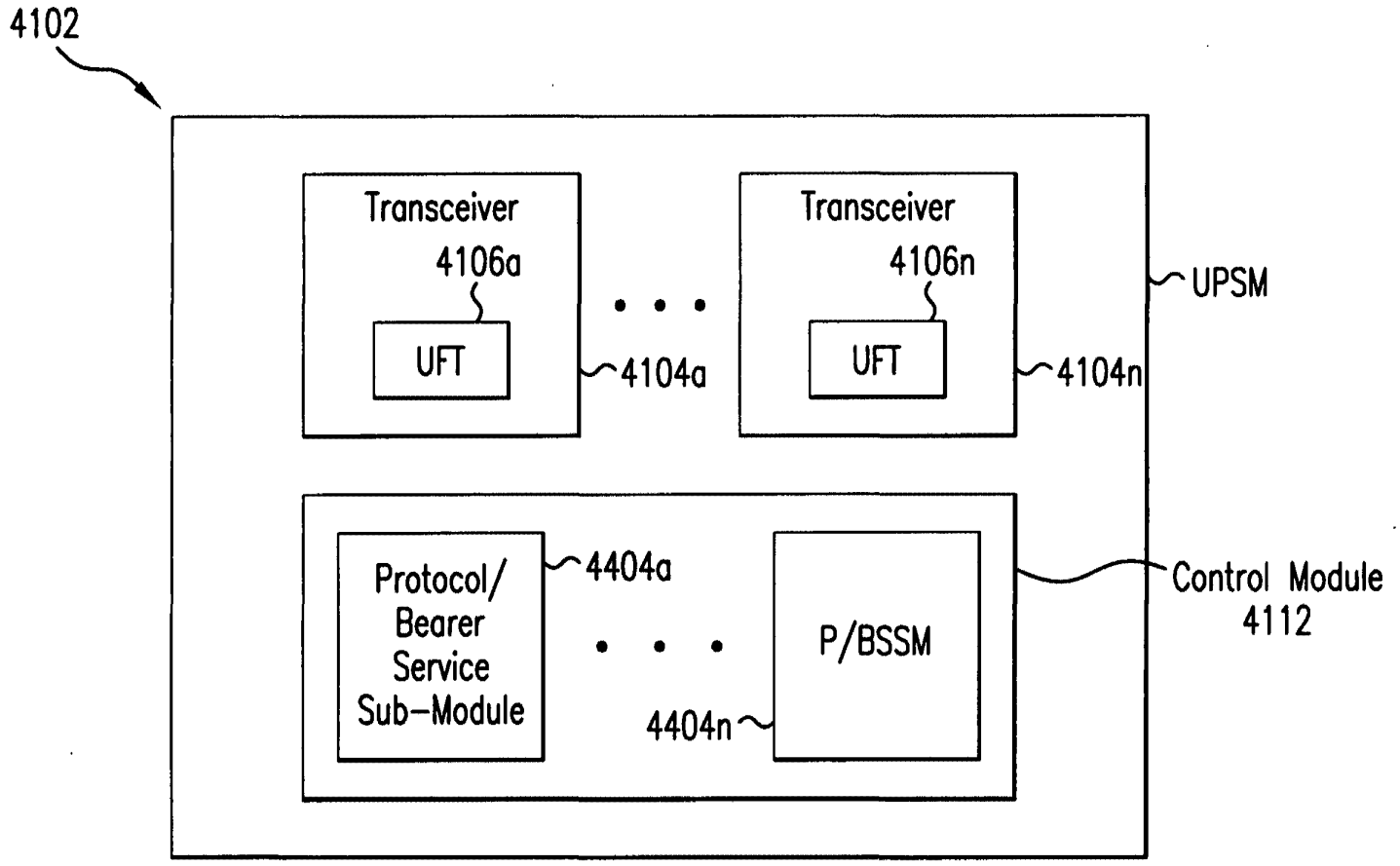

4102
Transceiver
4106a
UFT
4104a
Transceiver
4106n
UFT
4104n
UPSM
Protocol/
Bearer
Service
Sub-Module
4404a
4404n
P/BSSM
Control Module
4112

FIG.44

FIG. 45A

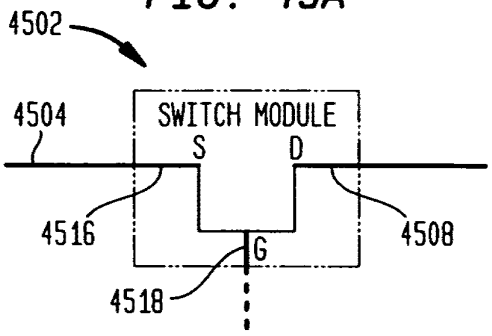


FIG. 45B

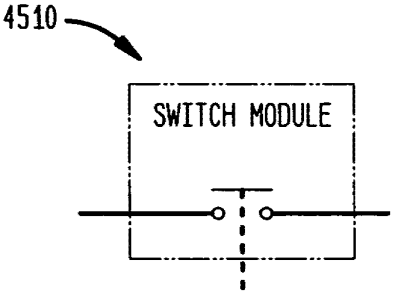


FIG. 45C

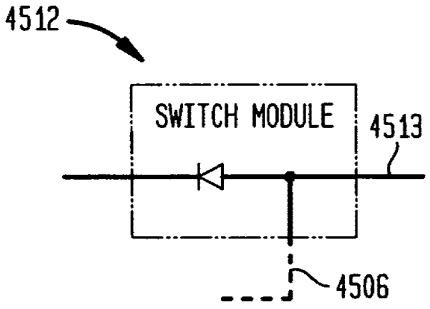


FIG. 45D

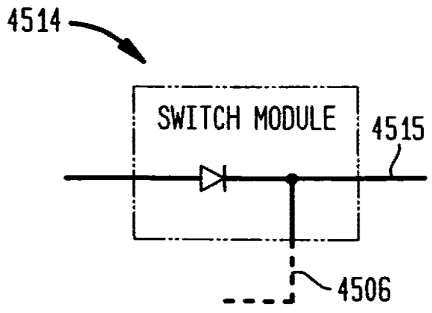
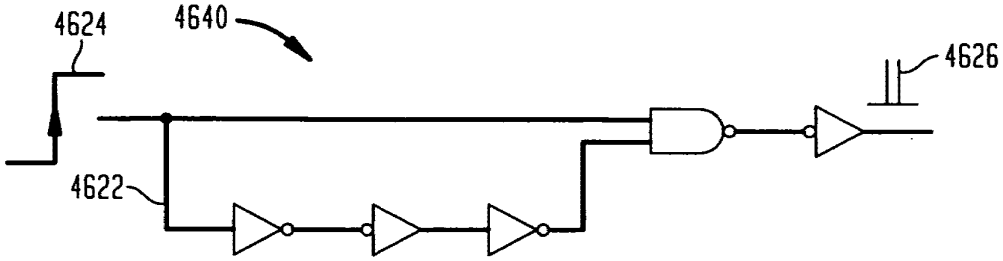
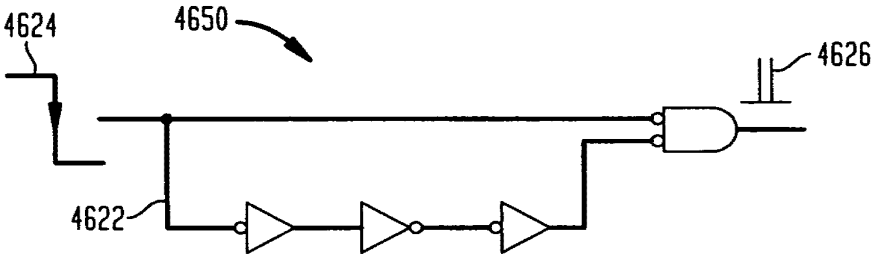


FIG. 46A



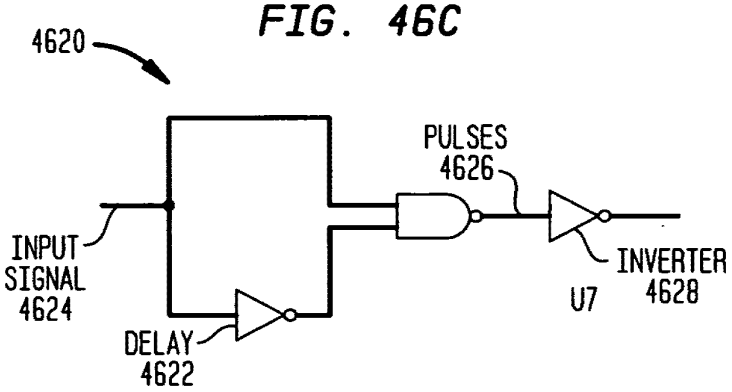
RISING EDGE PULSE GENERATOR

FIG. 46B



FALLING-EDGE PULSE GENERATOR

FIG. 46C



-SUBSTANTIAL EQUIVALENCE IN LOGIC ONLY IS NECESSARY.
-u7 SHOWN FOR POLARITY CONSISTENCY WITH
CKT EXAMPLES DESCRIBED ELSEWHERE

FIG. 46D

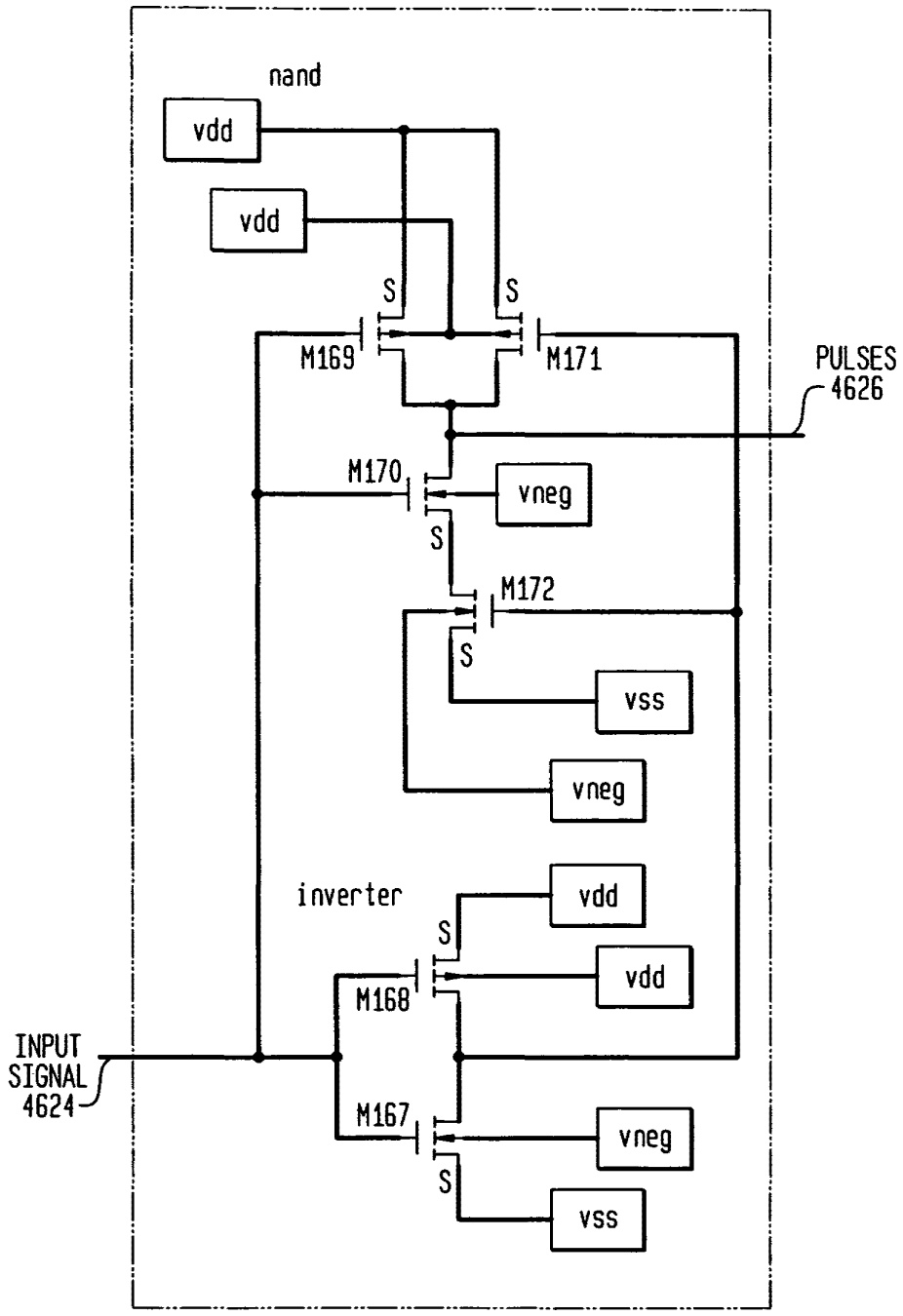


FIG. 46E

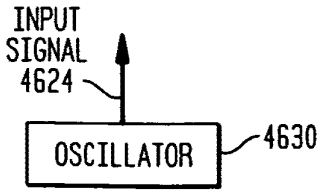


FIG. 47

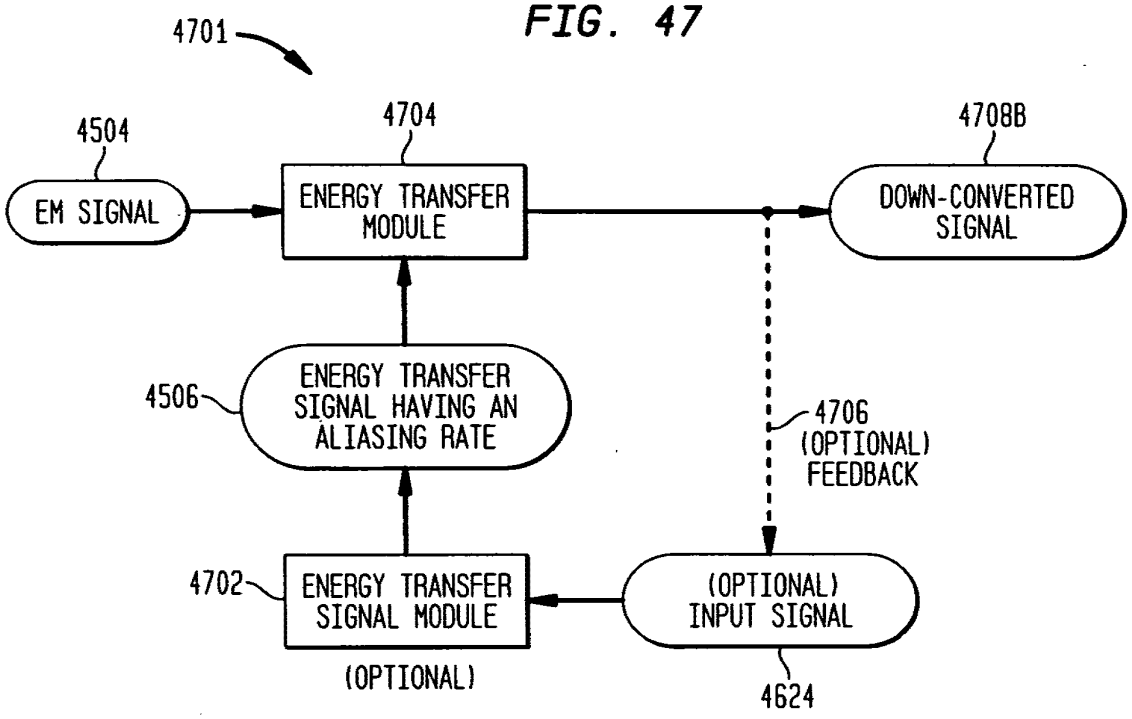

4701
4504
EM SIGNAL
4704
ENERGY TRANSFER MODULE
4708B
DOWN-CONVERTED SIGNAL
4506
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
4706
(OPTIONAL)
FEEDBACK
4702
ENERGY TRANSFER SIGNAL MODULE
(OPTIONAL)
(OPTIONAL) INPUT SIGNAL
4624

FIG. 48

IMPEDANCE MATCHED ALIASING MODULE

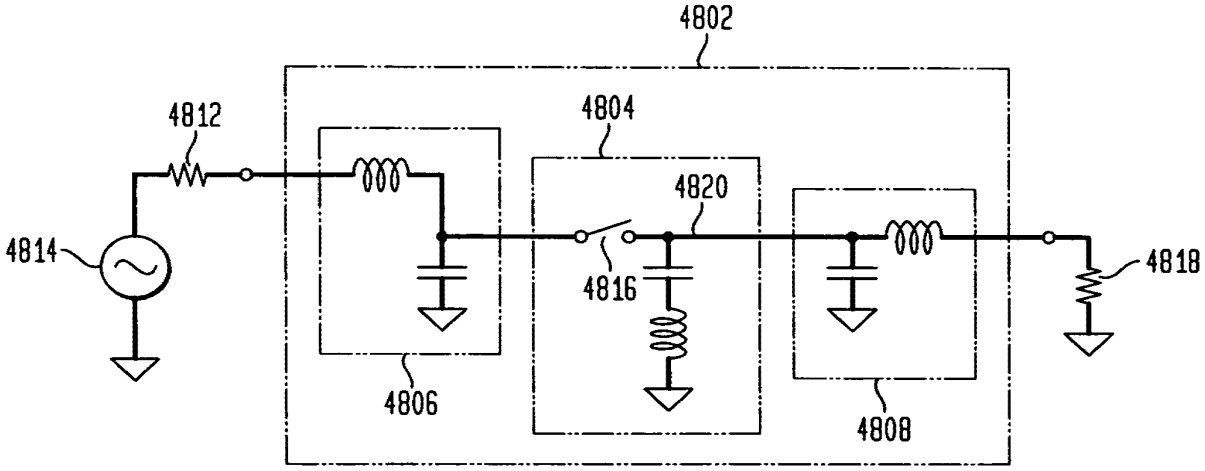


FIG. 49A

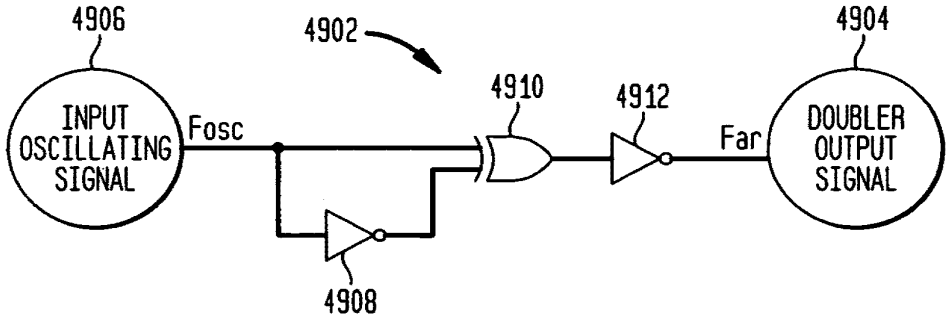


FIG. 49B

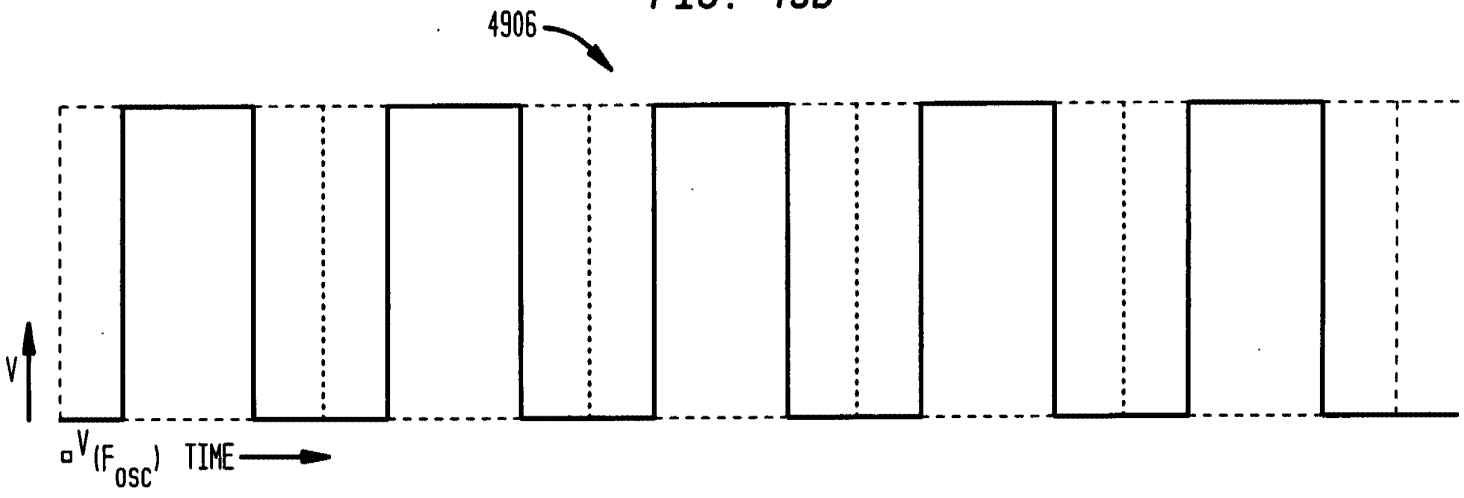


FIG. 49C

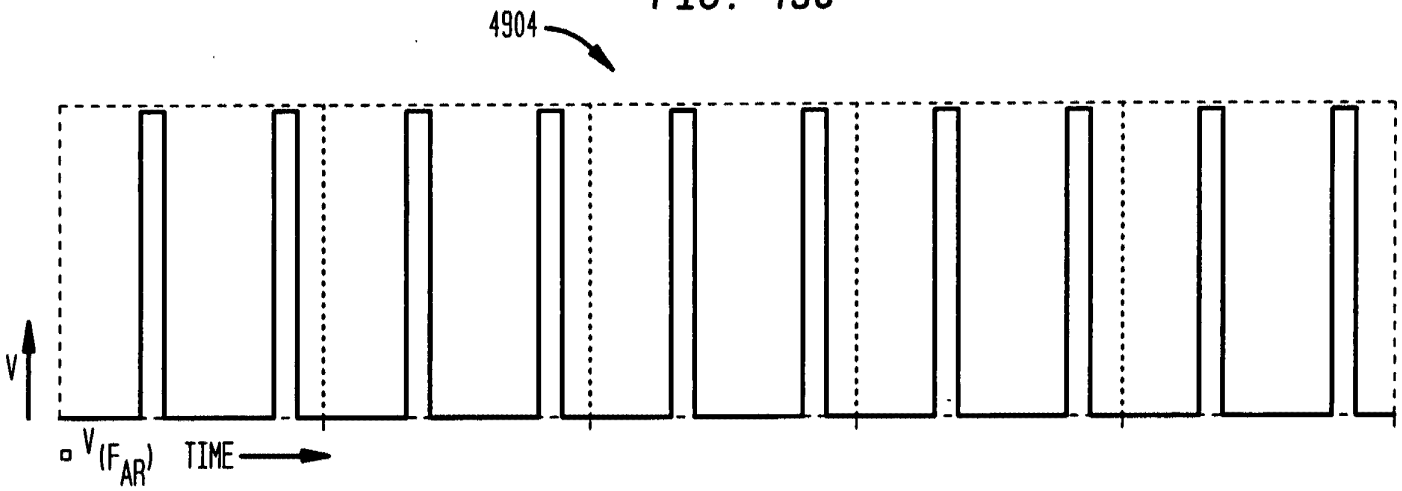


FIG. 50

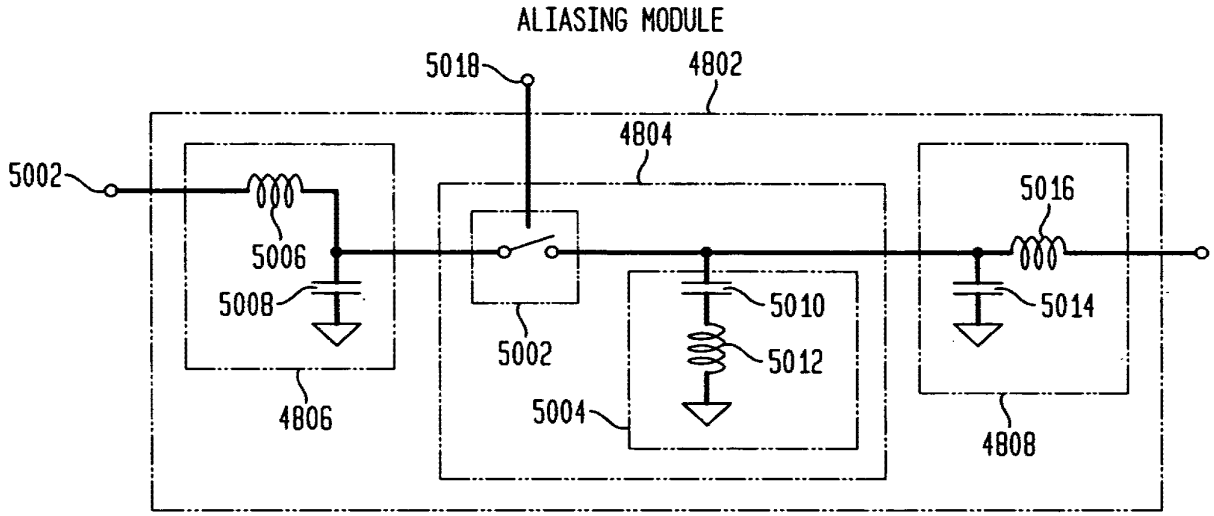

ALIASING MODULE
5018
4802
4804
5002
5006
5008
4806
5002
5010
5012
5004
5016
5014
4808

FIG. 51A

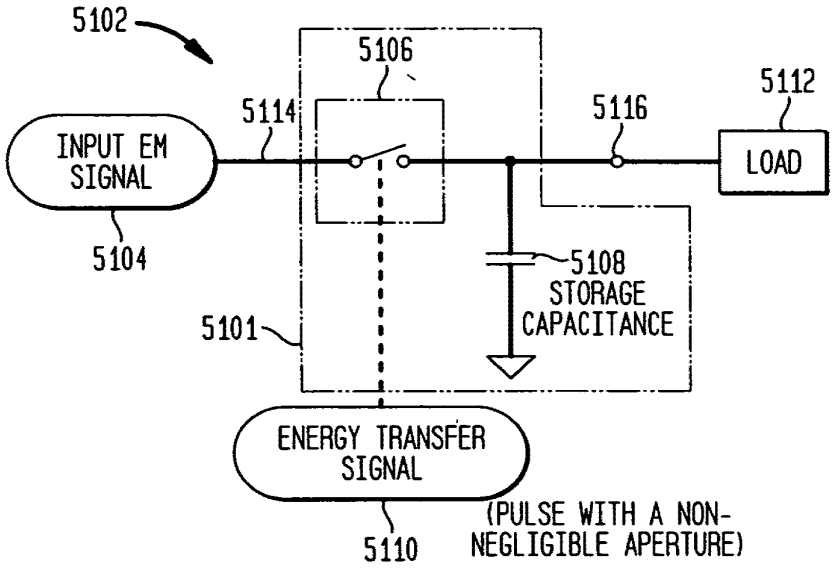


FIG. 51B

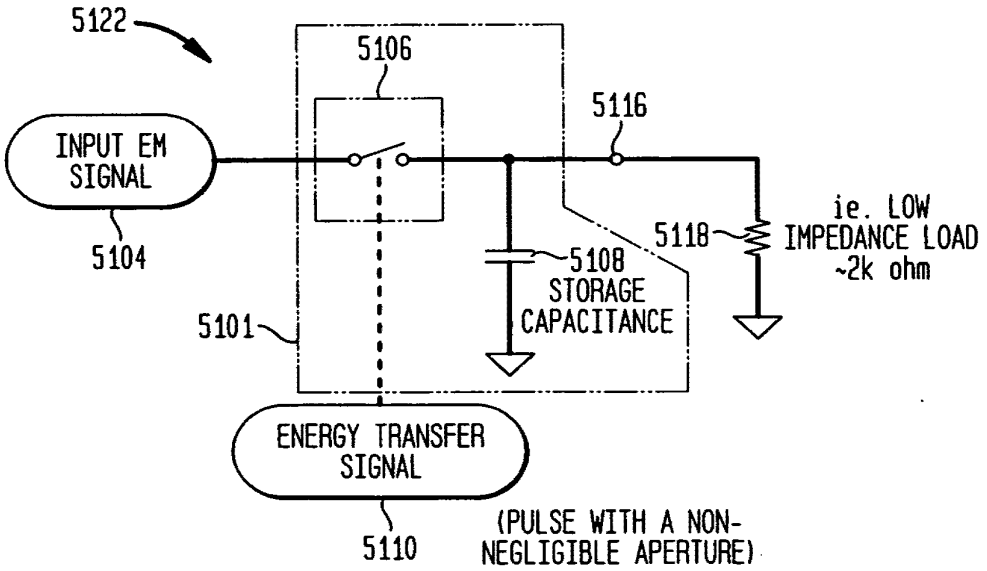


FIG. 52A

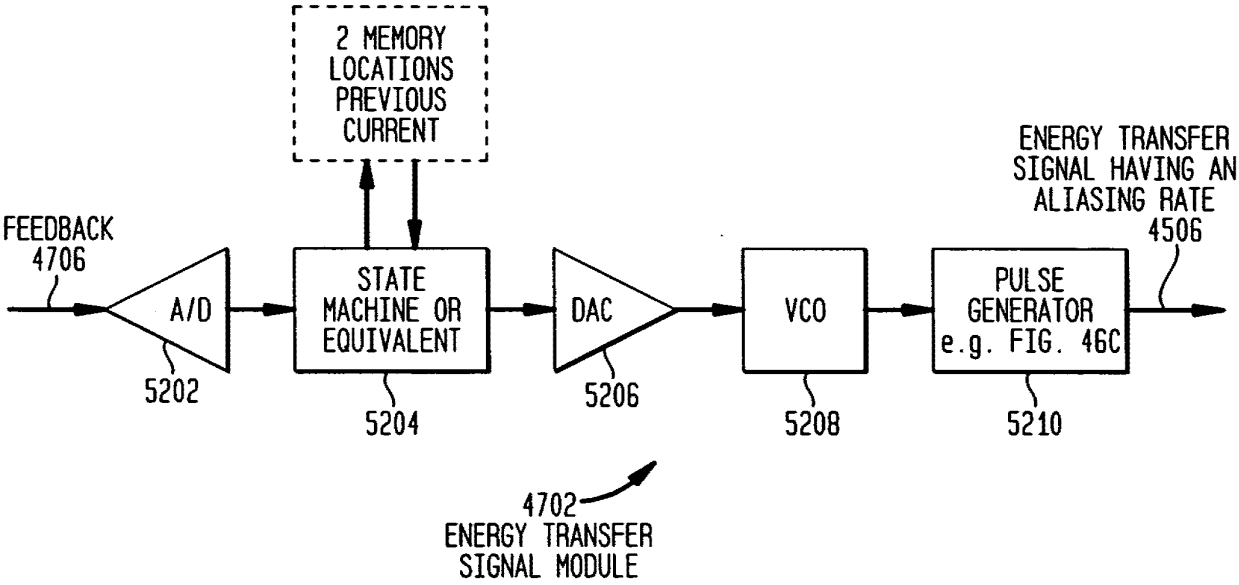

2 MEMORY LOCATIONS PREVIOUS CURRENT
FEEDBACK 4706
A/D
5202
STATE MACHINE OR EQUIVALENT
5204
DAC
5206
VCO
5208
PULSE GENERATOR e.g. FIG. 46C
5210
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE 4506
4702
ENERGY TRANSFER SIGNAL MODULE

FIG. 52B

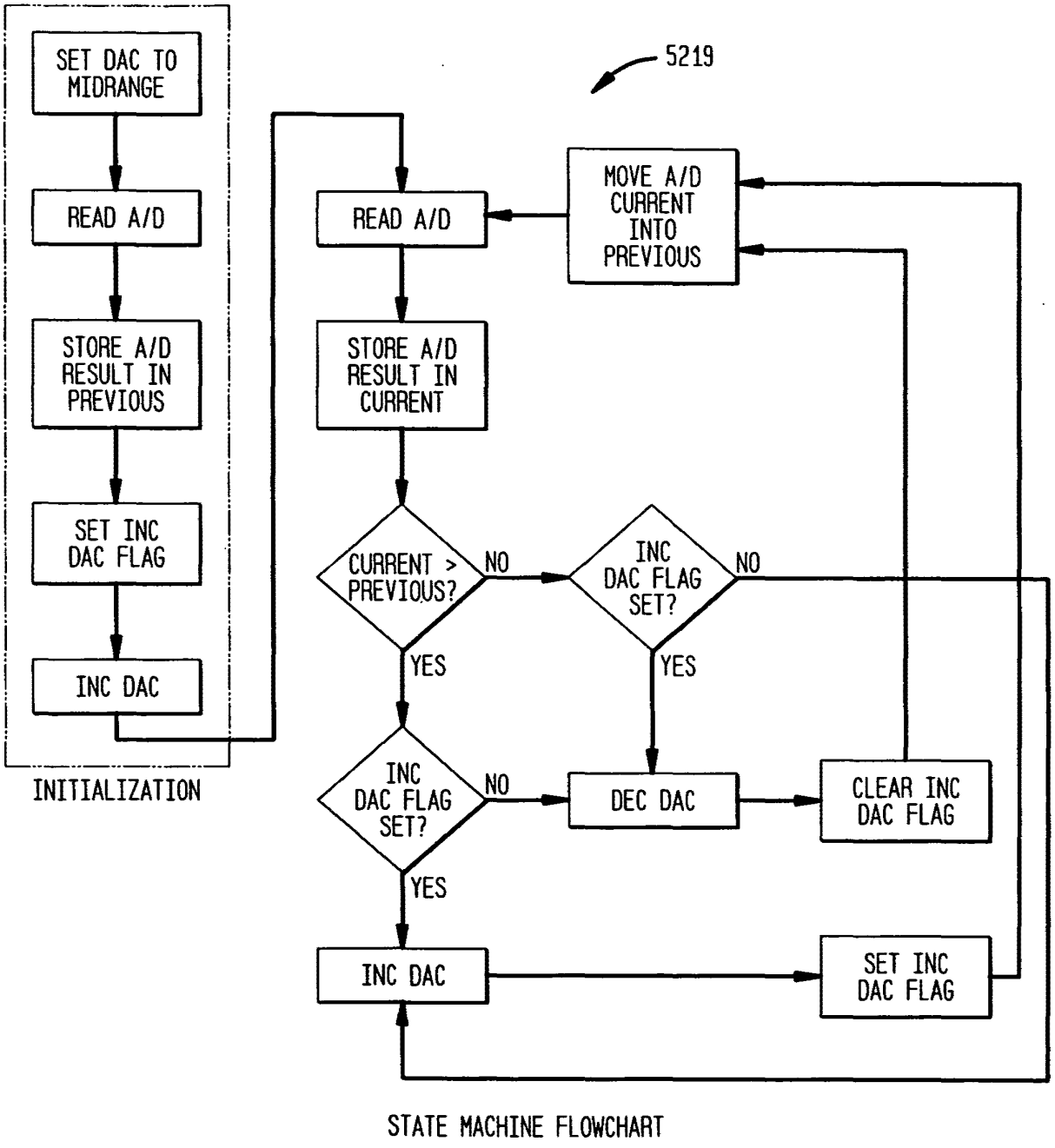
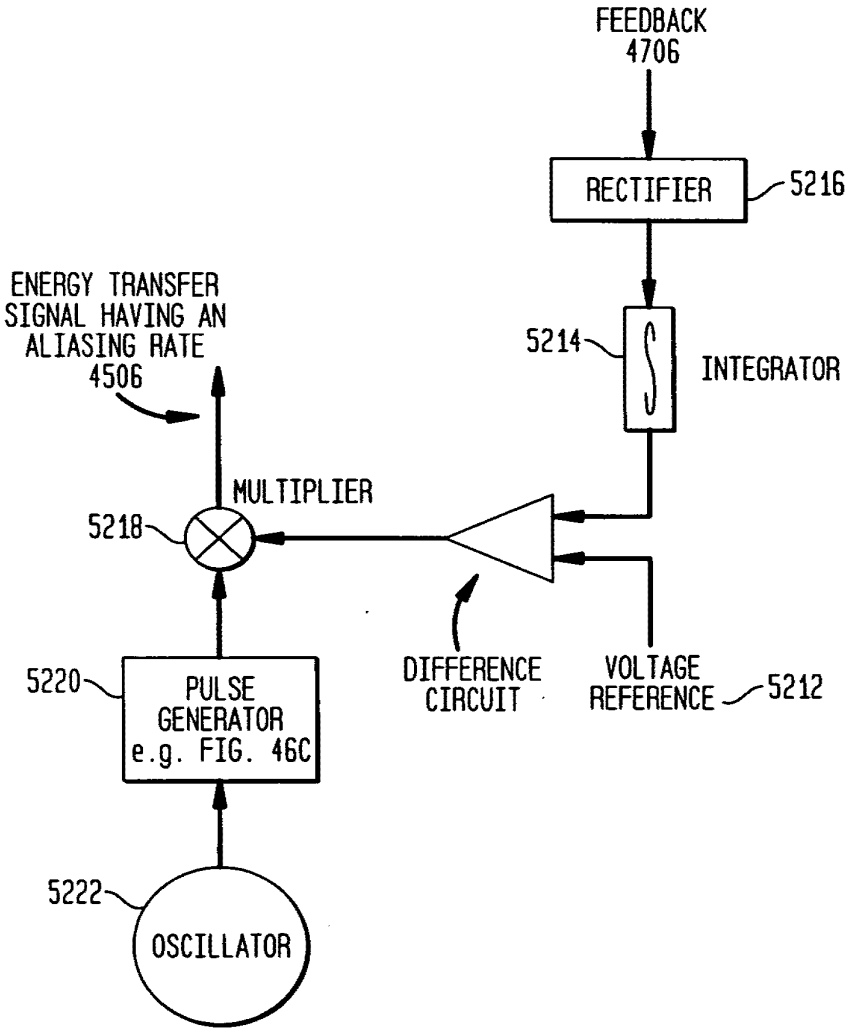

SET DAC TO MIDRANGE
READ A/D
STORE A/D RESULT IN PREVIOUS
SET INC DAC FLAG
INC DAC
INITIALIZATION
5219
READ A/D
MOVE A/D CURRENT INTO PREVIOUS
STORE A/D RESULT IN CURRENT
CURRENT > PREVIOUS?
NO
INC DAC FLAG SET?
NO
YES
YES
INC DAC FLAG SET?
NO
DEC DAC
CLEAR INC DAC FLAG
YES
INC DAC
SET INC DAC FLAG
STATE MACHINE FLOWCHART

FIG. 52C



ENERGY TRANSFER SIGNAL MODULE 4702

FIG. 53

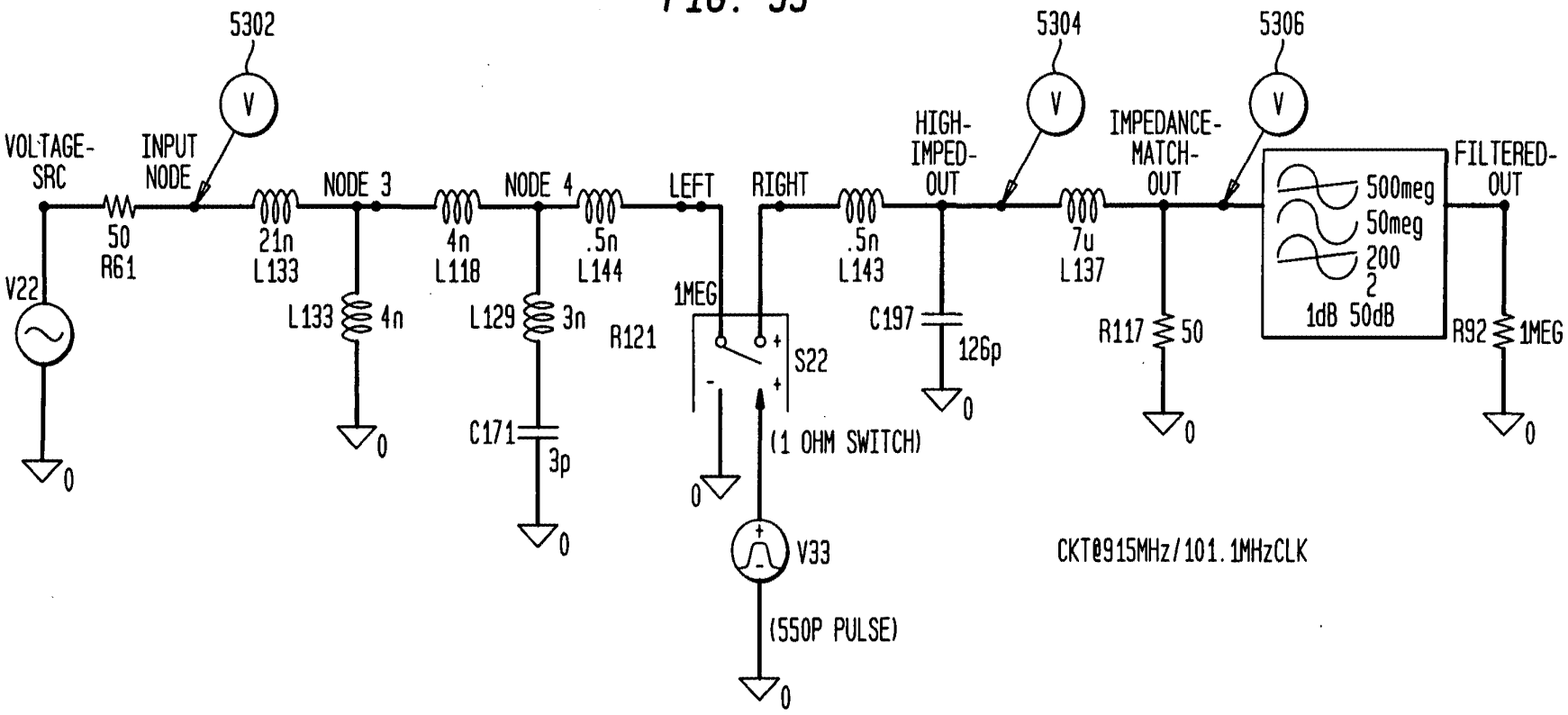

5302
5304
5306
V
V
V
VOLTAGE-
SRC
INPUT
NODE
NODE 3
NODE 4
LEFT
RIGHT
HIGH-
IMPED-
OUT
IMPEDANCE-
MATCH-
OUT
FILTERED-
OUT
V22
50
R61
21n
L133
L133 4n
4n
L118
L129 3n
.5n
L144
1MEG
R121
S22
.5n
L143
C197
126p
7u
L137
R117 50
500meg
50meg
200
2
1dB 50dB
R92 1MEG
C171
3p
(1 OHM SWITCH)
V33
(550P PULSE)
CKT@915MHz/101.1MHzCLK
0

FIG. 54

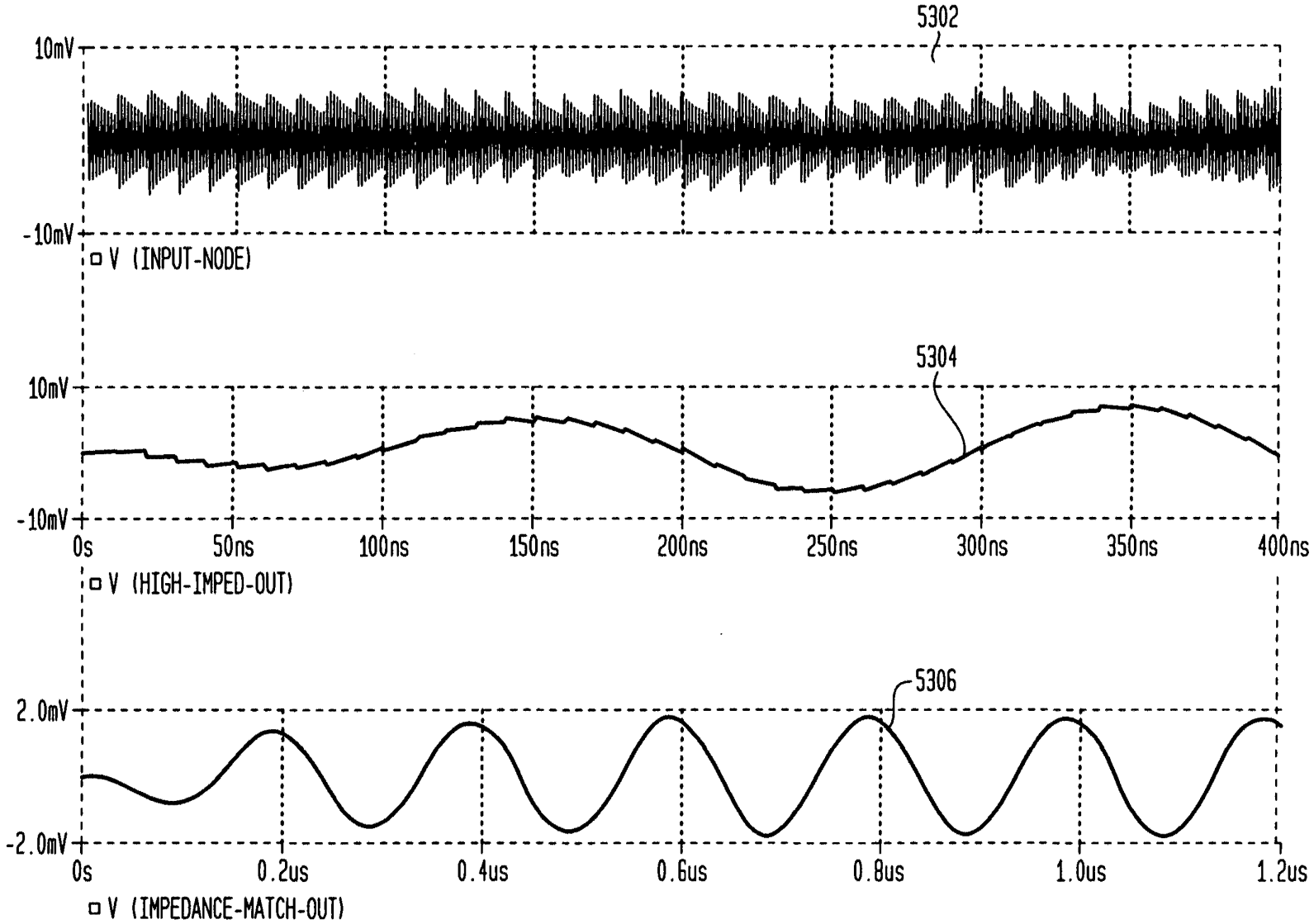

5302
10mV
-10mV
V (INPUT-NODE)
5304
10mV
-10mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V (HIGH-IMPED-OUT)
5306
2.0mV
-2.0mV
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
V (IMPEDANCE-MATCH-OUT)

FIG. 55

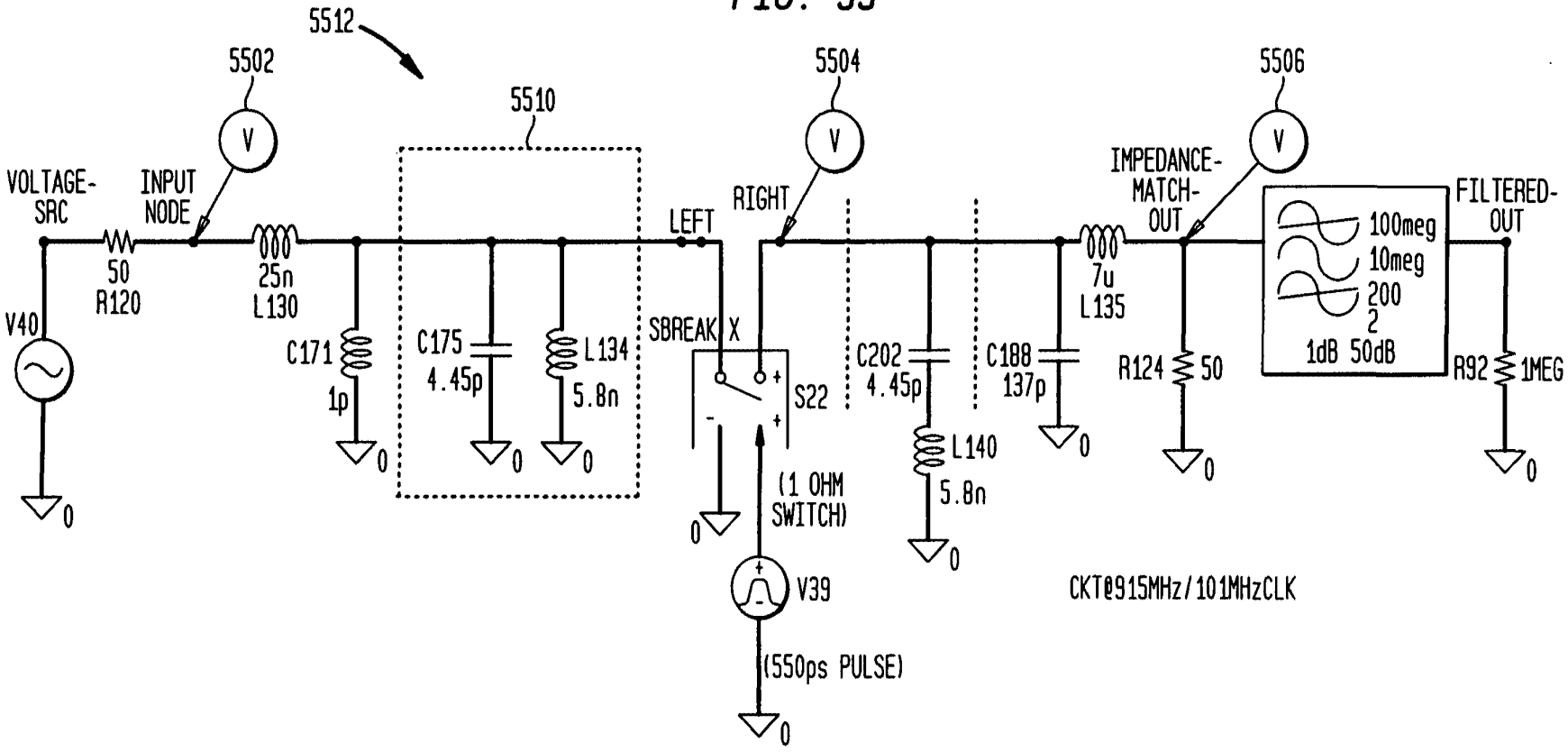

5512
5502
5510
5504
5506
VOLTAGE-SRC
INPUT NODE
V
V
V
V40
50
R120
25n
L130
C171
1p
C175
4.45p
L134
5.8n
LEFT
RIGHT
SBREAK X
S22
(1 OHM SWITCH)
V39
(550ps PULSE)
C202
4.45p
L140
5.8n
C188
137p
7u
L135
IMPEDANCE-MATCH-OUT
R124
50
100meg
10meg
200
2
1dB 50dB
FILTERED-OUT
R92
1MEG
CKT@915MHz/101MHzCLK
0

FIG. 56

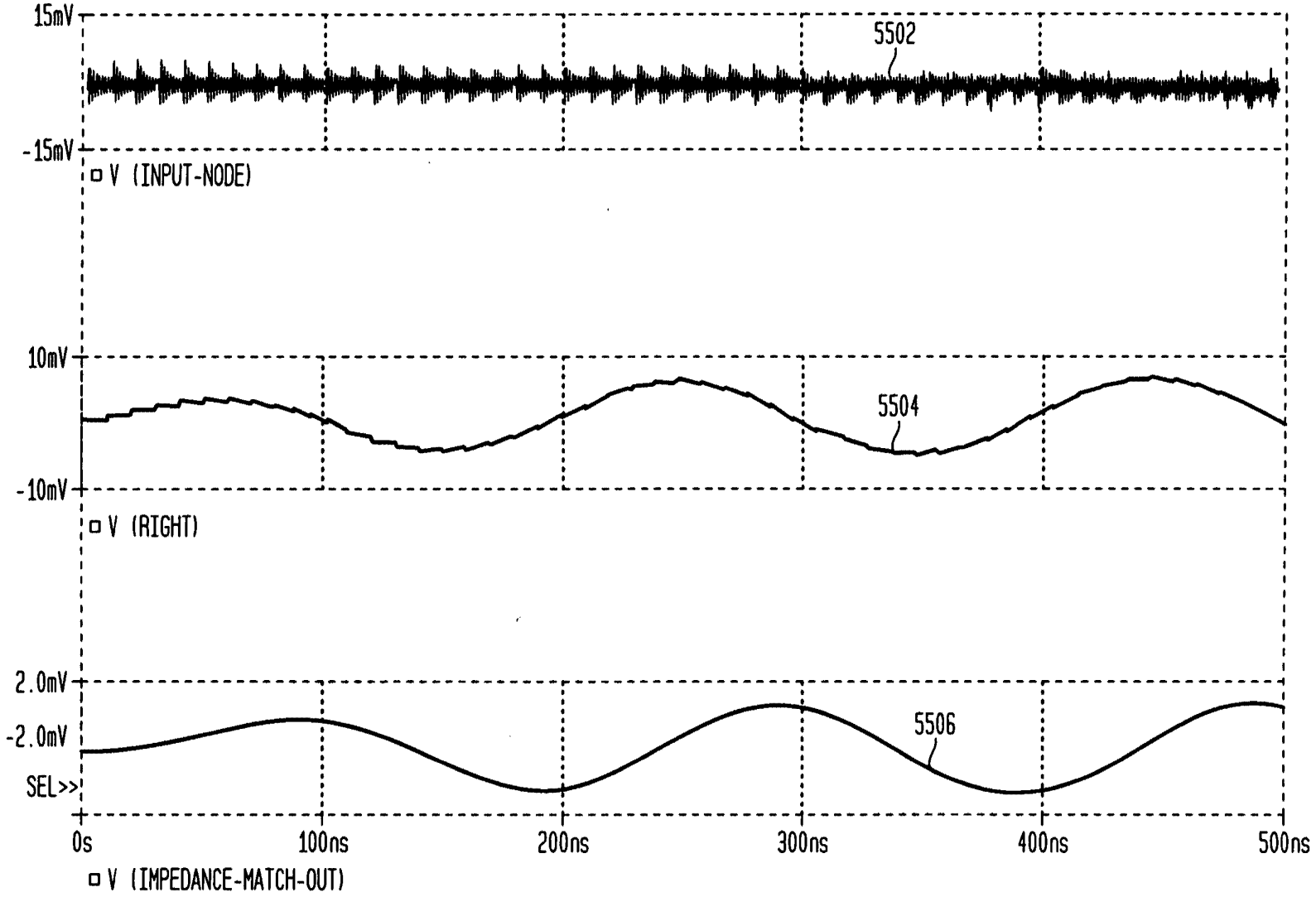

15mV
-15mV
V (INPUT-NODE)
5502
10mV
-10mV
V (RIGHT)
5504
2.0mV
-2.0mV
SEL>>
5506
0s
100ns
200ns
300ns
400ns
500ns
V (IMPEDANCE-MATCH-OUT)

FIG. 57

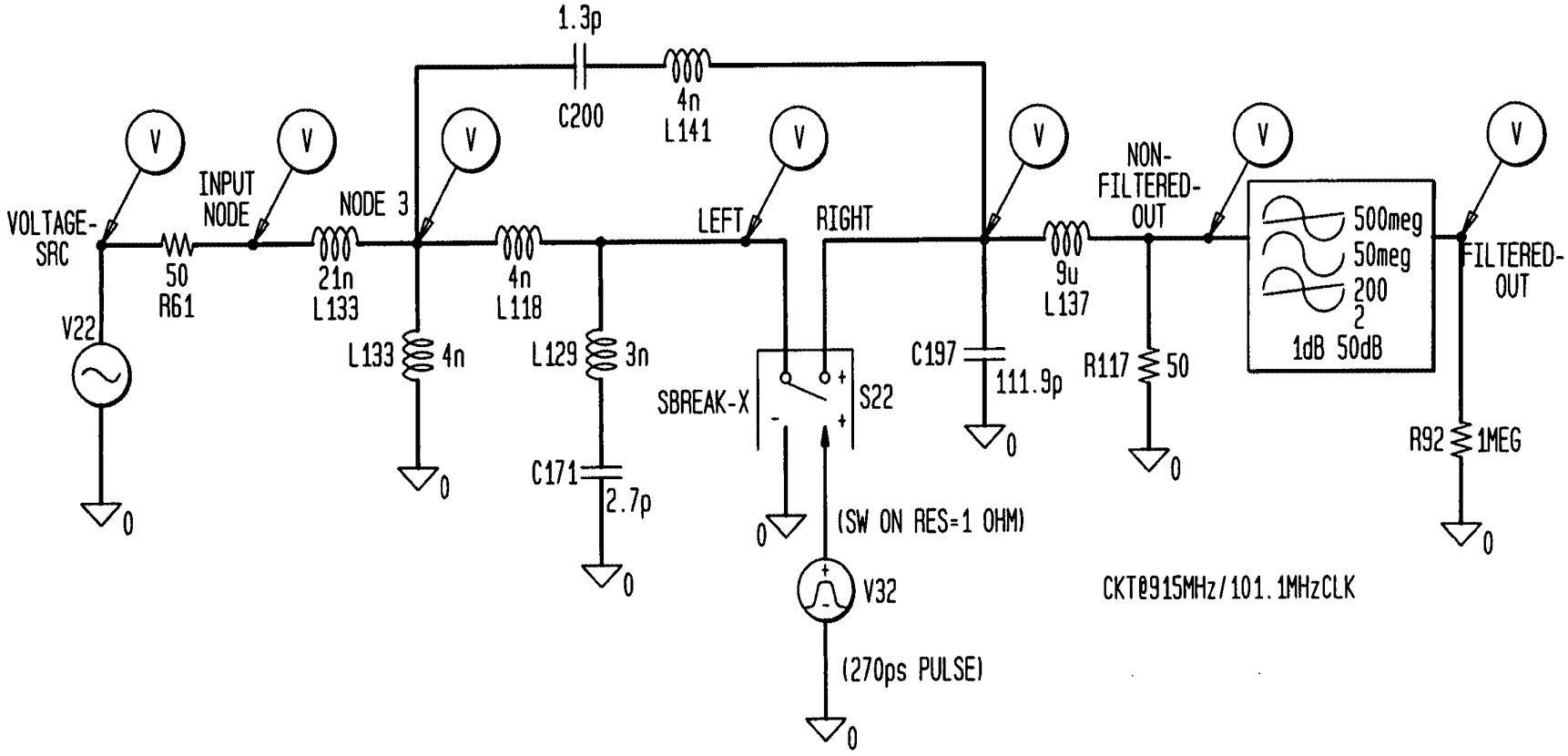

1.3p
C200
4n
L141
V
VOLTAGE-
SRC
INPUT
NODE
NODE 3
LEFT
RIGHT
NON-
FILTERED-
OUT
FILTERED-
OUT
50
R61
21n
L133
4n
L118
9u
L137
V22
L133 4n
L129 3n
C171
2.7p
SBREAK-X
S22
C197
111.9p
R117 50
500meg
50meg
200
2
1dB 50dB
R92 1MEG
(SW ON RES=1 OHM)
V32
(270ps PULSE)
CKT@915MHz/101.1MHzCLK
0

FIG. 58

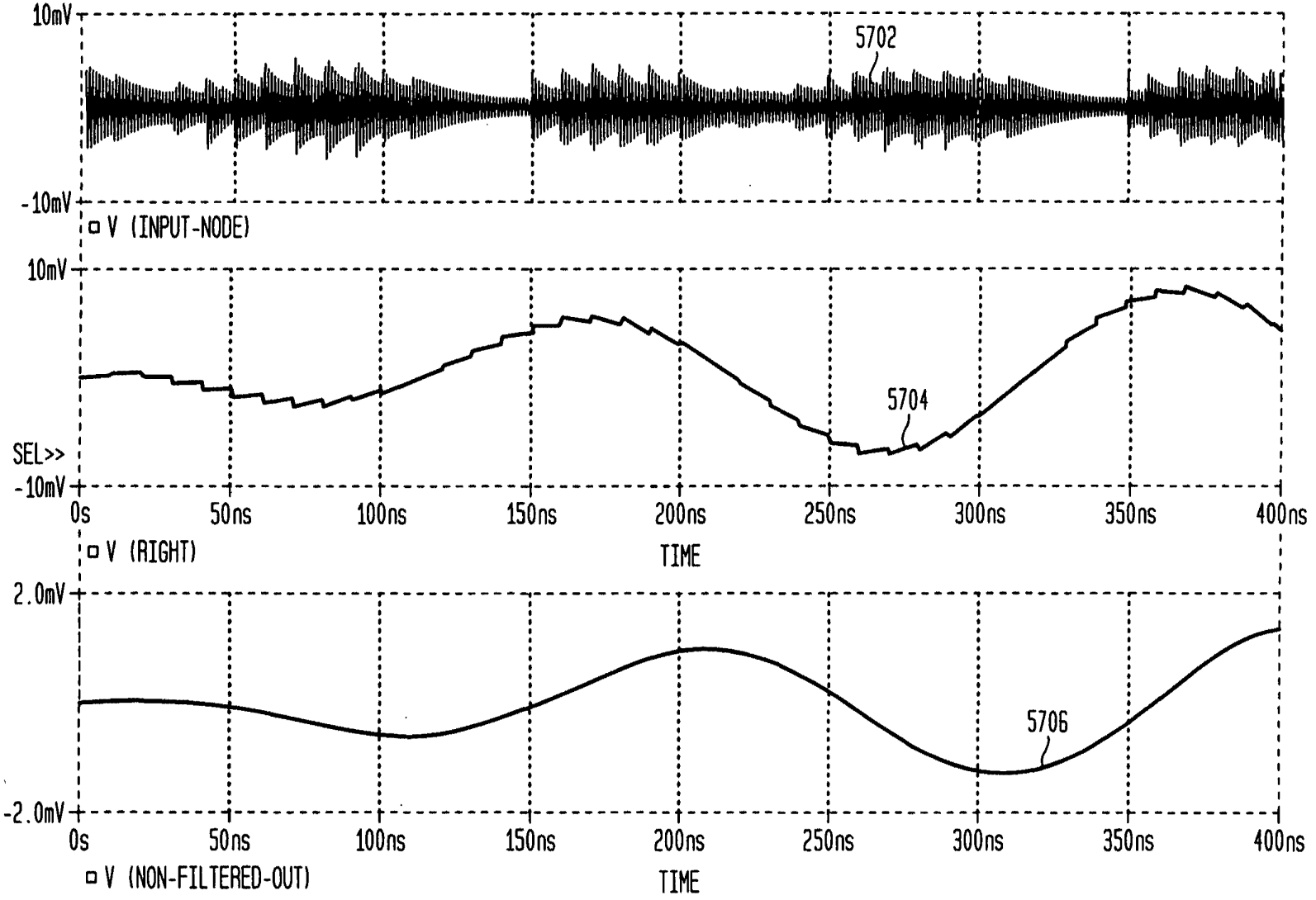
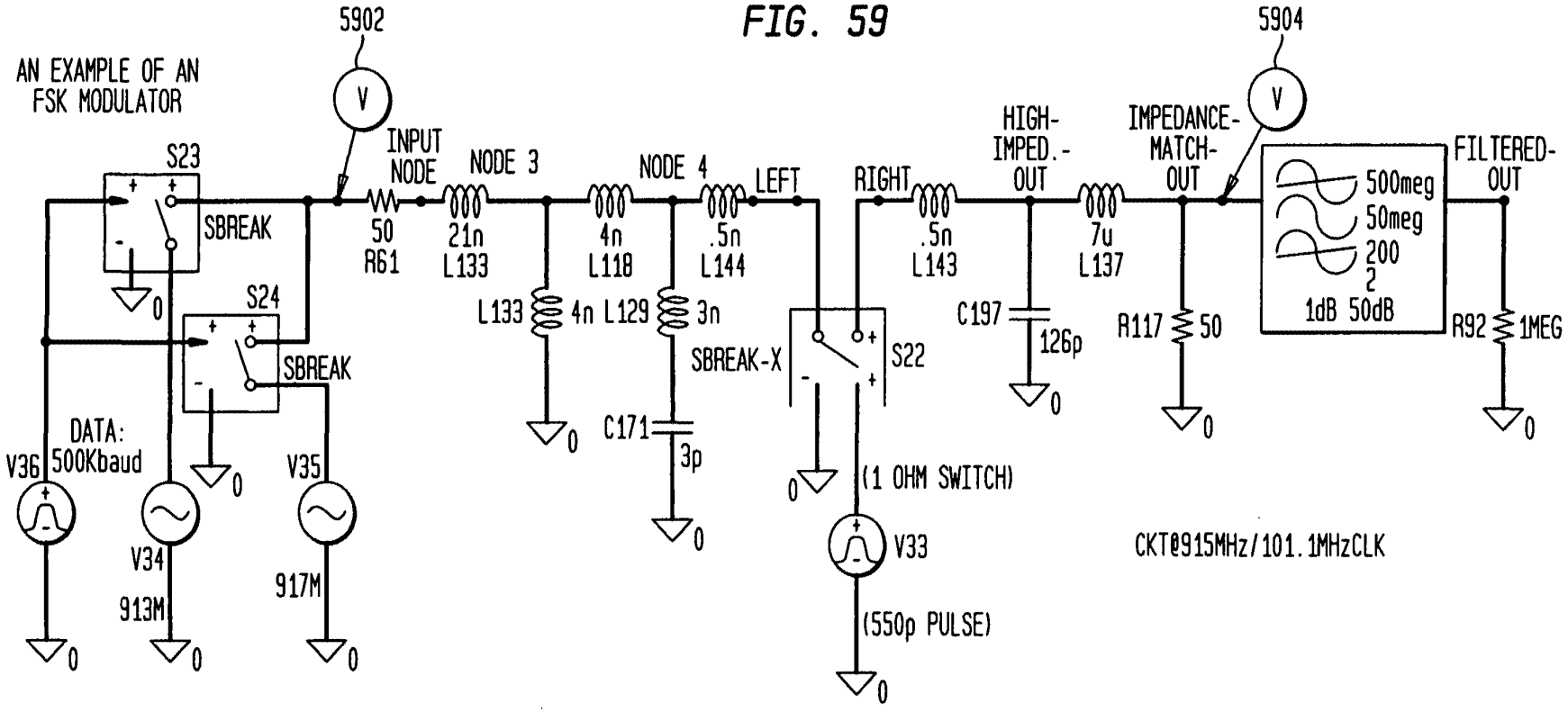

10mV
-10mV
V (INPUT-NODE)
5702
10mV
SEL>>
-10mV
5704
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V (RIGHT)
TIME
2.0mV
-2.0mV
5706
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V (NON-FILTERED-OUT)
TIME

FIG. 59


AN EXAMPLE OF AN FSK MODULATOR
5902
V
INPUT NODE
NODE 3
NODE 4
LEFT
RIGHT
HIGH-IMPED.-OUT
IMPEDANCE-MATCH-OUT
5904
V
FILTERED-OUT
S23
SBREAK
50
R61
21n
L133
4n
L118
.5n
L144
.5n
L143
7u
L137
500meg
50meg
200
2
1dB 50dB
L133 4n
L129 3n
S24
SBREAK
SBREAK-X
S22
C197
126p
R117
50
R92
1MEG
C171
3p
DATA:
500Kbaud
V36
V34
913M
V35
917M
(1 OHM SWITCH)
V33
(550p PULSE)
CKT@915MHz/101.1MHzCLK
0

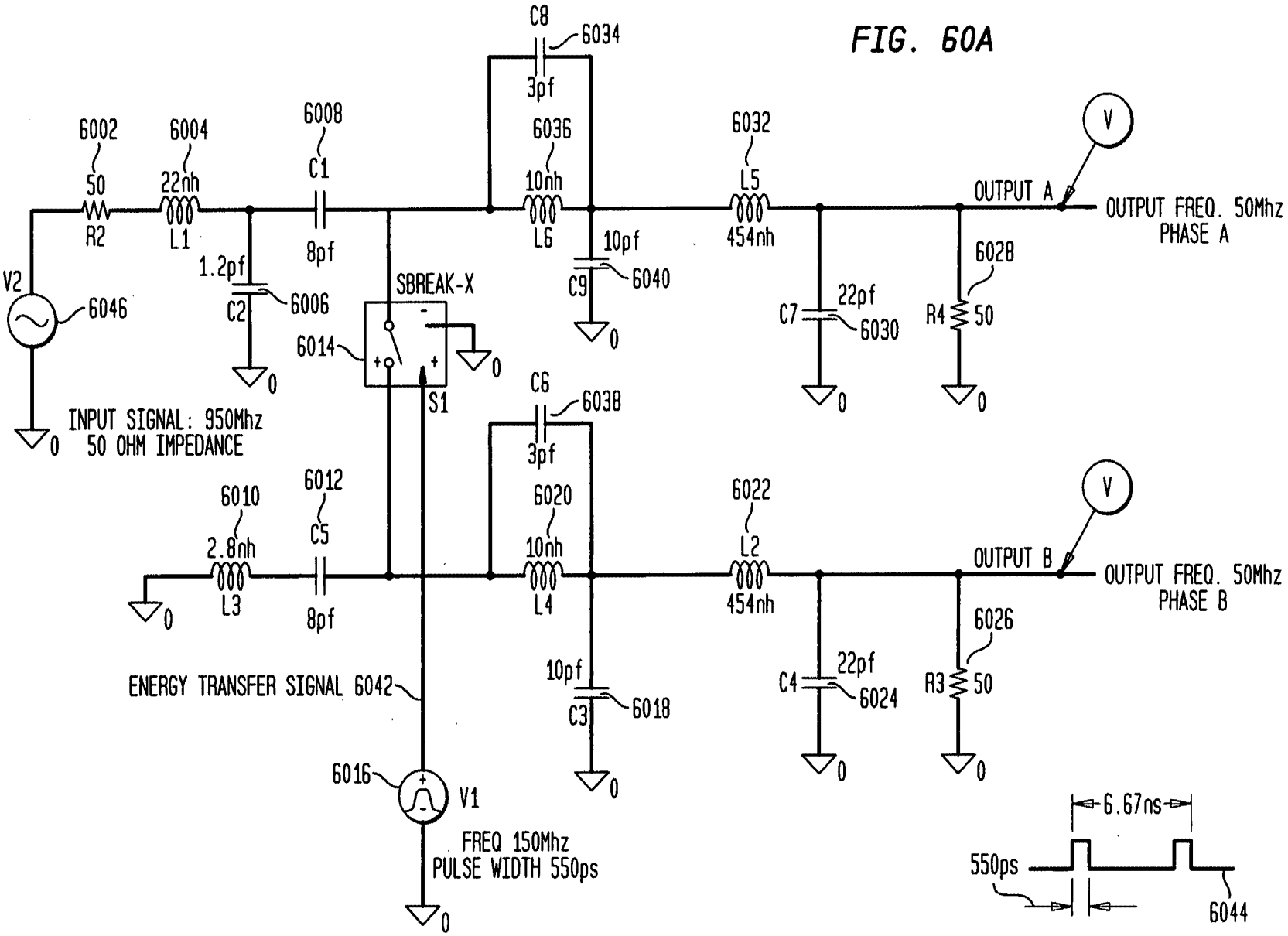

C8
6034
3pf
6002
6004
6008
C1
6036
6032
V
50
22nh
10nh
L5
OUTPUT A
OUTPUT FREQ. 50Mhz
PHASE A
R2
L1
8pf
L6
10pf
454nh
6028
1.2pf
SBREAK-X
V2
6046
C2
6006
C9
6040
22pf
C7
6030
R4
50
6014
0
S1
C6
6038
3pf
INPUT SIGNAL: 950Mhz
50 OHM IMPEDANCE
6010
6012
6020
6022
V
2.8nh
C5
10nh
L2
OUTPUT B
OUTPUT FREQ. 50Mhz
PHASE B
L3
8pf
L4
454nh
6026
ENERGY TRANSFER SIGNAL 6042
10pf
C4
22pf
6024
R3
50
C3
6018
6016
V1
6.67ns
FREQ 150Mhz
PULSE WIDTH 550ps
550ps
6044

FIG. 60A

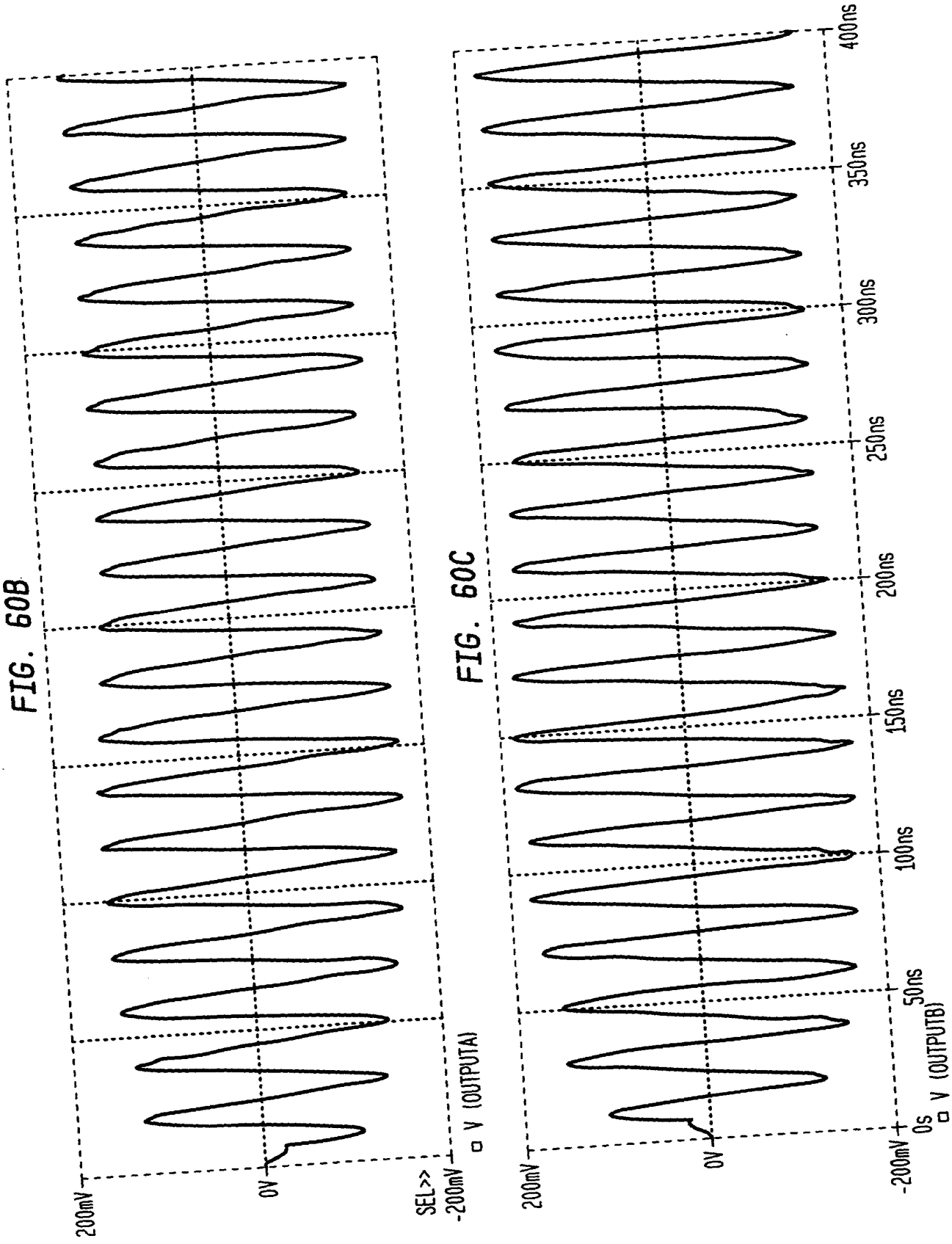

FIG. 60B
200mV
0V
SEL>>
-200mV
V (OUTPUTA)
FIG. 60C
200mV
0V
-200mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V (OUTPUTB)

FIG. 61

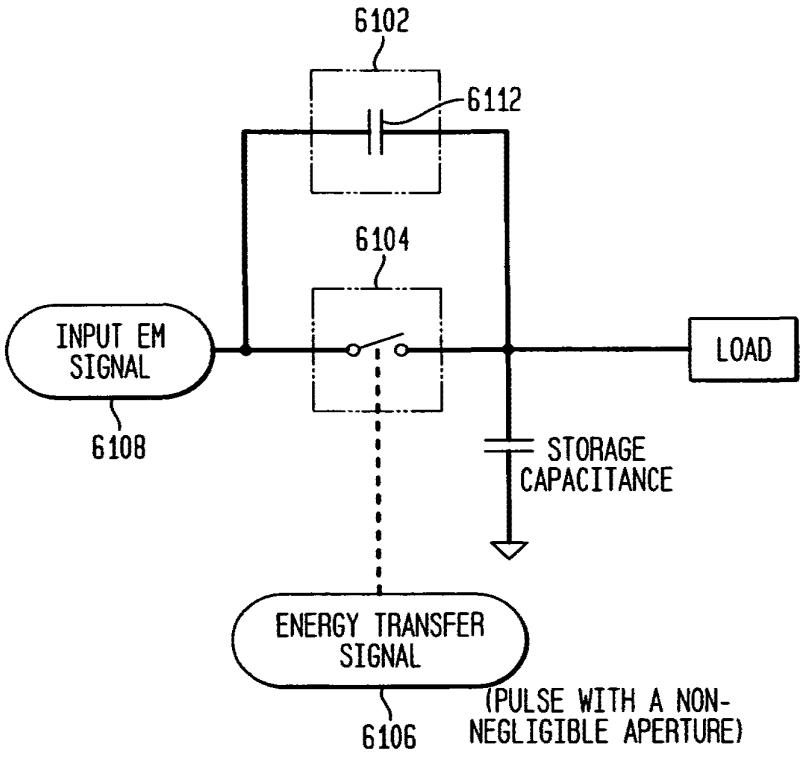

6102
6112
6104
INPUT EM SIGNAL
6108
LOAD
STORAGE CAPACITANCE
ENERGY TRANSFER SIGNAL
6106
(PULSE WITH A NON-NEGLIGIBLE APERTURE)

FIG. 62

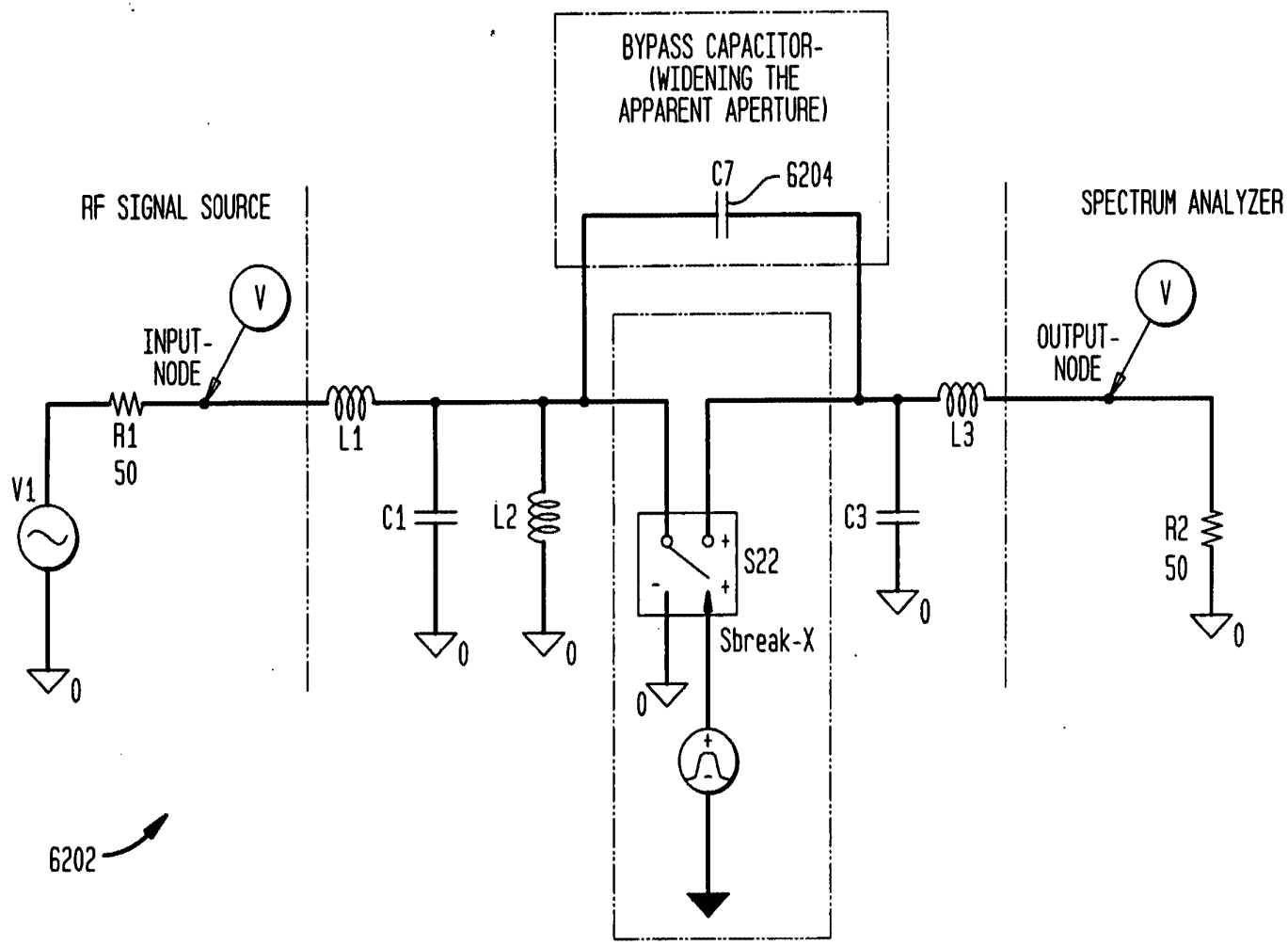

BYPASS CAPACITOR-
(WIDENING THE
APPARENT APERTURE)
C7
6204
RF SIGNAL SOURCE
SPECTRUM ANALYZER
V
INPUT-
NODE
OUTPUT-
NODE
R1
50
L1
L3
V1
C1
L2
S22
C3
R2
50
Sbreak-X
0
6202

FIG. 63

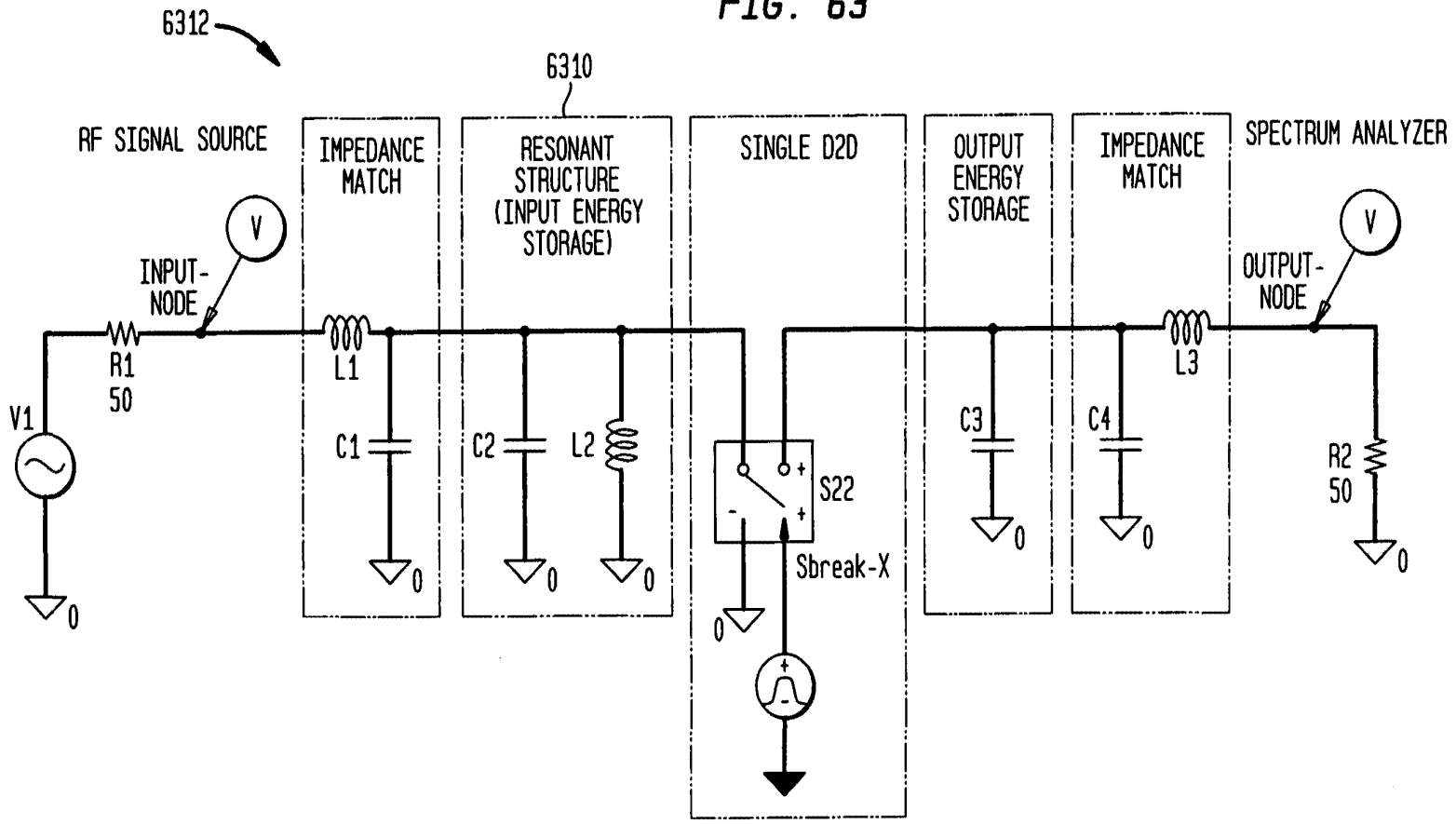
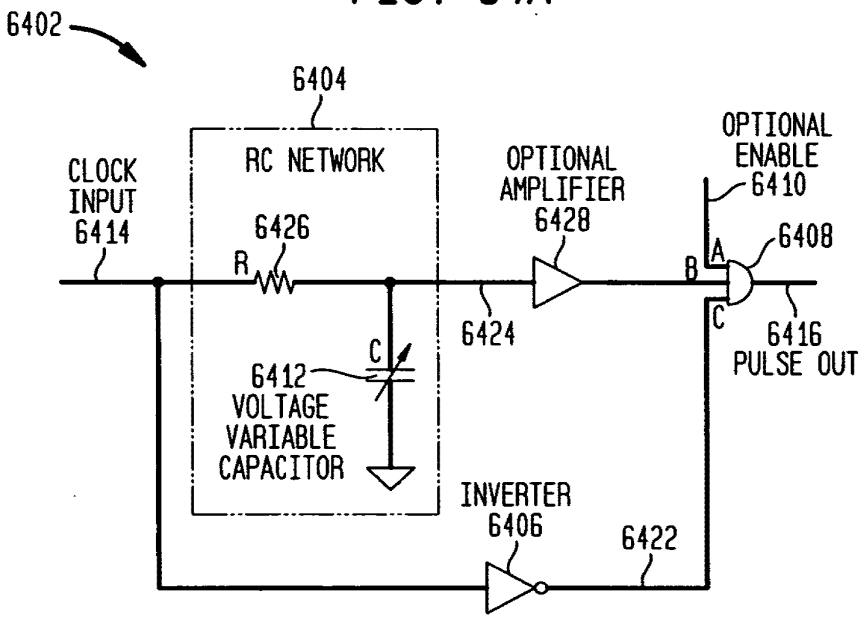

6312
6310
RF SIGNAL SOURCE
IMPEDANCE MATCH
RESONANT STRUCTURE (INPUT ENERGY STORAGE)
SINGLE D2D
OUTPUT ENERGY STORAGE
IMPEDANCE MATCH
SPECTRUM ANALYZER
V
INPUT-NODE
OUTPUT-NODE
R1
50
V1
L1
C1
C2
L2
S22
Sbreak-X
C3
C4
L3
R2
50
0

FIG. 64A


6402
6404
RC NETWORK
CLOCK INPUT 6414
6426
R
C
6412 VOLTAGE VARIABLE CAPACITOR
OPTIONAL AMPLIFIER 6428
6424
OPTIONAL ENABLE 6410
6408
A
B
C
6416 PULSE OUT
INVERTER 6406
6422

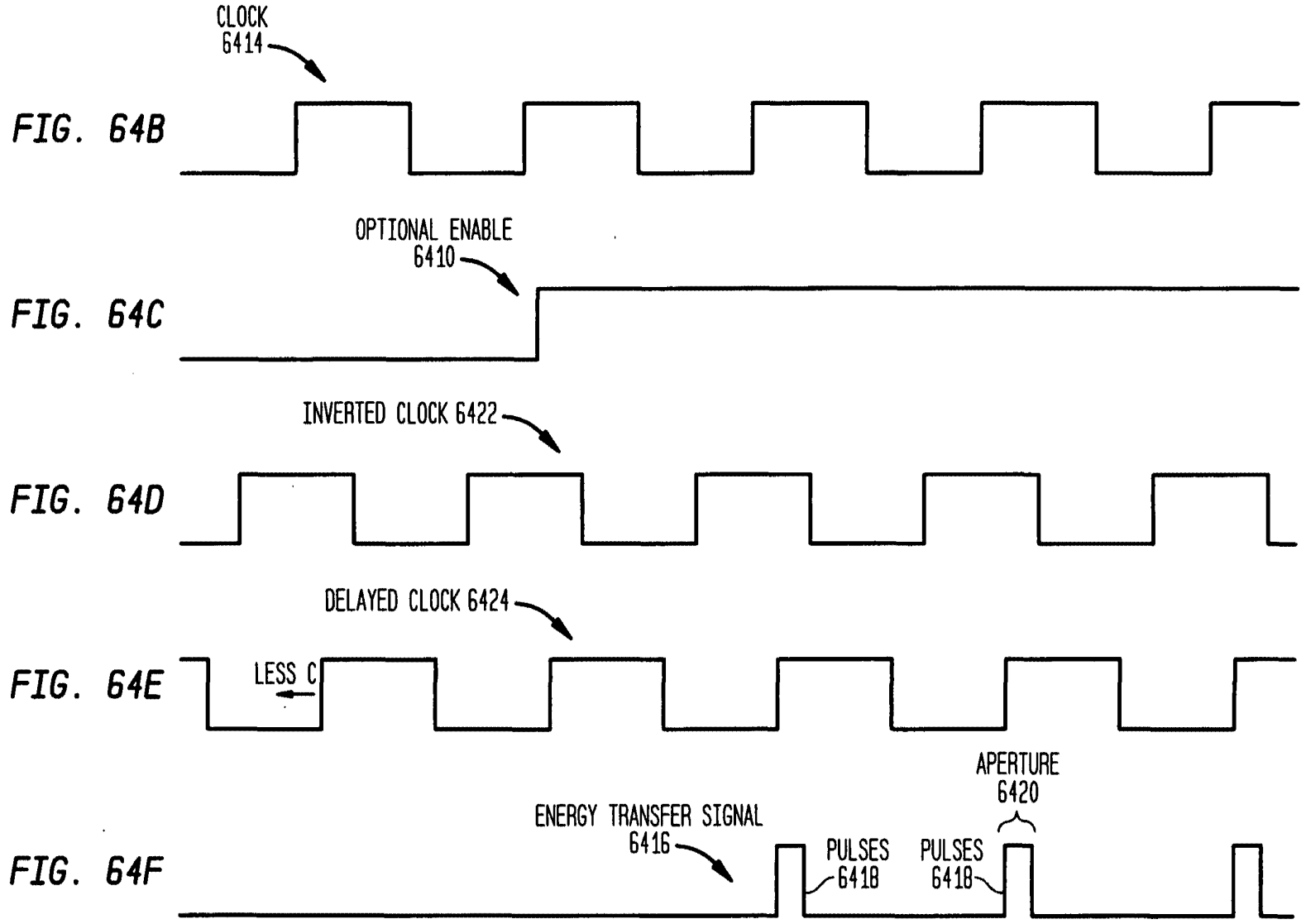


FIG. 64B

FIG. 64C

FIG. 64D

FIG. 64E

FIG. 64F

FIG. 65

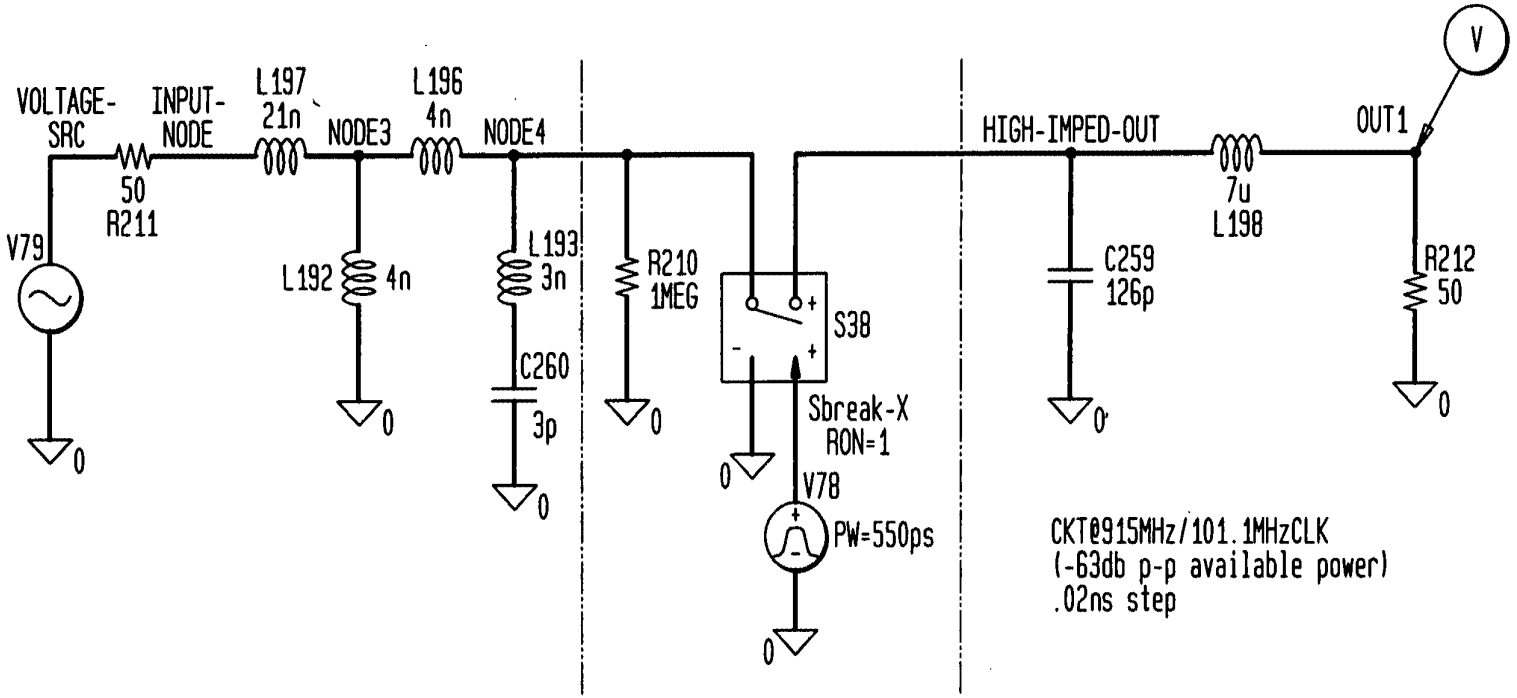

VOLTAGE-SRC
INPUT-NODE
50
R211
L197
21n
NODE3
L196
4n
NODE4
V79
L192
4n
L193
3n
C260
3p
R210
1MEG
S38
Sbreak-X
RON=1
V78
PW=550ps
HIGH-IMPED-OUT
7u
L198
C259
126p
OUT1
V
R212
50
0
CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

FIG. 66

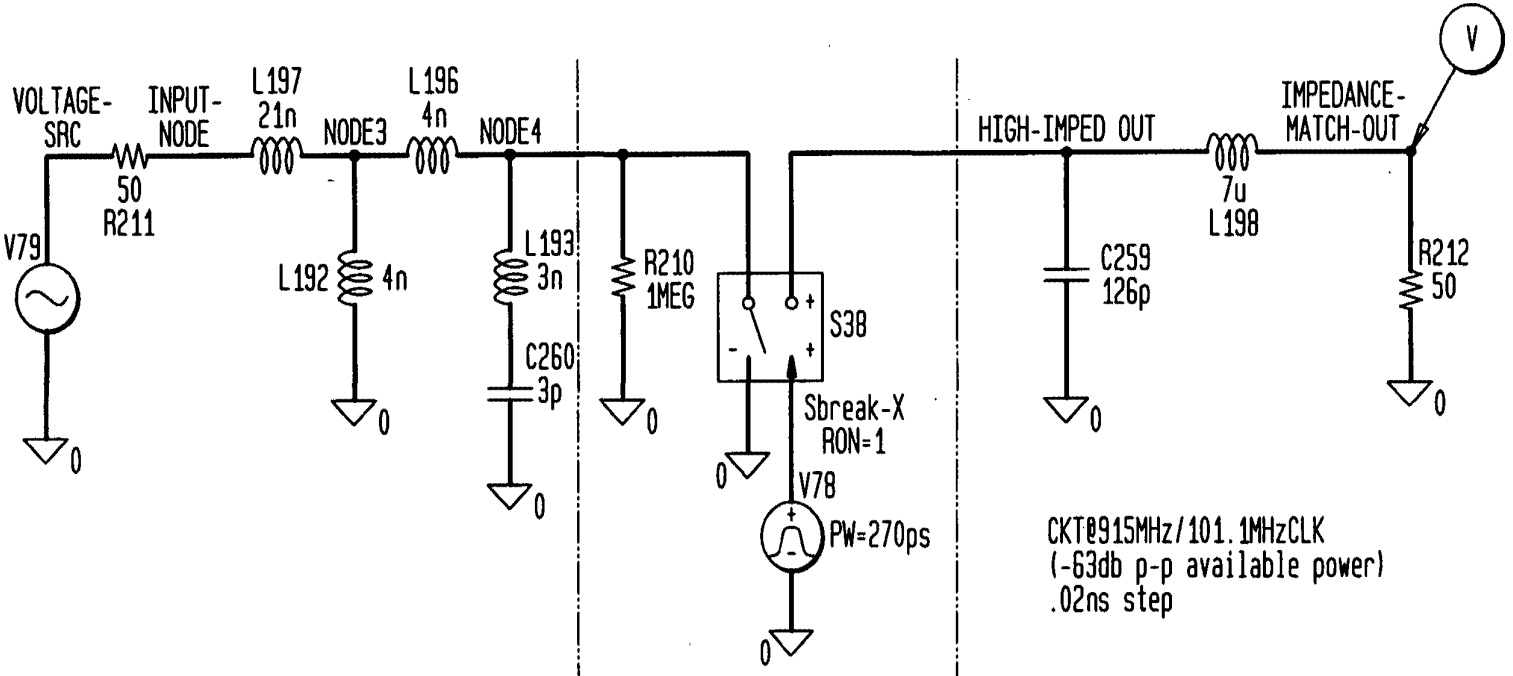

VOLTAGE-SRC
INPUT-NODE
L197 21n
NODE3
L196 4n
NODE4
HIGH-IMPED OUT
IMPEDANCE-MATCH-OUT
V
50 R211
V79
L192 4n
L193 3n
C260 3p
R210 1MEG
S38
Sbreak-X RON=1
V78
PW=270ps
C259 126p
7u L198
R212 50
0
CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

FIG. 67

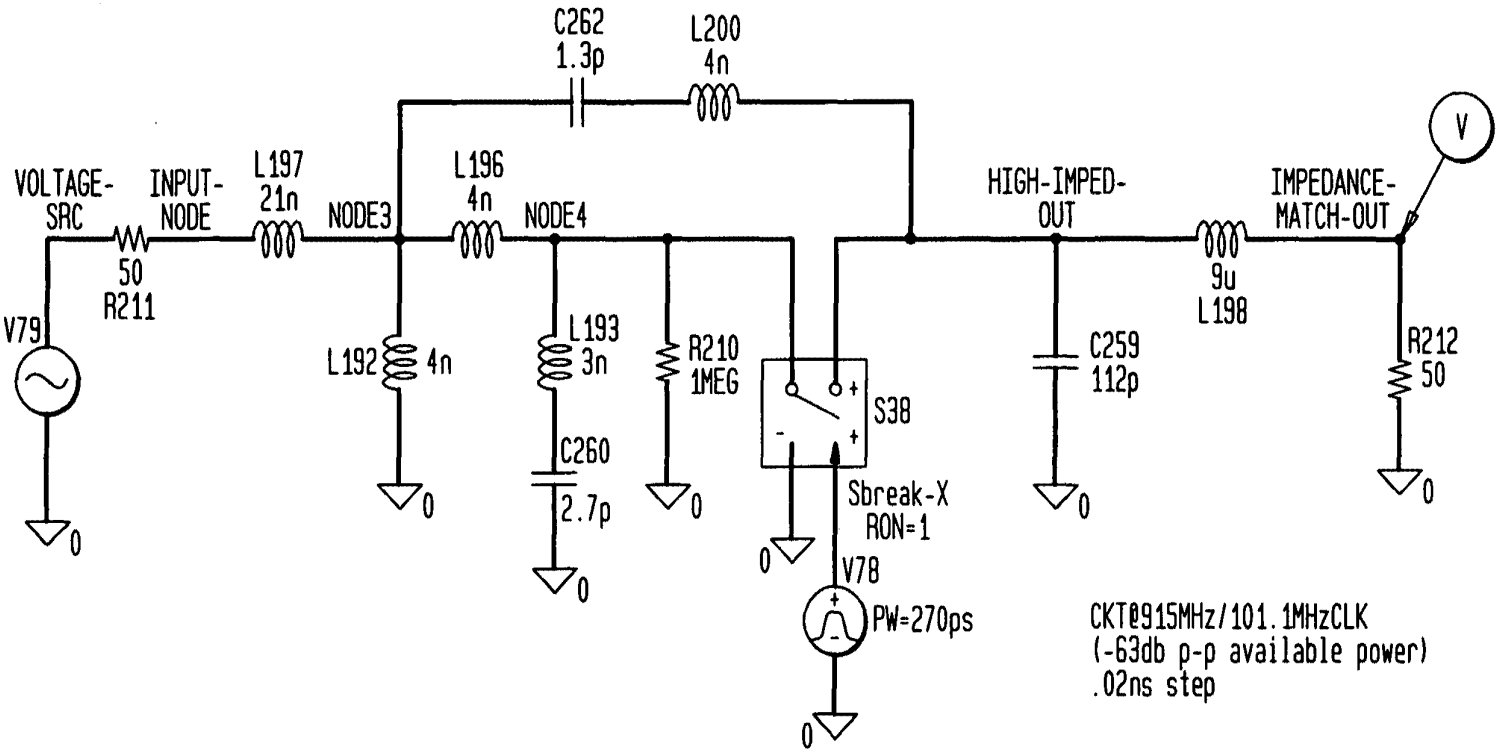

C262
1.3p
L200
4n
VOLTAGE-
SRC
INPUT-
NODE
L197
21n
NODE3
L196
4n
NODE4
HIGH-IMPED-
OUT
IMPEDANCE-
MATCH-OUT
V
50
R211
V79
L192
4n
L193
3n
C260
2.7p
R210
1MEG
S38
Sbreak-X
RON=1
V78
PW=270ps
C259
112p
9u
L198
R212
50
0
CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

FIG. 68

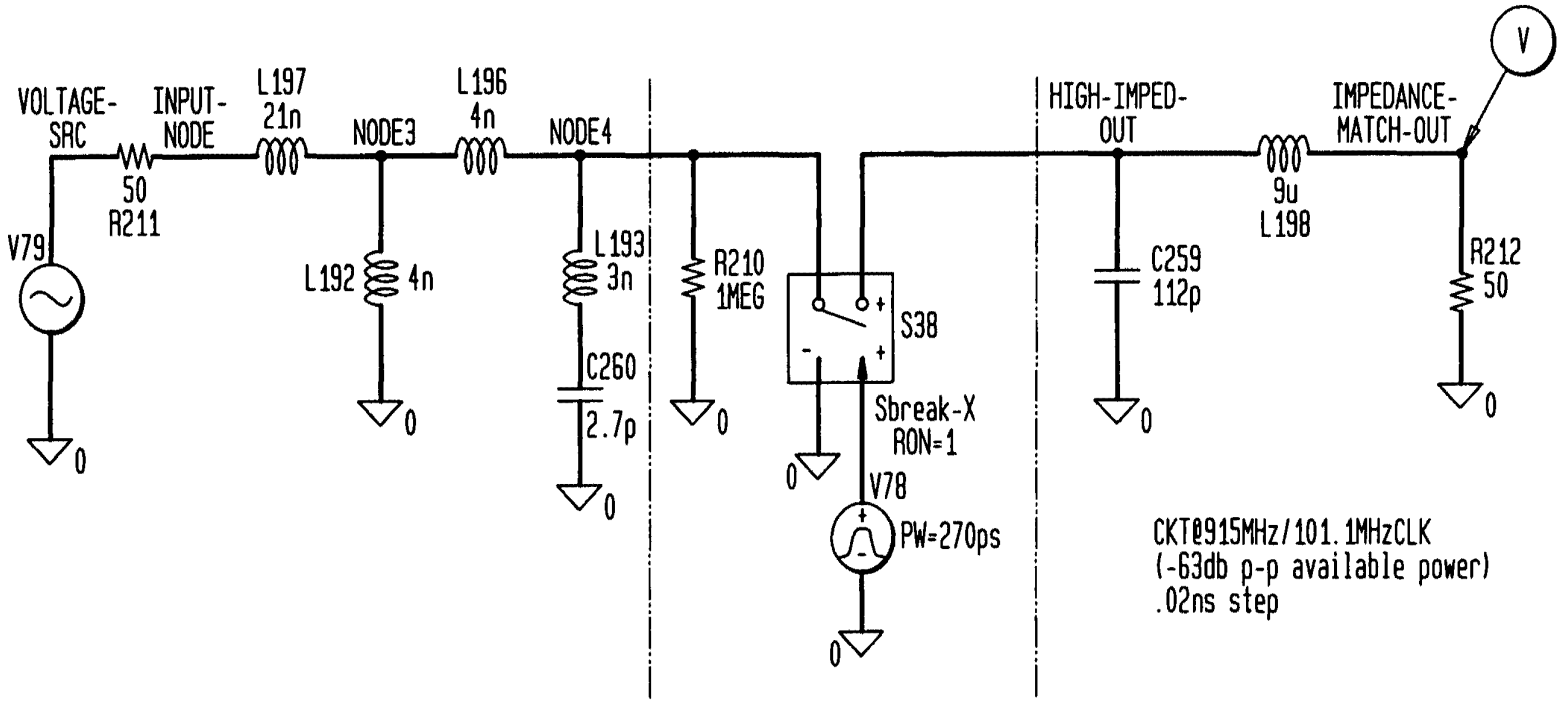
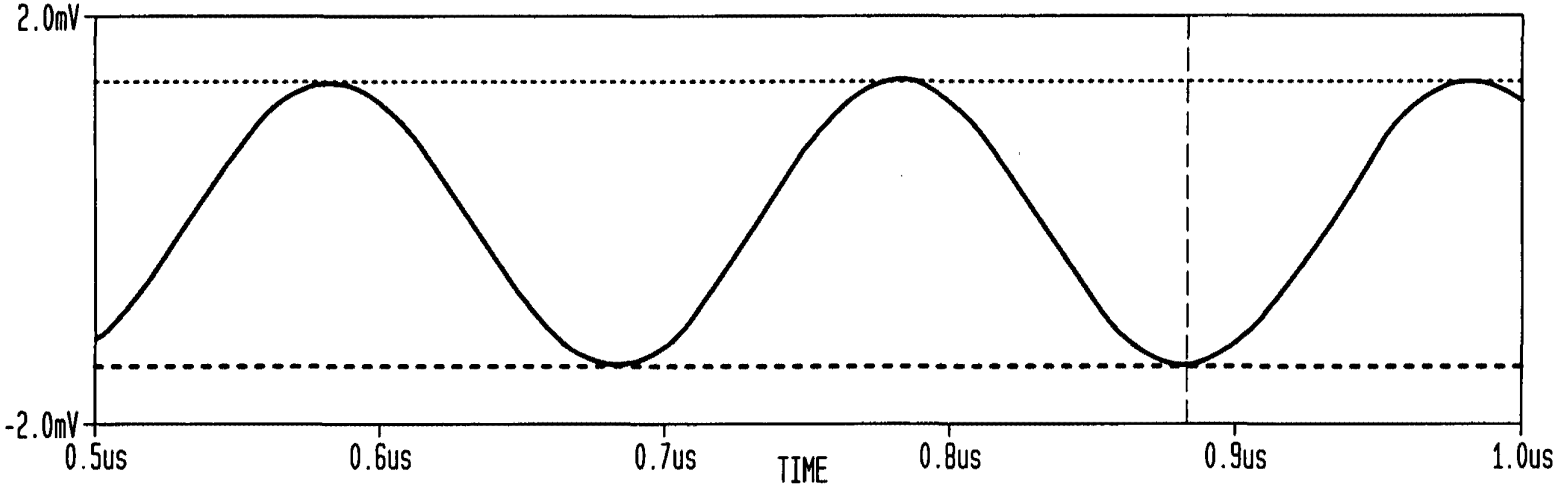
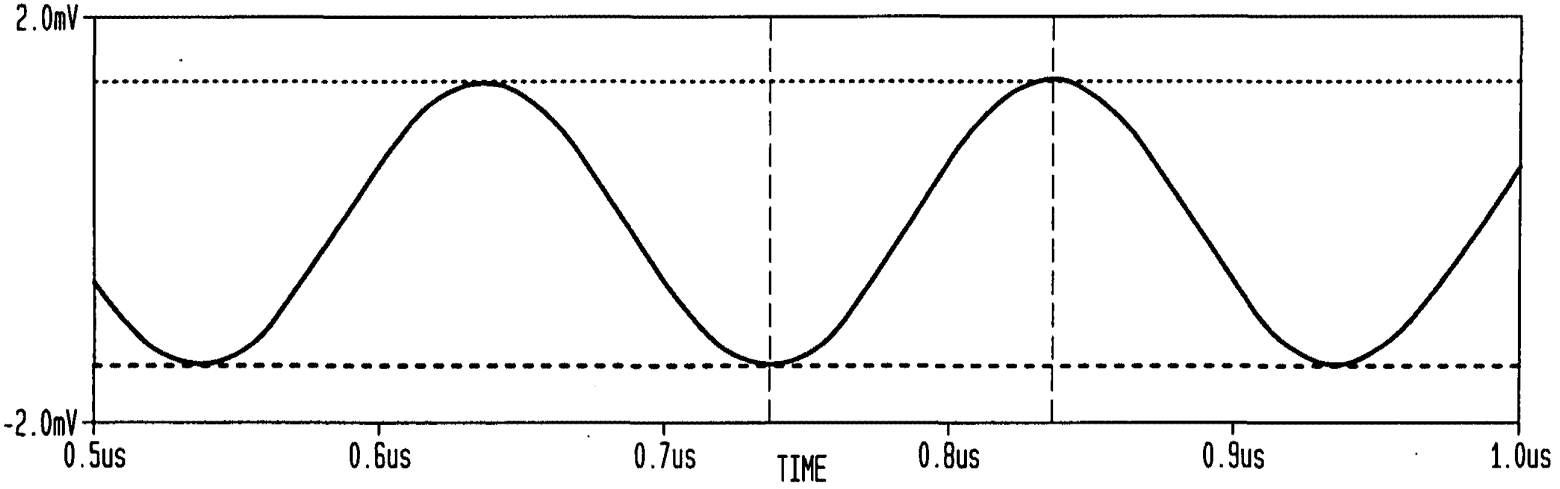

VOLTAGE-SRC
INPUT-NODE
50
R211
L197
21n
NODE3
L196
4n
NODE4
V79
L192
4n
L193
3n
C260
2.7p
R210
1MEG
S38
Sbreak-X
RON=1
V78
PW=270ps
HIGH-IMPED-OUT
C259
112p
9u
L198
IMPEDANCE-MATCH-OUT
R212
50
V
0
CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

FIG. 69A



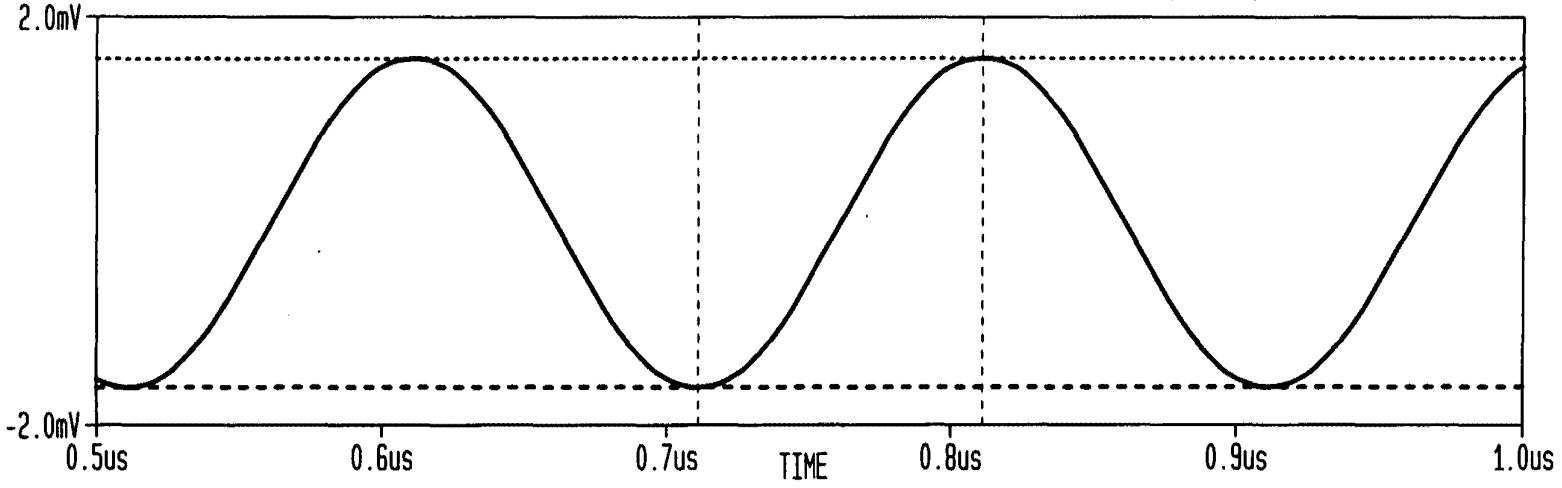
V(out1)
E1: (981.86n, 1.404m) E2: (883.04n, -1.402m) DIFF(E): (98.82n, 2.806m)
F1: (837.43n, 1.253m) F2: (738.01n, -1.252m) DIFF(F): (99.42n, 2.505m)

FIG. 69B



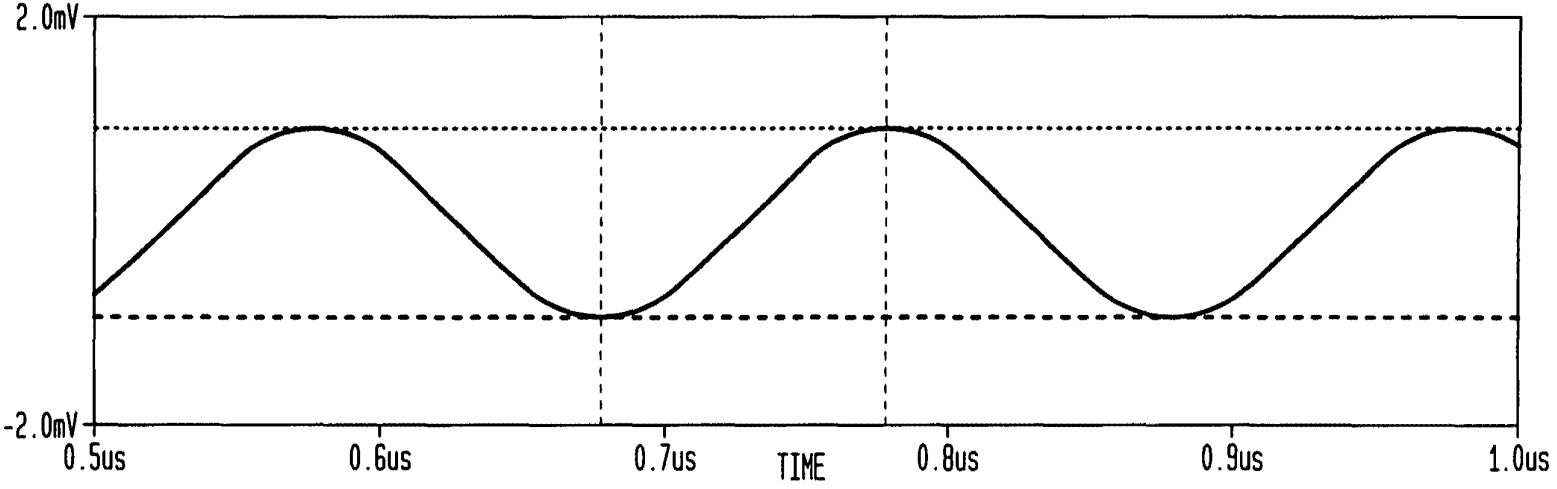
V(impedance-match-out)
E1: (981.86n, 1.404m) E2: (883.04n, -1.402m) DIFF(E): (98.82n, 2.806m)
F1: (837.43n, 1.253m) F2: (738.01n, -1.252m) DIFF(F): (99.42n, 2.505m)

FIG. 70A



V(impedance-match-out)
A1: (810.53n, 1.642m) A2: (710.52n, -1.621m) DIFF(A): (100.01n, 3.263m)
B1: (777.78n, 942.32u) B2: (677.18n, -942.51u) DIFF(B): (100.60n, 1.885m)

FIG. 70B



V(impedance-match-out)
A1: (810.53n, 1.642m) A2: (710.52n, -1.621m) DIFF(A): (100.01n, 3.263m)
B1: (777.78n, 942.32u) B2: (677.18n, -942.51u) DIFF(B): (100.60n, 1.885m)

FIG. 71A

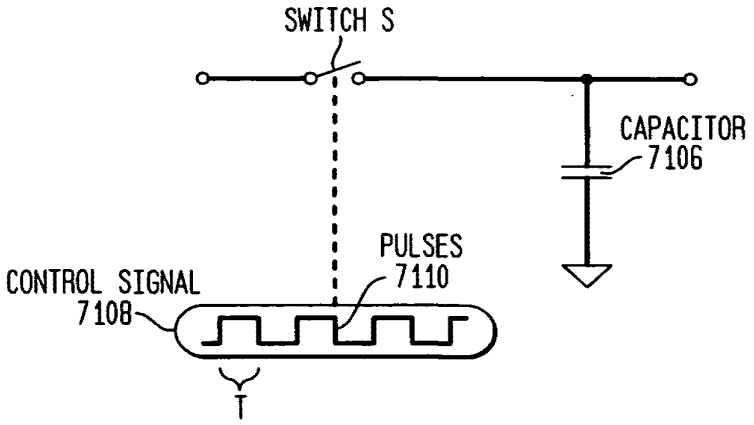


FIG. 71B

$$q=C\cdot V \qquad \text{EQ. 10}$$

$$V=A\cdot\sin(t) \qquad \text{EQ. 11}$$

$$q(t)=C\cdot A\cdot\sin(t) \qquad \text{EQ. 12}$$

$$\Delta q(t)=C\cdot A\cdot\sin(t)-C\cdot A\cdot\sin(t-T) \qquad \text{EQ. 13}$$

$$\Delta q(t)=C\cdot A\cdot(\sin(t)-\sin(t-T)) \qquad \text{EQ. 14}$$

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{EQ. 15}$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right] \qquad \text{EQ. 16}$$

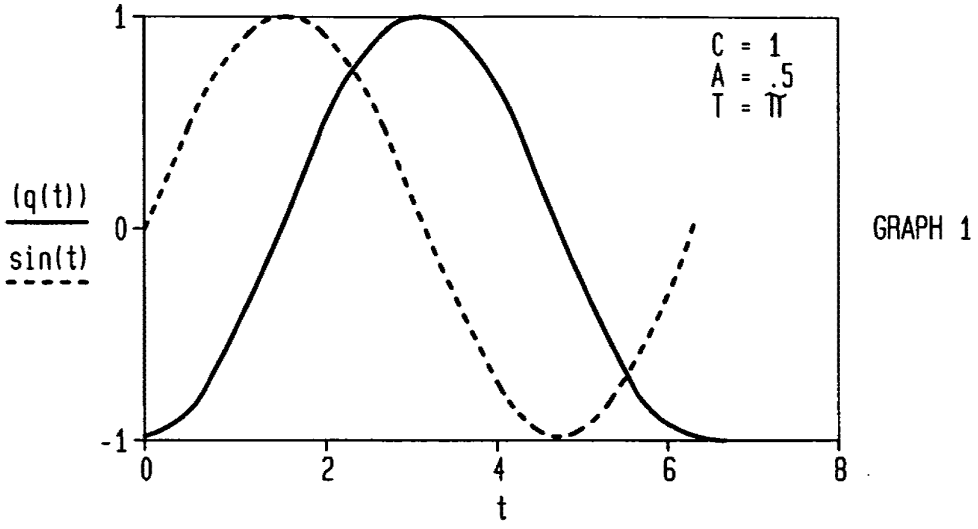
$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQ. 17}$$

$$q(t)=\int C\cdot A\cdot(\sin(t)-\sin(t-T))\,dt \qquad \text{EQ. 18}$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A \qquad \text{EQ. 19}$$

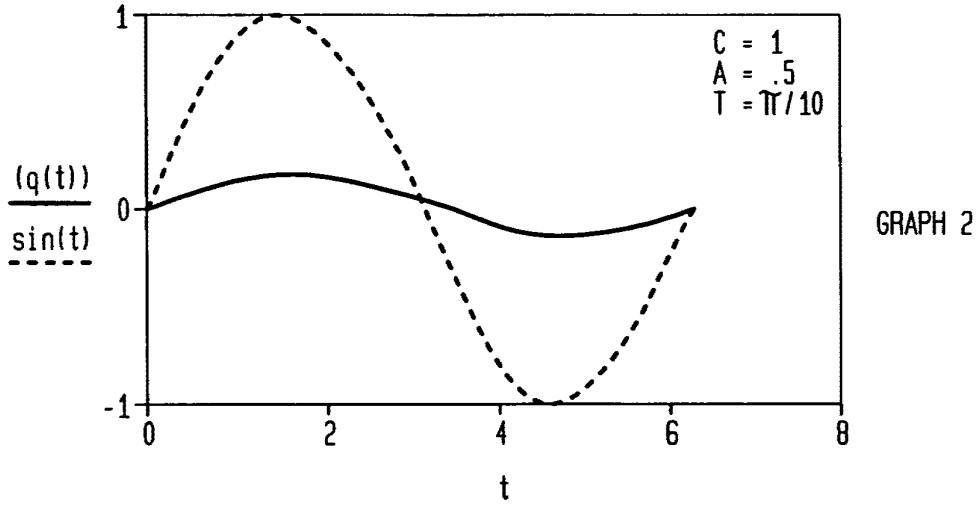
$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \qquad \text{EQ. 20}$$

FIG. 71C



GRAPH 1

FIG. 71D



GRAPH 2

FIG. 71E

POWER-CHARGE RELATIONSHIP

$q=C \cdot V$	EQ. 21
$V=q/C$	EQ. 22
$V=J/q$	EQ. 23
$J=q^2/C$	EQ. 24
$P=J/S$	EQ. 25
$P=q^2/(C \cdot S)$	EQ. 26

FIG. 71F

INSERTION LOSS

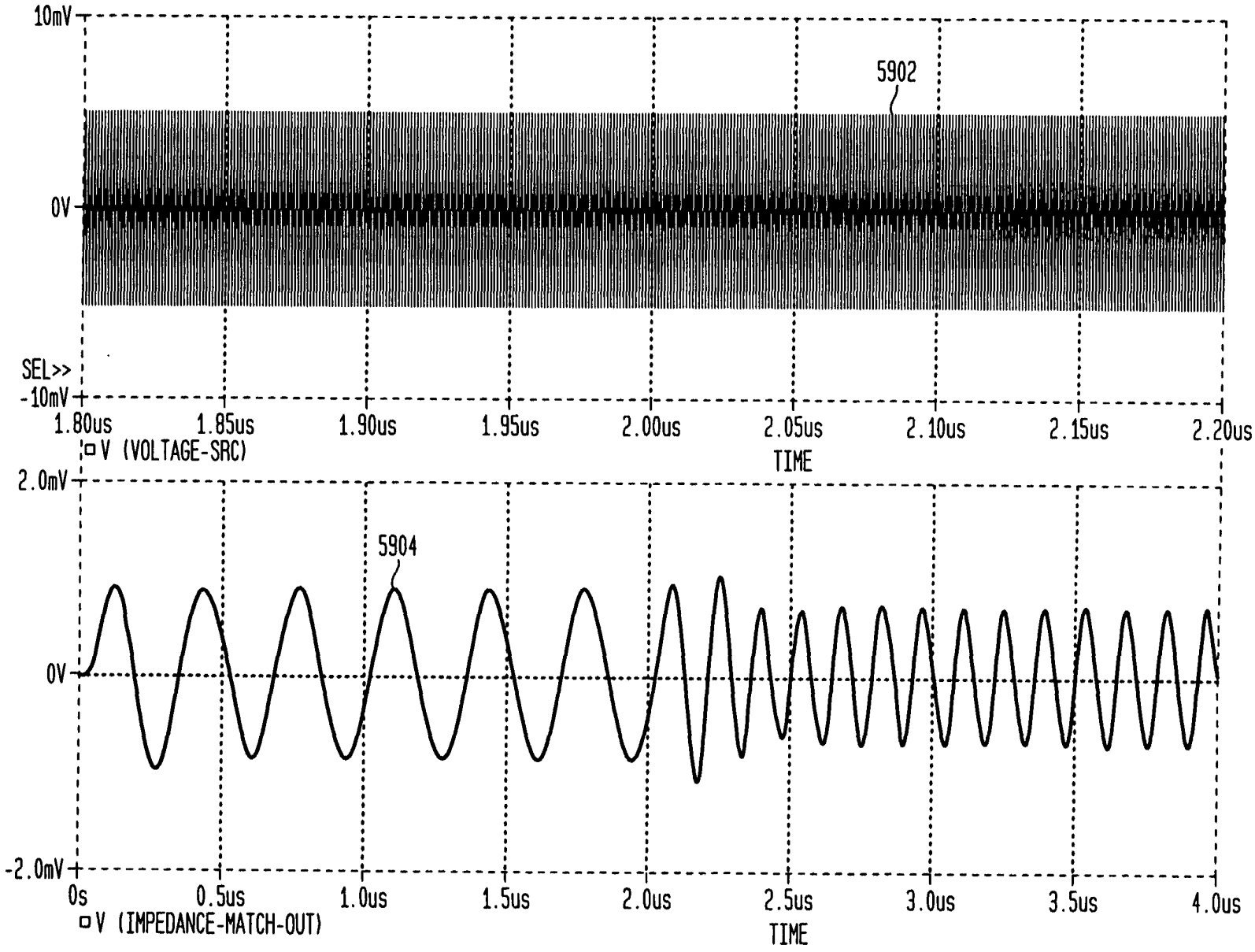
INSERTION LOSS IN dB IS EXPRESSED BY:

$$ILdB=10 \cdot \log\left(\frac{Pin}{Pout}\right) \quad \text{EQ. 27}$$

or

$$ILdB=10 \cdot \log\left[\frac{\left(\frac{Vin^2}{Rin}\right)}{\left(\frac{Vout^2}{Rout}\right)}\right] \quad \text{EQ. 28}$$

FIG. 72


10mV
0V
SEL>>
-10mV
5902
1.80us
1.85us
1.90us
1.95us
2.00us
2.05us
2.10us
2.15us
2.20us
V (VOLTAGE-SRC)
TIME
2.0mV
0V
-2.0mV
5904
0s
0.5us
1.0us
1.5us
2.0us
2.5us
3.0us
3.5us
4.0us
V (IMPEDANCE-MATCH-OUT)
TIME

Declaration for Patent Application

Docket Number: **1744.1030000**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation**, the specification of which is attached hereto unless the following box is checked:

☒ was filed on **May 10, 2000** ;
as United States Application Number **09/569,044**; and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application, which designated at least one country other than the United States listed below, and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____	_____	_____	☐ Yes ☐ No
(Application No.)	(Country)	(Day/Month/Year Filed)	
_____	_____	_____	☐ Yes ☐ No
(Application No.)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

60/195,328	**April 10, 2000**
(Application No.)	(Filing Date)
60/147,129	**August 4, 1999**
(Application No.)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or under § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56 that became available between the filing date of the prior application and the national or PCT international filing date of this application.

09/261,129	**March 3, 1999**	**Pending**
(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)
09/514,004	**February 25, 2000**	**Pending**
(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)

09/476,093 (Application No.)	January 3, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)
09/476,330 (Application No.)	January 3, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)
09/525,615 (Application No.)	March 14, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)
09/526,041 (Application No.)	March 14, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor **David F. SORRELLS**	
Signature of sole or first inventor X	Date X
Residence **Middleburg, FL**	
Citizenship **United States of America**	
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Full name of second inventor **Michael J. BULTMAN**	
Signature of second inventor X	Date X 25 Oct 00
Residence **Jacksonville, FL**	
Citizenship **United States of America**	
Post Office Address **2244 Aztec Drive West, Jacksonville, Florida 32246**	

09/476,093 (Application No.)	January 3, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)
09/476,330 (Application No.)	January 3, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)
09/525,615 (Application No.)	March 14, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)
09/526,041 (Application No.)	March 14, 2000 (Filing Date)	Pending (Status - patented, pending, abandoned)

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Full name of sole or first inventor David F. SORRELLS	
Signature of sole or first inventor X	X 10/26/00 Date
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Post Office Address 3129 Rideout Lane, Middleburg, FL 32068	
Full name of second inventor Michael J. BULTMAN	
Signature of second inventor X	X 25 Oct 00 Date
Residence Jacksonville, FL	
Citizenship United States of America	
Post Office Address 2244 Aztec Drive West, Jacksonville, Florida 32246	

Full name of third inventor **Robert W. COOK**	
Signature of third inventor X Robert W Cook	Date x 10/25/00
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Citizenship **United States of America**	
Post Office Address **1432 Roberts Road, Switzerland, Florida 32259**	
Full name of fourth inventor **Richard C. LOOKE**	
Signature of fourth inventor X R C. Looke	Date x 10/27/00
Residence **Jacksonville, FL**	
Citizenship **United States of America**	
Post Office Address **3170 Ricky Drive, Jacksonville, Florida 32223**	
Full name of fifth inventor **Charley D. MOSES, Jr.**	
Signature of fifth inventor **X**	Date **X**
Residence **Jacksonville, FL**	
Citizenship **United States of America**	
Post Office Address **4314 Naranja Drive, Jacksonville, Florida 32217**	

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SKGF Rev. 9/2/98 mac

(Supply similar information and signature for subsequent joint inventors, if any)

Full name of third inventor Robert W. COOK	
Signature of third inventor X Robert W Cook	Date x 10/25/00
Residence Switzerland, FL	
Citizenship United States of America	
Post Office Address 1432 Roberts Road, Switzerland, Florida 32259	
Full name of fourth inventor Richard C. LOOKE	
Signature of fourth inventor X	Date X
Residence Jacksonville, FL	
Citizenship United States of America	
Post Office Address 3170 Ricky Drive, Jacksonville, Florida 32223	
Full name of fifth inventor Charley D. MOSES, Jr.	
Signature of fifth inventor X Charley D. Moses	Date x 10/26/2000
Residence Jacksonville, FL	
Citizenship United States of America	
Post Office Address 4314 Naranja Drive, Jacksonville, Florida 32217	

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SE.GF Rev. 10/00

(Supply similar information and signature for subsequent joint inventors, if any)

POWER OF ATTORNEY FROM ASSIGNEE

ParkerVision, Inc., a corporation of **Florida**, having a principal place of business at **8493 Baymeadows Way, Jacksonville, FL 32256**, is assignee of the entire right, title and interest for the United States of America (as defined in 35 U.S.C. § 100), by reason of an Assignment to the Assignee executed on 1) 10-26-00; 2) 10-25-00; 3) 10-25-00; 4) 10-27-00; and 5) 10-26-00 of an invention known as **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology** (Attorney Docket No. **1744.103000**), which is disclosed and claimed in a patent application of the same title by the inventor(s) **1) David F. SORRELLS; 2) Michael J. BULTMAN; 3) Robert W. Cook; 4) Richard C. Looke; and 5) Charley D. Moses, Jr.**, (said application filed on **May 10, 2000** at the U.S. Patent and Trademark Office, having Application Number **09/569,044**).

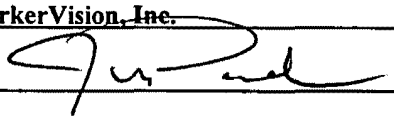
The Assignee hereby appoints the following U.S. attorneys to prosecute this application and any continuation, divisional, continuation-in-part, or reissue application thereof, and to transact all business in the U.S. Patent and Trademark Office connected therewith: Robert Greene Sterne, Esq., Reg. No. 28,912; Edward J. Kessler, Esq., Reg. No. 25,688; Jorge A. Goldstein, Esq., Reg. No. 29,021; Samuel L. Fox, Esq., Reg. No. 30,353; David K.S. Cornwell, Esq., Reg. No. 31,944; Robert W. Esmond, Esq., Reg. No. 32,893; Tracy-Gene G. Durkin, Esq., Reg. No. 32,831; Michele A. Cimbala, Esq., Reg. No. 33,851; Michael B. Ray, Esq., Reg. No. 33,997; Robert E. Sokohl, Esq., Reg. No. 36,013; Eric K. Steffe, Esq., Reg. No. 36,688, Michael Q. Lee, Esq., Reg. No. 35,239; Steven R. Ludwig, Esq., Reg. No. 36,203; John M. Covert, Esq., Reg. No. 38,759; and Linda E. Alcorn, Esq., Reg. No. 39,588. The Assignee hereby grants said attorneys the power to insert on this Power of Attorney any further identification that may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office.

Send correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
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U.S.A.

Direct phone calls to 202-371-2600.

FOR: **ParkerVision, Inc.**

SIGNATURE: X 

BY: **Jeffrey L. Parker**

TITLE: **Chairman and Chief Executive Officer**

DATE: X 10-25-00

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PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

10/28/2004 KBETEMA1 00000057 10973917

01 FC:1001 790.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/59033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2004

Application or Docket Number: 10973917

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	4	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	4 minus 20=	* 0
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	395.00	OR	BASIC FEE	790.00
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL		OR	TOTAL	790

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: (to be assigned)
SORRELLS *et al.*	Art Unit: (to be assigned)
Appl. No.: (to be assigned)	
(*Continuation of Appl. No. 09/569,044*)	Examiner: (to be assigned)
Filed: (herewith)	Atty. Docket: 1744.0330003
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**	

Preliminary Amendment Under 37 C.F.R. § 1.115

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In advance of prosecution, Applicants submit the following amendments and remarks. This Preliminary Amendment is provided in the following format:

(A) Each section begins on a separate sheet;

(B) Starting on a separate sheet, amendments to the specification by presenting replacement paragraphs marked up to show changes made;

(C) Starting on a separate sheet, a complete listing of all of the claims:

- in ascending order;

- with status identifiers; and

- with markings in the currently amended claims;

(D) Starting on a separate sheet, the Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent

abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Specification

Please replace lines 10-25 on page one of the specification with the following paragraphs:

This is a continuation application of U.S. Application No. 09/569,044 (Atty. Dkt. No. 1744.0330002), titled, "Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology," filed May 10, 2000, (allowed), incorporated herein by reference in its entirety, which is a continuation-in-part application of the following ~~pending~~ U.S. applications, all of which are herein incorporated by reference in their entireties:

"Additional Applications of Frequency Translation Technology," Ser. No. 09/261,129, filed March 3, 1999, Attorney Docket No. 1744.0140001, now U.S. Patent No. 6,370,371.

"Universal Frequency Translation and Applications of Same," Ser. No. 09/514,004, filed February 25, 2000, Attorney Docket No. 1744.0140004, now abandoned.

"Family Radio System with Multi-Mode and Multi-Band Functionality," Ser. No. 09/476,093, filed January 3, 2000, Attorney Docket No. 1744.0260001.

"Multi-Mode, Multi-Band Communications System," Ser. No. 09/476,330, filed January 3, 2000, Attorney Docket No. 1744.0330001, now U.S. Patent No. 6,704,549.

"Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, filed March 14, 2000, Attorney Docket No. 1744.0450003.

"DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Ser. No. 09/526,041, filed March 14, 2000, Attorney Docket No. 1744.0880000.

Please replace lines 1-7 on page two of the specification with the following paragraph:

~~This application~~ U.S. Application No. 09/569,044 (Atty. Dkt. No. 1744.0330002), titled, "Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology," filed May 10, 2000, (allowed), also claims the benefit of U.S. Provisional Application "Wireless Telephone Using Universal Frequency and Translation," Ser. No. 60/195,328, filed April 10, 2000, Attorney Docket No. 1744.0070000, and U.S. Provisional Application "Wireless Local Area Network (LAN) Using Universal Frequency Translation Technology," Ser. No. 60/147,129, filed August 4, 1999, Attorney Docket No. 1744.0630000, both of which are herein incorporated by reference in their entireties.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1-4. (*cancelled*)

5. (*new*) An apparatus capable of performing simultaneous multi-platform operations, comprising:

at least one multi-platform module including a plurality of transceivers each having at least one frequency translating module; and

a control module for enabling the at least one multi-platform module to communicate with at least one of a plurality of communication links, the control module including a plurality of protocol/standard sub-modules;

wherein a first protocol/standard sub-module operates a first transceiver in conformance with a first protocol/standard combination; and

wherein a second protocol/standard sub-module simultaneously operates a second transceiver in conformance with a second protocol/standard combination.

6. (*new*) The apparatus of claim 5, wherein the control module enables the at least one multi-platform module to simultaneously communicate with a quantity of the plurality of communication links by employing an equal quantity of the plurality of standard/protocol sub-modules.

7. (*new*) The apparatus of claim 5, wherein the at least one multi-platform module includes a plurality of receivers and a plurality of transmitters each having at least one frequency translating module.

8. (*new*) The apparatus of claim 5, wherein the first protocol/standard combination is different from the second protocol/standard combination.

9. (*new*) The apparatus of claim 5, wherein the first and second protocol/standard sub-modules contain respective first and second implementation and operational instructions for the at least one multi-platform sub-module.

10. (*new*) The apparatus of claim 9, wherein the first and second implementation and operational instructions include respective first and second protocol stacks and specification information about the first and second protocol architectures.

11. (*new*) The apparatus of claim 9, wherein the first and second implementation and operational instructions can be updated, upgraded, replaced, or modified to provide the at least one multi-platform sub-module with additional functionality.

12. (*new*) The apparatus of claim 5, wherein the first and second protocol/standard sub-modules operate the first and second transceivers in conformance

with respective requirements of the first and second protocols and operating environments.

13. (*new*) The apparatus of claim 12, wherein the first and second operating environments include at least one of respective standards, content encoders and decoders, and protocol gateways.

14. (*new*) A method for performing simultaneous multi-platform operations, comprising:

(1) controlling at least one multi-platform module to communicate with at least one of a plurality of communication links using a control module having a plurality of standard/protocol sub-modules, wherein the at least one multi-platform module includes a plurality of transceivers each having at least one frequency translation module;

(2) operating a first transceiver in conformance with a first protocol/standard combination using a first standard/protocol sub-module; and

(3) simultaneously operating a second transceiver in conformance with a second protocol/standard combination using a second standard/protocol sub-module.

15. (*new*) The method of claim 14, wherein step (1) comprises:

controlling the at least one multi-platform module to simultaneously communicate with a quantity of the plurality of communications links by employing an equal quantity of the plurality of standard/protocol sub-modules.

16. (*new*) The method of claim 14, wherein step (1) comprises:

controlling at least one multi-platform module to communicate with at least one of the plurality of communication links using the control module, the at least one multi-platform module including a plurality of receivers and a plurality of transmitters each having at least one frequency translating module.

17. (*new*) The method of claim 14, wherein step (3) comprises:

simultaneously operating the second transceiver in conformance with a second protocol/standard combination that is different from the first protocol/standard combination.

18. (*new*) The method of claim 14, wherein steps (2) and (3) comprise:

programming the first and second protocol/standard sub-modules with respective first and second implementation and operational instructions for the at least one multi-platform sub-module.

19. (*new*) The method of claim 18, wherein steps (2) and (3) further comprise:

programming the first and second protocol/standard sub-modules with respective first and second protocol stacks and specification information about the first and second protocol architectures.

20. (*new*) The method of claim 18, wherein steps (2) and (3) further comprise:

updating, upgrading, replacing, or modifying the first and second implementation and operational instructions to provide the at least one multi-platform sub-module with additional functionality.

21. (*new*) The method of claim 14, wherein steps (2) and (3) comprise:

simultaneously operating the first and second transceivers in conformance with respective requirements of the first and second protocols and operating environments.

22. (*new*) The method of claim 21, wherein steps (2) and (3) further comprise:

simultaneously operating the first and second transceivers in conformance with respective standards, content encoders and decoders, and protocol gateways of the first and second protocols and operating environments.

Remarks

Upon entry of the foregoing amendment, claims 5-22 are pending in the application, with claims 5 and 14 being the independent claims. Claims 1-4 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. New claims 5-22 are sought to be added. Lines 10-25 on page one of the specification and lines 1-7 on page two of the specification are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Conclusion

Prompt and favorable consideration of this Preliminary Amendment is respectfully requested. Applicants believe the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 10/27/04

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323073_1.DOC

APPLICATION DATA SHEET

Electronic Version v14
Stylesheet Version v14.0

Title of Invention	Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology

Application Type: regular, utility
Attorney Docket Number: 1744.0330003

Correspondence address:

Customer Number: 26111 *26111*

Continuing Data:

This is a Continuation of US application number 09/569,044, filed 2000-05-10 , now allowed.

US application number 09/569,044, filed 2000-05-10 is a Continuation-in-part of US application number 09/261,129, filed 1999-03-03 , now US patent number 6,370,371, issued 2002-04-09.

US application number 09/569,044, filed 2000-05-10 is a Continuation-in-part of US application number 09/514,004, filed 2000-02-25 , now abandoned.

US application number 09/569,044, filed 2000-05-10 is a Continuation-in-part of US application number 09/476,093, filed 2000-01-03 , now pending.

US application number 09/569,044, filed 2000-05-10 is a Continuation-in-part of US application number 09/476,330, filed 2000-01-03 , now US patent number 6,704,549, issued 2004-03-09.

US application number 09/569,044, filed 2000-05-10 is a Continuation-in-part of US application number 09/525,615, filed 2000-03-14 , now allowed.

US application number 09/569,044, filed 2000-05-10 is a Continuation-in-part of US application number 09/526,041, filed 2000-03-14 , now allowed.

US application number 09/569,044, filed 2000-05-10 is a Non-Provisional of US application number 60/195,328, filed 2000-04-10 , now abandoned.

US application number 09/569,044, filed 2000-05-10 is a Non-Provisional of US application number 60/147,129, filed 1999-08-04 , now abandoned.

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Phone:
Fax:
E-mail:

Attorney Information:

practitioner(s) at Customer Number:

28393 *28393*

as our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business

in the United States Patent and Trademark Office connected therewith.

Publication Information:
Suggested Figure for Publication -
Suggested Classification -
Suggested Technology Center -
Total Number of Drawing Sheets - 92

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Phone:	
Fax:	
E-mail:	

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2004

Application or Docket Number: 10973917

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	18	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	18 minus 20=	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	395.00	OR	BASIC FEE	790.00
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL		OR	TOTAL	790

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PTO/SB/07 (08-03)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

Substitute for Form PTO-1360
(For use with Form PTO/SB/06)

Application Number: 10/973,917
Filing Date:
Applicant(s):

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT		*		*		*	
	Indep	Depend	Indep	Depend	Indep	Depend	Indep	Depend	Indep	Depend	Indep	Depend
1	/		X		X		51					
2		/		X		X	52					
3		/		X		X	53					
4	/		X				54					
5			/		/	X	55					
6				/		/	56					
7				/		/	57					
8				/		/	58					
9				/		/	59					
10				/		/	60					
11				/		/	61					
12				/		/	62					
13				/		/	63					
14			/		/		64					
15				/		/	65					
16				/		/	66					
17				/		/	67					
18				/		/	68					
19				/		/	69					
20				/		/	70					
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46							96					
47							97					
48							98					
49							99					
50							100					
Total Indep	2		2		2		Total Indep					
Total Depend	2		16		16		Total Depend					
Total Claims	4		18		18		Total Claims					

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Cancel clms 1-4

Add new clms 5-22

Amdtdt. 3/30/05 - 5- Previously presented

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/973,917	10/27/2004	David F. Sorrells	1744.0330003

CONFIRMATION NO. 3273

26111
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1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000014691474

Date Mailed: 12/08/2004

NOTICE OF OMITTED ITEM(S) IN A NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

A filing date has been accorded to the above-identified nonprovisional application papers; however, the following item(s) appear to have been omitted from the application:

- Figure(s) **20A-1** described in the specification.

I. Should applicant contend that the above-noted omitted item(s) was in fact deposited in the U.S. Patent and Trademark Office (USPTO) with the nonprovisional application papers, a copy of this Notice and a petition (and $130.00 petition fee *(37 CFR 1.17(h))*) with evidence of such deposit **must** be filed within **TWO MONTHS** of the date of this Notice. The petition fee will be refunded if is determined that the item(s) was received by the USPTO.

II. Should applicant desire to supply the omitted item(s) and accept the date that such omitted item(s) was filed in the USPTO as the filing date of the above-identified application, a copy of this Notice, the omitted item(s) (with a supplemental oath or declaration in compliance with 37 CFR 1.63 and 1.64 referring to such items), and a petition under 37 CFR 1.182 (with the $130.00 petition fee *(37 CFR 1.17(h))* requesting the later filing date **must** be filed within **TWO MONTHS** of the date of this Notice.

Applicant is advised that generally the filing fee required for an application is the filing fee in effect on the filing date accorded the application and that payment of the requisite basic filing fee on a date later than the filing date of the application requires payment of a surcharge (37 CFR 1.16(e)). To avoid processing delays and payment of a surcharge, applicant should submit any balance due for the requisite filing fee based on the later filing date being requested when submitting the omitted items(s) and the petition (and petition fee) requesting the later filing date.

III. The failure to file a petition (and petition fee) under the above options (I) or (II) within **TWO MONTHS** of the date of this Notice (37 CFR 1.181(f)) will be treated as a constructive acceptance by the applicant of the application as deposited in the USPTO. **THIS TWO MONTH PERIOD IS NOT EXTENDABLE UNDER 37 CFR 1.136(a) or (b)**. In the absence of a timely filed petition in reply to this Notice, the application will maintain a filing date as of the date of deposit of the application papers in the USPTO, and original application papers (*i.e.*, the original disclosure of the invention) will include only those application papers present in the USPTO on the date of deposit.

In the event that applicant elects not to take action pursuant to options (I) or (II) above (thereby constructively electing option (III)), amendment of the specification to renumber the pages consecutively and cancel incomplete sentences caused by any omitted page(s), and/or amendment of the specification to cancel all references to any omitted drawing(s), relabel the drawing figures to be numbered consecutively (if necessary), and correct the

references in the specification to the drawing figures to correspond with any relabeled drawing figures, is required. A copy of the drawing figures showing the proposed changes in red ink should accompany with any drawing changes . Such amendment and/or correction to the drawing figures, if necessary, should be by way of preliminary amendment submitted prior to the first Office action to avoid delays in the prosecution of the application.

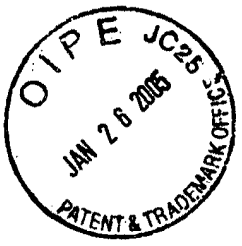
Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

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+Admitted only in Virginia
•Practice Limited to Federal Agencies

January 26, 2005

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop Missing Parts

Re: U.S. Nonprovisional Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS et al.
Our Ref: 1744.0330003

Sir:

In reply to the "Notice of Omitted Item(s) in a Nonprovisional Application," dated December 8, 2004, Applicants submit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. Credit Card Payment Form (PTO-2038);

2. A copy of the Notice of Omitted Item(s);

3. Petition Fee Transmittal Form (PTO/SB/17p);

4. Petition to Accept Omitted Item(s) in a Nonprovisional Application under 37 C.F.R. § 1.53(e);

5. A copy of a return receipt postcard date-stamped on May 8, 2001 by the USPTO in support of Applicants' Petition;

6. A copy of an SKGF cover letter as submitted on May 8, 2001, in support of Applicants' Petition;

7. A copy of the Request to Approve Proposed Drawing Corrections as submitted on May 8, 2001, in support of Applicants' Petition;

8. A copy of a drawing sheet showing FIG. 20A-1, as submitted on May 8, 2001 in support of Applicants' Petition;

9. One new drawing sheet (FIG. 20A-1); and

10. One return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/NDD/sjc
Enclosures

351563_1.DOC

OIPE JAN 26 2005 PATENT & TRADEMARK OFFICE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/973,917	10/27/2004	David F. Sorrells	1744.0330003

CONFIRMATION NO. 3273

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STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000014691474

Date Mailed: 12/08/2004

NOTICE OF OMITTED ITEM(S) IN A NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

A filing date has been accorded to the above-identified nonprovisional application papers; however, the following item(s) appear to have been omitted from the application:

- Figure(s) **20A-1** described in the specification.

I. Should applicant contend that the above-noted omitted item(s) was in fact deposited in the U.S. Patent and Trademark Office (USPTO) with the nonprovisional application papers, a copy of this Notice and a petition (and $130.00 petition fee *(37 CFR 1.17(h))*) with evidence of such deposit **must** be filed within **TWO MONTHS** of the date of this Notice. The petition fee will be refunded if is determined that the item(s) was received by the USPTO.

II. Should applicant desire to supply the omitted item(s) and accept the date that such omitted item(s) was filed in the USPTO as the filing date of the above-identified application, a copy of this Notice, the omitted item(s) (with a supplemental oath or declaration in compliance with 37 CFR 1.63 and 1.64 referring to such items), and a petition under 37 CFR 1.182 (with the $130.00 petition fee *(37 CFR 1.17(h))* requesting the later filing date **must** be filed within **TWO MONTHS** of the date of this Notice.

Applicant is advised that generally the filing fee required for an application is the filing fee in effect on the filing date accorded the application and that payment of the requisite basic filing fee on a date later than the filing date of the application requires payment of a surcharge (37 CFR 1.16(e)). To avoid processing delays and payment of a surcharge, applicant should submit any balance due for the requisite filing fee based on the later filing date being requested when submitting the omitted items(s) and the petition (and petition fee) requesting the later filing date.

III. The failure to file a petition (and petition fee) under the above options (I) or (II) within **TWO MONTHS** of the date of this Notice (37 CFR 1.181(f)) will be treated as a constructive acceptance by the applicant of the application as deposited in the USPTO. **THIS TWO MONTH PERIOD IS NOT EXTENDABLE UNDER 37 CFR 1.136(a) or (b)**. In the absence of a timely filed petition in reply to this Notice, the application will maintain a filing date as of the date of deposit of the application papers in the USPTO, and original application papers (*i.e.*, the original disclosure of the invention) will include only those application papers present in the USPTO on the date of deposit.

In the event that applicant elects not to take action pursuant to options (I) or (II) above (thereby constructively electing option (III)), amendment of the specification to renumber the pages consecutively and cancel incomplete sentences caused by any omitted page(s), and/or amendment of the specification to cancel all references to any omitted drawing(s), relabel the drawing figures to be numbered consecutively (if necessary), and correct the

references in the specification to the drawing figures to correspond with any relabeled drawing figures, is required. A copy of the drawing figures showing the proposed changes in red ink should accompany with any drawing changes . Such amendment and/or correction to the drawing figures, if necessary, should be by way of preliminary amendment submitted prior to the first Office action to avoid delays in the prosecution of the application.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

OIPE JC26
JAN 26 2005
PATENT & TRADEMARK OFFICE

COPY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.
Sorrells *et al.*	Art Unit: 2682
Appl. No. 09/569,044	Examiner: Lester Kinkaid
Filed: May 10, 2000	Atty. Docket: 1744.0330002 (Formerly 1744.1030000)

For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**

Request to Approve Proposed Drawing Corrections

Commissioner for Patents
Washington, D.C. 20231

Sir:

Attached is 1 drawing sheet, showing Figure 20A-1. Applicants request that the Examiner add the figure to the application. Applicants inadvertently omitted the figure from the original filing. However, the figure is fully supported and disclosed in the specification. Applicants refer the Examiner to page 6, line 8, and page 18, lines 10 through page 19, line 7. Applicants assert that addition of this figure adds no new matter to the application and respectfully request that the Examiner approve this change.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 5/5/01

1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

0330002.drwg

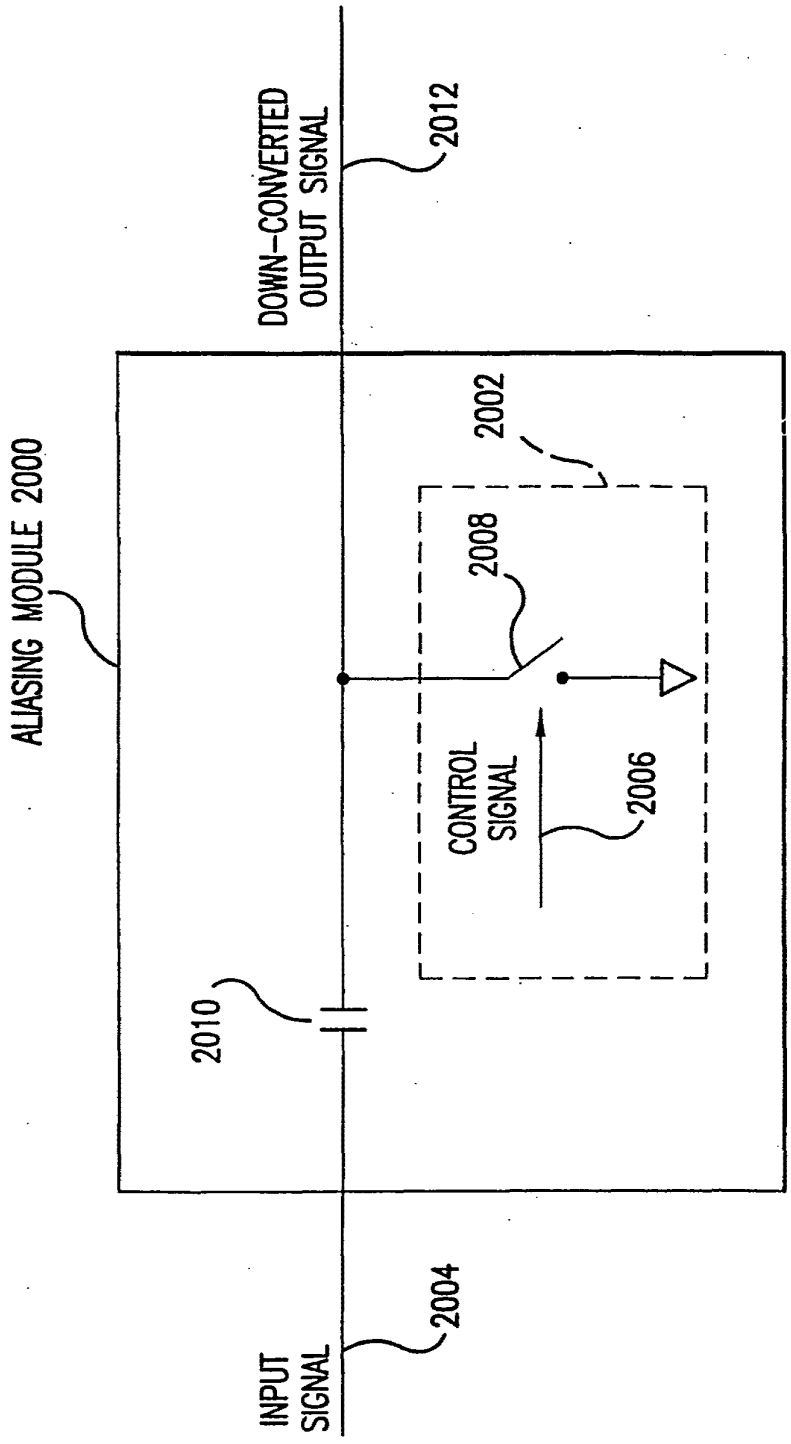

DOWN-CONVERTED OUTPUT SIGNAL
2012
ALIASING MODULE 2000
2002
2008
CONTROL SIGNAL
2006
2010
INPUT SIGNAL
2004

FIG. 20A-1

JAN 26 2005
PATENT & TRADEMARK OFFICE

PTO/SB/17p (11-04)
Approved for use through 07/31/2007: OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FEE
Under 37 CFR 1.17(f), (g) & (h)
TRANSMITTAL
(Fees are subject to annual revision)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number	10/973,917
Filing Date	October 27, 2004
First Named Inventor	David F. SORRELLS
Art Unit	(to be assigned)
Examiner Name	2661
Attorney Docket Number	1744.0330003

Enclosed is a petition filed under 37 CFR 1.53(e) that requires a processing fee (37 CFR 1.17(f), (g), or (h)). Payment of $ 400.00 is enclosed.

This form should be included with the above-mentioned petition and faxed or mailed to the Office using the appropriate Mail Stop (e.g., Mail Stop Petition), if applicable. *For transmittal of processing fees under 37 CFR 1.17(i), see form PTO/SB/17i.*

Payment of Fees (small entity amounts are NOT available for the petition fees)

☒ The Commissioner is hereby authorized to charge the following fees to Deposit Account No. 19-0036:
☐ petition fee under 37 CFR 1.17(f), (g) or (h) ☒ any deficiency of fees and credit of any overpayments
Enclose a duplicative copy of this form for fee processing.

☐ Check in the amount of $_____ is enclosed.

☒ Payment by credit card (Form PTO-2038 or equivalent enclosed). Do not provide credit card information on this form.

Petition Fees under 37 CFR 1.17(f): Fee $400 Fee Code 1462
For petitions filed under:
§ 1.53(e) - to accord a filing date.
§ 1.57(a) - to accord a filing date.
§ 1.182 - for decision on a question not specifically provided for.
§ 1.183 - to suspend the rules.
§ 1.378(e) - for reconsideration of decision on petition refusing to accept delayed payment of maintenance fee in an expired patent.
§ 1.741(b) - to accord a filing date to an application under § 1.740 for extension of a patent term.

Petition Fees under 37 CFR 1.17(g): Fee $200 Fee Code 1463
For petitions filed under:
§ 1.12 - for access to an assignment record.
§ 1.14 - for access to an application.
§ 1.47 - for filing by other than all the inventors or a person not the inventor.
§ 1.59 - for expungement of information.
§ 1.103(a) - to suspend action in an application.
§ 1.136(b) - for review of a request for extension of time when the provisions of section 1.136(a) are not available.
§ 1.295 - for review of refusal to publish a statutory invention registration.
§ 1.296 - to withdraw a request for publication of a statutory invention registration filed on or after the date the notice of intent to publish issued.
§ 1.377 - for review of decision refusing to accept and record payment of a maintenance fee filed prior to expiration of a patent.
§ 1.550(c) - for patent owner requests for extension of time in ex parte reexamination proceedings.
§ 1.956 - for patent owner requests for extension of time in inter partes reexamination proceedings.
§ 5.12 - for expedited handling of a foreign filing license.
§ 5.15 - for changing the scope of a license.
§ 5.25 - for retroactive license.

Petition Fees under 37 CFR 1.17(h): Fee $130 Fee Code 1464
For petitions filed under:
§ 1.19(g) - to request documents in a form other than that provided in this part.
§ 1.84 - for accepting color drawings or photographs.
§ 1.91 - for entry of a model or exhibit.
§ 1.102(d) - to make an application special.
§ 1.138(c) - to expressly abandon an application to avoid publication.
§ 1.313 - to withdraw an application from issue.
§ 1.314 - to defer issuance of a patent.

Signature	11/26/05 Date
Michael O. Lee Typed or printed name	35,239 Registration No., if applicable

This collection of information is required by 37 CFR 1.17. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

OIPE JC26 JAN 26 2005 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
SORRELLS *et. al.*
Application No.: 10/973,917
Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**

Confirmation No.: 3273
Art Unit: 2661
Examiner: (to be assigned)
Atty. Docket: 1744.0330003

Petition to Accept Omitted Item(s) in a Nonprovisional Application under 37 C.F.R. § 1.53(e)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Attn: Mail Stop Missing Parts

Sir:

In response to the Notice of Omitted Item(s) in a Nonprovisional Application mailed December 8, 2004, Applicants submit herewith a new drawing sheet (FIG. 20A-1) and the petition fee set forth in 37 C.F.R. § 1.17(f) in the amount of $400.00.

Applicants assert that FIG. 20A-1, identified in the Notice as apparently having been omitted from the instant application, was in fact deposited in the U.S. Patent and Trademark Office (USPTO) on May 8, 2001, in parent Application No. 09/569,044, which was incorporated by reference in its entirety upon filing of the instant application on October 27, 2004.

As evidence of this deposit, enclosed is a copy of a return receipt postcard evidencing receipt by the USPTO on May 8, 2001, of a Request to Approve Proposed Drawing Corrections with a drawing sheet showing FIG. 20A-1 attached thereto. Also enclosed are copies of an SKGF cover letter, the Request to Approve Proposed Drawing

01/28/2005 AADOF01 00000058 10973917
01 FC:1462 400.00 OP

Corrections, and the attached drawing sheet showing FIG. 20A-1, as submitted on May 8, 2001.

Accordingly, Applicants respectfully request that FIG. 20A-1 be accepted and accorded the filing date of the instant application. If the Examiner believes, for any reason, that personal communication will expedite this matter, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

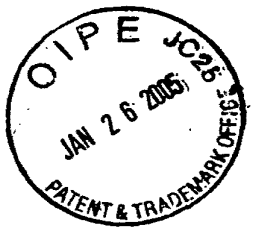
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 1/26/05

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Washington, D.C. 20005-3934
(202) 371-2600

357768_1.DOC



COPY

		Due Date:	N/A
Applicant:	David Sorrells *et al.*	**Art Unit:**	2682
		Examiner:	Lester Kinkaid
Application No.:	09/569,044	**Docket:**	1744.0330002 (formerly 1744.1030000)
Filed:	May 10, 2000	**Atty:**	MQL/WRS

For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**

When receipt stamp is placed hereon, the USPTO acknowledges receipt of the following documents:

1. SKG&F Cover Letter (in duplicate);
2. Change of Attorney Docket Number;
3. Request to Approve Proposed Drawing Corrections;
4. Request for Corrected Official Filing Receipt; and
5. Return postcard.

PLEASE DATE STAMP AND RETURN TO OUR COURIER



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ATTORNEYS AT LAW
1100 NEW YORK AVENUE, N.W. • WASHINGTON, D.C. 20005-3934
PHONE: (202) 371-2600 • FACSIMILE: (202) 371-2540 • www.skgf.com

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*LIMITED TO MATTERS AND PROCEEDINGS BEFORE FEDERAL COURTS & AGENCIES
**REGISTERED PATENT AGENT
***SENIOR COUNSEL

WRITER'S DIRECT NUMBER:
(202) 371-2674
INTERNET ADDRESS:
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OIPE JAN 26 2005 PATENT & TRADEMARK OFFICE

May 8, 2001

COPY

Commissioner for Patents
Washington, D.C. 20231

Re: U.S. Utility Patent Application
Appl. No. 09/569,044; Filed: May 10, 2000
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: Sorrells *et al.*
Our Ref: 1744.0330002 (formerly 1744.1030000)

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Change of Attorney Docket Number;

2. Request to Approve Proposed Drawing Corrections;

3. Request for Corrected Official Filing Receipt; and

4. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. A duplicate copy of this letter is enclosed.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

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PATENT & TRADEMARK OFFICE JAN 26 2005 OIPE

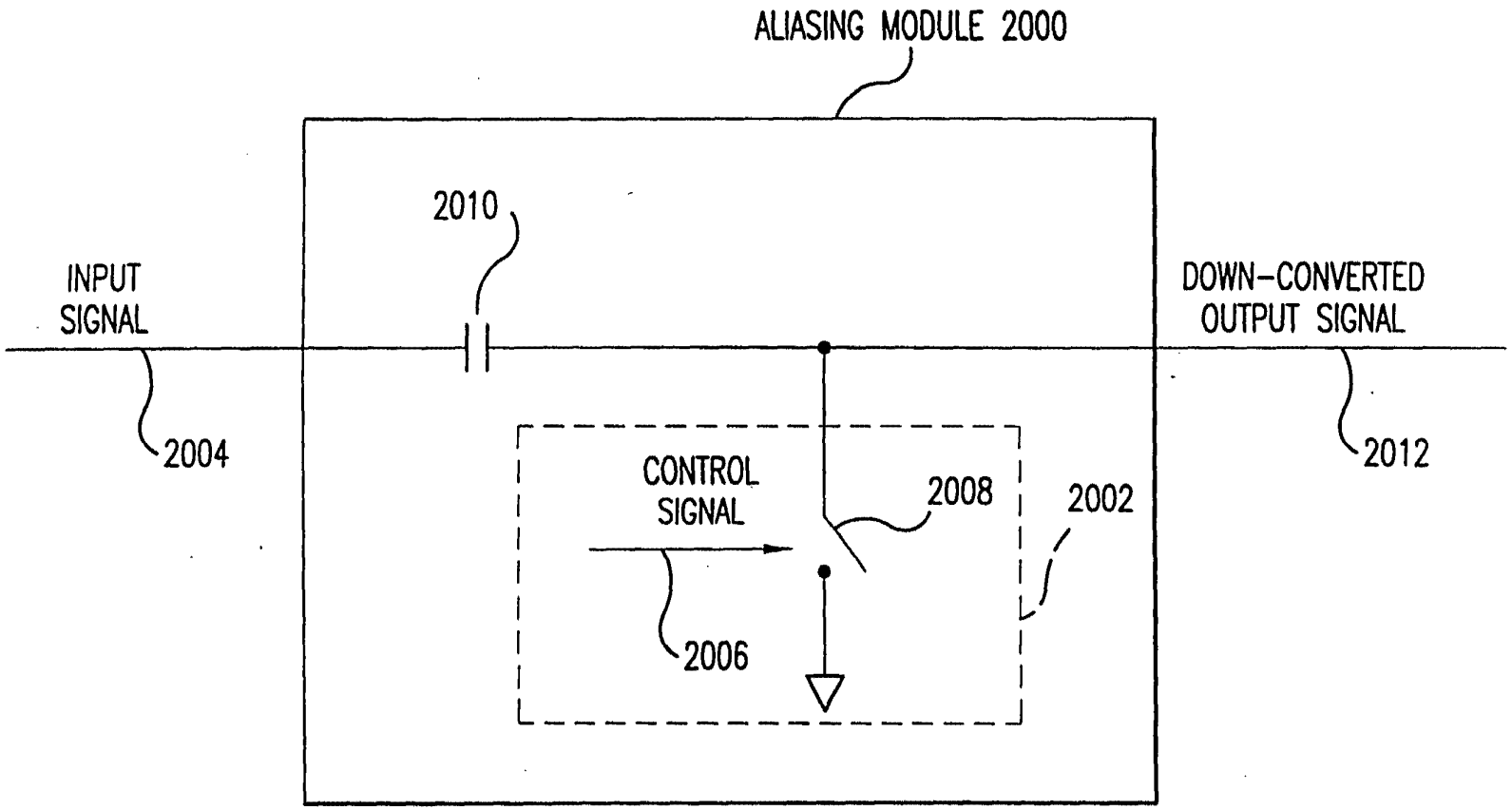


FIG. 20A-1

COPY

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON DC 20005

COPY MAILED

MAR 11 2005

OFFICE OF PETITIONS

In re Application of :
Sorrells, et al. :
Application No. 10/973,917 : ON PETITION
Filed: October 27, 2004 :
Attorney Docket No. 1744.0330003 :
For: UNIVERSAL PLATFORM MODULE AND METHODS AND APPARATUSES RELATING THERETO ENABLED BY UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY

This is a decision on the petition filed January 26, 2005, requesting, in effect, withdrawal of a Notice mailed December 8, 2004.

The application was filed on October 27, 2004. However, on December 8, 2004, The Office of Initial Patent Examination mailed a "Notice of Omitted Item(s) in a Nonprovisional Application" (Notice) stating that the application had been accorded a filing date of October 27, 2004, and advising applicant that figure 20A-1 appeared to have been omitted.

In response, the present petition was filed. Petitioners argue that the drawing should be included with the papers filed on October 27, 2004, because (1) it is not new matter and (2) it was filed in prior application No. 09/569,044, the entire disclosure of which was incorporated by reference at the time of this application's filing.

The petition is dismissed.

The mailing of a "Notice of Omitted Items" permits the applicant to either: (1) promptly establish prior receipt in the PTO of the items at issue (generally by way of a date-stamped postcard receipt (MPEP 503)), or (2) promptly submit the omitted items in a nonprovisional application and accept the date of such submission as the application filing date. An applicant asserting that the missing items were in fact deposited in the PTO with the application papers must file a petition (and the appropriate petition fee) with evidence of such deposit. An applicant desiring to submit the omitted items in a nonprovisional application and accept the date of such submission as the application filing date must file any omitted items with an oath or declaration in compliance with 37 CFR 1.63 and 1.64 referring to such items and a petition under 37 CFR 1.182 (with the petition fee under 37 CFR 1.17(h)) requesting the later filing date within two months of the date of the "Notice of Omitted Items" (37 CFR 1.181(f)).

In this case, petitioners neither assert that the missing drawing was actually deposited in the PTO on October 27, 2004 with the other application papers nor request a later filing date.

Instead, applicants seek to add the figure to the present application on the basis that the figure

does not contain new matter. However, no petition is necessary for that purpose. Additional figures may be entered by the primary examiner without a petition so long as the pages contain no new matter. See MPEP § 608.02(a).

MPEP 201.06(c) states that:

> . . . an applicant may incorporate by reference the prior application by including, in the application-as-filed, a statement that such specifically enumerated prior application or applications are "hereby incorporated herein by reference." The statement may appear in the specification or in the application transmittal letter. The inclusion of this incorporation by reference of the prior application(s) will permit an applicant to amend the continuing application to include any subject matter in such prior application(s), without the need for a petition. (emphasis supplied)

If applicants desire that figure 20A-1 be added to the application, the appropriate procedure is by way of amendment requesting the entry of the figure.

Accordingly, the petition is inappropriate and is subject to dismissal.

The petition fee will not be refunded, since the petition was not necessitated by any error on the part of the Office.

The application is being returned to the Office of Initial Patent Examination for further processing with a filing date of October 27, 2004. Drawing figure 20A-1 will not be processed at this time.

Thereafter, the application will be forwarded to Technology Center 2600 for examination in due course. The examiner may consider the January 26, 2005 "Request to Approve Proposed Drawing Corrections" as an amendment requesting the entry of the figure or the examiner may require a more formal submission.

Telephone inquiries specific to this matter should be directed to the undersigned at (571) 272-3230.

E. Shirene Willis
Senior Petitions Attorney
Office of Petitions
Office of the Deputy Commissioner
for Patent Examination Policy

OIPE
MAR 3 0 2005
PATENT & TRADEMARK

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*Admitted only in Maryland
+Admitted only in Virginia
•Practice Limited to Federal Agencies

March 30, 2005

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2661

Re: U.S. Nonprovisional Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: Sorrells *et al.*
Our Ref: 1744.0330003

Sir:

Applicants submit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. SKGF Cover Letter;

2. A Second Preliminary Amendment under 37 C.F.R. § 1.115; and

3. One new drawing sheet (FIG. 20A-1).

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby

petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/NDD/sjc
Enclosures

380578_1.DOC

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MAR 3 0 2005
PATENT & TRADEMARK OFFICE
JC25

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2661
Appl. No.: 10/973,917	Examiner: (to be assigned)
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**	

Second Preliminary Amendment Under 37 C.F.R. § 1.115

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In advance of prosecution, and pursuant to the USPTO Office of Petitions paper mailed March 11, 2005, Applicants submit the following amendments and remarks. This Preliminary Amendment is provided in the following format:

(A) Each section begins on a separate sheet;

(B) Starting on a separate sheet, amendments to the specification by presenting replacement paragraphs marked up to show changes made;

(C) Starting on a separate sheet, a complete listing of all of the claims:

- in ascending order;
- with status identifiers; and
- with markings in the currently amended claims;

(D) Starting on a separate sheet, the Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent

abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1-4. (*cancelled*)

5. (*previously presented*) An apparatus capable of performing simultaneous multi-platform operations, comprising:

at least one multi-platform module including a plurality of transceivers each having at least one frequency translating module; and

a control module for enabling the at least one multi-platform module to communicate with at least one of a plurality of communication links, the control module including a plurality of protocol/standard sub-modules;

wherein a first protocol/standard sub-module operates a first transceiver in conformance with a first protocol/standard combination; and

wherein a second protocol/standard sub-module simultaneously operates a second transceiver in conformance with a second protocol/standard combination.

6. (*previously presented*) The apparatus of claim 5, wherein the control module enables the at least one multi-platform module to simultaneously communicate with a quantity of the plurality of communication links by employing an equal quantity of the plurality of standard/protocol sub-modules.

7. (*previously presented*) The apparatus of claim 5, wherein the at least one multi-platform module includes a plurality of receivers and a plurality of transmitters each having at least one frequency translating module.

8. (*previously presented*) The apparatus of claim 5, wherein the first protocol/standard combination is different from the second protocol/standard combination.

9. (*previously presented*) The apparatus of claim 5, wherein the first and second protocol/standard sub-modules contain respective first and second implementation and operational instructions for the at least one multi-platform sub-module.

10. (*previously presented*) The apparatus of claim 9, wherein the first and second implementation and operational instructions include respective first and second protocol stacks and specification information about the first and second protocol architectures.

11. (*previously presented*) The apparatus of claim 9, wherein the first and second implementation and operational instructions can be updated, upgraded, replaced, or modified to provide the at least one multi-platform sub-module with additional functionality.

12. (*previously presented*) The apparatus of claim 5, wherein the first and second protocol/standard sub-modules operate the first and second transceivers in conformance with respective requirements of the first and second protocols and operating environments.

13. (*previously presented*) The apparatus of claim 12, wherein the first and second operating environments include at least one of respective standards, content encoders and decoders, and protocol gateways.

14. (*previously presented*) A method for performing simultaneous multi-platform operations, comprising:

(1) controlling at least one multi-platform module to communicate with at least one of a plurality of communication links using a control module having a plurality of standard/protocol sub-modules, wherein the at least one multi-platform module includes a plurality of transceivers each having at least one frequency translation module;

(2) operating a first transceiver in conformance with a first protocol/standard combination using a first standard/protocol sub-module; and

(3) simultaneously operating a second transceiver in conformance with a second protocol/standard combination using a second standard/protocol sub-module.

15. (*previously presented*) The method of claim 14, wherein step (1) comprises:

controlling the at least one multi-platform module to simultaneously communicate with a quantity of the plurality of communications links by employing an equal quantity of the plurality of standard/protocol sub-modules.

16. (*previously presented*) The method of claim 14, wherein step (1) comprises:

controlling at least one multi-platform module to communicate with at least one of the plurality of communication links using the control module, the at least one multi-platform module including a plurality of receivers and a plurality of transmitters each having at least one frequency translating module.

17. (*previously presented*) The method of claim 14, wherein step (3) comprises:

simultaneously operating the second transceiver in conformance with a second protocol/standard combination that is different from the first protocol/standard combination.

18. (*previously presented*) The method of claim 14, wherein steps (2) and (3) comprise:

programming the first and second protocol/standard sub-modules with respective first and second implementation and operational instructions for the at least one multi-platform sub-module.

19. (*previously presented*) The method of claim 18, wherein steps (2) and (3) further comprise:

programming the first and second protocol/standard sub-modules with respective first and second protocol stacks and specification information about the first and second protocol architectures.

20. (*previously presented*) The method of claim 18, wherein steps (2) and (3) further comprise:

updating, upgrading, replacing, or modifying the first and second implementation and operational instructions to provide the at least one multi-platform sub-module with additional functionality.

21. (*previously presented*) The method of claim 14, wherein steps (2) and (3) comprise:

simultaneously operating the first and second transceivers in conformance with respective requirements of the first and second protocols and operating environments.

22. (*previously presented*) The method of claim 21, wherein steps (2) and (3) further comprise:

simultaneously operating the first and second transceivers in conformance with respective standards, content encoders and decoders, and protocol gateways of the first and second protocols and operating environments.

Remarks

Upon entry of the foregoing amendment, claims 5-22 are pending in the application, with claims 5 and 14 being the independent claims.

Pursuant to the USPTO's comments in the Office of Petitions paper mailed March 11, 2005, a new drawing sheet, showing FIG. 20A-1, is sought to be added. FIG. 20A-1 is believed to introduce no new matter, and its entry is respectfully requested.

Conclusion

Prompt and favorable consideration of this Second Preliminary Amendment is respectfully requested. Applicants believe the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 3/30/05

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Washington, D.C. 20005-3934
(202) 371-2600

377698_1.DOC

Amendments to the Drawings

Applicants submit herewith a new drawing sheet showing FIG. 20A-1.

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MAR 30 2005
PATENT & TRADEMARK OFFICE

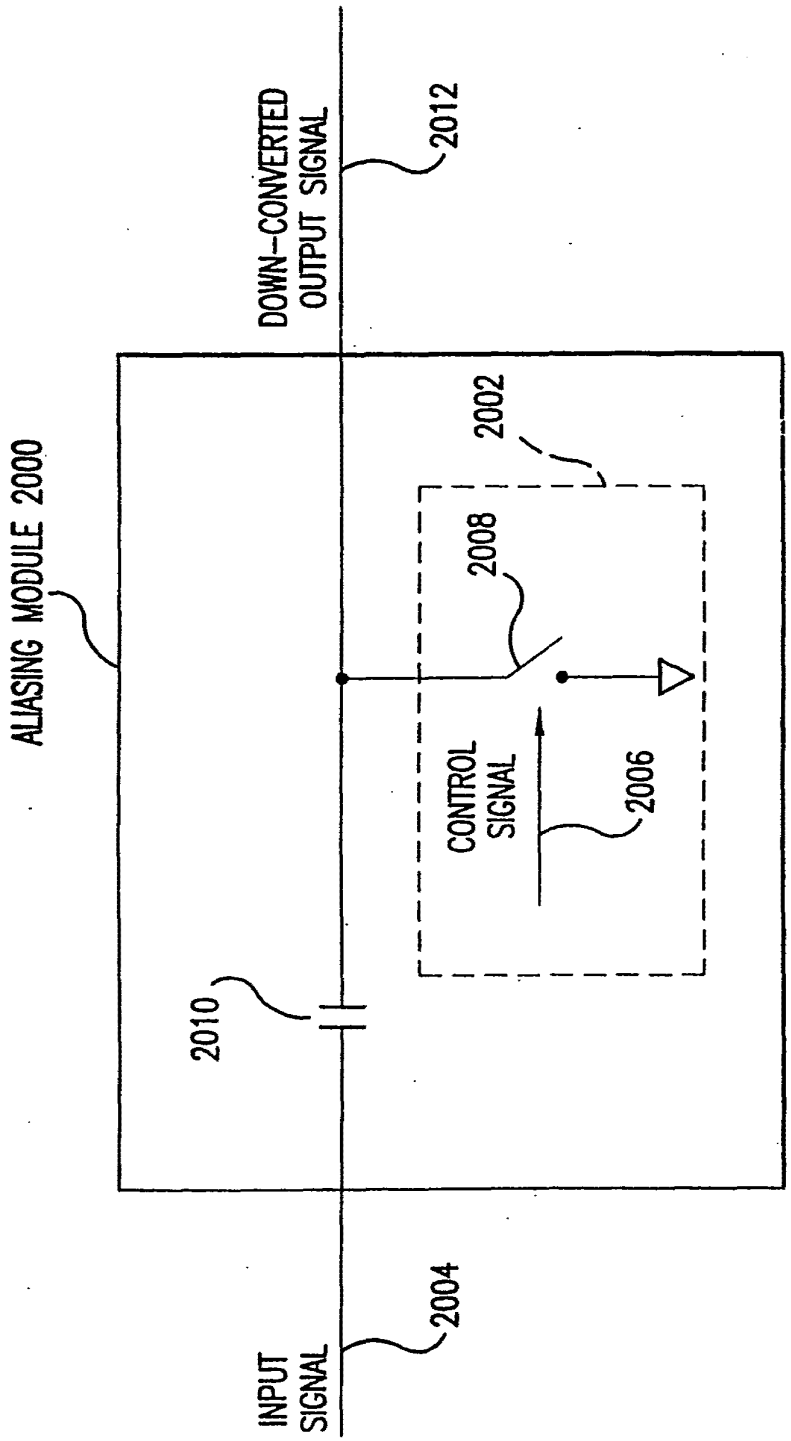


FIG. 20A-1

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2004

Application or Docket Number: 10/973917

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	4	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	4 minus 20=	* 0
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐			OR	OTHER THAN SMALL ENTITY	
RATE	FEE			RATE	FEE
BASIC FEE	395.00		OR	BASIC FEE	790.00
X$ 9=			OR	X$18=	
X44=			OR	X88=	
+150=			OR	+300=	
TOTAL			OR	TOTAL	790

10-27-04

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 20	= 0
Independent	* 3	Minus	*** 3	= 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY			OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	0
X44=			OR	X88=	0
+150=			OR	+300=	0
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	0

3-30-05

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 20	= 0
Independent	* 2	Minus	*** 3	= 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	0
X44=			OR	X88=	0
+150=			OR	+300=	0
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	0

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	
X44=			OR	X88=	
+150=			OR	+300=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

IPW

Sterne Kessler Goldstein Fox
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OIPE JC75
JUN 13 2005
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+Admitted only in Virginia
•Practice Limited to Federal Agencies

June 13, 2005

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2661

Re: U.S. Nonprovisional Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: Sorrells *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Resubmission of Statement under 37 CFR § 3.73(b);

2. A copy of the executed Statement under 37 CFR § 3.73(b) from Assignee with a copy of the "do not forward"-stamped Assignment attached, as filed on October 27, 2004; and

3. One return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/NDD/sjc
Enclosures

408948_1.DOC

OIPE JC25 JUN 13 2005 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2661
Appl. No.: 10/973,917	Examiner: (to be assigned)
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**	

Resubmission of Statement under 37 CFR § 3.73(b)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The attached Statement under 37 CFR § 3.73(b) was previously filed on October 27, 2004, but the copy of the attached assignment was not entered into the file wrapper. Instead, the copy of the Assignment was forwarded to the Recordation Branch, notwithstanding the designation stamped "Do Not Forward to Assignment Branch - Not For Recordation."

Applicants respectfully request that the Statement under 37 CFR § 3.73(b), along with the copy of the assignment, be entered into the file wrapper.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 6/13/05

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

408956_1.DOC

OIPE JC25 JUN 13 2005 PATENT & TRADEMARK OFFICE

Certificate Under 37 C.F.R. § 3.73(b)

Applicant/Patent Owner: David F. SORRELLS *et al.*

Application No./Patent No.: 09/569,044 Filed/Issue Date: May 10, 2000

Entitled: Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology

ParkerVision, Inc., a Corporation,
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [X] **the assignee of the entire right, title, and interest, or**

2. [ ] an assignee of an undivided part interest

in the patent application/patent identified above by virtue of either:

A. [X] **An Assignment from the inventor(s) of the patent application/patent identified above, for which a copy thereof is attached.**

OR

B. [ ] A chain of title from the inventor(s) of the patent application/patent identified above to the current assignee as shown below:

1. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[X] Copies of assignments or other documents in the chain of title are attached.

[NOTE: A separate copy (*i.e.*, the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the PTO. See MPEP 302-302.8]

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

Date: X 10-28-00

Name: Jeffrey L. Parker

Title: Chairman and Chief Executive Officer

Signature: X

P:\USERS\VBLADES\Russ Swindell\1744\1030000.373(b)
SKGF Rev.3/31/00 mac

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ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the undersigned inventor(s): 1) David F. SORRELLS; 2) Michael J. BULTMAN; 3) Robert W. Cook; 4) Richard C. LOOKE; and 5) Charley D. MOSES, JR., the undersigned inventor(s) hereby sell(s) and assign(s) to ParkerVision, Inc., 8493 Baymeadows Way, Jacksonville, FL 32256 (the Assignee) his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages:

check applicable box(es) ☒ for the United States of America (as defined in 35 U.S.C. § 100),
☒ and throughout the world,

(a) in the invention(s) known as Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled By Universal Frequency for which application(s) for patent in the United States of America has (have) been executed by the undersigned on 1) 10-26-00; 2) 10-25-00; 3) 10-25-00; 4) 10-27-00; and 5) 10-25-00 (also known as United States Application No. 09/569,044, filed May 10, 2000, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

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(b) in any and all applications that claim the benefit of the patent application listed above in part (a), including continuing applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application listed above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The undersigned inventor(s) agree(s) to execute all papers necessary in connection with the application(s) and any continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The undersigned inventor(s) agree(s) to execute all papers necessary in connection with any interference or patent enforcement action (judicial or otherwise) related to the application(s) or any continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such interference or patent enforcement action.

The undersigned inventor(s) hereby represent(s) that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

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The undersigned inventor(s) hereby grant(s) Robert Greene Sterne, Esquire, Registration No. 28,912; Edward J. Kessler, Esquire, Registration No. 25,688; Jorge A. Goldstein, Esquire, Registration No. 29,021; Samuel L. Fox, Esquire, Registration No. 30,353; David K.S. Cornwell, Esquire, Registration No. 31,944; Robert W. Esmond, Esquire, Registration No. 32,893; Tracy-Gene G. Durkin, Esquire, Registration No. 32,831; Michele A. Cimbala, Esquire, Registration No. 33,851; Michael B. Ray, Esquire, Registration No. 33,997; Robert E. Sokohl, Esquire, Registration No. 36,013; Eric K. Steffe, Esquire, Registration No. 36,688; Michael Q. Lee, Esquire, Registration No. 35,239; Steven R. Ludwig, Esquire, Registration No. 36,203; John M. Covert, Esquire, Registration No. 38,759; and Linda E. Alcorn, Esquire, Registration No. 39,588; all of STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C., 1100 New York Avenue, N.W., Suite 600, Washington, D.C. 20005-3934, power to insert in this assignment any further identification that may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

IN WITNESS WHEREOF, executed by the undersigned inventor(s) on the date opposite his/her name.

DO NOT FORWARD
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Date: X _____ Signature of Inventor: X _____

1) David F. SORRELLS

Date: X 25 Oct 00 Signature of Inventor: X _____

2) Michael J. BULTMAN

Date: X 10/25/00 Signature of Inventor: X _____

3) Robert W. COOK

Date: X 10/27/00 Signature of Inventor: X _____

4) Richard C. LOOKE

Date: X _____ Signature of Inventor: X _____

5) Charley D. MOSES, Jr.

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IN WITNESS WHEREOF, executed by the undersigned inventor(s) on the date opposite his/her name.

Date: X 10/26/00 Signature of Inventor: X _____
1) David F. SORRELLS

Date: X 25 Oct 00 Signature of Inventor: X _____
2) Michael J. BULTMAN

Date: X 10/25/00 Signature of Inventor: X _____
3) Robert W. COOK

Date: X _____ Signature of Inventor: X _____
4) Richard C. LOOKE

Date: X 10/25/2000 Signature of Inventor: X _____
5) Charley D. MOSES, Jr.

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AUG 09 2005
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TJW

Sterne Kessler Goldstein Fox
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August 9, 2005

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Commissioner for Patents
PO Box 1450
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Art Unit 2661
Mail Stop Amendment

Re: U.S. Nonprovisional Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: Sorrells *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;
2. Form PTO-1449 listing 985 documents and accompanied by two (2) documents;
3. Two compact discs labeled *IDS References Disc 1* and *IDS References Disc 2*; and
4. One return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/NDD/sjc
Enclosures

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THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Sorrells *et al.*	Confirmation No.: 3273
Appl. No.: 10/973,917	Art Unit: 2661
Filed: October 27, 2004	Examiner: (to be assigned)
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**	Atty. Docket: 1744.0330003

Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

In addition to providing hard copies of the documents as required by applicable rules (see boxes 7 and 8 below), Applicants herewith provide two Compact Discs labeled "Disc 1" and "Disc 2" having stored thereon searchable electronic copies (in PDF format) of the documents listed on the PTO-1449. More specifically, "Disc 1" contains electronic copies of documents AA1-AR1, AA2-AR2, AA3-AR3, AA4-AR4, AA5-AR5, AA6-AR6, AA7-AR7, AA8-AR8, AA9-AR9, AA10-AL10, AN10-AR10, AA11-AI11, AN11-AR11, AA12-AI12, AN12-AR12, AA13-AI13, AN13-AR13, AA14-AI14, AN14-AR14, AA15-AI15, AN15-AR15, AA16-AI16, AN16-AR16, AA17-AI17, AN17-AR17, AA18-AI18, AN18-AR18, AA19-AI19, AN19-AR19, AA20-AI20, AN20-AR20, AA21-AI21, AN21-AR21, AA22-AI22,

AN22-AR22, AA23-AI23, AN23-AR23, AA24-AI24, AN24-AR24, AA25-AI25, AN25-AR25, AA26-AI26, AN26-AR26, AA27-AI27, AN27-AR27, AA28-AI28, AN28-AR28, AA29-AI29, AN29-AR29, AA30-AI30, AN30-AR30, AA31-AI31, AN31-AR31, AA32-AI32, AN32-AR32, AA33-AI33, AN33-AR33, AA34-AI34, AN34-AR34, AA35-AI35, AN35-AR35, AA36-AI36, AN36-AR36, AA37-AI37, AN37-AR37, AA38-AI38, AN38-AR38, AA39-AI39, AN40-AR40, AN41-AR41, AN42-AR42, AN43-AR43, AN44-AR44, AN45-AR45, AN46-AR46, AN47-AR47, AN48-AR48, AN49-AR49, AN50, and AO50; and "Disc 2" contains electronic copies of documents AM10, AJ11-AM11, AJ12-AM12, AJ13-AM13, AJ14-AM14, AJ15-AM15, AJ16-AM16, AJ17-AM17, AJ18-AM18, AJ19-AM19, AJ20-AM20, AJ21-AM21, AJ22-AM22, AJ23-AL23, AA40-AI40, AA41-AI41, AA42-AI42, AA43-AI43, AA44-AI44, AA45-AI45, AA46-AI46, AA47-AI47, AA48-AI48, AA49-AI49, AA50-AI50, AP50-AR50, AA51-AI51, AN51-AR51, AA52-AI52, AN52-AR52, AA53-AI53, AN53-AR53, AA54-AI54, AN54-AR54, AA55-AI55, AN55-AR55, AA56-AI56, AN56-AR56, AA57-AI57, AN57-AR57, AA58-AI58, AN58-AR58, AA59-AI59, AN59-AP59, AA60-AI60, AA61-AI61, AA62-AI62, AA63-AI63, AA64-AI64, AA65-AI65, and AA66-AH66. Documents AQ59, AI66, and AA67-AF67 have not been scanned at this time. The file names on the CDs correspond to the identifiers on the PTO-1449. It is noted that the CDs are being provided in addition to hard copies of the documents (as required by applicable rules) for the convenience of the Examiner.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication

dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents AD1, AL1, AO1, AC2, AF2, AG2, AI2, AC5, AG5, AB6, AF7, AI7, AB8, AF8, AG9, AK9, AO9, AO11, AA12, AE14, AN14, AB15, AE15, AH15, AO15, AF16, AD18, AG18, AB20, AC20, AQ20, AA22, AH22, AI23, AC24, AF26, AC30, AH31, AC32, AA33, AR33, AH34, AP35 and AO48 were included with Petitions to Make Special pleadings in co-owned related U.S. Patent Nos. 6,061,551, 6,061,555, 6,049,706 and 6,091,940.

Documents AJ1, AL9, AJ10, AA19, AC25, AB30 and AF32 were cited in search reports in the corresponding foreign applications of the above-referenced co-owned related patents.

Documents AM4, AH6, AL7, AJ9, AM9, AC17, AA20, AG20, AG21, AA24, AD24, AG24, AI31, AA32, AG34, AD36 and AQ37 were cited in searches performed at Applicants' request by the European Patent Office's Searching Authority in the above-referenced co-owned related patents.

Documents AH5, AH17, AD21, AB34, AE34, AB36, AI36 and AI38 were cited by the Examiners in the above-referenced co-owned related patents.

Documents AP6-AR6 and AN7-AP7 are copies of Declarations (including Exhibits) made by Messrs. Bultman, Cook, Holtz, Looke, Moses, Parker, and Sorrells, filed in the above-referenced co-owned related patents.

Documents AA6, AD6, AO6, AE7, AE8, AA11, AE11, AH11, AI12, AB13, AD13, AH13, AC14, AG14, AE16, AB17, AF19, AD20, AN21, AG23, AH27, AI27, AI28, AH29, AG30, AD37, AR40, AO49 and AQ49 were suggested or identified by potential licensees.

Documents AR21, AN22-AR22, AN23-AR23, AN24-AR24, AN25-AR25, AN26-AR26, AN27-AR27, AN28-AR28, AN29-AR29, AN30-AR30, AN31-AR31, AN32-AR32 and AN33-AP33 are press releases issued by assignee ParkerVision, Inc.

Documents AA1, AB1, AD1-AG1, AA2, AH21, AD44, and AD59-AF59 were cited by an Examiner in related U.S. Patent Application No. 09/569,044, filed May 10, 2000, entitled "Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Document AA1-AD1, AB48, and AH64 were cited by an Examiner in related U.S. Patent Application No. 10/197,441, filed July 18, 2002, entitled "Method and System for Frequency Up-Conversation With a Variety of Transmitter Configurations," directed to related subject matter.

Documents AJ1, AK9-AM9, AG28, AB30, AA32, AN52 and AP55 were cited by an Examiner in related European Patent Application No. 99954905.8, filed October 18, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

Documents AI7, AJ9, AK9, AG20, AG21, AB30 and AI43 were cited in a written opinion in related PCT Application No. PCT/US00/23923, filed October 18, 1999, entitled "Applications of Frequency Translation," directed to related subject matter.

Documents AI7, AE34, AA46, and AB48 were cited by an Examiner in related U.S. Patent Application No. 09/293,580, filed April 16, 1999, entitled "Method and System for Frequency Up-Conversion with a Variety of Transmitted Configurations," directed to related subject matter.

Documents AK9, AM9, AE15, AL19, AM19, AB46 and AA50 were cited in a search report in related PCT Application No. PCT/US01/08969, filed March 22, 2001, entitled, "Integrated Frequency Translation and Selectivity with a Gain Control Functionality, and Applications Thereof," directed to related subject matter.

Documents AK9, AE15, AK22-AM22, AA27, AC32, AE45, AI51, AA52, and AQ58 were cited in a search report in related PCT Application No. PCT/US01/15555, filed May 16, 2001, entitled, "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AK9, AC17, AD36 and AD40 were cited in a search report in related PCT Application No. PCT/US00/21359, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AJ10, AH17, AG28, AH34, AD44-AI44, and AA45-AD45 were cited by an Examiner in related U.S. Patent Application No. 09/261,129, filed March

3, 1999, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Documents AM10, AJ11, AK11 and AE40 were cited in a communication issued by the International Preliminary Examination Authority in related PCT Application No. PCT/US00/01108, filed January 19, 2000, entitled "Frequency Translation and Embodiments Thereof Such as the Family Radio Service," directed to related subject matter.

Documents AL11, AM11, AA44, and AQ50 were cited in a communication issued by the International Searching Authority in related PCT Application No. PCT/US00/09911, filed April 14, 2000, entitled "Method And System For Down-converting an Electromagnetic Signal, And Transforms For Same," directed to related subject matter.

Documents AJ12, AK12, AE45, and AF45 were cited in a search report in related PCT Application No. PCT/US00/27555, filed October 6, 2000, entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AL12, AM12, AG45, and AH45 were cited in a search report in related PCT Application No. PCT/US00/34771, filed January 21, 2000, entitled "Phase Comparator Using Undersampling," directed to related subject matter.

Documents AJ13-AL13, AI45, and AB46 were cited in a search report issued in related PCT Application No. PCT/US00/27281, filed October 4, 2000, entitled "Frequency Converter and Method," directed to related subject matter.

Documents AL13, AM18, AJ19, and AI45 were cited in a search report in related PCT Application No. PCT/US00/31659, filed November 20, 2000, entitled "Phase Shifting Applications of Universal Frequency Translation," directed to related subject matter.

Documents AM13, AJ14, AK14, AM21, AJ22 and AQ51 were cited by an Examiner in related Japanese Patent Application No. 2000-577,765, filed June 21, 2000, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AL14, AM14, AJ15 and AK15 were cited by an Examiner in related Japanese Patent Application No. 2000-577,761, filed June 20, 2000, entitled "Method and System for Frequency Up-conversion," directed to related subject matter.

Documents AL15, AM15, AJ16-AM16, AJ17-AM17, AJ20, and AK23 were cited by an Examiner in related Japanese Patent Application No. 2000-577,764, filed June 21, 2000, entitled "Applications of Frequency Translation," directed to related subject matter.

Documents AJ18-AL18, AB47, AC47, AE47-AG47, AB48, and AC49 were cited by an Examiner in related U.S. Patent Application No. 09/489,675, filed January 24, 2000, entitled "Bar Code Scanner Using Universal Frequency Translation Technology for Up-Conversion and Down-Conversion," directed to related subject matter.

Documents AK19 and AF48 were cited in a search report in related PCT Application No. PCT/US01/15111, filed October 5, 2001, entitled "Method and

Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Documents AK20, AL20, AJ21, AK21, AL21, AE42, AP56 and AQ56 were cited in a search report in related PCT Application No. PCT/US01/12086, filed April 13, 2001, entitled, "Frequency Converter," directed to related subject matter.

Documents AI23, AB30, AB60-AE60, and AC65 were cited by an Examiner in related U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Methods and Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Document AI23 and AD46 were cited by an Examiner in related U.S. Patent Application No. 09/293,095, filed April 16, 1999, entitled "Method and System for Down-Converting an Electromagnetic Signal Having Optimized Switch Structures," directed to related subject matter.

Documents AI23, AH50, AB55, AI59, and AA60 were cited by an Examiner in related U.S. Patent Application No. 09/525,185, filed March 14, 2000, entitled "Spread Spectrum Applications of Universal Frequency Translation Technology," directed to related subject matter.

Documents AI23, AI59, AF60-AH60, and AA65 were cited by an Examiner in related U.S. Patent Application No. 09/590,955, filed June 9, 2000, entitled "Phase-Shifting Applications of Universal Frequency Translation," directed to related subject matter.

Documents AJ23 and AB52 were cited in an Invitation to Pay Additional Fees in PCT Application No. PCT/US01/43077, filed November 14, 2001, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Documents AL23, AH47, AB49, AG51, AF56-AH56, AO59, and AE61 were cited by an Examiner in related U.S. Patent Application No. 09/669,634, filed September 26, 2000, entitled "High Frequency Translator and Method of High Frequency Translation," directed to related subject matter.

Documents AC24, AD47, AA48, and AB50 were cited by an Examiner in related U.S. Patent Application No. 09/376,509, filed August 18, 1999, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AG27, AH47, AI47, AC52, AC56, AE64, AI65, and AA66-AG66 were cited by an Examiner in related U.S. Patent Application No. 09/855,851, filed May 16, 2001, entitled "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AD35, AB44, AC44, AE46-AI46, and AA47 were cited by an Examiner in parent U.S. Patent Application No. 09/293,342, filed April 16, 1999, entitled "Method and System for Down-Converting Electromagnetic Signals Including Resonant Structures for Enhanced Energy Transfer," directed to related subject matter.

Documents AA38 and AG48 were cited by an Examiner in related U.S. Patent Application No. 09/476,091, filed January 3, 2000, entitled "Image-Reject Down-

Converter and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AI43, AH47 and AH48 were cited by an Examiner in related U.S. Patent Application No. 09/293,283, filed April 16, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

Documents AC46 and AA48 were cited by an Examiner in related U.S. Patent Application No. 09/670,831, filed September 28, 2000, entitled "Universal Frequency Translation, Embodiments Thereof, and a Web Site and Web Pages Directed to Same," directed to related subject matter.

Documents AH47, AI47, AA48-AE48, AB49, AF51, AG51, AC52, AG54, AF55, AC56, AD56, AI56, AA57, AD64, AE64, AB65, AH65, AH66, and AI66 are co-owned patents which are directed to related subject matter.

Documents AI47, AH50, AF55, AC56, AD56, AI56, AA57, and AH59 were cited by an Examiner in related U.S. Patent Application No. 09/838,387, filed April 20, 2001, entitled "Method and System for Down-Converting and Up-Converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AB48, AD48, AH54, AI54, and AA55-AC55 were cited by an Examiner in related U.S. Patent Application No. 09/548,923, filed April 13, 2000, entitled "Method and System for Frequency Conversion with Modulation Embodiments," directed to related subject matter.

Documents AB48, AE48, AD56, AI56, AG651, and AH61 were cited by an Examiner in related U.S. Patent Application No. 09/525,615, filed March 14, 2000, entitled "Method, System, and Apparatus for Balanced Frequency Up-conversion of a Baseband Signal," directed to related subject matter.

Documents AI48, AA49, and AF50 were cited by an Examiner in related U.S. Patent Application No. 09/567,963, filed May 10, 2000, entitled "Frequency Synthesizer Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AD49-AI49, AE51, and AB67 were cited by an Examiner in related U.S. Patent Application No. 09/476,092, filed January 3, 2000, entitled "Analog Zero IF FM Decoder and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AI49, AH50, AI50, AA51, AB51, AI62, AA63, and AB63 were cited by an Examiner in related U.S. Patent Application No. 09/632,857, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter.

Documents AC50-AE50, AG50, AI50 and AC51 were cited by an Examiner in related U.S. Patent Application No. 09/476,330, filed January 3, 2000, entitled, "Multi-Mode, Multi-Band Communication System," directed to related subject matter.

Documents AH50, AA51 and AB51 were cited in by an Examiner in related U.S. Patent Application No. 09/526,041, filed March 14, 2000, entitled, "DC Offset,

Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AH50, AC53-AI53, and AF61 were cited by an Examiner in related U.S. Patent Application No. 09/476,093, filed January 3, 2000, entitled "Family Radio System with Multi-Mode and Multi-Band Functionality," directed to related subject matter.

Documents AH50 and AB57-AE57 were cited by an Examiner in related U.S. Patent Application No. 09/567,978, filed May 10, 2000, entitled "Carrier and Clock Recovery Using Universal Frequency Translation," directed to related subject matter.

Documents AH51, AB56, AE56, AN58-AP58, AN59, AP59, AG63, and AC67-AF67 were cited by an Examiner in related U.S. Patent Application No. 09/567,977, filed May 10, 2000, entitled "Optical Down-converter Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AA52, AF52, AI52, and AG59 were cited by an Examiner in related U.S. Patent Application No. 10/289,377, filed November 7, 2002, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AD52-AG52 and AC63-AF63 were cited by an Examiner in related U.S. Patent Application No. 09/986,764, filed November 9, 2001, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AA52, AE52, AH52, AI52, AA53, and AB53 were cited in a search report in related PCT Application No. PCT/US02/35861, filed November 8, 2002, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AA54-AD54 were cited in a search report in a related PCT Application No. PCT/US03/16403, filed May 27, 2003, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AB54, AI61, AA62, and AB62 were cited in a written opinion in related PCT Application No. PCT/US03/16403, filed May 27, 2003, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AB54, AQ59, AI61, and AA62-AH62 were cited by an Examiner in related U.S. Patent Application No. 10/290,323, filed November 8, 2002, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AE54, AF54, AH55, AI60, AA61, AB61, and AA67 were cited by an Examiner in related U.S. Patent Application No. 09/550,642, filed April 14, 2000, entitled "Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AD55 and AE55 were cited by an Examiner in related U.S. Patent Application No. 09/543,867, filed April 5, 2000, entitled "Automated Meter Reader Applications of Universal Frequency Translation," directed to related subject matter.

Documents AG55 and AH55 were cited by an Examiner in related U.S. Patent Application No. 10/317,181, filed December 12, 2002, entitled "Differential Frequency Down-Conversion Using Techniques of Universal Frequency Translation Technology," directed to related subject matter.

Documents AI55, AA56, AC61, and AD61 were cited by an Examiner in related U.S. Patent Application No. 10/317,165, filed December 12, 2002, entitled "Method and Apparatus for Reducing DC Offsets in Communication Systems Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AF57 and AG57 were cited by an Examiner in related U.S. Patent Application No. 10/330,219, filed December 30, 2002, entitled "Methods and Systems for Down-Converting Electromagnetic Signals, and Applications Thereof," directed to related subject matter.

Documents AH57, AI57, AA58-AI58, and AA59 were cited by an Examiner in related U.S. Patent Application No. 09/566,188, filed May 5, 2000, entitled "Integrated Frequency Translation and Selectivity with Gain Control Functionality, and Applications Thereof," directed to related subject matter.

Documents AB59 and AC59 were cited by an Examiner in related U.S. Patent Application No. 09/632,856, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation," directed to related subject matter.

Documents AH63, AI63, AA64, and AB64 were cited by an Examiner in parent U.S. Patent Application No. 09/987,193, filed November 13, 2001, entitled

"Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Document AC64 was cited by an Examiner in related U.S. Patent Application No. 09/632,857, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter.

Documents AF64 and AG64 were cited by an Examiner in related U.S. Patent Application No. 10/289,377, filed November 7, 2002, entitled "Method and Apparatus for Reducing DC Offsets in A Communication System," directed to related subject matter.

Document AI64 was cited by an Examiner in related U.S. Patent Application No. 10/086,250, filed March 4, 2002, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Documents AD65-AG65 were cited by an Examiner in related U.S. Patent Application No. 09/770,675, filed January 29, 2001, entitled "Wireless and Wired Cable Modem Applications of Universal Frequency Translation Technology," directed to related subject matter.

The other documents in the PTO-1449 do not fall within the above categories.

It is noted that some of these documents could be classified in more than one of the above categories.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The

Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a

communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. Concise explanations of the relevance of the non-English language documents AJ1, AK1, AJ6, AK7, AJ8-AL8, AK11-AM11, AJ12, AM13, AJ14-AM14, AJ15-AM15, AJ16-AM16, AJ17-AM17, AJ18-AL18, AJ20-AL20, AK21, AM21, AJ22, AK23, AL23, AQ50 and AQ51 appear below:

Document AJ1 (DE 42 37 692 C1) appears to be a receiver for a digital radio signal. Document AJ1 is a counterpart German application of document AG28, which is in the English language.

Document AK1 (EP 0 035 166 A1) appears to describe a digitized receiver. An English language abstract of document AK1 is enclosed as document AQ8.

Document AJ6 (EP 0 785 635 A1) appears to describe a method and apparatus for frequency diversity transmission using a plurality of uncorrelated carriers. An English language abstract of document AJ6 is enclosed as document AP8.

Document AK7 (FR 2 743 231 A1) is the corresponding French application of document AJ6 (EP 0 785 635 A1), which is described above.

Document AJ8 (JP 2-39632) appears to describe a transmitter for frequency diversity. An English language abstract of document AJ8 is enclosed as document AO8.

Document AK8 (JP 2-131629) appears to describe a transmitter-receiver for frequency diversity. An English language abstract of document AK8 is enclosed as document AN8.

Document AL8 (JP 2-276351) appears to describe an FSK demodulating circuit. An English language abstract of document AL8 is enclosed as document AR7.

Document AK11 (FR 2245130) appears to describe a converter. A partial English language translation of document AK11 is enclosed as document AP50.

Document AL11 (DE 3541031) appears to describe a method and device for demodulating high-frequency modulated signals. An English language translation of document AL11 is enclosed as document AR50.

Document AM11 (EP 0 732 803) appears to describe a procedure and device for demodulation by sampling. An English translation of document AM11 is enclosed as document AN51.

Document AJ12 (DE 19735798) appears to describe a transceiver. An English translation of document AJ12 is enclosed as document AP51.

Document AM13 (JP 56-114451) appears to describe a system for diversity radio transmission. Document AM13 is a counterpart Japanese application of document AF8, which is in the English language.

Document AJ14 (JP 8-32556) appears to describe a data transmitter-receiver. An English language abstract of document AJ14 is enclosed as document AO52.

Document AK14 (JP 8-139524) appears to describe a frequency converting circuit and radio communication device. An English language abstract of document AK14 is enclosed as document AP52.

Document AL14 (JP 59-144249) appears to describe a pulse signal transmission system. An English language abstract of document AL14 is enclosed as document AQ52.

Document AM14 (JP 63-54002) appears to describe a microwave burst signal generator which incorporates a FET frequency multiplier. An English language abstract of document AM14 is enclosed as document AR52.

Document AJ15 (JP 6-237276) appears to describe a quadrature modulator. An English language abstract of document AJ15 is enclosed as document AN53.

Document AK15 (JP 8-23359) appears to describe a digital quadrature modulation device. An English language abstract of document AK15 is enclosed as document AO53.

Document AL15 (JP 47-2314) appears to describe a demodulator. An English language translation of document AL15 is enclosed as document AP53.

Document AM15 (JP 58-7903) appears to describe a switched capacitor modulator. A partial English language translation of document AM15 is enclosed as document AQ53.

Document AJ16 (JP 58-133004) appears to describe an amplitude detector. An English language abstract of document AJ16 is enclosed as document AR53.

Document AK16 (JP 60-58705) appears to describe a frequency converting circuit. An English language abstract of document AK16 is enclosed as document AN54.

Document AL16 (JP 4-123614) appears to describe a level converting circuit. An English language abstract of document AL16 is enclosed as document AO54.

Document AM16 (JP 4-127601) appears to describe a frequency conversion circuit. An English language abstract of document AM16 is enclosed as document AP54.

Document AJ17 (JP 5-175730) appears to describe a time division direct receiver. An English language abstract of document AJ17 is enclosed as document AQ54.

Document AK17 (JP 5-175734) appears to describe an FM demodulator. An English language abstract of document AK17 is enclosed as document AR54.

Document AL17 (JP 7-154344) appears to describe a receiver for receiving modulated carrier signals and an IQ mixer/demodulator using it's receiving constitution. An English language abstract of document AL17 is enclosed as document AN55.

Document AM17 (JP 7-307620) appears to describe a bottom detection circuit. An English language abstract of document AM17 is enclosed as document AO55.

Document AJ18 (JP 55-66057) appears to describe a bar-code detection circuit. An English language abstract of document AJ18 is enclosed as document AQ55.

Document AK18 (JP 63-65587) appears to describe a wireless light pen device. An English language abstract of document AK18 is enclosed as document AR55.

Document AL18 (JP 63-153691) appears to describe a data transfer for a semiconductor data carrier system. An English language abstract of document AL18 is enclosed as document AN56.

Document AJ20 (JP 60-130203) appears to describe a frequency converter. An English language abstract of document AJ20 is enclosed as document AO56.

Document AK20 (DE 196 27 640 A1) appears to describe a mixer. Document AK20 is a counterpart German application of document AA33, which is in the English language.

Document AL20 (EP 0 087 336 A1) appears to describe a transistorized mixer for microwave transmitters. The granted version of document AL20 is cited as document AM20 (EP 0 087 336 B1) and contains an English language version of the claims.

Document AK21 (FR 2 669 787 A1) appears to describe a symmetrical super high frequency mixer. An English language abstract of document AK21 is enclosed as document AR56.

Document AM21 (JP 61-30821) appears to describe a squelch device. An English language abstract of document AL21 is enclosed as document AP57.

Document AJ22 (JP 5-327356) appears to describe a frequency converter. An English language abstract of document AJ22 is enclosed as document AQ57.

Document AK23 (JP 9-36664) appears to describe a frequency conversion circuit. An English language abstract of document AK23 is enclosed as document AR58.

Document AL23 (DE 196 48 915 A1) appears to describe a process of frequency conversion. An English language translation of document AL23 is enclosed as document AO59.

Document AQ50 (Fest et al.) appears to discuss analog-digital converters. An English language translation of document AQ50 is enclosed as document AO51.

Document AQ51 (Miki et al.) appears to describe modulation systems. A partial English language translation of document AQ51 is enclosed as document AR51.

☒ 7. In accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent application publications cited on the attached Form PTO-1449 are not enclosed.

☒ 8. Copies of documents AP59 and AQ59 are enclosed. The remaining documents listed under 'Foreign Patent Documents' and 'Other Documents' were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of the 'Foreign Patent Documents' and 'Other Documents' cited in the parent application are not enclosed. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000, 09/476,093, filed January 3, 2000, 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication

from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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OIPE JC73 AUG 18 2005 PATENT & TRADEMARK OFFICE
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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. Sorrells	
FILING DATE	ART UNIT
October 27, 2004	2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	2,057,613	10/1936	Gardner			
	AB1	2,241,078	05/1941	Vreeland			
	AC1	2,270,385	01/1942	Skillman			
	AD1	2,283,575	05/1942	Roberts			
	AE1	2,358,152	09/1944	Earp			
	AF1	2,410,350	10/1946	Labin *et al.*			
	AG1	2,451,430	10/1948	Barone			
	AH1	2,462,069	02/1949	Chatterjea *et al.*			
	AI1	2,462,181	02/1949	Grosselfinger			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	DE 42 37 692 C1	03/1994	DE			No
	AK1	EP 0 035 166 A1	09/1981	EP			No
	AL1	EP 0 193 899 B1	06/1990	EP			N/A
	AM1	EP 0 380 351 A2	08/1990	EP			N/A

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN1	Aghvami, H. *et al.*, "Land Mobile Satellites Using the Highly Elliptic Orbits- The UK T-SAT Mobile Payload," *Fourth International Conference on Satellite Systems for Mobile Communications and Navigation*, IEE, pp. 147-153 (October 17-19, 1988).
	AO1	Akers, N.P. *et al.*, "RF Sampling Gates: a Brief Review," *IEE Proceedings*, IEE, Vol. 133, Part A, No. 1, pp. 45-49 (January 1986).
	AP1	Al-Ahmad, H.A.M. *et al.*, "Doppler Frequency Correction for a Non-Geostationary Communications Satellite. Techniques for CERS and T-SAT," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizers,* IEE, pp. 4/1-4/5 (January 23, 1986).
	AQ1	Ali, I. *et al.*, "Doppler Characterization for LEO Satellites," *IEEE Transactions on Communications*, IEEE, Vol. 46, No. 3, pp. 309-313 (March 1998).
	AR1	Allan, D.W., "Statistics of Atomic Frequency Standards," *Proceedings Of The IEEE Special Issue on Frequency Stability*, IEEE, pp. 221-230 (February 1966).

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FORM PTO-1449	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
INFORMATION DISCLOSURE STATEMENT	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	2,472,798	06/1949	Fredendall			
	AB2	2,497,859	02/1950	Boughtwood *et al.*			
	AC2	2,499,279	02/1950	Peterson			
	AD2	2,802,208	08/1957	Hobbs			
	AE2	2,985,875	05/1961	Grisdale *et al.*			
	AF2	3,023,309	02/1962	Foulkes			
	AG2	3,069,679	12/1962	Sweeney *et al.*			
	AH2	3,104,393	09/1963	Vogelman			
	AI2	3,114,106	12/1963	McManus			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2	EP 0 380 351 A3	02/1991	EP			N/A
	AK2	EP 0 411 840 A2	02/1991	EP			N/A
	AL2	EP 0 411 840 A3	07/1991	EP			N/A
	AM2	EP 0 411 840 B1	10/1995	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN2	Allstot, D.J. *et al.*, "MOS Switched Capacitor Ladder Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 806-814 (December 1978).
	AO2	Allstot, D.J. and Black Jr. W.C., "Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 967-986 (August 1983).
	AP2	Alouini, M. *et al.*, "Channel Characterization and Modeling for Ka-Band Very Small Aperture Terminals," *Proceedings Of the IEEE*, IEEE, Vol. 85, No. 6, pp. 981-997 (June 1997).
	AQ2	Andreyev, G.A. and Ogarev, S.A., "Phase Distortions of Keyed Millimeter-Wave Signals in the Case of Propagation in a Turbulent Atmosphere," *Telecommunications and Radio Engineering*, Scripta Technica, Vol. 43, No. 12, pp. 87-90 (December 1988).
	AR2	Antonetti, A. *et al.*, "Optoelectronic Sampling in the Picosecond Range," *Optics Communications*, North-Holland Publishing Company, Vol. 21, No. 2, pp. 211-214 (May 1977).

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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. Sorrells	
FILING DATE	ART UNIT
October 27, 2004	2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	3,118,117	01/1964	King *et al.*			
	AB3	3,226,643	12/1965	McNair			
	AC3	3,258,694	06/1966	Shepherd			
	AD3	3,383,598	05/1968	Sanders			
	AE3	3,384,822	05/1968	Miyagi			
	AF3	3,454,718	07/1969	Perreault			
	AG3	3,523,291	08/1970	Pierret			
	AH3	3,548,342	12/1970	Maxey			
	AI3	3,555,428	01/1971	Perreault			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3	EP 0 423 718 A2	04/1991	EP			N/A
	AK3	EP 0 423 718 A3	08/1992	EP			N/A
	AL3	EP 0 486 095 A1	05/1992	EP			N/A
	AM3	EP 0 486 095 B1	02/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN3	Austin, J. *et al.*, "Doppler Correction of the Telecommunication Payload Oscillators in the UK T-SAT," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 851-857 (September 12 - 15, 1988).
	AO3	Auston, D.H., "Picosecond optoelectronic switching and gating in silicon," *Applied Physics Letters*, American Institute of Physics, Vol. 26, No. 3, pp. 101-103 (February 1, 1975).
	AP3	Baher, H., "Transfer Functions for Switched-Capacitor and Wave Digital Filters," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-33, No. 11, pp. 1138-1142 (November 1986).
	AQ3	Baines, R., "The DSP Bottleneck," *IEEE Communications Magazine*, IEEE Communications Society, pp. 46-54 (May 1995).
	AR3	Banjo, O.P. and Vilar, E., "Binary Error Probabilities on Earth-Space Links Subject to Scintillation Fading," *Electronics Letters*, IEE, Vol. 21, No. 7, pp. 296-297 (March 28, 1985).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	3,617,892	11/1971	Hawley *et al.*			
	AB4	3,621,402	11/1971	Gardner			
	AC4	3,623,160	11/1971	Giles *et al.*			
	AD4	3,626,417	12/1971	Gilbert			
	AE4	3,629,696	12/1971	Bartelink			
	AF4	3,662,268	05/1972	Gans *et al.*			
	AG4	3,689,841	09/1972	Bello *et al.*			
	AH4	3,714,577	01/1973	Hayes			
	AI4	3,717,844	02/1973	Barret *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4	EP 0 512 748 A2	11/1992	EP			N/A
	AK4	EP 0 512 748 A3	07/1993	EP			N/A
	AL4	EP 0 512 748 B1	11/1998	EP			N/A
	AM4	EP 0 548 542 A1	06/1993	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN4	Banjo, O.P. and Vilar, E., "The Dependence of Slant Path Amplitude Scintillations on Various Meteorological Parameters," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 277-280 (March 30 - April 2, 1987).
	AO4	Banjo, O.P. and Vilar, E. "Measurement and Modeling of Amplitude Scintillations on Low-Elevation Earth-Space Paths and Impact on Communication Systems," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. COM-34, No. 8, pp. 774-780 (August 1986).
	AP4	Banjo, O.P. *et al.*, "Tropospheric Amplitude Spectra Due to Absorption and Scattering in Earth-Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, IEE, pp. 77-82 (April 16-19, 1985).
	AQ4	Basili,P. *et al.*, "Case Study of Intense Scintillation Events on the OTS Path," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. 38, No. 1, pp. 107-113 (January 1990).
	AR4	Basili, P. *et al.*, "Observation of High C^2 and Turbulent Path Length on OTS Space-Earth Link," *Electronics Letters,* IEE, Vol. 24, No. 17, pp. 1114-1116 (August 18, 1988).

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	FIRST NAMED INVENTOR David F. Sorrells	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5	3,735,048	05/1973	Tomsa *et al.*			
	AB5	3,806,811	04/1974	Thompson			
	AC5	3,868,601	02/1975	MacAfee			
	AD5	3,949,300	04/1976	Sadler			
	AE5	3,967,202	06/1976	Batz			
	AF5	3,980,945	09/1976	Bickford			
	AG5	3,987,280	10/1976	Bauer			
	AH5	3,991,277	11/1976	Hirata			
	AI5	4,003,002	01/1977	Snijders *et al.*			

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	AJ5	EP 0 632 288 A2	01/1995	EP			N/A
	AK5	EP 0 632 288 A3	07/1996	EP			N/A
	AL5	EP 0 696 854 A1	02/1996	EP			N/A
	AM5	EP 0 782 275 A2	07/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN5	Blakey, J.R. *et al.*, "Measurement of Atmospheric Millimetre-Wave Phase Scintillations in an Absorption Region," *Electronics Letters*, IEE, Vol. 21, No. 11, pp. 486-487 (May 23, 1985).
	AO5	Burgueño, A. *et al.*, "Influence of rain gauge integration time on the rain rate statistics used in microwave communications," *annales des tèlècommunications*, International Union of Radio Science, pp. 522-527 (September/October 1988).
	AP5	Burgueño, A. *et al.*, "Long-Term Joint Statistical Analysis of Duration and Intensity of Rainfall Rate with Application to Microwave Communications," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 198-201 (March 30 - April 2, 1987).
	AQ5	Burgueño, A. *et al.*, "Long Term Statistics of Precipitation Rate Return Periods in the Context of Microwave Communications," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 297-301 (April 4-7, 1989).
	AR5	Burgueño, A. *et al.*, "Spectral Analysis of 49 Years of Rainfall Rate and Relation to Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 9, pp. 1359-1366 (September 1990).

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	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6	4,013,966	03/1977	Campbell			
	AB6	4,019,140	04/1977	Swerdlow			
	AC6	4,035,732	07/1977	Lohrmann			
	AD6	4,047,121	09/1977	Campbell			
	AE6	4,066,841	01/1978	Young			
	AF6	4,066,919	01/1978	Huntington			
	AG6	4,081,748	03/1978	Batz			
	AH6	4,130,765	12/1978	Arakelian *et al.*			
	AI6	4,130,806	12/1978	Van Gerwen *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6	EP 0 785 635 A1	07/1997	EP			No
	AK6	EP 0 795 978 A2	09/1997	EP			N/A
	AL6	EP 0 837 565 A1	04/1998	EP			N/A
	AM6	EP 0 862 274 A1	09/1998	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN6	Catalan, C. and Vilar, E., "Approach for satellite slant path remote sensing," *Electronics Letters,* IEE, Vol. 34, No. 12, pp. 1238-1240 (June 11, 1998).
	AO6	Chan, P. et al., "A Highly Linear 1-GHz CMOS Downconversion Mixer," *European Solid State Circuits Conference*, IEEE Communication Society, pp. 210-213 (September 22-24, 1993).
	AP6	Copy of Declaration of Michael J. Bultman filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AQ6	Copy of Declaration of Robert W. Cook filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AR6	Copy of Declaration of Alex Holtz filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 3 pages.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7	4,142,155	02/1979	Adachi			
	AB7	4,170,764	10/1979	Salz *et al.*			
	AC7	4,204,171	05/1980	Sutphin, Jr.			
	AD7	4,210,872	07/1980	Gregorian			
	AE7	4,245,355	01/1981	Pascoe *et al.*			
	AF7	4,253,066	02/1981	Fisher *et al.*			
	AG7	4,253,069	02/1981	Nossek			
	AH7	4,308,614	12/1981	Fisher *et al.*			
	AI7	4,320,361	03/1982	Kikkert			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7	EP 0 874 499 A2	10/1998	EP			N/A
	AK7	FR 2 743 231 A1	07/1997	FR			No
	AL7	GB 2 161 344 A	01/1986	GB			N/A
	AM7	GB 2 215 945 A	09/1989	GB			N/A

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN7	Copy of Declaration of Richard C. Looke filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AO7	Copy of Declaration of Charley D. Moses, Jr. filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AP7	Copy of Declaration of Jeffrey L. Parker and David F. Sorrells, with attachment Exhibit 1, filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 130 pages.
	AQ7	Dewey, R.J. and Collier, C.J., "Multi-Mode Radio Receiver," *Electronics Division Colloquium on Digitally Implemented Radios,* IEE, pp. 3/1-3/5 (October 18, 1985).
	AR7	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-276351, 1 page (November 13, 1990 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8	4,320,536	03/1982	Dietrich			
	AB8	4,346,477	08/1982	Gordy			
	AC8	4,355,401	10/1982	Ikoma *et al.*			
	AD8	4,356,558	10/1982	Owen *et al.*			
	AE8	4,360,867	11/1982	Gonda			
	AF8	4,363,132	12/1982	Collin			
	AG8	4,365,217	12/1982	Berger *et al.*			
	AH8	4,370,572	01/1983	Cosand *et al.*			
	AI8	4,389,579	06/1983	Stein			

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	AJ8	JP 2-39632	02/1990	JP			No
	AK8	JP 2-131629	05/1990	JP			No
	AL8	JP 2-276351	11/1990	JP			No
	AM8	WO 80/01633 A1	08/1980	PCT			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-131629, 1 page (May 21, 1990 - Date of publication of application).
	AO8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-39632, 1 page (February 8, 1990 - Date of publication of application).
	AP8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 0 785 635 A1, 3 pages (December 26, 1996 - Date of publication of application).
	AQ8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 35166 A1, 2 pages (February 18, 1981 - Date of publication of application).
	AR8	"DSO takes sampling rate to 1 Ghz," *Electronic Engineering*, Morgan Grampian Publishers, Vol. 59, No. 723, pp. 77 and 79 (March 1987).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9	4,392,255	07/1983	Del Giudice			
	AB9	4,430,629	02/1984	Betzl *et al.*			
	AC9	4,446,438	05/1984	Chang *et al.*			
	AD9	4,456,990	06/1984	Fisher *et al.*			
	AE9	4,472,785	09/1984	Kasuga			
	AF9	4,479,226	10/1984	Prabhu *et al.*			
	AG9	4,481,490	11/1984	Huntley			
	AH9	4,481,642	11/1984	Hanson			
	AI9	4,485,488	11/1984	Houdart			

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	AJ9	WO 94/05087 A1	03/1994	PCT			N/A
	AK9	WO 96/02977 A1	02/1996	PCT			N/A
	AL9	WO 96/08078 A1	03/1996	PCT			N/A
	AM9	WO 96/39750 A1	12/1996	PCT			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN9	Erdi, G. and Henneuse, P.R., "A Precision FET-Less Sample-and-Hold with High Charge-to-Droop Current Ratio," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 864-873 (December 1978).
	AO9	Faulkner, N.D. and Vilar, E., "Subharmonic Sampling for the Measurement of Short Term Stability of Microwave Oscillators," *IEEE Transactions on Instrumentation and Measurement*, IEEE, Vol. IM-32, No. 1, pp. 208-213 (March 1983).
	AP9	Faulkner, N.D. *et al.*, "Sub-Harmonic Sampling for the Accurate Measurement of Frequency Stability of Microwave Oscillators," *CPEM 82 Digest: Conference on Precision Electromagnetic Measurements*, IEEE, pp. M-10 and M-11 (1982).
	AQ9	Faulkner, N.D. and Vilar, E., "Time Domain Analysis of Frequency Stability Using Non-Zero Dead-Time Counter Techniques," *CPEM 84 Digest Conference on Precision Electromagnetic Measurements*, IEEE, pp. 81-82 (1984).
	AR9	Filip, M. and Vilar, E., "Optimum Utilization of the Channel Capacity of a Satellite Link in the Presence of Amplitude Scintillations and Rain Attenuation," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 11, pp. 1958-1965 (November 1990).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10	4,504,803	03/1985	Lee *et al.*			
	AB10	4,517,519	05/1985	Mukaiyama			
	AC10	4,517,520	05/1985	Ogawa			
	AD10	4,518,935	05/1985	van Roermund			
	AE10	4,521,892	06/1985	Vance *et al.*			
	AF10	4,563,773	07/1986	Dixon, Jr. *et al.*			
	AG10	4,577,157	03/1986	Reed			
	AH10	4,583,239	04/1986	Vance			
	AI10	4,591,736	05/1986	Hirao *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ10	WO 97/38490 A1	10/1997	PCT			N/A
	AK10	WO 98/00953 A1	01/1998	PCT			N/A
	AL10	WO 98/24201 A1	06/1998	PCT			N/A
	AM10	EP 0 099 265 A1	01/1984	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN10	Fukahori, K., "A CMOS Narrow-Band Signaling Filter with Q Reduction," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-19, No. 6, pp. 926-932 (December 1984).
	AO10	Fukuchi, H. and Otsu, Y., "Available time statistics of rain attenuation on earth-space path," *IEE Proceedings-H: Microwaves, Antennas and Propagation*, IEE, Vol. 135, Pt. H, No. 6, pp. 387-390 (December 1988).
	AP10	Gibbins, C.J. and Chadha, R., "Millimetre-wave propagation through hydrocarbon flame," *IEE Proceedings*, IEE, Vol. 134, Pt. H, No.2 , pp. 169-173 (April 1987).
	AQ10	Gilchrist, B. *et al.*, "Sampling hikes performance of frequency synthesizers," *Microwaves & RF*, Hayden Publishing, Vol. 23, No. 1, pp. 93-94 and 110 (January 1984).
	AR10	Gossard, E.E., "Clear weather meteorological effects on propagation at frequencies above 1 Ghz," *Radio Science*, American Geophysical Union, Vol. 16, No. 5, pp. 589-608 (September - October 1981).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA11	4,602,220	07/1986	Kurihara			
	AB11	4,603,300	07/1986	Welles, II *et al.*			
	AC11	4,612,464	09/1986	Ishikawa *et al.*			
	AD11	4,612,518	09/1986	Gans *et al.*			
	AE11	4,616,191	10/1986	Galani *et al.*			
	AF11	4,621,217	11/1986	Saxe *et al.*			
	AG11	4,628,517	12/1986	Schwarz *et al.*			
	AH11	4,634,998	01/1987	Crawford			
	AI11	4,648,021	03/1987	Alberkrack			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ11	EP 0 560 228 A1	09/1993	EP			N/A
	AK11	FR 2 245 130	04/1975	FR			Yes (See AP50)
	AL11	DE 35 41 031 A1	05/1986	DE			Yes (See AR50)
	AM11	EP 0 732 803 A1	09/1996	EP			Yes (See AN51)

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN11	Gregorian, R. *et al.*, "Switched-Capacitor Circuit Design," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 941-966 (August 1983).
	AO11	Groshong *et al.*, "Undersampling Techniques Simplify Digital Radio," *Electronic Design*, Penton Publishing, pp. 67-68, 70, 73-75 and 78 (May 23, 1991).
	AP11	Grove, W.M., "Sampling for Oscilloscopes and Other RF Systems: Dc through X-Band," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, pp. 629-635 (December 1966).
	AQ11	Haddon, J. *et al.*, "Measurement of Microwave Scintillations on a Satellite Down-Link at X-Band," *Antennas and Propagation*, IEE, pp. 113-117 (1981).
	AR11	Haddon, J. and Vilar, E., "Scattering Induced Microwave Scintillations from Clear Air and Rain on Earth Space Paths and the Influence of Antenna Aperture," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 5, pp. 646-657 (May 1986).

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	AA12	4,651,034	03/1987	Sato			
	AB12	4,675,882	06/1987	Lillie *et al.*			
	AC12	4,688,253	08/1987	Gumm			
	AD12	4,716,376	12/1987	Daudelin			
	AE12	4,716,388	12/1987	Jacobs			
	AF12	4,718,113	01/1988	Rother *et al.*			
	AG12	4,726,041	02/1988	Prohaska *et al.*			
	AH12	4,733,403	03/1988	Simone			
	AI12	4,734,591	03/1988	Ichitsubo			

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	AJ12	DE 197 35 798 C1	07/1998	DE			Yes (See AP51)
	AK12	WO 98/40968 A2&A3	09/1998	PCT			N/A
	AL12	EP 0 529 836 A1	03/1993	EP			N/A
	AM12	EP 0 795 955 A2&A3	09/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN12	Hafdallah, H. *et al.*, "2-4 Ghz MESFET Sampler," *Electronics Letters*, IEE, Vol. 24, No. 3, pp. 151-153 (February 4, 1988).
	AO12	Herben, M.H.A.J., "Amplitude and Phase Scintillation Measurements on 8-2 km Line-Of-Sight Path at 30 Ghz," *Electronics Letters*, IEE, Vol. 18, No. 7, pp. 287-289 (April 1, 1982).
	AP12	Hewitt, A. *et al.*, "An 18 Ghz Wideband LOS Multipath Experiment," *International Conference on Measurements for Telecommunication Transmission Systems - MTTS 85*, IEE, pp. 112-116 (November 27-28, 1985)
	AQ12	Hewitt, A. *et al.*, "An Autoregressive Approach to the Identification of Multipath Ray Parameters from Field Measurements," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 37, No. 11, pp. 1136-1143 (November 1989).
	AR12	Hewitt, A. and Vilar, E., "Selective fading on LOS Microwave Links: Classical and Spread-Spectrum Measurement Techniques," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 36, No. 7, pp. 789-796 (July 1988).

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	AA13	4,737,969	04/1988	Steel *et al.*			
	AB13	4,743,858	05/1988	Everard			
	AC13	4,745,463	05/1988	Lu			
	AD13	4,751,468	06/1988	Agoston			
	AE13	4,757,538	07/1988	Zink			
	AF13	4,768,187	08/1988	Marshall			
	AG13	4,769,612	09/1988	Tamakoshi *et al.*			
	AH13	4,785,463	11/1988	Janc *et al.*			
	AI13	4,791,584	12/1988	Greivenkamp, Jr.			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ13	EP 0 817 369 A2&A3	01/1998	EP			N/A
	AK13	WO 91/18445 A1	11/1991	PCT			N/A
	AL13	WO 99/23755 A1	05/1999	PCT			N/A
	AM13	JP 56-114451	09/1981	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN13	Hospitalier, E., "Instruments for Recording and Observing Rapidly Varying Phenomena," *Science Abstracts*, IEE, Vol. VII, pp. 22-23 (1904).
	AO13	Howard, I.M. and Swansson, N.S., "Demodulating High Frequency Resonance Signals for Bearing Fault Detection," *The Institution of Engineers Australia Vibration and Noise Conference*, Institution of Engineers, Australia, pp. 115-121 (September 18-20, 1990).
	AP13	Hu, X., *A Switched-Current Sample-and-Hold Amplifier for FM Demodulation*, Thesis for Master of Applied Science, Dept. of Electrical and Computer Engineering, University of Toronto, UMI Dissertation Services, pp. 1-64 (1995).
	AQ13	Hung, H-L. A. *et al.*, "Characterization of Microwave Integrated Circuits Using An Optical Phase-Locking and Sampling System," *IEEE MTT-S Digest*, IEEE, pp. 507-510 (1991).
	AR13	Hurst, P.J., "Shifting the Frequency Response of Switched-Capacitor Filters by Nonuniform Sampling," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. 38, No. 1, pp. 12-19 (January 1991).

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	AA14	4,801,823	01/1989	Yokoyama			
	AB14	4,806,790	02/1989	Sone			
	AC14	4,810,904	03/1989	Crawford			
	AD14	4,810,976	03/1989	Cowley *et al.*			
	AE14	4,811,362	03/1989	Yester, Jr. *et al.*			
	AF14	4,819,252	04/1989	Christopher			
	AG14	4,833,445	05/1989	Buchele			
	AH14	4,862,121	08/1989	Hochschild *et al.*			
	AI14	4,868,654	09/1989	Juri *et al.*			

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	AJ14	JP 8-32556	02/1996	JP			No
	AK14	JP 8-139524	05/1996	JP			No
	AL14	JP 59-144249	08/1984	JP			No
	AM14	JP 63-54002	03/1988	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN14	Itakura, T., "Effects of the sampling pulse width on the frequency characteristics of a sample-and-hold circuit," *IEE Proceedings Circuits, Devices and Systems,* IEE, Vol. 141, No. 4, pp. 328-336 (August 1994).
	AO14	Janssen, J.M.L., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: I. Fundamentals," *Philips Technical Review,* Philips Research Laboratories, Vol. 12, No. 2, pp. 52-59 (August 1950).
	AP14	Janssen, J.M.L. and Michels, A.J., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: II. Electrical Build-Up," *Philips Technical Review*, Philips Research Laboratories, Vol. 12, No. 3, pp. 73-82 (September 1950).
	AQ14	Jondral, V.F. *et al.*, "Doppler Profiles for Communication Satellites," *Frequenz*, Herausberger, pp. 111-116 (May-June 1996).
	AR14	Kaleh, G.K., "A Frequency Diversity Spread Spectrum System for Communication in the Presence of In-band Interference," *1995 IEEE Globecom*, IEEE Communications Society, pp. 66-70 (1995).

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	AA15	4,870,659	09/1989	Oishi *et al.*			
	AB15	4,871,987	10/1989	Kawase			
	AC15	4,885,587	12/1989	Wiegand *et al.*			
	AD15	4,885,756	12/1989	Fontanes *et al.*			
	AE15	4,888,557	12/1989	Puckette, IV *et al.*			
	AF15	4,890,302	12/1989	Muilwijk			
	AG15	4,893,316	01/1990	Janc *et al.*			
	AH15	4,893,341	01/1990	Gehring			
	AI15	4,894,766	01/1990	De Agro			

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	AJ15	JP 6-237276	08/1994	JP			No
	AK15	JP 8-23359	01/1996	JP			No
	AL15	JP 47-2314	02/1972	JP			Yes (See AP53)
	AM15	JP 58-7903	01/1983	JP			Yes (See AQ53)

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN15	Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).
	AO15	Kirsten, J. and Fleming, J., "Undersampling reduces data-acquisition costs for select applications," *EDN*, Cahners Publishing, Vol. 35, No. 13, pp. 217-222, 224, 226-228 (June 21, 1990).
	AP15	Lam, W.K. *et al.*, "Measurement of the Phase Noise Characteristics of an Unlocked Communications Channel Identifier," *Proceedings Of the 1993 IEEE International Frequency Control Symposium*, IEEE, pp. 283-288 (June 2-4, 1993).
	AQ15	Lam, W.K. *et al.*, "Wideband sounding of 11.6 Ghz transhorizon channel," *Electronics Letters*, IEE, Vol. 30, No. 9, pp. 738-739 (April 28, 1994).
	AR15	Larkin, K.G., "Efficient demodulator for bandpass sampled AM signals," *Electronics Letters*, IEE, Vol. 32, No. 2, pp. 101-102 (January 18, 1996).

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	AA16	4,896,152	01/1990	Tiemann			
	AB16	4,902,979	02/1990	Puckette, IV			
	AC16	4,908,579	03/1990	Tawfik *et al.*			
	AD16	4,910,752	03/1990	Yester, Jr. *et al.*			
	AE16	4,914,405	04/1990	Wells			
	AF16	4,920,510	04/1990	Senderowicz *et al.*			
	AG16	4,922,452	05/1990	Larsen *et al.*			
	AH16	4,931,921	06/1990	Anderson			
	AI16	4,944,025	07/1990	Gehring *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ16	JP 58-133004	08/1983	JP			No
	AK16	JP 60-58705	04/1985	JP			No
	AL16	JP 4-123614	04/1992	JP			No
	AM16	JP 4-127601	04/1992	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN16	Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).
	AO16	Lau, W.H. *et al.*, "Improved Prony Algorithm to Identify Multipath Components," *Electronics Letters*, IEE, Vol. 23, No. 20, pp. 1059-1060 (September 24, 1987).
	AP16	Lesage, P. and Audoin, C., "Effect of Dead-Time on the Estimation of the Two-Sample Variance," *IEEE Transactions on Instrumentation and Measurement*, IEEE Instrumentation and Measurement Society, Vol. IM-28, No. 1, pp. 6-10 (March 1979).
	AQ16	Liechti, C.A., "Performance of Dual-gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. MTT-23, No. 6, pp. 461-469 (June 1975).
	AR16	Linnenbrink, T.E. *et al.*, "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No. 4, pp. 4443-4449 (August 1979).

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	AA17	4,955,079	09/1990	Connerney *et al.*			
	AB17	4,965,467	10/1990	Bilterijst			
	AC17	4,967,160	10/1990	Quievy *et al.*			
	AD17	4,970,703	11/1990	Hariharan *et al.*			
	AE17	4,982,353	01/1991	Jacob *et al.*			
	AF17	4,984,077	01/1991	Uchida			
	AG17	4,995,055	02/1991	Weinberger *et al.*			
	AH17	5,003,621	03/1991	Gailus			
	AI17	5,005,169	04/1991	Bronder *et al.*			

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	AJ17	JP 5-175730	07/1993	JP			No
	AK17	JP 5-175734	07/1993	JP			No
	AL17	JP 7-154344	06/1995	JP			No
	AM17	JP 7-307620	11/1995	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN17	Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).
	AO17	Lo, P. *et al.*, "Coherent Automatic Gain Control," *IEE Colloquium on Phase Locked Techniques*, IEE, pp. 2/1-2/6 (March 26, 1980).
	AP17	Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).
	AQ17	Lo, P.S.L.O. *et al.*, "Observations of Amplitude Scintillations on a Low-Elevation Earth-Space Path," *Electronics Letters*, IEE, Vol. 20, No. 7, pp. 307-308 (March 29, 1984).
	AR17	Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

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	AA18	5,006,810	04/1991	Popescu			
	AB18	5,010,585	04/1991	Garcia			
	AC18	5,014,304	05/1991	Nicollini *et al.*			
	AD18	5,015,963	05/1991	Sutton			
	AE18	5,017,924	05/1991	Guiberteau *et al.*			
	AF18	5,020,149	05/1991	Hemmie			
	AG18	5,020,154	05/1991	Zierhut			
	AH18	5,052,050	09/1991	Collier *et al.*			
	AI18	5,065,409	11/1991	Hughes *et al.*			

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	AJ18	JP 55-66057	05/1980	JP			No
	AK18	JP 63-65587	03/1988	JP			No
	AL18	JP 63-153691	06/1988	JP			No
	AM18	EP 0 276 130 A2&A3	07/1988	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN18	Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).
	AO18	Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).
	AP18	Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).
	AQ18	Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).
	AR18	McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

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	AA19	5,083,050	01/1992	Vasile			
	AB19	5,091,921	02/1992	Minami			
	AC19	5,095,533	03/1992	Loper *et al.*			
	AD19	5,095,536	03/1992	Loper			
	AE19	5,111,152	05/1992	Makino			
	AF19	5,113,094	05/1992	Grace *et al.*			
	AG19	5,113,129	05/1992	Hughes			
	AH19	5,122,765	06/1992	Pataut			
	AI19	5,124,592	06/1992	Hagino			

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	AJ19	WO 95/01006 A1	01/1995	PCT			N/A
	AK19	WO 97/08839 A2&A3	03/1997	PCT			N/A
	AL19	EP 0 254 844 A2	02/1988	EP			N/A
	AM19	EP 0 632 577 A1	01/1995	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN19	Merkelo, J. and Hall, R.D., "Broad-Band Thin-Film Signal Sampler," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-7, No. 1, pp. 50-54 (February 1972).
	AO19	Merlo, U. *et al.*, "Amplitude Scintillation Cycles in a Sirio Satellite-Earth Link," *Electronics Letters*, IEE, Vol. 21, No. 23, pp. 1094-1096 (November 7, 1985).
	AP19	Morris, D., "Radio-holographic reflector measurement of the 30-m millimeter radio telescope at 22 Ghz with a cosmic signal source," *Astronomy and Astrophysics*, Springer-Verlag, Vol. 203, No. 2, pp. 399-406 (September (II) 1988).
	AQ19	Moulsley, T.J. *et al.*, "The efficient acquisition and processing of propagation statistics," *Journal of the Institution of Electronic and Radio Engineers*, IERE, Vol. 55, No. 3, pp. 97-103 (March 1985).
	AR19	Ndzi, D. *et al.*, "Wide-Band Statistical Characterization of an Over-the-Sea Experimental Transhorizon Link," *IEE Colloquium on Radio Communications at Microwave and Millimetre Wave Frequencies*, IEE, pp. 1/1-1/6 (December 16, 1996).

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	AA20	5,136,267	08/1992	Cabot			
	AB20	5,140,705	08/1992	Kosuga			
	AC20	5,150,124	09/1992	Moore *et al.*			
	AD20	5,151,661	09/1992	Caldwell *et al.*			
	AE20	5,159,710	10/1992	Cusdin			
	AF20	5,170,414	12/1992	Silvian			
	AG20	5,172,070	12/1992	Hiraiwa *et al.*			
	AH20	5,191,459	03/1993	Thompson *et al.*			
	AI20	5,204,642	04/1993	Ashgar *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ20	JP 60-130203	07/1985	JP			Yes (See AO56)
	AK20	DE 196 27 640 A1	01/1997	DE			No
	AL20	EP 0 087 336 A1	08/1983	EP			No
	AM20	EP 0 087 336 B1	07/1986	EP			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN20	Ndzi, D. *et al.*, "Wideband Statistics of Signal Levels and Doppler Spread on an Over-The-Sea Transhorizon Link," *IEE Colloquium on Propagation Characteristics and Related System Techniques for Beyond Line-of-Sight Radio*, IEE, pp. 9/1-9/6 (November 24, 1997).
	AO20	"New zero IF chipset from Philips," *Electronic Engineering*, United News & Media, Vol. 67, No. 825, p. 10 (September 1995).
	AP20	Ohara, H. *et al.*, "First monolithic PCM filter cuts cost of telecomm systems," *Electronic Design*, Hayden Publishing Company, Vol. 27, No. 8, pp. 130-135 (April 12, 1979).
	AQ20	Oppenheim, A.V. *et al.*, *Signals and Systems*, Prentice-Hall, pp. 527-531 and 561-562 (1983).
	AR20	Ortgies, G., "Experimental Parameters Affecting Amplitude Scintillation Measurements on Satellite Links," *Electronics Letters*, IEE, Vol. 21, No. 17, pp. 771-772 (August 15, 1985).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA21	5,212,827	05/1993	Meszko *et al.*			
	AB21	5,214,787	05/1993	Karkota, Jr.			
	AC21	5,220,583	06/1993	Solomon			
	AD21	5,220,680	06/1993	Lee			
	AE21	5,222,144	06/1993	Whikehart			
	AF21	5,230,097	07/1993	Currie *et al.*			
	AG21	5,239,686	08/1993	Downey			
	AH21	5,241,561	08/1993	Barnard			
	AI21	5,249,203	09/1993	Loper			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ21	EP 0 789 449 A2 & A3	08/1997	EP			N/A
	AK21	FR 2 669 787 A1	05/1992	FR			No
	AL21	GB 2 324 919 A	11/1998	GB			N/A
	AM21	JP 61-30821	02/1986	JP			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN21	Pärssinen et al., "A 2-GHz Subharmonic Sampler for Signal Downconversion," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 45, No. 12, 7 pages (December 1997).
	AO21	Peeters, G. *et al.*, "Evaluation of Statistical Models for Clear-Air Scintillation Prediction Using Olympus Satellite Measurements," *International Journal of Satellite Communications*, John Wiley and Sons, Vol. 15, No. 2, pp. 73-88 (March-April 1997).
	AP21	Perrey, A.G. and Schoenwetter, H.K., *NBS Technical Note 1121: A Schottky Diode Bridge Sampling Gate*, U.S. Dept. of Commerce, pp. 1-14 (May 1980).
	AQ21	Poulton, K. *et al.*, "A 1-Ghz 6-bit ADC System," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-22, No. 6, pp. 962-969 (December 1987).
	AR21	Press Release, "Parkervision, Inc. Announces Fiscal 1993 Results," Lippert/Heilshorn and Associates, 2 Pages (April 6, 1994).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA22	5,251,218	10/1993	Stone *et al.*			
	AB22	5,251,232	10/1993	Nonami			
	AC22	5,260,970	11/1993	Henry *et al.*			
	AD22	5,263,194	11/1993	Ragan			
	AE22	5,263,196	11/1993	Jasper			
	AF22	5,267,023	11/1993	Kawasaki			
	AG22	5,278,826	01/1994	Murphy *et al.*			
	AH22	5,282,023	01/1994	Scarpa			
	AI22	5,287,516	02/1994	Schaub			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ22	JP 5-327356	12/1993	JP			No
	AK22	EP 0 643 477 A2 & A3	03/1995	EP			N/A
	AL22	EP 0 877 476 A1	11/1998	EP			N/A
	AM22	EP 0 977 351 A1	02/2000	EP			N/A

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN22	Press Release, "Parkervision, Inc. Announces the Appointment of Michael Baker to the New Position of National Sales Manager," Lippert/Heilshorn and Associates, 1 Page (April 7, 1994).
	AO22	Press Release, "Parkervision's Cameraman Well-Received By Distance Learning Market," Lippert/Heilshorn and Associates, 2 Pages (April 8, 1994).
	AP22	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 2 Pages (April 26, 1994).
	AQ22	Press Release, "Parkervision, Inc. Announces The Retirement of William H. Fletcher, Chief Financial Officer," Lippert/Heilshorn and Associates, 1 Page (May 11, 1994).
	AR22	Press Release, "Parkervision, Inc. Announces New Cameraman System II™ At Infocomm Trade Show," Lippert/Heilshorn and Associates, 3 Pages (June 9, 1994).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*NAME*	*CLASS*	*SUB-CLASS*	*FILING DATE*
	AA23	5,293,398	03/1994	Hamao *et al.*			
	AB23	5,303,417	04/1994	Laws			
	AC23	5,307,517	04/1994	Rich			
	AD23	5,315,583	05/1994	Murphy *et al.*			
	AE23	5,321,852	06/1994	Seong			
	AF23	5,325,204	06/1994	Scarpa			
	AG23	5,337,014	08/1994	Najle *et al.*			
	AH23	5,339,054	08/1994	Taguchi			
	AI23	5,339,459	08/1994	Schiltz *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*COUNTRY*	*CLASS*	*SUB-CLASS*	*TRANSLATION*
	AJ23	WO 00/31659 A1	06/2000	PCT			N/A
	AK23	JP 9-36664	02/1997	JP			No
	AL23	DE 196 48 915 A1	06/1998	DE			Yes (See AO59)
	AM23						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	*DOC. REF.*	*CITATION*
	AN23	Press Release, "Parkervision, Inc. Announces Appointments to its National Sales Force," Lippert/Heilshorn and Associates, 2 Pages (June 17, 1994).
	AO23	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (August 9, 1994).
	AP23	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (October 28, 1994).
	AQ23	Press Release, "Parkervision, Inc. Announces First Significant Dealer Sale of Its *Cameraman*® System II," Lippert/Heilshorn and Associates, 2 Pages (November 7, 1994).
	AR23	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Lippert/Heilshorn and Associates, 2 Pages (March 1, 1995).

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	AA24	5,355,114	10/1994	Sutterlin *et al.*			
	AB24	5,361,408	11/1994	Watanabe *et al.*			
	AC24	5,369,800	11/1994	Takagi *et al.*			
	AD24	5,375,146	12/1994	Chalmers			
	AE24	5,379,040	01/1995	Mizomoto *et al.*			
	AF24	5,379,141	01/1995	Thompson *et al.*			
	AG24	5,388,063	02/1995	Takatori *et al.*			
	AH24	5,390,364	02/1995	Webster *et al.*			
	AI24	5,400,084	03/1995	Scarpa			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ24						Yes No
	AK24						Yes No
	AL24						Yes No
	AM24						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN24	Press Release, "Parkervision, Inc. Announces Joint Product Developments With VTEL," Lippert/Heilshorn and Associates, 2 Pages (March 21, 1995).
	AO24	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 3 Pages (April 28, 1995).
	AP24	Press Release, "Parkervision Wins Top 100 Product Districts' Choice Award," Parkervision Marketing and Manufacturing Headquarters, 1 Page (June 29, 1995).
	AQ24	Press Release, "Parkervision National Sales Manager Next President of USDLA," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 6, 1995).
	AR24	Press Release, "Parkervision Granted New Patent," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 21, 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA25	5,404,127	04/1995	Lee *et al.*			
	AB25	5,410,541	04/1995	Hotto			
	AC25	5,410,743	04/1995	Seely *et al.*			
	AD25	5,412,352	05/1995	Graham			
	AE25	5,416,803	05/1995	Janer			
	AF25	5,422,913	06/1995	Wilkinson			
	AG25	5,423,082	06/1995	Cygan *et al.*			
	AH25	5,428,638	06/1995	Cioffi *et al.*			
	AI25	5,428,640	06/1995	Townley			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ25						Yes No
	AK25						Yes No
	AL25						Yes No
	AM25						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN25	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 31, 1995).
	AO25	Press Release, "Parkervision, Inc. Expands Its Cameraman System II Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 22, 1995).
	AP25	Press Release, "Parkervision Announces New Camera Control Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 25, 1995).
	AQ25	Press Release, "Parkervision, Inc. Announces Completion of VTEL/Parkervision Joint Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).
	AR25	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA26	5,434,546	07/1995	Palmer			
	AB26	5,438,692	08/1995	Mohindra			
	AC26	5,444,415	08/1995	Dent *et al.*			
	AD26	5,444,416	08/1995	Ishikawa *et al.*			
	AE26	5,444,865	08/1995	Heck *et al.*			
	AF26	5,446,421	08/1995	Kechkaylo			
	AG26	5,446,422	08/1995	Mattila *et al.*			
	AH26	5,448,602	09/1995	Ohmori *et al.*			
	AI26	5,451,899	09/1995	Lawton			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ26						Yes No
	AK26						Yes No
	AL26						Yes No
	AM26						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN26	Press Release, "Parkervision's Cameraman Personal Locator Camera System Wins Telecon XV Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (November 1, 1995).
	AO26	Press Release, "Parkervision, Inc. Announces Purchase Commitment From VTEL Corporation," Parkervision Marketing and Manufacturing Headquarters, 1 Page (February 26, 1996).
	AP26	Press Release, "ParkerVision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (February 27, 1996).
	AQ26	Press Release, "ParkerVision, Inc. Expands its Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 7, 1996).
	AR26	Press Release, "ParkerVision Files Patents for its Research of Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 1 Page (March 28, 1996).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA27	5,454,007	09/1995	Dutta			
	AB27	5,454,009	09/1995	Fruit *et al.*			
	AC27	5,463,356	10/1995	Palmer			
	AD27	5,463,357	10/1995	Hobden			
	AE27	5,465,071	11/1995	Kobayashi *et al.*			
	AF27	5,465,410	11/1995	Hiben *et al.*			
	AG27	5,465,415	11/1995	Bien			
	AH27	5,471,162	11/1995	McEwan			
	AI27	5,479,120	12/1995	McEwan			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ27						Yes No
	AK27						Yes No
	AL27						Yes No
	AM27						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN27	Press Release, "Parkervision, Inc. Announces First Significant Sale of Its Cameraman® Three-Chip System," Parkervision Marketing and Manufacturing Headquarters, 2 pages (April 12, 1996).
	AO27	Press Release, "Parkervision, Inc. Introduces New Product Line For Studio Production Market," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1996).
	AP27	Press Release, "Parkervision, Inc. Announces Private Placement of 800,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 1 Page (April 15, 1996).
	AQ27	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 30, 1996).
	AR27	Press Release, "ParkerVision's New Studio Product Wins Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (June 5, 1996).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA28	5,479,447	12/1995	Chow *et al.*			
	AB28	5,483,193	01/1996	Kennedy *et al.*			
	AC28	5,483,549	01/1996	Weinberg *et al.*			
	AD28	5,483,691	01/1996	Heck *et al.*			
	AE28	5,490,173	02/1996	Whikehart *et al.*			
	AF28	5,493,581	02/1996	Young *et al.*			
	AG28	5,493,721	02/1996	Reis			
	AH28	5,495,200	02/1996	Kwan *et al.*			
	AI28	5,495,202	02/1996	Hsu			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ28						Yes No
	AK28						Yes No
	AL28						Yes No
	AM28						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN28	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (August 1, 1996).
	AO28	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 29, 1996).
	AP28	Press Release, "PictureTel and ParkerVision Sign Reseller Agreement," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1996).
	AQ28	Press Release, "CLI and ParkerVision Bring Enhanced Ease-of-Use to Videoconferencing," CLI/Parkervision, 2 Pages (January 20, 1997).
	AR28	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (February 27, 1997).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA29	5,495,500	02/1996	Jovanovich *et al.*			
	AB29	5,499,267	03/1996	Ohe *et al.*			
	AC29	5,500,758	03/1996	Thompson *et al.*			
	AD29	5,517,688	05/1996	Fajen *et al.*			
	AE29	5,519,890	05/1996	Pinckley			
	AF29	5,523,719	06/1996	Longo *et al.*			
	AG29	5,523,726	06/1996	Kroeger *et al.*			
	AH29	5,523,760	06/1996	McEwan			
	AI29	5,539,770	07/1996	Ishigaki			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ29						Yes No
	AK29						Yes No
	AL29						Yes No
	AM29						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN29	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 29, 1997).
	AO29	Press Release, "NEC and Parkervision Make Distance Learning Closer," NEC America, 2 Pages (June 18, 1997).
	AP29	Press Release, "Parkervision Supplies JPL with Robotic Cameras, Cameraman Shot Director for Mars Mission," Parkervision Marketing and Manufacturing Headquarters, 2 pages (July 8, 1997).
	AQ29	Press Release, "ParkerVision and IBM Join Forces to Create Wireless Computer Peripherals," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 23, 1997).
	AR29	Press Release, "ParkerVision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 31, 1997).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA30	5,555,453	09/1996	Kajimoto *et al.*			
	AB30	5,557,641	09/1996	Weinberg			
	AC30	5,557,642	09/1996	Williams			
	AD30	5,579,341	11/1996	Smith *et al.*			
	AE30	5,579,347	11/1996	Lindquist *et al.*			
	AF30	5,584,068	12/1996	Mohindra			
	AG30	5,592,131	01/1997	Labreche *et al.*			
	AH30	5,602,847	02/1997	Pagano *et al.*			
	AI30	5,602,868	02/1997	Wilson			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ30						Yes No
	AK30						Yes No
	AL30						Yes No
	AM30						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN30	Press Release, "Parkervision, Inc. Announces Private Placement of 990,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 8, 1997).
	AO30	Press Release, "Wal-Mart Chooses Parkervision for Broadcast Production," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 24, 1997).
	AP30	Press Release, "Parkervision, Inc. Announces Third Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1997).
	AQ30	Press Release, "ParkerVision Announces Breakthrough in Wireless Radio Frequency Technology," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 10, 1997).
	AR30	Press Release, "Parkervision, Inc. Announces the Appointment of Joseph F. Skovron to the Position of Vice President, Licensing - Wireless Technologies," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 9, 1998).

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	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA31	5,604,732	02/1997	Kim *et al.*			
	AB31	5,608,531	03/1997	Honda *et al.*			
	AC31	5,610,946	03/1997	Tanaka *et al.*			
	AD31	RE 35,494	04/1997	Nicollini			
	AE31	5,617,451	04/1997	Mimura *et al.*			
	AF31	5,619,538	04/1997	Sempel *et al.*			
	AG31	5,621,455	04/1997	Rogers *et al.*			
	AH31	5,630,227	05/1997	Bella *et al.*			
	AI31	5,640,415	06/1997	Pandula			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ31						Yes No
	AK31						Yes No
	AL31						Yes No
	AM31						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN31	Press Release, "Parkervision Announces Existing Agreement with IBM Terminates-- Company Continues with Strategic Focus Announced in December," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 27, 1998).
	AO31	Press Release, "Laboratory Tests Verify Parkervision Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 3, 1998).
	AP31	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1998).
	AQ31	Press Release, "Parkervision Awarded Editors' Pick of Show for NAB 98," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1998).
	AR31	Press Release, "Parkervision Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (May 4, 1998).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA32	5,640,424	06/1997	Banavong *et al.*			
	AB32	5,640,428	06/1997	Abe *et al.*			
	AC32	5,640,698	06/1997	Shen *et al.*			
	AD32	5,648,985	07/1997	Bjerede *et al.*			
	AE32	5,650,785	07/1997	Rodal			
	AF32	5,661,424	08/1997	Tang			
	AG32	5,663,878	09/1997	Walker			
	AH32	5,663,986	09/1997	Striffler			
	AI32	5,668,836	09/1997	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ32						Yes No
	AK32						Yes No
	AL32						Yes No
	AM32						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN32	Press Release, "Parkervision 'DIRECT2DATA' Introduced in Response to Market Demand," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 9, 1998).
	AO32	Press Release, "Parkervision Expands Senior Management Team," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 29, 1998).
	AP32	Press Release, "Parkervision Announces Second Quarter and Six Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 4 Pages (July 30, 1998).
	AQ32	Press Release, "Parkervision Announces Third Quarter and Nine Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1998).
	AR32	Press Release, "Questar Infocomm, Inc. Invests $5 Million in Parkervision Common Stock," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 2, 1998).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA33	5,680,078	10/1997	Ariie			
	AB33	5,680,418	10/1997	Croft *et al.*			
	AC33	5,689,413	11/1997	Jaramillo *et al.*			
	AD33	5,699,006	12/1997	Zele *et al.*			
	AE33	5,705,955	01/1998	Freeburg *et al.*			
	AF33	5,710,998	01/1998	Opas			
	AG33	5,714,910	02/1998	Skoczen *et al.*			
	AH33	5,715,281	02/1998	Bly *et al.*			
	AI33	5,721,514	02/1998	Crockett *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ33						Yes No
	AK33						Yes No
	AL33						Yes No
	AM33						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN33	Press Release, "Parkervision Adds Two New Directors," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 5, 1999).
	AO33	Press Release, "Parkervision Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1999).
	AP33	Press Release, "Joint Marketing Agreement Offers New Automated Production Solution," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 13, 1999).
	AQ33	"Project COST 205: Scintillations in Earth-satellite links," *Alta Frequenza: Scientific Review in Electronics*, AEI, Vol. LIV, No. 3, pp. 209-211 (May-June, 1985).
	AR33	Razavi, B., *RF Microelectronics*, Prentice-Hall, pp. 147-149 (1998).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA34	5,724,002	03/1998	Hulick			
	AB34	5,724,653	03/1998	Baker *et al.*			
	AC34	5,729,577	03/1998	Chen			
	AD34	5,729,829	03/1998	Talwar *et al.*			
	AE34	5,732,333	03/1998	Cox *et al.*			
	AF34	5,736,895	04/1998	Yu *et al.*			
	AG34	5,737,035	04/1998	Rotzoll			
	AH34	5,742,189	04/1998	Yoshida *et al.*			
	AI34	5,748,683	05/1998	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ34						Yes No
	AK34						Yes No
	AL34						Yes No
	AM34						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN34	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 1)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 373, pp. 130-137 (March 1959).
	AO34	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 2)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 374, pp. 204-212 (April 1959).
	AP34	Rein, H.M. and Zahn, M., "Subnanosecond-Pulse Generator with Variable Pulsewidth Using Avalanche Transistors," *Electronics Letters*, IEE, Vol. 11, No. 1, pp. 21-23 (January 9, 1975).
	AQ34	Riad, S.M. and Nahman, N.S., "Modeling of the Feed-through Wideband (DC to 12.4 Ghz) Sampling-Head," *IEEE MTT-S International Microwave Symposium Digest*, IEEE, pp. 267-269 (June 27-29, 1978).
	AR34	Rizzoli, V. *et al.*, "Computer-Aided Noise Analysis of MESFET and HEMT Mixers," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 37, No. 9, pp. 1401-1410 (September 1989).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA35	RE 35,829	06/1998	Sanderford, Jr.			
	AB35	5,760,645	06/1998	Comte *et al.*			
	AC35	5,764,087	06/1998	Clark			
	AD35	5,767,726	06/1998	Wang			
	AE35	5,768,118	06/1998	Faulk *et al.*			
	AF35	5,771,442	06/1998	Wang *et al.*			
	AG35	5,777,692	07/1998	Ghosh			
	AH35	5,777,771	07/1998	Smith			
	AI35	5,786,844	07/1998	Rogers *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ35						Yes No
	AK35						Yes No
	AL35						Yes No
	AM35						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN35	Rowe, H.E., *Signals and Noise in Communication Systems*, D. Van Nostrand Company, Inc., Princeton, New Jersey, including, for example, Chapter V, Pulse Modulation Systems (1965).
	AO35	Rücker, F. and Dintelmann, F., "Effect of Antenna Size on OTS Signal Scintillations and Their Seasonal Dependence," *Electronics Letters*, IEE, Vol. 19, No. 24, pp. 1032-1034 (November 24, 1983).
	AP35	Russell, R. and Hoare, L., "Millimeter Wave Phase Locked Oscillators," *Military Microwaves '78 Conference Proceedings*, Microwave Exhibitions and Publishers, pp. 238-242 (October 25-27, 1978).
	AQ35	Sabel, L.P., "A DSP Implementation of a Robust Flexible Receiver/Demultiplexer for Broadcast Data Satellite Communications," *The Institution of Engineers Australia Communications Conference*, Institution of Engineers, Australia, pp. 218-223 (October 16-18, 1990).
	AR35	Salous, S., "IF digital generation of FMCW waveforms for wideband channel characterization," *IEE Proceedings-I*, IEE, Vol. 139, No. 3, pp. 281-288 (June 1992).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA36	5,793,801	08/1998	Fertner			
	AB36	5,793,818	08/1998	Claydon *et al.*			
	AC36	5,802,463	09/1998	Zuckerman			
	AD36	5,809,060	09/1998	Cafarella *et al.*			
	AE36	5,818,582	10/1998	Fernandez *et al.*			
	AF36	5,825,254	10/1998	Lee			
	AG36	5,834,985	11/1998	Sundegård			
	AH36	5,864,754	01/1999	Hotto			
	AI36	5,881,375	03/1999	Bonds			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ36						Yes No
	AK36						Yes No
	AL36						Yes No
	AM36						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN36	"Sampling Loops Lock Sources to 23 Ghz," *Microwaves & RF*, Penton Publishing, p. 212 (September 1990).
	AO36	Sasikumar, M. *et al.*, "Active Compensation in the Switched-Capacitor Biquad," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 1008-1009 (August 1983).
	AP36	Saul, P.H., "A GaAs MESFET Sample and Hold Switch," *Fifth European Solid State Circuits Conference-ESSCIRC 79*, IEE, pp. 5-7 (1979).
	AQ36	Shen, D.H. *et al.*, "A 900-MHZ RF Front-End with Integrated Discrete-Time Filtering," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Council, Vol. 31, No. 12, pp. 1945-1954 (December 1996).
	AR36	Shen, X.D. and Vilar, E., "Anomalous transhorizon propagation and meteorological processes of a multilink path," *Radio Science*, American Geophysical Union, Vol. 30, No. 5, pp. 1467-1479 (September-October 1995).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA37	5,892,380	04/1999	Quist			
	AB37	5,894,239	04/1999	Bonaccio *et al.*			
	AC37	5,896,562	04/1999	Heinonen			
	AD37	5,900,747	05/1999	Brauns			
	AE37	5,901,054	05/1999	Leu *et al.*			
	AF37	5,901,187	05/1999	Iinuma			
	AG37	5,901,344	05/1999	Opas			
	AH37	5,901,347	05/1999	Chambers *et al.*			
	AI37	5,901,348	05/1999	Bang *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ37						Yes No
	AK37						Yes No
	AL37						Yes No
	AM37						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN37	Shen, X. and Tawfik, A.N., "Dynamic Behaviour of Radio Channels Due to Trans-Horizon Propagation Mechanisms," *Electronics Letters*, IEE, Vol. 29, No. 17, pp. 1582-1583 (August 19, 1993).
	AO37	Shen, X. *et al.*, "Modeling Enhanced Spherical Diffraction and Troposcattering on a Transhorizon Path with aid of the parabolic Equation and Ray Tracing Methods," *IEE Colloquium on Common modeling techniques for electromagnetic wave and acoustic wave propagation*, IEE, pp. 4/1-4/7 (March 8, 1996).
	AP37	Shen, X. and Vilar, E., "Path loss statistics and mechanisms of transhorizon propagation over a sea path," *Electronics Letters*, IEE, Vol. 32, No. 3, pp. 259-261 (February 1, 1996).
	AQ37	Shen, D. *et al.*, "A 900 MHZ Integrated Discrete-Time Filtering RF Front-End," *IEEE International Solid State Circuits Conference*, IEEE, Vol. 39, pp. 54-55 and 417 (February 1996).
	AR37	Spillard, C. *et al.*, "X-Band Tropospheric Transhorizon Propagation Under Differing Meteorological Conditions," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 451-455 (April 4-7, 1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA38	5,901,349	05/1999	Guegnaud *et al.*			
	AB38	5,903,178	05/1999	Miyatsuji *et al.*			
	AC38	5,903,187	05/1999	Claverie *et al.*			
	AD38	5,903,196	05/1999	Salvi *et al.*			
	AE38	5,903,421	05/1999	Furutani *et al.*			
	AF38	5,903,553	05/1999	Sakamoto *et al.*			
	AG38	5,903,595	05/1999	Suzuki			
	AH38	5,903,609	05/1999	Kool *et al.*			
	AI38	5,903,827	05/1999	Kennan *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ38						Yes No
	AK38						Yes No
	AL38						Yes No
	AM38						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN38	Stafford, K.R. *et al.*, "A Complete Monolithic Sample/Hold Amplifier," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-9, No. 6, pp. 381-387 (December 1974).
	AO38	Staruk, W. Jr. *et al.*, "Pushing HF Data Rates," *Defense Electronics*, EW Communications, Vol. 17, No. 5, pp. 211, 213, 215, 217, 220 and 222 (May 1985).
	AP38	Stephenson, A.G., "Digitizing multiple RF signals requires an optimum sampling rate," *Electronics*, McGraw-Hill, pp. 106-110 (March 27, 1972).
	AQ38	Sugarman, R., "Sampling Oscilloscope for Statistically Varying Pulses," *The Review of Scientific Instruments*, American Institute of Physics, Vol. 28, No. 11, pp. 933-938 (November 1957).
	AR38	Sylvain, M., "Experimental probing of multipath microwave channels," *Radio Science*, American Geophysical Union, Vol. 24, No. 2, pp. 160-178 (March-April 1989).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA39	5,903,854	05/1999	Abe *et al.*			
	AB39	5,905,449	05/1999	Tsubouchi *et al.*			
	AC39	5,907,149	05/1999	Marckini			
	AD39	5,907,197	05/1999	Faulk			
	AE39	5,911,116	06/1999	Nosswitz			
	AF39	5,911,123	06/1999	Shaffer *et al.*			
	AG39	5,914,622	06/1999	Inoue			
	AH39	5,920,199	07/1999	Sauer			
	AI39	5,943,370	08/1999	Smith			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ39						Yes No
	AK39						Yes No
	AL39						Yes No
	AM39						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN39	Takano, T., "NOVEL GaAs Pet Phase Detector Operable To Ka Band," *IEEE MT-S Digest*, IEEE, pp. 381-383 (1984).
	AO39	Tan, M.A., "Biquadratic Transconductance Switched-Capacitor Filters," *IEEE Transactions on Circuits and Systems- I: Fundamental Theory and Applications*, IEEE Circuits and Systems Society, Vol. 40, No. 4, pp. 272-275 (April 1993).
	AP39	Tanaka, K. *et al.*, "Single Chip Multisystem AM Stereo Decoder IC," *IEEE Transactions on Consumer Electronics*, IEEE Consumer Electronics Society, Vol. CE-32, No. 3, pp. 482-496 (August 1986).
	AQ39	Tawfik, A.N., "Amplitude, Duration and Predictability of Long Hop Trans-Horizon X-band Signals Over the Sea," *Electronics Letters*, IEE, Vol. 28, No. 6, pp. 571-572 (March 12, 1992).
	AR39	Tawfik, A.N. and Vilar, E., "Correlation of Transhorizon Signal Level Strength with Localized Surface Meteorological Parameters," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 335-339 (March 30- April 2, 1993).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA40	4,017,798	04/1977	Gordy *et al.*			
	AB40	4,032,847	06/1977	Unkauf			
	AC40	4,253,067	02/1981	Caples *et al.*			
	AD40	4,393,395	07/1983	Hacke *et al.*			
	AE40	4,816,704	03/1989	Fiori, Jr.			
	AF40	4,841,265	06/1989	Watanabe *et al.*			
	AG40	4,943,974	07/1990	Motamedi			
	AH40	5,115,409	05/1992	Stepp			
	AI40	5,353,306	10/1994	Yamamoto			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ40						Yes No
	AK40						Yes No
	AL40						Yes No
	AM40						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN40	Tawfik, A.N. and Vilar, E., "Dynamic Structure of a Transhorizon Signal at X-band Over a Sea Path," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 446-450 (April 4-7, 1989).
	AO40	Tawfik, A.N. and Vilar, E., "Statistics of Duration and Intensity of Path Loss in a Microwave Transhorizon Sea-Path," *Electronics Letters*, IEE, Vol. 26, No. 7, pp. 474-476 (March 29, 1990).
	AP40	Tawfik, A.N. and Vilar, E., "X-Band Transhorizon Measurements of CW Transmissions Over the Sea- Part 1: Path Loss, Duration of Events, and Their Modeling," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 41, No. 11, pp. 1491-1500 (November 1993).
	AQ40	Temes, G.C. and Tsividis, T., "The Special Section on Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 915-916 (August 1983).
	AR40	Thomas, G.B., *Calculus and Analytic Geometry*, Third Edition, Addison-Wesley Publishing, pp. 119-133 (1960).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA41	5,515,014	05/1996	Troutman			
	AB41	5,563,550	10/1996	Toth			
	AC41	5,574,755	11/1996	Persico			
	AD41	5,604,592	02/1997	Kotidis *et al.*			
	AE41	5,638,396	06/1997	Klimek			
	AF41	5,675,392	10/1997	Nayebi *et al.*			
	AG41	5,694,096	12/1997	Ushiroku *et al.*			
	AH41	5,757,870	05/1998	Miya *et al.*			
	AI41	5,768,323	06/1998	Kroeger *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ41						Yes No
	AK41						Yes No
	AL41						Yes No
	AM41						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN41	Tomassetti, Q., "An Unusual Microwave Mixer," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 754-759 (September 8-12, 1986).
	AO41	Tortoli, P. *et al.*, "Bidirectional Doppler Signal Analysis Based on a Single RF Sampling Channel," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, Vol. 41, No. 1, pp. 1-3 (January 1984).
	AP41	Tsividis, Y. and Antognetti, P. (Ed.), *Design of MOS VLSI Circuits for Telecommunications*, Prentice-Hall, p. 304 (1985).
	AQ41	Tsividis, Y., "Principles of Operation and Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 926-940 (August 1983).
	AR41	Tsurumi, H. and Maeda, T., "Design Study on a Direct Conversion Receiver Front-End for 280 MHZ, 900 MHZ, and 2.6 Ghz Band Radio Communication Systems," *41st IEEE Vehicular Technology Conference*, IEEE Vehicular Technology Society, pp. 457-462 (May 19-22, 1991).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA42	5,770,985	06/1998	Ushiroku *et al.*			
	AB42	5,778,022	07/1998	Walley			
	AC42	5,812,546	09/1998	Zhou *et al.*			
	AD42	5,818,869	10/1998	Miya *et al.*			
	AE42	5,844,449	12/1998	Abeno *et al.*			
	AF42	5,872,446	02/1999	Cranford, Jr. *et al.*			
	AG42	5,909,447	06/1999	Cox *et al.*			
	AH42	5,933,467	08/1999	Sehier *et al.*			
	AI42	5,952,895	09/1999	McCune, Jr. *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ42						Yes No
	AK42						Yes No
	AL42						Yes No
	AM42						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN42	Valdmanis, J.A. *et al.*, "Picosecond and Subpicosend Optoelectronics for Measurements of Future High Speed Electronic Devices," *IEDM Technical Digest*, IEEE, pp. 597-600 (December 5-7, 1983).
	AO42	van de Kamp, M.M.J.L., "Asymmetric signal level distribution due to tropospheric scintillation," *Electronics Letters*, IEE, Vol. 34, No. 11, pp. 1145-1146 (May 28, 1998).
	AP42	Vasseur, H. and Vanhoenacker, D., "Characterization of tropospheric turbulent layers from radiosonde data," *Electronics Letters*, IEE, Vol. 34, No. 4, pp. 318-319 (February 19, 1998).
	AQ42	Verdone, R., "Outage Probability Analysis for Short-Range Communication Systems at 60 Ghz in ATT Urban Environments," *IEEE Transactions on Vehicular Technology*, IEEE Vehicular Technology Society, Vol. 46, No. 4, pp. 1027-1039 (November 1997).
	AR42	Vierira-Ribeiro, S.A., *Single-IF DECT Receiver Architecture using a Quadrature Sub-Sampling Band-Pass Sigma-Delta Modulator*, Thesis for Degree of Master's of Engineering, Carleton University, UMI Dissertation Services, pp. 1-180 (April 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA43	5,960,033	09/1999	Shibano *et al.*			
	AB43	6,041,073	03/2000	Davidovici *et al.*			
	AC43	6,054,889	04/2000	Kobayashi			
	AD43	6,084,922	07/2000	Zhou *et al.*			
	AE43	6,125,271	09/2000	Rowland *et al.*			
	AF43	6,147,340	11/2000	Levy			
	AG43	6,147,763	11/2000	Steinlechner			
	AH43	6,150,890	11/2000	Damgaard *et al.*			
	AI43	5,126,682	06/1992	Weinberg *et al.*			

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	AJ43						Yes No
	AK43						Yes No
	AL43						Yes No
	AM43						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN43	Vilar, E. *et al.*, "A Comprehensive/Selective MM-Wave Satellite Downlink Experiment on Fade Dynamics," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.98-2.101 (April 14-17, 1997).
	AO43	Vilar, E. *et al.*, "A System to Measure LOS Atmospheric Transmittance at 19 Ghz," *AGARD Conference Proceedings No. 346: Characteristics of the Lower Atmosphere Influencing Radio Wave Propagation*, AGARD, pp. 8-1 - 8-16 (October 4-7, 1983).
	AP43	Vilar, E. and Smith, H., "A Theoretical and Experimental Study of Angular Scintillations in Earth Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 1, pp. 2-10 (January 1986).
	AQ43	Vilar, E. *et al.*, "A Wide Band Transhorizon Experiment at 11.6 Ghz," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 441-445 (March 30- April 2, 1993).
	AR43	Vilar, E. and Matthews, P.A., "Amplitude Dependence of Frequency in Oscillators," *Electronics Letters*, IEE, Vol. 8, No. 20, pp. 509-511 (October 5, 1972).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA44	5,841,811	11/1998	Song			
	AB44	4,051,475	09/1977	Campbell			
	AC44	5,953,642	09/1999	Feldtkeller *et al.*			
	AD44	4,653,117	03/1987	Heck			
	AE44	5,859,878	01/1999	Phillips *et al.*			
	AF44	5,894,496	04/1999	Jones			
	AG44	5,915,278	06/1999	Mallick			
	AH44	6,028,887	02/2000	Harrison *et al.*			
	AI44	6,081,691	06/2000	Renard *et al.*			

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	AJ44						Yes No
	AK44						Yes No
	AL44						Yes No
	AM44						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN44	Vilar, E. *et al.*, "An experimental mm-wave receiver system for measuring phase noise due to atmospheric turbulence," *Proceedings of the 25th European Microwave Conference*, Nexus House, pp. 114-119 (1995).
	AO44	Vilar, E. and Burgueño, A., "Analysis and Modeling of Time Intervals Between Rain Rate Exceedances in the Context of Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 39, No. 9, pp. 1306-1312 (September 1991).
	AP44	Vilar, E. *et al.*, "Angle of Arrival Fluctuations in High and Low Elevation Earth Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, Electronics Division of the IEE, pp. 83-88 (April 16-19, 1985).
	AQ44	Vilar, E., "Antennas and Propagation: A Telecommunications Systems Subject," *Electronics Division Colloquium on Teaching Antennas and Propagation to Undergraduates*, IEE, pp. 7/1-7/6 (March 8, 1988).
	AR44	Vilar, E. *et al.*, "CERS*. Millimetre-Wave Beacon Package and Related Payload Doppler Correction Strategies," *Electronics Division Colloquium on CERS- Communications Engineering Research Satellite*, IEE, pp. 10/1-10/10 (April 10, 1984).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA45	6,121,819	09/2000	Traylor			
	AB45	6,144,236	11/2000	Vice *et al.*			
	AC45	6,144,846	11/2000	Durec			
	AD45	6,175,728 B1	01/2001	Mitama			
	AE45	5,705,949	01/1998	Alelyunas *et al.*			
	AF45	5,883,548	03/1999	Assard *et al.*			
	AG45	4,484,143	11/1984	French *et al.*			
	AH45	5,841,324	11/1998	Williams			
	AI45	4,855,894	08/1989	Asahi *et al.*			

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	AJ45						Yes No
	AK45						Yes No
	AL45						Yes No
	AM45						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN45	Vilar, E. and Moulsley, T.J., "Comment and Reply: Probability Density Function of Amplitude Scintillations," *Electronics Letters*, IEE, Vol. 21, No. 14, pp. 620-622 (July 4, 1985).
	AO45	Vilar, E. *et al.*, "Comparison of Rainfall Rate Duration Distributions for ILE-IFE and Barcelona," *Electronics Letters*, IEE, Vol. 28, No. 20, pp. 1922-1924 (September 24, 1992).
	AP45	Vilar, E., "Depolarization and Field Transmittances in Indoor Communications," *Electronics Letters*, IEE, Vol. 27, No. 9, pp. 732-733 (April 25, 1991).
	AQ45	Vilar, E. and Larsen, J.R., "Elevation Dependence of Amplitude Scintillations on Low Elevation Earth Space Paths," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 150-154 (April 4-7, 1989).
	AR45	Vilar, E. *et al.*, "Experimental System and Measurements of Transhorizon Signal Levels at 11 Ghz," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 429-435 (September 12 - 15, 1988).

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	AA46	5,319,799	06/1994	Morita			
	AB46	5,801,654	09/1998	Traylor			
	AC46	5,369,404	11/1994	Galton			
	AD46	3,716,730	02/1973	Cerny, Jr.			
	AE46	4,080,573	03/1978	Howell			
	AF46	4,334,324	06/1982	Hoover			
	AG46	4,369,522	01/1983	Cerny, Jr. *et al.*			
	AH46	5,465,418	11/1995	Zhou *et al.*			
	AI46	5,513,389	04/1996	Reeser *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ46						Yes No
	AK46						Yes No
	AL46						Yes No
	AM46						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN46	Vilar, E. and Matthews, P.A., "Importance of Amplitude Scintillations in Millimetric Radio Links," *Proceedings of the 4th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 202-206 (September 10-13, 1974).
	AO46	Vilar, E. and Haddon, J., "Measurement and Modeling of Scintillation Intensity to Estimate Turbulence Parameters in an Earth-Space Path," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. AP-32, No. 4, pp. 340-346 (April 1984).
	AP46	Vilar, E. and Matthews, P.A., "Measurement of Phase Fluctuations on Millimetric Radiowave Propagation," *Electronics Letters*, IEE, Vol. 7, No. 18, pp. 566-568 (September 9, 1971).
	AQ46	Vilar, E. and Wan, K.W., "Narrow and Wide Band Estimates of Field Strength for Indoor Communications in the Millimetre Band," *Electronics Division Colloquium on Radiocommunications in the Range 30-60 Ghz*, IEE, pp. 5/1-5/8 (January 17, 1991).
	AR46	Vilar, E. and Faulkner, N.D., "Phase Noise and Frequency Stability Measurements. Numerical Techniques and Limitations," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizer,* IEE, 5 pages (January 23, 1986).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA47	5,959,850	09/1999	Lim			
	AB47	5,157,687	10/1992	Tymes			
	AC47	5,945,660	08/1999	Nakasuji *et al.*			
	AD47	6,091,939	07/2000	Banh			
	AE47	6,091,941	07/2000	Moriyama *et al.*			
	AF47	6,098,886	08/2000	Swift *et al.*			
	AG47	6,215,475 B1	04/2001	Meyerson *et al.*			
	AH47	6,049,706	04/2000	Cook *et al.*			
	AI47	6,061,551	05/2000	Sorrells *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ47						Yes No
	AK47						Yes No
	AL47						Yes No
	AM47						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN47	Vilar, E. and Senin, S., "Propagation phase noise identified using 40 Ghz satellite downlink," *Electronics Letters,* IEE, Vol. 33, No. 22, pp. 1901-1902 (October 23, 1997).
	AO47	Vilar, E. *et al.*, "Scattering and Extinction: Dependence Upon Raindrop Size Distribution in Temperate (Barcelona) and Tropical (Belem) Regions," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.230-2.233 (April 14-17, 1997).
	AP47	Vilar, E. and Haddon, J., "Scintillation Modeling and Measurement - A Tool for Remote-Sensing Slant Paths," *AGARD Conference Proceedings No. 332: Propagation Aspects of Frequency Sharing, Interference And System Diversity*, AGARD, pp. 27-1 - 27-13 (October 18-22, 1982).
	AQ47	Vilar, E., "Some Limitations on Digital Transmission Through Turbulent Atmosphere," *International Conference on Satellite Communication Systems Technology,* Electronics Division of the IEE, pp. 169-187 (April 7-10, 1975).
	AR47	Vilar, E. and Matthews, P.A., "Summary of Scintillation Observations in a 36 Ghz Link Across London," *International Conference on Antennas and Propagation Part 2: Propagation,* IEE, pp. 36-40 (November 28-30, 1978).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA48	6,061,555	05/2000	Bultman *et al.*			
	AB48	6,091,940	07/2000	Sorrells *et al.*			
	AC48	6,266,518 B1	07/2001	Sorrells *et al.*			
	AD48	6,353,735 B1	03/2002	Sorrells *et al.*			
	AE48	6,370,371 B1	04/2002	Sorrells *et al.*			
	AF48	5,628,055	05/1997	Stein			
	AG48	5,678,220	10/1997	Fournier			
	AH48	5,926,065	07/1999	Wakai *et al.*			
	AI48	3,622,885	11/1971	Oberdorf *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ48						Yes No
	AK48						Yes No
	AL48						Yes No
	AM48						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN48	Vilar, E. *et al.*, "Wideband Characterization of Scattering Channels," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.353-2.358 (April 14-17, 1997).
	AO48	Vollmer, A., "Complete GPS Receiver Fits on Two Chips," *Electronic Design*, Penton Publishing, pp. 50, 52, 54 and 56 (July 6, 1998).
	AP48	*Voltage and Time Resolution in Digitizing Oscilloscopes: Application Note 348*, Hewlett Packard, pp. 1-11 (November 1986).
	AQ48	Wan, K.W. *et al.*, "A Novel Approach to the Simultaneous Measurement of Phase and Amplitude Noises in Oscillator," *Proceedings of the 19th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 809-813 (September 4-7, 1989).
	AR48	Wan, K.W. *et al.*, "Extended Variances and Autoregressive/Moving Average Algorithm for the Measurement and Synthesis of Oscillator Phase Noise," *Proceedings Of the 43rd Annual Symposium on Frequency Control*, IEEE, pp. 331-335 (1989).

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	AA49	4,483,017	11/1984	Hampel *et al.*			
	AB49	6,421,534 B1	07/2002	Cook *et al.*			
	AC49	6,330,244 B1	12/2001	Swartz *et al.*			
	AD49	4,384,357	05/1983	deBuda *et al.*			
	AE49	4,470,145	09/1984	Williams			
	AF49	5,600,680	02/1997	Mishima *et al.*			
	AG49	5,606,731	02/1997	Pace *et al.*			
	AH49	5,870,670	02/1999	Ripley *et al.*			
	AI49	6,314,279 B1	11/2001	Mohindra			

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	AJ49						Yes No
	AK49						Yes No
	AL49						Yes No
	AM49						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN49	Wan, K.W. *et al.*, "Wideband Transhorizon Channel Sounder at 11 Ghz," *Electronics Division Colloquium on High Bit Rate UHF/SHF Channel Sounders - Technology and Measurement*, IEE, pp. 3/1-3/5 (December 3, 1993).
	AO49	Wang, H., "A 1-V Multigigahertz RF Mixer Core in 0.5 - μm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Society, Vol. 33, No. 12, pp. 2265-2267 (December 1998).
	AP49	Watson, A.W.D. *et al.*, "Digital Conversion and Signal Processing for High Performance Communications Receivers," *Digital Processing of Signals in Communications*, Institution of Electronic and Radio Engineers, pp. 367-373 (April 22nd -26th, 1985).
	AQ49	Weast, R.C. *et al.* (Ed.), *Handbook of Mathematical Tables*, Second Edition, The Chemical Rubber Co., pp. 480-485 (1964).
	AR49	Wiley, R.G., "Approximate FM Demodulation Using Zero Crossings," *IEEE Transactions on Communications*, IEEE, Vol. COM-29, No. 7, pp. 1061-1065 (July 1981).

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	AA50	5,633,815	05/1997	Young			
	AB50	3,246,084	04/1966	Kryter			
	AC50	3,702,440	11/1972	Moore			
	AD50	3,767,984	10/1973	Shinoda *et al.*			
	AE50	3,852,530	12/1974	Shen			
	AF50	4,220,977	09/1980	Yamanaka			
	AG50	5,016,242	05/1991	Tang			
	AH50	5,937,013	08/1999	Lam *et al.*			
	AI50	6,014,551	01/2000	Pesola *et al.*			

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	AJ50						Yes No
	AK50						Yes No
	AL50						Yes No
	AM50						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN50	Worthman, W., "Convergence... Again," *RF Design*, Primedia, p. 102 (March 1999).
	AO50	Young, I.A. and Hodges, D.A., "MOS Switched-Capacitor Analog Sampled-Data Direct-Form Recursive Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-14, No. 6, pp. 1020-1033 (December 1979).
	AP50	Translation of Specification and Claims of FR Patent No. 2245130, 3 pages (April 18, 1975- Date of publication of application).
	AQ50	Fest, Jean-Pierre, "Le Convertisseur A/N Revolutionne Le Recepteur Radio," *Electronique*, JMJ (Publisher), No. 54, pp. 40-42 (December 1995).
	AR50	Translation of DE Patent No. 35 41 031 A1, 22 pages (May 22, 1986- Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA51	6,073,001	06/2000	Sokoler			
	AB51	6,085,073	07/2000	Palermo *et al.*			
	AC51	6,400,963 B1	06/2002	Glöckler *et al.*			
	AD51	6,230,000 B1	05/2001	Tayloe			
	AE51	5,483,695	01/1996	Pardoen			
	AF51	6,542,722 B1	04/2003	Sorrells *et al.*			
	AG51	6,560,301 B1	05/2003	Cook *et al.*			
	AH51	6,098,046	08/2000	Cooper *et al.*			
	AI51	5,564,097	10/1996	Swanke			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ51						Yes No
	AK51						Yes No
	AL51						Yes No
	AM51						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN51	Translation of EP Patent No. 0 732 803 A1, 9 pages (September 18, 1996- Date of publication of application).
	AO51	Fest, Jean-Pierre, "The A/D Converter Revolutionizes the Radio Receiver," *Electronique*, JMJ (Publisher), No. 54, 3 pages (December 1995). (Translation of Doc. AQ50).
	AP51	Translation of German Patent No. DE 197 35 798 C1, 8 pages (July 16, 1998- Date of publication of application).
	AQ51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-154 (April 30, 1956).
	AR51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-149 (April 30, 1956). (Partial Translation of Doc. AQ51).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA52	5,898,912	04/1999	Heck *et al.*			
	AB52	4,660,164	04/1987	Leibowitz			
	AC52	6,580,902 B1	06/2003	Sorrells *et al.*			
	AD52	4,857,928	08/1989	Gailus *et al.*			
	AE52	5,389,839	02/1995	Heck			
	AF52	5,471,665	11/1995	Pace *et al.*			
	AG52	6,327,313 B1	12/2001	Traylor *et al.*			
	AH52	5,751,154	05/1998	Tsugai			
	AI52	5,793,817	08/1998	Wilson			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ52						Yes No
	AK52						Yes No
	AL52						Yes No
	AM52						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN52	Rabiner, L.R. and Gold, B., *Theory And Application Of Digital Signal Processing*, Prentice-Hall, Inc., pp. v-xii and 40-46 (1975).
	AO52	English-language Abstract of Japanese Patent Publication No. 08-032556, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 2, 1996 - Date of publication of application).
	AP52	English-language Abstract of Japanese Patent Publication No. 08-139524, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (May 31, 1996 - Date of publication of application).
	AQ52	English-language Abstract of Japanese Patent Publication No. 59-144249, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 18, 1984 - Date of publication of application).
	AR52	English-language Abstract of Japanese Patent Publication No. 63-054002, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (March 8, 1988 - Date of publication of application).

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	FIRST NAMED INVENTOR David F. Sorrells	
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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA53	6,225,848 B1	05/2001	Tilley *et al.*			
	AB53	6,313,685 B1	11/2001	Rabii			
	AC53	3,614,627	10/1971	Runyan *et al.*			
	AD53	3,940,697	02/1976	Morgan			
	AE53	4,016,366	04/1977	Kurata			
	AF53	4,045,740	08/1977	Baker			
	AG53	4,115,737	09/1978	Hongu *et al.*			
	AH53	5,710,992	01/1998	Sawada *et al.*			
	AI53	5,790,587	08/1998	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ53						Yes No
	AK53						Yes No
	AL53						Yes No
	AM53						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN53	English-language Abstract of Japanese Patent Publication No. 06-237276, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 23, 1994 - Date of publication of application).
	AO53	English-language Abstract of Japanese Patent Publication No. 08-023359, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (January 23, 1996 - Date of publication of application).
	AP53	Translation of Japanese Patent Publication No. 47-2314, 7 pages (February 4, 1972- Date of publication of application).
	AQ53	Partial Translation of Japanese Patent Publication No. 58-7903, 3 pages (January 17, 1983- Date of publication of application).
	AR53	English-language Abstract of Japanese Patent Publication No. 58-133004, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 8, 1993 - Date of publication of application).

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	FIRST NAMED INVENTOR David F. Sorrells	
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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA54	4,740,675	04/1988	Brosnan *et al.*			
	AB54	5,483,600	01/1996	Werrbach			
	AC54	6,011,435	01/2000	Takeyabu *et al.*			
	AD54	6,321,073 B1	11/2001	Luz *et al.*			
	AE54	6,026,286	02/2000	Long			
	AF54	6,178,319 B1	01/2001	Kashima			
	AG54	6,634,555 B1	10/2003	Sorrells *et al.*			
	AH54	3,736,513	05/1973	Wilson			
	AI54	4,488,119	12/1984	Marshall			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ54						Yes No
	AK54						Yes No
	AL54						Yes No
	AM54						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN54	English-language Abstract of Japanese Patent Publication No. 60-058705, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 4, 1985 - Date of publication of application).
	AO54	English-language Abstract of Japanese Patent Publication No. 04-123614, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 23, 1992 - Date of publication of application).
	AP54	English-language Abstract of Japanese Patent Publication No. 04-127601, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 28, 1992 - Date of publication of application).
	AQ54	English-language Abstract of Japanese Patent Publication No. 05-175730, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (July 13, 1993 - Date of publication of application).
	AR54	English-language Abstract of Japanese Patent Publication No. 05-175734, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (July 13, 1993 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA55	4,633,510	12/1986	Suzuki *et al.*			
	AB55	5,369,789	11/1994	Kosugi *et al.*			
	AC55	5,416,449	05/1995	Joshi			
	AD55	5,438,329	08/1995	Gastouniotis *et al.*			
	AE55	6,611,569 B1	08/2003	Schier *et al.*			
	AF55	6,647,250 B1	11/2003	Bultman *et al.*			
	AG55	5,682,099	10/1997	Thompson *et al.*			
	AH55	6,094,084	07/2000	Abou-Allam *et al.*			
	AI55	6,067,329	05/2000	Kato *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ55						Yes No
	AK55						Yes No
	AL55						Yes No
	AM55						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN55	English-language Abstract of Japanese Patent Publication No. 07-154344, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (June 16, 1995 - Date of publication of application).
	AO55	English-language Abstract of Japanese Patent Publication No. 07-307620, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (November 21, 1995 - Date of publication of application).
	AP55	Oppenheim, A.V. and Schafer, R.W., *Digital Signal Processing*, Prentice-Hall, pp. vii-x, 6-35, 45-78, 87-121 and 136-165 (1975).
	AQ55	English-language Abstract of Japanese Patent Publication No. 55-066057, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (May 19, 1980 - Date of publication of application).
	AR55	English-language Abstract of Japanese Patent Publication No. 63-065587, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (March 24, 1988 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA56	6,516,185 B1	02/2003	MacNally			
	AB56	6,608,647 B1	08/2003	King			
	AC56	6,687,493 B1	02/2004	Sorrells *et al.*			
	AD56	6,694,128 B1	02/2004	Sorrells *et al.*			
	AE56	6,031,217	02/2000	Aswell *et al.*			
	AF56	5,955,992	09/1999	Shattil			
	AG56	5,999,561	12/1999	Naden *et al.*			
	AH56	6,686,879 B2	02/2004	Shattil			
	AI56	6,704,549 B1	03/2004	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ56						Yes No
	AK56						Yes No
	AL56						Yes No
	AM56						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN56	English-language Abstract of Japanese Patent Publication No. 63-153691, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (June 27, 1988 - Date of publication of application).
	AO56	Translation of Japanese Patent Publication No. 60-130203, 3 pages (July 11, 1985- Date of publication of application).
	AP56	Razavi, B., "A 900-MHz/1.8-Ghz CMOS Transmitter for Dual-Band Applications," *Symposium on VLSI Circuits Digest of Technical Papers*, IEEE, pp. 128-131 (1998).
	AQ56	Ritter, G.M., "SDA, A New Solution for Transceivers," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 729-733 (September 8, 1986).
	AR56	DIALOG File 351 (Derwent WPI) English Language Patent Abstract for FR 2 669 787, 1 page (May 29, 1992- Date of publication of application).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA57	6,704,558 B1	03/2004	Sorrells *et al.*			
	AB57	5,490,176	02/1996	Peltier			
	AC57	5,970,053	10/1999	Schick *et al.*			
	AD57	6,078,630	06/2000	Prasanna			
	AE57	6,600,911 B1	07/2003	Morishige *et al.*			
	AF57	5,179,731	01/1993	Tränkle *et al.*			
	AG57	5,589,793	12/1996	Kassapian			
	AH57	4,510,467	04/1985	Chang *et al.*			
	AI57	4,772,853	09/1988	Hart			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ57						Yes No
	AK57						Yes No
	AL57						Yes No
	AM57						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN57	Akos, D.M. *et al.*, "Direct Bandpass Sampling of Multiple Distinct RF Signals," *IEEE Transactions on Communications*, IEEE, Vol. 47, No. 7, pp. 983-988 (July 1999).
	AO57	Patel, M. *et al.*, "Bandpass Sampling for Software Radio Receivers, and the Effect of Oversampling on Aperture Jitter," *VTC 2002*, IEEE, pp. 1901-1905 (2002).
	AP57	English-language Abstract of Japanese Patent Publication No. 61-030821, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 13, 1986- Date of publication of application).
	AQ57	English-language Abstract of Japanese Patent Publication No. 05-327356, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (December 10, 1993 - Date of publication of application).
	AR57	Tayloe, D., "A Low-noise, High-performance Zero IF Quadrature Detector/Preamplifier," *RF Design*, Primedia Business Magazines & Media, Inc., pp. 58, 60, 62 and 69 (March 2003).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA58	4,972,436	11/1990	Halim *et al.*			
	AB58	5,012,245	04/1991	Scott *et al.*			
	AC58	5,422,909	06/1995	Love *et al.*			
	AD58	5,440,311	08/1995	Gallagher *et al.*			
	AE58	5,926,513	07/1999	Suominen *et al.*			
	AF58	5,995,030	11/1999	Cabler			
	AG58	6,047,026	04/2000	Chao *et al.*			
	AH58	6,049,573	04/2000	Song			
	AI58	6,076,015	06/2000	Hartley *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ58						Yes No
	AK58						Yes No
	AL58						Yes No
	AM58						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN58	Dines, J.A.B., "Smart Pixel Optoelectronic Receiver Based on a Charge Sensitive Amplifier Design," *IEEE Journal of Selected Topics in Quantum Electronics*, IEEE, Vol. 2, No. 1, pp. 117-120 (April 1996).
	AO58	Simoni, A. *et al.*, "A Digital Camera for Machine Vision," *20th International Conference on Industrial Electronics, Control and Instrumentation*, IEEE, pp. 879-883 (September 1994).
	AP58	Stewart, R.W. and Pfann, E., "Oversampling and sigma-delta strategies for data conversion," *Electronics & Communication Engineering Journal*, IEEE, pp. 37-47 (February 1998).
	AQ58	Rudell, J.C. *et al.*, "A 1.9-Ghz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, pp. 2071-2088 (December 1997).
	AR58	English-language Abstract of Japanese Patent Publication No. 09-036664, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 7, 1997 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA59	6,144,331	11/2000	Jiang			
	AB59	6,018,553	01/2000	Sanielevici *et al.*			
	AC59	6,317,589 B1	11/2001	Nash			
	AD59	5,058,107	10/1991	Stone *et al.*			
	AE59	5,757,858	05/1998	Black *et al.*			
	AF59	6,531,979 B1	03/2003	Hynes			
	AG59	6,018,262	01/2000	Noro *et al.*			
	AH59	4,761,798	08/1988	Griswold, Jr. *et al.*			
	AI59	5,982,315	11/1999	Bazarjani *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ59						Yes No
	AK59						Yes No
	AL59						Yes No
	AM59						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN59	Simoni, A. *et al.*, "A Single-Chip Optical Sensor with Analog Memory for Motion Detection," *IEEE Journal of Solid-State Circtuits*, IEEE, Vol. 30, No. 7, pp. 800-806 (July 1995).
	AO59	English Translation of German Patent Publication No. DE 196 48 915 A1, 10 pages.
	AP59	Deboo, Gordon J., *Integrated Circuits and Semiconductor Devices*, 2nd Edition, McGraw-Hill, Inc., pp. 41-45 (1977).
	AQ59	Hellwarth, G.A. and Jones, G.D, "Automatic Conditioning of Speech Signals," *IEEE Transactions on Audio and Electroacoustics*, Vol. AU-16, No. 2, pp. 169-179 (June 1968).
	AR59	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA60	6,459,721 B1	10/2002	Mochizuki *et al.*			
	AB60	6,151,354	11/2000	Abbey			
	AC60	6,169,733 B1	01/2001	Lee			
	AD60	6,363,262 B1	03/2002	McNicol			
	AE60	6,697,603 B1	02/2004	Lovinggood *et al.*			
	AF60	5,282,222	01/1994	Fattouche *et al.*			
	AG60	5,949,827	09/1999	DeLuca *et al.*			
	AH60	6,014,176	01/2000	Nayebi *et al.*			
	AI60	5,678,226	10/1997	Li *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ60						Yes No
	AK60						Yes No
	AL60						Yes No
	AM60						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN60	
	AO60	
	AP60	
	AQ60	
	AR60	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA61	5,760,632	06/1998	Kawakami *et al.*			
	AB61	6,160,280	12/2000	Bonn *et al.*			
	AC61	5,481,570	01/1996	Winters			
	AD61	5,745,846	04/1998	Myer *et al.*			
	AE61	5,345,239	09/1994	Madni *et al.*			
	AF61	4,132,952	01/1979	Hongu *et al.*			
	AG61	5,260,973	11/1993	Watanabe			
	AH61	6,307,894 B2	10/2001	Eidson *et al.*			
	AI61	6,091,289	07/2000	Song *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ61						Yes No
	AK61						Yes No
	AL61						Yes No
	AM61						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN61	
	AO61	
	AP61	
	AQ61	
	AR61	

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA62	6,437,639 B1	08/2002	Nguyen *et al.*			
	AB62	2002/0037706 A1	03/2002	Ichihara			
	AC62	4,441,080	04/1984	Saari			
	AD62	4,873,492	10/1989	Myer			
	AE62	5,697,074	12/1997	Makikallio *et al.*			
	AF62	5,784,689	07/1998	Kobayashi			
	AG62	6,335,656 B1	01/2002	Goldfarb *et al.*			
	AH62	6,690,232 B2	02/2004	Ueno *et al.*			
	AI62	5,636,140	06/1997	Lee *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ62						Yes No
	AK62						Yes No
	AL62						Yes No
	AM62						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN62	
	AO62	
	AP62	
	AQ62	
	AR62	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*NAME*	*CLASS*	*SUB-CLASS*	*FILING DATE*
	AA63	6,366,622 B1	04/2002	Brown *et al.*			
	AB63	6,600,795 B1	07/2003	Ohta *et al.*			
	AC63	4,250,458	02/1981	Richmond *et al.*			
	AD63	5,760,629	06/1998	Urabe *et al.*			
	AE63	6,084,465	07/2000	Dasqupta			
	AF63	6,204,789 B1	03/2001	Nagata			
	AG63	6,064,054	05/2000	Waczynski *et al.*			
	AH63	5,218,562	06/1993	Basehore *et al.*			
	AI63	5,239,496	08/1993	Vancraeynest			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*COUNTRY*	*CLASS*	*SUB-CLASS*	*TRANSLATION*
	AJ63						Yes No
	AK63						Yes No
	AL63						Yes No
	AM63						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	*DOC. REF.*	*CITATION*
	AN63	
	AO63	
	AP63	
	AQ63	
	AR63	

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA64	5,896,304	04/1999	Tiemann *et al.*			
	AB64	6,005,903	12/1999	Mendelovicz			
	AC64	5,834,979	11/1998	Yatsuka			
	AD64	6,798,351 B1	09/2004	Sorrells *et al.*			
	AE64	6,813,485 B2	11/2004	Sorrells *et al.*			
	AF64	5,410,270	04/1995	Rybicki *et al.*			
	AG64	6,509,777 B2	01/2003	Razavi *et al.*			
	AH64	5,982,329	11/1999	Pittman *et al.*			
	AI64	6,208,636 B1	03/2001	Tawil *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ64						Yes No
	AK64						Yes No
	AL64						Yes No
	AM64						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
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	AO64	
	AP64	
	AQ64	
	AR64	

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA65	3,614,630	10/1971	Rorden			
	AB65	6,836,650 B2	12/2004	Sorrells *et al.*			
	AC65	5,844,868	12/1998	Takahashi *et al.*			
	AD65	6,385,439 B1	05/2002	Hellberg			
	AE65	6,741,139 B2	05/2004	Pleasant *et al.*			
	AF65	6,823,178 B2	11/2004	Pleasant *et al.*			
	AG65	6,850,742 B2	02/2005	Fayyaz			
	AH65	6,853,690 B1	02/2005	Sorrells *et al.*			
	AI65	4,789,837	12/1988	Ridgers			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ65						Yes No
	AK65						Yes No
	AL65						Yes No
	AM65						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN65	
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	AQ65	
	AR65	

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA66	5,634,207	05/1997	Yamaji *et al.*			
	AB66	5,642,071	06/1997	Sevenhans *et al.*			
	AC66	6,211,718 B1	04/2001	Souetinov			
	AD66	6,212,369 B1	04/2001	Avasarala			
	AE66	6,308,058 B1	10/2001	Souetinov *et al.*			
	AF66	6,633,194 B2	10/2003	Arnborg *et al.*			
	AG66	2001/0036818 A1	11/2001	Dobrovolny			
	AH66	6,873,836 B1	03/2005	Sorrells *et al.*			
	AI66	6,879,817 B1	04/2005	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ66						Yes No
	AK66						Yes No
	AL66						Yes No
	AM66						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
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	AO66	
	AP66	
	AQ66	
	AR66	

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA67	6,057,714	05/2000	Andrys *et al.*			
	AB67	2003/0081781 A1	05/2003	Jensen *et al.*			
	AC67	5,994,689	11/1999	Charrier			
	AD67	6,512,544 B1	01/2003	Merrill *et al.*			
	AE67	6,628,328 B1	09/2003	Yokouchi *et al.*			
	AF67	6,801,253 B1	10/2004	Yonemoto *et al.*			
	AG67						
	AH67						
	AI67						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ67						Yes No
	AK67						Yes No
	AL67						Yes No
	AM67						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN67	
	AO67	
	AP67	
	AQ67	
	AR67	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ARTIFACT SHEET

Enter artifact number below. Artifact number is application number + artifact type code (see list below) + sequential letter (A, B, C ...). The first artifact folder for an artifact type receives the letter A, the second B, etc..
Examples: 59123456PA, 59123456PB, 59123456ZA, 59123456ZB

10/973,917 UA

Indicate quantity of a single type of artifact received but not scanned. Create individual artifact folder/box and artifact number for each Artifact Type.

☐ CD(s) containing:

- computer program listing ☐
  Doc Code: Computer Artifact Type Code: P
- pages of specification and/or sequence listing and/or table ☐
  Doc Code: Artifact Artifact Type Code: S
- content unspecified or combined ☑
  Doc Code: Artifact Artifact Type Code: U

☐ Stapled Set(s) Color Documents or B/W Photographs
Doc Code: Artifact Artifact Type Code: C

☐ Microfilm(s)
Doc Code: Artifact Artifact Type Code: F

☐ Video tape(s)
Doc Code: Artifact Artifact Type Code: V

☐ Model(s)
Doc Code: Artifact Artifact Type Code: M

☐ Bound Document(s)
Doc Code: Artifact Artifact Type Code: B

☐ Confidential Information Disclosure Statement or Other Documents marked Proprietary, Trade Secrets, Subject to Protective Order, Material Submitted under MPEP 724.02, etc.
Doc Code: Artifact Artifact Type Code X

☐ Other, description: _____
Doc Code: Artifact Artifact Type Code: Z

March 8, 2004

Please forward to Group Art Unit 2662

Amended Compact Discs

EXAMINER NOTE: THIS PAPER IS AN INTERNAL WORKSHEET ONLY. DO NOT ENCLOSE WITH ANY COMMUNICATION TO THE APPLICANT. ITS PURPOSE IS ONLY THAT OF AN AID IN HIGHLIGHTING A PARTICULAR PROBLEM IN A COMPACT DISC.

THE ATTACHED CD (COPY 1) HAS BEEN REVIEWED BY OIPE FOR COMPLIANCE WITH 37 CFR 1.52(E). ***Please match this CD with the application listed below.***

Date: 8/31/2005
Serial No./Control No. 16/973917
Reviewed By: K. SMITH Phone: 308 9210 Ref. 118

☐ The compact discs are readable and acceptable.

☐ Copy 1 and Copy 2 of the compact discs are not the same.

☐ The compact discs are unreadable.

☐ The files on the compact discs are not in ASCII.

☐ The compact discs contain at least one virus.

☑ Other NOT PROPER SUBJECT MATTER FOR CD.

IPW

Sterne Kessler Goldstein Fox
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OIPE IAP13 OCT 24 2005 PATENT & TRADEMARK OFFICE

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Christopher J. Walsh
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Jeffrey Mills

Of Counsel
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Marvin C. Guthrie

*Admitted only in Maryland
*Admitted only in Virginia
•Practice Limited to Federal Agencies

October 24, 2005

WRITER'S DIRECT NUMBER:
(202) 772-8898
INTERNET ADDRESS:
NDRETAR@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2662

Attn: Mail Stop Amendment

Re: U.S. Patent Application
Application No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Supplemental Information Disclosure Statement;

2. Form PTO-1449 listing nineteen (19) documents and accompanied by two (2) documents (IDS Doc. Refs. AM23 and AR59); and

3. One (1) Return Postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Nicole D. Dretar
Attorney for Applicants
Registration No. 54,076

NDD/srb
Enclosures

457328_1.DOC

OIPE
OCT 24 2005
PATENT & TRADEMARK OFFICE

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
Sorrells *et al.*	Art Unit: 2662
Appl. No.: 10/973,917	Examiner: Kizou, Hassan
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Information Disclosure Statement filed on August 9, 2005 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Document AM23 was cited in an Office Action in related German Patent Application No. 19983659.0-35, filed October 20, 1999, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,557,641, which as already been cited in the present application.

Document AR59 is an English-language abstract of document AM23.

Document AN60 is a co-pending U.S. patent application, directed to related subject matter.

Documents AG67 and AH67 were cited in a Notice of Allowance in related U.S. Patent Application No. 09/632,855, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments," directed to related subject matter.

Document AI67 was cited in an Office Action in related U.S. Patent Application No. 09/796,824, filed March 2, 2001, entitled " Phased Array Antenna Applications of Universal Frequency Translation," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,742,189, which has already been cited in the present application.

Documents AA68-AC68 were cited in an Office Action in related U.S. Patent Application No. 10/318,207, filed December 13, 2002, entitled "Method And Apparatus For Reducing Re-Radiation Using Techniques Of Universal Frequency Translation Technology," directed to related subject matter.

Documents AD68-AG68 were cited in a Notice of Allowance in related U.S. Patent Application No. 09/855,851, filed May 16, 2001, entitled "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AH68, AI68, and AA69 were cited in an Office Action in related U.S. Patent Application No. 10/315,174, filed December 10, 2002, entitled "Reducing DC Offsets Using Spectral Spreading," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,999,561 and 6,686,879, which have already been cited in the present application.

Documents AB69-AD69 were cited in a Notice of Allowance in related U.S. Patent Application No. 10/359,636, filed February 7, 2003, entitled "Integrated Frequency Translation and Selectivity," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,126,682; 5,926,054; 6,049,706; 6,421,534; and 6,560,301, which have already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received

by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more

than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of ____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language document AM23 appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document AM23 (DE 69221098T2) appears to describe a radiofrequency frequency multiplier comprising an automatic level control circuit. An English-language abstract of document AM23 is enclosed as document AR59. It is also noted that document AM23 is a counterpart of European Patent Publication EP 0 548 542 A1, which has already been cited in the present application.

☒ 7. Copies of documents AM23 and AR59 are enclosed. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents cited on the attached Form PTO-1449 are not enclosed. In addition, document AN60 is available to the Examiner on the USPTO's IFW System, therefore a copy is not submitted herewith.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No.

6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000, 09/476,093, filed January 3, 2000, 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Nicole D. Dretar
Attorney for Applicants
Registration No. 54,076

Date: October 24, 2005

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

453165_1.DOC

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2662

U.S. PATENT & TRADEMARK OFFICE
OCT 24 2005
TECH CENTER 1600/2900

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG67	3,737,778	06/1973	Van Gerwen *et al.*			
	AH67	4,286,283	08/1981	Clemens			
	AI67	4,241,451	12/1980	Maixner *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM23	DE 692 21 098 T2	01/1998	DE			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
	AR59	English Abstract for German Patent No. DE 692 21 098 T2, 1 page, data supplied from the espacenet.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

453141_1.DOC

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2662

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OCT 24 2005
PATENT & TRADEMARK OFFICE
MAIL 13

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA68	5,014,130	05/1991	Heister *et al.*			
	AB68	5,390,215	02/1995	Anita *et al.*			
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	AL						Yes No
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(54) Radiofrequenzvervielfachen mit selbsttätiger Pegelsteuerungsschaltung

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BESCHEIBRUNG

Die vorliegende Erfindung bezieht sich auf das Gebiet der Erzeugung von Sinuswellensignalen mit Abtastfrequenz und, spezifischer, auf einen Radiofrequenzvervielfacher mit selbstständiger Pegelsteuerungsschaltung.

Wie bekannt, entstehen bei den verschiedenen Anwendungen der Elektroniktechnik Probleme hinsichtlich der Erzeugung von Sinuswellen-Bezugssignalen mit einer angemessenen voreingestellten Frequenz.

So ist es beispielweise bei Sende- und Empfangsgeräten die Präsenz eines lokalen Oszillatorsignals von wesentlicher Bedeutung, um die erforderlichen und bekannten Umwandlungen vornehmen zu können.

In der funkunterstützten Navigation existiert ein Netz von Leitstrahlsendern zur Überwachung der mit Schiffen oder Flugzeugen zurückzulegenden Strecken. Jeder dieser Leitstrahlsender übermittelt kontinuierlich ein eigenes, extrem starkes Sinuswellen-Radiofrequenzsignal.

Aus Gründen der Knappheit beziehen sich die oben aufgeführten Beispiele lediglich auf zwei von mehreren Anwendungsgebieten von Funkfrequenz-Bezugssignalen.

In vielen Fällen ist es von Vorteil, besagte Funkfrequenz-Bezugssignale über den Einsatz von Oszillatoren mit extrem tiefer Frequenz zu erzeugen, die entsprechend einfacher eingebaut werden können. In diesem Fall reicht es aus, die Oszillatorsignalfrequenz in der erforderlichen ganzen Zahl zu vervielfältigen.

Die Vervielfältigung von Frequenzen wird bekanntlich ausgeführt, indem das Submultipel-Frequenzsignal durch eine Vorrichtung gesandt wird, die eine Verzerrung des Eingangssignals bewirkt und Oberwellen eines höheren Größenordnung erzeugt. Das Submultipel-Frequenzsignal wird erzeugt, indem das verzerrte Signal über einen Bandpaßfilter gefiltert wird, dessen Schmalbandbereich auf die entsprechenden Oberwellen der gewünschten Frequenz abgestimmt ist.

In den meisten Fällen der Anwendungstechniken ist es erforderlich, daß das über Frequenzvervielfältigung erzielte Bezugssignal einen konstanten Leistungspegel hat. In der praktischen

Anwendung können jedoch Fälle auftreten, in denen die Ebene des Oszillatorsignals große Schwankungen aufweist; in diesen Fällen ist selbst das über Vervielfältigung erziele Signal, soweit keine entsprechenden Maßnahmen getroffen werden, von diesem Schwankungen betroffen.

Dieses Phänomen tritt hauptsächlich auf, wenn der Oszillator nicht im gleichen Gerät eingebaut ist, in welchem auch die Multipliziereinheit installiert ist, so beispielweise, wenn die Übertragung des Oszillatorsignals zur Multipliziereinheit über Koaxialkabel stattfindet.

Um dieser Problematik zu begegnen, enthalten die gängigen und bekannten Bezugssignalerzeuger, die zur Frequenzvervielfältigung eingesetzt werden, einen Regelkreis mit oder ohne Rückkopplung, welcher den Pegel der Ausgangsleistung des erzeugten Signals regelt.

In den zunächst bekannten Bezugssignalerzeugern mit einem nicht rückgekoppelten Regelkreis findet die Regelung der Ausgangsleistung des erzeugten Signals über ein Gerät zur Amplitudenkomprimierung statt, welches am Ausgang des Frequenzvervielfältigers installiert wird.

Diese leicht herzustellenden Erzeuger weisen jedoch verschiedene Probleme auf. Ein erstes Problem betrifft den Umstand, daß die Dynamik der Pegel der Ausgangsleistung des Oszillatorsignals durch diese Erzeuger stark begrenzt werden. Ein zweites Problem bezieht sich auf den Umstand, daß das Gerät zur Amplitudenkomprimierung einen exzessiven Anteil von Oberwellen einer unerwünschten Größenordnung erzeugt. Dazu kommt, daß die Stabilisierung des Ausgangspegels schlecht ist.

Ein zweiter Typ der bekannten Bezugssignalerzeuger mit einem rückgekoppelten Regelkreis wird im Schriftstück US-A-3808539 beschrieben. Bei dieser Beschreibung ist der Bezugssignalerzeuger ein Frequenzvervielfältiger, der zu einem über Batterie betriebenen Radiosender gehört. Zur dieser Einheit zur Frequenzmultiplikation gehören drei kapazitiv gekoppelte NPN-Transistoren, von denen der erste (Q1) zu einer Vorverstärkungsstufe, der zweite (Q2) zur Frequenzmultiplikation gehören, während und der dritte (Q3) Transistor ein RF-Leistungsverstärker ist. Zwischen dem zweiten und dem dritten Transistor ist ein Bandpaßfilter installiert, über den die gewünschten RF-Oberwellen selektioniert werden. Ein lokaler Oszillator (in den Abbildungen nicht zu sehen) erzeugt das zum Vorverstärker (Q1) geleitete RF-Sinuswelleneingangssignal. Der Regelkreis erzeugt im Emitter-Kollektor-Pfad des dritten Transistors

einen Leistungsdetektor-Rückkopplungswiderstand, um für den Emitter-Kollektor-Pfad des ersten Transistors eine Gleichstrom-Rückkopplungsspannung zu erzeugen. Diese Rückkopplungsspannung liefert eine Vorspannung für den ersten Transistor, so daß bei einem Abfall der Batteriespannung (und folglich der RF-Ausgangsleistung) der Grad der Vorverstärkerstufe gesteigert wird, und somit die RF-Ausgangsleistung der selektionierten Oberwelle nahezu konstant gehalten werden kann. Zusätzlich zu vorstehend beschriebenen Regelung stabilisiert der rückgekoppelte Regelkreis die Ausgangsleistung in Abhängigkeit zu den Schwankungen des Oszillatorsignals. In diesem Falle dient die Vorverstärkerstufe als Dämpfungsregler des Oszillatorsignals, oder, allgemeiner gesagt, zur Regulierung des Pegels des Oszillatorsignals.

Die größte Problematik dieses zweiten Typs der Bezugssignalerzeuger liegt in einem extrem kostenaufwendigen Einbau, insbesonders in Fällen, wenn das Signal, dessen Frequenz multipliziert werden soll, im Mikrowellenbereich liegt. In diesen Fällen ist es daher notwendig, daß sowohl die Rückkopplungseinheit (Leistungsdetektor) als auch den Regler des Oszillationssignalpegels (Dämpfungsregler) entsprechend der Mikrowellentechnik gespeist wird. Des weiteren muß zwischen den Ausgang der Einheit zur Frequenzmultiplikation und der Rückkopplungseinheit ein Koppler eingefügt werden.

Der Zweck, den die vorliegende Erfindung verfolgt, richtet sich somit auf eine Behebung der oben beschriebenen Probleme und die Angabe eines Radiofrequenz-Sinuswellensignalerzeugers, welcher aus einer Einheit zur Frequenzmultiplikation besteht, die den Leistungspegel der erzeugten Oberwellen selbsttätig steuert.

Um dieser Zielsetzung gerecht zu werden, liegt der Sinn der vorliegenden Erfindung in einer Einheit zur Funkfrequenzvervielfachung, die ausgestattet ist mit einem Transistor, welcher das Oszillatorsignal verstärkt und verzerrt, einem Bandpaßfilter, der am Ausgang des auf die im Ausgang gewünschte Oberwelle abgestimmten Transistors installiert ist sowie einem Regelkreis zur Leistungsstabilisation der obengenannten Oberwelle über automatische Veränderung der Polarisationsspannung des Transistors bei Veränderung des Leistungspegels des Oszillatorsignals, wie genauer beschrieben unter Punkt 1) der Inanspruchnahme.

Die wesentliche Neuigkeit der Einheit zur Funkfrequenzvervielfachung, die den Gegenstand der vorliegenden

Erfindung darstellt, ist der Umstand, daß zur dieser Einheit im Gegensatz zu bekannten Technologien ein Regelkreis gehört, welcher den Transistor versorgt und polarisiert. Dieser Regelkreis kann ebenso als idealer Erzeuger einer Voltspannung angesehen werden, welche abhängig zur eingesetzten Transistorart sowie abhängig zur Größenordnung der im Ausgang selektionierten Oberwelle und des zu stabilisierenden Leistungspegels über eine entsprechende Regelfunktion entsprechend verändert werden kann.

Der vorgenannte Regelkreis arbeitet unter Quasi-Gleichstrom-Bedingungen sowie unabhängig zur Frequenz des Signals, dessen Leistung gesteuert wird. Aus diesem Grunde kann die Einheit zur Funkfrequenzvervielfachung, die den Gegenstand der vorliegenden Erfindung darstellt, unabhängig zur Frequenz des erzeugten Signals kostengünstig hergestellt und problemlos installiert werden. Insbesondere ist die Einheit von Vorteil, wenn die Frequenz des Oszillatorsignals im Mikrowellenbereich liegt.

Ein weiterer Vorteil besteht in der Tatsache, daß die Leistung des erzeugten Oberwellensignals ohne eine Begrenzung der Dynamik des Leistungspegels des Oberwellensignals stabilisiert werden kann.

Weitere Zielsetzungen und Vorteile der vorliegenden Erfindung gehen aus der genauen Beschreibung hervor, die nach einem Beispiel zur Ausführung der Einheit aufgeführt ist sowie die nachstehend beschriebenen technischen Zeichnungen in der Anlage, welche als unverbindliche Beispiele abgebildet sind:

Die ABB. 1 zeigt ein teilweise als Blockdiagramm ausgeführtes Verdrahtungsschema der Einheit zur Funkfrequenzvervielfachung, die den Gegenstand der vorliegenden Erfindung darstellt.

Die ABB. 2, 3, 4 und 5 zeigen Diagramme einiger elektrischen Charakteristiken, welche die Funktion der in Abb. 1 dargestellten Einheit zur Funkfrequenzvervielfachung erläutern.

Die ABB. 6 zeigt ein genaues Verdrahtungsschema einer zur Einheit zur Funkfrequenzvervielfachung, die den Gegenstand der vorliegenden Erfindung darstellt, gehörenden Steuereinheit.

Unter Bezugnahme auf die ABB. 1 wird mit T1 ein MESFET Feldtransistor bezeichnet, dessen Steueranschluß G an je eine Endklemme des Kondensators C1, eines Widerstandes R_G und eines Induktors L1 angeschlossen ist. Die zweiten Endklemmen C1, RG und L1 sind jeweils an einen Steuereingang IN, an Masse sowie an die Eingangsklemme 1 einer Baugruppe CONTR angeschlossen, deren Ausgangsklemme 2 an eine Endklemme des Induktors L2 angeschlossen

ist. Die andere Endstelle des Induktors L2 ist an den Drain-Anschluß D des Feldtransistors T1 sowie an einen Endpunkt eines Kondensators C2 angeschlossen, dessen anderer Endpunkt mit dem Eingang eines Bandpaßfilters FBP verbunden ist. Der Source-Anschluß S des Feldtransistors T1 ist direkt an Erde angeschlossen. Der Ausgang des Bandpaßfilters FBP ist an einen Steuerausgang OUT angeschlossen. Ein Widerstand R_L ist zwischen den Port OUT und Masse angeschlossen. Die Baugruppe CONTR ist weiterhin an einen Gleichstrom-Source-Anschluß angeschlossen, über die eine positive Voltspannung V+ und eine negative Voltspannung V- erzeugt wird.

Beim Betriebs bezieht sich der in der ABB. 1. dargestellte Kreis auf einen im Mikrowellenbereich arbeitenden Radiofrequenzvervielfacher. Dies bedeutet, daß am Steuereingang IN ein Signal $v_i\cos(\omega_o t)$ vorliegt, welches von einem nicht in der Abbildung gezeigten Oszillator ausgeht, dessen Schwingungsfrequenz $f_o = \omega_o/2\pi$ 12 GHz beträgt. Vom Steuerausgang OUT kann ein Signal $v_o\cos(2\omega_o t)$ abgenommen werden, welches der zweiten Oberwellenkomponente bei einer Frequenz von 24 GHz entspricht.

Der Schaltkreis besteht aus einem dünnen Film in Hybridschaltkreistechnik. Sämtliche angegebenen Verbindungen sind Mikrostrip-Verbindungen. Der InduktorL1 besteht aus einer Leitung mit hoher Impedanz zur Übertragung des Oszillatorsignals bei einer Frequenz von 12 GHz sowie einer Leitung mit extrem niedriger Impedanz für Gleichstrom (erzielt über entsprechende Kopplung von Teilstrecken der Leitung in $\lambda/4$ gemäß der den Fachleuten bekannten Technik). Der Induktor L2 besteht aus einer Leitung mit extrem niedriger Impedanz für Gleichstrom sowie einer Leitung mit hoher Impedanz zur Übertragung der 12 GHz Grundschwingung und der 24 GHz zweiten Oberwelle am Ausgang von T1. Die Kondensatoren C1 und C2 bestehen aus gekoppelten Leitungen; die Widerstände R_G und R_L sind Mikrostrip-Leitungsabschnitte, welche für die Signalströme Abschlußwiderstände darstellen. Der im Schaltkreis eingesetzte MESFET-Feldtransistor T1 ist von Typ NEC 673 und speziell auf die betroffenen Frequenzen abgestimmt. Das Signal $v_i\cos(\omega_o t)$ ist an die Endklemme des Source-Anschlusses G von T1 über einen Kondensator C1 und den Abschlußwiderstand R_G gekoppelt.

Die Baugruppe CONTR, deren genaue Funktion nachstehend beschrieben wird, besteht aus einem Regelkreis, über den der Kanal des MESFET-Feldtransistor T1 auf regelbare Art polarisiert wird.

Der obengenannte Regelkreis besteht im Wesentlichen aus Operationsverstärkern und arbeitet unter Quasi-Gleichstrom-Bedingungen. Die Polarisationsströme passieren in unveränderter Form die Induktoren L1 und L2, welche sich zu diesem Zweck wie Kurzschlüsse verhalten. Dagegen wird der Durchgang des Oszillatorsignals und der Grundwelle mitsamt allen Oberwellen am Ausgang von T1 zum Eingang und Ausgang desCONTR-Regelkreises verhindert, da die Induktoren L1 und L2 sich wie offene Stromkreise für die Polarisationsströme und wie Kurzschlüsse für Signale mit Frequenzen $\geq f_o$ verhalten. Die Kapazitanzwerte von C1 und C2 sind derart, daß sie sich wie offene Stromkreise für die Polarisationsströme und wie Kurzschlüsse für Signale mit Frequenzen $\geq f_o$ verhalten.

Wenn am Steuereingang IN kein Signal $v_i\cos(\omega_o t)$ vorliegt, so erzeugt die Baugruppe CONTR eine schwache positive Gleichspannung V_{GS}. In diesem Falle nimmt der Drain-Polarisationsstrom I_D einen Wert an, der leicht über dem Wert des Sättigungsstroms I_{DSS} liegt. Dieser Wert wird jedoch nicht erreicht, da die Baugruppe CONTR den Polarisationsstrom I_D entsprechend begrenzt. Die Baugruppe CONTR erzeugt in Abwesenheit des Signals $v_i\cos(\omega_o t)$ an der Endklemme 2 eine Ausgangsspannung, deren Wert leicht unter dem der Versorgungsspannung V+ liegt. Da keine mit L2 in Reihe geschalteten Widerstände vorhanden sind, entspricht die Ausgangsspannung der Baugruppe CONTR der Polarisationsspannung V_{DS} des MESFET-Feldtransistors T1.

Wenn am Steuereingang IN kein Signal $v_i\cos(\omega_o t)$ vorliegt, wird das besagte Signal über die Gate-Source-Verbindung des Feldtransistors T1 halbwellengleichgerichtet. Dabei bewirken die positiven Halbwellen die Zirkulation eines Stroms innerhalb der Gate-Source-Verbindung des Feldtransistors T1, so daß in diesem Falle eine geringe positive Voltspannung zwischen der Gate-Source-Verbindung entsteht und der Polarisationsstrom I_D als Drain-Strom dient. Durch die negativen Halbwellen dagegen wird die Gate-Source-Verbindung des Feldtransistors T1 polarisiert , so daß Drain-Stromimpulse $i_D(t)$ erzeugt werden.. Der Kondensator C1 sowie der Widerstand R_G bilden einen Hochpaßfilterbereich, in dem das durch die Gate-Source-Verbindung des Feldtransistors T1 gleichgerichtete Signal gefiltert wird. Unter Betriebsbedingungen, wird an den

Endpunkten von C1 eine negative Gleichspannung V_{GS} erzeugt, welche der Direktkomponente des gleichgerichteten Signals $v_i\cos(\omega_o t)$ entspricht. Die besagte Voltspannung V_{GS} trägt zur Polarisierung der Gate-Source-Verbindung des Feldtransistors T1 bei und wird über den InduktorL1 als Steuerspannung an die Eingangsklemme 1 der Baugruppe CONTR geleitet.

Die Impulse des Drain-Stroms i_D enthalten, wie aus den von Fourier vorgenommenen Reihenentwicklungen der mathematischen Funktion $i_D(t)$ hervorgeht, einen Anteil an Sinuswellen an der Grundwellenfrequenz f_o sowie Oberwellen höherer Größenordnung.

Der Strom i_D wird durch den Kondensator C2 geleitet und erreicht den Bandpaßfilter FPB, welcher lediglich den zweiten Oberwellenanteil bei einer Frequenz von 24 GHz unverändert an den Steuerausgang OUT leitet. Dieser Filter ist entsprechend der für Mikrowellenfilter gängigen Technik ausgelegt. Zu seinem Eingangsbereich gehört ein Mikrostrip-Adaptionsnetz, welches den Grundwellenausgang zur Drain-Endklemme des Feldtransistors T1 zurück reflektiert. Der Abstand zwischen FPB und T1 ist derart, daß die reflektierten Wellen in Phase zur im Strom i_D enthaltenen Grundwelle addiert wird, so daß eine entsprechend höhere Leistung an die zweite Oberwelle übertragen werden kann. Die relative Bandbreite um die Frequenz 2 f_o beträgt etwa 10%, was 2,4GHz entspricht, und ermöglicht eine Veränderung der Oszillatorfrequenz in einem breiten Bereich.

Die Baugruppe CONTR steuert die Leistung P_{out}, indem sie als Optimalwertsteuerung (feed forward control) fungiert. Zu diesem Zweck empfängt die Baugruppe am Eingang die Information des Leistungspegels des Signals $v_i\cos(\omega_o t)$, zu dem die Voltspannung VGS in direkter Beziehung steht, und gibt eine angemessen Voltspannung zur Polarisierung des MESFET-Feldtransistors T1 ab.

Die Stabilisierung des Leistungspegels der Baugruppe CONTR kann direkt ermittelt werden über die Auswertung der ABB. 2, die ein Diagramm zeigt, dessen Abszisse den Leistungsstift des Oszillatorsignals $v_i\cos(\omega_o t)$ darstellt, während die Ordinate für die Leistung P_{out} des Ausgangs des Signals $v_i\cos(\omega_o t)$ steht. Die Grafik zeigt die beiden Kurven P_{fet} und P_{gen}. Die Kurve P_{fet} bezieht sich auf eine Messung, die ausschließlich für den Transistor T1 und ohne

Berücksichtigung der Funktion der Baugruppe CONTR vorgenommen wurde, während sich die Kurve P_{gen} auf den gesamten in ABB. 1 gezeigten Kreis bezieht. In beiden Fällen wurden die Kurven bei einem konstanten Wert der Voltspannung V_{DS} von 0,88V ermittelt. Wie im Diagramm ersichtlich wird, ergibt sich eine gute Gleichrichtung.

Wie aus der ABB. 1, und besser noch aus einer Auswertung des in der ABB.6 dargestellten Kreises ersichtlich wird, versorgt die Baugruppe CONTR den Transistor T1 direkt mit einer Voltspannung, die abhängig zur Leistung des Eingangssignals variiert. Die Steuerwirkung beruht auf der Tatsache, daß die Polarisationsspannung V_{DS} abhängig zur Veränderung der Speisespannung von T1 variiert. Folglich berechnet sich die maximale Schwankung der Voltspannung V_{DS} auf der Last RL, bezogen auf die Leistung des Ausgangssignals auf der Relation $P_{out}\ V_{DS}^2/2RL$.

In allen Beispielen bekannter Signalerzeuger mit Transistoren, die als Verstärker/Verzerrer eingesetzt werden, existiert kein Regelkreis zur Regelung der Leistung des Ausgangssignals über automatische Veränderung der Versorgungsspannung des Gerätes. Im Gegenteil wird in normalen Anwendungen von mit Transistoren ausgestatteten Regelkreisen im allgemeinen spezielle Vorkehrungen getroffen, welche sich auf die Gleichrichtung des Betriebspunktes gegenüber Variationen der Transistorversorgungsspannung richten.

Die Ausführbarkeit der Baugruppe CONTR hängt davon ab, ob eine Regelfunktion V_{DS} (V_{GS}) existiert, die die Leistung P_{out} bei einer Veränderung von P_{in} konstant hält. Wenn diese Regelfunktion vorliegt, müssen die Eingangs-/Ausgangsübertragungseigenschaften der Baugruppe CONTR annähernd der Kurve V_{DS} (V_{GS}) des MESFET-Feldtransistors T1 bei P_{out} = ca. 8 dBm entsprechen. Die Existenz einer derartigen Regelfunktion kann theoretisch demonstriert werden. Die Bestimmung dieser Regelfunktion in Bezug zur Einheit zur Frequenzmultiplikation, die den Gegenstand der vorliegenden Erfindung darstellt, erfolgt, wie nachstehend erläutert wird, über entsprechende Versuche.

Der Beweis der Existenz einer Regelfunktion V_{DS} (V_{GS}) besteht in der mathematischen Ermittlung dieser Funktion, wobei ausgegangen wird vom mathematischen Ausdruck der Ausgangsleistung P_{out} . Wie bekannt, ist $P_{out} = (I_n^2/R_L)/2$, wobei I_n für den Strom in Verbindung mit der Oberwellengrößenordnung $\underline{n}$ entsprechend der von Fourier

vorgenommenen Reihenentwicklungen steht der mathematischen Funktion steht, welche die Gesamtheit des Drain-Stroms $i_D(t)$ darstellt.

Eine Methode zur Ermittlung der Funktion $i_D(t)$ und zur Berechnung der Koeffizienten der entsprechenden Reihenentwicklung von Fourier wird im Anhang an das Kapitel Vier (Seiten 144-148) der Veröffentlichung "Communication Circuits: Analysis and Design" von Kenneth K. Clarke und Donald T. Hess beschrieben, veröffentlicht 1971 im Verlag Addison-Wesley Publishing Company.

Diese in dieser Veröffentlichung beschriebene Methode setzt die Kenntnis der Übertragungseigenschaft $i_D(VGS)$ des MESFET-Feldtransistors T1 voraus. Diese Übertragungseigenschaft, in der Veröffentlichung auf den Seiten 134 bis 135 angegeben, wird in einer ersten Annäherung mit $i_D = i_{DSS} (1 - V_{GS}/V_P)^2$ angesetzt, wobei der Ausdruck i_{DSS} für den Drain-Sättigungsstrom steht (Drain-Strom des MESFET-Feldtransistors bei $V_{GS} = 0$ mit jedem beliebigen V_{DS}-Wert innerhalb des Sättigungsbereichs), während der Ausdruck V_P für die Pinch-Off-Spannung steht (Wert V_{GS} für $i_D = 0$).

In der obengenannten Veröffentlichung ist des weiteren eine Grafik des Stroms $i_D(t)$ dargestellt, die in einem zweiten Schritt der Methode ermittelt wurde, indem die Punkte der Funktion $V_{GS}(t) = v_i\cos(\omega_o t)$ auf die Übertragungsfunktion $i_D(V_{GS})$ des MESFET-Feldtransistors projiziert wurden. Die Grafik zeigt eine Abfolge von Stromimpulsen $i_D(t)$ in Entsprechung zu den positiven Halbperioden von $v_i\cos(\omega_o t)$. Die Breite jedes einzelnen Impulses entspricht der Halbwellenfraktion von v_i , in dem der im MESFET-Feldtransistor präsente Drain-Strom zirkuliert, wie dies für einen Verstärker der Klasse C der Fall ist. Die Berechnung des Fourier-Koeffizienten wird abgeschlossen mit Hilfe eines als "Zirkulationswinkel" bezeichneten Parameters $\varnothing$, der zur Begrenzung des Feldes zur Integration der aktuellen Pulsbreite i_D eingeführt wird.

In den in der ABB. 4.A-2 auf der Seite 147 der oben genannten Veröffentlichung gezeigten Beispielen ist $\varnothing = \text{arc cos } (V_P/V_i)$, wobei V_i die maximale Amplitude des Signals $v_i\cos(\omega_o t)$ darstellt und V_P für die Pinch-Off-Spannung des MESFET-Feldtransistors steht. In der Mehrzahl der praktischen Anwendungen, so zum Beispiel im für Fall den Feldtransistor T1 geltenden Fall, ist der

Zirkulationswinkel Ø ebenfalls eine Funktion der Polarisierungswerte V_{GS} und V_{DS}.

In der letzten Phase der Methode wird der mathematische Ausdruck für den allgemeinen Koeffizienten I_n ermittelt. Dieser Koeffizient ist eine recht komplexe Funktion des Zirkulationswinkels Ø und des Spitzenwertes I_p des Stromimpulses i_D. Der Spitzenwert I_p dagegen ist von i_{DSS} und dem Quadrat von V_i abhängig.

Die oben beschriebene Berechnungsmethode ist ebenso für den MESFET-Feldtransistor T1 anwendbar, da der Strom $i_D(t)$ in diesem Falle ebenso in einer Abfolge von Impulsen besteht, die ähnlich zu den in der oben beschriebenen Grafik aufgeführten Impulsen sind. Die wichtigsten Unterschiede zwischen dem Betrieb von T1 und dem in der obengenannten Methode aufgeführten FET-Betrieb besteht darin, daß die Impulse $i_D(t)$ eine Entsprechung zu den negativen Halbwellen von $v_i\cos(\omega_o t)$ zirkulieren und daß T1 im linearen Bereich eher von der Sättigung als von der Sperrung ausgehend gesteuert wird. Wie ersichtlich ist, sind die Unterschiede nicht besonders groß.

Eine standardisierte Darstellung von (I_n/ I_p) zur Tendenz der ersten drei Koeffizienten als Funktion des Zirkulationswinkels Ø wird in der ABB. 4.4-4 auf Seite 102 der obengenannten Veröffentlichung gezeigt.

Die Leistung $P_{out} = (I_n^2/R_L)/2$ einer allgemeinen, am Ausgang selektionierten Oberwelle ist, wie aus der Gesamtheit der oben beschriebenen theoretischen Betrachtungen abgeleitet werden kann, eine Funktion des physischen Wertes I_{DSS} ,V_P von T1 sowie der Amplitude v_i des Oszillationssignals $v_i\cos(\omega_o t)$; es gilt daher $P_{out} = P_{out}\ (I_{DSS}, V_P, v_i)$.

In Anbetracht, daß V_{GS} von der Berichtigung des Oszillationssignals $v_i\cos(\omega_o t)$ über T1 abhängig ist, ergibt sich $P_{out} = P_{out}\ (I_{DSS}, V_P, V_{GS})$.

Aus den oben beschriebenen theoretischen Betrachtungen geht in keiner Weise die Abhängigkeit von P_{out} zur Polarisationsspannung V_{DS} hervor, da der Kanalwiderstand r_o des Feldtransistors T1 in der ersten Annäherung nicht berücksichtigt wird. Es ist möglich, diese Berücksichtigung des Kanalwiderstand in die Methode zur Berechnung des Koeffizienten I_n der Fourier-Berechnungen des Stroms $i_D(t)$

einzubeziehen, in dem man anstelle des Sättigungsstroms I_{DSS} einen Sättigungsstrom

$I'_{DSS} = I_{DSS} [1 + (V_{DS} + V_p) / r_o I_{DSS})]$ ansetzt;

so daß deutlich wird, daß der Ausdruck P_{out} zur Polarisationsspannung V_{DS} abhängig ist.

Zusammengefaßt gilt für den Ausdruck P_{out}:

$P_{out} = P_{out} (I_{DSS}, V_P, V_{GS}, V_{DS})$.

Da nach der Auswahl des im Kreis einzusetzenden MESFET Feldtransistortyps die Parameter I_{DSS}, V_P, und r_o konstant sind, kann der Ausdruck P_{out} vereinfacht werden, so daß sich als Endergebnis $P_{out} = P_{out} (V_{GS}, V_{DS})$ ergibt.

Es ist nun möglich, die Regelfunktion $V_{GS} (V_{DS})$ auf rein analytische Weise zu bestimmen, in dem zunächst die Größenordnung der am Ausgang selektionierten Oberwelle und anschließend für diese Oberwelle die Funktion P_{out} bestimmt wird. Anschließend wählt man den gleichzurichtenden Wert P_{out}, der im allgemeinen im unmittelbar an den Höchstwert angrenzenden Bereich gesucht werden sollte, den der FET- Feldtransistor zur Übertragung zur selektionierten Oberwelle benötigt. Schließlich wird die Variable V_{DS} aus der Relation $P_{out} (V_{GS}, V_{DS}) =$ konstant expliziert, so daß die gewünschte Regelfunktion $V_{GS} (V_{DS})$ erzielt wird.

Wie man sieht, stellt sich die mathematische Bestimmung der Regelfunktion als allzu kompliziert und somit recht schwierig heraus. Die Folge der einzelnen in der Berechnungsmethode angesetzten Schritte wird primär in der Absicht angegeben, um die grundsätzliche Existenz dieser Regelfunktion zu belegen. In der Praxis ist es einfacher, die Regelfunktion experimentell über eine Reihe von Messungen des MESFET Feldtransistors T1 zu ermitteln, wie angegeben in den Erläuterungen zu den ABB. 3, 4 und 5, die sich auf Messungen beziehen, die ausschließlich für den MESFET Feldtransistor T1, d.h. unter Ausschluß des CONTR-Regelkreises vorgenommen wurden.

Die ABB. 3 zeigt ein Diagramm, dessen Abszisse den Logarithmus der Leistung P_{in} des Oszillatorsignals $v_i \cos(\omega_o t)$ und dessen Ordinate das Modul der Polarisationsspannung V_{GS} des Feldtransistors T1 darstellt. Die Kurve wurde für einen konstanten Wert der Polarisationsspannung V_{DS} gleich 0,88V angelegt. Wie aus dem Diagramm hervorgeht, erfolgt der Anstieg der Polarisationsspannung

V_{GS} linear zum Dezimallogarithmus der Leistung P_{in} , so daß abgeleitet werden kann, daß sich die Gate-Source-Verbindung des Feldtransistors T1 wie ein Detektor der Leistung des Oszillationssignals verhält.

Die ABB. 4 zeigt ein Diagramm, dessen Abszisse der Polarisationsspannung V_{DS} des Feldtransistors T1 entspricht und dessen Ordinate den Logarithmus der Leistung P_{out} der auf der Last RL gemessenen zweiten Oberwellenkomponente $v_o\cos(2\omega_o t)$ darstellt. Die Kurve ergab sich, indem an den Eingang des Feldtransistors T1 ein Oszillationssignal mit einer konstanten Leistung von 10 dBm übermittelt wurde. Wie aus dem Diagramm hervorgeht, ist der Logarithmus der Leistung P_{out} auf beinahe lineare Art von der Polarisationsspannung V_{DS} abhängig, was die Realisation eines Kreises zur Regelung der Leistung P_{out} über die Polarisationsspannung V_{DS} beweist.

Die ABB. 5 zeigt ein Diagramm, dessen Abszisse der Voltspannung V_{GS} und dessen Ordinate der Polarisationsspannung V_{DS} des Feldtransistors T1 entspricht. In der Grafik sind zwei Kurven eingetragen, von denen sich die erste, mit G1 gekennzeichnete, auf die experimentell erzielte Regelfunktion V_{GS} (V_{DS}) bezieht, während die zweite, mit G2 gekennzeichnete Kurve die Übertragungsfunktion der Baugruppe CONTR darstellt. Die mit G2 gekennzeichnete Kurve nähert sich der Kurve G1 über zwei Segmente einer Geraden mit unterschiedlichen Neigungen G2' und G2", welche sich im Punkt A treffen.

Die Kurve G1 wurde über Punkte erzielt, indem die Leistung P_{in} verändert und die entsprechende Voltspannung V_{GS} gemessen wurde. Für jeden Wert von V_{GS} wurde die Voltspannung V_{DS} soweit verändert, bis daß die Leistung P_{out} des auf der Last RL gemessenen Signals $v_o\cos(2\omega_o t)$ konstant 8 dBm betrug. Die Ordinate der Grafik zeigt die entsprechenden V_{DS}-Werte. Wie aus der Grafik hervorgeht, verläuft der Abstieg der Kurve G1 auf expenetiale Weise. Die wichtigste Veränderung der Regelfunktion V_{GS} (V_{DS}) bezieht sich auf etwa ein Drittel der auf der Abszisse zur Achse V_{GS} bezogenen Werte. Diese Eigenschaft paßt bestens zur Annäherung der beiden Segmente der Kurve G2. In der Tat hat das Segment G2' eine stärkere Steigung und nähert sich dem ersten Teil der Funktion an, während das Segment G2"

eine geringere Steigung hat und sich dem asymptotischen Teil der Funktion nähert. Im in der ABB. 6 gezeigten Kreis wird die Kurve G2 über den Einsatz von Operationsverstärkern synthetisiert.

Unter Bezugnahme auf die ABB. 6 werden mit OP1. OP2, OP3 und OP4 vier identische Operationsverstärker angegeben, die gemeinsam mit Voltspannungen +V und -V gespeist werden. Der Umkehrungseingang (-) von OP1 ist angeschlossen an einen Endpunkt von zwei Widerständen R3 und R6, deren anderen Endpunkte an Masse sowie jeweils an den Ausgang des OP1 angeschlossen sind. Die nichtumkehrenden Endklemme (+) von OP1 ist an einem Endpunkt von zwei Widerständen R4 und R5 angeschlossen, deren anderen Endpunkte jeweils an den Eingang des der Endklemme 1 des Regelkreises CONTR sowie an den Mittelpunkt der Reihe der beiden Widerstände R1 und R2, deren anderen Endpunkte an den Source-Anschluß der Voltspannung +V sowie an Masse angeschlossen sind.

Der Eingang (+) des Operationsverstärkers OP2 ist direkt an Masse angeschlossen. Der Eingang (-) dieses Operationsverstärkers ist angeschlossen an einen Endpunkt von drei Widerständen R9, R10 und R11, deren andere Endpunkte jeweils an die Eingangsklemme 1 des CONTR- Regelkreises, an den Mittelpunkt der Reihe der beiden Widerstände R7 und R8 und an die Kathode einer Diode D1 angeschlossen sind, deren Anode mit dem Ausgang des Operationsverstärkers OP2 verbunden ist. Die anderen Endpunkte der Widerstände R7 und R8 sind jeweils an den Source-Anschluß der Voltspannung +V sowie an Masse angeschlossen. Ein Widerstand R12 ist zwischen Kathode der Diode D1 und Masse angeschlossen.

Der Eingang (+) des Operationsverstärkers OP3 ist direkt an Masse angeschlossen. Der Eingang (-) dieses Operationsverstärkers ist angeschlossen an einen Endpunkt von zwei Widerständen R14 und R15, deren andere Endpunkte jeweils an die Anode der Diode D2 sowie an den Ausgang des Operationsverstärkers OP3 angeschlossen sind. Ein Widerstand R13 ist zwischen dem Source-Anschluß der Voltspannung +V und der Anode der Diode D2 angeschlossen, deren Kathode an Masse angeschlossen ist.

Der Eingang (-) des Operationsverstärkers OP4 ist an einen Endpunkt von zwei Widerständen R16 und R20 angeschlossen, deren andere Endpunkte jeweils an Masse sowie an den Ausgang des Operationsverstärkers OP4 angeschlossen sind, während die entgegengesetzten Enden an die Endklemmen des Ausgangs 2 des CONTR-Regelkreises angeschlossen sind. Der Eingang (+) des Operationsverstärkers OP4 ist an einen Endpunkt von drei

Widerständen R17, R18 und R19 angeschlossen, deren andere Endpunkte jeweils an den Ausgang des Operationsverstärkers OP1, die Kathode der Diode D1 sowie an den Ausgang des Operationsverstärkers OP3 angeschlossen sind. Die Ausgangsspannungen der Opertionsverstärker OP1, OP2 und OP3 sind jeweils an V1, V2 und V3 angeschlossen. Die Ausgangsspannung des Operationsverstärkers OP4 ist die Polarisationsspannung des MESFET Feldtransistors T1.

Im Betriebsstaus fungiert der OperationsverstärkerOP1 als nichtumkehrender Voltspannungsaddierer; seine Ausgangsspannung V1 ist durch den Ausdruck $V1 = \mu 1 V_{GS} + K1$ gegeben, wobei $\mu 1$ für die Voltsumme bei geschlossenem Ring des OP1-Addierers steht und K1 die Voltspannung für $V_{GS} = 0$ ist. Der Ausdruck $\mu 1 > 0$ wird definiert durch die Wahl der entsprechenden, für die Widerstände R1, R2, R3, R4, R5 und R6 geltenden Werte. Der Ausdruck $K1 > 0$ wird definiert durch das Produkt der positiven Voltspannungen +V, multipliziert mit einem entsprechenden für die obengenannten Widerstände geltenden Beziehungswert. Auf der Ebene (V_{DS} ,V_{GS}) der ABVB. 5 entspricht die Voltspannung V1 einer Geraden mit positiver Neigung (in Abb. nicht zu sehen), die parallel zum Streckenabschnitt G2' verläuft.

Der OperationsverstärkerOP2 ist ein umkehrender Voltspannungsaddierer, der an dem Ausgang mit einer Diode ausgerüstet ist, über welchen ein Schwellenwert für die Voltspannung VGs eingefügt wird, bevor der Ausgangssignalspannung V2 Null beträgt. Die Voltspannung V2 ist durch den folgenden Ausdruck gegeben:

$$V2 = (-\mu 2 V_{GS} - K2) \times F_{scal} (V_{GS} - V_{SL}),$$

wobei $-\mu 2$ für die Voltsumme bei geschlossenem Ring des OP2-Addierers steht, die bestimmt wird durch die entsprechenden, für die Widerstände R7, R8, R9, R10, R11 und R12 geltenden Werte. Der Ausdruck -K2 ist abhängig vom Produkt der positiven Voltspannungen +V, multipliziert mit einem entsprechenden für die obengenannten Widerstände geltenden Beziehungswert. F_{scal} steht für die Schrittfunktion, die für $|V_{GS}| < V_{SL}$ gleich 0 und für $|V_{GS}| > V_{SL}$ gleich 1 ist, wobei V_{SL} für einen entsprechend voreingestellten Grenzwert steht. Zusammenfassend gilt $V_2 = 0$ bei $|V_{GS}| \leq V_{SL}$ und $V_2 = -\mu 2 V_{GS} - K2$ bei $|V_{GS}| > V_{SL}$; wenn $V_{SL} = -1{,}3$ V ist, wird durch die oben angegebenen Beziehungen eine halbe Gerade gebildet (in Abb. 5 nicht zu sehen) mit negativer Neigung und Ausgangspunkt in A.

Der OperationsverstärkerOP3 ist ein umkehrender Verstärker, dessen Ausgangsspannung V3 über den Ausdruck $V3 = -\mu 3 V_{K3}$ gegeben ist, wobei $-\mu 3$ für die Voltsumme bei geschlossenem Ring des OP3-Verstärkers steht und durch die entsprechenden, für die Widerstände R13, R1, und R15 geltenden Werte bestimmt wird. V_{K3} ist eine Voltspannung, welche von den selben Widerständen sowie von der Voltspannung VD2 abhängig ist, die bei Leitung zwischen der Anode und der Kathode der Diode D2 vorliegt. Wie zu sehen ist, ist V3 nicht von V_{GS} abhängig und entspricht gemäß der Ebene (V_{DS} , V_{GS}) in Abb. 5 einer Geraden (in Abb. nicht zusehen). Die parallel zur Achse V_{GS} verläuft und zu dieser Achse in einem Abstand von $-V_{K3}$ liegt. Die Voltspannung V3 kompensiert die Stromveränderungen i_D (t), die durch in der Gate-Source-Verbindung des MESFET-Feldtransistors T1 auftretende thermische Veränderungen bedingt sind.

Der OperationsverstärkerOP4 ist ein nichtumkehrender Voltspannungsaddierer, dessen Ausgangsspannung V_{DS} durch den Ausdruck $V_{DS} = \mu 4V\ (V1 + V2 + V3)$ gegeben ist, wobei $\mu 4$ für die Voltsumme bei geschlossenem Ring des OP4-Verstärkers steht, definiert durch die entsprechenden für die Widerstände R16 und R20 geltenden Beziehungswerte.

Wenn $\mu 4 = 1$ ist, wird die Voltspannung $V_{DS} = V1 + V2 + V3$ durch die in der ABB. 5 gezeigte Kurve G2 dargestellt, die erzielt werden kann, indem man zunächst den Punkt A (1, -1,3) wählt und dann bei $\mu 1 \geq \mu 2$ die Werte für $\mu 1$, $\mu 2$ und $\mu 3$ bestimmt.

Der in ABB. 1 dargestellte Kreis legt hinsichtlich des Bereichs der Betriebsfrequenzen grobe Verallgemeinerungen nahe, die sich sowohl auf den Wert der gleichzurichtenden Leistung als auch auf die Art des eingesetzten Transistors beziehen.

So ist es zum Beispiel möglich, am Ausgang einer Oberwelle hoher Größenordnung im Mikrowellenbereich zu selektionieren, wobei ausgegangen wird von einem Oszillatorsignal mit einer extrem niedrigeren Frequenz.. In diesem Fall wird der Eingangskreis des T1 aus digitalen Komponenten gebaut, während der Ausgangskreis in Mikrostrip-Technik ausgeführt wird. Im allgemeinen und abhängig von der Frequenz des Oszillatorsignals ist es erforderlich, die Größen der Werte von C1, L1 und L2 zu korrigieren und auf der Grundlage der Oberwellen einer vorher selektionierten Größenordnung sowie ausgehend vom Wert von C2 und von der Mittelbandfrequenz des FPB-

Filters die unter dem Gesichtspunkt der Kosten und der Wirksamkeit am besten geeigneten Transistoren zu wählen. Sofern es der spezifische Fall zuläßt, kann es von Vorteil sein, einen abstimmbaren FPB-Bandpaßfilter einzusetzen, dessen Durchlaßbereich um eine der im Ausgangssignal von T1 enthaltenen Oberwellen beliebig abgestimmt werden kann.

Die in der ABB. 5 gezeigten Kurven G1 und G2 beziehen sich auf den Fall einer zweiten Oberwelle mit einer gleichzurichtenden Leistung von 8dBm, einem Wert, der, wie durch die in der Abbildung gezeigten Kurven P_{fet} und P_{gen} ersichtlich wird, in der Nähe des für T1 maximal möglichen Wertes liegt. Im Fall der Gleichrichtung von Leistungen mit tieferen Werten entsteht, für eine vorgegebene Oberwelle, eine Familie von Kurven V_{DS} , V_{GS}, die ähnlich sind wie die in der ABB. 5 gezeigten Kurven, welche alle parallel zueinander sind. Die Form der regulierenden Kurve V_{DS} (V_{GS}) bei Veränderung der am Ausgang selektionierten Oberwellengröße ist nicht wesentlich anders als die exponentiale, in der Kurve G1 (ABB. 5)gezeigten. Auch wenn die Dämpfungskonstante variieren kann, hat dies keine Auswirkung auf die Möglichkeit des Einsatzes eines CONTR-Regelkreises, solange man einen geeigneten Punkt A wählt, der in der Annäherung an zwei Segmente der Kurve G2 (ABB. 5) liegen muß.

Des weiteren ist möglich, die allgemeine Regelfunktion V_{DS} (V_{GS}) zu synthetisieren, indem die Funktion einer durchbrochenen Linie mit mehr als zwei Segmenten angenähert wird; in diesem Falle müssen zum in der ABB. 6 gezeigten CONTR-Regelkreis umkehrende Summierer N-1 wie etwa OP2 gehören, wobei N für die Anzahl der Segmente der durchbrochenen Linie steht. Die einzige in diesem Fall erforderliche Vorkehrung besteht in einer Veränderung der Verstärkerleistung sowie der Schwellenwerte der Diodenzuschaltung.

In Hinsicht auf T1 ist es, soweit es die betroffenen Frequenzen zulassen, möglich, einen zweipoligen Transistor (BJT) einzusetzen. Sowohl FET- als auch BJT-Transitoren sind aktive Transistoren mit drei Endstellen, die, was das gesteuerte Signal betrifft, als Stromerzeuger betrachtet werden können, im Fall des FET-Transistors mit gesteuerter Vorspannung und im Fall des BJT-Transistors mit Stromsteuerung. Bekanntlich müssen beide obengenannten Transistoren zum Betrieb über geeignete, an Batterien angeschlossene Widerstandsnetze polarisiert werden. Der Pegel des Eingangssignals und der Polarisationsspannungen und -ströme ist für die Art des Transistorbetriebs ausschlaggebend.

Beim BJT-Transistor regelt der CONTR-Regelkreis die Polarisationsspannung V_{CE} zwischen den Kollektor- und Emitter-Endstellen in Entsprechung zu einer Regelfunktion V_{CE} (I_B), welche einen ähnlichen Verlauf wie die für den FET-Transistor definierte Funktion V_{DS} (V_{GS}) hat. Der Grundpolarisationsstrom IB wird primär durch das Oszillationssignal $v_i\cos(\omega_o t)$ erzeugt, das durch die obengenannte Verbindung gleichgerichtet wird.

Schließlich ist es möglich, den in der ABB. 1 gezeigten Kreis minimale zu verändern, in dem man einen mit L2 in Reihe geschalteten Widerstand einsetzt, dessen Wert, um die Wirkung des CONTR-Regelkreises zu sensitivieren, ähnlich zu dem des Kanalwiderstandes r_o sein muß. Im Falle des BJT-Transistors besteht die kostengünstigste und effektivste Lösung im Einsatz eines bereits benannten zusätzlichen Widerstandes, der mit dem Emitter in Reihe geschaltet werden muß. In beiden Fällen muß der CONTR-Regelkreis eine Regelspannung erzeugen, die gleich zur vorgenannten Regelspannung ist, zuzüglich eines konstanten Wertes zwecks Ermöglichung der Zirkulation des Gleichstromanteils i_D des Stroms $i_D(t)$ im zusätzlich eingesetzten Widerstand. Die Gesamtregelspannung kann erzielt werden über den zusätzlichen Einsatz eines geeigneten Voltspannungsteilers auf dem nichtumkehrenden Eingang von OP4 (ABB. 6).

INANSPRUCHNAHMEN

1. Der Radiofrequenzvervielfacher, der bestückt ist mit einen Transistor (T1), über den ein eingehende Oszillationssignal verstärkt und verzerrt wird, sowie mit einem Bandpaßfilter (FPB), über den eine im Ausgangsstrom des Transistors enthaltene Oberwelle einer vorher definierten Größenordnung N selektioniert werden kann, sowie weiterhin bestückt mit einem Regelkreis zur automatischen Pegelregelung (CONTR), welcher zwischen den Eingangsklemmen (G-S) und den Ausgangsklemmen (D-S) des besagten Transistors (T1) installiert wird und welcher die Leistung (P_{out}) der besagten, im Ausgang des Bandpaßfilters (FPB) präsenten Oberwellen einer vorher definierten Größenordnung N konstant hält; ist dadurch gekennzeichnet, daß im besagten Radiofrequenzvervielfacher Mittel installiert sind (T1, R_G, C1, L1), die eine Steuerspannung (V_{GS}) erzeugen, welche in direktem Bezug steht zum Leistungspegel (P_{in}) des eingehenden Oszillationssignals ($v_i\cos(\omega_o t)$), und daß zum besagten Regelkreis zur automatischen Pegelregelung (CONTR) Mittel zur Voltspannungs- und Stromerzeugung (OP1, OP2, OP3, OP4, D1, D2) gehören, die zur Polarisation des besagten Transistors (T1) dienen; diese Mittel werden durch die besagte Steuerspannung (V_{GS}) geregelt, so daß eine veränderbarer Polarisationsspannung (V_{DS}) erzeugt wird, welche zwischen den besagten Ausgangsklemmen (D-S) des besagten Transistors (T1) präsent ist und eingestellt ist auf eine umgekehrte Art zur Veränderung des Pegels der Steuerspannung (V_{GS}).

2. Radiofrequenzvervielfacher entsprechend dem unter Punkt 1) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß besagtes Oszillationssignal durch einen Hochbandpaßfilter (C1, R_G) zum Transistor (T1) geleitet wird, und dadurch gekennzeichnet, daß der Transistor (T1) das Oszillationssignal halbwellengleichrichtet, indem am Ausgang des besagten Hochbandpaßfilters (C1, R_G) eine Gleichstromkomponente erzeugt wird, welche mit der besagten Steuerspannung (V_{GS}) übereinstimmt.

3. Radiofrequenzvervielfacher entsprechend dem unter Punkt 1) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß der besagte Regelkreis zur automatischen Pegelregelung (CONTR) über entsprechende Verbindungen an besagten Transistor (T1) angeschlossen ist; zu diesen Verbindungen gehören:

- ein erster Induktor (L1) zur Verbindung des Ausgangs des besagten Hochbandpaßfilters (C1, R_G) mit den Eingang (1) des besagten Regelkreises (CONTR), so daß die besagte Steuerspannung (V_{GS}) den Durchlaß und die Sperrung des besagten Oszillationssignal ermöglicht;

- ein zweiter Induktor (L2), der mit dem Ausgang (2) des besagten Regelkreises (CONTR) in Reihe geschaltet ist und lediglich den Gleichstromanteil des Ausgangsstroms des besagten Transistors (T1) durchläßt.

4. Radiofrequenzvervielfacher entsprechend dem unter Punkt 1) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß zu den besagten, zum besagten Regelkreis (CONTR) gehörenden Mitteln folgende Geräte gehören:

- ein erstes Gerät (OP1), welches eine erste Voltspannung (V1) erzeugt, indem von einer anfänglich voreingestellten Voltspannung eine Voltspannung abgezogen wird, welche über Vervielfältigung des absoluten Wertes der besagten Steuerspannung (V_{GS}) mittels einer ersten Vervielfältigungskonstante erzielt wird;

- zweite Geräte (OP2, D1), welche zweite Voltspannungen (V2) erzeugen, indem der absolute Wert der besagten Steuerspannung (V_{GS}) mittels entsprechender zweiter Vervielfältigungskonstanten vervielfältigt wird und welche eine Null-Voltspannung erzeugen, bis daß der Wert der besagten Steuerspannung unter dem jedem zweiten Gerät zugeordneten Schwellenwert liegt;

- ein drittes Gerät (OP3, D2), welches eine Voltspannung erzeugt, die in Funktion zur Temperatur variiert, so daß die Veränderung der thermischen Leistung des Transistors (T1) ausgeglichen werden,

- ein viertes Gerät (OP4), welches die besagte Polarisationsspannung (V_{DS}) des Transistors (T1) erzeugt, in die vom ersten, zweiten und dritten Gerät erzeugten Spannungen summiert werden.

5. Radiofrequenzvervielfacher entsprechend dem unter Punkt 4) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß die besagten Schwellenwerte gegenseitig unterschiedlich sind, daß die besagte Vervielfältigungskonstante größer oder gleich ist als bzw. wie die breitere der besagten zweiten Vervielfältigungskonstanten sowie dadurch gekennzeichnet, daß die besagten zweiten Vervielfältigungskonstanten in umgekehrten Bezug zu den Schwellenwerten der entsprechenden zweiten Geräte sind.

6. Radiofrequenzvervielfacher entsprechend dem unter Punkt 4) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß:

- es sich bei besagtem ersten Gerät um einen ersten Operationsverstärker (OP1) und umkehrenden Spannungssummierer handelt, dessen Leistung der besagten ersten Vervielfältigungskonstante entspricht;
- es sich bei den besagtem zweiten Geräten um zweite Operationsverstärker (OP2) und nicht umkehrende Spannungssummierer handelt, die zum Ausgang jeweils in Reihe geschaltet sind mit einer Diode (D1), welche zur absoluten Regelung von Spannungswerte (V_{GS}) dient, welche größer sind als besagter Schwellenwert und innerhalb deren die Leistung der besagten zweiten Operationsverstärker (OP2) den besagten zweiten Vervielfältigungskonstanten entsprechen;
- es sich beim besagtem dritten Gerät um einen dritten Operationsverstärker (OP3) und umkehrenden Spannungssummierer handelt, über den die Anoden-/Kathodenspannung einer im Leitung befindlichen Diode (D2) verstärkt wird;
- es sich beim besagtem vierten Gerät um einen vierten Operationsverstärker (OP4) und nicht umkehrenden Spannungssummierer handelt.

7. Radiofrequenzvervielfacher entsprechend dem unter Punkt 6) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß der besagte vierte Operationsverstärker (OP4) den im Transistor (T1) zirkulierenden Maximalstrom begrenzt.

8. Radiofrequenzvervielfacher entsprechend dem unter Punkt 4) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß besagte voreingestellte Voltspannung der Speisespannung angenähert wird und daß die Anzahl der besagten zweiten Geräte (OP2, D1) gleich eins ist und daß der entsprechende besagte Schwellenwert etwa ein Drittel des Höchstwertes der besagten Steuerspannung (V_{GS}) entspricht.

9. Radiofrequenzvervielfacher entsprechend dem unter Punkt 1) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß es sich bei besagtem Transistor um einen MESFET Feldtransistor handelt, daß die Frequenz des Oszillationssignals im Mikrowellenbereich liegt und dadurch gekennzeichnet, daß der besagte Bandpaßfilter (FPB) den Durchgang der zweiten Oberwelle des Oszillationssignals ermöglicht.

10. Radiofrequenzvervielfacher entsprechend dem unter Punkt 1) oder 3) der Inanspruchnahme beschriebenen Gerät, dadurch gekennzeichnet, daß in Reihe geschaltet mit dem besagten zweiten Induktor (L2) ein Widerstand angeschlossen ist, dessen Wert annähernd gleich dem des Widerstandes zwischen den Ausgangsklemmen (D-S) des besagten Transistors (T1) ist.

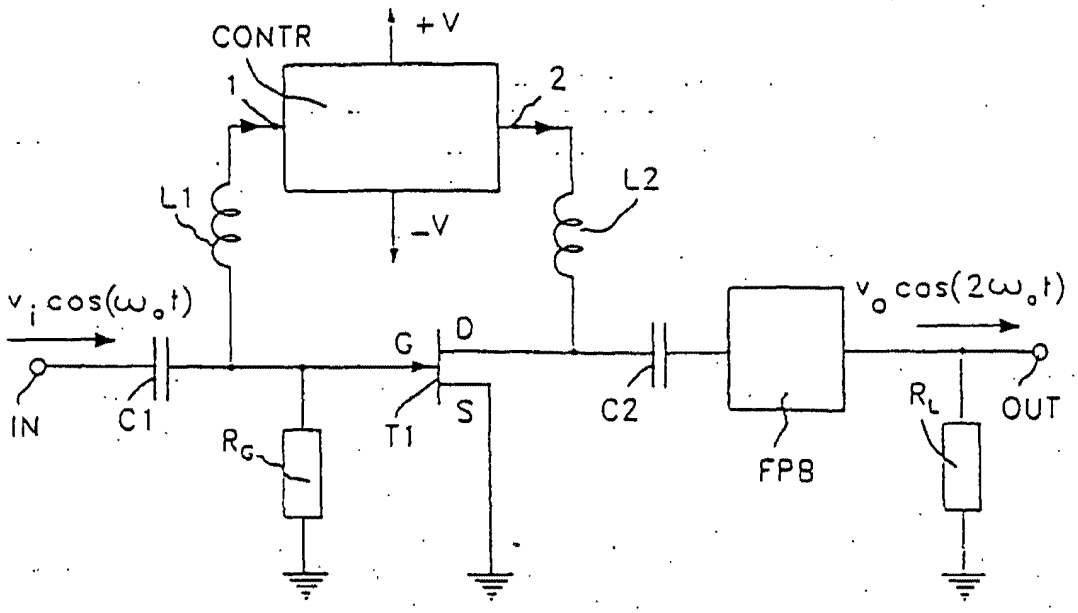

CONTR
+V
1
2
L1
L2
-V
$v_i \cos(\omega_o t)$
$v_o \cos(2\omega_o t)$
G
D
IN
C1
R_G
T1
S
C2
FPB
R_L
OUT

FIG. 1

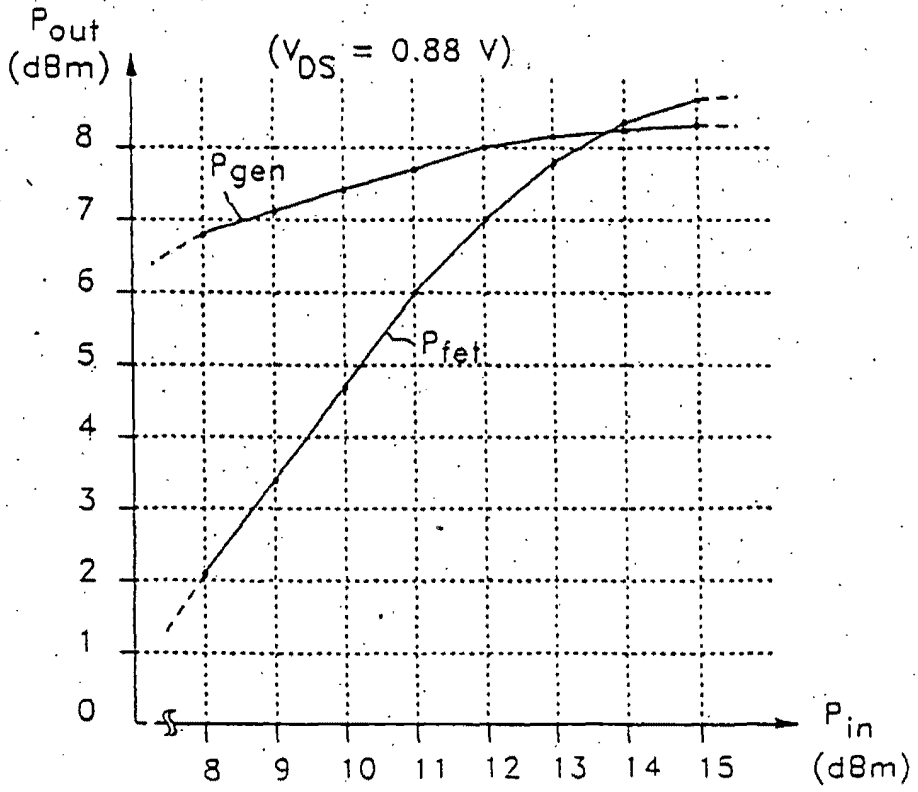

P_{out} (dBm)
(V_{DS} = 0.88 V)
P_{gen}
P_{fet}
P_{in} (dBm)
0
1
2
3
4
5
6
7
8
8
9
10
11
12
13
14
15

FIG. 2

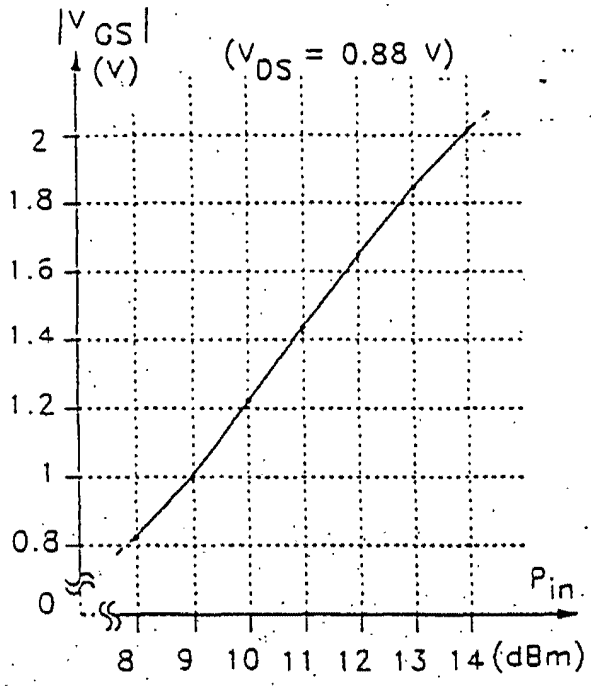


FIG. 3

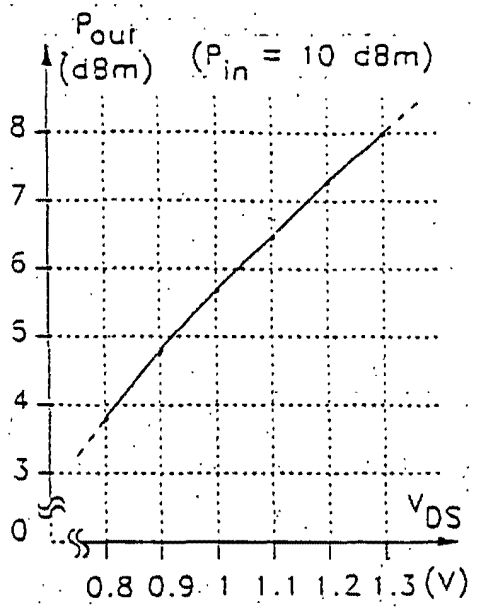


FIG. 4

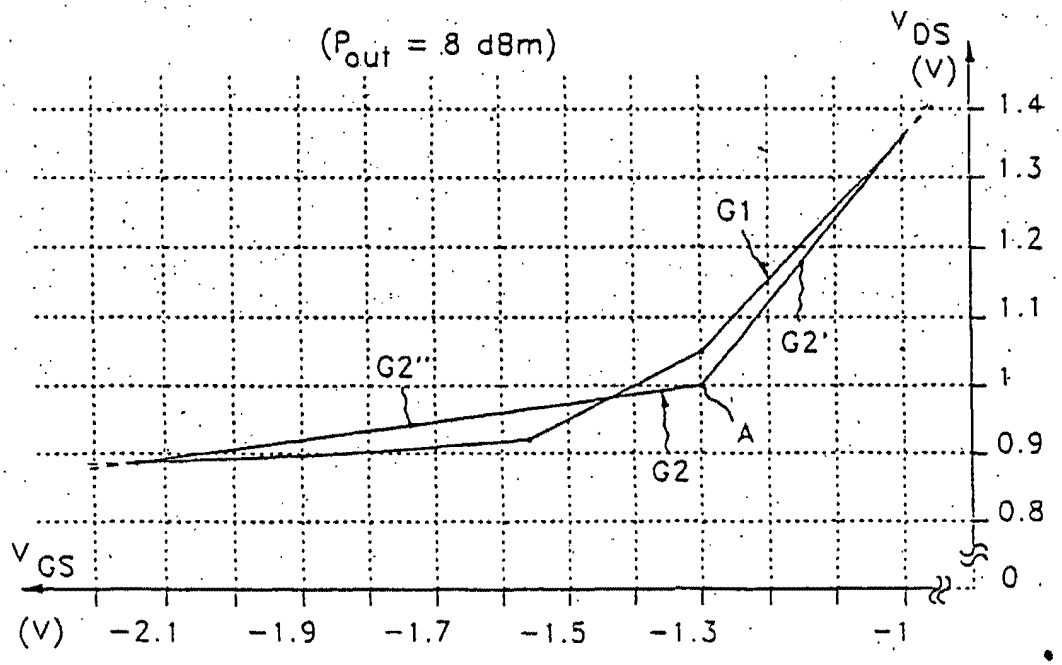


FIG. 5

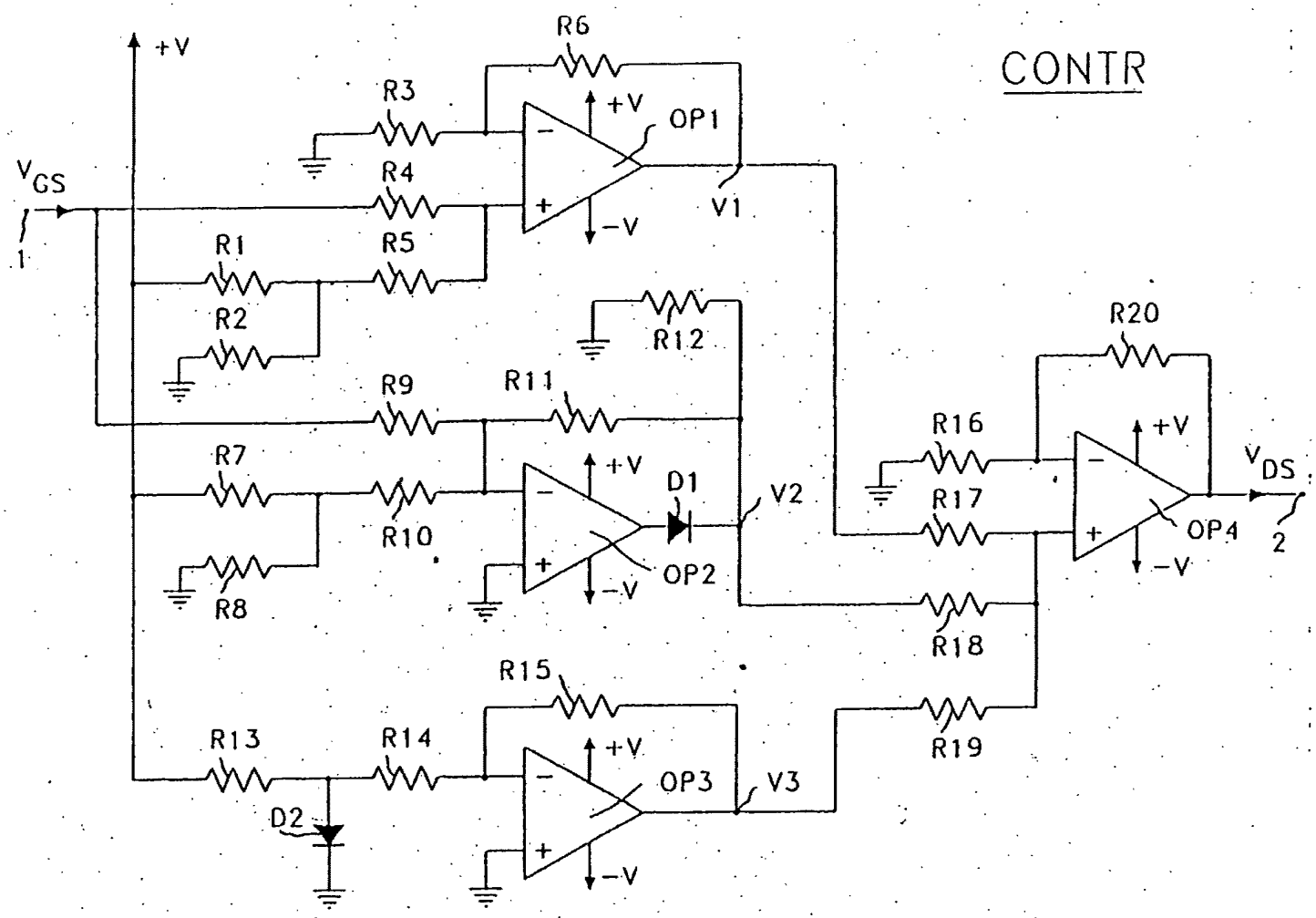


FIG. 6

CONTR

24

Radiofrequency frequency multiplier comprising an automatic level control cicuit

Patent number: DE69221098T
Publication date: 1998-01-15
Inventor: PILONI MARCO (IT); BRAMBILLA MASSIMO (IT)
Applicant: ITALTEL SPA (IT)
Classification:
- International: H03B19/14; H03G3/30
- european: H03B19/14; H03G3/30D2
Application number: DE19926021098T 19921119
Priority number(s): IT1991MI03168 19911127

Also published as:
EP0548542 (A1)
EP0548542 (B1)

Report a data error here

Abstract not available for DE69221098T
Abstract of corresponding document: **EP0548542**

Radiofrequency frequency multiplier comprising an automatic level control circuit consisting of a microwave MESFET (TI) used as an oscillator signal distorter amplifier followed by a band-pass filter (FPB) tuned to the desired harmonic. The power of the harmonic is stabilized by means of a control circuit (CONTR) placed between the gate (G) and drain (D) terminals of the MESFET. Said control circuit operates as a feedforward controller varying the polarization voltage VDS of the MESFET with the variation in the power level of the oscillator signal in accordance with a law which holds constant the power transferred from the MESFET to the selected output harmonic.

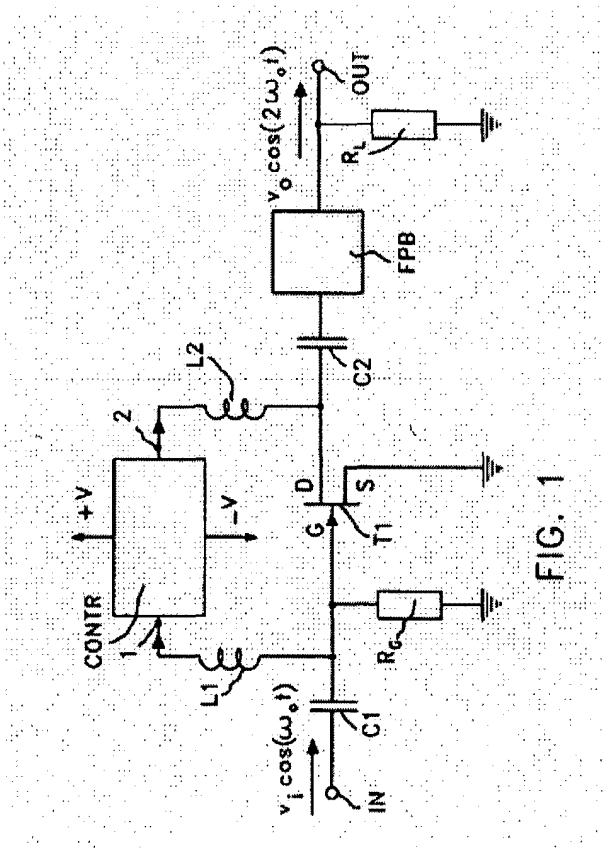


FIG. 1

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•Admitted only in Virginia
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March 28, 2006

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2616

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Second Supplemental Information Disclosure Statement;

2. A listing of the cited documents on Form PTO-1449 (*4 pages*);

3. Copies of the cited documents (AJ24-AM24, AJ25-AL25, AO60-AR60, AN61-AP61); and

4. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL:apg
Enclosures

512499_1.DOC



THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2616
Appl. No.: 10/973,917	Examiner: Chin, Wellington
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Second Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Second Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Supplemental Information Disclosure Statement filed on October 24, 2005 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Document AJ24 was cited in a search report in related European Patent Application No. 04020115.4, filed October 6, 2000, entitled "Down Converter Using Subsampling," directed to related subject matter. Also cited in said search report were U.S. Patent Nos. 5,454,007; 5,705,949; and 5,883,548, PCT Publication Nos. WO 94/05087 and WO 98/40968, German Patent Nos. DE 35 41 031 A and DE 197 35 798 C, and Fest, Jean-Pierre, "Le Convertisseur A/N Revolutionne Le Recepteur Radio," Electronique, JMJ (Publisher), No. 54, pp. 40-42 (December 1995), which have already been cited in the present application.

Documents AK24 and AE71 were cited in an Office Action in related European Patent Application No. 01977965.1, filed May 16, 2001, entitled "Apparatus, System, and Method for Down converting and Up converting Electromagnetic Signals," directed to related subject matter. Also cited in said search report were U.S. Patent Nos. 5,564,097 and 5,640,698; PCT Publication No. WO 96/02977; and Rudell, J.C. *et al.*, "A 1.9-Ghz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," IEEE Journal of Solid-State Circuits, IEEE, Vol. 32, No. 12, pp. 2071-2088 (December 1997), which have already been cited in the present application.

Documents AL24, AM24, AJ25-AL25, and AF71 were cited in an Office Action in related Israel Patent Application No. 142,699, filed October 18, 1999, entitled "Method and System for Frequency Up-Conversion,", directed to related subject matter. Also cited in said Office Action was European Patent Publication No. EP 0 548 542, which has already been cited in the present application.

Documents AO60 and AD71 were cited in an Office Action in related U.S. Patent Application No. 10/197,253, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter.

Documents AE69-AI69 were cited in an Office Action in related U.S. Patent Application No. 10/197,255, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,850,742, which has already been cited in the present application.

Documents AA70, AA71, and AG71-AI71 are co-owned patents which are directed to related subject matter.

Documents AB70 and AC70 were cited in an Office Action in related U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Methods And Apparatuses Relating To A Universal Platform Module And Enabled By Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,844,868, which has already been cited in the present application.

Documents AD70-AI70 were cited in a Notice of Allowance in related U.S. Patent Application No. 10/961,272, filed October 12, 2004, entitled "Apparatus, System, And Method For Down-Converting And Up-Converting Electromagnetic Signals," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,853,690, which has already been cited in the present application.

Documents AB71 and AC71 were cited in an Office Action in related U.S. Patent Application No. 09/550,644, filed April 14, 2000, entitled "Method And System For Down-

Converting An Electromagnetic Signal, Transforms For Same, And Aperture Relationships," directed to related subject matter.

Documents AA72 and AB72 were cited in an Office Action in related U.S. Patent Application No. 10/394,069, filed March 24, 2003, entitled "Method and Circuit for Down-Converting a Signal," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,836,650, which has already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final

Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document AK24 (DE 1936252) appears to describe a modulator or demodulator in integrated technology. An English language translation of document AK24 is enclosed as document AP60.

Document AL24 (JP 62-12381) appears to describe a pulse-width modulation control system of an inverter. An English language abstract of document AL24 is enclosed as document AQ60.

Document AM24 (JP 4-154227) appears to describe a relay monitoring device for broadcasting radio waves. An English language abstract of document AM24 is enclosed as document AR60.

Document AJ25 (JP 6-284038) appears to describe a transceiver. An English language abstract of document AJ25 is enclosed as document AN61.

Document AK25 (JP 10-96778) appears to describe a distance measuring device. An English language abstract of document AK25 is enclosed as document AO61.

Document AL25 (JP 11-98205) appears to describe a demodulator for digital radio communication. An English language abstract of document AL25 is enclosed as document AP61.

☒ 7. Copies of documents AJ24-AM24, AJ25-AL25, AO60-AR60, and AN61-AP61 are enclosed. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent publications cited on the attached Form PTO-1449 are not enclosed.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000, 09/476,093, filed January 3, 2000, 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 3/28/06

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(202) 371-2600

511368_1.DOC

Atty. Docket: 1744.0330003

OIPE IAP13
MAR 28 2006
PATENT & TRADEMARK OFFICE

FORM PTO-1449

SECOND SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE69	5,703,584	12/1997	Hill			
	AF69	5,887,001	03/1999	Russell			
	AG69	6,298,065 B1	10/2001	Dombkowski *et al.*			
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FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
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U.S. PATENT DOCUMENTS

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AL						Yes No
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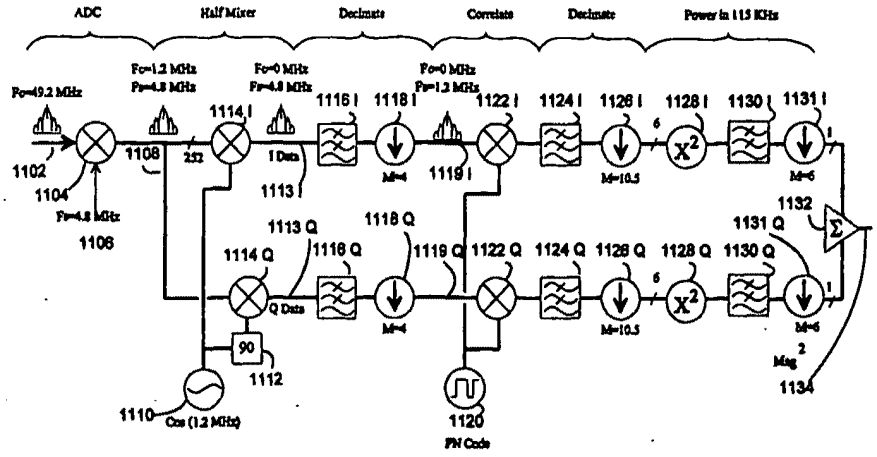
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(54) Title: DIRECT SEQUENCE SPREAD SPECTRUM METHOD, COMPUTER-BASED PRODUCT, APPARATUS AND SYSTEM TOLERANT TO FREQUENCY REFERENCE OFFSET



(57) Abstract

A system employs a digital receiver (or transceiver) to receive, digitize and process a direct sequence spread spectrum signal using digital signal processing components. A radio front end portion of the receiver receives and digitizes the signal, and a digital signal processing portion downconverts and despreads the signal by applying a pseudorandom noise (PN) code, used at a transmitter to spread a data signal contained in the direct sequence spread spectrum signal, to the received signal. A timing and state control mechanism is included to provide time reference correction information to the signal processing components of the receiver for alignment of the PN code with the direct sequence spread spectrum signal, allowing the receiver to be compatible with transmitters using inaccurate frequency references which impart a significant frequency ambiguity in the received signal. Computer-based synchronization methods and mechanisms suitable for use for low performance digital signal processors, and power management mechanisms are employed to enable long-term operations using battery power, enabling utilization in network settings.

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TITLE OF THE INVENTION

DIRECT SEQUENCE SPREAD SPECTRUM METHOD, COMPUTER-BASED PRODUCT, APPARATUS AND SYSTEM TOLERANT TO FREQUENCY REFERENCE OFFSET

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention is directed to communications-related systems, networks apparatuses and methods as well as computer-based digital signal processing mechanisms and methods used therein. More particularly, the invention is directed to the field of direct sequence spread spectrum (DSSS) communication that employ a DSSS transmitter and a DSSS receiver, or transceiver configured to convey a data signal in a transmitted DSSS signal by spreading the data signal on transmission and correlating on reception so as to "despread" the DSSS signal and recover the data signal.

Discussion of the Background

Conventional narrowband (i.e., non-spread spectrum) radio communication devices transmit signals in frequency bandwidths that are roughly equivalent to a data signal bandwidth (or information bandwidth). These devices typically use a radio-frequency (RF) carrier derived from a frequency reference (i.e., a device that produce a precise frequency, although the accuracy of the frequency usually depends on the cost of the device) and modulate the data on the RF carrier. Common conventional data modulation methods such as frequency modulation (FM), phase modulation or amplitude modulation (AM) cause the RF carrier to occupy slightly larger bandwidth then the RF carrier alone, but the total bandwidth for the RF carrier and data is not much larger. As such, interference signals (e.g. jammers) that are transmitted in the same bandwidth as the RF carrier and data can effectively "jam" the signal and prevent a receiver from reproducing the data signal. Aside from jamming, disturbances in the communications path between the transmitter and receiver can interfere with reception. For example, fading due to multipath or atmospheric obstruction can attenuate the signal significantly. Also, shadowing becomes significant if the signal must pass through solid matter such as buildings, walls, floors or trees and vegetation.

Spread spectrum radio communication addresses the shortcomings of narrowband communications by mixing (i.e. applying) a wideband spreading signal to the data signal so as the "spread" the data signal. In these types of systems, the transmitter also modulates a RF carrier with data, as with the narrowband systems, but then adds one more modulation step by modulating the signal with a wideband, noise-like signal (e.g. a PN code). Consequently, the data signal is spread in frequency over a much larger bandwidth, typically several million Hertz (MHZ). Common spread spectrum techniques include frequency hopping and DSSS. Frequency hopping systems move (i.e., "hop") the data modulated carrier to frequencies following a pseudo-random pattern defined by the PN code. DSSS mix a PN code with the

data modulated carrier to create a DSSS signal which simultaneously occupies roughly the bandwidth of the pseudo noise signal.

Narrowband interference signals transmitted at same frequency as a portion of the spread signal, "jam" the spread signal by an amount proportional to the ratio of jammer bandwidth to pseudo-noise bandwidth. At a minimum, the interference signal will at least be attenuated by a "processing gain" of the spread spectrum signal, where processing gain is defined as a ratio of data signal bandwidth to spread signal bandwidth. For similar reasons, spread spectrum signals also offer some degree of immunity to channel fading and multipath loss.

DSSS systems have been used in the past to achieve low probability of intercept (LPI) for secure communication and thus are valuable in military applications or other scenarios requiring covert communications. DSSS is also used in places where multipath or fading is prevalent, such as satellite communication. For example, Global Positioning System (GPS) operates using DSSS techniques. However, as recognized by the present inventors, conventional DSSS systems are expensive (considering the transmitter and receiver) because relatively high performance frequency references and digital signal processing equipment is used. Accordingly, DSSS techniques are most commonly used in military and high-end consumer market, where component cost is less of a factor than with low-end consumer product.

Conventional direct sequence spread spectrum transceivers are directed towards high-end systems (e.g. systems costing in the hundreds or thousands of dollars in 1997) that require advanced, if not state-of-the-art, digital signal processing equipment, and associated components. Past DSSS systems have avoided using lower cost components because conventional wisdom dictates that selectively high fidelity frequency references are required at the transmitter and receiver, as well as powerful digital signal processing equipment so to compensate for even minor frequency deviations between transmitter and receiver systems. Contrary to conventional DSSS design practice, the present inventors have identified that these conventional DSSS devices are not applicable for low-end, inexpensive, commercial use applicable for high-volume sale, nor are they well suited for small packages, that may be used in a variety of non-standard field uses, such as, for example, home security and fire systems, data telemetry, access control, remote meter reading as well as other applications.

As recognized by the present inventors, one factor that drives the cost of conventional systems is the use of lengthy PN codes that require substantial digital signal processing to be despread in a receiver. While there are many advantages to using a long code (such as with code division multiple access, CDMA, telephony which permits many users to transmit on a common channel at the same time) the present inventors have recognized that a shorter code, such as a 63 bit PN code, may enable the use of components applicable for lower cost applications.

Figure 1 is a block diagram of a conventional receive system that of either a conventional receiver (either narrowband or DSSS receiver). The receive system includes a RF front end section 120, a first local oscillator (109, 112, 111, and 110, as will be discussed) section, an analog-to-digital conversion section 121, baseband mixing section (115, as will be discussed) and a baseband processing section 122, as shown. The details of the conventional receiver are described below, following a general overview description. The RF section 120 performs the function of converting electromagnetic wave energy (including the transmitted signal) and outputting an analog signal. The analog signal is maintained within a predetermined signal level range, as controlled by an automatic gain control circuit (AGC) as shown. The output from the RF front end is provided to a first local oscillator section having a mixer 109, which translates the analog signal to a lower frequency by using a precise, and generally expensive, voltage controlled oscillator 110. By employing the precise voltage controlled oscillator 110, the position of the translated signal (i.e., a down converted signal), is controlled to within a narrow predetermined frequency range.

The downconverted signal is then passed to the intermediate frequency processing section 121, that adds appropriate gain prior to a digitalization process while filtering out-of-band images necessary for the digitization process, as will be discussed herein. The output of the intermediate frequency section is passed to the analog to digital converter ADC shown as mixer 115 (as will be discussed), which converts the analog signal into a digital representation for subsequent processing in the baseband section 122.

In this conventional architecture, the analog AGC's function is to keep the signal level applied to the ADC 115 within an operational range of the ADC. Once digitized, the signal is passed to the baseband section 122, where digital signal processing operations are performed on the signal and the signal is detected and demodulated, resulting in outputting the data signal originally transmitted from the transmitter (either in a spread or non-spread form).

In the special case of direct sequence spread spectrum receivers, the burden of performing the "inverse spreading" (despreading) operation on the signal usually falls on the digital signal processor 116 section 1 of the baseband processing section 122. In some cases, the despreading code is mixed in the RF front end 120, first LO or intermediate frequency (IF) sections of the receiver, but such analog architectures require significantly precise components or specialized compensation mechanisms. Accordingly, conventional direct sequence spread spectrum receivers, require high performance digital signal processors or complicated analog sections in order to perform the despreading and correlation functions, as well as signal acquisition and demodulation processes. As a corollary, a precise frequency reference at the DSSS transmitter is assumed to be present so little to no frequency ambiguity is presented into the signal received by the receiver.

Conventional digital receiver design wisdom is such that the loss in performance associated with using low cost, low power desirable and possible components does not justify their use in light of the fact that slightly more expensive components provide greater precision and processing power and therefore avoid performance problems associated with low-cost, inaccurate components. As identified by the present inventors, the high performance digital signal processors, as well as high fidelity voltage controlled oscillators, are not conducive to low cost, low power applications, and that with proper compensation mechanisms, the adverse effects of low cost components can be justified.

More particularly, Figure 1 depicts RF downconversion and signal conditioning components used to prepare a received analog signal for sampling. Antenna 101 receives the RF signal sent from a transmitter and passes the signal through RF diversity switch 102 and on to a bandpass filter (BPF) 103. Alternatively, a controllable select mechanism 104 may select antenna 105 to receive the RF signal. The antennas may be physically separated and/or of different polarizations so as to enable spatial or polarization diversity reception. The BPF 103 rejects undesired frequencies prior to signal amplification by an amplifier 106. The RF signal is then filtered by BPF 107 and amplified by another amplifier 108 prior to downconversion in a mixer 109. The frequency of the downconversion tone applied to the mixer 109 is controlled by a voltage controlled oscillator (VCO) 110. The output of the VCO 110 is filtered by a BPF 111 and amplified by an amplifier 112.

After downconversion, the downconverted signal is positioned at an intermediate frequency (IF) determined by the downconversion tone applied to the mixer 109, and additional gain is provided by an amplifier 113. A BPF 114 serves as an anti-aliasing filter prior to a second downconversion operation that, as recognized by the present inventors, may be performed with the sampling ADC 115. After the second downconversion operation, the signal is positioned near baseband (i.e. near 0 Hz).

The digital signal processor (DSP) 116 performs various operations including despreading the signal if it is a spread spectrum signal and then sends the baseband signal to a demodulation block 117 so as to extract the data originally added to the transmitted signal by the transmitter. Frequency control of the DSP 116 is provided by an oscillator 118 and using the DSP 116 passes the frequency control to all relevant sections 110, 115 and 117 to compensate for mismatch in received signal frequency, and/or chip phase, though frequency mismatch is usually minimized by using accurate frequency references at the transmitter and receiver. While Figure 1 depicts a single RF downconversion step, other downconversion steps may be added to properly center the received signal at the desired ADC IF frequency.

Countering Channel Disturbances

Conventional receivers, and transceivers (which are receivers that also include a transmitter), employ various types of diversity transmission and reception features so as to overcome disturbances in the communications channel (such as signal loss due to blockage by trees, buildings and other obstructions,

for example, in a cellular telephone application). Various types of diversity techniques include frequency diversity, time diversity, spatial diversity and code diversity such as that employed in code division multiple access (CDMA). Diversity reception techniques, conventionally require some information being provided by the baseband digital signal processing section, so as to determine how to optimally employ the diversity features of the system. For example, in the conventional system of Figure 1, two antennas, 101 and 105, may be controlled by an antenna select line, that connects with the baseband processing section 122, as shown. The decision process for which the antenna to select, will draw additional processing resources from the digital signal processor 116, thereby further establishing a need for digital signal processor resources with substantial processing power.

The present inventors have identified that a need exists for integrating diversity reception techniques for receiving DSSS signals having relatively low signal processing gain in low-end products with minimal signal processing resources.

Techniques For Digitizing RF and IF Signals

Figures 2 and 3 show respective frequency plots of a signal of interest, before and after, respectively, being passed through a harmonic sampling operation, a technique that may be used to reduce signal processing complexity in digital receivers. One special case of harmonic sampling is shown in Figures 4 and 5, where the harmonic sampling is performed using a "real", not complex or quadrature, harmonic sampling approach, as will be discussed.

Harmonic Sampling

Harmonic sampling (also known as undersampling, bandpass sampling or Super-Nyquist sampling) is a technique that may be used to translate a signal at an RF or intermediate frequency (IF) to a resulting frequency near or at baseband.

Figures 2 and 3 illustrate an example scenario where the sampling rate for the ADC is between 0 Hz (labeled as 204) and the maximum analog input frequency 214. (These specific frequencies are used to simplify the later discussion with respect to these present invention and should not be construed as a specific implementation of a prior art device). The signal of interest 210 exists at an IF frequency 212 of 10.8 MHZ, and the sample rate of the converter 206, as recognized by the present inventors and as will be discussed in the context of one of the preferred embodiments, is an integer multiple such as 4 times the chipping rate (i.e., a rate at which chip of the PN sequence are produced). In the conventional oversampled application, with a sample rate (Fs) any signal that exists between 0 Hertz (Hz) 204 and Fs/2 205 (i.e., the Nyquist bandwidth) is digitized and represented untranslated following digitization. Thus, making it necessary to use an anti-alias lowpass filter to attenuate frequencies above the Nyquist frequency 205. However in harmonic (undersampled) applications such as that depicted in Figure 2, the anti-alias filter

is a bandpass filter (208). The purpose of the filter remains unchanged, as all frequencies except the signal of interest must be attenuated to a point of insignificance.

The sampling device operates as a discrete component whose sample event is set by a clock edge. The signal is tracked until the sample edge occurs, and is then immediately held. In an ideal sampling device, this track and hold system operates on an infinitesimally small time window (a clock edge). This time domain operation is an impulse function and can be expressed as a series of fundamental frequencies (tones) in the frequency domain separated by the frequency of the sampling clock. Each of these tones is equal in magnitude and extend to infinity. For sampling applications, these tones act as harmonics in an ideal mixer and the input signal is mixed against these harmonics, creating repetitive images in the digitized spectrum.

Care must be taken to ensure that the relative frequency of the IF with respect to the harmonic tones do not create overlapped images, because the overlapping will degrade the dynamic range of the system. The optimal frequency separation for the IF with respect to any given tone is one-fourth the sampling frequency because this translates the signal and all images to the center of the Nyquist bandwidth. Accordingly, frequency error inherent in the system is therefore afforded the greatest guardband and usable dynamic range is maximized.

Figure 3 depicts the resultant digitized spectrum after the signal is sampled at Fs = 4.8 MHZ and demonstrates a zero guardband system where the signal of interest occupies the entire Nyquist bandwidth 316 for a given sample rate. The resulting images 318, 319, 320, 321, 322, and 323 are separated every Fs/2 in frequency. Ideal IF center frequencies (F_c) will therefore exist at multiples of the sample rate ± ¼ of the sample rate. The following equation may be used to select ideal IF frequencies for a given Fs.

$$IF = Fs(N \pm ¼),$$

where N is an integer harmonic sampling multiplicand. For the example depicted in Figure 2, N = 2 and "+¼"is selected. Whenever the "-¼"option is selected, the downconverted image is "high side injected" and will be spectrally flipped (high frequencies at 0, and 0 at Fs/2). The actual IF frequency can exist at any harmonic of the sample rate. Although, practical limitations should be observed because the input frequency range 202 is limited primarily due to the limitations in the track and hold operator to adequately follow the signal without introducing distortion. Any slew limiting or overshoot will introduce noise into the system, which is true for limiting single-bit digitizers as well as multi-bit digitizers.

The effect of aperture jitter contributes to phase noise in the digitized signal, where aperture jitter is defined as a time difference present in a decision threshold for realizable sampling components. Assuming the sample clock has zero phase noise (which seldom is true), the sampling component will observe the clock edge with some degree of time error based on the voltage comparison window of edge recognition. The error is often only a few picoseconds; yet, it is quantifiable and contributes negatively as

phase noise. As recognized by the present inventors, because the signal of interest is placed at higher IF frequencies, and therefore higher harmonic frequencies, the aperture jitter increases proportional to the harmonic multiplicand.

Real-only Sampling

A way to achieve lower computational loading is to process the sampled data as real-only, thus discarding the quadrature processing altogether. Figures 4 and 5 depict a signal IF spectrum prior to sampling and after real-only sampling. In Figure 4, the analog input range 402 for the ADC is between 0 Hz and the maximum analog input frequency 414. The signal of interest 410 exists at an IF frequency 412 of 10.8 MHZ. As previously discussed, the presently described frequencies were identified by the present inventor and presented in the prior context only for the purposes of explaining real-only sampling. The sample rate 406 is shown to be 4 times the chipping rate, and the anti-alias lowpass filter 408 attenuates undesired frequencies. The downsampled, digitized spectrum exists at 0 Hz, 519 (i.e., baseband), and present in the Nyquist bandwidth 516 are two copies of the same spectrum flipped about 0 Hz. All of the signal information is available now in the previous bandwidth of interest, but, 3 dB off orthogonal transmitter loss is present resulting in degraded performance. Repetitive images of the signal exist throughout the frequency spectrum and are depicted as items 518, and 520 through 522.

Techniques for Processing Digital Signals Having High Sample Rates

A challenge with modern digital receivers is identifying how to convert radio frequency energy into digitized samples which occur at extremely high sampling rates (in most applications well over 1 MHZ) and providing enough digital signal processing power to process in real time the samples provided from the analog to digital converter. A technique that has been used to lower the sample rate of digital signals is to low pass filter the digital signal samples, followed by decimating in time the respective samples. Decimation in time is a process in which a set of adjacent samples are combined into a lesser number of samples so as to produce a lower sample rate. This lesser number of samples is then more easily handled by digital signal processors. Accordingly, decimation reduces signal processing demands in digital receivers by lowering sample rate. For a general discussion of decimation and sample rate reduction techniques, see Frerking, M, "Digital Signal Processing and Communication Systems", Van Nostrand Reinhold, 1994, the contents of which is incorporated herein by reference, in particular pp 65-66, 193-199. Nonetheless, while decimation is an approach for reducing sample rate, conventional wisdom suggests that performance in digital receivers requires high performance digital signal processors that can operate at very fast clock rates. In contrast, the present inventors have identified that the combination of decimation, downconversion, and judicial use of harmonic sampling, contributes to enabling the use of lower-end digital signal processor that performs adequately even when receiving a signal from a transmitter having an inaccurate frequency reference.

Setting Detection Bandwidth

Receive systems typically contain cascaded filters to band-limit the received signal prior to detection. The final filter prior to detection sets the predetection bandwidth of the system. Typically, this predetection bandwidth is as narrow as possible so as to maximize receiver sensitivity. The wider the filter, the more noise energy is present in the signal detection process. Typical direct sequence systems set this final predetection bandwidth to be equal to the desired signal of interest, thus maximizing the receive sensitivity.

As recognized by the present inventors, the conventional approach is only possible if the transmitter and receiver are perfectly aligned in frequency, either by tightly controlling the transmitter and receiver frequency references or by using a frequency acquisition and control loop to adjust the receiver reference to match the transmitter's reference. Both approaches are expensive in component cost and/or complexity. Poor frequency stability in transmitters and/or receivers may be accommodated by widening the receiver predetection bandwidth to compensate for frequency error in the data link, but at increased noise power and lower system performance.

Figure 6 depicts a probability distribution function for noise versus signal plus noise in two predetection bandwidths. For conventional systems having a bandwidth of 20 kHz, distribution 605 depicts the probability distribution function of noise. In contrast to conventional systems, Applicants have identified a need for receivers with a much wider detection bandwidth (115 KHz, versus 20 KHz) so as to capture the transmitted signal with a 115 kHz transmitter uncertainty bandwidth. The distribution for a bandwidth of 115 KHz is shown as the element labeled 610.

Distributions 630 and 625 are for a keyed, or "ON" signal of -110 dBm as detected in a 115 kHz and 20 kHz predetection bandwidth respectively. As depicted, the signal to noise ratio (SNR) is greater for predetection bandwidth of 20 kHz (640) than for 115 kHz (645). SNR is measured as the difference in mean power for noise 615, 620 and signal 635. Consequently, the present inventors have identified that a performance penalty is to be paid in the form of decreased SNR if low-cost, inaccurate frequency references are used for transmitting and receiving a signal.

Figure 6 further demonstrates that the wider predetection bandwidth of 115 KHz incurs a sensitivity loss relative to a narrower predetection bandwidth. As the predetection bandwidth is allowed to grow wider, the noise distribution function approaches the signal distribution function actually overlapping it and inducing errors on detection which corresponds to a reduction in sensitivity. Accordingly, the present inventors have identified that when constructing a system, a balance must be struck between the predetection bandwidth and frequency error budget accounting for reasonable performance degradation as well

Code Chip Coarse Synchronization

Direct sequence transmission systems require that the receiver and the transmitter have aligned pseudorandom codes in order to properly despread the received signal. The receiver has the burden of aligning the receiver pseudorandom code with a transmitter pseudorandom code in order to properly despread the signal.

Direct sequence receivers must correlate the received signal in order to recover data. The correlation process can be described as either a serial or parallel process. Prior art has typically performed low cost correlation in a serial process wherein multiple bit intervals (or multiple code repetition intervals) of received data are used against successive relative chip phases of the receiver PN code to correlate data. High cost, high end systems typically achieve correlation much faster using a technique called parallel correlation. System which use parallel correlation use one or a few code periods of data to correlate against many phases of the PN code in parallel to produce a correlation function over one or a few code periods of data.

The present inventors have recognized that with either the slow serial search or the parallel search, the RF front end must remain active in order to continuously receive the signal, and thus, cannot be turned off during the computation of the correlation function, so as to conserve battery power.

For conventional systems that use a slow serial search, the burden is put on the transmitter to transmit a long preamble which allows the receiver to sequence through all possible combinations of the PN code for acquisition. Prior systems that use slow serial searches therefore require transmitters to transmit long preambles, shortening battery life and increasing power requirements. The present inventors have identified a need for a fast serial search method that would enable transmitters to optionally shorten their preamble period, and conserve battery power.

Conventional systems have been fielded with 92 code period preambles (i.e., preambles that repeat the entire code 92 times) so as to enable slow serial search receivers to acquire the 63 chip phases (63 candidate chip phases requiring a separate code period) with remaining code periods required for fine search and antenna diversity. The present inventors have realized that there is a need for new receivers that are backwards compatible with the existing transmitters that transmit 92 code periods in a preamble but can make better use of the long preamble, perhaps to employ additional diversity techniques to improve signal detection and demodulation, as well as reduce receive power.

Fine Synchronization (Fine Sync)

For direct sequence receivers, a fine sync process , sometimes called a fine search process, further reduces correlation error following the coarse synchronization process (course sync, or coarse search process). The coarse sync process terminates when a correlation result surpasses a predetermined threshold (i.e., a trip condition) indicating that the received signal is aligned to within +/- ½ of a code chip interval

of the PN code. Ideally, however, the signal and the PN code should be perfectly aligned to provide optimum performance. So as to more closely align the signal with the PN sequence, a fine sync process is initiated after the coarse sync process so as to further reduce the relative chip interval between the received signal and the receiver PN code.

Figure 7 illustrates results observed in an ideal receiver when attempting to align the PN code to the received signal through successive 1/4 chip fractional chips steps as part of a fine sync process. The circles in Figure 7 represent respective powers (i.e., correlation results) received from the fine sync correlation process for relative 1/4 chip fractional offsets of a signal, absent noise, and the PN code. A perfect correlation yields the maximum process gain at zero chip phase error, as shown by the center circle. For a PN code of length 63, which the inventors have recognized is relevant to one PN code for the present invention, the maximum process gain is 18 dB. Also, chip errors that are greater than 1 chip width result in the loss of all system process gain, such that the received signal cannot be detected or demodulated.

Conventional systems typically use either a slow fine serial search process, parallel fine search process or code tracking loops to compute the correlation function for fine sync. Slow fine serial search systems typically require one code period of data per fractional chip step to compute the correlation power, followed by a process for determining the maximum correlation from those data samples. As depicted in Figure 7, computation for each of those correlation powers will require 9 code periods to compute the correlation peak (i.e., ± 1, $\pm 3/4$, $\pm 1/2$, $\pm 1/4$, and 0). Alternatively, conventional systems may employ parallel processes where 1 code period of data is applied to 9 different correlators, arranged in parallel, each with a distinct fractional PN code offset, so as to compute the correlation peak simultaneously. The present inventors have recognized that the slow serial process requires more time to compute than the fast parallel process, but requires less computational processing power.

Fine search processes are used to initially acquire the spread spectrum signal and at predetermined time intervals through the data message in order to maintain correlation alignment. The term "reposition" or "repo" is a term used in spread spectrum systems, such as in transceiver systems designed by Axonn, to reposition the PN code and received signal while receiving a data message portion of the received signal.

Drift Offset Between Transmit and Receive Frequency References

Typical direct sequence spread spectrum systems require very stable local frequency references for transmit and receive operations in order to maintain near coherent (i.e., in phase) operation. Ideally, transmitters and receivers will operate using a common frequency reference in order to maintain correlation throughout the data message. An example of such a direct sequence system is the Global Positioning Satellite (GPS) system, which requires very accurate frequency references, typically Cesium based or other atomic standards. These precise, expensive frequency references provide adequate timing accuracy to virtually eliminate frequency and code phase drift between the received signal, as sent from the transmitter,

and the downconversion tones and PN code generated in the receiver. Additionally, the receiver must employ complex digital signal processing in order to resolve time difference of arrival between multiple direct sequence signals in order to derive a stable local time reference for use. The direct sequence receiver must, therefore, measure and track frequency errors and code phase errors for transmitters in order to maintain reliable data communications.

As recognized by the present inventors, conventional direct sequence spread spectrum systems have opted to virtually eliminate by frequency and code phase drift problems by employing reasonably accurate frequency references at the transmitters and receivers. However, accurate frequency references are expensive for low-end commercial applications and draw more power than desired for battery powered applications (often because the frequency references will add heaters and other current drawing devices to help stabilize the reference). Related to this observation, the present inventors recognized that, frequency drift attributable to the transmitters frequency reference, a carrier frequency error will correspond to a related chipping rate error present in the PN code generator because the inaccurate frequency reference taints both the carrier frequency and the chip phase. Based on this observation, it is feasible that the receiver may employ methods to measure the frequency error and predict the code phase error.

Provided that search and trip are successful (i.e., the signal and PN code are aligned), frequency offset between the transmitter and the receiver may be measured to determine the magnitude and direction of the frequency uncertainty. Frequency and /or phase detectors, as will be discussed, may be used to determine the magnitude and direction of the frequency uncertainty. Once a frequency error is determined, a local oscillator (LO) downconversion tone is changed to compensate for the frequency error. This method is the classic Automatic Frequency Control (AFC) loop. The present inventors identified that a problem with this approach is that it requires the LO AFC loop to settle, often taking many code periods to complete. For systems that have adequate time to implement a frequency locking loop, this may be an acceptable trade-off. Also, as recognized by the present inventors, making the frequency correction in the RF downconversion portion of the receiver, and not in the baseband processing section of the receiver, preserves the signal processing efficiency, thereby enabling the use of lower cost, lower performance digital signal processing components as compared with state-of-the-art signal processing components.

In a receiver, a first LO is usually generated by a phase and/or frequency locked synthesizer. A block diagram of an integrated circuit-based LO synthesizer, such as a National Semiconductor LMX1501A, is given in Figure 8. Conventional phase lock frequency synthesizers are described in Manassewitsch, V., "Frequency Synthesizers Theory and Design", John Wiley & Sons, 1987, pp. 43-48, the contents of which is incorporated herein by reference. The synthesizer of Figure 8 includes a stable reference frequency source 800 (such as a quartz crystal oscillator), a reference divider 805, a phase and/or

frequency detector 810, a loop filter 820, a voltage controlled oscillator 830 and feedback dividers 840 and 850. An output 860 of the synthesizer is a signal at the desired frequency. The desired frequency is set by programming the moduli of the dividers 805, 840 and 850.

Making such an adjustment does correct for frequency error, however it does not adjust for code phase error or code phase drift over time. Traditional systems which employ frequency references, as depicted in Figure 8, typically use high power expensive components to set that reference very accurately. As will be discussed, the present inventors have identified a method to set the LO synthesizer very inexpensively, requiring a minimum of digital signal processing resources and subsequently track code drift throughout acquisition and demodulation without adjusting the receive local frequency reference.

Decimation

Digital signal processing systems typically employ decimation as a way to lower a number of samples that need to be processed at various processing steps. The effect of decimation is to combine a number of samples into a lesser number of samples, or merely select a subset of samples within a block of adjacent samples for subsequent processing. Decimation is typically preceded by a filter whose characteristics often impact signal strength adversely, particularly because the decimation operation has a characteristic transfer function that preferentially passes signals occurring in a middle portion of the characteristic transfer function, but attenuating signal offset from the middle portion. The present inventors have identified methods for eliminating or limiting the effects of decimation loss while minimally impacting processing requirements.

SUMMARY OF THE INVENTION

Accordingly, one object of the present invention is to overcome the above identified limitations and excesses in conventional direct sequence spread spectrum systems that prohibit the use of low-cost, low-end frequency references and digital signal processing components for performing the substantive direct sequence spread spectrum transceiver operations.

It is another object of the present invention to provide a method and apparatus for receiving a direct sequence spread spectrum signal sent from a transmitter having a relatively inaccurate frequency reference.

It is yet another object of the present invention to provide a method and apparatus for receiving and/or transmitting a direct sequence spread spectrum signal over a long period of time using only battery power as controlled by a power saving mechanism and/or signaling protocol.

It is still a further object of the present invention to provide a method and apparatus for receiving and/or transmitting a direct sequence spread spectrum signal with a device having a size (i.e., footprint) about equivalent to that of a conventional credit card.

Yet another object of the present invention to provide a method and apparatus for quickly acquiring a transmitted direct sequence spread spectrum signal. An aspect of this object is to provide a fast serial

search method that offers the simplicity attributes of a conventional slow serial search method and efficiency attributes of a parallel correlator, while also conserving battery power by disabling an RF front-end of a transceiver after receiving a portion of the signal and while attempting to acqire the direct sequence spread spectrum signal.

Still a further object of the present invention is to provide a receiver and/or transceiver architecture that includes a scalable sensitivity attribute that allows the sensitivity of the receiver/transceiver to be incrementally improved, at the expense of increasing computational loading.

It is still a further object of the present invention to provide a receiver and/or transceiver that includes a distributed decimation architecture that reduces computational load for baseband processing, while maintaining minimal decimation loss and reliable data communications.

It is another object of the present invention to provide a multi-channel direct sequence spread spectrum receiver and/or transceiver variant that offers increased sensitivity relative to a single channel receiver and/or transceiver, with provisions for improving system performance with enhanced automatic gain control (AGC) mechanisms, false trip avoidance mechanisms, direct current (DC) removal mechanisms, and predictive reposition mechanisms.

It is a further object of the present invention to provide a method and system for operating a receiver and/or transceiver in a direct sequence spread spectrum application using battery for power, with power management features.

It is still a further object of the present invention to provide a method and apparatus in a direct sequence spread spectrum communication system, with variable data rate option, by adjusting a relation of bit length to number of code chips per bit, using a relatively short pseudo-noise sequence length.

Another object of the present invention to provide a method for receiving OOK signals using a receiver and/or transceiver that employs a hard limited analog to digital converter.

Still another object of the present invention is to provide a direct sequence spread spectrum system/ network that establishes a communications protocol for saving battery power at various remote receiver/transceiver elements in the network.

It is another object of the present invention to provide a computer-based product including digital signal processing methods and data structures for efficiently implementing a direct sequence spread spectrum receiver/transceiver.

It is another object of the present invention to provide a direct sequence spread spectrum transceiver, and system that uses the transceiver that may be adapted to improve performance by substituting higher performance transceiver mechanisms for less capable mechanisms, although more computationally demanding and generally at higher cost.

These and other objects are provided by a method, apparatus, computer-based product and system that uses a receiver (or transceiver) to receive, digitize and process a direct sequence spread spectrum signal using efficient, low-cost digital signal processing components. A radio front end, and/or analog to digital conversion (ADC) apparatus are included to receive the direct spectrum signal and convert the received signal into a digitized signal. Downconversion and decimation are performed on the digitized signal at an intermediate frequency prior to despreading and correlating the digitized signal with a pseudorandom noise (PN) code used at a transmitter to spread a data signal contained in the direct sequence spread spectrum signal. Despreading and correlating the signal with PN signal extracts the data signal portion of the direct sequence spread spectrum signal for subsequent processing.

In order to initially align, and maintain alignment of, the PN code with the direct sequence spread spectrum signal, a timing and state control mechanism is included and provides time reference correction information to the signal processing components of the receiver and/or transceiver, without expressly modifying a locally generated time reference. Additional features include synchronization algorithms, suitable for use for low performance digital signal processors, implemented in coarse search and fine search algorithms for acquiring the direct sequence spread spectrum signal, using minimal processing resources.

The receiver and transceiver, according to the present invention, employ power management mechanisms that, at least in selected embodiments, may be powered by small batteries that apply power only to those components necessary to maintain an operational state of the receiver and/or transceiver, based on a present operational state of the receiver and transceiver. Using the power management features, the receiver and/or transceiver may communicate with other direct sequence spread spectrum transmitters and receivers as part of a communications network for multi-year periods of time.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

Figure 1 is a block diagram of a conventional Digital Signal Processor (DSP)-based receiver;

Figure 2 is a graph illustrating a signal spectrum before conventional harmonic sampling of an Intermediate Frequency (IF) signal when the IF signal is converted to "near baseband";

Figure 3 is graph illustrating a resulting frequency spectrum of conventional harmonic sampling of the Intermediate Frequency (IF) signal of Figure 2 when the IF signal is converted to "near baseband";

Figure 4 is a graph illustrating the signal spectrum before conventional harmonic sampling of an IF signal;

Figure 5 is graph illustrating a resulting frequency spectrum of conventional harmonic sampling of the IF signal of Figure 4 when the IF signal is brought directly to baseband;

Figure 6 is a graph that shows signal level distributions for 115 kHz and 20 kHz of noise bandwidth;

Figure 7 is a graph of a conventional correlation function with associated power loss due to fractional chip error of spreading code alignment;

Figure 8 is a block diagram of a conventional local oscillator frequency synthesizer;

Figure 9 is a block diagram of a single channel transceiver of the first embodiment of the present invention;

Figure 10 is plan view of the single channel transceiver, and associated battery pack of the first embodiment;

Figure 11 is a block diagram of a digital signal processing portion of the single channel receiver portion of the transceiver of Figure 9;

Figure 12 is a circuit diagram of a digital downconversion and decimation stage of the transceiver of the first embodiment, as realized by a table lookup process;

Figure 13 is a circuit diagram that shows an alternative digital downconversion and decimation stage, realized by Boolean logic;

Figure 14 is a graph that demonstrates (1) how decimation can reduce system performance, and (2) how this reduction in system performance can be avoided according to the signal processing architecture of the first embodiment;

Figures 15A-B are graphs that illustrate a signal acquisition process of the first embodiment;

Figure 16 is a flow chart of a fast time domain serial search process of the first embodiment;

Figure 17 is a graph that shows how the ideal correlation process of Figure 7 is adversely affected by noise;

Figure 18 is a graph that compares respective results of different inventive fine search methods;

Figure 19 is a flow chart of a Center of Mass fine search method;

Figure 20 is a flow chart of a Center of Mass 9 method;

Figure 21 is a flow chart of a Center of Mass 5+ method;

Figure 22 is a flow chart of a Center of Mass 9' method;

Figure 23 is a flow chart of a top-level search process performed by the transceiver of the first embodiment of the present invention;

Figure 24 is a graph that shows how antenna diversity can improve the received signal to noise ratio;

Figure 25 is a block diagram of a low-cost implementation of a frequency diversity transmitter portion of the transceiver of Figure 9;

Figures 26A-B are graphs showing the respective transmitted signals with frequency diversity disabled and enabled;

Figures 27A-D are timing diagrams showing how a transceiver of the first embodiment implements antenna and frequency diversity;

Figure 28 is a graph showing how averaging a signal in the first embodiment reduces an effects of noise;

Figure 29 is a graph showing how averaging reduces a false alarm rate in the first embodiment;

Figures 30A-F are respective approaches for incrementally increasing data rate using partial sums of the correlation function;

Figure 31 is block diagram of an alternative demodulator of the first embodiment showing a differential binary phase shift keying (DBPSK) demodulator, with scaleable bit rate;

Figure 32 is a block diagram of an alterative embodiment of a receiver portion shown in Figure 9 for resolving frequency ambiguity between a remote transmitter and the receiver;

Figure 33 is a illustration of an approach for implementing a frequency detection portion of the receiver shown in Figure 32;

Figure 34 is a block diagram of an implementation of the digital-to-analog converter of Figure 32;

Figure 35 is a block diagram of the digital downconversion, decimation, and removal of Analog-to-Digital converter (ADC) DC offset of a multi-channel receiver portion of a second embodiment transceiver embodiment of the present invention;

Figure 36 is a block diagram of channel formation portion of the multichannel receiver shown in Figure 35, which reduces processing requirements for symmetric channel filters;

Figure 37 is a block diagram of a center channel forming portion, having reduced processing requirement attributes, for a center channel filter of the multichannel receiver of Figure 35;

Figure 38 is a graph demonstrating how a reduction in decimation loss may be achieved in the multi-channel receiver of the second embodiment of the present invention;

Figure 39 is a graph showing how non-uniformly spaced frequency channels in the multi-channel receiver of the second embodiment limits system performance loss;

Figure 40 is a block diagram of a fast frequency domain code correlator portion of the second embodiment;

Figure 41 is a block diagram of a conventional correlator;

Figure 42 is a block diagram of a conventional circular correlator;

Figure 43 is a block diagram of a conventional circular correlator implemented with a convolution process;

Figure 44 is a block diagram of a conventional circular convolution correlator, operating in the frequency domain;

Figure 45 is a illustrative flow diagram of an implementation of an inventive frequency domain code correlator of the second embodiment;

Figure 46 is a graph of signal conditions that can cause false trips (i.e., false correlation detection indications);

Figure 47 is a graph that shows how the power of a received noise signal will be distributed among frequency channels in a multi-channel receiver;

Figure 48 is a graph that shows how the power of a received Carrier Wave (CW) jammer signal will be distributed among frequency channels in a multi-channel receiver;

Figure 49 is a graph that shows how the power of a received non-correlated spread spectrum signal will be distributed among frequency channels in a multi-channel receiver;

Figure 50 is a graph that shows how the power of a received correlated spread spectrum signal will be distributed among frequency channels in a multi-channel receiver;

Figure 51 is a flow chart of false trip avoidance method implementable in the multi-channel receiver;

Figure 52 is a graph illustrating results of a correlation function of a single code period of data in the multi-channel receiver embodiment;

Figure 53 is a graph similar to Figure 52, but including an averaging mechanism to reduce the effect of noise;

Figure 54 is another graph showing how averaging reduces a false alarm rate in the multi-channel receiver;

Figures 55-61 are flow charts of an Automatic Gain Control (AGC) method implementable in the multi-channel receiver of the second embodiment;

Figure 62 is a graph showing signal power loss in a multi-channel receiver of the second embodiment due to past frequency drift of the transmitter;

Figure 63 is a graph showing received signal loss due to fast transmitter frequency drift;

Figure 64 is a flowchart of a process implementable in the multi-channel receiver to compensate for fast frequency drift in a signal transmitted by a transmitter;

Figure 65 is a graph showing a method for limiting noise contribution and corresponding to the process illustrated in Figure 64;

Figures 66A-C are graphs of signal loss due to frequency error and how this loss may be reduced by implementing a code phase repositioning and predictive code phase repositioning process throughout the message;

Figure 67 is a block diagram of a system with multiple transmitters, and multiple receivers that are connected to a processor via a common bus in a network, according to a third embodiment of the present invention;

Figure 68 is a block diagram showing a battery operated remote transceiver (BORT) application of the network of Figure 67;

Figures 69A-B are graphs shows network timing, corresponding to Figures 67 and 68;

Figures 70A-C jointly present a flow diagram of a process flow implemented in a BORT device of Figure 68;

Figures 71A-B jointly present a flow diagram of a process flow of a system transceiver of Figure 68;

Figures 72A-C jointly present a timing diagrams showing the steady state communication exchanges between a system transceiver and a BORT device;

Figures 73A-B jointly present a flow diagram showing the steady state operation of a BORT device;

Figure 74 is a timing diagram showing the initialization sequence of a BORT device in a BORT-based system, or network;

Figure 75 is a flow diagram showing a BORT initialization process;

Figures 76A-C are timing diagrams showing the re-synchronization sequence of a BORT device in a BORT-based system, or network; and

Figure 77 is a flow diagram of a BORT re-synchronization process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, and more particularly to Figures 9 and 10 thereof, there is illustrated a first embodiment of the present invention in the form of a credit card sized single channel transceiver (which includes a receiver and a transmitter, hence the term "transceiver"), that is included as part of a direct sequence spread spectrum network of transmitters, and receivers, which include transceivers. As will be discussed in reference to Figures 9-34, the present transceiver is of a sufficiently small size that it may be operated under battery control, and require low end, low performance digital signal processors in order to perform the digital receiver, transceiver and other control functions.

Figure 9 is a block diagram of the single channel transceiver that includes two antennas 901 and 903 that feed a radio frequency (RF) front end 905. A direct sequence spread spectrum signal, formed at a transmitter preferably with a 63 bit pseudorandom noise (PN) code at a transmitter, is coupled into the antennas 901 and 903 and to the RF front end 905. An output of the RF front end 905, provides, at an intermediate frequency (IF), the received signal to a single bit analog to digital converter (ADC) 907. The ADC 907 converts the analog signal into a series of digital samples, as a particular sample rate as will be discussed, which are then be processed in baseband processing section 908. The digital signal processing section 908 includes a low performance 16-bit digital signal processor, which operates at less than 20 MHZ clock. One example of such a digital signal processor is Model 893x1, available in the United States from Zilog.

More particularly, the digital samples from the ADC 907 are passed to a quadrature (i.e., inphase, I and quadrature, Q) downconversion mechanism 909 that further reduces the center frequency of the received signal to baseband, and decimates the digital signals. By downconverting and decimating the digital signal sample rate is reduced, which in turn reduces a digital signal processing load placed on the digital signal processing section 908. The output of the quadrature downconversion mechanism 909 is provided to a direct sequence despreading/correlator mechanism 911. The despreading correlation mechanism 911 aligns the PN code, which is the same code as that used to spread a data signal at the transmitter but generated locally at the transceiver, to the incoming signal so as to correlate the received signal with the locally generated PN code. As a consequence (as will be explained), the despreading/correlating mechanism 911 further decimates the correlated signal so as to further reduce the data rate and realize the 18 dB of processing gain (i.e., the gain associated with the PN spread spectrum signal) so that the signal may then later be passed to additional mechanisms for identifying when the signal is correlated, how well the signal was correlated, and ultimately for extracting the data from the correlated signal.

The output of the direct sequence despread/correlator 911 passes to a switch 913, preferably implemented as a state-driven digital process, under control of a timing and state control mechanism 921,

as shown. The timing and state control mechanism 921 first throws the switch 913 so as to connect to a coarse search and trip mechanism 919 which performs initial signal acquisition, and acquisition detection respectively. Once the coarse search and trip mechanism 919 determines that the signal has been acquired, the timing and state control mechanism 921 throws the switch 913 into a middle position, as illustrated, so as to pass the output of the direct sequence despread/correlator 911 to a fine search mechanism 917.

The fine search mechanism adjusts the receive PN sequence to align within a small predetermined chip interval with respect to the transmitted PN sequence. In the preferred embodiment the fine search mechanism 917 positions the received PN sequence to less than 1/4 of a chip interval. Once within the 1/4 chip alignment, the timing and state control circuit 921 moves the switch 913 to the upper position, as illustrated, so as to pass the output of the direct sequence despread/correlator 911 to the demodulation circuit 915 which extracts the data from the transmitted signal and passes the data to a data sink as shown.

The output of the demodulation mechanism 915 is also passed to the timing and state control mechanism 921 as a reposition signal to perform a reposition operation like that discussed in U.S. Patent 5,457,713, incorporated herein by reference.

The time reference correction mechanism 923 provides a time reference correction signal to the ADC 907, quadrature downconversion mechanism 909, and direct sequence despread/correlator mechanism 911, in order to compensate for time drift errors induced by differences in transmitter and receiver time references (a time reference being a particular implementation of a frequency reference, and thus the two terms being used in a corresponding sense herein), due to inherent inaccuracies in low-cost, low performance time references such as receiver time reference 927 as shown. The time reference correction mechanism does not adjust the receiver time reference 927, as is done in convention receivers. Rather the time reference correction signal compensates for the inaccuracies induced by the time reference 927 in the various elements that employ an input from the receiver time reference 927.

The timing and state control mechanism 921 also includes an antenna select control signal which selects between antennas 901 and 903 when antenna diversity (such as for spatial or polarization diversity purposes) is employed. In addition, the select signal includes a frequency control select signal, illustrated by a dashed line, applied to the RF front end 905, so as to control frequency diversity reception when frequency diversity is employed in the transceiver of Figure 9, as will be discussed.

The transceiver of Figure 9 includes a power control mechanism 925 that is controlled by the states determined in the timing and state control mechanism 921, so as to provide a power management function for the transceiver. More particularly, when the transceiver is operated in selected states, where not all of the components, such as the RF front end 905, are required for successful operation, the power control mechanism 925, places the selected components in a reduced power consumption mode of operation.

Although not shown for clarity purposes in Figure 9, the power control mechanism 925 is operatively coupled to a battery pack 1003 (Figure 10) and to each of the active components in the transceiver illustrated in Figure 9. Consequently, the power control mechanism, can remove power from the RF front-end 905, transmitter 929 and the entire, or subsections of, the digital signal processing section 908.

The transmitter 929 that is connected to a transmit antenna 931, which may be a separate element, but preferably is the same as antenna 901 or 903 with an accompanying diplexer (not shown). The transmitter 929 is provided with an external data source as shown, and derives time and frequency information from the receiver time reference 927 such that transmissions by the transmitter 929 will also be subject to the timing uncertainties caused by low cost receiver time reference 927. The transmit feature associated with the transmitter 929, and the waveform produced therein are discussed in U.S. Patent 4,977,577, incorporated herein by reference.

Figure 10 is a plan view of the credit card outline transceiver 1000 as was discussed in Figure 9. The two dimensional footprint of the credit card outline transceiver 1000 includes a length in an X direction of about 3.4", and a width in a Y direction of about 2.1" as shown. A thickness (not shown) is roughly .4". The battery pack 1003 connects to the credit card outline transceiver 1000 via a connector 1002 as shown. The battery pack 1003, includes two external 3.6V lithium thionyl chloride ($LiSOCl_2$) cells (such as a LS-14500 cell available from Faft Corporation), which provide sufficient power to operate the transceiver, as discussed herein, for multiple years.

The data source and data sink on the credit card transceiver shown in Figure 9, is provided via bidirectional interface 1004 as shown in Figure 10. The connector includes a serial interface such as a RS232C, pseudo RS232C (0-5V RS232C) or other interfaces such as RS-485. In addition, other interfaces may also be suitable, such as universal serial bus USB, Fire Wire (IEEE 1394), and other data interfaces available in data communication equipment.

Selecting Sequence Length Based on Prime Factors

The process gain that a radio exhibits is driven by the length of the spreading sequence. The present invention uses the class of codes referred to as maximal length (ML) sequences, due to their correlation properties, and preferably a 63-bit ML sequence.

ML sequences are always of length 2^k-1, where k is any positive integer. The process gain associated with a particular spreading sequence is 20log(n), where n is the length of the spreading sequence. Longer spreading sequences allow for more process gain; but require more computational loading to achieve correlation. The present invention does not attempt to achieve the greatest possible processing gain (because too much processing power is required) but provides a reasonable amount of processing gain that can be realized with limited computational resources.

For any given relative code phase alignment between the transmitter and receiver spreading codes, a single power value must ultimately be calculated, where the phrase "code phase" refers to an alignment of the code chips used to spread the signal relative to the code chips of the PN code generated locally at the transceiver. The present invention uses decimation in the time domain and Fourier transforms in the frequency domain to achieve this result. The present invention utilizes partial decimation (i.e., multiple decimation stages distributed throughout the transceiver) and partial transformation techniques to reduce computational loading. These techniques are enabled by selection of length of the spreading sequence that can be factored into prime numbers. In the preferred embodiment, a code length of 63 is selected and can be factored into prime numbers 3, 3, and 7. Table 3 depicts ML sequences of length 2^k-1 for k up to 13, as well as the number of prime factors for each length and a processing gain associated with each code length.

k	2^k-1	*# of Prime Factors*	*Process Gain(dB)*
1	1	1	0.000
2	3	1	4.771
3	7	1	8.451
4	15	2	11.451
5	31	1	14.914
6	63	3	17.993
7	127	1	21.038
8	255	3	24.065
9	511	2	27.084
10	1023	3	30.099
11	2047	2	33.111
12	4095	5	36.123
13	8191	1	39.133

Maximal Length Sequence Lengths

Table 3

One example of computational savings resulting from selecting a code sequence that is factorable by multiple prime factors is illustrated by comparing a length-31 sequence (which is not factorable) and a length-63 sequence (factorable by three prime factors). The length-31 sequences have about 15dB process gain, which would generally be recognized as having an adequate process gain, without resorting to a longer code sequence. However, since 31 is a prime number, a Fourier transform performed on a signal that was spread with this code sequence would require 31 * 31 = 961 multiply-accumulate operations. In contrast, the length-63 code sequence has prime factors 7, 3, and 3, and thus requires a Fourier transform with only 63 * (7 + 3 + 3) = 819 multiply-accumulate operations. Therefore, scaling

from 31 to 63 provides 3 dB of additional process gain with no additional, actually a decrease, in computational loading.

Another computational efficiency feature offered by a code sequence that is factorable by multiple prime numbers is that increase flexibility is achieved in selecting intermediate decimation factors. This in turn enables flexibility in the number and position of decimation, filtering, and downconversion processes employed in the transceiver.

Single Channel Receiver Partial Decimation Method

The single channel embodiment of this invention employs a distributed (partial) decimation scheme configured to reduce the Nyquist bandwidth of the signal to equal the frequency uncertainty caused by inaccurate frequency references in the transmitter and receiver. To this end, in this embodiment, the signal is sampled at 4 times the chip rate (i.e., the number of chips per second applied in the despreading stage), downconverted and decimated by 4 immediately so as to drop the resulting sample rate to 1.2 MHZ. The signal is correlated (despread) and subsequently decimated again to drop the Nyquist bandwidth to ± 57.6 kHz, which in the preferred embodiment is the frequency uncertainty bandwidth (BW).

The digital signal processing flow for the receiver portion of the transceiver shown in Figure 9 is depicted in Figure 11. In Figure 11, a signal of interest lies at an IF frequency of 49.2 MHZ and is applied to an input 1102 of a ADC 1104 at a sampling frequency of 4.8 MHZ (1106). The resulting signal at the output 1108 of the ADC 1104 is at a near baseband frequency of 1.2 MHZ with a sampling of 4.8 MHZ. A tone generator 1110, combined with phase delay element 1112 and mixers 1114I and 1114Q, combine to form a quadrature half mixer. A first decimation stage is implemented with low pass filters 1116I and 1116Q and decimation blocks 1118I and 1118Q. Code correlation is performed as the signal from PN code generator 1120 is mixed in 1122I and 1122Q to generate correlated I and Q data streams. This data is further filtered by low pass filters 1124I and 1124Q and then decimated by elements 1126I and 1126Q.

The resulting I and Q data streams form a set of partial decimation sums, each sum being the correlation of 42 processed samples. The decimation from the sample rate with 252 points to 6 points reduces the effective Nyquist bandwidth for the signal and sets the predetection bandwidth to 115 kHz. Finally, the magnitude of the resulting signal power is calculated by respective squaring mechanisms 1128 I and 1128 Q and summation blocks 1130I, 1130Q, and 1132. The result is signal a 1134, which is a magnitude scalar value representative of the correlated signal power in a 115 kHz noise bandwidth.

The leftmost portion of Figure 11 performs the quadrature downconversion and partial decimation. The right portion of Figure 11 performs the subsequent despreading and decimation required to limit the noise bandwidth and achieve maximum sensitivity, while spanning a frequency uncertainty of 115 kHz.

Alternating a decimate-by-10 operation followed by a decimate-by-11 operation, three times in succession, realizes the decimate-by-10.5 block 1126 in Figure 11. The resulting 6 data points of I and 6 data points of Q are squared, thus destroying their phase relationship prior to final decimation which is performed as a summing function. As the phase relationship is lost in the squaring block, further techniques for limiting noise bandwidth is prevented so that the subsequent summation yields a predetection noise bandwidth of 115 kHz. Once again, the wide predetection noise bandwidth of 115 kHz, which is much larger than the approximately 19.2 kHz baseband signal is needed because the exact position of the baseband signal cannot be a priori predicted with any degree of certainty, owing to the inaccuracy of the transmitters frequency reference.

The above-described process is used to create a single channel receiver tolerant to various frequency uncertainties. It is limited only in the number of decimation end points and associated decimation bandwidth prior to squaring. Reducing the 63 data points to 5 (decimate-by-13, 12,13,12,13) would result in a final noise bandwidth and frequency uncertainty of 96.3 kHz. Similarly reducing the 63 data points to 4 (decimate-by-16, 15,16,16) would result in a final noise bandwidth and frequency uncertainty of 77.1 kHz; 3 points (21,21,21) = 57.8 kHz; 2 points (32,31)=38.5 kHz. Finally, decimating all the way to one point before squaring is the implementation of one of the channel filters used in the most sensitive embodiment that yields a single channel equal to the data bandwidth of 19.2 kHz.

Digital Downconversion at Fs/4 Centered IF Minimizes Computational Loading

Preferably the ADC 1104 is a 1-bit sampled limiter. However, a multi-bit ADC may also, albeit at greater expense and possible requirement that an Automatic Gain Function (AGC) function be used to avoid applying the signal at a level that is outside of the multi-bit ACC's dynamic range.

The overall noise contribution due to IF slew limiting and aperture jitter is evaluated to ensure that remaining dynamic range supports signal processing requirements. For the present invention, the dynamic range must be able to receive both noise and at least 18 dB (and preferably 36 dB) of signal. Because the low-cost embodiment of the instant invention is a 1-bit limited system, the dynamic range of the system is limited to the process gain of 18 dB. But since the system can also produce carrier insertion for jamming signals, the theoretic process gain against a frequency coincident jamming signal is 36 dB.

The resulting spectrum following digitization is centered at +¼ Fs so as to maximize distance to the nearest image (as was discussed in reference to Figure 3). Additional images exist at -¾ Fs as well as – ¼ Fs. Because the signal is sampled real, the image is ideally centered in the Nyquist bandwidth prior to final downconversion as shown previously in Figure 3. The final conversion to baseband must be performed in quadrature to ensure that negative images do not overlap. The digitized signal is downconverted to baseband using a half-mixer, as discussed in reference to the background art. The

present invention completes the signal downconversion operation by moving the quadrature signal centered at Fs/4 (i.e., 1.2 MHZ) to baseband (i.e., 0 Hz), as performed with components 1110, 1112 and 1114.

Figure 11 illustrates the sampled limiter (i.e., ADC) 1104 as a mixer because the sampled limiter 1004 is operating as a harmonic sampler and thus also downconverts the IF centered at 49.2 MHZ. Several IF frequencies are preferred based on the availability of inexpensive surface acoustic wave (SAW) filters. Inexpensive bandpass SAW filters enable the harmonic sampling technique due to their sharp roll-off and excellent ultimate rejection characteristics. 10.8 MHZ is very near the standard SAW frequency of 10.7 MHZ used widely as a communication IF. 34.8 MHZ is ideal due to SAW filters that are present in many color televisions. 49.2 MHZ, the preferred embodiment, is also ideal due to the volume of portable telephones using this frequency. 70 MHZ SAW filters are also available, but the harmonic multiplicand (and corresponding aperture jitter noise) increases and the slew limiting requirements of the sampling device increase component cost. The 10th harmonic multiplicand of the sample rate 1106 of 4.8 MHZ creates a mixing tone at 48 MHZ, the difference yielding the digitized downconverted image 1108 centered at 1.2 MHZ. The half-mixer (1144) performs a complex translation of the real signal centered at 1.2 MHZ and completes the downconversion to the baseband signal at 0 Hz. Signal processing efficiencies exist with under these special circumstances when the IF is centered in the Nyquist bandwidth. Namely, the downconversion tone 1110 is realized digitally as a series of values of 1.2 MHZ as sampled at 4.8 MHZ, which in turn defines a 4:1 relationship between Fs and the IF center frequency (Fc). This 4:1 relationship enables a particularly efficient downconversion operation because a coefficient set for the I (In phase) data downconversion mixer may be represented as follows:

I Coefficients [cos (kπ/2)]: 1, 0, -1, 0, 1, 0, -1, 0, 1, 0, -1, 0...

Similarly, the Q (Quadrature) coefficients related to I by 90 degrees become:

Q Coefficients [sin (kπ/2)]: 0, 1, 0, -1, 0, 1, 0, -1, 0, 1, 0, -1...

for all $k \in \{0, 1, 2, 3, \ldots\}$. This relationship assumes an initial phase of 0 degrees for the coefficient set, but because the present invention does not provide coherent detection, an initial phase relationship is arbitrary. Forcing the initial phase to 0 degrees greatly simplifies the computational task for performing the quadrature downconversion because each mixer 1114I and 1114 Q need only perform half of the multiplies because one-half of the coefficient terms are zero. The processing efficiency is further simplified by recognizing that when a multiply is to be performed with a non-zero coefficient, the sampled data is either multiplied with a 1 or a −1, which corresponds to a sign inversion of the sample. Consequently, these samples are either left unchanged or simply inverted in sign by a sign inversion operation.

Under the above-described conditions, the half-mixer multipliers 1114I and 1114Q become simple XOR gates for single-bit data. A single XOR gate performs the same task for parallel ADC data provided

the data is already in Gray code or other binary weighted format in which a single bit change creates a signed inversion of equal magnitude. Marvin E. Frerking teaches this technique for narrowband systems in his text entitled "Digital Signal Processing in Communication Systems", 1994, the contents of which is incorporated herein by reference. As presently recognized, this technique is similarly applicable to a direct sequence spread spectrum receiver.

The resulting complex signal 1113I and 1113Q at the input to the lowpass filters 1116I and 1116Q have a Nyquist bandwidth of 2.4 MHZ. The time resolution provides ¼-chip steps for fine search by skipping or reusing a data point. The fine search algorithm uses this technique to correlate the incoming signal against a fixed PN at ¼-chip resolution.

Coarse search does not require ¼-chip time resolution. Rather, a reduction of data and corresponding computational loading is realized by decimating the complex signal to the chip rate. Figure 11 performs this function in the lowpass filters 1116I and 1116Q and decimators 1118I and 1118Q. Decimation-in-time processes may be viewed as providing mixing and sampling operations. Filters 1116I and 1116Q are used to reject unwanted images that exist in the digitized spectrum separated by the Nyquist bandwidth, in this case 2.4 MHZ. A digitally implemented "boxcar-averaging" filter is used in the instant invention so as to minimize correlation loss while rejecting image power below the trip threshold.

Decimate-by-four 1118I and 1118Q mechanisms follow the filters 1116I and 1116Q so as to lower the effective sample rate to 1.2 MHZ, shown as signals 1119I and 1119Q. The decimation process immediately following the half-mixer may be realized as a simple adder that adds every other sample, ignoring the products containing zero coefficients. The combined downconversion/decimation block is therefore optimized for minimized computation and signal processing load, reducing multipliers to single XOR gates and the decimators to simple adders.

Alternatively, the entire downconversion/decimation process is performed without any mathematical processing operations being performed on samples originating from a one-bit ADC converter. Specific signal processing functions are avoided by using two 16-element lookup tables and indirect addressing based on a serialized 4-bit nibble. The 16-element lookup tables may be implemented in semiconductor memory or other mechanism for holding database entries (such as boolean operators, as will be discussed). Data structures for the database entries are shown in Tables 1 and 2, where respective fields of the respective data structures include decimated and downconverted data samples corresponding to particular sets of pre-decimated samples.

Figure 12 depicts a digitizing system that would use this technique replacing the half mixer and decimate operators of Figure 11. In Figure 12, a signal of interest 1202 lies at an IF frequency of 49.2 MHZ and is sampled by the 1 bit ADC 1204 at a sampling frequency of 4.8 MHZ (1206). The resulting signal 1208 is at a near baseband frequency of 1.2 MHZ with a sampling rate of 4.8 MHZ. Because the

sampling rate is four times the code repetition rate, four samples represent a single code chip. These four samples are converted into parallel by the serial-to-parallel converter 1210 and then passed to a database implemented as the lookup tables 1212 I and 1212 Q implemented as semiconductor memory. The four parallel samples are used as the address input (address or database indica) of these lookup tables 1212I and 1212Q. The four address bits are weighted according to the I coefficients (1, 0, -1, 0) and the corresponding Q coefficients (0, 1, 0, -1) to produce the D0 and D1 output bits. The divide-by-four device 1216 serves to clock latches 1214 I and 1214 Q to produce the output data streams 1218 I and 1218 Q at one fourth the rate of the original sample stream. The table lookup feature of Figure 12 takes full advantage of the 4:1 ratio of Fs to Fc.

Table 1 illustrates the content and data structure of the lookup tables that simultaneously perform this downconversion and decimation function. In Table 1, downconversion coefficient values of A3-A0 are represented in parentheses, and all possible input patterns are presented. Note that for the purposes of correlation, a '1' in the input data corresponds to a '+1' value and that a '0' in the input data corresponds to a '-1' value. These sampled data values are multiplied by the downconversion coefficient values, in parentheses, then summed to produce the binary weighted D0 and D1 output values.

The I data only uses alternating data points exclusive of the Q data (unused points are shaded gray in Table 1), and therefore, Table 1 collapses into two 4-element tables as shown in Table 2. Conversely, in systems where additional memory is available, the shift register 1210 can be expanded and the table appropriately increased in scale to perform a wide variety of decimation ratios and downconversion tones. For example, if the Fs to Fc ratio were 8:1, eight samples of the data would be sufficient for multiplication (mixing) with one period of the downconversion tone. The shift register 1210 would be lengthened to 8, and the lookup table would have 256 values. The data width of the output would be scaleable, and the quantization error would be predictable and programmed into the lookup table. This quantization error is not a problem in the case of 4:1 ratios because the coefficients are integer. Fractional coefficients, however, create a need to represent non-integer decimation results. The output of the lookup table can represent the fractional results to whatever resolution is required by the system implementation at the cost of widening the datapath (e.g., a bus).

I Data Lookup Table					
$A3_{(}$	$A2_{(0)}$	$A1_{(-1)}$	$A0_{(0)}$	D1	D0
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	0	1

Q Data Lookup Table					
$A3_{(0)}$	$A2_{(1)}$	$A1_{(0)}$	$A0_{(-1)}$	D1	D0
0	0	0	0	0	1
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	9	1
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	0	1

Downconvert and Decimate Lookup Table

Table 1

I Data Lookup Table					
$A3_{(}$	$A2_{(0)}$	$A1_{(-1)}$	$A0_{(0)}$	D1	D0
0	X	0	X	0	1
0	X	1	X	0	0
1	X	0	X	1	0
1	X	1	X	0	1

Q Data Lookup Table					
$A3_{(0)}$	$A2_{(1)}$	$A1_{(0)}$	$A0_{(-1)}$	D1	D0
X	0	X	0	0	1
X	0	X	1	0	0
X	1	X	0	1	0
X	1	X	1	0	1

Downconvert and Decimate Lookup Table

Table 2

The example in Figure 12 uses a 16-element table that holds the sum of the two valid samples in a two-bit result. Processors that have an abundance of memory and excellent memory access operations but do not have fast multiply-accumulators will benefit from this technique. This enables the class of general purpose microcontrollers to perform "DSP" functions without the need of fast multiply-accumulator operations.

In another alternative, reference is made to data in Table 2, where the resulting I data and Q data are simplified into logical combinations of the input samples. The lookup table itself can be replaced with a few logic gates (serving as the database, which is a hardwired, preprogrammed alternative to the

semiconductor database of Figure 12) implemented in the decimation stage. The Boolean logic expression for these is given by:

I [D0]= !(A3 XOR A1), I [D1] = A3 AND !A1

Q [D0] = !(A2 XOR A0), Q [D1] = A2 AND !A0,

where "!" denotes negation of Boolean term. A 2-bit sum for each I and Q data path is denoted as D1, D0 where D0 is the least significant bit. Figure 13 depicts the downconversion and decimation circuit that performs this function.

In Figure 13, a signal of interest 1302 lies at an IF frequency of 49.2 MHZ and is sampled by the 1 bit ADC 1304 at a sampling frequency of 4.8 MHZ (1306). A center of the resulting signal 1308 is above a baseband frequency by about 1.2 MHZ and represented with a stream of samples at a sampling rate of 4.8 MHZ. Because the sampling rate is four times the code repetition rate (i.e., a rate at which the PN code repeats itself), four samples correspond to a single code chip interval. These four samples are converted into a parallel representation by the serial-to-parallel converter 1310 and then passed to Boolean logic blocks 1312I and 1312Q. The combinatorial block 1312I performs the same function as the lookup table and produces a decimated, downconverted signal. A divide-by-four device 1316 serves to clock latches 1314I and 1314Q so to produce the decimated, downconverted output data samples as 1318I and 1318Q.

Coefficient-less Downconversion, Despread and Decimation in a DSP Processor

Another alternative approach for implementing the quadrature downconversion and decimation function uses a signal processing engine such as a DSP or other processor to perform this function as the data is read from the sampling device.

This approach will only be computationally efficient if the processor possesses the capability for sign inversion of the data without adding computational complexity. This is often true in commercial digital signal processors because the read function is highly pipelined into the execution process so as to maximize performance. Sign inversion can most simply be performed by adding or subtracting the value as read, requiring no multiply function at all. Provided this condition is met, the processor combines the 4:1 downconversion ratio efficiencies discussed previously with the data collection and decimation to perform the downconversion, despreading and decimation process without the need for storing any data coefficients. This is particularly useful for processors with limited RAM memory such as very inexpensive processors or a hardware state-machine implementation (as implemented in a programmable logic device--PLD, application specific integrated circuit--ASIC, etc.).

Coefficient-less decimation, downconversion and despreading as implemented in the present embodiment is based on the processor's ability to sign-accumulate data as read from the sampling device. Two parallel interleaved processes are executed to compute the inphase and quadrature data streams.

When avoiding the storage of coefficients to perform the downconvert, despread and decimate function, an in-line execution process is performed that adds/subtracts in the accumulation process to represent multiplication by 1 or −1. In this context, the in-line code itself serves as the database repository for the resulting downconverted, despread, and decimated samples. So as to further illustrate to explain this technique, exemplary pseudo-code for the in-line code is listed below:

```
LOAD      A,PORT    ;read data from port, seed the accumulator with value
ACCUM     A,PORT    ;read data from port, accumulate value into register A
SUBTRACT  A,PORT    ;read data from port, subtract value from register A
NOP                 ;perform no function, wait for next sample.
```

A single processor can interleave the inphase and quadrature functions if there exists multiple accumulators or registers in the processor to hold intermediate values. For the purpose of this example, the above instructions would be modified to replace the "A" register with a "B" register. Either multiple accumulators, context switched register files or temporary storage of intermediate values performs this function.

Provided that the processor is executing at a multiple of the sample rate, the downconversion and decimation algorithm may be encoded into the firmware without using any data store. For example, if the processor executed four instructions per sample, the downconversion and decimation function becomes as follows:

```
LOAD      A,PORT    ;I read, seed accum (I virtual coefficient = 1, Q = 0)
NOP                 ;wait for new data
NOP                 ;wait for new data
NOP                 ;wait for new data
LOAD      B,PORT    ;Q read, seed accum (I virtual coefficient = 0, Q = 1)
NOP                 ;wait for new data
NOP                 ;wait for new data
NOP                 ;wait for new data
SUBTRACT  A,PORT    ; read sample, accum (I virtual coefficient = -1, Q = 0)
STORE     MEM,A     ;save decimated I value for later processing.
                    ;no need to wait for next sample since it is a 0 coefficient
```

```
NOP                     ;wait for new data
NOP                     ;wait for new data
SUBTRACT   B,PORT       ; read sample, accum (I virtual coefficient = 0, Q = -1)
STORE      MEM,B        ;save decimated Q value for later processing.
NOP                     ;wait for new data
NOP                     ;wait for new data
```

The above pseudo-code performs a quadrature downconversion and 4:1 decimation on an input data stream. It is repeated as in-line code for however many iterations necessary to correspond with a symbol interval. For concurrently run processes, the NOP instructions are replaced with instructions for performing concurrent processes, such as moving data or subsequent signal processing.

The above example is implemented in a loop structure when downconversion and decimation is the only function to be performed. Alternatively, despreading could be combined with the method where the spreading code inverts the sign of accumulation on a chip by chip basis. For chips where the spreading code is a "1", the above described process leaves the resulting sample unchanged. For chips where the spreading code is a "0", the above process sign inverts the decimated result prior to performing the STORE operation, or alternatively the LOAD and SUBTRACT functions could be replaced with a LOAD_NEGATIVE and ACCUM instruction where the data is sign inverted on the initial read and accumulated on the second sample instead of subtracted. The code becomes an in-line algorithm where the length of the algorithm extends to the encompass the received signal spreading code.

Because multiplication is an associative operation, the downconversion and decimation functions can be performed concurrently even if the downconversion and oversample ratios are different. The downconversion ratio is given by the ratio of Fs to Fc which must be 4:1 for this process to function properly.

An oversample ratio is given by a ratio of Fs to the frequency of chipping rate, F_{chip} which may be any integer number. The present embodiment uses an oversample rate of 4:1, but a 5:1 is used in the multi-channel embodiment (discussed later). Table 3 depicts how the associative property of multiplication allows for simultaneous downconvert and despread without the need for coefficient store.

Data Sample Index	Fs:Fc = 4:1 Down-conversion		Fs:F_{chip}= 5:1 Despread PN	Combined Virtual Coefficient		In Line Operation for I	In Line Operation for Q	In Line Interleaved I & Q Downconvert & Despread
	I	Q		I	Q			
1	1	0	1	1	0	ADDI	NOP	ADDI
2	0	1	1	0	1	NOP	ADDQ	ADDQ
3	-1	0	1	-1	0	SUBI	NOP	SUBI

4	0	-1	1	0	-1	NOP	SUBQ	SUBQ
5	1	0	1	1	0	ADDI	NOP	ADDI
6	0	1	-1	0	-1	NOP	SUBQ	SUBQ
7	-1	0	-1	1	0	ADDI	NOP	ADDI
8	0	-1	-1	0	1	NOP	ADDQ	ADDQ
9	1	0	-1	-1	0	SUBI	NOP	SUBI
10	0	1	-1	0	-1	NOP	SUBQ	SUBQ
11	-1	0	-1	-1	0	SUBI	NOP	SUBI

Coefficient -less Downconvert & Despread

Table 3

As shown in Table 3, for the I data sample, an in-line coded series of accumulate and subtract operation performs the downconversion, despread and decimate function without using coefficients even in the case where the oversample ratio is 5:1.

The decimation ratio becomes a straight-forward operation in that the accumulated sum may be stored as an intermediate partial decimation result at any integer number of samples. This provides for intermediate decimation results for setting a predetection noise bandwidth similarly for the quadrature data. For example, assuming the receiver is already PN aligned with the received signal and demodulating the signal, the 252 samples may be decimated by 42, i.e., 42 successive samples accumulated and stored as intermediate values, setting the predetection bandwidth to +/- 57.6 kHz.

This technique has application for programmable processors or hardware state-driven engines where memory limitations prohibit access to enough coefficients (of the PN code) to encompass the received signal spreading code length. For example, in a DSP processor with 128 memory locations available for coefficient storage, a spreading code length of 63 and an oversample ratio of 4:1, the number of data samples corresponding to a code repetition interval is 252. Most processors are optimized for a one-to-one correspondence of data sample to PN code coefficient. With only 128 memory locations, there are too few locations to hold 252 coefficients. Using this technique, the downconvert, despread and decimation function requires no memory locations for coefficient storage using the processing efficiency principles discussed herein.

The sampled signal interval is initially decimated to a sampling rate equal to the chipping rate. During coarse search mode, before the signal is aligned with the PN code, the sampled data is mixed with the PN code at increments of 1-chip steps. For each spreading code phase position, the correlation result is bandwidth limited down to the predetection bandwidth so as to determine if that particular spreading code position resulted in a high correlation result, indicative of code alignment.

Because decimation is similar to sampling, the effects of aliasing must be avoided, and therefore a decimation filter is included prior to the decimation step to ensure that alias images do not destroy system

performance. Also, this filter should attenuate the desired signal to a minimal extent because the signal may still contain mismatches in PN alignment. In order to maximize correlation gain (process gain), a boxcar averaging filter is used as the decimation filter. A boxcar averaging filter has a rectangular time domain window characteristic and therefore maximizes correlation gain derived near the sample window discontinuities.

The boxcar averaging decimation filters implemented in the preferred embodiment are unitary scaled at the window discontinuities. In the frequency domain, this is a sinc function, which is characteristic of a transfer function of the decimation filter, having a roll-off that is a function of the decimation frequency. Because the transfer function will have a rounded shape, signals that are not centered in the middle of the transfer function will be attenuated by an amount corresponding to a frequency offset error imparted on the transmit signal by the inaccurate frequency reference employed by the transmitter while forming and transmitting the signal.

The present embodiment reduces the effects of decimation loss as a way to keep from incurring as much as 3.9 dB loss for transmitters that have a significant frequency offset error that place the transmitted signal at the edge of the detection bandwidth, Nyquist band edge. Several approaches for addressing the decimation loss (due to a filtering effect) are discussed below.

Digital Frequency Correction and Downconversion

Curve 1402 in Figure 14 represents how a frequency uncertainty error imparted on the received signal will reduce a signal power in an initial downconversion and decimation operation. Suppose the frequency of the transmitted signal is close to the Nyquist band edge, (i.e., at a left hand side or right hand side of the "transmitter frequency uncertainty range", as illustrated) the receiver will suffer a 3.9 dB loss in signal power, which, among other things, will inhibit the receiver's ability to align the signal. After the alignment is performed and the frequency error is determined (as will be discussed), a correction is then made to the downconversion tone so as to shift the frequency of the receiver by ± ½ the frequency uncertainty. As explained below, the effective signal loss of the transmitter will then be represented by either curve 1404 or 1406 depending on whether the signal is shifted up or down in frequency.

Once the processor determines that the transmitter frequency error exceeds at least 50% of the decimation bandwidth, the downconversion tone is altered by ± 50% of the Nyquist bandwidth, which moves the desired signal from the center to 50%. The resulting effect is that depicted in Figure 14 of moving the decimation center by ± 50% where it can be seen that the worst case decimation loss is limited to .9 dB. This shifting operation recovers 3 dB at band edge relative to using the center channel alone.

The added step of altering the digital downconversion tone adds complexity to the receiver because the downconversion coefficients become a complex tone sampled at the ADC rate. The sign of the tone is a function of whether the I component leads or lags the Q component. Preferably, the tone should be

50% of the decimation bandwidth so as to limit loss to .9 dB. However, a tone close to .9 dB will yield similar results and may improve computational efficiencies in performing the downconversion. By choosing the tone to be evenly divisible into the data sample set, the coefficient set may be represented by only a portion of the cycle. For example, 252 data samples would be collected if the sample rate were 4 times the chip rate for a 63 chip sequence. The sample rate is approximately 4.8 MHZ, so a downconversion tone equal to Fs/4 would repeat every 4 samples, thus the coefficient set need only be 4 samples long. Only ¼ cycle of the downconversion tone need be stored as coefficients since the I and Q processes access the same coefficient set in offset sequence. The order and the sign of coefficient retrieval completes the downconversion coefficient set with the only restriction being that the ¼ cycle must divide into the data record by an integer.

Frequency Offsetting the 1st Local Oscillator

A second approach for correcting the frequency of an incoming signal is to adjust the downconversion frequency in the 1st local oscillator. This is accomplished by programming the conventional LO synthesizer of Figure 8 to a new frequency.

Changing the Decimation Filter

Yet another method to reduce decimation loss is to increase the computational complexity of the digital signal processing IF filter. Rectangular window time averaging is used up to the final decimate-by-2 stage and in this stage a sinc time response FIR filter is used which has no appreciable decimation loss. On the other hand, the FIR filter approach increases the computational load and potentially requires a more costly, and more power consuming digital signal processor.

Improving Trip Sensitivity to Overcome Band Edge Decimation Loss

The synchronization search process is modifiable in yet another method for reducing frequency uncertainty decimation loss. In the previous discussion the digital or RF/IF frequency correction was made following initial search and trip determination. As demonstrated in Figure 14, there exists a significant loss of signal power at the frequency uncertainty band edge. This loss also has an adverse impact for signal detection. The previous discussion makes the assumption that the signal can first be detected and roughly located so an appropriate correction be made to limit the loss for demodulation. It is often true that signal detectors are more sensitive than demodulators, yet it is preferred that the detection process have the same signal-to-noise ratio (SNR) advantage as the demodulation process.

The detection process is enhancable by incorporating the techniques discussed above into the search process. One method for improving detection at band edge is to subdivide the frequency uncertainty band into a set of center frequencies which set the worst case loss for decimation loss at tolerable limits. In the present invention as depicted in Figure 14, only two bands are necessary to maintain worst case loss to .9 dB. Lines 1404 and 1406 represent 2 center frequencies which will perform this task. The search process simply makes an adjustment, alternating between these two candidate frequencies. As before, frequency selection can be made either in the digital downconversion or in a RF/IF downconversion step. The signal leader (or preamble, as will be discussed) or synchronization interval needs to have sufficient duration for all candidate frequencies to be evaluated.

Alternatively, both lobes may be simultaneously performed, the two lobes being depicted in Figure 14. In this method, downconversion must be performed digitally to re-use the sampled data twice or however many times is necessary to limit the decimation loss to system requirements. This method trades off computational loading for sensitivity in that the initial decimation process and search function must be duplicated.

Upon a trip (i.e., synchronization detection) in one of the redundant search processes, the other is suspended and data demodulation proceeds from the offset which produced the trip so as to save computational loading.

Another method for improving band edge sensitivity is averaging, which as discussed later herein, is a technique for improving sensitivity across the predetection bandwidth, including the frequency uncertainty band edge. Optimal sensitivity can be achieved using averaging, band limiting and frequency adjustments as discussed above at the cost of system complexity, transmitted duration and receive algorithmic loading.

In systems where sampled limiters are used, the signal amplitude information is stripped, and thus, except for signals which are at the same relative power as thermal noise, all signals appear in the final correlation function at the same relative power level. Because of this, a simplified threshold mechanism searches only the maximum and compares it to an absolute threshold, thus skipping a noise estimation process.

Fast Serial Search

Following sampling, downconversion to baseband, and initial decimation, correlation of the signal must be achieved. Correlation could be accomplished in the first RF mixer by combining the downconversion tone with the PN code. However, this approach would prohibit the use of the fast search algorithms disclosed herein, and would require the RF front-end 905 to remain on. More preferably, the

correlation (or despreading) task is performed in software at the minimum frequency possible, namely the chipping rate.

Direct sequence receivers align the receiver PN code with the transmitter PN code (as represented in the received signal) in order to realize the process gain. This search process can be performed serially by evaluating a sampled data set with respect to a given receiver code phase, stepping the code phase by one chip, and repeating the process until a power increase is noted. Since the information provided by the correlation function is relevant for only a 1 chip width of the PN code, the correlation process must be repeated so as to cover each possible chip location. Because the code length in the present embodiment is 63 chips long, a serial search approach would require as many as 63 steps before alignment is attained.

So as to assist in code alignment, the transmitter transmits, as a first part of the direct sequence spread spectrum signal, a leader which is a repeated copy of the PN code. Figures 15A-B help illustrate this alignment process, where Figure 15A depicts the transmitter power over time. For an ASK data modulation (such as on-off-keying for binary channel symbols), the transmitter keys-on at a time 1502, dwells for a time corresponding to the leader, where the transmitter repeated sends copies of the PN code, and then transmits the ASK data at a time 1504.

Figure 15B depicts the received power developed in the receiver corresponding to the transmitted signal. An increase in transmitted power is detected at point 1506. Signal correlation is achieved at point 1508, which is the initial trip event. Because the search process steps in one chip increments (or multiples thereof), the resulting trip alignment up to point 1508 will be within ½ chip. This degree of alignment is insufficient because a ½ chip offset error represents a 6 dB process gain loss. Consequently, to improve performance by further limiting alignment loss, a fine search process follows the course search so as to resolve the code misalignment to within a small fraction of a chip, which is accomplished at a time 1510. Once fine search is performed, the receiver waits until a time 1512 to begin receiving the ASK data.

Regarding the coarse search process, the present embodiment uses the fast serial search to achieve initial trip. This approach offers a preferred trade-off of performance versus computational complexity in the first embodiment. The fast serial search operates in the receiver in the time domain by collecting and storing one code repetition interval (i.e., one portion of the leader that corresponds in length to a PN code repetition). At the beginning of the coarse search process, the receiver initiates a real-time clock and then sequentially steps the PN code in one-chip steps against the collected and stored data until the portion of received signal has been correlated with all 63 code positions. At the end of the process, the maximum correlation power is determined along with the associated phase position of the PN code that generated the maxima. For systems that use an ADC, the trip condition would require that the maximum value exceed the average of the remaining values by a predetermined threshold. For systems that use a sampled limiter, the trip condition may optionally use a predetermined threshold because systems with a sampled limiter are

amplitude indifferent. The real-time timer is used during the process to count the passing of code intervals so the receiver can resume collecting data at the chip position which produced the maxima, thereby maintaining correlation for a subsequent sample.

This fast serial search process has several key advantages for digital receivers as implemented in the present invention. Because the receiver only collects one code repetition, the RF front-end may be powered down during the subsequent DSP search, saving battery life. Also, the physical collection of data as described in the serial search consumes much of the processors computational bandwidth. By halting the collection process, the computational bandwidth is recovered in the present invention. Even with low-cost DSP processors, the search time is reduced from 63 code periods to approximately 10. The transmitter leader can therefore be reduced, extending transmitter battery life.

To be most effective, the fast serial search, or other search, is performed in less than ½ the time required to transmit the leader so as to ensure detection by the receiver. Moreover, assuming that a first sampled bit was collected immediately before the key-on of the transmitter, i.e., time 1502 in Figure 15A. The receiver's search process will not report a trip event because the receiver's locally generated PN code will be compared to an incomplete portion of the transmitters PN code contained in the leader. Under these conditions, if the receiver spends more than ½ the leader transmit time performing the search, the next portion of the leader sampled by the receiver would lie past a mid-point of the leader, and thus the receiver would once again fail to synchronize with the transmitted signal because the receiver would be attempting to correlate based on a portion of the transmitters PN sequence, contained at the end of the leader, and a beginning portion of the ASK data contained in the transmitted signal. Moreover, the new search would extend into the data section of transmission and the receiver would not be ready to demodulate.

Figure 16 is a flowchart explaining the steps performed in the fast serial search process. The process beings in step 1605 and proceeds to step 1610, where a data record corresponding to a PN code length is captured and stored in memory. The process proceeds to step 1615, where an initial PN sequence phase is set to zero. The data sample is correlated against the current PN sequence and the result is stored in step 1620; subsequently, the PN sequence phase is incremented by one in step 1625. A decision block is performed in step 1630 wherein the process determines whether or not the data sample has been correlated against all possible PN sequence phase positions. If the data sample has not been correlated against all possible PN sequence phase positions, the process returns to step 1620 to correlate the data against the next PN phase position. If the data sample has been correlated against all possible PN sequence phase positions, the process continues to step 1635 wherein the maximum value of the 63 correlation calculations is determined. The process proceeds to step 1640, where the two largest power values are ignored and an average power value is calculated from the remaining 61 values. Step 1645 compares the maximum power value with the average power value. If the maximum value exceeds the average value by

the trip threshold, the process proceeds to step 1650 wherein a trip event is declared and the fine search and demodulation process begins. If the maximum value does not exceed the average value by the trip threshold, the process returns to step 1610 to sample and store another code period of data.

Searching over all 63 code phases prior to making a trip decision provides maximum sensitivity, minimizes the likelihood of failing to detect code alignment, and reporting false trip events. Also, alterative steps include stepping the PN code relative to the data, data relative to the PN code or both, because the relative phase positions is the relevant information sought in the correlation process.

Fine Search

If the coarse search process yields a trip event, the degree of alignment will be within ± ½ chip of the optimum code phase alignment because the correlation peak is only one chip wide. (If the chip offset were greater than ½ chip, then the adjacent relative phase alignment would result in a higher correlation result). However, as previously discussed, even fractional code misalignments can result in significant signal loss. For optimal performance, the receiver aligns the two spreading codes as closely as possible, therefore maximizing the signal strength of the received spread spectrum signal.

So as to more closely align the two spreading codes, the receiver of the present embodiment initiates a fine search process wherein the receiver changes the spreading code by fractional chips and attempts to establish a better code alignment. The processor (ASIC, PLD, microprocessor, or other signal processing apparatus) slips or advances a single sample by 1/4 chip intervals. Because the processor executes several instructions per sample interval, a fraction of the 1/4 chip step is achieved by hesitating instruction intervals combined with slipping samples. In the preferred embodiment, the processor controls the sample clock to the ADC, so that the processor executes 4 instructions per sample. Therefore, the processor can affect a slip of the locally generated PN code relative to transmit PN code (as represented in the received portion of the leader) by 1/16 of a chip by inserting a single NOP instruction into the bit-time processing loop.

Figure 17 shows a "real world" fine search process, to be contrasted with the ideal correlation process discussed in reference to Figure 7. The solid triangular line 1705 represents the ideal correlation peak, and the vertical lines 1710 at each fractional chip phase position show the potential signal drift due to instantaneous noise. The dashed line 1720 shows an example of a fine search process in the presence of noise. Conventional fine search algorithms, correlate each relative code position with the data sample, and then choose the code position that generates the highest signal level. In Figure 17, such an algorithm will result in a ¼ chip error, resulting in a mean 2.5 dB signal loss; the error will resulting from the process detecting that correlation occurred at position 1730 rather than 1725. The standard deviation of the noise becomes a significant factor in identifying the true correlation peak. More particularly, a larger standard

deviation noise will cause the lengths of the vertical lines 1710 to increase causing greater numbers of correlation errors in the serial fine search process.

A conventional method to overcome the effects of instantaneous noise is to dwell on each fine search position for more than one code period and average the values. However, a disadvantage to this method, for battery operated applications, is that increased amounts of transmitter leader time is required to obtain enough samples to average.

A goal of the fine search algorithm in the present embodiment is to obtain the best possible spreading code correlation as quickly as possible. To do this, the receiver of the present embodiment dwells on each fractional spreading code position for only one code period, but does not select the strongest signal out of the data set. Rather, the present fine sync process uses both chip offset and correlation strength of the entire data set to determine the ideal code alignment. Preferably, application of a center of mass operation on this entire data set improves fine search accuracy. Alternative operations including least squares, curvefitting and convolution may be used, but are less computationally efficient in the present application. By employing the center of mass operation, artifacts of noise are suppressed without having to dwell on each chip position multiple bit times. The function employed in the center of mass operation is represented by:

$$\overline{X} = \frac{\sum m\overline{x}}{\sum m},$$

where $\overline{X}$ is the x-coordinate of the center of mass, $\overline{Xx}$ is the x-coordinate of the relative chip position, and m is the linear signal strength (mass) at each relative chip position.

Figure 18 shows the results of three different search processes evaluated over several hundred fine search passes on real data containing noise. These processes slip the phase position of the receiver despreading code by 1/5 chip steps, and seven discrete positions are used (-3/5, -2/5, -1/5, 0, +1/5, +2/5, and +3/5). Because the initial trip can occur within ½ chip of the transmitted spreading code, the respective processes at least include data from –½ chip to +½ chip of the trip position. Also, the processes may utilize any fractional value, keeping in mind that smaller fractional positions may yield a better result but will require more data samples as well as require more computational power.

The "Peak 7" process searches the 7 different chip phase positions and selects the maximum signal value. The "Peak 7" line 1810 depicts the results when the maximum signal strength value is selected from the 7 chip positions. Note that even though the initial trip sometimes occurs at the best possible code alignment, the fine search process will, on the average, result in a 1.5 to 2.0 dB loss in received signal. This process has been previously implemented.

Inventive methods described as "CM 7" and "CM 7+" algorithms have an effect of averaging out the noise of 7 bit times without dwelling on each chip position for 7 bit times. The "CM 7" process calculates the center of mass of the 7 different chip positions and selects the chip value which coincides with the center of mass. This process works well if the initial trip is within 1/5 of a chip of the ideal relative code phase position. However, if the initial trip is greater than 1/5 of a chip from the ideal position, the correlation loss becomes severe, as seen at the end points of curve 1820 of Figure 18. This shortcoming is addressed in the CM7+ process, explained below.

The "CM 7+" process is a conditional two-step process. If the initial trip and subsequent center of mass calculation results in a fine search adjustment of less than 1/5 chip, then the condition is satisfied. If, however, the center of mass calculation shows that the initial trip error was greater than 1/5 chip, then the process moves the trip location by 2/5 chips, collects new data points out to 1 chip from the initial trip position, and re-calculates the center of mass, by re-using 5 of the first correlation sums. The fine search error results in less than a .75 dB loss, as seen on curve 1830 of Figure 18.

Steps in the "CM 7+" algorithm are explained with reference to Figure 19 where the method begins in steps 1905 and then 1910, where an initial PN sequence phase is set to the initial trip phase minus 3/5 of a chip. The process proceeds to step 1915, where one code period of data is taken and stored. The data sample is correlated against the current PN sequence and stored in step 1920; subsequently, the PN sequence phase is incremented by 1/5 of a chip in step 1925. A decision block is performed in step 1930 wherein the process determines whether or not the data sample has been correlated against all seven fractional phase positions. If the data sample has not been correlated against all fractional code chip phase positions, the process returns to step 1920 to correlate the data against the next phase position. If the data sample has been correlated against all fractional phase positions, the process continues to step 1935 wherein the center of mass calculation is performed. The process proceeds to step 1940, where the center of mass result is compared against the initial trip value. If the center of mass indicates that the fine search position is within 1/5 of a chip of the coarse search position, then the algorithm proceeds to step 1945 to begin the demodulation process. If the center of mass indicates that the fine search position is more than 1/5 of a chip away from the coarse search position, then the algorithm proceeds to step 1950, where the algorithm recenters the trip location by 2/5 of a chip, collects new data points, and recomputes the center of mass. As stated earlier, other algorithms such as least squares, curve fitting, and convolution can also be used to implement this fine search technique.

Center of Mass 9

A variant of the fine sync process uses the decimation process to acquire a minimum of data points and gives a reasonable trade-off between accuracy and computational loading. Upon an initial trip event identified from the coarse search process, the initial code phase will be within ½ chip of the ideal code phase position. The process, as described below, uses a sample rate (Fs) at 4x the chipping rate.

Once a data sample is acquired, it can be correlated against different phases of the spreading code, and, if not decimated, the data sample can be correlated against all fractional code phase positions, provided that a fractional resolution of the spreading code equals the sampling rate of the data. This approach requires storage of a single data sample with a duration equal to the code repetition. The initial downconversion and decimation process is performed prior to despreading and the result is a data set containing one element for each chip of the spreading sequence. This data set is used in coarse search where all possible combinations of the phase of the spreading code are used to determine if a trip event occurs, and thus the coarse search step resolution is in integer chip steps.

The receiver of the present embodiment re-uses the decimation process in the fine search process. Multiple data samples are taken at fractional phase offsets so as to calculate the correlation power over the correlation peak. This center of mass 9 process is explained with reference to the flowchart of Figure 20. The process begins in step 2005 and then block 2010 where a first data sample is acquired at a 4:1 multiple of the chip rate and then decimated to the chip rate. This data sample is correlated three times in block 2011 with the spreading code at −1, 0, and +1 chip offsets from the initial trip position. In step 2012, the spreading code is adjusted by +¼ chip from the initial trip phase position. In block 2020 a second data sample is acquired and then decimated to the chip rate. This data sample is correlated twice in block 2021 with the spreading code at −¾ and +¼ chip offsets from the initial trip position. In step 2022, the spreading code is adjusted by +¼ chip from the previously sampled phase position. In block 2030 a third data sample is acquired and then decimated to the chip rate. This data sample is correlated twice in block 2031 with the spreading code at −½ and +½ chip offsets from the initial trip position. In step 2032, the spreading code is adjusted by +¼ chip from the previously sampled phase position. In block 2040 a fourth data sample is acquired and then decimated to the chip rate. This data sample is correlated twice in block 2041 with the spreading code at −¼ and +¾ chip offsets from the initial trip position.

In block 2050, the center of mass calculation is performed on the correlation results from the −1, −¾, −½, −¼, 0, +¼, +½, +¾, and +1 code phase offsets. This calculation is used in step 2051 to establish the code position to receive and demodulate data in block 2052.

An alternative process that does not use initial decimation, but rather stores the entire data sample array. This method is explained with reference to the flowchart of Figure 21 where the algorithm begins in step 2105 and then 2110 where a data record is acquired at a multiple of the chip rate and stored for re-

use. The process continues in step 2111 where this data is despread and power measurement determined for five relative code chip offsets of –½, -¼, 0, –+½, +¼ chips where the 0 chip offset equals the initial trip phase. In step 2112, the center of mass is calculated on the correlation results from the –½, –¼, 0, +¼ and +½ chip phase offset power measurements. From block 2115, if the initial center of mass calculation is within ¼ chip from the initial trip position, the process proceeds to block 2140 wherein the relative phase of the receiver code generator is adjusted to the center of mass value. From block 2120, if the center of mass calculation yields a miss distance greater than –¼ chip from the initial trip position, the algorithm proceeds to block 2121 where the original data signal is despread and power measured for -¾ and -1 chip offset. In block 2122, the center of mass is calculated on the correlation results from the –1, -¾, -½, -¼ and 0 chip phase offset power measurements. The process then proceeds to block 2140 where the relative phase of the receiver code generator is adjusted to the center of mass value. From block 2130, if the center of mass calculation yields a miss distance greater than +¼ chip from the initial trip position, the algorithm proceeds to block 2131 where the data signal is despread and power measured for +¾ and +1 chip offset. In block 2132, the center of mass is calculated on the correlation results from the 0, +¼, +½, +¾ and +1 chip phase offset power measurements. The process then proceeds to block 2140 where the relative phase of the receiver code generator is adjusted to the center of mass value.

In some applications it is beneficial to simplify the processes, either due to memory restrictions for holding code or to take advantage of a processor's pipelined architecture. Thus, alternatively, steps 2115, 2120, and 2130 may be removed from the process, although in this variant all possible data points must now be calculated. This alternative process is explained with reference to Figure 22 where the process begins in step 2205 and then 2210 where a data record is acquired at said multiple of the chip rate and stored for re-use. The algorithm proceeds to block 2211 where the data is despread and power measured determined for nine relative code chip offsets of –1, -¾, –½, -¼, 0, +¼, +½, +¾ and +1 chips where the 0 chip offset equals the initial trip phase. In block 2212, the center of mass is calculated on the correlation results from the –1, -¾, -½, -¼, 0, +¼, +½, +¾ and +1 code phase offset power measurements. The process then proceeds to block 2240 where the relative phase of the receiver code generator is adjusted to the center of mass value.

Receiving OOK Data in a Hard-Limiting DSSS Receiver.

On / Off Keyed (OOK) systems, a subset of ASK modulation systems, use OOK modulation to format transmitted messages, and rely on an ability of the receiver to detect the presence or absence of energy coincident with particular bit (or symbol) times. This is the extreme case for amplitude modulation where data is encoded linearly or at discrete amplitude steps relative to a peak value.

Hard-limited receivers are not typically used for ASK systems because hard-limited receivers use a detection mechanism that inherently strips the amplitude information from the signal. Thus, hard-limited systems are mostly used in phase or frequency modulated systems, where the data information is encoded in the phase of a carrier. Nonetheless, because of the hard limiting receiver's wide dynamic range, it is desirable to use it in a low-cost receiver to receive transmission from an OOK transmitter.

A transmitter feature of the present embodiment implements on-off-keying by imposing a requirement to not only amplitude attenuate the signals during a "0" state, but also suspend the PN code generator used to spread the transmitted signal as shown in Figure 25, 2510, 2552. In turn, the receiver that uses a hard-limiter will not notice the amplitude key but it will be able to use the code on / code off aspect to make a determination between correlation sum and no correlation sum. The bit state determination is therefore a function of the ability to produce process gain in the receiver.

Because the receiver is relatively indifferent to amplitude changes, it may seem reasonable to modulate only by employing code on / code off, but not varying a power. However, it is presently identified that systems operating near power per unit bandwidth restrictions should not use this approach because removal of the code will cause the transmitted narrow band signal to have a higher peak power roughly equal to the process gain. Otherwise, a combination of amplitude and code keying is desired to create a OOK transmitter which operates at controlled power spectral density.

Scalable Signal Acquisition and Synchronization

The present invention has scaleable embodiments that allow for increased system improvement for increase processing power and, perhaps, battery power. Accordingly, the several approaches discussed herein, in some instances, are specialized algorithms to acquire, synchronize, detect a trip condition and subsequently demodulate data using the least amount of computational resources. Processes that appear to be equivalent in function must be compared based on their computational efficiency, and related power draw for a particular application. To this end some processes disclosed herein may appear to be less elegant than known algorithms, but, as is often the case, these known, conventional algorithms presuppose that a certain amount of processing resources and power is available.

Top Level Receive Algorithm

Figure 23 is a flow chart of a top level receiver signal acquisition process, which is applicable to a battery mode of operation where "time to search" is triggered by a wake-up interval timer. The process of Figure 23 is also applicable to continuous search receivers that stay on line continuously where "time to search" merely is a start point in a continuous loop.

The process begins in step 2305 and then step 2310 where the receiver samples and stores one code period of data. Subsequently, the process proceeds to step 2315 where the antenna and/or frequency settings are selected for the subsequent search to allow for settling in the VCO, as will be discussed in reference to Figure 27. Alternatively, if averaging is used, these steps may be delayed until the last sample is taken so as to complete the average. The decision to perform antenna or frequency selection is an optional step and depends on the specific system requirements and architecture. The process continues at step 2325, where a coarse search process is performed. Coarse search may be any of the fast search methods discussed previously, or any known methods.

If time-averaging is used, the process continues to step 2330 through branch 2331 and then branch 2333 is taken, where the steps of 2310 and 2325 are repeated until the proper amount of data has been sampled, stored, and averaged. Averaging is implemented on a single antenna and frequency setting; therefore, step 2315 is not repeated in the averaging algorithm. When sufficient data samples have been taken, control is passed through branch 2332 to decision block 2335 where a trip decision is made based on the process depicted in Figure 28 . If a trip is detected, then the receiver performs the fine search and demodulation processes in step 2340, where the fine search operation uses a center of mass algorithm discussed previously or other known methods. Subsequently, the process proceeds to step 2345, where the process decides whether or not to enter into sleep mode, based upon the receiver type. If the receiver is battery powered, the receiver will either go into sleep mode in step 2350, or return to step 2305 to repeat the signal acquisition process. If the receiver is externally powered, the receiver returns to step 2305. If in step 2335 a trip is not achieved, the process proceeds to step 2355 where the receiver verifies that the acquisition process has been performed for all possible antennas and frequencies. If not, the process returns to step 2310 to collect new data and select another antenna (if necessary) or another frequency (if necessary) 2315. From step 2355, the process proceeds to the sleep decision step 2345 only if all possible antennas and frequency values have been searched.

Many possibilities exist for a specific path followed in process of Figure 23, depending on system requirements, transmitter leader length and averaging options. Nonetheless, the flexibility afforded by the scaleable approach for acquisition, trip and demodulation based on system requirements is evident.

Spatial Diversity (Antenna Diversity)

The present transceiver includes redundant receive antennas 901, 903 (Figure 9) so as to offer recourse in overcoming signal fading or shadowing by allowing the antennas 901, 903 to be physically separated and/or orthogonally polarized. The receiver utilizes the antennas 901, 903 in acquisition to select the channel with greatest power for demodulation. Figure 24 depicts the antenna selection process, assuming the coarse search process has already been performed. The fine search process is complete with

an optimal phase position calculated at time 2405 and verified at time 2410, all of which being performed using the same antenna. At time 2415, the alternate antenna is evaluated for reception, using the same PN phase that was selected at the end of the fine search process. If the received power on the alternate antenna port (i.e., the opposite port to the primary port on which trip was determined) is greater than that of the primary port, the alternate port is selected and demodulation begins during interval 2430. The process is also repeated at various points throughout the data collection during bit periods where known symbols are expected.

Frequency Diversity

To maximize data throughput, transmitters and receivers must overcome the effects of jammers. Many systems use time diversity, or data redundancy, to overcome the effects of instantaneous jammers. Continuous jammers, or jammers which maintain the same frequency output over long periods of time, are unaffected by time diversity tactics and must be circumvented by other techniques. Systems that use frequency diversity by way of frequency hopping exist, but require the additional components, control, cost and power associated with an agile frequency synthesizer.

As will be discussed below, the transceiver of the present embodiment uses a frequency diversity scheme in an economical manner that does not force the requirement of a frequency synthesizer in a compatible transmit-only or transceiver device.

Transmitter and Frequency Diversity

Figure 25 is a block diagram of a DSSS transmitter that may be used to communicate with the receiver of the first embodiment or may be in the transmitter portion of a transceiver according to the first embodiment. In Figure 25, the transmitter includes a frequency reference source 2502, which is low cost crystal having accuracy of 50 ppm (parts per million) error. This example shows one frequency reference for the entire transmitter. clock divider circuit 2504 produces a code clock signal 2506 for a data generator 2508 and a PN generator 2510. The data generator 2508 is implemented by a microprocessor, external source or other data source. The PN generator 2510 is also implemented, although it does not have to be, by the same device as data generator 2508. A Clock divider circuit 2512 produces a diversity clock signal 2514, which is an integer multiple of the code clock 2506. The frequency diversity enable signal 2516 controls switch 2518 (implemented as an AND gate), either producing a logic "0" (2520 with diversity disabled) or passing the diversity clock signal (2522 with diversity enabled).

The data generator 2508 generates a binary data stream 2524 at baseband and is combined with the PN code 2526 in the XOR gate 2528 so as to produce a waveform spectrum 2530, also at baseband.

With frequency diversity enabled, the baseband signal is mixed in a second XOR gate 2532 with diversity enable signal 2522 and low-pass filtered 2534 to produce a signal with spectrum 2538. With frequency diversity disabled and signal 2520 held at a logic "0", the second XOR gate 2532 and LPF 2534 serve as a buffer, producing a signal with spectrum 2536, which is identical to the signal with spectrum 2530.

The output of frequency source 2502 is upconverted in upconverstion circuit 2540 to produce an RF carrier 2542 with a center frequency of about 915 MHZ (plus the frequency error of 2502 multiplied by the upconversion factor of 2540). With diversity disabled, the signal with spectrum 2536 is combined with the carrier 2542 in mixer 2544. This product is band-pass filtered in 2546 to produce a signal with single sinc spectrum 2548 with a center frequency of about 915 MHZ. This signal is amplified at 2552 and transmitted from antenna 2554.

With diversity enabled, the signal with spectrum 2538 is combined with the carrier 2542 in mixer 2544. This product is band-pass filtered in 2546 to produce a signal with dual sinc spectrum 2550 with a center frequency of about 915 MHZ. This signal is amplified at 2552 and broadcast on antenna 2554.

If frequency diversity is enabled, the generated signal will be as depicted in Figure 26B, with dual images 2601 and 2602 centered at about 915 MHZ. The signal power of either lobe of this signal is 3dB down from the power output of the signal from Figure 26A, because the signal power is now distributed in twice the bandwidth as the signal in Figure 26A. With frequency diversity enabled, the receiver may select from either of two frequency components from which to retrieve the data signal. As an alternative, the receiver performs signal searches at all three frequency values, using the algorithm from Figure 27 to cycle through all possible frequency settings. This approach assumes a transmitter that alternates, or coexists with other transmitters, between diversity (Figure 26B) and no diversity (Figure 26A).

The present receiver includes a select mechanism for selecting one of several receive frequencies. This mechanism is provided for two primary modes of operation. In the first mode, the receiver is tasked to use one of the available frequencies to select transmitters using that frequency band. This allows the receiver to be compatible with pools of transmitters separated by frequency to be selected through receive frequency tasking. The time to switch between frequencies is typically not critical in this mode of operation.

The second mode of operation is intended to capture a transmitter pool (i.e., a group of one or more transmitters) that transmit simultaneously at different frequencies using the previously discussed frequency diversity process. Such transmitters use this diversity technique where the signal is split and separated in frequency by a fixed amount. The receiver must monitor the two (or three) frequencies as part of the acquisition process. Because the frequency selection is integrated into the acquisition process, a timely transition between selection helps minimize transmitter leader time. This mode of operation adds diversity in frequency to increase the probability of data throughput in the presence of intentional or unintentional

interference and multipath propagation. If a static interference signal and/or a fade exists at one of the transmitted frequencies, the other frequency may be used to demodulate the data. The receiver of the present embodiment uses this technique to improve throughput, quickly alternating search frequencies while processing a previous captured bit interval. By pipelining the process, the frequency transition time can be absorbed thus minimizing the impact on search time.

Figures 27A-D depicts this receive acquisition schedule which includes the antenna and frequency diversity processes discussed above. Figure 27D depicts a transmitted signal and Figures 27A-C depict the receiver process used to acquire the signal. Figure 27A represents different candidate frequencies on which the receiver attempts to acquire the signal; Figure 27B represents the antennas on which the receiver attempts to acquire the signal; Figure 27C represents different samples obtained by the receiver and used by the receiver to determine if the transmitter is presently transmitting.

As shown in Figure 27D, the transmitter presents a leader (i.e., preamble) signal prior to data, where the leader is of sufficient duration to allow the receiver to evaluate all combinations of diversity provided for in the system architecture. As shown in Figure 27C, the receiver samples data at times 2735 for one code period then processes the data using the fast serial search process for a duration 2737, lasting several code periods. The leader is of sufficient length that allows for the receiver to perform successive searches which coincide with all diversity combinations used in the system.

By using the fast search algorithms taught, it is possible that a change in diversity at the transmitter will occur while the receiver is attempting to acquire the signal. Changes to the frequency or antenna may be made and a settling time for frequency change (shown at time 2715) therefore must be absorbed into the receiver's signal acquisition process, as will be discussed.

Time Domain Averaging to improve Coarse Search Sensitivity

Figure 28 depicts the benefit of averaging over successive correlation processes to improve acquisition sensitivity. Each coarse search 2812, 2814, 2816, 2818 produces a cross correlation of the received signal and the PN code embedded in the receive coefficients, with 2810 being the average value over the previous N multiple searches. This process requires that subsequent samples are phase coherent to each other, meaning that the time relationship of the first sampled data point in each code period is identical. This phase coherency is obtained using a timer and/or counted state processes to ensure zero relative code phase alignment. Only the frequency reference drift is left uncompensated, but this drift is low relative to the time interval of search.

The averaging is performed as a box-car or finite impulse response (FIR) filter structure where the last N symbols are averaged, or the averaging may be performed in an exponential or Infinite Impulse Response (IIR) averaging process where the previous results are decayed and added to a fraction of the

current sample. In the present embodiment, an exponential averaging process is used so as to minimize memory requirements because only the current sample plus one decaying average need be maintained. The weight "N", as shown in Figure 28, is 6 where the previous average is multiplied by 5/6 to decay the previous result, the current sample is multiplied by 1/6 and summed to the previous product. The result is stored for future decay and then passed to the trip decision process.

Figure 29 depicts the reduction in false alarm rate for averaging 6 samples in the present single channel receiver embodiment. Curves 2910 and 2920 show the power distribution of noise in a 115 kHz noise bandwidth with and without averaging, respectively. Curves 2930 and 2940 show the power distribution of a –110 dBm signal in 115 kHz noise bandwidth with and without averaging, respectively. Improvement is visualized by comparing a minimized overlap of distributions (2920 and 2940, and 2910 and 2930) which is a measure of false alarm rate and degradation in bit error rate. The mean power for the noise and signal plus noise distributions remain unchanged, yet the deviations are reduced creating a greater miss distance between the minimum "On" and the maximum "Off" distributions.

Averaging is only useful if coordinated with the leader length of the transmitter, and in the case of the present signal channel receiver embodiment, each coarse search operation takes less than 12 PN code intervals. Accordingly, averaging over 6 searches produces a maximum benefit after 72 code intervals. Because the leader length is 92 code intervals on the transmitter, this leaves 20 code intervals for fine search, AGC and overhead. In systems where the leader length must be reduced, the averaging time-base may be reduced accordingly. There is an asymptotic diminishing return on investment for averaging. Averaging two noise samples together reduces the noise deviations by 3 dB. To gain another 3 dB, the number of samples must be doubled to 4. Each significant reduction of noise deviations requires a doubling of time. The most effective average is, therefore, the first average and subsequent averages, while helpful, provide diminishing returns. Also, the improvement cannot exceed the mean signal to noise ratio (SNR) at the output of the bandpass filter preceding the magnitude computation.

While averaging can improve trip sensitivity to overcome the greatest portion of the 3.9 dB loss at maximum frequency ambiguity due to decimation loss, the system performance and cost is at odds according to a trade off of sensitivity for leader length in the transmitter and power/computation loading in the receiver.

Increased Data Rate Using Partial Code Correlation

A "scalable" feature of the present invention is an adjustable data rate. Data rate may be increased in the receiver while using partial decimation coupled with data modulation transitions in the transmitter that occur at fractional PN code boundaries.

A standard modulation method for transmitting data in the present inventive system is OOK where a data value "1" is represented by the presence of signal for a repetition of the PN code and a data value "0" is represented by the absence of signal for the same interval.

An alternative data modulation method is BPSK data where the signal is present for both "1" and "0" data symbols, yet the carrier phase is inverted 180 degrees to delineate the data state. In this data modulation method, the correlation sum will either sum positively or negatively depending on the arbitrary carrier relationship at acquisition. The data "1" is assigned the state during the preamble (leader) so that the PN sequence will be transmitted "in the clear". A Costas loop or other technique for translating the received phase normal to that of the phase detector is used to create a maximum data miss distance and therefore maximize SNR.

Alternatively, data is differentially encoded (DBPSK)which simplifies the incoherent reception problem. In a differentially encoded signal, the phase inversion event marks a data state where the absence of inversion marks the alternate bit state.

In either OOK, BPSK or DBPSK system, the data rate can be increased by creating artificial symbol boundaries within the PN code. The present transceiver system uses a 63 chip PN code length to represent a standard symbol, and therefore provides a data symbol (or data bit) rate of approximately 19.2 Kbits/second. The data rate can be effectively doubled by arbitrarily assigning the first 31.5 chips to one data symbol, and the second 31.5 chips to the second. The transmitter must perform the BPSK or DPSK phase inversion at the 31.5 chip boundary or amplitude key the signal, and the receiver must perform the correlation process by parts (i.e., treating the first 31.5 chips separate from the subsequent 31.5 chips).

Boundary conditions are relatively arbitrary and data rates may be increased at any fractional code interval provided the rate divides evenly into the code repeat rate or a multiple of the code repeat rate. For example, it may be desirable to send three symbols over two code repeat intervals. The transmitter and receiver need only have a synchronization method, or other prearranged agreement, to know when to expect phase inversion or keying of the carrier.

Regulatory restrictions (such as Federal Communication Commission, FCC, restrictions) may place a practical limit to this technique, because the regulations require a minimum process gain for systems to operate as a spread spectrum systems, which are allowed to use special signal bands. However, the process gain is typically specified at the data symbol rate, and thus, by dividing the 63 chip PN code by 2 effectively loses 3 dB of process gain for each symbol, and if the PN code is further divided, the system may no longer be entitled to "spread spectrum" status. Furthermore, the effect of the system process gain on other facets of the system also bear on increasing the data rate, including correlation loss due to filtering, sampled limiting or noise bandwidth.

Figures 30A-F depict a PN code repetition interval and the 63 chips collected at 4 times the chip rate, and respective symbol intervals at predetermined fractions of the 63 chips. A total of 252 samples represent the data collected for one PN pattern generated in the present invention. Assuming the data is correlated with the receiver PN code, Figure 30A depicts the maximum process gain available for a symbol rate equal to the code repeat rate resulting in 17.99 dB of process gain at a 19.2 kbits/sec data rate. Figure 30B depicts the maximum process gain per symbol for a symbol rate equal to twice the code repeat rate. This effectively doubles the data rate to 38.4 kbits/sec with a corresponding process gain maximum of 14.98 dB. Figure 30C depicts three symbols per code interval yielding a data rate of 57.6 kbits/sec with a maximum process gain of 13.22 dB. Figure 30D depicts four symbols per code interval yielding a data rate of 76.8 kbits/sec with a maximum process gain of 11.97 dB. Figure 30E depicts five symbols per code interval yielding a data rate of 96.0 kbits/sec with a maximum process gain of 10.97 dB. Figure 30E depicts six symbols per code interval yielding a data rate of 115.2 kbits/sec with a maximum process gain of 10.21 dB.

Beyond 6 symbols per code interval the process gains drops below 10 dB which is the minimum allowable process gain for spread spectrum systems operating in the 902-928 MHZ band per FCC regulations. However, aside from the FCC regulation, more that 6 symbols may be achieved, or even a composite of different symbol lengths may be used for certain applications or users that require greater data rates/or symbol rates. Similarly, adaptations to the receiver mechanisms may be made so that multiple PN codes may be used to lower data rate, but increase processing gain, and therefore, robustness of selected transmitted signals.

Frequency Tracking during Data Demodulation

Data demodulation may proceed after acquiring spreading code synchronization of the receiver to the transmitter. If the transmitter derives its spreading code sequence from the same frequency reference as its RF carrier, it is sufficient for the receiver to track the transmitter carrier so as to maintain spreading code synchronization throughout data demodulation. Also, to demodulate a phase modulated signal, it is preferred to remove the effect of the carrier frequency error between transmitter and receiver.

One way to remove the effect of the carrier frequency error between transmitter and receiver is to use conventional DBPSK demodulation augmented with frequency error correction. According to this approach, assume the received signal is despread, downconverted to baseband and decimated to a bandwidth greater than or equal to the frequency error as previously discussed. This is shown as 3100 in Figure 31 with 6 output samples C(n') 3105 per code period. Choi, Z. Y, Lee, Y. H., "Compensating Frequency Drift in DPSK Systems via Baseband Signal Processing", IEEE Transactions on Communications Vol. 45 No. 8, August 1997, pp 921-924, the contents of which is incorporated herein

by reference, discusses this technique using one sample per code period as unduly limiting the frequency range that can be corrected. A conventional DBPSK demodulator 3110 as taught in Frerking, M., "Digital Signal Processing and Communications Systems", Van Nostrand Reinhold, 1994, pp 433-435, 448-450, is shown in Figure 31. The bit rate being scaleable by the parameter L in the DBPSK demodulator 3110.

R (kbit/s)	L
19.2	6
38.4	3
57.6	2
115.2	1

In reference to Figure 31, a product of the present bit samples C(n') 3105 are multiplied by a complex conjugate of the previous bit samples and decimated to one sample C(n) 3115 in the DBPSK demodulator so as to convert the frequency error to a static phase error θ. The complex sample $C_\theta(n)$ 3125, whose angle is the static phase error θ, averaged over the previous M bits, is estimated in a decision feedback loop 3120. The static phase error θ is canceled before making the demodulated data bit decision bit(n) 3130 as shown in Figure 31, and is accomplished by multiplying C(n) by the complex conjugate of $C_\theta(n)$ and taking the sign of the real part of the product to make the bit decision bit(n) 3130. The $C_\theta(n)$ average is updated with C(n) multiplied by the sign of bit(n). This approach enables the conventional DBPSK demodulator to work in the presence of frequency error. The computational burden is low and does not increase the cost of the DSP over that required for an ASK data demodulator.

An alternative way to remove the effect of the carrier frequency error between transmitter and receiver is to null the error with an automatic frequency control (AFC) loop. Off-the-shelf components that implement the digital signal processor 3280, such as a DSP integrated circuit (IC), a general purpose micro-controller (uC) IC, general purpose digital logic, or a custom digital IC or any combination of these, can be adapted with appropriate software to implement the phase and/or frequency detector and loop filter.

A block diagram of a LO synthesizer using the DSP 3280 is shown in Figure 32. With the switch 3205 in position 1, the synthesizer includes a stable reference frequency source (such as a quartz crystal oscillator) which is the master clock for the DSP 3280, a downconvert despread and decimate function 3210 as previously disclosed, a frequency detector 3220, a loop filter 3230, a voltage controlled oscillator 3250 and feedback divider 3255. The output 3260 of the synthesizer is a signal at the desired frequency. A digital to analog converter (DAC) 3240 is placed between the loop filter 3230 and the VCO 3250 to provide an analog control signal to the VCO 3250. Low cost DACs 3240 are available in a dual 8-bit converter package where fine converter steps are set to 1/64 of the coarse converter steps. The loop filter algorithm 3230 first adjusts the coarse converter to the coarse frequency error 3232 and then the fine converter to the fine frequency error 3233 during frequency control loop settling.

After the LO is locked to the receiver frequency reference, the receiver is reconfigured by changing the switch 3205 to position 2 in Figure 32. The receive antenna 3201 feeds the conventional analog RF front end 3203 which includes an analog to digital converter (ADC) at its output. The downconvert coefficients in block 3210 are the computationally efficient Fs/4 set, as previously discussed, and thus a computational burden is minimal and may be shared by other receiver functions. The frequency locked loop drives the coarse and fine frequency errors 3232, 3233 between the transmitter and receiver and hence the decimation loss to zero.

Figure 33 illustrates part of a frequency detector implementation as was shown as the decimating frequency detector 3220 in Figure 32, and preferably uses the output of the digital down conversion operation, decimated to 12 samples per spreading code period. The formula

$$\omega = \dot{\theta} = \frac{I\dot{Q} - Q\dot{I}}{I^2 + Q^2}$$

is the well-known result that signal frequency is the first derivative of signal phase with respect to time. (The over dot signifies first derivative with respect to time.) The continuous time first derivative is approximated by the discrete time first difference 3320 as is known in the DSP art. For the frequency detector to function without error, a group delay of the first difference must be independent of frequency and must equal a group delay of the decimated I and Q samples. This is accomplished by the structure 3310 shown in Figure 33, where the values I_n are the I samples from block 3210. The 12 I and Q samples per code period are initially decimated by 2 as shown by the "+" sign in brackets combining adjacent I_n samples. Figure 33 is also representative of a similar structure for the Q samples. The computations may done as the I and Q samples are acquired so as to conserve DSP memory. When the frequency detector is preceded by a sampled limiter, the denominator term $I^2 + Q^2$, which is the signal power, is constant and can be set to one without loss of functionality. The formula

$$\omega = \sum_{6} (I\dot{Q} - Q\dot{I})$$

computes the frequency computation ω and the decimation by combining the intermediate results of 3310 summing over a code period. This causes the frequency detector to have the same noise performance as the data demodulators previously discussed.

Figure 34 is a block diagram of a very low cost DAC that includes a coarse 3401 charge pump and a fine 3403 charge pump (controlled current source) driving a capacitive voltage divider 3405. In this

DAC the output voltage is proportional to the charge on the capacitors. The "Charge Control" logic 3410 turns on a charge pump for a predetermined time interval required to deposit or remove a particular charge on the capacitors 3405. This produces an output voltage proportional to the frequency error 3415 computed by the loop filter. The charge estimate logic 3420 keeps track of the charge on the capacitors. To conserve power in a battery operated device, the power to the synthesizer is cycled on and off. During a power-off event, the estimated charge on the capacitors is saved in non-volatile memory. During a power-on event, the estimated charge is retrieved from non-volatile memory and used, as will be discussed, to replace the charge on the capacitors that was present prior to the power-off event. The recharge to estimate logic 3430 and the charge control logic 3410 restore the charge on the capacitors by driving the respective current sources 3401 and 3403 for predetermined periods of time corresponding with the estimated charge values stored in memory. Then the frequency locked loop is activated while minimizing the power-on settling time of the LO synthesizer because the charges where restored prior to the frequency locked loop becoming activated.

A third way to remove the effect of the carrier frequency error between transmitter and receiver is to control the first LO VCO 3250 (Figure 32) in a Costas carrier recovery loop for BPSK demodulation. This is shown in Figure 32 where the Costas phase error detector is substituted for the frequency detector 3220. The downconvert coefficients are the computationally efficient Fs/4 set. The computational burden is minimal and some of the diagram blocks in Figure 32 may be shared by other receiver functions.

A fourth way to remove the effect of the carrier frequency error between transmitter and receiver uses the Costas carrier recovery loop for BPSK demodulation. This shown in Figure 32 with the frequency detector 3220 replaced with a Costas phase error detector. The digital down conversion coefficients in conjunction with the downconvert and decimate function 3210 previously discussed in reference to Figure 32, form a numeric controlled oscillator (NCO). The DAC 3240 is fed a constant frequency setting and the loop filter 3230 outputs 3232, 3233 control the down conversion coefficients. Some of the diagram blocks in Figure 32 may be shared by other receiver functions. According to this approach the NCO must generate arbitrary frequencies for the downconvert tone so the computational efficiencies discussed previously may not be as prevalent.

A fifth way to remove the effect of the carrier frequency error between transmitter and receiver is to measure the frequency error using the frequency detector 3220 shown in Figure 32. An additional computation downconverts the decimated I and Q signals from downconvert and despread and decimate block 3210 to zero frequency error in a feedforward arrangement prior to DBPSK demodulation. These steps add computational complexity.

Multi Channel Receiver

A second embodiment of the present invention is directed to a multi channel transceiver, having a receiver and transmitter that provides enhanced system sensitivity and performance relative to the single channel transceiver of the first embodiment, although requiring additional digital signal processing power than the single channel transceiver of the first embodiment.

The multi channel transceiver contains several common components with the single channel transceiver of the first embodiment. In particular, the multi-channel transceiver includes the antennas 901, 903, RF front end 905, transmitter 929, associated antenna 931, and low performance receiver time reference 927 of the single channel receiver, as discussed in Figure 9. Differences, however, will be described with respect to the digital signal processing section 908 of the single channel receiver in Figure 9, and these differences, as well as other functions for enhancing performance, are discussed below.

As discussed, the single channel receiver compensates for a frequency ambiguity of the transmitted signal by using a 115 kHz predetection bandwidth so as to be assured of capturing the transmitted signal therein. However, as discussed previously, the wider bandwidth caused a sensitivity loss, as compared with a conventional receiver that does not attempt to compensate for transmitter frequency uncertainty and therefore uses a detection bandwidth that is commensurate in size to a signal bandwidth. Like the single channel embodiment, the multi-channel receiver (actually transceiver, but for simplicity referred to as a receiver) includes a baseband processing stage that is sufficiently wide to account for the transmitter frequency uncertainty range, although the multi-channel receiver offers improved sensitivity by further subdividing the frequency ambiguity bandwidth into smaller overlapping bandwidths, each of which match the bandwidth of the desired signal.

In order to determine which of the channels actually contains the signal, the multi-channel receiver includes a channel selection mechanism that selects one of a plurality of smaller bandwidths in order to acquire the spread spectrum signal and demodulate the data contained therein. The multi channel receiver, therefore, offers slightly better performance than the single channel receiver of the first embodiment because at least one of the channels will capture the signal, and that channel will have a bandwidth that more closely approximates a bandwidth of the signal.

The multi channel receiver uses a multi-bit ADC 3504 that serves the same function as the single bit converter in the single channel receiver, in that it digitizes the analog signal into a series of digital samples, however the ADC 3504 represents the digital samples in multi bit words for subsequent processing in the baseband processor. Because the ADC 3504 has limited dynamic range (i.e., a range from lowest signal representable by the ADC 3504 to the highest signal representable by the ADC 3504), an automatic gain control AGC mechanism 3502, as depicted on Figure 35, is used to adjust the incoming

signal from the RF front end (similar to the RF front end 905 of Figure 9) to fall within the dynamic range of the ADC 3504. Keeping the received signal within the dynamic range of the ADC 3504 prevents the signal from being "clipped" (i.e., causing the ADC to perform a non-linear operation on the signal) if the signal is too high, and prevents the signal from being "swamped" by quantization noise generated by the ADC 3504, if the received signal is too low. The AGC mechanism 3502 is shown as an adjustable attenuator having an AGC control input that is controlled by a processor.

Figure 35 also shows a quadrature downconvert and decimate operator similar to 909 in Figure 9, although processor 3530 depicts the mechanisms used for creating the downconversion and decimation coefficients used in the multi-channel receiver. Tone generator 3532 generates a tone at frequency (Fc) equal to an IF center frequency (Fc) of the received signal. The tone generator 3532 feeds phase shifter 3534 so as to impart a 90 degree phase shift and thus provide a quadrature tone. These in-phase and quadrature tones serve as I and Q downconversion tones for the incoming signal sampled by the ADC 3504. Each downconversion tone is mixed with the PN code generator 3536, which has been spectrally compressed with a filter 3538 and mixed in mixers 3540 and 3542 so as to create a downconversion and despreading coefficient table that is precalculated and stored in semiconductor memory in the DSP processor.

Mixers 3512 and 3522 perform the downconversion and despread process using the signal from the ADC 3504 and the quadrature downconversion despreading signal from the precalculated look-up table stored in memory. The resulting signal is a quadrature, baseband, despread signal passed to low pass filters 3514 and 3524 and decimated in downsampling operators 3516 and 3526 to lower the signal sample rate prior to DC (0 Hz) removal in DC removal mechanisms 3518 and 3528. The resulting signal is a despread downconverted and decimated representation of the sample signal received at the input of the quadrature downconversion, despread and decimation process.

The signal processing mechanism depicted in Figure 35 has sufficient processing power to perform either a slow serial search, or a fast serial search, as long as the data record for one code repetition interval is stored in memory and correlated against all possible combinations of the PN code generated locally in PN code generator 3536. To this end, the decimation efficiencies previously discussed may also be employed herein.

As shown in Figure 35, the sample rate (Fs) of the ADC is 6.0 MHZ which differs from the single channel sample rate of 4.8 MHZ. The preferred over sample rate of the multi-channel receiver is a 5:1 ratio relative to the chipping rate of 1.2 MHZ which sets the sample rate at a slightly higher frequency. The over sample ratio is immaterial to the operation of the device and only sets the requirements for the anti-aliasing filter preceding to the ADC. Accordingly, a subsequent description for the multi-channel receiver will be based on a 5:1 over sample ratio.

The present inventors have identified that by precalculating the hybrid coefficients, a coefficient lookup table may enable the downconvert, despread and decimate process to be implemented in very modest DSP components that are presently available.

The final process step depicted in Figure 35 is DC removal, and is performed by DC removal mechanisms 3518 and 3528 that remove undesirable effects of a voltage bias introduced at an analog signal side of the ADC 3504. By canceling this DC component, as discussed below, the present multi-channel receiver may use a low precision voltage reference at the ADC 3504, compensating in real-time in firmware. This further reduces hardware complexity and cost in realizable systems at a very small computational loading cost.

Analog to Digital Converter DC Removal

ADC devices typically have an AC coupled input with a voltage reference set by precision resistors and active components. Drift in the resistors due to aging and temperature will vary the reference voltage and center point, creating a DC bias in the incoming data stream. ADC bias on the signal will be interpreted as a CW jammer in the system, exactly centered in the IF, and will be translated to the Nyquist extremes (0 and Fs/2). This creates an elevated noise floor and will decrease radio sensitivity if left uncorrected.

Traditional DC removal techniques are implemented in firmware and calculate a mean of the sampled data and subtract the mean from each data sample. This process works adequately, yet requires that each data sample be acted on by a math function prior to any signal processing. This roughly doubles the computational loading for processing a data sample.

The present multi-channel receiver performs DC removal at a later point in the signal processing, removing the need to perform the math function at the sample rate. In reference to Figure 35, DC removal is performed in operators 3518 I and 3528 Q, not at point 3508, and thus performs DC removal on downconverted, decimated and despread samples. The multi-channel receiver performs a despread-and-decimate function on the raw data, reducing the number of samples by the decimation ratio of decimators 3516 and 3526 as shown in Figure 35.

The incoming data is preferably sampled at 5 times the chip rate such that 315 (315 = 63 x 5) samples per bit interval are collected and are subjected to DC compensation. The signal is decimated by 21 to produce 15 quadrature samples per bit period, yielding a Nyquist-bandwidth frequency uncertainty of 288 kHz, of which only 120 kHz is of interest. Removing the DC component from the input data following the decimation reduces the loading from 315 math operations to 30 (15 I terms and 15 Q terms).

Decimation often implements an averaging function, but instead of averaging, the decimation process can instead compute the sum. This introduces an error factor that will be proportional to 1/N

where N is the decimation ratio. For low-end processors, ignoring the divide-by-N to compute a true average may result in an overflow in the processor, but this can be avoided by judiciously scaling coefficients, or incoming data, or using sufficient bits in the accumulation process to hold the worst case sum. The decimation (summing) process can be expressed as 15 multiply-accumulate processes against independent data and coefficient sets. Each decimation block *I* can be expressed as:

$$DECOUT_I = \sum_{n=1}^{21} D_i(n)\, C_i(n)$$

where $D_i(n)$ represents 21 ADC data words and $C_i(n)$ represents the corresponding 21 coefficient words. The result is a scalar value representing one of 15 downsampled data points per I and Q processor. Because a DC offset value is present in the samples, the term $D_i(n)$ contains the sampled data plus a constant, A, added to each data point.

$$D_i(n) = D_i(n) + A$$

The decimation scalar is distorted by this constant, A, expressed as:

$$DECOUT_I = \sum_{n=1}^{21} [D_i(n) + A]\, C_i(n)$$

Because the coefficients are unchanging (stored in ROM), they can be treated as constants and the following simplification is possible:

$$DECOUT_I = \sum_{n=1}^{21} [D_i(n)\, C_i(n) + AC_i(n)]$$

$$DECOUT_I = \sum_{n=1}^{21} D_i(n)\, C_i(n) + A \sum_{n=1}^{21} C_i(n)$$

$$DECOUT_I = \underbrace{AK_I}_{\text{DC Removal}} + \underbrace{\sum_{n=1}^{21} D_i(n)\, C_I(n)}_{\text{Despread/Despread Block}}$$

The new constant K_i represents the sum of the coefficients for the decimation block. As the decimation block boundary is arbitrary, a non-zero mean for the decimation block acts as a multiplier for

DC offset if a correction is not performed. The product AK_i must be compensated within each decimation block if the computation is to be correct.

Each I and Q decimation block therefore has an independent K scalar multiplier that magnifies DC. A mean measure of the DC component is needed so as to complete the decimation correction. To this end, a number of random sampled data points are averaged for each bit interval to produce an estimate of the mean. More particularly, in the present embodiment, 16 random ADC data points per code period are averaged to compute a mean. The "code period" mean is then time-averaged over an the most recent 8 code periods to calculate a running approximation of A.

The summation of each decimation coefficient block (K_i) is computed at a compile time and provided as a lookup table. The time-averaged mean (A) is multiplied with each of the I and Q coefficient sums (K_i) to create 30 DC removal products (AK_i) which are subtracted from their respective I and Q decimation results.

Optimization of Coefficients and Implementation for Channelized Receivers

A final bandwidth in a receiver must match the information bandwidth to achieve maximum sensitivity. The present multi-channel receiver embodiment uses overlapped channel filters to achieve an optimal signal-to-noise ratio (SNR). The data sampled at the ADC 3504 is despread and partially decimated to a point where the decimated signal bandwidth is at least as great as the frequency uncertainty of the transmitter (greater to reduce decimation loss at band edge, as was discussed). The receiver next sends the partially decimated data into a bank of channel filters to complete the decimation process and make the decimation bandwidth equal to the signal bandwidth.

The channel filters may be implemented using a fast Fourier transform (FFT) or discrete Fourier transform (DFT), finite impulse response (FIR) filter or infinite impulse response (IIR) filter or other similar transform that band-limits the data signal. Figure 39 depicts the channel implementation method where channel filters are implemented using a DFT. By spacing the channel filters non-uniformly, the between-channel roll-off intercept can all be made to be equal in absolute power to achieve better performance across the entire frequency uncertainty of interest. Moreover, arranging the respective channel filters in the frequency uncertainty bandwidth in a way that the intercept points between any two channels is limited to a fixed number, say 1.5, dB, then there will be a lowered risk that the signal may be missed because it occurred in a "gap" between adjacent channels. For this reason, a DFT is preferred over an FFT because an FFT provides uniform channel spacing that is equal to the channel bandwidths. If an FFT is used, the between-channel roll-off adds 3.9 dB of loss to the decimation loss.

Signal processing efficiencies are realizable by using channel filters that are symmetrically spaced about 0 Hz. Because each channel filter is implemented as a complex vector multiplication, the negative channel

can be implemented using intermediate components of the positive channel, as will be expressed using complex (real and imaginary numbers) expressions. The input data stream may be represented as:

$$Data = A + jB,$$

where "A" and "B" represent vector components of sampled data. In this case, the vector holds 1 code period of sampled data partially decimated down to a sampling rate greater than 2 times the frequency uncertainty. The channel filter coefficient is a tone represented by the complex vector C + jD. The positive channel filter becomes the product of these two tones.

$$+CF = (A + jB) * (C + jD) = (AC - BD) + j(BC + AD)$$

The negative channel filter has the same offset frequency about 0 Hz as the positive channel filter. It therefore has the same coefficients as the positive filter, but the imaginary term is sign reversed represented as C – jD, and so the negative channel filter becomes the product of these two tones.

$$-CF = (A + jB) * (C - jD) = (AC + BD) + j(BC - AD)$$

While calculating each channel filter, the intermediate product terms AC, BD, BC and AD are temporarily saved. In the case of the 15-point channel filters implemented in the channelized embodiment, each product term represents 15 multiply-accumulate instructions. The total channel filter therefore takes 60 multiply-accumulate instructions, plus 2 add or subtract operations to complete a complex vector result. The negative channel filter need only perform the 2 add or subtract operations, thus saving the 60 multiply-accumulate instructions. The preferred embodiment employs this technique to maximize the number of usable overlapped channels. Adding more channels reduces the between-channel losses and more efficiently utilizes processor computational bandwidth. This technique enables the realization of many channels in a very modest digital signal processor.

Figure 36 depicts a signal processing mechanism that implements the above-described symmetrical channel filter efficiencies, for realizing a single pair of channel filters, symmetric about 0 Hz. Other mechanisms are used for calculating the other symmetrical channel filter pairs.

As seen in Figure 36, signals 3602 and 3604 represent the I and Q decimated data streams of a baseband signal. A frequency generator 3606 and delay element 3608 (i.e., a phase shifter) generate the frequency offset for both the positive and negative frequency channels. Multiply operators 36M1 through 36M4 generate the product terms 36P1 through 36P4 respectively by multiplying signals 3602 and 3604 with inphase and quadrature frequency offsets produced by frequency generator 3606 and delay element 3608, as shown. The product terms 36P1-36P4 are decimated by lowpass filters 36F1 through 36F4 and then decimated by 15 in the downsampling elements 36D1 through 36D4 so as to produce the signals AC, BD, BC, and AD. The signals AC, BD, BC, and AD are then either added or subtracted in elements 36A1 through 36A4 to produce the intermediate values that will be used to determine the signal power in the respective symmetric channel filters. These intermediate values are squared in squaring operators 36S1

through 36S4 and then combined in adders 3614 and 3616 to produce both the positive and negative channel filter outputs for a particular frequency offset.

Similarly, computational efficiencies are realized in the implementation of the center channel filter (i.e., 0 Hz offset). The center channel filter is the most straight forward to implement because it may be noted that for a 0 Hz frequency offset, as noted in Figure 36, the quadrature component of the sinusoidal transform may be constant 0 while the in-phase component may be constant 1. Thus, half of the product terms go to 0 while the other product term is the data itself (multiplied by 1). The 0 Hz channel filter therefore becomes the sum of the squares of the decimated in-phase and quadrature data.

Figure 37 illustrates a center frequency channel determination mechanism that receives the I and Q decimated data streams, 3702 and 3704 respectively, and applies the same to lowpass filters 37F1 and 37F2 and decimation blocks 37D1 and 37D2 so as to produce single data points. These single data points are squared in squaring operators 37S1 and 37S2 and then added in adder 3706 to produce the center channel output.

The purpose for employing the decimation filter is to attenuate image frequencies that exist above the Nyquist frequency. According to the filter roll-off, these image frequencies are rejected by at least 13 dB. However, the decimation loss with regard to transmitter frequency error is the loss across the center of the main lobe of the sinc function. Figure 38 is a graph illustrating an amount of decimation loss for the transmitter frequency uncertainty range as a function of percent of Nyquist bandwidth. When a signal of interest 3803 approaches the band edge of the Nyquist bandwidth 3802 or 3804, up to 3.9 dB of decimation loss can be expected, as shown.

The multi-channel receiver performs decimation to reduce the data rate prior to channel filter implementation. For a channelized radio, the optimal decimation would bring the Nyquist bandwidth down to equal the transmitter frequency uncertainty at a cost of significant decimation loss. Maximizing decimation means that each channel filter performs its function on the minimum of data points. Relaxing the decimation increases the channel filter computational loading, yet provides relief against decimation loss.

For channelized digital receivers, the sampled data is processed to create overlapping filters that span the frequency uncertainty. The sensitivity of each channel filter is set by the bandwidth of the channel filter and the total decimation loss. The ideal channel filter would be performed at the maximum data rate, thus suffering no decimation loss. This is not practical, in systems having limited computational resources, as is the case with the present multi-channel receiver. Accordingly, the realization of the present multi-channel receiver performs a partial initial decimation, lowering the effective bandwidth and associated data rate prior to channelization. Thus, when scaling the multi-channel receiver to provide a most sensitive performance, samples are made at 5 times the chipping rate, and decimated by 21 so as to achieve a pre-

channel filter Nyquist Bandwidth of ± 144 kHz. Subsequent overlapping channel filters continue the decimation process so that the noise bandwidth ideally matches the signal bandwidth. The initial decimation brings the uncertainty down only far enough to make it feasible to implement enough channel filters to span the frequency uncertainty of interest.

The non-uniform overlapped channel filters shown in Figure 39 span the transmitter frequency uncertainty of Figure 38, shown between points 3806 and 3808. Because the individual filters have non-uniform spacing (i.e., non-uniform with respect to the channel centers) the between-channel loss can be controlled to create a worst case system loss of 1.4 dB (as illustrated by the dashed line 3903) at cross-point 3908 inclusive of decimation and between-channel loss. The curve 3902 of Figure 39 represents the signal loss due to initial decimation of the signal from 6 MHZ to 288 kHz and is the same as line 3801 as depicted in Figure 38. Curve 3902 corresponds to the top of line 3801 (Figure 38) between points 3806 and 3808. Channel filter 3904 is shown offset from the center channel by –59.65 kHz and represents the negative-most channel spanning the transmitter frequency uncertainty. If the signal of interest is located in the center of this channel filter 3904, the power loss of the signal at 3906 is entirely due to initial decimation. However, if the transmitted signal is located close to the intercept point 3908, the additional signal loss is due to between-channel roll-off.

Alternatively, a set-on channel filter may be used to further reduce system loss due to filter shape. Set-on channel filter 3910 is used to eliminate or reduce the effects of between-channel loss, where the set-on channel filter has variable center frequency that may be moved to be centered overtop of a signal, once the signal is detected. Following a trip event in one of the static channels, the processor implements an interpolation mechanism that interpolates a power in two adjacent channel filters so as to determine a best estimate of actual frequency offset. The set-on channel filter is subsequently steered to exactly match the desired signal center frequency, thus removing any channel filter roll-off. Total system loss is therefore limited to the decimation loss. Figure 39 depicts the set-on filter as a dashed line 3910 which recovers the roll-off loss between two fixed channels.

Fast Search in Multi-Channel Receiver

The principles taught for fast serial search in the single channel receiver embodiment work equally well for the present multi-channel receiver embodiment. In addition, the present inventors have developed frequency domain algorithms for computing a fast correlation function as will be discussed.

Fast Frequency Domain Coarse Search

An alternative search method uses a frequency domain parallel correlator 4000 shown in Figure 40. Correlation is performed by calculating the Woodward radar ambiguity function

$$A_{XY}(\tau,\nu) = \sum_{N} (n-\tau)x(n)e^{j2\pi\nu n}$$

The ambiguity function is the received signal energy as a function of spreading code phase τ and carrier frequency shift ν between transmitter and receiver. The receiver is adjusted by the code phase and carrier frequency shift that results in greatest received signal energy so as to acquire synchronization with the transmitted signal. A size of the phase step in the search method is one code chip and a size of the frequency shift step is the frequency of the code repetition.

When the number of frequency shift steps is smaller than the number of phase steps to be covered, a frequency domain technique is computationally efficient. This is illustrated in Figure 40 for 7 frequency shift steps and 63 phase steps. The process steps are as follows:

Step 1. A real input fast Fourier transform (FFT) 4010 is performed on an input record 4005 of one period of the reference code. The 63 output (frequency) points centered on 0 Hz are saved in memory and the remaining output points are zeroed, which results in a reference code 4014 being filtered by an ideal low pass transfer function 4012. This computation is performed only once.

Step 2. The received signal is preferably sampled at the rate of 5 samples per spreading code chip (or 4 may be used as well). A real input fast Fourier transform (FFT) 4020 is performed on an input record 4015 one code period long.

Step 3. A circular indexing shift operation of ν -$f_s/4$ 4030 is performed on the output points 4024 so as to downconvert from the IF to baseband, and the resulting 63 output (frequency) points 4034 centered on 0 Hz are saved. The remaining output points are then zeroed, which results in an ideal low pass filtered baseband received signal at a frequency shift ν.

Step 4. These 63 frequency points 4034 are multiplied in a multiplier 4040 by the complex conjugate 4045 of the 63 reference code frequency points 4014. An inverse fast Fourier transform (IFFT) operation 4050 is performed on the product, and the result is a slice of the ambiguity function at one frequency shift ν.

Step 5. Steps 3 and 4 are repeated for each frequency shift so as to complete the computation of an ambiguity function 4060, and from this result the receiver can be synchronized using the methods

disclosed elsewhere herein. This algorithm is exemplified with a 63 chip spreading sequence, although parameters of the algorithm may be changed to accommodate other spreading sequence lengths, intermediate frequencies, and sampling rates.

Fast Frequency Domain Fine Search

After resolving the carrier frequency shift ν between transmitter and receiver, it is preferable to resolve the spreading code phase τ to ¼ of a chip. This is preferably accomplished by repeating step 3 with ν set for greatest received signal energy. See Figure 40.

The 63 frequency points 4034 are multiplied in the multiplier 4040 by the complex conjugate 4045 of the 63 reference code frequency points 4014. The 63 point product is zero padded to 252 points (i.e., add points having zero value) in zero pad operator 4070, and perform an inverse fast Fourier transform (IFFT) 4080 on the zero padded product. The result is a slice of an ambiguity function 4090 at the optimum frequency shift ν with a phase resolution of ¼ of a chip, from which the receiver can be synchronized to within ± 1/8 of a chip using the methods discussed herein.

This method is exemplified with a 63 chip spreading sequence, but parameters of the algorithm may be changed so as to accommodate other spreading sequence lengths, intermediate frequencies, and sampling rates.

Fast Frequency-Domain Search Implementations

The purpose of this algorithm is to synchronize the PN code of the receiver to that of the transmit signal. Two parameters need to be resolved in order to achieve this end: transmitter-receiver frequency offset ν and code-delay τ. By evaluating the receive signal energy at every (τ, ν)-pair, the processor can chose the best parameters for synchronization. This 2-dimensional correlation function over code-delay and frequency is called the Ambiguity function $A(\tau, \nu)$. Assuming a strong-enough signal is indeed being transmitted, the (τ, ν)-pair that best aligns with the transmit signal will have the strongest Ambiguity function value. See Figures 41 through 45.

When each chip is oversampled in the spreading sequence by some integer amount Q, and if the spreading sequence has M chips, $N=Q*M$ samples are taken. The synchronization process would then resolve τ to $1/Q$th chip. However, in an effort to hasten the acquisition time, the present alternative synchronization process trades $1/Q$th-chip resolution at slower speeds for single-chip resolution search at higher speeds, and reduces its processing load by band-limiting the receive signal. However, this will not be apparent until later in the procedure. Note that lower search resolution will cause a sensitivity loss.

Figure 41 illustrates the conventional process of evaluating the Ambiguity function at a specific (τ, ν)-pair. Figure 41 shows N samples over a time span of one code period, $d[n]$ 4101 and N coefficients of one code period, $a[n]$ 4102. Both enter a correlator 4103 and the correlation between the two signals 4104 is the Ambiguity function evaluated at (τ, ν).

Figure 42 illustrates a conventional process where a slice of the Ambiguity function 4201 is evaluated for all delays τ using a circular correlation operator 4202 with the same inputs.

Figure 43 illustrates a conventional circular correlation process that is very similar to a process known as circular convolution. Reversing one input sequence *a[n]* 4301 produces a sequence *b[n]* 4302, as shown and thus the circular convolution operator 4303 can be used as part of the circular correlation operator 4304 to produce the ambiguity function.

A conventional circular convolution process is shown in Figure 44 and is based on an understanding that convolution in the time domain is equivalent to multiplication operator 4401 in the frequency domain. Sequences 4402 and 4403 entering the circular convolver are reformatted into a frequency representation using the DFT operators 4404 and 4405, and combined in the multiplication operator 4401 an output as product 4406. The product 4406 is reformatted into a time-domain representation 4407 using an Inverse Discrete Fourier Transform operator (IDFT) 4408. Without the frequency transformations, a circular convolution requires N^2 multiply-accumulate operations, that, at first glance may seem inefficient, but in fact is not so inefficient when considering the possible computational savings offered by an FFT-based implementation (as is discussed below, after the discussion of Figure 45).

Figure 45 illustrates an inventive fast-frequency search process employed in the multi-channel receiver embodiment, which is relatively more computationally intensive than any search process employed in the single-channel receiver of the first embodiment, but uses bandpass filtering, and decimation-in-time as a way to reduce processing load. *C[n]* 4501 is an extracted *M*-length frequency-domain subsequence from *B[n]* 4502 centered around $f_s/4$, where *B[n]* 4502 is a product of an N-point DFT performed on time domain representations (a[n] ... b[n]) of the spreading sequence, as generated by the receiver. Likewise, *E[n]* 4503 is an extracted *M*-length frequency-domain sub-sequence from *D[n]* 4504 centered around $(f_s/4)+\nu$, where *D[n]* 4504 is an N-point result of a DFT operation performed on N time domain samples, d[n] of the received signal. These data extractions C[n] and E[n] are equivalent to ideal band-pass filtering in the frequency domain and decimating in the time domain. *D[n]* 4504 are stored in RAM so that *D[n]* 4504 can re-extract *E[n]* 4505 as the process steps through values of ν to fill in the Ambiguity function, as shown in the graph portion of Figure 45. A gray region of Figure 45 represents precalculated values stored in ROM. A data structure of the stored data includes a field configured to hold the M points corresponding to the portion of the code spectrum centered around $f_s/4$. The product F[n] 4505 is transformed back to the time domain sequence f[n] 4506 before being put into the Ambiguity array 4507, as shown in Figure 45.

The DFT and its Inverse can be calculated using the Fast Fourier Transform process. Ordinarily the DFT (or the IDFT) takes N^2 multiply-accumulate operations, just as many as circular convolution. The FFT, on the other hand, relies on the number of prime factors of *N*, which results in computational

efficiencies. If N is the product of q prime numbers P_1, P_2, ... P_q,, then a number of multiply-accumulate operations becomes $N*(P_1 + P_2 + ... + P_q)$, assuming all of the prime numbers are greater than or equal to 2, noting that $(P_1 + P_2 + ... + P_q) \leq (P_1 * P_2 * ... * P_q) = N$ for all prime integers $P_i \geq 2$. The more prime factors for N, the faster the FFT algorithm can compute the DFT. However, a savings exists over the straightforward circular convolution method only when $2(P_1 + P_2 + ... + P_q) \leq N$. For the preferred 63 chip spreading code, 63 is evenly divisible by prime factors 7, 3, and 3, and thus $2(7 + 3 + 3) = 26 \leq 63$, which means the preferred chip spreading code enables the realization of these computational efficiencies.

The FFT algorithm breaks the large DFT into smaller DFT's. Depending on the target architecture and the prime factors, the Winograd DFT method may be used as a substitute for the smaller prime DFTs. Winograd's method minimizes the number of multiply operations for certain prime DFTs but also incurs higher indexing complexity. Most effective digital signal processing devices will perform multiply operations as efficiently as addition operations, and may have provisions for successive and modulo indexing. Winograd's method will not be as advantageous in such processors as it could be with a processor that does not have single-instruction multiply operations. Preferably the Winograd method is not used in the present embodiment for the indivisible DFTs because digital signal processing devices are generally more efficient in the N^2 calculation in general. In addition, 3 and 7 are relative low number primes and thus N^2 is somewhat small. Because of these computational efficiencies, prime factors should also play a role selecting a spreading sequence, as they are in the preferred case of 63 chip spreading sequence.

False Trip Avoidance in a Multi-Channel Receiver

Identifying valid trip events is a challenge in multichannel receivers because there are several false signals, such as impulsive jammers, undesired signals, and signals or noise that will occasionally give the appearance of false synchronization detection. However, by employing false synchronization avoidance mechanisms, the multi-channel receiver of the present embodiment offers relatively fast signal acquisition and reduced transmitter preamble time.

False trips events are received power fluctuations at an erroneous code phase that are sufficient to cause the receiver to dwell at that code phase and evaluate the incoming signal to determine if correlation has, in fact, been obtained. Sources of received RF signals include ambient noise, keyed carrier wave (CW) jammers, non-correlated spread spectrum signals, and correlated spread spectrum signals. Non-correlated spread spectrum signals are signals that may properly be decoded by the receiver, provided that the receiver can eventually obtain code phase coherence with the received signal; a correlated spread spectrum signal is one in which spreading code phase coherence has already been achieved. A trip event occurs when there is a measurable increase in received signal power over successive periods of time, however, this increase

may be due to several sources and, perhaps, many of these increases will not result in a legitimate, true trip event signifying that the received signal should be demodulated. The presently described inventive process is arranged to reduce the instances of reporting a trip event on a keyed CW jammer or a non-correlated spread spectrum signal.

Figure 46 is a graph of time versus signal power, where power 4605 represents a background noise floor and power 4610 represents an observed power increase owing to a CW jammer beginning to transmit a CW signal. Because the CW jammer may modulate the signal by frequency hopping, or "keying" for "mark" symbols or "not keying" for "space" symbols, signals received from these CW jammers may appear to turn-on and turn-off. However, a marked increase in signal power will also occur whenever a transmitter of interest initially begins transmitting as shown by the power 4620 in Figure 46, resulting in a non-correlated signal. Another increase in signal power occurs when the receiver has achieved spreading code coherency with the transmitter, resulting in a correlated signal power 4625, the increase being due to the process gain provided by the spreading code. It is this third increase in signal power that is of interest for identifying a trip event, however a legitimate trip event may occur with no appreciable increase in received signal power 4635. Thus, simply observing raw power levels, which is the technique employed by existing systems, will result in numerous false trips or missed trips.

In the present multi-channel embodiment, trip event decisions are made after the signals have been despread and after the signal has been separated into various frequency bins, where a highest performance is obtained by using 11 overlapping frequency bins (channels). The aforementioned signal types will have unique power distribution characteristics (e.g., signal "signatures") as cumulatively viewed in the frequency bins. Figures 47-50 depict the power levels of these signals distributed throughout the bins. Figure 47 represents random noise and in Figures 48-50, a center frequency of a received signal is depicted as being coincident with the center frequency 4805, 4905, 5005 (i.e., in bin 5) of the channel filters in the respective figures. In Figures 48 and 49, the signals have similar characteristics, even though Figure 48 depicts an undesired CW jammer while Figure 49 depicts a desired signal at an uncorrelated relative code phase. The power level of the frequency bins 4805, 4905 is lower than the power level in the surrounding bins due to code carrier suppression.

Figure 50 illustrates the power distribution in the respective bins when the correlated spread spectrum signal is present. Frequency bin 5 (5005) holds the center frequency of the transmitted signal as depicted by the maximum signal level. Because the frequency bins overlap, some of the energy present in bin 5 will also be in bins 4 (5004) and 6 (5006), but powers in the remaining bins begins to drop off sharply after that, as set by the attenuation provided by each channel filter (i.e., because much, or all, of the signal energy falls outside of the filter passband).

Steps in the false trip avoidance process are explained with reference to Figure 51 where the method begins in step 5105, where the power level is measured in each channel filter. The process proceeds to step 5110 where the frequency bin with the maximum signal strength is determined and designated as *max1*. Subsequently, step 5120 ignores the frequency bins that are adjacent to *max1* providing for channel overlap. Step 5120 calculates the average value of the signal strength values in the remaining frequency bins and designate this value as *avg*. A decision is performed in step 5125 wherein if *max1* is greater than *avg* by a predetermined threshold, process control is passed to step 5140, where the fine search process is initiated. If block 5125 determines that *max1* is not greater than *avg* by a predetermined threshold, process control is passed to step 5150, where the coarse search process is continued.

Figure 51 also illustrates an alternative method where the method begins in step 5105, where the power level is measured in each channel filter. The process proceeds to step 5110 where the frequency bin with the maximum signal strength is determined and designated as *max1*. Subsequently, step 5130 ignores the frequency bins that are adjacent to *max1* providing for channel overlap. Out of the remaining frequency bins, step 5130 will then locate the bin with the maximum signal strength and designate that frequency bin as *max2*. A decision is performed in process 5135 wherein if *max1* is greater than *max2* by a predetermined threshold, process control is passed to step 5140, where the fine search process is initiated. If block 5125 determines that *max1* is not greater than *max2* by a predetermined threshold, process control is passed to step 5150, where the coarse search process is continued.

Figure 51 also illustrates another process that uses the approach discussed earlier for the 1-bit ADC for the single channel embodiment. In particular, the process begins in step 5105, as previously discussed, and proceeds to step 5110, as previously discussed. If the 1-bit ADC process is employed, the process flows to step 5141, where a stored predetermined threshold is retrieved from memory and, in step 5145 is compared with *max1* obtained in step 5110. If the response to the inquiry in step 5145 is affirmative, the process proceeds to step 5140, where the fine search process is initiated. However, if the response to the inquiry in step 5145 is negative, the process proceeds to step 5150, where the course search process continues by returning to step 5105.

Enhancing Coarse Search

Averaging similarly improves signal acquisition performance in the present multi-channel receiver embodiment, as was the case for the single channel receiver embodiment. However, in the multi-channel receiver, where the final decision bandwidth equals the signal bandwidth and multiple channels are spaced apart so as to span the frequency uncertainty range, the averaging process is a different in several respects. For example, instead of the correlation data being represented as vectors, for each sampled code period, the correlation data exists in another dimension as well, so as to be arranged in a plane of information, each data point being described by three axes coordinates: frequency channel, code phase and power. Figure

52 depicts a sample data set from one code period (i.e., no averaging), while Figure 53 shows the collection of several data sets, appropriately averaged. A most noticeable result of averaging is a suppression of background noise, as is evident from a comparison of noise floors 5220 and 5320 in Figures 52 and 53, respectively.

As discussed with respect to the single channel embodiment, averaging may be performed as a box-car or FIR structure where the last N symbols are averaged. Alternatively, averaging may be performed in an exponential or IIR averaging process where the previous results are decayed and added to a fraction of a present sample.

Figures 52 and 53 depict the desired signal correlation peak at points 5210 and 5310, respectively, in a plane of frequency channel versus correlation code phase. The preferred multi-channel receiver embodiment employs 11 frequency channels and 63 code chips, although the number of channels and chips may be varied in accordance with the discussion of trade-offs as presented herein.

Figure 54 is a histogram of power versus occurrences that illustrates a reduction in false alarm rate achieved by averaging 6 samples in the multi-channel receiver embodiment. Curves 5410 and 5420 show the power distribution of a 20 kHz noise bandwidth with and without averaging respectively. Curves 5430 and 5440 show the power distribution of a -110 dBm signal in 20 kHz noise bandwidth with and without averaging respectively. The mean power for the noise and signal plus noise distributions remain unchanged, yet the deviations are reduced creating a greater distance between the minimum "On" and the maximum "Off". Consequently, extending the distance between the minimum "On" and the maximum "Off" corresponds directly with decreasing the probability of reporting a false trip condition.

Frequency domain averaging is identical to the multi-channel case depicted in Figure 45, where the result of the fast frequency coarse search is a plane of power versus frequency and code phase. This process, however, uses different mathematical operations to achieve the same result, yet the result may be averaged as in the channelized time domain coarse search to achieve better SNR. Applying the method for reducing false trips for impulsive interference following averaging provides the maximum sensitivity achievable, under the presently described circumstances.

Automatic Gain Control (AGC)

As previously discussed, AGC is used to adjust a signal level of a received signal to fall within an instantaneous dynamic range of the ADC. At times this is a challenge, because the receiver may be exposed to signals of varying strengths. For example, a receiver placed within a few feet of a transmitter will be exposed to a very strong signal level, but a receiver located far from the transmitter will be exposed to a very weak signal level. AGC allows the received signal, in either case, to be adjusted to within a predetermined range, prior to being applied to the ADC. One factor considered in the AGC mechanism, is a level of a received noise floor and thus the AGC mechanism monitors the received noise floor,

attempting to keep it within an operable range of the ADC. However, as the noise floor rises, there is a risk that the AGC mechanism will not act to lower the signal level applied to the ADC and will result in clipping an intended signal, as a result of inadequate "headroom", which has profound adverse affects on signal correlation and reception. Accordingly, if the AGC mechanism detects that the noise level has risen too much, the AGC mechanism will act to attenuate the received signal (and noise) to a lower level, ensuring that the received signal will remain within the ADC's dynamic range.

The AGC process is implemented in software and is executed once per code period while the search process is attempting to correlate. If an attenuation change is deemed necessary by the AGC process determining that the sample values are above a predetermined threshold, for example, the search process is interrupted while AGC adjusts the receiver gain, over several code periods, which in turn adjusts the corresponding signal strength of the received signal. Decisions made by the AGC process are based on the measured noise floor (where the measurement may be made with a discrete level detector or by digital analysis on the received sample stream) and serves to keep the noise floor within the operable region of the ADC. The AGC process may be augmented with time constant mechanisms to offset the effect of impulsive interference, and averaging mechanisms that combine several sample sets so as to avoid invoking an AGC adjustment if short-term perturbances in the noise floor are observed. Similarly, the AGC process may be adapted to operate off of the strongest received signal, so as to avoid driving the ADC outside of the ADC's dynamic range by the strong signal, whether the strong signal is the intended signal or not.

Attenuation of the received signal is set with two controls, implemented in hardware, although other software or firmware driven control may be used as well. The signal level may be adjusted (preferably attenuated) in the attenuator 3502 by a maximum of 75 dB using a step and digital attenuator that operates under the control of the AGC signal (as shown in Figure 35). A 4-bit digital attenuator located in the attenuator 3502 is positioned prior to the ADC and provides attenuation in 3 dB steps up to a maximum of 45 dB attenuation. A coarse 30 dB step attenuator may optionally be applied in front of the first RF amplifier, thus protecting the mixer from very strong signals and related intermodulation products created by excessively strong signals being applied to the mixer.

A related problem caused by excessively strong signals is that the signals may result in the digital signal processing operations performed on the signals to enter an overflow state. For example, the digital signal processor used to compute the correlation sum on the received signal also implements the decimation process concurrently therewith. In an implementation of the multi-channel receiver a digital signal processor that computes this correlation sum has the undesirable attribute of failing to retain an indication of intermediate overflow. This means that in the decimation process, should an accumulator in the digital signal processor overflow at some intermediate point, there may be no report of the overflow condition after the decimation process is complete. Even though a digital signal processor may retain an overflow

condition immediately following a mathematical instruction, the digital signal processor may reset the overflow flag on the next mathematical instruction. A similar problem exists if the decimation process were fabricated using discrete components such as adders and accumulators.

It is possible to prevent overflow from ever occurring provided the accumulator has enough resolution for all worst case summations, but digital signal processors with such attributes are relatively expensive and otherwise not suitable for use in low-end applications. An alternative method scales the signal or coefficients used in the digital signal processing operation such that an overflow will never occur in a given number of accumulator bits. However, both techniques require the hardware to be more complex than minimally necessary as extending the accumulator adds hardware expense and complexity and attenuating the signal loses fidelity and resolution in signal quantization.

Accordingly, the overflow concern is easily avoidable by using modern digital signal processors having sufficient processing capability, overflow indication mechanisms, and/or large accumulators. However, because it is preferred to minimize cost by using a low-end processor in the present receiver, identifying the source of the problem and solution to the problem requires innovative processes and mechanisms. The present multi-channel receiver uses a small accumulator while managing the possibility of overflow by integrating signal scaling into the AGC process. To more completely understand the problem identified by the inventors and the solution therefor, a discussion on the failure mechanism and how it impacts data integrity is presented below.

Provided that an overflow condition may occur for strong signals at a given AGC setting, the receiver's processes and mechanisms must be able to detect the presence of strong or weak signals and act accordingly, making adjustments in the attenuator 3502 (Figure 32) to keep the signal in the desired received power band. Weak signals do not create a problem, because the signal power drops monotonically with signal attenuation, and a low threshold near the minimum correlation limit triggers a signal drop event.

A problem arises when the signal is greater than that which can be supported in the resolution of a signal data word (e.g., 16-bit word) because the end decimation result becomes non-monotonic due to clipping of the signal (by inadequately representing the full size of the signal power in a given data word). So as to prevent the signal from being clipped, the present multi-channel receiver uses a threshold set near the maximum correlation limit of the accumulator so as to create a value driven overflow condition. The threshold is effective in determining a need for AGC (e.g., provides a warning signal), yet the value reported is not used because it becomes non-monotonic.

The AGC process addresses this unreliable reporting of an overflow condition by searching backward, keeping a range of untrustworthy samples (i.e., perhaps tainted by an unreported overflow condition) shadowed in previous evaluation ranges where the power can be trusted. As will be explained,

the range of ambiguity can be eliminated by asserting first maximum attenuation and then subsequently stepping through progressively less attenuation.

When first initiated, the AGC process starts by asserting maximum attenuation (so as to produce a minimum signal level applied to the ADC) and then progressively lowering the amount of attenuation in roughly 9 dB steps (or other suitable step sizes), through 7 coarse acquisition steps. By first applying maximum attenuation, there is no ambiguity regarding whether the data samples have been caused an overflow condition during the decimation process. When the noise level detected in one of these steps is near optimal (i.e., at a preferred level within the ADC's instantaneous dynamic range), the AGC process causes a fine attenuation step to be executed so as to place the received noise floor within 3 dB of the desired level. Subsequently, the AGC process terminates and the normal correlation (search function) resumes.

The AGC process as implemented in the present embodiment accounts for a three-code period delay set by pipeline processing. Thus, when the AGC process causes an AGC attenuation change, the next two code periods are already being processed. The third code period, following a setting operation, will hold data that reflects the change. For this reason, the AGC acquisition process is heavily pipelined to minimize waiting for data. Figures 55 through 65 depict the state process implemented in the AGC process and mechanism. The following description details the steps used in the most sensitive exemplary embodiment of the multi-channel receiver.

The AGC process flow shown in Figure 55 begins in step 5501 and then to step 5502 where a Boolean flag is maintained. An inquiry is made so the AGC process recalls, between program calls, whether the AGC process is currently acquiring a signal. If the response to the inquiry is affirmative, the process proceeds to step 5506 so as to determine where the AGC process is in the acquisition cycle. If AGC is not acquiring, the process continues by computing a time averaged noise floor in step 5503 using the last 8 code periods for smoothing the instantaneous noise. A counter (code interval timer) is decremented and tested in steps 5504 and 5505 so as to add hysterisis to the AGC process. If the counter has expired, the AGC algorithm is enabled to begin an acquisition if necessary by proceeding to step 5507 where the instantaneous noise floor is monitored so as to determine if there exists enough headroom in the ADC and decimation process to support a correlation operation. If the noise level is too high, and there exists more attenuation as inquired in step 5508 for use, the process proceeds to step 5506 so as to initiate the acquisition process. However, if the instantaneous noise value requires attenuation but there is not any additional attenuation available, the process proceeds to step 5511, where the process aborts. If the instantaneous noise level is not too high, the process continues at 5509 where the time averaged noise floor is evaluated as being too low. If the time averaged noise floor is too low, and attenuation can be removed from the current setting 5510, an acquisition is necessary, so the process proceeds to step 5506 to properly

set the lower attenuation level. If the time averaged noise level is too low, but no further attenuation can be removed, the algorithm aborts in step 5511.

Figure 56 is a flowchart of a decision tree for determining where the AGC algorithm is in the AGC acquisition cycle. Step 5601 continues from step 5506 as shown on Figure 35. After step 5601 the process proceeds to step 5602 where an inquiry is made regarding the AGC processing state, which is determined by checking a state variable. Depending on the value of the state variable, the process continues to respective of steps 5603 through 5613, as will be explained below with respect to Figures 57-61.

Figure 57 is a flowchart of four of the decision tree branches depicted in the flowchart of Figure 56. Step 5701 is the continuation of step 5603; Step 5704 is the continuation of step 5604. Step 5711 is the continuation of step 5605. Step 5714 is the continuation of step 5606. When the acquisition process begins in step 5701, the maximum attenuation (minimum sensitivity) is applied in step 5702. Subsequently, the state variable is advanced to step 5703 and the AGC process terminates in step 5710 and waits for a new code period of data. However, on the next code interval, the process flow resumes to step 5704 where a recheck of the previous decision to perform AGC is performed in step 5705. If the test of the instantaneous noise floor results in a decision not to need AGC, the noise value has crept up to the decision threshold and only a small adjustment is needed. Thus, to determine the magnitude of the adjustment, the last two noise samples are averaged in step 5706 and a small adjustment is made step 5707. If in step 5705 the test for AGC shows the receiver remains saturated, the attenuation is set at maximum in step 5708, the state is advanced in step 5709 and the process waits for a new code interval of data in step 5710.

On the next code interval, the process flow resumes through step 5711 and then to step 5712 where attenuation is lowered prior to beginning the search process. As previously discussed, this attenuation setting will not be available for next 3 code intervals due to the pipelining of the DSP process, so the state variable is advanced in step 5713 and the process waits for a new code interval of data in step 5717.

On the next code interval, the process flow resumes through step 5714 and then in step 5715, attenuation is lowered to continue the search process. Subsequently, the state variable is advanced in step 5716 and the process waits for a new code interval of data in step 5717.

Figures 58, 59 and 60 are flowcharts of six of the decision tree branches depicted in Figure 56. Step 5801 is the continuation of step 5607. Step 5810 is the continuation of step 5608. Step 5901 is the continuation of step 5609. Step 5910 is the continuation of step 5610. Step 6001 is the continuation of step 5611. Step 6010 is the continuation of step 5612. The processes depicted in Figures 58, 59 and 60 demonstrate the evaluation of the attenuation levels set 3 code intervals previous (due to pipeline delay).

In reference to Figure 58, the first evaluation step 5801 the instantaneous noise level is evaluated in step 5802. If the noise level is too high, the optimum point has already been passed, and thus a blind

9 dB is added in step 5806 before the AGC process terminates in step 5807, instructing the calling module that it has completed acquisition. However, if the noise level as determined in step 5802 is not too high, the noise level is tested for being too low in step 5803 indicating the attenuation is still to great. Subsequently, the next attenuation step is applied in step 5804, the state is advanced in step 5805 and the process is suspended in step 5809, waiting for the next code interval of data. If the test performed in step 5803 indicates the noise value is between the low and high thresholds, the search only needs a fine step and the process flow resumes at step 5808.

On the subsequent code intervals the evaluation steps 5810, 5901, 5910, 6001, 6010 evaluate the instantaneous noise level 5811, 5902, 5911, 6002, 6011, respectively. If the noise level is too high, the optimum point has already been passed, and a blind 9 dB is added in steps 5815, 5906, 5915, 6006, 6015 respectively before the AGC process terminates in steps 5816, 5907, 5916, 6007, 6016 respectively, instructing the calling module that it has completed acquisition. If the noise level of steps 5811, 5902, 5911, 6002, 6011 is not too high, the noise level is tested for being too low in steps 5812, 5903, 5912, 6003, 6012 indicating the attenuation is still to great. The next attenuation step is applied in steps 5813, 5904, 5913, 6004, 6013; the state is advanced in steps 5814, 5905, 5914, 6005, 6014; and the routine suspends in steps 5818, 5909, 5918, 6009, 6018 and waits for the next code interval of data. If the test of steps 5812, 5903, 5912, 6003, 6012 indicates the noise value is between the low and high thresholds, the search only needs a fine step and algorithmic flow resumes at steps 5817, 5908, 5917, 6008, 6017.

Figure 61 is a flowchart of the last evaluation step and the small step algorithm process flow. The last attenuation step is evaluated if the search thus far has not found a solution. Step 6101 is the continuation of step 5613 depicted in Figure 56. Step 6109 is the continuation of steps 5707, 5808, 5817, 5908, 5917, 6008, 6017 or 6108. The attenuation is set to a minimum three bit code intervals previous, so the current data represents the maximum sensitivity setting. The noise level is tested in step 6102 and if the noise level is too high, the optimum point has already been passed, and a blind 9 dB is added in step 6106. The algorithm suspends operation in step 6107, instructing the calling module that the AGC process is finished. If the noise value measured in step 6102 is not too high, it is evaluated as being too low step 6103. If too low, there are no further steps to minimize attenuation so the attenuation is set to a minimum in step 6104, the state variable is set to indicate the AGC is not acquiring in step 6105 and the process suspends operation in step 6107, instructing the calling module that the AGC process is finished. However, if the noise power is between the upper and lower thresholds, a small adjustment is needed and the process continues through 6108 to 6109. Once one of the evaluation steps determines the measured noise value to be between upper and lower thresholds, the process proceeds to step 6109 and subsequently to step 6110 where the measured instantaneous noise power is subtracted from the desired power and the difference is used to adjust the current attenuation setting to optimum. Then, in step 6111, an inquiry is made to

determine if the result is different from the passed attenuation value. If the small adjustment test determines the attenuation setting should be changed, the attenuation is adjusted in step 6112 and the process terminates in step 6113, instructing the calling module that the AGC process is finished.

Reception of Data Transmission with Fast Frequency Drift

Multi-channel receiver systems enjoy excellent sensitivity, as compared with receiver systems that use detection bandwidths that are appreciatively wider than the data bandwidth. Ideal systems exactly match the channel bandwidth to the data bandwidths, because SNR (and hence communication quality) is maximized when the received, despread signal exactly matches in frequency one of the channels in the channelized receiver and the receiver detects and monitors the signal from the single channel of coincidence.

Problems exists when the ideal channelized system attempts to demodulate a signal from a specific channel and the transmitter fails to maintain frequency fidelity during data transmission. Factors leading to the frequency error include the transmitter frequency pulling, or receiver local frequency reference pulling, each of which may occur if the respective frequency reference is in some way subjected to environmental changes, such as supply power variation. All contribute to short term, intra-message frequency instability which degrade the ability of a channelized receiver to optimally demodulate a signal, because the received signal "drifts" between adjacent channels.

The conventional approach has been to avoid drift problems altogether by ensuring the transmitter and receiver reference components not experience frequency drift, primarily by using crystal controlled or direct digital synthesis frequency references. Cost efficient transmitters often have frequency references which are sensitive to changes in power supply voltage or electro-mechanical interference, even self interference. This is especially true for OOK transmitters which often enable and disable amplification stages to modulate data which can effect local frequency references such as voltage controlled oscillators. In other words, the combination of an OOK transmitters with an inaccurate frequency references causes particular challenges for a low-cost receiver that has available only minimal processing capacity.

In contrast to conventional practice, the present invention employs cost efficient components and combines them so as to be used in systems having transmitters that transmit messages with, perhaps, significant frequency drift and offset. Conventional practice accommodates the sizable transmitter frequency drift by quantifying the total frequency error budget, for all of the relevant system components, and expanding the channel bandwidths in the receiver to exactly match the worst case frequency drift. The wider receiver bandwidth de-sensitizes the receiver because the increased channel bandwidth degrades SNR (and hence performance) by the increase of noise bandwidth.

At the expense of increased computational complexity, the present multi-channel receiver embodiment uses several channels, each matching the data bandwidth, so as to track frequency drift throughout a message. Figure 62 depicts a bank of channel filters where a specific filter matched to the

data bandwidth has shape 6200. A signal exactly aligned in channel 6203 transmitting a "1" would have a measured mean power denoted as 6201 in Figure 62. Because the channel filters have independent roll-off characteristics, a signal adjacent to the desired channel will be attenuated according to the shape of the filter 6200. As such, there exists a between-channel loss (i.e., because the signal falls in between to channels) denoted by point 6202, signifying a worst case system sensitivity for signals which have no frequency drift. A signal exactly centered between two channel filters would be measured in either filter with a mean power as denoted at 6202. For this reason, it is most beneficial to overlap the channel filters to limit the between channel loss. The system loss budget can then be specified using this worst case estimation.

The above description remains valid as long as the transmitters do not exhibit frequency drift during transmission of a message. But, if the transmitters do exhibit frequency drift beyond the between-channel frequency, the signal will continue to roll off, until the drift becomes so pronounced the signal is ultimately completely rejected by the selected channel filter.

In Figure 62, the Curve 6204 depicts the ideal signal 6203 which has been pulled off frequency beyond the between-channel point 6202 to a high attenuation point 6205. Under these conditions, if the receiver was demodulating, the signal from the initial channel 6200 would progressively drop power, during bit interval, because the drift would cause signal to move away from the center of the channel and toward an edge of the channel. If the transmitter drift was constrained between the frequency excursions shown as curves 6203 and 6204, the signal power will fluctuate between points 6201 and 6206 (heavy line 6206).

The present multi-channel receiver uses several channel filters to track frequency fluctuations during data demodulation. The total frequency excursion must be quantified for the transmitters in question and system application. The technique is most feasible for correcting small scale frequency drift on the order of the data bandwidth. Wide scale frequency drift could be corrected in the transmitter.

As long as the frequency drift is relatively small, overlapping only a few channels in the system at worst, and provided the steady state condition can be measured, the frequency drift loss can be recovered using the adjacent channels and a process described below. The steady state condition is defined as the resting frequency of the transmitter. Typically frequency drift is caused by changes in the transmitter power structures, most typically caused by keying an OOK transmitter. As such, it is common for the frequency to have error coincident with a change in amplitude key state. The steady state condition is therefore measured when there is a run of same state values while the transmitter is keyed, perhaps in a preamble or initiation sequence of the signal data structure.

In the graph of Figure 63, the lines 6301 represent the respective powers measured in a single channel filter over a sequence of bit intervals. Variation between the heights of the lines indicates that there is a time variable power variation. Explaining the power variation in the depicted example, the transmitter

exhibits signal loss during a 0 to 1 transition state shown as line 6303. After a period of time while transmitting a series of 1s, the power is recovered by the bit interval corresponding with the line 6304. This recovery coincides with the transmitter drift correction over time. The loss in power when the sequence of 1s is transmitted effects the bit error rate, and may influence the decision threshold mechanism to call the bit a "0" (i.e., a bit error) in cases where there is low SNR, i.e., where the noise floor 6302 approaches the 1s level (6303).

A method for using alternate channels to overcome the frequency drift is explained with respect to Figure 64. Assuming the drift direction and relative magnitude may be determined, where the direction may be bi-directional or uni-directional depending on the design and nature of failure in the transmitter, the trip determination step 6400 may be any of the processes discussed herein or any other determination of signal activity. Following a trip event, the primary channel determination is determined in step 6401 where the primary channel is determined as the channel which most closely aligns with the steady state power of the transmitter, while the transmitter is transmitting a preamble portion of the signal. The primary channel is the channel with the largest measured mean power during a run of 1s in the preamble of the transmitted message. Subsequently, the process proceeds to step 6402 when an initial primary OOK decision threshold for determining a 1 or a 0 is set. This may be static based on the measured amplitude of a 1, a zero or combination thereof, or it may be dynamic and change to track with the message as received. An alternate channel threshold is then set in step 6403 so as to track with the primary channel threshold. The value of this alternate channel threshold must be equal to or greater than the primary channel threshold as explained below to keep from adversely affecting the bit error rate of the receiver.

Data demodulation commences following initialization, and at each new bit interval collected in step 6404, the received signal power is measured in each of the candidate channels in step 6405 where the signal may deviate. The power in the primary channel is compared to the primary OOK decision threshold in step 6406. If the power exceeds the threshold,, a 1s determination is made in step 6408 and the next bit is processed. If the power is below the primary OOK decision threshold, the alternate channels are evaluated in step 6407 using the alternate decision threshold. If any of the alternate channels exceed the alternate decision threshold, a 1s decision is made in step 6408 and the next bit is processed. If none of the alternate channels exceed the alternate decision threshold, a 0's determination is made in step 6409 and the next bit is processed.

The difference between the primary and alternate channel decision threshold effects the bit error rate (BER). The alternate decision threshold must be at least equal to the primary decision threshold and preferably larger so as to minimally impact the receiver BER. Figure 65 depicts noise versus signal plus noise graphs, where it is seen that a 1/0 decision threshold 6503 may be set such that the BER contribution from the primary channel zero determination equals the percentage of noise to the right of the decision

threshold 6505. If the same decision threshold were used for each of the alternative channels, then the system BER would be increased to include the total of all the percentages to the right of each decision threshold for zeros determination. This is true due the fact that noise is generally uniform in distribution (for spread signals), and each channel filter will have a noise distribution as depicted by 6500. The likelihood that noise power in each channel exceeds any arbitrary value within the distribution is identical. This distorts the combined channel noise distribution adversely weighing it toward the signal plus noise distribution and increasing BER.

A second threshold is used for the alternate channels which is set such that the combined zeros determination BER contribution for the alternate channels is small relative to the primary zeros BER. The overall system BER is not adversely affected and the benefit of using the alternate channels is achieved. Exact placement for decision thresholds and separation for primary and alternate decision thresholds is determined based on system requirements for signal detection and data integrity.

Predictive Code Reposition

Once a receiver has achieved coarse and fine search, the time references, e.g., crystals in the transmitter and receiver will drift (relative to each other) over time, particularly if low-cost components are used. If the drift is too large, the receiver will begin to lose process gain, and gets progressively worse for longer messages. U.S. Patent No. 5,457,713 (Sanderford, et. al) discusses a method to maintain spreading code coherency between a transmitter and receiver for long messages. At predetermined points in a message, the transmitter will transmit an expected symbol. The receiver uses this symbol to perform an additional fine search process to re-align the receiver spreading code. This method maintains code coherency at the expense of added overhead in the transmitted message.

The present receiver embodiments use the results of the initial search process to predict the rate of time base drift. This method requires that the transmitter use one time base to control the RF frequency as well as to generate the code chip rate. Conversely, the receiver must use one time base to generate the downconversion tones as well as generate its code chip rate. This method also requires that the receiver be able to quantify the frequency error so that the spreading code phase drift can be predicted. In the multi-channel receiver embodiment, one of the eleven channels will be selected as the candidate filter by the coarse search process. The receiver then uses the channel index (e.g., channel number) relative to 0 frequency error to predict the time base drift as follows:

Figure 39 shows the spacing and center frequencies of the frequency channels (as has previously been discussed). If the transmission frequency is 915 MHZ and the frequency channel at 37.4 kHz is chosen as the candidate filter, this means that the crystal drift between transmitter and receiver is:

37 kHz / 915 MHZ = 40.4 ppm error.

This ppm error also affects the spreading code chip rate. For example, over a period of 100 bit times, the error associated with this crystal drift is

100 bits x 63 chips/bit x 40.4 ppm = .25 chip error,

which results in a 2.5 dB loss of signal correlation. If the system specification requires that the receiver stay within a certain code phase distance of the transmitter throughout the duration of the message, the receiver must periodically adjust its spreading code phase, under the present conditions. The frequency at which this adjustment is made is driven by the resolution of the spreading code generator, the ppm of the transmitted signal, and the system requirements. The present embodiment acquires 5 data samples per code chip, and executes 3 instructions per sample interval. By optionally inserting an additional instruction, the computer is able to achieve a despreading code adjustment resolution of $1/15^{th}$ of a chip.

This technique, while helping to maintain spreading code coherency, has a limitation in that each channel filter is 20 kHz wide, and thus the error of the predictive value is given by:

20 kHz / 915 MHZ = 21.8 ppm

which means that over time, this predictive repositioning technique will not necessarily adequately correct spreading code alignment error. Techniques such as frequency and/or phase discrimination provide frequency resolution that is even narrower that the 20 kHz channel filter, and the optional use of these techniques will reduce the error of the prediction reposition process. Depending on system requirements, the predictive reposition method may be sufficient to maintain code coherence over a message duration without the use of the standard reposition method.

The effects of reposition are explained in Figures 66A, 66B, and 66C wherein points 6610, 6620, and 6630 represent the signal level after the coarse and fine search algorithms have been performed. After the duration of the message 6611, the signal strength of the message will have decreased to points 6615, 6625, and 6635 due to crystal drift. Item 6613 shows the signal strength of an ideal message with no loss of process gain. Items 6626 and 6636 show the signal recovery provided by the use of the standard reposition method. The repetition rate 6624 of the standard reposition algorithm is pre-determined by the positioning of the reposition symbols within the transmitted message.

The feature 6627 shows a signal recovery provided by the predictive reposition method. An amount of signal recovery 6628 is determined by the system's ability to discern the frequency error of the received RF signal. The repetition rate 6634 of the predictive reposition method is set by the worst-case system loss requirement and the amount of signal recovery 6628 that can be achieved.

Alternatively, the two reposition methods can be used together to provide enhanced performance. Feature 6638 shows the combination of the two methods as providing better results (signal levels) than either method working alone.

Elimination of Redundant Data in a Multi-Drop Network

In some RF installations, physical obstacles will cause the performance of the system to degrade due to fading. In reference to Figure 67, a network with multiple transmitters 6710 through 6715 and multiple receivers 6720 through 6724 are installed in various locations and each of which may be required to assure adequate coverage. In many installations it is desirable to connect all of the receivers to a common processor 6740 with some type of shared medium 6730, such as a multi-drop bus, such as an RS-485 bus, a local area network, USB, FireWire, etc. Once having received a message, the respective receivers would then relay data to the processor 6740 in some pre-determined fashion. Poll-response, Ethernet, and token-ring protocols are just three of many methods that would serve this purpose, and would be used whenever some type of data collection and/or processing is to be performed at a central location (such as security alarm applications, tracking systems, etc.).

As shown in Figure 67, multiple receivers R2, R3, and R4 (which may be transceivers) may, or may not, receive the same transmitted message 6717 from transmitter T4. Each of these receivers would then attempt to forward the message to the application processor 6740. Present network systems allow the bus peripherals (the receivers) to forward all messages to the common processor 6740, forcing the processor 6740 to detect and eliminate redundant messages. However, this technique increases bus traffic and forces the processor to perform extra processing to detect and eliminate redundant data messages. The present invention eliminates this extra bus traffic by requiring that the receivers monitor the bus 6730 for redundant data messages.

Whenever a data message is received, the receiver will store the message in a queue until it is time for that receiver to relay the messages to the common processor 6740. Since the receiver is attached to a multi-drop network, the receiver is able to monitor all messages transmitted on the bus 6730. Whenever a receiver is not transmitting data to the common processor 6740, that receiver will monitor the bus 6730, reading all data messages transferred to the processor 6740. Each data message will have some type of unique identification such as a property code, system code, transmitter ID tag, Cyclical Redundancy Check (CRC), CDMA channel, or the like. The waiting receiver will compare each data message on the bus with the messages stored in its local message queue. Whenever the waiting receiver detects that another receiver is transmitting a message to the processor 6740 that is identical to a message in its local queue, that waiting receiver will delete the message from its local queue. Each waiting receiver will attempt to eliminate as many messages from its local queue prior to relaying the messages to the common processor, thereby reducing bus traffic and reducing the processing requirements of the common processor.

Figure 67 shows that transceivers and/or receivers on the same hard-wired interface communicate with all remote transmitters and transceivers within a defined proximity. Further, the present network embodiment uses the same CDMA and system property code for all devices associated with a particular

hard-wired line. This method allows redundancy and the ability of the system to eliminate redundant messages.

Battery Operation

Another embodiment of the present invention is a very small, battery operated transceiver that incorporates combinations of features of the single-channel and multi-channel transceiver embodiments. An advantage of being small and low cost is that the transceiver can be installed in places and in quantities that are not possible or practical for larger devices. For example, an attribute of being small is that the transceiver may operate for long periods of time off of battery power, and thus may be used in remote locations where commercial power service (e.g., electrical wall outlets) are not available (e.g., on top of flagpoles, buildings, and mobile platforms, such as cars, airplanes, etc.) Such applications might include two-way smoke detection, strobe light and/or sounder control, two-way keypad, two-way thermostate, remote auto-dialer, remote sensor/controller, two-way remote meter reading/power cut-off, and process control/energy management.

Using a battery operated remote transceiver (BORT) creates problems with feasibility of use and battery life. Conserving battery life is a challenge for battery operated transceivers that may be located in accessible locations where it is difficult to replace the batteries. Conventional transmitters conserve power by operating in sleep modes where the transmitter alternately sleeps, wakes up, transmits, and then returns to sleep. These transmitters are not restricted to transmit on any particular schedule and thus do not care when they transmit, because these transmitters assume that a receiver is continuously available (powered on).

So as to maximize battery life in the BORT, the BORT will go into alternate sleep and active cycles, which in turn creates an additional difficulty when the BORT is used in a network setting. As will be discussed, to maintain network coherency, the transceivers must be active during predetermined windows of time (i.e., scheduled events). Otherwise, one device in the network may transmit while the would-be receive devices are in sleep mode, resulting in lost data messages. To maintain this network coherency, a 'system' transceiver (or alternatively, multiple system transceivers) will be active all of the time and will be powered by a continuous external power supply and will periodically generate a network synchronization message. The maximum period between these synchronization message transmissions is adjustable, but is set according to the frequency drifts of the system transceiver and the respective BORT devices. During normal operation a BORT device will communicate with a single system transceiver. Over successive communication periods, the BORT device can narrow the frequency ambiguity between itself and its assigned system transceiver. This technique will allow the BORT device to increase its receiver sensitivity and increase its process gain (and provide additional isolation from transmitters).

For efficient power consumption, each BORT device turns off its RF front-end (905 in Figure 9) and signal processing sections (907, 909, 911, 913, 915, 917, and 919, in Figure 9) when not in use. Upon a wake-up event and once a full power-up condition is completed, the BORT device will pause until the analog components in the RF section have had time to settle. The BORT device then samples only enough data to make network synchronization and trip decisions, and then disables power to the RF front-end 905. If the trip threshold decision is made, the BORT device will re-apply power to the RF front-end 905, use the data to determine code phase coherency, and then re-acquire the data signal. This acquisition process uses a fast search process as previously described, but if no signal is detected, the BORT device must reacquire system timing, which it does by remaining active and continuing to acquire data samples until a network synchronization pulse is detected. Alternatively, the BORT device can query the system transceiver, by transmitting a query message, requesting network timing information.

Figure 68 depicts a BORT application where several system transceivers 6811-6813 maintain communication with a plurality of BORT devices 6801-6803. A system controller 6820 maintains supervision of the system transceivers via multi-drop bus 6825, such as an RS-485 bus or the like.

The transceivers 6811-6813 and BORT devices 6801-6803 have access to 6 code-division multiple access (CDMA) channels, based on 6 unique PN sequences. The network uses CDMA channel 1 for ALOHA-type transmissions 6832, 6833, and the system transceivers use CDMA channel 2 to broadcast system synchronization messages 6830. A phase of the PN sequence will be random throughout the system transceivers, so as to allow all transceivers to broadcast the synchronization message simultaneously. This method allows fast signal acquisition without undue destructive self-interference due to the fact that the correlation function is only one chip wide. The respective BORT devices 6801-6803 will then acquire the transmitted signals that, in all likelihood, are the first to produce a Trip event. CDMA channels 2 and/or 3 are used by the system transceivers 6811-6813 to broadcast commands 6831 to the BORT devices 6801-6803.

Figures 69A-B depict the signal timing of the BORT network. The system transceivers 6811-6813 (Figure 68) issue synchronization messages 6901, 6902 every 5 seconds. Due to a 100 parts per million (ppm) inaccuracy of the crystals and a 7.8 ms inaccuracy of the sleep timer circuit on the BORT device, the synchronization (sync) message must be at least 8.3 ms long. Alternatively, a sleep timer circuit with no inaccuracy allows this value to be reduced to 500 μs to cover only the timing ambiguity of the crystal drift, less if the drift is tracked using a delay-lock loop (DLL).

Within this synchronization window, the BORT device will power up at a time 6910 (Figure 69B) from a low-power sleep mode. After device initialization, the BORT device will sample one code period of data at time 6911 and then go off-line at time 6912. After performing the fast search and fine search algorithms, the BORT device will reacquire the signal at time 6914 and wait until the end of the

synchronization signal 6916. The BORT device will measure and store the duration of the received synchronization signal. By keeping a running log of the signal duration, the BORT can determine if its wake-up timer is moving relative to the system synchronization timing. If so, the BORT device can then make corrections to its wake-up timer so as to better maintain system coherency.

The system transceivers 6811-6813 have multiple options after the completion of the sync message at time 6916. If no commands need to be transmitted to the BORT devices 6801-6803, the transceivers 6811-6813 will key-off their transmitters (i.e., stop transmitting). If commands need to be transmitted to the BORT devices 6801-6803, the system transceivers 6811-6813 will transmit the command immediately following the synchronization message 6904. If one of the BORT devices 6801-6803 is actively tracking the synchronization message and then fails to detect a spread spectrum signal at this time, that BORT device will decide that no commands are pending. After performing system housekeeping duties, the BORT device will go immediately into sleep mode at time 6917. However, if the BORT device is tracking the synchronization message and detects the beginning of a command message 6918, the BORT device remains active to receive the command and carry out the system command 6920. After completion of the task, the BORT device may optionally transmit an acknowledge (ACK) message 6922 via an ALOHA messaging protocol, and then after performing system housekeeping duties, the BORT device will enter a sleep mode at time 6924.

Other signaling protocols may be used so as to avoid synchronization message collisions from other system elements that can fill in the ASK key-off window and force a needless command search. To eliminate this needless command search, commands are transmitted on CDMA channel 3. After the completion of the synchronization message 6916 on CDMA channel 2, the BORT device will switch to CDMA channel 3 and sample one code period of data. The BORT device will then perform a fast search as before. If a signal is detected on CDMA channel 3, the BORT device will perform fine search and receive and process the command as before. If no signal is detected on CDMA channel 3, then the BORT device will enter sleep mode. This alternative is preferred if the network modulation convention is ASK. So as to have adequate time for the BORT device to perform the search algorithms on the initial CDMA 3 transmission, the transceiver pauses for 700 ms prior to transmitting command message 6904.

Alternatively, the system transceivers 6811-6813 can maintain code phase coherence when changing from CDMA channel 2 to CDMA channel 3. In this manner, the BORT devices 6801-6803 may achieve instant spreading code synchronization with CDMA channel 3 codes since there will be no code phase ambiguity.

Alternatively, protocol messages may also be used to maintain system coherency. If one of the the BORT devices 6801-6803 wakes up and does not detect a system sync message on CDMA channel 2, then that BORT device may send a 'not acknowledge' (NAK) message to the system transceivers 6811-6813

on CDMA channel 1. Upon receipt of the NAK message, the closest of the system transceivers 6811-6813 will transmit a timing correction message to the BORT device on CDMA channel 1. The BORT device will adjust its sleep timer accordingly, and may or may not reply to the transceiver with an ACK message on CDMA channel 1. The BORT device will then go into sleep mode and wake up during the next available system sync message.

From the following expression it is clear that the impact of system synchronization loading on ALOHA availability is minimal:

(8.3 ms/5 sec) * 100% = .17% vs. (500 us/5 sec) * 100% = .01%.

The system controller 6820 can send commands to the system transceiver of the system transceivers 6811-6813 nearest the desired BORT device of the BORT devices 6801-6803 at any time. This command will be queued and sent behind the next sync pulse; the system controller 6820 creates the timing and gives the command to initiate the sync pulse.

Some destructive interference occurs due to multiple system transceivers sending simultaneous sync pulses, although simultaneous transmission is nonetheless used so as to reduce loss of ALOHA air time. This approach is preferred over an alternative approach of assigning each system transceiver 6811-6813 an independent time slot.

The BORT system, or network, includes two types of devices, namely the BORT devices 6801-6803 and the system transceivers 6811-6813, each of which may include the single channel or the multi-channel transceivers of the first and second embodiments, respectively. A flowchart explaining the control process implemented in respective processors in the BORT devices 6801-6803 begins in Figure 70A. The process begins in step 7001, where one of the BORT devices 6801-6803 is in a low-power sleep state, and then the process continues to step 7002, where the BORT device powers up into an active state based upon a wake-up signal provided by a wake-up timer that is preferably contained in the BORT device. In step 7003, the BORT device executes a coarse search process on CDMA channel 2, where the steps for this coarse search routine begin in step 7070, continuing in step 7071 where the device powers up the RF section on the CDMA channel provided by the calling routine. The BORT device will then acquire a data sample in step 7072 and power down its RF front-end in step 7073. The BORT device will then perform a fast serial search in step 7074 and return to the calling routine in step 7075.

Subsequent to the coarse search in step 7003, the BORT device makes a trip event decision in step 7004. If in step 7004 it was decided that a trip event occurred, the process proceeds to step 7005 where the BORT device powers up its RF front-end for reception on CDMA channel 2 and demodulates the data message in step 7006. In step 7007, the BORT device determines whether or not the BORT device acquired a synchronization message. If a synchronization message was present, the BORT device performs an additional coarse search on CDMA 3 (in steps 7008 and 7009) and then searches for an additional data

message in step 7020, which is continued in Figure 70B. If the respective condition of either step 7004 or step 7007 is not met, the BORT device has become active and has not detected a valid synchronization message, and so control is then passed to step 7010.

If the BORT device is receive only, the BORT device remains active, repeating steps 7003 through 7006 until a subsequent synchronization message is detected, satisfying the condition of step 7007. From step 7010, if the device has transmit capability, then the device has the option to power up its RF section in step 7011 in preparation for transmitting a handshaking message. The process then proceeds to step 7012 where the BORT device initiates a handshaking protocol with a system transceiver on CDMA channel 1 to acquire system timing information and then proceeds to step 7060, which is the beginning of a shutdown routine.

This shutdown process is explained in reference to Figure 70B where the shutdown routine begins in step 7060 and continues to step 7061, where the RF front-end is powered down. Subsequently, in step 7062, the BORT device sets the low-power sleep timer correctly so that the BORT device will awaken during the next network synchronization period. Other tasks are performed as necessary to minimize sleep current loading and to assist the BORT device in its subsequent wake-up interval. Finally, the shutdown process proceeds to step 7063 where the BORT device enters a low-power sleep state.

Step 7020, shown in Figure 70B, initiates a data message search process which occurs after the BORT device has performed a coarse search, as was discussed in reference to step 7007 in Figure 70A. If a trip condition is met in step 7021, the BORT device starts a message timer in step 7022 and receives and demodulates the message in step 7023. Next, in step 7024 the BORT device verifies that the incoming message was intended for that device. If that BORT device was the intended recipient of the message, the process continues to step 7025 where the BORT device verifies that the incoming message was valid. If the message was valid, then the process continues to step 7026 where the BORT device transmits an acknowledgment on CDMA channel 1 and then in step 7027 responds to any commands that were embedded within the message. The process then proceeds to step 7028, where BORT device determines if there are any outgoing messages to be transmitted to the system transceivers 6811-6813. From step 7021, if the BORT device does not detect any incoming messages from the system transceiver, then process flow also passes to step 7028. Also from step 7024, if the BORT device determines that it was not the intended recipient of any incoming messages, then the process proceeds to step 7028, where the BORT device determines if there are any outgoing messages that are to be transmitted to the system transceivers 6811-6813. If not, the process continues to step 7060, which initiates the shutdown procedure. If there are one or more messages to be transmitted to the system transceivers 6811-6813, the BORT device will initiate preparations for transmission in step 7029.

From step 7026, if the received message had an error, the process proceeds to step 7032 where the device determines if the message timer has expired. If the timer has expired, then the BORT device will quit (e.g., time out) and pass control to step 7028. If the timer has not expired, the BORT will send a "not acknowledge" command on CDMA 1 (step 7033). The process then proceeds to step 7034 where the device performs a coarse search on CDMA channel 1. In step 7035, if no trip condition is met, then the device performs the steps of 7033 and 7034 until either a trip condition is met or the timer expires. If a trip condition is met in 7035, the process proceeds to step 7036 where the BORT device will apply power to its RF front-end on CDMA channel 1 and demodulate the message in step 7037.

In step 7038 the BORT device verifies that the incoming message was intended for that device. If the BORT device was the intended recipient of the message, the process continues to step 7039 where the BORT device verifies that the incoming message was valid. If the message was valid, the process continues to step 7026 where the BORT device transmits an acknowledgment on CDMA channel 1. If the conditions of either steps 7038 or 7039 are not met, then process control is returned to step 7032.

From step 7029, the device will power down its RF front-end and then seed a random timer as shown in step 7030. After the timer determines the time corresponding to the seed expires in step 7031, the process continues in step 7040, as will be discussed in reference to Figure 70C. The process continues in step 7042, where the BORT device powers up its RF front-end with channel CDMA 1 settings as its default settings. The BORT device is configured so that an external event (step 7080) can cause the device to awaken from sleep mode (step 7041) and power up its RF section in CDMA channel 1 (step 7042). The device will start its message timer in 7043, and then transmit the outgoing messages in step 7044. At this point, the BORT device is expecting an acknowledgment from the system transceiver. In step 7045, the device performs a coarse search on CDMA channel 1. The process proceeds to step 7046, where a trip decision is made. If a trip occurred, the BORT device will receive and demodulate the message in 7047 and then verify that the incoming message was intended for that device in 7048. If the device was the intended recipient of the message, the process continues to step 7049 where the device verifies that the incoming message was valid. If the message was valid, then the process continues in step 7050 where the BORT device verifies that the message was an acknowledgment message from the system transceiver. If the message was a valid acknowledgment message, then the device will clear its outgoing message queue in 7051 and then enter shutdown mode in 7060. Note that if the conditions of steps 7046, 7049, or 7050 are not met, then the process proceeds to step 7052 where the device determines if its message timer has expired. If the message timer has not expired, then process control returns to step 7044. Otherwise, control is passed to 7053, where the BORT device transmits an error message and then proceeds to step 7060, which initiates the shutdown routine.

A flow diagram for the processes implemented in the system transceivers 6811-6813 begins in step 7102 of Figure 71A and continues to step 7104 when a command is received from the system controller 6820 (from Figure 68) to broadcast a synchronization pulse. As a background task in step 7100, the transceiver monitors the system bus 6825 and queue all messages that need to be transmitted to the BORT devices 6801-6803. From step 7104, the process proceeds to step 7106 where the transceiver transmits a synchronization pulse on CDMA channel 2. After the synchronization pulse has completed, the transceiver checks its message queue in step 7108 to see if there are any messages to be transmitted to the BORT devices 6801-6803. If there are messages to be transmitted, the transceiver will switch to CDMA channel 3 in step 7112 and then start a message timer in step 7114. The transceiver will then transmit the message to the BORT device and pause long enough for the BORT device to respond (steps 7116, and 7117). If an acknowledgment is received in step 7118, the transceiver clears its message queue for that particular BORT device step 7120 and then the proceeds to step 7110, (as will be discussed in reference to Figure 71B). From step 7118, if the transceiver does not receive an acknowledgment from the BORT device, it will then check to see if the message timer has expired. If the timer has not expired, control is returned to step 7116, where the message is retransmitted to the BORT device. If the timer has expired, control is passed to step 7110 (Figure 71B).

In Figure 71B, the process continues to step 7130, where the system transceiver monitors CDMA channel 1 for incoming messages from the BORT devices 6801-6803. The transceiver remains in this loop until in step 7132 it is determined that either a message is received in step 7134 or (as was discussed in reference to Figure 71A) the transceiver receives a message from the system controller to transmit a synchronization pulse (step 7104). In step 7134, the transceiver starts its message timer and then in step 7136 transceiver receives and demodulates the message. Decision step 7138 determines whether or not the message was valid. If the message was invalid, the process proceeds to step 7140 where the transceiver transmits a "not acknowledgment" message. If the message timer has expired (step 7142), then process control returns to step 7130 to monitor for additional messages. Otherwise, process control returns to step 7136 to attempt to re-acquire the message. From step 7138, if the message was valid, the transceiver will transmit an acknowledgment message (step 7144) and respond to the message if necessary (step 7146). If there is any queued message for this particular BORT device, process control returns to step 7150 (as is seen in Figure 71A), otherwise, control is returned to step 7130.

Figures 72, 73, 74, 75, 76 and 77 show an alternative time division multiple access-based (TDMA) system/network architecture for the BORT devices. The following discussion explains the low level operation of the BORT system devices, as were previously discussed.

Figure 72 shows a steady state communication timing diagram between a system transceiver and a BORT device for three types of messages. The term steady state means that these are messages used for

normal exchange of information in three modes of operation. Initialization and exception handling will be discussed following the steady state discussion.

The system architecture is configured to minimize power drain at the BORT device. A significant amount of battery power is expended in the BORT device whenever it receives RF energy or transmit messages; a modest amount of battery power is expended whenever the BORT device is active, but has selected circuitry in a reduced power state, examples including initialization, Fast Serial Search as discussed earlier, and sleep mode preparation; and a minimum amount of battery power is expended while the BORT device is in sleep mode because the only active circuit is a low power oscillator and counter. The overall system architecture is configured to maintain positive control of the BORT devices with recovery mechanisms for re-establishing a communication link in the event of a lost message due to timing error or interference.

In order to minimize BORT power, the system transceivers behave predictably over time, and as discussed before, the BORT devices wake up on a schedule so as to retrieve a system sync message. To this end, one approach is for the system controller to manage the synchronization process, which is a different approach than pre-arranged options such as staggered, coincident or interleaved system transceiver sync intervals. As an exemplary embodiment, the system sync interval is fixed at 5 seconds with all transceivers interleaved and timing controlled by the system controller. Other options are also available, the preferences for each option depending on implementation trade-offs including consideration of on-air time, probability of receipt based on interleaved system controllers and asynchronous neighbor interference.

Figures 72A-C respectively show three messages which are all used to maintain sync with the system transceiver. The sync message is the most common system message (Figure 72A), where this message occurs once every sync interval, 5 seconds for the purposes of this discussion. The top line, labeled "System Xcvr" shows the system transceiver sync message as transmitted. The bottom line shows relatively timing of the BORT device receiving the sync message. The transmitted sync message contains a leader 7202 which has sufficient duration to compensate for all timing errors in the wake-up process in the BORT device. The leader 702 contains copies of the spreading code, and the leader 7202 is followed by a sync data pattern 7204, a message type data pattern 7206, a transceiver identification (ID) data pattern 7208 and a cyclical redundant check (CRC) which serves to qualify the data message as non-corrupted. Each of the data fields may be of length necessary to satisfy system requirements. The BORT device wakes up based on a stored parameter in the previous sync interval, initializes and powers up the necessary sections of the device and collects one code period of data during time interval 7214 before shutting down the receive gain circuits for search 7215, fast serial or fast parallel search method as previously discussed. Following search, the BORT re-energizes the receive circuits, performs fine search, diversity search and begins demodulating data waiting for the sync data pattern 7216. Once the sync data

pattern has been received, the BORT device calculates the actual wake-up time based on the time difference from initial search to sync data pattern. This information will be used later to calculate the next sleep interval. The BORT device continues to demodulate the remaining data 7218, detecting the message type and transceiver ID. The message type data field instructs the BORT device that the message is for sync only and no further action is required. The transceiver ID data field instructs the BORT device that it is accurately tracking the same system transceiver and has not drifted off with another transceiver. A positive lock for system integrity is therefore established by the BORT device without a need to energize a transmit circuit for the most common of system exchanges.

Figure 72B shows a second steady state communication exchange denoted as a Point to Point message between a system transceiver and a BORT device. This message may occur once every sync interval in place of a sync message. In normal operation this message is infrequent relative to the sync message by an order of magnitude. In this mode of operation, the system transceiver appends additional data to a sync message intended for a specific BORT device. It is assumed that the system controller maintains an allocation database for which BORT devices are slaved to which system transceivers. The allocation mechanism will be discussed later in the discussion of system initialization. The top line of Figure 72B shows the system transceiver transmit process followed by the receive process. The bottom line shows the BORT receive process followed by the acknowledge (transmit) process. As in the sync message, the system transceiver sends the Point to Point message leader 7222, followed by the sync 7226, message type 7228 and transceiver ID 7230 data patterns. But unlike the sync message, additional data is appended to include a BORT ID 7231 and optional data 7232 followed by the CRC 7234. The BORT device follows the normal wake-up process and samples a code repetition interval 7242, performs search processes and demodulates the message 7244. The BORT decodes the message as a Point to Point message, notes the transceiver ID and his BORT ID and responds with an acknowledge (ACK). The ACK follows similar structure including a leader 7246, followed by data fields of sync 7248, message type (ACK) 7250, BORT ID 7252, optional data 7254 and a CRC 7256. The system transceiver is always in listen mode when not transmitting, and so the transceiver detects the BORT acknowledge 7236 and demodulates the ACK 7238 completing the point to point exchange. The system controller either polls the ACK from the system transceiver or the transceiver initiates the interchange completing a positive handshake to the system controller.

Figure 72C shows a third steady state communication exchange denoted as an "All Call" message between a system transceiver and a BORT device. This message may occur once every sync interval in place of a sync message. In normal operation, this All Call message is very infrequent relative to any other system message. In this mode of operation, the system transceiver appends additional data to a sync message intended for any BORT device able to detect the message. This mode of operation is typically

reserved for emergency status when the BORT devices are required to become active and remain active until the emergency state is cleared. The top line of Figure 72C shows the system transceiver transmitting the All Call message followed by receiving the BORT ACK. The bottom line shows the BORT device receiving the All Call followed by transmitting the ACK.

As in the sync and Point to Point message, the system transceiver sends the All Call message leader 7260, followed by the sync 7262, message type 7264 and transceiver ID 7266 data patterns. The message may optionally include end-user data 7268 followed by the CRC 7270. Every BORT device slaved to the system transceiver issuing the All Call follows its normal wake-up process and samples a code repetition interval 7278, performs search processes and demodulates the message 7280. When the BORT decodes the message as an All Call message, the BORT notes the transceiver ID and responds with an acknowledge (ACK). A high potential for collision exists as all BORT devices are trying to ACK the message simultaneously. So as to reduce contention probability, a delay is initiated by the BORT prior to sending the ACK to stagger the respective replies to the system transceiver. The BORT calculates the delay 7282 based on the sync interval divided by the BORT ID (or a number of bits in the BORT ID) which staggers the BORT devices to assist in collision avoidance. The ACK data structure includes a leader 7284, followed by data fields of sync 7286, message type (ACK) 7288, BORT ID 7290, optional data 7292 and a CRC 7294. The system transceiver is always in listen mode when not transmitting 7272. The transceiver detects the BORT acknowledge 7273 and demodulates the ACK 7274 completing the communication exchange. The system controller either polls the ACK from the system transceiver or the transceiver initiates the interchange completing a positive handshake to the system controller.

Figure 73A and 73B show a flow diagram of the steady state processing corresponding with Figure 72. The steady state process begins in step 7300 where once per sync interval the BORT wakes up, performs a search in step 7302 and makes a decision as to whether a trip condition exists in step 7304. The coarse search step 7302 is implemented as a subroutine call which is shown starting in step 7380 where the receiver RF front-end components are energized in step 7382, one code repetition interval is sampled and stored in step 7384 and the RF front-end is de-energized prior to a fast serial search step 7388 where the correlation function is performed prior to returning, in step 7390, to step 7302. This coarse search subroutine is also called, as shown in Figures 75 and 77. Because the present portion of the process is a sync processing thread, the BORT device expects to find a trip condition, but if no trip condition is found, the BORT device assumes sync has been lost or the expected message was jammed and processing continues in step 7320 where the system transceiver is re-acquired. Re-sync operation will be discussed later as shown in Figures 76 and 77.

If a trip was found as expected, the receive thread is initiated in step 7306 and the BORT device performs fine search, waits for the sync byte in order to establish a time-tag for use later in setting the sleep

interval (in step 7308). The message is demodulated and data fields extracted. As the BORT device is attempting to maintain lock with one system transceiver, a check is made to determine if the message originated from the correct transceiver in step 7310. If the transceiver ID is not as expected, then synchronization with the desired transceiver is lost and a re-sync operation is performed in step 7318. If the transceiver ID is correct, then the BORT device has maintained sync and the message type is evaluated in steps 7312, 7314 and 7316.

If the message type does not match one of the three allowed steady state messages, the exception handler defaults to the re-sync function of step 7318. If the received message type is a standard sync message, the algorithm continues through steps 7324 and 7330 to 7332 where the time of sync byte relative to the wake up time is used in a digital lock loop in step 7334 to calculate the sleep time which will wake up the BORT device in the leader of the next sync message. The sleep timer is set in step 7336 and the BORT device enters a power down mode in step 7338 awaiting sleep timer wake up in the next sync interval.

If the received message was a Point to Point message in step 7314, the algorithm continues through steps 7326 and 7340 to 7342 where the BORT ID is evaluated in step 7342. If the received BORT ID matches the ID of the BORT device, the data bits are used to instruct the BORT on which function to perform in step 7344. An optional short delay is performed in step 7346 prior to a BORT ACK message in step 7348. The delay may be necessary to ensure the system transceiver is ready to receive the message, i.e. settling time for reversal of transmit to receive. Once the ACK has been sent, the BORT is ready to enter sleep mode and exits through the sync message process 7330 as discussed before. If the received message was an All Call message in step 7316, the algorithm continues through steps 7328 and 7350 to 7352 where the BORT performs the All Call function based on the message data in step 7352. The delay is calculated in step 7354 to stagger the BORT devices acknowledge messages and the ACK is sent in step 7356. The BORT then enters an extended search cycle continually searching in step 7358 looking for a new trip condition as step 7359. The BORT device does not sleep following an All Call reception. If a trip is found in step 7359, the process continues in the normal steady state processing thread at step 7306 through steps 7360 and 7322. In this manner, successive All Call messages are received and processed at whatever rate the system controller and transceiver desires. If the All Call condition is resolved, the system controller and transceivers send either a sync or Point to Point message where the BORT device enters a sleep mode following receipt.

The above discussion assumes the system is operating in a steady state mode. Exception handling and initialization are detailed below.

Figures 74A and B depict the system initialization sequence, where Figure 74A shows a timeline of two system transceivers, both being received by a BORT device on the lines shown in Figure 74B.

Transceiver A and Transceiver B of Figure 74A are shown staggered to demonstrate this process and the blocks on each line depict a complete transmitted or received message, solid blocks representing message steps in the acquisition flow. Each system transceiver continues to transmit sync messages 7402 and 7406 at a predefined system interval. The BORT device on power-up or initialization remains active continually searching at 7408 looking for a trip. Once a trip is found, the message is demodulated at times 7410, 7412 for a period so as to establish a good estimate of signal to noise ratio per system transceiver. A running average of SNR is maintained for several transceivers. This process is continued until at least four sync messages are collected from at least one system transceiver.

Once an estimate of SNR is complete, the BORT device nominates its selection to the system controller at time 7414 which contains as data the transceiver ID and SNR for the best of up to three system transceivers evaluated. All system transceivers hearing the nomination receive it at 7413, and 7415 and relay it to the system controller along with the SNR of receipt by the system transceivers. The system controller now has the SNR measurements relative to the BORT device and all system transceivers able to hear the BORT device where a determination is made as to allocation. The system controller allocates which system transceiver is associated with the BORT device and the chosen system controller relays this information to the BORT device at 7416. The BORT device continues to receive all messages following its nomination at time 7414 awaiting the allocation assignment which comes in the form of a Point to Point message at time 7416 from the system controller assigned. The BORT device receives the allocation Point to Point message at 7418 and acknowledges at time 7420 to complete the Point to Point exchange. The BORT device now has its transceiver ID and timing to enter sleep mode and enter steady state operation. If the allocation message at 7416 does not arrive within a predetermined time-out interval 7422, the BORT device assumes its nomination was not heard and re-issues it. Alternatively, the BORT may sleep for an extended period of time and attempt a new initialization, which may be a reasonable strategy for non-critical systems to compensate for extended power outages or system failures while preserving valuable BORT battery life.

Figure 75 is a flowchart of the above-described procedure, where upon wake-up or initialization determination in step 7500 an array of sync counters is initialized in step 7502 to keep track of how many sync messages have been received from a few system transceivers. The BORT device continues to search in step 7504 until a trip is found in step 7506 where the RF front-end section is re-energized in step 7508 and the message is captured and demodulated in step 7510. The RF front-end section is placed in a reduced power state in step 7516 and the message is evaluated to see if it is a sync type (repetitive) message in step 7518. If the message is not repetitive, it is not considered as the time tag captured will be used to seed the sleep timer and the BORT resumes search 7504. If the message is repetitive, the time information is stored in an array based on the transceiver ID 7520 since the decision as to which transceiver to use is not yet

made. In step 7522, a running average is made for the SNR of each transceiver being evaluated and a counter is incremented in step 7524 counting the number of sync messages received from a specific transceiver. If none of the counts exceed a predetermined number as determined in step 7526 the BORT resumes search in step 7504. If any of the counts exceed a predetermined number as determined in step 7526 the three best transceivers are selected based on SNR in step 7528 and a BORT nomination message is sent containing the transceiver ID and SNR for the best three candidates as observed by the BORT 7530.

A response time-out is started in step 7532 and the BORT searches continually in step 7534 until a trip is received in step 7536, the trip may or may not be the response expected. The RF front-end section is energized in step 7542 and the message is demodulated in step 7544 and considered in step 7546. If the message is not the expected response, the BORT device resumes search in step 7534. If the message is the response to the nomination, the allocated system transceiver ID is decoded from the data in step 7548 and stored for future reference in non-volatile memory. A Point to Point ACK is formed in step 7550 and sent and the BORT device enters sleep mode in steps 7552 and 7554. If while the BORT is waiting for a response at 7536 and not found, a time-out is incremented in step 7538 and evaluated at step 7540. If the time-out expires before the response is received the process starts over step 7502 (or alternatively the BORT device may enter an extended sleep interval to preserve battery conditions before resuming at step 7502).

If a BORT device detects loss of sync, it enters a re-sync mode depicted in Figures 76A-C and 77. Figure 76A depicts a first tier of re-sync where the BORT device initiates a negative acknowledge (NAK) exchange. If re-sync fails according to that method, the procedure according to Figure 76B is used as a second tier where the BORT device waits for the next sync message and resets. If re-sync fails according to that method, the procedure according to Figure 76C is used as a third and final tier where the BORT device eventually enters the initialization mode, discussed earlier.

In Figure 76A, the top line illustrates exemplary system transceiver activity at particular times such as sending sync messages 7602 and 7604, as shown. The BORT device processes the sync message at time 7608 but has a failure at time 7610 where the captured search interval does not coincide with the sync message of 7604. The same condition would exist if the system transceiver sync of 7604 were jammed relative to the BORT device. The BORT device initiates a NAK message 7612 and begins to immediately listen at 7616 for a NAK Reply 7614. When the system transceiver hears the NAK it repeats the previous message sent at the sync interval as a NAK Reply 7614 which includes a time value to the next scheduled sync message. The BORT device seeds the sleep mode timer and resumes normal processing at 7620. If the system controller fails to respond with the NAK Reply of 7614 or the BORT device cannot hear the NAK Reply, the BORT device continues to listen 7622 until the next sync message is heard at 7624 and

normal processing resumes. If the BORT device fails to reacquire by either the NAK or waiting for sync, the BORT assumes the transceiver has failed, and enters an initialization mode 7630 following a predetermined time-out at 7628.

Figure 77 is a flow diagram of the re-sync process starting at step 7700. In the normal wake-up process of Figure 73A a deterination is made that a re-sync is necessary (steps 7318 or 7320), thus initiating the re-sync process in step 7700, after which in step 7704, a wait time is calculated for generating a NAK message based on the BORT ID (or some number of bits of the BORT ID). The wait time is necessary to compensate for the situation where a jammer jams reception of the sync message to several BORT devices at the same time. By staggering their reply, the reliability, at the system level, of re-acquiring sync improves. The NAK is transmitted by the BORT device in step 7706 and a time-out interval is started in step 7708. The BORT device continually searches in step 7710 and upon finding a trip event in step 7712 energizes the RF front-end at step 7718 and demodulates the message in step 7720.

If the message received is the NAK Reply in step 7722, the sleep timer is seeded with a value to wake up the BORT device in the next sync interval in step 7726 based on the time value passed in the NAK Reply. The BORT system then enters a sleep mode in step 7728 and resumes normal operation. If the response received was not a NAK Reply, the response is evaluated to determine if the response is a standard steady state sync type message in step 7724. If so, the timer is set for a standard sync interval in step 7726 and the BORT device sleeps in step 7728. If the received message is neither a NAK Reply nor a sync message, the NAK time-out is incremented at step 7713 and evaluated at step 7714. While waiting for a NAK Reply in step 7712, the NAK time-out is incremented in step 7713 and evaluated in step 7714. If the NAK time-out expires, the BORT device enters the initialization mode 7716, 7500.

The mechanisms and processes set forth in the present description may also be implemented using a conventional general purpose microprocessor or digital signal processor (such as a TMS320C40, although, as discussed many of the inventive mechanisms and processes disclosed herein may be implemented in lower cost, lower performance processors) programmed according to the teachings in the present specification, as will be appreciated to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will also be apparent to those skilled in the relevant art(s).

The present invention thus also includes a computer-based product which may be hosted on a storage medium and include instructions which can be used to program a computer to perform a process in accordance with the present invention. This storage medium can include, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, magneto-optical disks, ROMs, RAMs, EPROMs,

EEPROMs, flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings, and in particular hybrids between the signal channel transceiver, multi-channel transceiver and BORT-based network embodiments. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

To this end, an exemplary single channel embodiment of a transceiver has been described as a first embodiment of the present invention (see e.g., Figures 9, 10, 11), and a multi-channel embodiment has also been described as a second embodiment (see, e.g., Figures 9, and 35-36), where features of the respective embodiments may be exchanged with one another, albeit for potential penalties of cost, performance and complexity, as has been discussed. Accordingly, the present invention is directed not only to the claims as individually described, but also directed to combinations of the claims and alternative mechanisms as discussed herein.

More particularly, the multi-channel transceiver and single channel transceiver may both use a one-bit limited ADC or a multi-bit linear ADC. The simplicity of the one-bit limited ADC does not require the AGC function as discussed in reference to the multi-channel embodiment, and Figure 35 for example, but the single channel embodiment could also use the multi-bit linear ADC, with AGC as discussed herein, although requiring additional processing power.

Both the single channel embodiment and the multi-channel embodiment have been explained with respect to particular examples given for decimation ratios, sampling rates etc. However, the approaches discussed for the single channel embodiment for digital downconversion-decimation, including the look-up table approach (see e.g., Figure 12), Boolean logic approach (see e.g., Figure 13) as well as coefficient-less approach, as discussed in the section entitled "Coefficient-less Down Conversation, Despread and Decimation in a DSP Processor" may also be implemented in the multi-channel embodiment.

While the discussion regarding DC removal with respect to Figure 35, was made in the context of the multi-channel embodiment, the discussion is equally applicable to the single channel embodiment in which a multi-bit linear ADC is also used. Regarding the techniques for compensating for decimation loss, both the digital offset approach discussed with respect to Figure 14, as well as the frequency offsetting of the first local oscillator, and cycling through various offsets, may be employed in either the single channel or the multi-channel embodiment. Simultaneously computing all the offsets was an option discussed herein, such an option may be more suitable for use in a multi-channel embodiment or a hybrid embodiment between the multi-channel embodiment and single channel embodiment due to processing complexity and cost concerns. As with the other alternatives, penalties paid are in terms of cost and complexity. Similarly, the averaging approach discussed with regard to improving trip sensitivity and limiting decimation loss may

also be employed in both the single channel and multi-channel embodiments, albeit for an increase in processing complexity. The set-on channel filter approach was discussed with respect to the multi-channel embodiment, see e.g., Figure 39, although it may also be applicable in the single channel embodiment, albeit at a more expensive computation cost to improve sensitivity and process gain during demodulation. The various fine search center of mass methods (see e.g, Figures 19-22 and DBPSK, as discussed with respect to Figures 31 and 32, for example), may be implemented in either the single channel or the multi-channel embodiment.

Both the single channel and the multi-channel embodiments are directed to direct sequence spread spectrum transceivers, that may be used in a system or network and both using a PN code as previously been discussed. The particular features of the PN code length, discussed with respect to Table 3, for example, is applicable to both the single channel and multi-channel embodiments. As was previously discussed, the selection of the PN code length, is an enabling feature regarding partial decimation as well as FFT radix based on small prime numbers, implemented in both embodiments.

Various other features have been discussed with respect to partial decimation in order to set a predetection bandwidth. While separate examples have been given with respect to the multi-channel and single channel embodiment, the present description should not be limited to only these particular descriptions, but rather other embodiments that will be extensions of the particular examples discussed herein, as well as devices which may be built in light of the present teachings.

Figures 30A-F have been presented in the context of the first embodiment, however, these approaches may be employed in either single channel or multi-channel embodiment, albeit for increased computational complexity as discussed herein. Figure 34 described a circuit for precharging a voltage controlled oscillator for fast settling acquisition, however, this circuit may also be used in the multi-channel embodiment as well, and any hybrid between the single channel embodiment and the multi-channel embodiment.

Figures 40-45, discussed various frequency domain code correlators, which were presented in the context of the multi-channel embodiment. However, provided sufficient processing resources are available, these approaches may also be implemented in the single channel embodiment so as to provide an FFT based down conversation despread and decimation operation subsequent decimation in the frequency domain may be used to expand or set the predetection bandwidth as necessary for system requirements. The fast serial search approach discussed with respect to Figures 15A-B and 16, for example, are equally applicable in the multi-channel receiver implementation. Likewise, various power management features of the inventive transceiver, as discussed with respect to Figure 9, the battery pack of Figure 10, and that as discussed with respect to the BORT, are equally applicable in a single channel or multi-channel transceivers.

Features regarding on-off keying, (see e.g. discussion regarding Figure 25, for example), may be applicable to either the single channel or multi-channel transceivers that use the one-bit limited ADC. The respective diversity approaches (antenna and frequency, for example, discussed with respect to Figures 9, 24-27, and Figures 68 (CDMA)), are applicable to both the single channel and multi-channel embodiment, and therefore are also applicable to hybrid embodiments. Likewise, the discussion regarding the BORT system and network (see e.g., Figures 67-77) are equally applicable to the single channel embodiment and the multi-channel embodiment, as either the single channel transceiver, multi-channel transceiver or a hybrid, may be employed in the BORT system/network. Furthermore, the discussion regarding the elimination of redundant data in a multi-drop network, (discussed with reference to Figure 67, for example) is also applicable to the single channel embodiment, as well as the multi-channel embodiment and any embodiment therebetween. Likewise, the discussion regarding predictive repositioning discussed with respect to Figures 66A-C, for example, as well as Figure 39, are applicable to both the single channel and multi-channel embodiment.

While a few examples of how the various features of the inventive transceiver have been discussed above, it should be understood that the above-described combinations are only a subset of those that are possible as a natural extension of the exemplary embodiments discussed herein. Therefore, the above-identified combinations should not be construed as being an exhaustive listing, but rather an exemplary set of combinations that are considered part of the invention.

CLAIMS:

What is Claimed is:

1. A direct sequence spread spectrum system comprising:

a transmitter configured to transmit a direct sequence spread spectrum signal, comprising,

a transmitter frequency reference that produces a frequency with a predetermined accuracy,

a spreading code generator that generates said spreading code with a predetermined transmit signal chipping frequency error and modulates a data signal with said spreading code to produce a spread data signal having a frequency error component attributable to said predetermined accuracy of the transmitter frequency reference,

a radio frequency generator that produces a radio frequency signal having a frequency error attributable to said predetermined accuracy of said frequency reference, and

a transmitter signal combiner configured to receive and combine said radio frequency signal and said spread data signal to produce the direct sequence spread spectrum signal; and

a receiver configured to extract said data signal from said direct sequence spread spectrum signal transmitted from said transmitter, comprising,

a receiver frequency reference that produces a frequency with another predetermined accuracy,

a code generator that generates said spreading code, said spreading code having a receiver chipping frequency error component,

a receiver radio frequency generator configured to produce a downconversion signal derived from said frequency of said receiver frequency reference, said downconversion signal having a frequency error attributable to said predetermined accuracy of said frequency from said receiver frequency reference,

a receiver signal combiner that combines the direct sequence spread spectrum signal with the downconversion signal to produce a translated signal, said translated signal including said frequency error of said transmitter radio frequency signal error component and the downconversion signal error component,

a sampling device that samples the translated signal at a frequency that is four times a center frequency of the translated signal to produce a sampled signal,

a despreading and downconverting combiner coupled to the code generator and configured to despread and downconvert the sampled signal, comprising,

a sign inversion mechanism that inverts a sign of respective samples of said sampled signal so as to despread and downconvert said sampled signal, and

at least one data signal detector configured to detect the data signal, a composite bandwidth of said at least one data signal detector being in a range including a data signal bandwidth and a frequency uncertainty bandwidth of said signal due to at least the predetermined accuracy of the transmitter frequency reference.

2. The system of Claim 1, wherein said receiver comprises at least one of a single channel receiver and a multi-channel receiver.

3. The system of Claim 1, wherein said predetermined accuracy of said transmitter frequency reference causing said frequency error of the radio frequency signal and said transmit signal chipping frequency error to be not independent of one another, said transmit signal chipping frequency error inducing a performance degradation at said receiver due to a time dependent reposition error.

4. The system of Claim 1, wherein:

said transmitter frequency reference comprises means for producing the frequency with the predetermined accuracy;

said spreading code generator of said generator comprises means for generating said spreading code ;

said radio frequency generator comprises means for producing said radio frequency signal;

said transmitter signal combiner comprises means for producing the direct sequence spread spectrum signal;

said receiver frequency reference comprises means for producing said frequency with another predetermined accuracy;

said code generator of said receiver comprises means for generating said spreading code having said receiver chipping frequency error component;

said receiver radio frequency generator comprises means for producing said downconversion signal;

said receiver signal combiner comprises means for combining the direct sequence spread spectrum signal with the downconversion signal to produce the translated signal;

said sampling device comprises means for sampling the translated signal at the frequency that is four times the center frequency of the translated signal so as to produce the sampled signal; and

said despreading and downconverting combiner comprises means for despreading and downconverting the sampled signal, comprising,

means for sign inverting the sign of respective samples of said sampled signal so as to despread and downconvert said sampled signal, and

means for detecting the data signal, the composite bandwidth of said at least one data signal detector being in the range including the data signal bandwidth and the frequency uncertainty bandwidth of said signal due to at least the predetermined accuracy of the transmitter frequency reference.

5. A method for implementing in a receiver digital downconversion and decimation on a received signal represented by a serial stream of data samples, comprising the steps of:

decimating said serial digital data by using a subset of said data samples to form a parallel digital data set and using said parallel digital data set as an input indica to a database mechanism configured to produce a baseband data sample that corresponds to the input indica;

downconverting said non-baseband signal by producing the baseband data sample that corresponds with said parallel digital data set; and

outputting the baseband data sample as a component of a baseband signal that corresponds with said received signal.

6. The method of Claim 5, wherein:

said decimating step comprises using said parallel data set as the input indica to the database, and implementing said database in at least one of a boolean logic circuit and semiconductor memory.

7. The method of Claim 5, wherein said downconversion step comprises complex downconverting with inphase and quadrature components.

8. A receiver comprising:

a digital downconverter and decimator that downconverts and decimates a received signal represented by a serial stream of data samples, comprising,

means for decimating said serial digital data by using a subset of said data samples to form a parallel digital data set and using said parallel digital data set as an input indica to a database mechanism configured to produce a baseband data sample that corresponds to the input indica;

means for downconverting said non-baseband signal by producing the baseband data sample that corresponds with said parallel digital data set; and

means for outputting the baseband data sample as a component of a baseband signal that corresponds with said received signal.

9. A method for simultaneously downconverting and applying a spreading code to a direct sequence spread spectrum signal, said spreading code having previously been used by a transmitter to spread a data signal at a predetermined chip rate, comprising the steps of:

sampling said signal at a sampling rate, Fs, to produce data samples, wherein said sampling rate, Fs, being four times a center frequency of said sampled signal, Fs being a multiple, M, of the code chip rate, M having a value of at least 1 and representing an oversample ratio;

downconverting and despreading respective samples in a signal signing step comprising,

inverting a sign value of one of said data samples if a product of a downconversion coefficient and a despreading code coefficient is negative, not inverting if said product is positive, and zeroing said data sample if said product is zero.

10. The method of Claim 9, wherein said downconverting and despreading step comprises:

assigning a value of 1 to respective downconversion coefficient that coincide in time with a positive maximum value of a sinusoid having a frequency equal to the center frequency of said sampled signal,

assigning a value of 0 to respective downconversion coefficients that coincide in time with a zero crossing at said sinusoid; and

assigning a value of -1 to respective downconversion coefficients that coincide in time with a negative maximum of said sinusoid.

11. A receiver configured to simultaneously downconvert and apply a spreading code to a direct sequence spread spectrum signal, said spreading code having previously been used by a transmitter to spread a data signal at a predetermined chip rate, comprising:

means for sampling said signal at a sampling rate, Fs, to produce data samples, wherein said sampling rate, Fs, being four times a center frequency of said sampled signal, Fs being a multiple, M, of the code chip rate, M having a value of at least 1 and representing an oversample ratio;

means for downconverting and despreading respective samples in a signal sample signing means comprising,

means for inverting a sign value of one of said data samples if a product of a downconversion coefficient and a despreading code coefficient is negative, not inverting if said product is positive, and zeroing said data sample if said product is zero.

12. A method for suppressing self-interference of a signal subjected to a digital decimation process in a receiver, comprising the steps of:

inputting said signal as digital data samples at a predetermined sample rate, respective of said digital data samples including a direct current error component;

approximating the direct current error component by combining at least a subset of said digital data samples;

decimating said digital data samples and producing decimated data samples at another predetermined sample rate that is lower than said predetermined sample rate of said digital data samples, wherein said decimating step applies a decimation gain to respective of the decimated data samples and enhances said direct current error component in respective of said decimated data samples;

identifying said decimation gain;

calculating a correction factor by combining the direct current error and the decimation gain for each decimation block; and

subtracting the correction factor from at least one of the decimated data samples so as to suppress a self-interference effect on the signal of the direct current error component after being enhanced by the decimating step.

13. The method of Claim 12, wherein said approximating step comprises approximating the direct current error component by calculating in a processor a mathematical means so as to determine an average.

14. The method of Claim 12, wherein said identifying step, comprises retrieving predetermined decimation gains from a look-up table.

15. A receiver for suppressing self-interference of a signal subjected to a digital decimation process, comprising:

means for inputting said signal as digital data samples at a predetermined sample rate, respective of said digital data samples including a direct current error component;

means for approximating the direct current error component by combining at least a subset of said digital data samples;

means for decimating said digital data samples and producing decimated data samples at another predetermined sample rate that is lower than said predetermined sample rate of said digital data samples, wherein said means for decimating applies a decimation gain to respective of the decimated data samples and enhances said direct current error component in respective of said decimated data samples;

means for identifying said decimation gain;

means for calculating a correction factor by combining the direct current error and the decimation gain for each decimation block; and

means for subtracting the correction factor from at least one of the decimated data samples so as to suppress a self-interference effect on the signal of the direct current error component after being enhanced by the means for decimating.

16. A method for removing ambiguity from an automatic gain control signal used to control a signal level of a received signal in a receiver, said receiver not configured to maintain an overflow indication for successive processing steps when an overflow result occurs therein, comprising the steps of:

adjusting a signal level control mechanism to position the signal level of the received signal to within a dynamic range of an analog-to-digital converter that converts the received signal into a corresponding digital signal;

inputting the received signal to the analog-to-digital converter;

determining a level of the received signal input to the analog-to-digital converter and detecting that the level is not within a predetermined portion of the dynamic range of the analog-to-digital converter, comprising the steps of,

sequentially adjusting said signal level from a minimum gain to a maximum gain when said level is detected as not being within the predetermined portion of the dynamic range,

identifying a noise power during while sequentially adjusting said signal level,

and

stopping said sequentially adjusting step at a gain setting that produces a minimum noise power; and

performing a digital signal operation on said digital signal using a signal processing element which does not maintain the overflow indication.

17. A method for reducing signal loss caused by decimating a digital signal in a receiver with a decimation operator having a predetermined bandwidth, a response characteristic of said decimation operator imparting a greater amount of attenuation in a first part of said bandwidth than in a second part of said bandwidth, comprising the steps of:

receiving said signal with said receiver, said receiver employing a receiver frequency reference that operates within a predetermined accuracy;

decimating said signal with said decimation operator to reduce a sample rate of said signal, where a position of said signal in said predetermined bandwidth being influenced by a frequency offset between a transmitter frequency reference and said receiver frequency reference;

determining an amount by which said signal is removed in frequency from said second part of said bandwidth and whether said amount is greater than a predetermined standard; and

adjusting a signal downconversion operation by an amount and a direction sufficient to reposition said signal within said second part of said bandwidth, when said determining step determines that the amount by which the signal is from the second part of said bandwidth is greater than said standard.

18. The method of Claim 17, wherein said determining step comprises calculating a magnitude and a direction of the frequency offset relative to said second part of said bandwidth.

19. The method of Claim 17, wherein said adjusting step comprises substituting a baseband downconversion coefficient set with another set that translates said signal to within said second part of said bandwidth.

20. The method of Claim 17, wherein said determining step comprises determining a center of said bandwidth as being said second part of said bandwidth, and a band edge as being said first part of said bandwidth.

21. A receiver that reduces signal loss caused by decimating a digital signal with a decimation operator having a predetermined bandwidth, a response characteristic of said decimation operator imparting a greater amount of attenuation in a first part of said bandwidth than in a second part of said bandwidth, comprising:

means for receiving said signal and a receiver frequency reference that operates within a predetermined accuracy;

means for decimating said signal with said decimation operator to reduce a sample rate of said signal, where a position of said signal in said predetermined bandwidth being influenced by a frequency offset between a transmitter frequency reference and said receiver frequency reference;

means for determining an amount by which said signal is removed in frequency from said second part of said bandwidth and whether said amount is greater than a predetermined standard; and

means for adjusting a signal downconversion operation by an amount and a direction sufficient to reposition said signal within said second part of said bandwidth, when said means for determining determines that the amount by which the signal is from the second part of said bandwidth is greater than said standard.

22. A method for reducing signal loss caused by decimation in a receiver of a direct sequence spread spectrum signal transmitted from a transmitter, said decimation having associated therewith a predetermined bandwidth and response characteristic, said response characteristic imparting a greater amount of attenuation in a first part of said bandwidth than in a second part of said bandwidth, comprising the steps of:

receiving said signal with said receiver, said receiver employing a receiver frequency reference and said transmitter employing a transmitter frequency reference where the tolerances of the respective references combine to create a predetermined signal position uncertainty range in which said signal is positioned prior to demodulation of the signal;

decimating said signal with said decimation operator to reduce a sample rate of said signal;

subdividing said predetermined signal position uncertainty range bandwidth into a plurality of candidate downconversion frequency bands;

changing an amount by which a downconversion operator translates the signal toward the second part of said bandwidth, where said amount is set by assuming the signal is placed in one of the plurality of candidate downconversion frequency bands, attempting to correlate said signal with a spreading code used to spread the signal at the transmitter and determining whether correlation is achieved; and

repeating sequentially said changing step for the other channels and stopping said repeating step when said determining step determines that correlation is achieved.

23. The method of Claim 22, wherein:

said repeating step comprises performing said changing step for the other channels until the changing step has been performed for all of the channels;

said determining step comprises,

deciding that correlation is achieved after the changing step has been performed for all of the channels, and

determining which of the plurality of candidate downconversion frequency bands yielded the greatest correlation result.

24. The method of Claim 22, further comprising the step of using the selected downconverted frequency bands for subsequent data demodulation and resuming simultaneous course search following said subsequent data demodulation.

25. A receiver that reduces signal loss caused by decimation of a direct sequence spread spectrum signal transmitted from a transmitter, said decimation having associated therewith a predetermined bandwidth and response characteristic, said response characteristic imparting a greater amount of attenuation in a first part of said bandwidth than in a second part of said bandwidth, comprising:

means for receiving said signal using a receiver frequency reference, said transmitter employing a transmitter frequency reference where the tolerances of the respective references combine to create a predetermined signal position uncertainty range in which said signal is positioned prior to demodulation of the signal;

means for decimating said signal with said decimation operator to reduce a sample rate of said signal;

means for subdividing said predetermined signal position uncertainty range bandwidth into a plurality of candidate downconversion frequency bands;

means for changing an amount by which a downconversion operator translates the signal toward the second part of said bandwidth, where said amount is set by assuming the signal is placed in one of the plurality of candidate downconversion frequency bands, attempting to correlate said signal with a spreading code used to spread the signal at the transmitter and determining whether correlation is achieved; and

means for repeating sequentially said changing step for the other channels and stopping said repeating step when said determining step determines that correlation is achieved.

26. The receiver of Claim 25, wherein:

said means for repeating comprises said means for changing for the other channels until the means for changing has been performed for all of the channels;

said means for determining comprises,

means for deciding that correlation is achieved after the means for changing has operated on all of the channels, and

means for determining which of the plurality of candidate downconversion frequency bands yielded the greatest correlation result.

27. A method of filtering a digital signal with digital symmetric channel filters in a digital spread spectrum receiver, comprising the steps of:

providing a quadrature stream of data samples that include said signal, said quadrature stream of samples having a bandwidth equal to or greater than a frequency uncertainty range, said frequency uncertainty range being a frequency range in which said signal is contained although a precise location of said signal within said range is not a priori known because of a frequency difference between a frequency reference used in a transmitter that transmitted said signal and another frequency reference in the receiver that receives said signal;

calculating in positive channel and negative channel pairs a power in respective of a plurality of channels each having a bandwidth being less than said bandwidth of said quadrature stream of samples, comprising the steps of,

performing a quadrature sinusoidal transform for the positive channel and preserving intermediate product terms,

performing another quadrature sinusoidal transform for the negative channel that is symmetric to the positive channel using the product terms preserved in said preserving step, and

computing a direct current center channel filter power.

28. A method for limiting signal power loss in a channelized receiver having a receiver frequency reference with a predetermined tolerance and having a plurality of channels arranged within a predetermined bandwidth corresponding to a frequency uncertainty range in which a signal is present, said signal being transmitted by a transmitter having a transmitter frequency reference with another predetermined tolerance, respective amounts of the predetermined tolerances affecting a width of said frequency uncertainty range, comprising the steps of:

representing said signal as a stream of data samples at a predetermined sample rate having a corresponding bandwidth being not less than the frequency uncertainty range;

decimating said predetermined sample rate to create a lower sample rate and narrow a corresponding bandwidth to be less than respective widths of said plurality of channels;

arranging pairs of said channels, comprising,

arranging said channels in symmetric pairs about a center of said frequency uncertainty range, and

separating adjacent pairs of said channels non-uniformly, where an amount of separation is different for at least two of said adjacent pairs, so that a maximum signal loss due to said signal being positioned between two channels is less than that if said channels were symmetrically and uniformly spaced within said frequency uncertainty range.

29. The method of Claim 28, wherein said arranging step comprises arranging said channels using a discrete cosine transform.

30. The method of Claim 28, wherein said arranging steps comprises arranging said channels such that a maximum signal loss caused by a signal being positioned between two adjacent channels of said channels is approximately equal for each of the adjacent channel pairs.

31. A channelized receiver that limits signal power loss, comprising:

a receiver frequency reference with a predetermined tolerance;

a plurality of channels arranged within a predetermined bandwidth corresponding to a frequency uncertainty range in which a signal is present, said signal being transmitted by a transmitter having a transmitter frequency reference with another predetermined tolerance, respective amounts of the predetermined tolerances affecting a width of said frequency uncertainty range;

means for representing said signal as a stream of data samples at a predetermined sample rate having a corresponding bandwidth being not less than the frequency uncertainty range;

means for decimating said predetermined sample rate to create a lower sample rate and narrow a corresponding bandwidth to be less than respective widths of said plurality of channels;

means for arranging pairs of said channels, comprising,

means for arranging said channels in symmetric pairs about a center of said frequency uncertainty range, and

means for separating adjacent pairs of said channels non-uniformly, where an amount of separation is different for at least two of said adjacent pairs, so that a maximum signal loss due to said signal being positioned between two channels is less than that if said channels were symmetrically and uniformly spaced within said frequency uncertainty range.

32. A method for limiting signal power loss in a channelized receiver having a receiver frequency reference with a predetermined tolerance and having a plurality of channels arranged within a predetermined bandwidth corresponding to a frequency uncertainty range in which a signal is present, said signal being transmitted by a transmitter have a transmitter frequency reference with another predetermined tolerance, comprising the steps of:

representing said signal as a stream of data samples at a predetermined sample rate having a corresponding bandwidth being not less than the frequency uncertainty range;

decimating said predetermined sample rate to create a lower sample rate and narrow a corresponding bandwidth to be less than respective widths of said plurality of channels;

detecting a presence of said signal between respective channels of a pair of adjacent of said plurality of channels;

determining an amount of signal frequency offset relative to either one of said pair of adjacent channels by interpolating an amount of signal power present in said pair of adjacent channels;

positioning a set-on channel filter between said adjacent pair of channels, a center of said set-on channel filter being offset in frequency relative to either one of said adjacent pair by said amount determined in said determining an amount step; and

demodulating the set-on channel filter for data demodulation.

33. A channelized receiver that limits signal power loss, comprising:

a receiver frequency reference with a predetermined tolerance;

a plurality of channels arranged within a predetermined bandwidth corresponding to a frequency uncertainty range in which a signal is present, said signal being transmitted by a transmitter have a transmitter frequency reference with another predetermined tolerance;

means for representing said signal as a stream of data samples at a predetermined sample rate having a corresponding bandwidth being not less than the frequency uncertainty range;

means for decimating said predetermined sample rate to create a lower sample rate and narrow a corresponding bandwidth to be less than respective widths of said plurality of channels;

means for detecting a presence of said signal between respective channels of a pair of adjacent of said plurality of channels;

means for determining an amount of signal frequency offset relative to either one of said pair of adjacent channels by interpolating an amount of signal power present in said pair of adjacent channels;

means for positioning a set-on channel filter between said adjacent pair of channels, a center of said set-on channel filter being offset in frequency relative to either one of said adjacent pair by said amount determined in said means for determining an amount; and

means for demodulating the set-on channel filter for data demodulation.

34. A method in a direct sequence spread spectrum receiver for avoiding false pseudorandom noise code synchronization detection caused by spontaneous in-band interference, said receiver having a plurality of channels arranged within a predetermined bandwidth corresponding to a frequency uncertainty range due to frequency offset in respective frequency references in a transmitter and said receiver, comprising the steps of:

attempting to despread said signal by applying the pseudorandom noise code to said signal and outputting a stream of digital samples;

applying said digital samples to said channel filters;

determining respective energy amounts within said channel filters;

identifying which channel filter has a maximum energy amount therein;

determining a composite average power for a portion of all remaining channels except for the channel filter identified as having the maximum energy and a pair of channels being adjacent thereto;

determining if said maximum energy exceeds said average energy by at least a predetermined amount, and deciding that an alignment of said pseudorandom noise code and said signal is within two chip intervals of said pseudorandom noise code so that course synchronization is achieved if said maximum energy exceeds said average energy by at least a predetermined amount; and

performing fine search correlation and data demodulation if course synchronization is achieved and returning to said attempting step where said signal and pseudorandom noise code are shifted relative to one anther before being applied to one another.

35. A method for reducing code phase correlation error in a direct sequence spread spectrum receiver after a direct sequence spread spectrum signal and a pseudorandom code used to spread the signal at a transmitter have been aligned to one another within one pseudorandom code chip interval, comprising the steps of:

sampling said signal at a predetermined sampling rate and producing signal samples;

despreading said signal by applying said pseudorandom code to said signal samples and obtaining a despread signal;

determining a power of said despread signal, said power being an indication of how closely said signal and said pseudorandom code are aligned to one another;

identifying respective powers of despread signal for other relative pseudorandom code phases by,

despreading said signal by shifting a relative position of said signal and said pseudorandom code by less than said pseudorandom code chip interval,

determining said another of said respective powers of said despread signal, and

repeating said identifying step until all of said respective powers have been identified;

determining an operational positional alignment between said pseudorandom code and said signal samples by performing a center of mass operation on said power and said respective powers; and

despreading said signal using said operational positional alignment previously determined and demodulating said despread signal.

36. The method of Claim 35 wherein said step of determining an operational positional alignment comprises the steps of:

retarding a relative position of the pseudorandom code relative to the signal samples by at least ½ of said chip interval relative to an initial alignment position that caused said receiver to determine that said pseudorandom code and said signal are aligned to within one chip interval;

computing and storing said another signal power;

advancing the relative position by a fractional chip step, to compute one of the other signal powers; and

continuing said advancing step until said relative position of the pseudorandom code relative to the signal samples meets or exceeds one chip relative to said position in said retarding step; and

determining said operational positional alignment between said pseudorandom code and said signal samples by performing a center of mass operation on said power and said relative powers.

37. The method of Claim 36, wherein:

said retarding step and said advancing step combine to provide relative position alignments of -1/2, -1/4, +1/4 and +1/2 of a chip, and said determining a power step provides an initial signal power for a 0 relative position, thereby providing a first set of five signal powers corresponding respectively to relative position alignments of -1/2, -1/4, 0, +1/4 and +1/2 of a chip;

said performing a center of mass operation step comprises,

calculating a first center of mass of said first set of five signal powers,

determining if the first center of mass is greater than +1/4 chip offset, and if so performing the advancing step to identify respective signal powers for +3/4 and +1 chip offset and computing a second center of mass on a second set of five signal powers associated with the 0 +1/4, +1/2, +3/4, and +1 relative position alignments,

determining if the first center of mass is less than -1/4 chip offset, and if so performing the advancing step in a retarding direction so as to identify respective signal powers for -3/4 and -1 chip offset and computing a third center of mass on a third set of five signal powers associated with the -1, -3/4, -1/2, -1/4, and 0 relative position alignments; and

adjusting the relative phase to the operational positional alignment using said second center of mass if said first center of mass is determined to be greater than +1/4 chip offset, and adjusting the relative phase to the operational positional alignment using said third center of mass if said second center of mass is determined to be less than -1/4 chip offset.

38. The method of Claim 38, wherein:

said sampling step comprises,

decimating said signal samples to reduce a sample rate of said samples to coincide with a chip code rate of said pseudorandom noise code, said samples being a first set of samples,

obtaining a second set of samples offset by 1/4 of a chip interval of said code chip rate relative to said first set of samples; said second set of samples being provided at said sample rate,

obtaining a third set of samples offset by ½ of a chip interval of said code chip rate relative to said first set of samples, said third set of samples being provided at said sample rate, and

obtaining a fourth set of samples offset by 3/4 of a chip interval of said code chip rate relative to said first set of samples, said fourth set of samples being provided at said sample rate;

said retarding step and said advancing step combine to provide relative position alignments of -1, 0, and +1 of a chip, and further comprising the steps of,

determining respective signal powers of said second set of samples for chip offsets of -3/4 and +1/4 relative to said relative position alignment for said first set of samples;

determining respective signal powers of said third set of samples for chip offsets of -1/2 and +1/2 relative to said relative position alignment for said first set of samples;

determining respective signal powers of said fourth set of samples for chip offsets of -1/4 and +3/4 relative to said relative position alignment for said first set of samples; wherein

said performing a center of mass operation step comprises,

calculating said center of mass using said signal powers associated with said chip set offsets for said first set of samples, second set of samples, third set of samples and fourth set of samples.

39. The method of Claim 35, wherein:

said sampling step comprises sampling said signal at a multiple M of a chipping rate of said pseudorandom code;

decimating said samples to reduce a sample rate of said samples to coincide with the chipping rate;

adjusting the relative position by at least -1/2 of a code chip interval;

obtaining other data samples after said adjusting step, determining a signal power of said other data samples, and adjusting the relative position further by +1/M;

repeating said steps of obtaining, determining and adjusting until said relative position is offset by at least +1/2 of a code chip interval;

determining a center of mass for said signal powers for respective of said relative positions;

if the center of mass is greater than 1/M of a chip code interval,

collecting and measuring a set of additional signal powers for additional relative positions at a predetermined fractional increment, set of additional signal powers comprising elements between 0 and 1, and

determining another center of mass using said additional signal powers; and

adjusting said relative position by said center of mass if said determining step determines that said center of mass is not greater than 1/M of a chip code interval and adjusting said relative position by said another center of mass if said determining step determines that said center of mass is greater than a 1/M chip code interval.

40. The method of Claim 35, wherein:

said sampling step comprises sampling said signal at by an amount corresponding to a product of N and M, where N is a length of said pseudorandom code and M is a multiple of a chipping rate of said pseudorandom code;

obtaining sets of data samples, respective sets corresponding to respective of plural fractional chip interval length relative position adjustments; and

despreading respective of said sets of samples using a receiver spreading code generator configured to produce a code chip sample at a rate of (2 x M) +1, comprising the steps of,

offsetting the relative position by an amount and direction corresponding to -1 of a chip interval,

despreading one of the sets of samples and obtaining a corresponding signal power,

advancing the relative position by an amount corresponding to 1/M of a code chip interval,

despreading another of the sets of samples and obtaining a corresponding signal power,

repeating said advancing and despreading another steps until the relative position corresponds to +1 of a code chip interval.

41. A direct sequence spread spectrum receiver for reducing code phase correlation error therein after a pseudorandom code used to spread the signal at a transmitter has been aligned to a locally produced pseudorandom code within one pseudorandom code chip interval, comprising:

means for sampling said signal at a predetermined sampling rate and producing signal samples;

means for despreading said signal by applying said pseudorandom code to said signal samples and obtaining a despread signal;

means for determining a power of said despread signal, said power being an indication of how closely said signal and said pseudorandom code are aligned to one another;

means for identifying respective powers of despread signal for other relative pseudorandom code phases comprising,

means for despreading said signal by shifting a relative position of said signal and said pseudorandom code by less than said pseudorandom code chip interval,

means for determining said another of said respective powers of said despread signal, and

means for repeating said identifying until all of said respective powers have been identified;

means for determining an operational positional alignment between said pseudorandom code and said signal samples by performing a center of mass operation on said power and said respective powers; and

means for despreading said signal using said operational positional alignment previously determined and demodulating said despread signal.

42. The receiver of Claim 41, wherein:

said means for sampling comprises means for sampling said signal at a multiple M of a chipping rate of said pseudorandom code;

means for decimating said samples to reduce a sample rate of said samples to coincide with the chipping rate;

means for adjusting the relative position by at least -1/2 of a code chip interval;

means for obtaining other data samples after said means for adjusting, determining a signal power of said other data samples, and adjusting the relative position further by +1/M;

means for repeating said means for obtaining, determining and adjusting until said relative position is offset by at least +1/2 of a code chip interval;

means for determining a center of mass for said signal powers for respective of said relative positions;

if the center of mass is greater than 1/M of a chip code interval,

means for collecting and measuring a set of additional signal powers for additional relative positions at a predetermined fractional increment, set of additional signal powers comprising elements between 0 and 1, and

means for determining another center of mass using said additional signal powers; and

means for adjusting said relative position by said center of mass if said means for determining determines that said center of mass is not greater than 1/M of a chip code interval and adjusting said relative position by said another center of mass if said determining step determines that said center of mass is greater than a 1/M chip code interval.

43. The receiver of Claim 41, wherein:

said means for sampling comprises means for sampling said signal at by an amount corresponding to a product of N and M, where N is a length of said pseudorandom code and M is a multiple of a chipping rate of said pseudorandom code;

means for obtaining sets of data samples, respective sets corresponding to respective of plural fractional chip interval length relative position adjustments; and

means for despreading respective of said sets of samples using a receiver spreading code generator configured to produce a code chip sample at a rate of (2 x M) +1, comprising,

means for offsetting the relative position by an amount and direction corresponding to -1 of a chip interval,

means for despreading one of the sets of samples and obtaining a corresponding signal power,

means for advancing the relative position by an amount corresponding to 1/M of a code chip interval,

means for despreading another of the sets of samples and obtaining a corresponding signal power,

means for repeating said means for advancing and means for despreading another until the relative position corresponds to +1 of a code chip interval.

44. A method for reducing code phase correlation error in a direct sequence spread spectrum receiver after a direct sequence spread spectrum signal and a pseudorandom code, used to spread the signal at a transmitter, have been determined by said receiver to be aligned to one another within one-half of a pseudorandom code chip interval, comprising the steps of:

sampling said signal at a predetermined sampling rate and producing signal samples;

performing a least-squares operation on signal powers associated with different fractional relative position offsets between said signal and pseudorandom code chip, comprising the steps of,

producing a pseudorandom code at a relative position being less than or equal to ½ of an initial code chip position when said receiver determined that said signal and said pseudorandom code are aligned;

identifying a signal power associated with said relative position,

producing at an advanced relative position the pseudorandom code, said pseudorandom code being advanced by a fractional chip step,

identifying a signal power associated with the advanced relative position, and

repeating said steps of producing and identifying until said relative position reaches or exceeds ½ chip beyond said initial code chip position,

determining a least-squares value of said signal powers and adjusting said relative position by said least-squares value if said value is less than a predetermined chip threshold;

performing a center of mass calculation on said signal powers and adjusting said relative position by a ½ chip offset if said determining step determines that said least-squares value is not less than said predetermined threshold;

readjusting said relative position by performing said step of performing the least-square operation for a second time and after performing at least one of said steps of determining a least-squares value and a performing a center of mass calculation; and

demodulating said signal after said readjusting step.

45. A method for removing a frequency uncertainty error at an output of a differential binary phase shift keyed direct sequence spread spectrum signal in a receiver, said frequency uncertainty caused in part by a frequency offset between a transmitter frequency reference and a receiver frequency reference, said signal after being despread having a complex Nyquist bandwidth being greater than or equal to said frequency uncertainty, comprising the steps of:

storing a first data bit of said signal;

multiplying a second data bit with a complex conjugate of the first data and producing a complex product;

decimating said complex product to a single complex sample C(n) per data bit interval so as to provide a resulting signal with a static phase angle being at least one of θ and $\theta + 180$ degrees;

removing said static phase angle with a decision feedback phase error canceler, comprising,

determining a complex number $C_\theta(n)$ having an angle being a resulting static phase error averaged over M previous bits;

translating the static phase error to 0 by multiplying C(n) with a complex conjugate of $C_\theta(n)$ and obtaining a multiplication result,

identifying a sign of a real part of said multiplication result and making a bit decision based thereon, and

update a C_θ average with C(n) multiplied with a sign of the second bit.

46. A direct sequence spread spectrum signal in a receiver that removes a frequency uncertainty error at an output of a differential binary phase shift keyed, said frequency uncertainty caused in part by a frequency offset between a transmitter frequency reference and a receiver frequency reference, said signal after being despread having a complex Nyquist bandwidth being greater than or equal to said frequency uncertainty, comprising:

said frequency reference;

means for storing a first data bit of said signal;

means for multiplying a second data bit with a complex conjugate of the first data and producing a complex product;

means for decimating said complex product to a single complex sample C(n) per data bit interval so as to provide a resulting signal with a static phase angle being at least one of θ and $\theta + 180$ degrees;

means for removing said static phase angle with a decision feedback phase error canceler, comprising,

means for determining a complex number $C_\theta(n)$ having an angle being a resulting static phase error averaged over M previous bits;

means for translating the static phase error to 0 by multiplying C(n) with a complex conjugate of $C_\theta(n)$ and obtaining a multiplication result,

means for identifying a sign of a real part of said multiplication result and making a bit decision based thereon, and

means for update a C_θ average with C(n) multiplied with a sign of the second bit.

47. A method for distributing a decimation operation into plural stages in a direct sequence spread spectrum receiver, comprising:

receiving a direct sequence spread spectrum signal at said receiver, said signal having been spread at a transmitter with a spreading code of length N, N being divisible by a plurality of prime factors;

sampling said signal at a predetermined sampling rate;

producing said spreading code at said receiver;

decimating said signal in a first decimation stage by a first fraction of the sampling rate and providing a first decimated signal having a lower sample rate than said predetermined sample rate; and

decimating said decimated signal in a second decimation stage by another fraction of the sampling rate and providing a second decimated signal have a lower sample rate than said first decimated signal, wherein because N being divisible by the plurality of prime factors being an enabling feature for separately performing said decimating steps.

48. The method of Claim 47, wherein said receiving step, comprises receiving said direct sequence spread spectrum receiver wherein said signal has been spread at a transmitter with a spreading code having at least one of a code length less than 100, being a 2^k-1 sequence, having prime factors being less than 10, but greater than 2.

49. The method of Claim 47, wherein said sampling step comprises sampling said signal at a rate being an integer multiple of N.

50. The method of Claim 47, wherein said step of decimating said signal in a first decimation stage comprises decimating before said signal has been despread with said spreading code and said decimating said decimated signal in a second decimation stage, comprising decimating after said despreading with said spreading signal.

51. A direct sequence spread spectrum receiver having a plurality of decimation operators, comprising:

means for receiving a direct sequence spread spectrum signal at said receiver, said signal having been spread at a transmitter with a spreading code of length N, N being divisible by a plurality of prime factors;

means for sampling said signal at a predetermined sampling rate;

means for producing said spreading code at said receiver;

means for decimating said signal in a first decimation stage by a first fraction of the sampling rate and providing a first decimated signal having a lower sample rate than said predetermined sample rate; and

means for decimating said decimated signal in a second decimation stage by another fraction of the sampling rate and providing a second decimated signal have a lower sample rate than said first decimated signal, wherein because N being divisible by the plurality of prime factors being an enabling feature for including at least two means for decimating.

52. A method for efficient synchronization of a direct sequence spread spectrum signal in a receiver, said signal being spread with a maximal length spreading code of length N at a transmitter, N being divisible by a plurality of prime factors, comprising the steps of:

receiving said signal;

digitizing said signal; and

correlating said spreading code with said signal by calculating a Fast Fourier transform with a predetermined number of computations, said predetermined number of computations being lower than a minimum number of calculations required to correlate another signal despread with another maximal length spreading code that is greater than or equal to 15 and divisible by a lesser number of prime factors than N.

53. A direct sequence spread spectrum receiver that efficiently performs synchronization of a direct sequence spread spectrum signal, said signal being spread with a maximal length spreading code of length N at a transmitter, N being divisible by a plurality of prime factors, comprising the steps of:

means for receiving said signal;

means for digitizing said signal; and

means for correlating said spreading code with said signal by calculating a Fast Fourier transform with a predetermined number of computations, said predetermined number of computations being lower than a minimum number of calculations required to correlate another signal despread with another maximal length spreading code that is greater than or equal to 15 and divisible by a lesser number of prime factors than N.

54. A method for setting a pre-detection bandwidth in a digital direct sequence spread spectrum receiver, comprising the steps of:

receiving and digitizing a direct sequence spread spectrum signal and producing data samples;

despreading a data set having N data samples with a pseudorandom noise code, used at a transmitter to originally spread a data signal to form said direct sequence spread spectrum signal, where N coincides in number with another set of samples representative of a pseudorandom noise code;

decimating by parts another data set corresponding to a despread signal and producing M partial decimation summed samples, a ratio of N to M being an amount by which said another data set is decimated, said decimation ratio being proportional to a reduction in effective sample rate and pre-detection Nyquist bandwidth;

squaring respective of said M partial decimation summed samples and producing squared samples; and

combining said squared samples to respective of said partial decimation summed samples, wherein said pre-detection bandwidth being greater than or equal to a bandwidth of the data signal.

55. The method of Claim 54, wherein said combining step comprises at least one of adding and averaging said squared samples.

56. A digital direct sequence spread spectrum receiver, comprising the steps of:

means for receiving and digitizing a direct sequence spread spectrum signal and producing data samples;

means for despreading a data set having N data samples with a pseudorandom noise code, used at a transmitter to originally spread a data signal to form said direct sequence spread spectrum signal, where N coincides in number with another set of samples representative of a pseudorandom noise code;

means for decimating by parts another data set corresponding to a despread signal and producing M partial decimation summed samples, a ratio of N to M being an amount by which said another data set is decimated, said decimation ratio being proportional to a reduction in effective sample rate and pre-detection Nyquist bandwidth;

means for squaring respective of said M partial decimation summed samples and producing squared samples; and

means for combining said squared samples to respective of said partial decimation summed samples, wherein said pre-detection Nyquist bandwidth being greater than or equal to a bandwidth of the data signal.

57. A communications system that communicates using a direct sequence spread spectrum signal having symbol rates which are a multiple of a pseudorandom noise code repetition rate, comprising:

a transmitter, comprising,

means for aligning respective data symbols with the pseudorandom noise code,

means for forming the direct sequence spread spectrum signal by inverting corresponding portions of said PN code for a portion of said symbols having a first logic value and not inverting corresponding portions for the other symbols, and

means for transmitting in a transmitter said direct sequence spread spectrum signal; and

a receiver, comprising,

means for receiving and correlating the direct sequence spread spectrum signal, and obtaining a correlation result,

means for partitioning said correlation result to align with said portions that were inverted in said means for forming ,

means for identifying partial correlation sums for fractional symbol correlation, and

means for demodulating said data using said partial correlation sums.

58. A method for reducing a settling time of a phase/frequency locked synthesizer in a receiver, said phase/frequency locked synthesizer being turned off and on repetitively, comprising the steps of:

using capacitors as storage elements for holding a charge used to feed a voltage controlled oscillator;

making an estimate with a processor of the charge on each of said capacitors;

saving the estimate in non-volatile memory at a power-down event;

retrieving from said non-volatile memory said estimate at a power-up event;

driving respective current sources connected to respective of said capacitors for a duration sufficient to reestablish the respective charge on said capacitors prior to said power-down event; and

enabling said phase/frequency locked synthesizer after the respective charge has been reestablished.

59. A receiver having a phase/frequency locked synthesizer that reduces a settling time when being repeatedly turned on and off, comprising:

capacitors used as storage elements for holding a charge used to feed a voltage controlled oscillator;

means for making an estimate with a processor of the charge on each of said capacitors;

a non-volatile memory configured to save the estimate at a power-down event;

means for retrieving from said non-volatile memory said estimate at a power-up event;

current sources connected to respective of said capacitors;

means for driving respective for a duration sufficient to reestablish the respective charge on said capacitors prior to said power-down event; and

means for enabling said phase/frequency locked synthesizer after the respective charge has been reestablished.

60. A method for implementing down conversion, channelization, and code filtering steps in a direct sequence spread spectrum receiver having a fast Fourier transform correlator, comprising the steps of:

applying one period of a spreading code at 4 samples/chip to a fast Fourier transform, said spreading code being used at a transmitter to form a direct sequence spread spectrum signal received by said receiver, said fast Fourier transform having output points;

filtering said output points in a rectangular filter having a bandwidth corresponding to a chip rate of said spreading code and retaining 1/4 of the output points centered on DC, and computing a complex conjugate of a filtered output and saving the complex conjugate as a filtered reference code;

maintaining a real-time counter for subsequent signal phase alignment;

sampling a received bandpass signal at 4 samples per chip for a duration of one code period, said bandpass signal having a center frequency approximately equal to a chip rate;

computing a fast Fourier transform of said bandpass signal and producing fast Fourier transform points;

downconverting said signal and channelizing a frequency uncertainty bandwidth by relabling 1/4 of said fast Fourier transform output points centered at a frequency corresponding to an intermediate frequency plus a channel offset frequency as points being centered at 0 Hz;

multiplying said relabled output points by said saved filtered reference code and obtaining an output data set;

performing a coarse search correlation operation in one chip steps in one channel by performing an inverse fast Fourier Transform on said output data set; and

repeating said downconverting, multiplying and performing step for the other channels.

61. A direct sequence spread spectrum receiver, comprising:

means for calculating a fast Fourier transform;

means for applying one period of a spreading code at 4 samples/chip to the means for calculating the fast Fourier transform, said spreading code being used at a transmitter to form a direct sequence spread spectrum signal received by said receiver, said fast Fourier transform having output points;

means for filtering said output points in a rectangular filter having a bandwidth corresponding to a chip rate of said spreading code and retaining 1/4 of the output points centered on DC, and computing a complex conjugate of a filtered output and saving the complex conjugate as a filtered reference code;

means for maintaining a real-time counter for subsequent signal phase alignment;

means for sampling a received bandpass signal at 4 samples per chip for a duration of one code period, said bandpass signal having a center frequency approximately equal to a chip rate, said means for calculating a fast Fourier transform computing a fast Fourier transform of said bandpass signal and producing fast Fourier transform points;

means for downconverting said signal and channelizing a frequency uncertainty bandwidth by relabling 1/4 of said fast Fourier transform output points centered at a frequency corresponding to an intermediate frequency plus a channel offset frequency as points being centered at 0 Hz;

means for multiplying said relabled output points by said saved filtered reference code and obtaining an output data set;

means for performing a coarse search correlation operation in one chip steps in one channel by performing an inverse fast Fourier Transform on said output data set; and

means for repeatedly applying said means for downconverting, multiplying and performing for the other channels.

62. A method for maximizing computational efficiency in a processor-based serial correlator in a direct sequence spread spectrum receiver, comprising the steps of:

sampling and storing as a signal data record of length N x M a portion of a direct sequence spread spectrum signal, where N is a spreading code length and M is an integer ≥ 1;

maintaining a real-time counter so that another sample of said direct sequence spread spectrum signal may be obtained at a later time, said real-time counter enabling said another sample to be taken a predetermined number of chip lengths after said sampling step was performed;

forming a coefficient data record of said spreading code, said coefficient data record having a length of N x M;

sequentially computing correlation sums in said processor for at least a portion of all possible phase relationships of the sampled signal data record and the coefficient data record;

determining if one of said correlation sums exceeded a predetermined threshold indicative of a coarse search detection event; and

using said real-time counter to align at least said another sample with said coefficient data if said course search event is detected, comprising the step of aligning said at least another sample with said coefficient list based on a maximum correlation sum determined in said determining step.

63. The method of Claim 62, wherein said sequentially computing step comprises sequentially computing correlation sums for all possible phase relationships of the sampled data record and the coefficient data record.

64. The method of Claim 62 wherein said sampling step comprises sampling said data record of a direct sequence spread spectrum signal, where said direct sequence spread spectrum signal comprises a leader having a length being at least N + 1, where N is for a combination of diversity options.

65. The method of Claim 62, further comprising the step of turning off a radio front end of said receiver after said first sample is received and before said second sample is received.

66. The method of Claim 62, wherein said determining step comprises the steps of:

determining a relative positional adjustment of the received signal with respect to the data coefficient data record corresponding to the spreading code and adjusting the data coefficient data record by the relative positional adjustment;

forming a mixed signal by mixing the received signal with the data coefficient data record after said adjusting step;

filtering the mixed signal with a lowpass filter to form a filtered signal;

measuring a power of the filtered signal and repeating said determining step, forming step and filtering step for each relative phase position between the received signal and the data coefficient data record;

determining which relative phase position provided a maximum power;

determining an average power over at least a portion of the all relative phase positions excluding phase positions where said the maximum power occurred and within one chip interval of where the maximum occurred; and

comparing the measured maximum with the average power and deciding that correlation was achieved to within 1 chip interval if said maximum power exceeds said average power by a predetermined amount.

67. The method of Claim 62, wherein said determining step comprises the steps of:

determining a relative positional adjustment of the received signal with respect to the data coefficient data record corresponding to the spreading code and adjusting the data coefficient data record by the relative positional adjustment;

forming a mixed signal by mixing the received signal with the data coefficient data record after said adjusting step;

filtering the mixed signal with a plurality of adjacent filters, each having a bandwidth greater than or equal to a bandwidth of the signal after being despread, and forming a plurality of filtered signals;

measuring respective powers for the plurality of filtered signals and repeating said determining step, forming step, filtering step and measuring step for each relative phase position between the received signal and the data coefficient data record and for each of the adjacent filters;

determining which relative phase position provided a maximum power;

determining an average power over at least a portion of all relative phase positions except for the maximum and within one chip interval of the maximum; and

comparing the measured maximum with the average power and deciding that correlation was achieved to within 1 chip interval if said maximum power exceeds said average power by a predetermined amount.

68. The method of Claim 62, wherein:

said sampling step comprising sampling with a sampled limiter; and

said determining step comprises the steps of,

determining a relative positional adjustment of the received signal with respect to the data coefficient data record corresponding to the spreading code and adjusting the data coefficient data record by the relative positional adjustment,

forming a mixed signal by mixing the received signal with the data coefficient data record after said adjusting step,

filtering the mixed signal with a plurality of adjacent filters, each having a bandwidth greater than or equal to a bandwidth of the signal after being despreads, and forming a plurality of filtered signals,

measuring respective powers for the plurality of filtered signals and repeating said determining step, forming step, filtering step and measuring step for each relative phase position between the received signal and the data coefficient data record and for each of the adjacent filters,

determining which relative phase position provided a maximum power, and

comparing the measured maximum with a predetermined value and deciding that correlation was achieved to within 1 chip interval if said maximum power exceeds said predetermined power by a predetermined amount.

69. A direct sequence spread spectrum receiver, comprising:

means for sampling and storing as a signal data record of length N x M a portion of a direct sequence spread spectrum signal, where N is a spreading code length and M is an integer ≥ 1;

means for maintaining a real-time counter so that another sample of said direct sequence spread spectrum signal may be obtained at a later time, said real-time counter enabling said another sample to be taken a predetermined number of chip lengths after sampling by said means for sampling;

means for forming a coefficient data record of said spreading code, said coefficient data record having a length of N x M;

means for sequentially computing correlation sums in said processor for at least a portion of all possible phase relationships of the sampled signal data record and the coefficient data record;

means for determining if one of said correlation sums exceeded a predetermined threshold indicative of a coarse search detection event; and

means for using said real-time counter to align at least said another sample with said coefficient data if said course search event is detected, comprising means for aligning said at least another sample with said coefficient list based on a maximum correlation sum determined in said means for determining.

70. A direct sequence spread spectrum system comprising:

a transmitter configured to transmit a direct sequence spread spectrum signal comprising,

a pseudorandom noise code generator that produces a pseudorandom spreading sequence having a predetermined length, and

a message formatting mechanism configured to form said direct sequence message to have a leader component followed by a data pattern component, said leader component comprising plural copies of said pseudorandom spreading sequence and having a predetermined transmission length, said data pattern being spread by said pseudorandom spreading sequence; and

a receiver that receives said spread spectrum signal comprising,

a radio front-end that receives a first sample of said signal corresponding in length to at least one copy of said pseudorandom spreading sequence in said leader,

an acquisition mechanism configured to correlate said first sample with the pseudorandom sequence and determine whether a correlation value exceeds a predetermined threshold, indicative of course synchronization being achieved, said acquisition mechanism requiring a predetermined amount of processing time to correlate said first sample with said pseudorandom sequence and determine whether course synchronization has been achieved, said processing time being not greater than ½ the transmission length, wherein if said first sample includes a beginning of said leader but not including a full copy of said pseudorandom code, said receiver has enough time to receive a second sample of said signal and acquire course synchronization before said data is transmitted by transmitter.

71. A direct sequence spread spectrum receiver that is adapted to conserve power when executing a serial search operation to determine if a sample of a received signal is aligned within a predetermined number of chip intervals relative to a spreading code produced in said receiver, said spreading code employed by a transmitter to spread a data signal and form the direct sequence spread spectrum signal, comprising:

a radio front end that acquires a first sample of said signal, said radio-front end comprising a digitizer that converts said sample into a digital signal;

a signal processor comprising,

a memory configured to hold said digital signal,

at least one of,

another memory configured to hold a copy of said spreading code, and

a spreading code generator,

a correlation mechanism that correlates said copy of the spreading code said digital signal, and

a detection mechanism that detects if a correlation output signal from said correlation mechanism is greater than a predetermined amount so as to signify that said copy of said spreading code is aligned with said signal to within a predetermined chip interval, said chip interval corresponding to a chip of said spreading code; and

a controller configured to control when power is applied to said radio front end, said controller accounting for a predetermined amount of settling time prior to data acquisition, said controller applying power to the data acquisition section when acquiring said sample, removing power after said first sample is acquired and while said correlation mechanism and said detection mechanism are correlating said sample and determining whether said sample and said spreading code are aligned.

72. The receiver of Claim 71, wherein said controller is configured to reapply power to the data acquisition section if said detection mechanism determines that said first sample did not correlate, and said data acquisition mechanism then acquires said second sample.

73. The receiver of Claim 71, wherein said signal processing section includes a timer connected to said controller so that if correlation was achieved, the data acquisition section will acquire the other portion of the signal in alignment with the relative positional alignment of the first sample and the spreading code as determined by the correlation mechanism.

74. The receiver of Claim 71, wherein:

said digitizer comprises means for converting said sample into a digital signal;

said correlation mechanism comprises means for correlating said copy of the spreading code said digital signal;

said detection mechanism comprises means for detecting if the correlation output signal from said means for correlating is greater than a predetermined amount so as to signify that said copy of said spreading code is aligned with said signal to within a predetermined chip interval, said chip interval corresponding to a chip of said spreading code; and

said controller comprises means for controlling when power is applied to said radio front end, and for applying power to the data acquisition section when acquiring said sample, removing power after said first sample is acquired and while said means for correlating and said means for detecting are correlating said sample and determining whether said sample and said spreading code are aligned.

75. The receiver of Claim 71 configured to perform a method comprising the steps of:

converting said sample into said digital signal;

correlating said copy of the spreading code said digital signal;

detecting if the correlation output signal from said means for correlating is greater than a predetermined amount so as to signify that said copy of said spreading code is aligned with said signal to within a predetermined chip interval, said chip interval corresponding to a chip of said spreading code; and

controlling when power is applied to said radio front end, and for applying power to the data acquisition section when acquiring said sample, removing power after said first sample is acquired and while said means for correlating and said means for detecting are correlating said sample and determining whether said sample and said spreading code are aligned.

76. A direct sequence spread spectrum system configured to communicate data from a transmitter to a receiver in a direct sequence spread spectrum on-off-keyed system, comprising:

the transmitter, comprising a mechanism for enabling and disabling a spreading code used to spread the data signal and form the direct sequence spread spectrum on-off-keyed signal; and

the receiver comprising,

a receiver front-end configured to receive the direct sequence spread spectrum on-off-keyed signal,

a sampled limiter coupled to said receiver front-end and configured to produce a sampled signal corresponding to said direct sequence spread spectrum on-off-keyed signal,

a correlator that correlates said spreading code with said direct sequence spread spectrum on-off-keyed signal and produces a despread signal, said despread signal being represented as a correlation sum having partial sums, said partial sums corresponding to data elements of said data signal, and

a data demodulator that forms an output data stream of data elements, values of respective of said data elements corresponding to respective of said partial sums of said correlation sum.

77. The system of Claim 76, wherein said transmitter further comprises:

an output signal port configured to couple the direct sequence spread spectrum on-off-keyed signal to a transmit antenna; and

an output power control mechanism configured to control a signal level of said direct sequence spread spectrum on-off-keyed signal, said power control mechanism adjusting said signal level to respective predetermined levels corresponding to respective portions of said signal corresponding to whether said spreading code was enabled or disabled for said respective portions, a difference between said predetermined levels being an amount that meets or exceeds a processing gain associated with said direct sequence spread spectrum on-off-keyed signal.

78. The system of Claim 76, wherein said output power control mechanism further comprises means to encode the signal with a synchronization data so as to enable the spreading code to align thereto with no signal output attenuation, and not encoding with the synchronization data attenuates an output signal by at least a process gain of said signal.

79. The system of Claim 76 configured to implement a method comprising the steps of enabling and disabling a spreading code used to spread the data signal and form the direct sequence spread spectrum on-off-keyed signal;

correlating in a receiver the spreading code with the direct sequence spread spectrum on-off-keyed signal and producing a despread signal; and

forming an output data stream of data elements, values of respective of said data elements corresponding to respective of said particular sums of said correlation sum.

80. A direct sequence spread spectrum system for transmitting a direct sequence spread spectrum signal from a transmitter to a receiver, comprising:

the transmitter, said transmitter being configured to transmit the direct sequence spread spectrum signal in at least one of a plurality of frequencies, comprising,

a carrier frequency selection device configured to select said at least one of said plurality of transmitting frequencies,

a signal formatting mechanism configured to form said signal, said signal comprising a leader portion followed by a data portion, said leader comprising a code having a predetermined length, said code being repeated a plurality of times in said leader, a length of said leader being transmitted for a duration

being at least twice as long as a maximum signal acquisition time required by the receiver to acquire the signal, said data portion being spread by said code; and

the receiver that receives said direct sequence spread spectrum signal, comprising,

a correlator configured to despread the spread spectrum signal and determine whether said direct sequence spread spectrum signal is present within said maximum signal acquisition time, wherein if said correlator attempts to acquire said transmitted signal based only on a fraction of a beginning portion of said leader, said leader being of sufficient length for said receiver to acquire the direct sequence spread spectrum signal by correlating a second portion of said leader, prior to said data portion of said direct sequence spread spectrum signal.

81. The system of Claim 80 configured to implement a process for transmitting and receiving said direct sequence spread spectrum signal comprising the steps of:

forming said signal so as to have a leader portion followed by a data portion, said leader portion comprising a code having a predetermined length, said code being repeated a plurality of times in said leader, a length of said leader being transmitted for a duration being at least twice as long as a maximum signal acquisition time required by the receiver to acquire the signal, said data portion being spread by said code; and

despreading in the receiver the spread spectrum signal and determining whether said direct sequence spread spectrum signal is present within said maximum signal acquisition time, wherein if said correlator attempts to acquire said transmitted signal based only on a fraction of said beginning portion of said leader, said leader being of sufficient length for said receiver to acquire the direct sequence spread spectrum signal by correlating a second portion of said leader, prior to said data portion of said direct sequence spread spectrum signal.

82. The system of Claim 80, wherein said receiver further comprises:

a frequency diversity frequency selector that selects at least one of said frequencies for receiving said signal and determining whether said signal is acquired;

said correlator comprising,

a relative position adjustment mechanism that adjusts a phase of received signal with respect to a locally generated spreading signal,

a signal combiner configured to combine the spreading signal with the received signal and produce a mixed signal,

a filter that limits a bandwidth of said mixed signal,

a power measuring device that measures a power of said mixed signal for respective of phases adjusted by said relative position adjustment mechanism, and that determines a maximum power,

an averaging device that determines an average power for each phase position adjusted by said relative position adjustment mechanism, said average power excluding said maximum power and powers measured within one code chip interval of said maximum, and

a comparator that compares said maximum with said average power and determines whether acquisition is achieved for the phase position corresponding with said maximum if said maximum exceeds said average by a predetermined amount.

83. The receiver of Claim 82 wherein:

said correlator is configured to determine whether acquisition is achieved for all frequencies selected by said frequency selector.

84. A direct sequence spread spectrum communications system comprising:

a transmitter that transmits a direct sequence spread spectrum signal formed by spreading a data signal with a pseudorandom code, said transmitter including a frequency reference that imparts a frequency uncertainty in said direct sequence spread spectrum signal due to a suboptimal frequency accuracy; and

a receiver that receives said direct sequence spread spectrum signal, comprising,

a timer configured to measure a length of time between when a portion of the direct sequence spread spectrum signal is received and when the receiver determines in a correlation mechanism that the direct sequence spread spectrum signal is acquired so that another portion of the direct sequence spread spectrum signal will be compared in phase with a despreading code used in the correlation mechanism,

the correlation mechanism which is configured to determine a cross correlation of the portion of the signal with the pseudorandom code so as to form a cross correlation result in a magnitude array, said pseudorandom code represented by a coefficient data record,

a memory configured to hold said magnitude array,

a signal acquisition section that uses said timer to acquire another portion of said direct sequence spread spectrum signal to be coincident with the despreading code for cross correlation in said correlation mechanism with the coefficient data record used for the portion of the signal and for producing subsequent magnitude arrays,

an averaging mechanism configured to average the magnitude array with the subsequent magnitude arrays to form an average array; and

an acquisition detection mechanism that determines if entries in said average array indicate that signal acquisition is achieved.

85. The system of Claim 84, wherein:

said timer of said receiver comprises means for measuring a length of time;

said correlation mechanism of said receiver comprises means for determining a cross correlation of the portion of the signal with the pseudorandom code;

said signal acquisition section comprises means for acquiring said another portion of said direct sequence spread spectrum signal to be coincident with the spreading code;

said averaging mechanism comprising means for averaging the magnitude array with the subsequent magnitude arrays to form the average array; and

said acquisition detection mechanism comprising means for determining if entries in said average array indicate that signal acquisition is achieved.

86. A direct sequence spread spectrum communications system comprising:

a transmitter that transmits a direct sequence spread spectrum signal formed by spreading a data signal with a pseudorandom code, said transmitter including a frequency reference that imparts a frequency uncertainty in said direct sequence spread spectrum signal due to a suboptimal frequency accuracy; and

a receiver that receives said direct sequence spread spectrum signal, comprising,

a timer configured to measure a length of time between when a portion of the direct sequence spread spectrum signal is received and when the receiver determines in a correlation mechanism that the direct sequence spread spectrum signal is acquired so that another portion of the direct sequence spread spectrum signal will be acquired so as to be aligned in phase with a despreading code used in the correlation mechanism,

the correlation mechanism which is configured to determine a cross correlation of the portion of the signal with the pseudorandom code and frequency plane so as to form a cross correlation result in a magnitude plane, said pseudorandom code represented by a coefficient data record,

a memory configured to hold said magnitude plane,

a signal acquisition section that uses said timer to acquire another portion of said direct sequence spread spectrum signal to be coincident with the despreading code for cross correlation in said correlation mechanism with the coefficient data record used for the portion of the signal and for producing subsequent magnitude planes,

an averaging mechanism configured to average the magnitude plane with the subsequent magnitude planes to form an average magnitude plane; and

an acquisition detection mechanism configured to determine if entries in said average magnitude plane indicate that signal acquisition is achieved.

87. The system of Claim 86, wherein:

said transmitter comprises means for forming said direct sequence spread spectrum signal;

said timer and said receiver comprise means for measuring the length of time;

the correlation mechanism comprises means for determining said cross correlation;

said signal acquisition section of said receiver comprising means for using said timer to acquire said another portion of said direct sequence spread spectrum signal;

said averaging mechanism comprising means for averaging the magnitude plane with the subsequent magnitude planes to form said average magnitude planes; and

said acquisition detection mechanism comprising means for determining if entries in said average magnitude plane indicate that signal acquisition is achieved.

88. A transmitter in a direct sequence spread spectrum communication system having frequency diversity, comprising:

a signal combiner that combines a data signal with a pseudorandom code that spreads the data signal into the direct sequence spread spectrum signal, said pseudorandom code comprising chips having a duration corresponding to a predetermined chipping rate;

a clock generator that generates a clock signal at a frequency that is a multiple of the chipping rate, said multiple being greater than or equal to 1, wherein

said combiner being configured to mix the direct sequence spread spectrum signal with said clock signal to produce a composite signal having two components centered at respective center frequencies that are separated by two times said clock frequency, said composite signal being transmitted to a direct sequence spread spectrum receiver that is configured to receive the composite signal and extract the data signal therefrom.

89. The receiver of Claim 71, further comprising:

a combiner that combines one period of a spreading code at 4 samples/chip to a fast Fourier transform, said fast Fourier transform having output points;

a filter that filters output points in a rectangular filter having a bandwidth corresponding to a chip rate of said spreading code and retaining 1/4 of the output points centered at 0 Hz, and computing a complex conjugate of a filtered output and saving the complex conjugate as a filtered reference code;

a real-time counter for subsequent signal phase alignment;

an analog to digital converter that digitized a received bandpass signal at 4 samples per chip for a duration of one code period, said bandpass signal having a center frequency approximately equal to a chip rate;

a processor comprising,

a fast Fourier transform mechanism that transforms said bandpass signal and produces fast Fourier transform points,

a downconversion and channelization mechanism that downconverts said signal and channelizes a frequency uncertainty bandwidth by relabling 1/4 of said fast Fourier transform output points centered at a frequency corresponding to an intermediate frequency plus a channel offset frequency as points being centered at 0 Hz,

a multiplication mechanism configured to multiply said relabled output points by said saved filtered reference code and obtaining an output data set,

a coarse search correlation mechanism that performs a correlation operation on said output data set in one chip steps in one channel by performing an inverse fast Fourier Transform on said output data set; and

a repeating mechanisms that applies signals from other channels to said downconversion and channelization mechanism, multiplication mechanism and coarse search correlation mechanism for the other channels;

a low-power, continuous, state-independent clock configured to cause said receiver to enter an idle state so as to draw minimal power while in the idle state and to enter an active state where said receiver performs communication functions, said state-independent clock causing said active and idle states to be synchronized with external events.

90. The receiver of Claim 71, further comprising:

a sampling device and memory configured to sample and store as a signal data record of length N x M a portion of a direct sequence spread spectrum signal, where N is a spreading code length and M is an integer ≥ 1;

a real-time counter so that another sample of said direct sequence spread spectrum signal may be obtained at a later time, a predetermined number of chip lengths after said sampling step was performed;

a spreading code generator configured to form a coefficient data record of said spreading code, said coefficient data record having a length of N x M;

a processor comprising,

a correlation mechanism that sequentially computes correlation sums for at least a portion of all possible phase relationships of the sampled signal data record and the coefficient data record and determining if one of said correlation sums exceeded a predetermined threshold indicative of a course search detection event;

an alignment mechanism configured to use said real-time counter to align at least said another sample with said coefficient data if said course search event is detected, and align said at least another sample with said coefficient list based on a maximum correlation sum determined in said correlation mechanism; and

a low-power, continuous, state-independent clock configured to cause said receiver and transmitter to enter an idle state so as to draw minimal power while in the idle state and to enter an active state where said transceiver performs communication functions, said state-independent clock causing said active and idle states to be synchronized with external events.

91. A spread spectrum communication network comprising:

at least one spread spectrum transmitter;

at least one spread spectrum receiver operating continuously, and having respective local time references;

a system controller managing said at least one transmitter and at least one receiver;

a remote spread spectrum receiver located away from said system controller and having a another local time reference; wherein

said system controller instructs said at least one transmitter to broadcast a synchronization signal at a repeating interval,

respective of said spread spectrum receivers being configured to receive said synchronization signal and adjust said respective local time references so as to minimize a risk of not receiving said synchronization signal broadcast by said system controller; and

respective of said spread spectrum receivers comprising a re-acquisition mechanism used to reacquire synchronization if as a result of an error synchronization is lost, said re-acquisition mechanism comprising,

a monitoring mechanism that causes respective of said receivers to recognize that synchronization is lost and continue to monitor for a broadcast of a next synchronization signal.

92. The network of Claim 91, wherein at least one of said spread spectrum receivers comprises a transmitter that is configured to transmit a timing request signal to said system controller so as to initiate a communication exchange with the system controller and resynchronize said local time reference .

93. The network of Claim 91, wherein said at least one transmitter is configured to interleave data with said synchronization message.

94. The spread spectrum communication network of Claim 91, wherein said remote receiver includes a delay lock loop so as to maintain network coherency by tracking a duration of an expected message.

95. The network of Claim 91, wherein:

said system controller comprising means for instructing said at least one transmitter to broadcast said synchronization signal at a repeating interval;

said spread spectrum receivers comprising means for receiving said synchronization signal and adjusting said respective local time reference; and

said re-acquisition mechanism of said receivers comprising means for re-acquiring synchronization if the result of the error synchronization is lost, comprising means for monitoring said broadcast of the next synchronization signal.

96. The network of Claim 91, configured to implement a method comprising the steps of:

managing at said system controller said at least one transmitter and said at least one receiver;

instructing in said system controller said at least one transmitter to broadcast said synchronization signal at said repeating interval;

receiving said synchronization signal at said receivers and, in response said receivers adjusting respective local time references; and

re-acquiring synchronization if a result of the synchronization is lost, comprising,

causing respective of said receivers to recognize that said synchronization is lost, and

continuing to monitor for the broadcast of the next synchronization signal.

97. A digital communication system comprising:

a transmitter configured to transmit a signal, comprising,

a transmitter frequency reference that produces a frequency with a predetermined accuracy,

a modulator configured to encode data in the signal to be transmitted by on-off-key modulating another signal with a data signal; and

a receiver configured to extract said data signal from said signal sent from said transmitter by demodulating said signal, comprising,

a detector having a bandwidth corresponding in width to a signal uncertainty bandwidth, where said signal uncertainty bandwidth accounts for a bandwidth of said data signal and a frequency uncertainty bandwidth caused by said predetermined accuracy of said transmitter frequency reference to be at least as great as said bandwidth of said data signal, said detector comprising,

a multichannel filtering mechanism that provides K channels each having a bandwidth as least as great as that of the data signal bandwidth and being distributed within said bandwidth of said detector so as to cover said frequency uncertainty bandwidth, one of said channels being a primary channel for signal reception,

an acquisition detection mechanism configured to set another of the K channels as a channel in which said data signal is present in response to determining that energy received in said another of said K channels is sufficiently high to have surpassed a predetermined threshold, comprising, a demodulator configured to demodulate said data signal using power measured across the K channels for a data bit interval comprising,

a processing mechanism configured to calculate power for a bit interval across the K channels and determine if an energy from said primary channel power exceeds a primary channel threshold, and if not determining whether an energy of any of the alternate channels exceeds said predetermined threshold.

98. A direct sequence spread spectrum communication network comprising:

a transmitter that transmits a direct sequence spread spectrum signal comprising a message;

a processor;

a plurality of receivers connected to one another in a multi-drop network, said processor being connected to the multi-drop network, respective of said receivers comprising a memory, wherein

respective of said receivers that receive said direct sequence spread spectrum signal store the message in said memory, said message having a unique identification,

respective of said receivers being configured to relay said message to said processor over the multi-drop network according to a signaling protocol, wherein

respective of the receivers monitor the multi-drop network for other message traffic and, if message traffic is present, determine if an identification of said message traffic is common with said message stored in said memory, and if said identification is common, eliminating the message in the memory because it is redundant with the message traffic being sent to the processor.

99. The network of Claim 98, wherein respective of said receivers comprise means for relaying said message to said processor over the multi-drop network;

means for monitoring the multi-drop network for other message traffic;

means for determining an identification of said message traffic in common with said message stored in memory if said message traffic is present; and

means for eliminating the message in the memory if said identification is common.

100. The network of Claim 98, configured to implement a process comprising the steps of:

storing said message in said memory;

relaying said message to said processor over the multi-drop network;

monitoring the multi-drop network for other message traffic;

determining if the identification of said message traffic is common with said message stored in said memory if said message traffic is present and

eliminating the message in the memory if said identification is common.

101. A method in a direct sequence spread spectrum receiver for avoiding false pseudorandom noise code synchronization detection caused by spontaneous in-band interference, said receiver having a plurality of channels arranged within a predetermined bandwidth corresponding to a frequency uncertainty range due to frequency offset in respective frequency references in a transmitter and said receiver, comprising the steps of:

attempting to despread said signal by applying the pseudorandom noise code to said signal and outputting a stream of digital samples;

applying said digital samples to said channel filters;

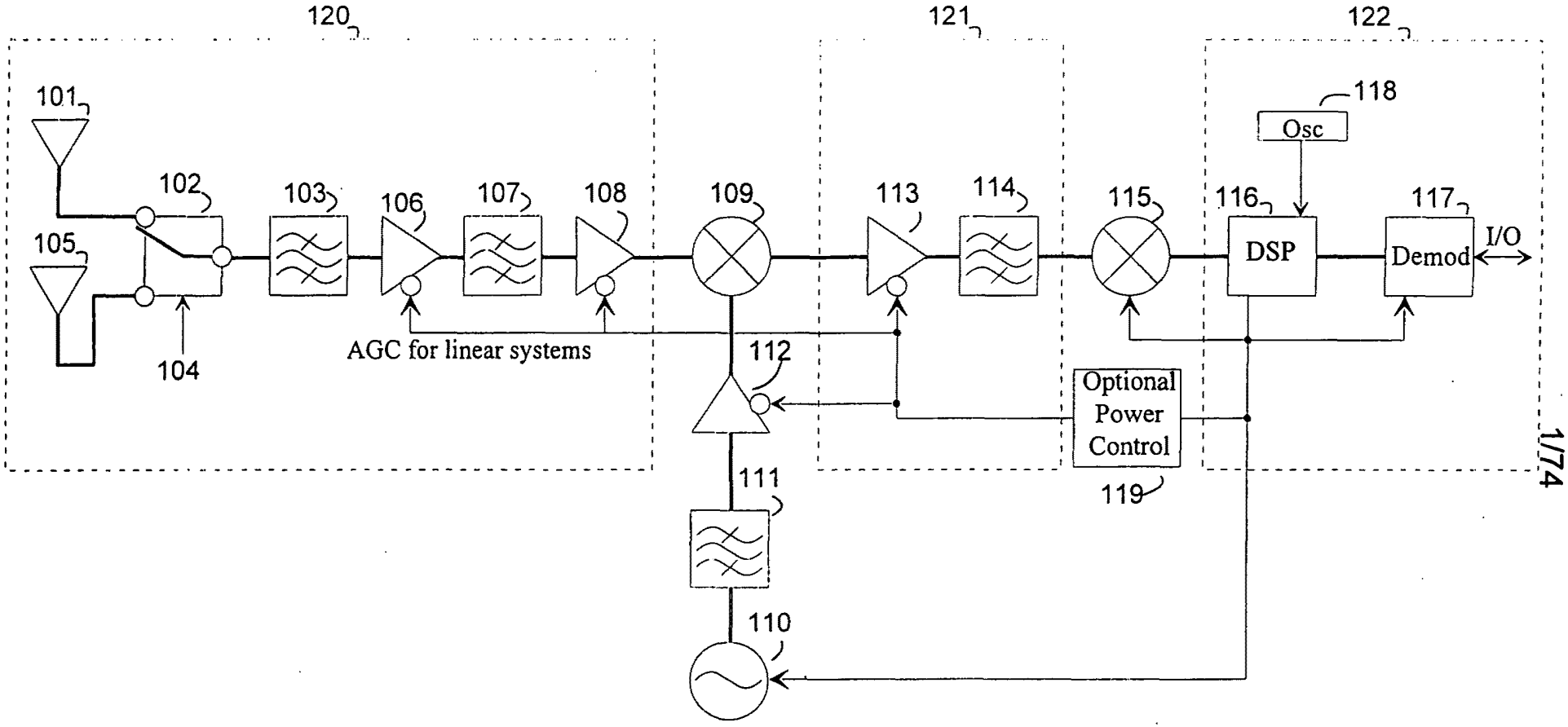
determining respective energy amounts within said channel filters;

identifying the channel filter having a maximum energy amount therein;

identifying another channel of said channels which has a second largest energy, said another channel not being one of a pair of channels being adjacent to the channel identified as having the maximum energy amount;

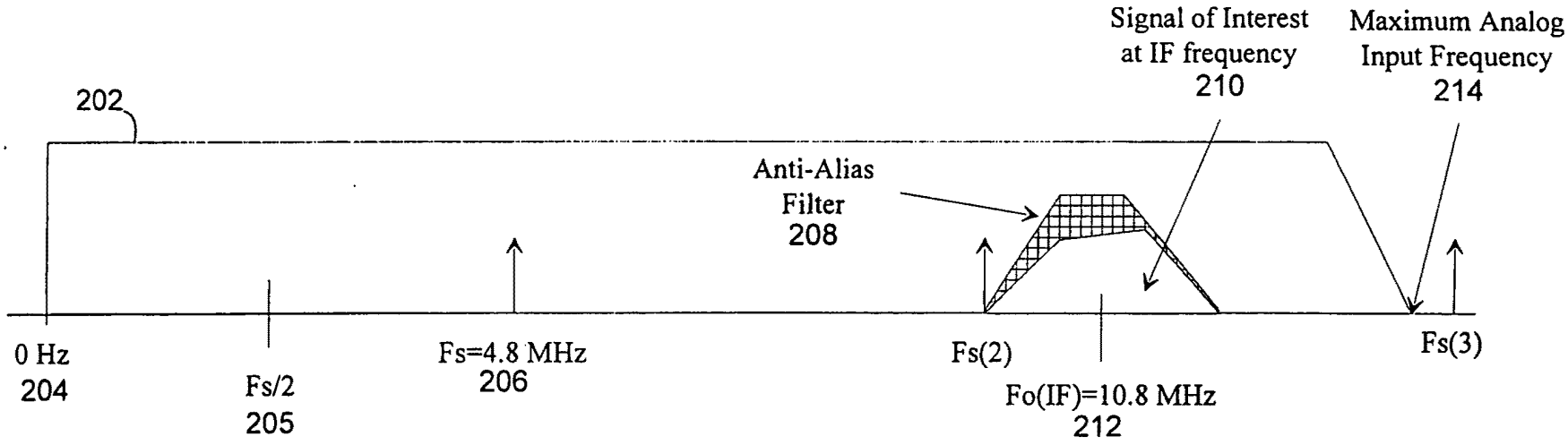
determining if said maximum energy exceeds said second largest energy by at least a predetermined amount; and

performing fine search correlation and data demodulation if course synchronization is achieved, and returning to said attempting step where said signal and pseudorandom noise code are shifted relative to one anther before being applied to one another.

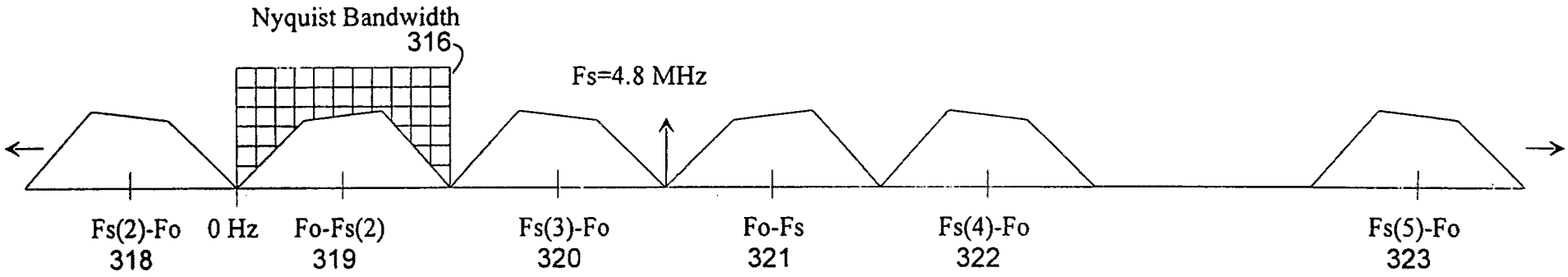


Prior Art

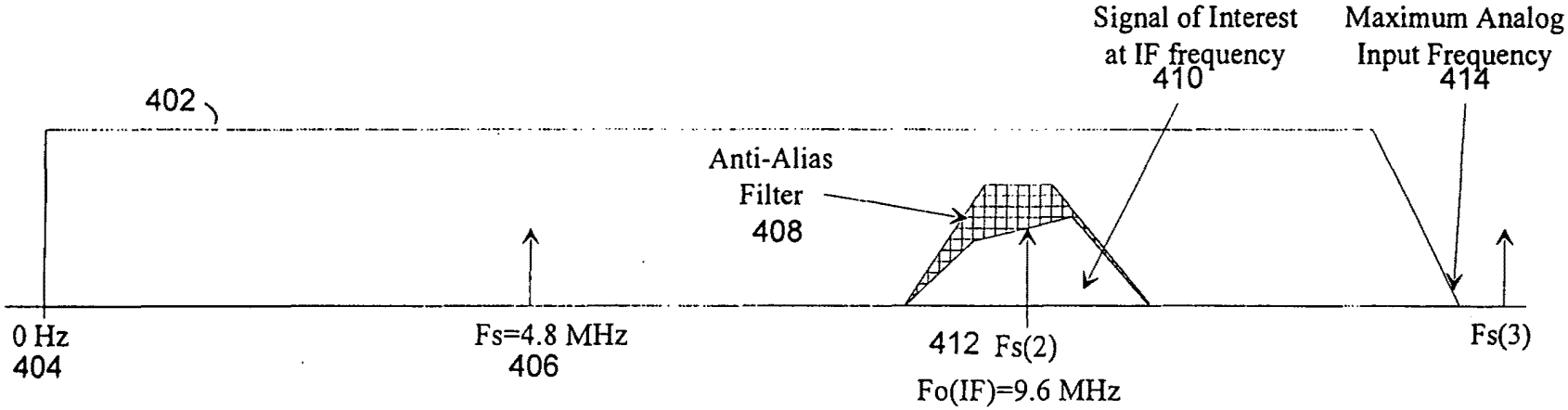
Figure 1



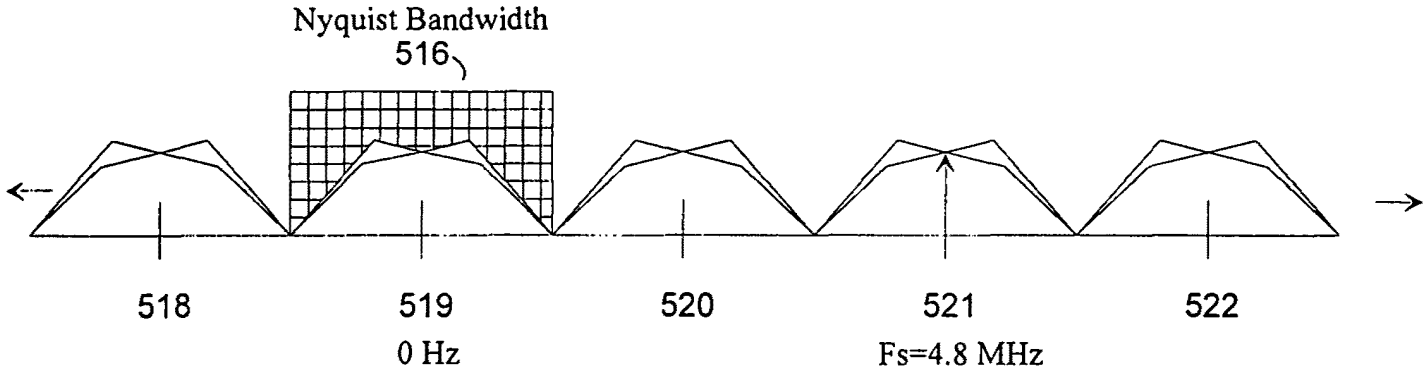
Prior Art
Figure 2



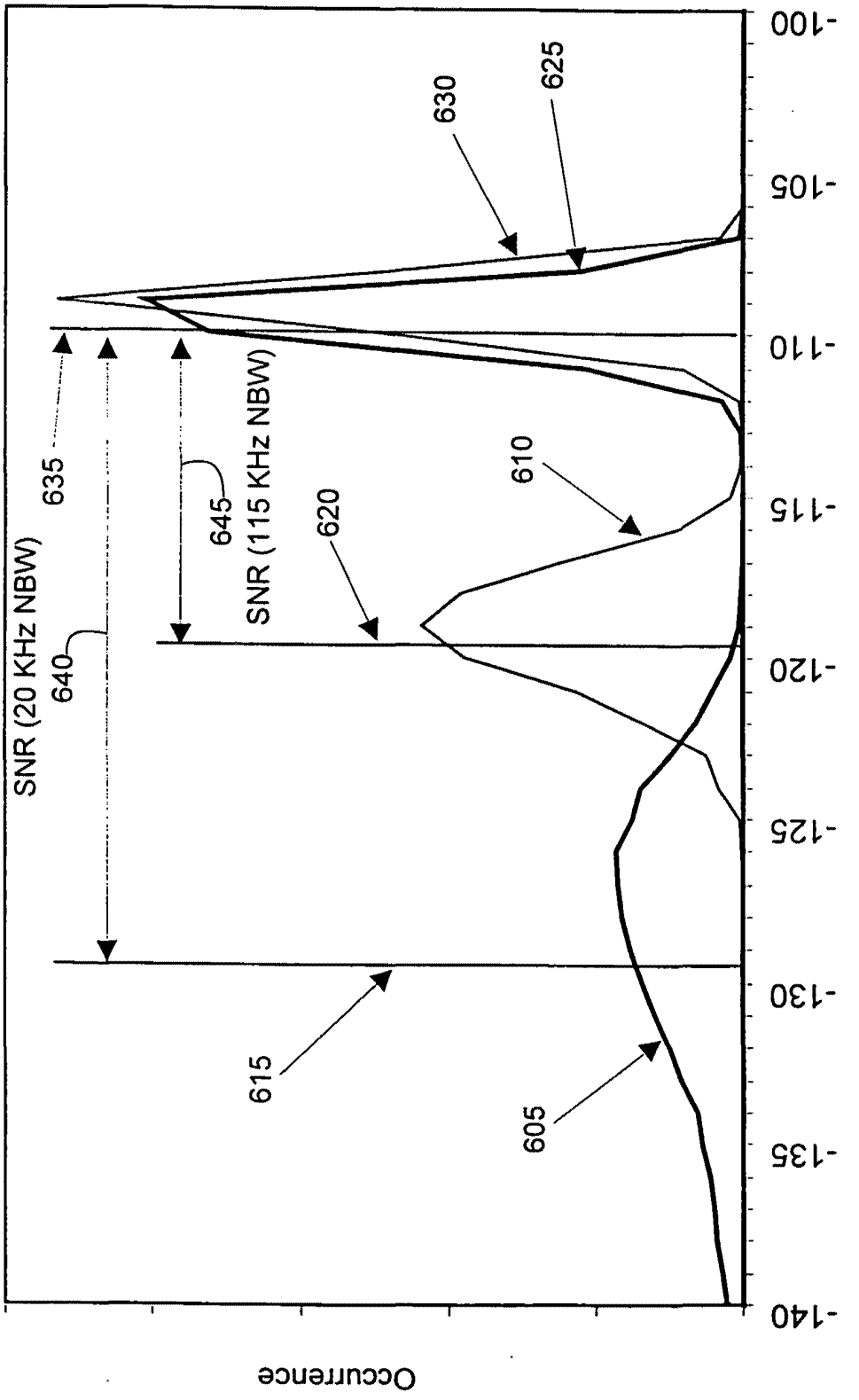
Prior Art
Figure 3



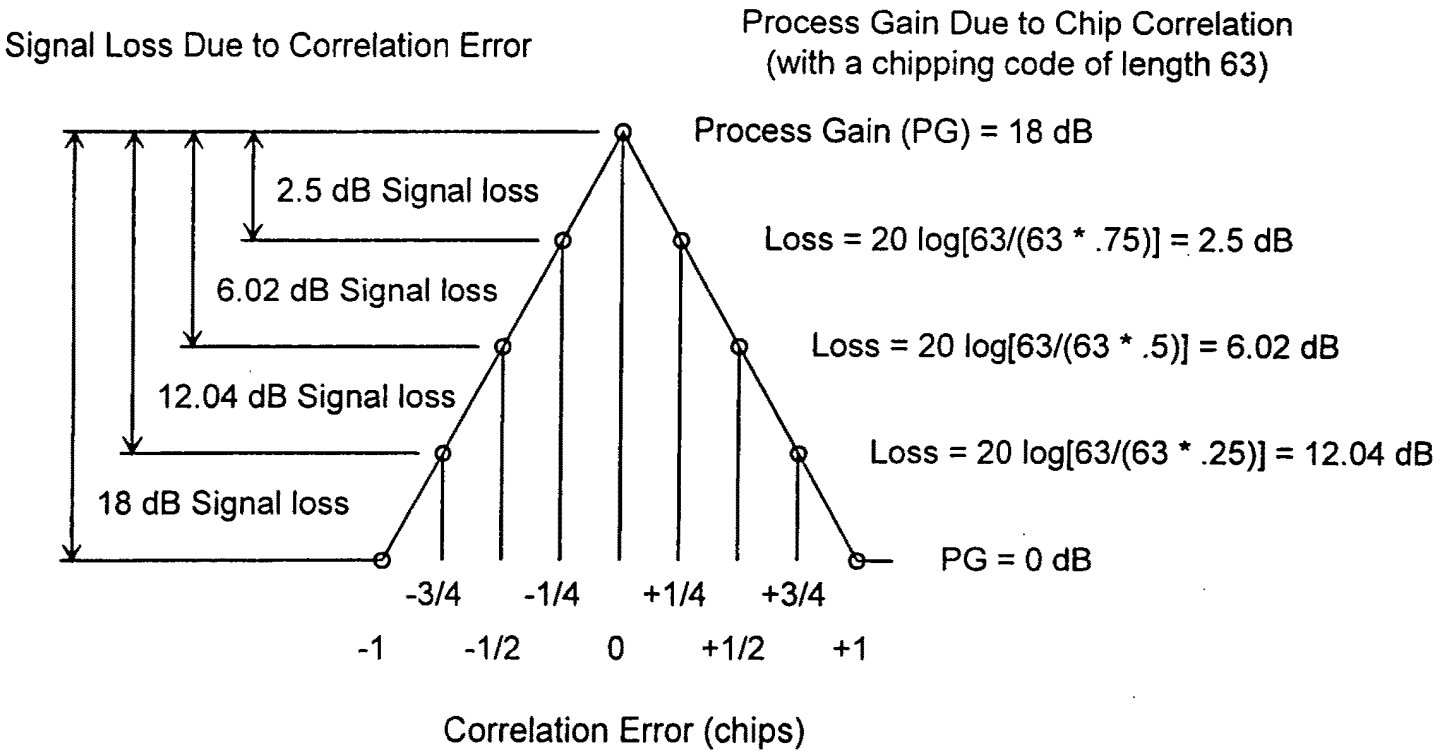
Prior Art
Figure 4



Prior Art
Figure 5

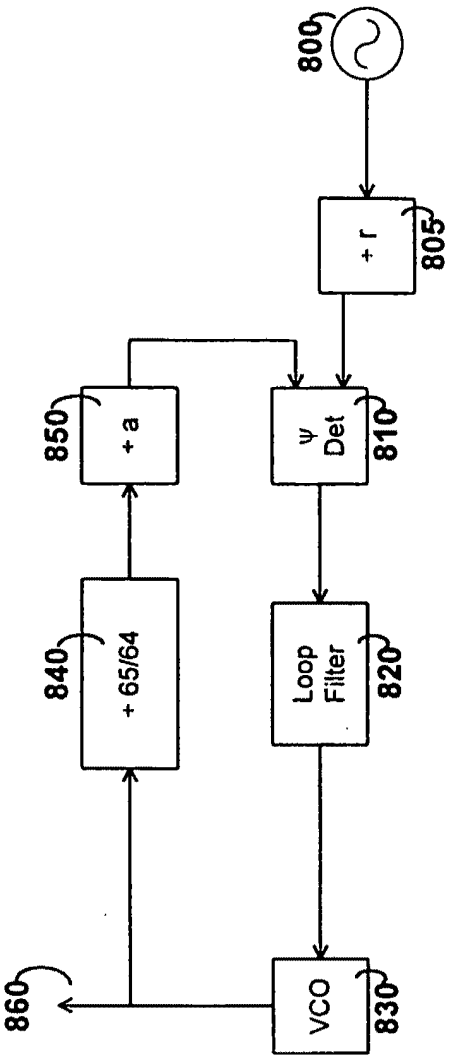


Prior Art
Figure 6



Prior Art

Figure 7



Prior Art

Figure 8

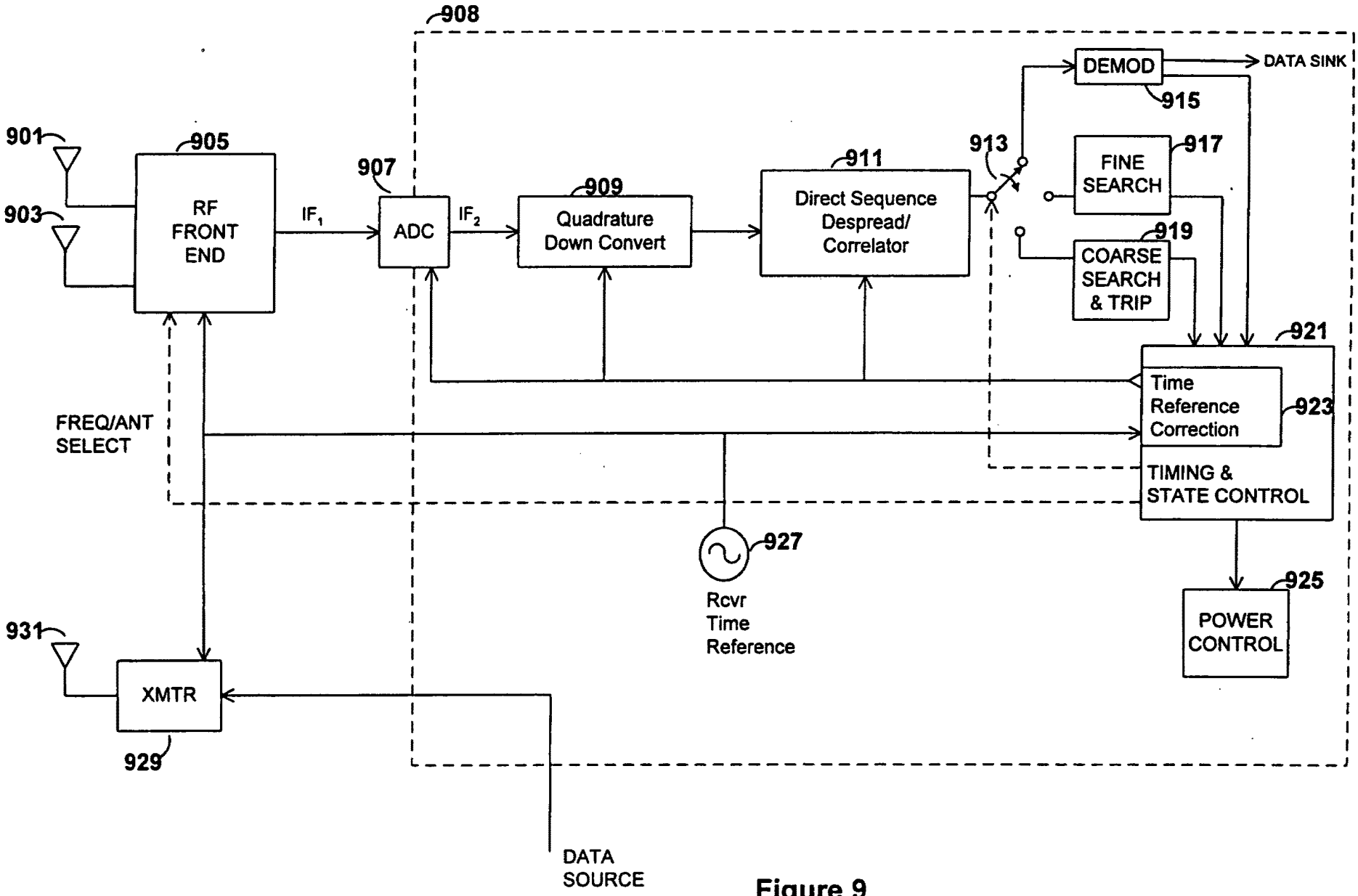

908
DEMOD
DATA SINK
915
901
905
913
917
911
907
909
903
RF FRONT END
IF1
ADC
IF2
Quadrature Down Convert
Direct Sequence Despread/ Correlator
FINE SEARCH
919
COARSE SEARCH & TRIP
921
Time Reference Correction
923
FREQ/ANT SELECT
TIMING & STATE CONTROL
927
925
Rcvr Time Reference
POWER CONTROL
931
XMTR
929
DATA SOURCE

Figure 9

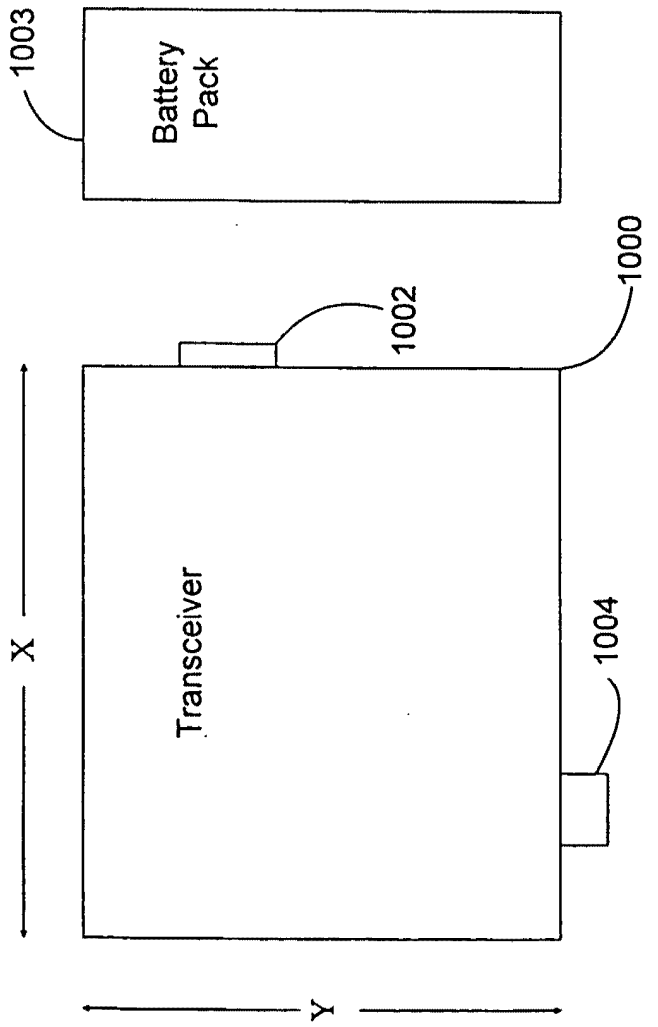


Figure 10

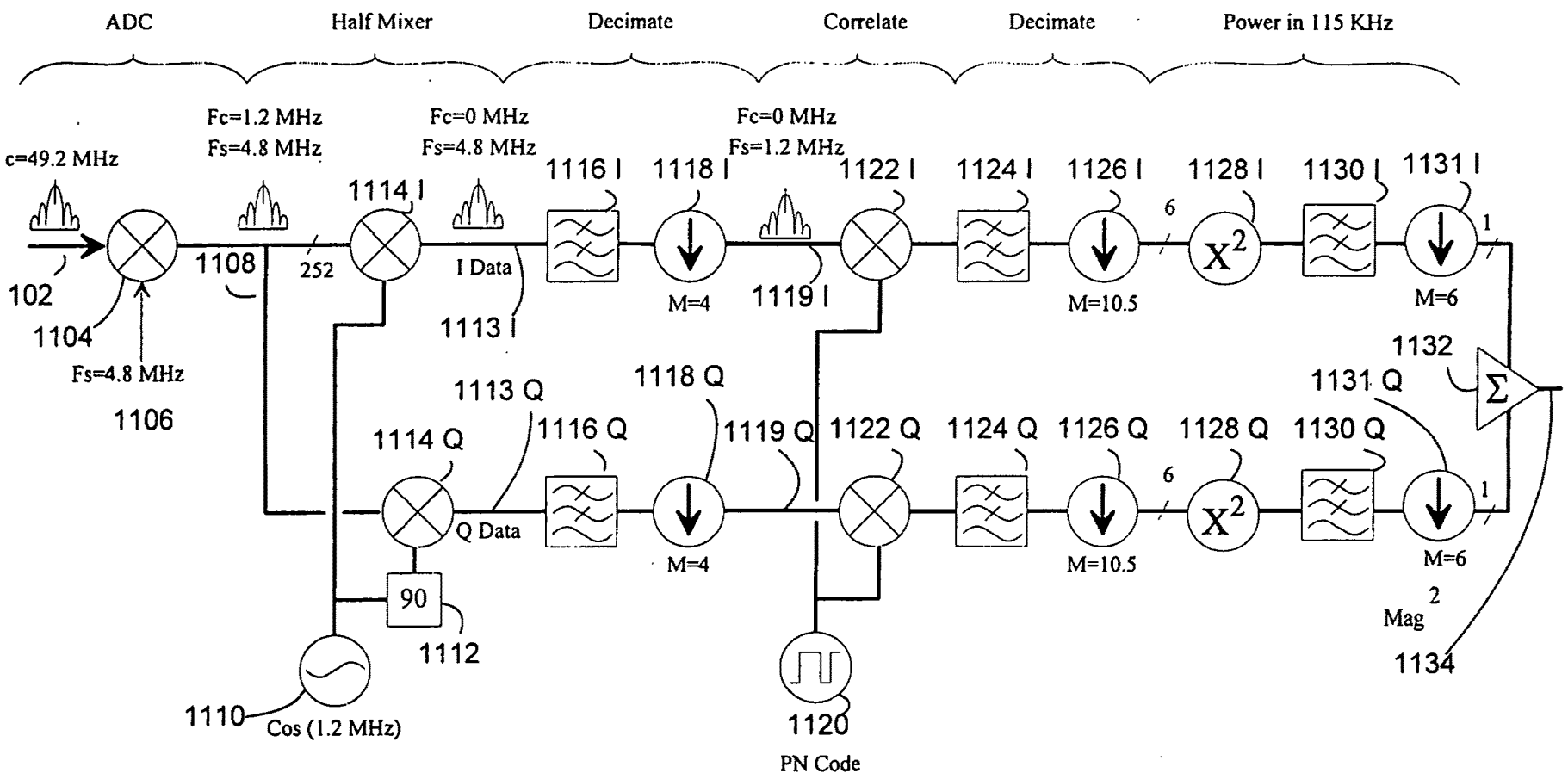

ADC
Half Mixer
Decimate
Correlate
Decimate
Power in 115 KHz
c=49.2 MHz
Fc=1.2 MHz
Fs=4.8 MHz
Fc=0 MHz
Fs=4.8 MHz
Fc=0 MHz
Fs=1.2 MHz
102
1104
Fs=4.8 MHz
1106
1108
252
1114 I
I Data
1113 I
1116 I
1118 I
M=4
1119 I
1122 I
1124 I
1126 I
M=10.5
6
X2
1128 I
1130 I
1131 I
M=6
1
1132
Σ
1131 Q
1113 Q
1118 Q
1114 Q
1116 Q
1119 Q
1122 Q
1124 Q
1126 Q
1128 Q
1130 Q
Q Data
M=4
M=10.5
6
X2
M=6
1
2
Mag
1134
90
1112
1110
Cos (1.2 MHz)
1120
PN Code

Figure 11

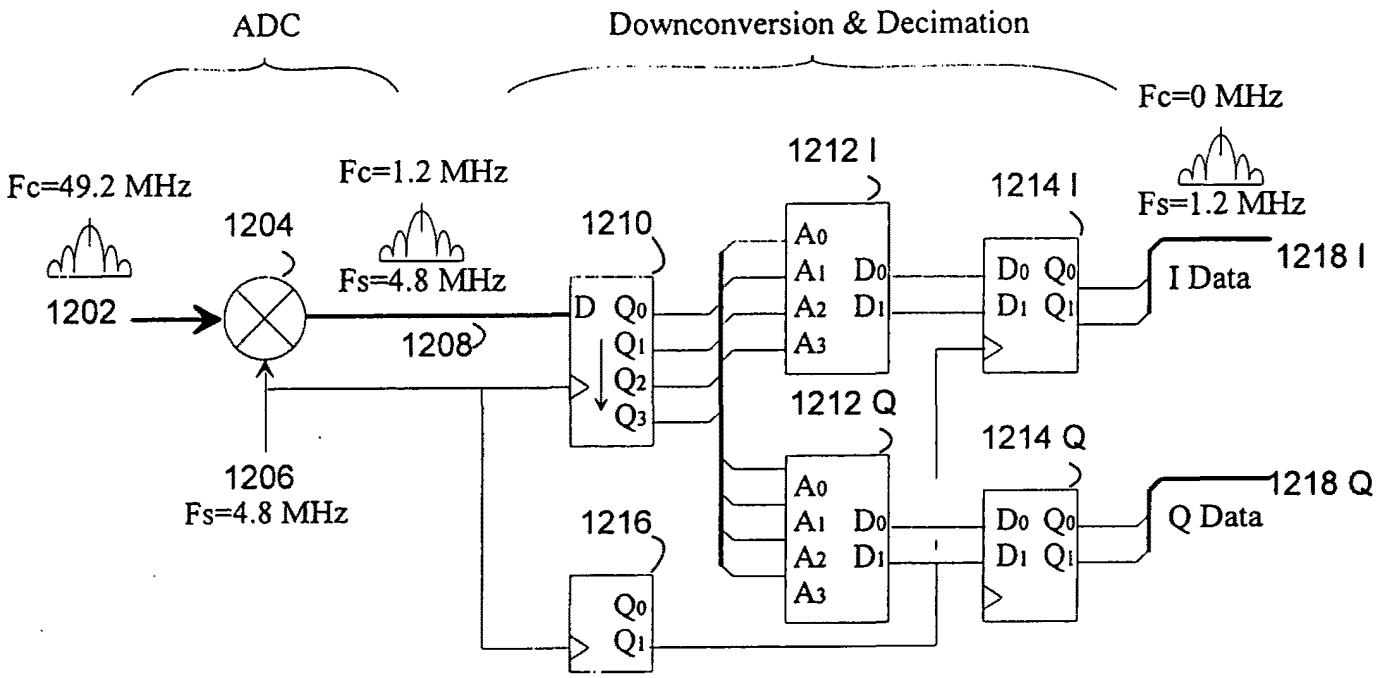

ADC
Downconversion & Decimation
Fc=49.2 MHz
1202
1204
Fc=1.2 MHz
Fs=4.8 MHz
1208
1206
Fs=4.8 MHz
1210
D Q0
Q1
Q2
Q3
1212 I
A0
A1 D0
A2 D1
A3
1212 Q
1214 I
D0 Q0
D1 Q1
Fc=0 MHz
Fs=1.2 MHz
1218 I
I Data
1214 Q
1218 Q
Q Data
1216
Q0
Q1

Figure 12

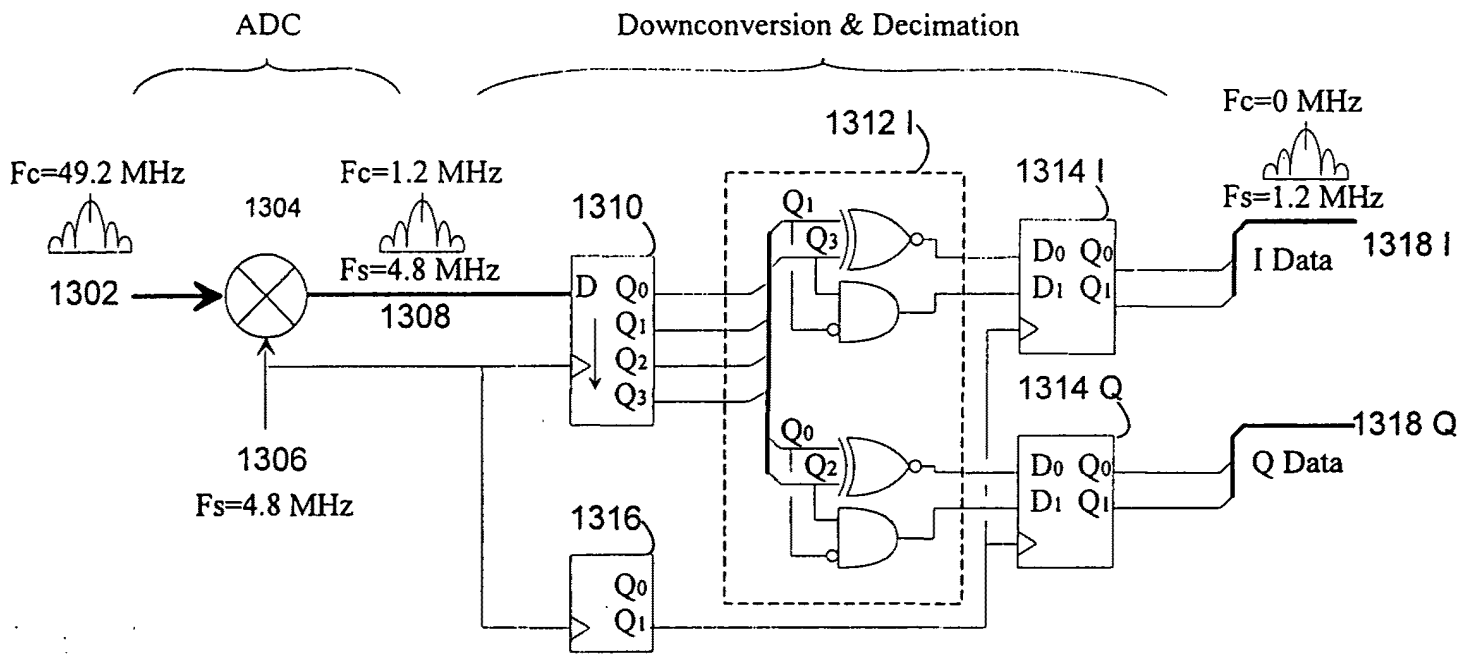

ADC
Downconversion & Decimation
Fc=49.2 MHz
1302
1304
Fc=1.2 MHz
Fs=4.8 MHz
1308
1306
Fs=4.8 MHz
1310
D Q0
Q1
Q2
Q3
1312 I
Q1
Q3
Q0
Q2
1314 I
D0 Q0
D1 Q1
1314 Q
D0 Q0
D1 Q1
1316
Q0
Q1
Fc=0 MHz
Fs=1.2 MHz
I Data
1318 I
Q Data
1318 Q

Figure 13

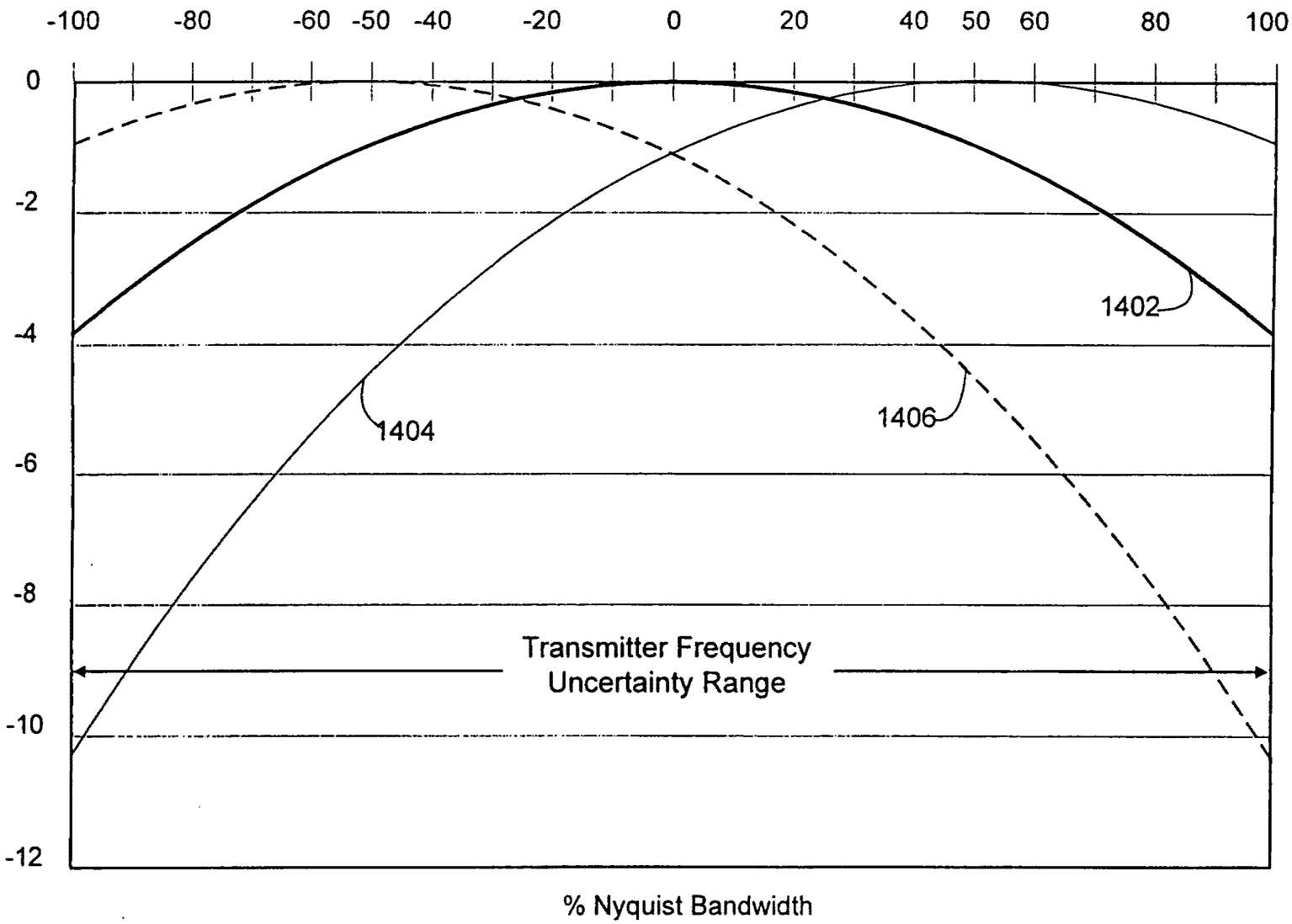

-100
-80
-60
-50
-40
-20
0
20
40
50
60
80
100
0
-2
-4
-6
-8
-10
-12
dB
1402
1404
1406
Transmitter Frequency
Uncertainty Range
% Nyquist Bandwidth

Figure 14

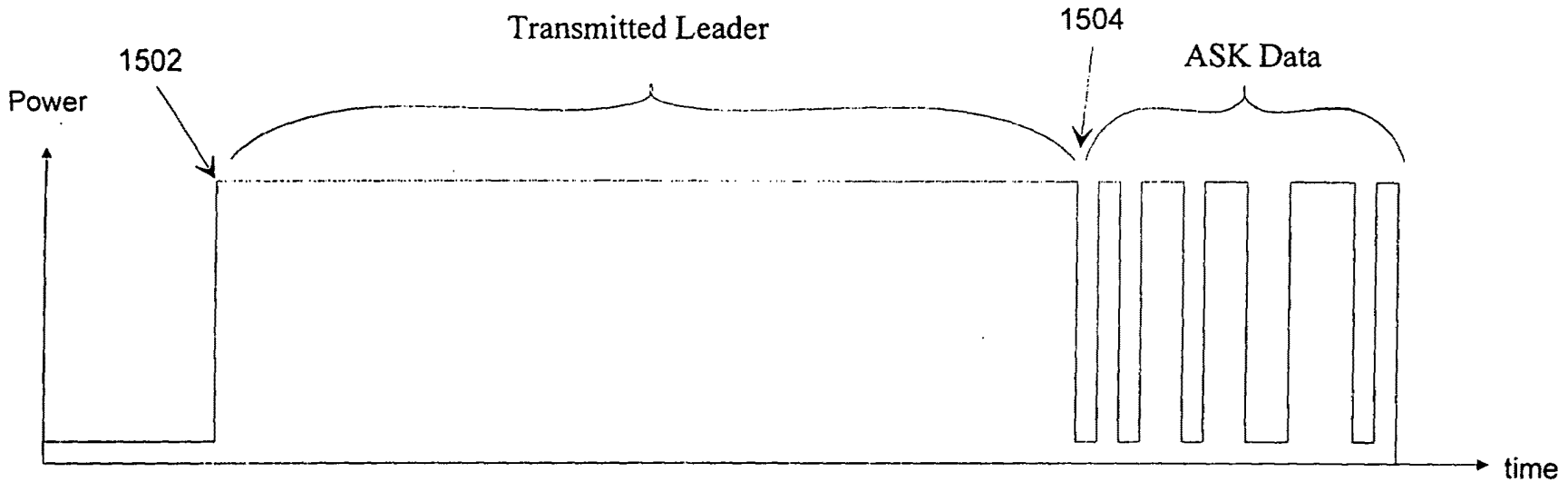


Figure 15A

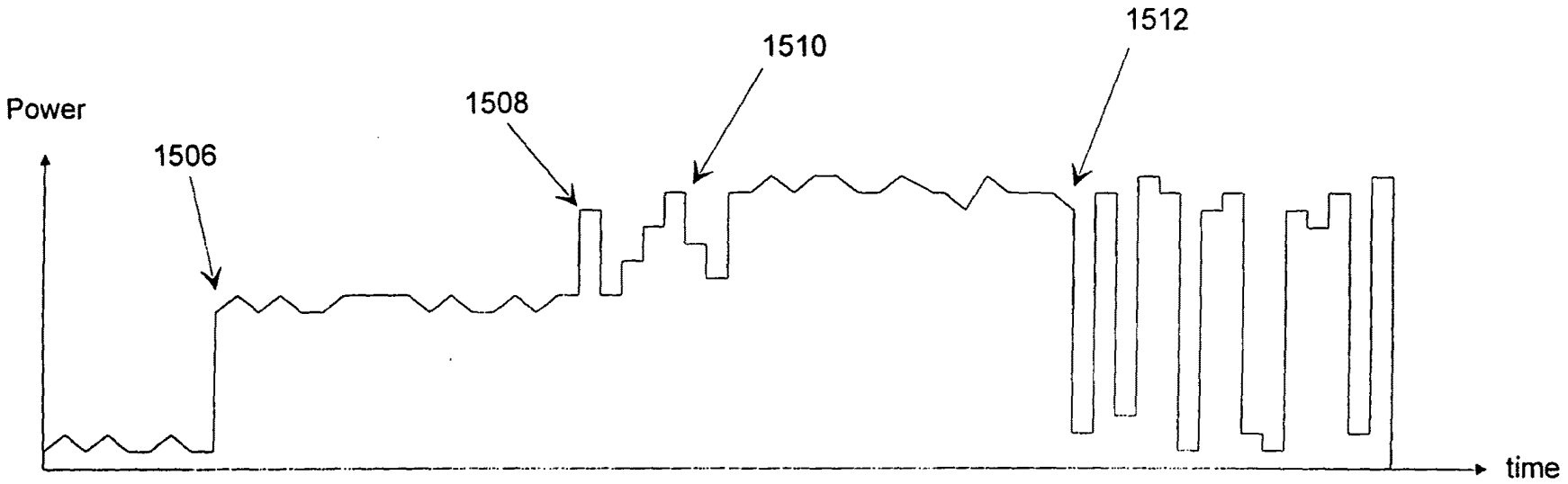


Figure 15B

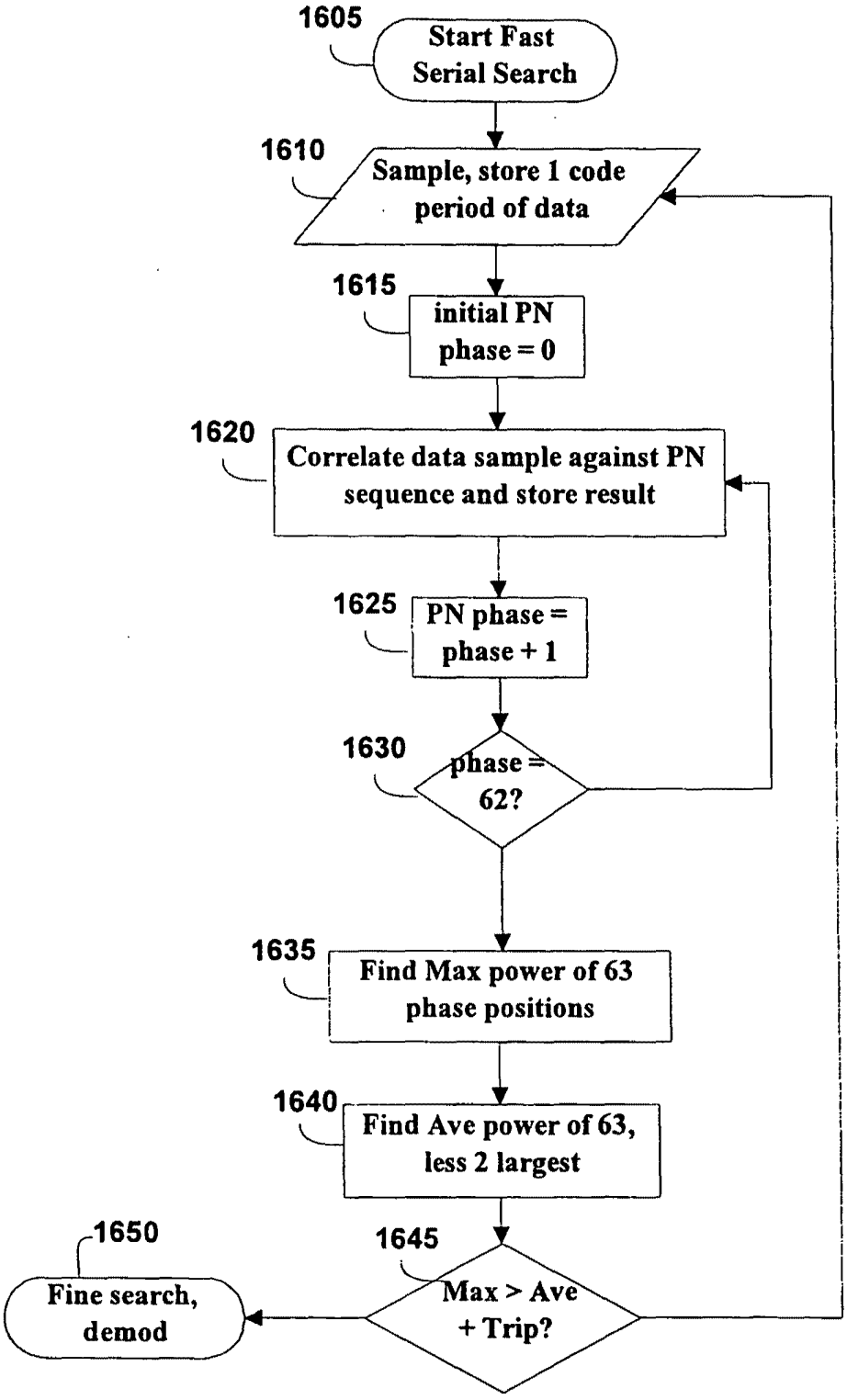

1605
Start Fast Serial Search
1610
Sample, store 1 code period of data
1615
initial PN phase = 0
1620
Correlate data sample against PN sequence and store result
1625
PN phase = phase + 1
1630
phase = 62?
1635
Find Max power of 63 phase positions
1640
Find Ave power of 63, less 2 largest
1645
Max > Ave + Trip?
1650
Fine search, demod

Figure 16

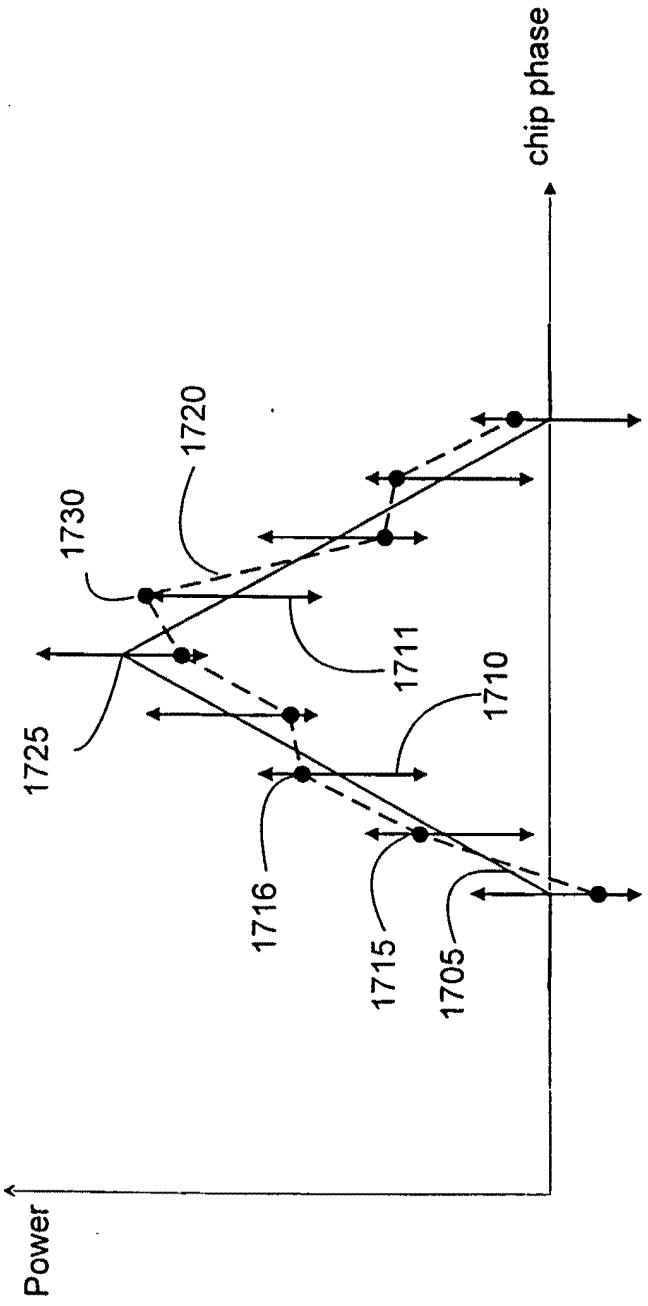


Figure 17

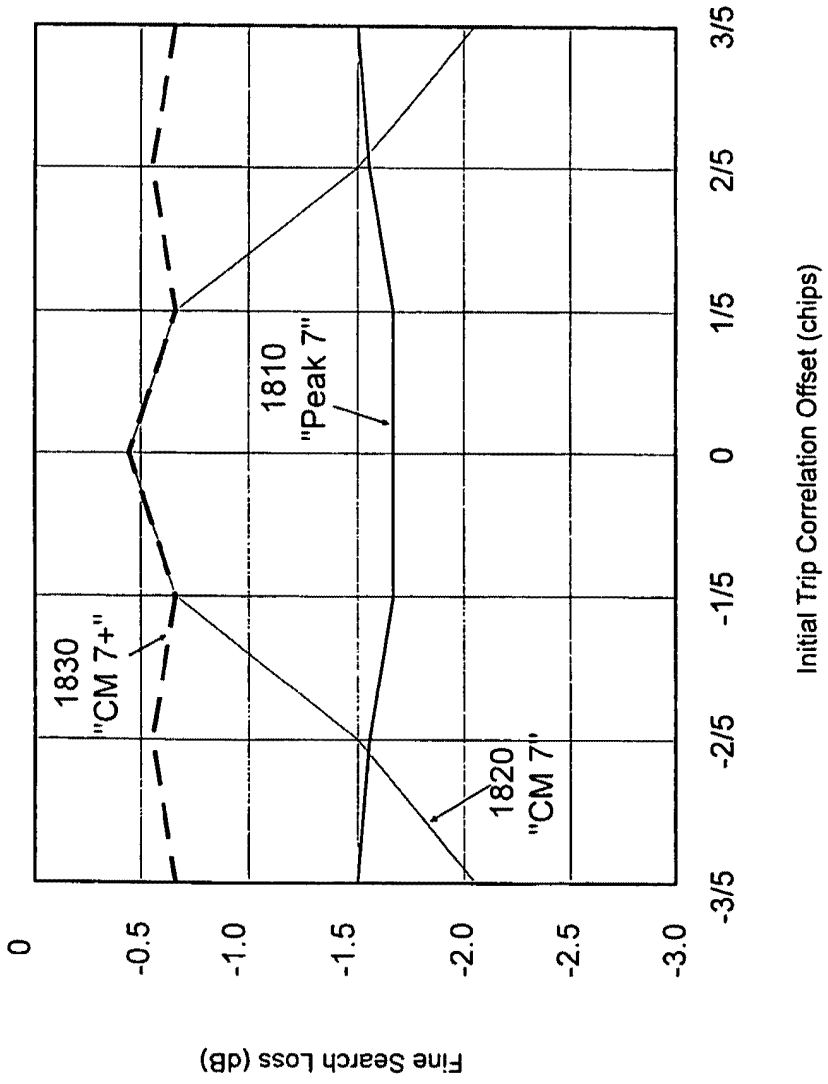

Fine Search Loss (dB)
0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
-3/5
-2/5
-1/5
0
1/5
2/5
3/5
Initial Trip Correlation Offset (chips)
1830
"CM 7+"
1810
"Peak 7"
1820
"CM 7"

Figure 18

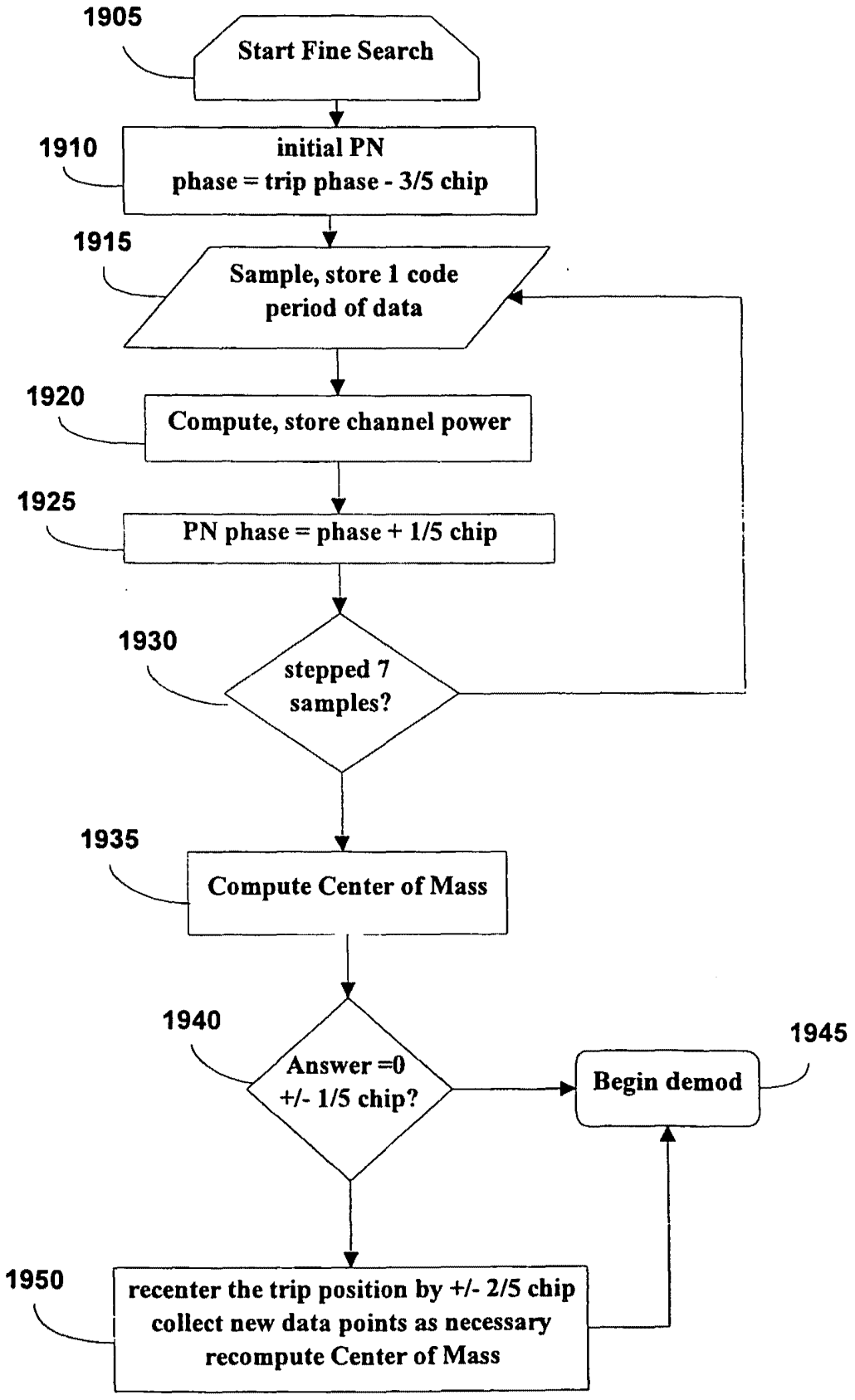

1905
Start Fine Search
1910
initial PN
phase = trip phase - 3/5 chip
1915
Sample, store 1 code
period of data
1920
Compute, store channel power
1925
PN phase = phase + 1/5 chip
1930
stepped 7
samples?
1935
Compute Center of Mass
1940
Answer =0
+/- 1/5 chip?
1945
Begin demod
1950
recenter the trip position by +/- 2/5 chip
collect new data points as necessary
recompute Center of Mass

Figure 19

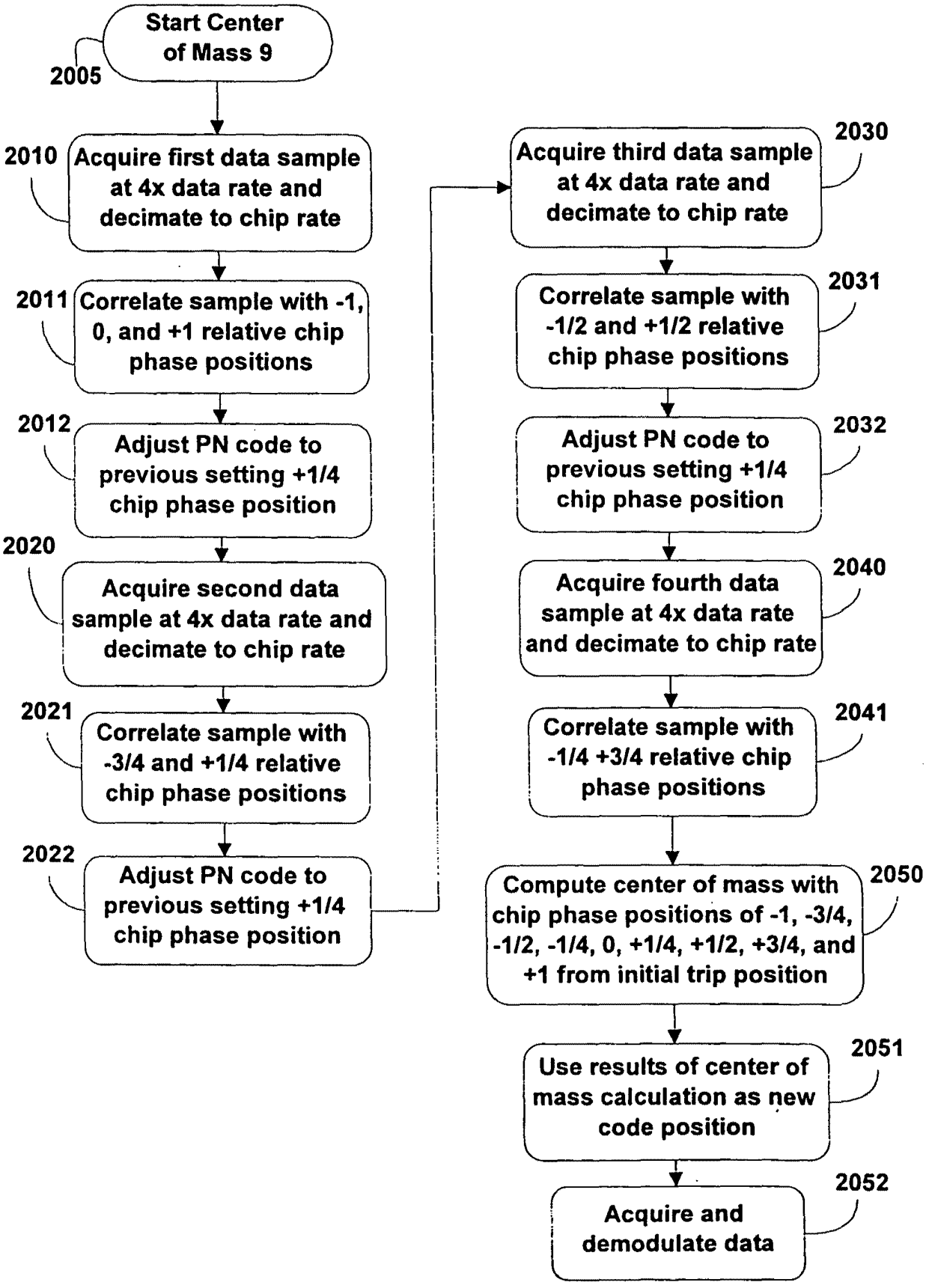

Start Center of Mass 9
2005
2010
Acquire first data sample at 4x data rate and decimate to chip rate
2011
Correlate sample with -1, 0, and +1 relative chip phase positions
2012
Adjust PN code to previous setting +1/4 chip phase position
2020
Acquire second data sample at 4x data rate and decimate to chip rate
2021
Correlate sample with -3/4 and +1/4 relative chip phase positions
2022
Adjust PN code to previous setting +1/4 chip phase position
2030
Acquire third data sample at 4x data rate and decimate to chip rate
2031
Correlate sample with -1/2 and +1/2 relative chip phase positions
2032
Adjust PN code to previous setting +1/4 chip phase position
2040
Acquire fourth data sample at 4x data rate and decimate to chip rate
2041
Correlate sample with -1/4 +3/4 relative chip phase positions
2050
Compute center of mass with chip phase positions of -1, -3/4, -1/2, -1/4, 0, +1/4, +1/2, +3/4, and +1 from initial trip position
2051
Use results of center of mass calculation as new code position
2052
Acquire and demodulate data

Figure 20

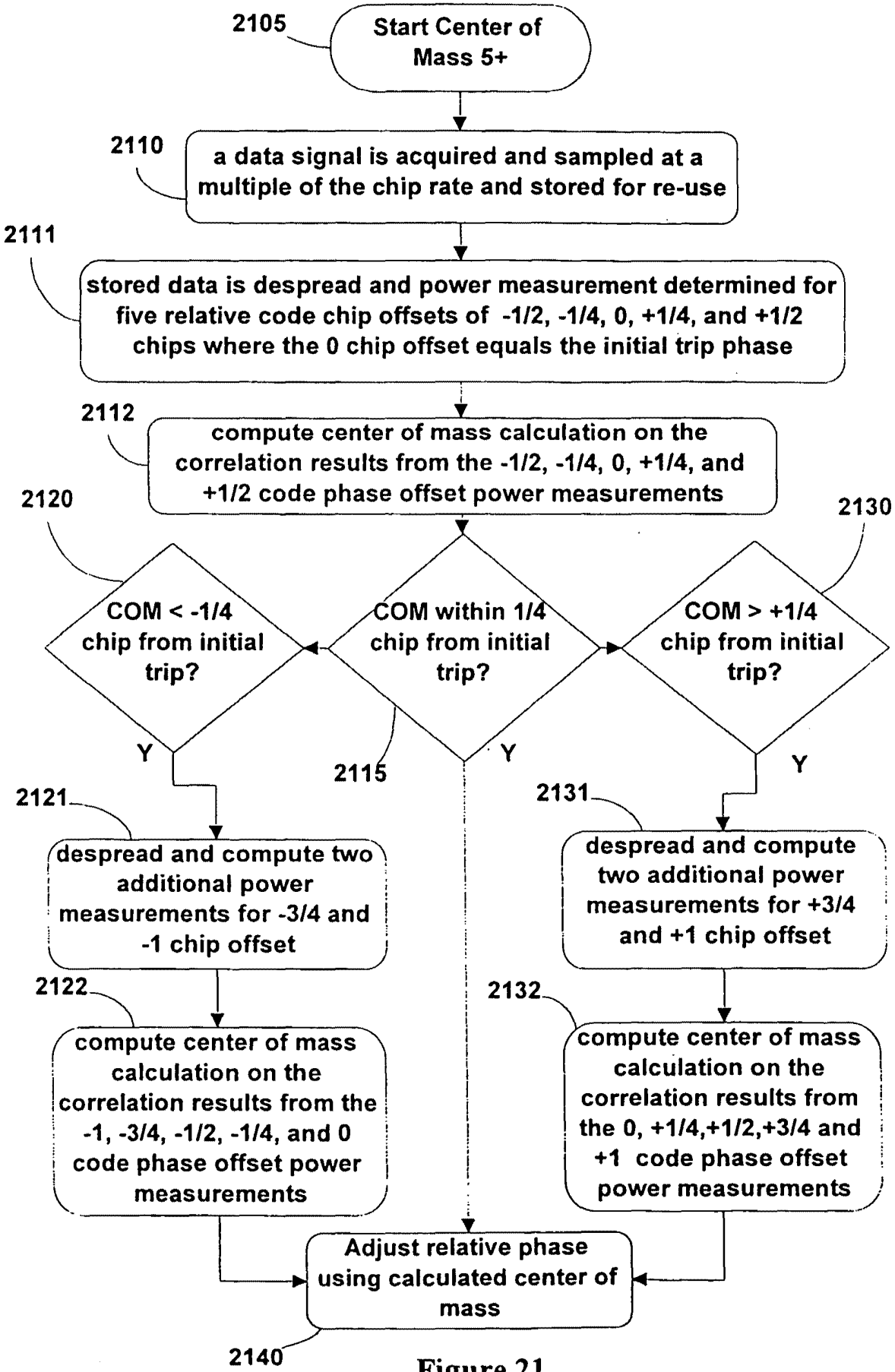

2105
Start Center of Mass 5+
2110
a data signal is acquired and sampled at a multiple of the chip rate and stored for re-use
2111
stored data is despread and power measurement determined for five relative code chip offsets of -1/2, -1/4, 0, +1/4, and +1/2 chips where the 0 chip offset equals the initial trip phase
2112
compute center of mass calculation on the correlation results from the -1/2, -1/4, 0, +1/4, and +1/2 code phase offset power measurements
2120
COM < -1/4 chip from initial trip?
COM within 1/4 chip from initial trip?
2130
COM > +1/4 chip from initial trip?
Y
2115
Y
Y
2121
despread and compute two additional power measurements for -3/4 and -1 chip offset
2131
despread and compute two additional power measurements for +3/4 and +1 chip offset
2122
compute center of mass calculation on the correlation results from the -1, -3/4, -1/2, -1/4, and 0 code phase offset power measurements
2132
compute center of mass calculation on the correlation results from the 0, +1/4,+1/2,+3/4 and +1 code phase offset power measurements
Adjust relative phase using calculated center of mass
2140

Figure 21

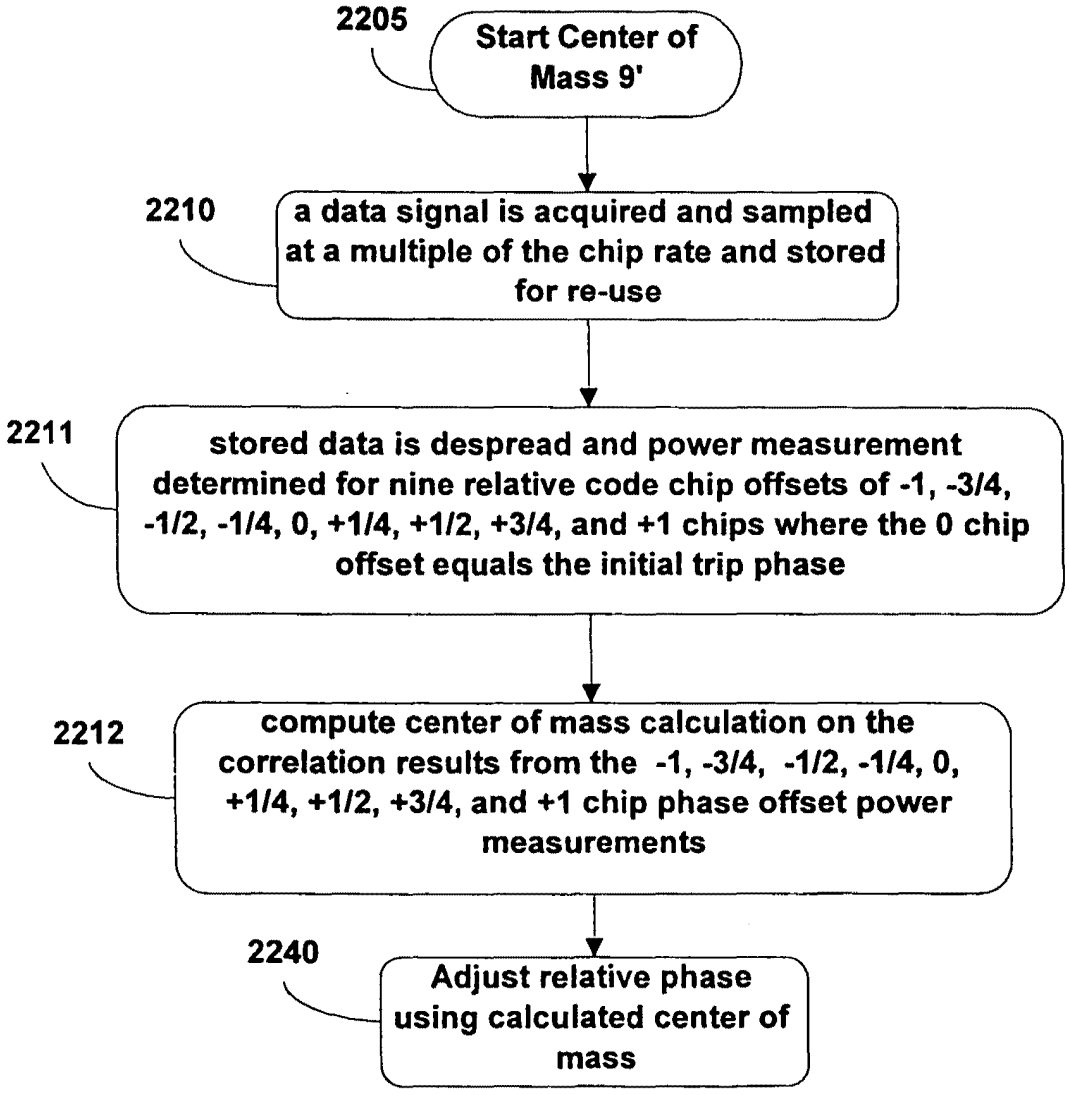

2205
Start Center of Mass 9'
2210
a data signal is acquired and sampled at a multiple of the chip rate and stored for re-use
2211
stored data is despread and power measurement determined for nine relative code chip offsets of -1, -3/4, -1/2, -1/4, 0, +1/4, +1/2, +3/4, and +1 chips where the 0 chip offset equals the initial trip phase
2212
compute center of mass calculation on the correlation results from the -1, -3/4, -1/2, -1/4, 0, +1/4, +1/2, +3/4, and +1 chip phase offset power measurements
2240
Adjust relative phase using calculated center of mass

Figure 22

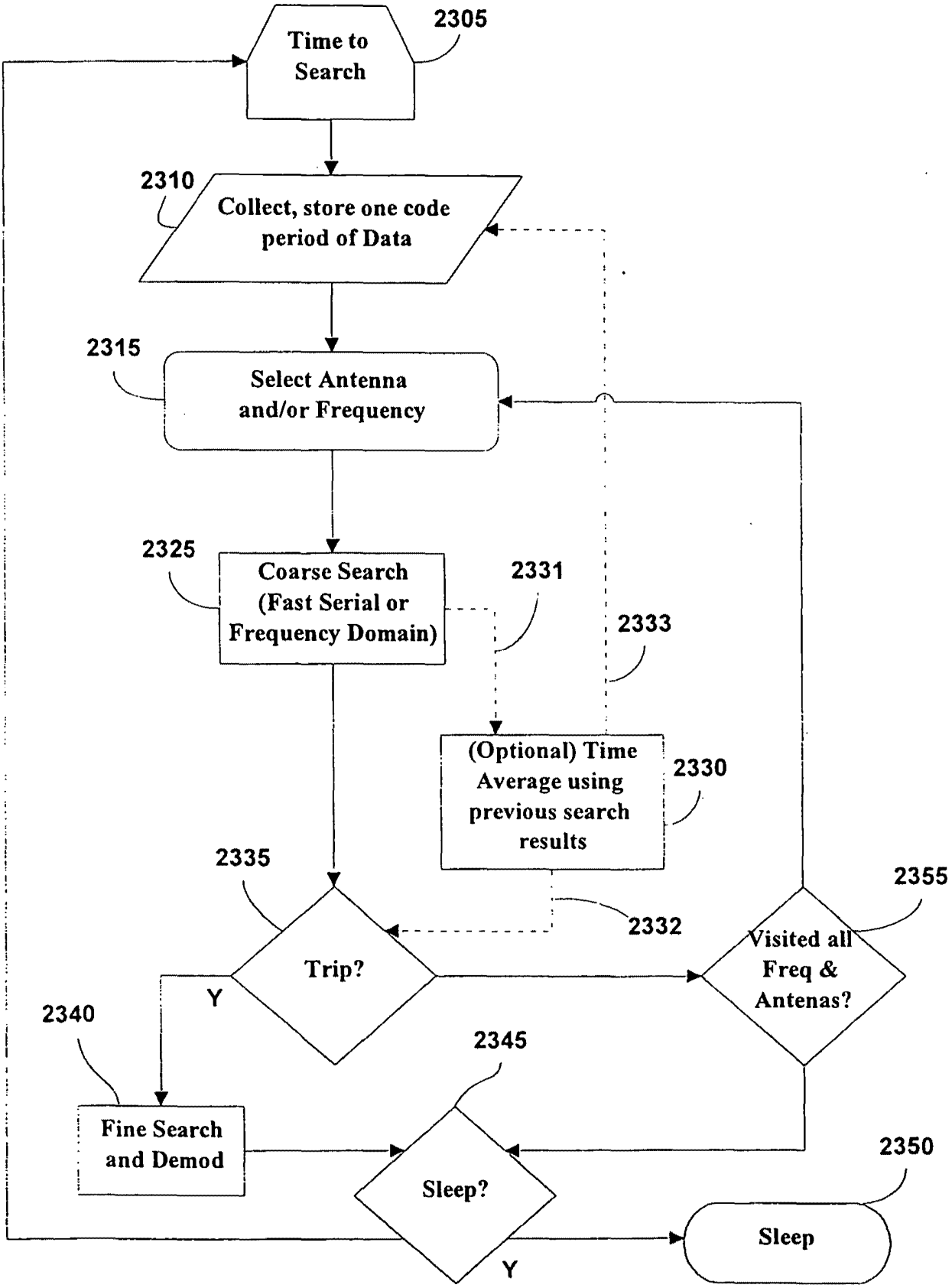

Time to Search
2305
2310
Collect, store one code period of Data
2315
Select Antenna and/or Frequency
2325
Coarse Search (Fast Serial or Frequency Domain)
2331
2333
(Optional) Time Average using previous search results
2330
2335
Trip?
Y
2332
2355
Visited all Freq & Antenas?
2340
Fine Search and Demod
2345
Sleep?
Y
2350
Sleep

Figure 23

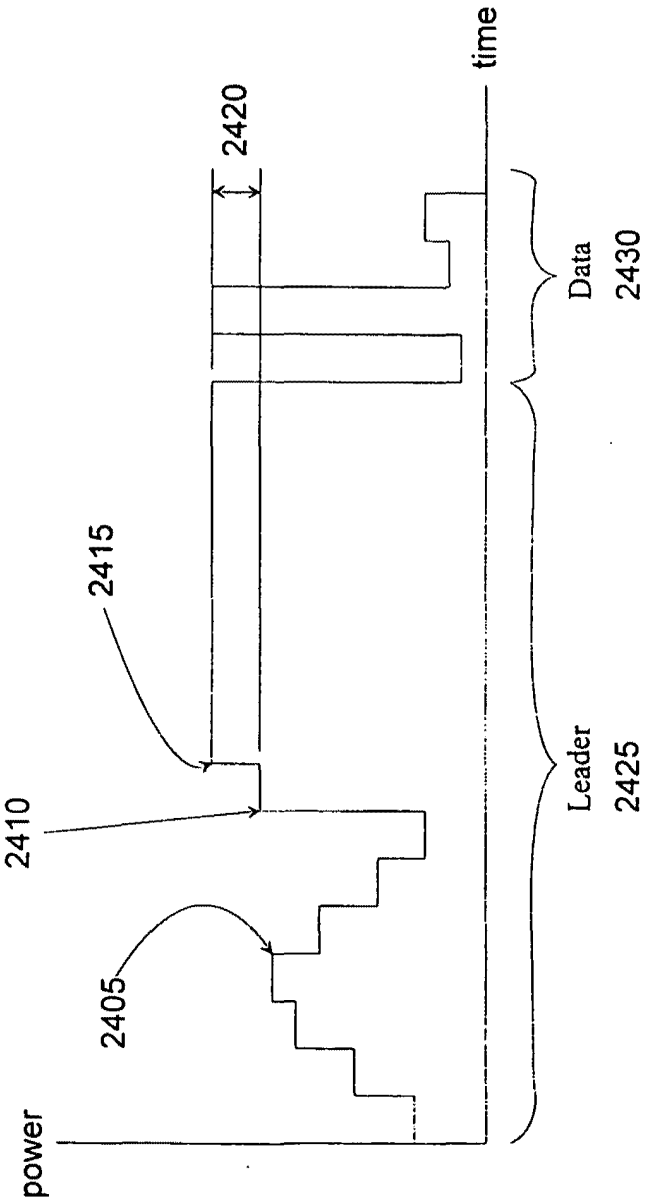


Figure 24

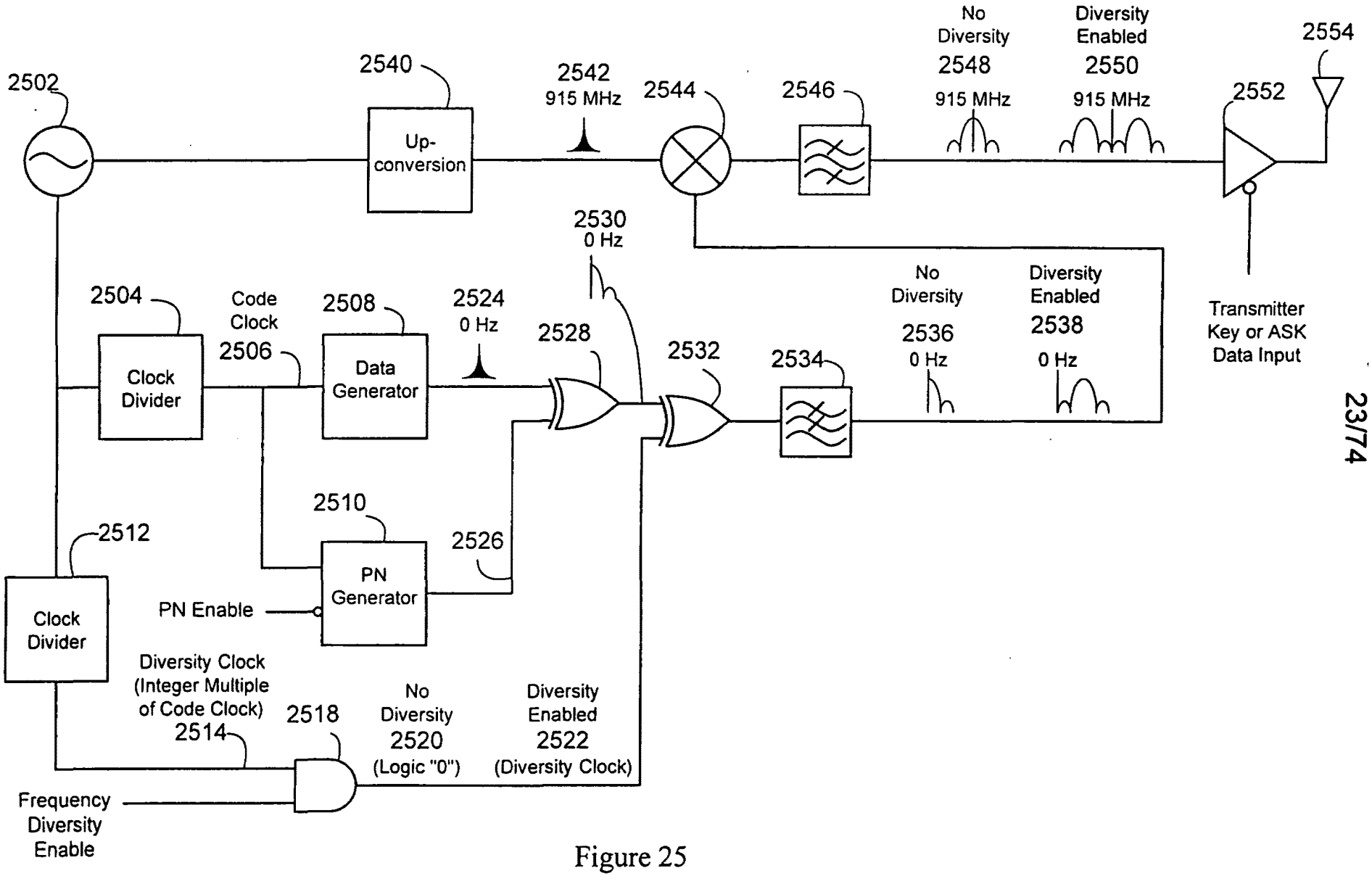

2502
2540
Up-conversion
2542
915 MHz
2544
2546
No Diversity
2548
915 MHz
Diversity Enabled
2550
915 MHz
2552
2554
Transmitter Key or ASK Data Input
2530
0 Hz
2504
Clock Divider
Code Clock
2506
2508
Data Generator
2524
0 Hz
2528
2532
2534
No Diversity
2536
0 Hz
Diversity Enabled
2538
0 Hz
2510
PN Generator
2526
2512
Clock Divider
PN Enable
Diversity Clock (Integer Multiple of Code Clock)
2514
2518
No Diversity
2520
(Logic "0")
Diversity Enabled
2522
(Diversity Clock)
Frequency Diversity Enable

Figure 25

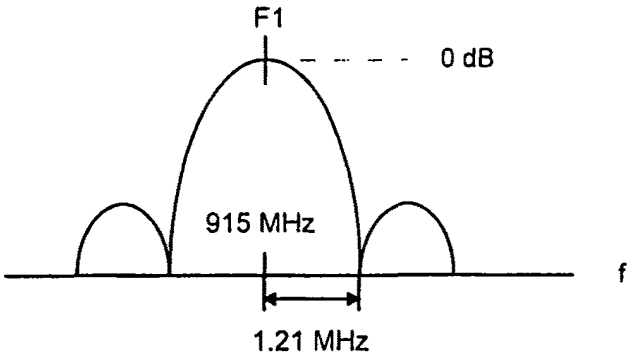


Figure 26A

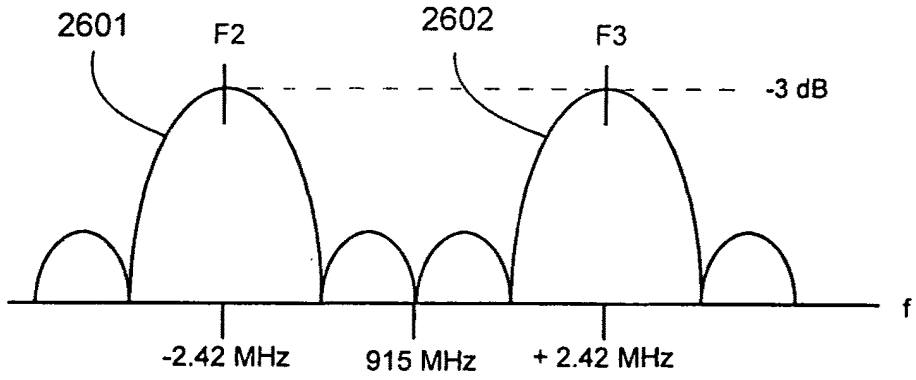


Figure 26B

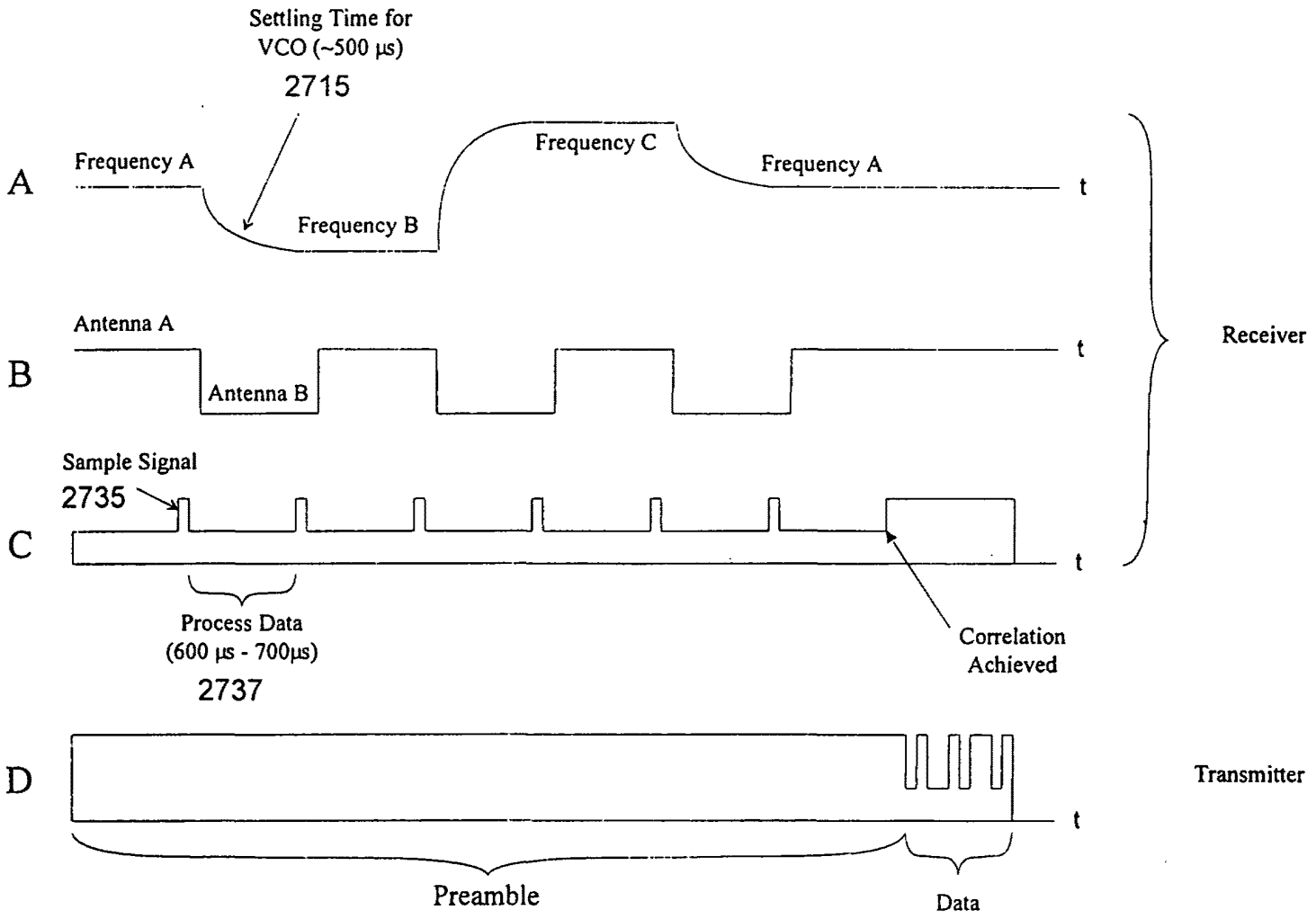

Settling Time for
VCO (~500 µs)
2715
A
Frequency A
Frequency B
Frequency C
Frequency A
t
B
Antenna A
Antenna B
t
Receiver
Sample Signal
2735
C
t
Process Data
(600 µs - 700µs)
2737
Correlation
Achieved
D
Transmitter
t
Preamble
Data

Figure 27

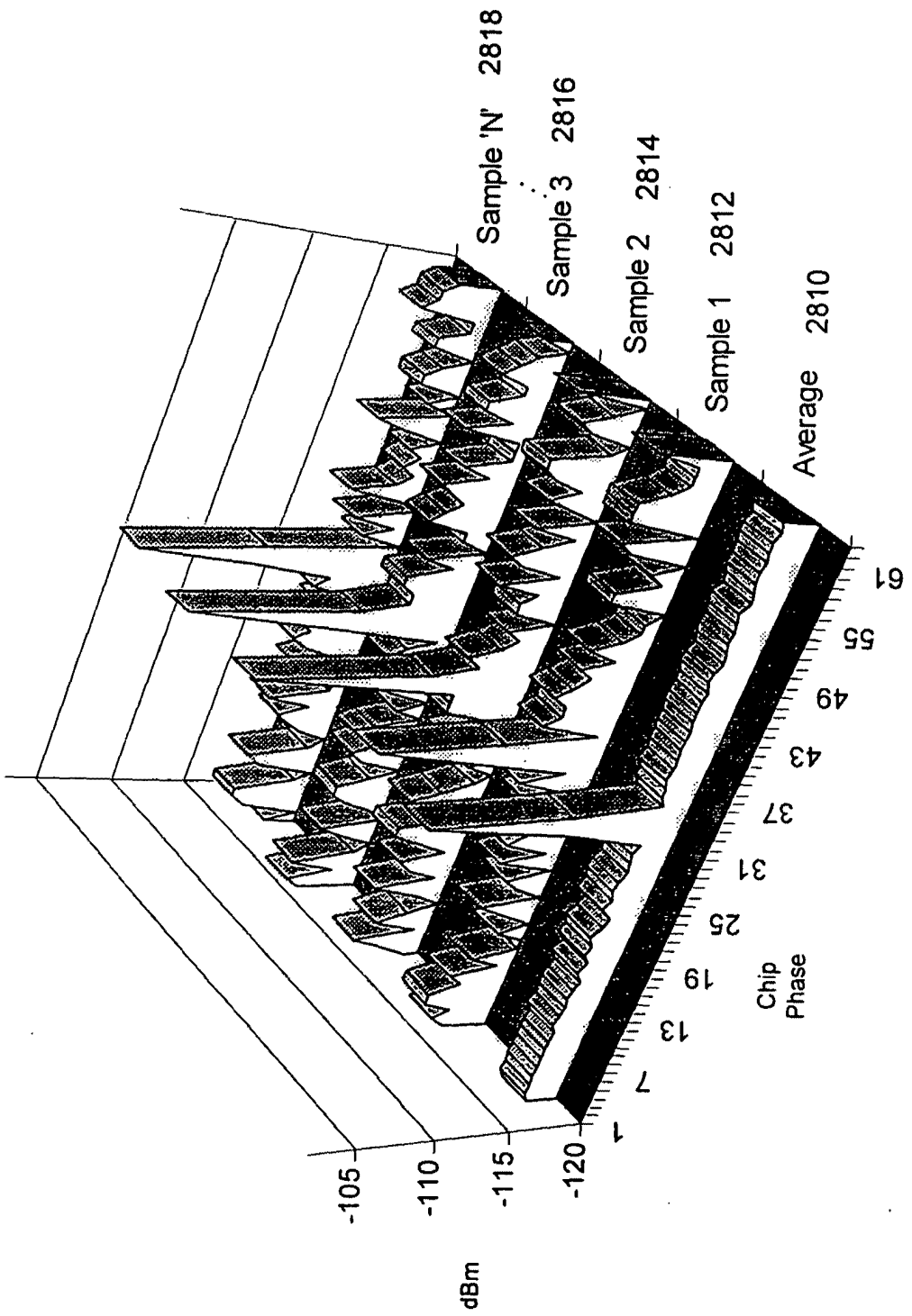

Sample 'N' 2818
Sample 3 2816
Sample 2 2814
Sample 1 2812
Average 2810
-105
-110
-115
-120
dBm
1
7
13
19
25
31
37
43
49
55
61
Chip Phase

Figure 28

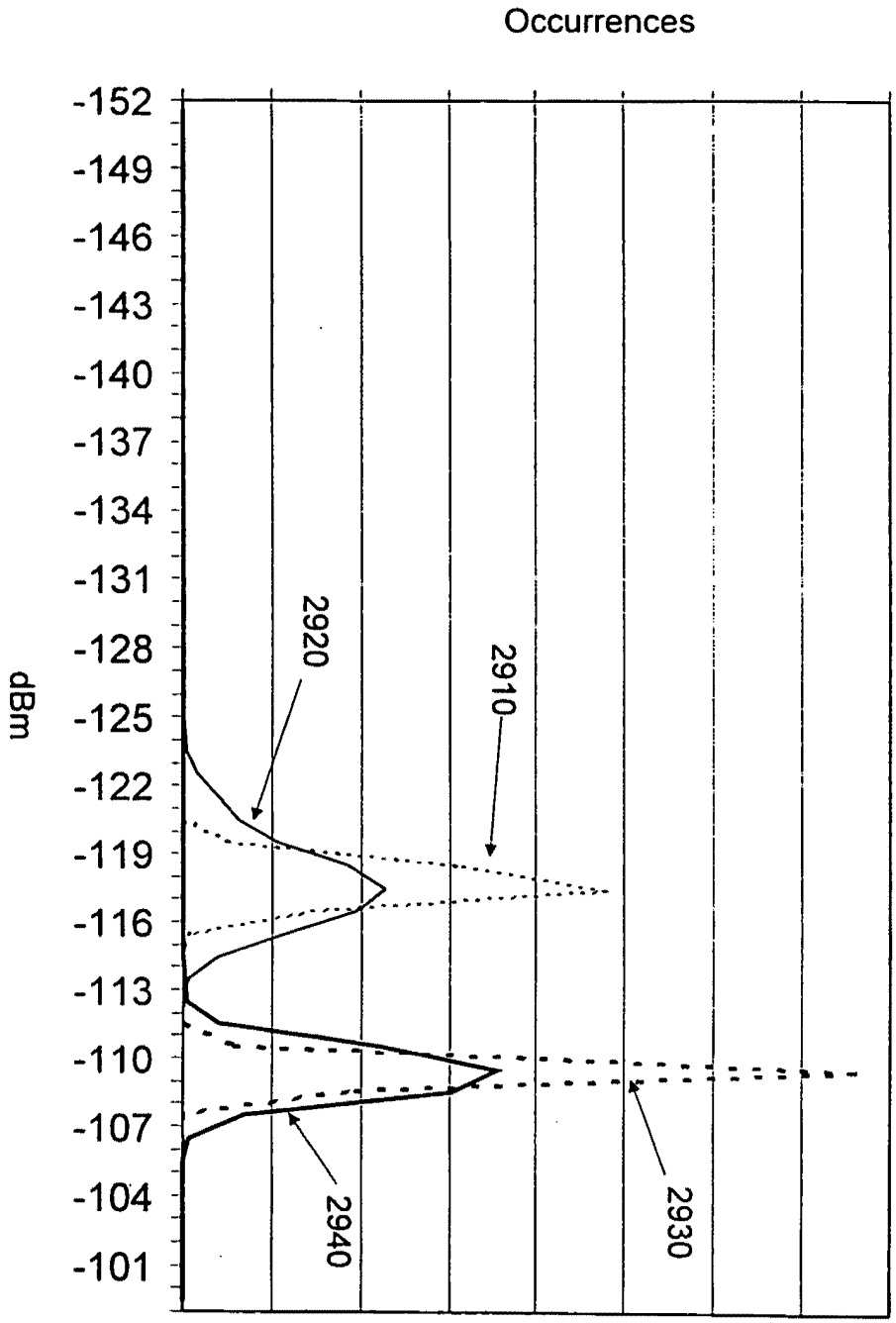

Occurrences
-152
-149
-146
-143
-140
-137
-134
-131
-128
-125
-122
-119
-116
-113
-110
-107
-104
-101
dBm
2920
2910
2940
2930

Figure 29

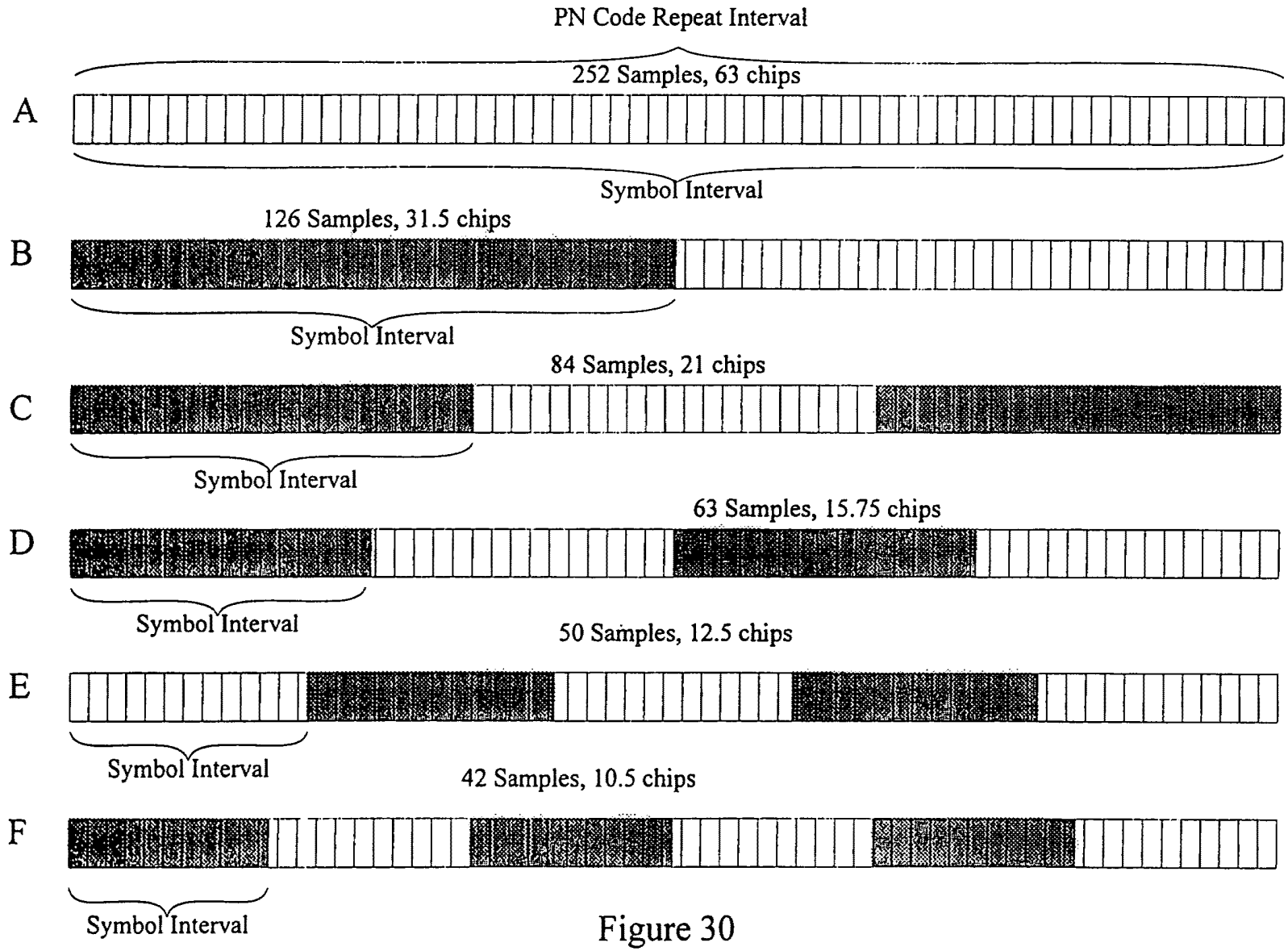

PN Code Repeat Interval
252 Samples, 63 chips
A
Symbol Interval
126 Samples, 31.5 chips
B
Symbol Interval
84 Samples, 21 chips
C
Symbol Interval
63 Samples, 15.75 chips
D
Symbol Interval
50 Samples, 12.5 chips
E
Symbol Interval
42 Samples, 10.5 chips
F
Symbol Interval

Figure 30

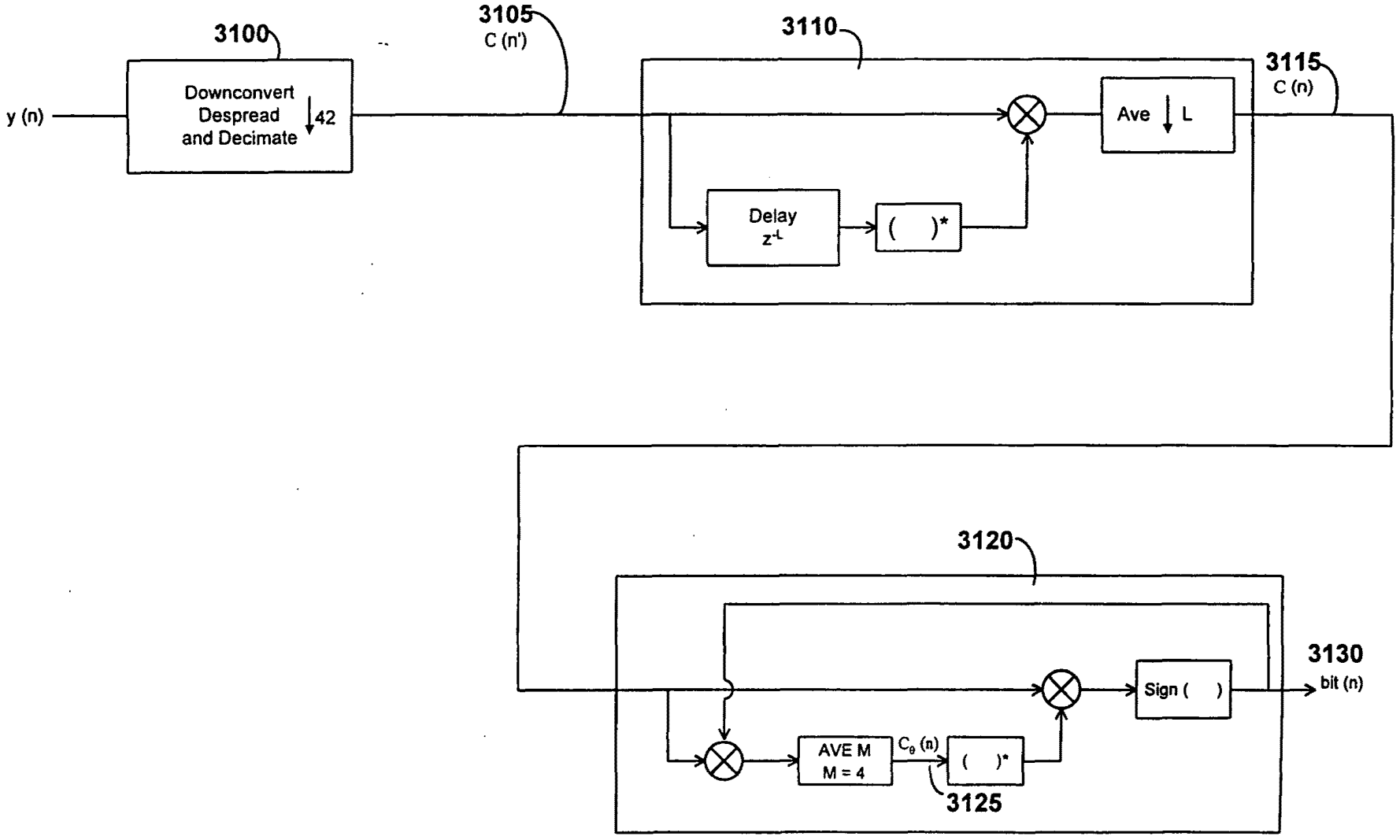

3100
3105
C (n')
3110
3115
C (n)
y (n)
Downconvert
Despread
and Decimate
42
Ave
L
Delay
z^{-L}
( )*
3120
3130
bit (n)
Sign ( )
AVE M
M = 4
C_θ (n)
( )*
3125

Figure 31

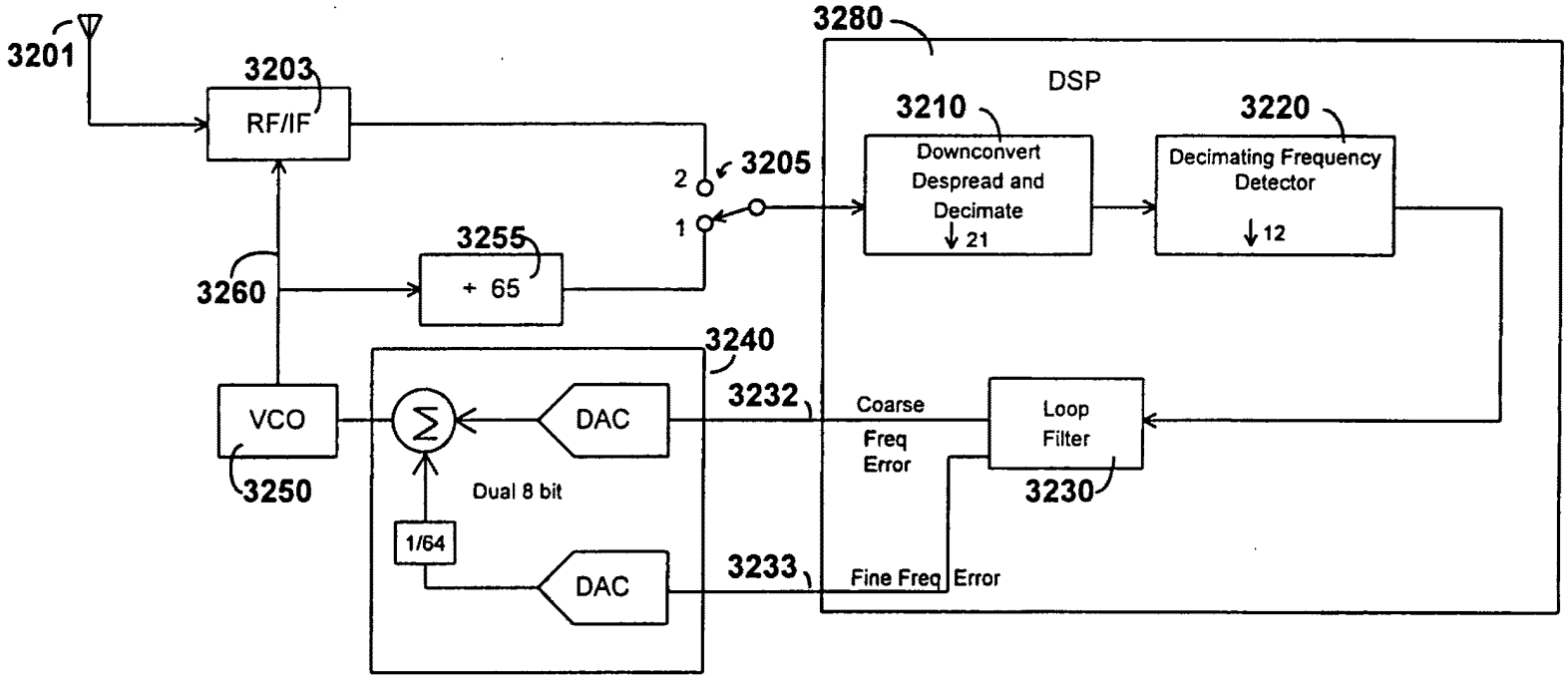

3201
3203
RF/IF
3280
DSP
3210
Downconvert
Despread and
Decimate
↓21
3220
Decimating Frequency
Detector
↓12
2
1
3205
3255
÷ 65
3260
3240
VCO
3250
DAC
3232
Coarse
Freq
Error
Loop
Filter
3230
Dual 8 bit
1/64
DAC
3233
Fine Freq Error

Figure 32

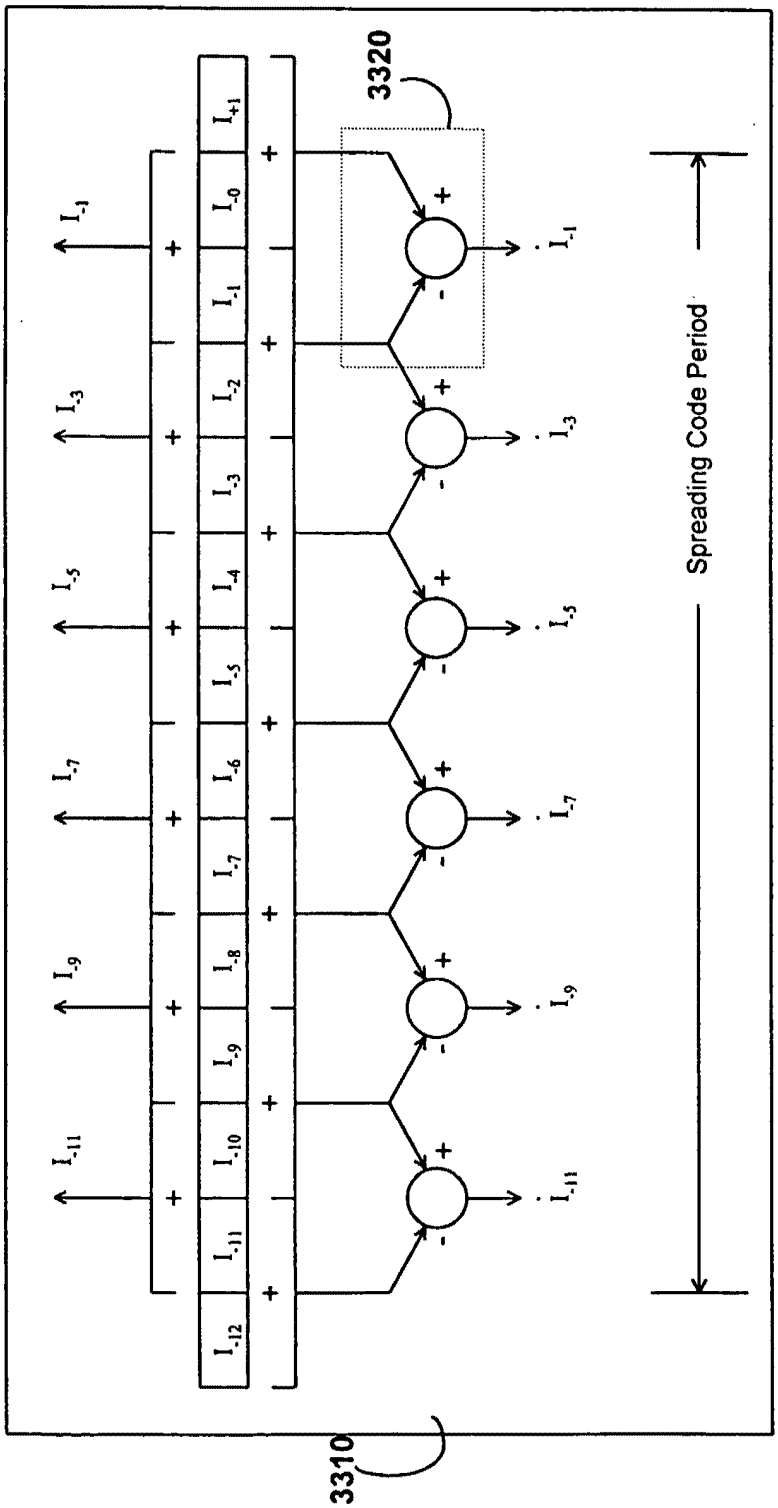

3320
3310
Spreading Code Period
I_{+1} I_0 I_{-1} I_{-2} I_{-3} I_{-4} I_{-5} I_{-6} I_{-7} I_{-8} I_{-9} I_{-10} I_{-11} I_{-12}
I_{-1} I_{-3} I_{-5} I_{-7} I_{-9} I_{-11}
$\dot{I}_{-1}$ $\dot{I}_{-3}$ $\dot{I}_{-5}$ $\dot{I}_{-7}$ $\dot{I}_{-9}$ $\dot{I}_{-11}$

Figure 33

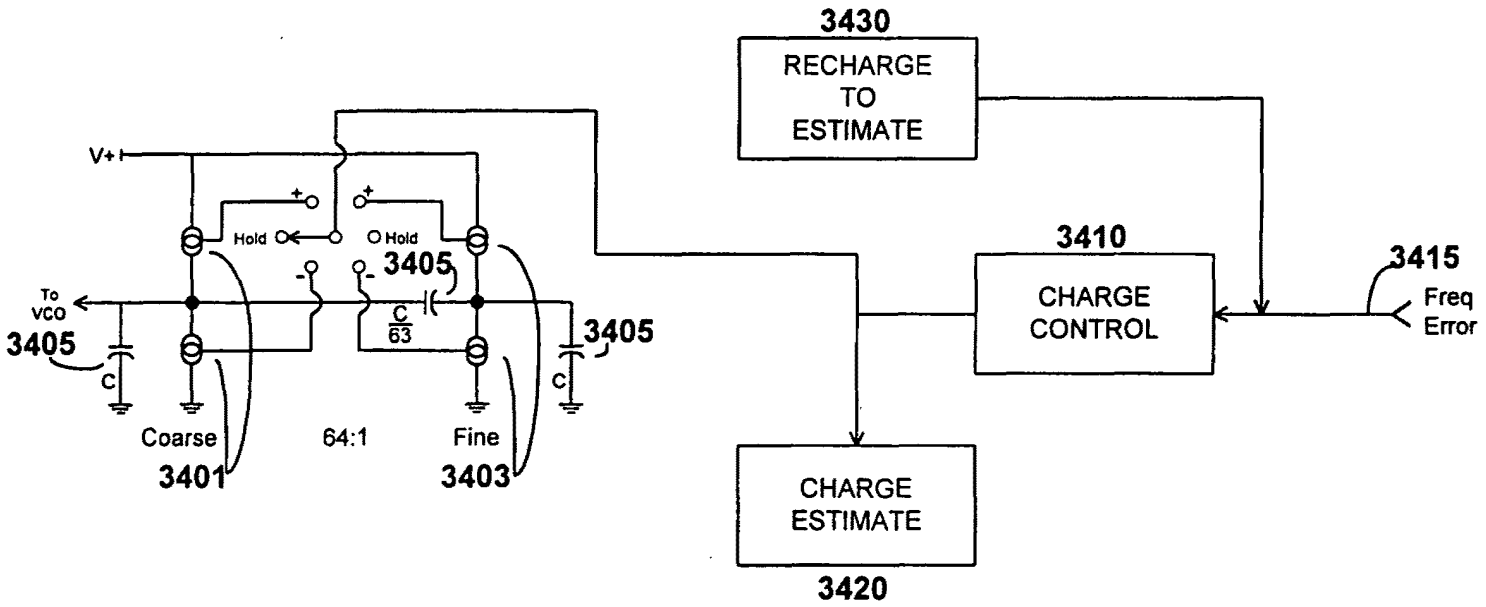

3430
RECHARGE TO ESTIMATE
3410
CHARGE CONTROL
3415
Freq Error
CHARGE ESTIMATE
3420
V+
Hold
Hold
3405
To VCO
3405
3405
C
C/63
C
Coarse
64:1
Fine
3401
3403

Figure 34

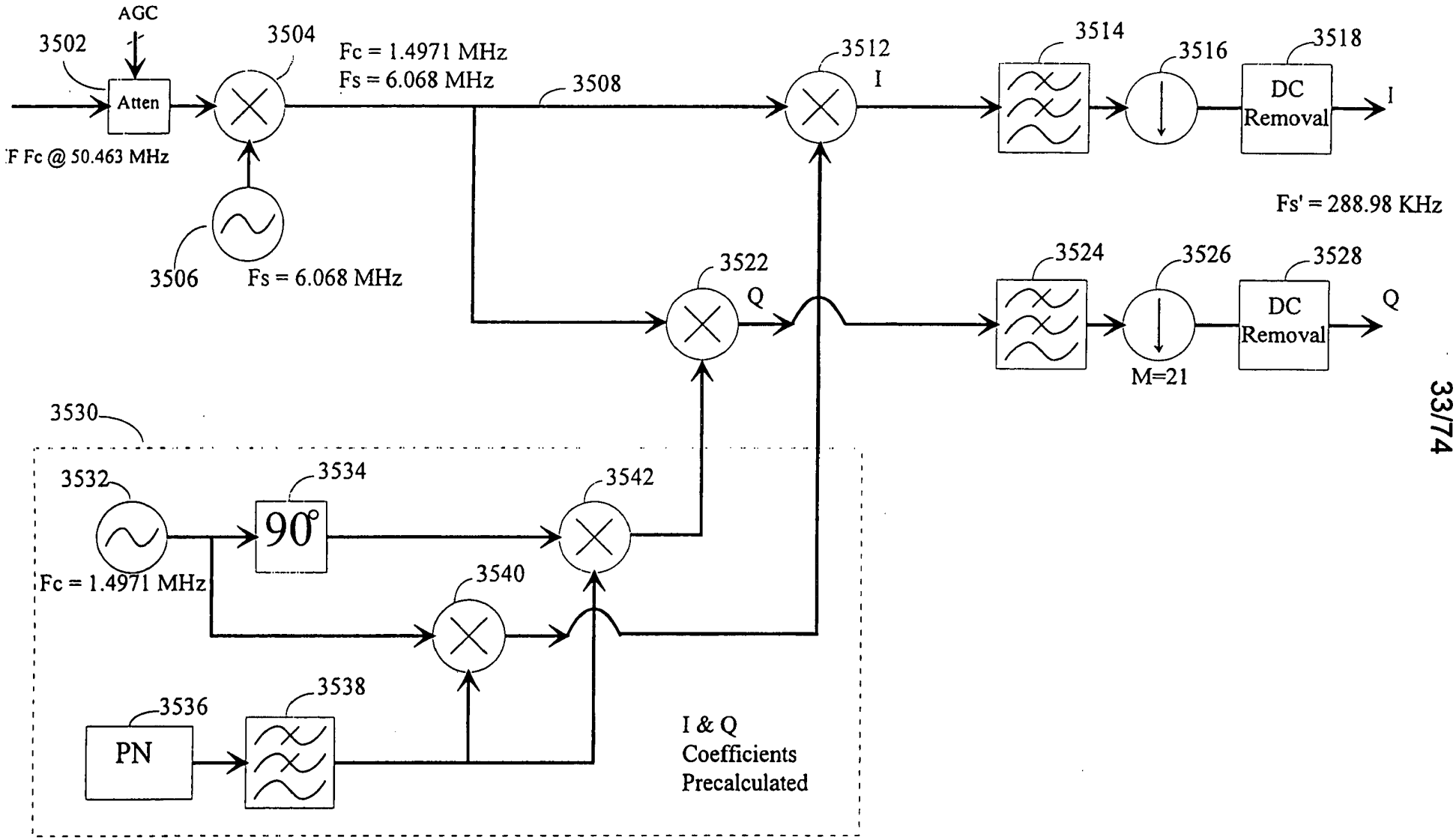

AGC
3502
Atten
F Fc @ 50.463 MHz
3504
Fc = 1.4971 MHz
Fs = 6.068 MHz
3508
3506
Fs = 6.068 MHz
3512
I
3514
3516
3518
DC
Removal
I
Fs' = 288.98 KHz
3522
Q
3524
3526
3528
DC
Removal
Q
M=21
3530
3532
3534
90°
Fc = 1.4971 MHz
3542
3540
3536
PN
3538
I & Q
Coefficients
Precalculated

Figure 35

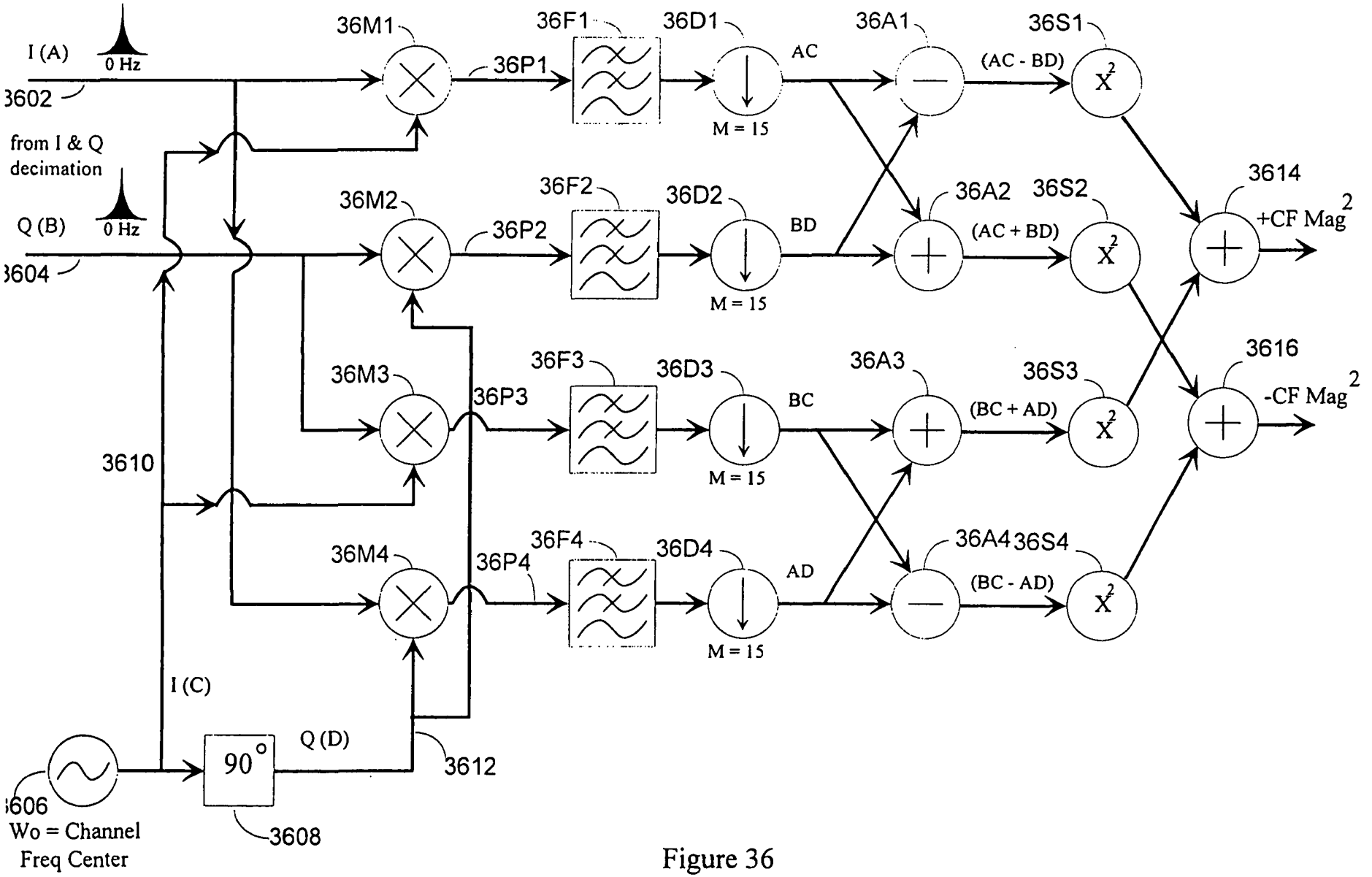

I (A)
0 Hz
3602
from I & Q decimation
Q (B)
0 Hz
3604
3610
I (C)
Q (D)
90°
3606
Wo = Channel Freq Center
3608
3612
36M1
36M2
36M3
36M4
36P1
36P2
36P3
36P4
36F1
36F2
36F3
36F4
36D1
36D2
36D3
36D4
M = 15
AC
BD
BC
AD
36A1
36A2
36A3
36A4
(AC - BD)
(AC + BD)
(BC + AD)
(BC - AD)
36S1
36S2
36S3
36S4
X²
3614
+CF Mag²
3616
-CF Mag²

Figure 36

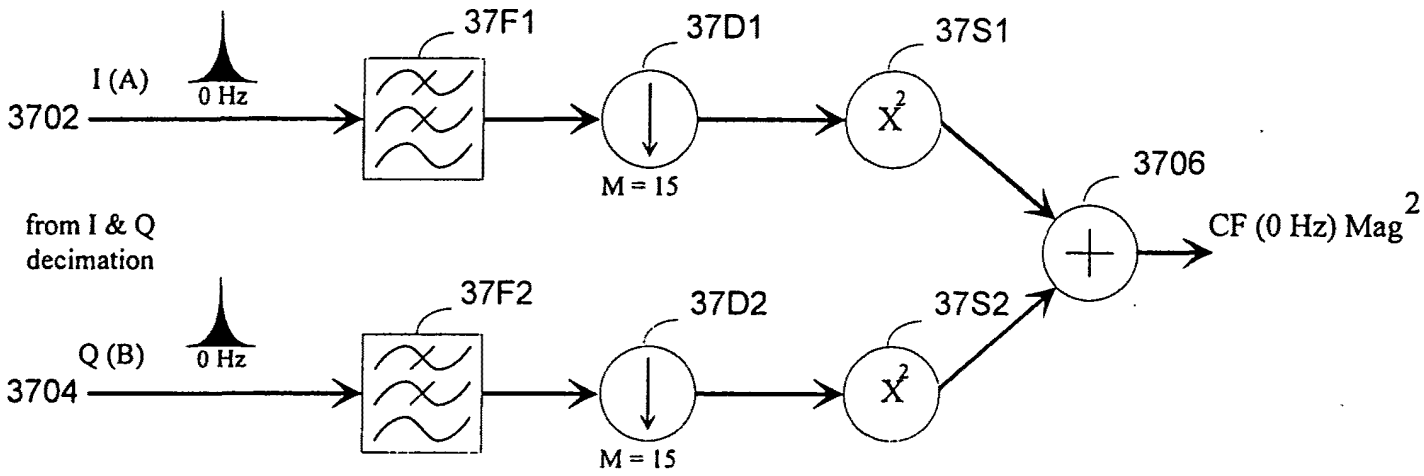

I (A)
0 Hz
3702
37F1
37D1
37S1
M = 15
3706
from I & Q
decimation
CF (0 Hz) Mag 2
Q (B)
0 Hz
3704
37F2
37D2
37S2
M = 15

Figure 37

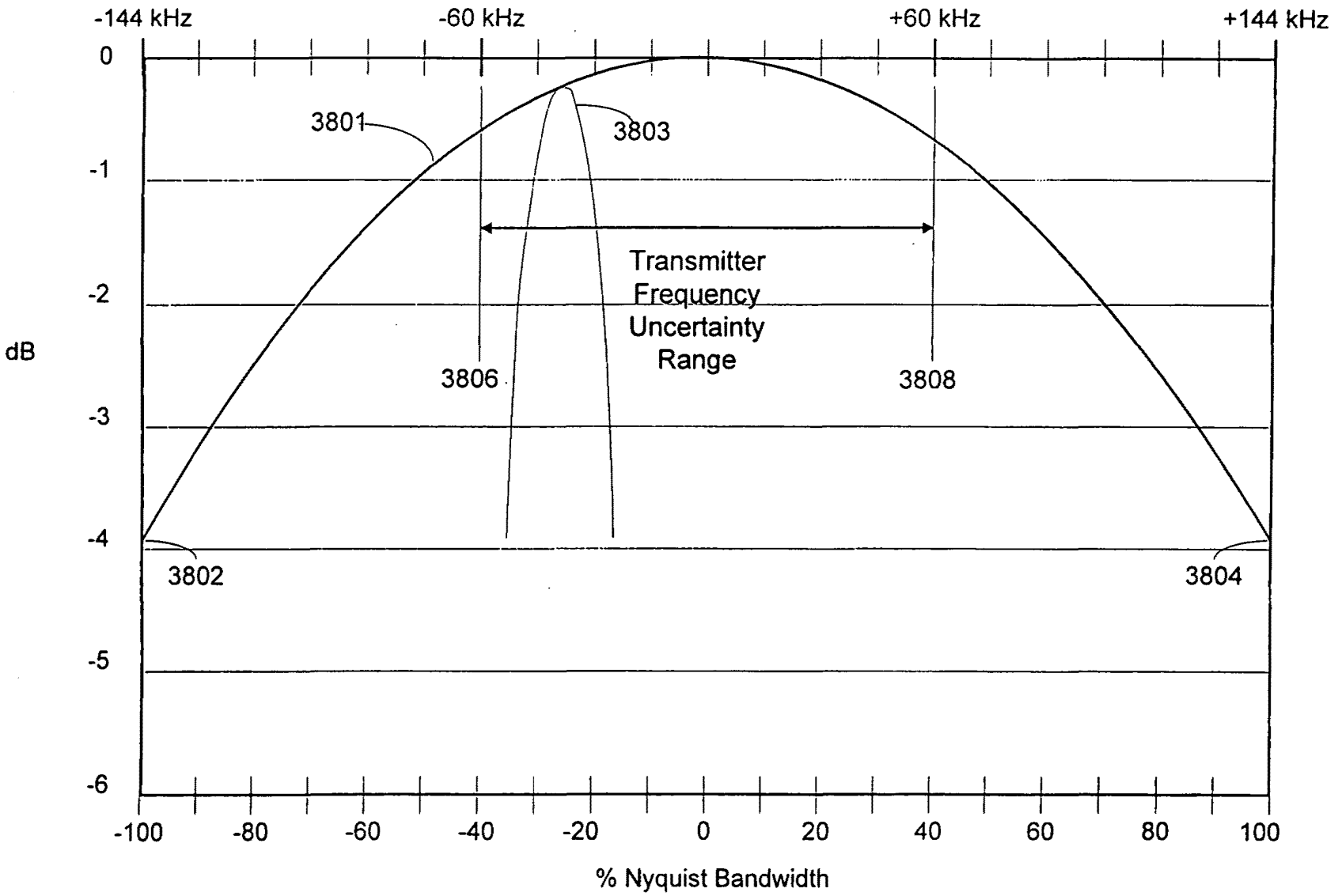

-144 kHz
-60 kHz
+60 kHz
+144 kHz
0
-1
-2
-3
-4
-5
-6
dB
3801
3803
Transmitter
Frequency
Uncertainty
Range
3806
3808
3802
3804
-100
-80
-60
-40
-20
0
20
40
60
80
100
% Nyquist Bandwidth

Figure 38

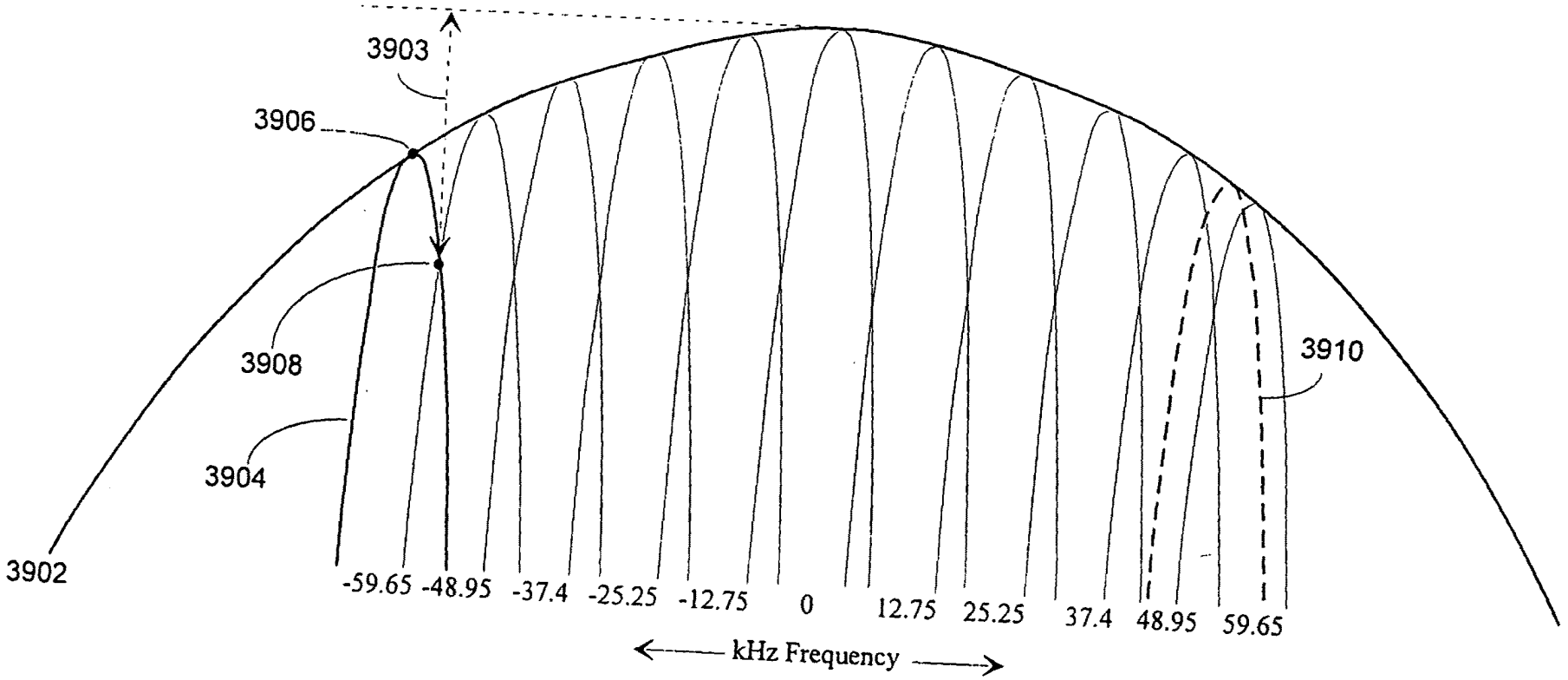

3903
3906
3908
3904
3902
3910
-59.65
-48.95
-37.4
-25.25
-12.75
0
12.75
25.25
37.4
48.95
59.65
kHz Frequency

Figure 39

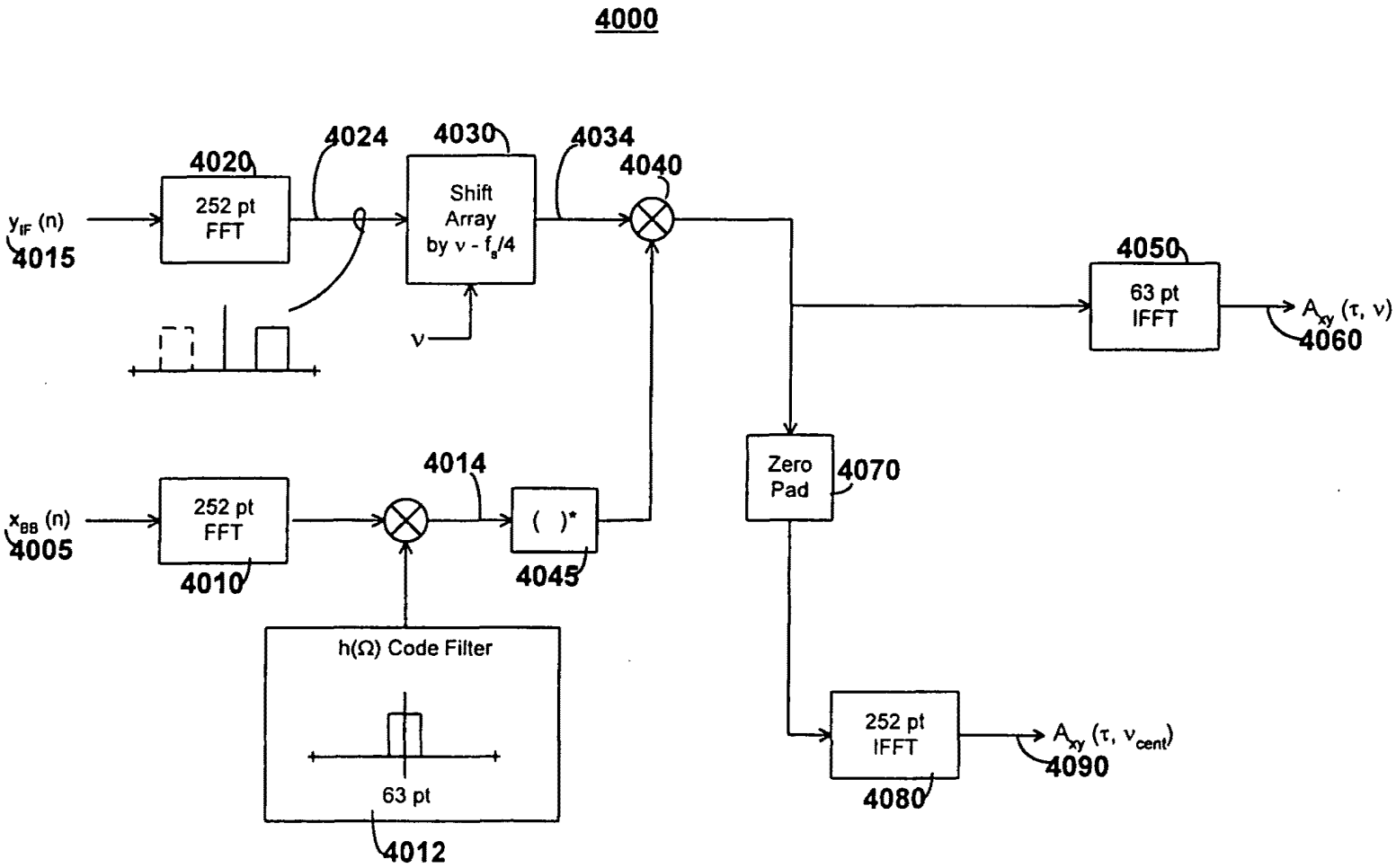
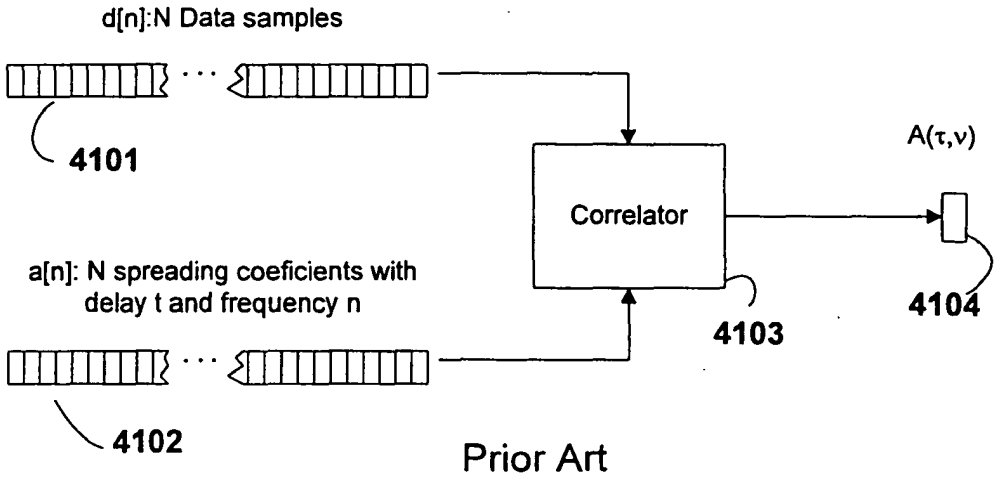
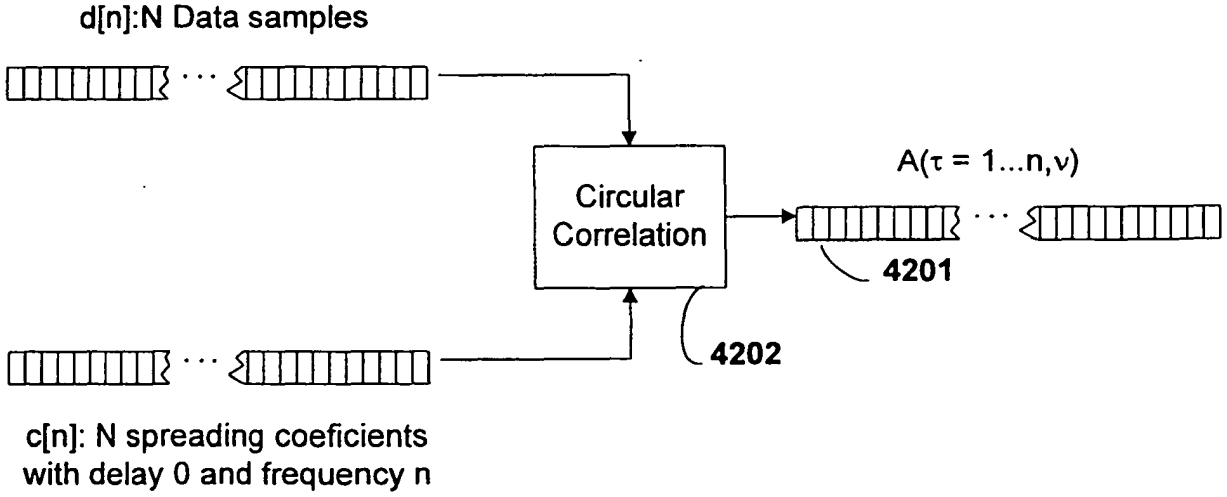

4000
4020
4024
4030
4034
4040
y_{IF} (n)
4015
252 pt FFT
Shift Array by $\nu - f_s/4$
ν
4050
63 pt IFFT
A_{xy} (τ, ν)
4060
4014
x_{BB} (n)
4005
252 pt FFT
4010
( )*
4045
Zero Pad
4070
h(Ω) Code Filter
63 pt
4012
252 pt IFFT
4080
A_{xy} (τ, ν_{cent})
4090

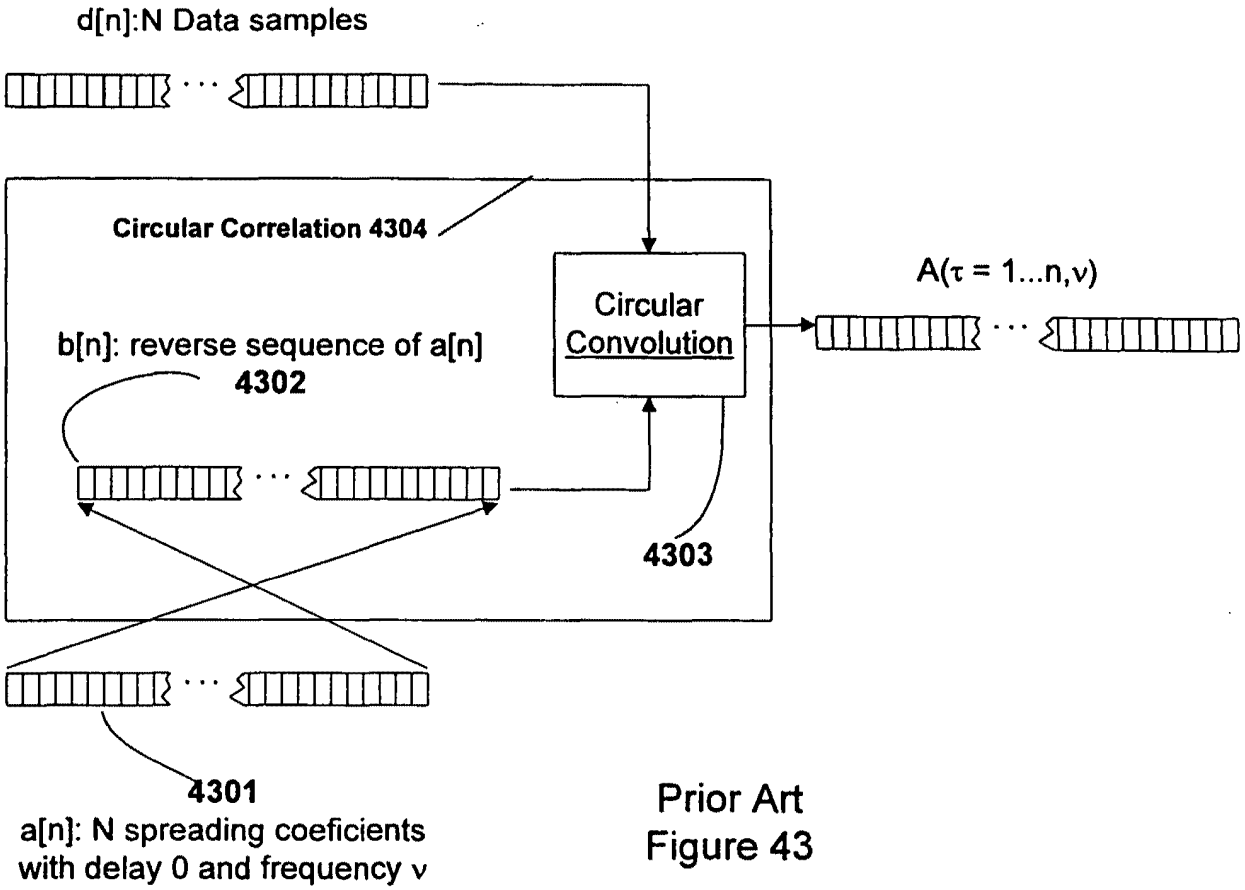
Figure 40



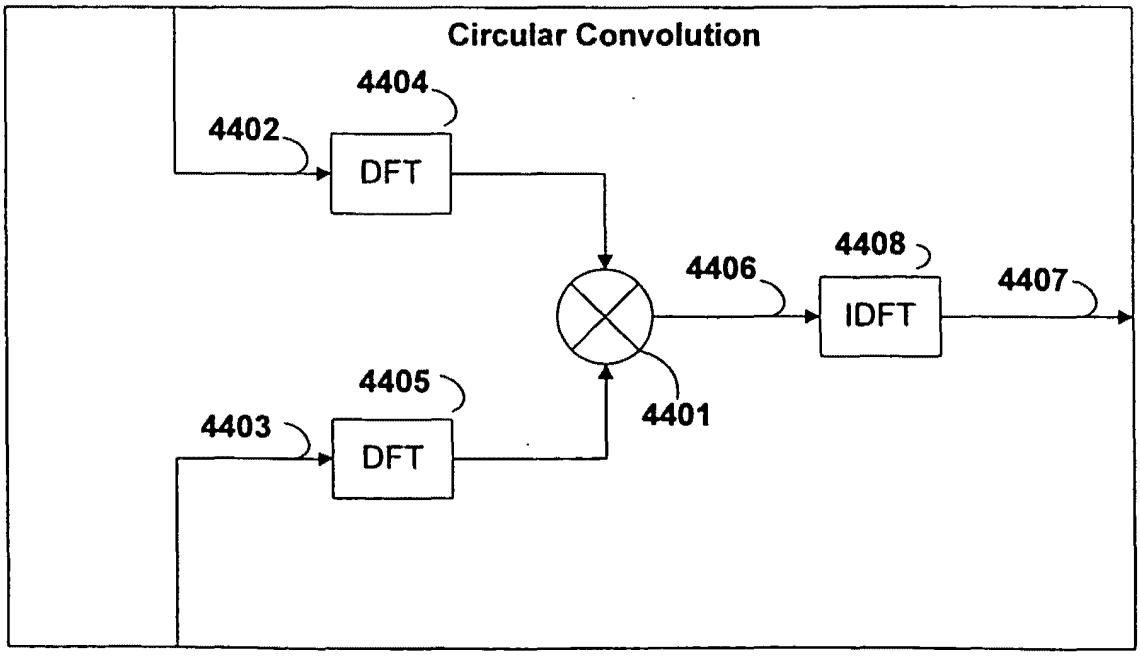
Prior Art
Figure 41



Prior Art
Figure 42



Prior Art
Figure 43



Prior Art
Figure 44

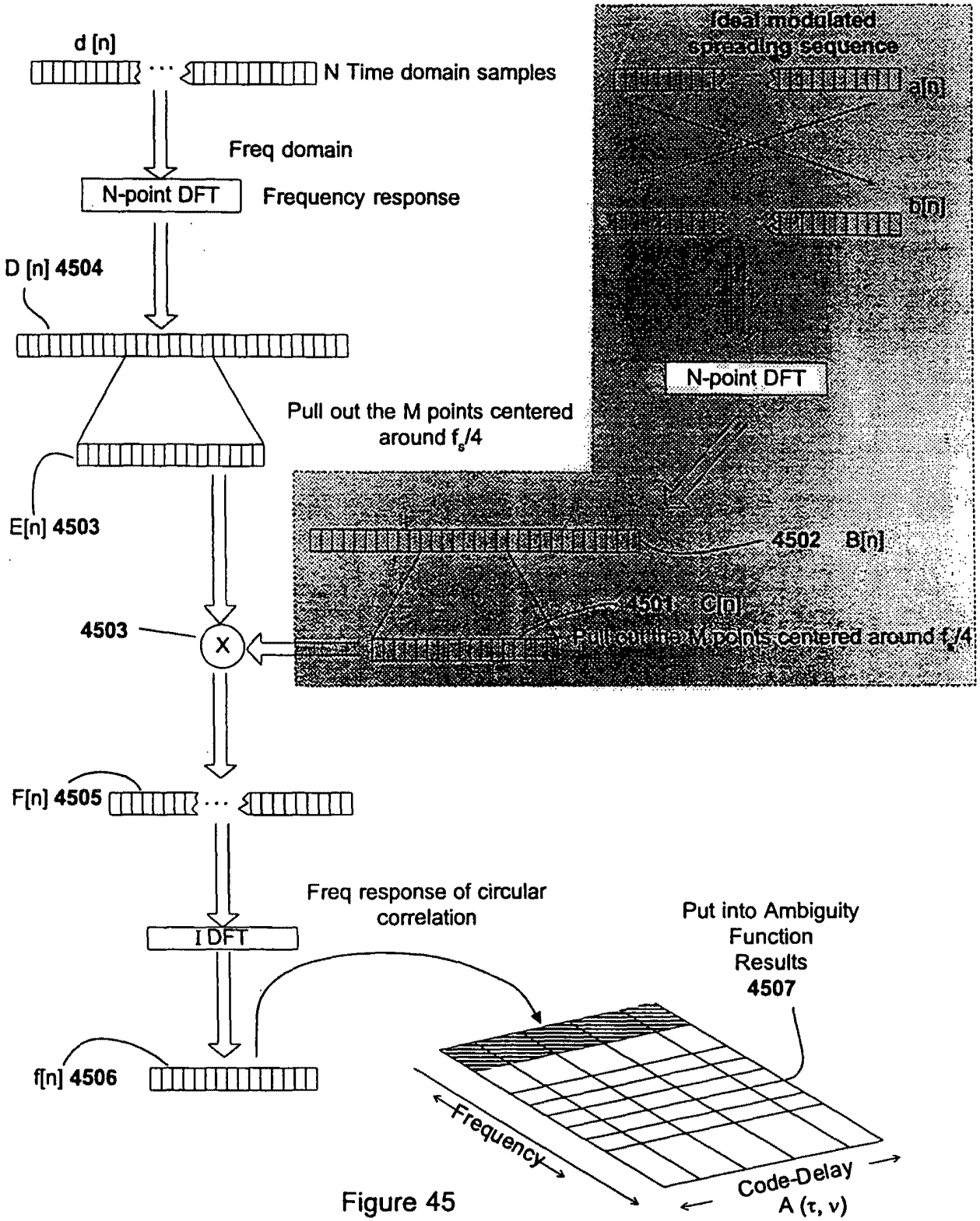

d [n]
N Time domain samples
Freq domain
N-point DFT
Frequency response
D [n] 4504
Pull out the M points centered around $f_s/4$
E[n] 4503
4503
X
F[n] 4505
I DFT
f[n] 4506
Freq response of circular correlation
Put into Ambiguity Function Results 4507
Frequency
Code-Delay
A (τ, ν)
Ideal modulated spreading sequence
a[n]
b[n]
N-point DFT
4502 B[n]
4501 C[n]
Pull out the M points centered around $f_s/4$

Figure 45

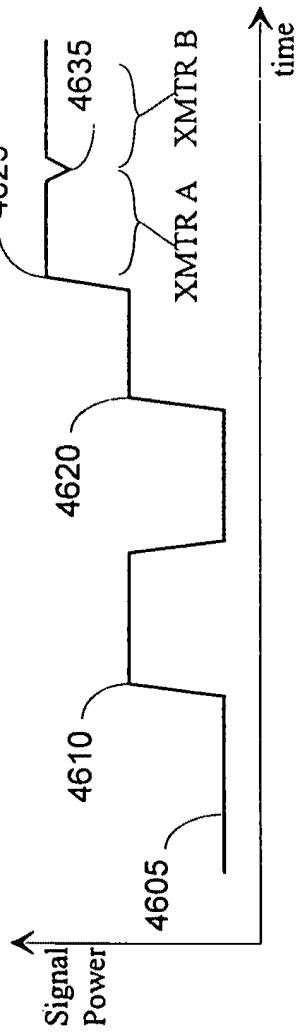
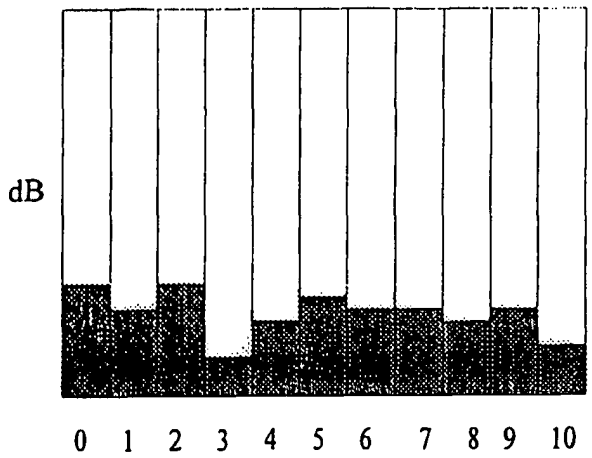


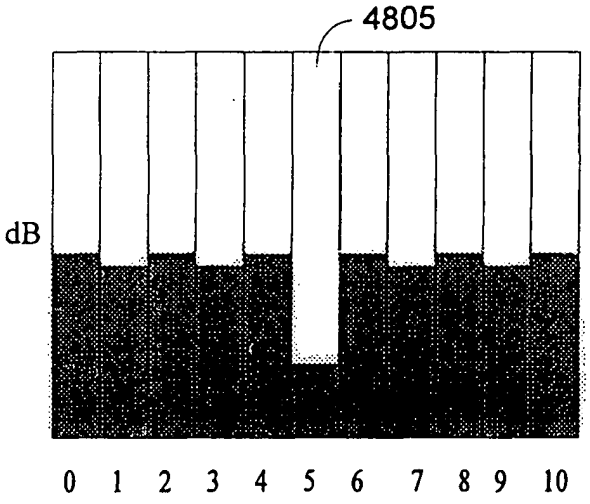
Figure 46

Figure 47



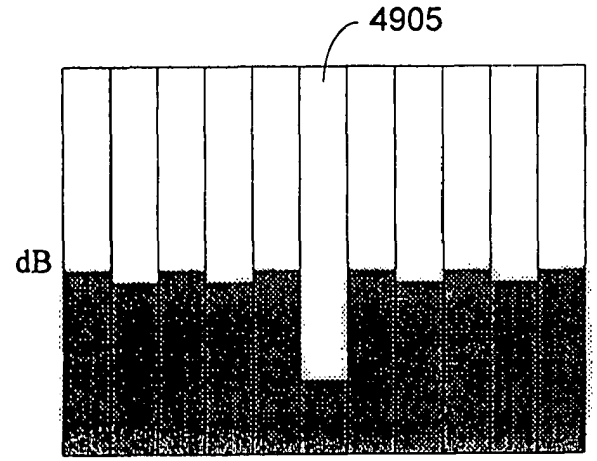
Frequency Bin vs. Signal Power
Ambient Noise

Figure 48



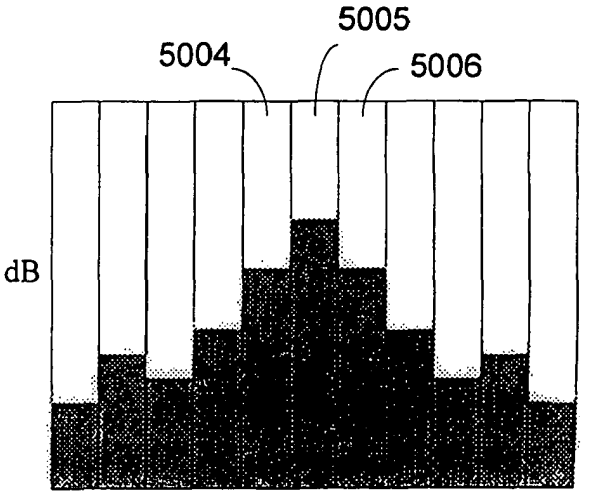
Frequency Bin vs. Signal Power
CW Jammer

Figure 49



Frequency Bin vs. Signal Power
Non - Correlated Spread Spectrum Signal

Figure 50



Frequency Bin vs. Signal Power
Correlated Spread Spectrum Signal

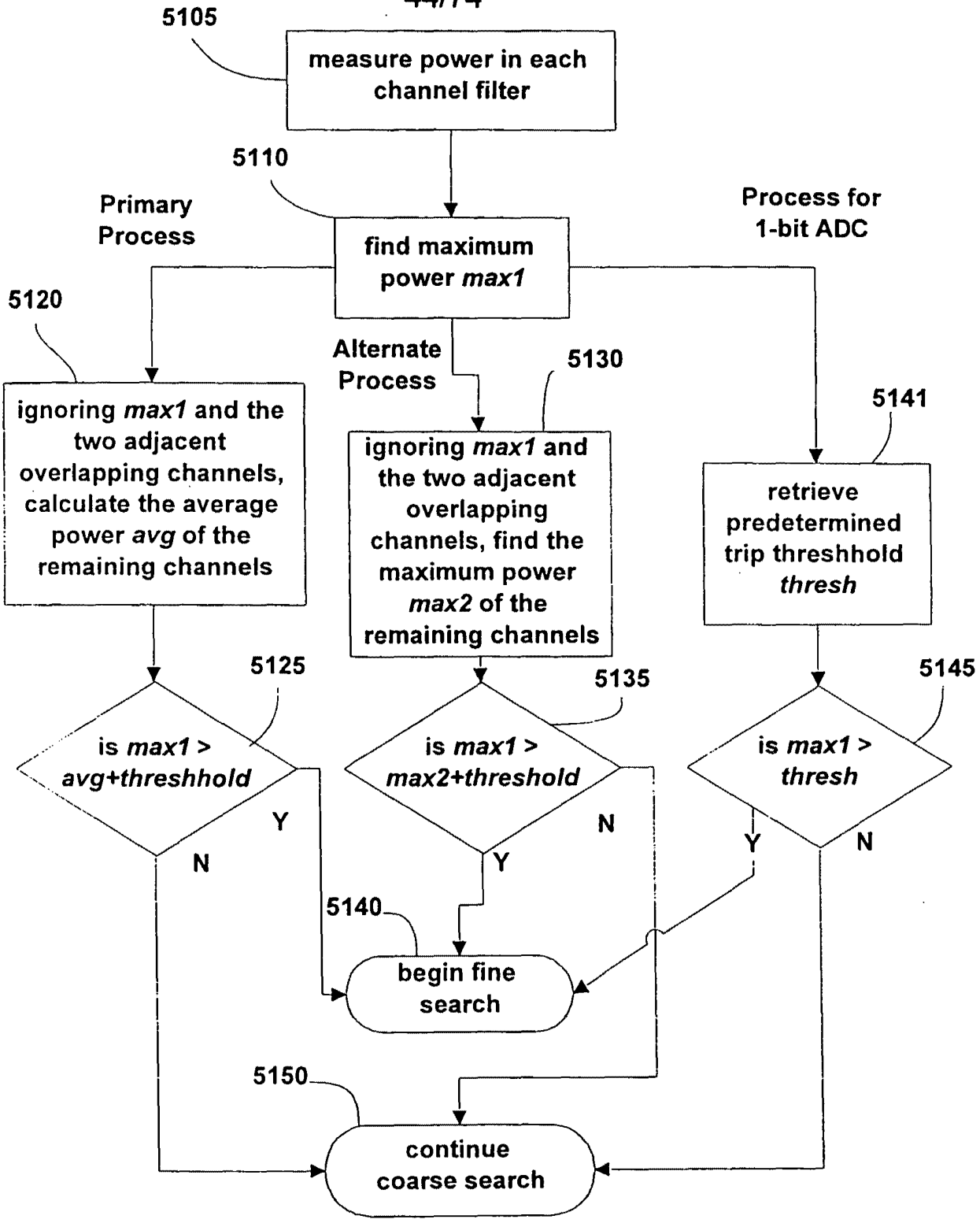

5105
measure power in each channel filter
5110
Primary Process
find maximum power max1
Process for 1-bit ADC
5120
Alternate Process
5130
5141
ignoring max1 and the two adjacent overlapping channels, calculate the average power avg of the remaining channels
ignoring max1 and the two adjacent overlapping channels, find the maximum power max2 of the remaining channels
retrieve predetermined trip threshhold thresh
5125
5135
5145
is max1 > avg+threshhold
is max1 > max2+threshold
is max1 > thresh
Y
N
N
Y
Y
N
5140
begin fine search
5150
continue coarse search

Figure 51

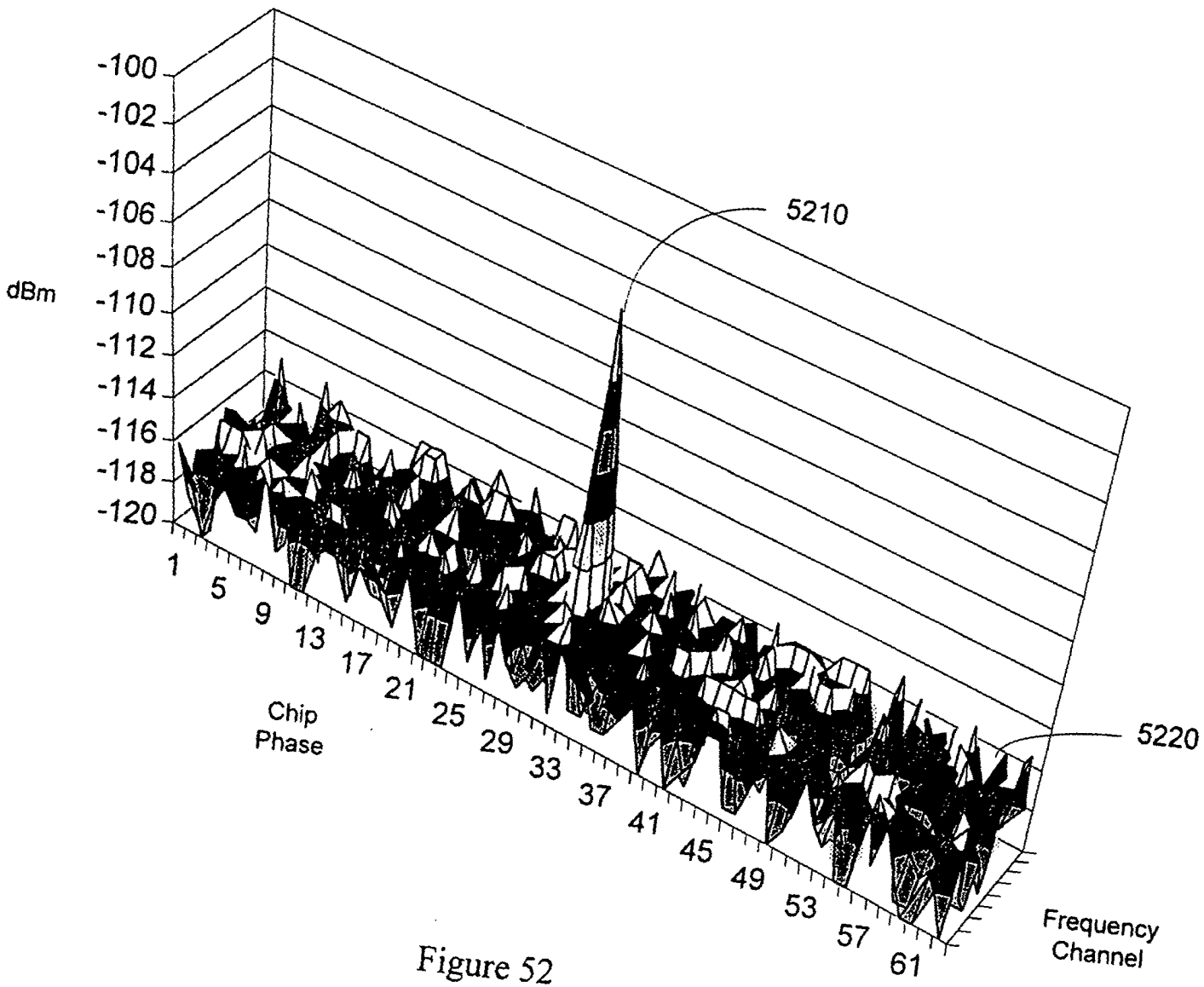

dBm
-100
-102
-104
-106
-108
-110
-112
-114
-116
-118
-120
5210
5220
1
5
9
13
17
21
25
29
33
37
41
45
49
53
57
61
Chip Phase
Frequency Channel

Figure 52

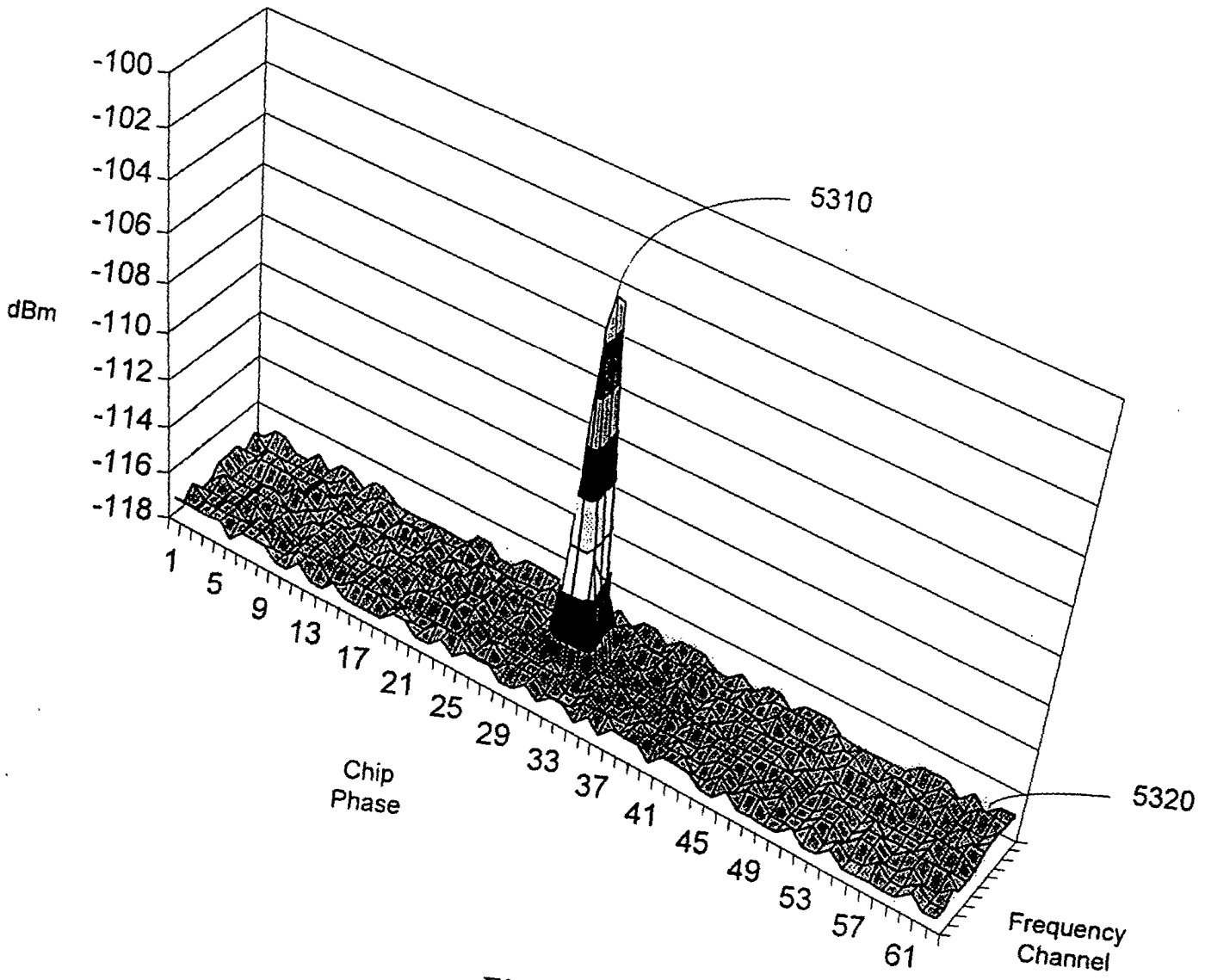

-100
-102
-104
-106
-108
-110
-112
-114
-116
-118
dBm
5310
5320
1
5
9
13
17
21
25
29
33
37
41
45
49
53
57
61
Chip Phase
Frequency Channel

Figure 53

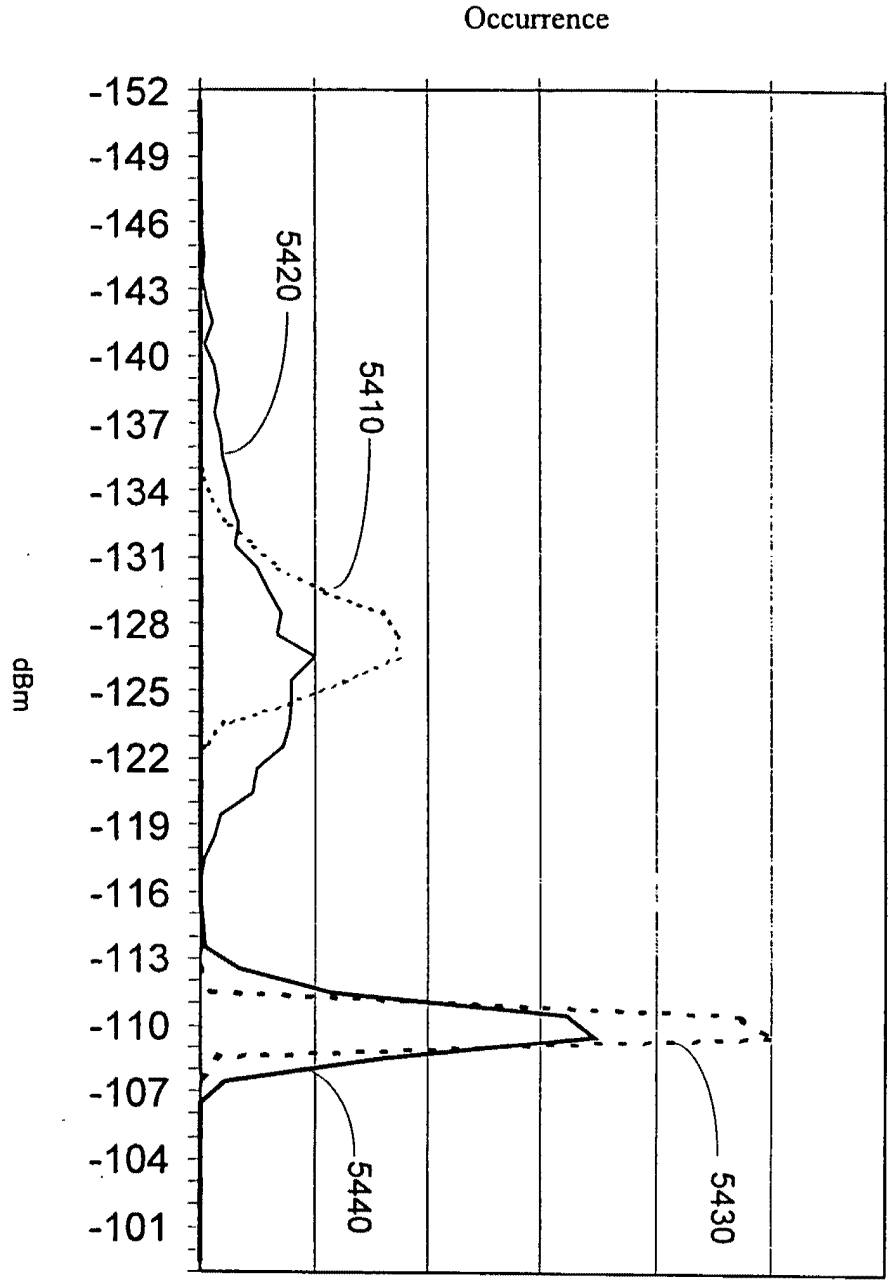

Occurrence
-152
-149
-146
-143
-140
-137
-134
-131
-128
-125
-122
-119
-116
-113
-110
-107
-104
-101
dBm
5420
5410
5440
5430

Figure 54

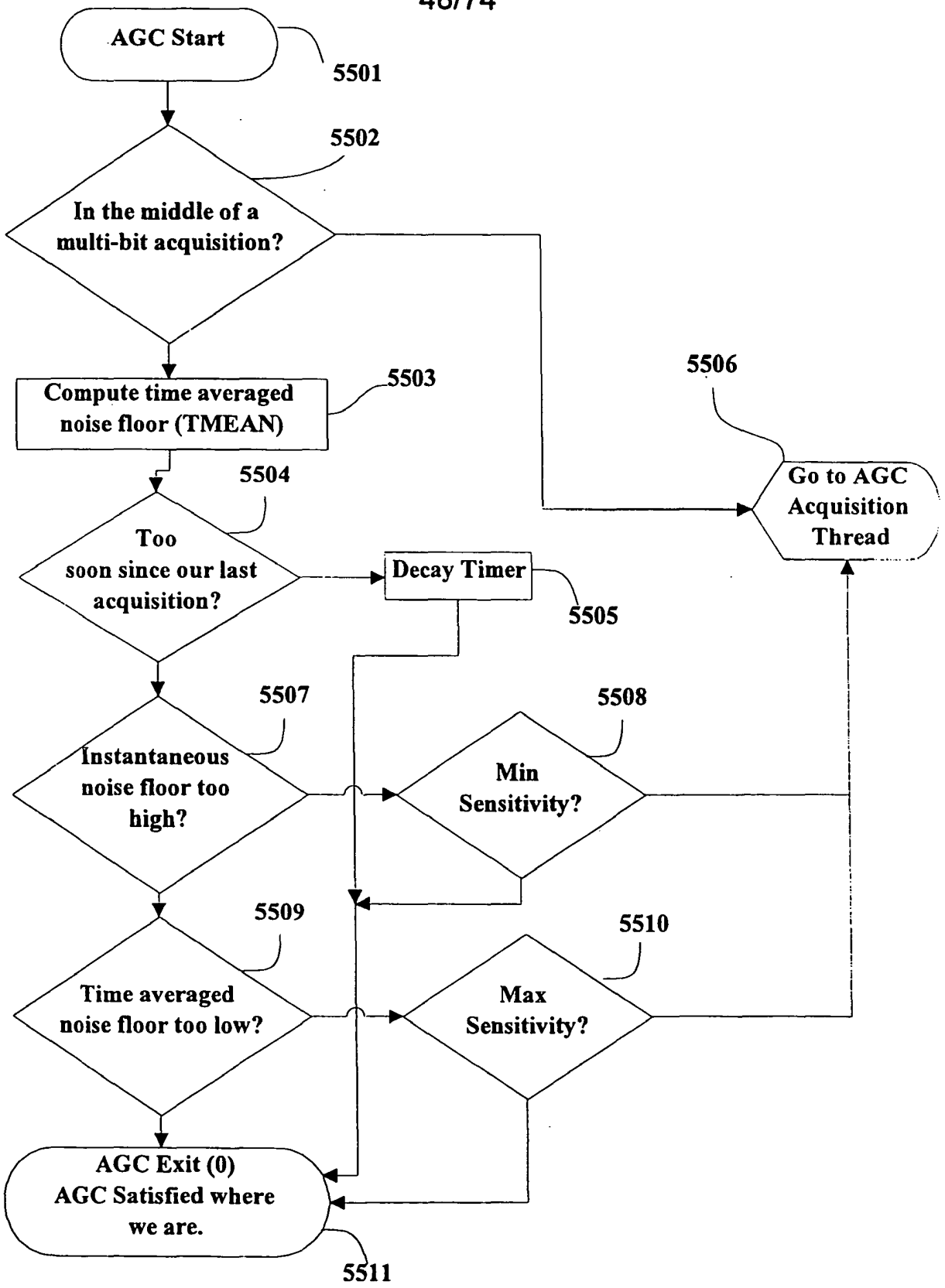

AGC Start
5501
5502
In the middle of a multi-bit acquisition?
5503
Compute time averaged noise floor (TMEAN)
5504
Too soon since our last acquisition?
Decay Timer
5505
5506
Go to AGC Acquisition Thread
5507
Instantaneous noise floor too high?
5508
Min Sensitivity?
5509
Time averaged noise floor too low?
5510
Max Sensitivity?
AGC Exit (0) AGC Satisfied where we are.
5511

Figure 55

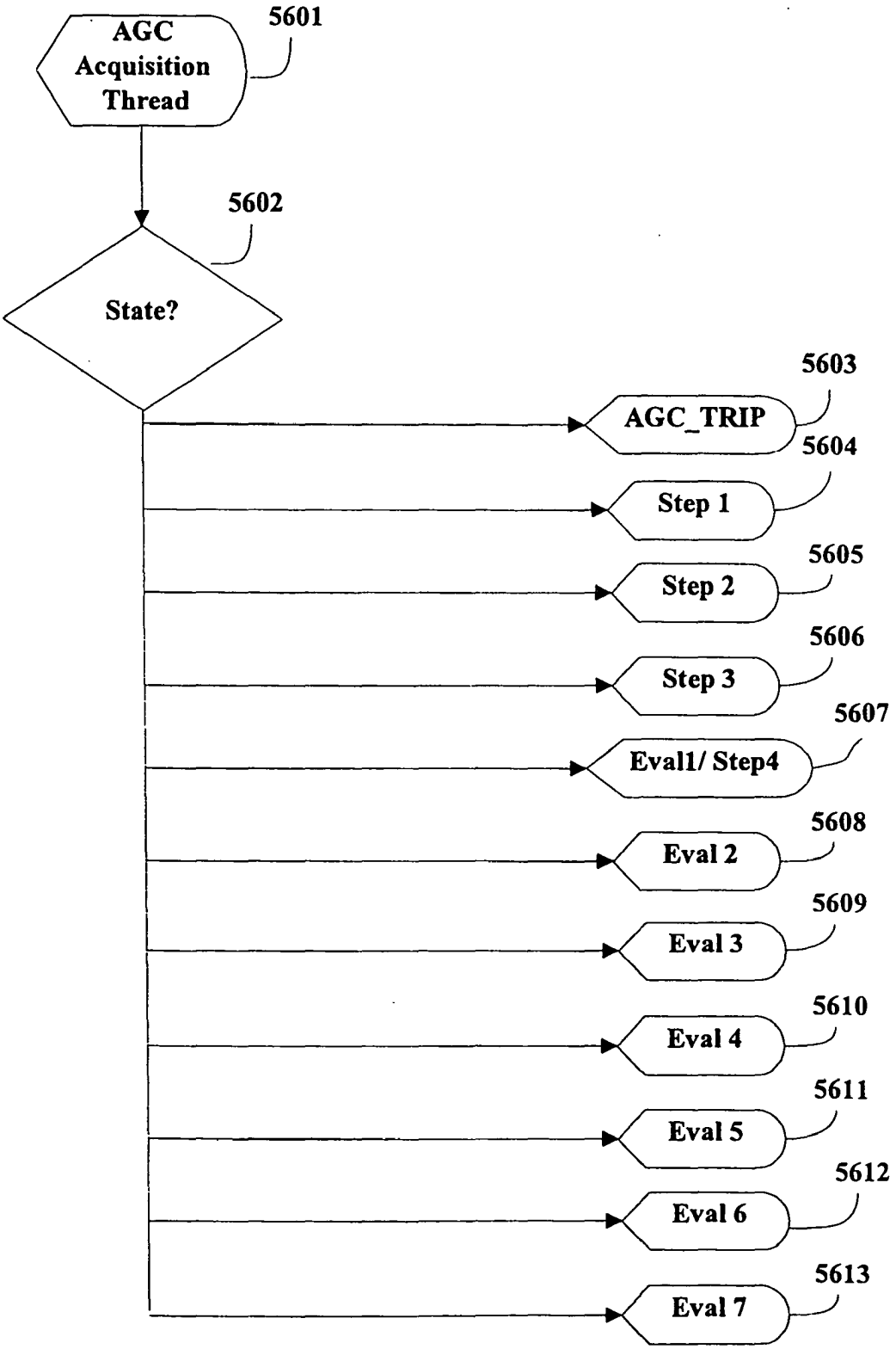

AGC Acquisition Thread
5601
5602
State?
5603
AGC_TRIP
5604
Step 1
5605
Step 2
5606
Step 3
5607
Eval1/ Step4
5608
Eval 2
5609
Eval 3
5610
Eval 4
5611
Eval 5
5612
Eval 6
5613
Eval 7

Figure 56

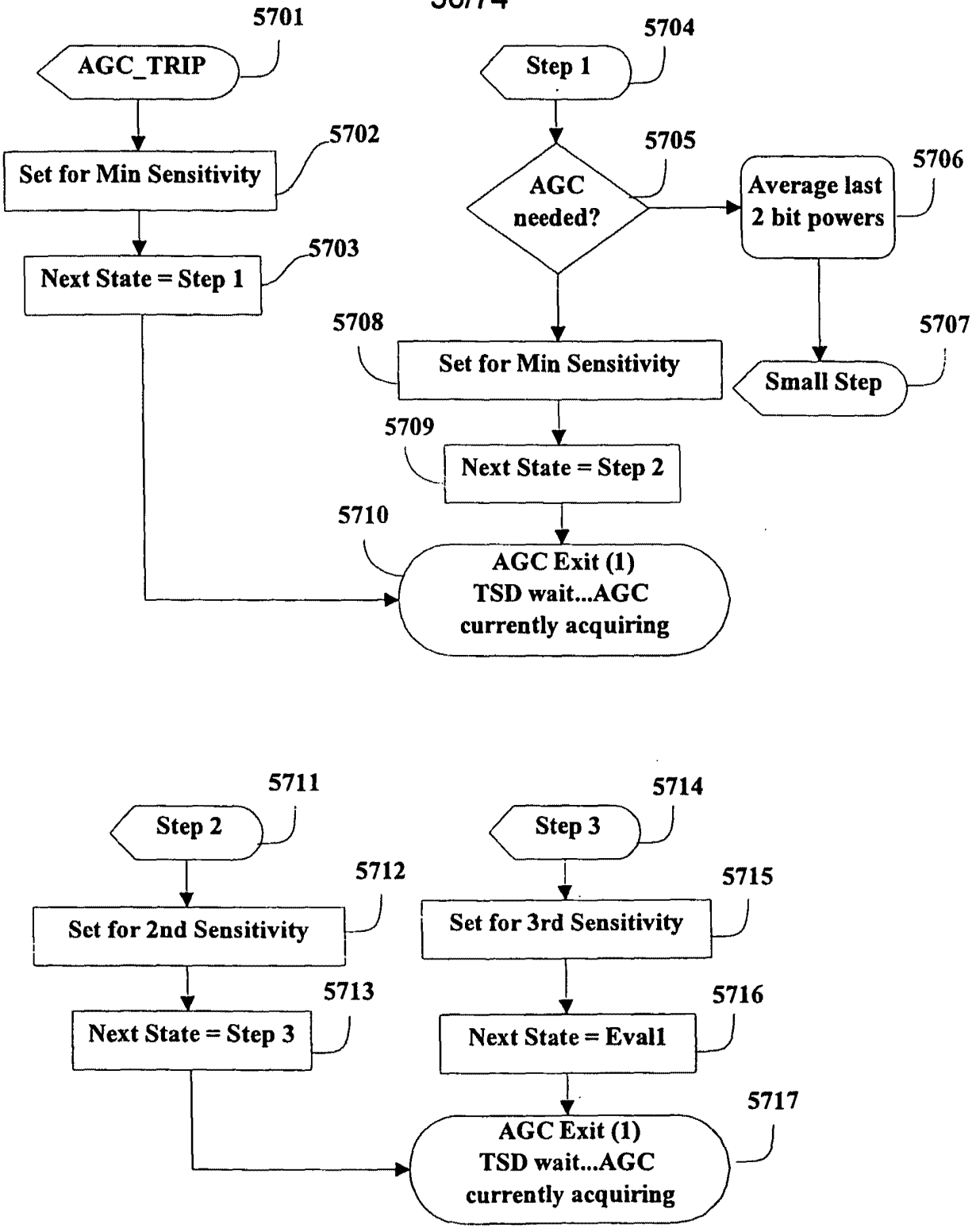

5701
AGC_TRIP
5702
Set for Min Sensitivity
5703
Next State = Step 1
5704
Step 1
5705
AGC needed?
5706
Average last 2 bit powers
5707
Small Step
5708
Set for Min Sensitivity
5709
Next State = Step 2
5710
AGC Exit (1) TSD wait...AGC currently acquiring
5711
Step 2
5712
Set for 2nd Sensitivity
5713
Next State = Step 3
5714
Step 3
5715
Set for 3rd Sensitivity
5716
Next State = Eval1
5717
AGC Exit (1) TSD wait...AGC currently acquiring

Figure 57

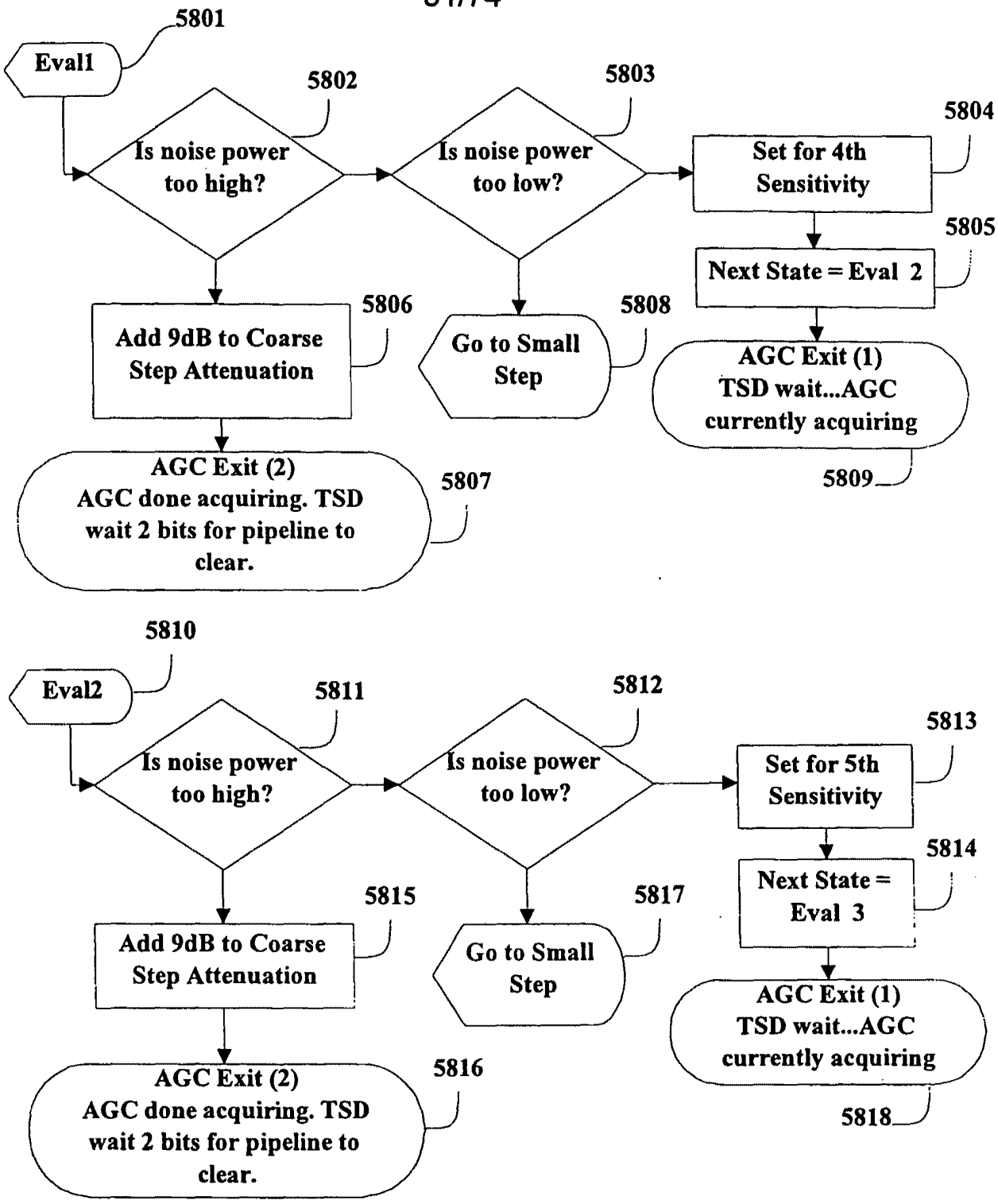

5801
Eval1
5802
Is noise power too high?
5803
Is noise power too low?
5804
Set for 4th Sensitivity
5805
Next State = Eval 2
5806
Add 9dB to Coarse Step Attenuation
5808
Go to Small Step
AGC Exit (1) TSD wait...AGC currently acquiring
5809
AGC Exit (2) AGC done acquiring. TSD wait 2 bits for pipeline to clear.
5807
5810
Eval2
5811
Is noise power too high?
5812
Is noise power too low?
5813
Set for 5th Sensitivity
5814
Next State = Eval 3
5815
Add 9dB to Coarse Step Attenuation
5817
Go to Small Step
AGC Exit (1) TSD wait...AGC currently acquiring
5818
AGC Exit (2) AGC done acquiring. TSD wait 2 bits for pipeline to clear.
5816

Figure 58

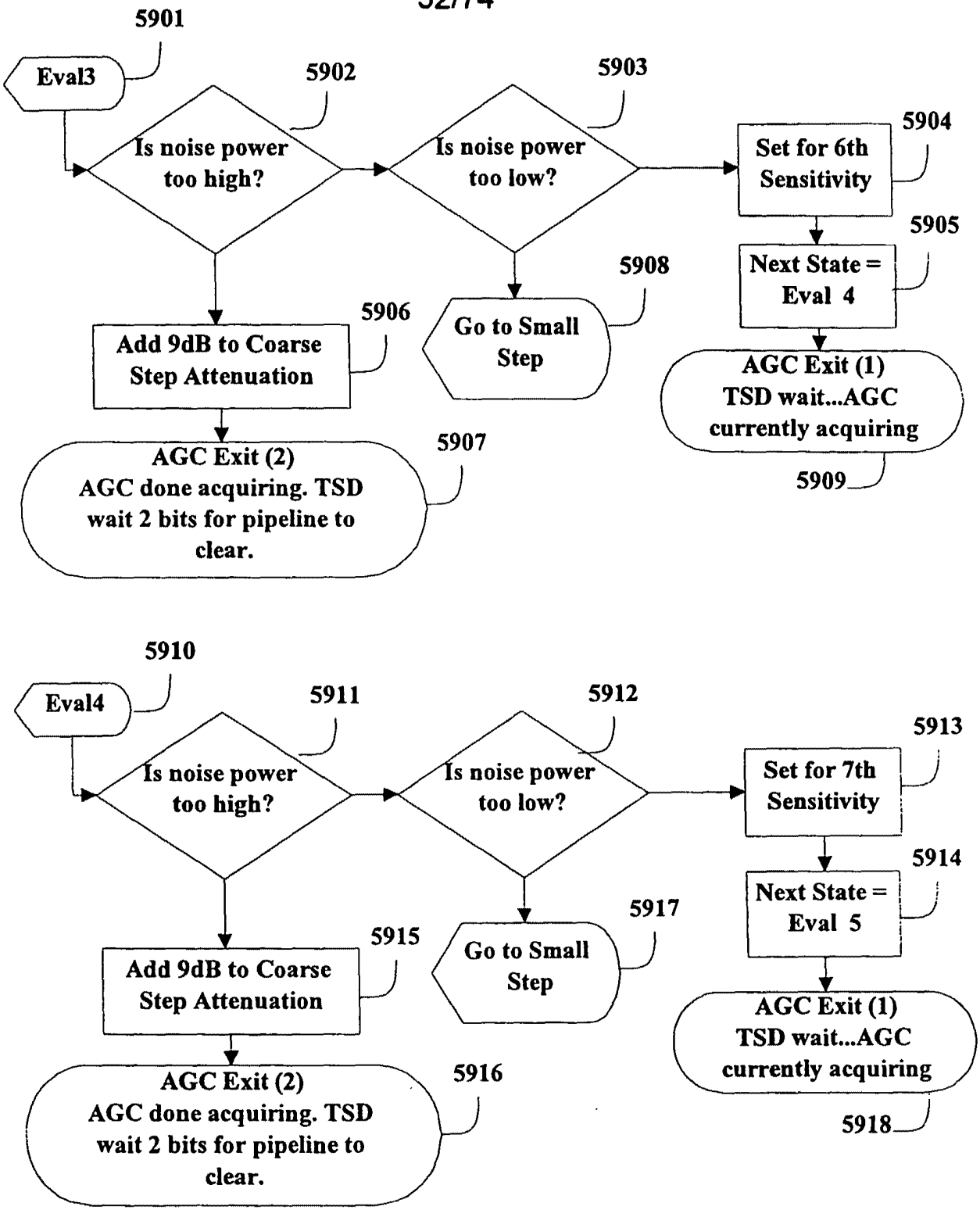
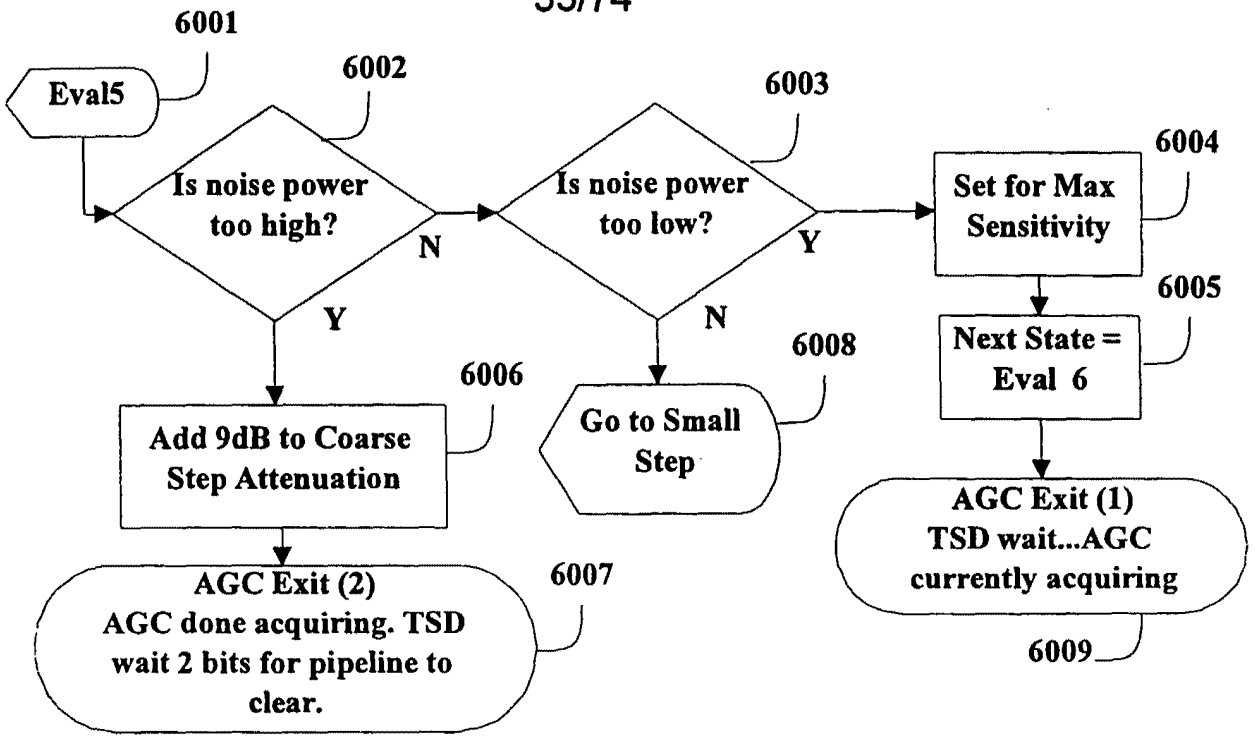

5901
Eval3
5902
Is noise power too high?
5903
Is noise power too low?
5904
Set for 6th Sensitivity
5905
Next State = Eval 4
5906
Add 9dB to Coarse Step Attenuation
5907
AGC Exit (2) AGC done acquiring. TSD wait 2 bits for pipeline to clear.
5908
Go to Small Step
AGC Exit (1) TSD wait...AGC currently acquiring
5909
5910
Eval4
5911
Is noise power too high?
5912
Is noise power too low?
5913
Set for 7th Sensitivity
5914
Next State = Eval 5
5915
Add 9dB to Coarse Step Attenuation
5916
AGC Exit (2) AGC done acquiring. TSD wait 2 bits for pipeline to clear.
5917
Go to Small Step
AGC Exit (1) TSD wait...AGC currently acquiring
5918

Figure 59


6001
Eval5
6002
Is noise power too high?
N
Y
6003
Is noise power too low?
Y
N
6004
Set for Max Sensitivity
6005
Next State = Eval 6
6006
Add 9dB to Coarse Step Attenuation
6008
Go to Small Step
AGC Exit (1) TSD wait...AGC currently acquiring
6009
AGC Exit (2) AGC done acquiring. TSD wait 2 bits for pipeline to clear.
6007

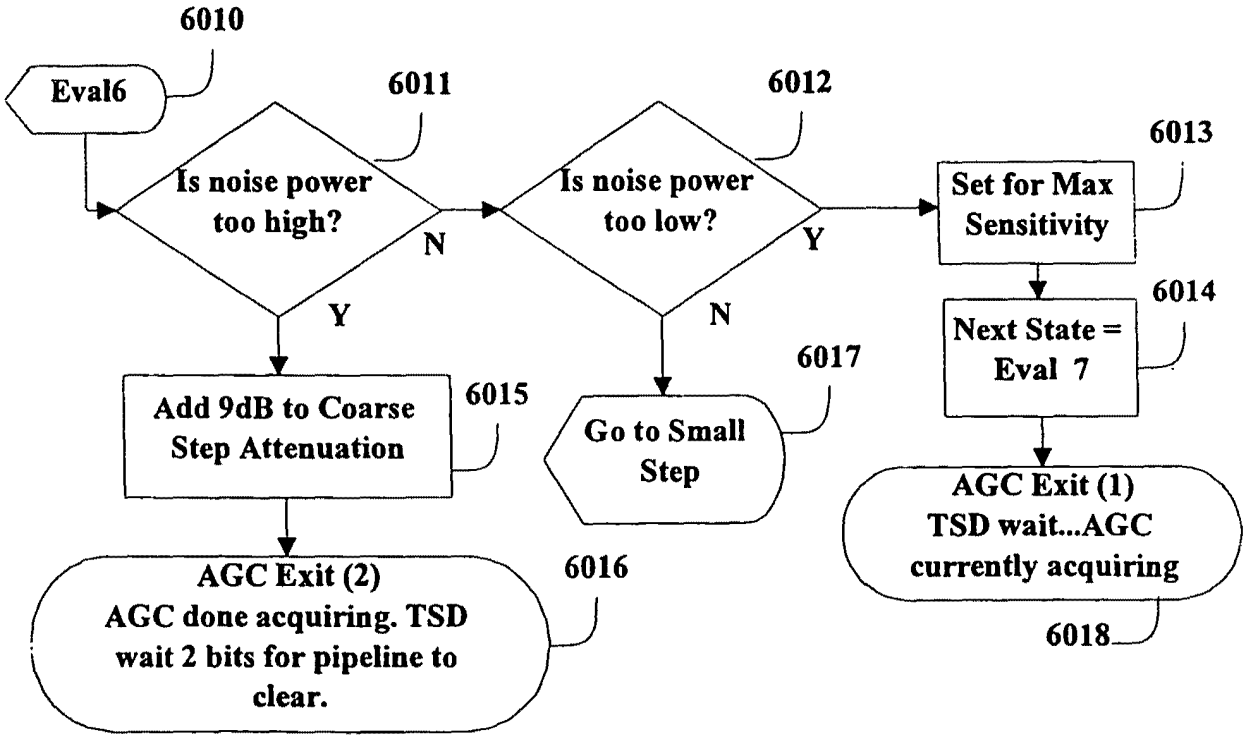

6010
Eval6
6011
Is noise power too high?
N
Y
6012
Is noise power too low?
Y
N
6013
Set for Max Sensitivity
6014
Next State = Eval 7
6015
Add 9dB to Coarse Step Attenuation
6017
Go to Small Step
AGC Exit (1) TSD wait...AGC currently acquiring
6018
AGC Exit (2) AGC done acquiring. TSD wait 2 bits for pipeline to clear.
6016

Figure 60

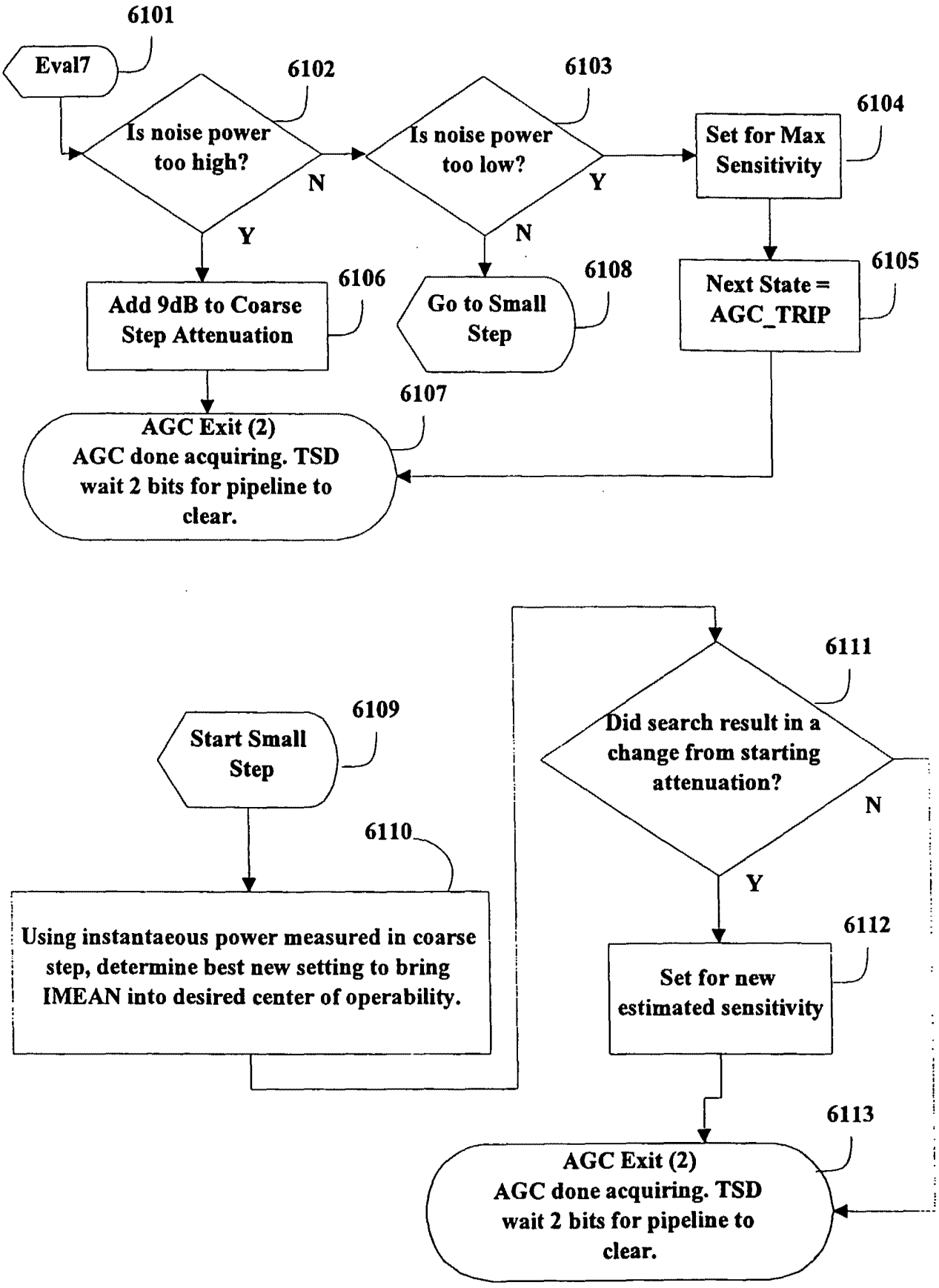

6101
Eval7
6102
Is noise power too high?
N
Y
6103
Is noise power too low?
Y
N
6104
Set for Max Sensitivity
6105
Next State = AGC_TRIP
6106
Add 9dB to Coarse Step Attenuation
6108
Go to Small Step
6107
AGC Exit (2)
AGC done acquiring. TSD wait 2 bits for pipeline to clear.
6109
Start Small Step
6110
Using instantaeous power measured in coarse step, determine best new setting to bring IMEAN into desired center of operability.
6111
Did search result in a change from starting attenuation?
N
Y
6112
Set for new estimated sensitivity
6113
AGC Exit (2)
AGC done acquiring. TSD wait 2 bits for pipeline to clear.

Figure 61

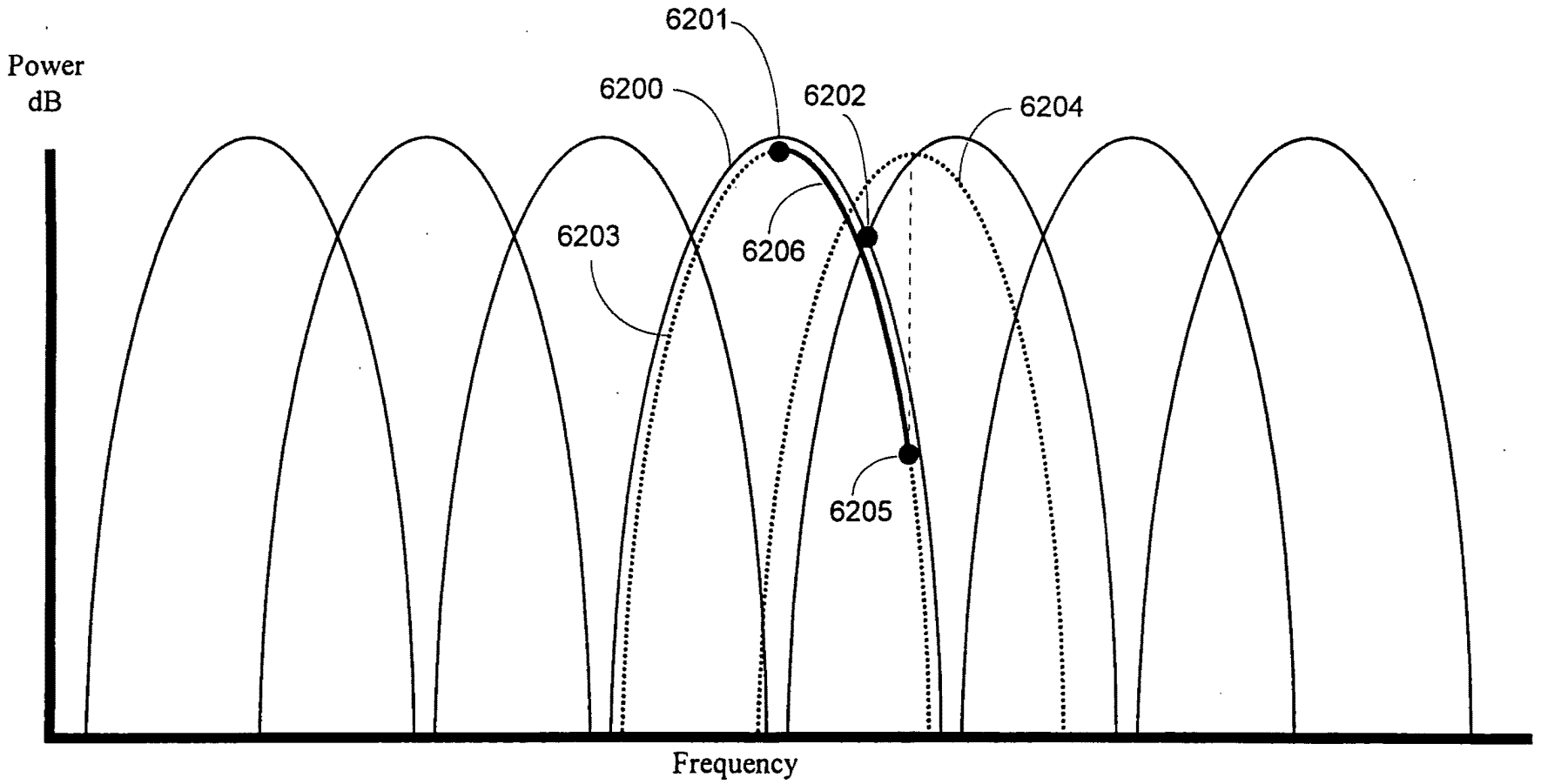


Figure 62

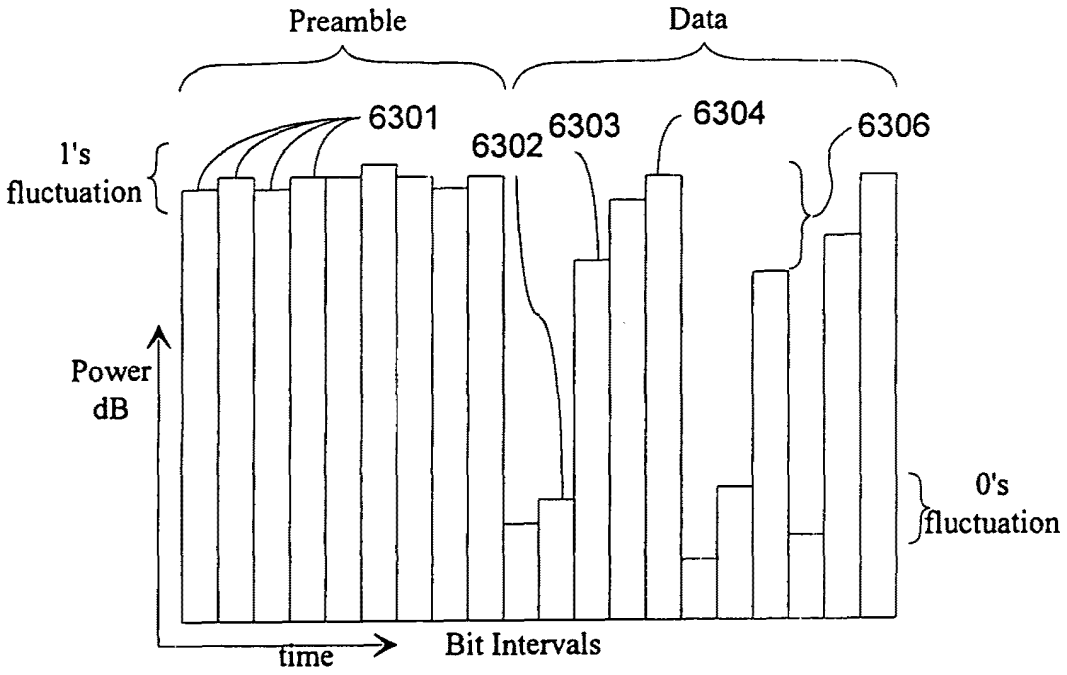

Preamble
Data
6301
6302
6303
6304
6306
1's
fluctuation
Power
dB
0's
fluctuation
time
Bit Intervals

Figure 63

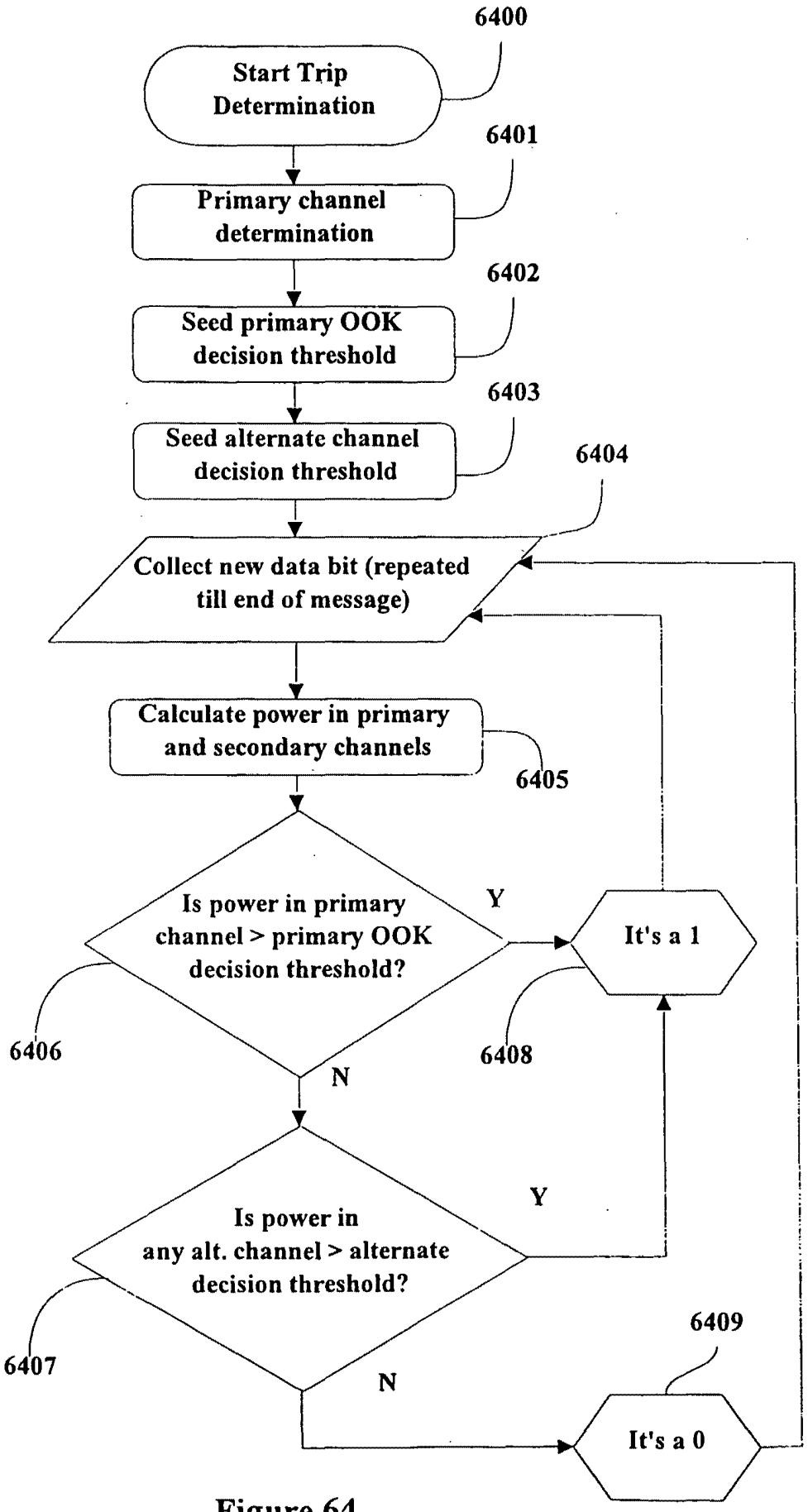

6400
Start Trip Determination
6401
Primary channel determination
6402
Seed primary OOK decision threshold
6403
Seed alternate channel decision threshold
6404
Collect new data bit (repeated till end of message)
Calculate power in primary and secondary channels
6405
Is power in primary channel > primary OOK decision threshold?
Y
It's a 1
6406
6408
N
Is power in any alt. channel > alternate decision threshold?
Y
6407
6409
N
It's a 0

Figure 64

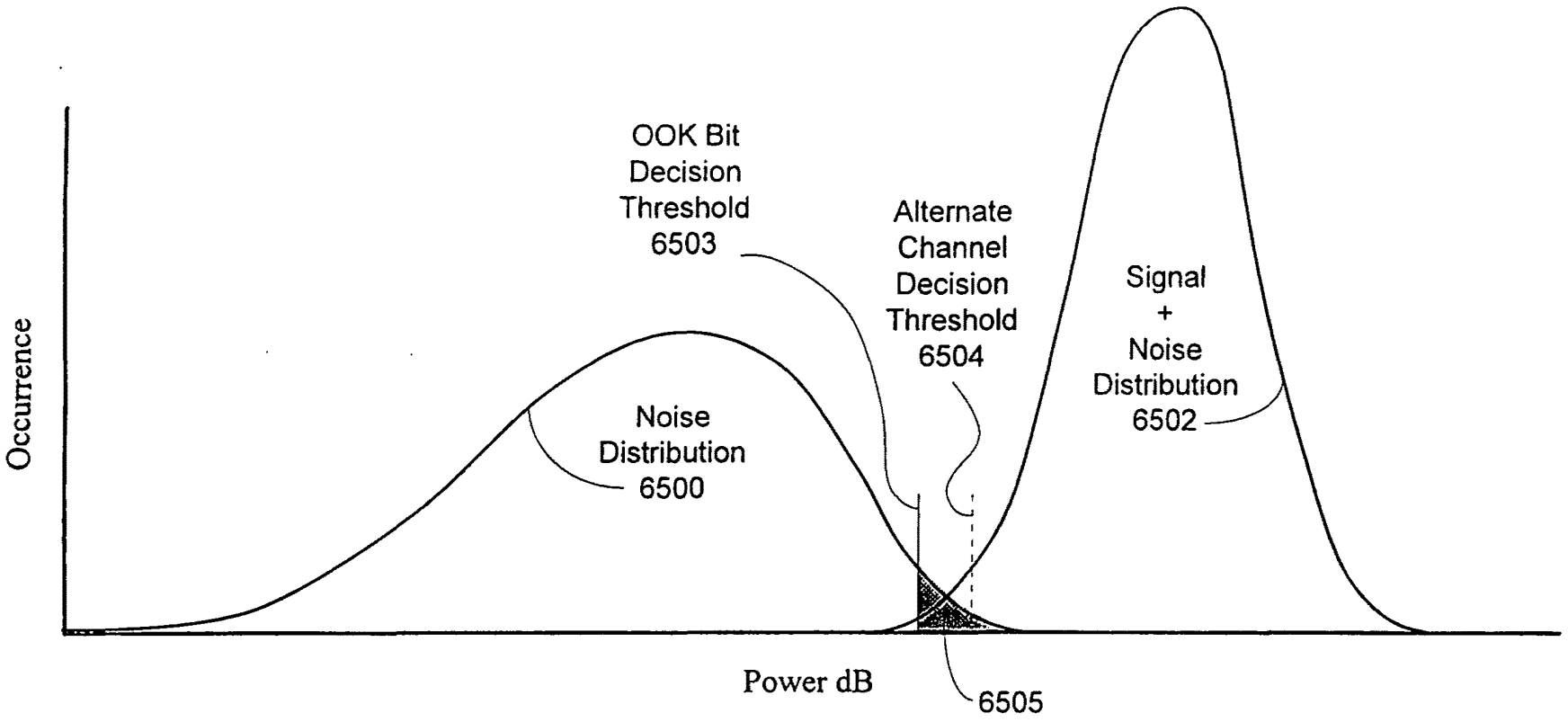

OOK Bit
Decision
Threshold
6503
Alternate
Channel
Decision
Threshold
6504
Signal
+
Noise
Distribution
6502
Noise
Distribution
6500
Occurrence
Power dB
6505

Figure 65

Figure 66A

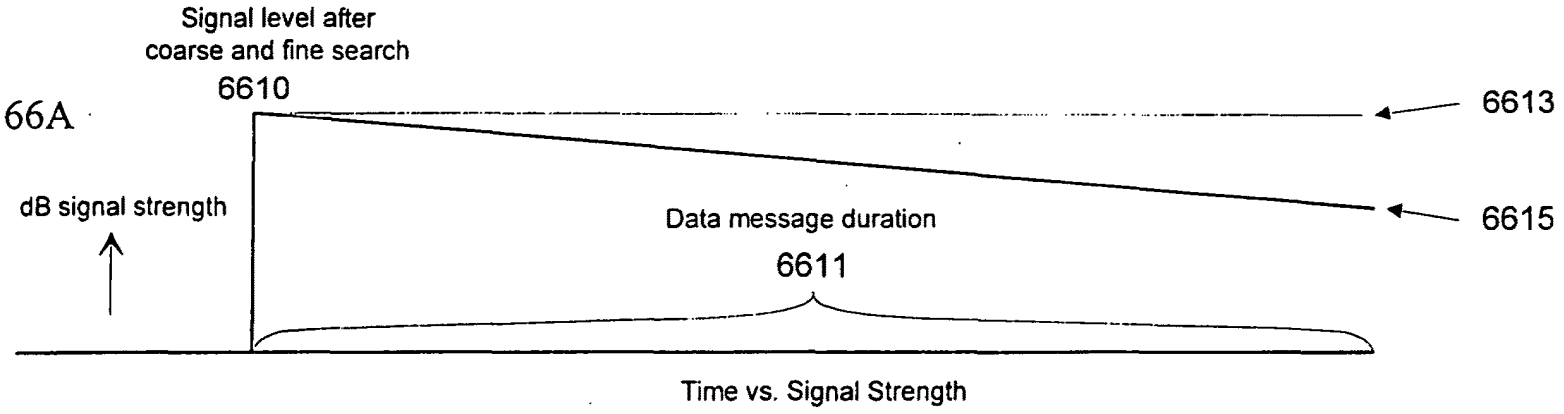


Figure 66B

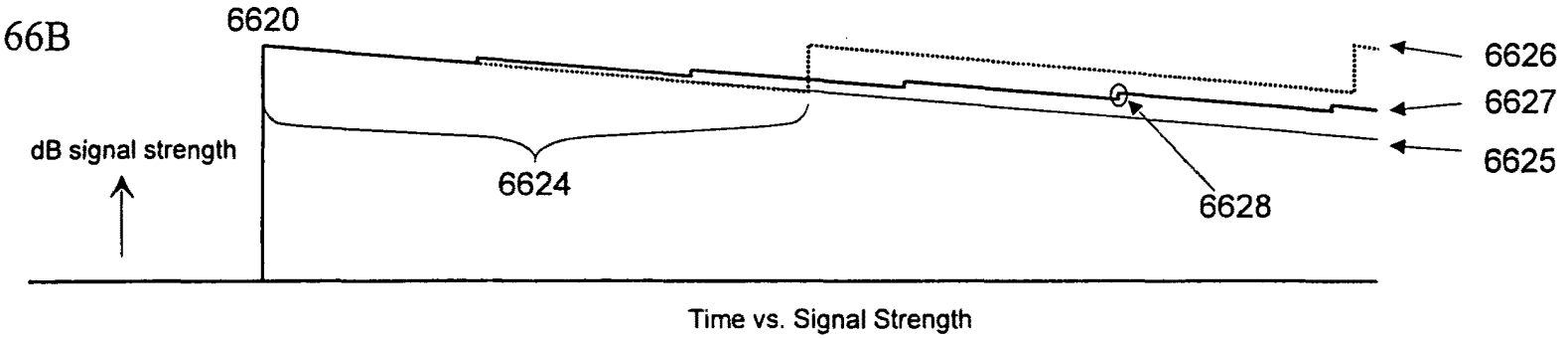
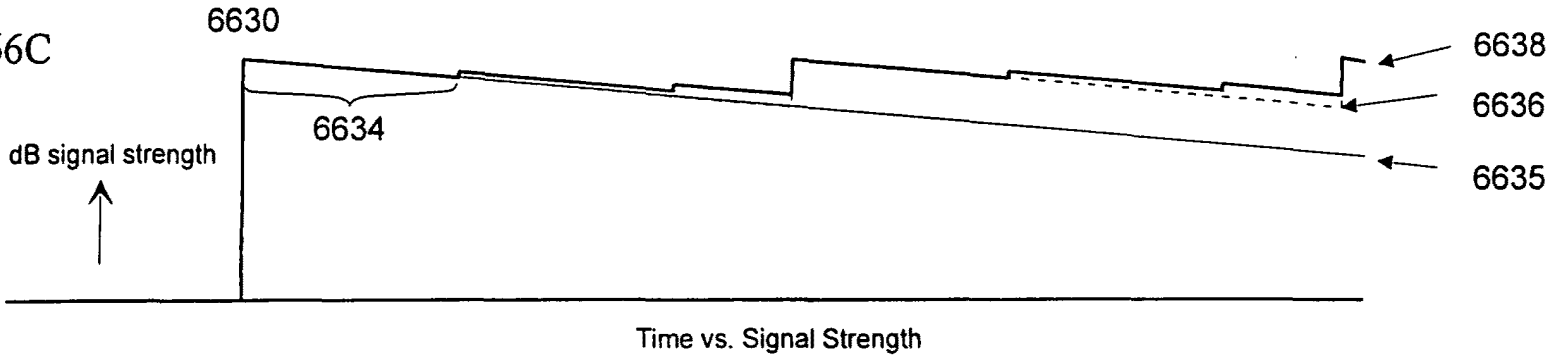


Figure 66C



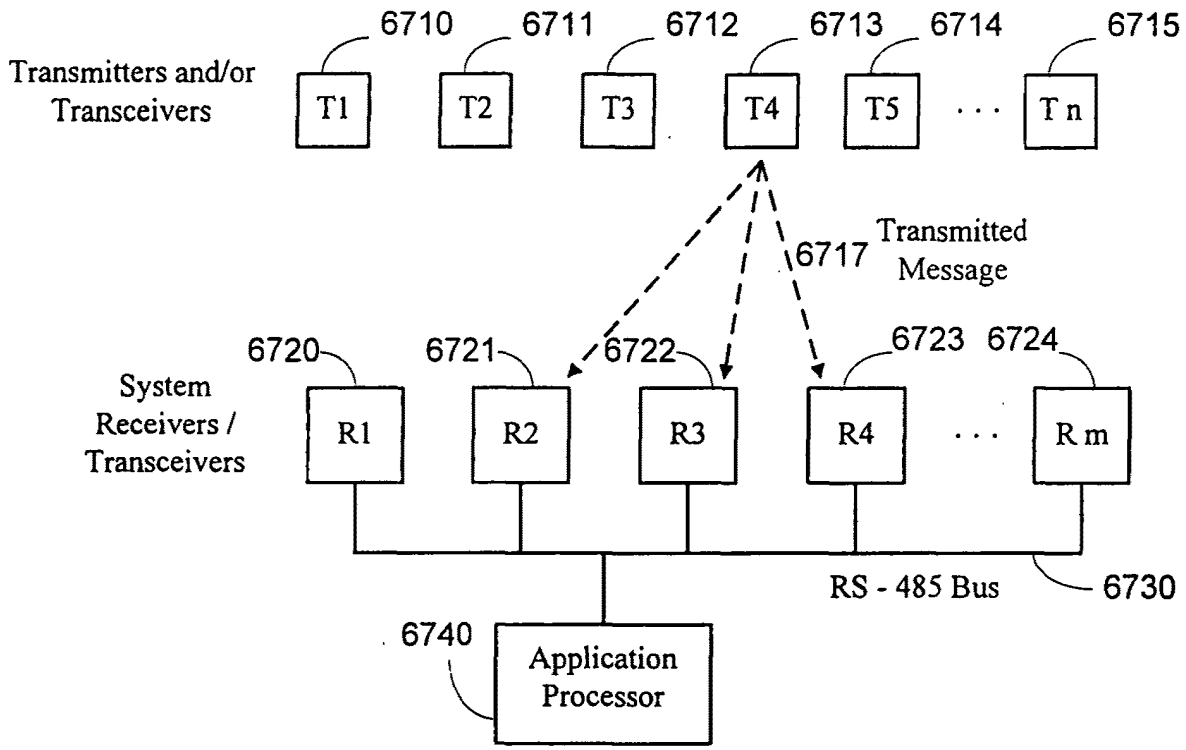

6710
6711
6712
6713
6714
6715
Transmitters and/or Transceivers
T1
T2
T3
T4
T5
T n
6717
Transmitted Message
6720
6721
6722
6723
6724
System Receivers / Transceivers
R1
R2
R3
R4
R m
RS - 485 Bus
6730
6740
Application Processor

Figure 67

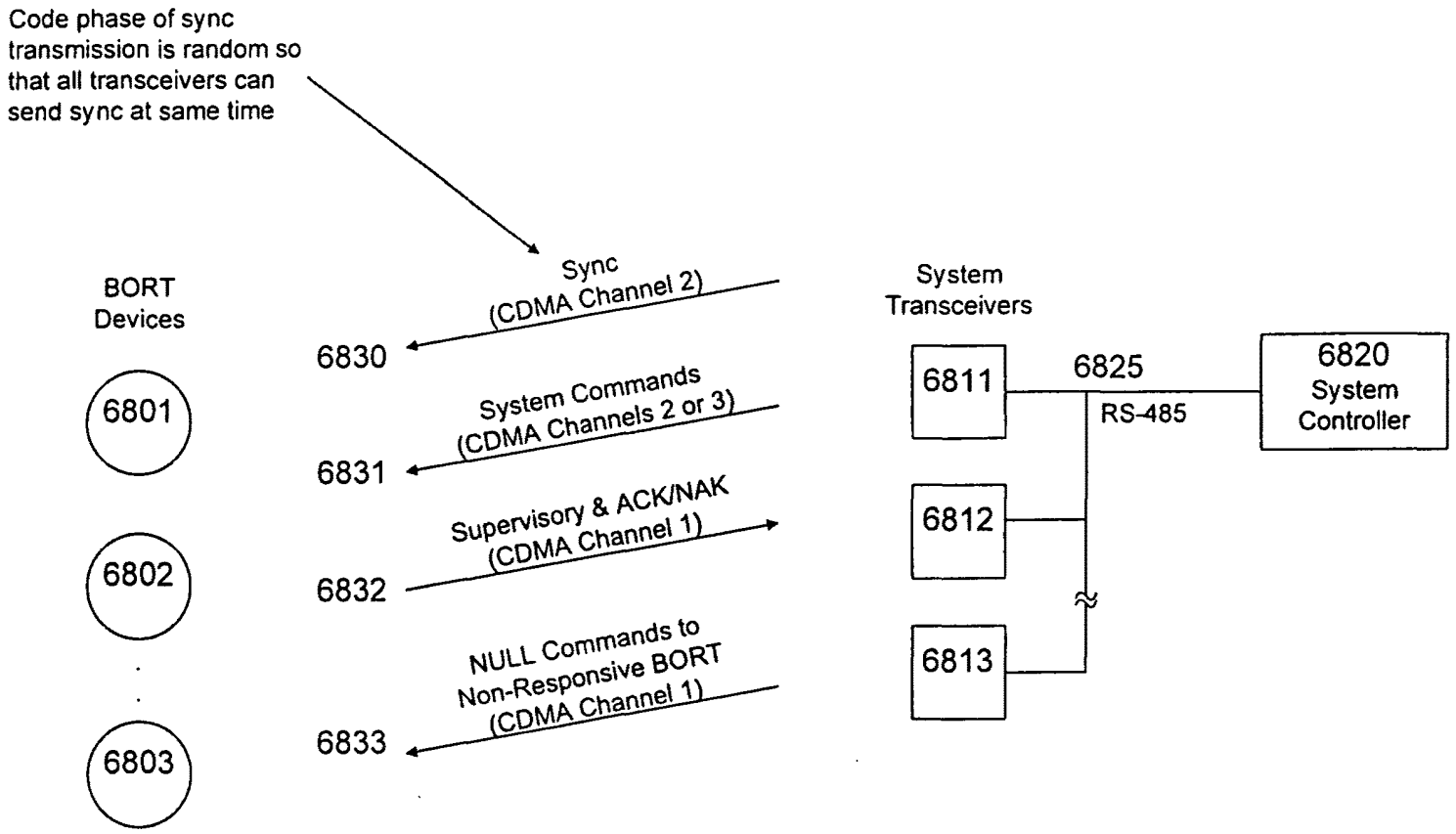

Code phase of sync transmission is random so that all transceivers can send sync at same time
BORT Devices
6801
6802
6803
Sync (CDMA Channel 2)
6830
System Commands (CDMA Channels 2 or 3)
6831
Supervisory & ACK/NAK (CDMA Channel 1)
6832
NULL Commands to Non-Responsive BORT (CDMA Channel 1)
6833
System Transceivers
6811
6812
6813
6825
RS-485
6820
System Controller

Figure 68

Figure 69A

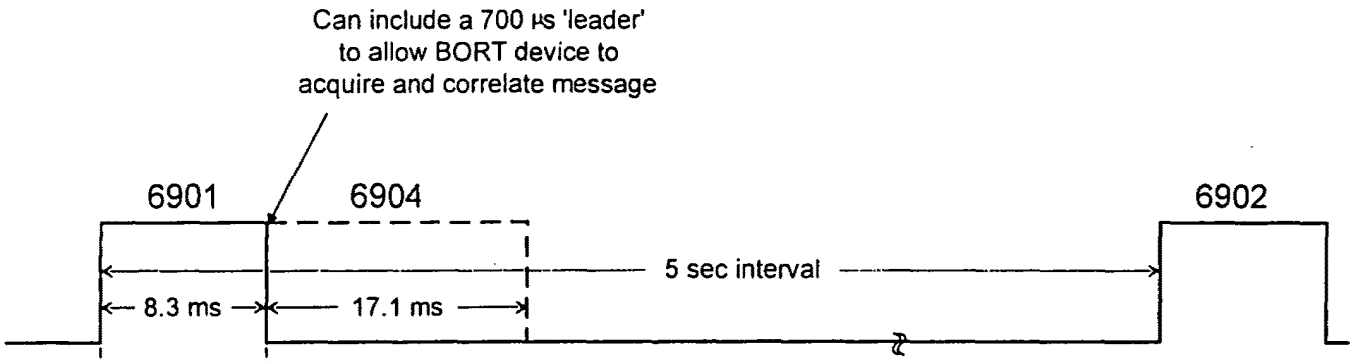
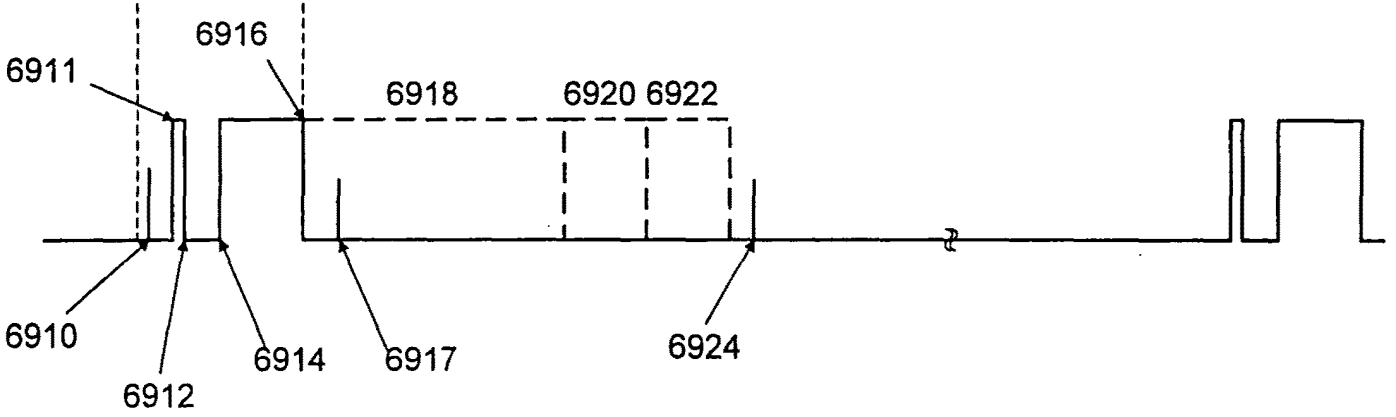


Figure 69B



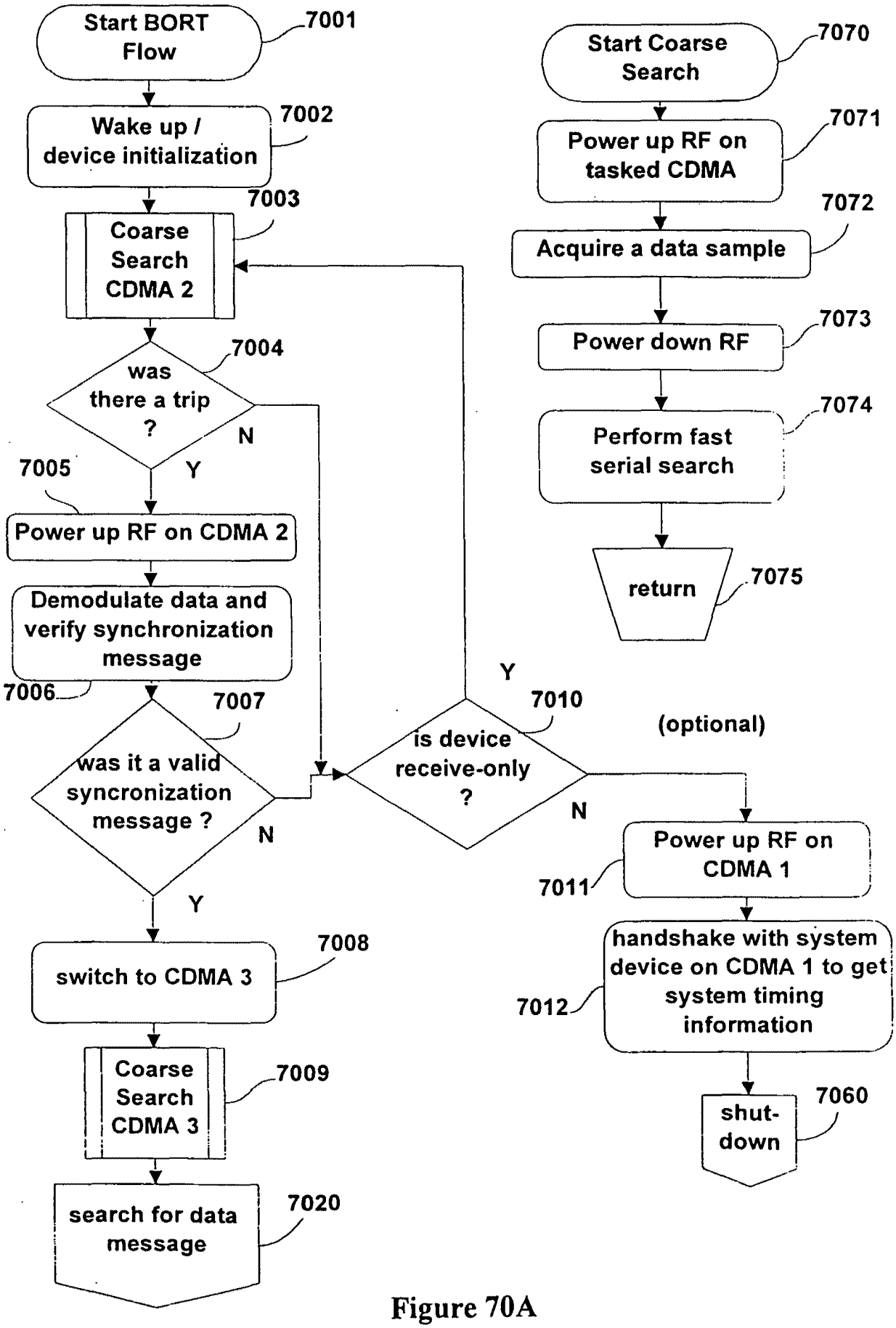

Start BORT Flow
7001
Wake up / device initialization
7002
Coarse Search CDMA 2
7003
was there a trip ?
7004
N
Y
7005
Power up RF on CDMA 2
Demodulate data and verify synchronization message
7006
was it a valid syncronization message ?
7007
N
Y
switch to CDMA 3
7008
Coarse Search CDMA 3
7009
search for data message
7020
Start Coarse Search
7070
Power up RF on tasked CDMA
7071
Acquire a data sample
7072
Power down RF
7073
Perform fast serial search
7074
return
7075
Y
is device receive-only ?
7010
(optional)
N
Power up RF on CDMA 1
7011
handshake with system device on CDMA 1 to get system timing information
7012
shut-down
7060

Figure 70A

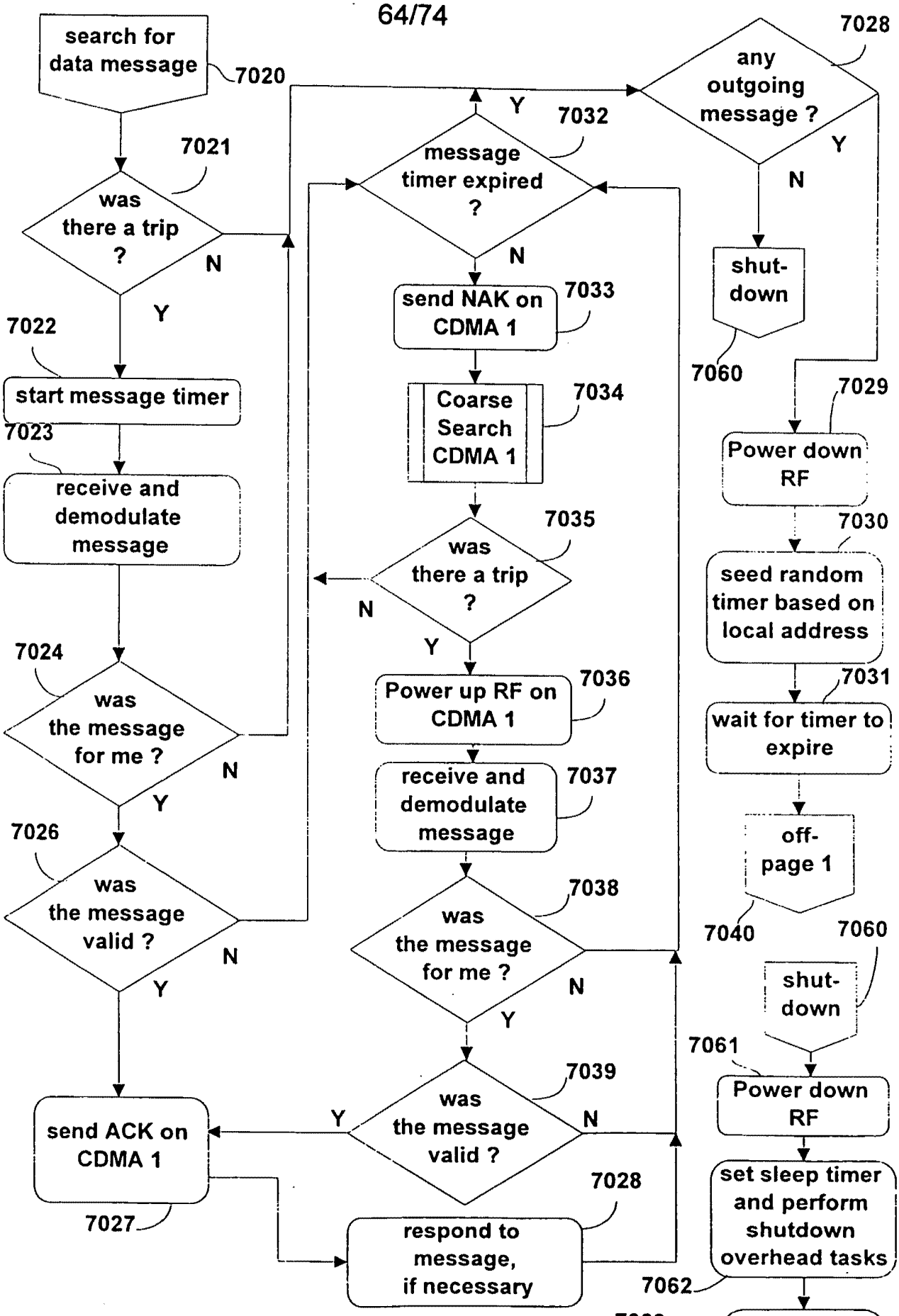

search for data message
7020
7021
was there a trip ?
N
Y
7022
start message timer
7023
receive and demodulate message
7024
was the message for me ?
N
Y
7026
was the message valid ?
N
Y
send ACK on CDMA 1
7027
7028
respond to message, if necessary
7032
message timer expired ?
Y
N
send NAK on CDMA 1
7033
Coarse Search CDMA 1
7034
7035
was there a trip ?
N
Y
Power up RF on CDMA 1
7036
receive and demodulate message
7037
7038
was the message for me ?
N
Y
7039
was the message valid ?
Y
N
7028
any outgoing message ?
Y
N
shut-down
7060
7029
Power down RF
7030
seed random timer based on local address
7031
wait for timer to expire
off-page 1
7040
7060
shut-down
7061
Power down RF
set sleep timer and perform shutdown overhead tasks
7062
7063
sleep

Figure 70B

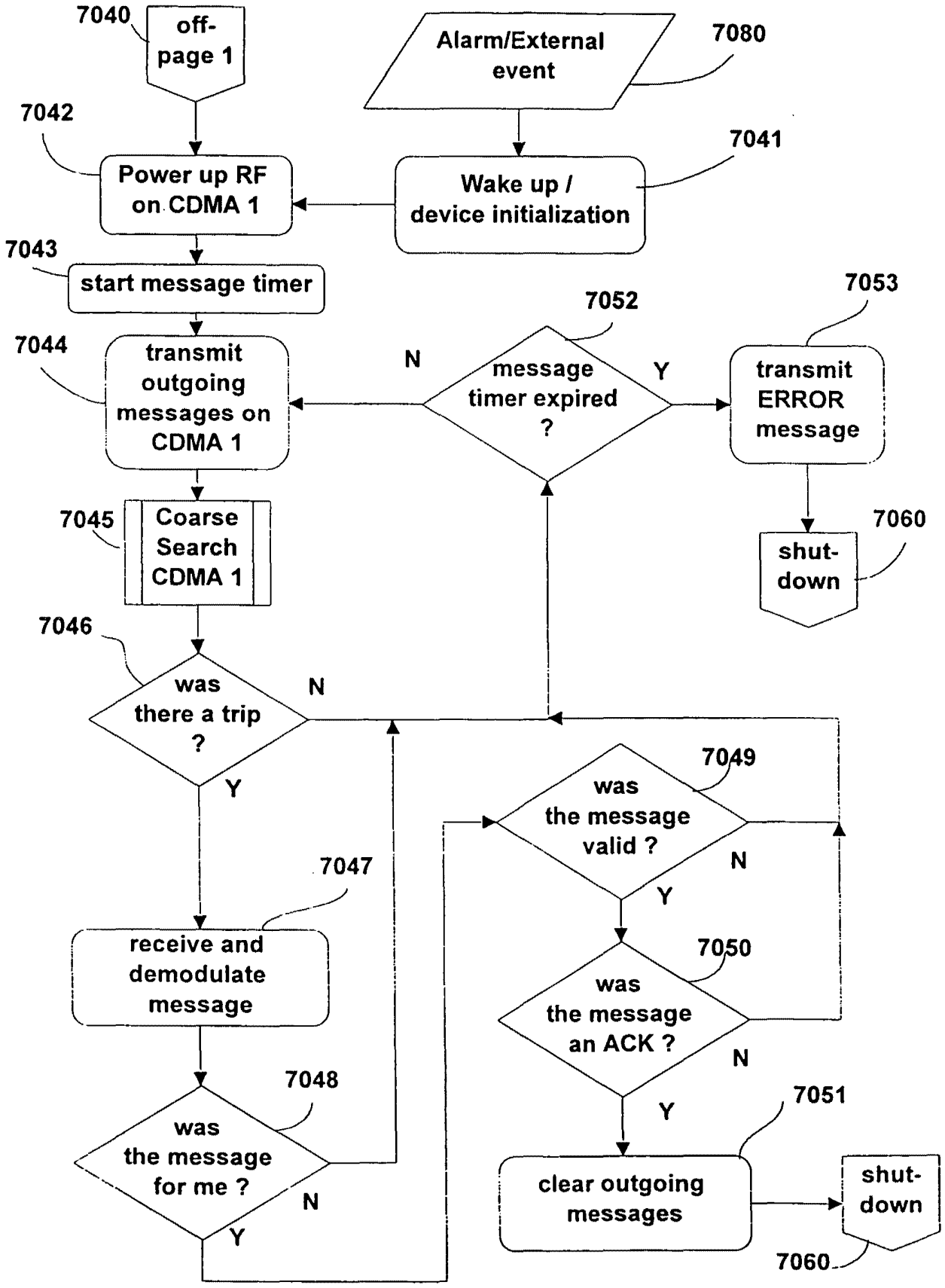

7040
off-page 1
Alarm/External event
7080
7042
7041
Power up RF on CDMA 1
Wake up / device initialization
7043
start message timer
7052
7053
7044
transmit outgoing messages on CDMA 1
N
message timer expired ?
Y
transmit ERROR message
7045
Coarse Search CDMA 1
7060
shut-down
7046
was there a trip ?
N
Y
7049
was the message valid ?
N
Y
7047
receive and demodulate message
7050
was the message an ACK ?
N
Y
7048
was the message for me ?
N
Y
7051
clear outgoing messages
shut-down
7060

Figure 70C

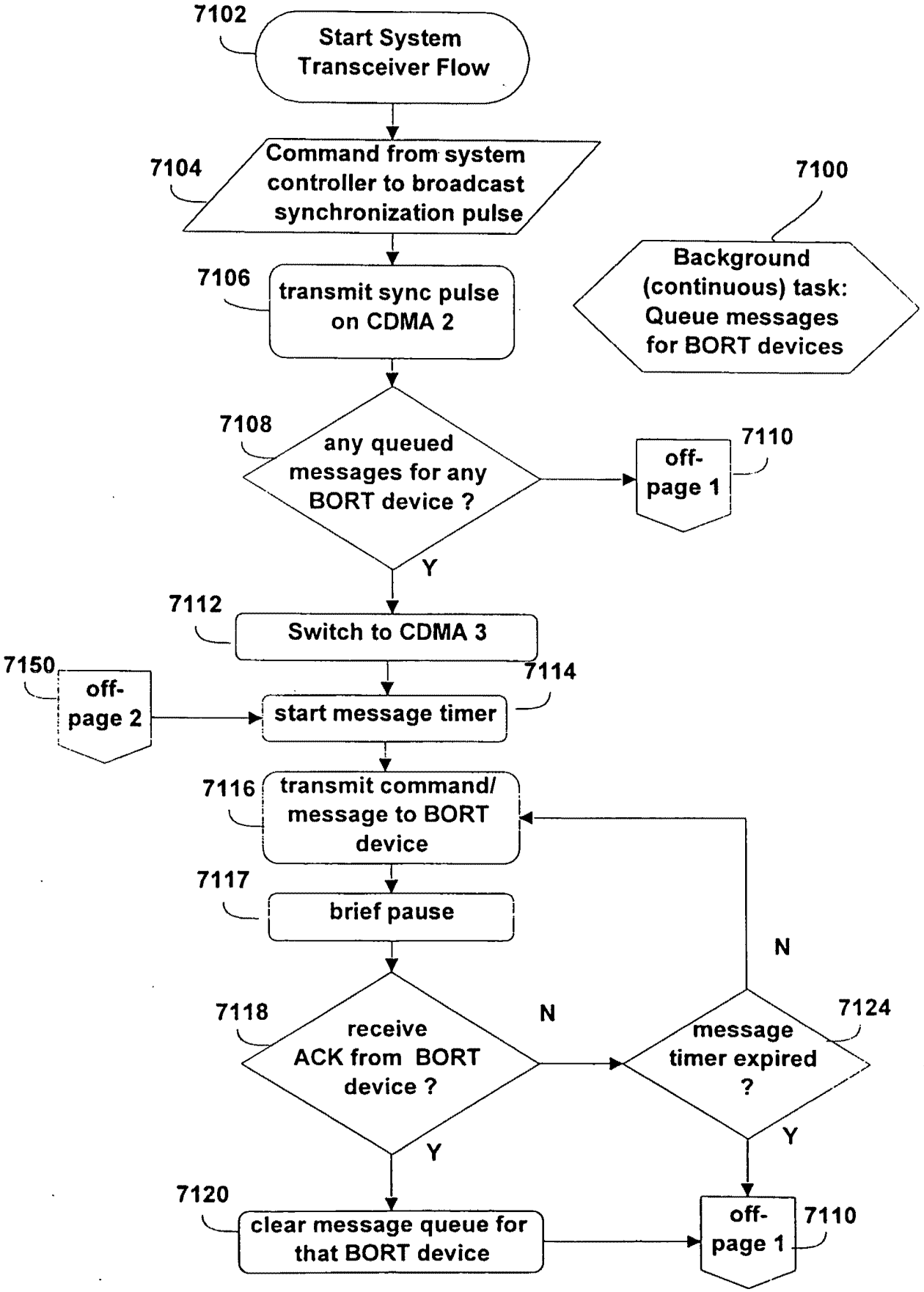

7102
Start System Transceiver Flow
7104
Command from system controller to broadcast synchronization pulse
7100
Background (continuous) task: Queue messages for BORT devices
7106
transmit sync pulse on CDMA 2
7108
any queued messages for any BORT device ?
7110
off-page 1
Y
7112
Switch to CDMA 3
7150
off-page 2
7114
start message timer
7116
transmit command/ message to BORT device
7117
brief pause
N
7118
receive ACK from BORT device ?
N
7124
message timer expired ?
Y
Y
7120
clear message queue for that BORT device
7110
off-page 1

Figure 71A

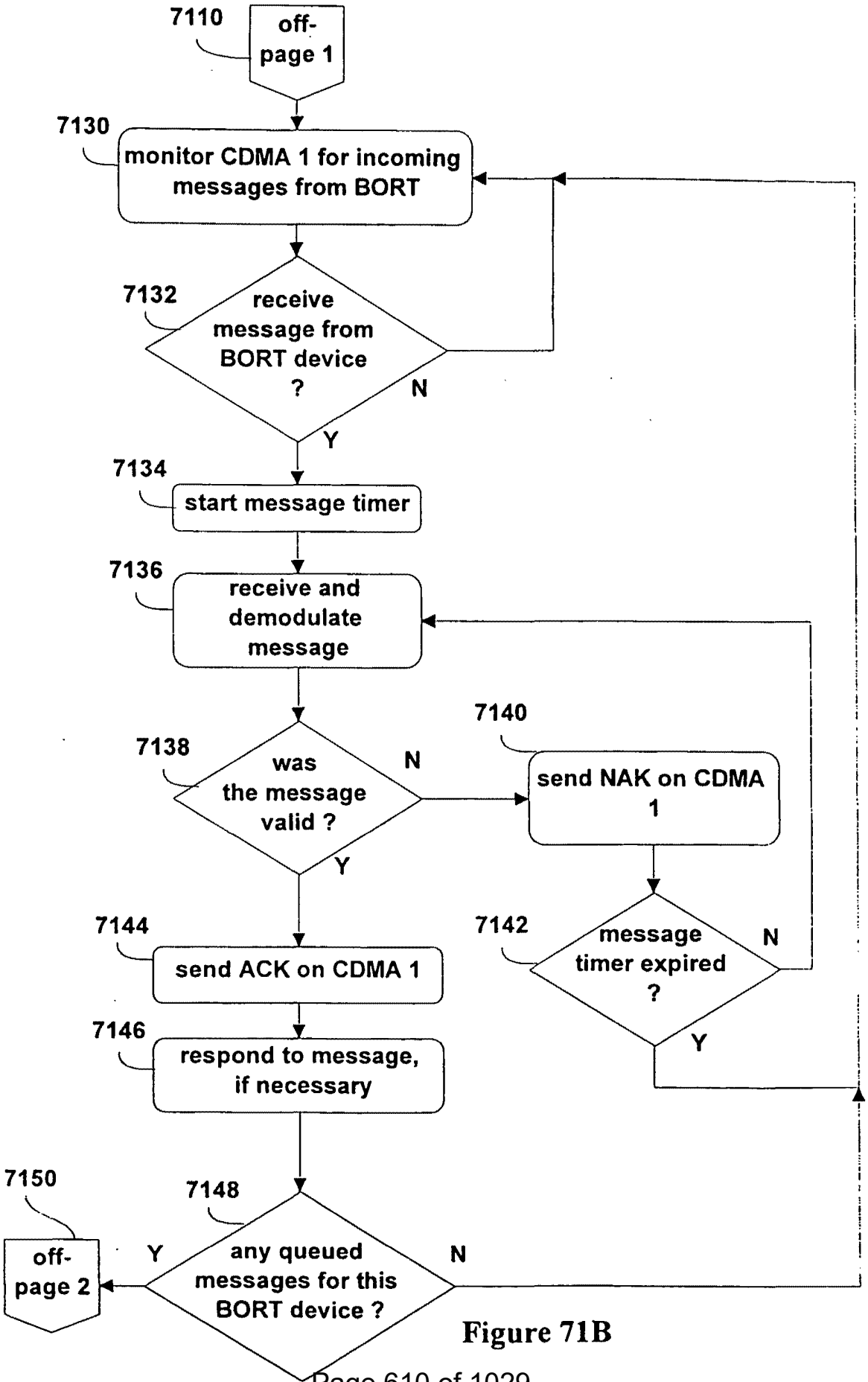

7110
off-page 1
7130
monitor CDMA 1 for incoming messages from BORT
7132
receive message from BORT device ?
N
Y
7134
start message timer
7136
receive and demodulate message
7138
was the message valid ?
N
Y
7140
send NAK on CDMA 1
7142
message timer expired ?
N
Y
7144
send ACK on CDMA 1
7146
respond to message, if necessary
7148
any queued messages for this BORT device ?
Y
N
7150
off-page 2

Figure 71B

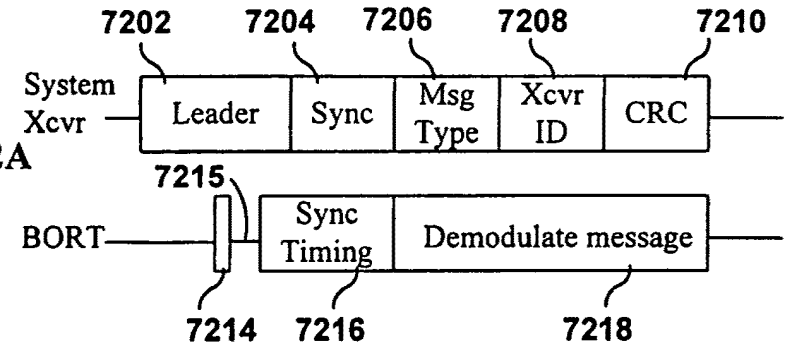


Figure 72A
Sync Message

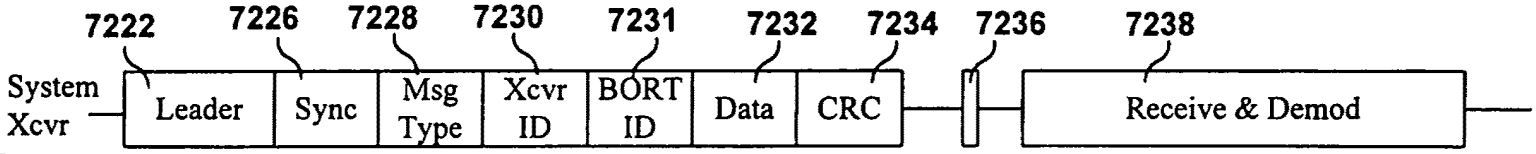
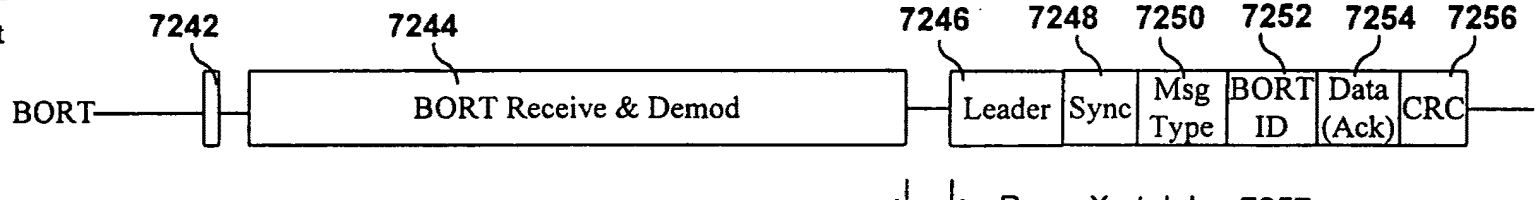


Figure 72B
Point to Point Message



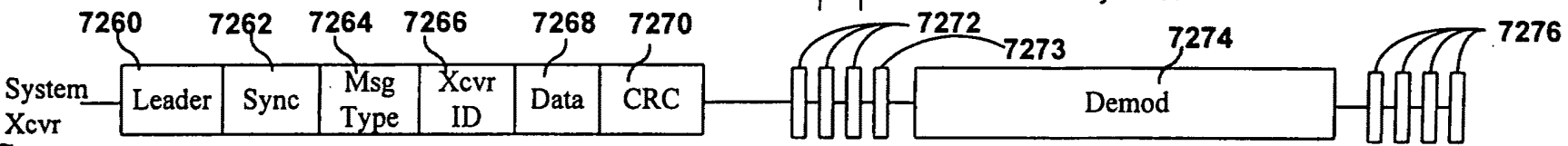
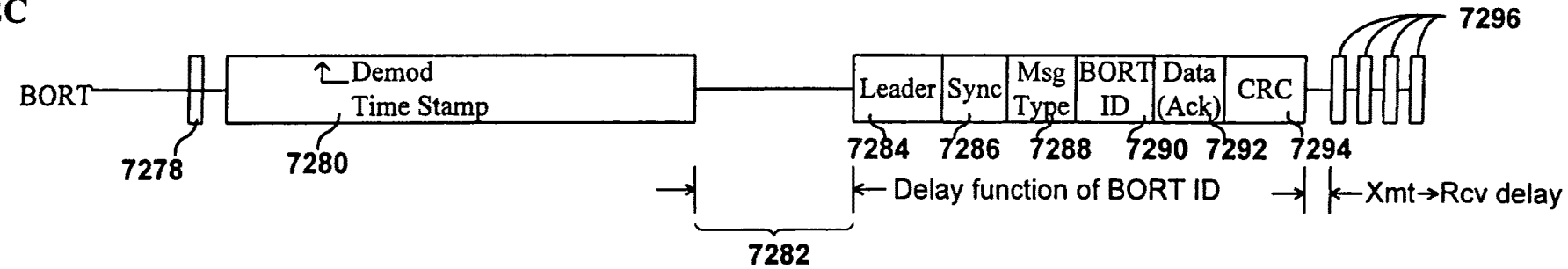


Figure 72C
All Call Message



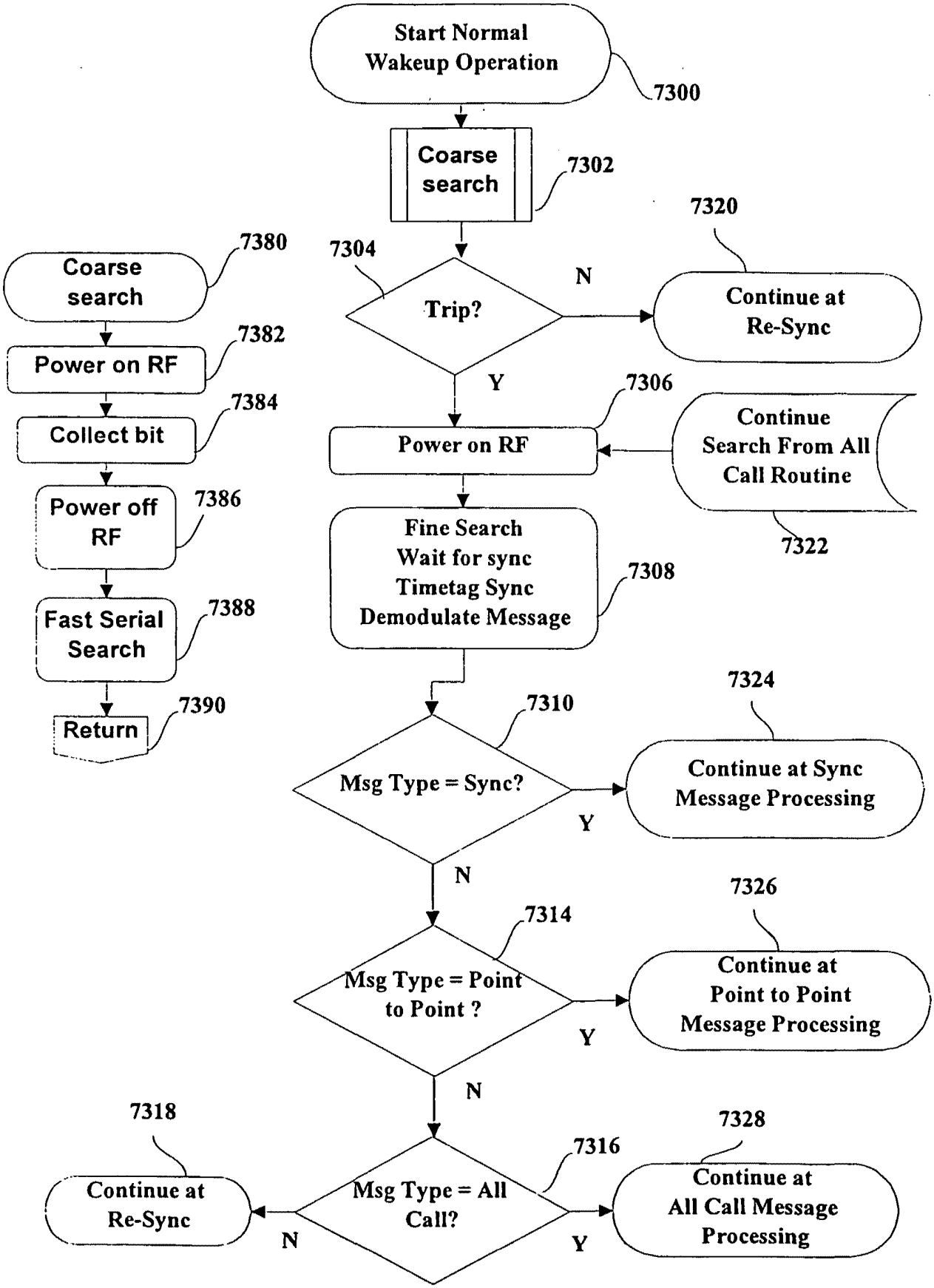

Start Normal Wakeup Operation
7300
Coarse search
7302
7304
Trip?
N
7320
Continue at Re-Sync
Y
7306
Power on RF
Continue Search From All Call Routine
7322
Fine Search
Wait for sync
Timetag Sync
Demodulate Message
7308
7310
Msg Type = Sync?
Y
7324
Continue at Sync Message Processing
N
7314
Msg Type = Point to Point ?
Y
7326
Continue at Point to Point Message Processing
N
7316
Msg Type = All Call?
N
7318
Continue at Re-Sync
Y
7328
Continue at All Call Message Processing
7380
Coarse search
7382
Power on RF
7384
Collect bit
7386
Power off RF
7388
Fast Serial Search
7390
Return

Figure 73A

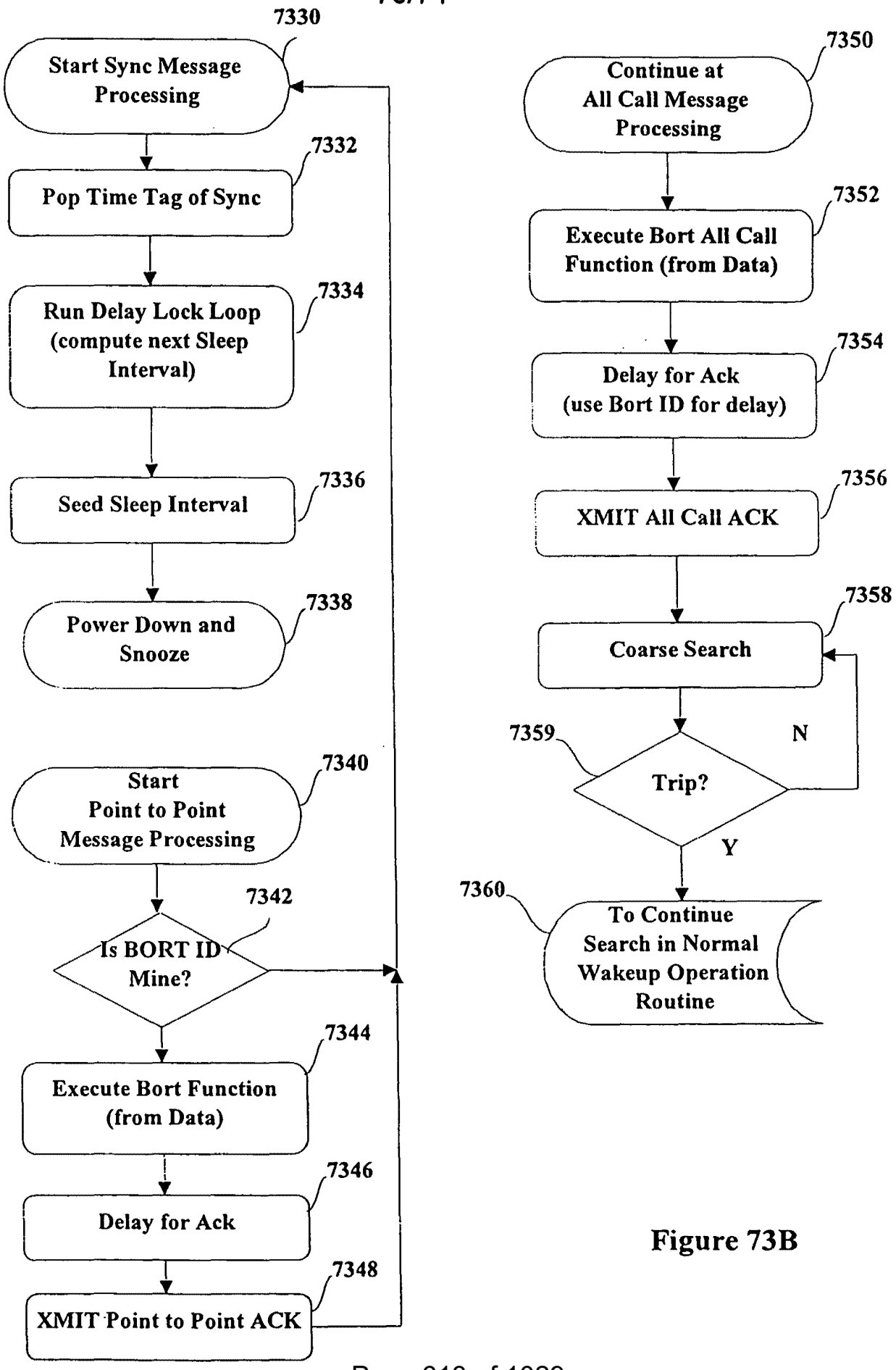

7330
Start Sync Message Processing
7332
Pop Time Tag of Sync
7334
Run Delay Lock Loop (compute next Sleep Interval)
7336
Seed Sleep Interval
7338
Power Down and Snooze
7340
Start Point to Point Message Processing
7342
Is BORT ID Mine?
7344
Execute Bort Function (from Data)
7346
Delay for Ack
7348
XMIT Point to Point ACK
7350
Continue at All Call Message Processing
7352
Execute Bort All Call Function (from Data)
7354
Delay for Ack (use Bort ID for delay)
7356
XMIT All Call ACK
7358
Coarse Search
7359
Trip?
N
Y
7360
To Continue Search in Normal Wakeup Operation Routine

Figure 73B

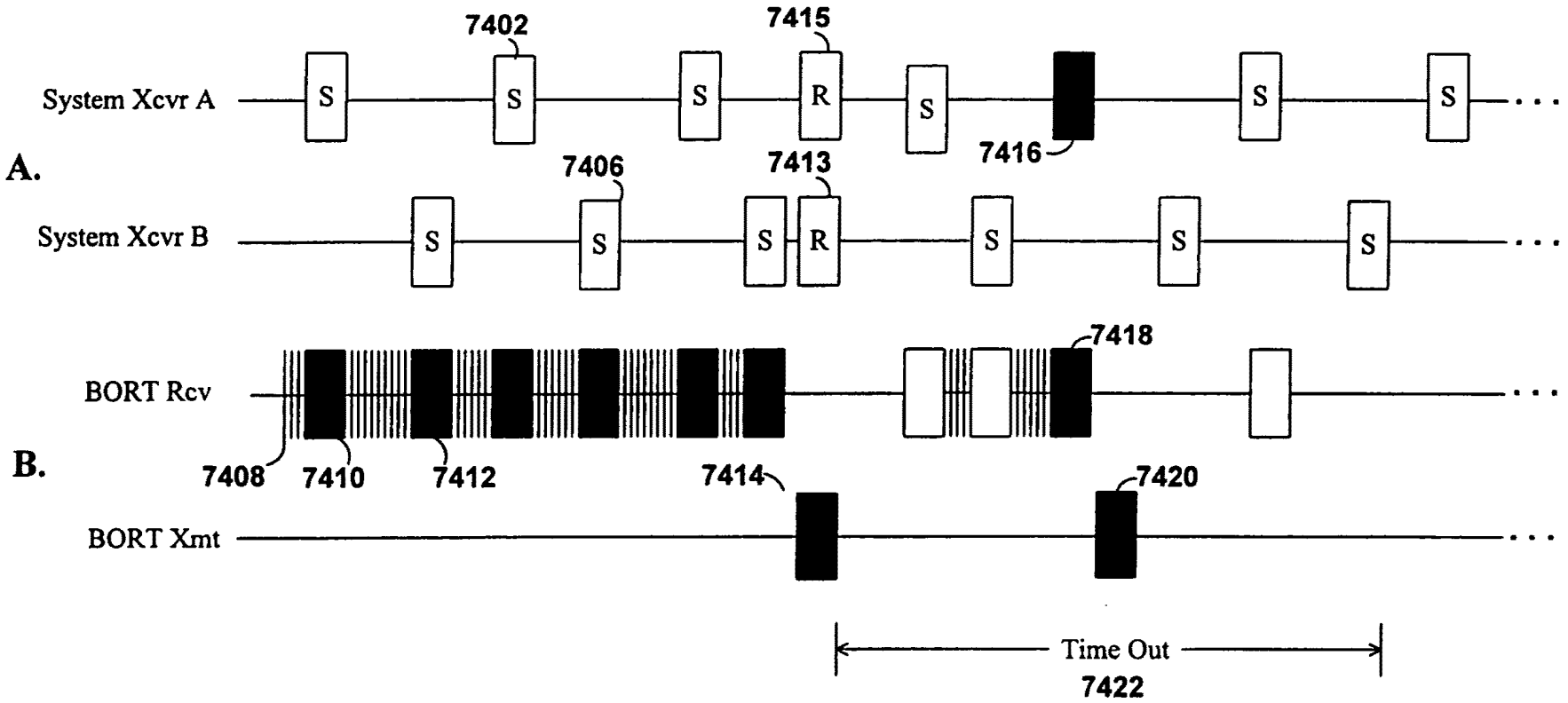

A.
System Xcvr A
S
S
S
R
S
S
S
7402
7415
7416
System Xcvr B
S
S
S
R
S
S
S
7406
7413
B.
BORT Rcv
BORT Xmt
7408
7410
7412
7414
7418
7420
Time Out
7422

FIGURE 74

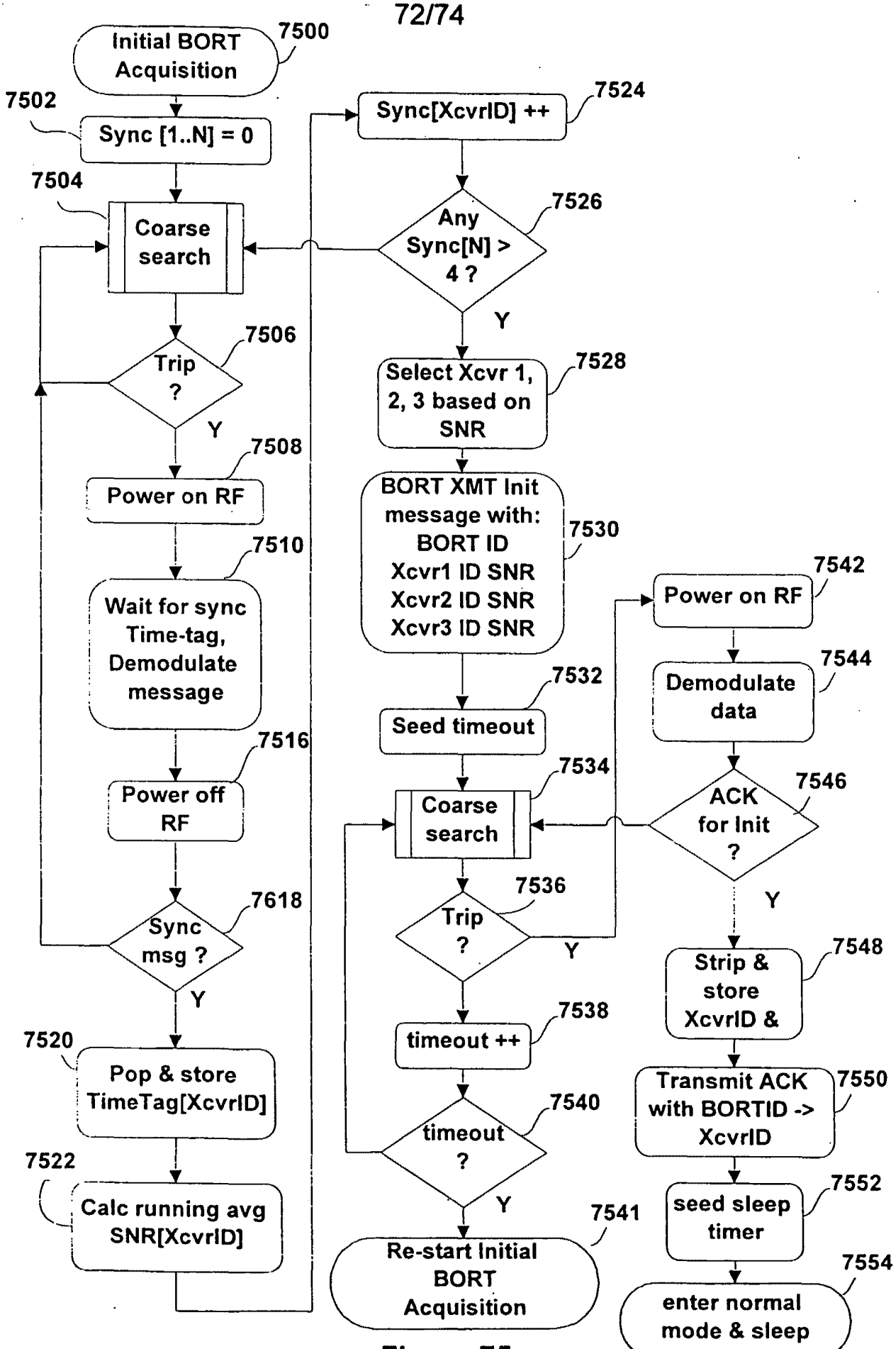

Initial BORT Acquisition
7500
7502
Sync [1..N] = 0
7504
Coarse search
7506
Trip ?
Y
7508
Power on RF
7510
Wait for sync Time-tag, Demodulate message
7516
Power off RF
7618
Sync msg ?
Y
7520
Pop & store TimeTag[XcvrID]
7522
Calc running avg SNR[XcvrID]
Sync[XcvrID] ++
7524
Any Sync[N] > 4 ?
7526
Y
Select Xcvr 1, 2, 3 based on SNR
7528
BORT XMT Init message with: BORT ID Xcvr1 ID SNR Xcvr2 ID SNR Xcvr3 ID SNR
7530
Seed timeout
7532
Coarse search
7534
Trip ?
7536
Y
timeout ++
7538
timeout ?
7540
Y
Re-start Initial BORT Acquisition
7541
Power on RF
7542
Demodulate data
7544
ACK for Init ?
7546
Y
Strip & store XcvrID &
7548
Transmit ACK with BORTID -> XcvrID
7550
seed sleep timer
7552
enter normal mode & sleep
7554

Figure 75

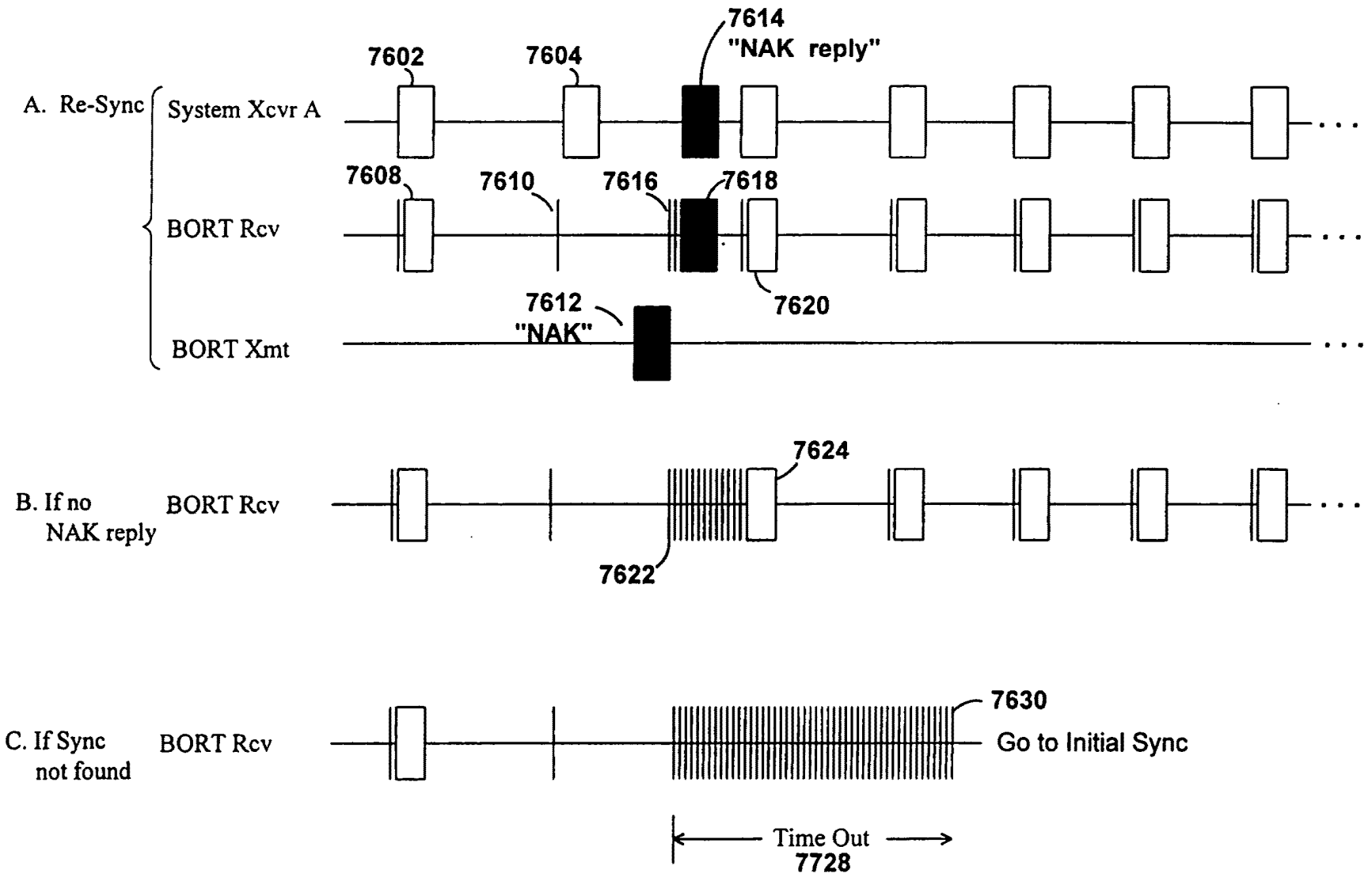

A. Re-Sync
System Xcvr A
BORT Rcv
BORT Xmt
7602
7604
7614
"NAK reply"
7608
7610
7616
7618
7620
7612
"NAK"
B. If no NAK reply
BORT Rcv
7624
7622
C. If Sync not found
BORT Rcv
7630
Go to Initial Sync
Time Out
7728

FIGURE 76

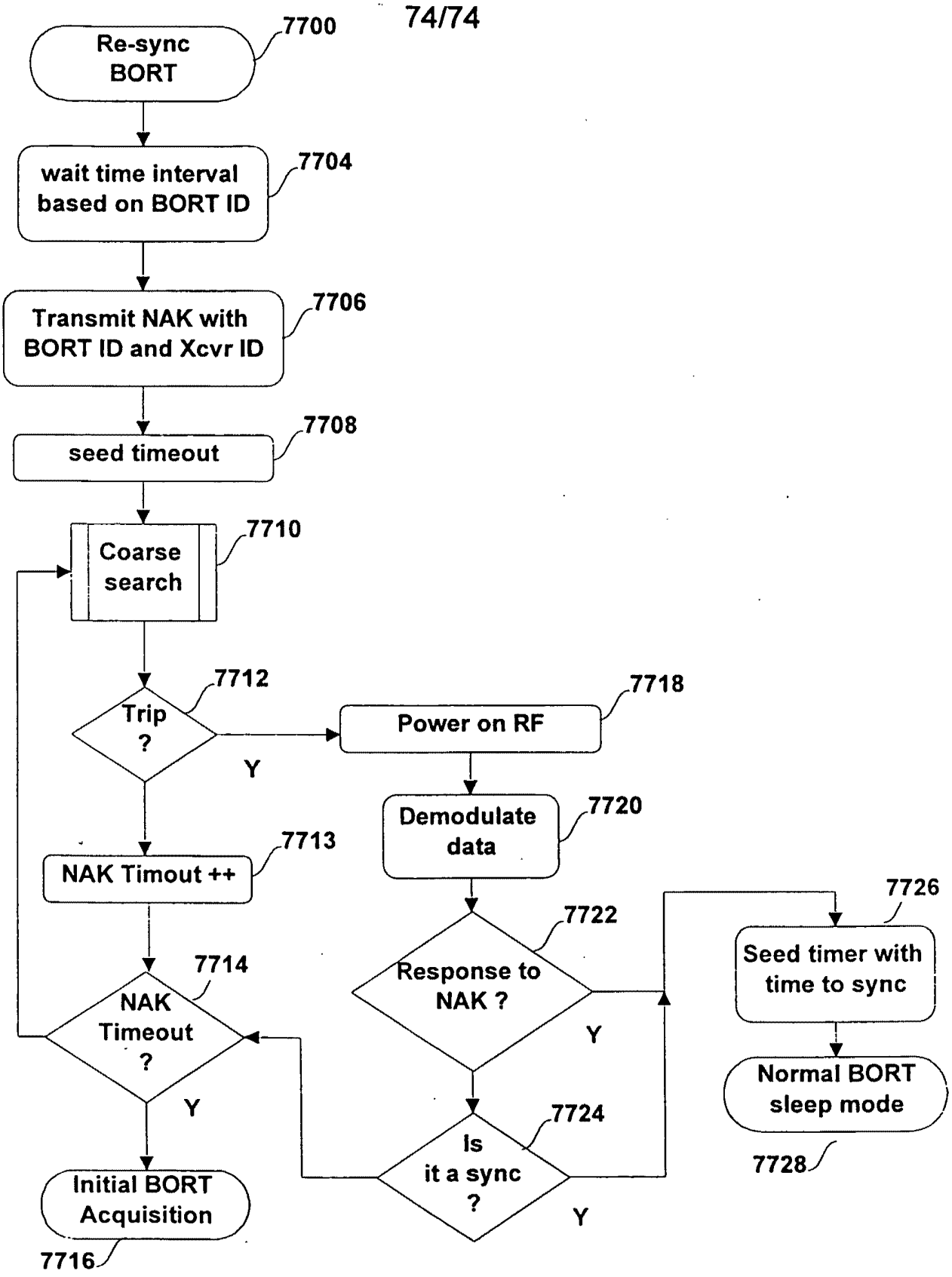

Re-sync BORT
7700
wait time interval based on BORT ID
7704
Transmit NAK with BORT ID and Xcvr ID
7706
seed timeout
7708
Coarse search
7710
Trip ?
7712
Y
Power on RF
7718
Demodulate data
7720
NAK Timout ++
7713
Response to NAK ?
7722
Y
Seed timer with time to sync
7726
NAK Timeout ?
7714
Y
Is it a sync ?
7724
Y
Normal BORT sleep mode
7728
Initial BORT Acquisition
7716

Figure 77

(51) Int. Cl.: H 03 c, 1/54

BUNDESREPUBLIK DEUTSCHLAND

DEUTSCHES PATENTAMT

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(33) Land: —
(31) Aktenzeichen: —

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(54) Bezeichnung: Modulator oder Demodulator in integrierter Technik

(61) Zusatz zu: —
(62) Ausscheidung aus: —

(71) Anmelder: Siemens AG, 1000 Berlin und 8000 München

Vertreter: —

(72) Als Erfinder benannt: Möhrmann, Dipl.-Ing. Karl-Heinz, 8000 München

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Benachrichtigung gemäß Art. 7 § 1 Abs. 2 Nr. 1 d. Ges. v. 4. 9. 1967 (BGBl. I S. 960): —

1936252

1936252

SIEMENS AKTIENGESELLSCHAFT
Berlin und München

München 2, den 16. JULI 1969
Wittelsbacherplatz 2

PA 69/2632

Modulator oder Demodulator in integrierter Technik

Die Erfindung betrifft einen integrierbaren aktiven Modulator oder Demodulator mit unsymmetrischem Eingang und unsymmetrischem Ausgang.

In der Trägerfrequenztechnik und auch auf anderen Gebieten der elektrischen Nachrichtentechnik werden zur Zeit aktive oder passive Modulatoren verwendet, die mindestens einen Übertrager verwenden. Derartige Schaltungen sind für die Übertragung in die integrierte Schaltungstechnik wenig geeignet, da sich Induktivitäten und Übertrager nur auf dem Umweg über Gyratoren und ähnliches und auch dann nur mit hohem Aufwand realisieren lassen. Bekannt sind Schaltungen mit zum Teil integrierten Elementen, bei denen zusätzlich Übertrager in konzentrierter Bauweise angeschlossen werden. Bisher bekannte Schaltungen, die nur aus Widerständen, Kondensatoren und Halbleiterbauelementen, wie Dioden und Transistoren, bestehen, haben den Nachteil, daß sie zum Teil einen recht hohen Aufwand erfordern, und daß außerdem das Eingangssignal symmetrisch sein muß.

Der Erfindung liegt die Aufgabe zugrunde, einen Modulator oder Demodulator der einleitend genannten Art anzugeben, der eine integrierbare Ausführung bei relativ geringem schaltungstechnischen Aufwand ermöglicht und daher als Ersatz für Ringmodulatoren, insbesondere in frequenzumsetzenden digitalen Filtern, Anwendung finden kann.

Erfindungsgemäß wird die Aufgabe dadurch gelöst, daß der Modulator aus einer Eingangsstufe mit zwei getrennten, gleiche Ausgangssignalamplituden abgebenden Ausgängen besteht, die über je einen Schaltervierpol an eine Ausgangsstufe angeschaltet sind, die die Ausgangssignale der beiden Schaltervierpole zusammenfaßt. Die Schaltervierpole werden wechselweise im Takt einer Trägerfrequenzschwingung betätigt. Die Phase eines der beiden Ausgangssignale der Eingangsstufe wird dabei entweder in der Eingangsstufe oder nach Durchlaufen des entsprechenden Schaltervierpols in der Ausgangsstufe um 180° verschoben.

Bei Phasendrehung in der Eingangsstufe ist es vorteilhaft, die Eingangsstufe als Phasenumkehrstufe auszubilden, deren Ausgangssignalamplituden gegenphasig gleich sind. Bei Phasendrehung in der Ausgangsstufe ist die Ausgangsstufe vorzugsweise als Differenzverstärker ausgebildet und die Phase eines der Ausgangssignale der Eingangsstufe erscheint am Ausgang des Differenzverstärkers um 180° verschoben.

Da es auf Grund der Schaltzeiten der Schaltelemente schwierig ist, den einen Schaltervierpol zum gleichen Zeitpunkt zu öffnen, an dem der andere Schaltervierpol schließt und umgekehrt, ist es günstig, die Schaltelemente in den beiden Schaltervierpolen durch zwei von der Trägerschwingung abgeleitete, um 180° verschobene Rechteckimpulsfolgen zu steuern, deren Verhältnis von Impulsdauer zu Impulspause kleiner als 1 ist. Es ist dann sichergestellt, daß jeweils nur ein Schaltervierpol für das Ausgangssignal der Eingangsstufe durchlässig ist. Bei einem Verhältnis von Impulsdauer zu Impulspause von 1/2 ergibt sich der weitere Vorteil, daß die dritte Harmonische der Schaltfrequenz in der

entstehenden Umpolfunktion nicht enthalten ist, wie sich mit Hilfe einer Fourier-Analyse feststellen läßt.

Vorteilhaft ist es auch, in den beiden Schaltervierpolen Feldeffekttransistoren zu verwenden, da die Offsetspannung bei Feldeffekttransistoren gegenüber der Offsetspannung bei üblichen Transistoren verschwindend gering ist.

Durch einen Aufbau des Modulators in der oben beschriebenen Art läßt sich erreichen, daß für die Schaltung des Modulators nur Widerstände und Halbleiterelemente, wie Transistoren und Dioden, erforderlich sind. Ein Aufbau des Modulators in integrierter Bauform ist daher besonders einfach zu realisieren. Ein besonders bevorzugtes Anwendungsgebiet dieses Modulators ist daher die Anwendung in frequenzumsetzenden digitalen Filtern in integrierter Bauform.

Einige Ausführungsformen des erfindungsgemäßen Modulators werden anhand der Zeichnungen noch näher erläutert. Es zeigen

Fig.1 einen Modulator mit gegenphasigen Ausgängen der Eingangsstufe,

Fig.2 einen weiteren Modulator mit gegenphasigen Ausgängen der Eingangsstufe,

Fig.3 einen Modulator mit gegenphasigen Eingängen der Ausgangsstufe,

Fig.4 ein bevorzugtes weiteres Ausführungsbeispiel eines Modulators mit gegenphasigen Ausgängen der Eingangsstufe,

Fig.5 den zeitlichen Verlauf einer Rechteckimpulsfolge zur Steuerung der Schaltervierpole der Modulatoren nach den Fig.1 bis 4.

Der Modulator nach Fig.1 enthält eine Eingangsstufe I mit dem Eingang E, dem Transistor T_0, dem Basisspannungsteiler mit den Widerständen $R1_0$ und $R2_0$, den Arbeitswiderständen $R3_0$ und $R4_0$ und den gegenphasigen Ausgangsanschlüssen A1 und A2, die mit den Eingangsanschlüssen E1 und E2 der Schaltervierpole SV1 und SV2 verbunden sind. Die Ausgangsanschlüsse A3 und A4 der Schaltervierpole sind parallelgeschaltet. Der Modulator stellt einen Gegentaktmodulator dar, bei dem beide Schaltervierpole abwechselnd durch einen von der Trägerschwingung abgeleiteten Takt S1 bzw. S2 in Form einer Rechteckimpulsfolge gesperrt oder durchgeschaltet werden. Am gemeinsamen Ausgang A der beiden Schaltervierpole ergeben sich in an sich bekannter Weise die das Eingangssignal darstellenden Seitenbänder der Frequenz der Trägerschwingung bei gleichzeitiger Unterdrückung des Trägers.

Die weiteren Ausführungsbeispiele nach den Figuren 2 bis 4 sind ebenfalls Gegentaktmodulatoren. Der Modulator nach Fig.2 enthält wiederum eine Eingangsstufe I mit zwei Verstärkern V1 und V2, deren gegenphasige Ausgangsanschlüsse A1 und A2 mit den Eingangsanschlüssen E1 und E2 zweier Schaltervierpole SV1 und SV2 verbunden sind. Die Ausgangsanschlüsse A3 und A4 der beiden Schaltervierpole sind mit den Eingangsanschlüssen eines die Ausgangsstufe darstellenden Summierers mit dem Ausgang A verbunden. Die Schaltervierpole SV1 und SV2 enthalten zwei Feldeffekttransistoren FET 1 und FET 2. Ihre Elektroden sind mit den bei Feldeffekttransistoren üblichen Bezeichnungen S = Source oder Kathode, D = Drain oder Anode und G = Gate oder Gitter versehen. Die Takte S1 und S2 sind den Gittern G der Feldeffekttransistoren über Spannungsteiler, bestehend aus der Reihenschaltung einer Diode D1 bzw. D2 mit einem Widerstand R3 bzw. R4, zugeführt. Die Ausgangsanschlüsse A1 und A2 der Eingangs-

stufe I sind über die u.a. der Entkopplung dienenden Widerstände R1 und R2 unmittelbar mit den Ausgangsanschlüssen A3 und A4 verbunden. Die Feldeffekttransistoren FET 1 und FET 2 sind mit ihrer Anode D jeweils an den gemeinsamen Verbindungspunkt des Widerstandes R1 bzw. R2 mit dem Ausgangsanschluß A3 bzw. A4 angeschaltet und bilden unter Berücksichtigung ihrer auf Erdpotential liegenden Kathoden K einen steuerbaren Kurzschluß für die Ausgänge der Schaltervierpole. In diesem Fall ist es unbedingt erforderlich, daß die Ausgangsstufe II eine Summierstufe ist, da sonst das Ausgangssignal des gesamten Modulators kurzgeschlossen würde.

Der Modulator nach Fig.3 enthält als Eingangsstufe I zwei Eingangsverstärker V1 und V2', von denen im Unterschied zum Verstärker V2 nach Fig.2 auch der Verstärker V2' zwischen Ein- und Ausgang keine Phasendrehung aufweist. Die sich an die Eingangsstufe I anschließenden Schaltervierpole SV1 und SV2 haben im Prinzip den gleichen Aufbau wie die Schaltervierpole nach Fig.2. Sie unterscheiden sich hiervon lediglich durch die Verwendung von normalen Transistoren T1 und T2 anstelle von Feldeffekttransistoren FET 1 und FET 2 und den Ersatz der Dioden D1 und D2 im Steuerkreis durch die Widerstände R5 und R6. Die Ausgangsstufe II ist hier ein Differenzverstärker, der die für die Funktion eines Gegentaktmodulators erforderliche Phasenumkehr in einem der beiden Übertragungswege bewirkt.

Fig.4 zeigt ein besonders vorteilhaftes Ausführungsbeispiel für einen Gegentaktmodulator nach der Erfindung. Seine Eingangsstufe I ist mit der Eingangsstufe I des Modulators nach Fig.2 identisch. Während beim Ausführungsbeispiel nach Fig.2 die Feldeffekttransistoren

FET 1 und FET 2 der Schaltervierpole SV1 und SV2 im Sinne steuerbarer Kurzschlüsse mit ihren Anoden-Kathodenstrecken den Ausgängen der Schaltervierpole parallel geschaltet sind, sind die Anoden-Kathodenstrecken der Feldeffekttransistoren FET1 und FET 2 hier im Sinne einer steuerbaren Unterbrechung der Verbindung zwischen dem Eingangsanschluß E1 bzw. E2 und dem Ausgangsanschluß A3 bzw. A4 dem Widerstand R1 bzw. R2 in Serie geschaltet. In diesem Fall kann der Takt S1 bzw. S2 dem Gitter G der Feldeffekttransistoren FET 1 bzw. FET 2 unmittelbar zugeführt werden, d.h. die beim Ausführungsbeispiel nach Fig.2 vorgesehenen Spannungsteiler kommen hier in Fortfall. Die Ausgangsstufe II ist hier ein Operationsverstärker V3, dessen invertierendem Eingang die Ausgangsanschlüsse A3 und A4 parallel angeschaltet sind. Der Operationsverstärker V3 kann entfallen, wenn durch eine entsprechende Eingangsschaltung das richtige Schaltverhalten der Feldeffekttransistoren FET 1 und FET 2 sichergestellt ist.

Der Vollständigkeit halber ist in Fig.5 noch der Verlauf der an den Steuereingängen der Schaltervierpole SV1 und SV2 anliegenden Takte S1 bzw. S2 über der Zeit t angegeben. Die Schaltervierpole SV1 und SV2 sind bei "O" für das Eingangssignal durchlässig, während sie bei "Z" gesperrt sind. Da es mit Halbleiterbauelementen kaum zu erreichen ist, daß zu dem Zeitpunkt, in dem der eine Schaltervierpol öffnet, der andere schließt, ist es günstig, von der Trägerschwingung zwei Rechteckimpulsfolgen der in Fig.5 gezeigten Form abzuleiten, bei der die Impulspause 240° und die Impulsdauer 120° einer Periode beträgt, und daß die Rechteckschwingungen der beiden Schaltervierpole um 180° gegeneinander verschoben sind. Dadurch ist sichergestellt, daß nur einer der beiden Schaltervierpole durchgeschaltet bzw. nicht

kurzgeschlossen ist. Durch das obengenannte Verhältnis von Impulsdauer zu Impulspause ergibt sich außerdem der Vorteil, daß die dritte Harmonische der Schaltfrequenz in der entstehenden Umpolfunktion nicht enthalten ist.

Die Schaltervierpole SV1, SV2 nach den Figuren 2 und 3 können gegeneinander ausgetauscht werden. Auch besteht die Möglichkeit, die Feldeffekttransistoren FET 1 und FET 2 der Schaltervierpole SV1 und SV2 nach Fig.4 durch gewöhnliche Transistoren zu ersetzen, die hierbei mit ihrer Emitter-Kollektorstrecke den Widerständen R1 und R2 in Serie zu schalten sind. Im übrigen ist festzustellen, daß Schaltervierpole mit seriengeschalteten Transistoren auch an die Stelle der Schaltervierpole nach den Figuren 1 bis 3 treten können.

5 Figuren
8 Patentansprüche

Patentansprüche

1. Integrierbarer aktiver Modulator oder Demodulator mit unsymmetrischem Eingang und unsymmetrischem Ausgang, dadurch gekennzeichnet, daß der Modulator aus einer Eingangsstufe mit zwei getrennten, gleiche Ausgangssignalamplituden abgebenden Ausgängen besteht, die über je einen Schaltervierpol an eine Ausgangsstufe angeschaltet sind, daß ferner die Schaltervierpole jeweils wechselweise im Takt einer Trägerfrequenzschwingung betätigt werden, daß außerdem die Ausgangsstufe die Ausgangssignale der beiden Schaltervierpole zusammenfaßt, und daß die Phase eines der beiden Ausgangssignale der Eingangsstufe entweder in der Eingangsstufe oder nach Durchlaufen des entsprechenden Schaltervierpols in der Ausgangsstufe um 180° verschoben ist.

2. Modulator nach Anspruch 1, bei dem die Phase eines der Ausgangssignale der Eingangsstufe gegenüber der Phase des anderen Ausgangssignals um 180° verschoben ist, dadurch gekennzeichnet, daß die Eingangsstufe als Phasenumkehrstufe mit zwei gegenphasige amplitudengleiche Ausgangssignale abgebenden Ausgängen ausgebildet ist.

3. Modulator nach Anspruch 1, bei dem die Phase eines der Ausgangssignale der Eingangsstufe in der Ausgangsstufe um 180° verschoben ist, dadurch gekennzeichnet, daß die Ausgangsstufe als Differenzverstärker ausgebildet ist.

4. Modulator nach Anspruch 1, dadurch gekennzeichnet, daß zum Betätigen der beiden Schaltervierpole zwei von der Trägerschwingung abge-

leitete, um 180° gegeneinander verschobene Rechteckimpulsfolgen vorgesehen sind.

5. Modulator nach Anspruch 4, dadurch gekennzeichnet, daß das Verhältnis von Impulsdauer zu Impulspause der von der Trägerschwingung abgeleiteten Rechteckimpulsfolge kleiner als 1, vorzugsweise zu 1/2 gewählt ist.

6. Modulator nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß in den Schaltervierpolen Feldeffekttransistoren als Schaltelemente vorgesehen sind.

7. Modulator nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Schaltung des Modulators nur Widerstände und Halbleiterelemente, wie Transistoren und Dioden, enthält.

8. Modulator nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß der Modulator insbesondere zur Anwendung in frequenzumsetzenden digitalen Filtern vorgesehen ist.

21 a 4 14-01 AT: 16.07.1969 OT: 28.01.1971

-11- 1936252

Fig.1

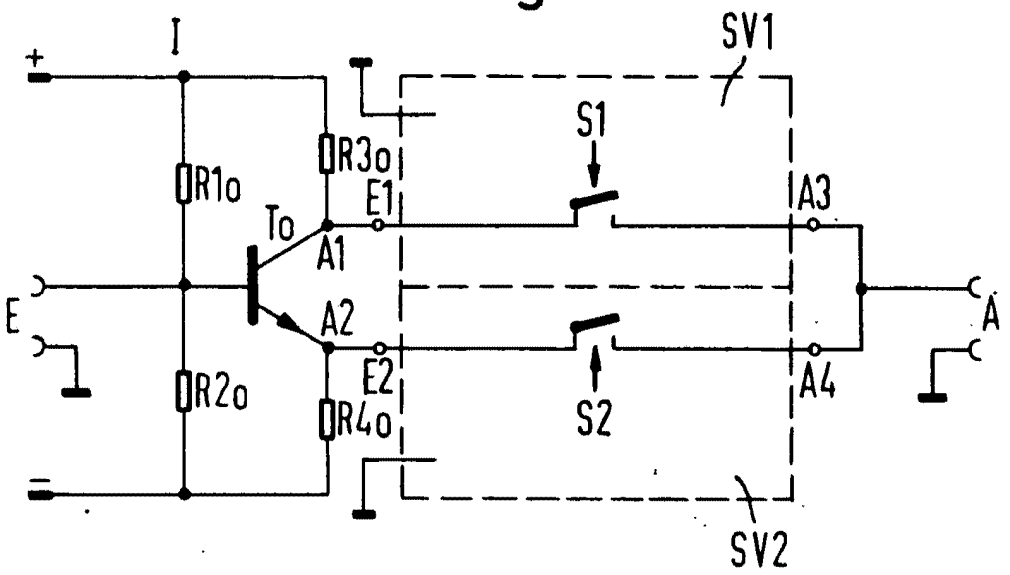


Fig.2

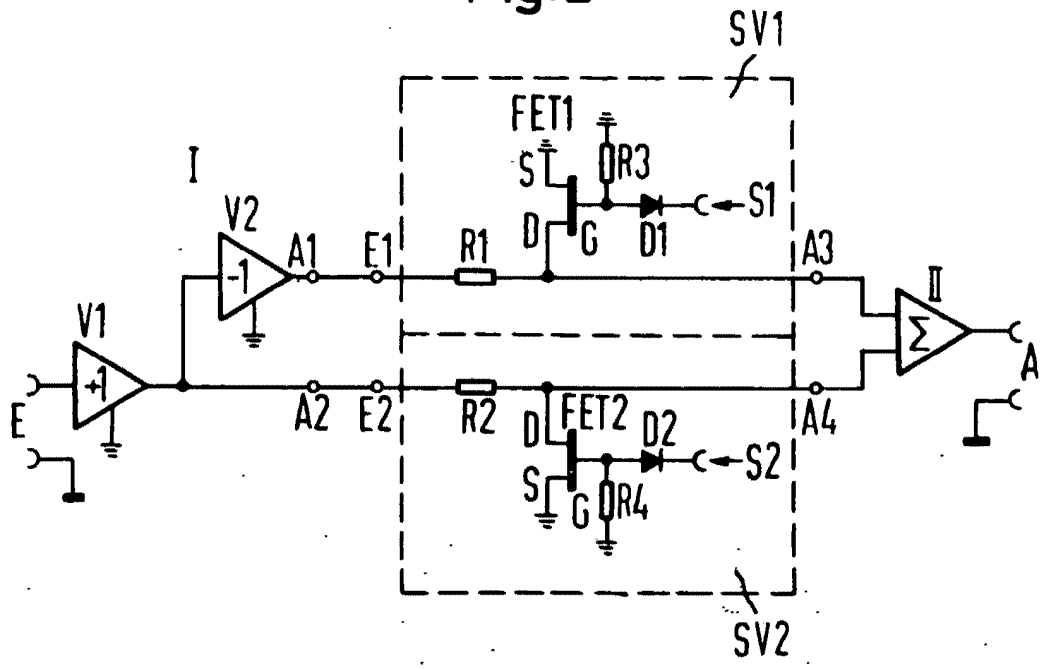


Fig.3

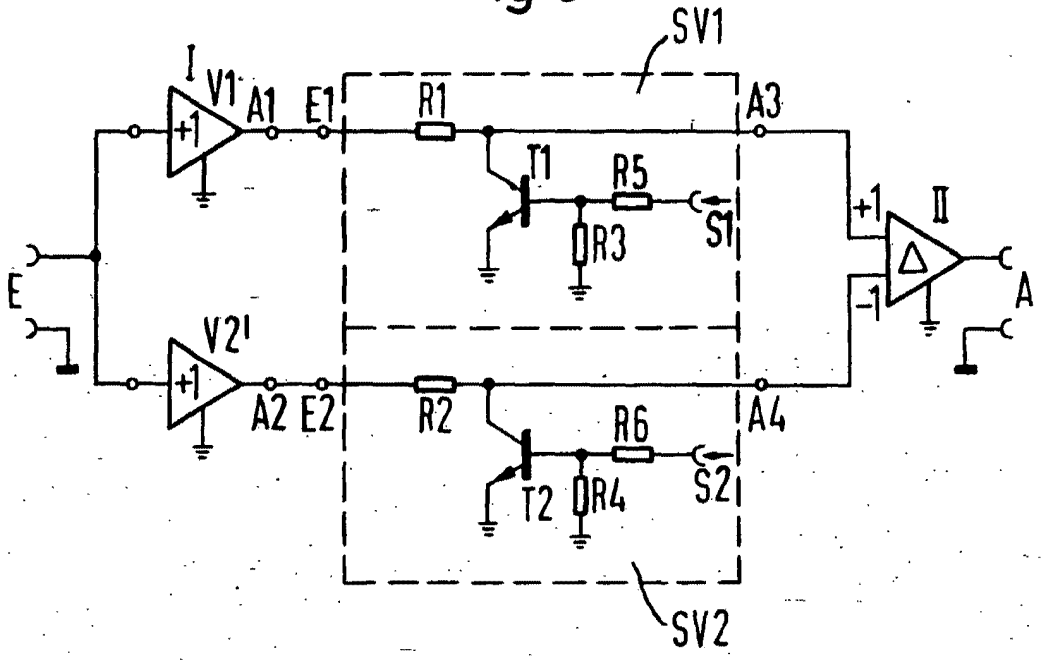


Fig.4

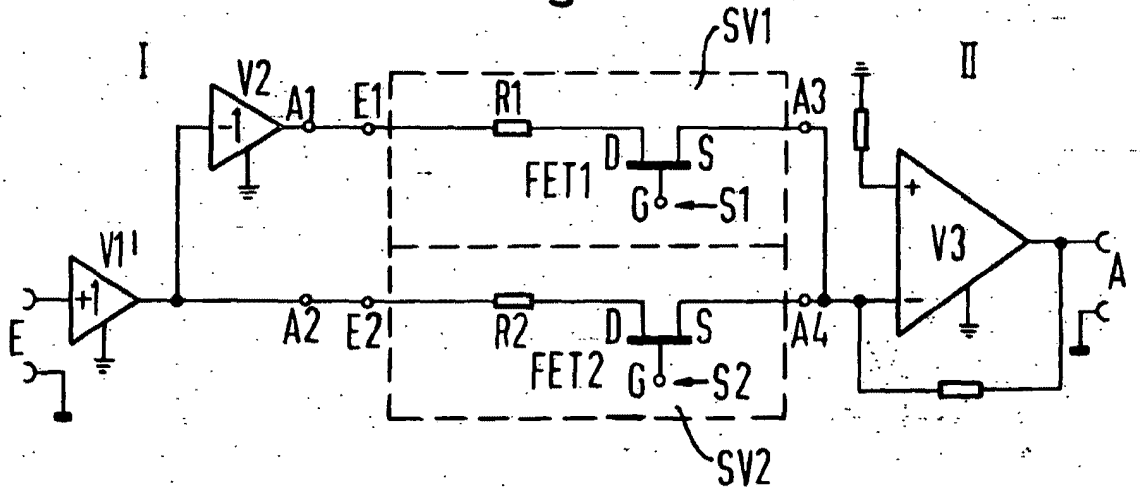
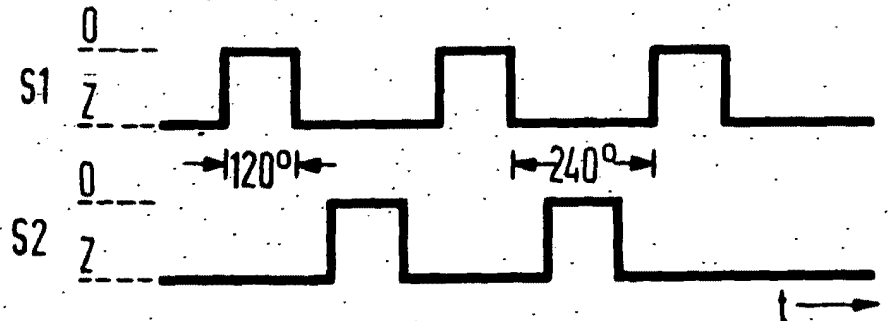


Fig.5



IDS Doc. Ref. AL24
for Appl. No. 10/973,917

⑲日本国特許庁（JP）　⑪特

⑫公開特許公報（A）　昭62－12381

⑤1Int.Cl.⁴	識別記号	庁内整理番号	⑬公開　昭和62年(1987)1月21日
H 02 M 7/48		F－7154－5H	

審査請求　未請求　発明の数 1　（全4頁）

⑤4発明の名称　インバータ装置のパルス幅変調制御方式

⑳特　願　昭60－151737
㉒出　願　昭60(1985)7月9日

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⑦4代理人　弁理士　青山　葆　外2名

明　細　書

1．発明の名称

インバータ装置のパルス幅変調制御方式

2．特許請求の範囲

(1) インバータ装置におけるパルス幅変調制御方式において、出力周波数が所定値より高くなったとき変調波を三角波からノコギリ波に切換えることを特徴とするインバータ装置のパルス幅変調制御方式。

3．発明の詳細な説明

[産業上の利用分野]

この発明はパルス幅変調インバータ装置におけるパルス幅変調制御方式に関する。

[従来技術とその問題点]

パルス幅変調(PWM)により、パルス幅の異なる方形波を出力し、これをリアクトル等を用いて等価的に任意の周波数の正弦波電圧を発生させるいわゆる、パルス幅変調インバータは、低次の高調波を抑制できる長所を有し、比較的小容量のインバータ装置に用いられている。第3図はパルス幅変調インバータ装置における従来のパルス幅変調制御部を示している。

マイクロプロセッサ1には、周波数設定器2からの電圧信号をV／Fコンバータ3により変換した周波数信号と、変調に必要な三角波発生回路4からの三角波と、過電流や過電圧を保護するための保護回路5からの信号、及びV／Fパターン回路6，トルクブースト回路7，加速時間設定回路8，減速時間設定回路9からの信号等が入力されていて、ROM(リードオンメモリ)10によるプログラムに従ってパルス幅変調の所定の演算が行なわれる。第4図は上述のパルス幅変調のタイムチャートを示していて、21は、周波数設定器2により設定された周波数による正弦波であり、例えばU相のみを示している。22は三角波発生回路4による三角波であり、両波形の交点であるa点，b点，c点，d点…がこのマイクロプロセッサ1により演算され、方形波信号23で示すように、パルスオン期間Ton＝b－a，パルスオフ期間Toff＝c－bがそれぞれ3相分求められ、出力タイマー回

路11に送出される。出力タイマー回路11からは時間出力Ut，Vt，Wt，として出力され、この信号は、オンディレィ回路12によりパルスU，V，W及びこのパルスの位相を180°遅らせたパルス$\overline{U}$，$\overline{V}$，$\overline{W}$との6パルスとして出力され、このパルス信号はゲート信号として、3相インバータ回路に送出される。

上述した回路構成においては、正弦波21と三角波22との交点を各相毎に三角波22の1周期に2回づつ高速に演算する必要があり、インバータ装置を高周波領域で動作させようと思えば、前記演算を更に高速で処理しなければならなくなるので、従来より、低周波領域では上述したパルス幅変調制御を行い、高周波領域になると、パルス振幅(PAM)制御に切換えていた。ところがこのパルス振幅変調制御によるインバータ装置では、パルス幅変調制御のように第5次，第7次の低次高周波を抑制することができず、多くの高周波が流出し、電動機等に悪影響を及ぼしていた。

〔発明の目的〕

この発明は上述した問題点をなくすためになされたものであり、従来と同一機種のインバータ装置でより高い出力周波数域においても高調波発生の恐れのないインバータ装置の変調切換制御方式を提供することを目的とする。

〔発明の構成〕

この発明のインバータ装置のパルス幅変調制御方式は、インバータ装置におけるパルス幅変調制御方式において、出力周波数が所定値より高くなったとき変調波を三角波からノコギリ波に切換えることを特徴とする。

〔実施例〕

第1図はこの発明の1実施例を示していて、従来例と異なるのは、三角波発生回路4の外にノコギリ波発生回路13を備え、又、ROM14には、周波数設定器2による設定周波数が所定値よりも高くなったときに変調波を三角波からノコギリ波に切換えてノコギリ波による変調制御を行うプログラムも含まれている。

従って、低周波帯域においては上述した従来例で説明した三角波による変調制御がなされ、設定周波数がROM14に書き込まれている周波数よりも高くなった高周波帯域ではマイクロプロセッサ1はノコギリ波発生回路13によるノコギリ波をとり込み、このノコギリ波を変調波として用いることにより変調制御される。

以下このノコギリ波による変調方式を第2図により説明する。

21はV／F変換器3からの正弦波であり、24は第1図におけるノコギリ波発生回路13によるノコギリ波である。この変調方式によれば、従来例のようにTon，Toffを求める場合、変調波であるノコギリ波の1周期Tcはあらかじめわかっているので、正弦波21とノコギリ波24の交点は、f点，g点のように、ノコギリ波24の1周期Tc内で1回求めるだけでパルスオン期間Tonは求まり、パルスオフ期間ToffはToff＝Tc－Tonにより簡単に求めることができ、マイクロプロセッサ1におけうる演算時間は大幅に短縮される。これにより、パルス幅変調制御方式でより高周波域まで動作可能となり、しかも高調波発生の恐れもなくなる。

〔発明の効果〕

以上説明したように、この発明は、パルス幅変調制御における変調波をインバータの使用周波数が所定値より高くなったとき、三角波からノコギリ波に切換えるようにしたのでマイクロプロセッサにおけるパルス幅変調のための演算が簡単になり、高速に処理できる。これにより、インバータ装置はより高周波域まで動作可能となり、しかも高調波発生を抑制することができる。

4．図面の簡単な説明

第1図はこの発明の1実施例を示すインバータ装置におけるパルス幅変調制御部のブロック図、第2図は第1図における動作を示すタイムチャート、第3図は変調波に三角波を用いたパルス幅変調制御部のブロック図、第4図は第3図における動作を示すタイムチャートである。

1…マイクロプロセッサ、　13…ノコギリ波発生回路、　14…ROM、　21…正弦波、

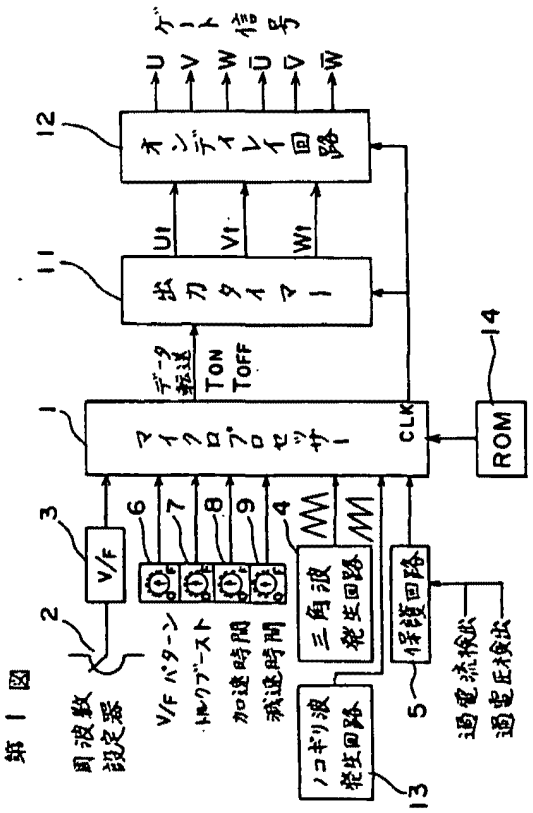
24…ノコギリ波、　Ton…パルスオン期間、

Toff…パルスオフ期間、　Tc…変調波周期。

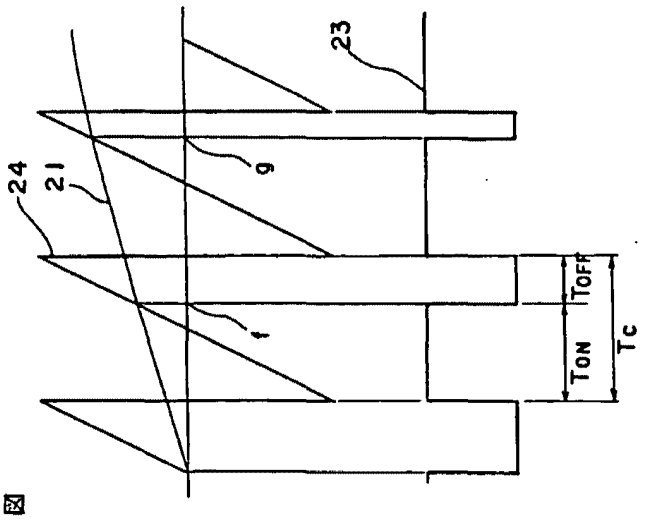
特許出願人　富士電機株式会社

代　理　人　弁理士　青山　葆　外2名

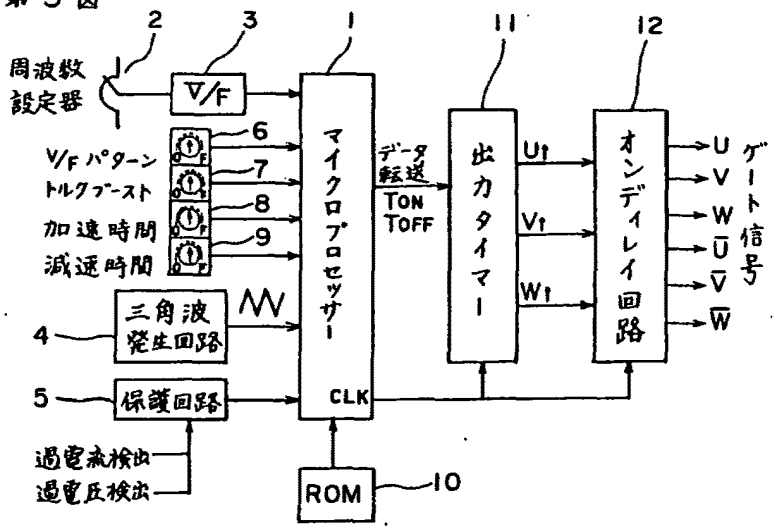
第1図



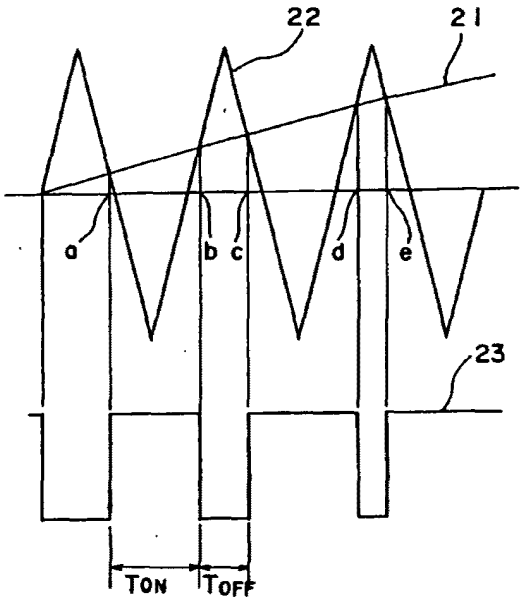
第2図



第３図



第４図



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㊹発明の名称　放送電波の中継監視装置

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㉒出　願　平2(1990)10月17日

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明　細　書

1．発明の名称　放送電波の中継監視装置

2．特許請求の範囲

1．受信した放送電波を復調する受信手段と、該受信手段によって復調されたアナログ信号をデジタル変換する変換手段と、該変換手段が変換したデジタル信号に変調をかけ、有線又は無線方式により外部へ送信する送信手段とを具備することを特徴とする放送電波の中継監視装置。

2．前記放送電波はテレビ電波であり、前記変換手段は該テレビ電波に含まれる信号のうち、少なくとも映像信号をデジタル変換することを特徴とする請求項1記載の放送電波の中継監視装置。

3．前記送信手段は、前記変換手段によってデジタル信号化された前記映像信号を所定のタイミングで静止画像信号として送信することを特徴とする請求項2記載の放送電波の中継監視装置。

3．発明の詳細な説明

(産業上の利用分野)

本発明は放送電波の中継監視装置に関する。

(従来の技術)

放送電波、特にテレビ電波のように到達距離の短い電波の場合、送信出力や地形等の関係で難視聴地域の存在は免れ得ない。この問題を解決するため放送各社は中継局(サテライト局)を置局し、サービスエリアの拡大・確保を図っている。サテライト局は、無人でしかも交通不便な山頂に設置されることが多く、サテライト局の送信電波の監視に種々の方式が提案されて来た。従来の方式について第6図と共に説明する。

第1の方式はサテライト局100のサービスエリア102内に設けられた委託監視所104へ監視中枢である本局106から電話で問い合わせ、サテライト局100の放送電波をテレビで受信してもらい、事故の有無、画質、音質について答えてもらうという方式である。

第2の方式は本発明の出願人が開発し、実用化

したもので、サテライト局１００のサテライト放送機１０８の故障接点情報をＶＨＦ無線電話の電波１１０で、送信所１１２へ一旦送る。この送信所１１２はサテライト局１００が放送する信号をサテライト局１００へ送信するために設置されている。一旦送信所１１２へ送られた故障接点情報は本局１０６と送信所１１２を結ぶマイクロ回線１１４を介して本局１０６へ送られ監視用データとして中枢監視装置１１６へ供される方式である。

さらに、第３の方式としてサテライト局１００と本局１０６との間を通信回線（電話回線）で直接接続し、サテライト放送機１０８の故障接点情報を直接本局１０６の中枢監視装置１１６へ送り監視用データとする方式である。

（発明が解決しようとする課題）

しかしながら、上記の従来のサテライト局の電波の監視方式には次のような課題が有る。

第１の方式においては委託監視者が専門家でない場合がほとんどであり詳細な監視データの収集ができない。また、深夜、早朝、委託監視者の外出中等には本局から問い合わせが難しかったり、不可能であったりするため常時監視体制がとれない。

第２の方式においては、送信所又は本局と無線電話回線が確保可能なサテライト局に限られてしまう。送信所に対して孫局に相当するサテライト局においては採用することができない。また、故障接点情報はあくまでサテライト機器の一定の機能について、一定の故障状態を示すのみであり、例えば画質についての細かい異常についてのデータを検出することはできない。

第３の方式は、第２の方式における全てのサテライト局に採用できないという問題点は解消し得るものの、サテライト機器の故障接点情報を本局へ送る点では同じである。従って、やはり細かい異常についてのデータを検出することはできない。

従って、本発明はサテライト局の放送電波を常時監視可能であって、当該放送電波の状態を詳細に監視可能な放送電波の中継監視装置を提供することを目的とする。

（課題を解決するための手段）

上記課題を解決するため、本発明は次の構成を備える。

すなわち、受信した放送電波を復調する受信手段と、該受信手段によって復調されたアナログ信号をデジタル変換する変換手段と、該変換手段が変換したデジタル信号に変調をかけ、有線又は無線方式により外部へ送信する送信手段とを具備することを特徴とする。特にテレビ用サテライト局の場合、前記放送電波はテレビ電波であり、前記変換手段は該テレビ電波に含まれる信号のうち、少なくとも映像信号をデジタル変換するようにしてもよい。さらにテレビ用サテライト局の場合は、前記送信手段は、前記変換手段によってデジタル信号化された前記映像信号を所定のタイミングで静止画像信号として送信するようにしてもよい。

（作用）

作用について説明する。

受信手段が受信した放送電波を復調し、復調したアナログ信号をデジタル変換した後、送信手段を介して外部へ送付するため、外部に設けられた監視施設において受信手段が受信した放送電波の状態を直接知ることができる。特に、テレビ電波の場合は受信手段が受信した画像の状態を知ることが可能となるため詳細な状況や画質も監視可能となる。

（実施例）

以下、本発明の好適な実施例について添付図面と共に詳述する。本実施例においてはサテライト局１００のテレビ放送電波を委託監視所１０４に設置した本発明に係る中継監視装置で監視用データを作成し、通信回線（有線電話回線）を介して本局１０６に設けられた中枢監視装置１１６へ前記監視用データを送る例を挙げて説明する（第６図参照）。

第１図にはサテライト局１００の構成を示す。サテライト局１００にはサテライト放送機１０８と、故障接点情報監視装置１０が設置されている。サテライト放送機１０８はテレビ放送電波１２をアンテナ１４から放送する。状態変化接点情報監

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視装置１０はサテライト放送機１０８に設けられている、故障時にＯＮ又はＯＦＦとなる接点１６・・・の状態を検出する装置である。なお本実施例においては接点１６・・・は１６個設けられており、１６種類の、異常を含む状態変化を検知可能になっている。状態変化接点情報監視装置１０はＣＰＵ１８に監視されたデータ変換部２０とＶＨＦ送信部２２とから成り、サテライト放送機１０８の１６個の状態変化接点１６・・・の状況をデータ変換部２０で例えば１６種類のオーディオ信号に変換し、ＶＨＦ送信部２２で変調をかけアンテナ２４からＶＨＦ電波２６として送信する。なおＶＨＦ送信部２２は状態変化接点情報監視装置１０が接点１６・・・の異常を送ってきた時、及び本局１０６から問い合わせがあった時にＶＨＦ電波２６を自動的に送信するようになっている。

次に第２図と共にサービスエリア１０２内の委託監視所１０４に設けられている中継監視装置２８について説明する。

３０はＶＨＦ受信部であり、ＶＨＦ電波２６をアンテナ３２で受信して復調する。

３４は第１の送信部であり、ＶＨＦ受信部３０で復調された状態変化接点情報を示す信号を有線方式の通信（電話）回線３６へ送り出すために変調をかけ、出力する。第１の送信部３４はＶＨＦ受信部３０が状態変化接点情報を受信したらネットワークコントロールユニット３８へ送信を知らせる信号を送り、加入電話４０及び後述する第２の送信部の通信回線３６への接続を不能にしてデジタル信号化した状態変化接点情報をモデム４２に送り、通信回線３６を介して本局１０６へ送る。

４４は受信手段であるチューナであり、アンテナ４６で受信したテレビ放送電波１２をアナログの映像信号と音声信号に復調する。

４８は変換手段及び送信手段である第２の送信部であり、静止画（スロースキャンテレビ）伝送機が含まれている。第２の送信部４８はチューナ４４で復調された音声信号をリアルタイムで、通信回線３６へ送り出すために変調をかけて出力する。一方、チューナ４４で復調された映像信号は第２の送信部４８の静止画像伝送機によって所定のタイミングの静止画像信号に変換される。この静止画像信号への変換について第４図（静止画像伝送機のブロックダイアグラム）と共に説明する。

第４図において、チューナ４４で復調された映像信号はＮＴＳＣ方式でＲＧＢデコータ５０へ送られデコードされる。ＲＧＢデコーダ５０でデコードされたカラーを示すパラレル信号はＲＧＢマルチプレクサ５２でシリアル化され、Ａ／Ｄコンバータ５４でデジタル変換され、１ライン２５６ドットのカラーデータが各カラーメモリ５６、５８、６０へ記憶される。この制御はＣＰＵ６２がタイミングジェネレータ６４の出力を検出することにより所定のタイミングで行うことができる。静止画像信号を通信回線３６へ送り出すためにはＣＰＵ６２は各カラーメモリ５６、５８、６０のデータを読出してシリアル化し、ＦＭジェネレータ６６でＳＣＦＭ変調をかけて出力し、ネットワークコントロールユニット３８及びモデム４２を介して通信回線３６へ送り出される。

再び第２図において、６８はＣＰＵであり、第１の送信部３４及び第２の送信部４８の動作を制御する。

ネットワークコントロールユニット３８は第１の送信部３４、加入電話４０、又は第２の送信部４８の通信回線３６への接続を制御すると共に、通信回線３６を介して送られてくる信号の識別等も行う。

続いて第３図と共に本局１０６に設置されている中枢監視装置７０について説明する。

７２は静止画像受信部であり、通信回線３６及びモデム７４を介して中継監視装置２８から送られてくるＳＣＦＭの静止画像信号を受信して復調する。

７６はＲＧＢモニタであり、静止画像受信部７２が復調した静止画像を表示する。静止画像を表示するための構成を第５図に示す。

中継監視装置２８から送られたＳＣＦＭ変調をかけた静止画映像信号は検波部７８でデジタル信号に検波され、ＣＰＵ８０が１ライン２５６ドッ

トのカラーデータを各カラーメモリ８２、８４、８６に書き込む。ＲＧＢモニタ７６へ画像表示を行うためにはＣＰＵ８０がタイミングジェネレータ８８の指示する所定のタイミングでカラーデータをカラーメモリ８２、８４、８６から１ライン２５６ドット（計２４０ライン）のデータとして読み出し、Ｄ／Ａコンバータ９０でアナログ変換してＲＧＢモニタ７６のカラー端子へ入力して静止画像が表示される。

再び第３図において、９１は音声モニタであり、中継監視装置２８からリアルタイムで送られてくる音声信号を静止画像受信部７２で音声信号に変換して出力する。

９２は画像プリンタであり、ＲＧＢモニタ７６へ出力されている静止画像のハードコピーを出力するために設けられている。ハードコピーは例えばビート、ゴースト等の障害の際の参考データとなる。

９３はパーソナルコンピュータのＣＰＵであり、通信回線３６及びモデム７４を介して中継監視装置２８より送られてくる状態変化接点情報を処理してサテライト局名、状態変化発生日時、状態変化内容等をディスプレイ９４に表示したり、プリンタ９５に印字出力する。また、本局１０６のオペレータがサテライト局１００の状態変化接点情報、映像信号又は音声信号を任意の時間に監視したい場合はキーボード９６から監視項目を指定するとＣＰＵ９３が自動的に通信回線３６を指定したサテライト局１００の中継監視装置２８へ接続し、指定された監視項目の情報（状態変化接点情報、静止画像情報、リアルタイム音声情報）をディスプレイ９４、プリンタ９５、ＲＧＢモニタ７６、画像プリンタ９２又は音声モニタ９１へ出力させる。

なお、９７はネットワークコントロールユニットであり、信号を識別して通信回線３６の接続を加入電話９８と静止画像受信部７２との間で切換える。

次に、上記のように構成された監視システムの動作について説明する。

本局１０６のオペレータがサテライト局１００のテレビ電波１２等の状況を監視したい場合、オペレータはキーボード９６から監視しようとするサテライト局１００の識別と、画像状況と、音声状況を監視する旨（監視項目）を入力する。

するとＣＰＵ９３はモデム７４を介して指定したサテライト局１００の中継監視装置２８へ通信回線３６を接続する。中継監視装置２８のネットワークコントロールユニット３８は指定された監視項目により第２の送信部４８を通信回線３６へ接続する。ＣＰＵ６８に制御された第２の送信部４８はチューナ４４からの信号をデジタルの静止画像信号に変換し、また音声信号はリアルタイムのデジタル信号として通信回線３６を介して中枢監視装置７０へ送る。

中枢監視装置７０のネットワークコントロールユニット９７は静止画像信号と音声信号が送られてきたことを判断したら通信回線３６を静止画像受信部７２へ接続し、前述の如く出力する。

一方、オペレータがサテライト局１００の状態変化接点情報を入手したい場合はキーボード９６から監視項目を「状態変化接点情報」と入力してやると、中継監視装置２８のネットワークコントロールユニット３８が第１の送信部３４の出力を送信可能にするので、状態変化接点情報が中枢監視装置７０へ通信回線３６を介して送られ、ＣＰＵ９３が情報処理を行ってディスプレイ９４及び／又はプリンタ９５へ状態変化接点情報を出力する。

上記実施例において、中継監視装置２８が受信したサテライト局１００の画像信号をスロースキャンテレビ技術を利用して静止画像信号に変換して本局１０６の中枢監視装置７０のＲＧＢモニタ７６に静止画像として出力したのはリアルタイムの画像信号を処理する場合と比較して装置に要する経費をかなり低く抑えることができるためであり、経費面で問題ない場合は画像信号も中枢監視装置７０へ音声と同時にリアルタイムで送信してもよい。

また、中継監視装置２８から本局１０６への送

信は通信回線３６の他、無線通信手段でもよいし、中継監視装置２８と本局１０６との間に中継局を介在させてもよい。

さらに、監視するサテライト局はテレビ電波の放送施設に限らずラジオやビーコン等の映像信号以外の放送信号の監視に使用することもできる。

以上、本発明の好適な実施例について種々述べて来たが、本発明は上述の実施例に限定されるのではなく、例えば状態変化接点信号情報は送信しなくてよいし、中継監視装置と中枢監視装置との間は双方向通信方式ではなく、中継監視装置から中枢監視装置への単方向通信方式でもよい等、発明の精神を逸脱しない範囲で多くの改変を施し得るのはもちろんである。

（発明の効果）

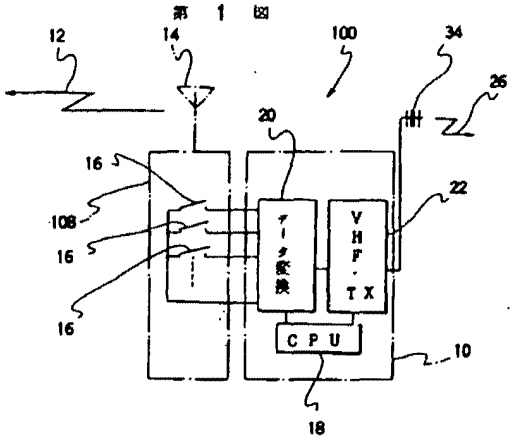
本発明に係る放送電波の中継監視装置を用いると、本局において直接放送電波の状態を知ることができるため、委託監視では不可能であった詳細な監視データを収集できると共に、専門家の的確な判断が可能となる。特にテレビ電波の場合は画質についての細かいデータの検出も可能となる。さらに、テレビ電波の監視において画像信号の監視を静止画像信号に基づいて行うと、リアルタイムの画像信号を扱う場合と比較して装置を極めて安価に構成することが可能となる等の著効を奏する。

４．図面の簡単な説明

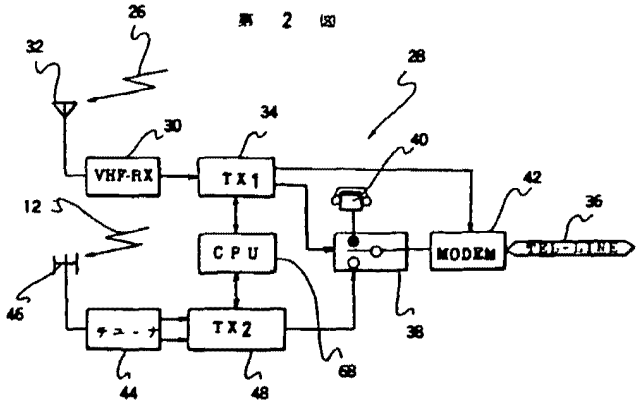
第１図はサテライト局の構成の概要を示したブロックダイアグラム、第２図は実施例の中継監視装置のブロックダイアグラム、第３図は中枢監視装置のブロックダイアグラム、第４図は中継監視装置の第２の送信部のブロックダイアグラム、第５図は中枢監視装置の静止画像受信部のブロックダイアグラム、第６図は従来のサテライト局の放送電波の監視システムを示した説明図。

１２・・・テレビ電波、　２８・・・中継監視装置、　３６・・・通信回線、
４４・・・チューナ、　４８・・・第２の送信部、
１００・・・サテライト局。

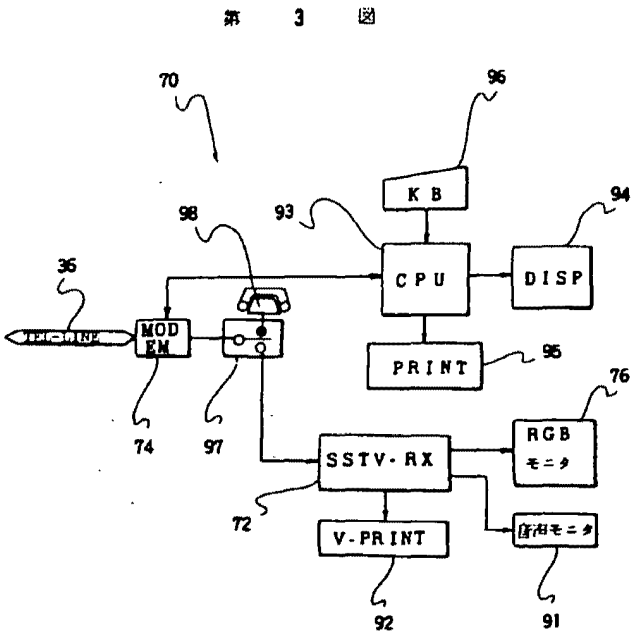
第１図



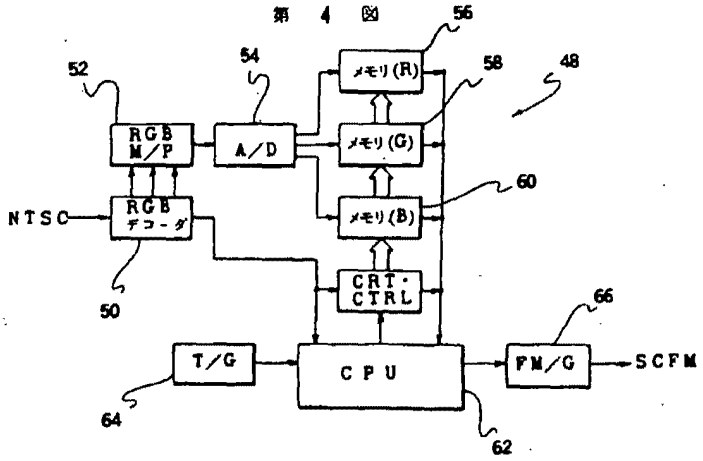
第２図



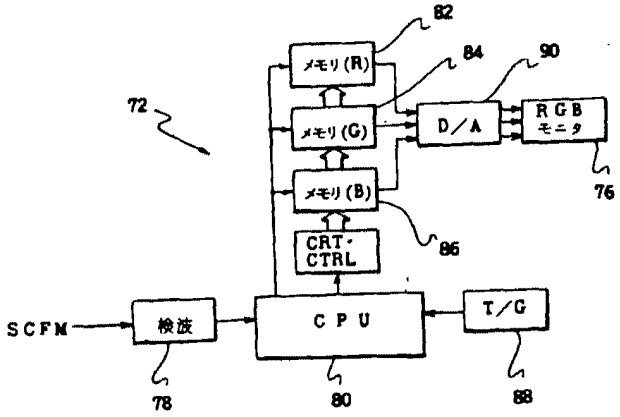
第３図



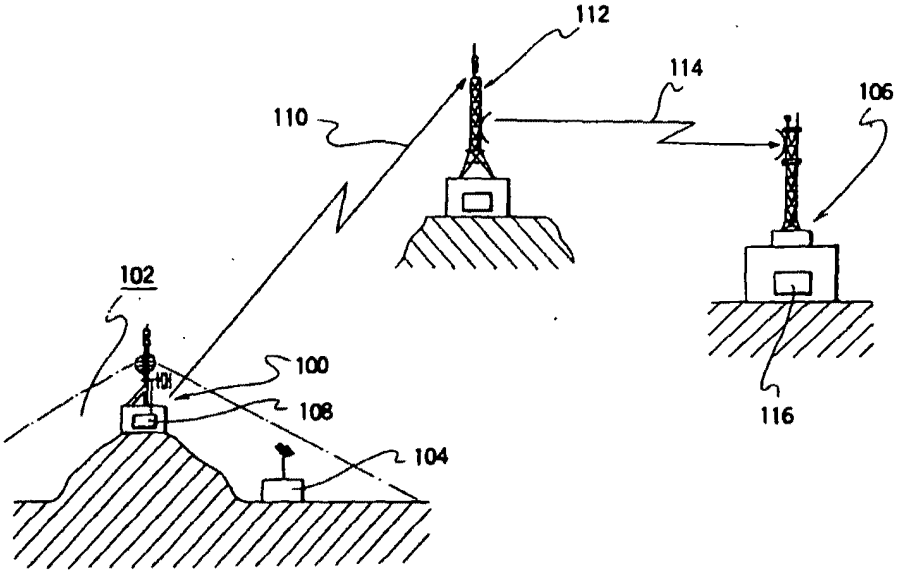
第 4 図


52
54
56
58
48
RGB M/P
A/D
メモリ(R)
メモリ(G)
メモリ(B)
NTSC
RGB デコーダ
60
50
CRT・CTRL
66
T/G
CPU
FM/G
SCFM
64
62

第 5 図


82
84
90
72
メモリ(R)
メモリ(G)
メモリ(B)
D/A
RGB モニタ
76
CRT・CTRL
86
SCFM
検波
CPU
T/G
78
80
88

第 6 図


112
114
106
110
102
100
108
104
116

IDS Doc. Ref. AJ25
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(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（A）　(11)特許出願公開番号

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Ｈ０４Ｂ	1/40		8949－5K		
	1/04	Ｆ	2116－5K		
	1/26	Ｂ			

審査請求　未請求　発明の数３　ＯＬ　（全３頁）

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(31)優先権主張番号　９３００２８０：６

(32)優先日　1993年１月８日

(33)優先権主張国　イギリス（ＧＢ）

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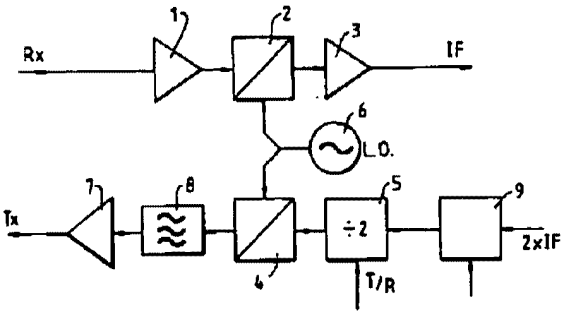
(74)代理人　弁理士　中村　稔　（外６名）

(54)【発明の名称】　送／受信装置

(57)【要約】　（修正有）

【構成】　半二重送／受信装置であって、受信信号は増幅のためにＩＦ周波数にダウン変換され、送信のための信号はＩＦ周波数の２倍の周波数でキャリア上に変調され、このキャリアは、送信が発生するときにアップ変換のために周波数分割のみなされる。

【効果】　受信信号のダウン変換と送信すべき中間周波数信号のアップ変換には、共通の局部発振器を利用することができ、受信モードでは周波数分割器をはたらかせないようにすることにより、ＩＦ信号が送信経路に生成されないようにし、また、送信経路からの干渉なしにＩＦ増幅がなされる。送信モードにおいては、周波数分割器が中間周波数で信号を生成している間、受信経路を無効とすることができる。



1

【特許請求の範囲】

【請求項1】　増幅を行うために受信信号を周波数に関して中間周波数にダウン変換し、送信すべき中間周波数信号を周波数に関して送信前にアップ変換するような送／受信装置において、前記送信すべき情報信号は、前記中間周波数の多重である周波数のキャリア信号上に変調されるようにされており、前記変調キャリアはアップ変換を行う前に前記多重によってその周波数が分割されるようにされていることを特徴とする送／受信装置。

【請求項2】　請求項1記載の送／受信装置において、前記受信信号のダウン変換と送信すべき中間周波数信号のアップ変換は共通の局部発振器を利用する送／受信装置。

【請求項3】　受信信号を中間周波数にダウン変換するための第1のミキサ手段と、送信のために信号を前記中間周波数にアップ変換するための第2のミキサ手段と、送信すべき情報信号を前記中間周波数の多重であるような周波数のキャリア信号上に変調するための手段と、前記変調キャリア信号を前記多重によって選択的に周波数分割して前記第2のミキサ手段に前記中間周波数で付与する手段と、を備える。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は送／受信装置に関するが、特にマイクロ波送／受信装置、若しくはトランシーバ装置に限定するものではない。

【0002】

【発明の概要】本発明の1つの特徴によれば、増幅を行うために受信信号を周波数に関して中間周波数にダウン変換し、送信すべき中間周波数信号を周波数に関して送信前にアップ変換するような送／受信装置において、前記送信すべき情報信号は、前記中間周波数の多重であるような周波数のキャリア信号上に変調されるようにされており、前記変調キャリアはアップ変換を行う前に前記多重によってその周波数が分割されるようにされている。受信信号のダウン変換と送信すべき中間周波数信号のアップ変換には、共通の局部発振器を利用することができる。本発明の他の特徴によれば、送／受信装置は、受信信号を中間周波数にダウン変換するための第1のミキサ手段と、送信のために信号を前記中間周波数にアップ変換するための第2のミキサ手段と、送信すべき情報

2

信号を前記中間周波数の多重であるような周波数のキャリア信号上に変調するための手段と、前記変調キャリア信号を前記多重によって選択的に周波数分割して前記第2のミキサ手段に前記中間周波数で付与する手段と、を備える。

【0003】

【実施例】本発明の送／受信装置を該送信／受信装置の一部を示した添付図面を参照しつつ以下に述べる。図から明かなように、受信信号は、ＲＦ増幅器1によって第1のミキサ、即ちダウン変換器2へ付与され、ここから、中間周波数にある信号がＩＦ増幅器3によって装置の出力回路（図示していない）に付与される。送信すべき情報信号は、変調器9で、中間周波数の2倍の周波数でキャリア信号上に変調される。この変調キャリア信号は、スイッチ切換可能な2分割周波数分割器5によって第2のミキサ、即ちアップ変換器4に付与される。ミキサ2および4は共通の局部発振器6を利用する。送信のためのアップ変換信号がバンドパスフィルタ8によってＲＦ増幅器7に付与される。この装置は半二重で動作するものであって、受信モードでは、周波数分割器5をバイアス解除し若しくはエネルギー供給されないようにして、ＩＦにおける信号が送信経路に生成されないようにし、また、送信経路からの干渉なしにＩＦ増幅器3によって受信信号がダウン変換され且つ増幅されるようになっており、2×ＩＦにあるいずれの信号も増幅器3と関連するＩＦフィルタによって拒否される。送信モードにおいて周波数分割器4が中間周波数で信号を生成しているときは、受信経路は無効とされてもよい（図示していない）。

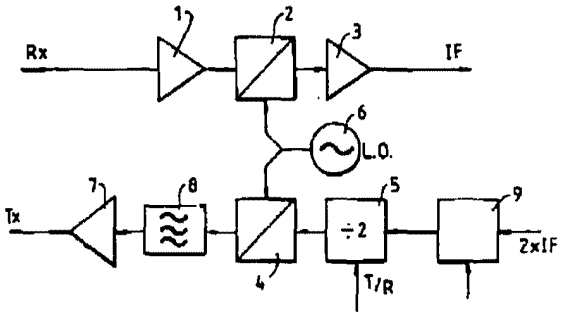
【図面の簡単な説明】

【図1】本発明による送信／受信装置の一部を示す図。

【符号の説明】

1　第1のミキサ
2　ダウン変換器
3　ＩＦ増幅器
4　第2のミキサ
5　2分割周波数分割器
6　局部発振器
7　ＲＦ増幅器
8　バンドパスフィルタ
9　変調器

【図1】



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(43)公開日　平成10年(1998)４月14日

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Ａ０１Ｂ　69/00	３０３	Ａ０１Ｂ　69/00	３０３Ｋ

審査請求　未請求　請求項の数６　ＯＬ　（全９頁）

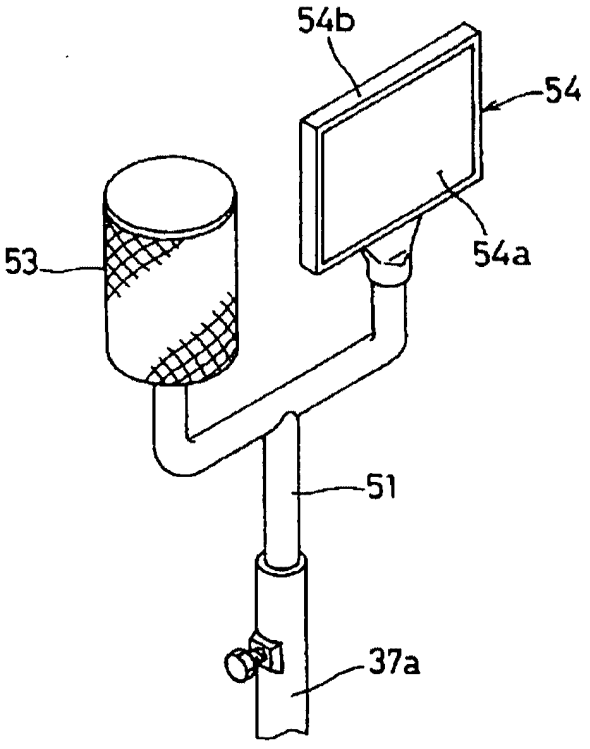
(21)出願番号　特願平8－251073

(22)出願日　平成８年(1996)９月24日

(71)出願人　000001052
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兵庫県尼崎市浜１丁目１番１号　株式会社クボタ技術開発研究所内
(74)代理人　弁理士　北村　修　（外１名）

(54)【発明の名称】　測距装置

(57)【要約】
【課題】　測距装置において測距精度の向上と測定時間の短縮を図る。
【解決手段】　測距装置に、測距対象に向けてパルス状の光線を投射する第１測距用光源ＦＬと、測距対象に向けて設定周期の基準信号にて変調された光線を投射する第２測距用光源ＳＬと、前記測距対象からの反射光を検出する受光手段６２と、第１測距用光源ＦＬから前記パルス状の光線を投射した後、前記測距対象にて反射された反射光を前記受光手段６２が検出するまでの時間を計測する計時手段６９と、第２測距用光源ＳＬから出射して、前記測距対象にて反射された反射光による受光手段６２の検出信号と、前記基準信号との位相差を検出する位相差検出手段ＦＤと、計時手段６９の計時情報から求めた前記測距対象までの絶対的な距離情報と、位相差検出手段ＦＤの検出情報から求めた距離情報とによって、前記測距対象までの距離を演算する距離演算手段ＤＤが設けられている。



【特許請求の範囲】
【請求項１】　測距対象に向けてパルス状の光線を投射する第１測距用光源（ＦＬ）と、
測距対象に向けて設定周期の基準信号にて変調された光線を投射する第２測距用光源（ＳＬ）と、
前記測距対象からの反射光を検出する受光手段（６２）と、
前記第１測距用光源（ＦＬ）から前記パルス状の光線を投射した後、前記測距対象にて反射された反射光を前記受光手段（６２）が検出するまでの時間を計測する計時手段（６９）と、
前記第２測距用光源（ＳＬ）から出射して、前記測距対象にて反射された反射光による前記受光手段（６２）の検出信号と、前記基準信号との位相差を検出する位相差検出手段（ＦＤ）と、
前記計時手段（６９）の計時情報から求めた前記測距対象までの絶対的な距離情報と、前記位相差検出手段（ＦＤ）の検出情報から求めた距離情報とによって、前記測距対象までの距離を演算する距離演算手段（ＤＤ）が設けられた測距装置。
【請求項２】　前記位相差検出手段（ＦＤ）は、ヘテロダイン検波により前記位相差を検出するように構成されている請求項１記載の測距装置。
【請求項３】　前記第１測距用光源（ＦＬ）と前記第２測距用光源（ＳＬ）とが、強度変調可能な単一の発光装置（６０）を備えて兼用構成され、
前記発光装置（６０）に対して、パルス状の信号と前記基準信号とによって、前記パルス状の信号による変調強度が大となる状態で強度変調をかける変調装置（ＡＭ）が備えられている請求項１又は２記載の測距装置。
【請求項４】　前記変調装置（ＡＭ）は、前記パルス状の信号を、予定する最大測定距離離れて位置する前記測距対象までの光の往復時間よりも長い時間幅で繰り返す周期信号としている請求項３記載の測距装置。
【請求項５】　前記変調装置（ＡＭ）は、前記パルス状の信号と前記基準信号とを同期させた状態で、前記発光装置（６０）に変調をかけるように構成されている請求項３又は４記載の測距装置。
【請求項６】　前記発光装置（６０）は、半導体レーザ素子（ＬＤ）にて構成されている請求項３～５のいずれか１項に記載の測距装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、測距対象に向けて光線を投射し、測距対象からの反射光を検出して、測距対象までの距離を検出する測距装置に関する。
【０００２】
【従来の技術】かかる測距装置としては、従来、測距対象に向けて光線を投射してから、その光線が測距対象で反射して戻ってくるまでの時間を測定し、その時間と光の速さとから測距対象までの距離を求める方式（以下、「ＴＯＦ方式」と略記する）と、測距対象に向けて一定周波数の信号で変調した光線を投射して、測距対象で反射して戻ってきた光線を検出し、その検出信号と上記一定周波数の信号との位相差から測距対象までの距離を求める方式（以下、「位相比較方式」と略記する）とが考えられている。
【０００３】位相比較方式の場合では、位相差が０～２π（１周期）の範囲でしか検出できないことから、原則として測定対象までの往復距離が上記変調周波数の１周期に対応する距離以内に制限される。つまり、測距対象までの距離Ｄは、第２測距用光源での変調信号の波長をλとすると、
Ｄ＝（ｎ×λ＋φ）／２　（ｎは０以上の整数）
と表されるが、位相比較方式で求まるのは、上式のうちの位相差に対応する距離φのみであるので、原則としてｎ＝０すなわち最大でλ／２の範囲に制限される。この範囲を超えて測距を行う場合は、従来、λを複数に変化させて、夫々φを測定し、その測定結果から整数ｎを特定して、距離Ｄを求めていた。
【０００４】
【発明が解決しようとする課題】しかしながら、上記従来構成では、ＴＯＦ方式の場合では、時間の測定精度のわりに光の速さが速いことから、測距精度が低くなってしまう不都合があり、位相比較方式の場合では、測定精度は高いものの、原則として測距範囲に制限を受け、その制限を超えて測距するときは、測定条件を複数に変化させて必要があり、測定時間が長くなる不都合があった。本発明は、上記実情に鑑みてなされたものであって、その目的は、可及的に測距精度の向上と測定時間の短縮を図る点にある。
【０００５】
【課題を解決するための手段】上記請求項１記載の構成を備えることにより、第１測距用光源から投射されたパルス状の光線は、測距対象にて反射されて受光手段に入射する。上記パルス状の光線が第１測距用光源から投射されてから、受光手段に入射して検出されるまでの時間は、計時手段にて計測されている。一方、第２測距用光源からは、設定周期の基準信号にて変調された光線が測距対象に向けて照射され、測距対象で反射して受光手段に入射する。この受光手段の検出信号は、位相差検出手段によって、上記基準信号との位相差が検出される。
【０００６】計時手段の計測情報と光の速さとからは、測距対象までの絶対的な距離情報が求まり、位相差検出手段の検出情報からは、基準信号の１周期に対応する距離内での距離情報（厳密には往復距離情報）が求まる。距離演算手段は、これらの距離情報から測距対象までの距離を演算する。つまり、測距対象までの距離Ｄは、位相差検出手段が検出する位相差に対応する距離をϕ_1、投射された光線における基準信号の繰り返し信号間の距

離（波長に対応）をλ_1とすると、

$D=(n_1\times\lambda_1+\phi_1)/2$　　(1) 式

と表されるが、この(1) 式のＤに、計時手段の計測情報（ｔ）と光の速さ（ｃ）とから求めた測距対象までの絶対的な距離情報Ｄ'（＝ｔ×ｃ／２）を代入することでn_1を特定でき、測距対象までの距離Ｄが求まる。

【０００７】従って、計時手段の計測情報から求めた絶対的な距離情報に多少の誤差があっても、n_1の特定に影響するほどの誤差とならないように設定しておけば、距離ϕ_1の測定精度が良いことから、距離Ｄを精度良く求めることができる。もって、計時手段の計測情報から求めた絶対的な距離情報及び位相差検出手段の検出情報から求めた距離情報夫々の特質を生かしながら結合することによって、可及的に測距精度の向上と測定時間の短縮を図れる測距装置を提供するに至った。

【０００８】又、上記請求項２記載の構成を備えることにより、位相差検出手段は、ヘテロダイン検波により、受光手段の検出信号と上記基準信号との位相差を検出する。測距分解能を向上するには、基準信号の周波数を高くすれば良いが、一般に、周波数を高くするほど位相差検出手段による位相差の検出が困難となるので、ヘテロダイン検波によって位相差の検出の対象となる信号の周波数を下げることで、位相差検出手段による位相差の検出を容易に行える。

【０００９】又、上記請求項３記載の構成を備えることにより、第１測距用光源と第２測距用光源とが、強度変調可能な単一の発光装置を備えて兼用構成されているので、装置構成の小型化及び簡素化を図れると共に、第１測距用光源及び第２測距用光源の光路が単一となるので、測距装置の取り付け調整等も容易となる。尚、第１測距用光源の機能に対応するパルス状の信号は、変調装置によって、第２測距用光源の機能に対応する基準信号よりも変調強度が大となる状態で強度変調されるので、単一の発光装置にて第１測距用光源及び第２測距用光源の機能を兼ね備えさせても、的確に計時手段による計時及び位相差検出手段により位相差の検出を行える。

【００１０】又、上記請求項４記載の構成を備えることにより、変調装置は、第１測距用光源の機能に対応するパルス状の信号を、予定する最大測定距離離れて位置する測距対象までの光の往復時間よりも長い時間幅で繰り返す周期信号としているので、絶対的な距離情報を繰り返し求めることができ、多数のデータを利用して精度向上を図れる。

【００１１】又、上記請求項５記載の構成を備えることにより、第１測距用光源の機能に対応するパルス状の信号と、第２測距用光源の機能に対応する基準信号とが同期しが状態で、発光装置に変調がかけられるので、測距対象からの反射光を検出した受光手段の検出信号において、上記のパルス状の信号に対応する成分と基準信号に対応する成分とを分離したときに、非同期で混合されているものに較べて分離後の信号を滑らかなものにし易く、測定精度の向上に寄与する。又、上記請求項６記載の構成を備えることにより、発光装置として半導体レーザ素子が備えられる。半導体レーザ素子は、注入電流により容易に強度変調をかけることができるので取扱いが容易であり、又、出射光に指向性があるので、測距用光源に好適である。

【００１２】

【発明の実施の形態】以下、本発明の実施の形態を、耕耘装置６を取り付けた農用トラクターＶ（以後、作業車Ｖという）が、圃場Ｆ内に設けた複数個の作業行程Ｌに沿って自動走行しながら、耕耘作業等を行うときの、作業車Ｖの測位に適用した場合について説明する。

【００１３】圃場Ｆの外側には、図２及び図５に示すように、レーザ測位装置４０が、水平面内における位置が判っている地上側の設定基準位置に設置されている。レーザ測位装置４０は、作業車Ｖまでの距離を測定すると共に、レーザ測位装置４０に対する作業車Ｖの存在方位を測定して、作業車Ｖの存在位置を測定するものであり、このため、ビーム光を水平方向に回転走査自在に構成され、そのビーム光が作業車Ｖに備えられた回帰反射体５３にて反射されて戻ってきた光を検出して、作業車Ｖまでの距離とビーム光が反射してきたときのビーム光の走査角とから、作業車Ｖの位置測定を行う。

【００１４】回帰反射体５３は、いわゆるコーナーキューブの反射面に相当するものを円筒の周面に多数配列したものであり、ビーム光が飛来して来た方向にそのビーム光を反射する。回帰反射体５３は、後述する受光器５４と共に二股状の支持アーム５１に取り付けられ、支持アーム５１は、図２等に示すように、耕耘装置６側に取り付けられている支持筒３７ａに内嵌状態で支持されネジ止め固定される。

【００１５】レーザ測位装置４０には、図４（イ）に示すように、半導体レーザ素子ＬＤにて構成される発光装置６０と、発光装置６０の出射光を平行光にするコリメートレンズ６１と、作業車Ｖからの反射光を検出する受光手段としての受光素子６２と、作業車Ｖからの反射光を受光素子６２に導くビームスプリッタ６３と、発光装置６０の出射光の向きを９０度偏向して水平方向に投射させ且つ図示しないモータによって縦軸芯周りに回動駆動される反射鏡６４と、その反射鏡６４の回転角を検出するロータリエンコーダ６５とが設けられており、反射鏡６４を回転駆動することによって、発光装置６０の出射光を水平方向に回転走査自在としている。

【００１６】この他、レーザ測位装置４０には、図４（イ）に示す発光装置６０の駆動回路及び受光素子６２の検出信号の信号処理回路等が備えられている。以下、これらの回路の作動について説明する。発光装置６０は、図４（ロ）に示すように、第１発振回路６６による数百ＭＨｚ程度の正弦波信号（同図（ロ）において

「Ａ」で示す）と、パルス発振回路６７による数μｓ～十数μｓ程度の繰り返し周期のパルス信号（同図（ロ）において「Ｂ」で示す）とが足し合わされた信号で駆動され、この結果、発光装置６０の出射光は図４（ロ）に示す信号で強度変調されることになる。この第１発振器６６の正弦波信号は、発光装置６０を変調するための設定周期に基準信号となる。従って、第１発振器６６及びパルス発振器６７は、発光装置６０を強度変調する変調装置ＡＭとして機能する。

【００１７】尚、パルス発振器６７のパルス信号のピーク値は、第１発振回路６６の正弦波信号の振幅より十分大きく、パルス信号による変調強度が正弦波信号による変調強度より大としてある。又、パルス発振器６７は、第１発振器６６からの同期信号によってパルス発振するので、図４（ロ）に示すようにパルス信号と正弦波信号の同期がとれており、パルス信号の信号幅を正弦波の周期に一致させてあるので、両信号が滑らかにつながっている。

【００１８】受光素子６２の検出信号は、図４（ロ）に示す信号に対して作業車Ｖまでの距離に応じて位相が異なる信号となっており、以下に説明する２系統で処理される。一方の処理系統は、比較信号レベルが正弦波信号のレベルより高い値に設定してあるコンパレータ６８に入力されて、パルス信号のみが検出され、計時手段としてのタイマ６９に入力される。このタイマ６９には、パルス発振器６７の出力信号も入力され、タイマ６９は、パルス発振器６７からパルス信号が入力されると共に計時を開始し、コンパレータ６８からパルス信号が入力されるまでの計時時間ｔを演算装置７０へ出力する。上記パルス信号の繰り返し周期は、作業車Ｖまでの距離として想定している最大距離を光が往復する時間より長くなるように設定してあるので、演算装置７０は、上記の計時時間から、上述の如く絶対的な距離情報Ｄ’（＝ｔ×ｃ／２）を求める（ｃは光の速さ）。

【００１９】他方の処理系統は、正弦波信号のレベルよりわずかに高い信号レベルを最大信号範囲とするアンプ７１に入力され、パルス信号がクランプされた状態で出力される。アンプ７１の出力信号は、第１発振器６７と数ＭＨｚ～十数ＭＨｚ程度発振周波数が異なる正弦波信号を発振する第２発振器７２の出力信号と混合され、その結果生じたビート信号がコンパレータ７３にて矩形波に変換されて、タイマ７４に入力される。タイマ７４には、第１発振器６６の出力信号と第２発振器７２の出力信号を混合して生じたビート信号をコンパレータ７５にて矩形波に変換した信号も入力されており、タイマ７４は、コンパレータ７５からパルス信号が入力されると共に計時を開始し、コンパレータ７３からパルス信号が入力されるまでの計時時間Ｔを演算装置７０へ出力する。すなわち、第２発振器７２、コンパレータ７３，７５及びタイマ７４を主要部として、受光素子６２の検出信号と第１発振器６６の出力信号（基準信号）との位相差を、ヘテロダイン検波により検出する位相差検出手段ＦＤが構成されている。

【００２０】演算装置７０は、この計時時間Ｔから、第１発振器６６の正弦波と、受光素子６２の検出信号に含まれる正弦波信号との位相差を求め、その位相差に対応する距離ϕ_1に換算し、上記の絶対的な距離情報Ｄ’とから、測距対象である作業車Ｖ（厳密には回帰反射体５３）までの距離を求める。従って、演算装置７０は、測距対象までの距離を演算する距離演算手段ＤＤとして機能する。つまり、第１発振器６６の正弦波の波長をλ_1として、Ｄ’／（λ_1／２）＋１／２の整数部分として上記(1) 式のn_1を求め、(1)式によって移動車Ｖまでの距離を求める。

【００２１】従って、レーザ測位装置４０は、測距対象（作業車Ｖ）に向けてパルス状の光線を投射する第１測距用光源ＦＬとしての機能と、測距対象に向けて設定周期の基準信号にて変調された光線を投射する第２測距用光源ＳＬとしての機能とを、単一の発光装置６０にて兼用構成される状態で、兼ね備えて構成されている。演算装置７０は、上記のようにして求めた作業車Ｖまでの距離と、反射鏡６４の回転角を検出するロータリエンコーダ６５の出力信号によって求めたビーム光の投射方位（図５におけるα）とから、作業車Ｖの圃場Ｆにおける水平面内の位置情報を求めて、ＳＳ無線装置５２にて作業車Ｖに送信する。

【００２２】次に、作業車Ｖの構成について説明する。図２及び図６に示すように、車体５の後部側のミッションケース２５に、３点リンク機構を構成する上下揺動自在なトップリンク２６と左右一対のロアリンク２７とが支持され、それらのリンク２６，２７を介して、ロータリー式の耕耘装置６が着脱自在に、且つ昇降及び傾斜自在に連結されている。耕耘装置６には、機体後部の駆動軸２８から動力が伝達されて内部の耕耘爪が回転するようになっている。

【００２３】ミッションケース２５の上部に、昇降用油圧シリンダ１３により上下に揺動駆動される左右一対のリフトアーム２９が備えられ、この一対のリフトアーム２９とロアリンク２７とが、リフトロッド３６及び複動型の傾斜用油圧シリンダ２３を介して連結されている。ここで、昇降用油圧シリンダ１３を作動させて耕耘装置６の車体５に対する昇降位置を変更することができ、傾斜用油圧シリンダ２３を作動させて耕耘装置６の車体５に対する傾き（リフトロッド３６との連結点周りでの機体横幅方向への傾き）を変更することができる。一方のロアリンク２７の基端部に、耕耘装置６の車体５に対する昇降位置をロアリンク２７の揺動角度として検出するポテンショメータ利用の昇降位置検出センサＳ１が設けられ、又、耕耘装置６の車体５に対する機体横幅方向での傾きを傾斜用油圧シリンダ２３の伸縮量として検出す

るストロークセンサＳ２が設けられている。

【００２４】図７及び図８にも示すように、前記３点リンク機構の後端側に背面視略Ａ字形の連結フレーム３７が連結され、この連結フレーム３７の上部にフック３８を取り付けるとともに、耕耘装置６の上部に設けた連結アーム３９に、上記フック３８に係合する係合ピン３９ａを固設してある。連結フレーム３７の上端には、支持アーム５１を支持する支持筒３７ａの下端部が固定されている。又、連結フレーム３７の下部に、横向きに架設固定した連結ピン４６ａを備えた連結部４６を取り付けるとともに、連結アーム３９の下方側に上記連結ピン４６ａに係合する凹部４７ａを備えた左右一対の板状係合部材４７を固設してある。これにより、連結アーム３９側の係合ピン３９ａを連結フレーム３７側のフック３８に係合させた状態で、リフトアーム２９を上方に揺動させて耕耘装置６を吊り上げると、連結アーム３９側の凹部４７ａが連結フレーム３７側の連結ピン４６ａに係合し、ロック部材４８にて上記連結ピン４６ａの凹部４７ａへの係合状態の外れを阻止するようになっている。つまり、耕耘装置６に代えて他の作業部を作業車Ｖに付設することができる。

【００２５】図１に示すように、車体５に備えた左右一対の前輪３及び後輪４は、左右を一対として各別に操向操作自在に構成され、ステアリング用の油圧シリンダ７，８と、電磁操作式の制御弁９，１０とが設けられている。つまり、前輪３のみを操向する２輪ステアリング形式、前後輪３，４を逆位相で且つ同角度に操向する４輪ステアリング形式の２種類のステアリング形式を選択使用できる。尚、各作業行程Ｌに沿っての直進走行時には、前輪３のみを操向する２輪ステアリング形式で行う。

【００２６】図１中、Ｅはエンジン、１１はエンジンＥからの出力を変速して前後輪３，４の夫々を同時に駆動する油圧式無段変速装置、１２はその変速操作用の電動モータ、１３は前記昇降用油圧シリンダ、１４はその制御弁、２３は前記傾斜用油圧シリンダ、２４はその制御弁、１５はエンジンＥから耕耘装置６への駆動を断続する電磁操作式の耕耘用クラッチである。１６は、作業車Ｖの走行並びに耕耘装置６の作動等を制御するマイクロコンピュータ利用の制御装置であって、前記昇降位置検出センサＳ１、前記ストロークセンサＳ２及び後述の各種センサによる検出情報や予め記憶された作業データに基づいて、変速用モータ１２、各制御弁９，１０，１４，２４、耕耘用クラッチ１５等を作動させる。

【００２７】作業車Ｖに装備されるセンサ類として、図１に示すように、前後輪３，４夫々の操向角を検出するポテンショメータ利用の操向角検出センサＲ１，Ｒ２と、変速装置１１の変速状態に基づいて間接的に前後進状態及び車速を検出するポテンショメータ利用の車速センサＲ３と、変速装置１１の出力軸の回転数を計数して走行距離を検出するためのエンコーダＳ３と、車体方位を検出する地磁気方位センサＳ４とが設けられている。

【００２８】作業車Ｖの制御装置１６には、上記各種のセンサ類の他に、スペクトラム拡散方式の無線装置であるＳＳ無線装置５０と受光器５４とが接続され、ＳＳ無線装置５０との通信相手として、レーザ測位装置４０に接続されたＳＳ無線装置５２が設置されている。受光器５４は、図３に示すように、受光パネル５４ａが支持部５４ｂの表裏両面に取り付けられて構成されている。受光パネル５４ａは、多数の受光素子が上下方向に配列されて構成され、高さ方向で受光位置が検出可能となっており、レーザ測位装置４０のビーム光の投射高さが一定であるので、そのビーム光が受光パネル５４ａのどの位置に当たるかによって耕耘装置６の絶対的な高さを検出できる。

【００２９】上記のようにして作業車Ｖに送信された作業車Ｖの水平面内における位置情報は、図５に示すように、作業車Ｖが圃場Ｆの作業行程Ｌに沿って走行するのに利用され、具体的には、水平面内の位置情報として記憶されている作業行程Ｌと、実際に検出した水平面内における位置情報との偏差が、設定範囲内に収まるように、ステアリング制御のための制御弁９，１０が制御される。

【００３０】このような操向制御によって、作業車Ｖは、図５で最右端側に位置する最初の作業行程Ｌのスタート地点Ｓｔから走行開始して、２輪ステアリングで各行程に沿って直進走行するとともに、各作業行程Ｌの終端部から隣接する作業行程Ｌの始端部に向けて、終端地点ｅから所定距離直進走行してから１８０度の旋回動作を開始し、所定の旋回区間ｇを経て旋回動作の終点ｆに至る経路ｅ～ｆを所望の回向軌跡とする回向パターンで、４輪ステアリングにて回向動作し、回向後は、逆方向に走行する往復走行を繰り返して、圃場Ｆの全範囲を走行する。そして、各作業行程Ｌにおける適正作業箇所において、耕耘装置６の絶対的な高さが設定高さを維持するように、耕耘装置６の高さ情報に基づいて、昇降用油圧シリンダ１３の制御弁１４が制御される。

【００３１】〔別実施形態〕以下、本発明の別実施形態を列記する。

① 上記実施の形態では、位相差検出手段ＦＤは、第２発振器７２を用いてヘテロダイン検波する構成を採っているが、受光素子６２の検出信号と、第１発振器６６の出力信号とを位相計にて直接比較する構成としても良い。

② 上記実施の形態では、第１測距用光源ＦＬと第２測距用光源ＳＬとを単一の発光装置６０を備えて兼用構成されているが、光源及び受光手段等を完全に独立に備えても良い。

③ 上記実施の形態では、発光装置６０として半導体レーザ素子ＬＤを採用しているが、発光ダイオード等の他

の光源を採用しても良い。

④　上記実施の形態では、測距のための光線を回転走査する構成としているが、測定の都度、作業者等が、測距対象に向けて測距のための光線を投射する構成としても良い。

【００３２】⑤　上記実施の形態では、回帰反射体５３等を支持する支持筒３７ａは、作業車Ｖの本体に対して揺動する連結フレーム３７に固定されているが、支持筒３７ａの下端部を連結フレーム３７に対して車体前後方向に揺動調節可能に取り付けて、支持アーム５１等の傾き調節できる構成としても良い。又、連結フレーム３７の車体前後方向での傾きを検出する傾斜センサと支持筒３７ａを揺動駆動するアクチュエータとを備えて、傾斜センサの検出情報に基づいて、上記支持アーム５１等が直立姿勢を維持するように、アクチュエータを制御して傾き調節するように構成しても良い。

【００３３】⑥　上記実施の形態では、発光装置６０から出射されたビーム光を回転走査して測距対象に投射しているが、作業者が手動調節により、測距対象（静止しているものでも良い）に向けてビーム光を投射する構成としても良い。この場合は、得られる測距情報が極めて多数となり、統計的処理を施すことにより、更に測距精度を向上させることができる。

【００３４】⑦　上記実施の形態では、本発明を、農用トラクターＶが圃場Ｆ内で耕耘作業を行うときの農用トラクターＶの測位に適用する場合を例示しているが、田植え機等の他の農機やバックホー等の建機の測位にも適用できる。又、作業車の測位ではなく、単純に作業車までの距離の測定に用いることができるのはもちろんのことである。尚、特許請求の範囲の項に図面との対照を便利にするために符号を記すが、該記入により本発明は添付図面の構造に限定されるものではない。

【図面の簡単な説明】

【図１】本発明の実施の形態にかかる作業車のブロック構成図

【図２】本発明の実施の形態にかかる測距装置の側面図

【図３】本発明の実施の形態にかかる要部斜視図

【図４】本発明の実施の形態にかかる測距装置のブロック構成図

【図５】本発明の実施の形態にかかる作業車の作業行程を示す平面図

【図６】本発明の実施の形態にかかる作業車の要部を示す斜視図

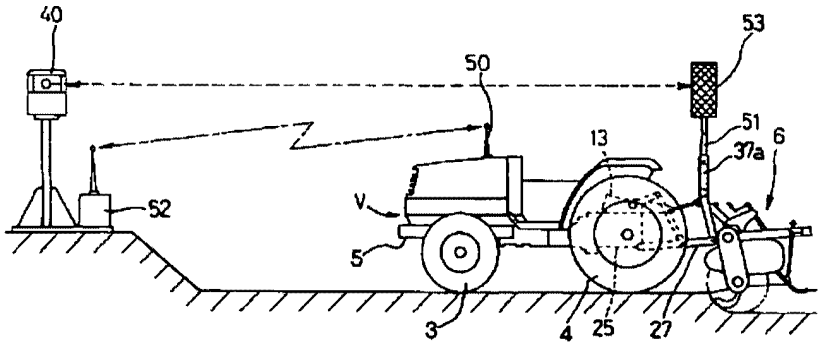
【図７】本発明の実施の形態にかかる作業車の要部を示す側面図

【図８】本発明の実施の形態にかかる作業車の要部を示す展開図

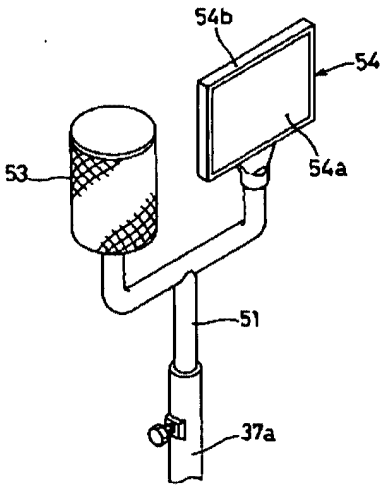
【符号の説明】

６０　発光装置
６２　受光手段
６９　計時手段
ＡＭ　変調装置
ＤＤ　距離演算手段
ＦＤ　位相差検出手段
ＦＬ　第１測距用光源
ＬＤ　半導体レーザ素子
ＳＬ　第２測距用光源

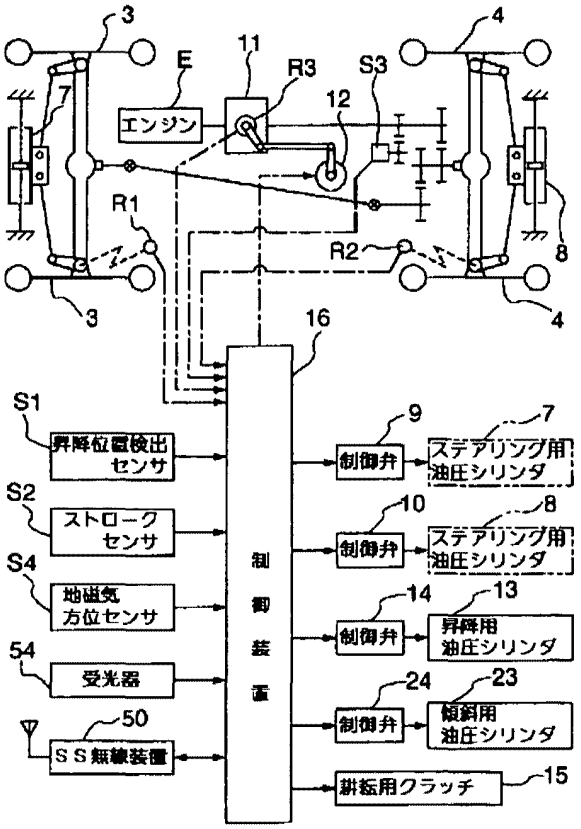
【図２】



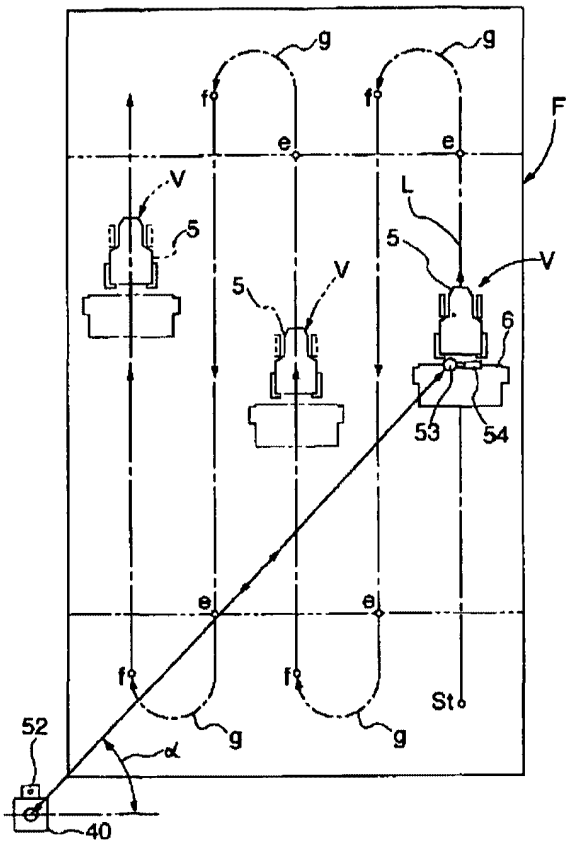
【図３】



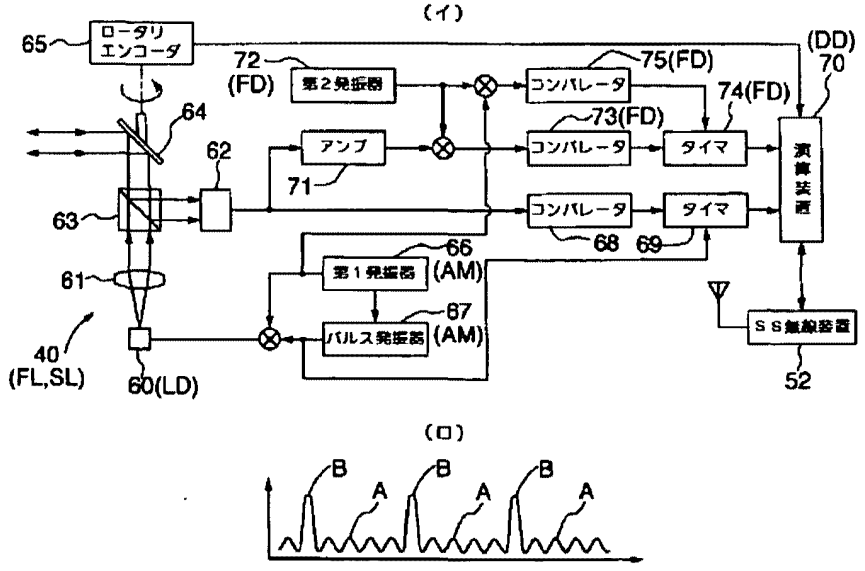
【図1】


3
4
E
11
R3
S3
12
エンジン
7
R1
R2
8
16
S1
昇降位置検出センサ
S2
ストロークセンサ
S4
地磁気方位センサ
54
受光器
50
ＳＳ無線装置
制御装置
9
制御弁
7
ステアリング用油圧シリンダ
10
制御弁
8
ステアリング用油圧シリンダ
14
制御弁
13
昇降用油圧シリンダ
24
制御弁
23
傾斜用油圧シリンダ
15
耕耘用クラッチ

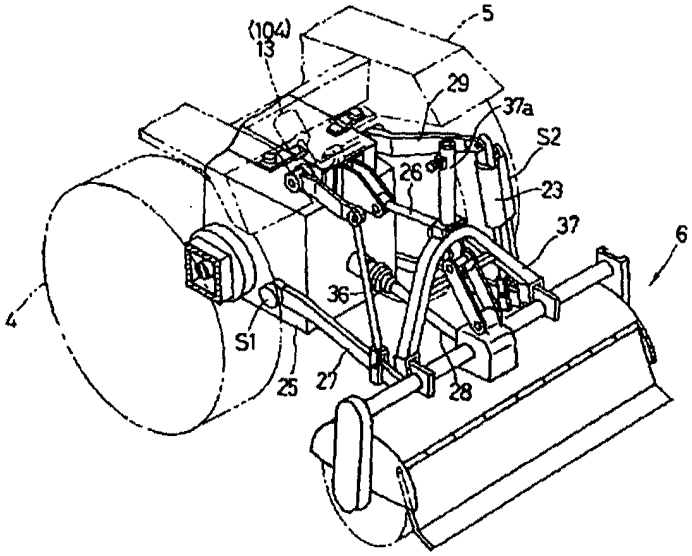
【図5】


g
f
e
F
V
5
L
6
53
54
St
52
α
40

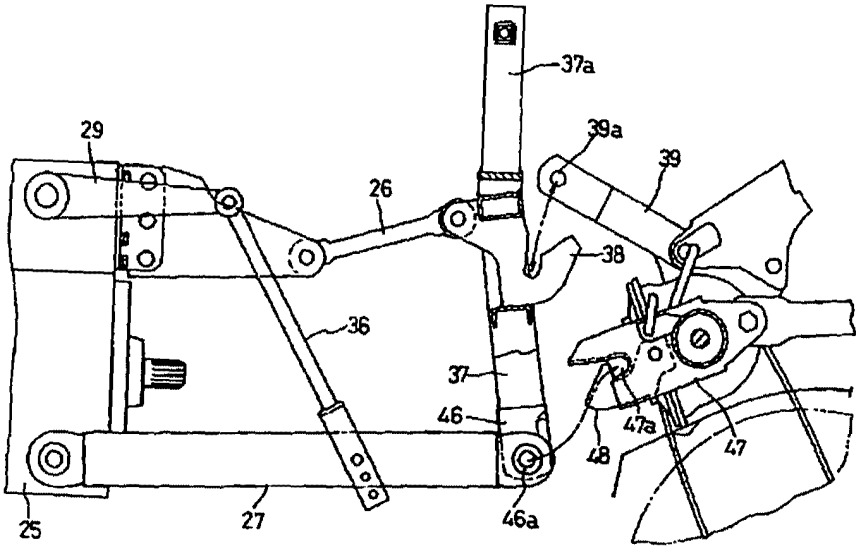
【図4】


（イ）
65
ロータリエンコーダ
72
(FD)
第２発振器
75(FD)
コンパレータ
(DD)
70
74(FD)
64
73(FD)
62
アンプ
71
コンパレータ
タイマ
演算装置
63
コンパレータ
タイマ
68
69
66
第１発振器
(AM)
61
67
パルス発振器
(AM)
ＳＳ無線装置
40
(FL,SL)
60(LD)
52
（ロ）
B
A
B
A
B
A

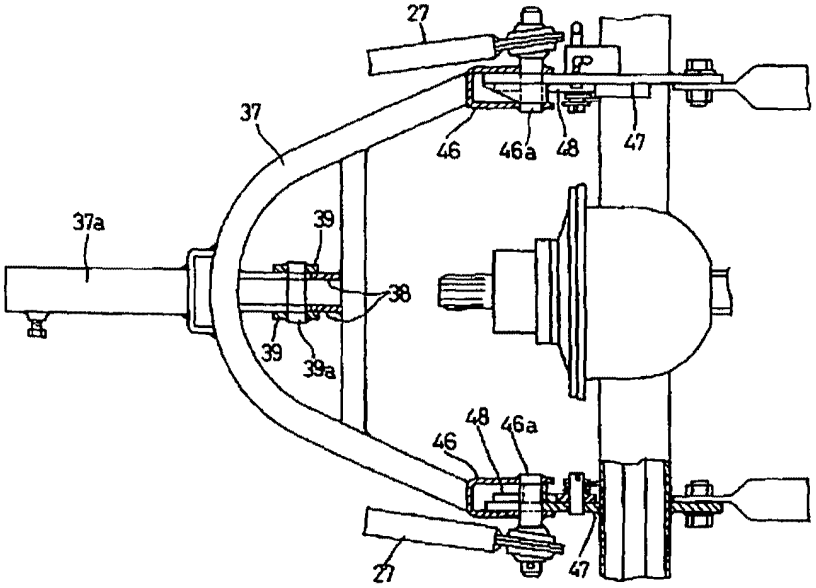
【図6】


(104)
13
5
29
37a
S2
26
23
37
6
4
36
S1
25
27
28

【図7】


37a
29
39a
39
26
38
36
37
46
47a
48
47
25
27
46a

【図8】



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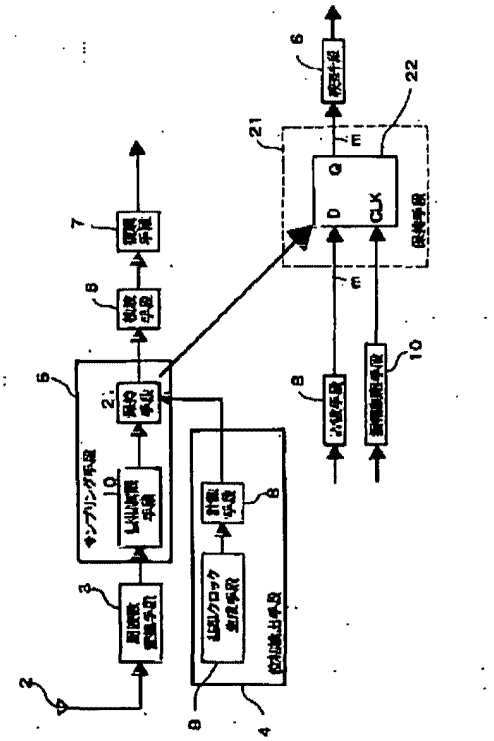
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(54)【発明の名称】　ディジタル無線通信用復調装置

(57)【要約】

【課題】　ディジタル信号によって周波数変調また位相変調された信号で通信を行う無線通信システムの基地局または端末局の復調装置において、差動変調方式に対する同期検波方式を小規模かつ簡便な検波判定処理機能で実現し、復調装置全体の小型化や低消費電力化、低コスト化、受信特性の向上を図る。

【解決手段】　受信したπ／４シフト差動ＱＰＳＫ変調信号を中間周波数の信号に変換する周波数変換手段３と、基準クロックで動作する計数手段８であって物理情報伝送周期の単位周期時間経過後の中間周波数受信信号との位相ずれが±π／４となるように計数周期が設定された計数手段８と、計数手段８の出力を中間周波数受信信号を基準にサンプリングして該中間周波数受信信号の位相情報を得るサンプリング手段５と、サンプリング手段５の出力を検波する検波手段６と、検波出力から送信情報を復調する復調手段７とを具備してなる。



【特許請求の範囲】
【請求項１】　ディジタル信号によって周波数変調または位相変調された信号を受信する受信手段と、
前記受信した信号を所定の中間周波数の信号に変換する周波数変換手段と、
前記中間周波数と異なる周期で所定の基準クロックにより動作する計数手段と、
前記計数手段の出力を前記中間周波数の受信信号を基準にサンプリングして該受信信号の位相情報を出力するサンプリング手段と、
前記サンプリング手段の出力を検波する検波手段と、
前記検波手段の出力から送信情報を復調する復調手段とを具備することを特徴とするディジタル無線通信用復調装置。
【請求項２】　請求項１記載のディジタル無線通信用復調装置において、
π／Ｎシフト差動Ｎ相ＰＳＫ変調方式を用いた場合に、前記計数手段の計数周期が、物理情報伝送周期の単位周期時間経過後の中間周波数の受信信号との間に±π／Ｎの位相ずれが生じる値に設定されていることを特徴とするディジタル無線通信用復調装置。
【請求項３】　請求項１記載のディジタル無線通信用復調装置において、
π／４シフト差動ＱＰＳＫ変調方式を用いた場合に、前記計数手段の計数周期が、物理情報伝送周期の単位周期時間経過後の中間周波数の受信信号との間に±π／４の位相ずれが生じる値に設定されていることを特徴とするディジタル無線通信用復調装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、ディジタル信号によって周波数変調または位相変調された信号で通信を行う無線通信システム、特に変調方式に差動符号化方式、例えばπ／４シフト差動ＱＰＳＫ方式等を採用している無線通信システムの基地局および端末局に用いられる復調装置に関するものである。
【０００２】
【従来の技術】近年、ディジタル自動車／携帯電話システムの、周波数資源の有効活用やデータ伝送の高速化といったマルチメディア対応へ向けての期待がよりいっそう膨らみつつある。ディジタル伝送方式は、誤り検出・誤り訂正技術を用いて高伝送品質・高信頼性・高秘匿性を実現しやすい上に、アナログ伝送のような忠実な伝送波形やスペクトルの再生が不要であるために狭帯域化や多重化に適し、さらに、音声・画像・データなどを統合的にシームレスに取り扱えることなどから、今後のマルチメディア情報化社会に欠かせない通信方式の一つとして注目されている。さらに、ここ数年のパソコン通信やインターネットに見られるようなパソコンを利用した情報アクセスサービスの急激な広がりや通信料金の低下は、ディジタル自動車／携帯電話システムの普及に更なる拍車をかけ、同システムの利用者は今後も増え続けると予想される。
【０００３】ところで、現在、ＰＨＳやＰＤＣに代表される携帯電話端末の中には、大きさにして１００ｃｃ以下、重さにして１００ｇ以下と言ったかなり小型のものまで登場しているが、このような端末の小型化は既存のディジタル伝送方式では限界に近づいてきている。
【０００４】一般に、ディジタル信号によって周波数変調または位相変調された信号で通信を行う無線通信システムの基地局および端末局の復調装置には、図６に示すような直交復調方式が採用されている。この直交復調方式の復調装置では、アンテナ８１で受信した信号を周波数変換手段８２、混合器８３、π／２位相器９０および局部発振器８９からなる部分にて、直交するベースバンド信号（同相成分および直交相成分）に周波数変換し、それぞれの相（チャネル）毎に、低域濾波器（ＬＰＦ）８４、ＡＤ変換器（ＡＤＣ）８５、ルートロールオフフィルタ（ＲＲＯＦ）８６、遅延検波器８７および判定・復調処理部８８を通してＡＤ変換、帯域制限および検波復調を行っており、全体の回路規模が大きなものとなる。
【０００５】また、ＰＨＳやＰＤＣで採用されている差動変調方式の場合、直交ベースバンド信号を差動検波するための複素乗算処理を実現するために、図７に示すように、通常は遅延検波器８７内に４つの乗算器９２と２つの加算器９３を用意する必要があり、やはり全体の回路規模が大きくなる。このような事情により携帯電話に直交復調方式を採用することは敬遠されつつある。また、最近注目されつつあるＤＳＰによるソフトウェア受信機でも、遅延検波処理で多くのインストラクションを費やすことになるので、処理量の削減が望まれる。
【０００６】以上の点から現在は直交復調方式に代わって中間周波数帯（ＩＦ）の受信信号から直接位相成分を抽出し検波処理を行うＩＦ復調方式が積極的に採用されている。この方式のメリットは以下の通りである。
【０００７】（１）直交ベースバンドへの周波数変換が不要
直交復調方式に不可欠なＩＦ信号分配器、混合器（×２）、π／２位相器、局部発振器、ローパスフィルタ（×２）等の部品が不要となる。
【０００８】（２）ＡＤ変換器が不要
直交復調方式に不可欠なベースバンド信号の同相成分用、直交成分用のＡＤ変換器が不要となる。
【０００９】（３）ディジタルフィルタが不要
直交復調方式に不可欠なベースバンド信号の同相成分用、直交相成分用のディジタルローパスフィルタが不要となる。
【００１０】（４）複素遅延検波（差動検波）器が不要
直交復調方式では、ベースバンド信号を複素信号として

取り扱うため、差動検波処理には4回の乗算処理と2回の加算処理を行う必要があるが、ＩＦ受信信号から直接位相成分を抽出すれば、差動検波処理は1回の減算処理で実現できる。（５）低量子化精度化
直交復調方式では、直交分解された受信信号の振幅成分を取り扱うため、フェージングによる振幅変動を考慮してダイナミックレンジを大きく設定しなくてはならず、高量子化精度が要求される。これに対し、ＩＦ受信信号から直接位相成分を抽出すれば、振幅成分とは無関係に、0～2πの位相成分に対するダイナミックレンジを設定できる。これはたかだか5～6ビット程度で十分である。
【００１１】以上のようにＩＦ復調方式は、従来の直交復調方式と比較して数多くの利点を持つため、ＰＨＳやＰＤＣだけでなく、今後成長が期持されるパーソナル通信の分野のコア技術となり得る。
【００１２】自動車電話および携帯電話をはじめ、これからのパーソナル通信端末ではモビリティが追及される。移動しながらの高品質な通信を実現することはかなり厳しく、通信システム自体に移動に対する耐性を持たせる必要性が増してきている。差動変調方式は、移動受信の要求を解決し得る手段の一つとして注目されており、多くの通信システムで採用されている。この差動変調方式は位相変調の一種で、絶対位相に送信情報をマッピングするのではなく、相対位相（位相差）に送信情報をマッピングすることにより達成される。その結果、移動受信に特有のフェージング歪みに対する極めて強い耐性を持たせることができる。
【００１３】しかし、差動変調方式に対する非同期の差動復調方式は、簡便な構成で実現できるものの受信Ｓ／Ｎが若干劣る。そこで受信特性を改善可能な同期検波方式が検討されている。同期検波方式は、非同期検波方式である差動検波（差動復調）方式よりも2～3（ｄＢ）程度の受信特性の改善が期待できる。しかしその反面、受信機を送信機に同期させるための処理が複雑になるという問題がある。
【００１４】さらに、一般に差動復調方式では、送信情報のマッピングの際に送信情報周期ごとに一定量の位相変化を付加する“シフト方式”を採用しているため、物理情報伝送周期毎に検波時の判定基準を切り換える必要があり、復調装置の構成が複雑になる。
【００１５】
【発明が解決しようとする課題】上述したように、ディジタル信号によって周波数変調または位相変調された信号で通信を行う無線通信システムの復調装置では、様々な新規技術の適用により小型・低消費電力化が図られ、低価格化とともに通話／待受時間延長に対する要望が満たされつつある。しかし、マルチメディア通信に対応するためには、これら要望に加え、通信品質の向上が不可欠である。現在、移動体通信で多く採用されている位相変調方式の一種であるシフト型の差動変調方式では、上述した理由からＩＦ復調方式で非同期検波方式が用いられているものの、受信特性の劣化が問題となっている。そこで、これに代わる同期検波方式の採用が検討されているものの、シフト型の差動変調方式では、検波判定処理部で符号判定基準を情報伝送周期単位で変化させなくてはならないため構成が複雑なものとなる、という問題があった。
【００１６】本発明はこのような課題を解決するためになされたもので、ディジタル信号によって周波数変調または位相変調された信号で通信を行う無線通信システム、特にシフト型位相変調方式で通信を行う無線通信システムの基地局または端末局の復調装置で同期検波方式を実現する場合に、情報伝送周期毎の符号判定基準の制御を不要とし装置の構成を簡素化することのできるディジタル無線通信用復調装置の提供を目的とする。
【００１７】
【課題を解決するための手段】上記した目的を達成するために、本発明のディジタル無線通信用の復調装置は、ディジタル信号によって周波数変調または位相変調された信号を受信する受信手段と、前記受信した信号を中間周波数の信号に変換する周波数変換手段と、前記中間周波数と異なる周期で所定の基準クロックにより動作する計数手段と、前記計数手段の出力を前記中間周波数の受信信号を基準にサンプリングして該受信信号の位相情報として出力するサンプリング手段と、前記サンプリング手段の出力を検波する検波手段と、前記検波手段の出力から送信情報を復調する復調手段とを具備することを特徴とするものである。
【００１８】そして本発明は、特に、π／Ｎシフト差動Ｎ相ＰＳＫ変調方式が採用されている場合に、計数手段の計数周期が、物理情報伝送周期の単位周期時間経過後の中間周波数の受信信号との間に±π／Ｎの位相ずれが生じる値に設定されている点に特徴がある。例えば、π／4シフト差動ＱＰＳＫ変調方式を用いた場合、計数手段の計数周期は、物理情報伝送周期の単位周期時間経過後の中間周波数の受信信号との間に±π／4の位相ずれが生じる値に設定される。
【００１９】このように計数手段の計数周期を設定することにより、中間周波数受信信号の位相の縮退を回避しつつ、物理情報伝送周期毎に生じるシフト型差動変調方式特有の位相シフトを吸収でき、符号判定基準を物理情報転送周期単位で変化させることなく一定の判定基準の下で検波・判定を行うことが可能となる。これにより、ディジタル無線通信用復調装置の小型化、低消費電力化等を実現することができる。
【００２０】
【発明の実施の形態】以下、本発明の実施の形態を図面を参照しながら詳細に説明する。
【００２１】図1は、本発明の一実施形態であるディジ

タル無線通信用復調装置、すなわちディジタル信号によって位相変調された信号で通信を行う無線通信システムの基地局または端末局に適用される復調装置の構成を示す図である。

【００２２】同図に示すように、本実施形態の復調装置１は、受信アンテナ２、周波数変換手段３、位相検出手段４、サンプリング手段５、検波手段６および復調手段７から構成されている。

【００２３】復調装置１に接続されている受信アンテナ２で受信した位相変調された信号は、周波数変換手段３にて所定の中間周波数の信号に変換される。図では省略したが、周波数変換手段３は例えばローカル、クロック生成器、ミキサー、帯域制限フィルタ、増幅器等から構成されている。周波数変換手段３によって周波数変換された中間周波数の受信信号はサンプリング手段５に入力される。サンプリング手段５は、後述する位相検出手段４の出力信号を周波数変換手段３より入力した中間周波数の受信信号を基準にサンプリングして該中間周波数の受信信号の位相情報として得る。

【００２４】位相検出手段４は、基準クロック生成手段９と、基準クロック生成手段９によって生成された基準クロックで動作する計数手段８から構成されている。計数手段８には所定の計数周期が設定されており、計数手段８は設定された計数周期でリセットを繰り返しながら基準クロック９の計数を実行し、その計数値をサンプリング手段５に出力する。

【００２５】計数手段８の計数周期は、中間周波数（の中心周波数）と異なる値で且つシフト型差動変調方式に依存した特定値に設定されている。例えば、π／４シフト差動ＱＰＳＫ変調方式の場合、計数器８の計数周期は、物理情報伝送周期の単位周期時間経過後の中間周波数受信信号との間に±π／４だけの位相ずれが生じる値に設定されている。同様に、π／２シフト、π／８シフト、π／１６シフト差動ＱＰＳＫ変調方式が採用されている場合は、計数器８の計数周期を、物理情報伝送周期の単位周期時間経過後の中間周波数受信信号との間にそれぞれ±π／２、±π／８、π／１６だけの位相ずれが生じる値に設定すればよい。

【００２６】図２にこの復調装置１の構成をサンプリング手段５の詳細な構成を含めて示す。同図に示すように、サンプリング手段５は、周波数変換手段３より出力された中間周波数受信信号の振幅を制限する振幅制限手段１０と保持手段２１とで構成される。保持手段２１は、例えば、Ｄタイプのフリップフロップ２２で実現することができる。このＤタイプフリップフロップ２２のＤ入力端子は計数手段８の出力端子と接続され、ＣＬＫ入力端子は振幅制御手段１０の出力端子と接続されている。すなわち、周波数変換手段３より出力された中間周波数受信信号は振幅制限手段１０にて一定の振幅に制限されることで矩形波のように整形され、中間周波数受信信号の変調成分がＰＷＭに変換される。Ｄタイプフリップフロップ２２は、計数手段８から出力された中間周波数受信信号の位相情報であるｍビットのデータを振幅制限手段１０の出力信号の立ち上げエッジ毎に保持する。

【００２７】サンプリング手段５の出力信号は中間周波数受信信号の位相成分を示す情報であり、このサンプリング手段５の出力信号に対して検波手段６にて変調方式に応じた検波を行う。検波手段６によって検波された受信信号は復調手段７に出力され、復調手段７はその受信信号に対して所定のデマッピング処理やパラレル・シリアル変換等の処理を行うことで送信情報系列を再構成する。

【００２８】図３は計数手段８の計数周期、物理情報伝送周期、並びに周波数変換手段３の出力である中間周波数受信信号周期の関係を示した図である。

【００２９】ここで物理情報伝送周期（通常、シンボル周期と呼ばれる。）をＴとする。シフト系差動変調方式の場合、同一情報を伝送しても、１Ｔ時間後に必ず一定の位相変化が生じ、ＩＦ受信信号の中心周波数でＩＦ受信信号を観測すると、１Ｔ時間後に位相が一定量θだけ進んで見えるか、もしくは遅れて見える。本実施形態の復調装置は、前述したように、π／４シフト差動ＱＰＳＫ変調方式等のπ／Ｎシフト差動Ｎ相ＰＳＫ変調方式において、計数手段８の計数周期を、物理情報伝送周期の単位周期時間経過後のＩＦ受信信号との位相ずれが±π／Ｎとなる値に設定しておくことで、上記の位相ずれを吸収するようにしたものである。

【００３０】本発明の原理を数式により説明する。

【００３１】計数手段８の計数周期をω_c、ＩＦ受信信号の中心周波数をω_{IF}、任意の初期位相をϕ、Ｔ秒後の位相ずれをπ／Ｎとして、

$$\cos(\omega_c T+\phi)=\cos(2n\pi+\phi\pm(\pi/N)) \quad \cdots\cdots(1)$$

を満たす正数ｎを求める。ただし、（１）式を解く際に次の条件が加わる。

【００３２】

$$\omega_{IF}T-\pi+\phi\leqq\omega_c T+\phi=2n\pi+\phi\pm(\pi/N)\leqq\omega_{IF}T+\pi+\phi \quad \cdots(2)$$

この条件のもとで求めたω_cから計数手段８の計数周期を設定する。そこで上式（２）を次のように変形する。

【００３３】

$$f_{IF}-(f_s/2)\leqq f_c=f_s(n\pm(1/2N))\leqq f_{IF}+(f_s/2) \quad \cdots\cdots(3)$$

ただし、1／T＝f_sとする。

$$(f_{IF}/f_s)-(1/2)\pm(1/2N)\leqq n\leqq(f_{IF}/f_s)+(1/2)\pm(1/2N)\quad\cdots\cdots(4)$$

が求められる。

【0035】一例としてf_{IF}＝500（kHz）、f_s＝21（kHz）、変調方式がπ／4シフト差動QPSK方式（N＝4）である場合の計数手段8の計数周期f_cを求める。これはPDCシステムを対象とした一例である。この場合、（4）式を満足する正数nは24となる。したがって、計数手段8の計数周期f_cは、

$f_c=f_s(n\pm(1/2N))\quad\cdots\cdots(5)$

＝21000×（24±（1／8））

＝501375（Hz），506625（Hz）

となる。

【0036】前者の周波数に相当する周期で計数手段8を動作させるとT時間経過後の計数手段8の動作位相は計数開始時刻の位相に対してπ／4だけ遅れ、また、後者の周波数に相当する周期で計数手段8を動作させた場合はT時間経過後の計数手段8の動作位相は計数開始時刻の位相に対してπ／4だけ進む。これに対し、IF受信信号は情報系列による変調を受けているためT時間経過後に±π／4もしくは±3π／4だけ位相が変化する。したがって、例えば、後者の周波数に相当する周期で計数手段8を動作させた場合、T時間経過後にπ／4だけ位相が変化するような情報を伝送すると、検出される位相は計数開始時刻とT時間経過後の2時刻で同一となる。

【0037】このように、シフト型差動変調方式が持つ固定的な位相変化成分を復調装置内で吸収することで、符号判定点の数を減らすことが可能となり、装置の縮小化が図れる。上記の例では8点必要であった判定点が4点に減る。

【0038】なお、この復調方式は、同期検波の実現を目指したものであるが、非同期系の差動復調方式に対しても有効である。

【0039】図4は直交座標上のπ／4シフト差動QPSK変調方式の信号点配置を示している。○から×への遷移、×から○への遷移は、それぞれ物理情報伝送周期で行われる。したがって、隔時刻ごとに×○を送信することになり、復調装置で同期検波する場合は、隔時刻ごとに×用判定および○用判定を計8点で行わなければならず、物理情報伝送周期毎に符号判定基準を変更しなければならない。

【0040】本実施形態の復調装置は、物理情報伝送周期毎に計数手段8の動作位相と中間周波数受信信号の位相との間にπ／4の位相差が生じるため、図5に示すように、判定点位置が4点に減る。この結果、符号判定基準を物理情報転送周期毎に変化させることなく検波・判定を行うことが可能となり、アナログ系、ディジタル系の部品点数を削減化できて復調装置の小型化、低消費電力化等を実現することができる。

【0041】さらに、本発明により、今後期特されるDSPによるソフトウェア復調装置の実現において同期検波プログラムの削減が可能となるという効果も生まれる。

【0042】また、本発明に係る復調装置は非同期の差動検波方式にも適用することが可能である。なぜなら、（1）～（5）式を満足している限り、IF受信信号の位相の縮退が生じないし、物理情報伝送周期を基準とした位相変化にしか情報を乗せていないためである。したがって、図1のサンプリング手段5からの出力を従来通りに検波手段6で検波することができる。

【0043】以上、ディジタル信号によって位相変調された信号で通信を行う無線通信システムの基地局または端末局に適用される復調装置に本発明を適用した実施形態について説明したが、本発明は、ディジタル信号によって周波数変調（例えばMSK変調方式）された信号で通信を行う無線通信システムに適用される復調装置にも適用することができ、同様の効果を得ることが可能である。

【0044】

【発明の効果】以上説明したように本発明によれば、ディジタル信号によって周波数変調または位相変調された信号で通信を行う無線通信システム、特にシフト型位相変調方式で通信を行う無線通信システムの基地局または端末局の復調装置で同期検波方式を実現する場合に、物理情報伝送周期毎に生じるシフト型差動変調方式特有の位相シフトを吸収でき、符号判定基準を物理情報転送周期単位で変化させることなく一定の判定基準の下で検波・判定を行うことが可能となる。これにより、ディジタル無線通信用復調装置の小型化、低消費電力化等を実現することが可能となる。

【図面の簡単な説明】

【図1】本発明の一実施形態であるディジタル無線通信用復調装置の全体構成を示す図である。

【図2】図1の復調装置の構成をサンプリング手段の詳細な構成を含めて示した図である。

【図3】図1の復調装置における計数手段の計数周期、物理情報伝送周期、並びにIF受信信号周期の関係を示す図である。

【図4】直交座標上のπ／4シフト差動QPSK変調方式の信号点配置を示す図である。

【図5】図1の復調装置における直交座標上の符号判定点配置を示す図である。

【図6】従来の差動変調方式を採用したディジタル無線通信用復調装置の全体構成を示す図である。

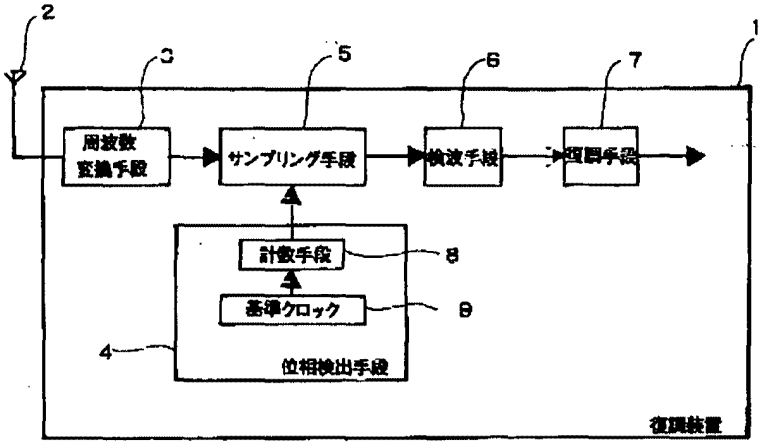
【図7】図6における遅延検波器の構成を示す図であ

る。

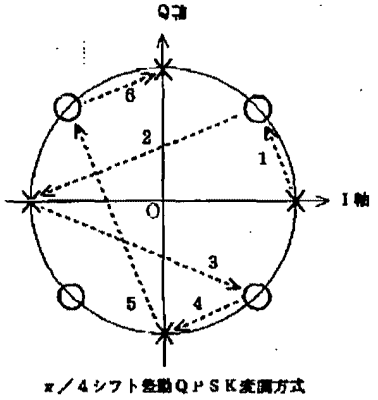
【符号の説明】

1……復調装置
2……受信アンテナ
3……周波数変換手段
4……位相検出手段
5……サンプリング手段
6……検波手段
7……復調手段
8……計数手段
9……基準クロック生成手段
１０……振幅制限手段
２１……保持手段
２２……Ｄタイプフリップフロップ

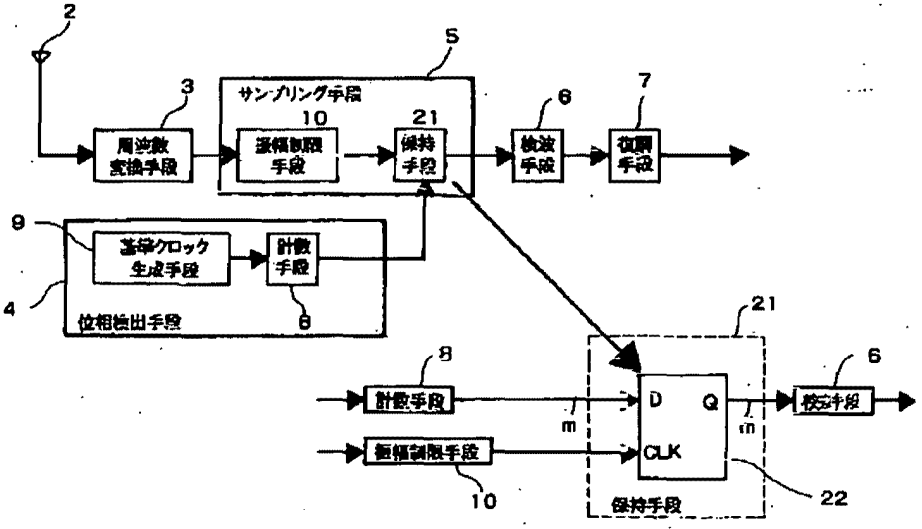
【図１】



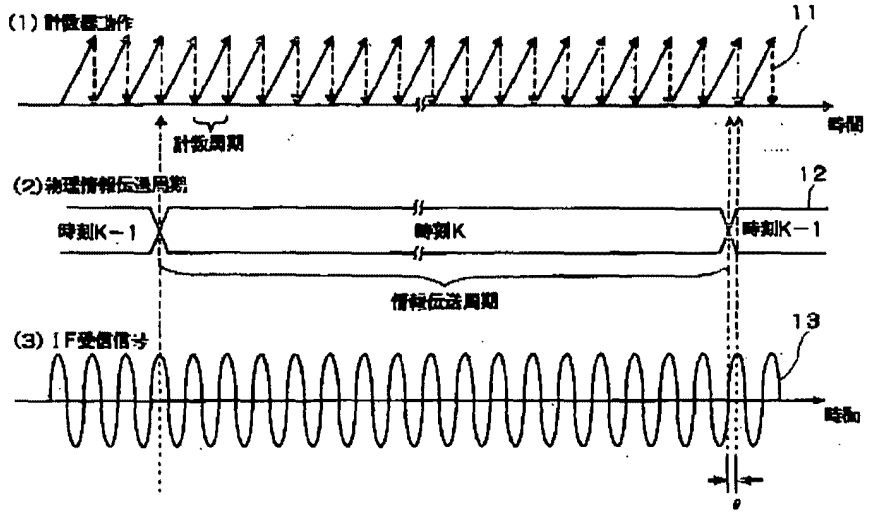
【図４】



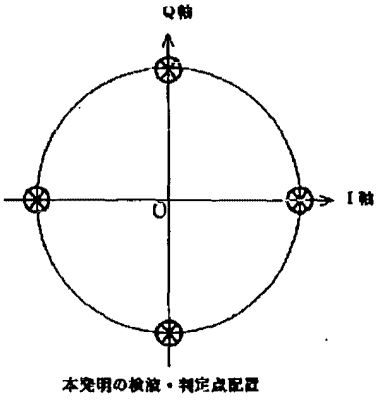
【図２】



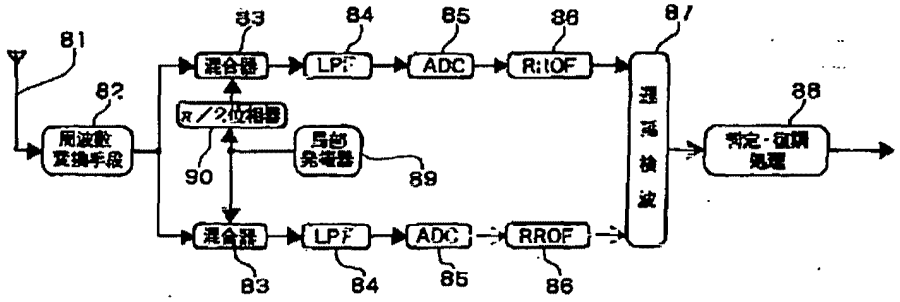
【図3】


(1) 計数器動作
11
時間
計数周期
(2) 物理情報伝送周期
12
時刻K－1
時刻K
時刻K－1
情報伝送周期
(3) IF受信信号
13
時間
θ

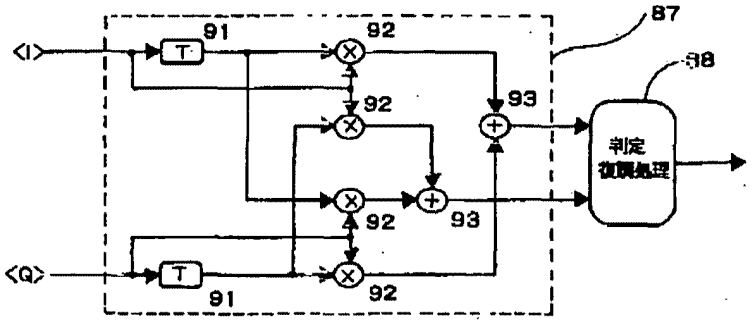
【図5】


Q軸
I軸
0
本発明の検波・判定点配置

【図6】


81
82
周波数変換手段
83
混合器
84
LPF
85
ADC
86
R:ROF
87
選局検波
88
判定・復調処理
π／2位相器
90
局部発振器
89
混合器
LPF
ADC
RROF
83
84
85
86

【図7】



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PA 69 / 2632

Modulator or Demodulator in Integrated Technology

The invention relates to an integrable active modulator or demodulator with single-ended input and single-ended output.

In the carrier frequency technology as well as in other areas of electrical communication engineering, at present active or passive modulators are used, which use at least one transformer. Such types of circuits are not quite suitable, because the inductances and the transformers can be realized only through the roundabout route of using gyrators and similar, and that too at a great expense. Known are circuits with integrated elements in part, in which the additional transformers with concentrated structures are connected. The hitherto known circuits, which contain only resistors, condensers and semiconductor components like diodes and transistors, have the disadvantage that they require to some extent very high expense, and that, apart from that, the input signal must be balanced.

The underlying problem of the invention lies in providing a modulator or a demodulator of the kind mentioned at the outset, which enables an integrated embodiment with relatively little elaborate circuitry and can therefore be employed as a substitute for ring modulators, especially in frequency converting digital filters.

This problem is solved according to the invention in that the modulator consists of an input stage with outputs, which deliver two separate output signals with the same amplitude, and each of these outputs is connected through a switching four-pole network to an output stage, which combines the output signals of the two switching four-pole networks. The switching four-pole networks are actuated alternately in cyclic timing with a carrier frequency oscillation. The phase of one of the two output signals of the input stage is thereby shifted by 180° either in the input stage or after passing the corresponding switching four-pole network in the output stage.

In the case of the phase rotation in the input stage, it is advantageous to design the input stage as a phase reversal stage, whose output signal amplitudes are the same and in antiphase. In the case of phase rotation in the output stage, the output stage is preferably designed as a differential amplifier and the phase of one of the output signals of the input stage appears with a shift of 180° at the output of the differential amplifier.

Since it is difficult, due to the response times of the circuit elements, to open one switching four-pole network at the same time the other switching four-pole network is closed and vice versa, it is more suitable to regulate the circuit elements in both the switching four-pole networks by two square pulse sequences, derived from the carrier frequency, that are shifted by 180°, whose ratio of the pulse width to the interpulse period is less than 1. In that case it is ensured that in each case only one switching four-pole network is conducting for the output signal of the input stage. For the ratio of the pulse width to the interpulse period of 1/2, there is the additional advantage that the third harmonic of the switching frequency is not present in the generated pole reversal function, as can be determined from the Fourier analysis. It is also

advantageous, if the field effect transistors are used in both the switching four-pole networks, because the offset voltage in the case of field effect transistors is vanishingly small compared to the offset voltage of the commonly used transistors.

By designing the modulator in the aforementioned manner, it can be achieved that only resistors and semiconductor elements like transistors and diodes are required in the circuit of the modulator. A design of the modulator in integrated form is therefore especially easy to realize. An especially preferred area of application of such a modulator is therefore the use in integrated form in frequency converting digital filters.

A few forms of the embodiments of the modulators according to the invention are explained further on the basis of the drawings. Shown are

Fig. 1 a modulator with outputs of the input stage in mutual antiphase,

Fig. 2 another modulator with outputs of the input stage in mutual antiphase,

Fig. 3 a modulator with inputs of the output stage in mutual antiphase,

Fig. 4 another preferred exemplary embodiment of a modulator with outputs of the input stage in mutual antiphase

Fig. 5 evolution in time of the square pulse sequences for regulation of the switching four-pole network of the modulator according to Fig. 1 to Fig. 4.

The modulator according to Fig. 1 contains an input stage I with the input E, transistor T_0, the base voltage divider with the resistors $R1_0$ and $R2_0$, the load resistors $R3_0$ and $R4_0$ and the output terminals A1 and A2 in antiphase, which are connected with the input terminals E1 and E2 of the switching four-pole network SV1 and SV2. The output terminals A3 and A4 for the switching four-pole network are connected in parallel. The modulator represents a counter-cyclic timing modulator, in which both the switching four-pole networks are alternately cut off or connected with one rhythmic timing S1 or S2 in the form of a square pulse sequence derived from the carrier oscillation. At the common output A of both the switching four-poles, side bands with the frequency of the carrier oscillation, which represent the input signal with simultaneous suppression of the carrier wave, are generated in the familiar manner.

The other exemplary embodiments according to Figures 2 to 4 are also balanced modulators. The modulator according to Fig. 2 contains again an input stage I with two amplifiers V1 and V2, whose output terminals A1 and A2 in antiphase are connected to the input terminals E1 and E2 of the two switching four-poles SV1 and SV2. The output terminals A3 and A4 of both the four-pole networks are connected to the input terminals of one of the summers with output A representing the output stage. The switching four-poles SV1 and SV2 contain two field effect transistors FET 1 and FET 2. Their electrodes are shown with the denotations S = source or cathode, D = drain or anode and G = gate or grid customarily used for field effect transistors. The cyclic timings S1 and S2 are fed to the grids G of the field effect transistors through the voltage dividers consisting of the series circuit with a diode D1 or D2 with a resistor R3 or R4. The output terminals A1 and A2 of the input stage I are connected through the resistors R1 and R2, serving among other things as decouplers, directly to the output terminals A3 and A4. The field effect transistors FET 1 and FET 2 are

connected at their respective diodes D at the common connection points of the resistor R1 or R2 with the output terminal A3 or A4, and form, taking their cathodes K at the earth potential into consideration, a regulable short-circuit for the outputs of the switching four-pole networks. In the latter case, it is absolutely necessary that the output stage II is a summing stage, because otherwise the output signal of the entire modulator would be short-circuited.

The modulator according to Fig. 3 contains, as the input stage I, two input amplifiers V1 and V2', of which, in contrast to the amplifier V2 in Fig. 2, the amplifier V2' does not have any phase rotation between input and the output. The switching four-poles SV1 and SV2 have in principle the same design as the switching four-poles according to Fig. 2. They differ from it only in that the normally used transistors T1 and T2 are used in place of the field effect transistors FET 1 and FET 2 and the diodes D1 and D2 in the control circuit are replaced by the resistors R5 and R6. The output stage II is a differential amplifier in this case, which causes the phase reversal in one of the two transmission routes necessary for the function of the balanced modulator.

Fig. 4 shows an especially advantageous exemplary embodiment for a balanced modulator according to the invention. Its input stage I is identical with the input stage I of the modulator according to Fig. 2. While in the exemplary embodiment according

to Fig. 2, the anode-cathode paths of the field effect transistors FET 1 and FET 2 of the switching four-poles SV1 and SV2 are connected in parallel to the outputs of the switching four-poles in the sense of the regulable short-circuits, the anode-cathode paths of the field effect transistors FET1 and FET2 are connected in series with the resistor R1 or R2 between the input terminal E1 or E2 and the output terminal A3 or A4 in the sense of a controllable break in the connection. In this case, cyclic timing S1 or S2 can be fed directly to the grid G of the field effect transistors, that is, the voltage dividers provided in the exemplary embodiment according to Fig. 2 are not needed. The output stage II is here an operation amplifier V3, whose inverting input is connected parallel to the output terminals A3 and A4. The operation amplifier V3 can be dispensed with, if the correct switching behavior of the field effect transistors FET 1 and FET 2 is ensured by means of the corresponding input circuit.

For the sake of completeness, the curves of the cyclic times S1 and S2 at the control inputs of the switching four-poles SV1 and SV2 against time t are shown in Fig. 5. The switching four-poles SV1 and SV2 are conducting for the input signal in the case of "0," while they are blocked in the case of "Z." Since it is hardly possible to achieve with semiconductor components that one switching four-pole opens just at the time when the other one closes, it is advantageous to derive two square pulse sequences of the form shown in Fig. 5 from the carrier oscillation, in which the interpulse period is 240° and pulse width is 120° of a period, and the square pulse oscillations of both the switching four-poles are mutually shifted with respect to each other by 180°. Therewith it is ensured that only one of the two switching four-poles is switched on or

not short-circuited. With the aforementioned ratio of the pulse width to interpulse period, one has the advantage that the third harmonic of the switching frequency is not present in the generated pole-reversal function.

The switching four-pole networks SV1, SV2 according to Figures 2 and 3 are mutually exchangeable. There is also the possibility of substituting the field effect transistors FET 1 and FET 2 of the switching four-poles SV1 and SV2 according to Fig. 4 with commonly used transistors, which are to be connected with their emitter collector paths to the resistors R1 and R2 in series. Besides that, note that the switching four-poles with transistors connected in the series can also appear in place of the switching four-poles according to Figures 1 to 3.

5 Figures
8 Patent claims

Patent Claims

1. Integrable active modulator or demodulator with single-ended input and single-ended output, characterized in that the modulator comprises an input stage with two separate outputs, giving the output signal with the same amplitudes, each of which is connected through a switching four-pole network at an output stage, that, further, the switching four-poles are in each case actuated alternately in cyclic timing of a carrier frequency oscillation, that, further, the output stage combines the output signals of the two switching four-pole networks, and that the phase of one of the two output signals of the input stage is shifted by 180° either in the input stage or after passing the corresponding switching four-pole network in the output stage

2. Modulator according to claim 1, in which the phase of one of the output signals in the input stage is shifted by 180° with respect to the phase of the other output signal, characterized in that the input stage is designed as a phase reversal stage with outputs which output two antiphase output signals with the same amplitude.

3. Modulator according to claim 1, in which the phase of one of the output signals of the input stage is shifted by 180° in the output stage, characterized in that the output stage is designed as a differential amplifier.

4. Modulator according to claim 1, characterized in that for the actuation of both the switching four-poles, two square pulse sequences with a mutual phase shift of 180°, derived from the carrier oscillation, are provided.

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5. Modulator according to claim 4, characterized in that the ratio of pulse width to interpulse period of the square pulse sequence derived from the carrier oscillation is selected to be less than 1, preferably less than 1/2.

6. Modulator according to one of the preceding claims, characterized in that in the switching four-pole field effect transistors are provided as switching elements.

7. Modulator according to one of the preceding claims, characterized in that the circuit comprises only resistors and semiconductor elements like transistors and diodes.

8. Modulator according to one of the preceding claims, characterized in that the modulator is foreseen especially for use in frequency converting digital filters.

PA 69/2032 2/

21 a 4 14-01 AS: 16.07.1969 OS: 28.01.1971

-11- 1936252

Fig.1

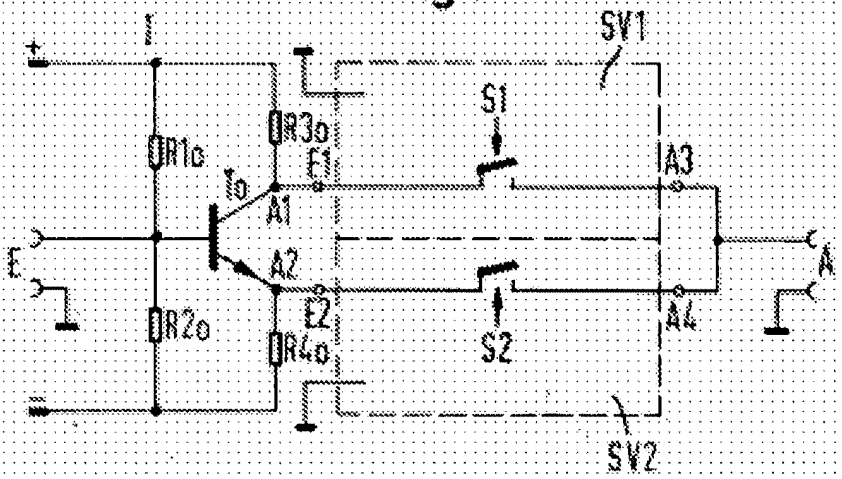
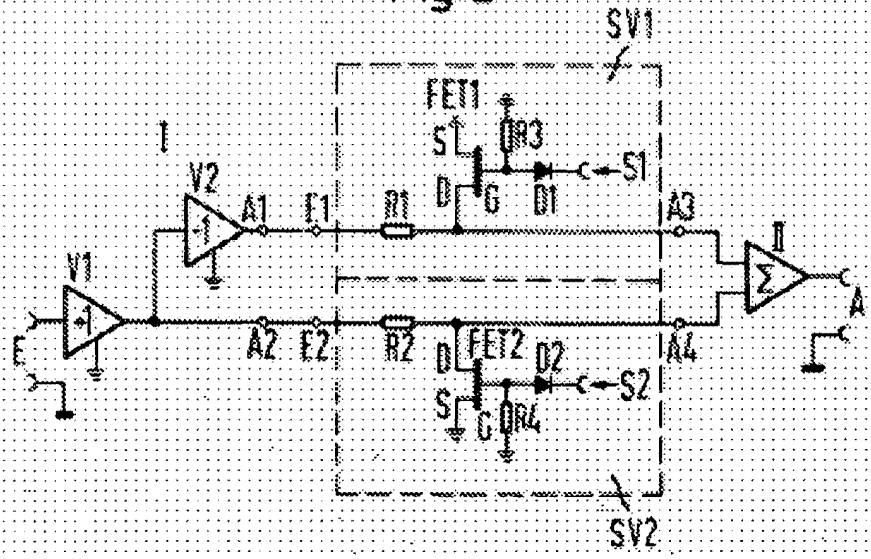


Fig.2



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Fig.3

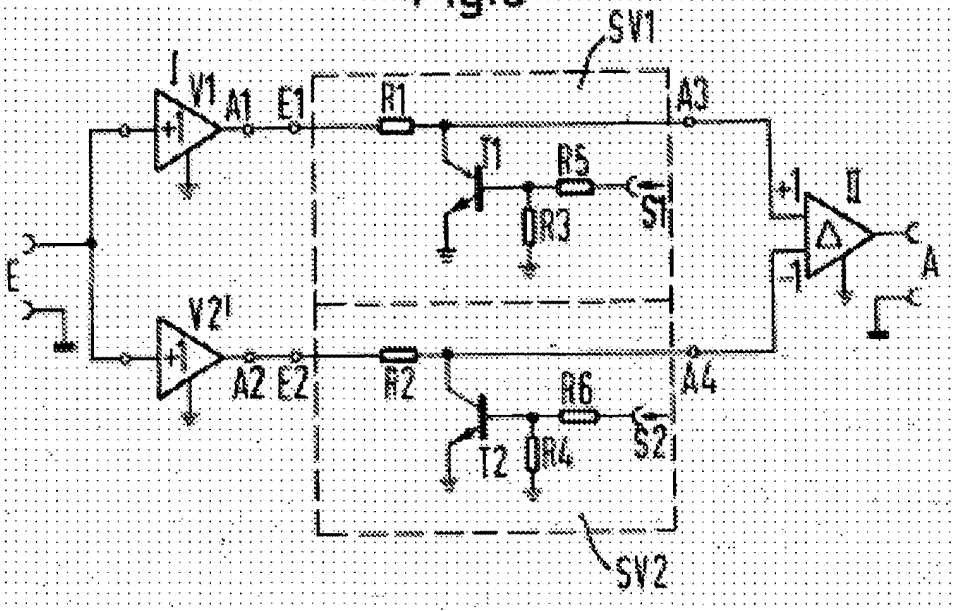


Fig.4

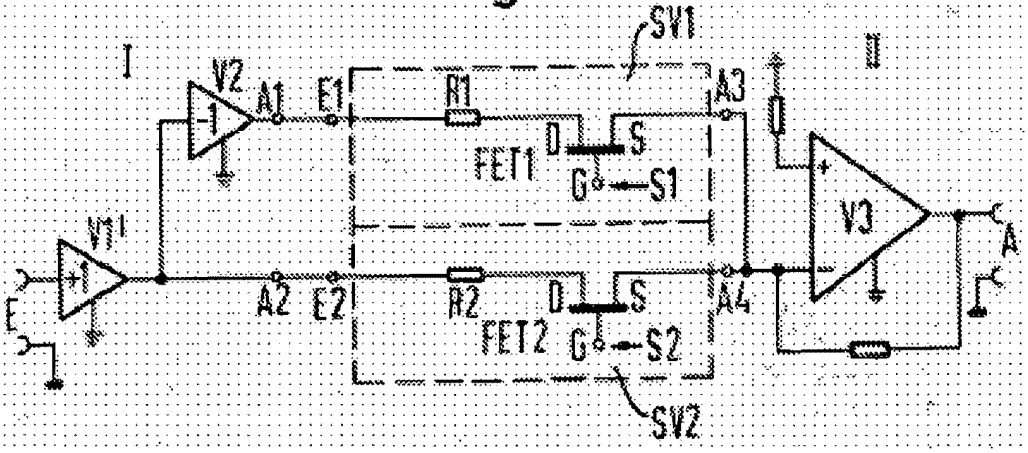
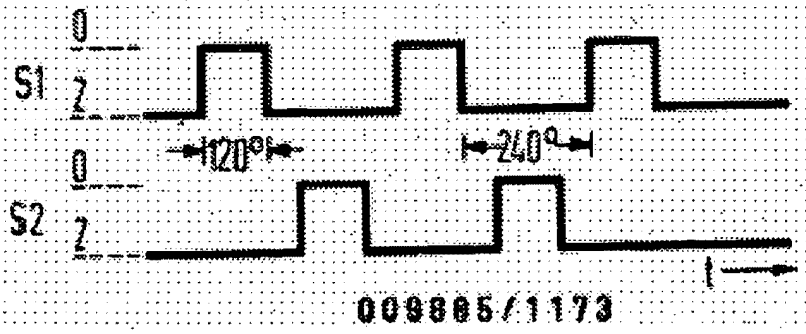


Fig.5



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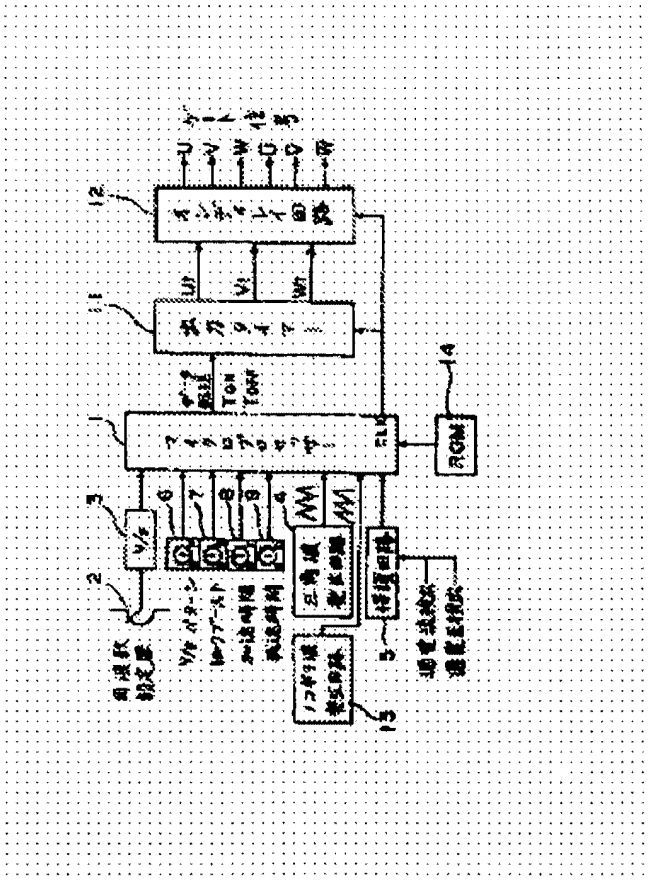
PULSE-WIDTH MODULATION CONTROL SYSTEM OF INVERTER

Patent number: JP62012381
Publication date: 1987-01-21
Inventor: IWASAKI MANABU
Applicant: FUJI ELECTRIC CO LTD
Classification:
- international: ***H02M7/48;*** **H02M7/48;** (IPC1-7): H02M7/48
- european:
Application number: JP19850151737 19850709
Priority number(s): JP19850151737 19850709

Report a data error here

Abstract of **JP62012381**

PURPOSE:To suppress a harmonic wave by switching a pulse-width modulation control wave from a triangular wave to a sawtooth wave when the using frequency of an inverter becomes higher than the prescribed value. CONSTITUTION:A microprocessor 1 inputs a frequency signal through a V/F converter 3 from a frequency setter 2, a modulated triangular wave from a triangular wave generator 4, and a signal from a protecting circuit 5, calculates as prescribed the pulse-width modulation by a program in a ROM 14, ad produces a gate signal through an output timer 11 to a 3-phase inverter. In this case, a sawtooth wave generator 13 is provided in addition to the generator 4, and a program for controlling to modulate by converting the modulation wave from a triangular wave to a sawtooth wave when the set frequency of the setter 2 becomes higher than the prescribed value is provided in the ROM 14. Thus, the triangular wave is modulated in a low frequency band, and the sawtooth wave is modulated in a high frequency band to suppress harmonic waves.



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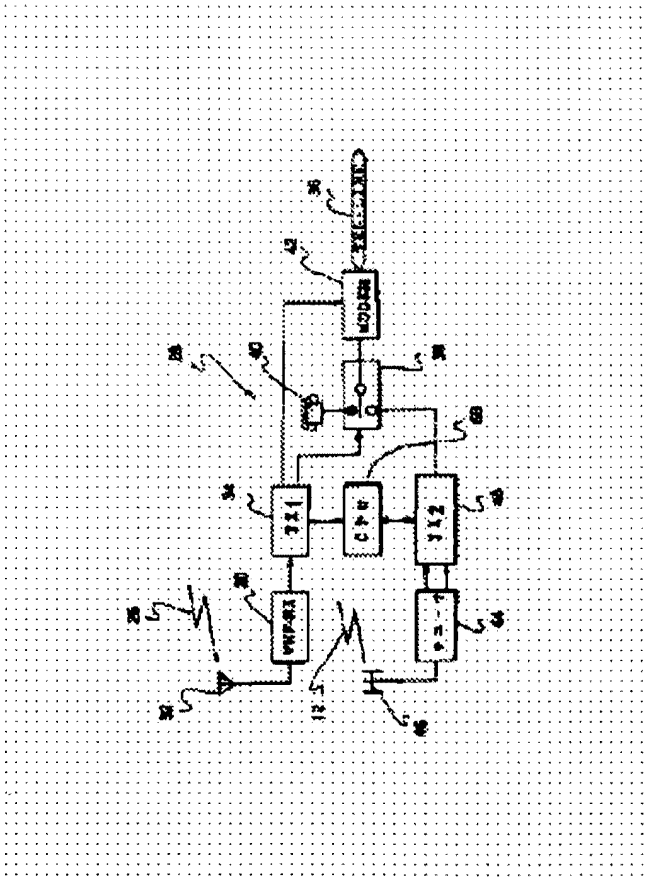
RELAY MONITORING DEVICE FOR BROADCASTING RADIO WAVE

Patent number: JP4154227
Publication date: 1992-05-27
Inventor: NASHIMOTO TAKEKI; MEGURO KIYOMI; WADA YOSHIRO
Applicant: NAGANO HOUSOU KK
Classification:
- international: ***H04B17/00;*** **H04B17/00**; (IPC1-7): H04B17/00
- european:
Application number: JP19900278127 19901017
Priority number(s): JP19900278127 19901017

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Abstract of **JP4154227**

PURPOSE:To collect detailed monitored data by demodulating received broadcasting radio wave, converting the wave to a digital wave, and sending the converted digital wave to an external device. CONSTITUTION:A first sending section 34 modulates a signal representing state change contact point information demodulated by a VHF reception section 30 in order to send the modulated signal to a cable communication (telephone) channel 36 and outputs it. A second sending section 48, in order to send an audio signal demodulated by a tuner 44 in a realtime mode to the communication channel 36, modulates the demodulated audio signal and outputs it. That is, after a reception signal 30 demodulates received broadcasting radio wave and converts the demodulated analog signal digitally, the converted digital signal is sent to an external device via the sending means 48. Thus, a monitor facility installed outside can directly catch up the state of the broadcasting radio wave received by the reception means 30. In particular, in case of television radio wave, since an external monitor device can catch up the state of an image received by the receiving means 30, detailed state and image quality can also be monitored.



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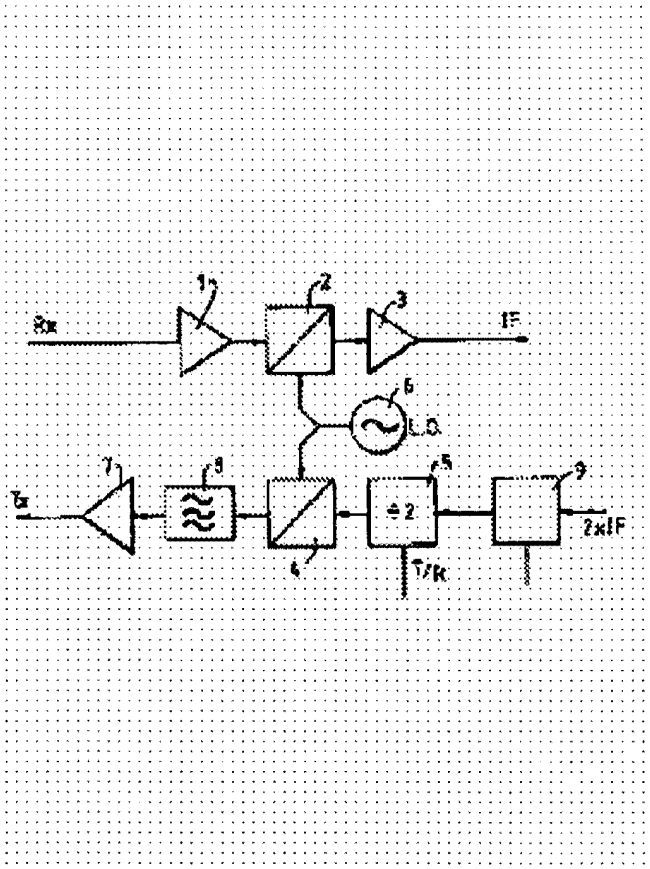
Patent number: JP6284038
Publication date: 1994-10-07
Inventor: ANTONII DEIBUITSUDO UIRIAMUSU
Applicant: PLESSEY SEMICONDUCTORS LTD
Classification:
- International: ***H04B1/40;*** **H04B1/40;** (IPC1-7): H04B1/40; H04B1/04; H04B1/26
- european: H04B1/40C6
Application number: JP19940000272 19940106
Priority number(s): GB19930000280 19930108

Also published as:
EP0605954 (A2)
GB2274222 (A)
EP0605954 (A3)

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Abstract of **JP6284038**

PURPOSE: To use a common local oscillator for down-conversion of a reception signal and up-conversion of an intermediate frequency signal by frequency- dividing a modulation carrier before up-converting the modulation carrier.
CONSTITUTION: A reception signal Rx is given to a down-converter 2 via an RF amplifier 1, and intermediate frequency signal is given to an IF amplifier 3, from which a signal IF is given to an output circuit. Furthermore, a transmission information signal Tx is modulated on a carrier signal with a frequency twice the intermediate frequency at a modulator 9. The modulated carrier signal is given to an UP-converter 4 through a 1/2 frequency divider 5. A common local oscillator 6 is used for the converters 2, 4. An UP conversion signal being an output of the converter 4 is given to an RF amplifier 7 via a band pass filter 8. In this transmitter-receiver, in the case of reception, a bias to the divider 5 is released or no energy is supplied to the divider 5 so as to prevent any IF signal from being produced on a transmission path, and the amplifier 3 amplifies a reception signal without interference from the transmission path.



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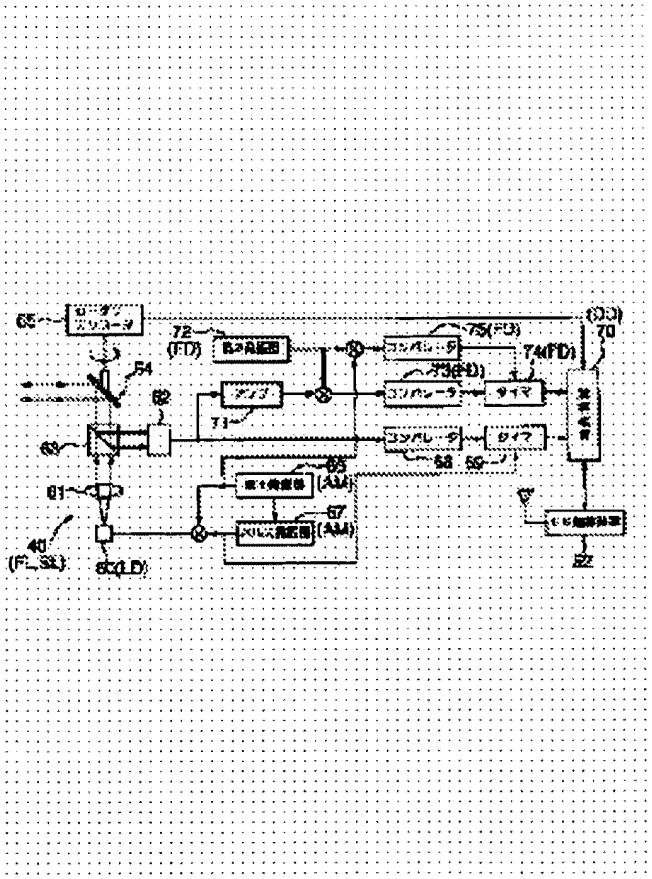
DISTANCE MEASURING DEVICE

Patent number: JP10096778
Publication date: 1998-04-14
Inventor: ADACHI TADASHI
Applicant: KUBOTA KK
Classification:
- international: ***A01B69/00; G01S17/08;*** **A01B69/00; G01S17/00;** (IPC1-7): G01S17/08; A01B69/00
- european:
Application number: JP19960251073 19960924
Priority number(s): JP19960251073 19960924

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Abstract of **JP10096778**

PROBLEM TO BE SOLVED: To improve distance measuring accuracy by making the most of respectrve characteristics of absolute distance information found from measuring information of a timer means by projecting a pulselike beam of light from a first distance measuring light source and distance information found by detecting a phase difference by a phase difference detecting means by applying a beam of light modulated from a second distance measuring light source, and joining them. SOLUTION: A laser position measuring device 40 is constituted so as to make common use of a single light emitting device 60 for a function as a first distance measuring light source FL to project a pulse-like beam of light toward a distance measuring object and a function as a second distance measuring light source SL to project a beam of light modulated by a reference signal of a preset period toward the distance measuring object. An operation device 70 finds absolute distance information from counting time of a timer 69. A phase difference detecting means FD finds a phase difference between a sine wave of a first oscillator 66 and a sine wave signal contained in a detecting signal of a light receiving element 62 from counting time of a timer 74. The operation device 70 finds a distance up to a distance measuring object from the absolute distance information by converting it into a distance corresponding to a phase difference.



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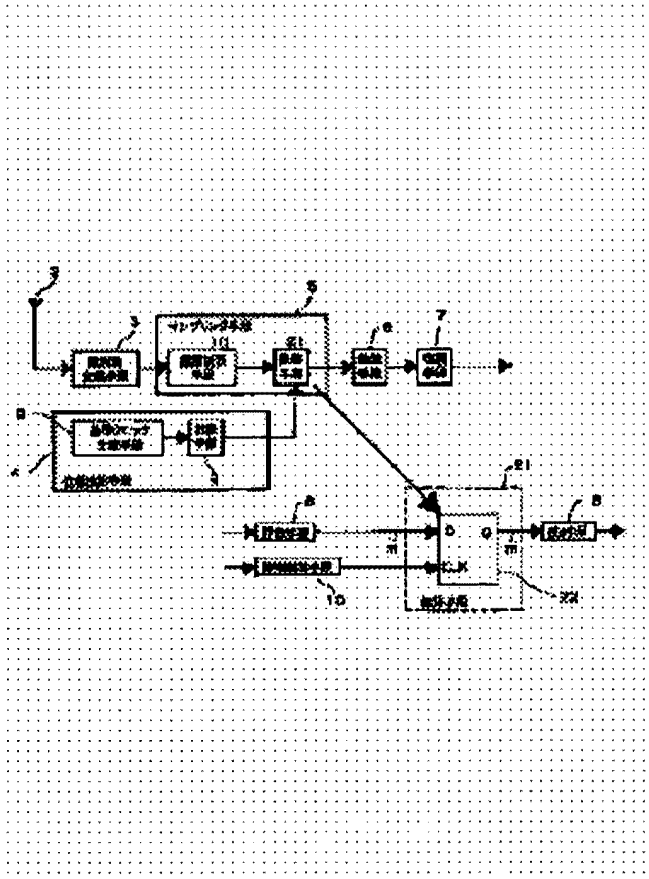
DEMODULATOR FOR DIGITAL RADIO COMMUNICATION

Patent number: JP11098205
Publication date: 1999-04-09
Inventor: NAMEKATA MINORU; KIMURA YASUYUKI
Applicant: TOKYO SHIBAURA ELECTRIC CO
Classification:
- international: ***H04B7/26; H04L27/22;*** **H04B7/26; H04L27/22;** (IPC1-7): H04L27/22; H04B7/26
- european:
Application number: JP19970252486 19970917
Priority number(s): JP19970252486 19970917

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Abstract of **JP11098205**

PROBLEM TO BE SOLVED: To simplify the configuration by converting a frequency-modulated or phase-modulated signal into an intermediate frequency signal and sampling an output of a counter means operated by a prescribed reference clock, based on a reception signal with an intermediate frequency so as to detect and demodulate phase information, thereby eliminating the need for controlling sign discrimination criterion for each information transmission period. SOLUTION: A sampling means 5 is made up of an amplitude limit means 10 that limits an amplitude of the intermediate frequency reception signal outputted from a frequency conversion means 3 and a latch means 21. The latch means 21 is realized by, e.g. a D-type flip-flop 22, its D input terminal connects to an output terminal of a counter means 8, and its CLK input terminal connects to an output terminal of the amplitude control means 10. The D-type flip-flop 22 latches data in m-bit which are phase information of the intermediate frequency reception signal outputted from the counter means 8 at each leading edge of an output signal of the amplitude limit means 10.



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June 6, 2006

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2616

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Third Supplemental Information Disclosure Statement;

2. A listing of the cited documents on Form PTO-1449 (*4 pages*); and

3. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL:apg
Enclosures

540839_1.DOC

OIPE IAP13 JUN 06 2006 PATENT & TRADEMARK OFFICE

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2616
Appl. No.: 10/973,917	Examiner: Chin, Wellington
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Third Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Third Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Second Supplemental Information Disclosure Statement filed on March 28, 2006 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents AC72, AH73, and AI73 are co-owned patents which are directed to related subject matter.

Documents AD72 and AE72 were cited in an Office Action in related U.S. Patent Application No. 11/173,021, filed July 5, 2005, entitled "Method and Circuit for Down-Converting a Signal," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,393,070, which has already been cited in the present application.

Documents AF72-AI72 and AA73-AG73 were cited in an Office Action in related U.S. Patent Application No. 10/305,299, filed November 27, 2002, entitled "Method and Apparatus for Improving Dynamic Range In a Communication System," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,339,459 and 5,517,688, which have already been cited in the present application.

Documents AA74 and AB74 were cited in an Office Action in related U.S. Patent Application No. 10/197,255, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,703,584; 5,887,001; 6,298,065; and 6,850,742; and U.S. Patent Publication Nos. 2002/0080728 and 2002/0163921, which have already been cited in the present application.

Documents AC74-AG74 were cited in an Office Action in related U.S. Patent Application No. 11/068,370, filed March 1, 2005, entitled "Method and System for Frequency Up-Conversion with a Variety of Transmitter Configurations," directed to

related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,903,854 and 5,914,622, which have already been cited in the present application.

Document AH74 was cited in an Office Action in related U.S. Patent Application No. 09/567,977, filed May 10, 2000, entitled "Optical Down-converter Using Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action was Deboo, Gordon J., *Integrated Circuits and Semiconductor Devices*, 2nd Edition, McGraw Hill, Inc., pp. 41-45 (1977), which has already been cited in the present application.

Documents AI74 and AA75 were cited in an Office Action in related U.S. Patent Application No. 10/086,367, filed March 4, 2002, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,091,940, which has already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the

search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☐ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

☒ 7. In accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent publications cited on the attached Form PTO-1449 are not enclosed.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000 (now abandoned), 09/476,093, filed January 3, 2000 (now U.S. Patent No. 7,006,805), 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: June 6, 2006

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

534717_1.DOC

OIPE IAP13 JUN 06 2006 PATENT & TRADEMARK OFFICE

FORM PTO-1449

THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
0744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC72	7,016,663 B2	03/2006	Sorrells *et al.*			
	AD72	3,694,754	09/1972	Baltzer			
	AE72	4,931,716	06/1990	Jovanovic *et al.*			
	AF72	3,617,898	11/1971	Janning, Jr.			
	AG72	3,764,921	10/1973	Huard			
	AH72	4,158,149	06/1979	Otofuji			
	AI72	4,380,828	04/1983	Moon			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
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EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

534711_1.DOC

FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA73	4,562,414	12/1985	Linder *et al.*			
	AB73	4,814,649	03/1989	Young			
	AC73	4,845,389	07/1989	Pyndiah *et al.*			
	AD73	5,172,019	12/1992	Naylor *et al.*			
	AE73	5,263,198	11/1993	Geddes *et al.*			
	AF73	5,551,076	08/1996	Bonn			
	AG73	5,633,610	05/1997	Maekawa *et al.*			
	AH73	7,027,786 B1	04/2006	Smith *et al.*			
	AI73	7,039,372 B1	05/2006	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA74	6,591,310 B1	07/2003	Johnson			
	AB74	6,963,626 B1	11/2005	Shaeffer *et al.*			
	AC74	4,811,422	03/1989	Kahn			
	AD74	5,825,257	10/1998	Klymyshyn *et al.*			
	AE74	5,986,600	11/1999	McEwan			
	AF74	6,865,399 B2	03/2005	Fujioka *et al.*			
	AG74	2006/0039449 A1	02/2006	Fontana *et al.*			
	AH74	5,847,594	12/1998	Mizuno			
	AI74	3,641,442	02/1972	Boucher			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA75	5,140,699	08/1992	Kozak			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
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534711_1.DOC

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September 25, 2006

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2616

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Fourth Supplemental Information Disclosure Statement;

2. A listing of the cited documents on Form PTO-1449 (*3 pages*);

3. Copies of the cited documents (AM25, AJ26, AK26, AQ61, AR61, AN62); and

4. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/JSW:apg
Enclosures

587193_1.DOC

OIPE
SEP 25 2006
PATENT & TRADEMARK OFFICE
IAP48

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2616
Appl. No.: 10/973,917	Examiner: Chin, Wellington
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Fourth Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Fourth Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Third Supplemental Information Disclosure Statement filed on June 6, 2006 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents AM25, AJ26, and AK26 were cited in an Office Action in related Japanese Patent Application No. 2002-048676, filed October 18, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter. Also cited in said Office Action was Japanese Patent Publication No. 60-130203, which has already been cited in the present application.

Documents AB75-AD75 and AC77-AG77 are co-owned patents which are directed to related subject matter.

Document AE75 was cited in an Office Action in related U.S. Patent Application No. 10/197,253, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter.

Document AF75 was cited in an Office Action in related U.S. Patent Application No. 09/550,644, filed April 14, 2000, entitled "Method and System for Down-Converting an Electromagnetic Signal, Transforms for Same, and Aperture Relationships," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,404,758, which has already been cited in the present application.

Documents AG75-AI75 and AA76 were cited in an Office Action in related U.S. Patent Application No. 11/107,861, filed April 18, 2005, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Documents AB76-AF76 were cited in an Office Action in related U.S. Patent Application No. 11/230,732, filed September 21, 2005, entitled "Applications of Universal Frequency Translation," directed to related subject matter. Also cited in said Office Action

were U.S. Patent Nos. 6,208,636 and 7,016,663, which have already been cited in the present application.

Documents AG76-AI76, AA77, and AB77 were cited in a Notice of Allowance in related U.S. Patent Application No. 10/961,253, filed October 12, 2004, entitled "Apparatus, System, and Method for Down Converting and Up Converting Electromagnetic Signals," directed to related subject matter. Also cited in said Notice of Allowance was U.S. Patent No. 6,404,823, which has already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final

Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document AM25 (JP 61-232706) appears to describe a frequency converter for signals. An English language abstract of document AM25 is enclosed as document AQ61.

Document AJ26 (JP 9-171399) appears to describe a sound synthesizing method and circuit. An English language abstract of document AJ26 is enclosed as document AR61.

Document AK26 (JP 10-41860) appears to describe an echo canceller. An English language abstract of document AK26 is enclosed as document AN62.

☒ 7. Copies of documents AM25, AJ26, AK26, AQ61, AR61, and AN62 are enclosed. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent publications cited on the attached Form PTO-1449 are not enclosed.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000 (now abandoned), 09/476,093, filed January 3, 2000 (now U.S. Patent No. 7,006,805), 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817),

in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 9/25/06

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
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SEP 25 2006
PATENT & TRADEMARK OFFICE

FORM PTO-1449

FOURTH SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB75	7,050,508 B2	05/2006	Sorrells *et al.*			
	AC75	7,054,296 B1	05/2006	Sorrells *et al.*			
	AD75	7,065,162 B1	06/2006	Sorrells *et al.*			
	AE75	2003/0149579 A1	08/2003	Begemann *et al.*			
	AF75	5,063,387	11/1991	Mower			
	AG75	5,535,402	07/1996	Leibowitz *et al.*			
	AH75	6,512,785 B1	01/2003	Zhou *et al.*			
	AI75	6,567,483 B1	05/2003	Dent *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM25	JP 61-232706	10/1986	JP			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ61	English-language Abstract of Japanese Patent Publication No. JP 61-232706, data supplied by the espacenet, 1 page (October 17, 1986 - Date of publication of application).
	AR61	English-language Abstract of Japanese Patent Publication No. JP 9-171399, data supplied by the espacenet, 1 page (June 30, 1997 - Date of publication of application).

EXAMINER	DATE CONSIDERED

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FORM PTO-1449

FOURTH SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA76	6,775,684 B1	08/2004	Toyoyama *et al.*			
	AB76	4,740,792	04/1988	Sagey *et al.*			
	AC76	5,239,687	08/1993	Chen			
	AD76	5,552,789	09/1996	Schuermann			
	AE76	5,905,433	05/1999	Wortham			
	AF76	6,647,270 B1	11/2003	Himmelstein			
	AG76	6,034,566	03/2000	Ohe			
	AH76	6,313,700 B1	11/2001	Nishijima *et al.*			
	AI76	6,959,178 B2	10/2005	Macedo *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ26	JP 9-171399	06/1997	JP			No
	AK26	JP 10-41860	02/1998	JP			No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN62	English-language Abstract of Japanese Patent Publication No. JP 10-41860, data supplied by the espacenet, 1 page (February 13, 1998 - Date of publication of application).
	AO	
	AP	
	AQ	
	AR	

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FORM PTO-1449

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ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA77	6,999,747 B2	02/2006	Su			
	AB77	2004/0125879 A1	07/2004	Jaussi *et al.*			
	AC77	7,072,390 B1	07/2006	Sorrells *et al.*			
	AD77	7,072,427 B2	07/2006	Rawlins *et al.*			
	AE77	7,076,011 B2	07/2006	Cook *et al.*			
	AF77	7,082,171 B1	07/2006	Johnson *et al.*			
	AG77	7,085,335 B2	08/2006	Rawlins *et al.*			
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AK						Yes No
	AL						Yes No
	AM						Yes No

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575838_1.DOC

IDS Doc. Ref. AM25
For Appl. No. 10/973,917

⑲日本国特許庁(JP)　⑪特許

⑫公開特許公報(A)　昭61-232706

⑤1Int.Cl.⁴	識別記号	庁内整理番号	㊸公開
H 03 D 7/00		7402-5J	昭和61年(1986)10月17日

審査請求　未請求　発明の数 1　(全5頁)

⑤4発明の名称　信号の周波数変換装置

㉑特　願　昭60-73135
㉒出　願　昭60(1985)4月6日

㉗発明者　宮越　一光　大阪市阿倍野区長池町22番22号　シャープ株式会社内
㉑出願人　シャープ株式会社　大阪市阿倍野区長池町22番22号
㉔代理人　弁理士　西教　圭一郎　外2名

明細書

1、発明の名称

信号の周波数変換装置

2、特許請求の範囲

入力アナログ信号を第1のサンプルホールド周波数でサンプルホールドする第1のサンプルホールド回路と、

第1のサンプルホールド回路からの出力を受信し、この出力信号に含まれる高調波成分のうち、第1高調波のみを通過するバンドパスフィルタと、

バンドパスフィルタからの前記第1高調波を受信し、第1高調波の周波数の2倍より小さい第2のサンプルホールド周波数でサンプルホールドする第2のサンプルホールド回路と、

第2のサンプルホールド回路からの出力を受信し、この出力信号に含まれる低周波成分および高調波成分のうち、低周波成分以上の高域を遮断して低周波成分のみを有する信号を出力するローパスフィルタとを含み、

前記第1および第2のサンプルホールド周波数を制御して入力信号の周波数を変換して出力することを特徴とする信号の周波数変換装置。

3、発明の詳細な説明

産業上の利用分野

本発明は、入力アナログ信号の周波数を変換して出力する装置に関する。

背景技術

従来からたとえば、通信機器などに用いられるアナログ入力信号の周波数を変換する装置では、一定周波数の信号を混合し入力アナログ周波数との差の周波数を取出して出力している。また入力アナログ信号を一旦デジテル信号に変換し、デジタル処理によって信号周期を変換し、この変換された周波数を有するデータ値を再びアナログ信号に変換して出力している。

発明が解決しようとする問題点

上記先行技術では、周波数を変換するための回路の構成が非常に複雑になる。

本発明の目的は、簡単な回路構成でしかも入力アナログ信号の周波数を任意に変換して出力する

ことができる信号の周波数変換装置を提供することである。

問題点を解決するための手段

本発明は、入力アナログ信号を第1のサンプルホールド周波数でサンプルホールドする第1のサンプルホールド回路と、

第1のサンプルホールド回路からの出力を受信し、この出力信号に含まれる高調波成分のうち、第1高調波のみを沪波するバンドパスフィルタと、

バンドパスフィルタからの前記第1高調波を受信し、第1高調波の周波数の2倍より小さい第2のサンプルホールド周波数でサンプルホールドする第2のサンプルホールド回路と、

第2のサンプルホールド回路からの出力を受信し、この出力信号に含まれる低周波成分および高調波成分のうち、低周波成分以上の高域を遮断して低周波成分のみを有する信号を出力するローパスフィルタとを含み、

前記第1および第2のサンプルホールド周波数を制御して入力信号の周波数を変換して出力することを特徴とする信号の周波数変換装置である。

作　用

本発明に従えば、周波数が変換されるべき入力アナログ信号が第1のサンプルホールド回路によってサンプルホールドされ、入力信号に関連する高調波成分を有する信号が出力される。この高調波成分を有する信号は、バンドパスフィルタに与えられ、このバンドパスフィルタによって前記高調波成分のうち、第1高調波成分のみが沪波される。そしてこの第1高調波を有する信号はバンドパスフィルタから第2のサンプルホールド回路に与えられる。第2のサンプルホールド回路では第1高調波の周波数の2倍よりも小さい周波数を有するサンプルホールド周波数でサンプルホールドを行なう。これによって第2のサンプルホールド回路からは、低周波成分および高調波成分が発生し、これらの周波数を有する信号はローパスフィルタに与えられる。ローパスフィルタでは、入力信号のうち、低周波成分以上の高域成分を遮断して、低周波成分のみを導出する。これによって入力信号の周波数が第1のサンプルホールド周波数によって減算され、さらに第2のサンプルホールド周波数によって加算されて、入力信号の周波数が変換されて出力されることになる。さらに第1のサンプルホールド周波数および第2のサンプルホールド周波数は任意に調整されるため、入力信号を所望の周波数に変換して出力することが可能となる。

実施例

第1図は、本発明に従う信号周波数変換装置1のブロック図である。この周波数変換装置1は、基本的には周波数が変換されるべき入力アナログ信号を受信してサンプルホールドする第1のサンプルホールド回路SH1と、このサンプルホールド回路SH1からの信号を受信して予め定めた帯域のみを沪波するバンドパスフィルタ2と、バンドパスフィルタ2からの出力を受信してサンプルホールドする第2のサンプルホールド回路SH2と、このサンプルホールド回路SH2からの出力を受信して予め定めた周波数以下の低域のみを沪波するローパスフィルタ3とを含む。

ここで入力アナログ信号の周波数スペクトルは、第2図(1)で示されるように中心周波数がfaである信号であるものと想定する。入力信号はサンプルホールド回路SH1によりサンプルホールド周波数fs1でサンプルホールドされる。このとき、出力パルス幅を第3図(1)に示すようにサンプルホールド周期と同じ幅にすると、サンプルホールド回路SH1からの出力波形の周波数スペクトルは、第2図(2)で示されるように高調波成分の減衰率が大きくなる。そこで第3図(2)で示されるようにパルス幅をサンプルホールド周期のより狭くすると、サンプルホールド回路SH1の出力波形は、第2図(3)の周波数スペクトルを持つ信号となり、第1高調波成分の減衰率を小さくすることができる。したがって本発明に用いられるサンプルホールド回路SH1の出力パルス幅は、サンプルホールド周期のより狭くすべきである。しかしながらパルス幅が狭い程高調波成分の減衰率は小さくなるが、信号パワーが小さくなって高いS

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／Ｎ比を確保できない可能性があり、そのためパルス幅は２分の１程度が最適であると考えれる。

このような理由に基づいて本発明で用いられるサンプルホールド回路ＳＨ１は、第４図に示される回路構成を有するものが用いられる。入力アナログ信号がラインℓ１からバッファアンプＡ１に与えられ、スイッチＳＷ１を介してもう１つのバッファアンプＡ２に与えられ、さらにこのバッファアンプＡ２の出力はスイッチＳＷ２を介してラインℓ２からバンドパスフィルタ２に導出される。スイッチＳＷ１とバッファアンプＡ２の間には、積分形コンデンサＣ１が接続される。クロック信号発生器４からのクロック信号は、スイッチＳＷ１，ＳＷ２に与えられる。クロック信号がハイレベルであるときには、スイッチＳＷ１はオン状態であり、またスイッチＳＷ２の共通接点ｐ１は個別接点ｑ２と導通しており、したがって入力信号はコンデンサＣ１に充電される。クロック信号がローレベルであるときには、スイッチＳＷ１はオフの状態となり、スイッチＳＷ２の共通接点ｐ１は切換えられて個別接点ｑ１に導通する。これによって、コンデンサＣ１は放電されてラインℓ２から出力される。

サンプルホールド回路ＳＨ２もまたサンプルホールド回路ＳＨ１と同様な構成を有している。

バンドパスフィルタ２は、第２図(４)における破線で示される帯域のみを沪波するように予め設定されている。そのため、ラインℓ２を介して与えられる高調波成分のうち第１高調波成分のみが沪波され、第２図(５)で示される第１高調波成分のみがサンプルホールド回路ＳＨ２に与えられる。サンプルホールド回路ＳＨ２では、サンプルホールド周波数ｆｓ２によってサンプルホールドされる。なおこのサンプルホールド回路ＳＨ２の出力パルス幅は、サンプルホールド回路ＳＨ１と同様にサンプルホールド周期の２分の１程度に選ばれる。しかもこのサンプルホールド回路ＳＨ２のサンプルホールド周波数ｆｓ２は、前記第１高調波の周波数の２倍よりも小さい周波数に選ばれており、そのためサンプルホールド回路ＳＨ２からの出力信号は第２図(６)で示されように高調波成分以外にも、低周波成分をも有している。ローパスフィルタ３では、前記低周波成分以上の高調波成分を遮断するような周波数特性を持つように予め設定されており、そのためローパスフィルタ３によって高調波成分が除去され、第２図(７)で示す周波数スペクトルを有する信号がラインℓ３から導出される。こうしてラインℓ１を介して与えられる入力アナログ信号がラインℓ３から周波数を変換して出力される。

入力信号の中心周波数ｆａと、出力信号の中心周波数ｆｂと、サンプルホールド周波数ｆｓ１，ｆｓ２との間には第１式の関係が成立する。

$$f_b = f_a - f_{s1} + f_{s2} \quad \cdots (1)$$

第１式から明らかなように、入力信号の周波数ｆａが第１のサンプルホールド周波数ｆｓ１によって減算され、さらに第２のサンプルホールド周波数ｆｓ２によって加算され、周波数ｆｂを有する信号に変換されて出力されることになる。したがってこのサンプルホールド周波数ｆｓ１，ｆｓ２を任意に調整し、かつこの調整された周波数に応じてバンドパスフィルタ２およびローパスフィルタ３の周波数特性をも変えることによって、入力信号を任意の周波数に変換して出力することが可能となる。

なおサンプルホールドを行なうクロック信号は、パルス波形でよいため、クロック周波数の制御が容易であり、たとえばクロック信号発生器４にプログラマカウンタなどを用いれば、分周比の設定によってクロック周波数を容易に制御できるため、変換周波数の設定をデジタル的に行なうことが可能となる。

発明の効果

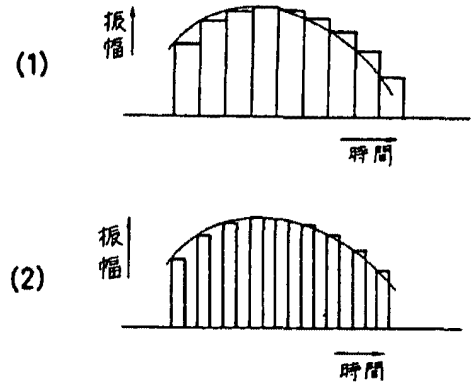
以上のように本発明によれば、簡単な回路構成でしかも入力アナログ信号の周波数を任意に変換して出力することが可能となる。

４、図面の簡単な説明

第１図は本発明に従う信号の周波数変換装置１のブロック図、第２図は本発明の動作を説明するための信号の周波数スペクトルを示す図、第３図はサンプルホールド回路によってサンプルホール

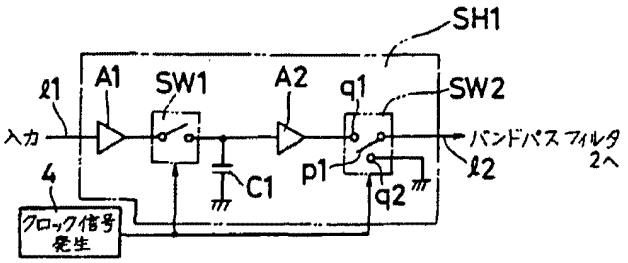
ドが行なわれたときの波形図、第4図はサンプルホールド回路SH1の具体的な回路図である。

1…信号周波数変換装置、2…バンドパスフィルタ、3…ローパスフィルタ、4…クロック信号発生器、SH1,SH2…サンプルホールド回路、ℓ1～ℓ3…ライン

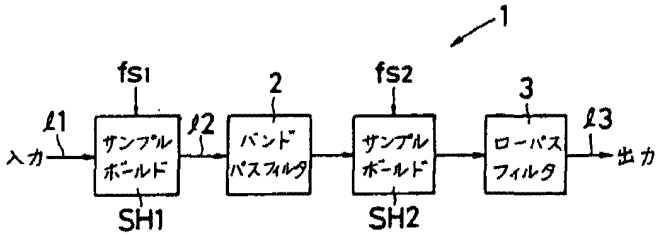


第3図

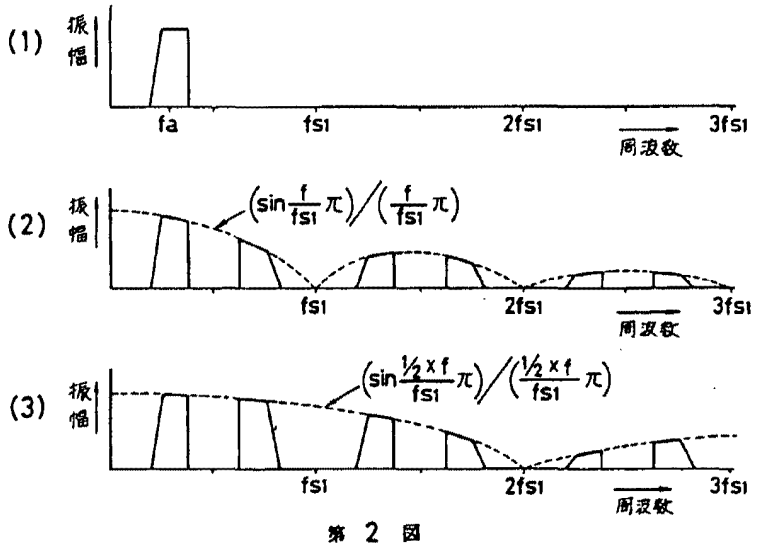
代理人　弁理士　西教　圭一郎



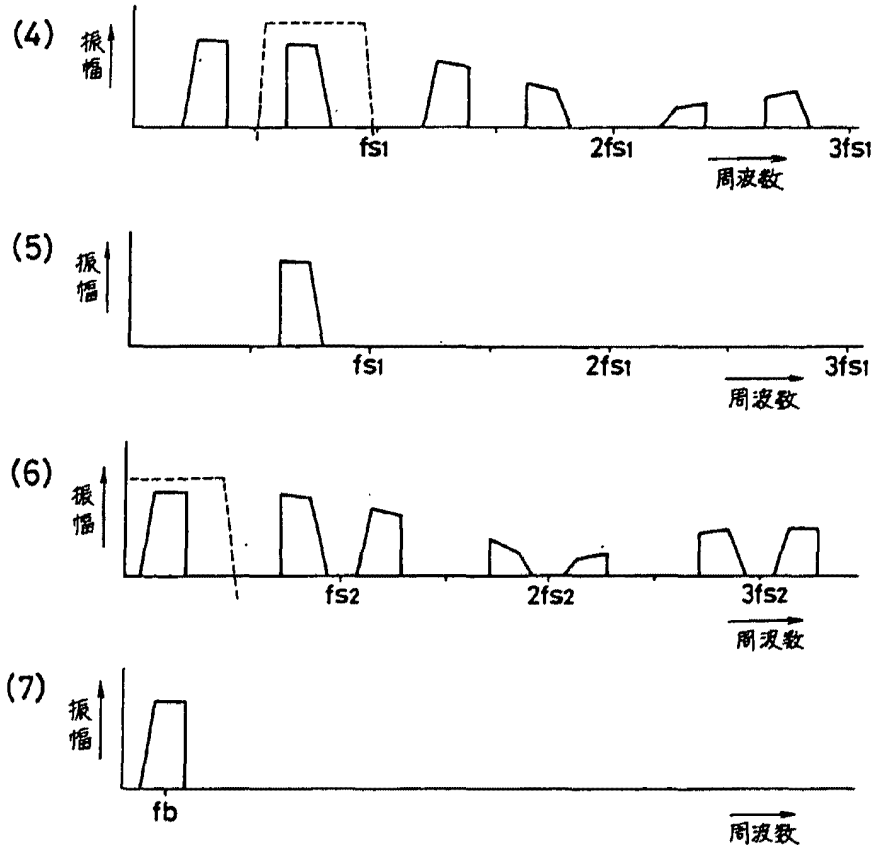
第4図



第1図



第2図


(4)
振幅
fs1
2fs1
3fs1
周波数
(5)
振幅
fs1
2fs1
3fs1
周波数
(6)
振幅
fs2
2fs2
3fs2
周波数
(7)
振幅
fb
周波数

第 2 図

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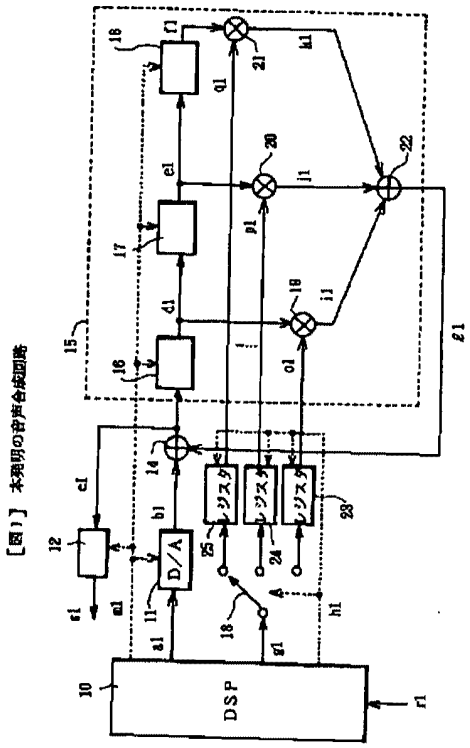
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(54)【発明の名称】　音声合成方法及びその合成回路

(57)【要約】
【課題】　演算量や消費電力を低減することにある。
【解決手段】　ＤＳＰ１０から出力する音源信号をＤ／Ａ変換器１１でアナログ変換し、アナログ音源信号と予測信号を加算器１４で加算して合成音声信号を出力しサンプルホールド回路１２でホールドした合成音声信号を出力する。予測信号の合成は、合成音声信号をアナログ遅延回路１６～１８で遅延させて複数の遅延合成音声信号を出力し、ＤＳＰ１０から出力する線形予測係数を切替器１３及びレジスタ２３～２５を通して重み係数として入力し、アナログ重み付け回路１９～２１により前記遅延合成音声信号に重み付けし、この複数の重み付け遅延合成音声信号をアナログ合成器２２で合成して予測信号を出力する。



【図１】本発明の音声合成回路

【特許請求の範囲】

【請求項1】　合成音声信号を遅延させて複数の遅延合成音声信号を生成し、線形予測係数を重み付け係数として前記遅延合成音声信号を重み付け合成して予測信号を出力し、入力音源信号をアナログ変換し、該アナログ変換した音源信号と前記予測信号とを加算して合成音声信号を出力することを特徴とする音声合成方法。

【請求項2】　音源信号と下記重み付け合成回路の出力である予測信号とを加算してその結果である合成音声信号を出力する加算器と、該加算器の出力する合成音声信号を遅延させて複数のタップ出力として出力する遅延回路と、線形予測係数を重み付け係数として前記該遅延回路のそれぞれのタップ出力を重み付け合成しその結果として予測信号を出力する重み付け合成回路とから構成される線形予測分析による音声合成回路において、

前記遅延回路および重み付け合成回路の少なくとも1つはアナログ回路を用いて構成されたことを特徴とする音声合成回路。

【請求項3】　前記アナログ遅延回路は、多段のサンプルホールド回路で構成されたことを特徴とする請求項2記載の音声合成回路。

【請求項4】　前記アナログ重み付け合成回路は、重み付けインピーダンス合成回路であることを特徴とする請求項2記載の音声合成回路。

【請求項5】　合成音声信号を所定のタイミングでシフトし線形予測分析次数pに対応するp段の遅延合成音声信号を出力するアナログ回路により構成された遅延回路と、線形予測係数を重み付け係数として前記遅延回路のp段の遅延合成音声信号にそれぞれ重み付けを行い重み付けされたp個の遅延合成音声信号を出力するp個のアナログ回路により構成された重み付け回路と、該重み付け回路の出力である重み付けされたp個の遅延合成音声信号を合成して、音源信号と加算することにより前記合成音声信号を生成するための予測信号を出力するアナログ回路により構成された合成器とで構成されたことを特徴とする音声合成回路。

【請求項6】　音声信号を入力し線形予測分析を実行して線形予測係数と音源信号を計算、または線形予測係数情報と音源信号情報を伝送路またはメモリから入力して線形予測係数と音源信号を出力するＤＳＰと、

該ＤＳＰより出力されるディジタル形式の音源信号をアナログ信号に変換し出力するＤ／Ａ変換器と、

該Ｄ／Ａ変換器の出力である音源信号とアナログ回路により構成された合成回路の出力である予測信号を加算して合成音声信号を出力する加算器と、

該加算器の出力である合成音声信号を所定のタイミングでホールドして出力するサンプルホールド回路とを備えて成り、

かつ、前記合成回路は、前記加算器の出力である合成音声信号を所定のタイミングでシフトし線形予測分析次数pに対応するp段の遅延合成音声信号を出力するアナログ回路により構成された遅延回路と、

前記ＤＳＰからの出力である線形予測係数を入力し各係数毎に別々のレジスタ回路に書き込むために出力を切り替える切り替え器と、

該切り替え器からの出力である線形予測係数を入力し一次的に蓄える線形予測分析次数pに対応するp個のレジスタ回路と、

該p個のレジスタ回路からの出力を重み付け係数として前記遅延回路のp段の遅延合成音声信号にそれぞれ重み付けを行い重み付けされたp個の遅延合成音声信号を出力するp個のアナログ回路により構成された重み付け回路と、

該重み付け回路の出力である重み付けされたp個の遅延合成音声信号を合成して予測信号を出力するアナログ回路により構成された合成器とで構成されたことを特徴とする音声合成回路。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、音声符復号化装置や音声合成装置に用いられる音声合成方法及び合成回路に関するものである。

【０００２】

【従来の技術】線形予測分析による音声合成回路は、ＤＳＰ（ディジタル・シグナル・プロセッサ）によりディジタル処理で実現されている。

【０００３】一般的に、音声符復号化装置や音声合成装置で用いられる線形予測分析による音声合成回路では、音源信号を数1式の全極型ディジタルフィルタＨ（ｚ）に入力し、出力として合成音声を得る。フィルタの重み係数としては線形予測係数を用い、分析フレーム（10～30ｍｓ）毎に重み係数を更新する。

【０００４】

【数1】

［数1］

$$H(z)=\frac{1}{Ap(z)},\quad Ap(z)=1+\alpha_1 Z^{-1}+\alpha_2 Z^{-2}+\cdots\cdots+\alpha_p Z^{-p}$$

$$Z=e^{j\lambda},\quad \lambda=2\pi f T,\quad T=\text{サンプリング周期}$$

【０００５】ここで、a_1、a_2、…、a_pは線形予測係数であり、分析次数ｐ＝10次が用いられる。数1で表される音声合成回路は、音源信号に声道特性（音声のスペクトル包絡特性）を付加する機能を持つ。音源信号

と、重み付け合成回路での重み付け係数として用いられる線形予測係数は、線形予測分析（公知の技術）により求められる。

【0006】数1式の構成は図1に示すようにＩＩＲフィルタとなる。同図において、Z^{-1}は遅延因子であり、遅延回路により遅延された合成音声を線形予測係数に（－1）を乗算した$-a_1$、$-a_2$、…、$-a_p$を重み係数として用いて、重み付け合成する。重み係数である線形予測係数は、分析フレーム（１０～３０ｍｓ）毎に更新される。現状では、これをＤＳＰによりソフト的に実現している。

【0007】

【発明が解決しようとする課題】ここで問題となるのは、この合成処理に必要な演算量がＤＳＰにとって負担になることである。即ち、サンプリング周波数を８０００Ｈｚ、1フレーム長を１０ｍｓ（８０サンプル）、分析次数を１０次とすれば、１フレーム内の演算量は、２０（積和算１０回（タップ数）、シフト１０回）＊８０（サンプル数）＝１６００回となる。この演算量は、ＤＳＰの消費電力を増加させる。また、これを携帯端末に用いる場合、通話時間が著しく制限されるなどの問題がある。

【0008】本発明の目的は、このＤＳＰの演算量や消費電力の増大の問題を解決することにある。

【0009】

【課題を解決するための手段】前記の目的は、携帯端末の低消費電力化を狙い、遅延回路、重み付け合成回路について低消費電力のアナログ回路を用いることによって達成される。

【0010】また、前記の目的は、入力信号である音源信号と重み付け合成回路の出力である予測信号を加算して、その結果である合成音声信号を出力する加算器と、該合成音声信号を遅延させ複数のタップ出力として出力する遅延回路と、線形予測係数を重み付け係数として前記遅延回路のそれぞれのタップ出力を重み付け合成し、その結果として予測信号を出力する重み付け合成回路とから構成される線形予測分析による音声合成回路において、前記遅延回路および重み付け合成回路の少なくとも1つをアナログ回路を用いて構成したことによって達成される。

【0011】前記の手段によると、線形予測分析による音声合成回路において遅延回路、重み付け合成回路をアナログ回路により実現することにより、音声合成回路の消費電力を低減することができ、これを携帯端末に使用した場合、通話時間を長く保つことができる。

【0012】

【発明の実施の形態】図1は本発明の線形予測係数を用いた音声合成回路の一実施形態を示す。ＤＳＰ１０は、本装置が音声符復号装置に用いられる場合は、入力ｒ１として音声信号を入力し、線形予測分析を実行し、線形予測係数と音源信号を計算する、または、入力ｒ１として線形予測係数情報と音源信号情報を伝送路から受信するとともに、後述するアナログ回路を制御するための種々の制御信号を生成する。また、本装置が音声合成装置に用いられる場合は、入力ｒ１としてメモリ等に記憶されている線形予測係数と音源信号の情報を入力するとともに、後述するアナログ回路を制御するための種々の制御信号を生成する。点線の枠で囲まれた部分１５、サンプルホールド回路１２、および加算器１４がアナログ回路で構成される部分である。

【0013】ＤＳＰ１０より音源信号ａ１がディジタル系列で出力され、Ｄ／Ａ変換器１１によりアナログ信号ｂ１に変換される。この時の変換速度は、サンプリング周波数８０００Ｈｚとし、クロックｍ１により与えられる。アナログに変換された音源信号ｂ１は、加算器１４により、後述する予測信号１１と加算され、合成音声信号ｃ１となる。合成音声信号ｃ１はサンプルホールド回路１２により所定のサンプリング間隔でホールドされ、その出力であるｐ１は、ＬＰＦを施された後、合成音声としてスピーカより出力される（全体的なタイミングについては後で説明する）。

【0014】遅延回路は、サンプルホールド回路１６，１７，１８，…により構成される（実際には、分析次数ｐ（ｐ＝１０）分の個数が存在する）。遅延回路は、合成音声信号ｃ１を遅延させ、タップ出力として、ｄ１，ｅ１，ｆ１，…を出力する。ここで、遅延回路のタップ数は、線形予測分析次数（１０次）に対応し、１０タップ構成とする。シフトタイミングは、クロックｍ１により与えられる。重み付け合成器は、重み付け回路（乗算器）１９，２０，２１，…と合成器２２により構成される（実際には、分析次数ｐ（ｐ＝１０）分の個数が存在する）。タップ出力ｄ１，ｅ１，ｆ１，…はそれぞれ重み付け回路（乗算器）１９，２０，２１，…により重み付けされた後、合成器２２により合成され予測信号１１が出力される。

【0015】ここで、各重み付け回路１９，２０，２１，…に入力される重み付け係数（線形予測係数）ｏ１，ｐ１，ｑ１，…は、レジスタ回路２３，２４，２５，…（レジスタ回路についても実際には分析次数分の個数が存在する）からの出力であり、フレーム（ここで、フレームとは線形予測係数、音源信号情報を抽出する時間単位（分析フレーム）を意味する）の先頭で更新され、次のフレームが来るまで固定される。ｏ１は線形予測係数$-a_1$、ｐ１は線形予測係数$-a_2$、ｑ１は線形予測係数$-a_3$に対応する。

【0016】線形予測係数$-a_1$，$-a_2$，$-a_3$，…，$-a_p$のレジスタ回路へのセットは以下のように行われる。フレームの先頭で、ＤＳＰ１０からのディジタル形式の線形予測係数ｇ１が出力され、制御信号ｈ１に基づき、切り替え器１３を切り替えながらレジスタ回路２

3，24，25，…にセットされる。セットの順番は、レジスタ回路23，24，25，…（遅延の小さい順に並んでいる遅延回路タップに対応）に対し、$-a_1$，$-a_2$，$-a_3$，…，$-a_p$（p＝10）のように次数の低い順にセットする。

【0017】各線形予測係数g1はnビット（例えばn＝16）の精度で符号化されている。これらを一時的に記憶するため、各レジスタ回路はnビット分のメモリを有している。これらのレジスタ回路への書き込みは、DSP10から線形予測係数出力の形態に合わせ、パラレルまたはシリアルで行われる。これらのレジスタ回路の内容の更新は、フレームの先頭で行われ、次のフレームの先頭が来るまで固定される。このタイミングについて後に説明する。

【0018】次に、重み付け回路19，20，21，…の構成を図2に示す。a2は重み付けされる入力であり、図1のd1，e1，f1に対応する。Z_i（i＝1，…，n）30，31，…，3nは入力側のインピーダンスであり、数2に示すようにコンデンサで構成される。

【0019】

【数2】

［数2］

$$Z_i=\frac{1}{j\omega c_i}\quad(i=1,\ 2\cdots\cdots n)$$

【0020】ここで、nは線形予測係数の精度に対応し、n＝16とする。各コンデンサC_i（i＝1，…，n）の容量は線形予測係数のMSBに近いほど大きな値をもっている。重み付け制御信号f2は図1の各レジスタ回路23，24，25からの出力である重み付け係数（線形予測係数）o1，p1，q1（各nビットで構成されている）に対応し、各ビットの値により図2のスイッチ40，41，…，4nをON／OFFする。これにより、Z_i（i＝1，…，n）またはC_i（i＝1，…，n）の総和の値を制御する。出力e2はアンプ51を通して出力し、この出力e2に対する帰還インピーダンスZ_f52は数3で表現される。

【0021】

【数3】

［数3］

$$Z_f=\frac{1}{j\omega c_f}$$

【0022】この重み付け回路の利得Gは、数4となる。

【0023】

【数4】

［数4］

$$G=-\frac{\sum_i c_i}{c_f}$$

$i\in$ ON

【0024】重み付けされた出力e2は、図1でi1，j1，k1，…に対応し、これらは同図の合成器22により加算され、予測信号11として出力される。

【0025】次に、図1においてサンプルホールド回路16，17，18，…により構成されるアナログ遅延回路の構成を図3に示す。図3はアナログ遅延回路の構成例であり、バッファ101，105と、サンプルホールド回路102～104とで構成されており、TP_1～TP_nはシフトした信号の出力端子である（図1のd1，e1，f1，…に対応する）。入力信号V_{in}は、バッファ101を経由して1段目のサンプルホールド回路102に入力される。1段目のサンプルホールド回路102ではクロックCKの立ち上がりに同期して入力信号をサンプル保持してTP_1に出力する。2段目のサンプルホールド回路103も同様に前段のサンプルホールド回路102の出力をサンプルして、そのまま次段に1クロック遅らせてTP_2に出力している。3段目以降も同様に1段について1クロックずつ信号をシフトさせn段のアナログシフトレジスタとして動作し、TP_3～TP_nに出力する。

【0026】図4はサンプルホールド回路の構成例を、図5，6はバッファの構成例を示している。図4はバッファ201，204，207とCKがLの時にONになりHの時にOFFになるスイッチ202と、CKがHの時にONになりLの時にOFFになるスイッチ205と、コンデンサ203，206とで構成される。このサンプルホールド回路の動作を図7を用いて説明する。

【0027】入力信号S_{in}はバッファ201を経由し、クロックCKがLでスイッチ202がONの時はコンデンサ203に信号が伝達され、クロックCKがHでスイッチ202がOFFになるとコンデンサ203に入力された信号は保持される。このときの入力信号S_{in}に対するコンデンサ203の動作をバッファ204を経由した出力をA点としている。同様にクロックCKがHでスイッチ205がONの時はコンデンサ206に信号が伝達され、クロックCKがLでスイッチ205がOFFになるとコンデンサ206に入力された信号は保持され、バッファ207を経由して出力信号S_{out}となる。

【0028】図5，6はバッファの構成例で、図5はオペアンプ301を用いたボルテージホロワ回路、図6はインピーダンス素子401，402とオペアンプ403で構成した反転バッファである。

【0029】これらバッファ，サンプルホールド回路

は、ともに公知の技術として知られている。アナログ遅延回路は、これら公知の技術を組み合わせる事により容易に構成が可能である。

【００３０】図８に本発明の動作説明を示す。同図（ａ）はクロックｍ１に基づいて行われるＤ／Ａ変換器１１の変換結果の出力及び遅延回路のシフトタイミングを示す。これは、入力音声のサンプリング周波数（８０００Ｈｚ）に対応する。同図（ｂ）は、レジスタ回路２３，２４，２５における線形予測係数の更新・固定のタイミングを示す。この実施例では、分析フレームの最初のサンプル区間（０．０１２５ｍｓ）の先頭から１／４以内（３．１２５μｓ以内）に$-a_1$，$-a_2$，…，$-a_p$（ｐ＝１０）の更新が行われる。その後、そのフレーム中は、$-a_1$，$-a_2$，…，$-a_p$（ｐ＝１０）は固定され、重み付け合成での重み係数として使用される。同図（ｃ）は、サンプルホールド回路１２により合成音声信号ｃ１をホールドするタイミングを示す。その出力であるｓ１は、同図（ｄ）のように変化する。これにＬＰＦを施せば、アナログの音声信号となり、スピーカから聞くことができる。

【００３１】

【発明の効果】以上のように本発明によれば、１フレーム当たりのＤＳＰ演算量はクロックｍ１、音源信号ａ１、線形予測係数ｇ１および制御信号ｈ１を出力するための処理のみとなり、８０（サンプル数）＊２＋１０（分析次数）＝１７０回であり、従来のＤＳＰ１６００回の１／１０となり、これにより他のアナログ回路も低消費電力で実現可能である。このように線形予測分析による音声合成回路において遅延回路、重み付け合成回路をアナログ回路により実現することにより、音声合成回路の消費電力を低減することができ、これを携帯端末に使用した場合、通話時間を長く保つことができる。

【図面の簡単な説明】

【図１】本発明の一実施形態の音声合成回路図。

【図２】図１の重み付け回路図。

【図３】図１のアナログ遅延回路図。

【図４】図３のサンプルホールド回路図。

【図５】図３のバッファ回路図。

【図６】図３のバッファ回路図。

【図７】図３の動作説明図。

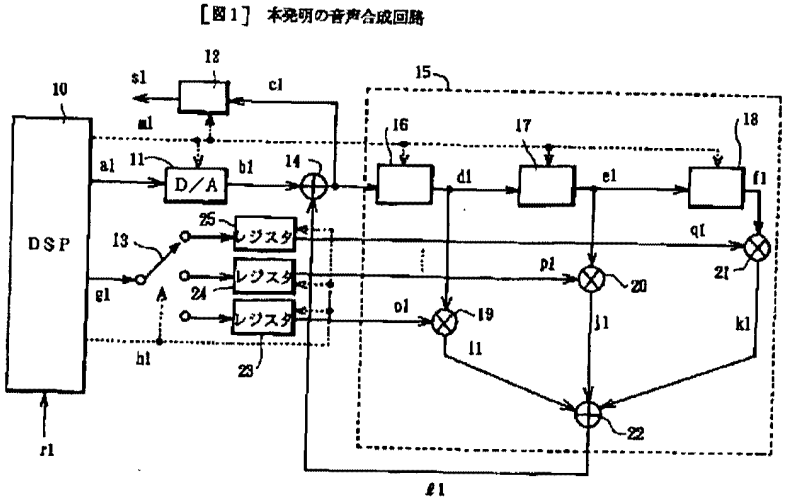
【図８】本発明の一実施形態の動作説明図。

【図９】従来の音声合成回路図。

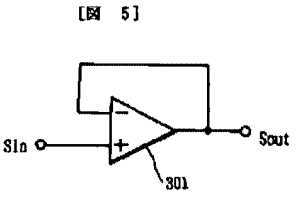
【符号の説明】

１０…ＤＳＰ、１１…Ｄ／Ａ変換器、１２…サンプルホールド回路、１３…切替器、１４…加算器、１６～１８…サンプルホールド回路、１９～２１…重み付け回路、２２…合成器、２３～２５…レジスタ、３０～３ｎ…入力側インピーダンス、４０～４ｎ…スイッチ、５１…アンプ、５２…帰還インピーダンス、１０１，１０５…バッファ、１０２～１０ｎ…サンプルホールド回路、２０１，２０４，２０７…バッファ、２０２，２０５…スイッチ、２０３，２０６…コンデンサ、４０１，４０２…インピーダンス素子、３０１，４０３…オペアンプ。

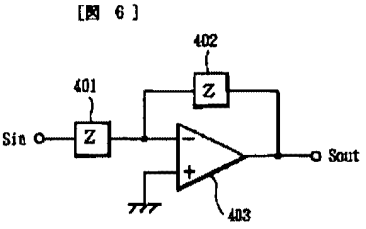
【図１】



【図５】

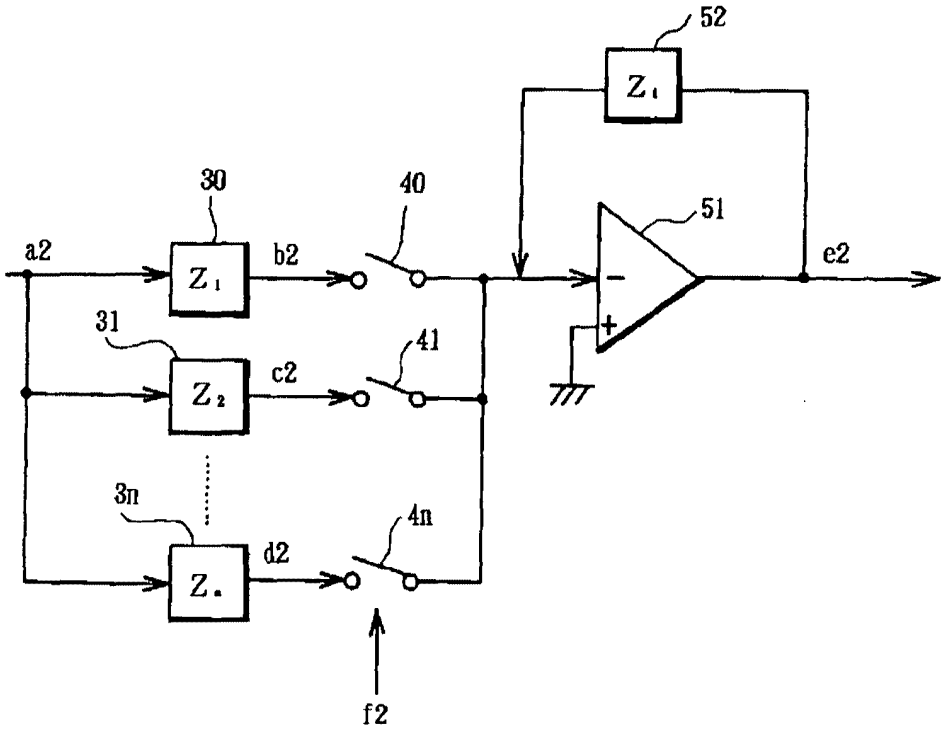


【図６】



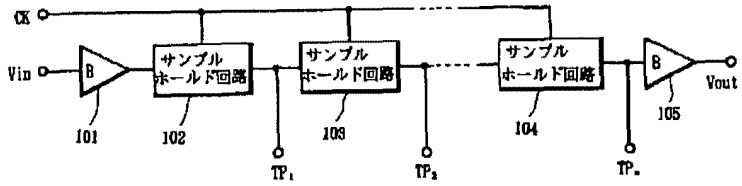
【図2】

[図2]　重み付け回路



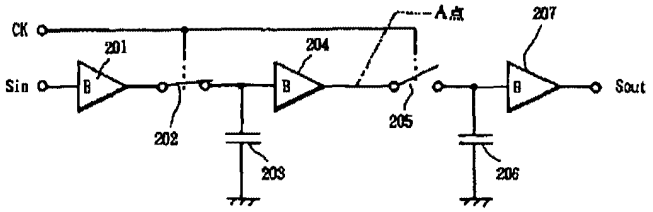
【図3】

[図3]　アナログ遅延回路



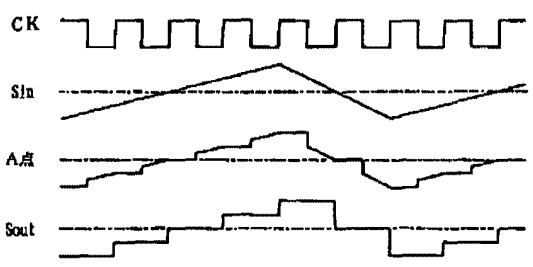
【図4】

[図　4]

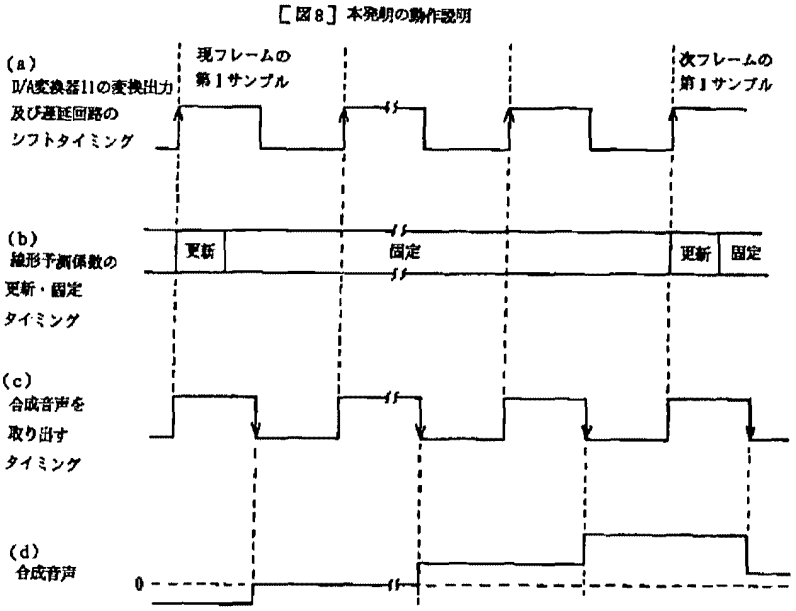


【図7】

[図　7]　アナログ遅延回路の動作説明図

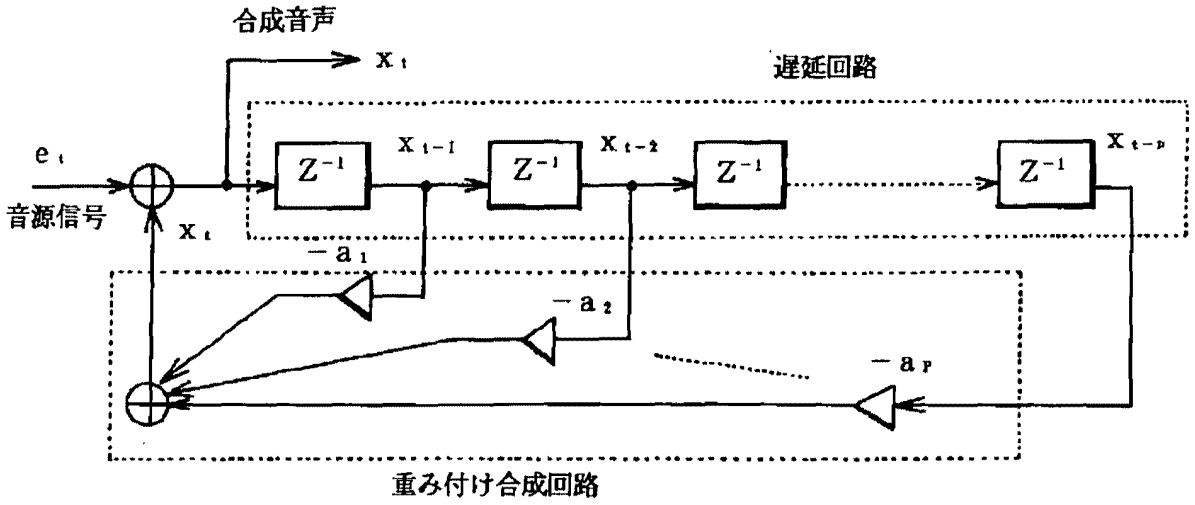


【図8】



【図9】

［図 9］　従来の音声合成回路



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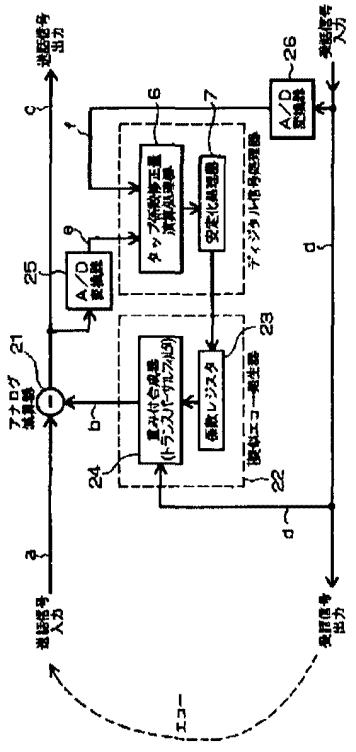
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(54)【発明の名称】　エコーキャンセラ

(57)【要約】
【課題】インパルス応答時間の長い音響エコーをキャンセルするための演算処理量の多い擬似エコーを生成する回路規模を小さくし処理時間を短縮して低消費電力化を図る。
【解決手段】送話信号と受話信号をそれぞれＡ／Ｄ変換器２５，２６でディジタル化し、残留エコーのインパルスレスポンスを推定してタップ係数を算出するタップ係数修正量演算処理器６と安定化処理器７のみをディジタル処理する。そのタップ係数によって重み付けを施し合成して擬似エコーｂを求めるトランスバーサルフィルタ演算をアナログ処理で行うことにより処理速度を高めた。



【特許請求の範囲】
【請求項1】　音響エコーが重畳されたアナログ入力送話信号から擬似エコー信号を差し引いて送話信号を出力するアナログ減算器と、
該アナログ減算器の出力をディジタル変換する第1のA／D変換器と、
通話相手からのアナログ入力受話信号をディジタル変換する第2のA／D変換器と、
該第1のA／D変換器と第2のA／D変換器のディジタル出力から残留エコーのインパルスレスポンスを推定しタップ係数を算出するタップ係数算出器と、
前記アナログ入力受話信号をシフトレジスタで遅延させて得られる複数のタップ出力を前記タップ係数算出器から得られるタップ係数によって重み付けした後加算した重み付け合成出力を前記擬似エコーとして前記アナログ減算器に入力する擬似エコー発生器とが備えられたことを特徴とするエコーキャンセラ。
【発明の詳細な説明】
【0001】
【発明の属する技術分野】本発明は、エコーキャンセラに関し、特に、電話を用いて通話を行う拡声通信において室内の反響によって廻り込む音響エコーを除去するためのエコーキャンセラに関するものである。
【0002】
【従来の技術】図9は電話網における回線エコーの説明図である。電話による音声通信系において、長距離回線は、図9に示すように両端の加入者回線は2本の線路で送受を行う2線式回線であり、それらを結ぶ長距離回線は信号の増幅の必要性から送受各々に別の線路を用いる4線式回線で構成されている。2線式回線と4線式回線の接続にはハイブリッドコイルHが用いられるが、接続点におけるインピーダンス不整合により受話信号の一部が送話路へ漏れ込む。この反射がエコーと呼ばれる。通話者は遅延を伴った自分のエコーを聞きながら話すことになり、話しづらく通話がスムーズに進まなくなる。
【0003】また、テレビ会議や自動車電話でのハンズフリー通話などの拡声通信系の場合も、上記回線エコーと同様に、スピーカからマイクロホンに廻り込む音響エコーが問題となる。図10は音響エコーの説明図である。音響エコーは、図10に示すように、スピーカからマイクロホンへの直接波と、室内の壁面等での多重反射からもたらされる間接波すなわち残響とを重ね合わせたものである。音響エコーは単にエコーにとどまらずハウリング発生の原因にもなる。
【0004】従来、これらエコーの問題に対し、エコーサプレッサが用いられてきた。エコーサプレッサは、スイッチ動作によりエコーを抑圧しているため、相手の音声の一部が途切れたり、エコーが漏れたりする場合があり通話品質の面で劣化は避けられない。そこで、これらの欠点を原理的に解決するため、近年ではエコーキャンセラが用いられている。
【0005】図11はエコーキャンセラの原理説明図である。エコーキャンセラは、4線区間に挿入されて設置局から加入者側をみたエコー路の伝達特性を適応的に推定して擬似エコー信号を出力する擬似エコー発生器と、実際のエコー信号を含んだ送話信号から擬似エコーを差し引く減算器とから構成されている。擬似エコー発生器としてはＦＩＲフィルタすなわちトランスバーサルフィルタが用いられ、そのフィルタ係数の修正アルゴリズムとして学習同定法を用いたものが多く報告されている。
【0006】ここで、学習同定法のアルゴリズムについて簡単に説明する。ある時刻jにおける受話信号をx_j、エコー路のインパルス応答をg_i（i＝0，1，2，…N－1）、擬似エコー発生器でのインパルス応答の推定値をg_i^j（i＝0，1，2，…N－1）、とすると、エコー信号を含む送話側入力信号y_j、擬似エコー信号z_j、送話側出力信号（誤差信号）e_jはそれぞれ次式で与えられる。
【0007】
【数1】

$$y_j = \sum_{i=0}^{N-1} g_i \cdot x_{j-i} + n_j \qquad (1)$$

$$z_j = \sum_{i=0}^{N-1} h_i^j \cdot x_{j-i} \qquad (2)$$

$$e_j = y_j - z_j \qquad (3)$$

ここで、n_jはエコー路で加わった雑音（や、近端話者の音声）である。
【0008】擬似エコー路のインパルス応答h_i^jの推定値は次のように逐次的に求められる。
【0009】
【数2】

$$h_i^{j+1} = h_i^j + \Delta h_i^j \qquad (4)$$

ただし、

$$\Delta h_i^j = K \cdot e_j \cdot x_{j-i} \Big/ \sum_{i=0}^{N-1} x_{j-i}^2 \qquad (5)$$

ここでKは修正係数で、あり0＜K＜2が安定条件である。Nはタップ数である。

【0010】図12は従来のエコーキャンセラの構成例図であり、回線エコーを除去するために用いられているエコーキャンセラである。図において、1，9は入力送話信号a，入力受話信号dをディジタル変換するA／D変換器、2はエコーを含んだディジタル送話信号a'から擬似エコー信号b'を減算する減算器、3は擬似エコー発生器、4は係数レジスタ、5はトランスバーサルフィルタ、6はタップ係数修正量演算処理器、7は安定化処理器、8，10はディジタル送話信号e，ディジタル受話信号fをアナログ変換して出力するD／A変換器である。この回路全体は、破線で囲ったようにDSP（ディジタルシグナルプロセッサ：ディジタル信号処理器）で処理されている。

【0011】エコーキャンセラをハードウェアの観点から眺めると、エコー消去という目的は同一であっても、適用目的によっては要求される性能が大きく異なる。電話回線の2線4線変換点におけるインピーダンス不整合によって生じる回線エコーは数十ms程度であるのに比べ、音響エコーはスピーカとマイクロホン間の信号伝搬速度が非常に遅い音響的廻り込み信号を対象としているため消去すべきエコー路のインパルス応答時間は2百数十msにわたる場合もある。

【0012】従って、エコーキャンセラの設計において、エコー消去の対象となるエコー路の最大インパルス応答時間Dを推定する必要がある。そして、エコーキャンセラの擬似エコー路の最大インパルス応答時間は、推定されたエコー路の最大インパルス応答時間Dに等しいか、またはそれをカバーするように設計しなければならない。エコーキャンセラの擬似エコー路（発生器）3をトランスバーサルフィルタ5で構成する場合において、最大インパルス応答時間をDに等しく選び、トランスバーサルフィルタのタップ数をN，タップ時間間隔をTとした時、次式が成立する。

【0013】

【数3】$D = N \times T$　　（6）

【0014】

【発明が解決しようとする課題】従って、消去すべきエコー路の最大インパルス応答時間Dとタップ時間間隔Tが与えられると、エコーキャンセラのタップ数Nは（6）式から求められる。回線エコーの場合の例として、インパルス応答時間Dが40ms、タップ時間間隔Tが125μsの時、タップ数Nは320タップとなる。一方、音響エコーの場合の例として、インパルス応答時間Dが250ms、タップ時間間隔Tが125μsの時、タップ数Nは2000タップとなる。これはハードウェアの処理量で比較すると回線エコーの場合の4～5倍になる。すなわち、従来の回路において積和演算を行うトランスバーサルフィルタは、タップ数に比例して演算量が増加する。そのため音響エコーの場合は、従来のトランスバーサルフィルタを実現しているDSPの回路規模が大きく、処理時間が長くかかり、消費電力も多いという問題が生じている。

【0015】本発明は、上記の事情に鑑みてなされたもので、インパルス応答時間の長い音響エコーのキャンセルを対象とし、積和演算を高速に実行できるアナログ回路をトランスバーサルフィルタ演算に用いることで、擬似エコーの生成を高速に実行でき、回線規模が小さく消費電力の少ないエコーキャンセラを提供することを目的とする。

【0016】

【課題を解決するための手段】本発明のエコーキャンセラは、音響エコーが重畳されたアナログ入力送話信号から擬似エコー信号を差し引いて送話信号を出力するアナログ減算器と、該アナログ減算器の出力をディジタル変換する第1のA／D変換器と、通話相手からのアナログ入力受話信号をディジタル変換する第2のA／D変換器と、該第1のA／D変換器と第2のA／D変換器のディジタル出力から残留エコーのインパルスレスポンスを推定しタップ係数を算出するタップ係数算出器と、前記アナログ入力受話信号をシフトレジスタで遅延させて得られる複数のタップ出力を前記タップ係数算出器から得られるタップ係数によって重み付けした後加算した重み付け合成出力を前記擬似エコーとして前記アナログ減算器に入力する擬似エコー発生器とが備えられたことを特徴とするものである。

【0017】

【発明の実施の形態】本発明では、上記課題を解決するために、従来トランスバーサルフィルタをDSP等のディジタル信号処理で実現していたものを、アナログ回路で処理することによって高速に擬似エコーを生成できるようにしたので、回路規模も小さく済み、消費電力も抑えられるようになった。

【0018】すなわち、本発明は、アナログ送話信号からアナログ擬似エコーを減算するアナログ減算器と、擬似エコーが減算された送話信号を出力するとともに、ディジタル信号に変換した送話信号から残留エコーのイン

パルスレスポンスを推定しタップ係数を算出するタップ係数算出手段と、アナログ受話信号を遅延させるシフトレジスタの各タップから出力されるディジタル信号をタップ係数で重み付けして合成演算を行い擬似エコーを生成して減算器に与えるように構成したエコーキャンセラである。

【００１９】

【実施例】図１は本発明の実施例を示す回路構成例図であり、アナログ重み付け合成器２４とアナログ減算器２１を用いたエコーキャンセラである。図において、本発明では、タップ係数修正量演算処理器６と安定化処理器７のみをディジタル信号処理器でディジタル処理し、減算器２１と擬似エコー発生器２２の重み付け合成器２４をアナログ処理するように構成したことを要旨とするものである。

【００２０】図１に示した本発明の実施例の動作を説明する。本実施例の回路素子は８ｋＨｚのシステムクロックＣＫで動作することとする。まず、送話信号ａは、減算器２１によって擬似エコーｂが差し引かれて残留エコーを含んだ送話信号ｃが出力される。動作開始直後は擬似エコーｂが生成されていないため、エコーを含んだ送話信号ａがそのまま出力ｃとして出力される。

【００２１】次に、減算器２１から出力される送話信号ｃはＡ／Ｄ変換器２５によってＡ／Ｄ変換されタップ修正量演算処理器６に入力される。同時に、受話信号入力ｄもＡ／Ｄ変換器２６でディジタル変換されタップ修正量演算処理器６に入力される。入力されたそれぞれの信号ｅ，ｆから学習同定法などによってタップ係数、すなわちエコー路のインパルスレスポンスが求められる。次に、安定化処理器７によってタップ修正量演算処理器６によって求められたタップ係数がエコー路からの外部雑音などの影響によって生じる誤差を一方向に蓄積しないように制御する。

【００２２】次に、タップ係数を係数レジスタ２３に入力する。次に、受話信号ｄと係数レジスタ２３に格納されているタップ係数を同時に重み付け合成器２４に入力する。重み付け合成器２４はトランスバーサルフィルタ演算を実行し、擬似エコーｂを生成する。次に、アナログ減算器２１によって入力送話信号ａから擬似エコーｂを差し引く。この一連の処理を繰り返すことで、エコーを含んだ送話信号からエコーを取り除くことができる。

【００２３】図２は、本発明の要部をなす図１に示したアナログ回路で構成された重み付け合成器２４の回路例図である。本回路は積和演算が高速に実行できる回路である。図において、３１は複数の遅延器（シフトレジスタ）からなる遅延回路、３２は重み付け器、３３は加算器である。

【００２４】ここで、重み付け合成器２４について簡単に説明する。まず遅延回路３１について説明する。遅延回路３１はアナログシフトレジスタによって構成されている。図３はアナログシフトレジスタの構成例図である。アナログシフトレジスタはバッファ４０と、サンプルホールド回路４１～４３とで構成されており、TP_1～TP_nはシフトした信号（タップ出力）の出力端子である。受話信号ｄは、バッファ４０を経由して１段目のサンプルホールド回路４１に入力される。１段目のサンプルホールド回路４１ではクロックＣＫの立ち上がりに同期して入力信号をサンプル保持しタップ出力端子TP_1に出力する。２段目のサンプルホールド回路４２も同様に前段のサンプルホールド回路４１の出力をサンプルして、１クロック遅らせて次段とTP_2に出力している。３段目以降も同様に１段について１クロックずつ信号をシフトさせｎ段のアナログシフトレジスタとして動作し、TP_3～TP_nに出力する。

【００２５】図４は図３に示したサンプルホールド回路とバッファの回路例図であり、（Ａ）はサンプルホールド回路の構成例を、（Ｂ），（Ｃ）はバッファの構成例を示している。図４（Ａ）はバッファ２０１，２０４，２０７とクロックＣＫがＬ（ロー）の時にＯＮになりＨ（ハイ）の時にＯＦＦになるスイッチ２０２と、ＣＫがＨの時にＯＮになりＬの時にＯＦＦになるスイッチ２０５と、コンデンサ２０３，２０６とで構成されている。

【００２６】図５は、図４（Ａ）のサンプルホールド回路の動作を説明する波形例図である。入力信号S_{in}はバッファ２０１を経由し、クロックＣＫがＬでスイッチ２０２がＯＮの時はコンデンサ２０３に信号が伝達され、クロックＣＫがＨでスイッチ２０２がＯＦＦになるとコンデンサ２０３に入力された信号は保持される。このときの入力信号S_{in}に対するコンデンサ２０３の動作をバッファ２０４を経由した出力をＡ点としている。同様にクロックＣＫがＨでスイッチ２０５がＯＮの時はコンデンサ２０６に信号が伝達され、クロックＣＫがＬでスイッチ２０５がＯＦＦになるとコンデンサ２０６に入力された信号は保持され、バッファ２０７を経由して出力信号S_{out}となる。

【００２７】図４（Ｂ），（Ｃ）はバッファ４０の構成例であり、（Ｂ）はオペアンプ３０１を用いたボルテージホロワ回路、（Ｃ）はインピーダンス素子４０１，４０２とオペアンプ４０３で構成した反転バッファである。これらバッファとサンプルホールド回路は、ともに公知の技術として知られている。サンプルホールド回路は、これら公知の技術を組み合わせることにより容易に構成が可能である。

【００２８】図６は図２に示した複数の重み付け器３２のそれぞれの回路例図である。図中の、Z_i（ｉ＝１，２，…，ｎ）は入力側のインピーダンスであり、（７）式に示すようにコンデンサで構成される。

【００２９】

【数４】

$$Z_i = \frac{1}{j\omega C_i} \qquad (7)$$

$$i = 0,\ 1,\ 2,\ \cdots,\ n$$

【００３０】ここで、ｎはＡ／Ｄ変換器の量子化ビット数に対応し、ｎ＝１６とする。各コンデンサC_i（ｉ＝１，２，…，ｎ）の容量は重み付けデータのＭＳＢに近いほど大きな値を持っている。１６ビットの重み付けデータの各ビットの値によりスイッチをＯＮ／ＯＦＦする。これにより、Ｚｉ（ｉ＝１，２，…，ｎ）またはＣｉ（ｉ＝１，２，…，ｎ）の総和の値を制御する。帰還インピーダンスＺｆは（８）式で表現される。

【００３１】

【数５】

$$Z_f = \frac{1}{j\omega C_f} \qquad (8)$$

この重み付け器３２の利得Ｇは（９）式で示される。

【００３２】

【数６】

$$G = -\frac{\sum_i c_i}{c_f} \qquad (9)$$

$$i \in ON$$

【００３３】図７は図２の加算器３３の回路例図であり、重み付け器３２で重み付けされた出力は、図７の加算器３２で合成され重み付け合成出力、すなわち擬似エコーｂを得る。

【００３４】次に、図１の減算器２１について説明する。減算器２１はアナログ回路によって実現されている。図８はアナログ減算器２１の構成例図である。アナログ減算器２１はオペアンプで構成できる公知の技術として知られている。この回路の出力電圧V_{OUT}（＝送話信号ｃ）は（１０）式で表される。

【００３５】

【数７】

$$V_{OUT} = \frac{Z_2}{Z_1}(V_{in1} - V_{in2}) \qquad (10)$$

ここで、$Z_1 = Z_2$ とすると

$$V_{OUT} = V_{in1} - V_{in2} \qquad (11)$$

となり減算器が構成できる。

【００３６】

【発明の効果】以上述べたように、本発明によれば、エコーを伴った送話信号ａからエコーを取り除くエコーキャンセラを構成する場合において、アナログ回路を用いることで、残響時間が多く膨大なタップ長を要する音響エコーをキャンセルする場合でも、タップ長に起因する演算処理量の増加が少なく処理時間を短縮でき、消費電力も抑えられるので実用上の効果は大きい。

【図面の簡単な説明】

【図１】本発明の実施例を示すブロック図である。

【図２】本発明の要部をなすアナログ重み付け合成器の回路構成例図である。

【図３】本発明のアナログ遅延回路の構成例図である。

【図４】本発明の遅延器の構成例及びバッファの構成例図である。

【図５】図４の回路の動作波形例図である。

【図６】本発明の重み付け器の回路例図である。

【図７】本発明の重み付け器の出力加算器の回路例図である。

【図８】本発明のアナログ減算器の回路例図である。

【図９】電話網における回線エコーの説明図である。

【図１０】拡声系通信における音響エコーの説明図である。

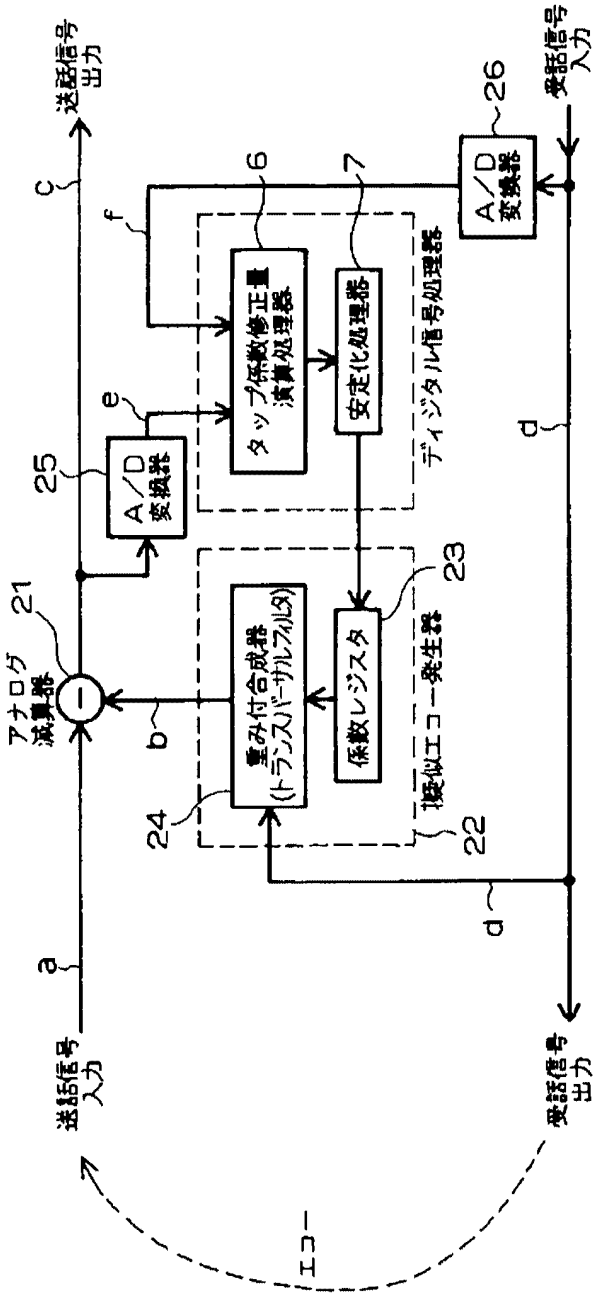
【図１１】エコーキャンセラの原理説明図である。

【図１２】従来の回線エコーキャンセラの回路構成例図である。

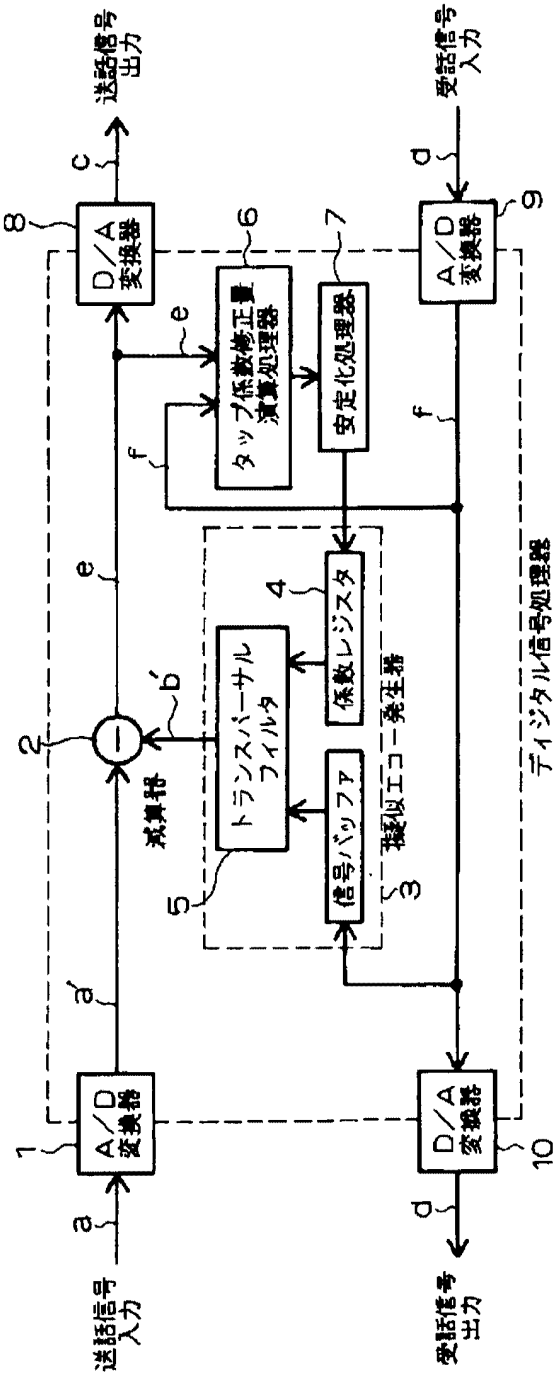
【符号の説明】

１，９　Ａ／Ｄ変換器
２　減算器
３　擬似エコー発生器
４　係数レジスタ
５　トランスバーサルフィルタ
６　タップ係数修正量演算処理器
７　安定化処理器
８，１０　Ｄ／Ａ変換器
２１　アナログ減算器
２２　擬似エコー発生器
２３　係数レジスタ
２４　重み付け合成器
２５　Ａ／Ｄ変換器
２６　Ａ／Ｄ変換器
３１　遅延回路
３２　重み付け器
３３　加算器
４０　バッファ
４１，４２，４３　サンプルホールド回路（遅延器）

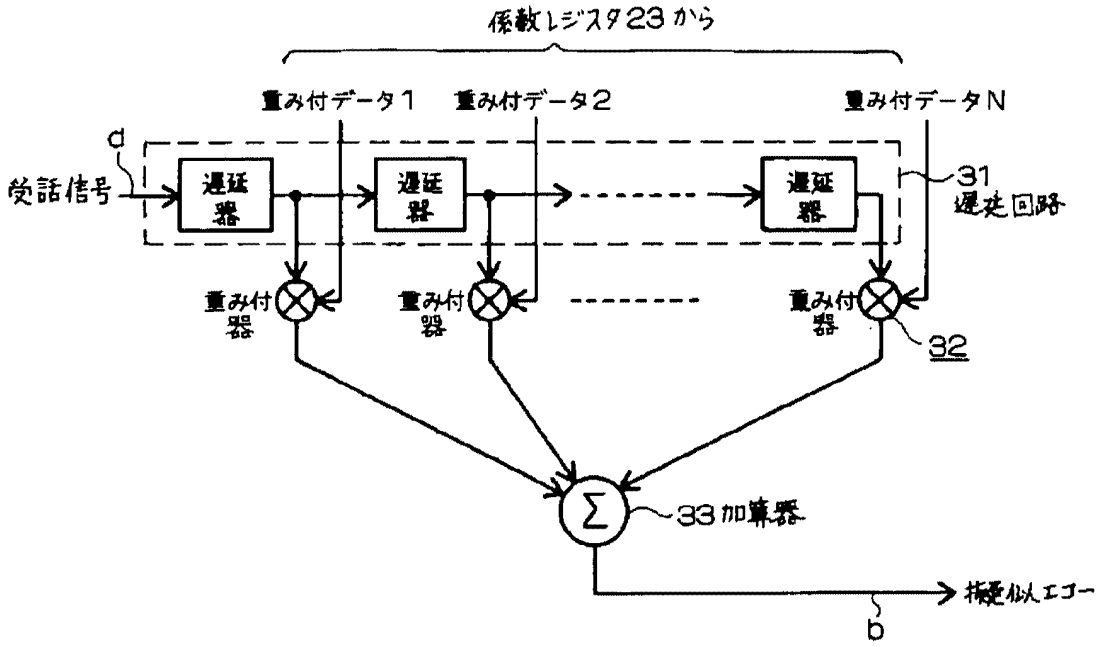
【図1】


送話信号出力
受話信号入力
A/D変換器
タップ係数修正量演算処理器
安定化処理器
ディジタル信号処理器
アナログ減算器
重み付合成器(トランスバーサルフィルタ)
係数レジスタ
擬似エコー発生器
送話信号入力
受話信号出力
エコー

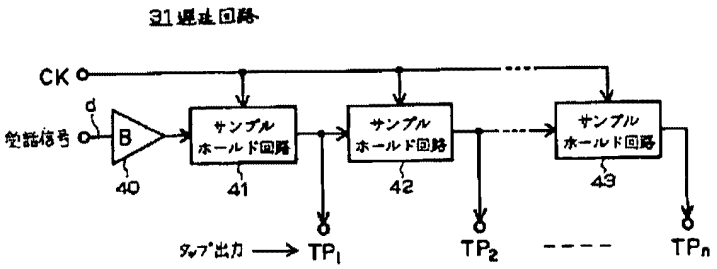
【図12】


送話信号出力
受話信号入力
D/A変換器
A/D変換器
タップ係数修正量演算処理器
安定化処理器
減算器
トランスバーサルフィルタ
係数レジスタ
信号バッファ
擬似エコー発生器
ディジタル信号処理器
送話信号入力
受話信号出力

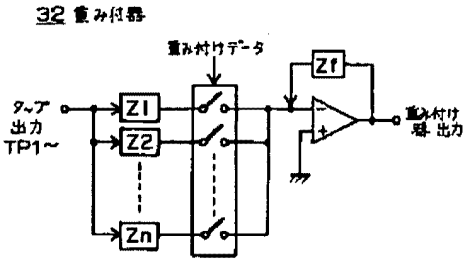
【図2】


24 重み付合成器
係数レジスタ23から
重み付データ1
重み付データ2
重み付データN
d
受話信号
遅延器
遅延器
遅延器
31
遅延回路
重み付器
重み付器
重み付器
32
Σ
33 加算器
指定似入エコー
b

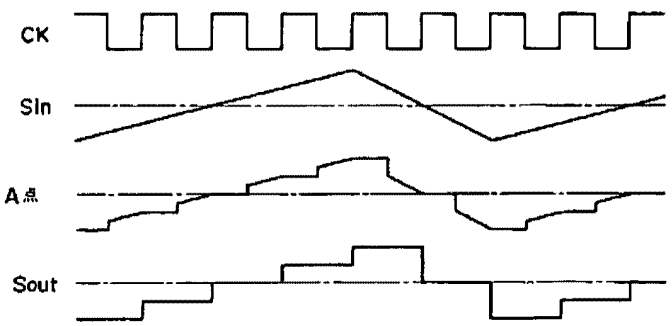
【図3】


31 遅延回路
CK
d
受話信号
B
40
サンプルホールド回路
41
サンプルホールド回路
42
サンプルホールド回路
43
タップ出力
TP1
TP2
TPn

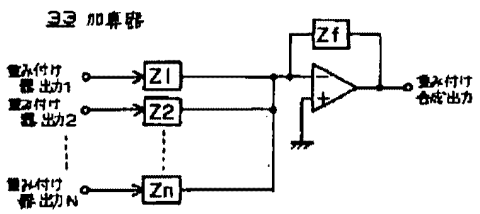
【図6】


32 重み付器
重み付けデータ
タップ出力 TP1～
Z1
Z2
Zn
Zf
重み付け器出力

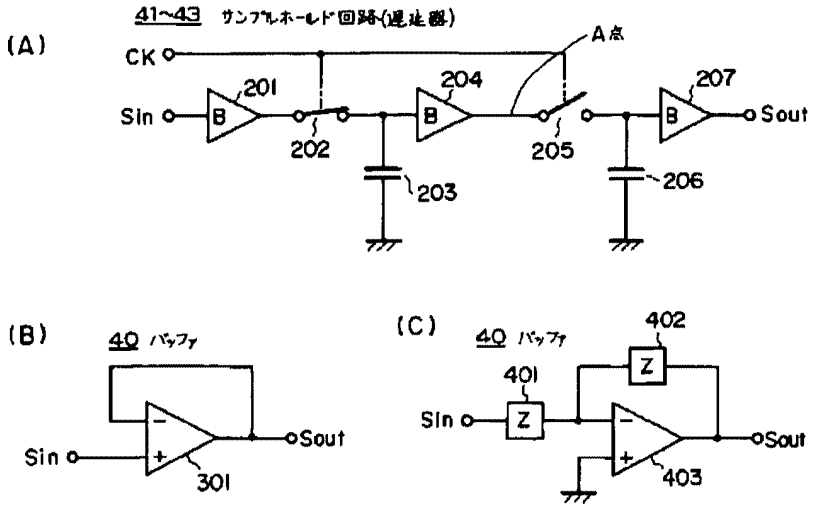
【図5】


CK
SIn
A点
Sout

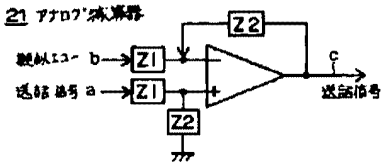
【図7】


33 加算器
重み付け器出力1
重み付け器出力2
重み付け器出力N
Z1
Z2
Zn
Zf
重み付け合成出力

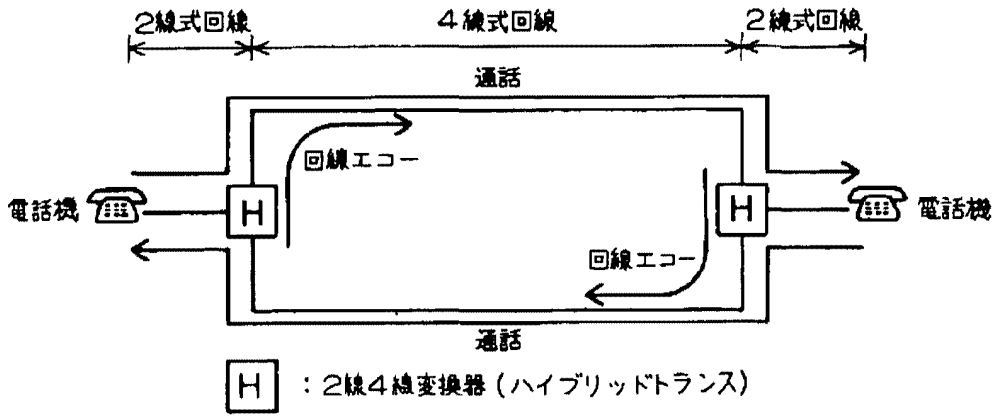
【図4】



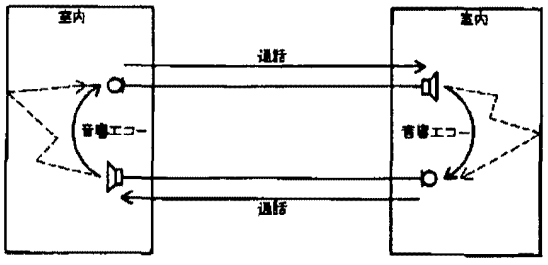
【図8】



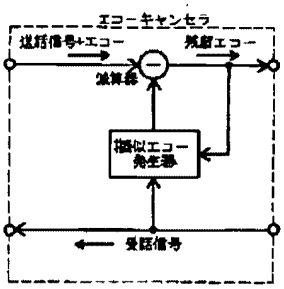
【図9】



【図10】



【図11】



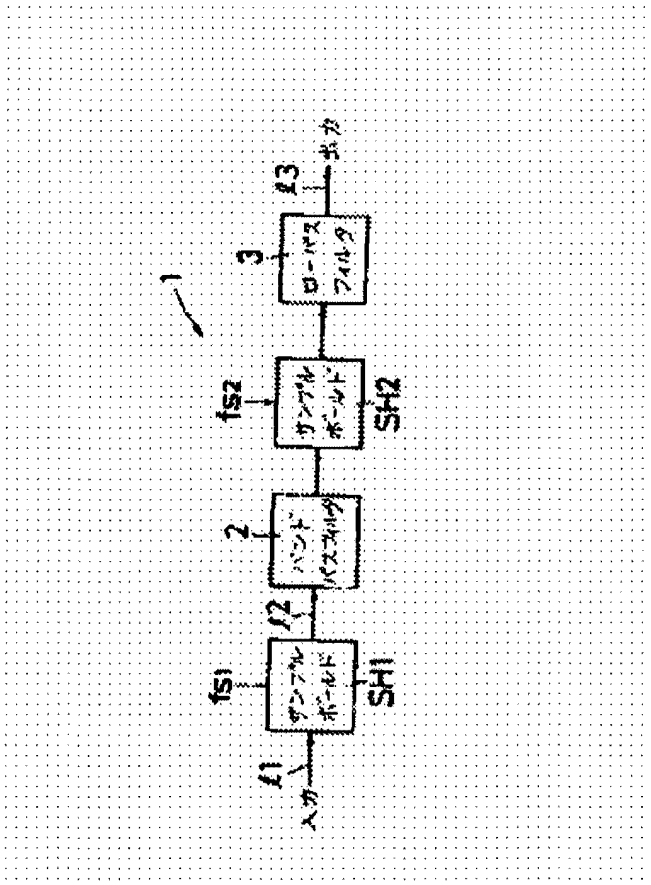
FREQUENCY CONVERTER FOR SIGNAL

Patent number: JP61232706
Publication date: 1986-10-17
Inventor: MIYAKOSHI KAZUMITSU
Applicant: SHARP KK
Classification:
- international: ***H03D7/00;*** **H03D7/00;** (IPC1-7): H03D7/00
- european:
Application number: JP19850073135 19850406
Priority number(s): JP19850073135 19850406

Report a data error here

Abstract of **JP61232706**

PURPOSE:To convert optionally and output the frequency of the input analog signal with a simple constitution by controlling the first and second sample holding frequencies, and converting and outputting the frequency of the input signal. CONSTITUTION:An input signal is sample-held at a sample holding frequency fs 1 by a sample holding circuit SH 1 from a line l1, next, the first higher harmonic wave component only is filtered by a band pass filter 2, given to the second sample holding circuit SH 2, and sample-held at a sample holding frequency fs 2 having the frequency smaller than two times of the first higher harmonic wave frequency. Next, the high area component above the low frequency component out of input signals, is interrupted by a low-pass filter 3 and the low frequency component only is derived from a line l3. Thus, the frequency of the input signal is subtracted by the first sample holding frequency fs 1, and applied by the second sample holding frequency fs 2 and the frequency is converted and outputted.



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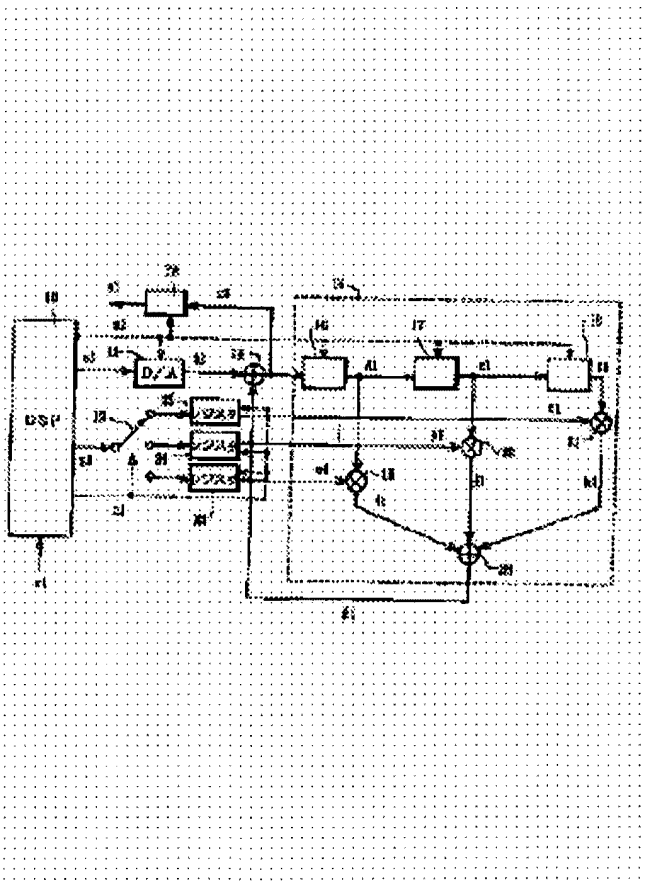
SOUND SYNTHESIZING METHOD AND CIRCUIT THEREFOR

Patent number: JP9171399
Publication date: 1997-06-30
Inventor: SASAKI SEIJI; URABE KENZO
Applicant: KOKUSAI ELECTRIC CO LTD
Classification:
- international: ***H03H17/02;*** **H03H17/02;** (IPC1-7): G10L9/14; H03H17/02
- european:
Application number: JP19950330590 19951219
Priority number(s): JP19950330590 19951219

Report a data error here

Abstract of **JP9171399**

PROBLEM TO BE SOLVED: To reduce the operation amount and power consumption. SOLUTION: A sound source signal outputted from a DSP 10 is analog- converted by a D/A converter 11, and an analog sound source signal and a predictive signal are added by an adder 14, and a synthetic sound signal is outputted, and the synthetic sound signal held by a sample-and-hold circuit 12 is outputted The predictive signal is synthesized so that the synthetic sound signal is delayed by analog delay circuits 16-18, and plural delayed synthetic sound signals are outputted, and a linear predictive coefficient outputted from a DSP 10 is inputted as a weight coefficient through a switcher 13 and registers 23-25, and the delayed synthetic sound signals are weighted by analog weight circuits 19-21, and plural weighted delayed synthetic sound signals are synthesized by an analog synthesizer 22, and the predictive signal is outputted.



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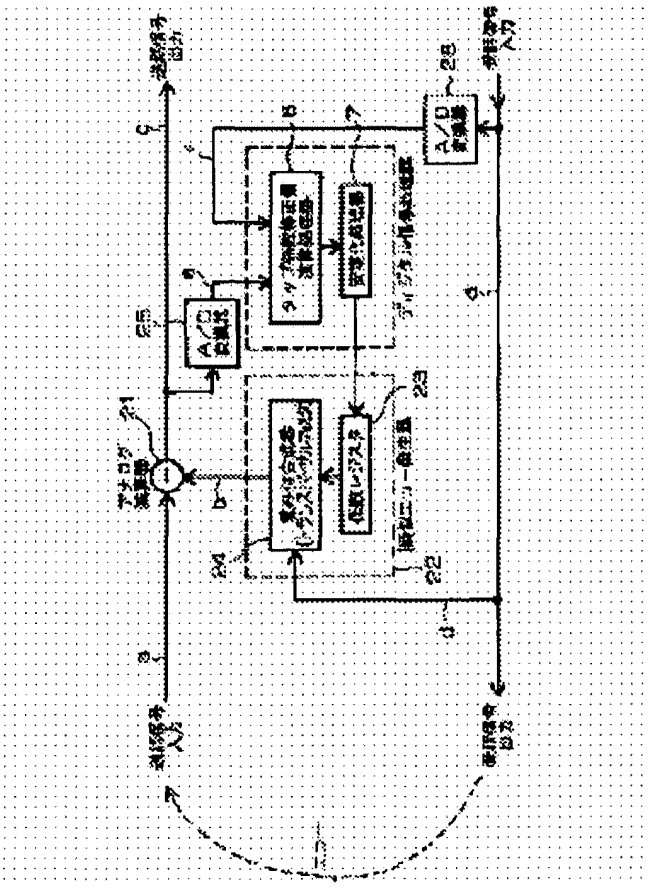
ECHO CANCELLER

Patent number: JP10041860
Publication date: 1998-02-13
Inventor: TEJIMA ISAO
Applicant: KOKUSAI ELECTRIC CO LTD
Classification:
- International: ***H04B3/23; H04M1/60;*** **H04B3/23; H04M1/60;** (IPC1-7): H04B3/23; H04M1/60
- european:
Application number: JP19960209396 19960722
Priority number(s): JP19960209396 19960722

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Abstract of **JP10041860**

PROBLEM TO BE SOLVED: To attain low power consumption by reducing a circuit scale for generating a pseudo-echo with large arithmetic processing quantity to cancel an acoustic echo having a long impulse response time and shortening a processing time. SOLUTION: A transmitting signal and a receiving signal are respectively digitized by A/D converters 25 and 26. Only a tap coefficient correction quantity operation processing equipment 6 for estimating the impulse response of a residual echo and calculating a tap coefficient and a stabilization processing equipment 7 are digitally processed. Processing speed is enhanced by executing a transversal filter operation by an analog processing, where weighting is executed by the tap coefficient, synthesis is executed and the pseudo-echo (b) is obtained.



Data supplied from the ***esp@cenet*** database - Worldwide

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2616
Appl. No.: 10/973,917	Examiner: Chin, Wellington
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Fifth Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Fifth Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Fourth Supplemental Information Disclosure Statement filed on September 25, 2006 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may

not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Document AL26 was cited in an Office Action in related U.S. Patent Application No. 10/305,299, filed November 27, 2002, entitled "Method and Apparatus for Improving Dynamic Range in a Communication System," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 4,380,828; 4,562,414; and 5,339,459, which have already been cited in the present application.

Documents AP62 and AE79-AH79 were identified in a search relating to U.S. Patent Application No. 11/582,367, filed October 18, 2006, entitled "Apparatus and Method for Communicating an Input Signal in Polar Representation," directed to related subject matter.

Documents AH77, AI77, and AA78-AG78 were cited in an Office Action in related U.S. Patent Application No. 10/318,207, filed December 13, 2002, entitled "Method and Apparatus for Reducing Re-Radiation Using Techniques of Universal Frequency Translation Technology," directed to related subject matter.

Document AH78 was cited in an Office Action in related U.S. Patent Application No. 09/476,092, filed January 3, 2000, entitled "Analog Zero IF FM Decoder and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Document AI78 was cited in an Office Action in related U.S. Patent Application No. 11/173,021, filed July 5, 2005, entitled "Method and Circuit for Down-Converting a

Signal," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 3,694,754 and 6,393,070, which have already been cited in the present application.

Documents AA79-AC79 are co-owned patents which are directed to related subject matter.

Document AD79 was cited in an International Search Report and Written Opinion in related PCT Application No. PCT/US2004/013813, filed April 30, 2004, entitled "Real-Time Wireless Exchange of Objects," directed to related subject matter.

Document AI79 was cited in an Office Action in related U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Methods and Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,844,868 and 5,982,315, which have already been cited in the present application.

Document AA80 was cited in an Office Action in related U.S. Patent Application No. 10/453,622, filed June 4, 2003, entitled "Active Polyphase Inverter Filter for Quadrature Signal Generation," directed to related subject matter. Also cited in said Office Action was Salous, S., "IF digital generation of FMCW waveforms for wideband channel characterization," IEE Proceedings-I, IEE, Vol. 139, No. 3, pp. 281-288 (June 1992), which has already been cited in the present application.

Document AB80 was cited in an Office Action in related U.S. Patent Application No. 10/086,367, filed March 4, 2002, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 3,641,442, which has already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign

application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document AL26 (JP 10-173563) appears to describe an up-down tuner. An English language translation of document AL26 is enclosed as document AO62.

☒ 7. Copies of documents AL26, AO62, and AP62 are enclosed. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent publications cited on the attached Form PTO-1449 are not enclosed.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No.

6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000 (now abandoned), 09/476,093, filed January 3, 2000 (now U.S. Patent No. 7,006,805), 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: November 9, 2006

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

606820_1.DOC

FORM PTO-1449 FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH77	3,739,282	06/1973	Bruch *et al.*			
	AI77	4,439,787	03/1984	Mogi *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL26	JP 10-173563	06/1998	JP			Yes (Doc. AO62)
	AM						Yes No

NON-PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO62	English-language Computer Translation of Japanese Patent Publication No. JP 10-173563, provided by the JPO, 10 pages (June 26, 1998 - Date of publication of application) and cited in U.S. Patent Application Ser. No. 10/305,299, directed to related subject matter.
	AP62	*What is I/Q Data?*, printed September 16, 2006, from http://zone.ni.com, 8 pages (Copyright 2003).
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

606809_1.DOC

FORM PTO-1449 FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA78	4,866,441	09/1989	Conway *et al.*			
	AB78	4,885,671	12/1989	Peil			
	AC78	5,164,985	11/1992	Nysen *et al.*			
	AD78	5,734,683	03/1998	Hulkko *et al.*			
	AE78	5,918,167	06/1999	Tiller *et al.*			
	AF78	6,445,726 B1	09/2002	Gharpurey			
	AG78	6,560,451 B1	05/2003	Somayajula			
	AH78	4,143,322	03/1979	Shimamura			
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	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

NON-PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
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	AP	
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EXAMINER	DATE CONSIDERED

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FORM PTO-1449 FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
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	AM						Yes No

NON-PATENT LITERATURE DOCUMENTS

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

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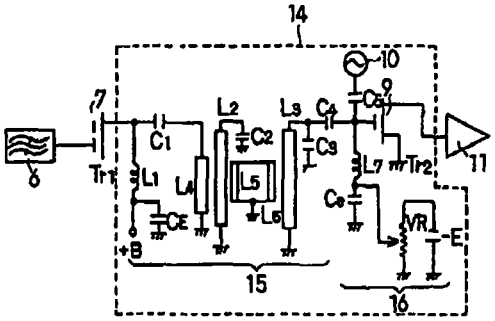
(74)代理人　弁理士　佐野　静夫

(54)【発明の名称】　U／Dチューナ

(57)【要約】

【課題】　U／Dチューナにおける第２ＩＦバンドパスフィルタのフィルタ特性を簡単確実に調整できるようにする。

【解決手段】　受信した入力信号を第１中間周波数の信号に変換する第１周波数変換手段４、５と、第１中間周波のバンドパスフィルタ８を備えた第１中間周波増幅回路７、８と、上記バンドパスフィルタ８の出力信号を第２中間周波数の信号に変換するミキサー９と、局部発振器１０より成る第２周波数変換手段を設けたダブルコンバージョン方式のU／Dチューナにおいて、上記バンドパスフィルタ８を平面分布定数型のマイクロストリップラインＬ２，Ｌ３，Ｌ４，Ｌ５とコンデンサＣ２，Ｃ３より成る共振回路で構成し、上記ミキサー９をシングルゲートＦＥＴで構成し、このミキサー９の入力ゲートバイアスを可変調整するバイアス可変回路Ｅ，ＶＲ，Ｌ７を設けた構成にする。



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【特許請求の範囲】

【請求項1】 受信した高周波信号を第1中間周波信号に変換する第1局部発振器と第1ミキサーより成る第1周波数変換手段と、上記第1中間周波信号を増幅する第1中間周波増幅手段と、該第1中間周波増幅手段より導出する第1中間周波信号を第2中間周波信号に変換する第2局部発振器と第2ミキサーより成る第2周波数変換手段と、上記第2中間周波信号を増幅する第2中間周波増幅手段とを設けたダブルコンバージョン方式のU/Dチューナにおいて、上記第1中間周波増幅手段に平面分布定数型のマイクロストリップラインで構成したインダクタンスとコンデンサより成る同調回路を有するバンドパスフィルタ手段を設け、上記第2ミキサーの入力インピーダンスを可変調整する入力インピーダンス調整手段を設け、上記入力インピーダンスの可変で、上記バンドパスフィルタ手段のフィルタ特性を調整するようにしたことを特徴とするU/Dチューナ。

【請求項2】 上記第2ミキサーをシングルゲート型FETで構成したことを特徴とする請求項1記載のU/Dチューナ。

【請求項3】 上記インピーダンス調整手段は、上記シングルゲート型FETのゲートバイアスを調整するゲートバイアス調整手段であることを特徴とする請求項2記載のU/Dチューナ。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、ケーブルテレビ（以下「CATV」という）の受信端末（セットトップボックス）で多チャンネルのテレビ信号等の受信を行わせるU/D（アップ/ダウン）チューナに関するものである。

【0002】

【従来の技術】近年CATVはアナログ信号からデジタル化の方向へと種々実用化試験が行われており、多チャンネル化に拍車をかけている。従来受信帯域は550MHzまでであったものがデジタルチャンネルが加わり、750MHz、860MHzへと広帯域になりつつある。U/Dチューナは上記のような多チャンネルの信号を受信するのに最適なチューナであり、CATVの分野では一般的に広く使用されている。尚、U/Dチューナは信号を、いったん高い周波数へコンバートし、それから低い周波数にコンバートするダブルコンバージョン式のものである。

【0003】図1は、U/Dチューナの構成図である。図1において、1はCATVの入力端子であり、50～750MHzの帯域のTV信号が印加される。2は50～750MHzのバンドパスフィルタであり、その出力は高帯域・高周波増幅回路3に導出される。4は第1ミキサー、5は第1局部発振器であり、上記高帯域・高周波増幅回路3からの信号は、上記第1ミキサー4及び第

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1局部発振器5より成る第1周波数変換回路で選局され、950MHzに周波数変換される。

【0004】6は950MHzの第1中間周波数に同調した第1IFバンドパスフィルタであり、7は第1中間周波増幅器、8はIF同調回路からなる第2IFバンドパスフィルタ、9は第2ミキサー、10は第2局部発振器であり、上記第2ミキサー9及び第2局部発振器10よりなる第2周波数変換回路で950MHzから第2中間周波数の信号に変換される。11は第2中間周波増幅器、12は第3IFバンドパスフィルタであり、13は第2中間周波信号の出力端子である。

【0005】図4は、従来例の要部の具体的な構成を示す回路図であり、上記図1に示すU/Dチューナにおいて、IF同調回路を構成する第2IFバンドパスフィルタ8及び第2ミキサー9と第2局部発振器10より成る第2周波数変換回路で構成した図中点線の枠で示す中間周波回路14に対応する部分を詳細に示したものである。

【0006】図4に示す従来の中間周波回路14-1において、図1に対応する部分には同一符号を付し、説明を省略する。図4において、L1は高周波チョークコイル、L2，L3は中心導体、Zoはトリマー、C1，C4は結合コンデンサ、C2，C3は同調コンデンサ、C5は第2局部発振器10と第2ミキサー9-1間に設けた結合コンデンサ、Ceは接地コンデンサ、+Bは電源電圧である。

【0007】トランジスタTr1より成る第1中間周波増幅器7-1で増幅された第1中間周波信号は、結合コンデンサC1を介して同調コンデンサC2と中心導体L2及び同調コンデンサC3と中心導体L3より成る共振回路に導かれる。そして、この共振回路でバンドパスフィルタを形成した同調回路を通過した後、結合コンデンサC4を介し、トランジスタTr2より成る第2ミキサー9-1に供給され、該第2ミキサー9-1で結合コンデンサC5を介して供給される第2局部発振器10からの第2局部発振信号と混合され、第2の中間周波信号に周波数変換される。

【0008】バンドパスフィルタを形成する1次側同調回路はコンデンサC2と中心導体L2で構成され、又、2次側同調回路はコンデンサC2と中心導体L3で構成される。そして、上記の各同調回路はトリマーZoで上記中心導体L2，L3との間隔を変えることにより分布常数回路の特性インピーダンスを変化させ、複同調特性の調整を行うことができるようになる。上記中心導体L2及びL3は、図5（a）、（b）に示すように、各々独立の筐体に設けられ、プリント基板（PWB）上に垂直に形成し、且つ平行にZoトリマーが配置される。

【0009】

【発明が解決しようとする課題】上記従来の回路構成によれば、中間周波回路14-1における第2IFバンド

パスフィルタ部の波形調整は、人的手段により、トリマーZoを可変して行っており、その調整には熟練を要し、時間がかかり、コストアップに要因になるという問題があった。また、バンドパスフィルタを構成する上記中間周波回路14-1の共振回路が、中心導体とトリマーZoより成る分布定数回路の立体構造になっているので、回路の取り扱いが面倒であるという問題があった。

【0010】

【課題を解決するための手段】上記の問題を解決するため、本発明の請求項1記載のU/Dチューナは、受信した高周波信号を第1中間周波信号に変換する第1局部発振器と第1ミキサーより成る第1周波数変換手段と、上記第1中間周波信号を増幅する第1中間周波増幅手段と、該第1中間周波増幅手段より導出する第1中間周波信号を第2中間周波信号に変換する第2局部発振器と第2ミキサーより成る第2周波数変換手段と、上記第2中間周波信号を増幅する第2中間周波増幅手段とを設けたダブルコンバージョン方式のU/Dチューナにおいて、上記第1中間周波増幅手段に平面分布定数型のマイクロストリップラインで構成したインダクタンスとコンデンサより成る同調回路を有するバンドパスフィルタ手段を設け、上記第2ミキサーの入力インピーダンスを可変調整する入力インピーダンス調整手段を設け、上記入力インピーダンスの可変で、上記バンドパスフィルタ手段のフィルタ特性を調整するようにしたことを特徴とする。

【0011】従って、受信した高周波信号は第1局部発振器と第1ミキサーより成る第1周波数変換手段で第1中間周波信号に変換された後、第1中間周波増幅手段で増幅されて、第2局部発振器と第2ミキサーより成る第2周波数変換手段に導かれ、ここで第2中間周波信号に変換される。

【0012】上記第1中間周波増幅手段には、平面分布定数型のマイクロストリップラインで構成したインダクタンスとコンデンサより成る共振回路を有するバンドパスフィルタ手段が設けられているので、バンドパスフィルタ手段により、上記共振回路に同調した周波数特性の第1中間周波信号が導出され、この第1中間周波信号は、上記第2ミキサーに供給される。

【0013】第2ミキサーには、入力インピーダンス調整手段が設けられているので、この入力インピーダンス調整手段を調整すると、上記第2ミキサーの入力インピーダンスが変化し、上記バンドパスフィルタ手段のフィルタ特性を可変調整することができ、上記第2ミキサーに供給する第1中間周波信号の周波数特性を調整することができる。

【0014】また、本発明の請求項2記載のU/Dチューナは、上記請求項1記載のU/Dチューナにおいて、第2ミキサーをシングルゲート型FETで構成したことを特徴とする。

【0015】従って、この発明では、第2ミキサーにシングルゲート型FETを用いるので、この第2ミキサーの入力インピーダンスの変化量を大きくすることができ、上記バンドパスフィルタ手段のフィルタ特性の可変調整範囲を拡げることができる。

【0016】また、本発明の請求項3記載のU/Dチューナは、上記請求項2記載のU/Dチューナにおいて、上記インピーダンス調整手段は、上記シングルゲート型FETのゲートバイアスを調整するゲートバイアス調整手段であることを特徴とする。

【0017】従って、この発明では、シングルゲート型FETのゲートバイアスをゲートバイアス調整手段により可変調整するので、上記シングルゲート型FETの入力インピーダンスを簡単に調整でき、上記バンドパスフィルタ手段のフィルタ特性の調整を簡単な構成で容易に行うことができる。

【0018】

【発明の実施の形態】以下、本発明の実施の形態を説明する。本発明のU/Dチューナの全体の構成は図1に示すように、バンドパスフィルタ2、高帯域・高周波増幅回路3より成る高周波増幅回路と、第1局部発振器5、第1ミキサー4より成る第1周波数変換回路と、第1IFバンドパスフィルタ6と第1中間周波増幅器7と、第1IFバンドパスフィルタ8及び、第2ミキサー9、第2局部発振器10より成る第2周波変換回路で構成した中間周波回路14と、第2中間周波増幅器11と第3IFバンドパスフィルタ12より成る。

【0019】図1に示すU/Dチューナにおいて、本発明が従来技術と相違する点は、図1中点線の枠で示す中間周波回路14の構成にあり、その詳細な回路を図2に示す。図2において、図3に示す従来例に対応する部分には同一符号を付し、説明を省略する。

【0020】図2に示す中間周波回路14は、バンドパスフィルタ部15と、第1の中間周波信号を第2の中間周波信号に変換する周波数変換部16より成る。

【0021】上記バンドパスフィルタ部15は、高周波チョークコイルL1、接地コンデンサCe、直流阻止用コンデンサC1、マイクロストリップラインL2，L3、上記マイクロストリップラインL2への結合用マイクロストリップラインL4、上記マイクロストリップラインL2，L3間を結合する結合用マイクロストリップラインL5，L6、上記マイクロストリップラインL2との間で共振回路を形成する共振用コンデンサC2、上記マイクロストリップラインL3との間で共振回路を形成する共振用コンデンサC3及び、上記共振回路の出力を次段のトランジスタTr2で構成する第2のミキサー9に結合する結合用コンデンサC4より成る。

【0022】上記各マイクロストリップラインL2，L3，L4，L5，L6は図3に示すように絶縁基板17上に導体18をパターン化して形成した平面型ストリップライン（マイクロストリップライン）であり、図5に

示す従来例のような立体型の分布定数線路（ストリップライン）とは相違した構成にしている。従って、中間周波回路１４のバンドパスフィルタがマイクロストリップラインより成る平面型分布定数回路で構成されるので、製造上のバラツキが少なくなり、所望の特性を持つ共振回路を得ることができる。

【００２３】一方、上記中間周波回路１４において、第２の中間周波数の信号に変換する周波数変換部１６は、上記第２ミキサー９を構成するトランジスタTr2と、上記第２ミキサー９に結合コンデンサＣ５を介して第２の局部発振周波信号を供給する第２局部発振器１０と、上記第２ミキサー９にバイアス電圧を供給する高周波チョークコイルＬ７、接地コンデンサＣｅ、バイアス電圧調整用ボリュームＶＲ及びバイアス供給用電源Ｅにより成るバイアス調整回路で構成する。

【００２４】そして、上記第２ミキサー９を構成するトランジスタTr2は、従来デュアルゲート型ＭＯＳＦＥＴを採用していたのに対して、シングルゲート型の接合型あるいは、ＭＯＳ型ＦＥＴにする。これは、シングルゲート型のＦＥＴの場合、バイアス電圧の変化により入力インピーダンスが変化し易く、また入力容量Ｃｉｓｓが約２Ｐ変化するのに対して相互コンダクタンスＧｍの変化が比較的緩やかであり、電力利得では３ｄＢ程度の変化になる。また、ミラー効果により更に変化量を大きくすることができるためである。

【００２５】本発明の実施形態は、以上のような構成であるので、トランジスタTr1より成る第１中間周波増幅器７で増幅された第１中間周波数信号は、中間周波回路１４に供給され、直流阻止用コンデンサＣ１を介して結合用マイクロストリップラインＬ４に入力し、マイクロストリップラインＬ２とコンデンサＣ２より成る１次側同調回路に導かれる。そして、この１次側同調回路より導出される同調出力は、結合用マイクロストリップラインＬ５，Ｌ６を介して、２次側のマイクロストリップラインＬ３に誘導され、該マイクロストリップラインＬ３と共振用コンデンサＣ３より成る２次側同調回路で共振する同調信号が出力される。

【００２６】上記共振用コンデンサＣ２，Ｃ３とマイクロストリップライン Ｌ２，Ｌ３より成る１次及び２次側同調回路は、バンドパスフィルタを形成する。このバンドパスフィルタの出力は、結合用コンデンサＣ４を介して、次段のシングルゲート型ＦＥＴより成る第２ミキサー９に入力される。

【００２７】第２ミキサー９の入力には、同時に第２局部発振器１０からの第２局部発振周波数信号が結合用コンデンサＣ５を介して供給されている。従って、上記第２ミキサー９で上記同調回路からの受信信号は第２の中間周波数の信号に周波数変換され、第２中間周波増幅器１１に供給される。

【００２８】上記第２ミキサー９を構成するシングルゲート型ＦＥＴのゲート端子には、バイアス電源Ｅよりバイアス電圧調整用ボリュームＶＲで可変分圧したバイアス電圧が供給されている。従って、上記バイアス電圧調整用ボリュームＶＲを調整すると、上記シングルゲート型ＦＥＴのゲート端子のバイアス電圧が変化し、このＦＥＴの入力インピーダンスが変化する。このように、上記シングルゲート型ＦＥＴの入力インピーダンスが変化すると、この変化する特性に応じ、上記シングルゲート型ＦＥＴに接続される上記の共振用コンデンサＣ２，Ｃ３及びマイクロストリップライン Ｌ２，Ｌ３より成る各同調回路の同調特性は連動して変化する。

【００２９】従って、上記バイアス電圧調整用ボリュームＶＲにより上記シングルゲート型ＦＥＴのゲートに印加するバイアス電圧を調整することにより、上記各同調回路の複同調特性の調整を行うことができる。上記のバイアス電圧調整用ボリュームＶＲは半固定式であるので、上記バンドパスフィルタ部１５におけるバンドパス特性の自動調整も可能になる。

【００３０】以上のようにシングルゲート型ＦＥＴのゲートバイアス電圧を調整して上記ＦＥＴの入力インピーダンスを変化させ、上記バンドパスフィルタ部１５の複同調特性を調整するものでは、従来技術で説明したトリマーＺｏによりバンドパスフィルタを構成する中心導体との結合度を調整するものに比べて調整範囲が狭くなる。しかし、絶縁基板上に設けた平面分布定数型のマイクロストリップラインで共振回路を構成するので、このマイクロストリップラインを高精度に形成することができ、特性のバラツキを少なくして調整に支障をきたさないようにすることができる。

【００３１】

【発明の効果】本発明は、以上の構成であるので、第２ミキサーの入力インピーダンスを可変調整するだけで、第１中間周波信号の周波数特性を簡単に調整することができ、調整に要する時間を短縮させることができる。また、上記の周波数特性の調整を第２ミキサーの入力バイアス電圧を可変するだけで行えるので、バラツキが少なく、しかも経時変化の少ない調整を行うことができる。

【００３２】また、第２ミキサーの入力バイアス電圧を調整するだけで、第１中間周波信号の周波数特性を調整することができるので、調整の自動化を容易に行うことができる。更にまた、第１中間周波信号の周波数特性を定めるバンドパスフィルタの共振手段は平面分布定数型のマイクロストリップラインとコンデンサで構成されているので、構造上の可動部分がなく、製造上のバラツキの少ない装置を提供することができる。

【図面の簡単な説明】

【図１】　Ｕ／Ｄチューナの全体構成を示すブロック図である。

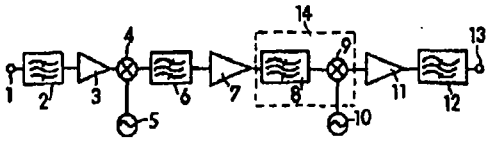
【図２】　本発明の要部の構成を示す回路図である。

【図３】　本発明の要部の構成を示す断面図である。

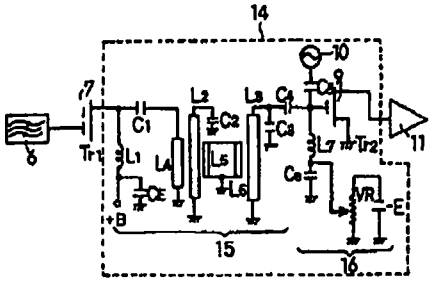
7　　8

【図4】　従来例の構成を示す回路図である。
【図5】　従来例の要部の断面図である。
【符号の説明】
2　バンドパスフィルタ
3　高帯域・高周波増幅器
4　第1ミキサー
5　第1局部発振器
6　第1IFバンドパスフィルタ
7　第1中間周波増幅器
8　第2IFバンドパスフィルタ
9　第2ミキサー
10　第2局部発振器
11　第2中間周波増幅器
14　中間周波回路
L2、L3、L4、L5、L6　中心導体
C2、C3　共振コンデンサ
E　バイアス電圧
VR　バイアス電圧調整用ボリューム
17　絶縁基板
18　マイクロストリップライン

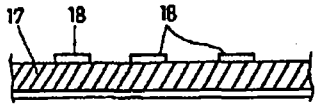
【図1】



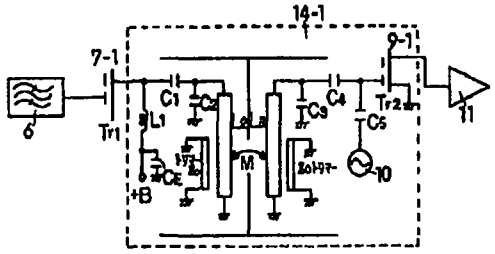
【図2】



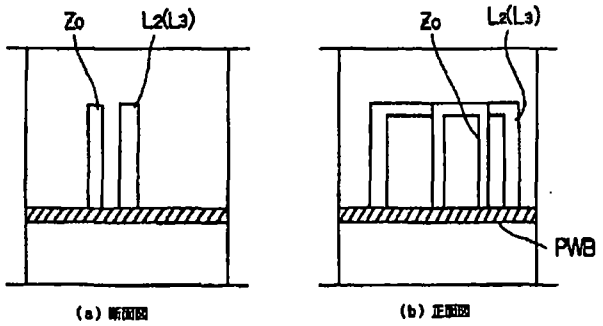
【図3】



【図4】



【図5】



Electronic Acknowledgement Receipt

EFS ID:	1305167
Application Number:	10973917
International Application Number:	
Confirmation Number:	3273
Title of Invention:	Universal platform module and methods and apparatuses relating thereto enabled by universal frequency translation technology
First Named Inventor/Applicant Name:	David F. Sorrells
Customer Number:	26111
Filer:	Michael Q. Lee/Jason Geider
Filer Authorized By:	Michael Q. Lee
Attorney Docket Number:	1744.0330003
Receipt Date:	13-NOV-2006
Filing Date:	27-OCT-2004
Time Stamp:	14:24:26
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	17440330003IDStransmittal.pdf	56471	no	2
Warnings:					

Information:					
2	Information Disclosure Statement (IDS) Filed	17440330003IDS.pdf	373261	no	11
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	AL26.pdf	350681	no	5
Warnings:					
Information:					
4	NPL Documents	AO62.pdf	619372	no	10
Warnings:					
Information:					
5	NPL Documents	AP62.pdf	963063	no	8
Warnings:					
Information:					
			Total Files Size (in bytes):	2362848	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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November 9, 2006

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Art Unit 2616

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Fifth Supplemental Information Disclosure Statement;
2. Form PTO-1449 (4 sheets) listing twenty-five (25) documents (AH77, AI77, AA78-AI78, AA79-AI79, AA80, AB80, AL26, AO62, and AP62);
3. Copies of the cited foreign document (AL26); and
4. Copies of the cited non-patent literature documents (AO62 and AP62).

The above listed documents are being electronically submitted through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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MQL/jeg
Enclosures

606908_1.DOC

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Art Unit 2618

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**
Inventors: Sorrells *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Sixth Supplemental Information Disclosure Statement;
2. Form PTO/SB/08A listing thirty-eight (38) documents (US1-US30 and FP1-FP8);
3. Form PTO/SB/08B listing eight (8) documents (NPL1-NPL8);
4. Copies of the cited foreign patent documents (FP1-FP8); and
5. Copies of the cited non patent literature documents (NPL1-NPL8).

This filing is being electronically submitted through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL:jeg
Enclosures

749766_1.DOC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
Sorrells *et al.*	Art Unit: 2618
Appl. No.: 10/973,917	Examiner: Trinh, Sonny
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Sixth Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying IDS Forms are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicants have listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Document US1 was cited in a Notice of Allowance in related U.S. Patent Application No. 11/020,547, filed December 27, 2004, entitled "Methods And Systems For Down-Converting A Signal Using A Complementary Transistor Structure," directed to related subject matter.

Documents US2-US4 were cited in an Office Action in related U.S. Patent Application No. 10/197,255, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter. Also cited in said Office Action were U.S. Publication Nos. 2002/0070728 and 2002/0163921, and U.S. Patent Nos. 6,963,626; 6,850,742; 6,591,310; and 5,703,584, all of which have already been cited in the present application.

Document US5 was cited in a Notice of Allowance in related U.S. Patent Application No. 10/453,622, filed June 4, 2003, entitled "Active Polyphase Inverter Filter for Quadrature Signal Generation," directed to related subject matter.

Documents US6-US14 and US28-US30 are co-owned patents which are directed to related subject matter.

Documents US15 and US16 were cited in a Notice of Allowance in related U.S. Patent Application No. 10/914,337, filed August 10, 2004, entitled "Method And System For Down-Converting And Up-Converting An Electromagnetic Signal, And Transforms For Same," directed to related subject matter. Also cited in said Notice of Allowance were U.S. Patent Nos. 4,761,798; 6,144,846; 6,400,963; 6,611,569; 6,836,650;

6,853,690; 6,873,836; and 7,194,246, all of which have already been cited in the present application.

Documents US17-US19 were cited in an Office Action in related U.S. Patent Application No. 11/355,167, filed February 16, 2006, entitled "Methods And Systems For Down-Converting A Signal Using A Complementary Transistor Structure," directed to related subject matter.

Documents US20, US21, and FP4-FP8 were cited in an Office Action in Israeli Patent Appl. No. 145,908, filed April 14, 2000, entitled "Device for Frequency Down-Converting Using Undersampling, and Method," directed to related subject matter.

Documents US22-US25 were cited in a Notice of Allowance in U.S. Patent Appl. No. 10/305,299, filed November 27, 2002, entitled "Method and Apparatus for Improving Dynamic Range in a Communication System," directed to related subject matter.

Documents US26 and US27 were cited in a Notice of Allowance in U.S. Patent Appl. No. 10/453,622, filed June 4, 2003, entitled "Active Polyphase Inverter Filter for Quadrature Signal Generation," directed to related subject matter.

Documents FP1-FP3 were cited in an Office Action in Japanese Patent Appl. No. 2000-577764, filed October 18, 1999, entitled "Applications of Universal Translation," directed to related subject matter.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited

in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. The required fee is provided through online credit card payment authorization in the amount of $___ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of $180.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

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in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document FP1 (JP 58-031622) appears to describe a frequency converting circuit. An English abstract is enclosed as document NPL1.

Document FP2 (JP 61-245749) appears to describe a PCM signal transmission system for CATV. An English abstract is enclosed as document NPL2.

Document FP3 (JP 64-048557) appears to describe a circuit for reforming and modulating at least two data signals. An English abstract is enclosed as document NPL3.

Document FP4 (JP 59-022438) appears to describe a bipolar analog-frequency converting circuit. An English abstract is enclosed as document NPL4.

Document FP5 (JP 59-123318) appears to describe an analog-digital converting circuit. An English abstract is enclosed as document NPL5.

Document FP6 (JP 61-193521) appears to describe an analog-digital converting circuit. An English abstract is enclosed as document NPL6.

Document FP7 (JP 62-047214) appears to describe a digital-analog converting circuit. An English abstract is enclosed as document NPL7.

Document FP8 (JP 63-274214) appears to describe a digital/analog converting circuit. An English abstract is enclosed as document NPL8.

☒ 7. Copies of documents FP1-FP8 and NPL1-NPL8 are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the attached IDS Forms are submitted.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), 09/514,004, filed February 25, 2000 (now abandoned), 09/476,093, filed January 3, 2000 (now U.S. Patent No. 7,006,805), 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), and 09/261,129, filed March 3, 1999 (now U.S. Patent No.

6,370,371), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 11/26/07

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SIXTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/973,917
Filing Date	October 27, 2004
First Named Inventor	David F. Sorrells
Art Unit	2618
Examiner Name	Trinh, Sonny
Attorney Docket Number	1744.0330003

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	5,884,154	03-16-1999	Sano *et al.*	
	US2	5,900,746	05-04-1999	Sheahan	
	US3	6,246,695 B1	06-12-2001	Seazholtz *et al.*	
	US4	6,597,240 B1	07-22-2003	Walburger *et al.*	
	US5	7,072,433 B2	07-04-2006	Bell	
	US6	7,190,941 B2	03-13-2007	Sorrells *et al.*	
	US7	7,194,246 B2	03-20-2007	Sorrells *et al.*	
	US8	7,209,725 B1	04-24-2007	Sorrells *et al.*	
	US9	7,218,899 B2	05-15-2007	Sorrells *et al.*	
	US10	7,218,907 B2	05-15-2007	Sorrells *et al.*	
	US11	7,224,749 B2	05-29-2007	Sorrells *et al.*	
	US12	7,233,969 B2	06-19-2007	Rawlins *et al.*	
	US13	7,236,754 B2	06-26-2007	Sorrells *et al.*	
	US14	7,245,886 B2	07-17-2007	Sorrells *et al.*	
	US15	7,194,044 B2	03-20-2007	Birkett *et al.*	
	US16	7,212,581 B2	05-01-2007	Birkett *et al.*	
	US17	4,485,347	11-27-1984	Hirasawa *et al.*	
	US18	5,724,041	03-03-1998	Inoue *et al.*	
	US19	2003/0193364 A1	10-16-2003	Liu *et al.*	
	US20	4,771,265	09-13-1988	Okui *et al.*	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP1	JP 58-031622	02-24-1983	Usui *et al.*		
	FP2	JP 61-245749	11-01-1986	Ito		
	FP3	JP 64-048557	02-23-1989	Booru *et al.*		
	FP4	JP 59-022438	02-04-1984	Shimizu		
	FP5	JP 59-123318	07-17-1984	Kune		
	FP6	JP 61-193521	08-28-1986	Takahashi		
	FP7	JP 62-047214	02-28-1987	Satou *et al.*		
	FP8	JP 63-274214	11-11-1988	Miyake		
	FP9					

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Sheet 2 of 2

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First Named Inventor	David F. Sorrells
Art Unit	2618
Examiner Name	Trinh, Sonny
Attorney Docket Number	1744.0330003

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	US21	5,006,854	04-09-1991	White *et al.*	
	US22	3,643,168	02-15-1972	Manicki	
	US23	4,048,598	09-13-1977	Knight	
	US24	4,145,659	03-20-1979	Wolfram	
	US25	4,313,222	01-26-1982	Katthän	
	US26	5,896,347	04-20-1999	Tomita *et al.*	
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	US28	7,272,164 B2	09-18-2007	Sorrells *et al.*	
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	US33				
	US34				
	US35				
	US36				
	US37				
	US38				
	US39				
	US40				

FOREIGN PATENT DOCUMENTS

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	FP10					
	FP11					
	FP12					
	FP13					
	FP14					
	FP15					
	FP16					
	FP17					
	FP18					

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Sheet 1 of 1

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Examiner Name	Trinh, Sonny
Attorney Docket Number	1744.0330003

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume issue number(s), publisher, city and/or country where published	T[2]
	NPL1	English-language Abstract of Japanese Patent Publication No. JP 58-031622, data supplied by ep.espacenet.com, 1 page (Feb. 24, 1983 - Date of publication of application).	
	NPL2	English-language Abstract of Japanese Patent Publication No. JP 61-245749, data supplied by ep.espacenet.com, 1 page (Nov. 1, 1986 - Date of publication of application).	
	NPL3	English-language Abstract of Japanese Patent Publication No. JP 64-048557, data supplied by ep.espacenet.com, 1 page (Feb. 23, 1989 - Date of publication of application).	
	NPL4	English-language Abstract of Japanese Patent Publication No. JP 59-022438, data supplied by ep.espacenet.com, 1 page (Feb. 4, 1984 - Date of publication of application).	
	NPL5	English-language Abstract of Japanese Patent Publication No. JP 59-123318, data supplied by ep.espacenet.com, 1 page (July 17, 1984 - Date of publication of application).	
	NPL6	English-language Abstract of Japanese Patent Publication No. JP 61-193521, data supplied by ep.espacenet.com, 1 page (Aug. 28, 1986 - Date of publication of application).	
	NPL7	English-language Abstract of Japanese Patent Publication No. JP 62-047214, data supplied by ep.espacenet.com, 1 page (Feb. 28, 1987 - Date of publication of application).	
	NPL8	English-language Abstract of Japanese Patent Publication No. JP 63-274214, data supplied by ep.espacenet.com, 1 page (Nov. 11, 1988 - Date of publication of application).	
	NPL9		
	NPL10		

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⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭58—31622

⑤1Int. Cl.³	識別記号	庁内整理番号
H 04 B 1/26		6538—5K
H 03 D 7/00		7402—5J
H 04 N 5/48		7423—5C

⑬公開　昭和58年(1983) 2 月24日

発明の数　3

審査請求　未請求

（全 6 頁）

⑤4周波数変換回路

⑳特　　願　昭56—130451

㉒出　　願　昭56(1981) 8 月19日

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⑦4代 理 人　弁理士　宮井暎夫

明　　細　　書

1. 発明の名称

周波数変換回路

2. 特許請求の範囲

(1) 第1のコイルと第1の容量からなる第1の並列共振回路と、第2のコイルと第2の容量からなり前記第1の並列共振回路に直列接続された第2の並列共振回路と、前記第1および第2の並列共振回路の接続点とアース間に接続されるとともに第1および第2の並列共振回路の共振周波数より低くなるように共振周波数が選択された第3のコイルおよび第3の容量よりなる第3の並列共振回路とを有するフィルタ回路を備えた周波数変換回路。

(2) 前記第1の並列共振回路と第2の並列共振回路の共振周波数は互いに異なる特許請求の範囲第(1)項記載の周波数変換回路。

(3) 直列接続された第1および第2の結合容量と、これらの結合容量の接続点とアース間に接続された第1のコイルおよび第3の容量よりなる直列共振回路と、この直列共振回路に並列接続されてその直列共振回路とともに並列共振回路を形成しかつ前記直列共振回路の共振周波数が並列共振回路の共振周波数よりも高くなるように選択された第2のコイルとを有するフィルタ回路を備えた周波数変換回路。

(4) 第1のコイルと第1の容量からなる第1の並列共振回路と、この第1の並列共振回路に直列接続された第2のコイルと第2の容量からなる第2の並列共振回路と、前記第1および第2の並列共振回路の接続点とアース間に接続されるとともに第3のコイルと第3の容量からなる直列共振回路に第4のコイルを並列接続したものであってその直列共振回路ならびに前記第1および第2の並列共振回路の共振周波数よりも低く設定された共振周波数をもつ並列共振回路とを有するフィルタ回路を備えた周波数変換回路。

(5) 前記第1の並列共振回路、第2の並列共振回路および直列共振回路の共振周波数の少なくとも1個は異なる周波数である特許請求の範囲第(4)

項記載の周波数変換回路。

3. 発明の詳細な説明

この発明はテレビのチャンネルコンバータ回路等に適用される周波数変換回路に関するものである。

第1図に従来のミクサ回路を示し、第2図にチャンネルコンバータ回路を示している。まず第1図において端子AよりRF（高周波）信号を入力し、端子Bよりローカル信号が入力される。ブロックV_1はRF信号に同調した帯域フィルタであり、コイルL_1，容量C_3で共振回路を構成している。一方端子Bより入力したローカル信号はローカル周波数に共振するコイルL_2，容量C_6の共振回路をもつブロックV_2の帯域フィルタを通過する。これらのブロックV_1，V_2の容量C_1，C_2，C_4，C_5は結合容量であり、前記2信号は、ブロックV_1，V_2の出力にて結合されブロックV_3のミクサ回路に供給される。ブロックV_3において、Q_1はミクサトランジスであり、抵抗R_1，R_2によりベースにバイアスを与え、エミッタ電流を制御してトランジスタQ_1のコレクタにRF信号とローカル信号の周波数の差でコイルL_3と容量C_8に共振した共振回路により変換出力を容量C_{10}を通して端子Cに得るようにしている。なおR_3～R_5は抵抗、C_7はコンデンサ容量である。この回路の手法はイメージリカバリー法と呼ばれ、変換利得を上げる手段として従来よく用いられるものである。

ところで、端子Bにはローカル信号の基本波とともに2次高調波が入力され、その2倍波は、端子Aから入力される他の妨害がある場合や、RF信号とローカル信号の2倍波との間でスプリアス妨害を発生させることになる。このような障害は、つぎに示すような周波数2重変換方式のチャンネルコンバータ等においては特に問題となる。

また、第2図に示すチャンネルコンバータにおいては、端子Aより入力信号を得、これを信号のある帯域を通過させるブロック1の広帯域フィルタを通したのちに、ブロック2のミクサ回路にてブロック3のローカル発振器OSCよりの出力信号と掛算し、信号周波数を受信周波数の最低周波数よりも上で、TV（テレビ）周波数内でも使用されていない帯域、あるいはTV周波数よりも上の中間周波数（IF）に一旦変換し、そのIF（中間）周波数の1CH（チャンネル）分のみを通すブロック4のIFフィルタを通した後に、ブロック5のIF－AMP（増幅器）を通し、あるいはIFフィルタとIF－AMPを多段構成にしてそれぞれを交互に縦続接続するようにする。ブロック5の出力をブロック6の第2のミクサ回路にて、前記IF周波数よりも変換するテレビCHの周波数だけ上にある固定発振器OSC7の出力と掛算し、端子Dより変換されたチャンネル周波数として信号をとりだすしくみになっている。

ところで、希望映像周波数をf_d，　…(1)

ローカル周波数をf_ℓ，　…(2)

IF周波数をf_i，　…(3)

固定発振器周波数をf_x，　…(4)

出力変換周波数をf_o，　…(5)

とすれば、

$2f_\ell - 2f_x = f_o$　…(6)

$2f_x - 2f_\ell = f_o$　…(7)

$f_\ell - f_x = f_o$　…(8)

となるスプリアス妨害が特定のチャンネルで生ずる。

その特定のチャンネルは、(6)式の場合、

$f_\ell = f_d + f_i$　…(9)

$f_x = f_i + f_o$　…(10)

を代入すれば、

$f_d = \frac{3}{2} f_o$　…(11)

(7)式の場合、(9)，(10)式を代入すれば、

$f_d = \frac{1}{2} f_o$　…(12)

(8)式の場合、(9)，(10)式を代入すれば、

$f_d = 2f_o$　…(13)

となる特定チャンネルのみに生ずることになる。

これら3つの妨害はIFフィルタの帯域外抑制能力が大きければ問題ないが、たとえば、f_ℓのレベルを10dBmとし、f_xのレベルを0dBmとし、f_dのレベルを－35dBmとして、このときのブロック2のミクサ回路の1次，2次のローカル抑制能力を30dBとすれば、D/u＝＋10dBとなる。さら

にＩＦフィルタ４の帯域外排除能は特に固体フィルタを用いたとき問題で、これを－50dBとすれば、D/u＝－40dB となる。さらに固定発振器７の２次抑圧比が10dB とすれば

D/u＝－50dB となる。一方、D/u 検知限は－55～－60dBであるから、この妨害はテレビ画面上に検知されてしまうという欠点がある。

そこで、このような特定チャンネルにて発生するスプリアス妨害を除去することができる提案例を第３図ないし第５図に示す。すなわち、第３図において、ブロック１～７は第２図と同機能をはたすものであるので説明は省略する。ブロック８はローカル発振器３の２次高調波を除去するものであり、これは第４図に示すローパスフィルタと、第５図に示すトラップ回路のいずれか一方または両方が用いられるものである。この場合、第４図のローパスフィルタについては(6)式および(7)式に示す２倍波を減衰できるようにインダクタンスL_1～L_nおよび容量C_1～C_nの値を選ぶ。また第５図のトラップ回路についてはインダクタンスL_0，容量C_0により、(6)，(7)式に相当する周波数のみに中心周波数を設定するようにする。このようにして$2f_\ell$の成分を減衰させ、－30～－40dBに減衰させれば、f_0でのD/uは、前述の例では－80dBになり検知限以下になる。またブロック９，１０は(6)，(7)式の$2f_\ell$を除去するとともに、(8)式のf_ℓをも減衰させる必要がある。特にブロック４のＩＦフィルタが弾性表面波フィルタを用いた場合には帯域外減衰度はうまく設定しても－50dB 以上を得るのは難しい。このため、第４図のローパスフィルタあるいは第５図のトラップ回路を用いる必要が生じてくるのである。特に、弾性表面波フィルタでは、通過ロスを－10dB 以下にするのは難しく、ブロック９，１０のローパスフィルタあるいはトラップ回路のロスが大きくなると、システムのトータルＮＦを劣化させるため、この場合には減衰度を大きくとることは難しい。そこで、システムのトータルＮＦには影響の少ないＩＦ増幅器５の後にブロック１１として、(6)，(7)式の$2f_\ell$，(8)式のf_ℓを減衰させるローパスフィルタおよびトラップ回路を挿入し、これによって減衰度を十分とるようにすると、たとえ通過ロスが大きくなってもＩＦ増幅器５により補償されているので問題はない。さらにブロック１２は固定発振器OSCの２倍波を抑えるもので、第４図および第５図のフィルタを挿入することにより、$2f_x$の成分を減衰させることができる。このようにして得られた信号f_0を端子Ｄより得ることができる。

なお、第４図および第５図のフィルタは、中間周波数f_1を高く選ぶことができれば、パターンにより小型な固定フィルタを構成することができる。また(6)，(7)式については、第３図のブロック８～１２の中の少なくとも１つを用いれば効果がある。(8)式についてはブロック９～１１のみに効果があり、その中の少なくとも１つを用いれば効果がある。また第３図においてＩＦフィルタ４として弾性表面波フィルタを用いる場合には、(6)～(8)式中の$2f_\ell$，f_ℓを除去する機能を、弾性表面波のパターン設計時にトラップ回路を設けるように設計することが可能である。ところが、これらのフィルタ回路は、複雑ないしコスト高になるという欠点があった。

したがって、この発明の目的は、簡単かつ安価にローカル信号の高調波その他の妨害信号を阻止でき、チャンネルコンバータ回路に適用した場合には特定チャンネルのスプリアス妨害を除去することができる周波数変換回路を提供することである。

第１の発明の一実施例のフィルタ回路を第６図および第７図に示す。すなわち、このフィルタ回路は、第１図のブロックV1，V2の各結合容量C_1，C_2あるいはC_4，C_5にコイルL_{11}，L_{21}を並列接続して、コイルL_{11}，容量C_1およびコイルL_{21}，容量C_2の第１および第２の並列共振回路を形成したものであり、その共振周波数をコイルL_3，容量C_3の第３の並列共振回路の共振周波数よりも高く選択するようにしている。この場合、第３の並列共振回路は通過帯域に対して共振し、第１および第２の並列共振回路はたとえば第１図のブロックV2に適用する場合、ローカル発振周波数の２倍以上

の高調波のいずれかに共振させるようにする。

並列共振回路のインピーダンス特性は、

$$jX=\frac{1}{\frac{1}{j\omega L}+j\omega C}=\frac{j\omega L}{(1+\omega LC)(1-\omega LC)} \quad \cdots (14)$$

となり、(14)式を第7図に示すと共振点ω_0では、リアクタンス成分の絶対値は最大であるがそれよりωが小さくなればL成分のLの値が小さくなる。このため、第6図において第1の並列共振回路（L_{11}，C_{11}），第2の並列共振回路（L_{21}，C_2）のω_0を(6)，(7)式の$2f_\ell$，$2f_x$に選べば、これらは阻止できるが、f_ℓ，f_xに対しては従来通りの通過特性を示し、この回路により、トラップ回路とタンク回路を同時に構成することもできる。また第1および第2の並列共振回路の共振点をたとえば$2f_\ell$，$3f_\ell$のようにそれぞれ異なった高周波とするトラップ回路をも構成することもできる。

こうしてこの回路を用いるとミクサ回路まわりを簡易化でき、コスト安になる。

第2の発明の一実施例のフィルタ回路を第8図および第9図に示す。すなわち、このフィルタ回路は、第1図のブロックV1，V2の容量C_3，C_6に直列にL_{22}を挿入するか、あるいはコイルL_1，L_2に直列に容量C_{32}を挿入したものである。その場合、L_{22}，C_{32}の直列共振回路の共振周波数をL_{12}，L_{22}，C_{32}の並列共振回路の共振周波数よりも高くなるようにする。

直列共振回路は

$$jX=j\omega L+\frac{1}{j\omega C}=j(\omega L-\frac{1}{\omega C}) \quad \cdots (15)$$

であるから第9図のようなインピーダンス特性となる。したがって直列共振回路（C_{32}，L_{22}）の共振点ω_0を(6)，(7)式の$2f_\ell$，$2f_x$にとれば、f_ℓ，f_xに対しては容量性となる。そこでこの容量成分と、コイルL_{12}とでf_ℓ，f_xに対する並列共振回路を構成すればf_ℓ，f_xに対する帯域特性と、$2f_\ell$，$2f_x$に対する阻止特性とを同時に得ることができることとなる。

なお第10図のようにL_{22}，C_{32}の直列共振回路に容量C'_{32}を並列接続する構成は、L_{22}，C_{32}が$2f_\ell$，$2f_x$で共振すると、f_ℓ，f_xでは容量性となり、容量C_{32}とでタンク回路を構成することができないので不適である。

第3の発明の一実施例のフィルタ回路を第11図に示す。すなわち、このフィルタ回路は、コイルL_{13}，容量C_{13}の第1の並列共振回路と、コイルL_{23}，容量C_{23}の第2の並列共振回路とを直列接続し、その接続点とアース間にコイルL_{43}，容量C_{33}の直列共振回路とコイルL_{33}とを並列接続し、コイルL_{43}，L_{33}，容量C_{33}により第3の並列共振回路を構成し、第1および第2の並列共振回路ならびに直列共振回路の共振周波数を第3の並列共振回路の共振周波数よりも高く選択したものであり、第1および第2の発明の実施例の双方の効果を同時にもたせたものである。その場合、（L_{13}，C_{13}），（L_{23}，C_{23}），（C_{33}，L_{43}）の共振点の少なくとも1つを(6)，(7)式の$2f_\ell$，$2f_x$あるいは$3f_\ell$，$3f_x$以上の高調波に共振させることにより、f_ℓ，f_xに対する帯域通過特性と高周波成分に関するトラップ回路とを同時に構成することができる。

なお、これらのL，C素子はパターンによりその特性をもたせてもよい。

前記第1ないし第3の発明の実施例をチャンネルコンバータに適用する場合、第3図のブロック8～12に適用できることはいうまでもない。また前記(8)式のf_ℓの妨害に関しては、第3図のブロック9～11において第1ないし第3の発明の実施例で与えたトラップ回路の共振点の少なくとも1つをf_ℓとすることにより阻止することができる。

なお、これらの発明はトランジスタミキサのみを限定するものではなく、シングルダイオードミキサ、バランスダイオードミキサ、ダブルバランスダイオードミキサにも適用できることはいうまでもない。またこれらの回路は中間周波数の帯域フィルタと妨害信号の阻止トラップ（主にローカルの高周波）を除去する一体化フィルタとしても用いることができる。

以上のように、この発明の周波数変換回路によれば、従来ミクサ回路に加っていたローカル信号の高調波あるいは他の妨害信号を阻止する回路を簡単かつ安価に構成できるとともに、チャンネル

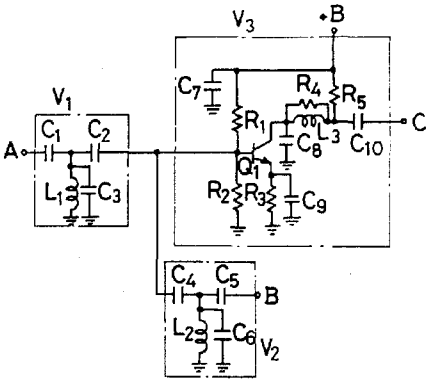
コンバータ回路に用いた場合には、特定チャンネルに生じていたスプリアス妨害を除去でき、品質のよい信号を得ることができるという効果がある。

4. 図面の簡単な説明

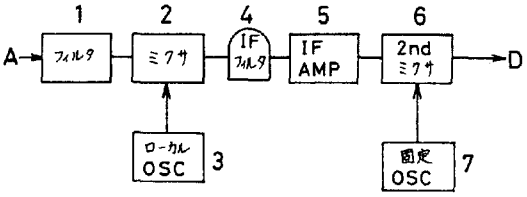
第1図は従来のミクサ回路図、第2図は従来のチャンネルコンバータのブロック図、第3図は提案例のチャンネルコンバータのブロック図、第4図はローパスフィルタ回路図、第5図はトラップ回路図、第6図は第1の発明の一実施例のフィルタ回路図、第7図はその並列共振回路のインピーダンス特性図、第8図は第2の発明の一実施例のフィルタ回路図、第9図はその直列共振回路のインピーダンス特性図、第10図はフィルタ回路例の回路図、第11図は第3の発明の一実施例のフィルタ回路図である。

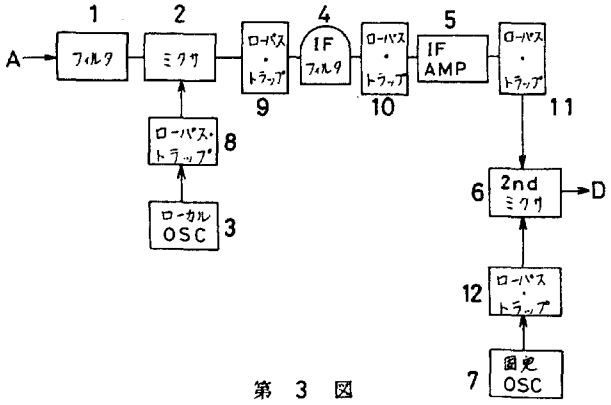
L_3, L_{11}, L_{21}, L_{12}, L_{22}, L_{13}, L_{23}, L_{33}, L_{43} … コイル、C_1, C_2, C_3, C_{32}, C_{13}, C_{23}, C_{33} … 容量

代理人　弁理士　宮井暎夫

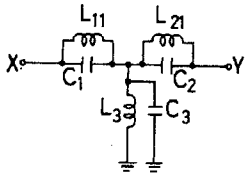


第 1 図

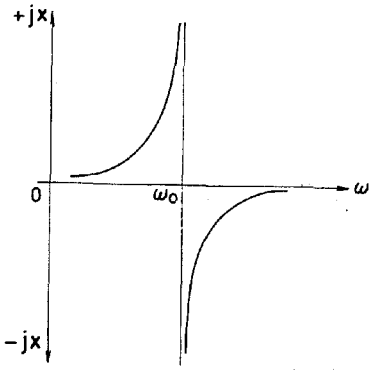




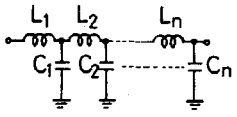
第 3 図



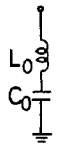
第 6 図



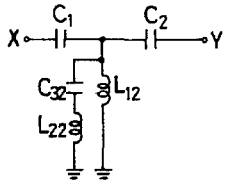
第 7 図



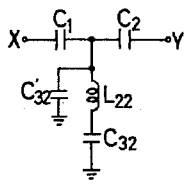
第 4 図



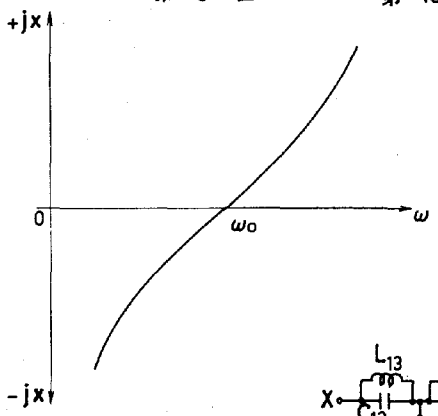
第 5 図



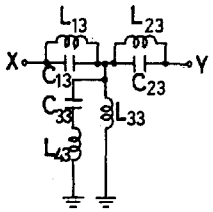
第 8 図



第 10 図



第 9 図



第 11 図

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭61－245749

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H 04 B 14/04		Z－7323－5K	
H 04 J 1/08		8226－5K	審査請求　未請求　発明の数 1　（全4頁）

⑤4発明の名称　ＣＡＴＶ用ＰＣＭ信号伝送方式

⑳特　願　昭60－87929
㉒出　願　昭60(1985)4月24日

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明　細　書

1. 発明の名称

ＣＡＴＶ用ＰＣＭ信号伝送方式

2. 特許請求の範囲

(1) ＰＣＭ信号で第1の搬送波を位相変調したあと更に第2の搬送波を振幅変調して所要側波帯の変調信号を送出する2段変調回路を少くとも一つ有する送信装置と，前記変調信号を受信し直接に位相復調して前記ＰＣＭ信号を再生する1段復調回路を少くとも一つ有する受信装置とを備えたことを特徴とするＣＡＴＶ用ＰＣＭ信号伝送方式。

(2) 前記復調回路は，前記第1および第2の搬送波の各周波数の和および差のいずれか一方に等しい周波数をもつ第3の搬送波で前記変調信号を同期検波して前記位相復調を行う特許請求の範囲第(1)項記載のＣＡＴＶ用ＰＣＭ信号伝送方式。

(3) 前記第3の搬送波は，前記送信装置から前記受信装置へ送られてくる予め定めた周波数をもつ基準波の該周波数成分を含む搬送波に応答して発生される特許請求の範囲第(2)項記載のＣＡＴＶ用ＰＣＭ信号伝送方式。

3. 発明の詳細な説明

〔産業上の利用分野〕

本発明はＣＡＴＶ用ＰＣＭ信号伝送方式、特にＣＡＴＶ（有線テレビジョン）回線を通して音声やデータなどのＰＣＭ信号を伝送するのに好適なＣＡＴＶ用ＰＣＭ信号伝送方式に関する。

〔従来の技術〕

ＣＡＴＶ回線でＰＣＭ信号を伝送する方式として従来、特願昭５９－１７９６８８号明細書記載の方式がある。

第3図は上記の従来のＣＡＴＶ用ＰＣＭ信号伝送方式の構成例を示すブロック図である。送信端側の装置は、音声信号やデータ信号をパルス符号変調し（必要に応じて時分割多重化し）て得られるＰＣＭ信号(1)ないしＰＣＭ信号(n)でそれぞれ周波数f_0の第1の搬送波を多相差動位相変調する

ための位相変調回路１－１ないし１－ｎと、位相変調回路１－１ないし１－ｎが送出する位相変調信号でそれぞれ周波数f_1ないし周波数f_nをもつ第２の搬送波を振幅変調するための振幅変調回路２－１ないし２－ｎとをそれぞれ有するｎ個の２段変調手段を具備している。送信端側の装置は更に、このｎ個の２段変調手段から送られてくる変調信号と、予め定めたチャンネル帯域内に配置するよう変調したテレビジョン信号とを重畳して、その結果得られる周波数分割多重化（ＦＤＭ）信号をＣＡＴＶ伝送路１０へ送出するための合成回路３を備えている。

受信端側の装置は、ＣＡＴＶ伝送路１０を介して送信端側から送られてくるＦＤＭ信号を、テレビジョン信号用の各チャンネルおよび振幅復調回路５－１ないし５－ｎにそれぞれ所定のレベルで分配（あるいは切換え接続）するための分配回路４を備えている。テレビジョン信号用の各チャンネルでは、チャンネル帯域を選択するチューナ(図示省略）でＦＤＭ信号に含まれているテレビジョン信号成分を抽出する。振幅復調回路５－１ないし５－ｎにはそれぞれ位相復調回路６－１ないし６－ｎを接続して、ＰＣＭ信号(1)ないしＰＣＭ信号（ｎ)に復調するためのｎ個の２段復調手段を構成してある。例えば振幅復調回路５－１では、受信したＦＤＭ信号を帯域フィルタ（ＢＰＦ）１１に通して、テレビジョン信号と、ＰＣＭ信号(1)以外の変調信号とを含む周波数帯域の信号成分を抑圧し、ＰＣＭ信号(1)の変調信号を含む周波数帯域の信号成分を通過し、これを復調器１２へ送る。復調器１２は、周波数f_1の第２の搬送波で振幅復調を行い、振幅復調した信号を帯域フィルタ（ＢＰＦ）１３へ送る。ＢＰＦ１３は、振幅復調信号中の不要帯域成分を抑圧して、ＰＣＭ信号(1)の位相変調信号を復元し、これを位相復調回路６－１に送る。位相復調回路６－１は、周波数f_0をもつ第１の搬送波で位相復調を行ってＰＣＭ信号(1)を再生する。他の２段復調手段でも、同様の処理過程によりＰＣＭ信号を再生する。

〔発明が解決しようとする問題点〕

上述した従来のＣＡＴＶ用ＰＣＭ信号伝送方式では、利用者端末側の受信装置内に設けた２段復調手段の回路規模が大きくなり、受信装置が大形化すると共に高価格化するという問題点がある。すなわち、振幅復調回路および位相復調回路を有する２段復調手段では、各段毎に復調器を要する上に、各段の復調後にそれぞれ不要信号成分を抑圧するためのフィルタを必要とするので、回路規模が大きくならざるを得ない。その上、通常のＣＡＴＶ方式では、ＣＡＴＶ伝送路に多数の利用者端末を分岐接続するので、受信装置の高価格化によりＣＡＴＶ方式の設置費用もかなり増大する。

本発明の目的は、上述の問題点を解決し利用者端末用装置を従来よりも小形化・低価格化できるＣＡＴＶ用ＰＣＭ信号伝送方式を提供することにある。

〔問題点を解決するための手段〕

本発明の方式は、ＰＣＭ信号で第１の搬送波を位相変調したあと更に第２の搬送波を振幅変調して所要側波帯の変調信号を送出する２段変調回路を少くとも一つ有する送信装置と，前記変調信号を受信し直接に位相復調して前記ＰＣＭ信号を再生する１段復調回路を少くとも一つ有する受信装置とを備えている。

〔実施例〕

次に、本発明について図面を参照して説明する。

第１図は本発明の一実施例を示すブロック図である。同図の方式は、従来の方式（第３図参照）における受信端側装置中のｎ個の２段復調手段の代りに、ｎ個の１段復調手段を設けるようにしたものである。例えば、ＰＣＭ信号(1)を再生するための復調経路には、受信ＦＤＭ信号に含まれているＰＣＭ信号(1)の変調信号の周波数帯域の信号成分を通過し他の信号成分（すなわち、テレビジョン信号や、ＰＣＭ信号(1)以外の変調信号の周波数帯域の信号成分）を抑圧するための帯域フィルタ（ＢＰＦ）7－1と、ＢＰＦ7－1から送られてくるＰＣＭ信号(1)の変調信号を周波数f_1*の第３の搬送波で位相復調するための位相復調回路８－１とを設けてある。周波数f_1*は、送信端側の振幅変調

回路２－１で上部側波帯（または下部側波帯）を送出する場合、周波数f_1+f_0（またはf_1-f_0）に等しく設定しておく。位相復調回路８－１としては、例えば多相位相変調方式の場合には、同期検波方式による多相位相復調回路を使用する。他の復調経路でも、同様の処理過程によりＰＣＭ信号を再生する。なお、位相復調回路８－１として遅延検波方式の復調回路を使用しても良く、この場合には第３の搬送波が不要になる。

本実施例では、従来の方式の場合と比べて復調器およびそのあとに接続するフィルタの個数を減らすことができ、従来よりも小形で低価格の装置が得られる。

本実施例で、同期検波方式を適用した位相復調回路８－１ないし８－ｎを使用する場合、ＰＣＭ信号(1)ないしＰＣＭ信号（ｎ）の各変調信号がそれぞれ周波数$f_1{}^*$ないし周波数$f_n{}^*$の第３搬送波成分を含んでおれば、受信端側の装置内に搬送波再生回路を設け、受信信号から各第３搬送波成分を抽出し再生して位相復調回路８－１ないし８－ｎに与えれば良い。ＰＣＭ信号(1)ないしＰＣＭ信号（ｎ）の各変調信号がそれぞれ第３搬送波成分を実質的に含んでおらず、受信信号から第３搬送波成分を再生できない場合には、次に説明するように、受信端側で第３の搬送波を発生するための基準となる周波数をもつ基準波信号を送信端側で作成し、この基準波信号を変調してＦＤＭ信号に重畳させ伝送して、受信端側で基準波信号から第３の搬送波を発生するようにすれば良い。

第２図は、第１図の方式において送信端側から基準波信号の変調信号を送信しこれに応答して受信端側で第３の搬送波を発生するための、搬送波発生手段を例示するブロック図である。送信端側に設けた位相同期回路（ＰＬＬ）２０－１ないし２０－ｎはいずれも周波数変換用のＰＬＬであり、周波数f_0をもつ第１の搬送波と、周波数f_aをもつ基準波信号とを受けて、それぞれ周波数f_1ないし周波数f_nをもつ第２の搬送波に変換する。但し、$f_k=N_k\cdot f_a-f_0$（あるいは、$f_k=N_k\cdot f_a+f_0$．$k=1,\cdots,n$，各N_kは予め定めた正整数）なる関係が成立している。更に基準波信号は変調器２１に送られて周波数f_cの搬送波を変調し、この変調信号は帯域フィルタ（ＢＰＦ）２２へ送られる。ＢＰＦ２２を通り不要帯域成分を除去された変調信号は、合成回路３でＦＤＭ信号に重畳されて送信される。

受信端側では、帯域フィルタ（ＢＰＦ）２３で抽出された基準波の変調信号が復調器２４で復調され、周波数f_aの基準波信号に復元される。この基準波信号は、周波数逓倍用の位相同期回路（ＰＬＬ）25－1ないし25－nに送られて、それぞれ周波数$f_1{}^*$ないし周波数$f_n{}^*$をもつ第３の搬送波を発生させる。但し、$f_k{}^*=N_k\cdot f_a$（$k=1,\cdots,n$）なる関係、すなわち$f_k{}^*=f_k+f_0$（あるいは、$f_k{}^*=f_k-f_0$）なる関係が成立している。

なお変調器２１および復調器２４での変復調方式は、振幅変復調あるいは周波数変復調などを適宜に用いる。このように基準波の変調信号をＰＣＭ信号の変調信号と同時に伝送することにより、同期検波用の第３の搬送波を高い周波数精度で容易に発生することができる。

〔発明の効果〕

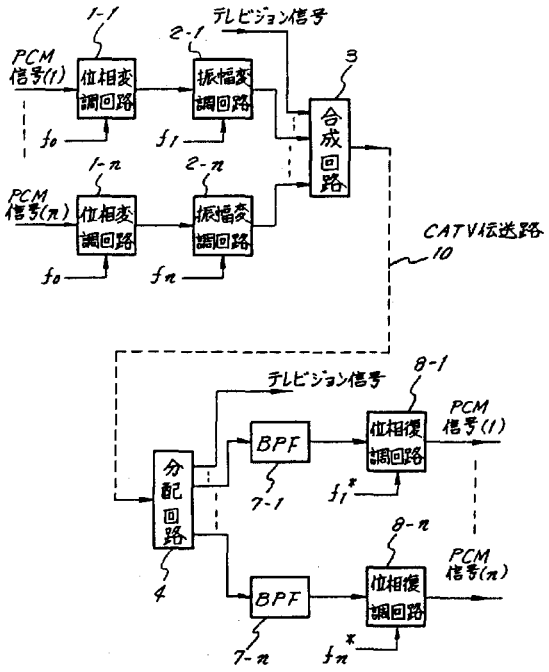
以上説明したように本発明には、利用者端末用装置を従来よりも小形化・低価格化したＣＡＴＶ用ＰＣＭ信号伝送方式を実現できるという効果がある。

4. 図面の簡単な説明

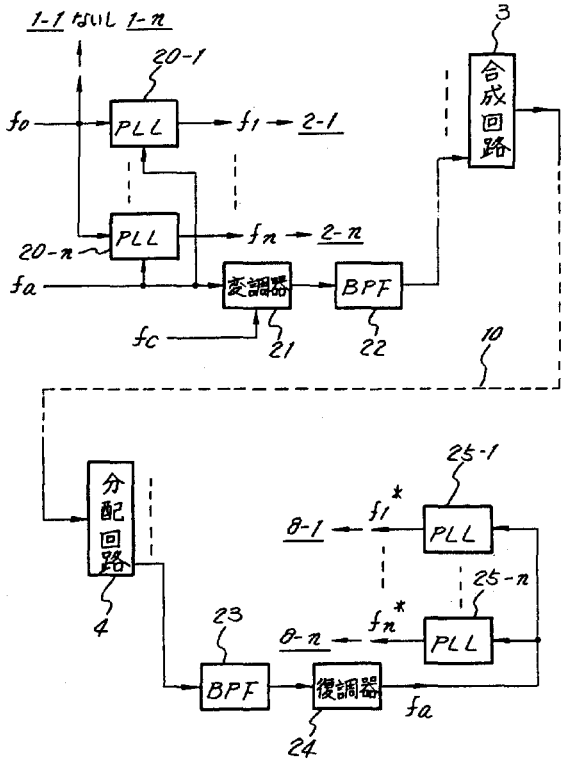
第１図および第２図はいずれも本発明の実施例を示すブロック図、第３図は従来のＣＡＴＶ用ＰＣＭ信号伝送方式を例示するブロック図である。

１－１～１－ｎ……位相変調回路、２－１～２～ｎ……振幅変調回路、３……合成回路、４……分配回路、７－１～７－ｎ、２２，２３……帯域フィルタ（ＢＰＦ）、８－１～８－ｎ……位相復調回路、２０－１～２０－ｎ、２５－１～２５－ｎ……位相同期回路（ＰＬＬ）、２１……変調器、２４……復調器。

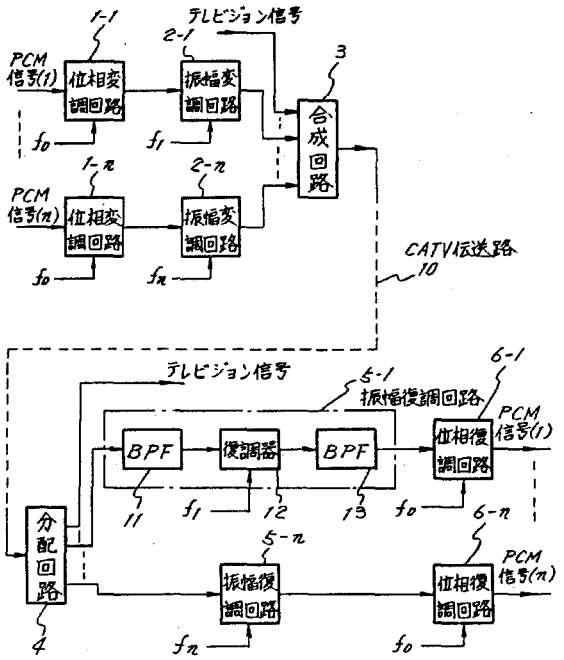
代理人　弁理士　内原　晋


1-1
テレビジョン信号
2-1
PCM信号(1)
位相変調回路
振幅変調回路
3
合成回路
f_0
f_1
1-n
2-n
PCM信号(n)
位相変調回路
振幅変調回路
f_0
f_n
CATV伝送路
10
テレビジョン信号
8-1
PCM信号(1)
分配回路
BPF
位相復調回路
7-1
f_1^*
8-n
PCM信号(n)
BPF
位相復調回路
4
7-n
f_n^*

第 1 図


1-1 ないし 1-n
20-1
PLL
f_0
f_1
2-1
3
合成回路
20-n
PLL
f_n
2-n
f_a
変調器
BPF
f_c
21
22
10
分配回路
4
25-1
8-1
f_1^*
PLL
25-n
8-n
f_n^*
PLL
23
BPF
復調器
f_a
24

第 2 図


1-1
テレビジョン信号
2-1
PCM信号(1)
位相変調回路
振幅変調回路
3
合成回路
f_0
f_1
1-n
2-n
PCM信号(n)
位相変調回路
振幅変調回路
f_0
f_n
CATV伝送路
10
テレビジョン信号
5-1
振幅復調回路
6-1
PCM信号(1)
BPF
復調器
BPF
位相復調回路
分配回路
11
f_1
12
13
f_0
6-n
5-n
PCM信号(n)
振幅復調回路
位相復調回路
4
f_n
f_0

第 3 図

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭64－48557

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審査請求　未請求　請求項の数 2　（全7頁）

㊹発明の名称　少くとも2つのデータ信号を整形し、変調する回路

㉑特　願　昭63－109806

㉒出　願　昭63(1988)5月2日

優先権主張　㉜1987年5月1日㉝米国(US)㉛044883

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明細書の浄書(内容に変更なし)

明　細　書

1. 発明の名称

少くとも2つのデータ信号を整形し、変調する回路

2. 特許請求の範囲

(1) 第1のデータ信号を格納する第1の記憶装置および第2のデータ信号を格納する第2の記憶装置と、

前記第1のデータ信号と前記第2のデータ信号を整形し、前記第1のデータ信号へ第1の搬送波信号を乗じ、前記第2のデータ信号へ第2の搬送波信号を乗ずるために前記第1の記憶装置と前記第2の記憶装置へ選択的に結合されるフイルタ手段と、

を備え、前記第1の搬送波信号と前記第2の搬送波信号は前記フイルタ手段へ結合され、任意の1つの時刻において前記第1の搬送波信号と前記第2の搬送波信号のうちの一方だけが非零であるように、前記第1の搬送波信号と前記第2の搬送波信号は重なり合わないステップ関数であり、それにより前記フイルタ手段の出力は前記第1のデータ信号と前記第2のデータ信号の和を含むことを特徴とする少くとも2つのデータ信号を整形し、変調する回路。

(2) 第1のデータ信号と第2のデータ信号を受ける入力手段と、

前記第1のデータ信号と前記第2のデータ信号を複数のコンデンサへ選択的に結合するために、前記第1のデータ信号と前記第2のデータ信号および前記複数のコンデンサへ結合される第1のスイツチング手段と、

前記コンデンサへ結合される加算手段と、

を備え、前記第1のスイツチング手段と、前記コンデンサと、前記加算手段は前記第1のデータ信号と前記第2のデータ信号に、前記第1のスイツチング手段へ結合されている前記第1の搬送波信号と前記第2の搬送波信号をそれぞれ乗じ、任意の1つの時刻において前記第1の搬送波信号と前記第2の搬送波信号のうちの一方だけが非零であるように、前記第1の搬送波信号と前記第2の搬

送波信号は重なり合わないステップ関数であり、前記加算手段は、前記第１のデータ信号と前記第２のデータ信号の整形され、かつ変調された和を表す第１の出力信号を出力することを特徴とする第１のデータ信号と第２のデータ信号を整形し、変調する回路。

3. 発明の詳細な説明

〔産業上の利用分野〕

本発明は信号伝送装置に使用する変調器の分野に関するものである。

〔従来の技術〕

電子的な信号処理およびデータ伝送においては、送信側から受信側へデータ信号を送信することがしばしば希望される。実際には、送信のためにデータ信号は変調され、受信時にデータ信号が復調される。そのようなデータ信号の伝送には無線伝送（AMとFMを含む）と、電話線伝送が含まれる。伝送すべき生データは、それがアナログとデジタルのいずれであつても、「ベースバンド信号」として知られている。典型的には、ベースバンド信号は、全くではないにしても、効率の高い伝送には不向きである。そのような情報の伝送を容易にするためには、ベースバンド信号を効率的な伝送に適する高い周波数まで高くしなければならない。これは、高周波搬送波の振幅、位相または周波数（あるいはそれらの組合わせ）を伝送すべき情報に従つて変えることにより行われる。この操作は「変調」として知られている。情報を受けるためには、搬送波を除去してその情報を復号しなければならない。この操作は「復調」として知られている。

したがつて、データの送信と受信を行うことができる１つの装置は変調器と復調器を含む。それらの変調器と復調器を一緒にしたものが「モデム」として知られている。近年、コンピュータの使用が増大するにつれてモデムの使用が増大してきた。モデムを使用することにより、一方のコンピュータ端末装置から電話線を介してデータを伝送し、伝送されたデータが１台または複数のコンピュータ端末装置により受信される。

〔発明が解決しようとする課題〕

従来は、ほとんどの変調器はデジタル集積回路により構成されていた。たとえば、デジタル化されているデータはデジタル的に変調され、他のビットがデジタル－アナログ（D/A）変換器へ送られ、変換された信号が伝送される。モデムおよびそれに関連する変調器は、デジタル符号の指令の下にマイクロプロセッサにより制御されるのが普通である。変調器がデジタル的に構成されている場合には、マイクロコントローラ中の符号スペースを変調器にゆだねなければならない。また、集積回路で構成する場合には、デジタル－アナログ変換器は広いシリコンウエハー面積を必要とし、そのために集積回路の製造費が高くなり、かつ集積回路が大きくなる。

更に、高速のモデムを得るためには、データの多ビットを表す「記号」を定めることが望ましい。そのような多ビット記号を得るためにデータを変調する１つの一般的な方法は直角振幅変調（QAM すなわち、Quadrature amplitude moduration）である。直角振幅変調においては、１６個の点をまとめた１つの群が定められる。それらの１６個の点は情報の４ビットから選択できる。ベースバンドデータは、同相チャネルおよび直角チャネルとして知られている２つのチャネルへ変換される。各チャネル情報は２ビットを表すから、２つのチャネルで１６個の点を定めることができる。それから、各チャネルを変調し、濾波してから送信しなければならない。したがつて、直角振幅変調を行うモデムは２つの変調チャネルを必要とするから、シリコンウエハーの面積を更に占める。

それらの欠点を解消するためには、完全なアナログ形式で構成され、かつデジタル変調器よりシリコンウエハーの占有面積が小さい変調器を得ることが望ましい。また、２つのデータチャネルを変調するために１つのアナログ変調器を使用することも望ましい。

したがつて、本発明の目的はモデム用のアナログ変調器を得ることである。

本発明の別の目的は、切換えられるコンデンサ

回路を用い、対応するデジタル変調器よりシリコンウエハーの占有面積が小さいアナログ変調器を得ることである。

本発明の別の更に別の目的は、１つの演算増幅器で構成でき、２つのデータチャネルに使用できるアナログ変調器を得ることである。

〔課題を解決するための手段〕

切換えられるコンデンサ回路がベースバンド、有限インパルス応答フイルタ（BBF）および平衡変調器を１つの演算増幅器で構成する。アナログ変調器は音声帯域モデムにとくに適し、マイクロプロセッサ符号スペースをほとんど、または全く必要としない。ただ1つのベースバンドフイルタの出力が任意の１つの時刻に求められるように、簡単化した正弦関数と余弦関数が実現される。このようにして、２つのデータチャネルの変調を行うために１つの演算増幅器を利用できる。切換えられるコンデンサ回路技術と１つの演算増幅器を使用することにより、対応するデジタル変調器よりもアナログ変調器が占有するシリコンウエハー面積が小さくなる。

この明細書においては切換えられるコンデンサ回路で実現されるアナログ変調器について説明する。本発明を完全に理解できるようにするために、以下の説明においては、コンデンサの数、正弦関数、余弦関数等のような特定の事項の詳細について数多く述べてある。しかし、そのような特定の詳細事項なしに本発明を実施できることが当業者には明らかであろう。その他の場合には、不必要に詳しく説明して本発明をあいまいにしないようにするために、周知の回路構成等については説明しない。

〔実施例〕

以下、図面を参照して本発明を詳しく説明する。

まず、典型的な従来の変調器が示されている第１図を参照する。実（同相）成分11rと虚（（直角位相）成分11iを有するデータ入力１０がベースバンドフイルタ（BBF） 12r,12iへそれぞれ入力される。ベースバンドフイルタ12rの出力３２が乗算器１３へ入力され、その乗算器において

$\cos w(c)t$ １８が乗ぜられ、加算器１５へ出力される。

ベースバンドフイルタ12iの出力３３は乗算器１４へ入力され、その乗算器において$\sin w(c)t$ 19が乗ぜられてから加算器１５へ入力される。加算器１５の出力は帯域フイルタ（BPF）16へ入力される。その帯域フイルタの出力１７は変調され、濾波されたデータ信号である。実際には、第１図に示されている回路は直角振幅変調（QAM）を行うために用いられる。前記したように、それらの変調器は汎用マイクロプロセッサすなわちデジタル信号プロセッサにプログラムされるのが普通である。そのためには符号を専用にすることと、シリコンウエハーの一部の面積を占有する必要がある。

本発明は、正弦乗算器と余弦乗算器をスイッチング変調器として実現するアナログ変調器を実現するものである。入力データ自体および変調周波数はスイッチング変調器のスイッチを制御する。

第２図は、従来の変調器回路の正弦乗算器と余弦乗算器の代りに利用される変調信号を示すタイミング図である。$\cos w(c)t$ １８の代りに変調信号２０が用いられる。この変調信号は３レベル信号であつて、１つおきのクロックで零である。

$\sin w(c)t$ １９は第２図の信号２１に代えられる。信号２１も３レベル変調信号であつて、１つおきのクロックで零である。各クロックにおいてそれらの変調信号の１つが零であるように、それらの変調信号２０と２１は重なり合わない。したがつて、変調信号を発生するベースバンドフイルタのただ１つの出力が任意の１つの時刻に求められる。データチャネル入力を多重化することにより、ただ１つのベースバンドフイルタ／変調器を必要とするから、性能を犠牲にすることなしにシリコンウエハーの面積を小さくできる。

本発明の好適な実施例を第３図に示す。各データチャネル11rと11iは、この実施例ではアナログシフトレジスタを含む遅延線に入力される。たとえば、第３図においては、ただ１つのアナログシフトレジスタ２２が示されている。しかし、シ

フトレジスタは各データチャネルに設けられ、それらのシフトレジスタの出力は、第3図に示されているような種類の1つのベースバンドフイルタ／変調器に多重化される。第3図にはその多重化する回路は示していないが、データチャネル11r，11iの入力を第3図に示されている回路へ交互に供給するための適当な任意の手段を、第5図に示すように用いることができる。

アナログシフトレジスタ22は2ビット／セルデジタルシフトレジスタと、その後段の2ビット／D/A変換器で構成される。ここで説明している実施例においては、初めの3個のセル22A～22Cと後の3個のセル22D～22Fが代表的な例として示されている。各セルの出力端子がNチャネル・トランジスタ23A～23Fのソースへそれぞれ結合される。

それらのトランジスタ23A～23Fのゲートが相B（PB）クロック信号39へ結合される。トランジスタ23A～23Fのドレインがトランジスタ24A～24Fのドレインへ結合される。トランジスタ24A～24Fのソースは接地され、ゲートは相A（PA）クロック信号38へ結合される。PA38とPB39は重なり合わないクロック信号であつて、ここで説明している実施例においては、第4図に示されている回路により発生される。

トランジスタ23A～23Fと24A～24Fのドレインはコンデンサ25A～25Fの1つの端子へそれぞれ結合される。コンデンサ25A～25Fの他の端子が回路点26へ結合される。その回路点26は演算増幅器27の反転入力端子へ結合される。演算増幅器27の非反転入力端子は接地され、出力端子は回路点29と、コンデンサ30とNチャネル・トランジスタ31の並列回路とを介して回路点26へ結合される。そのトランジスタ31のゲートは相1クロック信号34へ結合される。

本発明の好適な実施例のベースバンドフイルタは直線形であるから、それのインパルス応答は対称的である。したがつて、ここで説明している実施例における24点インパルス応答はただ12個の入力コンデンサを必要とし、対称的なインパルス応答の半分を発生する。

入来データx(n)は1秒間当り2400ビットのビット率で変化する。変調器／ベースバンドフイルタは、ここで説明している実施例においては、9600Hzの速さで標本化する。

600Hzボー速度で一緒にまとめられる4ビットデータは2つの2ビット信号11r，11iにそれぞれ分割される。適切なシフトレジスタへ入力される前は、データは差動符号器を通され、その差動符号器において2つの信号11rと11iはプラスまたはマイナス1およびプラスまたはマイナス3の値を得て16個の点のQAM信号群を構成する。前記したように、アナログシフトレジスタ22は、セル当り2つのデジタルビットと、その後段の2ビットD/A変換器により構成される。

トランジスタ23A～23Fと24A～24Fは、ここで説明している実施例においては、9600Hzの標本化周波数で制御されるスイッチとして機能する。したがつて、コンデンサ25A～25Fはアースとシフトレジスタ22の間で切換えられる。コンデンサ25A～25Fのスイッチングはクロック信号PA38とPB39により制御される。それらのクロック信号は第4図に示されている回路により発生される。2ビットカウンタ40がクロック信号50へ結合される。そのクロック信号の周波数は搬送波の周波数（すなわち、変調信号20，21の周波数）の4倍である。カウンタ40は最下位ビット(LSB)41と最上位ビット（MSB）42を出力する。

最上位ビット42はアンドゲート44，47の1つの入力端子へ入力される。アンドゲート47の他の入力端子へ相1（P1）信号34が入力される。アンドゲート44の他の入力はP1 34であり、アンドゲート46の他の入力はP2 35である。

アンドゲート44，45の出力端子はオアゲート48へ結合される。アンドゲート46，47の出力端子はオアゲート49へ結合される。オアゲート48の出力はPA 38である。オアゲート49の出力はPB 39である。

第4図に示されている回路は、2クロックサイ

クルに対してPA 38 がP1 34 に等しく（およびPD 39=P2 35)、その後に続く2クロックサイクルではPAがP2に等しい（およびPBはP1に等しい）。しかし、前記したように、データチャネル11rと11iは、1つおきのクロックサイクルで、第3図の変調器／ベースバンドフイルタ回路へ結合される。このようにして、3レベル正弦関数20と3レベル余弦関数21により求められる+1と-1の乗算をベースバンドフイルタで行うことができる。ベースバンドフイルタは直線フイルタであるから、入力+1または-1を乗ずることは出力に+1または-1を乗ずることと同じである。+1の乗算は、PB 39がP1 34に等しく、PA 38がP2 35に等しい時に行われる。-1の乗算はPB 39がP2 35に等しく、したがつてPA 38がP1 34に等しい時に行われる。

前記したように、データx(n)の実数部と虚数部はプラスまたはマイナスの1と、プラスまたはマイナスの3の値をとる。それらの入力レベルは分圧器または他の任意の適当な手段で発生できる。

の容量、

CFB＝コンデンサ30の容量、

x(n)＝入力データ（第1図の11rまたは11i）

である。

以上、1つの加算増幅器を用いて、切換えられたコンデンサ技術で実現されたアナログ変調器について説明した。

4. 図面の簡単な説明

第1図は従来の変調器の回路図、第2図は本発明で用いられる簡単化した正弦関数と余弦関数を示すタイミング図、第3図は本発明のアナログ変調器の切換えられるコンデンサの回路構成を示す回路図、第4図は第3図の回路のためのスイッチング信号の発生を示す回路図、第5図は本発明の2つのデータ入力チャネルを示すブロック図である。

22・・・・アナログシフトレジスタ、22A～22F・・・・シフトレジスタのセル、27・・・・演算増幅器、40・・・・カウンタ、44～47・・・・アンドゲート、48，49・・・・オアゲート。

種々の値のデータ入力の例がシフトレジスタ22のセル22A，22Eに示されている。

いくつかのセルが0値を含んでいる様子が示されている。しかし、ここで説明している実施例においては、0はシフトレジスタに格納されない。それよりも、入力コンデンサ25A～25Fは任意の1つの時刻に非零のセルだけに結合される。9600 Hzの標本化速度のために、ある時刻にはシフトレジスタ22にはただ2つの非零値がある。

第3図の回路は有限インパルス応答ベースバンドフイルタおよび変調器として機能する。正弦と余弦の搬送波の代りに3レベル波形の独特の実現のために、実数データチャネルと虚数データチャネルのために1つの組合わされた変調器／ベースバンドフイルタを使用できる。

本発明のベースバンドフイルタの出力は次式で与えられる。

$$Out(n) = -\sum_{M=1}^{34}[(Cm)/(CFB)]\{x(n-m)\}$$

ここに、Cm＝選択されたコンデンサ25A～25F

特許出願人　シリコン・システムズ・インコーポレーテッド

代理人　山川政樹（ほか2名）

図面の浄書(内容に変更なし)

Fig. 1 (従来技術)

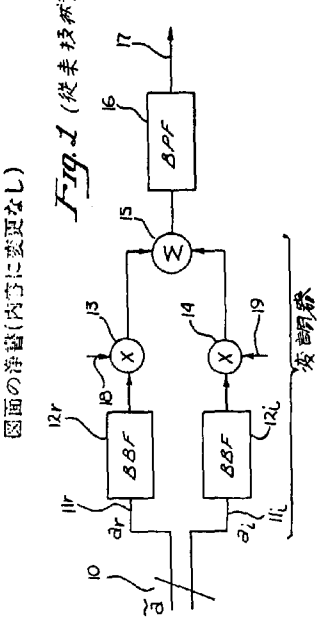


Fig. 2

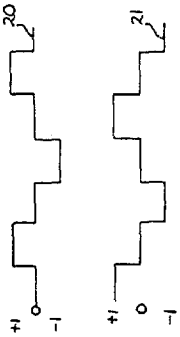
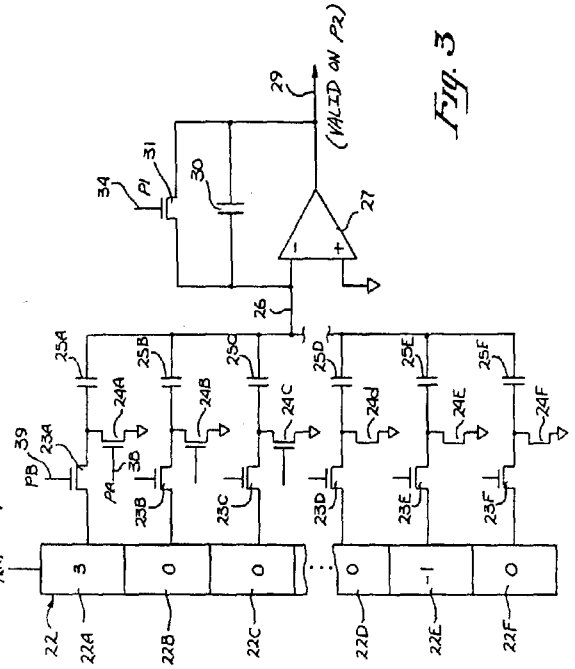


Fig. 3



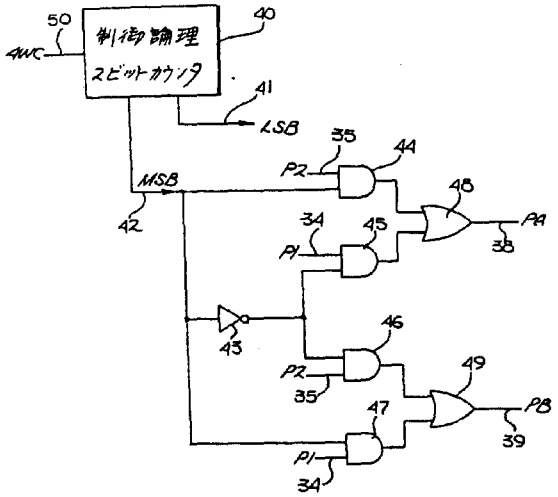


Fig. 4

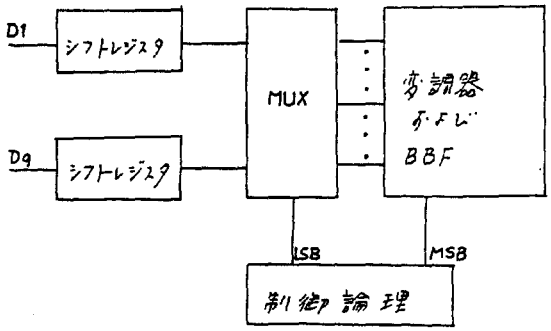


Fig. 5

手続補正書(方式)

特許庁長官殿　　昭和 63. 8. 25

1. 事件の表示

昭和 63 年 特 許 願 第 109806 号

2. 発明の名称

少くとも2つのデータ信号を整形し受信する回路

3. 補正をする者

事件との関係　特 許 出願人

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5. 補正命令 ~~拒絶理由通知~~ の日付　昭和 63 年 7 月 26 日

~~補正により増加する発明の数~~

6. 補正の対象
(1) 願書の出願人の欄
(2) 委任状
(3) 明細書
(4) 図面

7. 補正の内容
(1) 別紙願書の通り
(2) 別紙の通り
(3) 明細書の浄書(内容に変更なし)
(4) 図面の浄書(内容に変更なし)

特許庁 63. 8. 25 出願第二課

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭59—22438

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H 03 K 7/06		6942—5 J	
//H 03 K 13/20	1 0 1	7530—5 J	発明の数　1
			審査請求　未請求

（全 7 頁）

⑤4両極性アナログ—周波数変換回路

⑳特　　願　昭57—130398
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明　　細　　書

1.発明の名称　両極性アナログ—周波数変換回路

2.特許請求の範囲

1. 極性を有する入力アナログ信号と、該入力アナログ信号とは逆極性の逆極性入力アナログ信号とを、交互に切り換える入力切換回路と、該入力切換回路から入力するアナログ信号を両極性共用の回路素子により積分し、アナログ信号の極性によつて異なる極性の積分出力信号を出力する積分回路と、一方の極性の積分出力信号レベルが一方の極性の基準値を越えた時に比較出力信号を第1出力端子から出力し、他方の極性の積分出力信号レベルが他方の極性の基準値を越えた時に比較出力信号を第2出力端子から出力し、第1出力端子及び第2出力端子の比較出力信号によつて積分回路をリセットさせる比較回路と、比較回路の第1出力端子からの比較出力信号と該信号に続く第2出力端子の比較出力信号とによつて1個の周波数出力信号を発生する周波数出力信号発生回路と、比較回路の第1出力端子及び第2出力端子からの比較出力信号の立上りによつて入力切換回路を切換える切換制御回路と、積分回路の積分出力信号の極性及び入力切換回路の切換状態に応じて極性を判別し、表示する極性表示回路とを備えた両極性アナログ—周波数変換回路。

3.発明の詳細な説明

本発明は電圧や電流などのアナログ信号を周波数に変換すると共に、そのアナログ信号の極性を表示する極性表示機能付両極性アナログ—周波数変換回路の改良に関する。

従来の両極性アナログ—周波数変換回路は、単極性アナログ—周波数変換回路を利用するものであり、その場合、バイアス入力をあらかじめ印加したり、アナログ信号を絶対値回路により絶対値に変換し、該絶対値をA/D変換器に入力するなどの手段がとられてきた。しかし、これらの手段は、正負アナログ信号の変換精度を等しくできない、アナログ信号の入力範囲をせ

ばめてしまう、アナログ信号の入力レベルが小さくなると、極性表示が不正確になる、などの問題があつた。また、微小アナログ信号入力時に影響するオフセットドリフト誤差を低減させること、及び無入力時のオフセットドリフトによる起動を防ぐことが課題であつた。

本発明の目的は、上述した問題点及び課題を解決し、正と負とでの変換精度を等しくすることができ、アナログ信号の入力範囲をせばめることがなく、アナログ信号の入力レベルが小さくなつても、極性を正確に判別することができ、しかもオフセットドリフト誤差を大幅に低減することができ、無入力時のオフセットドリフトによる起動をなくすことができる両極性アナログ－周波数変換回路を提供することである。

この目的を達成するために、本発明は、極性を有する入力アナログ信号と、該入力アナログ信号とは逆極性の逆極性入力アナログ信号とを、交互に切り換える入力切換回路と、該入力切換回路から入力するアナログ信号を両極性共用の回路素子により積分し、アナログ信号の極性によつて異なる極性の積分出力信号を出力する積分回路と、一方の極性の積分出力信号レベルが一方の極性の基準値を越えた時に比較出力信号を第１出力端子から出力し、他方の極性の積分出力レベルが他方の極性の基準値を越えた時に比較出力信号を第２出力信号から出力し、第１出力端子及び第２出力端子の比較出力信号によつて積分回路をリセットさせる比較回路と、比較回路の第１出力端子からの比較出力信号と該信号に続く第２出力端子からの比較出力信号とによつて１個の周波数出力信号を発生する周波数出力信号発生回路と、比較回路の第１出力端子及び第２出力端子からの比較出力信号の立上りによつて入力切換回路を切り換える切換制御回路と、積分回路の積分出力信号の極性及び入力切換回路の切換状態に応じて極性を判別し、表示する極性表示回路とを備えたものである。

以下、本発明を図示の実施例に基づいて詳細に説明する。

第１図は本発明の一実施例を示す。入力端子t_1には極性を有する入力アナログ信号E_xが入力し、入力端子t_2には入力アナログ信号E_xとは逆極性の逆極性入力アナログ信号$-E_x$が入力する。入力切換回路１は切換スイッチ２、３及びスイッチドライバ４、５から成る。積分回路６は、抵抗Ｒ、コンデンサＣ、演算増幅器７、リセットスイッチ８及びリセットスイッチドライバ９から成り、これらは両極性共用の回路素子である。１０は比較回路で、二つのコンパレータ１１、１２及び等しい基準電圧E_sの基準電源１３、１４から成る。コンパレータ１１の反転入力端子には正の基準電圧$+E_s$が印加され、コンパレータ１２の非反転入力端子には負の基準電圧$-E_s$が印加される。比較回路１０の第１出力端子１５と第２出力端子１６とは波形整形用のバッファ１７、１８を経てＲＳフリップフロップ１９、オアゲート２０及び極性表示回路２１にそれぞれ接続される。ＲＳフリップフロップ１９の出力端子Ｑから周波数出力信号fが出力される。オアゲート２０の出力側にはリセットスイッチドライバ９及び単一パルス発生回路２２が接続され、単一パルス発生回路２２の出力側にはＴフリップフロップ２３が接続される。Ｔフリップフロップ２３の出力端子Ｑは極性表示回路２１に接続されると共に、スイッチドライバ４及びインバータ２４を経てスイッチドライバ５に、それぞれ接続される。極性表示回路２１は極性表示信号Ｐを出力するもので、本実施例では極性表示信号Ｐは、ローレベルで正を、ハイレベルで負を、それぞれ表示する。なお、切換スイッチ２、３及びリセットスイッチ８は例えば電界効果トランジスタにより構成される。

次に、動作を第２図のタイムチャートを参照しつつ説明する。入力アナログ信号E_xの極性が正である場合には、入力端子t_1には入力アナログ信号$+|E_x|$が、入力端子t_2には逆極性入力アナログ信号$-|E_x|$が、それぞれ印加される。Ｔフリップフロップ２３の出力初期状態がローレベルであると、インバータ２４を経てスイッ

チドライバ5が動作し、切換スイッチ3がオンとなる。スイッチドライバ4は動作しないので、切換スイッチ2はオフである。これによつて、逆極性入力アナログ信号－|Ex|が積分回路6に入力され、正の方向に積分される。コンパレータ11は正の積分出力信号を正の基準電圧＋Esと比較し、この積分出力信号レベルが正の基準電圧＋Esを越えた時にハイレベルの比較出力信号を第1出力端子15から出力する。その結果、バッファ17及びオアゲート20の出力もハイレベルとなる。オアゲート20のハイレベルの出力によつてリセットスイッチ8はオンとなり、コンデンサCの充電電荷を放電し、積分出力信号のレベルを積分開始電位である零電位とする。同時に、バッファ17の出力によつてRSフリップフロップ19はセットされ、その出力端子Qの出力レベルはハイレベルとなる。また、オアゲート20の出力の立上りによつて単一パルス発生回路22は所定パルス幅の単一パルスを発生し、Tフリップフロップ23の入力端子Tに入力し、その出力端子Qの出力レベルをハイレベルにする。これによつて、スイッチドライバ4が動作して、切換スイッチ2をオンにし、スイッチドライバ5が動作を止めて、切換スイッチ3をオフにするので、入力アナログ信号＋|Ex|が積分回路6に入力される。積分出力信号レベルが零電位に戻つたことによつて、比較出力信号が零レベルになるので、リセットスイッチ8はオフとなり、今度は積分回路6は負の方向に入力アナログ信号＋|Ex|を積分する。コンパレータ12は負の積分出力信号が負の基準電圧－Esを下まわつた時にハイレベルの比較出力信号を第2出力端子16から出力する。その結果、バッファ18及びオアゲート20の出力はハイレベルとなり、RSフリップフロップ19はリセットされて、その出力端子Qの出力レベルはローレベルとなり、リセットスイッチ8はオンとなつて、コンデンサCの充電電荷を放電し、単一パルス発生回路22は単一パルスを発生して、Tフリップフロップ23の出力をローレベルにし、切換スイッチ2をオフとし、切換スイッチ3をオンとする。このような動作が繰り返されて、入力アナログ信号Exの極性が変わらない限り、積分回路6の積分出力信号は第2図に示されるように周期T_1、T_2で鋸歯状波を交互に折り返した波形となる。そして、入力アナログ信号Exの極性が変化しない間、比較回路10の第1出力端子15と第2出力端子16とは交互に比較出力信号を出力し、第1出力端子15からの比較出力信号とそれに続く第2出力端子16からの比較出力信号の両方によつてRSフリップフロップ19は1個のパルスを発生し、このパルスを周波数出力信号fとして出力する。

極性表示回路21はバッファ17、18の出力及びTフリップフロップ23の出力に応じて入力アナログ信号Exの極性を判別し、表示するもので、その一例を第3図に示す。25は遅延回路、26、27はインバータ、28～31はアンドゲート、32、33はオアゲート、34はRSフリップフロップである。この極性表示回路21は、バッファ17がハイレベルの出力を出す直前のTフリップフロップ23の出力がローレベルであれば、極性を正と判別し、ハイレベルであれば、極性を負と判別し、バッファ18がハイレベルの出力を出す直前のTフリップフロップ23の出力がローレベルであれば、極性を負と判別し、ハイレベルであれば、極性を正と判別する。即ち、バッファ17がハイレベルの出力を出す直前は積分回路6は正の方向に積分しているから、積分回路6に入力しているアナログ信号の極性は負であり、その時Tフリップフロップ23の出力がローレベルということは切換スイッチ3がオンしていることであるから、入力しているアナログ信号は逆極性入力アナログ信号－Exであり、その極性が負なら、入力アナログ信号Exの極性は正となるのである。

第3図において、バッファ17のハイレベルの出力がアンドゲート28、31に入力した時、その直前のTフリップフロップ23の出力は遅

延回路25によつて遅延されて、アンドゲート28に直接、そしてアンドゲート31にインバータ27を経て、それぞれ入力されているので、遅延回路25の出力がローレベルであれば、アンドゲート31がハイレベルの出力をオアゲート33を経てRSフリップフロップ34のリセット入力端子Rに送り、これをリセットして、極性表示信号Pをローレベルとし、極性を正であると表示する。遅延回路25の出力がハイレベルであれば、アンドゲート28がハイレベルの出力をオアゲート32を経てRSフリップフロップ34のセット入力端子Sに送り、これをセットして、極性表示信号Pをハイレベルとし、極性を負であると表示する。

バッファ18のハイレベルの出力がアンドゲート29、30に入力した時に、その直前のTフリップフロップ23の出力は遅延回路25によつて遅延されて、アンドゲート29にインバータ26を経て、そしてアンドゲート30に直接、それぞれ入力されているので、遅延回路25の出力がローレベルであれば、アンドゲート29がハイレベルの出力を出して、RSフリップフロップ34をセットし、極性表示信号Pをハイレベルとし、遅延回路25の出力がハイレベルであれば、アンドゲート30がハイレベルの出力を出して、RSフリップフロップ34をリセットし、極性表示信号Pをローレベルとする。

入力アナログ信号E_xと周波数出力信号fとの関係をオフセットドリフトV_fによる影響も含めて求めると、以下のようになる。

周波数出力信号fはRSフリップフロップ19の出力であるから、その周期は積分回路6の積分出力信号の周期$T=T_1+T_2$と等しくなる。周期T_1と周期T_2とは下式で表わされる。

$$T_1=\frac{C\cdot R\cdot E_s}{E_x+V_f} \tag{1}$$

$$T_2=\frac{C\cdot R\cdot(-E_s)}{-E_x+V_f}=\frac{C\cdot R\cdot E_s}{E_x-V_f} \tag{2}$$

したがつて、

$$T=T_1+T_2=\frac{C\cdot R\cdot E_s}{E_x+V_f}+\frac{C\cdot R\cdot E_s}{E_x-V_f}=\frac{2E_x\cdot C\cdot R\cdot E_s}{E_x^2-V_f^2} \tag{3}$$

$$f=\frac{1}{T}=\frac{E_x^2-V_f^2}{2E_x\cdot C\cdot R\cdot E_s}=\frac{E_x}{2\cdot C\cdot R\cdot E_s}-\frac{\frac{V_f^2}{E_x^2}}{2\cdot C\cdot R\cdot E_s} \tag{4}$$

即ち、(4)式の第2項がオフセットドリフトV_fによる変換誤差である。この変換誤差を$\triangle f$とし、f'をオフセットドリフトV_fのない時の周波数出力信号とすると、(5)式が求まる。

$$\triangle f=\frac{f-f'}{f'}=-\frac{V_f^2}{E_x^2} \tag{5}$$

つまり、周波数出力信号fの1周期T内で、オフセットドリフトV_fの影響が(1)式及び(2)式からわかるように正と負とに振り分けられた形となり、オフセットドリフトV_fの影響は$-V_f^2/E_x^2$に減少する。

積分回路6の積分方向を入力アナログ信号E_xの極性によつて正の方向のみ、或は負の方向のみに限ることによつて入力アナログ信号E_xを周波数に変換することができるが、この方法では回路構成が簡単であるという長所はあるが、オフセットドリフトV_fによる影響は低減されない。例えば正方向の積分のみの場合、その周波数出力信号f_1及び変換誤差$\triangle f_1$は下記のようになる。

$$f_1=\frac{1}{T_1}=\frac{E_x+V_f}{C\cdot R\cdot E_s} \tag{6}$$

$$\triangle f_1=\frac{f_1-f_1'}{f_1'}=\frac{V_f}{E_x} \tag{7}$$

例として、$E_x=100\,mV$の時に$V_f=10\,mV$であつた場合の変換誤差を求めてみると、本実施例では−1%であるのに対し、正方向の積分のみの場合には10%となる。

また、周波数出力信号fの1周期T内で、積分出力信号の極性を反転させていることにより以下の長所が生ずる。即ち、正方向又は負方向のみの積分の場合、$E_x=0$とすると、(6)式は下記の(8)式となり、無入力時においてもオフセットドリフトV_fに比例した周波数出力信号f_1を出

してしまう。

$$f_1 = \frac{1}{T_1} = \frac{V_f}{C \cdot R \cdot E_s} \qquad (8)$$

これに対して、本実施例によれば、(4)式において$E_x = 0$とおけば、

$$f = -\infty \qquad (9)$$

となり、即ち無入力時では起動しないことになる。

本実施例によれば、積分回路6の各回路素子は入力する正負両極性のアナログ信号$+|E_x|$又は$-|E_x|$に共用されるものであり、その積分出力信号のレベルは正負で絶対値が等しくなるので、正と負とでの変換精度を等しくすることができる。これに対して、従来の絶対値回路を有する両極性アナログ—周波数変換回路においては、絶対値回路が一方の極性の誤差、例えば抵抗のマッチング誤差、オフセット誤差などを有し、これらの誤差は正の入力と負の入力とでは逆に作用するので、正負の入力の変換精度を等しくすることはできない。また、本実施例によれば、バッファ17、18及びTフリップフロップ23の出力に応じて入力アナログ信号E_xの極性を判別しているので、入力アナログ信号E_xのレベルが小さくても、極性の判別を正確にすることができるが、従来の両極性アナログ—周波数変換回路では、入力アナログ信号のレベルを零レベルとコンパレータにより比較することで、極性を判別しているので、入力アナログ信号のレベルが小さくなると、コンパレータの出力が不安定となり、極性を正確に判別することができない。更に、本実施例によれば、積分回路6は異なる極性の積分出力信号を出力するもので、正負両極性ともフルレンジ使用することができるので、アナログ信号の入力範囲をせばめることがない。従来のバイアス入力を印加するタイプの両極性アナログ—周波数変換回路では、積分回路は正負両極性の入力に対して出力レンジは正のみを用いるので、アナログ信号の入力範囲が½にせばめられてしまう。

図示実施例において、RSフリップフロップ19が本発明の周波数出力信号発生回路に相当し、単一パルス発生回路22、Tフリップフロップ23及びインバータ23が本発明の切換制御回路に相当する。

なお、第2図において入力アナログ信号E_xが正又は負に保持されている時間は積分回路6の積分出力信号の周期Tの2倍程度に示されているが、これは図の関係からで、実際は周期Tに比べて著しく長い。

積分回路6は演算増幅器7を用いるものには限定されない。例えば、入力アナログ信号が電流の場合には、抵抗、コンデンサ及びリセットスイッチのみから成るものでもよい。

比較回路10は二つのコンパレータ11、12を用いるものには限定されず、コンパレータを一つにして、その出力を積分出力信号の正負に応じて第1出力端子15と第2出力端子16とに振り分けるようにしてもよい。

極性表示回路21は第3図のものには限定されない。積分回路6において、負方向の積分が2回続いたこと、又は正方向の積分が2回続いたことをアナログ的又はデジタル的に検出し、その時のTフリップフロップ23の出力によつて極性を判別するようにしてもよい。

以上説明したように、本発明によれば、積分回路において入力アナログ信号又は逆極性入力アナログ信号を両極性共用の回路素子により積分するようにしたから、正と負とでの変換精度を等しくすることができる。また、積分回路を入力するアナログ信号の極性によつて異なる極性の積分出力信号を出力するものにしたから、アナログ信号の入力範囲をせばめることがない。更に、積分回路の積分出力信号の極性及び入力切換回路の切換状態に応じて極性を判別し、表示するようにしたから、アナログ信号の入力レベルが小さくなつても、極性を正確に判別することができる。しかも、積分出力信号が基準値を越える毎に入力アナログ信号と逆極性入力アナログ信号とを交互に切り換えて積分回路に入力させるようにしたから、オフセットドリフト

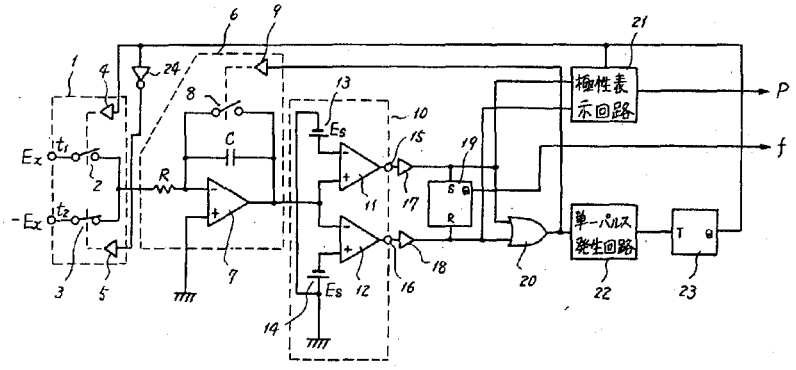
誤差を大幅に低減することができ、無入力時のオフセットドリフトによる起動をなくすことができる。その結果、微小入力時の直線性を優れたものにすることができる。

4. 図面の簡単な説明

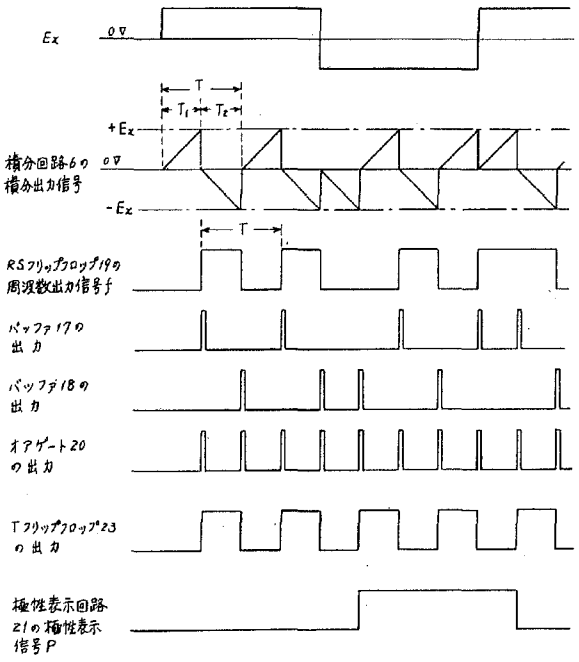
第1図は本発明の一実施例の回路図、第2図はその各部の電圧波形のタイムチャート、第3図は本発明の一実施例における極性表示回路の回路図、第4図はその各部の電圧波形のタイムチャートである。

1…入力切換回路、 2、3…切換スイッチ、6…積分回路、 8…リセットスイッチ、 10…比較回路、 13、14…基準電源、 15…第1出力端子、 16…第2出力端子、 19…RSフリップフロップ、 21…極性表示回路、 22…単一パルス発生回路、 23…Tフリップフロップ、 E_x…入力アナログ信号、$-E_x$…逆極性入力アナログ信号、 E_s…基準電圧、 f…周波数出力信号、 P…極性表示信号

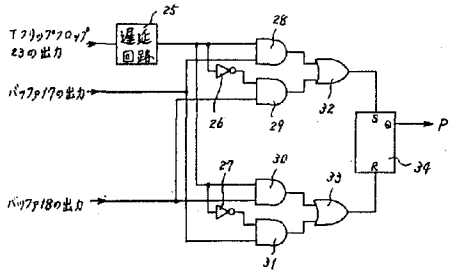
第1図



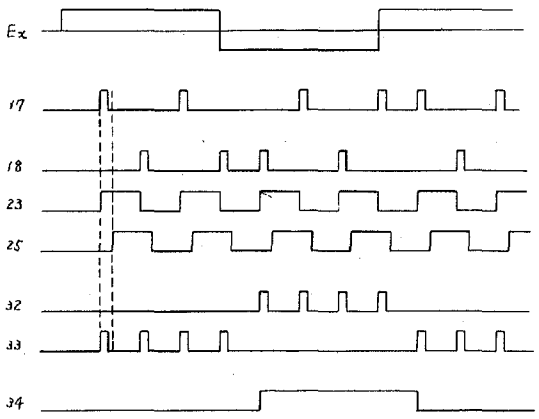
第 2 図


Ex
0V
T
T1
T2
+Ex
積分回路6の積分出力信号
0V
-Ex
T
RSフリップフロップ19の周波数出力信号f
バッファ17の出力
バッファ18の出力
オアゲート20の出力
Tフリップフロップ23の出力
極性表示回路21の極性表示信号P

第 3 図


Tフリップフロップ23の出力
遅延回路
25
28
バッファ17の出力
26
29
32
S
Q
P
R
34
27
30
33
バッファ18の出力
31

第 4 図


Ex
17
18
23
25
32
33
34

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭59—123318

⑤1Int. Cl.³	識別記号	庁内整理番号	⑬公開　昭和59年(1984)7月17日
H 03 K 13/20	101	7530—5 J	

発明の数　1
審査請求　未請求

（全 5 頁）

⑤4アナログーデイジタル変換回路

⑳特　　願　昭57—234449
㉒出　　願　昭57(1982)12月28日

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発明の名称

アナログーデイジタル変換回路

特許請求の範囲

入力電圧を積分して、その値に比例したデイジタル値に変換する積分型アナログーデイジタル変換回路において、積分回路に複数の積分抵抗、あるいは複数の積分コンデンサーにそれぞれ接続された選択切り換え手段を具備し、該入力電圧の大小に応じて、レンジ切り換えを行なうことを特徴とするアナログーデイジタル変換回路。

発明の詳細な説明

本発明は、入力信号電圧値の大小に応じたレンジ切り換え機能を有するアナログーデイジタル変換回路（以下A/D変換回路と称する。）に関するものである。

二重積分型A/D変換回路は、基本的には、積分用演算増幅器及び、積分抵抗と積分コンデンサーによる構成であり、入力アナログ信号電圧の一定時間の積分（正積分期間「T_I」と呼ぶ）を、その後、上記入力アナログ信号電圧とは逆極性の一定電圧を基準電圧源「VR」から供給し積分（逆積分期間「T_s」と呼ぶ）を順次行ない、積分回路出力電圧が一定値、すなわち積分回路の出力側に設けられた比較回路の比較電圧に達するまでの時間をカウントすることにより、入力アナログ信号電圧を、これに比例したデイジタル値に変換するものである。

従来の入力信号電圧値の大小に応じたレンジ切り換え機能を有する二重積分型A/D変換回路の一般的構成例を第1図に示す。

第1図において、1はA/D変換回路のアナログ入力端子、3は大規模集積回路の入力端子である。また、6は入力切換えアナログスイッチ群、7は基準電圧源、8は入力バッファーアンプである。10は積分器用演算増幅器14の反転入力端子(−)と入力バッファーアンプ8の出力端子9間に接続された積分抵抗であり、12は比較器用演算増幅

器１５の非反転入力端子(+)に一端が接続された積分コンデンサーである。

以上、入力バッファーアンプ、積分器用演算増幅器、比較器用演算増幅器、及び積分抵抗、積分コンデンサーによりA/D変換回路を構成している。１５は、積分回路の出力電圧と比較電圧（通常は接地電位とする）とを比較する比較器用演算増幅器で、その比較器用演算増幅器の出力は、制御論理回路１６に接続されている。

入力切換えアナログスイッチ群６は、制御論理回路１６で制御されるが、アナログスイッチ「Ｓ１」に対して、アナログスイッチ「Ｓ２」，「Ｓ３」は、外部接続された、レンジ切換えの基準抵抗２（通常では約１０メガオームが選ばれる。）とレンジ切換えの分割抵抗４（レンジ切換えの基準抵抗の１０分の１＝約１メグオーム）を選択するスイッチであり、例えば入力電圧が小さい場合（ダウンレンジと呼ぶ）には、アナログスイッチ「Ｓ１」＝ＯＮ，「Ｓ２」＝「Ｓ３」＝ＯＦＦとなり、入力電圧を直接アナログーデイジタル変換するが、入力電圧が増大すると、アナログスイッチ「Ｓ１」＝ＯＦＦ，「Ｓ２」＝「Ｓ３」＝ＯＮとなって、レンジ切換えの基準抵抗と分割抵抗とで分割された入力電圧でアナログーデイジタル変換する方式となっている（アップレンジと呼ぶ）。また、アナログスイッチ「Ｓ４」，「Ｓ５」は、積分抵抗１０の他端に、入力アナログ信号電圧と基準電圧源７とを選択するスイッチである。

第２図は、第１図の動作を示すタイミングチャートである。

まず、積分器用演算増幅器１４の出力電圧が、「Ｈ」レベルから「Ｌ」レベルになったとすると比較器用演算増幅器１５の出力は、「Ｌ」レベルから「Ｈ」レベルになり、入力切換えアナログスイッチ群１６を制御して一定時間（正積分期間「ＴＩ」）積分される。この入力積分が終了すると、入力アナログ信号とは逆極性の基準電圧が印加され、積分器用演算増幅器の出力電圧＝比較電圧となるまで積分される。この期間（逆積分期間「Ｔｓ」と呼ぶ）を計数し、デイジタル表示回路により表示する。

ところが実際には、第１図に示す様に、A/D変換回路のアナログ入力端子から、入力バッファアンプ迄の経路には、入力切換えアナログスイッチ群のオフ抵抗、大規模集積回路の静電気保護用ダイオードのオフ抵抗、及びジャンクションリーク等の微少リーク電流が存在し、入力信号の大小によってはその値は１０ピコアンペア（10×10^{-12}アンペア）以上となり、当然そのリーク電流は、アナログ入力端子を短絡してもレンジ切換え用基準抵抗を流れる為、そのレンジ切換え用基準抵抗の両端に発生する電圧は、「リーク電流」と、「レンジ切換え用基準抵抗（通常は高入力インピダンスとする為10メグオームとなる）」との積となるので（10×10^{-12}）×（10×10^{6}）〔$Volts$〕＝10^{-4}〔$Volts$〕となり、例えばこのA/D変換回路の最小分解能が１００マイクロボルト（100×10^{-6} $Volts$）の計測器であった場合には、アナログ入力端子が短絡状態でも、ゼロ点浮き上がり現象（入力電圧０でも表示値が０とならない）となってアナログーデイジタル変換表示値として現われ、計測精度に影響を与えている。上記レンジ切換えの基準抵抗及び分割抵抗をともに低減させれば、問題ないが、前記の様に実際には、アナログ入力端子からの入力インピダンスは、極端にこのレンジ切換えの分割抵抗で決定される為回路の入力インピダンスが低下してしまい、計測器として好ましくない結果となる。

本発明は、上記に述べた欠点を除去したものであり、その目的とする所は、微少リーク電流が小さく（入力切換えアナログスイッチの個数が少ない。$etc.$）かつ、微少リーク電流をほとんど無視でき、しかもレンジに無関係な高入力インピダンスのレンジ切換え機能を有するA/D変換回路を提供することにある。入力アナログ信号はレンジのアップレンジ・ダウンレンジに無関係に常に直接入力バッファーアンプに入力され、積分回路に依り、レンジ切り換えを行なうことにより、上記の目的を達成したものである。

第３図に本発明の方式を採用した、A/D変換回

路の一実施例を示す。

第3図に示すように、本発明の方式は、第1図の回路構成とは異なり、入力バッファーアンプ8の出力に、レンジ切り換え用アナログスイッチ「S8」,「S9」と、アップレンジ専用正積分抵抗20を付加したものである。その為、従来の回路におけるレンジ切り換えの為の入力切り換えアナログスイッチと、外付のレンジ切り換えの基準抵抗及びレンジ切り換えの分割抵抗は全く不要で、アナログ入力端子の微少リーク電流による影響も皆無となり、著しく計測精度の向上が計れるものである。

本方式によると、ダウンレンジにおける積分抵抗10と積分コンデンサー12に依る積分回路定数は従来の方式と何ら違いはない。ところが、入力アナログ電圧が増大し、制御論理回路22に依り、アップレンジに入った場合には、積分期間「TI」においては、アップレンジ正積分専用アナログスイッチ(「S8」)をON状態とし、そのアナログスイッチに直列接続された、アップレンジ専用正積分抵抗20で積分を行ない、逆積分期間「Ts」においては、ダウンレンジと同様のアナログスイッチ(「S9」)をON状態とし、そのアナログスイッチに直列接続された、積分抵抗10で逆積分を行ない、積分回路の利得を制御する方式としている。

第4図は、第3図に示す本発明の一実施例の動作を示すタイミングチャートである。

以上の様に、本発明の方式は、第1図のレンジ切り換えの基準抵抗、レンジ切換えの分割抵抗、レンジ切換えのアナログスイッチ(「S1」,「S2」,「S3」)の代替として、アップレンジ正積分専用アナログスイッチ(「S8」)と、アップレンジ専用正積分抵抗のみを追加したものであり、この様にすることにより、アナログ入力部の構成が非常に簡単であるが故にリーク電流が少なく、しかも高入力インピダンス高精度のレンジ切換え機能付のA/D変換回路を構成することができる効果を有するものである。

尚、上記説明では、積分抵抗にそれぞれ直列接続されたアナログスイッチによる切り換え手段としてあつかったが、本発明はそれに限らず、2系統を越えるレンジ切り換え、及び第5図,第6図に示す様な回路方式でもまったく同様な効果が得られるものである。

図面の簡単な説明

第1図は、従来のレンジ切り換え付A/D変換回路の構成例を示す図であり、第2図はそのタイミングチャートである。

第3図は、本発明によるレンジ切り換え付A/D変換回路の構成例を示す図であり、第4図はそのタイミングチャートである。第5図は本発明の第2実施例を示す回路例,第6図は本発明の第3実施例を示す回路図である。

1・・A/D変換回路のアナログ入力端子。
2・・基準抵抗
3・・大規模集積回路入力端子
4・・A/D変換回路のCOM端子
5・・分割抵抗
6・・分割抵抗接続用端子
7・・入力切換えアナログスイッチ群
8・・基準電圧源
9・・入力バッファーアンプ
10・・入力バッファーアンプ出力端子
11,25・・積分抵抗
12・・積分器入力端子
13・・積分コンデンサー
14・・比較器入力端子
15・・積分器用演算増幅器
16・・比較器用演算増幅器
17・・制御論理回路
18・・従来の大規模集積回路ブロック
19,27,30・・本発明による入力アナログスイッチ群
20・・アップレンジ用バッファーアンプ出力端子
21,28・・アップレンジ専用正積分抵抗
22・・積分器入力端子
23・・本発明による制御論理回路
24,26,29・・本発明による大規模集積回路ブロック
S1・・従来のダウンレンジ用アナログスイッ

チ群

S2,S3 ・・従来のアップレンジ用アナログスイッチ群

S4,S6 ・・入力積分用アナログスイッチ

S5,S7 ・・逆積分用アナログスイッチ

S8 ・・アップレンジ正積分専用アナログスイッチ。

S9 ・・ダウンレンジ積分・アップレンジ逆積分専用アナログスイッチ

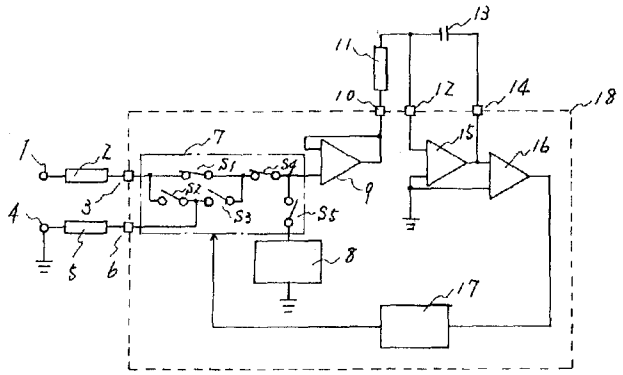
(A) ・・積分波形

(B) ・・アナログスイッチの開閉タイミング

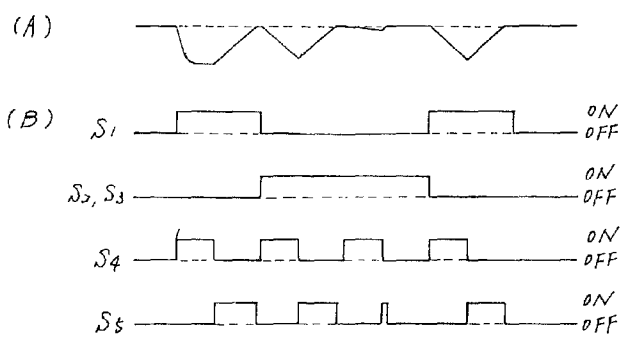
以　上

出願人　株式会社諏訪精工舎

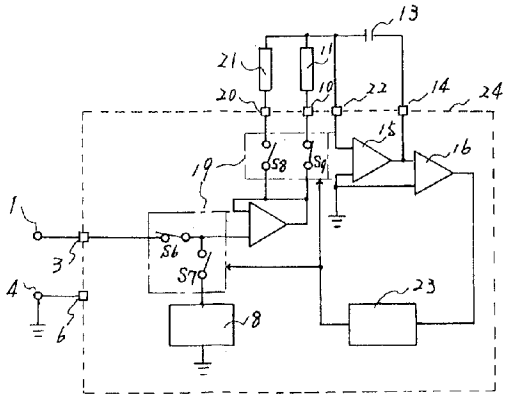
代理人　弁理士　最　上



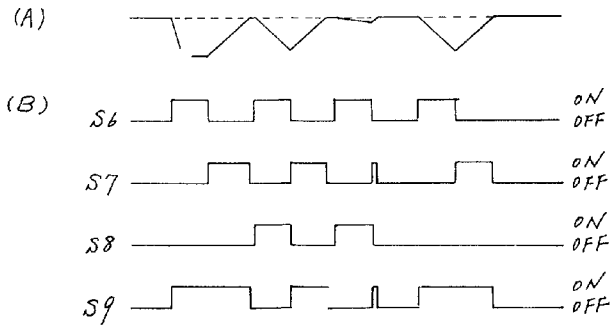
第 1 図



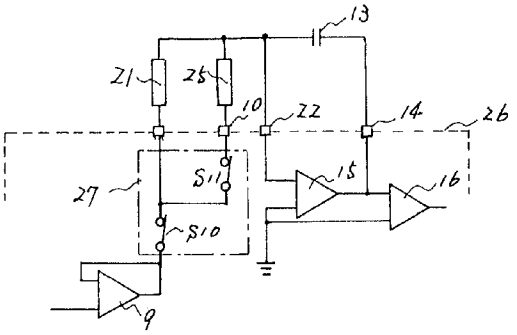
第 2 図



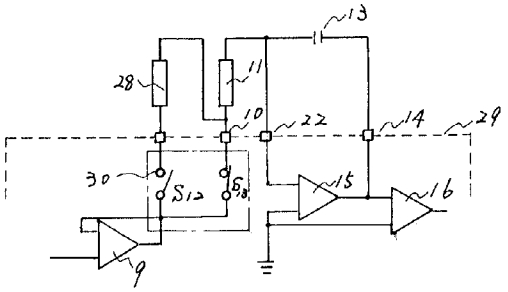
第 3 図



第 4 図



第 5 図



第 6 図

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭61－193521

⑤1Int.Cl.⁴	識別記号	庁内整理番号	㊸公開　昭和61年(1986)8月28日
H 03 M 1/52		6832－5J	

審査請求　未請求　発明の数 1　（全3頁）

㊹発明の名称　AD変換回路

㉑特　願　昭60－33807
㉒出　願　昭60(1985)2月22日

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㉔代理人　弁理士　内原　晋

明　細　書

1. 発明の名称

AD変換回路

2. 特許請求の範囲

積分器と、この積分器を構成するオペアンプの非反転入力端子に零補償期間に出力電圧を印加して零補償部を形成するMOS型スイッチとを有し単一電源で動作するデュアルスロープ型AD変換回路において、前記非反転入力端子にゲートおよびソースが接続され前記MOSスイッチと同一特性をもつMOS型トランジスタと、このMOS型トランジスタのドレインに前記オペアンプの非反転入力端子の電圧を2倍に増幅した電圧を印加する増幅回路とを備えたことを特徴とするAD変換回路。

3. 発明の詳細な説明

〔産業上の利用分野〕

本発明は単電源動作の自動ゼロ補償回路をもったデュアルスロープ型AD変換回路に関する。

〔従来の技術〕

従来、この自動ゼロ補償回路のあるデュアルスロープ型AD変換回路は、単電源動作の場合、第2図の回路図に示す構成となっている。図において1はコントロールロジック、2はカウンタおよびラッチ、A_1は抵抗R_1、コンデンサC_1と共に積分回路となるオペアンプ、A_2は基準電圧源V_sと比較するコンパレータ、A_3はインバータ、C_2は積分器の入力電圧を保持するコンデンサ、S_1～S_4はMOSスイッチである。この回路がAD変換を実施する第1ステップは自動ゼロ補償である。この自動ゼロ補償の期間では、スイッチS_1とスイッチS_4とがONとなり、抵抗R_1とコンデンサC_1とオペアンプA_1とからなる積分器およびコンパレータA_2を含むアンプ系の利得は1となる。その結果、積分器の入力オフセットV_{os}はそのまま出力に現れ、コンデンサC_2に電圧$V_{os}+V_s$として蓄えられる。

第2ステップは入力電圧V_iがあったときの積分期間T_1である。この期間T_1は、単電源動作のため入力信号として反転入力電圧$-V_i$に定電圧源V_sを重畳した信号を用い、スイッチS_1のみがONとなり、積分器の出力はコンパレータA_2の入力オフセットV_{os2}から変化を始める。この変化は正方向に直線的に一定時間T_1続く。

次の第3ステップは、比較電圧V_{REF}による積分期間T_{REF}で、スイッチS_3がONとなり、積分器出力の変化は第2ステップのときとは逆に負方向に直線的にコンパレータA_2のオフセット電圧V_{os2}まで続く。この期間T_{REF}でAD変換が行われ、1AD変換サイクル終了する。

なお、スイッチS_1, S_2, S_3, S_4のコントロールはコントロールロジック1で行われ、またAD変換結果はカウンタおよびラッチ2に蓄わえられてディジタル出力として送出される。

〔発明が解決しようとする問題点〕

この第2図の回路をバイポーラとMOSとが混在する集積回路上に実現しようとする場合、この回路の低電圧動作まで保証するにはスイッチS_1, S_2, S_3, S_4を構成するMOSスイッチのスレッショルド電圧V_Tを下げる必要が生じる。ところが、このスレッショルド電圧V_Tを、例えば、0.2～0.5v程度まで下げると、MOSトランジスタ特有のスレッショルド電圧以下でもゲート電圧に対して指数的に変化する電流が流れるというテーリング現象のため、AD変換の第2ステップ目でスイッチS_4のゲート電圧が0vになっても、コンデンサC_2に蓄積された電荷がMOSスイッチS_4を通して放電してしまう。その結果、オペアンプA_1の非反転入力電圧は時間とともに負方向に直線的に降下し、AD変換結果に誤差を生じてしまう。

今、MOSスイッチのゲート電圧0vにおける電流をI_oとすれば、次式が成立する。

$$V_i=\frac{C_1R_1}{C_2}I_o\left(\frac{T_1+T_{REF}}{T_1}\right)+\frac{V_{REF}}{T_1}\cdot T_{REF} \quad \cdots\cdots(1)$$

この式で第1項がI_oによる誤差分となる。例えば$C_1=0.1\mu F$, $R_1=50k\Omega$, $T_1=10ms$, $T_{REF}=10ms$, $C_2=0.01\mu F$, $I_o=100mA$の場合、第1項は100mvにもなって、入力電圧V_iが(V_i−100mv)でAD変換されてしまうことになるという問題点を生ずる。

本発明の目的はこのような問題点を解決し、ゼロ補償部を形成する低スレッショルド電圧を有するMOSスイッチのテーリング現象によるAD変換誤差を改善したAD変換回路を提供することにある。

〔問題点を解決するための手段〕

本発明の構成は、積分器と、積分器を構成するオペアンプの非反転入力端子に零補償期間に出力電圧を印加して零補償部を形成するMOS型スイッチとを有し単一電源で動作するデュアルスロープ型AD変換回路において、前記非反転入力端子にゲートおよびソースが接続され前記MOSスイッチと同一特性をもつMOS型トランジスタと、このMOS型トランジスタのドレインに前記オペアンプの非反転入力端子の電圧を2倍に増幅した電圧を印加する増幅回路とを備えたことを特徴とする。

〔実施例〕

次に本発明を図面により詳細に説明する。

第1図は本発明の一実施例の回路図である。本実施例は、積分器を形成するオペアンプA_1の非反転端子にN−MOSトランジスタQ_{10}のソース、ゲートを接続し、またそのドレインにはコンデンサC_2の端子電圧をオペアンプA_{10}等抵抗値の抵抗R_{10}, R_{11}からなる正相増幅器を用いて2倍にして印加する。このN−MOSトランジスタQ_{10}はN−MOSスイッチS_4と同じ製法によって同一サイズで作られたトランジスタとし、オペアンプA_1、オペアンプA_{10}はMOS入力型オペアンプである。

この回路構成により、AD変換の第2ステップでは、MOSスイッチS_4のドレイン・ソース間電圧が定電圧源V_sにほぼ等しくなっているのでMOSスイッチS_4のテーリング現象によるドレイン電流と等しい電流をN−MOSトランジスタQ_{10}により供給して、補償することができる。従って、(1)式における第1項が無視できるようになるので、AD変換を誤差なく行うことができる。

〔発明の効果〕

以上、説明したように、本発明によれば、ゼロ補償部を形成するＭＯＳスイッチ部にそれと同じサイズのＭＯＳトランジスタと２倍の正相増幅器とを付加することにより、低電圧動作及び単電源動作が可能な高精度のＡＤ変換器が得られる。

また、このＡＤ変換器をＣ－ＭＯＳ型集積回路化することは、ＭＯＳ入力型オペアンプA_{10}により容易に実現できるため、より精度の高いＡＤ変換器を得ることが可能となる。

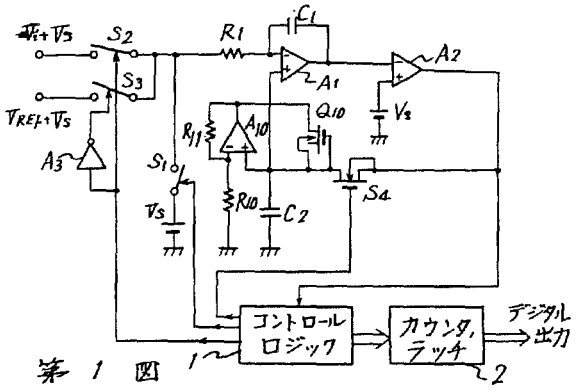
4. 図面の簡単な説明

第１図は本発明の一実施例の回路図、第２図は従来の自動ゼロ補償回路付デュアルスロープ型ＡＤ変換回路の回路図である。図において、

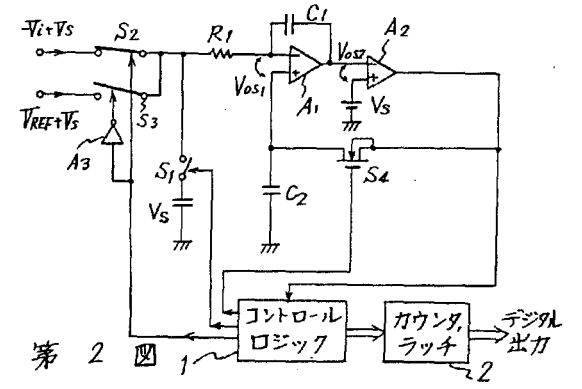
１……コントロールロジック、２……カウンタ、ラッチ、S_1，S_2，S_3，S_4……ＭＯＳスイッチ、A_1……積分器用オペアンプ、A_2……コンパレータ、A_3……インバータ、A_{10}……正相増幅器用オペアンプ、C_1……積分器用コンデンサ、C_2……入力保存コンデンサ、Q_{10}……Ｎ－ＭＯＳトランジスタ、R_1……積分器用抵抗、R_{10}，R_{11}……正相増幅用抵抗、V_s……バイアス用定電圧源、V_I……入力電圧、V_{REF}……比較電圧

である。

代理人　弁理士　内原　晋



第１図



第２図

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⑫公開特許公報（A）　昭62－47214

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H 03 M 1/52　6832－5J

審査請求　未請求　発明の数 1　（全5頁）

⑭発明の名称　デジタル・アナログ変換回路

⑳特　願　昭60－186982

㉒出　願　昭60(1985)8月26日

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明　細　書

1. 発明の名称

デジタル・アナログ変換回路

2. 特許請求の範囲

入力デジタルデータに対する演算項として少なくとも微分演算項と2次微分演算項とを有し、各演算項のデータを時分割で出力するとともに各演算項に対応する所定のパルス幅の信号を出力するデジタルフィルタ部と、

該デジタルフィルタ部より時分割で出力される上記各演算項のデータをアナログ化するデジタル・アナログ変換器と、

該デジタル・アナログ変換器より出力されるアナログ信号が供給される積分回路とを備え、

上記デジタル・アナログ変換器から順次出力される上記各演算項のデータに対応するアナログ信号を上記積分回路において積分することにより記各演算項の和に対応するアナログ信号を得るようにしたことを特徴とするデジタル・アナログ変換回路。

3. 発明の詳細な説明

〔産業上の利用分野〕

本発明は例えば自動制御系において適用可能デジタルフィルタを用いて構成したデジタル・アナログ（D／A）変換回路に関する。

〔発明の概要〕

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〔従来の技術〕

一般的に、自動制御系は第3図に示すように目標値が入力される基準入力要素40、基準入力信号とフィードバック信号との差を得る誤差検出器41、誤差信号が入力される制御要素42、該制御要素42の出力により制御される制御対象43、該制御対象43の制御量を上記誤差検出器41へフィードバックするフィードバック要素44等より構成される。

この自動制御系は上記誤差検出器41より得られる誤差信号に応じて上記制御対象43を制御し、上記誤差信号が極めて小さい状態、すなわち上記制御対象43が目標値に整した状態を得る。

このような自動制御系において、上記制御要素42に、デジタルフィルタを用いることが考えられる。

デジタルフィルタはデジタルな加算器、乗算器、単位時間遅延素子等を用いて、ハードウェアにより実現することも、マイクロコンピュータ等を用いてソフトウェアにより実現することもできるが、

いずれもアナログフィルタに比較して、安定性精度、経年変化において優れている。また、ソフトウェアにより実現した場合には、フィルタの性を決めるパラメータの変更が容易であり、種の特性のフィルタを簡単に実現できるという利がある。

上記制御要素42をこのようなデジタルフィルタを用いて実現した場合には、第5図に示すように、デジタルフィルタ50の入力側にA／D変換器51が、出力側にD／A変換器52が各々必となる。

今、デジタルフィルタで実現すべき伝達関数すなわち、微分項をAS、比例項をB、積分項をCSとすると、この伝達関数(AS＋B＋C/S)を実する場合、例えば上記微分項、比例項、積分項独立に計算した後で加算する方法が考えられるすなわち、第6図に示すようにA入力データをA/D変換器60でデジタル化した後、微分回路61、積分回路62、乗算器64に供給する。上記微回路61の出力は乗算器63によりA倍され加

器66にはASの項が入力される。また、上記積分回路62の出力は乗算器65によりC倍され上記加算器66にC／Sの項が入力される。また、上記乗算器64よりBの項が上記加算回路66に入力される。結局、該加算回路66からは(AS＋B＋C／S)がD／A変換器67に供給され、アナログ信号が得られる。

このような構成において精度を上げるためには上記D／A変換器67の分解能を上げること、すなわちビット数を多くとることが要求される。

〔発明が解決しようとする問題点〕

上述したように、デジタルフィルタで精度を上げるためには高分解能のD／A変換器が必要にな

であり、簡単な構成でデジタルフィルタを用い高精度のD／A変換回路を実現し、デジタルフィルタの適用を容易にすることを目的とする。

〔問題点を解決するための手段〕

上述の問題を解決するために本発明では、入デジタルデータに対する演算項として少なくと微分演算項と2次微分演算項とを有し、各演算のデータを時分割で出力するとともに、各演算に対応する所定のパルス幅の信号を出力するデタルフィルタ部と、該デジタルフィルタ部より分割で出力される上記各演算項のデータをアナグ化するD／A変換器と、該D／A変換器よりナログ信号が供給され、上記デジタルフィルタ

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〔作　用〕

本発明に係るD／A変換回路では、入力デジタルデータに対して上記デジタルフィルタ部において微分演算と2次微分演算が行なわれ、各演算の結果のデータが時分割で上記D／A変換器に出力される。該D／A変換器により得られた各演算の結果のデータに対応するアナログ信号は上記デジタルフィルタ部より出力される所定のパルス幅の信号のパルス幅の期間、上記積分回路において順次積分され上記各演算項の和に対応したアナログ信号が出力される。

〔実施例〕

以下、本発明をVTR（Video Tape Recoder）のドラムサーボ系に適用した場合の一実施例について図面を参照して説明する。

第1図は本実施例の構成を示すブロック図であり、前述した自動制御系に対応させると制御対象はドラムモータ4であり、フィードバック要素は積分器5であり、制御要素はA／D変換器2及び

D／A変換部3である。該D／A変換部3は周

数特性を有する。

このドラムサーボ系では、上記ドラムモータが基準位相 θ_{ref} で回転するような制御が行なれる。すなわち、上記ドラムモータ4の角速度から上記積分器5によりドラム位相θが得られ該ドラム位相θと基準位相 θ_{ref} との差が誤差出器1で検出される。ここで得られた誤差信号θは上記A／D変換器2を介して上記D／A変部3に供給される。

該D／A変換部3はデジタルフィルタ部3a、D／A変換器3e、スイッチ3b、積分回路3等より構成され、上記デジタルフィルタ部3a及び積分回路3dにより定まる周波数特性によりジタル化された誤差信号Δθに応じた上記ドラモータ4の駆動電圧emを出力する。この結果該ドラムモータ4はドラム位相θが上記基準位 θ_{ref} と一致した状態で回転する状態に安定化れる。

次に、上記D／A変換部3について詳細に説

する。まず、上記デジタルフィルタ部3aでは、（AS^2+BS+C）で表わされる伝達関数の各項を別々に計算して計算結果のデータを時分割で上記D／A変換器3eに出力するとともに、各項の出力に対応してΔTのパルス幅を有する制御信号（H／L）を上記スイッチ3bに供給する。上記D／A変換器3eより出力されるアナログ信号は上記ΔTの期間、該スイッチ3bを介して抵抗R、コンデンサC、オペアンプ3cから成る上記積分回路3dに供給される。

該積分回路3dは上記抵抗R、コンデンサC、上記時間幅ΔTでその利得が定まり、上記ΔTの時間、入力信号を積分し、上記スイッチ3bがオフになる期間は積分した値を保持する。従って、

記デジタルフィルタ部3aの伝達関数（AS^2+ $B+C$）と上記K／Sとの積となる。すなわち

$$(AS^2+BS+C)\times\frac{K}{S}=(AS+B+\frac{C}{S})K$$

が該D/A変換部3の実現する伝達関数であり、これによって周波数特性が定まる。

以上の動作を上記伝達関数のうち、C項、B項、AS^2項の順に処理した場合を第2図に従って説明する。

まず、同図aに示すように時間ΔT₁において上記C項の演算がなされ、上記積分回路3dよりC・K／Sに対応する電圧の信号が出力される。次に同図bに示すように時間ΔT₂において上記B項の演算がなされ、上記積分回路3dの出力は

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で、各項の演算が簡単になり、また、上記D／A変換器3cのビット数は例えば上記A／D変換器2のビット数より少なくてもよく、低分解能のD／A変換器を用いても精度等を維持することが可能になる。

また上記伝達関数（AS^2+BS+C）のA，B，Cは定数であるから、上記制御信号のパルス幅ΔTを可変にすることにより上記積分回路3dの利得を可変にして上記A，B，Cの定数を実現するようにしてもよい。次に、このように処理を行なった場合を第3図に従って説明する。

まず、同図aに示すように時間ΔT_1において上記デジタルフィルタ部3aでは入力データに対して演算処理を行なわず、上記制御信号（H／L）のパルス幅をC・ΔTに設定して出力する。これにより上記積分回路3dよりC・K／Sに対応する電圧が出力される。次に、同図bに示すように時間ΔT_2において上記デジタルフィルタ部3aではS項の演算がなされ、演算結果のデータが出力されるとともに上記制御信号（H／L）のパルス

幅がB・ΔTに設定され出力される。これにより上記積分回路3dより（BS＋C）・K／Sに応する電圧が出力される。最後に同図cに示すように時間ΔT_3において上記デジタルフィルタ3ではS²項の演算がなされ、演算結果のデータが力されるとともに、上記制御信号（H／L）のルス幅がA・ΔTに設定され出力される。これより上記積分回路3dの出力は（AS^2+BS+・K／Sに対応した電圧となり周期Tの間保持れる。

このように上記制御信号（H／L）のパルスを可変にして上記A，B，Cの定数を実現するで上記デジタルフィルタ部3aでの演算が減少演算が簡単になる。また、各演算項ごとに分けデータを出力するので上記D／A変換器3cのット数は少なくても精度等を維持することができる。

また、上記積分回路3dは、高域利得が極端大きいので上記ドラムモータ4のバラツキを吸収することができる。

〔発明の効果〕

以上述べたように本発明によれば、簡潔な構成でデジタルフィルタを用いた高精度のD／A変換回路を実現することができ、デジタルフィルタの適用が容易になる。

また、実施例で示したように本発明をVTRのドラムサーボ系に適用した場合、積分回路によりドラムモータのバラツキを吸収することができる。

4. 図面の簡単な説明

第1図は本発明に係るD／A変換回路をVTRのドラムサーボ系に適用した本実施例の概略を示すブロック図である。

第2図は上記D／A変換回路において、パルス

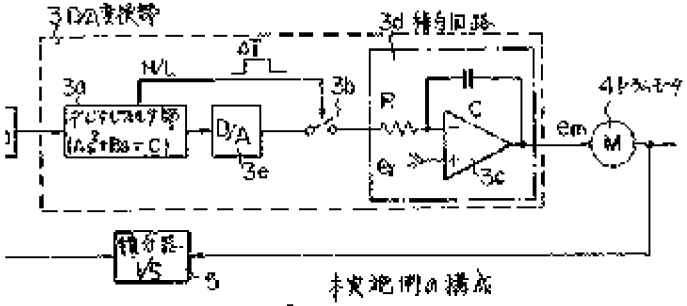
化デジタルフィルタを用いた場合の説明図であ

第6図は伝達関数（$AS+B+\frac{C}{S}$）を実現すデジタルフィルタの従来の構成の一例を示すブック図である。

1 …… 誤差検出器
2 …… A／D変換器
3 …… D／A変換部
3a …… デジタルフィルタ部
3b …… スイッチ
3c …… オペアンプ
3d …… 積分回路
3e …… D／A変換器
4 …… ドラムモータ
5 …… 積分器

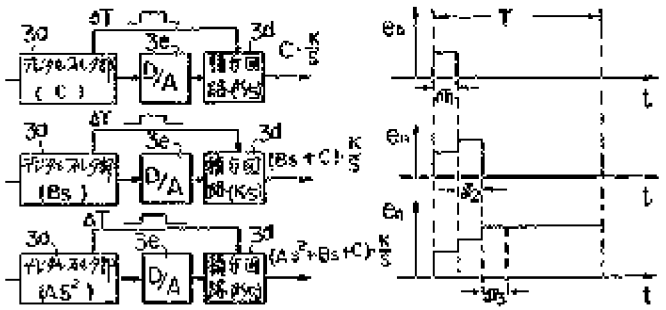
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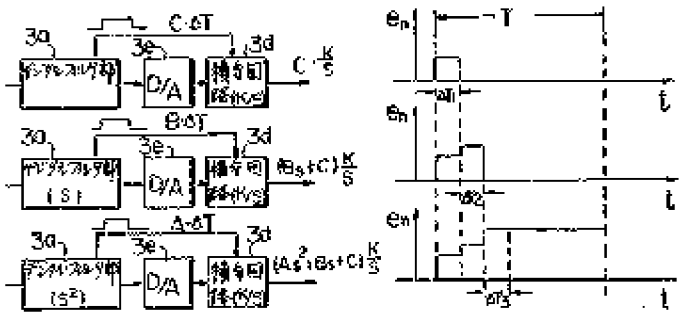
本実施例の構成

第1図



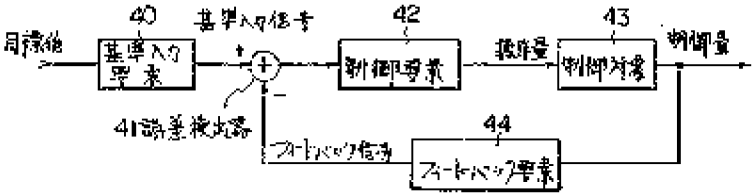
D/A 変換の動作

第2図



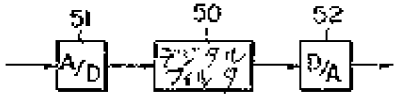
D/A 変換の動作

第3図



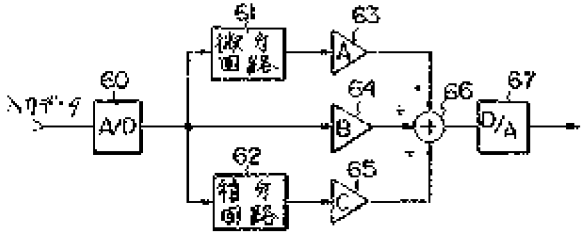
自動制御系の構成

第4図



デジタルフィルタからなる制御要素

第5図



$As+B+\frac{C}{s}$ を実現する構成例

第6図

9/5/2007

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭63－274214

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H 03 M 1/08　B－6832－5J

審査請求　有　発明の数 1 （全3頁）

⑤4発明の名称　ディジタル・アナログ変換回路

⑳特　願　昭62－108561
㉒出　願　昭62(1987)5月1日

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⑦4代 理 人　弁理士 大 塚　学　外1名

明　細　書

1．発明の名称

ディジタル・アナログ変換回路

2．特許請求の範囲

ディジタル出力信号とその1標本周期遅延したディジタル信号との減算回路と、その出力のディジタル・アナログ変換回路と、その変換出力を標本周期の間だけ積分する回路と、その積分開始直前の積分値との加算回路を備えたことを特徴とするディジタル・アナログ変換回路。

3．発明の詳細な説明

（発明の属する技術分野）

本発明はＤＡ変換回路特にその折り返し雑音の低減に関するものである。

（従来技術）

第2図(a)は従来のディジタル・アナログ変換回路例の系統図で、(7)はディジタル信号処理部、(8)はＤＡ変換回路、(9)は低域沪波回路である。第2図(b)は第2図(a)における信号処理部(7)の出力ＡとＤＡ変換回路(8)の出力Ｂと低域沪波器(9)の出力Ｃの波形をそれぞれ示すタイムチャートである。また第2図(c)はＤＡ変換器出力の出力スペクトラムを示す。

しかし従来のディジタル・アナログ変換においては、折り返し雑音と呼ばれる不要信号成分が、第2図(c)に示すように標本周波数 f_s の整数倍の周波数を中心として斜線部 b_1, b_2 のように発生する。そこで第2図(c)の点線(c)で示すような特性を持つ低域沪波器が必要となる。ところが標本化周波数が信号のもつ上限の周波数 f_u に近付くと、(ただし標本化定理から $f_s \geq 2f_u$ の条件が成立する必要があるが) 低域沪波器としては第2図(c)の点線(c)で示すような急峻な特性のものが必要となる。即ちＤＡ変換後の信号は階段状のアナログ信号であり、これは零次ホールド波形と呼ばれるもので、その折返し雑音の大きさは希望信号に比べ－13dBの大きさである。従って、その設計製作が

困難であるばかりではなく、素子数も多くなり、また安定性に欠ける嫌いがある。

（発明の目的）

本発明は上述のような従来技術の欠点に鑑みてなされたもので、第2図で示した従来の回路におけるDA変換器とこれに続くLPFの代わりに、DA変換を行なう前に前処理を行なう回路および、DA変換後に積分回路と累積加算回路とを追加することによって、線形補間を行った波形を得て、LPFに要求される特性を緩やかなものにすることが出来るディジタル・アナログ変換回路を得ることを目的とするものである。即ち線形補間を行った波形のアナログ出力では、その折り返し雑音の大きさは希望信号に比べ−26.5dBで、これは前述の階段状の零次ホールド波形に比べ約¼である。以下実施例によって本発明を詳細に説明する。

（発明の構成と作用）

第1図(a)は本発明の一実施例回路の系統図で、ディジタル信号処理された信号Aは（第1図bの出力波形図A参照）1標本周期の遅延素子(T)と減算回路(2)とよりなる前処理回路のそれぞれに入力され、その遅延信号B（第1図(b)のB参照）とA信号との減算出力信号Cは第1図(b)のCで示される。今入力信号AをX_iとすると信号BはX_{i-1}で表わされる。ただしiは標本番号を示す添字である。従って、信号CをΔX_iとするとこれは$\Delta X_i = X_i - X_{i-1}$で表わされる。そしてこの信号CはDA変換回路(3)でアナログ信号Dに変換される（第1図(b)のD参照）。このアナログ信号Dは階段波であるが、これをR_1, C_1およびスイッチS_1と増幅器とから成る積分回路(4)で積分する。スイッチS_1は積分器が1標本分DA変換器出力Dを積分したときにC_1に蓄積された電荷を放電し、積分器が常に零から積分を行なうようにするためのもので、その制御はパルス列H（第1図(b)H参照）で行われ、パルス列(H)のパルス幅は標本周期に比して充分狭いものである。この積分出力Eは第1図(b)のEに示すように3角波であり、これは加算器(5)で前の標本点までの1周期間の加算された積分値の標本化信号Gと加算され、出力信号F（第1図(b)F参照）即ち線形補間を行った出力となる。標本化保持(SH)回路(6)は1標本周期の積分が終わった時点での出力(F)を標本し、次の1標本周期の間だけ保持するもので、その制御パルスは前記の(H)と同じである。即ちSH回路(6)の出力信号(G)は階段波（第1図(b)のG参照）である。そしてこの出力信号Fのスペクトラムは第1図(C)のようになり、希望のスペクトラムaと折り返し雑音b_1, b_2が標本周波数f_s, $2f_s$の周囲に現れるが、これらは先に述べた従来のもの即ち第2図(C)に示したものに比して低減されていることは前述の信号理論の通りであり、従って沪波器LPFの特性(C)は従来に比し緩やかでよいので、沪波器は素子数の少ない簡単安価なものでよい。

（発明の効果）

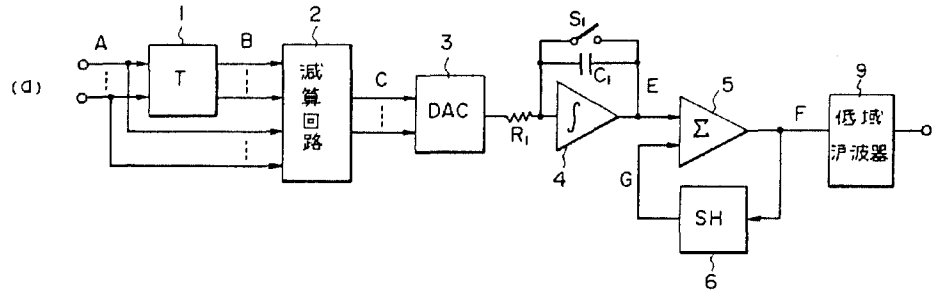
以上の説明から明らかなように、本発明によるときは標本出力を線形補間した出力を得ることが出来るので、折り返し雑音が低減し、雑音除去用の沪波器が簡単安価なものですみ、実用上の効果大なるものがある。

4．図面の簡単な説明

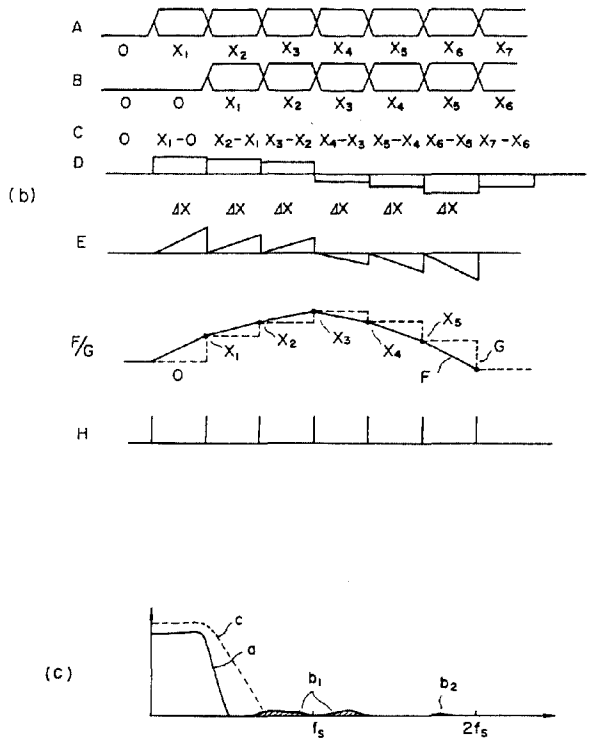
第1図(a), (b), (c)は本発明の一実施例回路の系統図、回路各部の出力波形図および出力信号のスペクトラム図、第2図(a), (b), (c)は従来回路の系統図、回路各部の出力波形図、および出力信号のスペクトラム図である。

(1)…遅延素子、 (2)…減算回路、 (3), (8)…ディジタル変換回路(DAC)、 (4)…積分回路、 (5)…加算回路Σ、 (6)…標本化保持SH回路、 (7)…ディジタル信号処理部、 9…低域沪波器、 (a)…希望スペクトラム、 (b_1)(b_2)…折り返し雑音、 c…沪波器の特性、 (f_s)…標本化周波数、 A…ディジタル入力信号、 B…Aの遅延信号、 C…減算回路出力信号、 D…ディジタル・アナログ変換回路出力信号、 E…積分回路出力信号、 F…加算回路の出力信号、 G…標本化保持回路の出力信号。

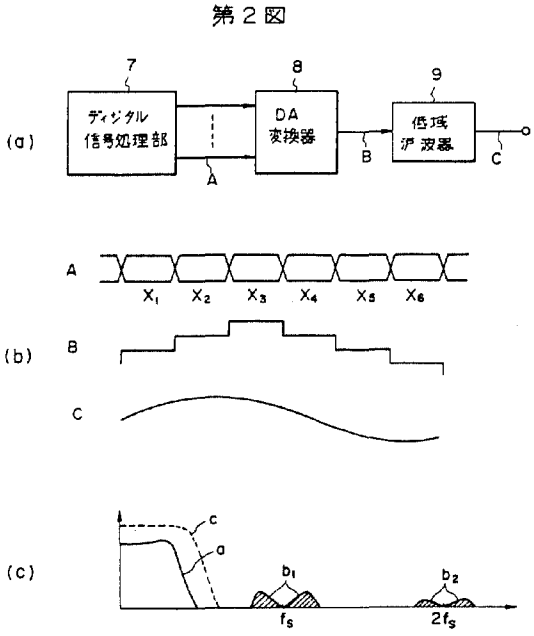
第1図


(a)
A
B
C
D
E
F
G
T
減算回路
DAC
SH
低域沪波器
Σ
S_1
C_1
R_1
1
2
3
4
5
6
9

第1図


(b)
A
B
C
D
E
F/G
H
0
X_1
X_2
X_3
X_4
X_5
X_6
X_7
X_1-0
X_2-X_1
X_3-X_2
X_4-X_3
X_5-X_4
X_6-X_5
X_7-X_6
ΔX
G
F
(c)
c
a
b_1
b_2
f_s
$2f_s$

第2図


(a)
ディジタル信号処理部
DA変換器
低域沪波器
7
8
9
A
B
C
(b)
A
B
C
X_1
X_2
X_3
X_4
X_5
X_6
(c)
c
a
b_1
b_2
f_s
$2f_s$

Electronic Acknowledgement Receipt

EFS ID:	2498954
Application Number:	10973917
International Application Number:	
Confirmation Number:	3273
Title of Invention:	Universal platform module and methods and apparatuses relating thereto enabled by universal frequency translation technology
First Named Inventor/Applicant Name:	David F. Sorrells
Customer Number:	26111
Filer:	Michael Q. Lee/Jason Geider
Filer Authorized By:	Michael Q. Lee
Attorney Docket Number:	1744.0330003
Receipt Date:	21-NOV-2007
Filing Date:	27-OCT-2004
Time Stamp:	13:52:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		17440330003IDSfiling.pdf	513380 80f1855fff154964a9f340867f350e0db521483d	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Information Disclosure Statement Letter	1	2
	Information Disclosure Statement Letter	3	10
	Information Disclosure Statement (IDS) Filed	11	13

Warnings:					
Information:					
2	Foreign Reference	FP1.PDF	304192 2427fdb59906c6ec5e7a9358f41c9ee97fe40766	no	6
Warnings:					
Information:					
3	Foreign Reference	FP2.PDF	255993 a9a9da260dada22d14be6baf663552739367efb6	no	4
Warnings:					
Information:					
4	Foreign Reference	FP3.PDF	378550 98ea96c24fb9016c031c6039658cf0856fe1400e	no	7
Warnings:					
Information:					
5	Foreign Reference	FP4.PDF	409572 b3a75c97adca0fbb4c672eea72c1152e888dc0ff	no	7
Warnings:					
Information:					
6	Foreign Reference	FP5.PDF	242924 99f2fa1e1ebf78ec90cab12b723804e919e44ea8	no	5
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Information:					
7	Foreign Reference	FP6.PDF	161812 b959f1e294764fb5b4d8d30d05b73997ba993eed	no	3
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Information:					
8	Foreign Reference	FP7.PDF	155265 25594d08d288808893c13078ffb050b0fd77c7e5	no	5
Warnings:					

Information:					
9	Foreign Reference	FP8.PDF	168437 df81b4319d1e227c6e39abb147d3c38329a69033	no	3
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10	NPL Documents	NPL1.PDF	36207 d61a4f7e5e15f56c4e9a70a0517f38b277322b1f	no	1
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11	NPL Documents	NPL2.PDF	42892 b1e897dd5111d379bfa8379f5b11d4cc9b8e1559	no	1
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Information:					
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Information:					
16	NPL Documents	NPL7.PDF	29727 6341c0d9c2a6cd2a9c5ae0b177a3966e4a7b6a70	no	1
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Information:					
17	NPL Documents	NPL8.PDF	39066 04430157983d2454672fd09e7ce15e37f7bdb8b8	no	1
Warnings:					

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,917	10/27/2004	David F. Sorrells	1744.0330003	3273

26111 7590 03/26/2008

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
TRINH, SONNY	
ART UNIT	PAPER NUMBER
2618	

MAIL DATE	DELIVERY MODE
03/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/973,917	SORRELLS ET AL.	
	Examiner	Art Unit	
	Sonny TRINH	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 119e as follows:

The later-filed application must be an application for a patent for an invention which is also disclosed in the prior application (the parent or original nonprovisional application or provisional application). The disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the requirements of the first paragraph of 35 U.S.C. 112. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994).

The disclosure of the prior-filed application, Application No. 09/261129, fails to provide adequate support or enablement in the manner provided by the first paragraph of 35 U.S.C. 112 for one or more claims of this application. The plurality of transceivers that operate in different protocol/standard were not disclosed, accordingly, claims 5-22 are not entitled to the benefit of the prior application (09/261129 filed 03/03/99).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 5-10, 12-19, 21-22** are rejected under 35 U.S.C. 102(e) as being anticipated by Zehavi (U.S. Patent Number 6,894,988).

Regarding **claim 5**, with reference to figures 1, 3, 5, Zehavi discloses an apparatus capable of performing simultaneous multi-platform operations (column 1 line 52 to column 2 line 5, column 2 line 65 to column 3 line 14), comprising: at least one multi-platform module (figure 1 element 100) including a plurality of transceivers (figure 1, transceiver 102a, 102b) each having at least one frequency translating module (inherent since each transceiver capable of communicate at different protocol/standard and they must communicate with the wireless device 100); and a control module for enabling the at least one multi-platform module to communicate with at least one of a plurality of communication links (figure 5, state machine 500), the control module including a plurality of protocol/standard sub-modules (figure 5, control managers 106a, 106b); wherein a first protocol/standard sub-module operates a first transceiver in conformance with a first protocol/standard combination and wherein a second protocol/standard sub-module simultaneously operates a second transceiver in conformance with a second protocol/standard combination (column 2 line 65 to column 4 line 26).

Regarding **claim 6**, since Zehavi discloses that the state machine of figure 1 controls the communication links of both transceiver 102a and 102b at the same time (column 3 lines 1-14), it is obvious that the control module enables the at least one

multi-platform module to simultaneously communicate with a quantity of the plurality of communication links by employing an equal quantity of the plurality of standard/protocol sub-modules.

Regarding **claim 7**, Zehavi further discloses that the multi-platform module includes a plurality of receivers (figures 1-2, transceiver 102a, 102b) and a plurality of transmitters (figures 1-2, transceiver 102a, 102b) each having at least one frequency translating module (inherent since each transceiver capable of communicate at different protocol/standard and they must communicate with the wireless device 100).

Regarding **claim 8**, Zehavi further discloses that the first protocol/standard combination is different from the second protocol/standard combination (abstract, column 1 line 52 to column 2 line 5).

Regarding **claim 9**, since the wireless device can operate in different standard/protocol such as 802.11, BlueTooth etc. (column1 line 53 to column 2 line 5), it is inherent that the control manager (figure 1, 106a, 106b) contain operational instructions for the at least one multi-platform sub-module so that transceivers 102a and 102b can communicate with other using different protocol/standard.

Regarding **claim 10**, since the wireless device can operate in different standard/protocol such as 802.11, BlueTooth etc. (column1 line 53 to column 2 line 5), it is inherent that the operational instructions include respective first and second protocol stacks and specification information about the first and second protocol architectures.

Regarding **claims 12-13**, since the wireless device can operate in different standard/protocol such as 802.11, BlueTooth etc. (column1 line 53 to column 2 line 5), it

is inherent that the first and second transceivers are in conformance with respective requirements of the first and second protocols and operating environments/standards.

Regarding **claims 14-19, 21-22**, these claims merely reflect the method claim as opposed to the apparatus claims of claims 5-10, 12-13 (respectively) and are therefore rejected for the same reasons.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 11, 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zehavi.

Regarding claim 11, Zehavi discloses the invention but does not disclose that the first and second implementation and operational instructions can be updated, upgraded, replaced, or modified to provide the at least one multi-platform sub-module with additional functionality. However, it would have been obvious and well within the level of a person of ordinary skill in the art to do so, the motivation for updating, upgrading, replacing or modifying is to make sure that the system will be compatible with new standard / protocol if such requirement arise.

Regarding **claim 20**, this claim merely reflects the method claim as opposed to the apparatus claim of claim 11 and is therefore rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sonny TRINH whose telephone number is 571-272-7927. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward URBAN can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sonny TRINH/
Primary Examiner, Art Unit 2618
3/28/08

Notice of References Cited	Application/Control No. 10/973,917	Applicant(s)/Patent Under Reexamination SORRELLS ET AL.	
	Examiner Sonny TRINH	Art Unit 2618	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,894,988	05-2005	Zehavi, Ephraim	370/278
*	B	US-7,193,965	03-2007	Nevo et al.	370/230
*	C	US-6,088,348	07-2000	Bell et al.	370/343
*	D	US-6,198,941	03-2001	Aho et al.	455/552.1
*	E	US-6,072,996	06-2000	Smith, James P.	455/189.1
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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CONFIRMATION NO. 3273

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/973,917	10/27/2004	370	2618	1744.0330003

APPLICANTS

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Robert W. Cook, Switzerland, FL;
Richard C. Looke, Jacksonville, FL;
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**** CONTINUING DATA ***************************

This application is a CON of 09/569,044 05/10/2000 PAT 6,873,836
which is a CIP of 09/261,129 03/03/1999 PAT 6,370,371
and is a CIP of 09/514,004 02/25/2000 ABN
and is a CIP of 09/476,093 01/03/2000 PAT 7,006,805
and is a CIP of 09/476,330 01/03/2000 PAT 6,704,549
and is a CIP of 09/525,615 03/14/2000 PAT 6,853,690
and is a CIP of 09/526,041 03/14/2000 PAT 6,879,817
and claims benefit of 60/195,328 04/10/2000
and claims benefit of 60/147,129 08/04/1999

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

12/07/2004

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /SONNY TRINH/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		FL	92	18	2

ADDRESS

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005
UNITED STATES

TITLE

Universal platform module and methods and apparatuses relating thereto enabled by universal frequency translation technology

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Sheet 1 of 2

Complete if Known	
Application Number	10/973,917
Filing Date	October 27, 2004
First Named Inventor	David F. Sorrells
Art Unit	2618
Examiner Name	Trinh, Sonny
Attorney Docket Number	1744.0330003

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	5,884,154	03-16-1999	Sano *et al.*	
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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP1	JP 58-031622	02-24-1983	Usui *et al.*		
	FP2	JP 61-245749	11-01-1986	Ito		
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	FP8	JP 63-274214	11-11-1988	Miyake		
	FP9					

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Sheet 2 of 2

Complete if Known	
Application Number	10/973,917
Filing Date	October 27, 2004
First Named Inventor	David F. Sorrells
Art Unit	2618
Examiner Name	Trinh, Sonny
Attorney Docket Number	1744.0330003

U.S. PATENT DOCUMENTS

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	FP10					
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	FP12					
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Art Unit	2618
Examiner Name	Trinh, Sonny
Attorney Docket Number	1744.0330003

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume issue number(s), publisher, city and/or country where published	T[2]
	NPL1	English-language Abstract of Japanese Patent Publication No. JP 58-031622, data supplied by ep.espacenet.com, 1 page (Feb. 24, 1983 - Date of publication of application).	
	NPL2	English-language Abstract of Japanese Patent Publication No. JP 61-245749, data supplied by ep.espacenet.com, 1 page (Nov. 1, 1986 - Date of publication of application).	
	NPL3	English-language Abstract of Japanese Patent Publication No. JP 64-048557, data supplied by ep.espacenet.com, 1 page (Feb. 23, 1989 - Date of publication of application).	
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	NPL5	English-language Abstract of Japanese Patent Publication No. JP 59-123318, data supplied by ep.espacenet.com, 1 page (July 17, 1984 - Date of publication of application).	
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	NPL9		
	NPL10		

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IP-W

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+Admitted only in Virginia
•Practice Limited to Federal Agencies

March 28, 2006

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2616

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Second Supplemental Information Disclosure Statement;

2. A listing of the cited documents on Form PTO-1449 (*4 pages*);

3. Copies of the cited documents (AJ24-AM24, AJ25-AL25, AO60-AR60, AN61-AP61); and

4. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL:apg
Enclosures

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THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2616
Appl. No.: 10/973,917	Examiner: Chin, Wellington
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Second Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Second Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Supplemental Information Disclosure Statement filed on October 24, 2005 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

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Applicants provide the following comments regarding the documents:

Document AJ24 was cited in a search report in related European Patent Application No. 04020115.4, filed October 6, 2000, entitled "Down Converter Using Subsampling," directed to related subject matter. Also cited in said search report were U.S. Patent Nos. 5,454,007; 5,705,949; and 5,883,548, PCT Publication Nos. WO 94/05087 and WO 98/40968, German Patent Nos. DE 35 41 031 A and DE 197 35 798 C, and Fest, Jean-Pierre, "Le Convertisseur A/N Revolutionne Le Recepteur Radio," Electronique, JMJ (Publisher), No. 54, pp. 40-42 (December 1995), which have already been cited in the present application.

Documents AK24 and AE71 were cited in an Office Action in related European Patent Application No. 01977965.1, filed May 16, 2001, entitled "Apparatus, System, and Method for Down converting and Up converting Electromagnetic Signals," directed to related subject matter. Also cited in said search report were U.S. Patent Nos. 5,564,097 and 5,640,698; PCT Publication No. WO 96/02977; and Rudell, J.C. *et al.*, "A 1.9-Ghz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," IEEE Journal of Solid-State Circuits, IEEE, Vol. 32, No. 12, pp. 2071-2088 (December 1997), which have already been cited in the present application.

Documents AL24, AM24, AJ25-AL25, and AF71 were cited in an Office Action in related Israel Patent Application No. 142,699, filed October 18, 1999, entitled "Method and System for Frequency Up-Conversion,", directed to related subject matter. Also cited in said Office Action was European Patent Publication No. EP 0 548 542, which has already been cited in the present application.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Documents AO60 and AD71 were cited in an Office Action in related U.S. Patent Application No. 10/197,253, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter.

Documents AE69-AI69 were cited in an Office Action in related U.S. Patent Application No. 10/197,255, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,850,742, which has already been cited in the present application.

Documents AA70, AA71, and AG71-AI71 are co-owned patents which are directed to related subject matter.

Documents AB70 and AC70 were cited in an Office Action in related U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Methods And Apparatuses Relating To A Universal Platform Module And Enabled By Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,844,868, which has already been cited in the present application.

Documents AD70-AI70 were cited in a Notice of Allowance in related U.S. Patent Application No. 10/961,272, filed October 12, 2004, entitled "Apparatus, System, And Method For Down-Converting And Up-Converting Electromagnetic Signals," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,853,690, which has already been cited in the present application.

Documents AB71 and AC71 were cited in an Office Action in related U.S. Patent Application No. 09/550,644, filed April 14, 2000, entitled "Method And System For Down-

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Converting An Electromagnetic Signal, Transforms For Same, And Aperture Relationships," directed to related subject matter.

Documents AA72 and AB72 were cited in an Office Action in related U.S. Patent Application No. 10/394,069, filed March 24, 2003, entitled "Method and Circuit for Down-Converting a Signal," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,836,650, which has already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final

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Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document AK24 (DE 1936252) appears to describe a modulator or demodulator in integrated technology. An English language translation of document AK24 is enclosed as document AP60.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Document AL24 (JP 62-12381) appears to describe a pulse-width modulation control system of an inverter. An English language abstract of document AL24 is enclosed as document AQ60.

Document AM24 (JP 4-154227) appears to describe a relay monitoring device for broadcasting radio waves. An English language abstract of document AM24 is enclosed as document AR60.

Document AJ25 (JP 6-284038) appears to describe a transceiver. An English language abstract of document AJ25 is enclosed as document AN61.

Document AK25 (JP 10-96778) appears to describe a distance measuring device. An English language abstract of document AK25 is enclosed as document AO61.

Document AL25 (JP 11-98205) appears to describe a demodulator for digital radio communication. An English language abstract of document AL25 is enclosed as document AP61.

☒ 7. Copies of documents AJ24-AM24, AJ25-AL25, AO60-AR60, and AN61-AP61 are enclosed. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent publications cited on the attached Form PTO-1449 are not enclosed.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000, 09/476,093, filed January 3, 2000, 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 3/28/06

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Washington, D.C. 20005-3934
(202) 371-2600

511368_1.DOC

Atty. Docket: 1744.0330003

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

OIPE IAP13 MAR 28 2006 PATENT & TRADEMARK OFFICE

FORM PTO-1449

SECOND SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE69	5,703,584	12/1997	Hill			
	AF69	5,887,001	03/1999	Russell			
	AG69	6,298,065 B1	10/2001	Dombkowski *et al.*			
	AH69	2002/0080728 A1	06/2002	Sugar *et al.*			
	AI69	2002/0163921 A1	11/2002	Ethridge *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ24	WO 98/53556 A2	11/1998	PCT			N/A
	AK24	DT 1936252	01/1971	DT			Yes (Doc. AP60)
	AL24	JP 62-12381	01/1987	JP			No
	AM24	JP 4-154227	05/1992	JP			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO60	Gaudiosi, J., "Retailers will bundle Microsoft's Xbox with games and peripherals," *Video Store Magazine*, Volume 23, Issue 36, pg. 8, 2 pages (September 2-8, 2001).
	AP60	English-language Translation of German Patent Publication No. DT 1936252, translation provided by Transperfect Translations, 12 pages (January 28, 1971 - Date of publication of application).
	AQ60	English-language Abstract of Japanese Patent Publication No. JP 62-12381, data supplied by the espacenet, 1 page (January 21, 1987 - Date of publication of application).
	AR60	English-language Abstract of Japanese Patent Publication No. JP 4-154227, data supplied by the espacenet, 1 page (May 27, 1992 - Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

511357_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA70	6,963,734 B2	11/2005	Sorrells *et al.*			
	AB70	6,005,506	12/1999	Bazarjani *et al.*			
	AC70	6,438,366 B1	08/2002	Lindfors *et al.*			
	AD70	5,196,806	03/1993	Ichihara			
	AE70	5,410,195	04/1995	Ichihara			
	AF70	6,404,823 B1	06/2002	Grange *et al.*			
	AG70	6,618,579 B1	09/2003	Smith *et al.*			
	AH70	2001/0015673 A1	08/2001	Yamashita *et al.*			
	AI70	2003/0045263 A1	03/2003	Wakayama *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ25	JP 6-284038	10/1994	JP			No
	AK25	JP 10-96778	04/1998	JP			No
	AL25	JP 11-98205	04/1999	JP			No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN61	English-language Abstract of Japanese Patent Publication No. JP 6-284038, data supplied by the espacenet, 1 page (October 7, 1994 - Date of publication of application).
	AO61	English-language Abstract of Japanese Patent Publication No. JP 10-96778, data supplied by the espacenet, 1 page (April 14, 1998 - Date of publication of application).
	AP61	English-language Abstract of Japanese Patent Publication No. JP 11-98205, data supplied by the espacenet, 1 page (April 9, 1999 - Date of publication of application).
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA71	6,975,848 B2	12/2005	Rawlins *et al.*			
	AB71	6,404,758 B1	06/2002	Wang			
	AC71	6,909,739 B1	06/2005	Eerola *et al.*			
	AD71	6,910,015 B2	06/2005	Kawai			
	AE71	3,719,903	03/1973	Goodson			
	AF71	4,591,930	05/1986	Baumeister			
	AG71	7,006,805 B1	02/2006	Sorrells *et al.*			
	AH71	7,010,286 B2	03/2006	Sorrells *et al.*			
	AI71	7,010,559 B2	03/2006	Rawlins *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

511357_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA72	5,131,014	07/1992	White			
	AB72	6,393,070 B1	05/2002	Reber			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

511357_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

DFW

Sterne Kessler Goldstein Fox
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OIPE IAP13
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PATENT & TRADEMARK OFFICE

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June 6, 2006

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2616

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Third Supplemental Information Disclosure Statement;

2. A listing of the cited documents on Form PTO-1449 (*4 pages*); and

3. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL:apg
Enclosures

540839_1.DOC

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

OIPE IAP13 JUN 06 2006 PATENT & TRADEMARK OFFICE

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2616
Appl. No.: 10/973,917	Examiner: Chin, Wellington
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Third Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Third Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Second Supplemental Information Disclosure Statement filed on March 28, 2006 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Applicants provide the following comments regarding the documents:

Documents AC72, AH73, and AI73 are co-owned patents which are directed to related subject matter.

Documents AD72 and AE72 were cited in an Office Action in related U.S. Patent Application No. 11/173,021, filed July 5, 2005, entitled "Method and Circuit for Down-Converting a Signal," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,393,070, which has already been cited in the present application.

Documents AF72-AI72 and AA73-AG73 were cited in an Office Action in related U.S. Patent Application No. 10/305,299, filed November 27, 2002, entitled "Method and Apparatus for Improving Dynamic Range In a Communication System," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,339,459 and 5,517,688, which have already been cited in the present application.

Documents AA74 and AB74 were cited in an Office Action in related U.S. Patent Application No. 10/197,255, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,703,584; 5,887,001; 6,298,065; and 6,850,742; and U.S. Patent Publication Nos. 2002/0080728 and 2002/0163921, which have already been cited in the present application.

Documents AC74-AG74 were cited in an Office Action in related U.S. Patent Application No. 11/068,370, filed March 1, 2005, entitled "Method and System for Frequency Up-Conversion with a Variety of Transmitter Configurations," directed to

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related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,903,854 and 5,914,622, which have already been cited in the present application.

Document AH74 was cited in an Office Action in related U.S. Patent Application No. 09/567,977, filed May 10, 2000, entitled "Optical Down-converter Using Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action was Deboo, Gordon J., *Integrated Circuits and Semiconductor Devices*, 2nd Edition, McGraw Hill, Inc., pp. 41-45 (1977), which has already been cited in the present application.

Documents AI74 and AA75 were cited in an Office Action in related U.S. Patent Application No. 10/086,367, filed March 4, 2002, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,091,940, which has already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the

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search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☐ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

☒ 7. In accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent publications cited on the attached Form PTO-1449 are not enclosed.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000 (now abandoned), 09/476,093, filed January 3, 2000 (now U.S. Patent No. 7,006,805), 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

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It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: June 6, 2006

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

534717_1.DOC

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OIPE IAP13 JUN 06 2006 PATENT & TRADEMARK OFFICE

FORM PTO-1449

THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
0744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC72	7,016,663 B2	03/2006	Sorrells *et al.*			
	AD72	3,694,754	09/1972	Baltzer			
	AE72	4,931,716	06/1990	Jovanovic *et al.*			
	AF72	3,617,898	11/1971	Janning, Jr.			
	AG72	3,764,921	10/1973	Huard			
	AH72	4,158,149	06/1979	Otofuji			
	AI72	4,380,828	04/1983	Moon			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

534711_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA73	4,562,414	12/1985	Linder *et al.*			
	AB73	4,814,649	03/1989	Young			
	AC73	4,845,389	07/1989	Pyndiah *et al.*			
	AD73	5,172,019	12/1992	Naylor *et al.*			
	AE73	5,263,198	11/1993	Geddes *et al.*			
	AF73	5,551,076	08/1996	Bonn			
	AG73	5,633,610	05/1997	Maekawa *et al.*			
	AH73	7,027,786 B1	04/2006	Smith *et al.*			
	AI73	7,039,372 B1	05/2006	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
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	AO	
	AP	
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	AR	

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA74	6,591,310 B1	07/2003	Johnson			
	AB74	6,963,626 B1	11/2005	Shaeffer *et al.*			
	AC74	4,811,422	03/1989	Kahn			
	AD74	5,825,257	10/1998	Klymyshyn *et al.*			
	AE74	5,986,600	11/1999	McEwan			
	AF74	6,865,399 B2	03/2005	Fujioka *et al.*			
	AG74	2006/0039449 A1	02/2006	Fontana *et al.*			
	AH74	5,847,594	12/1998	Mizuno			
	AI74	3,641,442	02/1972	Boucher			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
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	AO	
	AP	
	AQ	
	AR	

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FORM PTO-1449 THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA75	5,140,699	08/1992	Kozak			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
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	AP	
	AQ	
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973917	SORRELLS ET AL.
	Examiner	**Art Unit**
	Sonny TRINH	2618

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/19/2008								
	1	-								
	2	-								
	3	-								
	4	-								
	5	✓								
	6	✓								
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	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973917	SORRELLS ET AL.
	Examiner	**Art Unit**
	Sonny TRINH	2618

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
455	41.2, 552.1, 422.1, 550.1, 556.1, 556.2, 39, 41., 67.113	3/19/08	ST

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
U.S. Patent, EPO, JPO, DERWENT, PG-PUB	3/19/08	ST

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

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Mail Date Cancel
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•Practice Limited to Federal Agencies

TJW

August 9, 2005

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2661
Mail Stop Amendment

Re: U.S. Nonprovisional Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: Sorrells *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;
2. Form PTO-1449 listing 985 documents and accompanied by two (2) documents;
3. Two compact discs labeled *IDS References Disc 1* and *IDS References Disc 2*; and
4. One return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/NDD/sjc
Enclosures

429710_1.DOC

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

OIPE JC73
AUG 09 2005
PATENT & TRADEMARK OFFICE

Mail Date Cancel
OIPE JC73
AUG 10 2005
PATENT & TRADEMARK OFFICE

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Sorrells *et al.*
Appl. No.: 10/973,917
Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**

Confirmation No.: 3273
Art Unit: 2661
Examiner: (to be assigned)
Atty. Docket: 1744.0330003

Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

In addition to providing hard copies of the documents as required by applicable rules (see boxes 7 and 8 below), Applicants herewith provide two Compact Discs labeled "Disc 1" and "Disc 2" having stored thereon searchable electronic copies (in PDF format) of the documents listed on the PTO-1449. More specifically, "Disc 1" contains electronic copies of documents AA1-AR1, AA2-AR2, AA3-AR3, AA4-AR4, AA5-AR5, AA6-AR6, AA7-AR7, AA8-AR8, AA9-AR9, AA10-AL10, AN10-AR10, AA11-AI11, AN11-AR11, AA12-AI12, AN12-AR12, AA13-AI13, AN13-AR13, AA14-AI14, AN14-AR14, AA15-AI15, AN15-AR15, AA16-AI16, AN16-AR16, AA17-AI17, AN17-AR17, AA18-AI18, AN18-AR18, AA19-AI19, AN19-AR19, AA20-AI20, AN20-AR20, AA21-AI21, AN21-AR21, AA22-AI22,

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AN22-AR22, AA23-AI23, AN23-AR23, AA24-AI24, AN24-AR24, AA25-AI25, AN25-AR25, AA26-AI26, AN26-AR26, AA27-AI27, AN27-AR27, AA28-AI28, AN28-AR28, AA29-AI29, AN29-AR29, AA30-AI30, AN30-AR30, AA31-AI31, AN31-AR31, AA32-AI32, AN32-AR32, AA33-AI33, AN33-AR33, AA34-AI34, AN34-AR34, AA35-AI35, AN35-AR35, AA36-AI36, AN36-AR36, AA37-AI37, AN37-AR37, AA38-AI38, AN38-AR38, AA39-AI39, AN40-AR40, AN41-AR41, AN42-AR42, AN43-AR43, AN44-AR44, AN45-AR45, AN46-AR46, AN47-AR47, AN48-AR48, AN49-AR49, AN50, and AO50; and "Disc 2" contains electronic copies of documents AM10, AJ11-AM11, AJ12-AM12, AJ13-AM13, AJ14-AM14, AJ15-AM15, AJ16-AM16, AJ17-AM17, AJ18-AM18, AJ19-AM19, AJ20-AM20, AJ21-AM21, AJ22-AM22, AJ23-AL23, AA40-AI40, AA41-AI41, AA42-AI42, AA43-AI43, AA44-AI44, AA45-AI45, AA46-AI46, AA47-AI47, AA48-AI48, AA49-AI49, AA50-AI50, AP50-AR50, AA51-AI51, AN51-AR51, AA52-AI52, AN52-AR52, AA53-AI53, AN53-AR53, AA54-AI54, AN54-AR54, AA55-AI55, AN55-AR55, AA56-AI56, AN56-AR56, AA57-AI57, AN57-AR57, AA58-AI58, AN58-AR58, AA59-AI59, AN59-AP59, AA60-AI60, AA61-AI61, AA62-AI62, AA63-AI63, AA64-AI64, AA65-AI65, and AA66-AH66. Documents AQ59, AI66, and AA67-AF67 have not been scanned at this time. The file names on the CDs correspond to the identifiers on the PTO-1449. It is noted that the CDs are being provided in addition to hard copies of the documents (as required by applicable rules) for the convenience of the Examiner.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication

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dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents AD1, AL1, AO1, AC2, AF2, AG2, AI2, AC5, AG5, AB6, AF7, AI7, AB8, AF8, AG9, AK9, AO9, AO11, AA12, AE14, AN14, AB15, AE15, AH15, AO15, AF16, AD18, AG18, AB20, AC20, AQ20, AA22, AH22, AI23, AC24, AF26, AC30, AH31, AC32, AA33, AR33, AH34, AP35 and AO48 were included with Petitions to Make Special pleadings in co-owned related U.S. Patent Nos. 6,061,551, 6,061,555, 6,049,706 and 6,091,940.

Documents AJ1, AL9, AJ10, AA19, AC25, AB30 and AF32 were cited in search reports in the corresponding foreign applications of the above-referenced co-owned related patents.

Documents AM4, AH6, AL7, AJ9, AM9, AC17, AA20, AG20, AG21, AA24, AD24, AG24, AI31, AA32, AG34, AD36 and AQ37 were cited in searches performed at Applicants' request by the European Patent Office's Searching Authority in the above-referenced co-owned related patents.

Documents AH5, AH17, AD21, AB34, AE34, AB36, AI36 and AI38 were cited by the Examiners in the above-referenced co-owned related patents.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Documents AP6-AR6 and AN7-AP7 are copies of Declarations (including Exhibits) made by Messrs. Bultman, Cook, Holtz, Looke, Moses, Parker, and Sorrells, filed in the above-referenced co-owned related patents.

Documents AA6, AD6, AO6, AE7, AE8, AA11, AE11, AH11, AI12, AB13, AD13, AH13, AC14, AG14, AE16, AB17, AF19, AD20, AN21, AG23, AH27, AI27, AI28, AH29, AG30, AD37, AR40, AO49 and AQ49 were suggested or identified by potential licensees.

Documents AR21, AN22-AR22, AN23-AR23, AN24-AR24, AN25-AR25, AN26-AR26, AN27-AR27, AN28-AR28, AN29-AR29, AN30-AR30, AN31-AR31, AN32-AR32 and AN33-AP33 are press releases issued by assignee ParkerVision, Inc.

Documents AA1, AB1, AD1-AG1, AA2, AH21, AD44, and AD59-AF59 were cited by an Examiner in related U.S. Patent Application No. 09/569,044, filed May 10, 2000, entitled "Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Document AA1-AD1, AB48, and AH64 were cited by an Examiner in related U.S. Patent Application No. 10/197,441, filed July 18, 2002, entitled "Method and System for Frequency Up-Conversation With a Variety of Transmitter Configurations," directed to related subject matter.

Documents AJ1, AK9-AM9, AG28, AB30, AA32, AN52 and AP55 were cited by an Examiner in related European Patent Application No. 99954905.8, filed October 18, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Documents AI7, AJ9, AK9, AG20, AG21, AB30 and AI43 were cited in a written opinion in related PCT Application No. PCT/US00/23923, filed October 18, 1999, entitled "Applications of Frequency Translation," directed to related subject matter.

Documents AI7, AE34, AA46, and AB48 were cited by an Examiner in related U.S. Patent Application No. 09/293,580, filed April 16, 1999, entitled "Method and System for Frequency Up-Conversion with a Variety of Transmitted Configurations," directed to related subject matter.

Documents AK9, AM9, AE15, AL19, AM19, AB46 and AA50 were cited in a search report in related PCT Application No. PCT/US01/08969, filed March 22, 2001, entitled, "Integrated Frequency Translation and Selectivity with a Gain Control Functionality, and Applications Thereof," directed to related subject matter.

Documents AK9, AE15, AK22-AM22, AA27, AC32, AE45, AI51, AA52, and AQ58 were cited in a search report in related PCT Application No. PCT/US01/15555, filed May 16, 2001, entitled, "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AK9, AC17, AD36 and AD40 were cited in a search report in related PCT Application No. PCT/US00/21359, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AJ10, AH17, AG28, AH34, AD44-AI44, and AA45-AD45 were cited by an Examiner in related U.S. Patent Application No. 09/261,129, filed March

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

3, 1999, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Documents AM10, AJ11, AK11 and AE40 were cited in a communication issued by the International Preliminary Examination Authority in related PCT Application No. PCT/US00/01108, filed January 19, 2000, entitled "Frequency Translation and Embodiments Thereof Such as the Family Radio Service," directed to related subject matter.

Documents AL11, AM11, AA44, and AQ50 were cited in a communication issued by the International Searching Authority in related PCT Application No. PCT/US00/09911, filed April 14, 2000, entitled "Method And System For Down-converting an Electromagnetic Signal, And Transforms For Same," directed to related subject matter.

Documents AJ12, AK12, AE45, and AF45 were cited in a search report in related PCT Application No. PCT/US00/27555, filed October 6, 2000, entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AL12, AM12, AG45, and AH45 were cited in a search report in related PCT Application No. PCT/US00/34771, filed January 21, 2000, entitled "Phase Comparator Using Undersampling," directed to related subject matter.

Documents AJ13-AL13, AI45, and AB46 were cited in a search report issued in related PCT Application No. PCT/US00/27281, filed October 4, 2000, entitled "Frequency Converter and Method," directed to related subject matter.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Documents AL13, AM18, AJ19, and AI45 were cited in a search report in related PCT Application No. PCT/US00/31659, filed November 20, 2000, entitled "Phase Shifting Applications of Universal Frequency Translation," directed to related subject matter.

Documents AM13, AJ14, AK14, AM21, AJ22 and AQ51 were cited by an Examiner in related Japanese Patent Application No. 2000-577,765, filed June 21, 2000, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AL14, AM14, AJ15 and AK15 were cited by an Examiner in related Japanese Patent Application No. 2000-577,761, filed June 20, 2000, entitled "Method and System for Frequency Up-conversion," directed to related subject matter.

Documents AL15, AM15, AJ16-AM16, AJ17-AM17, AJ20, and AK23 were cited by an Examiner in related Japanese Patent Application No. 2000-577,764, filed June 21, 2000, entitled "Applications of Frequency Translation," directed to related subject matter.

Documents AJ18-AL18, AB47, AC47, AE47-AG47, AB48, and AC49 were cited by an Examiner in related U.S. Patent Application No. 09/489,675, filed January 24, 2000, entitled "Bar Code Scanner Using Universal Frequency Translation Technology for Up-Conversion and Down-Conversion," directed to related subject matter.

Documents AK19 and AF48 were cited in a search report in related PCT Application No. PCT/US01/15111, filed October 5, 2001, entitled "Method and

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Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Documents AK20, AL20, AJ21, AK21, AL21, AE42, AP56 and AQ56 were cited in a search report in related PCT Application No. PCT/US01/12086, filed April 13, 2001, entitled, "Frequency Converter," directed to related subject matter.

Documents AI23, AB30, AB60-AE60, and AC65 were cited by an Examiner in related U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Methods and Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Document AI23 and AD46 were cited by an Examiner in related U.S. Patent Application No. 09/293,095, filed April 16, 1999, entitled "Method and System for Down-Converting an Electromagnetic Signal Having Optimized Switch Structures," directed to related subject matter.

Documents AI23, AH50, AB55, AI59, and AA60 were cited by an Examiner in related U.S. Patent Application No. 09/525,185, filed March 14, 2000, entitled "Spread Spectrum Applications of Universal Frequency Translation Technology," directed to related subject matter.

Documents AI23, AI59, AF60-AH60, and AA65 were cited by an Examiner in related U.S. Patent Application No. 09/590,955, filed June 9, 2000, entitled "Phase-Shifting Applications of Universal Frequency Translation," directed to related subject matter.

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Documents AJ23 and AB52 were cited in an Invitation to Pay Additional Fees in PCT Application No. PCT/US01/43077, filed November 14, 2001, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Documents AL23, AH47, AB49, AG51, AF56-AH56, AO59, and AE61 were cited by an Examiner in related U.S. Patent Application No. 09/669,634, filed September 26, 2000, entitled "High Frequency Translator and Method of High Frequency Translation," directed to related subject matter.

Documents AC24, AD47, AA48, and AB50 were cited by an Examiner in related U.S. Patent Application No. 09/376,509, filed August 18, 1999, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AG27, AH47, AI47, AC52, AC56, AE64, AI65, and AA66-AG66 were cited by an Examiner in related U.S. Patent Application No. 09/855,851, filed May 16, 2001, entitled "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AD35, AB44, AC44, AE46-AI46, and AA47 were cited by an Examiner in parent U.S. Patent Application No. 09/293,342, filed April 16, 1999, entitled "Method and System for Down-Converting Electromagnetic Signals Including Resonant Structures for Enhanced Energy Transfer," directed to related subject matter.

Documents AA38 and AG48 were cited by an Examiner in related U.S. Patent Application No. 09/476,091, filed January 3, 2000, entitled "Image-Reject Down-

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Converter and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AI43, AH47 and AH48 were cited by an Examiner in related U.S. Patent Application No. 09/293,283, filed April 16, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

Documents AC46 and AA48 were cited by an Examiner in related U.S. Patent Application No. 09/670,831, filed September 28, 2000, entitled "Universal Frequency Translation, Embodiments Thereof, and a Web Site and Web Pages Directed to Same," directed to related subject matter.

Documents AH47, AI47, AA48-AE48, AB49, AF51, AG51, AC52, AG54, AF55, AC56, AD56, AI56, AA57, AD64, AE64, AB65, AH65, AH66, and AI66 are co-owned patents which are directed to related subject matter.

Documents AI47, AH50, AF55, AC56, AD56, AI56, AA57, and AH59 were cited by an Examiner in related U.S. Patent Application No. 09/838,387, filed April 20, 2001, entitled "Method and System for Down-Converting and Up-Converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AB48, AD48, AH54, AI54, and AA55-AC55 were cited by an Examiner in related U.S. Patent Application No. 09/548,923, filed April 13, 2000, entitled "Method and System for Frequency Conversion with Modulation Embodiments," directed to related subject matter.

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Documents AB48, AE48, AD56, AI56, AG651, and AH61 were cited by an Examiner in related U.S. Patent Application No. 09/525,615, filed March 14, 2000, entitled "Method, System, and Apparatus for Balanced Frequency Up-conversion of a Baseband Signal," directed to related subject matter.

Documents AI48, AA49, and AF50 were cited by an Examiner in related U.S. Patent Application No. 09/567,963, filed May 10, 2000, entitled "Frequency Synthesizer Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AD49-AI49, AE51, and AB67 were cited by an Examiner in related U.S. Patent Application No. 09/476,092, filed January 3, 2000, entitled "Analog Zero IF FM Decoder and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AI49, AH50, AI50, AA51, AB51, AI62, AA63, and AB63 were cited by an Examiner in related U.S. Patent Application No. 09/632,857, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter.

Documents AC50-AE50, AG50, AI50 and AC51 were cited by an Examiner in related U.S. Patent Application No. 09/476,330, filed January 3, 2000, entitled, "Multi-Mode, Multi-Band Communication System," directed to related subject matter.

Documents AH50, AA51 and AB51 were cited in by an Examiner in related U.S. Patent Application No. 09/526,041, filed March 14, 2000, entitled, "DC Offset,

Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AH50, AC53-AI53, and AF61 were cited by an Examiner in related U.S. Patent Application No. 09/476,093, filed January 3, 2000, entitled "Family Radio System with Multi-Mode and Multi-Band Functionality," directed to related subject matter.

Documents AH50 and AB57-AE57 were cited by an Examiner in related U.S. Patent Application No. 09/567,978, filed May 10, 2000, entitled "Carrier and Clock Recovery Using Universal Frequency Translation," directed to related subject matter.

Documents AH51, AB56, AE56, AN58-AP58, AN59, AP59, AG63, and AC67-AF67 were cited by an Examiner in related U.S. Patent Application No. 09/567,977, filed May 10, 2000, entitled "Optical Down-converter Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AA52, AF52, AI52, and AG59 were cited by an Examiner in related U.S. Patent Application No. 10/289,377, filed November 7, 2002, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AD52-AG52 and AC63-AF63 were cited by an Examiner in related U.S. Patent Application No. 09/986,764, filed November 9, 2001, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

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Documents AA52, AE52, AH52, AI52, AA53, and AB53 were cited in a search report in related PCT Application No. PCT/US02/35861, filed November 8, 2002, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AA54-AD54 were cited in a search report in a related PCT Application No. PCT/US03/16403, filed May 27, 2003, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AB54, AI61, AA62, and AB62 were cited in a written opinion in related PCT Application No. PCT/US03/16403, filed May 27, 2003, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AB54, AQ59, AI61, and AA62-AH62 were cited by an Examiner in related U.S. Patent Application No. 10/290,323, filed November 8, 2002, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AE54, AF54, AH55, AI60, AA61, AB61, and AA67 were cited by an Examiner in related U.S. Patent Application No. 09/550,642, filed April 14, 2000, entitled "Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AD55 and AE55 were cited by an Examiner in related U.S. Patent Application No. 09/543,867, filed April 5, 2000, entitled "Automated Meter Reader Applications of Universal Frequency Translation," directed to related subject matter.

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Documents AG55 and AH55 were cited by an Examiner in related U.S. Patent Application No. 10/317,181, filed December 12, 2002, entitled "Differential Frequency Down-Conversion Using Techniques of Universal Frequency Translation Technology," directed to related subject matter.

Documents AI55, AA56, AC61, and AD61 were cited by an Examiner in related U.S. Patent Application No. 10/317,165, filed December 12, 2002, entitled "Method and Apparatus for Reducing DC Offsets in Communication Systems Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AF57 and AG57 were cited by an Examiner in related U.S. Patent Application No. 10/330,219, filed December 30, 2002, entitled "Methods and Systems for Down-Converting Electromagnetic Signals, and Applications Thereof," directed to related subject matter.

Documents AH57, AI57, AA58-AI58, and AA59 were cited by an Examiner in related U.S. Patent Application No. 09/566,188, filed May 5, 2000, entitled "Integrated Frequency Translation and Selectivity with Gain Control Functionality, and Applications Thereof," directed to related subject matter.

Documents AB59 and AC59 were cited by an Examiner in related U.S. Patent Application No. 09/632,856, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation," directed to related subject matter.

Documents AH63, AI63, AA64, and AB64 were cited by an Examiner in parent U.S. Patent Application No. 09/987,193, filed November 13, 2001, entitled

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"Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Document AC64 was cited by an Examiner in related U.S. Patent Application No. 09/632,857, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter.

Documents AF64 and AG64 were cited by an Examiner in related U.S. Patent Application No. 10/289,377, filed November 7, 2002, entitled "Method and Apparatus for Reducing DC Offsets in A Communication System," directed to related subject matter.

Document AI64 was cited by an Examiner in related U.S. Patent Application No. 10/086,250, filed March 4, 2002, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Documents AD65-AG65 were cited by an Examiner in related U.S. Patent Application No. 09/770,675, filed January 29, 2001, entitled "Wireless and Wired Cable Modem Applications of Universal Frequency Translation Technology," directed to related subject matter.

The other documents in the PTO-1449 do not fall within the above categories.

It is noted that some of these documents could be classified in more than one of the above categories.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The

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Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

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☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a

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communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. Concise explanations of the relevance of the non-English language documents AJ1, AK1, AJ6, AK7, AJ8-AL8, AK11-AM11, AJ12, AM13, AJ14-AM14, AJ15-AM15, AJ16-AM16, AJ17-AM17, AJ18-AL18, AJ20-AL20, AK21, AM21, AJ22, AK23, AL23, AQ50 and AQ51 appear below:

Document AJ1 (DE 42 37 692 C1) appears to be a receiver for a digital radio signal. Document AJ1 is a counterpart German application of document AG28, which is in the English language.

Document AK1 (EP 0 035 166 A1) appears to describe a digitized receiver. An English language abstract of document AK1 is enclosed as document AQ8.

Document AJ6 (EP 0 785 635 A1) appears to describe a method and apparatus for frequency diversity transmission using a plurality of uncorrelated carriers. An English language abstract of document AJ6 is enclosed as document AP8.

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Document AK7 (FR 2 743 231 A1) is the corresponding French application of document AJ6 (EP 0 785 635 A1), which is described above.

Document AJ8 (JP 2-39632) appears to describe a transmitter for frequency diversity. An English language abstract of document AJ8 is enclosed as document AO8.

Document AK8 (JP 2-131629) appears to describe a transmitter-receiver for frequency diversity. An English language abstract of document AK8 is enclosed as document AN8.

Document AL8 (JP 2-276351) appears to describe an FSK demodulating circuit. An English language abstract of document AL8 is enclosed as document AR7.

Document AK11 (FR 2245130) appears to describe a converter. A partial English language translation of document AK11 is enclosed as document AP50.

Document AL11 (DE 3541031) appears to describe a method and device for demodulating high-frequency modulated signals. An English language translation of document AL11 is enclosed as document AR50.

Document AM11 (EP 0 732 803) appears to describe a procedure and device for demodulation by sampling. An English translation of document AM11 is enclosed as document AN51.

Document AJ12 (DE 19735798) appears to describe a transceiver. An English translation of document AJ12 is enclosed as document AP51.

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Document AM13 (JP 56-114451) appears to describe a system for diversity radio transmission. Document AM13 is a counterpart Japanese application of document AF8, which is in the English language.

Document AJ14 (JP 8-32556) appears to describe a data transmitter-receiver. An English language abstract of document AJ14 is enclosed as document AO52.

Document AK14 (JP 8-139524) appears to describe a frequency converting circuit and radio communication device. An English language abstract of document AK14 is enclosed as document AP52.

Document AL14 (JP 59-144249) appears to describe a pulse signal transmission system. An English language abstract of document AL14 is enclosed as document AQ52.

Document AM14 (JP 63-54002) appears to describe a microwave burst signal generator which incorporates a FET frequency multiplier. An English language abstract of document AM14 is enclosed as document AR52.

Document AJ15 (JP 6-237276) appears to describe a quadrature modulator. An English language abstract of document AJ15 is enclosed as document AN53.

Document AK15 (JP 8-23359) appears to describe a digital quadrature modulation device. An English language abstract of document AK15 is enclosed as document AO53.

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Document AL15 (JP 47-2314) appears to describe a demodulator. An English language translation of document AL15 is enclosed as document AP53.

Document AM15 (JP 58-7903) appears to describe a switched capacitor modulator. A partial English language translation of document AM15 is enclosed as document AQ53.

Document AJ16 (JP 58-133004) appears to describe an amplitude detector. An English language abstract of document AJ16 is enclosed as document AR53.

Document AK16 (JP 60-58705) appears to describe a frequency converting circuit. An English language abstract of document AK16 is enclosed as document AN54.

Document AL16 (JP 4-123614) appears to describe a level converting circuit. An English language abstract of document AL16 is enclosed as document AO54.

Document AM16 (JP 4-127601) appears to describe a frequency conversion circuit. An English language abstract of document AM16 is enclosed as document AP54.

Document AJ17 (JP 5-175730) appears to describe a time division direct receiver. An English language abstract of document AJ17 is enclosed as document AQ54.

Document AK17 (JP 5-175734) appears to describe an FM demodulator. An English language abstract of document AK17 is enclosed as document AR54.

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Document AL17 (JP 7-154344) appears to describe a receiver for receiving modulated carrier signals and an IQ mixer/demodulator using it's receiving constitution. An English language abstract of document AL17 is enclosed as document AN55.

Document AM17 (JP 7-307620) appears to describe a bottom detection circuit. An English language abstract of document AM17 is enclosed as document AO55.

Document AJ18 (JP 55-66057) appears to describe a bar-code detection circuit. An English language abstract of document AJ18 is enclosed as document AQ55.

Document AK18 (JP 63-65587) appears to describe a wireless light pen device. An English language abstract of document AK18 is enclosed as document AR55.

Document AL18 (JP 63-153691) appears to describe a data transfer for a semiconductor data carrier system. An English language abstract of document AL18 is enclosed as document AN56.

Document AJ20 (JP 60-130203) appears to describe a frequency converter. An English language abstract of document AJ20 is enclosed as document AO56.

Document AK20 (DE 196 27 640 A1) appears to describe a mixer. Document AK20 is a counterpart German application of document AA33, which is in the English language.

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Document AL20 (EP 0 087 336 A1) appears to describe a transistorized mixer for microwave transmitters. The granted version of document AL20 is cited as document AM20 (EP 0 087 336 B1) and contains an English language version of the claims.

Document AK21 (FR 2 669 787 A1) appears to describe a symmetrical super high frequency mixer. An English language abstract of document AK21 is enclosed as document AR56.

Document AM21 (JP 61-30821) appears to describe a squelch device. An English language abstract of document AL21 is enclosed as document AP57.

Document AJ22 (JP 5-327356) appears to describe a frequency converter. An English language abstract of document AJ22 is enclosed as document AQ57.

Document AK23 (JP 9-36664) appears to describe a frequency conversion circuit. An English language abstract of document AK23 is enclosed as document AR58.

Document AL23 (DE 196 48 915 A1) appears to describe a process of frequency conversion. An English language translation of document AL23 is enclosed as document AO59.

Document AQ50 (Fest et al.) appears to discuss analog-digital converters. An English language translation of document AQ50 is enclosed as document AO51.

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Document AQ51 (Miki et al.) appears to describe modulation systems. A partial English language translation of document AQ51 is enclosed as document AR51.

☒ 7. In accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent application publications cited on the attached Form PTO-1449 are not enclosed.

☒ 8. Copies of documents AP59 and AQ59 are enclosed. The remaining documents listed under 'Foreign Patent Documents' and 'Other Documents' were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of the 'Foreign Patent Documents' and 'Other Documents' cited in the parent application are not enclosed. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000, 09/476,093, filed January 3, 2000, 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication

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from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. Sorrells	
FILING DATE	ART UNIT
October 27, 2004	2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	2,057,613	10/1936	Gardner			
	AB1	2,241,078	05/1941	Vreeland			
	AC1	2,270,385	01/1942	Skillman			
	AD1	2,283,575	05/1942	Roberts			
	AE1	2,358,152	09/1944	Earp			
	AF1	2,410,350	10/1946	Labin *et al.*			
	AG1	2,451,430	10/1948	Barone			
	AH1	2,462,069	02/1949	Chatterjea *et al.*			
	AI1	2,462,181	02/1949	Grosselfinger			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	DE 42 37 692 C1	03/1994	DE			No
	AK1	EP 0 035 166 A1	09/1981	EP			No
	AL1	EP 0 193 899 B1	06/1990	EP			N/A
	AM1	EP 0 380 351 A2	08/1990	EP			N/A

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN1	Aghvami, H. *et al.*, "Land Mobile Satellites Using the Highly Elliptic Orbits- The UK T-SAT Mobile Payload," *Fourth International Conference on Satellite Systems for Mobile Communications and Navigation*, IEE, pp. 147-153 (October 17-19, 1988).
	AO1	Akers, N.P. *et al.*, "RF Sampling Gates: a Brief Review," *IEE Proceedings*, IEE, Vol. 133, Part A, No. 1, pp. 45-49 (January 1986).
	AP1	Al-Ahmad, H.A.M. *et al.*, "Doppler Frequency Correction for a Non-Geostationary Communications Satellite. Techniques for CERS and T-SAT," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizers,* IEE, pp. 4/1-4/5 (January 23, 1986).
	AQ1	Ali, I. *et al.*, "Doppler Characterization for LEO Satellites," *IEEE Transactions on Communications*, IEEE, Vol. 46, No. 3, pp. 309-313 (March 1998).
	AR1	Allan, D.W., "Statistics of Atomic Frequency Standards," *Proceedings Of The IEEE Special Issue on Frequency Stability*, IEEE, pp. 221-230 (February 1966).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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OIPE Mail Date Cancel AUG 10 2005 PATENT & TRADEMARK OFFICE

FORM PTO-1449	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
INFORMATION DISCLOSURE STATEMENT	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	2,472,798	06/1949	Fredendall			
	AB2	2,497,859	02/1950	Boughtwood *et al.*			
	AC2	2,499,279	02/1950	Peterson			
	AD2	2,802,208	08/1957	Hobbs			
	AE2	2,985,875	05/1961	Grisdale *et al.*			
	AF2	3,023,309	02/1962	Foulkes			
	AG2	3,069,679	12/1962	Sweeney *et al.*			
	AH2	3,104,393	09/1963	Vogelman			
	AI2	3,114,106	12/1963	McManus			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2	EP 0 380 351 A3	02/1991	EP			N/A
	AK2	EP 0 411 840 A2	02/1991	EP			N/A
	AL2	EP 0 411 840 A3	07/1991	EP			N/A
	AM2	EP 0 411 840 B1	10/1995	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN2	Allstot, D.J. *et al.*, "MOS Switched Capacitor Ladder Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 806-814 (December 1978).
	AO2	Allstot, D.J. and Black Jr. W.C., "Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 967-986 (August 1983).
	AP2	Alouini, M. *et al.*, "Channel Characterization and Modeling for Ka-Band Very Small Aperture Terminals," *Proceedings Of the IEEE*, IEEE, Vol. 85, No. 6, pp. 981-997 (June 1997).
	AQ2	Andreyev, G.A. and Ogarev, S.A., "Phase Distortions of Keyed Millimeter-Wave Signals in the Case of Propagation in a Turbulent Atmosphere," *Telecommunications and Radio Engineering*, Scripta Technica, Vol. 43, No. 12, pp. 87-90 (December 1988).
	AR2	Antonetti, A. *et al.*, "Optoelectronic Sampling in the Picosecond Range," *Optics Communications*, North-Holland Publishing Company, Vol. 21, No. 2, pp. 211-214 (May 1977).

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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. Sorrells	
FILING DATE	ART UNIT
October 27, 2004	2661

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	3,118,117	01/1964	King *et al.*			
	AB3	3,226,643	12/1965	McNair			
	AC3	3,258,694	06/1966	Shepherd			
	AD3	3,383,598	05/1968	Sanders			
	AE3	3,384,822	05/1968	Miyagi			
	AF3	3,454,718	07/1969	Perreault			
	AG3	3,523,291	08/1970	Pierret			
	AH3	3,548,342	12/1970	Maxey			
	AI3	3,555,428	01/1971	Perreault			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3	EP 0 423 718 A2	04/1991	EP			N/A
	AK3	EP 0 423 718 A3	08/1992	EP			N/A
	AL3	EP 0 486 095 A1	05/1992	EP			N/A
	AM3	EP 0 486 095 B1	02/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN3	Austin, J. *et al.*, "Doppler Correction of the Telecommunication Payload Oscillators in the UK T-SAT," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 851-857 (September 12 - 15, 1988).
	AO3	Auston, D.H., "Picosecond optoelectronic switching and gating in silicon," *Applied Physics Letters*, American Institute of Physics, Vol. 26, No. 3, pp. 101-103 (February 1, 1975).
	AP3	Baher, H., "Transfer Functions for Switched-Capacitor and Wave Digital Filters," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-33, No. 11, pp. 1138-1142 (November 1986).
	AQ3	Baines, R., "The DSP Bottleneck," *IEEE Communications Magazine*, IEEE Communications Society, pp. 46-54 (May 1995).
	AR3	Banjo, O.P. and Vilar, E., "Binary Error Probabilities on Earth-Space Links Subject to Scintillation Fading," *Electronics Letters*, IEE, Vol. 21, No. 7, pp. 296-297 (March 28, 1985).

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	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	3,617,892	11/1971	Hawley *et al.*			
	AB4	3,621,402	11/1971	Gardner			
	AC4	3,623,160	11/1971	Giles *et al.*			
	AD4	3,626,417	12/1971	Gilbert			
	AE4	3,629,696	12/1971	Bartelink			
	AF4	3,662,268	05/1972	Gans *et al.*			
	AG4	3,689,841	09/1972	Bello *et al.*			
	AH4	3,714,577	01/1973	Hayes			
	AI4	3,717,844	02/1973	Barret *et al.*			

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	AJ4	EP 0 512 748 A2	11/1992	EP			N/A
	AK4	EP 0 512 748 A3	07/1993	EP			N/A
	AL4	EP 0 512 748 B1	11/1998	EP			N/A
	AM4	EP 0 548 542 A1	06/1993	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN4	Banjo, O.P. and Vilar, E., "The Dependence of Slant Path Amplitude Scintillations on Various Meteorological Parameters," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 277-280 (March 30 - April 2, 1987).
	AO4	Banjo, O.P. and Vilar, E. "Measurement and Modeling of Amplitude Scintillations on Low-Elevation Earth-Space Paths and Impact on Communication Systems," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. COM-34, No. 8, pp. 774-780 (August 1986).
	AP4	Banjo, O.P. *et al.*, "Tropospheric Amplitude Spectra Due to Absorption and Scattering in Earth-Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, IEE, pp. 77-82 (April 16-19, 1985).
	AQ4	Basili,P. *et al.*, "Case Study of Intense Scintillation Events on the OTS Path," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. 38, No. 1, pp. 107-113 (January 1990).
	AR4	Basili, P. *et al.*, "Observation of High C^2 and Turbulent Path Length on OTS Space-Earth Link," *Electronics Letters*, IEE, Vol. 24, No. 17, pp. 1114-1116 (August 18, 1988).

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	FIRST NAMED INVENTOR David F. Sorrells	
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	AA5	3,735,048	05/1973	Tomsa *et al.*			
	AB5	3,806,811	04/1974	Thompson			
	AC5	3,868,601	02/1975	MacAfee			
	AD5	3,949,300	04/1976	Sadler			
	AE5	3,967,202	06/1976	Batz			
	AF5	3,980,945	09/1976	Bickford			
	AG5	3,987,280	10/1976	Bauer			
	AH5	3,991,277	11/1976	Hirata			
	AI5	4,003,002	01/1977	Snijders *et al.*			

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	AJ5	EP 0 632 288 A2	01/1995	EP			N/A
	AK5	EP 0 632 288 A3	07/1996	EP			N/A
	AL5	EP 0 696 854 A1	02/1996	EP			N/A
	AM5	EP 0 782 275 A2	07/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN5	Blakey, J.R. *et al.*, "Measurement of Atmospheric Millimetre-Wave Phase Scintillations in an Absorption Region," *Electronics Letters*, IEE, Vol. 21, No. 11, pp. 486-487 (May 23, 1985).
	AO5	Burgueño, A. *et al.*, "Influence of rain gauge integration time on the rain rate statistics used in microwave communications," *annales des tèlècommunications*, International Union of Radio Science, pp. 522-527 (September/October 1988).
	AP5	Burgueño, A. *et al.*, "Long-Term Joint Statistical Analysis of Duration and Intensity of Rainfall Rate with Application to Microwave Communications," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 198-201 (March 30 - April 2, 1987).
	AQ5	Burgueño, A. *et al.*, "Long Term Statistics of Precipitation Rate Return Periods in the Context of Microwave Communications," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 297-301 (April 4-7, 1989).
	AR5	Burgueño, A. *et al.*, "Spectral Analysis of 49 Years of Rainfall Rate and Relation to Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 9, pp. 1359-1366 (September 1990).

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	FIRST NAMED INVENTOR David F. Sorrells	
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	AA6	4,013,966	03/1977	Campbell			
	AB6	4,019,140	04/1977	Swerdlow			
	AC6	4,035,732	07/1977	Lohrmann			
	AD6	4,047,121	09/1977	Campbell			
	AE6	4,066,841	01/1978	Young			
	AF6	4,066,919	01/1978	Huntington			
	AG6	4,081,748	03/1978	Batz			
	AH6	4,130,765	12/1978	Arakelian *et al.*			
	AI6	4,130,806	12/1978	Van Gerwen *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6	EP 0 785 635 A1	07/1997	EP			No
	AK6	EP 0 795 978 A2	09/1997	EP			N/A
	AL6	EP 0 837 565 A1	04/1998	EP			N/A
	AM6	EP 0 862 274 A1	09/1998	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN6	Catalan, C. and Vilar, E., "Approach for satellite slant path remote sensing," *Electronics Letters,* IEE, Vol. 34, No. 12, pp. 1238-1240 (June 11, 1998).
	AO6	Chan, P. et al., "A Highly Linear 1-GHz CMOS Downconversion Mixer," *European Solid State Circuits Conference*, IEEE Communication Society, pp. 210-213 (September 22-24, 1993).
	AP6	Copy of Declaration of Michael J. Bultman filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AQ6	Copy of Declaration of Robert W. Cook filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AR6	Copy of Declaration of Alex Holtz filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 3 pages.

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	AA7	4,142,155	02/1979	Adachi			
	AB7	4,170,764	10/1979	Salz *et al.*			
	AC7	4,204,171	05/1980	Sutphin, Jr.			
	AD7	4,210,872	07/1980	Gregorian			
	AE7	4,245,355	01/1981	Pascoe *et al.*			
	AF7	4,253,066	02/1981	Fisher *et al.*			
	AG7	4,253,069	02/1981	Nossek			
	AH7	4,308,614	12/1981	Fisher *et al.*			
	AI7	4,320,361	03/1982	Kikkert			

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	AJ7	EP 0 874 499 A2	10/1998	EP			N/A
	AK7	FR 2 743 231 A1	07/1997	FR			No
	AL7	GB 2 161 344 A	01/1986	GB			N/A
	AM7	GB 2 215 945 A	09/1989	GB			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN7	Copy of Declaration of Richard C. Looke filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AO7	Copy of Declaration of Charley D. Moses, Jr. filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AP7	Copy of Declaration of Jeffrey L. Parker and David F. Sorrells, with attachment Exhibit 1, filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 130 pages.
	AQ7	Dewey, R.J. and Collier, C.J., "Multi-Mode Radio Receiver," *Electronics Division Colloquium on Digitally Implemented Radios,* IEE, pp. 3/1-3/5 (October 18, 1985).
	AR7	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-276351, 1 page (November 13, 1990 - Date of publication of application).

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	AA8	4,320,536	03/1982	Dietrich			
	AB8	4,346,477	08/1982	Gordy			
	AC8	4,355,401	10/1982	Ikoma *et al.*			
	AD8	4,356,558	10/1982	Owen *et al.*			
	AE8	4,360,867	11/1982	Gonda			
	AF8	4,363,132	12/1982	Collin			
	AG8	4,365,217	12/1982	Berger *et al.*			
	AH8	4,370,572	01/1983	Cosand *et al.*			
	AI8	4,389,579	06/1983	Stein			

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	AJ8	JP 2-39632	02/1990	JP			No
	AK8	JP 2-131629	05/1990	JP			No
	AL8	JP 2-276351	11/1990	JP			No
	AM8	WO 80/01633 A1	08/1980	PCT			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-131629, 1 page (May 21, 1990 - Date of publication of application).
	AO8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-39632, 1 page (February 8, 1990 - Date of publication of application).
	AP8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 0 785 635 A1, 3 pages (December 26, 1996 - Date of publication of application).
	AQ8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 35166 A1, 2 pages (February 18, 1981 - Date of publication of application).
	AR8	"DSO takes sampling rate to 1 Ghz," *Electronic Engineering*, Morgan Grampian Publishers, Vol. 59, No. 723, pp. 77 and 79 (March 1987).

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	AA9	4,392,255	07/1983	Del Giudice			
	AB9	4,430,629	02/1984	Betzl *et al.*			
	AC9	4,446,438	05/1984	Chang *et al.*			
	AD9	4,456,990	06/1984	Fisher *et al.*			
	AE9	4,472,785	09/1984	Kasuga			
	AF9	4,479,226	10/1984	Prabhu *et al.*			
	AG9	4,481,490	11/1984	Huntley			
	AH9	4,481,642	11/1984	Hanson			
	AI9	4,485,488	11/1984	Houdart			

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	AJ9	WO 94/05087 A1	03/1994	PCT			N/A
	AK9	WO 96/02977 A1	02/1996	PCT			N/A
	AL9	WO 96/08078 A1	03/1996	PCT			N/A
	AM9	WO 96/39750 A1	12/1996	PCT			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN9	Erdi, G. and Henneuse, P.R., "A Precision FET-Less Sample-and-Hold with High Charge-to-Droop Current Ratio," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 864-873 (December 1978).
	AO9	Faulkner, N.D. and Vilar, E., "Subharmonic Sampling for the Measurement of Short Term Stability of Microwave Oscillators," *IEEE Transactions on Instrumentation and Measurement*, IEEE, Vol. IM-32, No. 1, pp. 208-213 (March 1983).
	AP9	Faulkner, N.D. *et al.*, "Sub-Harmonic Sampling for the Accurate Measurement of Frequency Stability of Microwave Oscillators," *CPEM 82 Digest: Conference on Precision Electromagnetic Measurements*, IEEE, pp. M-10 and M-11 (1982).
	AQ9	Faulkner, N.D. and Vilar, E., "Time Domain Analysis of Frequency Stability Using Non-Zero Dead-Time Counter Techniques," *CPEM 84 Digest Conference on Precision Electromagnetic Measurements*, IEEE, pp. 81-82 (1984).
	AR9	Filip, M. and Vilar, E., "Optimum Utilization of the Channel Capacity of a Satellite Link in the Presence of Amplitude Scintillations and Rain Attenuation," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 11, pp. 1958-1965 (November 1990).

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U.S. PATENT DOCUMENTS

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	AA10	4,504,803	03/1985	Lee *et al.*			
	AB10	4,517,519	05/1985	Mukaiyama			
	AC10	4,517,520	05/1985	Ogawa			
	AD10	4,518,935	05/1985	van Roermund			
	AE10	4,521,892	06/1985	Vance *et al.*			
	AF10	4,563,773	07/1986	Dixon, Jr. *et al.*			
	AG10	4,577,157	03/1986	Reed			
	AH10	4,583,239	04/1986	Vance			
	AI10	4,591,736	05/1986	Hirao *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ10	WO 97/38490 A1	10/1997	PCT			N/A
	AK10	WO 98/00953 A1	01/1998	PCT			N/A
	AL10	WO 98/24201 A1	06/1998	PCT			N/A
	AM10	EP 0 099 265 A1	01/1984	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN10	Fukahori, K., "A CMOS Narrow-Band Signaling Filter with Q Reduction," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-19, No. 6, pp. 926-932 (December 1984).
	AO10	Fukuchi, H. and Otsu, Y., "Available time statistics of rain attenuation on earth-space path," *IEE Proceedings-H: Microwaves, Antennas and Propagation*, IEE, Vol. 135, Pt. H, No. 6, pp. 387-390 (December 1988).
	AP10	Gibbins, C.J. and Chadha, R., "Millimetre-wave propagation through hydrocarbon flame," *IEE Proceedings*, IEE, Vol. 134, Pt. H, No.2 , pp. 169-173 (April 1987).
	AQ10	Gilchrist, B. *et al.*, "Sampling hikes performance of frequency synthesizers," *Microwaves & RF*, Hayden Publishing, Vol. 23, No. 1, pp. 93-94 and 110 (January 1984).
	AR10	Gossard, E.E., "Clear weather meteorological effects on propagation at frequencies above 1 Ghz," *Radio Science*, American Geophysical Union, Vol. 16, No. 5, pp. 589-608 (September - October 1981).

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	AB11	4,603,300	07/1986	Welles, II *et al.*			
	AC11	4,612,464	09/1986	Ishikawa *et al.*			
	AD11	4,612,518	09/1986	Gans *et al.*			
	AE11	4,616,191	10/1986	Galani *et al.*			
	AF11	4,621,217	11/1986	Saxe *et al.*			
	AG11	4,628,517	12/1986	Schwarz *et al.*			
	AH11	4,634,998	01/1987	Crawford			
	AI11	4,648,021	03/1987	Alberkrack			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ11	EP 0 560 228 A1	09/1993	EP			N/A
	AK11	FR 2 245 130	04/1975	FR			Yes (See AP50)
	AL11	DE 35 41 031 A1	05/1986	DE			Yes (See AR50)
	AM11	EP 0 732 803 A1	09/1996	EP			Yes (See AN51)

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN11	Gregorian, R. *et al.*, "Switched-Capacitor Circuit Design," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 941-966 (August 1983).
	AO11	Groshong *et al.*, "Undersampling Techniques Simplify Digital Radio," *Electronic Design*, Penton Publishing, pp. 67-68, 70, 73-75 and 78 (May 23, 1991).
	AP11	Grove, W.M., "Sampling for Oscilloscopes and Other RF Systems: Dc through X-Band," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, pp. 629-635 (December 1966).
	AQ11	Haddon, J. *et al.*, "Measurement of Microwave Scintillations on a Satellite Down-Link at X-Band," *Antennas and Propagation*, IEE, pp. 113-117 (1981).
	AR11	Haddon, J. and Vilar, E., "Scattering Induced Microwave Scintillations from Clear Air and Rain on Earth Space Paths and the Influence of Antenna Aperture," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 5, pp. 646-657 (May 1986).

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	AA12	4,651,034	03/1987	Sato			
	AB12	4,675,882	06/1987	Lillie *et al.*			
	AC12	4,688,253	08/1987	Gumm			
	AD12	4,716,376	12/1987	Daudelin			
	AE12	4,716,388	12/1987	Jacobs			
	AF12	4,718,113	01/1988	Rother *et al.*			
	AG12	4,726,041	02/1988	Prohaska *et al.*			
	AH12	4,733,403	03/1988	Simone			
	AI12	4,734,591	03/1988	Ichitsubo			

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	AJ12	DE 197 35 798 C1	07/1998	DE			Yes (See AP51)
	AK12	WO 98/40968 A2&A3	09/1998	PCT			N/A
	AL12	EP 0 529 836 A1	03/1993	EP			N/A
	AM12	EP 0 795 955 A2&A3	09/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN12	Hafdallah, H. *et al.*, "2-4 Ghz MESFET Sampler," *Electronics Letters*, IEE, Vol. 24, No. 3, pp. 151-153 (February 4, 1988).
	AO12	Herben, M.H.A.J., "Amplitude and Phase Scintillation Measurements on 8-2 km Line-Of-Sight Path at 30 Ghz," *Electronics Letters*, IEE, Vol. 18, No. 7, pp. 287-289 (April 1, 1982).
	AP12	Hewitt, A. *et al.*, "An 18 Ghz Wideband LOS Multipath Experiment," *International Conference on Measurements for Telecommunication Transmission Systems - MTTS 85*, IEE, pp. 112-116 (November 27-28, 1985)
	AQ12	Hewitt, A. *et al.*, "An Autoregressive Approach to the Identification of Multipath Ray Parameters from Field Measurements," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 37, No. 11, pp. 1136-1143 (November 1989).
	AR12	Hewitt, A. and Vilar, E., "Selective fading on LOS Microwave Links: Classical and Spread-Spectrum Measurement Techniques," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 36, No. 7, pp. 789-796 (July 1988).

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	AA13	4,737,969	04/1988	Steel *et al.*			
	AB13	4,743,858	05/1988	Everard			
	AC13	4,745,463	05/1988	Lu			
	AD13	4,751,468	06/1988	Agoston			
	AE13	4,757,538	07/1988	Zink			
	AF13	4,768,187	08/1988	Marshall			
	AG13	4,769,612	09/1988	Tamakoshi *et al.*			
	AH13	4,785,463	11/1988	Janc *et al.*			
	AI13	4,791,584	12/1988	Greivenkamp, Jr.			

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	AJ13	EP 0 817 369 A2&A3	01/1998	EP			N/A
	AK13	WO 91/18445 A1	11/1991	PCT			N/A
	AL13	WO 99/23755 A1	05/1999	PCT			N/A
	AM13	JP 56-114451	09/1981	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN13	Hospitalier, E., "Instruments for Recording and Observing Rapidly Varying Phenomena," *Science Abstracts*, IEE, Vol. VII, pp. 22-23 (1904).
	AO13	Howard, I.M. and Swansson, N.S., "Demodulating High Frequency Resonance Signals for Bearing Fault Detection," *The Institution of Engineers Australia Vibration and Noise Conference*, Institution of Engineers, Australia, pp. 115-121 (September 18-20, 1990).
	AP13	Hu, X., *A Switched-Current Sample-and-Hold Amplifier for FM Demodulation*, Thesis for Master of Applied Science, Dept. of Electrical and Computer Engineering, University of Toronto, UMI Dissertation Services, pp. 1-64 (1995).
	AQ13	Hung, H-L. A. *et al.*, "Characterization of Microwave Integrated Circuits Using An Optical Phase-Locking and Sampling System," *IEEE MTT-S Digest*, IEEE, pp. 507-510 (1991).
	AR13	Hurst, P.J., "Shifting the Frequency Response of Switched-Capacitor Filters by Nonuniform Sampling," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. 38, No. 1, pp. 12-19 (January 1991).

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	AA14	4,801,823	01/1989	Yokoyama			
	AB14	4,806,790	02/1989	Sone			
	AC14	4,810,904	03/1989	Crawford			
	AD14	4,810,976	03/1989	Cowley *et al.*			
	AE14	4,811,362	03/1989	Yester, Jr. *et al.*			
	AF14	4,819,252	04/1989	Christopher			
	AG14	4,833,445	05/1989	Buchele			
	AH14	4,862,121	08/1989	Hochschild *et al.*			
	AI14	4,868,654	09/1989	Juri *et al.*			

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	AJ14	JP 8-32556	02/1996	JP			No
	AK14	JP 8-139524	05/1996	JP			No
	AL14	JP 59-144249	08/1984	JP			No
	AM14	JP 63-54002	03/1988	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN14	Itakura, T., "Effects of the sampling pulse width on the frequency characteristics of a sample-and-hold circuit," *IEE Proceedings Circuits, Devices and Systems,* IEE, Vol. 141, No. 4, pp. 328-336 (August 1994).
	AO14	Janssen, J.M.L., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: I. Fundamentals," *Philips Technical Review,* Philips Research Laboratories, Vol. 12, No. 2, pp. 52-59 (August 1950).
	AP14	Janssen, J.M.L. and Michels, A.J., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: II. Electrical Build-Up," *Philips Technical Review*, Philips Research Laboratories, Vol. 12, No. 3, pp. 73-82 (September 1950).
	AQ14	Jondral, V.F. *et al.*, "Doppler Profiles for Communication Satellites," *Frequenz*, Herausberger, pp. 111-116 (May-June 1996).
	AR14	Kaleh, G.K., "A Frequency Diversity Spread Spectrum System for Communication in the Presence of In-band Interference," *1995 IEEE Globecom*, IEEE Communications Society, pp. 66-70 (1995).

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	AA15	4,870,659	09/1989	Oishi *et al.*			
	AB15	4,871,987	10/1989	Kawase			
	AC15	4,885,587	12/1989	Wiegand *et al.*			
	AD15	4,885,756	12/1989	Fontanes *et al.*			
	AE15	4,888,557	12/1989	Puckette, IV *et al.*			
	AF15	4,890,302	12/1989	Muilwijk			
	AG15	4,893,316	01/1990	Janc *et al.*			
	AH15	4,893,341	01/1990	Gehring			
	AI15	4,894,766	01/1990	De Agro			

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	AJ15	JP 6-237276	08/1994	JP			No
	AK15	JP 8-23359	01/1996	JP			No
	AL15	JP 47-2314	02/1972	JP			Yes (See AP53)
	AM15	JP 58-7903	01/1983	JP			Yes (See AQ53)

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN15	Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).
	AO15	Kirsten, J. and Fleming, J., "Undersampling reduces data-acquisition costs for select applications," *EDN*, Cahners Publishing, Vol. 35, No. 13, pp. 217-222, 224, 226-228 (June 21, 1990).
	AP15	Lam, W.K. *et al.*, "Measurement of the Phase Noise Characteristics of an Unlocked Communications Channel Identifier," *Proceedings Of the 1993 IEEE International Frequency Control Symposium*, IEEE, pp. 283-288 (June 2-4, 1993).
	AQ15	Lam, W.K. *et al.*, "Wideband sounding of 11.6 Ghz transhorizon channel," *Electronics Letters*, IEE, Vol. 30, No. 9, pp. 738-739 (April 28, 1994).
	AR15	Larkin, K.G., "Efficient demodulator for bandpass sampled AM signals," *Electronics Letters*, IEE, Vol. 32, No. 2, pp. 101-102 (January 18, 1996).

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	AA16	4,896,152	01/1990	Tiemann			
	AB16	4,902,979	02/1990	Puckette, IV			
	AC16	4,908,579	03/1990	Tawfik *et al.*			
	AD16	4,910,752	03/1990	Yester, Jr. *et al.*			
	AE16	4,914,405	04/1990	Wells			
	AF16	4,920,510	04/1990	Senderowicz *et al.*			
	AG16	4,922,452	05/1990	Larsen *et al.*			
	AH16	4,931,921	06/1990	Anderson			
	AI16	4,944,025	07/1990	Gehring *et al.*			

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	AJ16	JP 58-133004	08/1983	JP			No
	AK16	JP 60-58705	04/1985	JP			No
	AL16	JP 4-123614	04/1992	JP			No
	AM16	JP 4-127601	04/1992	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN16	Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).
	AO16	Lau, W.H. *et al.*, "Improved Prony Algorithm to Identify Multipath Components," *Electronics Letters*, IEE, Vol. 23, No. 20, pp. 1059-1060 (September 24, 1987).
	AP16	Lesage, P. and Audoin, C., "Effect of Dead-Time on the Estimation of the Two-Sample Variance," *IEEE Transactions on Instrumentation and Measurement*, IEEE Instrumentation and Measurement Society, Vol. IM-28, No. 1, pp. 6-10 (March 1979).
	AQ16	Liechti, C.A., "Performance of Dual-gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. MTT-23, No. 6, pp. 461-469 (June 1975).
	AR16	Linnenbrink, T.E. *et al.*, "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No. 4, pp. 4443-4449 (August 1979).

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	AA17	4,955,079	09/1990	Connerney *et al.*			
	AB17	4,965,467	10/1990	Bilterijst			
	AC17	4,967,160	10/1990	Quievy *et al.*			
	AD17	4,970,703	11/1990	Hariharan *et al.*			
	AE17	4,982,353	01/1991	Jacob *et al.*			
	AF17	4,984,077	01/1991	Uchida			
	AG17	4,995,055	02/1991	Weinberger *et al.*			
	AH17	5,003,621	03/1991	Gailus			
	AI17	5,005,169	04/1991	Bronder *et al.*			

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	AJ17	JP 5-175730	07/1993	JP			No
	AK17	JP 5-175734	07/1993	JP			No
	AL17	JP 7-154344	06/1995	JP			No
	AM17	JP 7-307620	11/1995	JP			No

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	AN17	Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).
	AO17	Lo, P. *et al.*, "Coherent Automatic Gain Control," *IEE Colloquium on Phase Locked Techniques*, IEE, pp. 2/1-2/6 (March 26, 1980).
	AP17	Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).
	AQ17	Lo, P.S.L.O. *et al.*, "Observations of Amplitude Scintillations on a Low-Elevation Earth-Space Path," *Electronics Letters*, IEE, Vol. 20, No. 7, pp. 307-308 (March 29, 1984).
	AR17	Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

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	AA18	5,006,810	04/1991	Popescu			
	AB18	5,010,585	04/1991	Garcia			
	AC18	5,014,304	05/1991	Nicollini *et al.*			
	AD18	5,015,963	05/1991	Sutton			
	AE18	5,017,924	05/1991	Guiberteau *et al.*			
	AF18	5,020,149	05/1991	Hemmie			
	AG18	5,020,154	05/1991	Zierhut			
	AH18	5,052,050	09/1991	Collier *et al.*			
	AI18	5,065,409	11/1991	Hughes *et al.*			

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	AJ18	JP 55-66057	05/1980	JP			No
	AK18	JP 63-65587	03/1988	JP			No
	AL18	JP 63-153691	06/1988	JP			No
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	AN18	Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).
	AO18	Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).
	AP18	Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).
	AQ18	Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).
	AR18	McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

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	AA19	5,083,050	01/1992	Vasile			
	AB19	5,091,921	02/1992	Minami			
	AC19	5,095,533	03/1992	Loper *et al.*			
	AD19	5,095,536	03/1992	Loper			
	AE19	5,111,152	05/1992	Makino			
	AF19	5,113,094	05/1992	Grace *et al.*			
	AG19	5,113,129	05/1992	Hughes			
	AH19	5,122,765	06/1992	Pataut			
	AI19	5,124,592	06/1992	Hagino			

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	AK19	WO 97/08839 A2&A3	03/1997	PCT			N/A
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	AN19	Merkelo, J. and Hall, R.D., "Broad-Band Thin-Film Signal Sampler," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-7, No. 1, pp. 50-54 (February 1972).
	AO19	Merlo, U. *et al.*, "Amplitude Scintillation Cycles in a Sirio Satellite-Earth Link," *Electronics Letters*, IEE, Vol. 21, No. 23, pp. 1094-1096 (November 7, 1985).
	AP19	Morris, D., "Radio-holographic reflector measurement of the 30-m millimeter radio telescope at 22 Ghz with a cosmic signal source," *Astronomy and Astrophysics*, Springer-Verlag, Vol. 203, No. 2, pp. 399-406 (September (II) 1988).
	AQ19	Moulsley, T.J. *et al.*, "The efficient acquisition and processing of propagation statistics," *Journal of the Institution of Electronic and Radio Engineers*, IERE, Vol. 55, No. 3, pp. 97-103 (March 1985).
	AR19	Ndzi, D. *et al.*, "Wide-Band Statistical Characterization of an Over-the-Sea Experimental Transhorizon Link," *IEE Colloquium on Radio Communications at Microwave and Millimetre Wave Frequencies*, IEE, pp. 1/1-1/6 (December 16, 1996).

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	AA20	5,136,267	08/1992	Cabot			
	AB20	5,140,705	08/1992	Kosuga			
	AC20	5,150,124	09/1992	Moore *et al.*			
	AD20	5,151,661	09/1992	Caldwell *et al.*			
	AE20	5,159,710	10/1992	Cusdin			
	AF20	5,170,414	12/1992	Silvian			
	AG20	5,172,070	12/1992	Hiraiwa *et al.*			
	AH20	5,191,459	03/1993	Thompson *et al.*			
	AI20	5,204,642	04/1993	Ashgar *et al.*			

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	AJ20	JP 60-130203	07/1985	JP			Yes (See AO56)
	AK20	DE 196 27 640 A1	01/1997	DE			No
	AL20	EP 0 087 336 A1	08/1983	EP			No
	AM20	EP 0 087 336 B1	07/1986	EP			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN20	Ndzi, D. *et al.*, "Wideband Statistics of Signal Levels and Doppler Spread on an Over-The-Sea Transhorizon Link," *IEE Colloquium on Propagation Characteristics and Related System Techniques for Beyond Line-of-Sight Radio*, IEE, pp. 9/1-9/6 (November 24, 1997).
	AO20	"New zero IF chipset from Philips," *Electronic Engineering*, United News & Media, Vol. 67, No. 825, p. 10 (September 1995).
	AP20	Ohara, H. *et al.*, "First monolithic PCM filter cuts cost of telecomm systems," *Electronic Design*, Hayden Publishing Company, Vol. 27, No. 8, pp. 130-135 (April 12, 1979).
	AQ20	Oppenheim, A.V. *et al.*, *Signals and Systems*, Prentice-Hall, pp. 527-531 and 561-562 (1983).
	AR20	Ortgies, G., "Experimental Parameters Affecting Amplitude Scintillation Measurements on Satellite Links," *Electronics Letters*, IEE, Vol. 21, No. 17, pp. 771-772 (August 15, 1985).

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA21	5,212,827	05/1993	Meszko *et al.*			
	AB21	5,214,787	05/1993	Karkota, Jr.			
	AC21	5,220,583	06/1993	Solomon			
	AD21	5,220,680	06/1993	Lee			
	AE21	5,222,144	06/1993	Whikehart			
	AF21	5,230,097	07/1993	Currie *et al.*			
	AG21	5,239,686	08/1993	Downey			
	AH21	5,241,561	08/1993	Barnard			
	AI21	5,249,203	09/1993	Loper			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ21	EP 0 789 449 A2 & A3	08/1997	EP			N/A
	AK21	FR 2 669 787 A1	05/1992	FR			No
	AL21	GB 2 324 919 A	11/1998	GB			N/A
	AM21	JP 61-30821	02/1986	JP			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN21	Pärssinen et al., "A 2-GHz Subharmonic Sampler for Signal Downconversion," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 45, No. 12, 7 pages (December 1997).
	AO21	Peeters, G. *et al.*, "Evaluation of Statistical Models for Clear-Air Scintillation Prediction Using Olympus Satellite Measurements," *International Journal of Satellite Communications*, John Wiley and Sons, Vol. 15, No. 2, pp. 73-88 (March-April 1997).
	AP21	Perrey, A.G. and Schoenwetter, H.K., *NBS Technical Note 1121: A Schottky Diode Bridge Sampling Gate*, U.S. Dept. of Commerce, pp. 1-14 (May 1980).
	AQ21	Poulton, K. *et al.*, "A 1-Ghz 6-bit ADC System," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-22, No. 6, pp. 962-969 (December 1987).
	AR21	Press Release, "Parkervision, Inc. Announces Fiscal 1993 Results," Lippert/Heilshorn and Associates, 2 Pages (April 6, 1994).

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U.S. PATENT DOCUMENTS

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	AA22	5,251,218	10/1993	Stone *et al.*			
	AB22	5,251,232	10/1993	Nonami			
	AC22	5,260,970	11/1993	Henry *et al.*			
	AD22	5,263,194	11/1993	Ragan			
	AE22	5,263,196	11/1993	Jasper			
	AF22	5,267,023	11/1993	Kawasaki			
	AG22	5,278,826	01/1994	Murphy *et al.*			
	AH22	5,282,023	01/1994	Scarpa			
	AI22	5,287,516	02/1994	Schaub			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ22	JP 5-327356	12/1993	JP			No
	AK22	EP 0 643 477 A2 & A3	03/1995	EP			N/A
	AL22	EP 0 877 476 A1	11/1998	EP			N/A
	AM22	EP 0 977 351 A1	02/2000	EP			N/A

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN22	Press Release, "Parkervision, Inc. Announces the Appointment of Michael Baker to the New Position of National Sales Manager," Lippert/Heilshorn and Associates, 1 Page (April 7, 1994).
	AO22	Press Release, "Parkervision's Cameraman Well-Received By Distance Learning Market," Lippert/Heilshorn and Associates, 2 Pages (April 8, 1994).
	AP22	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 2 Pages (April 26, 1994).
	AQ22	Press Release, "Parkervision, Inc. Announces The Retirement of William H. Fletcher, Chief Financial Officer," Lippert/Heilshorn and Associates, 1 Page (May 11, 1994).
	AR22	Press Release, "Parkervision, Inc. Announces New Cameraman System II™ At Infocomm Trade Show," Lippert/Heilshorn and Associates, 3 Pages (June 9, 1994).

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	AA23	5,293,398	03/1994	Hamao *et al.*			
	AB23	5,303,417	04/1994	Laws			
	AC23	5,307,517	04/1994	Rich			
	AD23	5,315,583	05/1994	Murphy *et al.*			
	AE23	5,321,852	06/1994	Seong			
	AF23	5,325,204	06/1994	Scarpa			
	AG23	5,337,014	08/1994	Najle *et al.*			
	AH23	5,339,054	08/1994	Taguchi			
	AI23	5,339,459	08/1994	Schiltz *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ23	WO 00/31659 A1	06/2000	PCT			N/A
	AK23	JP 9-36664	02/1997	JP			No
	AL23	DE 196 48 915 A1	06/1998	DE			Yes (See AO59)
	AM23						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN23	Press Release, "Parkervision, Inc. Announces Appointments to its National Sales Force," Lippert/Heilshorn and Associates, 2 Pages (June 17, 1994).
	AO23	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (August 9, 1994).
	AP23	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (October 28, 1994).
	AQ23	Press Release, "Parkervision, Inc. Announces First Significant Dealer Sale of Its *Cameraman*® System II," Lippert/Heilshorn and Associates, 2 Pages (November 7, 1994).
	AR23	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Lippert/Heilshorn and Associates, 2 Pages (March 1, 1995).

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	AA24	5,355,114	10/1994	Sutterlin *et al.*			
	AB24	5,361,408	11/1994	Watanabe *et al.*			
	AC24	5,369,800	11/1994	Takagi *et al.*			
	AD24	5,375,146	12/1994	Chalmers			
	AE24	5,379,040	01/1995	Mizomoto *et al.*			
	AF24	5,379,141	01/1995	Thompson *et al.*			
	AG24	5,388,063	02/1995	Takatori *et al.*			
	AH24	5,390,364	02/1995	Webster *et al.*			
	AI24	5,400,084	03/1995	Scarpa			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ24						Yes No
	AK24						Yes No
	AL24						Yes No
	AM24						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN24	Press Release, "Parkervision, Inc. Announces Joint Product Developments With VTEL," Lippert/Heilshorn and Associates, 2 Pages (March 21, 1995).
	AO24	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 3 Pages (April 28, 1995).
	AP24	Press Release, "Parkervision Wins Top 100 Product Districts' Choice Award," Parkervision Marketing and Manufacturing Headquarters, 1 Page (June 29, 1995).
	AQ24	Press Release, "Parkervision National Sales Manager Next President of USDLA," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 6, 1995).
	AR24	Press Release, "Parkervision Granted New Patent," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 21, 1995).

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	AA25	5,404,127	04/1995	Lee *et al.*			
	AB25	5,410,541	04/1995	Hotto			
	AC25	5,410,743	04/1995	Seely *et al.*			
	AD25	5,412,352	05/1995	Graham			
	AE25	5,416,803	05/1995	Janer			
	AF25	5,422,913	06/1995	Wilkinson			
	AG25	5,423,082	06/1995	Cygan *et al.*			
	AH25	5,428,638	06/1995	Cioffi *et al.*			
	AI25	5,428,640	06/1995	Townley			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ25						Yes No
	AK25						Yes No
	AL25						Yes No
	AM25						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN25	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 31, 1995).
	AO25	Press Release, "Parkervision, Inc. Expands Its Cameraman System II Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 22, 1995).
	AP25	Press Release, "Parkervision Announces New Camera Control Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 25, 1995).
	AQ25	Press Release, "Parkervision, Inc. Announces Completion of VTEL/Parkervision Joint Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).
	AR25	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA26	5,434,546	07/1995	Palmer			
	AB26	5,438,692	08/1995	Mohindra			
	AC26	5,444,415	08/1995	Dent *et al.*			
	AD26	5,444,416	08/1995	Ishikawa *et al.*			
	AE26	5,444,865	08/1995	Heck *et al.*			
	AF26	5,446,421	08/1995	Kechkaylo			
	AG26	5,446,422	08/1995	Mattila *et al.*			
	AH26	5,448,602	09/1995	Ohmori *et al.*			
	AI26	5,451,899	09/1995	Lawton			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ26						Yes No
	AK26						Yes No
	AL26						Yes No
	AM26						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN26	Press Release, "Parkervision's Cameraman Personal Locator Camera System Wins Telecon XV Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (November 1, 1995).
	AO26	Press Release, "Parkervision, Inc. Announces Purchase Commitment From VTEL Corporation," Parkervision Marketing and Manufacturing Headquarters, 1 Page (February 26, 1996).
	AP26	Press Release, "ParkerVision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (February 27, 1996).
	AQ26	Press Release, "ParkerVision, Inc. Expands its Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 7, 1996).
	AR26	Press Release, "ParkerVision Files Patents for its Research of Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 1 Page (March 28, 1996).

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	AA27	5,454,007	09/1995	Dutta			
	AB27	5,454,009	09/1995	Fruit *et al.*			
	AC27	5,463,356	10/1995	Palmer			
	AD27	5,463,357	10/1995	Hobden			
	AE27	5,465,071	11/1995	Kobayashi *et al.*			
	AF27	5,465,410	11/1995	Hiben *et al.*			
	AG27	5,465,415	11/1995	Bien			
	AH27	5,471,162	11/1995	McEwan			
	AI27	5,479,120	12/1995	McEwan			

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	AJ27						Yes No
	AK27						Yes No
	AL27						Yes No
	AM27						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN27	Press Release, "Parkervision, Inc. Announces First Significant Sale of Its Cameraman® Three-Chip System," Parkervision Marketing and Manufacturing Headquarters, 2 pages (April 12, 1996).
	AO27	Press Release, "Parkervision, Inc. Introduces New Product Line For Studio Production Market," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1996).
	AP27	Press Release, "Parkervision, Inc. Announces Private Placement of 800,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 1 Page (April 15, 1996).
	AQ27	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 30, 1996).
	AR27	Press Release, "ParkerVision's New Studio Product Wins Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (June 5, 1996).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA28	5,479,447	12/1995	Chow *et al.*			
	AB28	5,483,193	01/1996	Kennedy *et al.*			
	AC28	5,483,549	01/1996	Weinberg *et al.*			
	AD28	5,483,691	01/1996	Heck *et al.*			
	AE28	5,490,173	02/1996	Whikehart *et al.*			
	AF28	5,493,581	02/1996	Young *et al.*			
	AG28	5,493,721	02/1996	Reis			
	AH28	5,495,200	02/1996	Kwan *et al.*			
	AI28	5,495,202	02/1996	Hsu			

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	AJ28						Yes No
	AK28						Yes No
	AL28						Yes No
	AM28						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN28	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (August 1, 1996).
	AO28	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 29, 1996).
	AP28	Press Release, "PictureTel and ParkerVision Sign Reseller Agreement," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1996).
	AQ28	Press Release, "CLI and ParkerVision Bring Enhanced Ease-of-Use to Videoconferencing," CLI/Parkervision, 2 Pages (January 20, 1997).
	AR28	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (February 27, 1997).

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	AA29	5,495,500	02/1996	Jovanovich *et al.*			
	AB29	5,499,267	03/1996	Ohe *et al.*			
	AC29	5,500,758	03/1996	Thompson *et al.*			
	AD29	5,517,688	05/1996	Fajen *et al.*			
	AE29	5,519,890	05/1996	Pinckley			
	AF29	5,523,719	06/1996	Longo *et al.*			
	AG29	5,523,726	06/1996	Kroeger *et al.*			
	AH29	5,523,760	06/1996	McEwan			
	AI29	5,539,770	07/1996	Ishigaki			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ29						Yes No
	AK29						Yes No
	AL29						Yes No
	AM29						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN29	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 29, 1997).
	AO29	Press Release, "NEC and Parkervision Make Distance Learning Closer," NEC America, 2 Pages (June 18, 1997).
	AP29	Press Release, "Parkervision Supplies JPL with Robotic Cameras, Cameraman Shot Director for Mars Mission," Parkervision Marketing and Manufacturing Headquarters, 2 pages (July 8, 1997).
	AQ29	Press Release, "ParkerVision and IBM Join Forces to Create Wireless Computer Peripherals," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 23, 1997).
	AR29	Press Release, "ParkerVision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 31, 1997).

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	AA30	5,555,453	09/1996	Kajimoto *et al.*			
	AB30	5,557,641	09/1996	Weinberg			
	AC30	5,557,642	09/1996	Williams			
	AD30	5,579,341	11/1996	Smith *et al.*			
	AE30	5,579,347	11/1996	Lindquist *et al.*			
	AF30	5,584,068	12/1996	Mohindra			
	AG30	5,592,131	01/1997	Labreche *et al.*			
	AH30	5,602,847	02/1997	Pagano *et al.*			
	AI30	5,602,868	02/1997	Wilson			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ30						Yes No
	AK30						Yes No
	AL30						Yes No
	AM30						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN30	Press Release, "Parkervision, Inc. Announces Private Placement of 990,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 8, 1997).
	AO30	Press Release, "Wal-Mart Chooses Parkervision for Broadcast Production," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 24, 1997).
	AP30	Press Release, "Parkervision, Inc. Announces Third Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1997).
	AQ30	Press Release, "ParkerVision Announces Breakthrough in Wireless Radio Frequency Technology," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 10, 1997).
	AR30	Press Release, "Parkervision, Inc. Announces the Appointment of Joseph F. Skovron to the Position of Vice President, Licensing - Wireless Technologies," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 9, 1998).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA31	5,604,732	02/1997	Kim *et al.*			
	AB31	5,608,531	03/1997	Honda *et al.*			
	AC31	5,610,946	03/1997	Tanaka *et al.*			
	AD31	RE 35,494	04/1997	Nicollini			
	AE31	5,617,451	04/1997	Mimura *et al.*			
	AF31	5,619,538	04/1997	Sempel *et al.*			
	AG31	5,621,455	04/1997	Rogers *et al.*			
	AH31	5,630,227	05/1997	Bella *et al.*			
	AI31	5,640,415	06/1997	Pandula			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ31						Yes No
	AK31						Yes No
	AL31						Yes No
	AM31						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN31	Press Release, "Parkervision Announces Existing Agreement with IBM Terminates-- Company Continues with Strategic Focus Announced in December," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 27, 1998).
	AO31	Press Release, "Laboratory Tests Verify Parkervision Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 3, 1998).
	AP31	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1998).
	AQ31	Press Release, "Parkervision Awarded Editors' Pick of Show for NAB 98," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1998).
	AR31	Press Release, "Parkervision Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (May 4, 1998).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA32	5,640,424	06/1997	Banavong *et al.*			
	AB32	5,640,428	06/1997	Abe *et al.*			
	AC32	5,640,698	06/1997	Shen *et al.*			
	AD32	5,648,985	07/1997	Bjerede *et al.*			
	AE32	5,650,785	07/1997	Rodal			
	AF32	5,661,424	08/1997	Tang			
	AG32	5,663,878	09/1997	Walker			
	AH32	5,663,986	09/1997	Striffler			
	AI32	5,668,836	09/1997	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ32						Yes No
	AK32						Yes No
	AL32						Yes No
	AM32						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN32	Press Release, "Parkervision 'DIRECT2DATA' Introduced in Response to Market Demand," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 9, 1998).
	AO32	Press Release, "Parkervision Expands Senior Management Team," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 29, 1998).
	AP32	Press Release, "Parkervision Announces Second Quarter and Six Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 4 Pages (July 30, 1998).
	AQ32	Press Release, "Parkervision Announces Third Quarter and Nine Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1998).
	AR32	Press Release, "Questar Infocomm, Inc. Invests $5 Million in Parkervision Common Stock," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 2, 1998).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA33	5,680,078	10/1997	Ariie			
	AB33	5,680,418	10/1997	Croft *et al.*			
	AC33	5,689,413	11/1997	Jaramillo *et al.*			
	AD33	5,699,006	12/1997	Zele *et al.*			
	AE33	5,705,955	01/1998	Freeburg *et al.*			
	AF33	5,710,998	01/1998	Opas			
	AG33	5,714,910	02/1998	Skoczen *et al.*			
	AH33	5,715,281	02/1998	Bly *et al.*			
	AI33	5,721,514	02/1998	Crockett *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ33						Yes No
	AK33						Yes No
	AL33						Yes No
	AM33						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN33	Press Release, "Parkervision Adds Two New Directors," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 5, 1999).
	AO33	Press Release, "Parkervision Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1999).
	AP33	Press Release, "Joint Marketing Agreement Offers New Automated Production Solution," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 13, 1999).
	AQ33	"Project COST 205: Scintillations in Earth-satellite links," *Alta Frequenza: Scientific Review in Electronics*, AEI, Vol. LIV, No. 3, pp. 209-211 (May-June, 1985).
	AR33	Razavi, B., *RF Microelectronics*, Prentice-Hall, pp. 147-149 (1998).

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	AA34	5,724,002	03/1998	Hulick			
	AB34	5,724,653	03/1998	Baker *et al.*			
	AC34	5,729,577	03/1998	Chen			
	AD34	5,729,829	03/1998	Talwar *et al.*			
	AE34	5,732,333	03/1998	Cox *et al.*			
	AF34	5,736,895	04/1998	Yu *et al.*			
	AG34	5,737,035	04/1998	Rotzoll			
	AH34	5,742,189	04/1998	Yoshida *et al.*			
	AI34	5,748,683	05/1998	Smith *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ34						Yes No
	AK34						Yes No
	AL34						Yes No
	AM34						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN34	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 1)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 373, pp. 130-137 (March 1959).
	AO34	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 2)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 374, pp. 204-212 (April 1959).
	AP34	Rein, H.M. and Zahn, M., "Subnanosecond-Pulse Generator with Variable Pulsewidth Using Avalanche Transistors," *Electronics Letters*, IEE, Vol. 11, No. 1, pp. 21-23 (January 9, 1975).
	AQ34	Riad, S.M. and Nahman, N.S., "Modeling of the Feed-through Wideband (DC to 12.4 Ghz) Sampling-Head," *IEEE MTT-S International Microwave Symposium Digest*, IEEE, pp. 267-269 (June 27-29, 1978).
	AR34	Rizzoli, V. *et al.*, "Computer-Aided Noise Analysis of MESFET and HEMT Mixers," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 37, No. 9, pp. 1401-1410 (September 1989).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA35	RE 35,829	06/1998	Sanderford, Jr.			
	AB35	5,760,645	06/1998	Comte *et al.*			
	AC35	5,764,087	06/1998	Clark			
	AD35	5,767,726	06/1998	Wang			
	AE35	5,768,118	06/1998	Faulk *et al.*			
	AF35	5,771,442	06/1998	Wang *et al.*			
	AG35	5,777,692	07/1998	Ghosh			
	AH35	5,777,771	07/1998	Smith			
	AI35	5,786,844	07/1998	Rogers *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ35						Yes No
	AK35						Yes No
	AL35						Yes No
	AM35						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN35	Rowe, H.E., *Signals and Noise in Communication Systems*, D. Van Nostrand Company, Inc., Princeton, New Jersey, including, for example, Chapter V, Pulse Modulation Systems (1965).
	AO35	Rücker, F. and Dintelmann, F., "Effect of Antenna Size on OTS Signal Scintillations and Their Seasonal Dependence," *Electronics Letters*, IEE, Vol. 19, No. 24, pp. 1032-1034 (November 24, 1983).
	AP35	Russell, R. and Hoare, L., "Millimeter Wave Phase Locked Oscillators," *Military Microwaves '78 Conference Proceedings*, Microwave Exhibitions and Publishers, pp. 238-242 (October 25-27, 1978).
	AQ35	Sabel, L.P., "A DSP Implementation of a Robust Flexible Receiver/Demultiplexer for Broadcast Data Satellite Communications," *The Institution of Engineers Australia Communications Conference*, Institution of Engineers, Australia, pp. 218-223 (October 16-18, 1990).
	AR35	Salous, S., "IF digital generation of FMCW waveforms for wideband channel characterization," *IEE Proceedings-I*, IEE, Vol. 139, No. 3, pp. 281-288 (June 1992).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA36	5,793,801	08/1998	Fertner			
	AB36	5,793,818	08/1998	Claydon *et al.*			
	AC36	5,802,463	09/1998	Zuckerman			
	AD36	5,809,060	09/1998	Cafarella *et al.*			
	AE36	5,818,582	10/1998	Fernandez *et al.*			
	AF36	5,825,254	10/1998	Lee			
	AG36	5,834,985	11/1998	Sundegård			
	AH36	5,864,754	01/1999	Hotto			
	AI36	5,881,375	03/1999	Bonds			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ36						Yes No
	AK36						Yes No
	AL36						Yes No
	AM36						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN36	"Sampling Loops Lock Sources to 23 Ghz," *Microwaves & RF*, Penton Publishing, p. 212 (September 1990).
	AO36	Sasikumar, M. *et al.*, "Active Compensation in the Switched-Capacitor Biquad," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 1008-1009 (August 1983).
	AP36	Saul, P.H., "A GaAs MESFET Sample and Hold Switch," *Fifth European Solid State Circuits Conference-ESSCIRC 79*, IEE, pp. 5-7 (1979).
	AQ36	Shen, D.H. *et al.*, "A 900-MHZ RF Front-End with Integrated Discrete-Time Filtering," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Council, Vol. 31, No. 12, pp. 1945-1954 (December 1996).
	AR36	Shen, X.D. and Vilar, E., "Anomalous transhorizon propagation and meteorological processes of a multilink path," *Radio Science*, American Geophysical Union, Vol. 30, No. 5, pp. 1467-1479 (September-October 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA37	5,892,380	04/1999	Quist			
	AB37	5,894,239	04/1999	Bonaccio *et al.*			
	AC37	5,896,562	04/1999	Heinonen			
	AD37	5,900,747	05/1999	Brauns			
	AE37	5,901,054	05/1999	Leu *et al.*			
	AF37	5,901,187	05/1999	Iinuma			
	AG37	5,901,344	05/1999	Opas			
	AH37	5,901,347	05/1999	Chambers *et al.*			
	AI37	5,901,348	05/1999	Bang *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ37						Yes No
	AK37						Yes No
	AL37						Yes No
	AM37						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN37	Shen, X. and Tawfik, A.N., "Dynamic Behaviour of Radio Channels Due to Trans-Horizon Propagation Mechanisms," *Electronics Letters*, IEE, Vol. 29, No. 17, pp. 1582-1583 (August 19, 1993).
	AO37	Shen, X. *et al.*, "Modeling Enhanced Spherical Diffraction and Troposcattering on a Transhorizon Path with aid of the parabolic Equation and Ray Tracing Methods," *IEE Colloquium on Common modeling techniques for electromagnetic wave and acoustic wave propagation*, IEE, pp. 4/1-4/7 (March 8, 1996).
	AP37	Shen, X. and Vilar, E., "Path loss statistics and mechanisms of transhorizon propagation over a sea path," *Electronics Letters*, IEE, Vol. 32, No. 3, pp. 259-261 (February 1, 1996).
	AQ37	Shen, D. *et al.*, "A 900 MHZ Integrated Discrete-Time Filtering RF Front-End," *IEEE International Solid State Circuits Conference*, IEEE, Vol. 39, pp. 54-55 and 417 (February 1996).
	AR37	Spillard, C. *et al.*, "X-Band Tropospheric Transhorizon Propagation Under Differing Meteorological Conditions," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 451-455 (April 4-7, 1989).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA38	5,901,349	05/1999	Guegnaud *et al.*			
	AB38	5,903,178	05/1999	Miyatsuji *et al.*			
	AC38	5,903,187	05/1999	Claverie *et al.*			
	AD38	5,903,196	05/1999	Salvi *et al.*			
	AE38	5,903,421	05/1999	Furutani *et al.*			
	AF38	5,903,553	05/1999	Sakamoto *et al.*			
	AG38	5,903,595	05/1999	Suzuki			
	AH38	5,903,609	05/1999	Kool *et al.*			
	AI38	5,903,827	05/1999	Kennan *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ38						Yes No
	AK38						Yes No
	AL38						Yes No
	AM38						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN38	Stafford, K.R. *et al.*, "A Complete Monolithic Sample/Hold Amplifier," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-9, No. 6, pp. 381-387 (December 1974).
	AO38	Staruk, W. Jr. *et al.*, "Pushing HF Data Rates," *Defense Electronics*, EW Communications, Vol. 17, No. 5, pp. 211, 213, 215, 217, 220 and 222 (May 1985).
	AP38	Stephenson, A.G., "Digitizing multiple RF signals requires an optimum sampling rate," *Electronics*, McGraw-Hill, pp. 106-110 (March 27, 1972).
	AQ38	Sugarman, R., "Sampling Oscilloscope for Statistically Varying Pulses," *The Review of Scientific Instruments*, American Institute of Physics, Vol. 28, No. 11, pp. 933-938 (November 1957).
	AR38	Sylvain, M., "Experimental probing of multipath microwave channels," *Radio Science*, American Geophysical Union, Vol. 24, No. 2, pp. 160-178 (March-April 1989).

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	AA39	5,903,854	05/1999	Abe *et al.*			
	AB39	5,905,449	05/1999	Tsubouchi *et al.*			
	AC39	5,907,149	05/1999	Marckini			
	AD39	5,907,197	05/1999	Faulk			
	AE39	5,911,116	06/1999	Nosswitz			
	AF39	5,911,123	06/1999	Shaffer *et al.*			
	AG39	5,914,622	06/1999	Inoue			
	AH39	5,920,199	07/1999	Sauer			
	AI39	5,943,370	08/1999	Smith			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ39						Yes No
	AK39						Yes No
	AL39						Yes No
	AM39						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN39	Takano, T., "NOVEL GaAs Pet Phase Detector Operable To Ka Band," *IEEE MT-S Digest*, IEEE, pp. 381-383 (1984).
	AO39	Tan, M.A., "Biquadratic Transconductance Switched-Capacitor Filters," *IEEE Transactions on Circuits and Systems- I: Fundamental Theory and Applications*, IEEE Circuits and Systems Society, Vol. 40, No. 4, pp. 272-275 (April 1993).
	AP39	Tanaka, K. *et al.*, "Single Chip Multisystem AM Stereo Decoder IC," *IEEE Transactions on Consumer Electronics*, IEEE Consumer Electronics Society, Vol. CE-32, No. 3, pp. 482-496 (August 1986).
	AQ39	Tawfik, A.N., "Amplitude, Duration and Predictability of Long Hop Trans-Horizon X-band Signals Over the Sea," *Electronics Letters*, IEE, Vol. 28, No. 6, pp. 571-572 (March 12, 1992).
	AR39	Tawfik, A.N. and Vilar, E., "Correlation of Transhorizon Signal Level Strength with Localized Surface Meteorological Parameters," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 335-339 (March 30- April 2, 1993).

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	AA40	4,017,798	04/1977	Gordy *et al.*			
	AB40	4,032,847	06/1977	Unkauf			
	AC40	4,253,067	02/1981	Caples *et al.*			
	AD40	4,393,395	07/1983	Hacke *et al.*			
	AE40	4,816,704	03/1989	Fiori, Jr.			
	AF40	4,841,265	06/1989	Watanabe *et al.*			
	AG40	4,943,974	07/1990	Motamedi			
	AH40	5,115,409	05/1992	Stepp			
	AI40	5,353,306	10/1994	Yamamoto			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ40						Yes No
	AK40						Yes No
	AL40						Yes No
	AM40						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN40	Tawfik, A.N. and Vilar, E., "Dynamic Structure of a Transhorizon Signal at X-band Over a Sea Path," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 446-450 (April 4-7, 1989).
	AO40	Tawfik, A.N. and Vilar, E., "Statistics of Duration and Intensity of Path Loss in a Microwave Transhorizon Sea-Path," *Electronics Letters*, IEE, Vol. 26, No. 7, pp. 474-476 (March 29, 1990).
	AP40	Tawfik, A.N. and Vilar, E., "X-Band Transhorizon Measurements of CW Transmissions Over the Sea- Part 1: Path Loss, Duration of Events, and Their Modeling," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 41, No. 11, pp. 1491-1500 (November 1993).
	AQ40	Temes, G.C. and Tsividis, T., "The Special Section on Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 915-916 (August 1983).
	AR40	Thomas, G.B., *Calculus and Analytic Geometry*, Third Edition, Addison-Wesley Publishing, pp. 119-133 (1960).

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	AA41	5,515,014	05/1996	Troutman			
	AB41	5,563,550	10/1996	Toth			
	AC41	5,574,755	11/1996	Persico			
	AD41	5,604,592	02/1997	Kotidis *et al.*			
	AE41	5,638,396	06/1997	Klimek			
	AF41	5,675,392	10/1997	Nayebi *et al.*			
	AG41	5,694,096	12/1997	Ushiroku *et al.*			
	AH41	5,757,870	05/1998	Miya *et al.*			
	AI41	5,768,323	06/1998	Kroeger *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ41						Yes No
	AK41						Yes No
	AL41						Yes No
	AM41						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN41	Tomassetti, Q., "An Unusual Microwave Mixer," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 754-759 (September 8-12, 1986).
	AO41	Tortoli, P. *et al.*, "Bidirectional Doppler Signal Analysis Based on a Single RF Sampling Channel," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, Vol. 41, No. 1, pp. 1-3 (January 1984).
	AP41	Tsividis, Y. and Antognetti, P. (Ed.), *Design of MOS VLSI Circuits for Telecommunications*, Prentice-Hall, p. 304 (1985).
	AQ41	Tsividis, Y., "Principles of Operation and Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 926-940 (August 1983).
	AR41	Tsurumi, H. and Maeda, T., "Design Study on a Direct Conversion Receiver Front-End for 280 MHZ, 900 MHZ, and 2.6 Ghz Band Radio Communication Systems," *41st IEEE Vehicular Technology Conference*, IEEE Vehicular Technology Society, pp. 457-462 (May 19-22, 1991).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA42	5,770,985	06/1998	Ushiroku *et al.*			
	AB42	5,778,022	07/1998	Walley			
	AC42	5,812,546	09/1998	Zhou *et al.*			
	AD42	5,818,869	10/1998	Miya *et al.*			
	AE42	5,844,449	12/1998	Abeno *et al.*			
	AF42	5,872,446	02/1999	Cranford, Jr. *et al.*			
	AG42	5,909,447	06/1999	Cox *et al.*			
	AH42	5,933,467	08/1999	Sehier *et al.*			
	AI42	5,952,895	09/1999	McCune, Jr. *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ42						Yes No
	AK42						Yes No
	AL42						Yes No
	AM42						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN42	Valdmanis, J.A. *et al.*, "Picosecond and Subpicosend Optoelectronics for Measurements of Future High Speed Electronic Devices," *IEDM Technical Digest*, IEEE, pp. 597-600 (December 5-7, 1983).
	AO42	van de Kamp, M.M.J.L., "Asymmetric signal level distribution due to tropospheric scintillation," *Electronics Letters*, IEE, Vol. 34, No. 11, pp. 1145-1146 (May 28, 1998).
	AP42	Vasseur, H. and Vanhoenacker, D., "Characterization of tropospheric turbulent layers from radiosonde data," *Electronics Letters*, IEE, Vol. 34, No. 4, pp. 318-319 (February 19, 1998).
	AQ42	Verdone, R., "Outage Probability Analysis for Short-Range Communication Systems at 60 Ghz in ATT Urban Environments," *IEEE Transactions on Vehicular Technology*, IEEE Vehicular Technology Society, Vol. 46, No. 4, pp. 1027-1039 (November 1997).
	AR42	Vierira-Ribeiro, S.A., *Single-IF DECT Receiver Architecture using a Quadrature Sub-Sampling Band-Pass Sigma-Delta Modulator*, Thesis for Degree of Master's of Engineering, Carleton University, UMI Dissertation Services, pp. 1-180 (April 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA43	5,960,033	09/1999	Shibano *et al.*			
	AB43	6,041,073	03/2000	Davidovici *et al.*			
	AC43	6,054,889	04/2000	Kobayashi			
	AD43	6,084,922	07/2000	Zhou *et al.*			
	AE43	6,125,271	09/2000	Rowland *et al.*			
	AF43	6,147,340	11/2000	Levy			
	AG43	6,147,763	11/2000	Steinlechner			
	AH43	6,150,890	11/2000	Damgaard *et al.*			
	AI43	5,126,682	06/1992	Weinberg *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ43						Yes No
	AK43						Yes No
	AL43						Yes No
	AM43						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN43	Vilar, E. *et al.*, "A Comprehensive/Selective MM-Wave Satellite Downlink Experiment on Fade Dynamics," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.98-2.101 (April 14-17, 1997).
	AO43	Vilar, E. *et al.*, "A System to Measure LOS Atmospheric Transmittance at 19 Ghz," *AGARD Conference Proceedings No. 346: Characteristics of the Lower Atmosphere Influencing Radio Wave Propagation*, AGARD, pp. 8-1 - 8-16 (October 4-7, 1983).
	AP43	Vilar, E. and Smith, H., "A Theoretical and Experimental Study of Angular Scintillations in Earth Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 1, pp. 2-10 (January 1986).
	AQ43	Vilar, E. *et al.*, "A Wide Band Transhorizon Experiment at 11.6 Ghz," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 441-445 (March 30- April 2, 1993).
	AR43	Vilar, E. and Matthews, P.A., "Amplitude Dependence of Frequency in Oscillators," *Electronics Letters*, IEE, Vol. 8, No. 20, pp. 509-511 (October 5, 1972).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA44	5,841,811	11/1998	Song			
	AB44	4,051,475	09/1977	Campbell			
	AC44	5,953,642	09/1999	Feldtkeller *et al.*			
	AD44	4,653,117	03/1987	Heck			
	AE44	5,859,878	01/1999	Phillips *et al.*			
	AF44	5,894,496	04/1999	Jones			
	AG44	5,915,278	06/1999	Mallick			
	AH44	6,028,887	02/2000	Harrison *et al.*			
	AI44	6,081,691	06/2000	Renard *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ44						Yes No
	AK44						Yes No
	AL44						Yes No
	AM44						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN44	Vilar, E. *et al.*, "An experimental mm-wave receiver system for measuring phase noise due to atmospheric turbulence," *Proceedings of the 25th European Microwave Conference*, Nexus House, pp. 114-119 (1995).
	AO44	Vilar, E. and Burgueño, A., "Analysis and Modeling of Time Intervals Between Rain Rate Exceedances in the Context of Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 39, No. 9, pp. 1306-1312 (September 1991).
	AP44	Vilar, E. *et al.*, "Angle of Arrival Fluctuations in High and Low Elevation Earth Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, Electronics Division of the IEE, pp. 83-88 (April 16-19, 1985).
	AQ44	Vilar, E., "Antennas and Propagation: A Telecommunications Systems Subject," *Electronics Division Colloquium on Teaching Antennas and Propagation to Undergraduates,* IEE, pp. 7/1-7/6 (March 8, 1988).
	AR44	Vilar, E. *et al.*, "CERS*. Millimetre-Wave Beacon Package and Related Payload Doppler Correction Strategies," *Electronics Division Colloquium on CERS- Communications Engineering Research Satellite*, IEE, pp. 10/1-10/10 (April 10, 1984).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA45	6,121,819	09/2000	Traylor			
	AB45	6,144,236	11/2000	Vice *et al.*			
	AC45	6,144,846	11/2000	Durec			
	AD45	6,175,728 B1	01/2001	Mitama			
	AE45	5,705,949	01/1998	Alelyunas *et al.*			
	AF45	5,883,548	03/1999	Assard *et al.*			
	AG45	4,484,143	11/1984	French *et al.*			
	AH45	5,841,324	11/1998	Williams			
	AI45	4,855,894	08/1989	Asahi *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ45						Yes No
	AK45						Yes No
	AL45						Yes No
	AM45						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN45	Vilar, E. and Moulsley, T.J., "Comment and Reply: Probability Density Function of Amplitude Scintillations," *Electronics Letters*, IEE, Vol. 21, No. 14, pp. 620-622 (July 4, 1985).
	AO45	Vilar, E. *et al.*, "Comparison of Rainfall Rate Duration Distributions for ILE-IFE and Barcelona," *Electronics Letters*, IEE, Vol. 28, No. 20, pp. 1922-1924 (September 24, 1992).
	AP45	Vilar, E., "Depolarization and Field Transmittances in Indoor Communications," *Electronics Letters*, IEE, Vol. 27, No. 9, pp. 732-733 (April 25, 1991).
	AQ45	Vilar, E. and Larsen, J.R., "Elevation Dependence of Amplitude Scintillations on Low Elevation Earth Space Paths," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 150-154 (April 4-7, 1989).
	AR45	Vilar, E. *et al.*, "Experimental System and Measurements of Transhorizon Signal Levels at 11 Ghz," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 429-435 (September 12 - 15, 1988).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA46	5,319,799	06/1994	Morita			
	AB46	5,801,654	09/1998	Traylor			
	AC46	5,369,404	11/1994	Galton			
	AD46	3,716,730	02/1973	Cerny, Jr.			
	AE46	4,080,573	03/1978	Howell			
	AF46	4,334,324	06/1982	Hoover			
	AG46	4,369,522	01/1983	Cerny, Jr. *et al.*			
	AH46	5,465,418	11/1995	Zhou *et al.*			
	AI46	5,513,389	04/1996	Reeser *et al.*			

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	AJ46						Yes No
	AK46						Yes No
	AL46						Yes No
	AM46						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN46	Vilar, E. and Matthews, P.A., "Importance of Amplitude Scintillations in Millimetric Radio Links," *Proceedings of the 4th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 202-206 (September 10-13, 1974).
	AO46	Vilar, E. and Haddon, J., "Measurement and Modeling of Scintillation Intensity to Estimate Turbulence Parameters in an Earth-Space Path," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. AP-32, No. 4, pp. 340-346 (April 1984).
	AP46	Vilar, E. and Matthews, P.A., "Measurement of Phase Fluctuations on Millimetric Radiowave Propagation," *Electronics Letters*, IEE, Vol. 7, No. 18, pp. 566-568 (September 9, 1971).
	AQ46	Vilar, E. and Wan, K.W., "Narrow and Wide Band Estimates of Field Strength for Indoor Communications in the Millimetre Band," *Electronics Division Colloquium on Radiocommunications in the Range 30-60 Ghz*, IEE, pp. 5/1-5/8 (January 17, 1991).
	AR46	Vilar, E. and Faulkner, N.D., "Phase Noise and Frequency Stability Measurements. Numerical Techniques and Limitations," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizer,* IEE, 5 pages (January 23, 1986).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA47	5,959,850	09/1999	Lim			
	AB47	5,157,687	10/1992	Tymes			
	AC47	5,945,660	08/1999	Nakasuji *et al.*			
	AD47	6,091,939	07/2000	Banh			
	AE47	6,091,941	07/2000	Moriyama *et al.*			
	AF47	6,098,886	08/2000	Swift *et al.*			
	AG47	6,215,475 B1	04/2001	Meyerson *et al.*			
	AH47	6,049,706	04/2000	Cook *et al.*			
	AI47	6,061,551	05/2000	Sorrells *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ47						Yes No
	AK47						Yes No
	AL47						Yes No
	AM47						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN47	Vilar, E. and Senin, S., "Propagation phase noise identified using 40 Ghz satellite downlink," *Electronics Letters,* IEE, Vol. 33, No. 22, pp. 1901-1902 (October 23, 1997).
	AO47	Vilar, E. *et al.*, "Scattering and Extinction: Dependence Upon Raindrop Size Distribution in Temperate (Barcelona) and Tropical (Belem) Regions," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.230-2.233 (April 14-17, 1997).
	AP47	Vilar, E. and Haddon, J., "Scintillation Modeling and Measurement - A Tool for Remote-Sensing Slant Paths," *AGARD Conference Proceedings No. 332: Propagation Aspects of Frequency Sharing, Interference And System Diversity*, AGARD, pp. 27-1 - 27-13 (October 18-22, 1982).
	AQ47	Vilar, E., "Some Limitations on Digital Transmission Through Turbulent Atmosphere," *International Conference on Satellite Communication Systems Technology,* Electronics Division of the IEE, pp. 169-187 (April 7-10, 1975).
	AR47	Vilar, E. and Matthews, P.A., "Summary of Scintillation Observations in a 36 Ghz Link Across London," *International Conference on Antennas and Propagation Part 2: Propagation,* IEE, pp. 36-40 (November 28-30, 1978).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA48	6,061,555	05/2000	Bultman *et al.*			
	AB48	6,091,940	07/2000	Sorrells *et al.*			
	AC48	6,266,518 B1	07/2001	Sorrells *et al.*			
	AD48	6,353,735 B1	03/2002	Sorrells *et al.*			
	AE48	6,370,371 B1	04/2002	Sorrells *et al.*			
	AF48	5,628,055	05/1997	Stein			
	AG48	5,678,220	10/1997	Fournier			
	AH48	5,926,065	07/1999	Wakai *et al.*			
	AI48	3,622,885	11/1971	Oberdorf *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ48						Yes No
	AK48						Yes No
	AL48						Yes No
	AM48						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN48	Vilar, E. *et al.*, "Wideband Characterization of Scattering Channels," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.353-2.358 (April 14-17, 1997).
	AO48	Vollmer, A., "Complete GPS Receiver Fits on Two Chips," *Electronic Design*, Penton Publishing, pp. 50, 52, 54 and 56 (July 6, 1998).
	AP48	*Voltage and Time Resolution in Digitizing Oscilloscopes: Application Note 348*, Hewlett Packard, pp. 1-11 (November 1986).
	AQ48	Wan, K.W. *et al.*, "A Novel Approach to the Simultaneous Measurement of Phase and Amplitude Noises in Oscillator," *Proceedings of the 19th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 809-813 (September 4-7, 1989).
	AR48	Wan, K.W. *et al.*, "Extended Variances and Autoregressive/Moving Average Algorithm for the Measurement and Synthesis of Oscillator Phase Noise," *Proceedings Of the 43rd Annual Symposium on Frequency Control*, IEEE, pp. 331-335 (1989).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA49	4,483,017	11/1984	Hampel *et al.*			
	AB49	6,421,534 B1	07/2002	Cook *et al.*			
	AC49	6,330,244 B1	12/2001	Swartz *et al.*			
	AD49	4,384,357	05/1983	deBuda *et al.*			
	AE49	4,470,145	09/1984	Williams			
	AF49	5,600,680	02/1997	Mishima *et al.*			
	AG49	5,606,731	02/1997	Pace *et al.*			
	AH49	5,870,670	02/1999	Ripley *et al.*			
	AI49	6,314,279 B1	11/2001	Mohindra			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ49						Yes No
	AK49						Yes No
	AL49						Yes No
	AM49						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN49	Wan, K.W. *et al.*, "Wideband Transhorizon Channel Sounder at 11 Ghz," *Electronics Division Colloquium on High Bit Rate UHF/SHF Channel Sounders - Technology and Measurement*, IEE, pp. 3/1-3/5 (December 3, 1993).
	AO49	Wang, H., "A 1-V Multigigahertz RF Mixer Core in 0.5 - μm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Society, Vol. 33, No. 12, pp. 2265-2267 (December 1998).
	AP49	Watson, A.W.D. *et al.*, "Digital Conversion and Signal Processing for High Performance Communications Receivers," *Digital Processing of Signals in Communications*, Institution of Electronic and Radio Engineers, pp. 367-373 (April 22nd -26th, 1985).
	AQ49	Weast, R.C. *et al.* (Ed.), *Handbook of Mathematical Tables*, Second Edition, The Chemical Rubber Co., pp. 480-485 (1964).
	AR49	Wiley, R.G., "Approximate FM Demodulation Using Zero Crossings," *IEEE Transactions on Communications*, IEEE, Vol. COM-29, No. 7, pp. 1061-1065 (July 1981).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA50	5,633,815	05/1997	Young			
	AB50	3,246,084	04/1966	Kryter			
	AC50	3,702,440	11/1972	Moore			
	AD50	3,767,984	10/1973	Shinoda *et al.*			
	AE50	3,852,530	12/1974	Shen			
	AF50	4,220,977	09/1980	Yamanaka			
	AG50	5,016,242	05/1991	Tang			
	AH50	5,937,013	08/1999	Lam *et al.*			
	AI50	6,014,551	01/2000	Pesola *et al.*			

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	AJ50						Yes No
	AK50						Yes No
	AL50						Yes No
	AM50						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN50	Worthman, W., "Convergence... Again," *RF Design*, Primedia, p. 102 (March 1999).
	AO50	Young, I.A. and Hodges, D.A., "MOS Switched-Capacitor Analog Sampled-Data Direct-Form Recursive Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-14, No. 6, pp. 1020-1033 (December 1979).
	AP50	Translation of Specification and Claims of FR Patent No. 2245130, 3 pages (April 18, 1975- Date of publication of application).
	AQ50	Fest, Jean-Pierre, "Le Convertisseur A/N Revolutionne Le Recepteur Radio," *Electronique*, JMJ (Publisher), No. 54, pp. 40-42 (December 1995).
	AR50	Translation of DE Patent No. 35 41 031 A1, 22 pages (May 22, 1986- Date of publication of application).

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA51	6,073,001	06/2000	Sokoler			
	AB51	6,085,073	07/2000	Palermo *et al.*			
	AC51	6,400,963 B1	06/2002	Glöckler *et al.*			
	AD51	6,230,000 B1	05/2001	Tayloe			
	AE51	5,483,695	01/1996	Pardoen			
	AF51	6,542,722 B1	04/2003	Sorrells *et al.*			
	AG51	6,560,301 B1	05/2003	Cook *et al.*			
	AH51	6,098,046	08/2000	Cooper *et al.*			
	AI51	5,564,097	10/1996	Swanke			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ51						Yes No
	AK51						Yes No
	AL51						Yes No
	AM51						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN51	Translation of EP Patent No. 0 732 803 A1, 9 pages (September 18, 1996- Date of publication of application).
	AO51	Fest, Jean-Pierre, "The A/D Converter Revolutionizes the Radio Receiver," *Electronique*, JMJ (Publisher), No. 54, 3 pages (December 1995). (Translation of Doc. AQ50).
	AP51	Translation of German Patent No. DE 197 35 798 C1, 8 pages (July 16, 1998- Date of publication of application).
	AQ51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-154 (April 30, 1956).
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	FILING DATE October 27, 2004	ART UNIT 2661

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	AA52	5,898,912	04/1999	Heck *et al.*			
	AB52	4,660,164	04/1987	Leibowitz			
	AC52	6,580,902 B1	06/2003	Sorrells *et al.*			
	AD52	4,857,928	08/1989	Gailus *et al.*			
	AE52	5,389,839	02/1995	Heck			
	AF52	5,471,665	11/1995	Pace *et al.*			
	AG52	6,327,313 B1	12/2001	Traylor *et al.*			
	AH52	5,751,154	05/1998	Tsugai			
	AI52	5,793,817	08/1998	Wilson			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ52						Yes No
	AK52						Yes No
	AL52						Yes No
	AM52						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN52	Rabiner, L.R. and Gold, B., *Theory And Application Of Digital Signal Processing*, Prentice-Hall, Inc., pp. v-xii and 40-46 (1975).
	AO52	English-language Abstract of Japanese Patent Publication No. 08-032556, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 2, 1996 - Date of publication of application).
	AP52	English-language Abstract of Japanese Patent Publication No. 08-139524, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (May 31, 1996 - Date of publication of application).
	AQ52	English-language Abstract of Japanese Patent Publication No. 59-144249, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 18, 1984 - Date of publication of application).
	AR52	English-language Abstract of Japanese Patent Publication No. 63-054002, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (March 8, 1988 - Date of publication of application).

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	AA53	6,225,848 B1	05/2001	Tilley *et al.*			
	AB53	6,313,685 B1	11/2001	Rabii			
	AC53	3,614,627	10/1971	Runyan *et al.*			
	AD53	3,940,697	02/1976	Morgan			
	AE53	4,016,366	04/1977	Kurata			
	AF53	4,045,740	08/1977	Baker			
	AG53	4,115,737	09/1978	Hongu *et al.*			
	AH53	5,710,992	01/1998	Sawada *et al.*			
	AI53	5,790,587	08/1998	Smith *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ53						Yes No
	AK53						Yes No
	AL53						Yes No
	AM53						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN53	English-language Abstract of Japanese Patent Publication No. 06-237276, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 23, 1994 - Date of publication of application).
	AO53	English-language Abstract of Japanese Patent Publication No. 08-023359, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (January 23, 1996 - Date of publication of application).
	AP53	Translation of Japanese Patent Publication No. 47-2314, 7 pages (February 4, 1972- Date of publication of application).
	AQ53	Partial Translation of Japanese Patent Publication No. 58-7903, 3 pages (January 17, 1983- Date of publication of application).
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	AB54	5,483,600	01/1996	Werrbach			
	AC54	6,011,435	01/2000	Takeyabu *et al.*			
	AD54	6,321,073 B1	11/2001	Luz *et al.*			
	AE54	6,026,286	02/2000	Long			
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	AH54	3,736,513	05/1973	Wilson			
	AI54	4,488,119	12/1984	Marshall			

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	AJ54						Yes No
	AK54						Yes No
	AL54						Yes No
	AM54						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN54	English-language Abstract of Japanese Patent Publication No. 60-058705, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 4, 1985 - Date of publication of application).
	AO54	English-language Abstract of Japanese Patent Publication No. 04-123614, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 23, 1992 - Date of publication of application).
	AP54	English-language Abstract of Japanese Patent Publication No. 04-127601, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 28, 1992 - Date of publication of application).
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	AC55	5,416,449	05/1995	Joshi			
	AD55	5,438,329	08/1995	Gastouniotis *et al.*			
	AE55	6,611,569 B1	08/2003	Schier *et al.*			
	AF55	6,647,250 B1	11/2003	Bultman *et al.*			
	AG55	5,682,099	10/1997	Thompson *et al.*			
	AH55	6,094,084	07/2000	Abou-Allam *et al.*			
	AI55	6,067,329	05/2000	Kato *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ55						Yes No
	AK55						Yes No
	AL55						Yes No
	AM55						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN55	English-language Abstract of Japanese Patent Publication No. 07-154344, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (June 16, 1995 - Date of publication of application).
	AO55	English-language Abstract of Japanese Patent Publication No. 07-307620, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (November 21, 1995 - Date of publication of application).
	AP55	Oppenheim, A.V. and Schafer, R.W., *Digital Signal Processing*, Prentice-Hall, pp. vii-x, 6-35, 45-78, 87-121 and 136-165 (1975).
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	AA56	6,516,185 B1	02/2003	MacNally			
	AB56	6,608,647 B1	08/2003	King			
	AC56	6,687,493 B1	02/2004	Sorrells *et al.*			
	AD56	6,694,128 B1	02/2004	Sorrells *et al.*			
	AE56	6,031,217	02/2000	Aswell *et al.*			
	AF56	5,955,992	09/1999	Shattil			
	AG56	5,999,561	12/1999	Naden *et al.*			
	AH56	6,686,879 B2	02/2004	Shattil			
	AI56	6,704,549 B1	03/2004	Sorrells *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ56						Yes No
	AK56						Yes No
	AL56						Yes No
	AM56						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN56	English-language Abstract of Japanese Patent Publication No. 63-153691, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (June 27, 1988 - Date of publication of application).
	AO56	Translation of Japanese Patent Publication No. 60-130203, 3 pages (July 11, 1985- Date of publication of application).
	AP56	Razavi, B., "A 900-MHz/1.8-Ghz CMOS Transmitter for Dual-Band Applications," *Symposium on VLSI Circuits Digest of Technical Papers*, IEEE, pp. 128-131 (1998).
	AQ56	Ritter, G.M., "SDA, A New Solution for Transceivers," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 729-733 (September 8, 1986).
	AR56	DIALOG File 351 (Derwent WPI) English Language Patent Abstract for FR 2 669 787, 1 page (May 29, 1992- Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA57	6,704,558 B1	03/2004	Sorrells *et al.*			
	AB57	5,490,176	02/1996	Peltier			
	AC57	5,970,053	10/1999	Schick *et al.*			
	AD57	6,078,630	06/2000	Prasanna			
	AE57	6,600,911 B1	07/2003	Morishige *et al.*			
	AF57	5,179,731	01/1993	Tränkle *et al.*			
	AG57	5,589,793	12/1996	Kassapian			
	AH57	4,510,467	04/1985	Chang *et al.*			
	AI57	4,772,853	09/1988	Hart			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ57						Yes No
	AK57						Yes No
	AL57						Yes No
	AM57						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN57	Akos, D.M. *et al.*, "Direct Bandpass Sampling of Multiple Distinct RF Signals," *IEEE Transactions on Communications*, IEEE, Vol. 47, No. 7, pp. 983-988 (July 1999).
	AO57	Patel, M. *et al.*, "Bandpass Sampling for Software Radio Receivers, and the Effect of Oversampling on Aperture Jitter," *VTC 2002*, IEEE, pp. 1901-1905 (2002).
	AP57	English-language Abstract of Japanese Patent Publication No. 61-030821, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 13, 1986- Date of publication of application).
	AQ57	English-language Abstract of Japanese Patent Publication No. 05-327356, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (December 10, 1993 - Date of publication of application).
	AR57	Tayloe, D., "A Low-noise, High-performance Zero IF Quadrature Detector/Preamplifier," *RF Design*, Primedia Business Magazines & Media, Inc., pp. 58, 60, 62 and 69 (March 2003).

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	AA58	4,972,436	11/1990	Halim *et al.*			
	AB58	5,012,245	04/1991	Scott *et al.*			
	AC58	5,422,909	06/1995	Love *et al.*			
	AD58	5,440,311	08/1995	Gallagher *et al.*			
	AE58	5,926,513	07/1999	Suominen *et al.*			
	AF58	5,995,030	11/1999	Cabler			
	AG58	6,047,026	04/2000	Chao *et al.*			
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	AI58	6,076,015	06/2000	Hartley *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ58						Yes No
	AK58						Yes No
	AL58						Yes No
	AM58						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN58	Dines, J.A.B., "Smart Pixel Optoelectronic Receiver Based on a Charge Sensitive Amplifier Design," *IEEE Journal of Selected Topics in Quantum Electronics*, IEEE, Vol. 2, No. 1, pp. 117-120 (April 1996).
	AO58	Simoni, A. *et al.*, "A Digital Camera for Machine Vision," *20th International Conference on Industrial Electronics, Control and Instrumentation*, IEEE, pp. 879-883 (September 1994).
	AP58	Stewart, R.W. and Pfann, E., "Oversampling and sigma-delta strategies for data conversion," *Electronics & Communication Engineering Journal*, IEEE, pp. 37-47 (February 1998).
	AQ58	Rudell, J.C. *et al.*, "A 1.9-Ghz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, pp. 2071-2088 (December 1997).
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	AA59	6,144,331	11/2000	Jiang			
	AB59	6,018,553	01/2000	Sanielevici *et al.*			
	AC59	6,317,589 B1	11/2001	Nash			
	AD59	5,058,107	10/1991	Stone *et al.*			
	AE59	5,757,858	05/1998	Black *et al.*			
	AF59	6,531,979 B1	03/2003	Hynes			
	AG59	6,018,262	01/2000	Noro *et al.*			
	AH59	4,761,798	08/1988	Griswold, Jr. *et al.*			
	AI59	5,982,315	11/1999	Bazarjani *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ59						Yes No
	AK59						Yes No
	AL59						Yes No
	AM59						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN59	Simoni, A. *et al.*, "A Single-Chip Optical Sensor with Analog Memory for Motion Detection," *IEEE Journal of Solid-State Circtuits*, IEEE, Vol. 30, No. 7, pp. 800-806 (July 1995).
	AO59	English Translation of German Patent Publication No. DE 196 48 915 A1, 10 pages.
	AP59	Deboo, Gordon J., *Integrated Circuits and Semiconductor Devices*, 2nd Edition, McGraw-Hill, Inc., pp. 41-45 (1977).
	AQ59	Hellwarth, G.A. and Jones, G.D, "Automatic Conditioning of Speech Signals," *IEEE Transactions on Audio and Electroacoustics*, Vol. AU-16, No. 2, pp. 169-179 (June 1968).
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	AA60	6,459,721 B1	10/2002	Mochizuki *et al.*			
	AB60	6,151,354	11/2000	Abbey			
	AC60	6,169,733 B1	01/2001	Lee			
	AD60	6,363,262 B1	03/2002	McNicol			
	AE60	6,697,603 B1	02/2004	Lovinggood *et al.*			
	AF60	5,282,222	01/1994	Fattouche *et al.*			
	AG60	5,949,827	09/1999	DeLuca *et al.*			
	AH60	6,014,176	01/2000	Nayebi *et al.*			
	AI60	5,678,226	10/1997	Li *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ60						Yes No
	AK60						Yes No
	AL60						Yes No
	AM60						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN60	
	AO60	
	AP60	
	AQ60	
	AR60	

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	AB61	6,160,280	12/2000	Bonn *et al.*			
	AC61	5,481,570	01/1996	Winters			
	AD61	5,745,846	04/1998	Myer *et al.*			
	AE61	5,345,239	09/1994	Madni *et al.*			
	AF61	4,132,952	01/1979	Hongu *et al.*			
	AG61	5,260,973	11/1993	Watanabe			
	AH61	6,307,894 B2	10/2001	Eidson *et al.*			
	AI61	6,091,289	07/2000	Song *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ61						Yes No
	AK61						Yes No
	AL61						Yes No
	AM61						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN61	
	AO61	
	AP61	
	AQ61	
	AR61	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA62	6,437,639 B1	08/2002	Nguyen *et al.*			
	AB62	2002/0037706 A1	03/2002	Ichihara			
	AC62	4,441,080	04/1984	Saari			
	AD62	4,873,492	10/1989	Myer			
	AE62	5,697,074	12/1997	Makikallio *et al.*			
	AF62	5,784,689	07/1998	Kobayashi			
	AG62	6,335,656 B1	01/2002	Goldfarb *et al.*			
	AH62	6,690,232 B2	02/2004	Ueno *et al.*			
	AI62	5,636,140	06/1997	Lee *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ62						Yes No
	AK62						Yes No
	AL62						Yes No
	AM62						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN62	
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	AR62	

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA63	6,366,622 B1	04/2002	Brown *et al.*			
	AB63	6,600,795 B1	07/2003	Ohta *et al.*			
	AC63	4,250,458	02/1981	Richmond *et al.*			
	AD63	5,760,629	06/1998	Urabe *et al.*			
	AE63	6,084,465	07/2000	Dasqupta			
	AF63	6,204,789 B1	03/2001	Nagata			
	AG63	6,064,054	05/2000	Waczynski *et al.*			
	AH63	5,218,562	06/1993	Basehore *et al.*			
	AI63	5,239,496	08/1993	Vancraeynest			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ63						Yes No
	AK63						Yes No
	AL63						Yes No
	AM63						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
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	AR63	

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA64	5,896,304	04/1999	Tiemann *et al.*			
	AB64	6,005,903	12/1999	Mendelovicz			
	AC64	5,834,979	11/1998	Yatsuka			
	AD64	6,798,351 B1	09/2004	Sorrells *et al.*			
	AE64	6,813,485 B2	11/2004	Sorrells *et al.*			
	AF64	5,410,270	04/1995	Rybicki *et al.*			
	AG64	6,509,777 B2	01/2003	Razavi *et al.*			
	AH64	5,982,329	11/1999	Pittman *et al.*			
	AI64	6,208,636 B1	03/2001	Tawil *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ64						Yes No
	AK64						Yes No
	AL64						Yes No
	AM64						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA65	3,614,630	10/1971	Rorden			
	AB65	6,836,650 B2	12/2004	Sorrells *et al.*			
	AC65	5,844,868	12/1998	Takahashi *et al.*			
	AD65	6,385,439 B1	05/2002	Hellberg			
	AE65	6,741,139 B2	05/2004	Pleasant *et al.*			
	AF65	6,823,178 B2	11/2004	Pleasant *et al.*			
	AG65	6,850,742 B2	02/2005	Fayyaz			
	AH65	6,853,690 B1	02/2005	Sorrells *et al.*			
	AI65	4,789,837	12/1988	Ridgers			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ65						Yes No
	AK65						Yes No
	AL65						Yes No
	AM65						Yes No

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA66	5,634,207	05/1997	Yamaji *et al.*			
	AB66	5,642,071	06/1997	Sevenhans *et al.*			
	AC66	6,211,718 B1	04/2001	Souetinov			
	AD66	6,212,369 B1	04/2001	Avasarala			
	AE66	6,308,058 B1	10/2001	Souetinov *et al.*			
	AF66	6,633,194 B2	10/2003	Arnborg *et al.*			
	AG66	2001/0036818 A1	11/2001	Dobrovolny			
	AH66	6,873,836 B1	03/2005	Sorrells *et al.*			
	AI66	6,879,817 B1	04/2005	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ66						Yes No
	AK66						Yes No
	AL66						Yes No
	AM66						Yes No

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419797_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA67	6,057,714	05/2000	Andrys *et al.*			
	AB67	2003/0081781 A1	05/2003	Jensen *et al.*			
	AC67	5,994,689	11/1999	Charrier			
	AD67	6,512,544 B1	01/2003	Merrill *et al.*			
	AE67	6,628,328 B1	09/2003	Yokouchi *et al.*			
	AF67	6,801,253 B1	10/2004	Yonemoto *et al.*			
	AG67						
	AH67						
	AI67						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ67						Yes No
	AK67						Yes No
	AL67						Yes No
	AM67						Yes No

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Marvin C. Guthrie

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+Admitted only in Virginia
•Practice Limited to Federal Agencies

September 25, 2006

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INTERNET ADDRESS:
MLEE@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2616

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Fourth Supplemental Information Disclosure Statement;

2. A listing of the cited documents on Form PTO-1449 (*3 pages*);

3. Copies of the cited documents (AM25, AJ26, AK26, AQ61, AR61, AN62); and

4. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/JSW:apg
Enclosures

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

OIPE IAP48
SEP 25 2006
PATENT & TRADEMARK OFFICE

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
SORRELLS *et al.*
Appl. No.: 10/973,917
Filed: October 27, 2004
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**

Confirmation No.: 3273
Art Unit: 2616
Examiner: Chin, Wellington
Atty. Docket: 1744.0330003

Fourth Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Fourth Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Third Supplemental Information Disclosure Statement filed on June 6, 2006 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Applicants provide the following comments regarding the documents:

Documents AM25, AJ26, and AK26 were cited in an Office Action in related Japanese Patent Application No. 2002-048676, filed October 18, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter. Also cited in said Office Action was Japanese Patent Publication No. 60-130203, which has already been cited in the present application.

Documents AB75-AD75 and AC77-AG77 are co-owned patents which are directed to related subject matter.

Document AE75 was cited in an Office Action in related U.S. Patent Application No. 10/197,253, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter.

Document AF75 was cited in an Office Action in related U.S. Patent Application No. 09/550,644, filed April 14, 2000, entitled "Method and System for Down-Converting an Electromagnetic Signal, Transforms for Same, and Aperture Relationships," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,404,758, which has already been cited in the present application.

Documents AG75-AI75 and AA76 were cited in an Office Action in related U.S. Patent Application No. 11/107,861, filed April 18, 2005, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Documents AB76-AF76 were cited in an Office Action in related U.S. Patent Application No. 11/230,732, filed September 21, 2005, entitled "Applications of Universal Frequency Translation," directed to related subject matter. Also cited in said Office Action

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

were U.S. Patent Nos. 6,208,636 and 7,016,663, which have already been cited in the present application.

Documents AG76-AI76, AA77, and AB77 were cited in a Notice of Allowance in related U.S. Patent Application No. 10/961,253, filed October 12, 2004, entitled "Apparatus, System, and Method for Down Converting and Up Converting Electromagnetic Signals," directed to related subject matter. Also cited in said Notice of Allowance was U.S. Patent No. 6,404,823, which has already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Document AM25 (JP 61-232706) appears to describe a frequency converter for signals. An English language abstract of document AM25 is enclosed as document AQ61.

Document AJ26 (JP 9-171399) appears to describe a sound synthesizing method and circuit. An English language abstract of document AJ26 is enclosed as document AR61.

Document AK26 (JP 10-41860) appears to describe an echo canceller. An English language abstract of document AK26 is enclosed as document AN62.

☒ 7. Copies of documents AM25, AJ26, AK26, AQ61, AR61, and AN62 are enclosed. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent publications cited on the attached Form PTO-1449 are not enclosed.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000 (now abandoned), 09/476,093, filed January 3, 2000 (now U.S. Patent No. 7,006,805), 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817),

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 9/25/06

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

OIPE IAP48
SEP 25 2006
PATENT & TRADEMARK OFFICE

FORM PTO-1449

FOURTH SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB75	7,050,508 B2	05/2006	Sorrells *et al.*			
	AC75	7,054,296 B1	05/2006	Sorrells *et al.*			
	AD75	7,065,162 B1	06/2006	Sorrells *et al.*			
	AE75	2003/0149579 A1	08/2003	Begemann *et al.*			
	AF75	5,063,387	11/1991	Mower			
	AG75	5,535,402	07/1996	Leibowitz *et al.*			
	AH75	6,512,785 B1	01/2003	Zhou *et al.*			
	AI75	6,567,483 B1	05/2003	Dent *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM25	JP 61-232706	10/1986	JP			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ61	English-language Abstract of Japanese Patent Publication No. JP 61-232706, data supplied by the espacenet, 1 page (October 17, 1986 - Date of publication of application).
	AR61	English-language Abstract of Japanese Patent Publication No. JP 9-171399, data supplied by the espacenet, 1 page (June 30, 1997 - Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

575838_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

OIPE IAP48
SEP 25 2006
PATENT & TRADEMARK OFFICE

FORM PTO-1449

FOURTH SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA76	6,775,684 B1	08/2004	Toyoyama *et al.*			
	AB76	4,740,792	04/1988	Sagey *et al.*			
	AC76	5,239,687	08/1993	Chen			
	AD76	5,552,789	09/1996	Schuermann			
	AE76	5,905,433	05/1999	Wortham			
	AF76	6,647,270 B1	11/2003	Himmelstein			
	AG76	6,034,566	03/2000	Ohe			
	AH76	6,313,700 B1	11/2001	Nishijima *et al.*			
	AI76	6,959,178 B2	10/2005	Macedo *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ26	JP 9-171399	06/1997	JP			No
	AK26	JP 10-41860	02/1998	JP			No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN62	English-language Abstract of Japanese Patent Publication No. JP 10-41860, data supplied by the espacenet, 1 page (February 13, 1998 - Date of publication of application).
	AO	
	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

575838_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

OIPE MAP48 SEP 25 2006 PATENT & TRADEMARK OFFICE

FORM PTO-1449

FOURTH SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
October 27, 2004	2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA77	6,999,747 B2	02/2006	Su			
	AB77	2004/0125879 A1	07/2004	Jaussi *et al.*			
	AC77	7,072,390 B1	07/2006	Sorrells *et al.*			
	AD77	7,072,427 B2	07/2006	Rawlins *et al.*			
	AE77	7,076,011 B2	07/2006	Cook *et al.*			
	AF77	7,082,171 B1	07/2006	Johnson *et al.*			
	AG77	7,085,335 B2	08/2006	Rawlins *et al.*			
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

575838_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

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Sterne Kessler Goldstein Fox
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OIPE IAP13 OCT 24 2005 PATENT & TRADEMARK OFFICE

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October 24, 2005

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2662

Attn: Mail Stop Amendment

Re: U.S. Patent Application
Application No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Supplemental Information Disclosure Statement;

2. Form PTO-1449 listing nineteen (19) documents and accompanied by two (2) documents (IDS Doc. Refs. AM23 and AR59); and

3. One (1) Return Postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Nicole D. Dretar
Attorney for Applicants
Registration No. 54,076

NDD/srb
Enclosures

457328_1.DOC

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OIPE
OCT 24 2005
PATENT & TRADEMARK OFFICE

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
Sorrells *et al.*	Art Unit: 2662
Appl. No.: 10/973,917	Examiner: Kizou, Hassan
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Information Disclosure Statement filed on August 9, 2005 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Applicants provide the following comments regarding the documents:

Document AM23 was cited in an Office Action in related German Patent Application No. 19983659.0-35, filed October 20, 1999, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,557,641, which as already been cited in the present application.

Document AR59 is an English-language abstract of document AM23.

Document AN60 is a co-pending U.S. patent application, directed to related subject matter.

Documents AG67 and AH67 were cited in a Notice of Allowance in related U.S. Patent Application No. 09/632,855, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments," directed to related subject matter.

Document AI67 was cited in an Office Action in related U.S. Patent Application No. 09/796,824, filed March 2, 2001, entitled " Phased Array Antenna Applications of Universal Frequency Translation," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,742,189, which has already been cited in the present application.

Documents AA68-AC68 were cited in an Office Action in related U.S. Patent Application No. 10/318,207, filed December 13, 2002, entitled "Method And Apparatus For Reducing Re-Radiation Using Techniques Of Universal Frequency Translation Technology," directed to related subject matter.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Documents AD68-AG68 were cited in a Notice of Allowance in related U.S. Patent Application No. 09/855,851, filed May 16, 2001, entitled "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AH68, AI68, and AA69 were cited in an Office Action in related U.S. Patent Application No. 10/315,174, filed December 10, 2002, entitled "Reducing DC Offsets Using Spectral Spreading," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,999,561 and 6,686,879, which have already been cited in the present application.

Documents AB69-AD69 were cited in a Notice of Allowance in related U.S. Patent Application No. 10/359,636, filed February 7, 2003, entitled "Integrated Frequency Translation and Selectivity," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,126,682; 5,926,054; 6,049,706; 6,421,534; and 6,560,301, which have already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received

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by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of ____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language document AM23 appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document AM23 (DE 69221098T2) appears to describe a radiofrequency frequency multiplier comprising an automatic level control circuit. An English-language abstract of document AM23 is enclosed as document AR59. It is also noted that document AM23 is a counterpart of European Patent Publication EP 0 548 542 A1, which has already been cited in the present application.

☒ 7. Copies of documents AM23 and AR59 are enclosed. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents cited on the attached Form PTO-1449 are not enclosed. In addition, document AN60 is available to the Examiner on the USPTO's IFW System, therefore a copy is not submitted herewith.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000, 09/476,093, filed January 3, 2000, 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Nicole D. Dretar
Attorney for Applicants
Registration No. 54,076

Date: October 24, 2005

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449

SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. Sorrells	
FILING DATE	ART UNIT
October 27, 2004	2662

PATENT & TRADEMARK OFFICE OCT 24 2005 IAP13

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG67	3,737,778	06/1973	Van Gerwen *et al.*			
	AH67	4,286,283	08/1981	Clemens			
	AI67	4,241,451	12/1980	Maixner *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM23	DE 692 21 098 T2	01/1998	DE			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
	AR59	English Abstract for German Patent No. DE 692 21 098 T2, 1 page, data supplied from the espacenet.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449

SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. Sorrells	
FILING DATE	ART UNIT
October 27, 2004	2662

OIPE
OCT 24 2005
PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA68	5,014,130	05/1991	Heister *et al.*			
	AB68	5,390,215	02/1995	Anita *et al.*			
	AC68	5,805,460	09/1998	Greene *et al.*			
	AD68	6,882,194 B2	04/2005	Belot *et al.*			
	AE68	6,892,062 B2	05/2005	Lee *et al.*			
	AF68	6,917,796 B2	07/2005	Setty *et al.*			
	AG68	6,920,311 B2	07/2005	Rofougaran *et al.*			
	AH68	5,062,122	10/1991	Pham *et al.*			
	AI68	6,182,011 B1	01/2001	Ward			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN60	Sorrells *et al.*, U.S. Patent Appl. No. 09/569,045, filed May 10, 2000, entitled " Methods and apparatuses relating to a universal platform module and enabled by universal frequency translation technology".
	AO	
	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

453141_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. Sorrells	
	FILING DATE October 27, 2004	ART UNIT 2662

OIPE 1AP13 OCT 24 2005 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA69	6,639,939 B1	10/2003	Naden *et al.*			
	AB69	5,787,125	07/1998	Mittel			
	AC69	5,878,088	03/1999	Knutson *et al.*			
	AD69	6,215,828	04/2001	Signell *et al.*			
	AE						
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
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EXAMINER	DATE CONSIDERED

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453141_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2616
Appl. No.: 10/973,917	Examiner: Chin, Wellington
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Fifth Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Fifth Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' Fourth Supplemental Information Disclosure Statement filed on September 25, 2006 in connection with the above-captioned application.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Document AL26 was cited in an Office Action in related U.S. Patent Application No. 10/305,299, filed November 27, 2002, entitled "Method and Apparatus for Improving Dynamic Range in a Communication System," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 4,380,828; 4,562,414; and 5,339,459, which have already been cited in the present application.

Documents AP62 and AE79-AH79 were identified in a search relating to U.S. Patent Application No. 11/582,367, filed October 18, 2006, entitled "Apparatus and Method for Communicating an Input Signal in Polar Representation," directed to related subject matter.

Documents AH77, AI77, and AA78-AG78 were cited in an Office Action in related U.S. Patent Application No. 10/318,207, filed December 13, 2002, entitled "Method and Apparatus for Reducing Re-Radiation Using Techniques of Universal Frequency Translation Technology," directed to related subject matter.

Document AH78 was cited in an Office Action in related U.S. Patent Application No. 09/476,092, filed January 3, 2000, entitled "Analog Zero IF FM Decoder and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Document AI78 was cited in an Office Action in related U.S. Patent Application No. 11/173,021, filed July 5, 2005, entitled "Method and Circuit for Down-Converting a

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

Signal," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 3,694,754 and 6,393,070, which have already been cited in the present application.

Documents AA79-AC79 are co-owned patents which are directed to related subject matter.

Document AD79 was cited in an International Search Report and Written Opinion in related PCT Application No. PCT/US2004/013813, filed April 30, 2004, entitled "Real-Time Wireless Exchange of Objects," directed to related subject matter.

Document AI79 was cited in an Office Action in related U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Methods and Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 5,844,868 and 5,982,315, which have already been cited in the present application.

Document AA80 was cited in an Office Action in related U.S. Patent Application No. 10/453,622, filed June 4, 2003, entitled "Active Polyphase Inverter Filter for Quadrature Signal Generation," directed to related subject matter. Also cited in said Office Action was Salous, S., "IF digital generation of FMCW waveforms for wideband channel characterization," IEE Proceedings-I, IEE, Vol. 139, No. 3, pp. 281-288 (June 1992), which has already been cited in the present application.

Document AB80 was cited in an Office Action in related U.S. Patent Application No. 10/086,367, filed March 4, 2002, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 3,641,442, which has already been cited in the present application.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below:

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

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☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign

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application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document AL26 (JP 10-173563) appears to describe an up-down tuner. An English language translation of document AL26 is enclosed as document AO62.

☒ 7. Copies of documents AL26, AO62, and AP62 are enclosed. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent publications cited on the attached Form PTO-1449 are not enclosed.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

6,873,836), 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), 09/514,004, filed February 25, 2000 (now abandoned), 09/476,093, filed January 3, 2000 (now U.S. Patent No. 7,006,805), 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), and 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: November 9, 2006

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

606820_1.DOC

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH77	3,739,282	06/1973	Bruch *et al.*			
	AI77	4,439,787	03/1984	Mogi *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL26	JP 10-173563	06/1998	JP			Yes (Doc. AO62)
	AM						Yes No

NON-PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO62	English-language Computer Translation of Japanese Patent Publication No. JP 10-173563, provided by the JPO, 10 pages (June 26, 1998 - Date of publication of application) and cited in U.S. Patent Application Ser. No. 10/305,299, directed to related subject matter.
	AP62	*What is I/Q Data?*, printed September 16, 2006, from http://zone.ni.com, 8 pages (Copyright 2003).
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

606809_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA78	4,866,441	09/1989	Conway *et al.*			
	AB78	4,885,671	12/1989	Peil			
	AC78	5,164,985	11/1992	Nysen *et al.*			
	AD78	5,734,683	03/1998	Hulkko *et al.*			
	AE78	5,918,167	06/1999	Tiller *et al.*			
	AF78	6,445,726 B1	09/2002	Gharpurey			
	AG78	6,560,451 B1	05/2003	Somayajula			
	AH78	4,143,322	03/1979	Shimamura			
	AI78	2,530,824	11/1950	King			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

NON-PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN	
	AO	
	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

606809_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

FORM PTO-1449 FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA79	7,107,028 B2	09/2006	Sorrells *et al.*			
	AB79	7,110,435 B1	09/2006	Sorrells *et al.*			
	AC79	7,110,444 B1	09/2006	Sorrells *et al.*			
	AD79	6,973,476 B1	12/2005	Naden *et al.*			
	AE79	5,834,987	11/1998	Dent			
	AF79	RE37,138 E	04/2001	Dent			
	AG79	6,441,694 B1	08/2002	Turcotte *et al.*			
	AH79	6,892,057 B2	05/2005	Nilsson			
	AI79	6,741,650 B1	05/2004	Painchaud *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

NON-PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
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EXAMINER	DATE CONSIDERED

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FORM PTO-1449 FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.0330003	APPLICATION NO. 10/973,917
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE October 27, 2004	ART UNIT 2616

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA80	6,441,659 B1	08/2002	Demone			
	AB80	2002/0132642 A1	09/2002	Hines *et al.*			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ						Yes No
	AK						Yes No
	AL						Yes No
	AM						Yes No

NON-PATENT LITERATURE DOCUMENTS

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	AN	
	AO	
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EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

606809_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,917	10/27/2004	David F. Sorrells	1744.0330003	3273

26111 7590 07/28/2008
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WASHINGTON, DC 20005

EXAMINER	
TRINH, SONNY	
ART UNIT	PAPER NUMBER
2618	

MAIL DATE	DELIVERY MODE
07/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Interview Summary	Application No.	Applicant(s)	
	10/973,917	SORRELLS ET AL.	
	Examiner	Art Unit	
	Sonny TRINH	2618	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Sonny TRINH*. (3)_____.

(2) *Mr. Christian CAMARCE*. (4)_____.

Date of Interview: *22 July 2008*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *5 and 14*.

Identification of prior art discussed: *parent Application 09/569,044 (US 6,873,836)*.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *claims 5 and 14 will be amended to incorporate the allowable subject matters of claim 5 from the parent Application*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/Sonny TRINH/
Primary Examiner, Art Unit 2618
Examiner's signature, if required

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2618
Appl. No.: 10/973,917	Examiner: Trinh, Sonny
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**	

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Office Action dated March 26, 2008, (PTO Prosecution File Wrapper Paper No. 20080319), Applicants submit the following Amendment and Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1-4. (Canceled)

5. (Currently Amended) An apparatus capable of performing simultaneous multi-platform operations, comprising:

at least one multi-platform module including a plurality of transceivers each having at least one frequency translating module, wherein said at least one frequency translating module comprises

a switch configured to operate according to an energy transfer signal, and to sub-sample and transfer energy from a first electromagnetic (EM) signal, and

a storage module coupled to said switch and configured to store said transferred energy, wherein a second EM signal is generated from said stored energy, said second EM signal having a frequency different from said first EM signal; and

a control module ~~for enabling~~ configured to enable the at least one multi-platform module to communicate with at least one of a plurality of communication links, the control module including a plurality of protocol/standard sub-modules[[;]]

~~wherein a first protocol/standard sub-module operates a first transceiver in conformance with a first protocol/standard combination; and~~

~~wherein a second protocol/standard sub-module simultaneously operates a second transceiver in conformance with a second protocol/standard combination~~.

6. (Currently Amended) The apparatus of claim 5, wherein the control module ~~enables~~ is configured to enable the at least one multi-platform module to simultaneously communicate with a quantity of the plurality of communication links by employing an equal quantity of the plurality of standard/protocol sub-modules.

7. (Previously Presented) The apparatus of claim 5, wherein the at least one multi-platform module includes a plurality of receivers and a plurality of transmitters each having at least one frequency translating module.

8. (Currently Amended) The apparatus of claim [[5]] 23, wherein the first protocol/standard combination is different from the second protocol/standard combination.

9. (Currently Amended) The apparatus of claim [[5]] 23, wherein the first and second protocol/standard sub-modules contain respective first and second implementation and operational instructions for the at least one multi-platform sub-module.

10. (Previously Presented) The apparatus of claim 9, wherein the first and second implementation and operational instructions include respective first and second protocol stacks and specification information about the first and second protocol architectures.

11. (Previously Presented) The apparatus of claim 9, wherein the first and second implementation and operational instructions can be updated, upgraded, replaced, or modified to provide the at least one multi-platform sub-module with additional functionality.

12. (Currently Amended) The apparatus of claim [[5]] 23, wherein the first and second protocol/standard sub-modules are configured to operate the first and second transceivers in conformance with respective requirements of [[the]] first and second protocols and operating environments.

13. (Previously Presented) The apparatus of claim 12, wherein the first and second operating environments include at least one of respective standards, content encoders and decoders, and protocol gateways.

14. (Currently Amended) A method for performing simultaneous multi-platform operations, comprising:

(1) controlling at least one multi-platform module to communicate with at least one of a plurality of communication links using a control module having a

plurality of standard/protocol sub-modules, wherein the at least one multi-platform module includes a plurality of transceivers each having at least one frequency translation module, wherein said at least one frequency translation module comprises

a switch configured to operate according to an energy transfer signal, and to sub-sample and transfer energy from a first electromagnetic (EM) signal, and

a storage module coupled to said switch and configured to store said transferred energy, wherein a second EM signal is generated from said stored energy, said second EM signal having a frequency different from said first EM signal;

(2) operating a first transceiver in conformance with a first protocol/standard combination using a first standard/protocol sub-module; and

(3) ~~simultaneously~~ operating a second transceiver in conformance with a second protocol/standard combination using a second standard/protocol sub-module.

15. (Previously Presented) The method of claim 14, wherein step (1) comprises:

controlling the at least one multi-platform module to simultaneously communicate with a quantity of the plurality of communications links by employing an equal quantity of the plurality of standard/protocol sub-modules.

16. (Currently Amended) The method of claim 14, wherein step (1) comprises:

controlling the at least one multi-platform module to communicate with at least one of the plurality of communication links using the control module, the at least one multi-platform module including a plurality of receivers and a plurality of transmitters each having at least one frequency translating module.

17. (Previously Presented) The method of claim 14, wherein step (3) comprises:

simultaneously operating the second transceiver in conformance with a second protocol/standard combination that is different from the first protocol/standard combination.

18. (Previously Presented) The method of claim 14, wherein steps (2) and (3) comprise:

programming the first and second protocol/standard sub-modules with respective first and second implementation and operational instructions for the at least one multi-platform sub-module.

19. (Currently Amended) The method of claim 18, wherein steps (2) and (3) further comprise:

programming the first and second protocol/standard sub-modules with respective first and second protocol stacks and specification information about [[the]] first and second protocol architectures.

20. (Previously Presented) The method of claim 18, wherein steps (2) and (3) further comprise:

updating, upgrading, replacing, or modifying the first and second implementation and operational instructions to provide the at least one multi-platform sub-module with additional functionality.

21. (Currently Amended) The method of claim 14, wherein steps (2) and (3) further comprise:

simultaneously operating the first and second transceivers in conformance with respective requirements of [[the]] first and second protocols and operating environments.

22. (Previously Presented) The method of claim 21, wherein steps (2) and (3) further comprise:

simultaneously operating the first and second transceivers in conformance with respective standards, content encoders and decoders, and protocol gateways of the first and second protocols and operating environments.

23. (New) The apparatus of claim 5, wherein the plurality of protocol/standard sub-modules comprise a first protocol/standard sub-module configured to operate a first transceiver in conformance with a first protocol/standard combination and a second protocol/standard sub-module configured to simultaneously operate a second transceiver in conformance with a second protocol/standard combination.

24. (New) The method of claim 14, wherein step (3) comprises simultaneously operating the second transceiver and the first transceiver.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 5-24 are pending in the application, with claims 5 and 14 being the independent claims. Claims 5, 6, 8, 9, 12, 14, 16, 19, and 21 are sought to be amended. New claims 23 and 24 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Applicants wish to thank the Examiner for his time during the telephone interview on July 22, 2008, during which the Examiner indicated that the above amendments to claims 5 and 14 would overcome the applied reference.

Based on the above amendments and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

It is noted that this application is related to a number of other patent(s) and application(s). The claims presented in this application should be interpreted solely based on the file history of this application, not the file history of any related patent(s) or application(s).

With respect to the present application, Applicant hereby rescinds any disclaimer of claim scope made in the parent application or any predecessor or related application. The Examiner is advised that any previous disclaimer of claim scope, if any in the parent application or any predecessor or related application, and the alleged prior art that it was made to allegedly avoid, may need to be revisited. Also, no disclaimer of claim scope, if

any, in the present application should be read back into any parent, predecessor or related application.

Objection to the Specification

On page 2 of the Office Action, the Examiner alleged that the disclosure of a prior-filed application, Appl. No. 09/261,129, fails to provide adequate support or enablement in the manner provided under 35 U.S.C. § 112, first paragraph, for one or more claims of the present application. Applicants do not acquiesce to the propriety of this objection and reserve the right to discuss the propriety of the objection at a later date.

Rejections under 35 U.S.C. § 102

On page 3 of the Office Action, the Examiner rejected claims 5-10, 12-19, and 21-22 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,894,988 to Zehavi (hereinafter "Zehavi"). Applicants respectfully traverse.

As discussed with the Examiner in the above-mentioned interview, claims 5 and 14 have been amended to include features distinguishable over the applied reference. To summarize, Zehavi does not teach or suggest a frequency translation module comprising "a switch configured to operate according to an energy transfer signal and to sub-sample and transfer energy from a first electromagnetic (EM) signal, and a storage module coupled to said switch and configured to store said transferred energy, wherein a second EM signal is generated from said stored energy, said second EM signal having a frequency different from said first EM signal," as recited in claims 5 and 14.

Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claims 5 and 14, and their respective dependent claims.

Rejections under 35 U.S.C. § 103

On page 5 of the Office Action, the Examiner rejected claims 11 and 20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Zehavi. Applicants respectfully traverse.

As discussed above, Zehavi does not teach or suggest all of the claim limitations of claims 5 and 14. At least based on their dependency to claims 5 and 14, claims 11 and 20 should also be found allowable over the cited art. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claims 11 and 20.

New Claims 23 and 24

Claims 23 and 24 depend on claims 5 and 14, respectively, which are both patentable over the cited reference for reasons discussed above. As such, Applicants respectfully submit that claims 23 and 24 are patentable over the cited art for at least the same reasons, as well as for its additional distinguishing features.

Accordingly, Applicants respectfully request the Examiner to pass claims 5-24 to allowance.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 7/28/08

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

832960_1.DOC

Electronic Patent Application Fee Transmittal

Application Number:	10973917
Filing Date:	27-Oct-2004
Title of Invention:	Universal platform module and methods and apparatuses relating thereto enabled by universal frequency translation technology
First Named Inventor/Applicant Name:	David F. Sorrells
Filer:	Michael Q. Lee/marilyn sumpter
Attorney Docket Number:	1744.0330003

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	120	120

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**300**

Electronic Acknowledgement Receipt

EFS ID:	3686960
Application Number:	10973917
International Application Number:	
Confirmation Number:	3273
Title of Invention:	Universal platform module and methods and apparatuses relating thereto enabled by universal frequency translation technology
First Named Inventor/Applicant Name:	David F. Sorrells
Customer Number:	26111
Filer:	Michael Q. Lee/marilyn sumpter
Filer Authorized By:	Michael Q. Lee
Attorney Docket Number:	1744.0330003
Receipt Date:	28-JUL-2008
Filing Date:	27-OCT-2004
Time Stamp:	16:25:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$300
RAM confirmation Number	1740
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1		17440330003-Amendment-and-IDS.pdf	868740 1e8274514087ee8b75b9e7109bab1b1d29bbee4b	yes	26

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Miscellaneous Incoming Letter	1	2
Extension of Time	3	3
Information Disclosure Statement Letter	4	12
Information Disclosure Statement (IDS) Filed	13	14
Amendment - After Non-Final Rejection	15	15
Claims	16	22
Applicant Arguments/Remarks Made in an Amendment	23	26

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	8377 aa38a709c65b247a64a8b4474c97ec2851709591	no	2

Warnings:

Information:

Total Files Size (in bytes):	877117

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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+Admitted only in Virginia
•Practice Limited to Federal Agencies

July 28, 2008

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2618

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Amendment and Reply Under 37 C.F.R. § 1.111;
2. Petition for Extension of Time;
3. Online Credit Card Payment Authorization for the amount of $300.00 to cover:

   $180.00 IDS fee under 37 C.F.R. § 1.17(p); and

   $120.00 Extension of Time fee;

4. Seventh Supplemental Information Disclosure Statement; and
5. Form PTO/SB/08A listing thirty-five (35) documents (US1-US35).

This filing is being electronically submitted through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/CAC:mls
Enclosures

853558_1.DOC

PTO/SB/22 (01-08)
Approved for use through 05/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARMENT OF COMMERCE
Under the paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless if displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2008 *(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)*	Docket Number (Optional) 1744.0330003
Application Number 10/973,917	Filed October 27, 2004
For Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology	
Art Unit 2618	Examiner Trinh, Sonny

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
[X]	One month (37 CFR 1.17(a)(1))	$120	$60	$ 120.00
[ ]	Two months (37 CFR 1.17(a)(2))	$460	$230	$
[ ]	Three months (37 CFR 1.17(a)(3))	$1050	$525	$
[ ]	Four months (37 CFR 1.17(a)(4))	$1640	$820	$
[ ]	Five months (37 CFR 1.17(a)(5))	$2230	$1115	$

[ ] Applicant claims small entity status. See 37 CFR 1.27.

[ ] A check in the amount of the fee is enclosed.

[X] Payment by credit card. Form PTO-2038 is attached.

[ ] The Director has already been authorized to charge fees in this application to a Deposit Account.

[X] The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 19-0036. I have enclosed a duplicate copy of this sheet.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

[ ] applicant/inventor.

[ ] assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

[X] attorney or agent of record. Registration Number 35,239

[ ] attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature	Date
	7/28/08
Michael Q. Lee	(202) 371-2600
Typed or printed name	Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

[ ] Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2618
Appl. No.: 10/973,917	Examiner: Trinh, Sonny
Filed: October 27, 2004	Atty. Docket: 1744.0330003
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**	

Seventh Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying IDS Forms are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicants have listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents US1 and US2 were cited in an Office Action in U.S. Patent Appl. No. 11/802,389, filed May 22, 2007, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter.

Document US3 was cited in an Office Action in U.S. Patent Appl. No. 11/356,419, filed February 17, 2006, entitled "Gain Control in a Communication Channel," directed to related subject matter.

Documents US4 and US5 were cited in an Office Action in related U.S. Patent Application No. 10/197,255, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter. Also cited in said Office Action were U.S. Patent Publication Nos. 2002/0080728 and 2002/0163921, and U.S. Patent Nos. 5,703,584; 6,591,310; and 6,963,626, which have already been cited in the present application.

Documents US6-US9 and US25-US29 are co-owned patents which are directed to related subject matter.

Documents US10-US14 were cited in a Notice of Allowance in related U.S. Patent Application No. 11/826,416, filed July 16, 2007, entitled "Method And System For Frequency Up-Conversion With Modulation Embodiments," directed to related subject matter. Also cited in said Notice of Allowance was U.S. Patent No. 5,734,683, which has already been cited in the present application.

Document US15 was cited in an Office Action in related U.S. Patent Application No. 11/015,653, filed December 20, 2004, entitled "Method, System, And Apparatus For

Balanced Frequency Up-Conversion, Including Circuitry To Directly Couple The Outputs Of Multiple Transistors," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 7,082,171; 6,853,690; and 6,687,493, all of which have already been cited in the present application.

Documents US16-US20 were cited in an Office Action in related U.S. Patent Application No. 10/973,917, filed October 27, 2004, entitled "Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology," directed to related subject matter.

Document US21 was cited in an Office Action in related U.S. Patent Application No. 11/082,389, filed May 22, 2007, entitled "Method And System For Frequency Up-Conversion," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,112,061, which was already cited in the present application.

Documents US22 and US23 were cited in an Office Action in related U.S. Patent Application No. 11/826,416, filed July 16, 2007, entitled "Method And System For Frequency Up-Conversion With Modulation Embodiments," directed to related subject matter.

Document US24 was cited in an Office Action in related U.S. Patent Application No. 11/292,118, filed December 2, 2005, entitled "Methods and Systems for Utilizing Universal Frequency Translators for Phase and/or Frequency Detection," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,512,798, which was already cited in the present application.

Documents US30-US31 were cited in an Office Action in related U.S. Patent Application No. 11/356,419, filed February 17, 2006, entitled "Gain Control in a Communication Channel," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 5,483,691, which has already been cited in the present application.

Document US32 was cited in an Office Action in related U.S. Patent Application No. 09/550,644, filed April 14, 2000, entitled "Method and System for Down-Converting an Electromagnetic Signal, Transforms for Same, and Aperture Relationships," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,404,758, which has already been cited in the present application.

Document US33 was cited in an Office Action in related U.S. Patent Application No. 11/802,389, filed May 22, 2007, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter. Also cited in said Office Action were U.S. Patent Nos. 4,688,237 and 6,112,061, which have already been cited in the present application.

Documents US34 and US35 were cited in an Office Action in related U.S. Patent Application No. 11/390,153, filed March 28, 2006, entitled "Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter. Also cited in said Office Action was U.S. Patent No. 6,018,553, which has already been cited in the present application.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☒ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than

three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ c. The required fee is provided through online credit card payment authorization in the amount of $180.00 in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of $180.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than

three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☐ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

☒ 7. In accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the attached IDS Forms are submitted.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in the parent Application Nos. 09/569,044, filed May 10, 2000 (now U.S. Patent No. 6,873,836), 09/525,615, filed March 14, 2000 (now U.S. Patent No. 6,853,690), 09/526,041, filed March 14, 2000 (now U.S. Patent No. 6,879,817), 09/514,004, filed February 25, 2000 (now abandoned), 09/476,093, filed January 3, 2000 (now U.S. Patent No. 7,006,805), 09/476,330, filed January 3, 2000 (now U.S. Patent No. 6,704,549), and 09/261,129, filed March 3, 1999 (now U.S. Patent No. 6,370,371), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 7/28/08

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Equivalent of Form PTO/SB/08A (09-06)
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SEVENTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/973,917
Filing Date	October 27, 2004
First Named Inventor	David F. SORRELLS
Art Unit	2618
Examiner Name	Sonny Trinh
Attorney Docket Number	1744.0330003

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	6,112,061	08-29-2000	Rapeli	
	US2	6,625,470 B1	09-23-2003	Fourtet *et al.*	
	US3	6,813,320 B1	11-02-2004	Claxton *et al.*	
	US4	2002/0021685 A1	02-21-2002	Sakusabe	
	US5	2003/0078011 A1	04-24-2003	Cheng *et al.*	
	US6	7,308,242 B2	12-11-2007	Sorrells *et al.*	
	US7	7,321,640 B2	01-22-2008	Milne *et al.*	
	US8	7,321,735 B1	01-22-2008	Smith *et al.*	
	US9	7,321,751 B2	01-22-2008	Sorrells *et al.*	
	US10	2006/0002491 A1	01-05-2006	Darabi *et al.*	
	US11	4,663,744	05-05-1987	Russell *et al.*	
	US12	5,559,809	09-24-1996	Jeon *et al.*	
	US13	6,038,265	03-14-2000	Pan *et al.*	
	US14	6,876,846 B2	04-05-2005	Tamaki *et al.*	
	US15	6,512,798 B1	01-28-2003	Akiyama *et al.*	
	US16	6,072,996	06-06-2000	Smith	
	US17	6,088,348	07-11-2000	Bell, III *et al.*	
	US18	6,198,941 B1	03-06-2001	Aho *et al.*	
	US19	6,894,988 B1	05-17-2005	Zehavi	
	US20	7,193,965 B1	03-20-2007	Nevo *et al.*	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP1					
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					
	FP6					
	FP8					
	FP9					

853542_1.DOC

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Equivalent of Form PTO/SB/08A (09-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

SEVENTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/973,917
Filing Date	October 27, 2004
First Named Inventor	David F. SORRELLS
Art Unit	2618
Examiner Name	Sonny Trinh
Attorney Docket Number	1744.0330003

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US21	4,688,237	08-18-1987	Brault	
	US22	5,461,646	10-24-1995	Anvari	
	US23	5,483,245	01-09-1996	Ruinet	
	US24	7,197,081 B2	03-27-2007	Saito	
	US25	7,376,410 B2	05-20-2008	Sorrells *et al.*	
	US26	7,379,515 B2	05-27-2008	Johnson *et al.*	
	US27	7,379,883 B2	05-27-2008	Sorrells	
	US28	7,386,292 B2	06-10-2008	Sorrells *et al.*	
	US29	7,389,100 B2	06-17-2008	Sorrells *et al.*	
	US30	4,651,210	03-17-1987	Olson	
	US31	5,659,372	08-19-1997	Patel *et al.*	
	US32	6,097,762	08-01-2000	Suzuki *et al.*	
	US33	5,512,946	04-30-1996	Murata *et al.*	
	US34	3,809,821	05-07-1974	Melvin	
	US35	6,275,542	08-14-2001	Katayama *et al.*	
	US36				
	US37				
	US38				
	US39				
	US40				

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP10					
	FP11					
	FP12					
	FP13					
	FP14					
	FP15					
	FP16					
	FP17					
	FP18					

853542_1.DOC

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/973,917	10/27/2004	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 07/28/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $50=	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $210=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
//TERRANCE LAWRENCE//

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 10/03/2008

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
TRINH, SONNY	
ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 10/03/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,917	10/27/2004	David F. Sorrells	1744.0330003	3273

TITLE OF INVENTION: UNIVERSAL PLATFORM MODULE AND METHODS AND APPARATUSES RELATING THERETO ENABLED BY UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	01/05/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 10/03/2008

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,917	10/27/2004	David F. Sorrells	1744.0330003	3273

TITLE OF INVENTION: UNIVERSAL PLATFORM MODULE AND METHODS AND APPARATUSES RELATING THERETO ENABLED BY UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	01/05/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRINH, SONNY	2618	455-313000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,917	10/27/2004	David F. Sorrells	1744.0330003	3273

26111 7590 10/03/2008

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
TRINH, SONNY	
ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 10/03/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 788 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 788 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/973,917	SORRELLS ET AL.	
	Examiner	Art Unit	
	Sonny TRINH	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 07/28/08*.

2. ☒ The allowed claim(s) is/are *5-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Sonny TRINH/
Primary Examiner, Art Unit 2618

Equivalent of Form PTO/SB/08A (09-06)
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Substitute for form 1449/PTO

SEVENTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/973,917
Filing Date	October 27, 2004
First Named Inventor	David F. SORRELLS
Art Unit	2618
Examiner Name	Sonny Trinh
Attorney Docket Number	1744.0330003

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number / Number-Kind Code[2] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/ST/	US1	6,112,061	08-29-2000	Rapeli	
	US2	6,625,470 B1	09-23-2003	Fourtet *et al.*	
	US3	6,813,320 B1	11-02-2004	Claxton *et al.*	
	US4	2002/0021685 A1	02-21-2002	Sakusabe	
	US5	2003/0078011 A1	04-24-2003	Cheng *et al.*	
	US6	7,308,242 B2	12-11-2007	Sorrells *et al.*	
	US7	7,321,640 B2	01-22-2008	Milne *et al.*	
	US8	7,321,735 B1	01-22-2008	Smith *et al.*	
	US9	7,321,751 B2	01-22-2008	Sorrells *et al.*	
	US10	2006/0002491 A1	01-05-2006	Darabi *et al.*	
	US11	4,663,744	05-05-1987	Russell *et al.*	
	US12	5,559,809	09-24-1996	Jeon *et al.*	
	US13	6,038,265	03-14-2000	Pan *et al.*	
	US14	6,876,846 B2	04-05-2005	Tamaki *et al.*	
	US15	6,512,798 B1	01-28-2003	Akiyama *et al.*	
	US16	6,072,996	06-06-2000	Smith	
	US17	6,088,348	07-11-2000	Bell, III *et al.*	
	US18	6,198,941 B1	03-06-2001	Aho *et al.*	
	US19	6,894,988 B1	05-17-2005	Zehavi	
/ST/	US20	7,193,965 B1	03-20-2007	Nevo *et al.*	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document / Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP1					
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					
	FP6					
	FP8					
	FP9					

853542_1.DOC

Examiner Signature	/Sonny Trinh/	Date Considered	09/25/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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Equivalent of Form PTO/SB/08A (09-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

SEVENTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/973,917
Filing Date	October 27, 2004
First Named Inventor	David F. SORRELLS
Art Unit	2618
Examiner Name	Sonny Trinh
Attorney Docket Number	1744.0330003

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/ST/	US21	4,688,237	08-18-1987	Brault	
	US22	5,461,646	10-24-1995	Anvari	
	US23	5,483,245	01-09-1996	Ruinet	
	US24	7,197,081 B2	03-27-2007	Saito	
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	US26	7,379,515 B2	05-27-2008	Johnson *et al.*	
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	US34	3,809,821	05-07-1974	Melvin	
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	US36				
	US37				
	US38				
	US39				
	US40				

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP10					
	FP11					
	FP12					
	FP13					
	FP14					
	FP15					
	FP16					
	FP17					
	FP18					

853542_1.DOC

Examiner Signature	/Sonny Trinh/	Date Considered	09/25/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973917	SORRELLS ET AL.
	Examiner	**Art Unit**
	Sonny TRINH	2618

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/19/2008	09/25/2008							
	1	-	-							
	2	-	-							
	3	-	-							
	4	-	-							
1	5	✓	=							
2	6	✓	=							
3	7	✓	=							
5	8	✓	=							
6	9	✓	=							
7	10	✓	=							
8	11	✓	=							
9	12	✓	=							
10	13	✓	=							
11	14	✓	=							
12	15	✓	=							
13	16	✓	=							
14	17	✓	=							
15	18	✓	=							
16	19	✓	=							
17	20	✓	=							
18	21	✓	=							
19	22	✓	=							
4	23		=							
20	24		=							

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
10973917	SORRELLS ET AL.
Examiner	**Art Unit**
Sonny TRINH	2618

ORIGINAL

CLASS	SUBCLASS
455	313

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
455	323	552.1			

INTERNATIONAL CLASSIFICATION

CLAIMED	NON-CLAIMED
H 04B 1/26 (2006.0)	
H 04M 1/00 ()	

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1	14	17												
-	2	15	18												
-	3	16	19												
-	4	17	20												
1	5	18	21												
2	6	19	22												
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6	9														
7	10														
8	11														
9	12														
10	13														
11	14														
12	15														
13	16														

NONE

(Assistant Examiner) (Date)

Total Claims Allowed: 20

/Sonny TRINH/
Primary Examiner.Art Unit 2618 09/25/08

(Primary Examiner) (Date)

O.G. Print Claim(s)	O.G. Print Figure
1	4

U.S. Patent and Trademark Office

Part of Paper No. 20080925

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10973917	SORRELLS ET AL.
	Examiner	**Art Unit**
	Sonny TRINH	2618

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
455	41.2, 552.1, 422.1, 550.1, 556.1, 556.2, 39, 41.1, 67.13, 552.1, 313, 323	9/25/08	ST

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
U.S. Patent, EPO, JPO, DERWENT, PG-PUB	9/25/08	ST

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**
455	552.1, 313, 323	9/25/08	ST

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 10/03/2008

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,917	10/27/2004	David F. Sorrells	1744.0330003	3273

TITLE OF INVENTION: UNIVERSAL PLATFORM MODULE AND METHODS AND APPARATUSES RELATING THERETO ENABLED BY UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	01/05/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRINH, SONNY	2618	455-313000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sterne, Kessler, Goldstein
2 & Fox P.L.L.C.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: ParkerVision, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Jacksonville, Florida

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☒ Advance Order - # of Copies One (1)

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☒ Payment by credit card. Form PTO-2038 is attached.

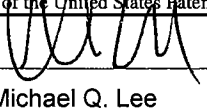
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-0036 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature  Date 12/1/08

Typed or printed name Michael Q. Lee Registration No. 35,239

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	10973917
Filing Date:	27-Oct-2004
Title of Invention:	UNIVERSAL PLATFORM MODULE AND METHODS AND APPARATUSES RELATING THERETO ENABLED BY UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY
First Named Inventor/Applicant Name:	David F. Sorrells
Filer:	Michael Q. Lee/Valee Bartels
Attorney Docket Number:	1744.0330003

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	1	3	3
		Total in USD ($)		**1813**

Electronic Acknowledgement Receipt

EFS ID:	4371942
Application Number:	10973917
International Application Number:	
Confirmation Number:	3273
Title of Invention:	UNIVERSAL PLATFORM MODULE AND METHODS AND APPARATUSES RELATING THERETO ENABLED BY UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY
First Named Inventor/Applicant Name:	David F. Sorrells
Customer Number:	26111
Filer:	Michael Q. Lee/Valee Bartels
Filer Authorized By:	Michael Q. Lee
Attorney Docket Number:	1744.0330003
Receipt Date:	01-DEC-2008
Filing Date:	27-OCT-2004
Time Stamp:	15:10:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1813
RAM confirmation Number	421
Deposit Account	190036
Authorized User	STERNE, KESSLER, GOLDSTEIN & FOX

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Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		17440330003IssueFee.pdf	137490 9bbfb9bb617472547a0d19d345d89d1638 9927e3	yes	3

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Miscellaneous Incoming Letter	1	2
Issue Fee Payment (PTO-85B)	3	3

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	33722 e2bc0a65197f131a52676fc35c8fe6301302 1e51	no	2

Warnings:

Information:

Total Files Size (in bytes):	171212

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Sterne Kessler Goldstein Fox
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*Admitted only in Maryland
+Admitted only in Virginia
•Practice Limited to Federal Agencies

December 1, 2008

WRITER'S DIRECT NUMBER:
(202) 772-8674
INTERNET ADDRESS:
MLEE@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 10/973,917; Filed: October 27, 2004
For: **Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

In response to the **Notice of Allowance and Fee(s) Due** dated October 3, 2008, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Issue Fee Transmittal (Form PTOL-85); and

2. Online Credit Card Payment Authorization for $1,813.00 to cover:
$1,510.00 - Issue Fee;
$300.00 - Publication Fee; and
$3.00 - Advance copy of patent.

The above-listed documents are filed electronically through EFS-Web.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/CAC/vb
Enclosures

908998_1.doc

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.0330003	10/973,917
FIRST NAMED INVENTOR	
David F. Sorrells	
FILING DATE	ART UNIT
October 27, 2004	2661

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10	4,504,803	03/1985	Lee *et al.*			
	AB10	4,517,519	05/1985	Mukaiyama			
	AC10	4,517,520	05/1985	Ogawa			
	AD10	4,518,935	05/1985	van Roermund			
	AE10	4,521,892	06/1985	Vance *et al.*			
12/3/08	AF10	4,563,773	~~07~~/1986	Dixon, Jr. *et al.*			
	AG10	4,577,157	03/1986	Reed			
	AH10	4,583,239	04/1986	Vance			
	AI10	4,591,736	05/1986	Hirao *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ10	WO 97/38490 A1	10/1997	PCT			N/A
	AK10	WO 98/00953 A1	01/1998	PCT			N/A
	AL10	WO 98/24201 A1	06/1998	PCT			N/A
	AM10	EP 0 099 265 A1	01/1984	EP			N/A

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER INITIAL	DOC. REF.	CITATION
	AN10	Fukahori, K., "A CMOS Narrow-Band Signaling Filter with Q Reduction," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-19, No. 6, pp. 926-932 (December 1984).
	AO10	Fukuchi, H. and Otsu, Y., "Available time statistics of rain attenuation on earth-space path," *IEE Proceedings-H: Microwaves, Antennas and Propagation*, IEE, Vol. 135, Pt. H, No. 6, pp. 387-390 (December 1988).
	AP10	Gibbins, C.J. and Chadha, R., "Millimetre-wave propagation through hydrocarbon flame," *IEE Proceedings*, IEE, Vol. 134, Pt. H, No.2 , pp. 169-173 (April 1987).
	AQ10	Gilchrist, B. *et al.*, "Sampling hikes performance of frequency synthesizers," *Microwaves & RF*, Hayden Publishing, Vol. 23, No. 1, pp. 93-94 and 110 (January 1984).
	AR10	Gossard, E.E., "Clear weather meteorological effects on propagation at frequencies above 1 Ghz," *Radio Science*, American Geophysical Union, Vol. 16, No. 5, pp. 589-608 (September - October 1981).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

419797_1.DOC ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /ST/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/973,917	01/27/2009	7483686	1744.0330003	3273

26111 7590 01/07/2009

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 788 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

David F. Sorrells, Middleburg, FL;
Michael J. Bultman, Jacksonville, FL;
Robert W. Cook, Switzerland, FL;
Richard C. Looke, Jacksonville, FL;
Charley D. Moses JR., DeBary, FL;

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of:	Confirmation No.: 3273
SORRELLS *et al.*	Art Unit: 2618
Patent. No.: 7,483,686	Examiner: Trinh, Sonny
Issued: January 27, 2009	Atty. Docket: 1744.0330003
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**	

Request for Certificate of Correction Under 37 C.F.R. § 1.322

Attn: Certificate of Correction Branch

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

It is hereby requested that a Certificate of Correction under 37 C.F.R. § 1.322 be issued for the above-captioned United States Patent. This Certificate of Correction is being requested due to mistakes which appear in the printed patent. These mistakes were made by the U.S. Patent and Trademark Office.

Specifically, the printed patent contains the following errors for which a Certificate of Correction is respectfully requested:

In Column 51, line 54 please replace "on" with --one--. See Amendment filed by Applicant July 28, 2008.

In Column 52, line 28 please replace "claim 14" with --claim 11--. See Amendment filed by Applicant July 28, 2008.

In Column 52, line 46 please insert "further" after "(3)". See Amendment filed by Applicant July 28, 2008.

Remarks

The above-noted corrections do not involve such changes in the patent as would constitute new matter or would require reexamination.

A completed Form PTO/SB/44 accompanies this request, with the above-noted corrections printed thereon. Accordingly, a Certificate of Correction is believed proper and issuance thereof is respectfully requested.

The Commissioner is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO: 7,483,686

DATED: January 27, 2009

INVENTOR(S): SORRELLS *et al.*

It is certified that error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below.

In Column 51, line 54 please replace "on" with --one--.

In Column 52, line 28 please replace "claim 14" with --claim 11--.

In Column 52, line 46 please insert "further" after "(3)".

MAILING ADDRESS OF SENDER (Please do not use customer number below):

1100 New York Avenue, NW
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Atty. Dkt. No. 1744.0330003

This collection of information is required by 37 CFR 1.322, 1.323 and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you are required to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	5685626
Application Number:	10973917
International Application Number:	
Confirmation Number:	3273
Title of Invention:	UNIVERSAL PLATFORM MODULE AND METHODS AND APPARATUSES RELATING THERETO ENABLED BY UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY
First Named Inventor/Applicant Name:	David F. Sorrells
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Attorney Docket Number:	1744.0330003
Receipt Date:	13-JUL-2009
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Time Stamp:	10:52:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		17440330003certofcorr.pdf	148498 285c2fc53e95709d8a9a7195823802a25fac12b0	yes	4

	Multipart Description/PDF files in .zip description		
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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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July 13, 2009

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Art Unit 2618

Attn: Certificate of Correction Branch

Re: U.S. Utility Patent
Patent No. 7,483,686; Issued: January 27, 2009
For: **Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology**
Inventors: SORRELLS *et al.*
Our Ref: 1744.0330003

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Request for Certificate of Correction Under 37 CFR 1.322; and

2. Certificate of Correction PTO/SB/44 form.

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Patentees
Registration No. 35,239

MQL/smh
Enclosure(s)

1003665_1.DOC

UNITED STATES PATENT AND TRADEMARK OFFICE

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PATENT NO. : 7,483,686 B2
APPLICATION NO. : 10/973917
DATED : January 27, 2009
INVENTOR(S) : Sorrells et al.

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Signed and Sealed this

Eighteenth Day of August, 2009

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office