

The Design of a Mobile Radio Receiver using a Direct Conversion Architecture

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Abstract

This paper outlines the advantages of building a mobile radio receiver using a direct downconversion architecture rather than the conventional heterodyne approach. Design problems particular to mobile radio direct conversion receivers, such as achieving good sensitivity and dynamic range, are discussed and solutions proposed. Namely the integrated approach taken for the design of the RF mixers, the subsequent low frequency amplifier, and active filter is detailed. This allows low conversion loss and high output impedance mixers to be designed, amplifiers with low noise performance over the dc to $\frac{BW_{RF}}{2}$ bandwidth to be constructed, and, filters that set selectivity without impacting the signal-to-noise ratio at their output to be specified. Design advantages that are a direct consequence of this choice of receiver architecture, such as high selectivity, small size, and low power consumption, are detailed. Finally we describe the receiver implementation and characterize its performance.

Introduction

The direct conversion receiver considered here is depicted in Figure 1. To illustrate its performance, consider the input signal, f_{RF} , to have a center frequency f_c and a bandwidth BW_{RF} . The input signal, after optional amplification, is power-split and sent to the inputs of two broadband mixers. The local oscillator frequency, f_{LO} , of both the in-phase and quadrature-phase (I/Q) mixers is locked to f_c . Consequently, the signal at the output of each mixer, f_o spans from dc to $BW_{RF}/2$. These signals are amplified, filtered, and finally processed together to reconstruct the transmitted signal.

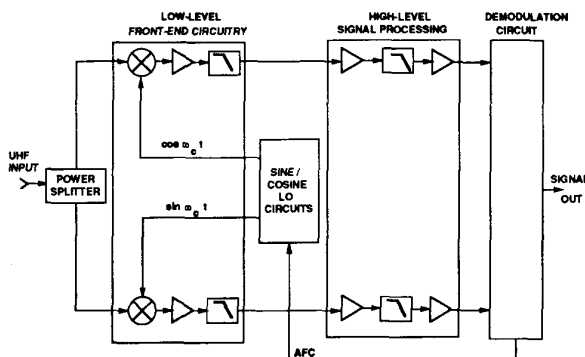


Figure 1: The direct conversion receiver.

†This work was performed as part of Ms. Estabrook's doctoral research at Stanford University.

The receiver lends itself to work with many signal frequencies and formats. The low level signal processing, comprised of the RF mixers and the first stage of amplification and filtering, is accomplished by low noise, high dynamic range, circuits. Although the input mixer will need to be designed for operation with a specific f_c and BW_{RF} for best performance, the subsequent low level amplifier-filter stage may be designed in several different bandwidths ($BW_{filter} \approx BW_{RF}/2$) to serve a wide number of applications. Thus by choosing the correct mixer and amplifier-filter stage for a specific application, a large range of signals with center frequency's between 50 and 900 MHz, thus covering all mobile radio bands, and signal bandwidth's from a few KHz, for SSB voice applications, to a few hundred KHz, for digital applications can be accommodated. The second stage of amplification and filtering is more application-specific; however, standard CMOS opamps and switched capacitor filters with variable cutoff frequencies can be used as the signal power has now been boosted above the noise floor. Finally, signal reconstruction – unfolding and correct frequency placing of the baseband signal – and demodulation must take place; these circuits are also application dependent. These functions can be implemented by one circuit and realized using standard processing techniques.

This paper discusses the application of direct conversion to the design of a mobile cellular radio at 900 MHz. This work has been inspired by Weaver's design of a SSB direct conversion receiver in 1956 [1] and by the more recent use of direct conversion receivers for VHF radio paging applications using BFSK modulation [2,3]. Translation of this work to higher signal frequencies and to more complex signal sets has been slowed pending clarification of certain issues, the most important being the determination of achievable gain and phase balance between the 'I' and 'Q' channel and the impact of this imbalance on signal reception for several modulation types, the development of a receiver front-end that can provide the sensitivity and dynamic range required, and finally the design of modulation specific demodulation circuits.

This paper addresses the first three issues as they are common to all applications. The design of the CMOS active filter, the modulation specific circuits, the AFC circuits and the LO generation circuits are outside the scope of this work. First the motivation to reconsider this receiver is outlined. Second issues concerning phase and gain balance between channels are examined. Third the functions performed by the front-end circuits are detailed and their design given. Finally the overall receiver specifications are calculated and compared with those of a typical heterodyne receiver. For the purpose of this design, signals are taken to be voice signals modulated with amplitude modulated single sideband (ACSB). The spectrum is assumed to have been divided up in 3.1 KHz channels, with 900 Hz guard bands between them.

The direct conversion architecture has several advantages over a standard heterodyne receiver: (1) the image frequency ($f_{\text{image}} = f_{\text{LO}} \mp f_c$ where $f_{\text{RF}} = f_{\text{LO}} \pm f_c$), potentially a source of interference in heterodyne systems, is here a frequency within the RF bandwidth – thus rejection of unwanted signals at f_{image} is infinite; (2) it possesses good selectivity because of the use of low pass filters (LPF) rather than band pass filters (BPF) as used in a heterodyne receiver, these can be designed with active op-amps and CMOS filters; (3) it has size and power consumption advantages due to the lack of IF filters; (4) the majority of the signal processing is done at very low frequencies where many high performance, special purpose, circuits already exist – thus signal processing is simple, low cost and of high performance; (5) lastly the receiver's performance is as good as or better than a comparable heterodyne receiver. From a technology development point-of-view, this receiver is ideal because it merges analog and digital signal processing, because it lends itself to monolithic realization – thereby permitting the construction of generic receiver building blocks, and, because its architecture, effectively an I/Q demodulator at RF, can work with many modulation schemes. The multipurpose nature of the direct conversion receiver's components can be used to justify the development of costly receiver LSI and VLSI building blocks.

The ability of this receiver to work with many modulation schemes merits further discussion. Historically the direct conversion receiver was proposed by Weaver in 1956 as a method to generate and receive SSB signals [1]. To demodulate SSB two baseband mixers and a summer are necessary. Accurate reconstruction of the baseband signal, or suppression of the unwanted sideband within the wanted signal band, is determined by the gain and phase balance that can be achieved between the 'I' and 'Q' channels. Weaver was able to keep the unwanted signal 20 dB to 40 dB below the wanted signal with varying levels of difficulty. The direct conversion receiver's lack of widespread acceptance at that time can probably be attributed to the unfamiliarity of its design, the need for higher received signal-to-noise (S/N) levels and the shift from SSB to FM as a preferred modulation.

FM signals can be received with the direct conversion receiver using the "sin-cosine" demodulation technique which consists of differentiator and mixer circuits. Here both gain and phase match between the channels is needed for correct demodulation. An FM receiver built with "sin-cosine" demodulation circuits was developed in 1979 by Vance et al. for radio reception at VHF; the demodulator performance is detailed in [4]. To receive AM modulation the output of the 'I' channel can be tapped, the 'Q' channel output is used to generate the control voltage for the LO. For this application phase match between 'I' and 'Q' channels is necessary to lock f_{LO1} to f_c . Finally the receiver works well with all types of digital modulation, such as QPSK and QAM, as it is effectively an I/Q demodulator placed at the RF frequency rather than at some intermediate frequency (IF) as is typical in heterodyne receivers. The direct conversion receiver then performs the dual function of conversion and demodulation in one process as opposed to heterodyne receivers which convert the RF to IF and then demodulate the digital signal with an I/Q demodulator. For these applications, phase match between channels is of primary importance to attain good QPSK reception as is amplitude match for QAM.

Gain and phase match between the 'I' and 'Q' channels affects the quality of signal reception for most modulation formats. One way to gauge the gain and phase match is to measure the suppression of the unwanted sideband in a SSB receiver. A schematic of a SSB direct conversion receiver is shown in Figure 2. Its operation can be detailed as follows. The RF signal, of center frequency f_c and bandwidth BW_{RF} , is downconverted to DC by the input mixers of both channels. The signal at the output of these mixers now spans from DC to $BW_{\text{RF}}/2$. The downconverted signal spectrum is folded over itself and no longer possesses the original RF spectral shape. The low frequency signals are then filtered, to remove any adjacent channel signals, and amplified to set the noise floor. To reconstruct the original spectrum both 'I' and 'Q' channel signals are mixed again with quadrature LO's at a frequency, f_{LO2} , equal to $BW_{\text{RF}}/2$. At the output of each of the baseband mixers the sum and difference signals created by beating the input spectrum, spanning DC to $BW_{\text{RF}}/2$, by $BW_{\text{RF}}/2$. At the mixer output the sum signal from DC to BW_{RF} and the difference signal from $BW_{\text{RF}}/2$ to DC therefore are present. For $f_{\text{RF}} > f_{\text{LO}}$ the sum signal at the output of the 'I' channel will be in phase with the sum signal at the output of the 'Q' channel and the difference signals will be 180° out-of-phase. For $f_{\text{RF}} < f_{\text{LO}}$ the reverse will occur. Thus, for $f_{\text{RF}} > f_{\text{LO}}$, when the outputs of the two baseband mixers are summed together only the sum signals will be added and the difference signals subtract. The extent to which the unwanted sideband is suppressed is an indication of the level of gain and phase matching. For analog voice signals, the level of the unwanted sideband relative to the desired sideband sets the signal-to-distortion (S/D) ratio at the output of the receiver. The extent of gain and phase match required to produce a given level of suppression can easily be calculated. For example 20 dB of suppression can be achieved by a gain match of 1.5 dB and a phase match of 5° or with a gain match of 0.5 dB and a phase match of 11°.

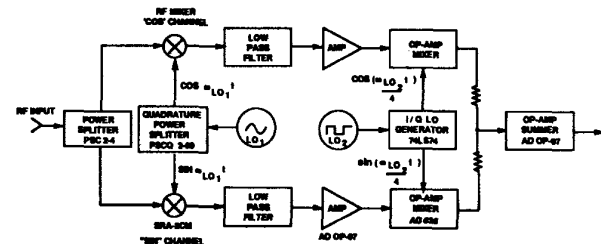
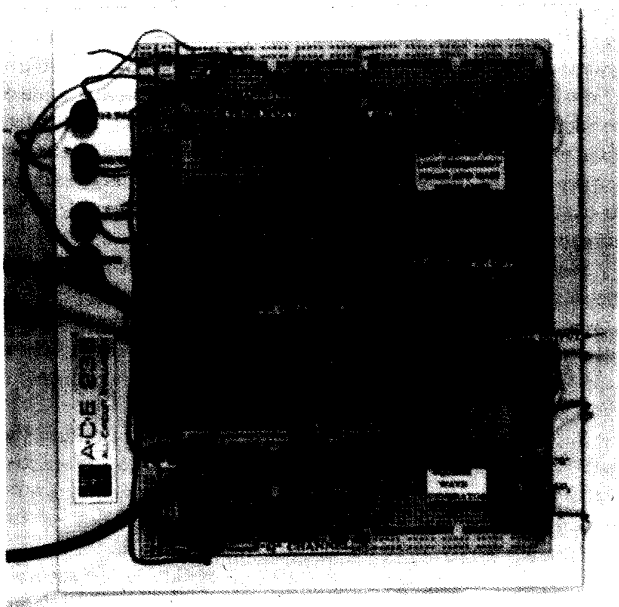
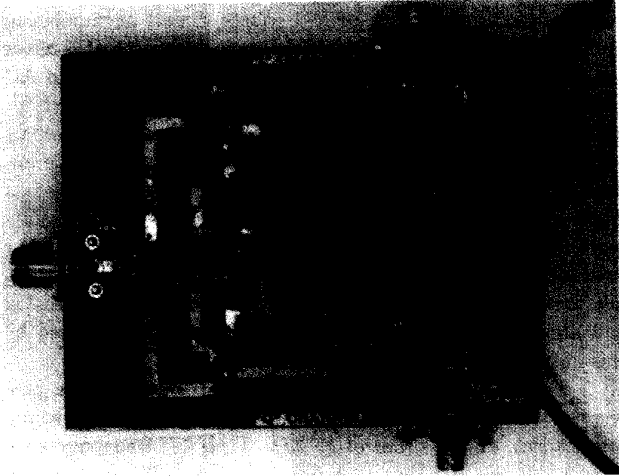


Figure 2: Schematic of the SSB receiver.

When the receiver is built with discrete parts, suppression levels similar to what was achieved by Weaver are expected. However when the direct conversion receiver is implemented with integrated circuits, so that circuits required by both channels can be built on one integrated circuit, then improved gain and phase matching between channels can be realized. Regardless of this potential improvement, it is important to remember that the S/D or S/N achievable at the output of the direct conversion receiver is not necessarily the S/N of the received signal. Higher S/N's are obtainable through the use of companding for SSB signals (ACSB) [5] and through the use of codes for digital signals.

To determine the level of gain and phase match possible for a direct conversion receiver, the SSB receiver shown in Figure 3 was built. Figure 3(a) shows the RF portion of the receiver; Figure 3(b) depicts the low-level processing circuits and the SSB demodulation circuits.

For the purposes of this experiment the SSB signal was assumed to have a 6 KHz bandwidth, its suppressed carrier was



(b) low-signal level amplifiers and SSB demodulation board

Figure 3: The direct conversion receiver implemented with discrete elements.

taken to be at 70 MHz. The RF signal could then be characterized by:

$$\begin{aligned} f_c &= 70.003\text{MHz} \\ BW_{RF} &= 6\text{KHz} \end{aligned}$$

To illustrate the generation of unwanted sidebands and to measure suppression in the direct conversion receiver, the reception of a SSB tone at

$$f_{RF, \text{tone}} = 70.005\text{MHz}$$

is examined. The outputs of the two UHF mixers, f_{oI} and f_{oQ} for the 'I' and 'Q' channels, respectively, will then be:

$$\begin{aligned} f_{oI} &= 2\text{KHz } \angle 0^\circ \\ f_{oQ} &= 2\text{KHz } \angle 90^\circ. \end{aligned}$$

The baseband mixers operate with

$$\begin{aligned} f_{LO_2} &= \frac{BW_{RF}}{2} \\ &= 3\text{KHz} \end{aligned}$$

so that the sum and difference signals produced are at 5 KHz and 1 KHz. The 5 KHz signals are in-phase with each other and the 1 KHz signals are $\approx 180^\circ$ out-of-phase with each other. When the spectrum at the output of the summer was measured, the 1 KHz signal was typically found to be 24 dB below the 5 KHz signal. This can be calculated to translate to a gain balance of less than 1 dB and a phase balance of better than 2.5° . With the low frequency amplifier and summer aligned for best channel match, a suppression of 40 dB was possible.

Design of the Low-Level Signal Processing

The low level signal processing circuits shown in Figure 1 are depicted in greater detail in Figure 4. Only one channel is shown. The RF mixer, the low frequency amplifier, and, filter comprise these low level circuits and form the front-end of the receiver. A typical RF spectra is shown at the input to the mixer, it consists of the wanted signal, W_s , and two interferers, I_1 and I_2 , adjacent to W_s and having higher power than W_s . The noise floor is illustrated by the darkened line. The spectrum at the output of each component is shown to elucidate their function and their design constraints.

The front-end components are processing the input signal while it is still at a low power level. These circuits contribute in setting the noise floor and dynamic range of the receiver contrary to the subsequent stages whose additional noise only contributes inconsequentially to the overall noise. To guarantee the greatest dynamic range possible, the low frequency amplifier possesses the minimum gain necessary to reduce filter noise components to an acceptable level.

Receiver noise temperature is given at the receiver input as a function of frequency as:

$$\begin{aligned} T_{rec}(f) &= T_{mixer}(f) + C_L \cdot T_{amp}(f) \\ &\quad + C_L \cdot \frac{T_{filter}(f)}{G_{tot,amp}} \end{aligned} \quad (1)$$

where T_{mixer} , T_{amp} , and, T_{filter} are the noise temperature of the mixer, amplifier, and, filter respectively, $G_{tot,amp}$ is the low

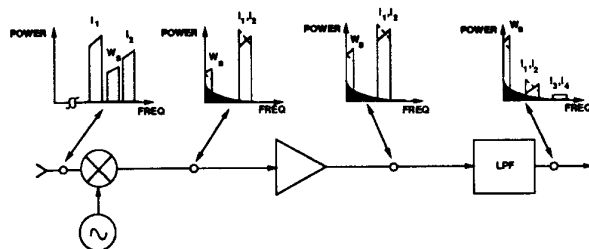


Figure 4: Front-end of one channel of the direct conversion receiver with typical spectrum plots.

frequency amplifier gain (this amplifier may be made of several stages of gain G_{amp}), and C_L is the mixer's conversion loss. All noise sources are a function of frequency due to the dominance excess noise term.

Noise figure is determined from noise temperature according to:

$$NF = 10 \cdot \log \left(1 + \frac{T}{290} \right). \quad (2)$$

When conjugate matching is used between components the gain of the front-end circuits can be written in terms of their individual gains as:

$$G_{rec} = \frac{G_{tot,amp} \cdot G_{filter}}{C_L}. \quad (3)$$

1. Mixer Design. Three design goals must be kept in mind while designing the direct conversion mixer: (1) efficient translation from the RF to f_o ; (2) low excess noise or 1/f noise at the mixer output; (3) impedance transformation from $R_{S_{RF}}$ to R_L . The first objective listed is common to all mixer designers especially for receivers with mixer front-ends. Translation of the input signal from the RF frequency at the mixer input port to some output frequency is specified by the mixer's conversion loss. Conversion loss is defined as:

$$C_L = \frac{\text{Power Available from the Source}}{\text{Power Delivered to the Load}}.$$

Minimization of mixer noise figure is the second criterion for a direct conversion mixer as the mixer generated noise, along with that generated by the amplifier and filter cascade, sets the noise floor of the receiver. The noise at the mixer output is due to shot noise, thermal noise and excess noise. Excess noise, or 1/f noise, is of particular importance in the direct conversion receiver: it is the dominant noise source at the low frequencies at which much of the receiver's signal processing is carried out. Excess noise is generated by all devices, active and passive alike, such as diodes, transistors, resistors etc. This noise source can be modelled as a noise current of mean squared value:

$$\overline{i_{ex}^2} = \frac{K \cdot I_d^a \cdot \Delta f}{f^b}$$

where K , a , and, b are device dependent parameters, $a \approx 0.5 - 2.0$ and $b \approx 1.0$. The noise spectrum of a typical device with shot and excess noise is shown in Figure 5. The 1/f frequency knee, or frequency where the excess noise contribution is equal to that caused by shot and thermal noise, is marked on the graph. Because this noise occurs in the band to which the RF signal has been translated, minimization of its magnitude is particularly important for the direct conversion receiver. The signal and noise spectrum at the mixer output is depicted in Figure 4.

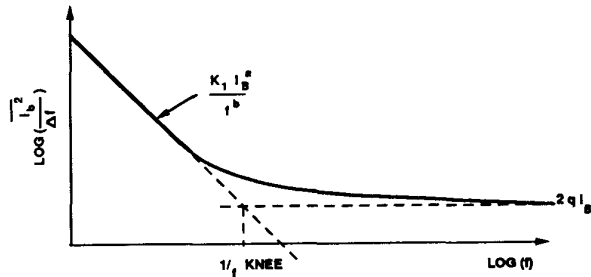


Figure 5: Noise spectrum, due to shot and excess noise, of a typical device.

Lastly direct conversion mixers have the unusual requirement that they must provide an impedance transformation from the low input impedance of the antenna (50 Ω or 75 Ω) to the high source impedance desired by the subsequent low frequency amplifier. As will be discussed, typical bipolar op-amps possess lowest noise temperature when they are driven by source impedances on the order of 10 K Ω .

This problem of 1/f noise generated by all front-end components and the problem of DC offsets signals accumulating throughout the receive chain and becoming a source of receiver instability lead to the idea of using a DC notch filter and AC coupled op-amps in the 'I' and 'Q' channels. This DC notch filter at baseband effectively removes the signal power previously centered about f_c . Phase lock loop circuitry will need to be implemented upstream from the notch filter. Certain modulation types may be unaffected by the filter's presence, others may require special generation circuits for use with this receiver. For example, techniques developed for fading channels such as transmit tone in band can be applied for generation of both analog and digital signals [6]. Determining the bandwidth required by this notch filter is one of the goals of this work.

2. Low Frequency Amplifiers. Standard bipolar amps possess the lowest noise temperature when operated with high source impedances, on the order of 10 K Ω . Their 1/f frequency knee occurs between 100 Hz and 1 KHz. As it is difficult to design low C_L RF mixers that can translate to such high R_L , the major impetus of this work was to identify noise mechanisms and circuit requirements so that low noise amplifiers could be designed to work with source impedances of 3 K or less, ie. those typical of RF mixers outputs, or to modify op-amps to perform in this range. The noise performance of these amplifiers must be identified as a function of frequency so that the DC notch filter can be constructed with a bandwidth sufficiently narrow to minimize its impact on the signal spectrum yet large enough so that the remaining noise in the signal band was set at an acceptable level.

Second the gain of the amplifier stage must be calculated to insure high receiver dynamic range; it cannot be too high lest the power in the adjacent channels, denoted in Fig. 4 by I_1 and I_2 , saturate the filter stage. Third the 1/f frequency knee of these amplifiers must be identified so that the bandwidth required of the DC notch filters can be determined.

3. Active Filter Design. These circuits serve to perform the first stage of filtering. Their bandwidth is that of the wanted signal ($BW_{filter} = \frac{BW_{SE}}{2}$). Because they are cascaded by a subsequent filtering stage as shown in Fig. 1 they do not set the receiver selectivity alone but act primarily to reduce the level of the out-of-band interferers so that these signals do not saturate the next filter stage. Reduction of adjacent channel interferers 900 Hz away from the edge of band of the wanted signal by 30 dB and of the subsequent channel interferer by 50 dB is desired. To reduce filter noise temperature it is implemented with bipolar op-amps rather than with CMOS circuits. Receiver selectivity is produced by both low level and high level filters.

Receiver Component Design

1. Direct Conversion Mixer.

A new time domain based technique for computer-aided mixer analysis and design has been developed in part to address problems specific to the design of a direct conversion mixer and in part to provide mixer designers with a different view on mixer

optimization. Once the mixer diode parameters are given and the mixer circuit has been specified, this tool calculates the voltage and current waveforms at each of the circuit's node. This is done by employing SPICE [7], a circuit simulator program, to arrive at the steady state solution for the network equations. To quantify conversion loss performance and to generate small signal impedances, Fourier transforms are taken at various nodes. With this technique the interaction of diode and mixer circuit can be understood and conversion loss performance optimized for realistic mixer circuits. (See [8] for a description of the mixer design tool.)

Previous mixer analysis techniques have been better suited to analysis of ideal circuits where the output load at each mixer produced frequency ($m f_{RF} \pm n f_{LO}$) are specified [9]. These techniques are ideally suited to the design of waveguide mixers or mixers where f_{RF} differs greatly from f_{LO} so that each mixer spur can be easily separated and matched by a simple circuit that are not necessarily very frequency selective.

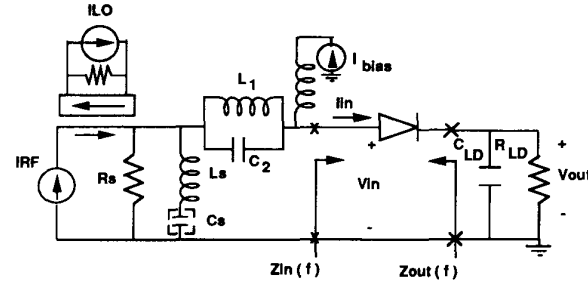
The time domain based mixer design tool has been used to optimize mixer performance, both conversion loss and impedance transformation, with practical mixer diode having both series resistance and capacitance. Medium barrier p-type Si Schottky diodes are used as they are thought to possess low $1/f$ noise. Mixers have been designed with devices whose barrier capacitance at zero bias, C_{j0} , is as great as 1.0 pF; the maximum typically encountered for UHF mixer diodes. Two mixer types have been optimized: single-ended and single-balanced mixers. Figure 6(a) depicts the optimized single-ended mixer. The local oscillator source is applied to the circuit via a directional coupler. The optimized single-balanced mixer is illustrated in Fig. 6(b). Balanced mixers differ from single-ended mixers in several ways: first the output signal has fewer spectral components as it is isolated from the LO source and its harmonics (therefore providing greater isolation of the RF and LO signals at the output port); second the mixer has fewer noise components at its output as the amplitude modulated component of the LO noise is cancelled internally by the balanced circuitry; third good circuit VSWR can be obtained. For these reasons the added circuit elements and active components of balanced mixers are often tolerated.

Table 1 lists the optimized performance of two single-ended mixers with C_{j0} of 0.25pF and 1.0pF and the performance of a single-balanced mixer with a C_{j0} of 0.25pF. Single-ended mixers have a phasing circuit (L_1 , C_2) to achieve low C_L ; balanced mixers have both phasing circuit (L_1 , C_2) for RF signal and driving waveform circuit (L_3 , C_4) for LO signal to achieve low C_L .

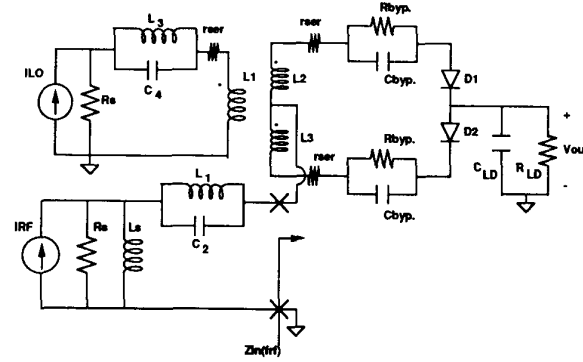
Noise temperature estimates at the mixer output frequency are based on mixer noise analysis for shot and thermal noise processes as detailed by Maas [10]. Only single-ended mixer noise temperatures can be calculated. The embedding network is assumed to be noiseless. The analysis makes use of the Fourier coefficients of the diode's small signal barrier resistance, $R_B(t)$, and barrier capacitance, $C_B(t)$, to calculate the noise power at the output termination. This method for evaluating mixer noise temperature does not include $1/f$ noise. The balanced mixer noise temperature has been estimated from Alpha manufacturer's characterization of $1/f$ diode noise¹ and from estimates of circuit effects on mixer noise. The latter is expected to be low as the mixer circuit parametrically pumps the barrier capacitance to achieve low conversion loss. The worst-case noise temperature for the balanced mixer is believed to be ≈ 500 K.

Better characterization of mixer noise over frequency remains to be done.

From Table 1 the conversion loss of the balanced mixer can be seen to be lower than that of the single-ended mixer. It is also capable of translating from a lower input impedance (73 Ω) to a higher output load impedance (2K Ω).



(a) single-ended mixer



(b) single-balanced mixer

Figure 6: Schematics of the two mixer types simulated.

2. Low frequency, low noise amplifier.

The goal of this work was to identify transistor noise mechanisms and circuit characteristics that determine the optimum source impedance for minimum amplifier noise, $R_{N_{opt}}$, and to find the variation of noise figure and $R_{N_{opt}}$ over frequency. The noise model for an amplifier consists of a current noise source, $\overline{i_i^2}$, across the input and a voltage noise source, $\overline{v_i^2}$, in series with the input to an ideal noiseless amplifier. The noise temperature of the amplifier, F_{amp} , is then defined as:

$$F = 1 + \frac{\overline{v_i^2}}{4kTR_s\Delta f} + \frac{\overline{i_i^2}R_s}{4kT\Delta f}. \quad (4)$$

From the above equation the optimum R_s for minimum noise temperature, $R_{N_{opt}}$, can be found to be:

$$R_{N_{opt}} = \frac{\overline{v_i^2}}{\overline{i_i^2}}.$$

Using the $\overline{v_i^2}$ and $\overline{i_i^2}$ values for two popular op-amps, the Analog Devices OP-07 and OP-27, an idea of the noise figure - R_s trade-off may be obtained by using Eqn. 4 to calculate amplifier noise figure. The results are shown in Figure 7 for operation at 10 Hz and 1 KHz. The results shown correspond to the minimum op-amp noise figure attainable as no feedback around the amp is assumed. (Actual op-amps would have slightly higher

¹Correspondance with Stanley Howe of Alpha Industries Inc. in March 1987.

noise figures.) At large R_s , $\overline{v_i^2}$ is the dominant noise source, at low R_s , $\overline{i_i^2}$ dominates. From Fig. 7 $R_{N_{opt}}$ can be seen to be 30K at 10Hz and 75K at 1KHz for the OP-07 with corresponding amplifier noise figures of 1.6 dB and 0.6 dB, respectively. The OP-27 is a ultra-low noise precision op-amp; it possesses a $R_{N_{opt}}$ of 2.2K at 10 Hz and 8K at 1KHz with corresponding noise figures of 2.6dB and 0.64dB. To understand if better noise figures are possible for $R_s < 8K$ with other bias and circuit designs, as will be necessary to optimize the loading of the low conversion loss direct conversion mixer, the noise mechanisms that set amplifier performance must be examined.

Table 1: Direct Conversion Mixer Performance

C_{j_o}	Single-Ended Mixer		Single-Balanced Mixer
	0.25 pF	1.0 pF	0.25 pF
Bias and LO Drive:			
I_{LO} Bias	13mA	20mA	13mA
Bias	13mA	30mA	-0.5 V
RF source impedance:			
$R_{S_{RF}}$	197 Ω	66 Ω	73 Ω
L_S	3.5 μ H	1.2 μ H	0.13 μ H
RF matching circuit:			
L_1	0.11 μ H	0.04 μ H	0.07 μ H
C_2	0.03 pF	0.12 pF	0.04 pF
LO matching circuit:			
L_3	none	none	0.08 μ H
C_4	none	none	0.04 pF
Output impedance:			
R_L	1.5 K Ω	500 Ω	2 K Ω
C_{LD}	3 pF	3 pF	3pF
Performance:			
C_L	3.1dB	4.3dB	2.1 dB
$\frac{R_L}{R_{S_{RF}}}$	7.6	7.6	27.4
T_{mizer}	135 K	265 K	$\approx$ 500 K

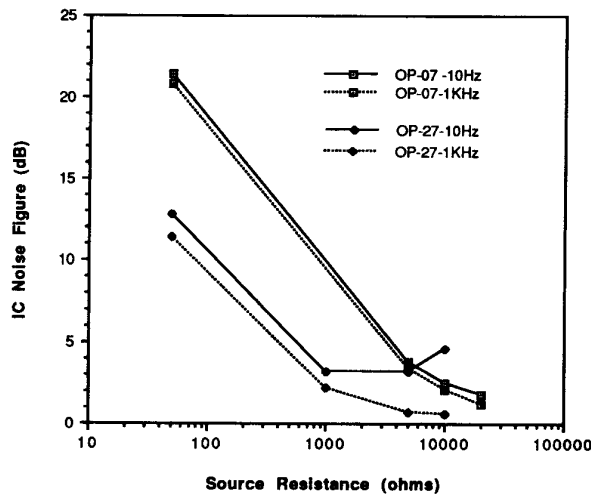


Figure 7: Best case noise figure of the Analog Devices OP-07 and OP-27.

The differential amplifier is chosen as the basic building block for the low frequency amplifier because of its rejection of signals which appear on both input ports. Differential amplifiers are commonly used as input stages for op-amps and hence will provide an understanding of their performance. Lastly, because their symmetrical design is less susceptible to thermal drifts causing performance changes, these amplifiers are often used where operation at low frequencies (and DC) is desired [11]. The three stage low frequency amplifier is illustrated in Figure 8. The differential amplifier gain stage is outlined. Transistors Q_1 and Q_2 are biased by a transistor current source, created by Q_3 and Q_4 . This is the common form of op-amp bias as transistor current sources provide increased circuit performance insensitivity to temperature and power supply variations than emitter resistors and require less space on the integrated circuit [12].

The voltage noise source at the input of the differential amplifier, $\overline{v_{N_{in}}^2}$, can be written as:

$$\begin{aligned} \overline{v_{N_{in}}^2} = & \left[\overline{v_{R_s}^2} + \overline{v_{b_1}^2} + (R_s + r_b + R_{E_1})^2 \cdot \overline{i_{b_1}^2} \right. \\ & + \left(\frac{R_s + r_b + r_{\pi} + R_{E_1}}{\beta_o} \right)^2 \cdot \overline{i_{c_1}^2} \\ & + \left(\frac{R_s + r_b + r_{\pi} + R'_{E_1}(\beta_o + 1)}{\beta_o} \right)^2 \cdot \overline{i_{R_c}^2} \left. \right] \cdot \left(\frac{2r_{\pi}}{2r_{\pi} + R_s} \right) \\ & + \overline{v_{b_2}^2} + (r_b + R_{E_2})^2 \cdot \overline{i_{b_2}^2} \\ & + \left(\frac{r_b + r_{\pi} + R_{E_2}}{\beta_o} \right)^2 \cdot \overline{i_{c_2}^2} \\ & + \left(\frac{r_b + r_{\pi} + R'_{E_2}(\beta_o + 1)}{\beta_o} \right)^2 \cdot \overline{i_{R_c}^2} \end{aligned} \quad (5)$$

where

$$\begin{aligned} R'_{E_1} &= \left(\frac{r_{b_2} + r_{\pi_2}}{\beta_2 + 1} \right) \parallel R_{EE} \\ R'_{E_2} &= \left(\frac{R_s + r_{b_1} + r_{\pi_1}}{\beta_1 + 1} \right) \parallel R_{EE} \\ R_{EE} &= r_{out_4} = \frac{V_A}{I_{c_4}} \end{aligned}$$

These equations stress the importance of choosing a device with a low series resistance, r_b , and a high β to minimize $\overline{v_{N_{in}}^2}$. Device parameters for a super beta differential transistor pair, the National Semiconductor LM 394, are used for transistors Q_1 to Q_4 . The collector current dependence of r_b and β is included

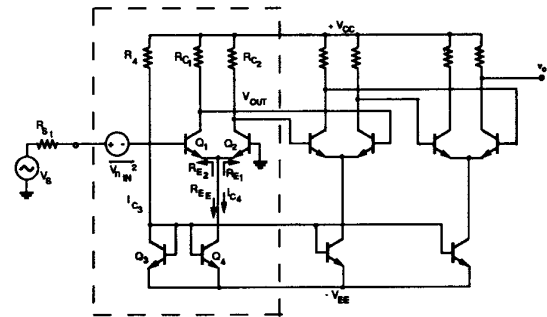
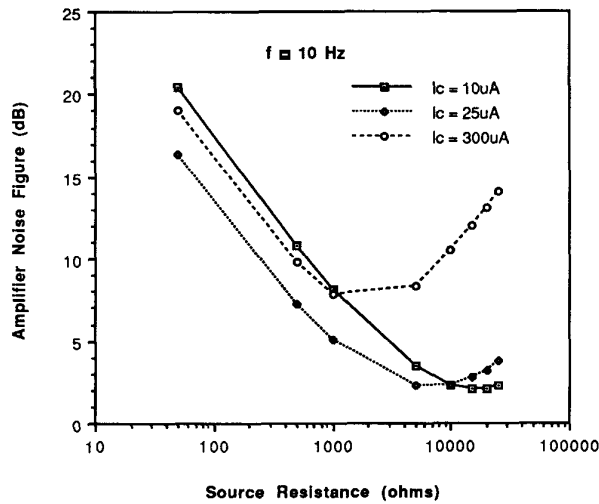


Figure 8: Low frequency amplifier implemented by a cascade of three differential amplifiers. The outlined input differential pair with transistor current source is fundamental gain block studied.

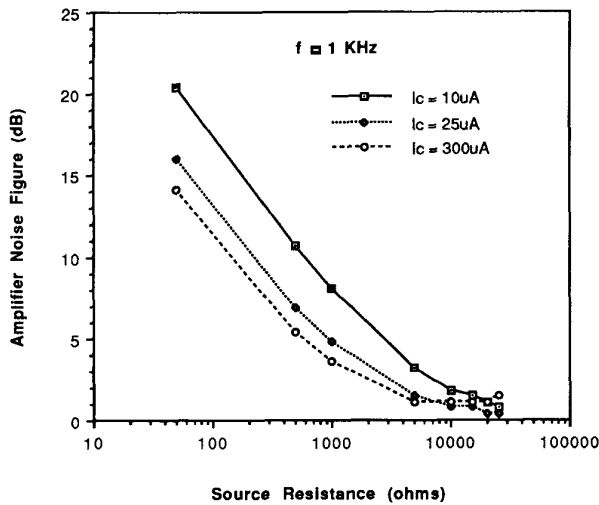
in the device model. Using this transistor in the circuit depicted in Fig. 8, the noise figures shown in Figures 9 are obtained; Fig. 9(a) gives the performance over R_s at 10 Hz, Fig. 9(b) charts performance at 1 KHz.

The frequency dependance of $I_{c_{opt}}$ and $R_{N_{opt}}$ for minimum noise figure is apparent from Fig.9. At 10 Hz, NF_{min} is 2.0 dB with $R_{N_{opt}}$ between 15 K and 20 K and a $I_{c_{opt}}$ of 10 μ A. At 1 KHz, NF_{min} is 0.4 dB with $R_{N_{opt}}$ between 20 K and 25 K and a $I_{c_{opt}}$ of 25 μ A.

Op-amps are typically biased at an I_c of 5 μ A for lower power consumption; they are generally intended for operation at $f > 100$ Hz, thus requiring a high R_s to minimize noise figure performance. To operate at a lower R_s without suffering a large penalty in increased noise figure, Fig. 9 indicates that one can operate the transistors at a higher bias. For example, at 10 Hz NF is 2.3 dB when a R_s of 5K is used with an I_c of 25 μ A (only 0.25dB higher than NF_{min}), or, at 1 KHz NF is 2.3 dB when a R_s of 5K is used with an I_c of 25 μ A (0.6dB higher).



(a) Performance at 10 Hz



(b) Performance at 1 KHz

Figure 9: Noise figure vs. R_s performance for the differential amplifier shown above.

To optimize operation with the optimized direct conversion mixers whose design is listed in Table 1, the differential amplifier can be analyzed for R_s equal to 500 Ω , 1.5 K and 2.0 K, the optimum load impedances for the two single-ended mixers and the balanced mixer. The required I_c for optimum noise figure are tabulated in Table 2 along with the noise temperature results.

Table 2: Gain and Noise Performance of the Gain Stage

R_s	$I_{c_{opt}}$	NF_{amp}	G_{amp}	R_{out}
$f = 10$ Hz:				
500 Ω	25 μ A	7.2	-50	52K
1.5 K Ω	25 μ A	4.0	-50	52K
2.0 K Ω	25 μ A	3.4	-50	52K
$f = 100$ Hz:				
500 Ω	300 μ A	5.9	-600	50K
1.5 K Ω	300 μ A	3.2	-600	50K
2.0 K Ω	100 μ A	2.8	-200	51K
$f = 1$ KHz:				
500 Ω	1 mA	5.3	-2000	46K
1.5 K Ω	300 μ A	2.8	-600	50K
2.0 K Ω	300 μ A	2.3	-600	50K

The large difference in optimum I_c for minimum noise figure is visible as the frequency of operation is varied. $I_{c_{opt}}$ is 25 μ A at 10Hz and 0.3 μ A at 1KHz. Thus if the notch filter is to be very narrow to minimize signal distortion, eg. 0 - 10 Hz, then the differential amplifier would have to be biased at low currents ≈ 25 μ A. However if a filter from 0 - 100 Hz can be tolerated then the appropriate bias current to minimize noise would probably be ≈ 100 μ A. Minimizing current is necessary to conserve power and maintain good performance stability over temperature and power supply fluctuations. The dependance of optimum bias and minimum noise figure on R_s is also illustrated in Table 2. At any of the frequencies the following two trends are observed: (1) more current is required to achieve $NF_{amp_{min}}$ as $R_s \downarrow$; (2) $NF_{amp_{min}} \uparrow$ as $R_s \downarrow$.

As the balanced mixer has the best conversion loss, the highest impedance transformation ratio, and, produces the lowest f_{amp} in addition to the inherent benefits of balanced structures it will be chosen as the prototypical direct conversion mixer. Table 3 gives the performance of the differential amplifier when driven by a 2K Ω source resistor, such as will be used with the balanced mixer, at two bias levels, 25 μ A and 100 μ A. The differential mode gain obtained at all frequency when I_c is equal to 25 μ A is -50; the power gain is 24 or 13.8 dB; R_{out} is 52 K Ω . When I_c is equal to 100 μ A the differential mode gain is -200, the power gain is 370 or 25.7 dB, and, R_{out} is 51 K Ω .

Table 3: Noise Figure of the Gain Block when Driven by a 2K Ω R_s at Two Bias Levels

Frequency	$I_c = 25 \mu A$		
	NF_{amp}	F_{amp}	$NF_{amp} - NF_{amp_{opt}}$
10 Hz	3.4 dB	340 K	0 dB
100 Hz	3.0 dB	290 K	0.2 dB
1 KHz	3.0 dB	290 K	0.7 dB
Frequency	$I_c = 100 \mu A$		
	NF_{amp}	F_{amp}	$NF_{amp} - NF_{amp_{opt}}$
10 Hz	5.5 dB	770 K	2.1 dB
100 Hz	2.8 dB	270 K	0 dB
1 KHz	2.5 dB	240 K	0.25 dB

3. Active filter.

The multiple loop feedback filter depicted in Figure 10 was analyzed for gain, noise, and, gain shape performance as a function of frequency. Fig. 10(a) shows the design of one op-amp stage. Fig. 10(b) gives the block diagram of the three filter cascade. The op-amp was assumed to be a 741 type op-amp; typical 741 values for $\overline{v_n^2}$ and $\overline{i_n^2}$ were used to calculate the noise performance of the overall filter. The gain of each stage was set to 10 dB in order that the out-of-band or interfering signal power could be reduced prior to saturating any of the stages. All filter stages are assumed to be identical to improve the modularity of the receiver design. Consequently the overall in band gain shape possesses some roll-off with frequency.

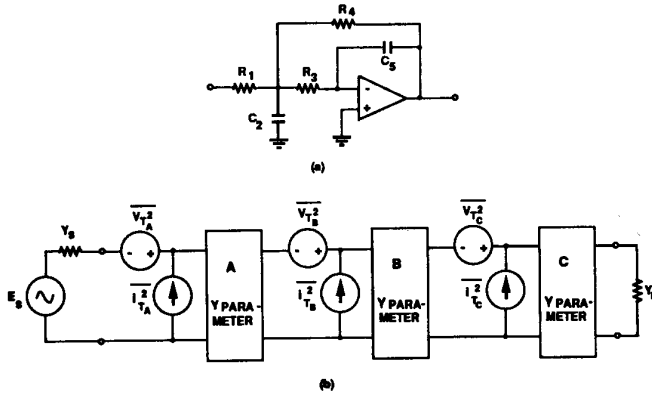


Figure 10: Active filter block diagram: (a) the multiple loop feedback filter stage; (b) the three stage filter cascade.

To analyze the filter behavior, the wanted signal was assumed to have a signal power of 2 nW in a bandwidth of 1.55 KHz, equivalent to $\frac{BW_{RF}}{2}$ of a typical 3.1 KHz voice signal. Two interferers, I_A and I_B are taken to occupy the two next adjacent channels, 4 KHz and 8 KHz, respectively, away from the center frequency of W_s . They are equal in power to W_s , having 1 nW in the channel bandwidth of 3.1 KHz. Noise analysis takes into account thermal noise due to the feedback resistances of each stage and the load impedance.

The feedback elements are chosen to be:

$$\begin{aligned} R_1 &= 23.8 K\Omega; \\ C_2 &= 0.0047 \mu F; \\ R_3 &= 105.6 K\Omega; \\ R_4 &= 75.3 K\Omega; \\ C_5 &= 0.00028 \mu F. \end{aligned}$$

When the filter is driven with a source resistor of 50 K Ω , corresponding to the output of the low frequency amplifier, the filter performance depicted in Figure 11 is obtained. In this figure the spectrum of W_s , I_A , and I_B are depicted at the output of the filter cascade. The load resistor is assumed to be 10 K Ω (increasing R_L give better performance). The signal-to-noise ratio in the signal band is calculated to be 45.1 dB, in the DC to 10 KHz band it is 44.9 dB. The amount of 1/f noise (calculated to within 0.0001 Hz of DC) can be gauged by the following comparison: the average noise temperature in the DC to 1.55 KHz signal band is 88000 K; in the 50 Hz to 1.55 KHz band it is 64000 K. The signal-to-interferer A ratio is 34.5 dB and the signal-to-interferer B ratio is 81.5 dB. As can be seen from Fig. 11, the power level of I_B at the filter output is comparable to the noise

power floor. Noise performance and filter selectivity is close to optimum with the choice of this source resistance.

The filter noise power possesses a very nonlinear spectrum. Its components are plotted in Figure 12. The current noise source of the last filter stage is seen to be a major contributor to overall noise. The dominant noise source however is due to the joint noise contribution from the two preceding stages as shown by the "input term" plot.

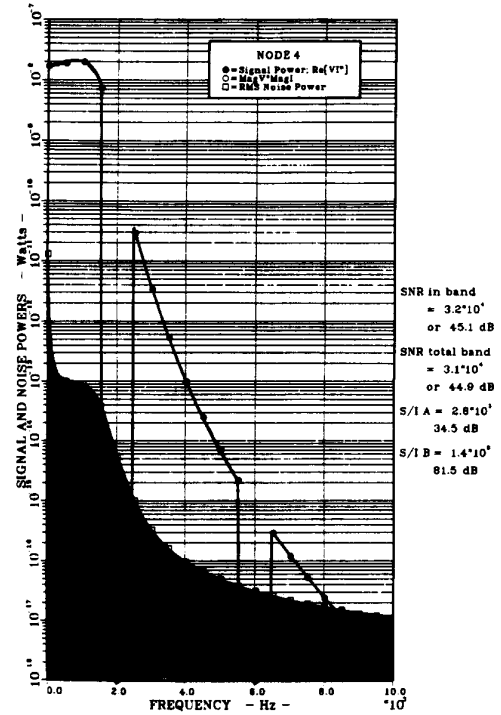


Figure 11: Multiple loop feedback filter characteristics.

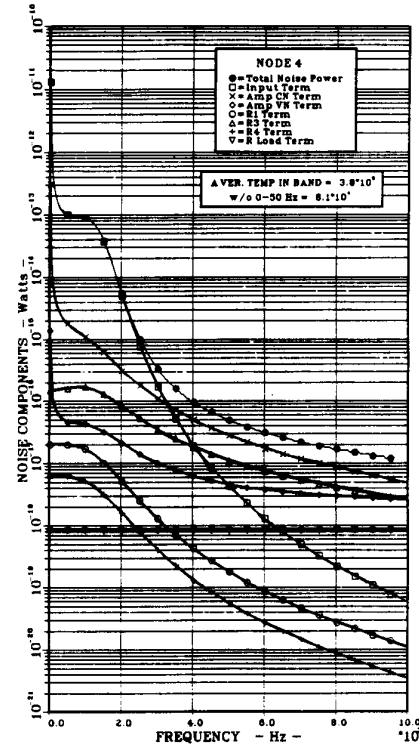


Figure 12: Components of filter noise spectrum.

Filter noise figure and gain in the signal band are given in Table 4. A comparison of worst-case noise temperatures for the balanced mixer (500 K estimated), the one-stage differential amplifier (770 K max. at 10 Hz when biased at 100 μ A) with that of the filter below highlights the magnitude of its noise power over the signal band.

Table 4: Active Filter Performance

Frequency	Gain	NF_{filter}	F_{filter}
25 Hz	27.2 dB	34.3 dB	770,000 K
525 Hz	27.7 dB	22.3 dB	49,000 K
1025 Hz	27.9 dB	21.9 dB	45,000 K
1525 Hz	23.6 dB	22.7 dB	53,000 K

A 1.55 KHz cut-off filter was built along the design of the multiple loop feedback filter stage described above. It was implemented with Burr-Brown UAF 41 IC's. The single stage gain performance was comparable to that of the single stage analyzed above.

Overall Receiver Performance

Receiver gain, noise, and first stage selectivity performance can be calculated from component specifications. Eqns. 1 and 3 can be used to calculate the receiver gain and noise figure. The front-end circuits of the direct conversion receiver consists of the balanced mixer, several gain stages, and the active filter. They have been designed to conjugately match each other. Conversion loss for the balanced mixer is 2.1 dB, its noise temperature has been estimated to have a worst-case value of 500 K. The low frequency amplifier is built from the differential gain stages analyzed above. The fewer gain blocks are used the better dynamic range the receiver will have when adjacent channel signals are present. However several gain blocks may be necessary to reduce the noise contribution of the active filter to the overall receiver noise temperature. Each gain stage has a power gain of 24 (or 13.8 dB) when operated at an I_c of 25 μ A and 370 (or 25.7 dB) when operated at an I_c of 100 μ A. The noise temperature over frequency of this gain stage is given in Table 3. Operation at 25 μ A is employed when a 0 - 10 Hz notch filter is used; operation at 100 μ A is employed when a 0 - 100 Hz notch filter is permitted. The active filter noise and temperature performance is given in Table 4; it can attenuate an adjacent channel interferer by 34.5 dB and an interferer two channels over by 81.5 dB.

Table 5 gives receiver noise figure and gain performance for operation with a 10 Hz wide notch filter and a 100 Hz wide notch filter. In the former case three stages of gain are necessary to keep the receiver noise figure under 7 dB; in the latter one stage of gain is enough. If the signal characteristics can be designed to operate with a 200 Hz wide notch in their spectrum at f_c , then this is the favored receiver construction.

As shown in Fig. 1, receiver selectivity is established by the bipolar op-amp filter in the low-level processing circuits and the CMOS filters in the high-level processing circuits. Overall selectivity, or adjacent channel rejection, is expected to be 70 - 90 dB.

Table 5: Receiver Gain and Noise Performance

	Notch Filter 0 - 10 Hz Gain Stage biased at 25 μ A			
	2 gain stages		3 gain stages	
	10 Hz	1 KHz	10 Hz	1 KHz
Gain	52.7 dB	53.4 dB	66.5 dB	67.2 dB
NF_{rec}	10.9 dB	6.9 dB	7.0 dB	6.5 dB
	Notch Filter 0 - 100 Hz Gain Stage biased at 100 μ A			
	1 gain stage			
	10 Hz		1 KHz	
Gain	N/A		60.3 dB	
NF_{rec}	N/A		6.8 dB	

Conclusions

This paper has reviewed the overall design challenges of a direct conversion receiver. Gain and phase balance between channels has been measured on a receiver implemented with discrete components and found to be adequate for a majority of communications applications. Table 6 compares receiver characteristics for the direct conversion receiver against those of a typical mixer front-end heterodyne receiver. The direct conversion receiver possesses better noise figure and selectivity with less complexity and lower cost. The dramatic advantage in selectivity is due to the use of LPF filters realized with bipolar filters and high performance CMOS circuits rather than conventionally designed BPF at various IF frequencies.

Table 6: Comparison of Direct Conversion Receivers and Typical Heterodyne Receivers for Mobile Radio Applications

	Direct Conversion Receiver	Heterodyne Receiver
NF_{rec} (mixer front-end)	7.0 dB	12 dB
Selectivity	70 - 90 dB	60 - 80 dB
Complexity	Simple	High
Cost	Low	High

Many topics pertinent to the general use of the direct conversion receiver still remain to be explored such as precise characterization of mixer temperature performance with frequency, the design of LO generation circuits, and certain modulation specific demodulation circuits. This work has examined the noise and impedance conditions for optimum I/Q channel performance, developed low conversion loss mixer design techniques, and studied low noise amplifier and filter design. Hopefully this work will contribute to the growing awareness of the advantages of this type of receiver architecture and will lead to its implementation at higher frequencies and with a greater number of signal formats.

References

- [1] Weaver, Donald K. Jr., "A Third Method of Generation and Detection of Single-Sideband Signals," *Proceedings of the IRE*, December, 1956, pp. 1703-1705.
- [2] Vance, I. A. W., "Fully Integrated Radio Paging Receiver," *IEEE Proceedings*, Vol. 129, Pt. F, No. 1, February, 1982, pp. 2-6.

- [3] Treleaven, D. and Wadsworth, Doug, "FSK Receiver Uses Direct Conversion," *RF Design*, Cardiff Publishing Company, July 1986, pg. 30 - 38.
- [4] Goatcher, J. K., Neale, M. W., and Vance, I. A. W., "Noise Considerations in an Integrated Circuit VHF Radio Receiver," *Proceedings of Conference on Radio Receivers and Associated Systems*, IERE No. 50, 1981, pp. 49 - 59.
- [5] R. M. Wilmotte and Lusignan, B. B., "Spectrum-Efficient Technology for Voice Communications," *UHF Task Force Report FCC/OPP UTF 78-01 (PB 278340)*, FCC, February, 1978.
- [6] McGeehan, J. P. and Bateman A. J., "The Use of Transparent Tone-In-Band (TTIB) for Coherent Data Schemes with Particular Reference to Single Sideband Modulation," *IEEE Trans. on Comm.*, COM-32, 1984, pg. 81-87.
- [7] Vladimirescu, A., Newton, A. R. and Pederson, D. O., *SPICE Version 2.G.1 User's Guide*, Technical Report, Dept. of Electrical Engin. and Computer Science, Univ. of Calif., Berkeley, 1980.
- [8] Estabrook, P. and Lusignan, B. B., "A Mixer Computer-Aided Design Tool Based in the Time Domain," *IEEE Microwave Theory and Techniques Symposium*, 1988, pg. 1107- 1110.
- [9] Held, Daniel N. and Kerr, Anthony R., "Conversion Loss and Noise of Microwave and Millimeter-wave Mixers: Part I and II," *IEEE Trans. on Microwave Theory and Techn.*, MTT-26, Feb. 1978, pg. 55-61.
- [10] Maas, Stephen A., *Microwave Mixers*, Artech House Inc., 1986.
- [11] Horowitz, Paul and Hill, Winfield, *The Art of Electronics*, Cambridge University Press, 1983.
- [12] Gray, Paul R. and Meyer, Robert G., *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, 1984.