UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK INC.,

Petitioner,

v.

PARKERVISION, INC.,

Patent Owner.

Case No.: IPR2024-00796
U.S. Patent No. 7,483,686

DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.

2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.

3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in

Machine Readable Catalog (herein referred to as "MARC") code and contain information such as a physical description of the material, metadata from the material's publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item's MARC record indicates the date of an item's public availability.

5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book's physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library's collection, it is my experience that an item's 008 field accurately indicates the date of an item's public availability.

6. I have reviewed Exhibit 1006, "S-band digital downconverter for radar applications based on a GaAs MMIC fast sample-and-hold" by G. Avitabile, A. Cidronali and G. Manes as published in *Proceedings of IEE Circuits, Devices and Systems*, 1996.

7. Attached hereto as Appendix AVITABILE01 is a true and correct copy of the MARC record for *Proceedings of IEE Circuits, Devices and Systems* as held by the Penn State University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix AVITABILE01 accurately describes the title, author, publisher, and ISSN number of *Proceedings of IEE Circuits, Devices and Systems.* The 'Availability' field of this record visible on page 2 indicates this collection includes the 1996 edition of *Proceedings of IEE Circuits, Devices and Systems* containing "S-band digital downconverter for radar applications based on a GaAs MMIC fast sample-and-hold." In comparing Exhibit 1006 to Appendix AVITABILE01, it is my determination that Exhibit 1006 is a true and correct copy of "S-band digital downconverter for radar applications based on a GaAs MMIC fast sample-and-hold" by G. Avitabile, A. Cidronali and G. Manes as published in *Proceedings of IEE Circuits, Devices and Systems* 1996.

8. The 008 field of the MARC record in Appendix AVITABILE01 indicates the date of record creation. The 008 field of Appendix AVITABILE01 indicates the Penn State University library first acquired these proceedings as of April 6, 1994 and secured new copies of these proceedings in perpetuity until 2006. Considering this information, it is my determination that *Proceedings of IEE Circuits, Devices and Systems* 1996 and therefore "S-band digital downconverter for radar

applications based on a GaAs MMIC fast sample-and-hold" was made available to the public shortly after its initial release in December 1996.

9. I have reviewed Exhibit 1005, a dissertation entitled *The direct conversion receiver: Analysis and design of the front-end components* by Polly Estabrook.

10. Attached hereto as Appendix ESTABROOK01 is a true and correct copy of *The direct conversion receiver: Analysis and design of the front-end components*. I secured this digital copy myself from ProQuest. In comparing Exhibit 1005 to Appendix ESTABROOK01, it is my determination that Exhibit 1005 is a true and correct copy of *The direct conversion receiver: Analysis and design of the front-end components* by Polly Estabrook.

11. Attached hereto as Appendix ESTABROOK02 is a screen capture of the ProQuest data entry for *The direct conversion receiver: Analysis and design of the front-end components*. I secured this record myself from ProQuest. Appendix ESTABROOK02 effectively indexes *The direct conversion receiver: Analysis and design of the front-end components* and was found in the ProQuest database, a digital catalog featuring advanced search tools for database users.

12. Attached hereto as Appendix ESTABROOK03 is a true and correct copy of the library catalog record for *The direct conversion receiver: Analysis and design of the front-end components* as held by the Stanford University library. I secured this record myself from the library's public catalog. The MARC record

contained within Appendix ESTABROOK03 accurately describes the title, author, publisher, and OCLC number of *The direct conversion receiver: Analysis and design of the front-end components.*

13. The 008 field of Appendix ESTABROOK03 visible on page 1 indicates the catalog record was first created as of March 1, 1990. The 260 field of this record visible on page 1 indicates *The direct conversion receiver: Analysis and design of the front-end components* was first published in 1989. The 'updatedDate' field visible on page 1 of this record indicates the Stanford Library indexed *The direct conversion receiver: Analysis and design of the front-end components* in a new record format as of August 21, 2023, representing *The direct conversion receiver: Analysis and design of the front-end components*' continual inclusion in the Stanford Library's collection since the first date of acquisition. The 'catalogedDate' field visible on page 8 of this record indicates *The direct conversion receiver: Analysis and design of the front-end components* was indexed in a different record format as of August 24, 1991.

14. Appendix ESTABROOK03 indicates *The direct conversion receiver: Analysis and design of the front-end components* was first published in 1989, first cataloged in MARC as of March 1, 1990, cataloged in a new record format as of August 24, 1991 and cataloged again in a new record format as of August 21, 2023. As such, it is my determination that *The direct conversion receiver: Analysis and*

design of the front-end components was likely available to the public from 1991 – 2023 due to the dissertation's inclusion in the Stanford University library.

15. I have reviewed Exhibit 1017, "The Design of a Mobile Radio Receiver using a Direct Conversion Architecture" by Polly Estabrook and Bruce B. Lusignan as published in *Proceedings of the 39th IEEE Vehicular Conference, 1989*.

16. Attached hereto as Appendix ESTABROOK04 is a true and correct copy of the MARC record for *Proceedings of the 39th IEEE Vehicular Conference, 1989* as held by the Linda Hall library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix ESTABROOK04 accurately describes the title, author, publisher, and ISSN number of *Proceedings of the 39th IEEE Vehicular Conference, 1989*. In comparing Exhibit 1017 to Appendix ESTABROOK04, it is my determination that Exhibit 1017 is a true and correct copy of "The Design of a Mobile Radio Receiver using a Direct Conversion Architecture" by Polly Estabrook and Bruce B. Lusignan as published in *Proceedings of the 39th IEEE Vehicular Conference, 1989*.

17. The 008 field of the MARC record in Appendix ESTABROOK04 indicates the date of record creation. The 008 field of Appendix ESTABROOK04 indicates the Linda Hall library first acquired these proceedings as of July 20, 1989. Considering this information, it is my determination that *Proceedings of the 39th*

IEEE Vehicular Conference, 1989 and therefore "The Design of a Mobile Radio Receiver using a Direct Conversion Architecture" was made available to the public shortly after its initial acquisition as of July 20, 1989.

18. I have reviewed Exhibit 1016, "A Mixer Computer-Aided Design Tool Based in the Time Domain" by Polly Estabrook and B. B. Lusignan as published in *IEEE MTT-S International Microwave Symposium, 1988*.

19. Attached hereto as Appendix ESTABROOK05 is a true and correct copy of the MARC record for *IEEE MTT-S International Microwave Symposium, 1988* as held by the University of Cincinnati library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix ESTABROOK05 accurately describes the title, author and publisher of *IEEE MTT-S International Microwave Symposium, 1988*. In comparing Exhibit 1016 to Appendix ESTABROOK05, it is my determination that Exhibit 1016 is a true and correct copy of "A Mixer Computer-Aided Design Tool Based in the Time Domain" by Polly Estabrook and B.B. Lusignan as published in *IEEE MTT-S International Microwave Symposium, 1988*.

20. The 008 field of the MARC record in Appendix ESTABROOK05 indicates the date of record creation. The 008 field of Appendix ESTABROOK05 indicates the University of Cincinnati library first acquired these proceedings as of July 28, 1988. Considering this information, it is my determination that *Proceedings*

of the 39th IEEE Vehicular Conference, 1989 and therefore "A Mixer Computer-Aided Design Tool Based in the Time Domain" was made available to the public shortly after its initial acquisition as of July 28, 1988.

21. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of $200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

22. I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 5/20/2024



June Ann Munford

MARC View

LEADER 02511nas a22004691a 4500				
001 1548210				
003 SIRSI				
005 20151215051926.0				
008 940406c19949999xx bu 0 0eng d				
010			a| sn 94039636	
019			a| MARS	
022			a| 1350-2409	
030			a| ICDSE7	
035			a| LIAS1760745	
035			a| (OCoLC)29965674	
040			d| UtOrBLW	
245	0	0	a| IEE proceedings. p| Circuits, devices and systems.	
246	3	9	a| IEE proceedings. Circuits, devices and systems	
246	3	0	a| Circuits, devices and systems	
264		1	a| London : b| Institution of Electrical Engineers, c| 1994-	
300			a| volumes : b| illustrations ; c| 30 cm	
336			a| text b| txt 2| rdacontent	
337			a| unmediated b| n 2| rdamedia	
338			a| volume b| nc 2| rdacarrier	
362	0		a| Vol. 141, no. 1 (Feb. 1994)-	
500			a| Title from cover.	
650		0	a| Electronic circuits v| Periodicals.	
650		0	a| Electronic systems v| Periodicals.	
780	0	0	t| IEE proceedings. G. Circuits, devices and systems.	
949			a| TK7867.I5401 v.141 1994 w| LCPER c| 1 i| 000051833053 d| 11/7/2000 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 4/13/2001 z| 7754	
949			a| TK7867.I5401 v.142 1995 w| LCPER c| 1 i| 000051833060 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 8/7/2009 z| 7754	
949			a| TK7867.I5401 v.143 1996 w| LCPER c| 1 i| 000051833077 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 8/7/2009 z| 7754	
949			a| TK7867.I5401 v.144 1997 w| LCPER c| 1 i| 000051833084 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 8/7/2009 z| 7754	
949			a| TK7867.I5401 v.145 1998 w| LCPER c| 1 i| 000051833091 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 8/7/2009 z| 7754	
949			a| TK7867.I5401 v.146 1999 w| LCPER c| 1 i| 000051833107 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 8/7/2009 z| 7754	
949			a| TK7867.I5401 v.147 2000 w| LCPER c| 1 i| 000052516191 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 7/10/2003 z| 6339	
949			a| TK7867.I5401 v.148 2001 w| LCPER c| 1 i| 000052516177 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 7/10/2003 z| 6339	
949			a| TK7867.I5401 v.149 2002 w| LCPER c| 1 i| 000052516184 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 7/10/2003 z| 6339	
949			a| TK7867.I5401 v.150 2003 w| LCPER c| 1 i| 000055050067 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 11/9/2005 z| 6339	
949			a| TK7867.I5401 v.151 2004 w| LCPER c| 1 i| 000055050050 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 11/9/2005 z| 6339	
949			a| TK7867.I5401 v.152 2005 w| LCPER c| 1 i| 000055181921 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 1/29/2007 z| 6339	
949			a| TK7867.I5401 v.153 2006 w| LCPER c| 1 i| 000055181914 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 1/29/2007 z| 6339	
852	0	1	a| PSt b| UP-ANNEX c| CATO-2 h| TK7867 i| .I5401	
866		0	8| 0 a| v.141(1994)-v.153(2006)	

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IEE proceedings. Circuits, devices and systems

Additional Titles: IEE proceedings. Circuits, devices and systems and Circuits, devices and systems

Published: London : Institution of Electrical Engineers, 1994-

Physical Description: volumes : illustrations ; 30 cm

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Availability

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Call number	Material	Location
Annexed Material: Holdings Summary v.141(1994)-v.153(2006)		
TK7867.I5401 v.153 2006	Bound Journal	Annexed Material
TK7867.I5401 v.152 2005	Bound Journal	Annexed Material
TK7867.I5401 v.151 2004	Bound Journal	Annexed Material
TK7867.I5401 v.150 2003	Bound Journal	Annexed Material
TK7867.I5401 v.149 2002	Bound Journal	Annexed Material
TK7867.I5401 v.148 2001	Bound Journal	Annexed Material
TK7867.I5401 v.147 2000	Bound Journal	Annexed Material
TK7867.I5401 v.146 1999	Bound Journal	Annexed Material
TK7867.I5401 v.145 1998	Bound Journal	Annexed Material
TK7867.I5401 v.144 1997	Bound Journal	Annexed Material
TK7867.I5401 v.143 1996	Bound Journal	Annexed Material
TK7867.I5401 v.142 1995	Bound Journal	Annexed Material
TK7867.I5401 v.141 1994	Bound Journal	Annexed Material

Continues:
IEE proceedings. G. Circuits, devices and systems.

Dates of Publication and/or Sequential Designation:
Vol. 141, no. 1 (Feb. 1994)-

Subject(s):
Electronic circuits—Periodicals
Electronic systems—Periodicals

ISSN:
1350-2409

Note:
Title from cover.

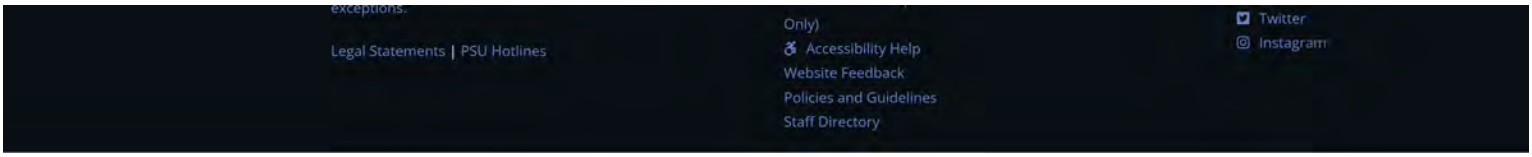
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June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.

- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.

- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in

Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over $400,000 and total assets of approximately $1,300,000.

● Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.

● Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.

● Led the organization and digitization of the library's archival records.

● Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.

● Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013
Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

● Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.

● Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.

● Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013
Library Assistant, Hart Area Public Library
Hart, MI

● Responsible for verifying imported MARC records and original MARC

cataloging for the local-level collection as well as the Michigan Electronic Library.

● Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter
- Treasurer, 2012

Library Of Michigan
- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014
- New Directors Conference Panel Member

Southwest Michigan Library Cooperative
- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008
Petoskey, MI
- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011
Nashville, TN
- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012
Fairbanks, AK
- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Civil Action No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Cases IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Civil Action No. 4:21-cv-149-ALM)

Limited Case and Clientele History

Alston & Bird

- Ericsson

  v. Collision Communications (IPR2022-01233)

- Nokia

  v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

  v. Roku Inc (IPR2022-00818)

Arnold & Porter

- Ivantis

  v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

  v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis

  v. Cathx (Case No. 5:21-cv-00077-RWS)

Erise I.P.

- Apple
  - v. Ericsson Inc. (IPR2022-00715)
  - v. Future Link Systems (IPRs 6317804, 6622108, 6807505, and 7917680)
  - v. INVT (Case No. 20-1881)
  - v. Navblazer LLC (IPR2020-01253)
  - v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
  - v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)
  - v. Telefonaktiebolaget LM Ericsson (IPR2022-00275)
- Fanduel
  - v. CGT (Case No. 19-1393)
- Garmin
  - v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)
- Netscout
  - v. Longhorn HD LLC (Case No. 2:20-cv-00349)
  - v. Implicit, LLC (Civil Action No. 2:18-cv-53-JRG)
- Sony Interactive Entertainment LLC
  - v. Bot M8 LLC (IPR2020-01288)
  - v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)
- Unified Patents

v. GE Video Compression (Civil Action No. 2:19-cv-248)

Fish & Richardson

- Apple
  - v. AliveCor (3:21-cv-03958)
  - v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)
  - v. Koss Corporation (IPR2021-00305)
  - v. Masimo (IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)
  - v. Neonode (Case No. 21-cv-08872-EMC)
  - v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
- Dell
  - v. Neo Wireless (IPR2022-00616)
- Dish Network
  - v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)
  - v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)
  - v. TQ Delta LLC (Case No. 18-1798)
- Evapco Dry Cooling
  - v. SPG Dry Cooling (IPR2021-00688)
- Genetec
  - v. Sensormatic Electronics (Case No. 1:20-CV-00760)
- Huawei

v. Bell Northern Research LLC (IPR2019-01174)

- Kianxis

  v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics

  v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)

- Metaswitch

  v. Sonus Networks (IPR2018-01719)

- Microsoft

  v. Throughputer Inc (IPR2022-00757)

- Mom Enterprises

  v. Ddrops Company (Case No. 1:22-cv-00332)

- MLC Intellectual Property

  v. MicronTech (Case No. 3:14-cv-03657-SI)

- Nearmap Inc

  v. EagleView Technologies (IPR2022-01009)

- Neuroderm Ltd.

  v. Abbvie, Inc (Case No. PGR2022-00040)

- Realtek Semiconductor

v. Future Link (IPR2021-01182)

- Quectel
  - v. Koninklijke Philips (Case No. 1:20-cv-01710)

- Samsung
  - v. Aire Technology (IPR2022-00877)
  - v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)
  - v. Communication Technologies Inc (IPR2022-01221)
  - v. Jawbone Innovations (IPR2022-00865)
  - v. MemoryWeb LLC (IPR2022-00885)
  - v. Dodots Licensing Solutions (IPR2023-00701)
  - v. Telefonaktiebolaget LM Ericsson (IPR2021-00615)

- Texas Instruments
  - v. Vantage Micro LLC (IPR2020-01261)

- Xilinx
  - v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Irell & Manella

- Curium

O'Melveny & Myers

- Apple
  - v. Maxell (Case No. 5:19-cv-00036-RWS)

- Micron Technology Inc.

  v. Besang Inc (IPR2023-00900)

- Samsung

  v. Daedalus Prime LLC (1335 Investigation)

Perkins-Coie

- Heru Industries

  v. The UAB Research Foundation (IPR2022-01148)

- Intel Corporation

  v. BitMICRO (Case No. 5:23-cv-00625)

- Realtek Semiconductor

  v. Future Link (IPR2021-01182)

- Twitter Inc

  v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)

- TCL Industries

  v. Koninklijke Philips NV (IPR2021-00495, IPR2021-00496 and IPR2021-00497)

Pillsbury Winthrop Shaw Pittman

- Intel

  v. FG SRC LLC (Case No. 6:20-cv-00315)

- Gravel Rating Systems

v. Costco (Case No. 4:21-cv-149)
v. Lowe's Home Centers (Case No. 4:21-cv-150)
v. T-Mobile USA (Case No. 4:21-cv-152)
v. Kohl's Inc. (Case No. 4:21-cv-258)
v. Under Armor (Case No. 4:21-cv-356)

Quinn Emanuel

- Wolfspeed

v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

Sheppard, Mullin, Richter & Hampton LLP

- Cadence Design Systems Inc.

v. Semiconductor Design Technologies (Case No. 3:23-cv-01001)

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The direct conversion receiver: Analysis and design of the front-end components

Estabrook, Polly, Ph.D.

Stanford University, 1989

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THE DIRECT CONVERSION RECEIVER: ANALYSIS AND DESIGN OF THE FRONT-END COMPONENTS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

By
Polly Estabrook
August 1989

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Abstract

This thesis discusses the design of a direct conversion receiver. This receiver architecture is intended for applications where single channel reception with low cost compact transceivers is desired. The issues of achievable gain and phase match between the receiver's 'I' and 'Q' channel and the design of receiver front-end components are specifically addressed. Designs for a low conversion loss RF mixer whose input frequency is 1GHz or lower, a low frequency (DC to 100's KHz) low noise amplifier, and a low frequency low noise active filter stage are developed and analyzed.

A mixer analysis and design tool has been developed to study the design of low conversion loss mixers with practical diodes, ie. ones having series resistance, barrier resistance, and barrier capacitance. Low levels of barrier capacitance are shown to improve mixer conversion loss over that of a purely resistive diode mixer. Simulation results predict the conversion loss of the direct conversion single-ended mixer to be 3.1dB and that of the balanced mixer to be 2.1dB; both mixers utilize diodes having a barrier capacitance of 0.25pF.

Low frequency amplifier design is performed by analyzing the noise performance of a typical bipolar op-amp input stage. Dominant noise sources are identified; noise temperature is optimized for operation at low frequencies and for low source resistances by selection of the input device and by bias adjustment. Noise figure is estimated to be 3.4dB at 10 Hz and 2.5dB at 1KHz when the amplifier is driven by a source impedance of 2KΩ.

An active filter stage consisting of a cascade of three identical multiple loop feedback filter stages is analyzed by considering the noise contributions of the op-amp and the resistive feedback elements in each stage. Feedback components are chosen

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to ensure good noise performance when cascaded by the direct conversion amplifier and to provide acceptable in-band gain and adjacent channel rejection. A filter gain of 30dB is realized with an adjacent channel rejection of 34dB and a subsequent channel rejection of 81 dB; filter noise figure ranges from 34dB at 25Hz to 22dB at 1KHz.

The expected performance of the direct conversion receiver can be computed from the performance of each of the front-end components. This receiver is found to perform as well as or better than a conventional super-heterodyne receiver with a mixer front-end. It is expected to have smaller volume, lower weight and power consumption, and, to be more versatile than receivers with heterodyne architectures.

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Chapter 1

Introduction

1.1 The Direct Conversion Receiver

This thesis discusses the design of a direct conversion receiver. This receiver is felt to be superior to a conventional super-heterodyne receiver for applications where single channel reception with low cost compact transceivers is required. The breadth of the thesis concerns the overall design criteria for the receiver and its application. The depth lies in the development of techniques for the design and analysis of low conversion loss UHF mixers.

The direct conversion receiver considered here is depicted in Figure 1. To illustrate its performance, consider the input signal, f_{RF}, to have a center frequency f_c and a bandwidth BW_{RF}. The input signal, after optional amplification, is power-split and sent to the inputs of two broadband mixers. The local oscillator frequency, f_{LO}, of both the in-phase and quadrature-phase (I/Q) mixers is locked to f_c. Consequently, the signal at the output of each mixer, f_o spans from DC to $BW_{RF}/2$. These signals are amplified, filtered, and finally processed together to reconstruct the transmitted signal.

The receiver lends itself to work with many signal frequencies and formats. The low level signal processing, comprising the RF mixers and the first stage of amplification and filtering, is accomplished by low noise, high dynamic range, circuits. Although the input mixer will need to be designed for operation with a specific f_c

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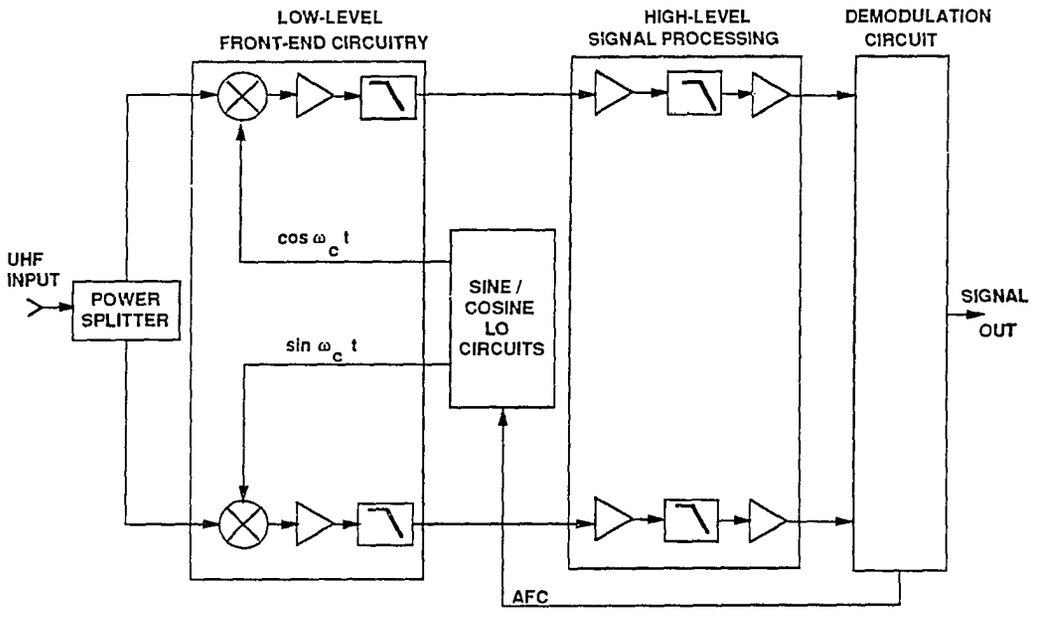


Figure 1: Block diagram of the direct conversion receiver.

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and BW_{RF} for best performance, the subsequent low level amplifier-filter stage may be designed in several different bandwidths ($BW_{filter} \approx BW_{RF}/2$) to serve a wide number of applications. Thus by choosing the correct mixer and amplifier-filter stage for a specific application, a large range of signals with center frequency's between 50 and 900 MHz, thus covering all mobile radio bands, and signal bandwidth's from a few KHz, for SSB voice applications, to a few hundred KHz, for digital applications can be accomodated. The second stage of amplification and filtering is more application-specific; however, standard CMOS opamps and switched capacitor filters with variable cutoff frequencies can be used as the signal power has now been boosted above the noise floor. Finally, signal reconstruction – unfolding and correct frequency placing of the baseband signal – and demodulation must take place; these circuits are also application dependent. These functions can be implemented by one circuit and realized using standard processing techniques. If the signal is in a digital format, the high level signal processing circuits described above can be replaced by analog to digital converters (A/D) and digital signal processing circuits that will demodulate and decode the signal. The low-level front-end circuits then act to downconvert the signal to DC where A/D conversion can be reliably and cheaply performed and to set the receiver's signal-to-noise ratio.

This thesis describes the application of direct conversion to the design of a mobile cellular radio at 900 MHz. This work has been inspired by Weaver's design of a SSB direct conversion receiver in 1956 [75] and by the more recent use of direct conversion receivers for VHF radio paging applications using BFSK modulation [71, 70]. Translation of this work to higher signal frequencies and to more complex signal sets has been slowed pending clarification of certain issues. These problems can be divided into two categories: those that are common to all applications and those that are application specific. In the first category the most important are the determination of achievable gain and phase balance between the 'I' and 'Q' channel and the impact of this imbalance on signal reception for several modulation types, and, the development of a receiver front-end that can provide the sensitivity and dynamic range required. Other receiver design topics in this area are the design of the frequency synthesizer and microwave local oscillator circuits, the automatic frequency control (AFC) circuits

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and the design of the CMOS active filter. In the second category lies the design of the modulation specific demodulation circuits.

This thesis concerns itself with the receiver design issues that are common to all signal formats and hence all applications. Among those topics mentioned above, the problems of achievable gain and phase match, and front-end receiver design have been selected as the focus of this work. The design of the CMOS active filter, of the modulation specific circuits, of the automatic frequency control (AFC) circuits and the LO generation circuits are outside the scope of this work. First, the advantages of building a mobile radio receiver using a direct downconversion architecture rather than the conventional heterodyne approach will be outlined. The design problems specific to mobile radio direct conversion receivers, such as achieving good sensitivity and dynamic range, will be discussed and solutions will be proposed. Second issues concerning phase and gain balance between channels are examined. Third, the integrated approach taken for the design of the signal processing circuits when the received signal is still at a low level is detailed. These circuits comprise the RF mixers, the subsequent low frequency amplifiers, and the active filters. This allows low conversion loss and high output impedance mixers to be designed, amplifiers with low noise performance over the DC to $\frac{BW_{RF}}{2}$ bandwidth to be constructed, and, filters that set selectivity without impacting the signal-to-noise ratio at their output to be specified. Design advantages that are a direct consequence of this choice of receiver architecture, such as high selectivity, small size, and low power consumption, are detailed. Finally the overall receiver specifications are calculated and compared with those of a typical heterodyne receiver. For the purpose of this design, signals are taken to be voice signals modulated with amplitude companded single sideband (ACSB). The spectrum is assumed to have been divided up in 3.1 KHz channels, with 900 Hz guard bands between them.

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1.2 Direct Conversion Receivers Compared with Heterodyne Receivers

Differences in the performance of the direct conversion receiver and the heterodyne receiver can be seen by comparing their reception of a SSB signal. In this way the role of each component in achieving receiver specifications such as selectivity, image rejection, spurious rejection and dynamic range can be seen.

The heterodyne receiver is shown in Fig. 2. The spectra is shown at various points along the receiver assuming coherent demodulation of a SSB signal in Fig 3. The spectra at the output of the first mixer shows that the power at the image frequency has been folded over on the signal band. The ratio of signal power to image power at the output of this mixer is set by the attenuation of the image frequency by the input RF filter. Hence this component, in general, determines the level of image rejection in the receiver. (Unless the input mixer is an image-reject mixer in which case about 20 dB of image rejection can be obtained due to the mixer alone.) Spurious rejection denotes the level to which all signals are attenuated prior to being downconverted into the signal band by any of the receiver's mixers. This is illustrated by the action of the second mixer. Here the mixer's harmonics are shown to downconvert input signals other than the wanted signal into the wanted signal band. Once these signals have been downconverted into the signal band they cannot be removed. Hence this will increase the signal-to-noise inband. Mixer selectivity is determined by the rejection of unwanted signals from the final demodulated signal band. This is accomplished by filters located along the receiver chain. Dynamic range, not shown in Fig. 3, refers to the difference in signal strengths between reception of the minimum signal level and the maximum signal level. This receiver parameter is set by the noise temperature of the receiver and by the intermodulation performance of the input components.

For comparison, the reception of a SSB signal by the direct conversion receiver is shown in Fig. 4. Only the spectra of the 'I' channel is shown. The receiver's local oscillators are assumed to be locked to the output signal with the result that ω_{LO_1} is set to the center frequency of the SSB signal. The SSB signal has a bandwidth BW_{RF}. The signal at the image frequency is not downconverted to the wanted signal band at

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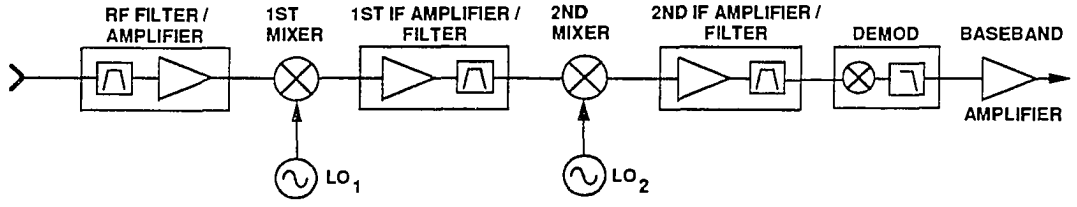


Figure 2: Block diagram of a typical heterodyne receiver.

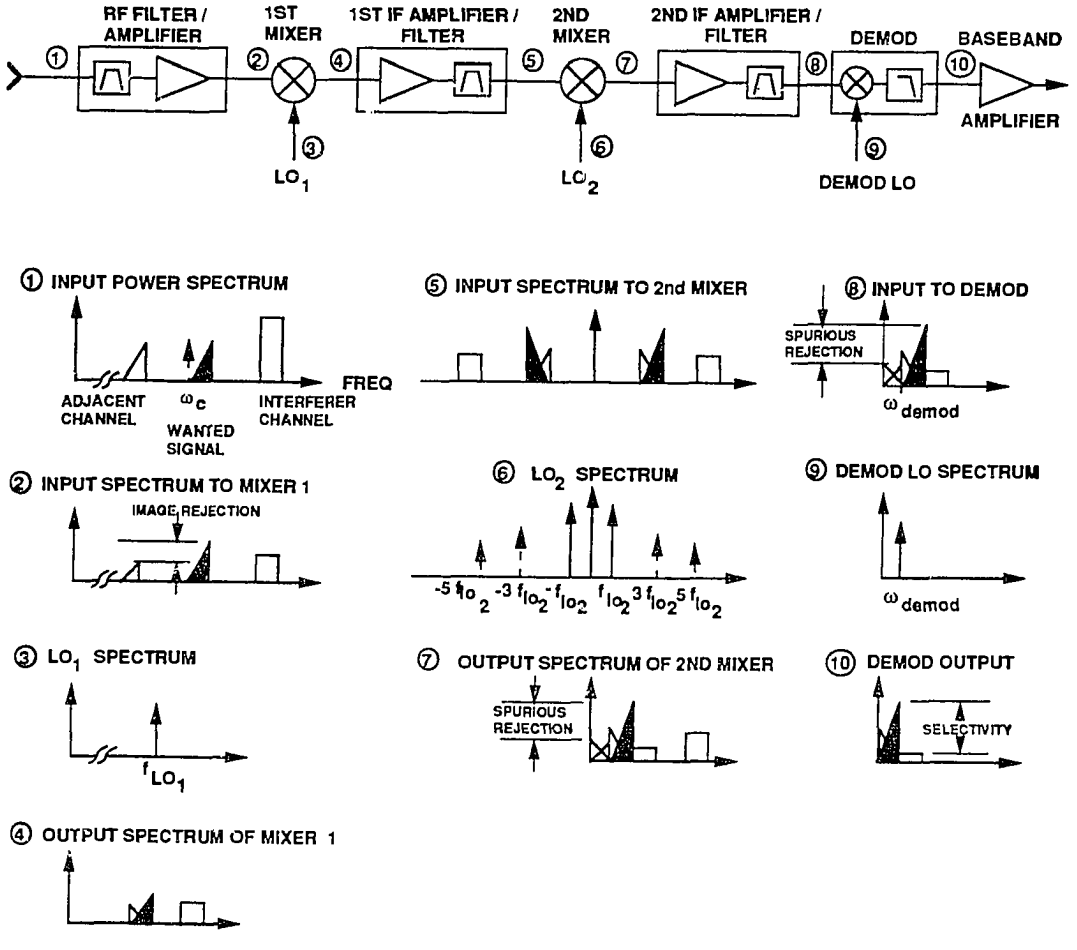


Figure 3: Reception of a SSB signal with a heterodyne receiver.

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the output of the first mixer. Image rejection is therefore infinite. The wanted signal, now downconverted to DC, spans from $-BW_{RF}/2$ to $BW_{RF}/2$. The selectivity of the receiver is set by the roll-off of the low signal level low pass filter (LPF) and the subsequent LPF in the high signal level processing circuits. Low pass filters can achieve higher selectivity than band pass filters centered at an IF frequency because LPFs can be realized with high performance active filters whereas BPFs are typically realized with passive elements which cannot provide as steep a filter characteristic. In addition filters composed of passive elements are heavier and bulkier.[1]

Further mixing is necessary to demodulate the SSB signal. The 'I' and 'Q' channels do not contain the wanted signal in its original format; instead they contain quadrature versions of the wanted signal folded over itself at DC. Final mixing with an LO of $BW_{RF}/2$ is performed to unfold the signal spectrum. The output of the demodulation mixer in the 'I' channel shows the wanted signal spanning from $-BW_{RF}$ to BW_{RF}. However a frequency inverted replica of the wanted signal also covers the same band. To eliminate this in-band distortion, the output of the 'I' channel must be summed with the 'Q' channel as shown in Fig. 4. If the gain and phase performance of both channels is identical, the in-band distortion caused by the existence of the frequency inverted signal will be successfully removed. If not, in-band distortion will exist. The level to which the unwanted spectrum can be suppressed in practical receiver circuits is discussed in Chapter 2.

The direct conversion architecture has several advantages over a standard heterodyne receiver: (1) the image frequency ($f_{image} = f_{LO} \mp f_o$ where $f_{RF} = f_{LO} \pm f_o$), potentially a source of interference in heterodyne systems, is here a frequency within the RF bandwidth – thus rejection of unwanted signals at f_{image} is infinite; (2) it possesses good selectivity because of the use of low pass filters (LPF) rather than band pass filters (BPF) as used in a heterodyne receiver, these can be designed with active op-amps and Complementary Metal Oxide Semiconductors (CMOS) filters[2];

[1] If the IF frequency is high enough (> 500 MHz) the BPF can be realized with distributed circuit elements etched on a dielectric substrate. However as the wavelength of these frequencies is still very long, the components will require a large surface area to realize. Consequently the number of filter elements and the yield per die will be small.

[2] The maximum bandwidth achievable with CMOS filter is typically less than 10 MHz.

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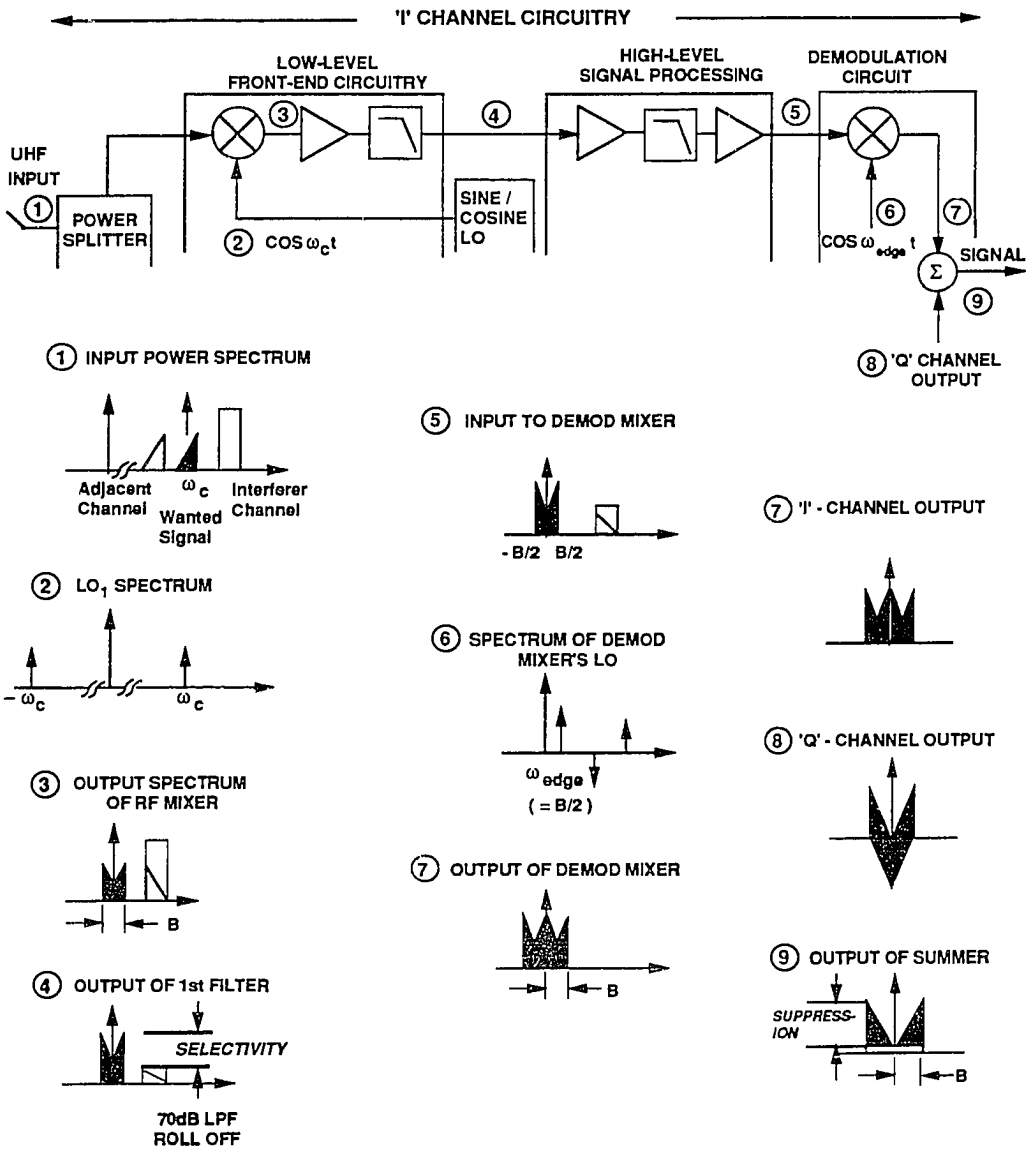


Figure 4: Reception of a SSB signal with a direct conversion receiver.

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(3) it has size and power consumption advantages due to the lack of IF filters; (4) the majority of the signal processing is done at very low frequencies where many high performance, special purpose, circuits already exist – thus signal processing is simple, low cost and of high performance; (5) lastly the receiver's performance is as good as or better than a comparable heterodyne receiver. From a technology development point-of-view, this receiver is ideal because it merges analog and digital signal processing, because it lends itself to monolithic realization – thereby permitting the construction of generic receiver building blocks –, and, because its architecture, effectively an I/Q demodulator at RF, can work with many modulation schemes. The multipurpose nature of the direct conversion receiver's components can be used to justify the development of costly receiver LSI and VLSI building blocks.

The ability of this receiver to work with many modulation schemes merits further discussion. Historically the direct conversion receiver was proposed by Weaver in 1956 as a method to generate and receive SSB signals [75]. To demodulate SSB two baseband mixers and a summer are necessary. Accurate reconstruction of the baseband signal, or suppression of the unwanted sideband within the wanted signal band, is determined by the gain and phase balance that can be achieved between the 'I' and 'Q' channels. Weaver was able, with varying levels of difficulty, to keep the unwanted signal 20 dB to 40 dB below the wanted signal which was sufficient to achieve the desired audio quality. The direct conversion receiver's lack of widespread acceptance at that time can probably be attributed to the unfamiliarity of its design, the need for higher received signal-to-noise (S/N) levels and the shift from SSB to FM as a preferred modulation.

FM signals can be received with the direct conversion receiver using the "sin-cosine" demodulation technique which consists of differentiator and mixer circuits. Here both gain and phase match between the channels is needed for correct demodulation. An FM receiver built with "sin-cosine" demodulation circuits was developed in 1979 by Vance et al. for radio reception at VHF; the demodulator performance is detailed in [23]. To receive AM modulation the output of the 'I' channel can be tapped, the 'Q' channel output is used to generate the control voltage for the LO. For this application phase match between 'I' and 'Q' channels is necessary to lock f_{LO_1}

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to f_c. Finally the receiver works well with all types of digital modulation, such as QPSK and QAM, as it is effectively an I/Q demodulator placed at the RF frequency rather than at some intermediate frequency (IF) as is typical in heterodyne receivers. The direct conversion receiver then performs the dual function of conversion and demodulation as one process as opposed to heterodyne receivers which convert the RF to IF and then demodulate the digital signal with an I/Q demodulator. For these applications, phase match between channels is of primary importance to attain good QPSK reception as is amplitude match for QAM.

The direct conversion receiver has the promise of resulting in a smaller size and lower cost receiver than the standard super-heterodyne receiver for applications where single channel reception (signalling and data) is necessary, such as mobile radio via terrestrial or satellite links. Although primarily digital receiver architectures may become prevalent in the future[3], the direct conversion receiver has an important role to play in current receiver design: not only can it offer good performance by taking advantage of the developments in high frequency analog signal processing techniques [63] and make use of existing high performance analog ICs but it can be realized at low cost. In contrast, receivers based primarily on digital signal processing techniques will remain too expensive in the short-term for most commercial applications.

1.3 Thesis Organization

Chapter 2 evaluates phase and gain match achieved with a direct conversion receiver designed with standard components. The design challenges of the direct conversion receiver are listed and the integrated approach taken for the design of the signal

[3]Here digital receivers refer to receivers that utilize several stages of downconversion to bring the signal center frequency into the range of an A/D converter. The input frequency and/or signal bandwidth must be less than 50 MHz if a low power, ie. CMOS, A/D is used and less than 500 MHz if a higher power, eg. ECL, A/D is used. The signal is bandpass sampled by the A/D and the resultant spectrum which spans DC to infinity is digitally filtered to obtain the baseband signal spectrum only. Digital signal processing techniques are used to demodulate and decode the signal. They can be used to lock the local oscillators in the receiver. This is in contrast to the direct conversion receiver which can employ A/D converters and digital signal processing techniques instead of the high level signal processing circuits if digital signal demodulation and decoding is desired. In other words, the direct conversion receiver allows A/D conversion at DC where future digital receivers will utilize A/D conversion at as high an RF as possible.

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processing circuits when the received signal is still at a low level is detailed. These circuits comprise the RF mixers, the low frequency amplifiers, and the active filters. The specific design goals of each component is detailed.

Chapter 3 reviews previous mixer analysis work and discusses the computer-aided mixer analysis and design tool developed for this work.

Chapter 4 examines the behavior of simple single-ended mixers and single-balanced mixers. First their performance with purely resistive diodes is studied. Then the degradation in performance is measured as barrier capacitance is added to the diode model and this behavior is explained. The performance of these mixers is compared with that predicted by conventional frequency domain analysis techniques.

Chapter 5 details the use of the tool for the design of direct downconversion mixers. Specifically the design of broadband mixers with diodes possessing barrier capacitance and series resistance in addition to barrier resistance is discussed. The performance criteria for these mixers is based upon their achieving low conversion loss when driven from low source resistances into high output impedances.

Chapter 6 discusses the design of the low noise amplifier chain that follows the direct downconversion mixer. Here low noise performance at low frequencies is desired when the amplifier is driven from a low impedance source.

Chapter 7 gives the design of the active filter stage which follows the low noise amplifier. This is the last of the low signal level processing circuits. Both gain and noise performance is of interest in its design.

Chapter 8 concludes this work. The expected performance of the direct conversion receiver is calculated based on the component design detailed in the previous chapters. Its performance is compared against that of a typical heterodyne receiver designed for mobile radio applications. Topics for future research in the development and use of direct conversion receivers are suggested. We conclude with a discussion of various trends in receiver development and an assessment of the role of direct conversion receiver in future systems.

There are several appendices to this thesis. In the mixer appendix, Appendix A, the output of several simulation runs of the mixer program is given, the output spectrum of two mixer runs with different sample sizes is contrasted, diode models

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used in the simulation are discussed, and lastly program listings for the design tool are given. The amplifier appendix, Appendix B, details the circuit models, gain and noise figure performance for three amplifier building blocks considered for the low noise amplifier work. Amplifier noise temperature performance is broken down into its constituent components created by various device and circuit noise sources. Appendix C contains the program listing for the active filter analysis program. Terms frequently used in the dissertation are defined in the Glossary.

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Chapter 2

Design Challenges

2.1 Introduction

In this chapter the application independent problems of the direct conversion receiver discussed in Chapter 1 are detailed. Two general problems fall in this category, the gain and phase match between the 'I' and 'Q' channels and the design of the front-end of the receiver. The first issue is addressed by measuring the performance of a direct conversion receiver built with discrete components. The results obtained give a worst-case value for gain and phase match as better results would inevitably occur if each the 'I' and 'Q' component were built on the same chip, or, if the low level signal processing circuits could be implemented on an LSI chip. The subsequent chapters deal with the second problem. In this chapter we outline the approach taken in the design of the direct conversion receiver front-end and specify the design challenges for each of the low level signal processing circuits.

2.2 Evaluation of Magnitude of Phase and Gain Imbalance Problem

Gain and phase match between the 'I' and 'Q' channels affects the quality of signal reception for most modulation formats. One way to gauge the gain and phase

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match is to measure the suppression of the unwanted sideband in a SSB receiver. A schematic of a SSB direct conversion receiver is shown in Figure 5. Its operation can be detailed as follows. The RF signal, of center frequency f_c and bandwidth BW_{RF}, is downconverted to DC by the input mixers of both channels. The signal at the output of these mixers now spans from DC to $BW_{RF}/2$. The downconverted signal spectrum is folded over itself and no longer possesses the original RF spectral shape. The low frequency signals are then filtered, to remove any adjacent channel signals, and amplified to set the noise floor. To reconstruct the original spectrum both 'I' and 'Q' channel signals are mixed again with quadrature LO's at a frequency, f_{LO_2}, equal to $BW_{RF}/2$. At the output of each of the baseband mixers the sum and difference signals created by beating the input spectrum, spanning DC to $BW_{RF}/2$, by $BW_{RF}/2$. At the mixer output the sum signal from $BW_{RF}/2$ to BW_{RF} and the difference signal from $BW_{RF}/2$ to DC therefore are present. For $f_{RF} > f_{LO}$ the sum signal at the output of the 'I' channel will be in phase with the sum signal at the output of the 'Q' channel and the difference signals will be 180° out-of-phase. For $f_{RF} < f_{LO}$ the reverse will occur. Thus, for $f_{RF} > f_{LO}$, when the outputs of the two baseband mixers are summed together only the sum signals will added and the difference signals subtract. The extent to which the unwanted sideband is suppressed is an indication of the level of gain and phase matching. For analog voice signals, the level of the unwanted sideband relative to the desired sideband sets the signal-to-distortion (S/D) ratio at the output of the receiver. The extent of gain and phase match required to produce a given level of suppression can easily be calculated. For example 20 dB of suppression can be achieved by a gain match of 1.5 dB and a phase match of 5° or with a gain match of 0.5 dB and a phase match of 11°.

When the receiver is built with discrete parts, suppression levels similar to those achieved by Weaver are expected. However when the direct conversion receiver is implemented with integrated circuits, so that circuits required by both channels can be built on one integrated circuit, then improved gain and phase matching between channels can be realized. Regardless of this potential improvement, it is important to remember that the S/D or S/N achievable at the output of the direct conversion receiver is not necessarily the S/N of the received signal. Higher S/N's are obtainable

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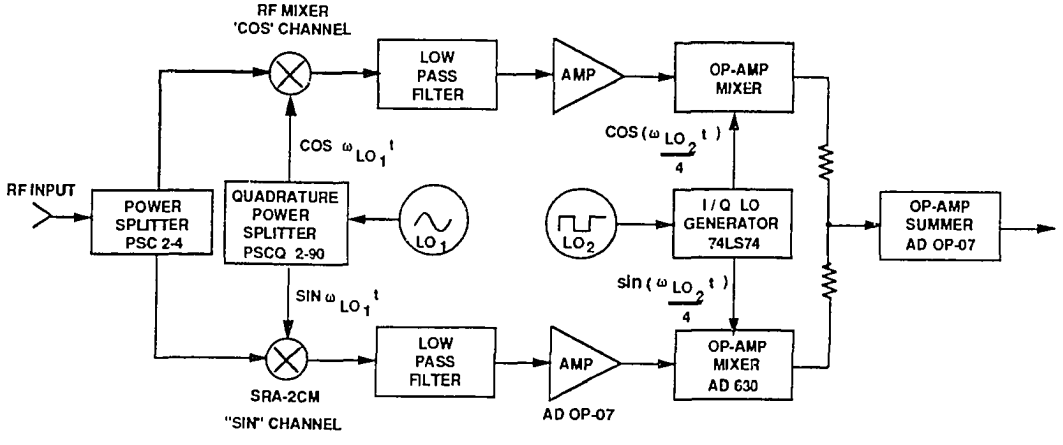


Figure 5: Schematic of the SSB receiver.

through the use of companding for SSB signals (ACSB) [76] and through the use of codes for digital signals.

To determine the level of gain and phase match possible for a direct conversion receiver, the SSB receiver shown in Figures 6 and 7 was built with discrete components. Figure 6 shows the RF portion of the receiver. In it the RF power splitter, 'I' and 'Q' mixers, and LO circuitry such as prescaler, voltage controlled oscillator (VCO), buffer and output amplifier are shown. The RF mixers are Mini-Circuits SRA-2CM; they are designed to operate with input signals from 5 MHz to 1 GHz. The power splitter, a Mini-Circuits PSC2-4, is also a broadband device; it operates with input signals from 10 MHz to 1 GHz. The quadrature power splitter, a Mini-Circuits PSCQ2-90, has a frequency range of 55 MHz to 90 MHz. The synthesizer, prescaler, and VCO are Motorola parts, namely MC145145, MC12016P, and MC1648, respectively. The buffer amplifier and amplifier are Avantek AT-17 and GPD-130 circuits, respectively.

Figure 7 depicts the low-level processing circuits and the SSB demodulation circuits. The low frequency amplifier, op-amp mixer, and op-amp summer are Analog Device parts. The OP-07 is used as the amplifier and summer and the AD630 is used for the mixer. The low frequency local oscillator is based on a 74LS74 chip. It converts a TTL pulse at ω to two quadrature pulses at $\omega/4$.

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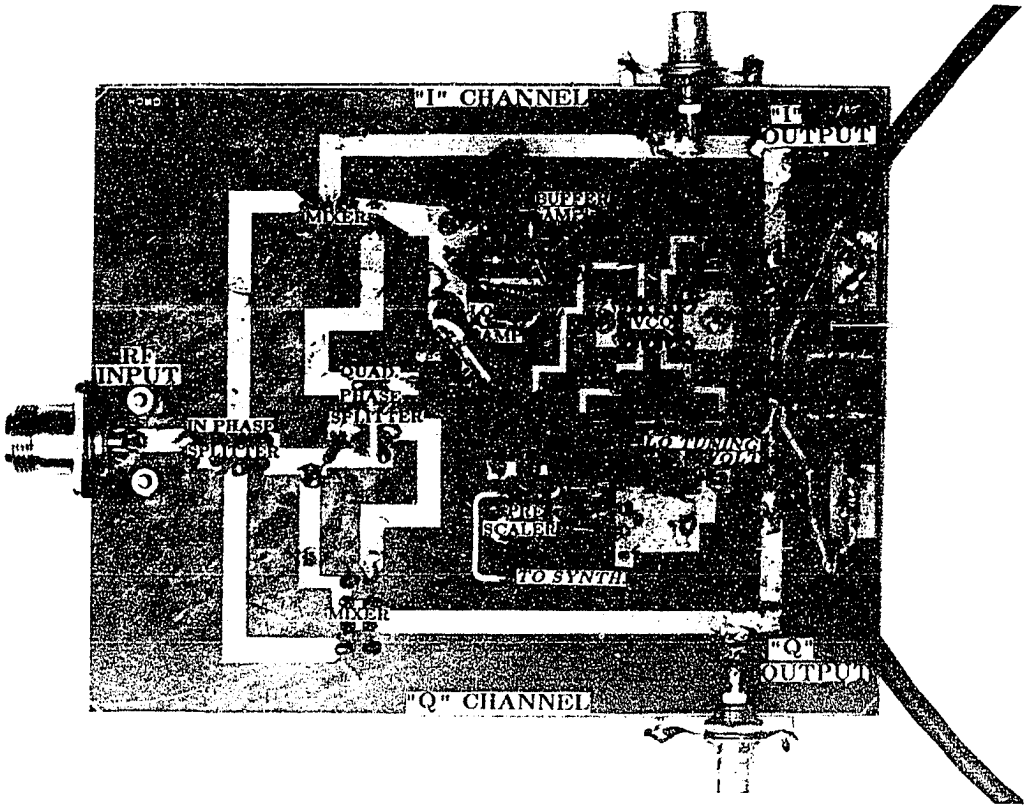


Figure 6: UHF portion of the direct conversion receiver.

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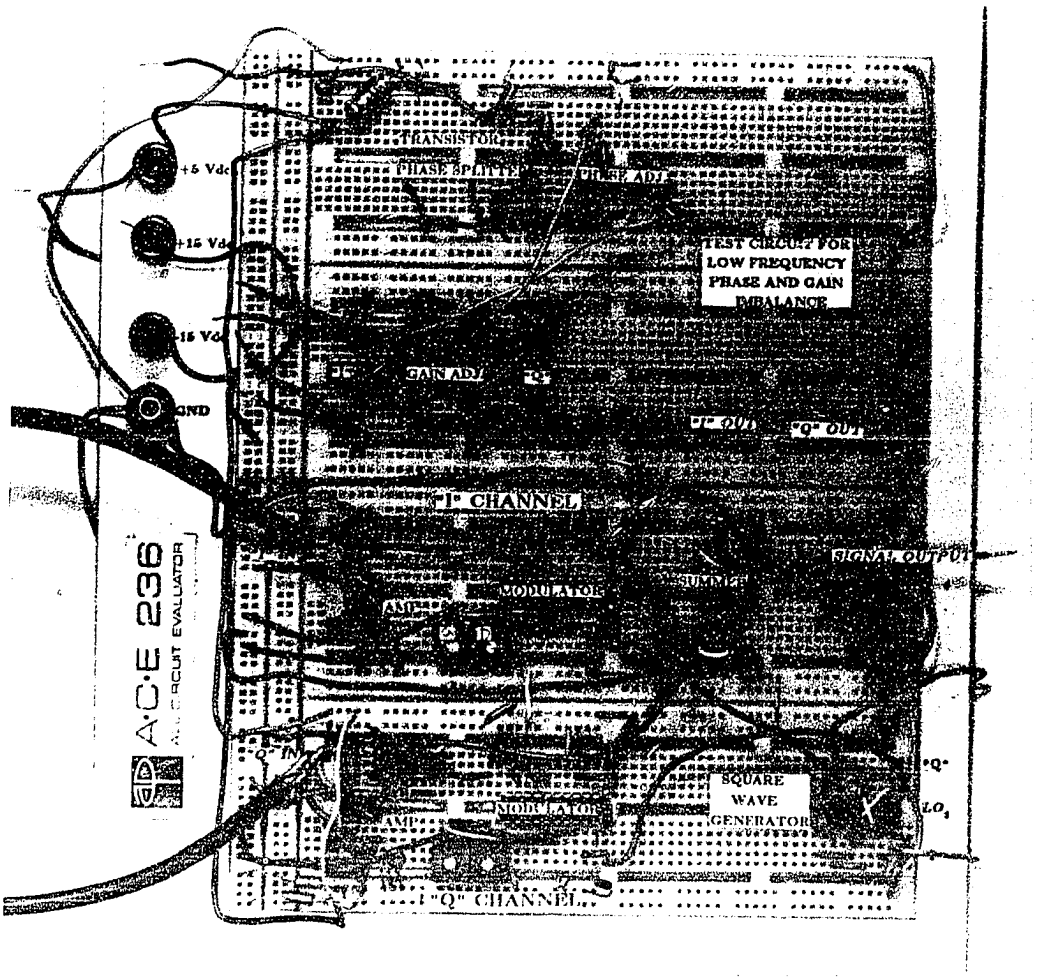


Figure 7: Low frequency portion of the direct conversion receiver implemented for SSB reception.

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For the purposes of this experiment the SSB signal was assumed to have a 6 KHz bandwidth, its suppressed carrier was taken to be at 70 MHz. The RF signal could then be characterized by:

$$\begin{aligned} f_c &= 70.003\text{MHz} \\ BW_{RF} &= 6\text{KHz} \end{aligned}$$

To illustrate the generation of unwanted sidebands and to measure suppression in the direct conversion receiver, the reception of a SSB tone at

$$f_{RF,\,tone} = 70.005\text{MHz}$$

is examined. The outputs of the two UHF mixers, f_{oI} and f_{oQ} for the 'I' and 'Q' channels, respectively, will then be:

$$\begin{aligned} f_{oI} &= 2\text{KHz} \angle 0° \\ f_{oQ} &= 2\text{KHz} \angle 90°. \end{aligned}$$

The baseband mixers operate with

$$\begin{aligned} f_{LO_2} &= \frac{BW_{RF}}{2} \\ &= 3\text{KHz} \end{aligned}$$

so that the sum and difference signals produced are at 5 KHz and 1 KHz. The 5 KHz signals are in-phase with each other and the 1 KHz signals are $\approx 180°$ out-of-phase with each other. When the spectrum at the output of the summer was measured, the 1 KHz signal was typically found to be 24 dB below the 5 KHz signal as can be seen in Fig. 8. This can be calculated to translate to a gain balance of less than 1 dB and a phase balance of better than 2.5°. With the low frequency amplifier and summer aligned for best channel match, a suppression of 40 dB was possible. The degradation in SSB reception causes by these imbalances can be easily calculated by using, for example, Song's formulas [66].

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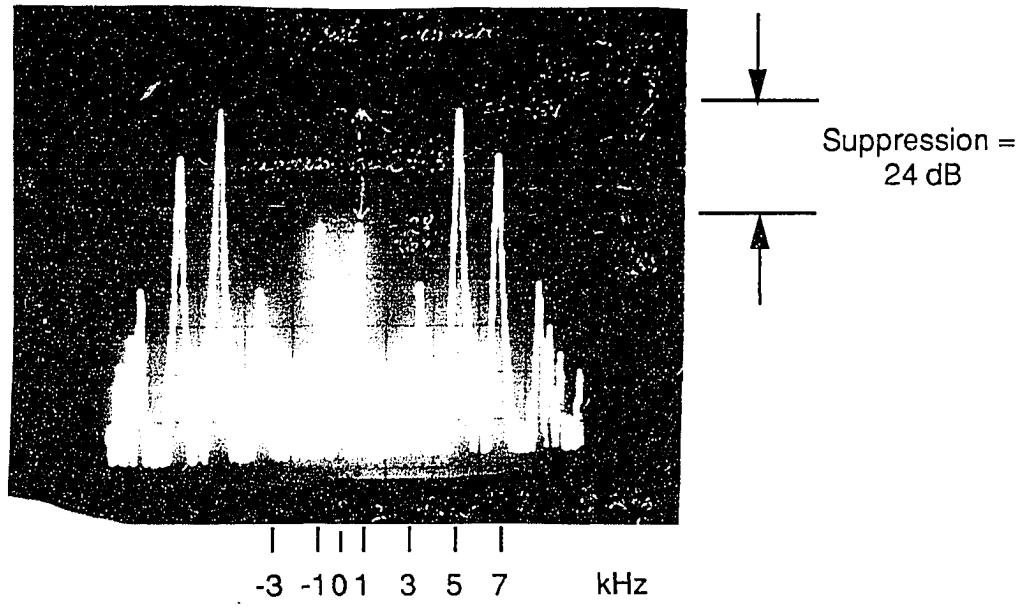


Figure 8: Photograph of output spectrum of the direct conversion receiver for SSB input.

2.3 Low-Level Signal Processing Circuits

The low level signal processing circuits shown in Figure 1 are depicted in greater detail in Figure 9. Only one channel is shown. The RF mixer, the low frequency amplifier, and, filter comprise these low level circuits and form the front-end of the receiver. A typical RF spectrum is shown at the input to the mixer, it consists of the wanted signal, W_s, and two interferers, I_1 and I_2, adjacent to W_s and having higher power than W_s. The noise floor is illustrated by the darkened line. The spectrum at the output of each component is shown to elucidate their function and their design constraints.

The front-end components are processing the input signal while it is still at a low power level. These circuits contribute in setting the noise floor and dynamic range of the receiver contrary to the subsequent stages whose additional noise only contributes inconsequentially to the overall noise. To guarantee the greatest dynamic range possible, the low frequency amplifier possesses the minimum gain necessary to

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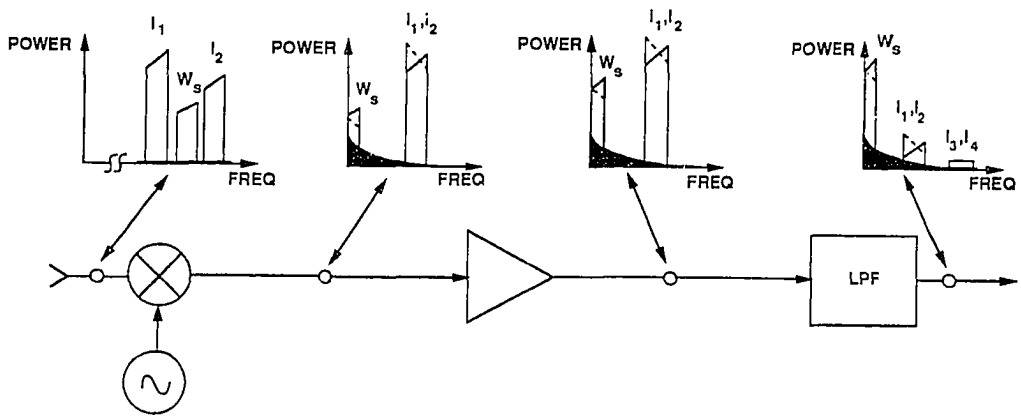


Figure 9: Front-end of one channel of the direct conversion receiver with typical spectrum plots.

reduce filter noise components to an acceptable level.

Receiver noise temperature is given at the receiver input as a function of frequency as:

$$T_{rec}(f) = T_{mixer}(f) + C_L \cdot T_{amp}(f) + C_L \cdot \frac{T_{filter}(f)}{G_{tot,amp}} \quad (1)$$

where T_{mixer}, T_{amp}, and, T_{filter} are the noise temperature of the mixer, amplifier, and, filter respectively, $G_{tot,amp}$ is the low frequency amplifier gain (this amplifier may be made of several stages of gain G_{amp}), and C_L is the mixer's conversion loss. All noise sources are a function of frequency due to the dominance excess noise term. Noise figure is determined from noise temperature according to:

$$NF = 10 \cdot log\left(1 + \frac{T}{290}\right). \quad (2)$$

When conjugate matching is used between components the gain of the front-end circuits can be written in terms of their individual gains as:

$$G_{rec} = \frac{G_{tot,amp} \cdot G_{filter}}{C_L}. \quad (3)$$

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2.3.1 Low Conversion Loss Mixers

Three design goals must be kept in mind while designing the direct conversion mixer: (1) efficient translation from the RF to f_o; (2) low excess noise or 1/f noise at the mixer output; (3) impedance transformation from a low $R_{S_{RF}}$ to a high R_L. The first objective listed is common to all mixer designers especially for receivers with mixer front-ends. Translation of the input signal from the RF frequency at the mixer input port to some output frequency is specified by the mixer's conversion loss. Conversion loss is defined as:

$$C_L = \frac{\text{Power Available from the Source}}{\text{Power Delivered to the Load}}.$$

Minimization of mixer noise figure is the second criterion for a direct conversion mixer as the mixer generated noise, along with that generated by the amplifier and filter cascade, sets the noise floor of the receiver. The noise at the mixer output is due to shot noise, thermal noise and excess noise. Excess noise, or 1/f noise, is of particular importance in the direct conversion receiver: it is the dominant noise source at the low frequencies at which much of the receiver's signal processing is carried out. Excess noise is generated by all devices, active and passive alike, such as diodes, transistors, resistors etc. This noise source can be modelled as a noise current of mean squared value:

$$\overline{i_{ex}^2} = \frac{K \cdot I_d^a \cdot \Delta f}{f^b}$$

where K, a, and, b are device dependent parameters, $a \approx 0.5$ - 2.0 and $b \approx 1.0$. The noise spectrum of a typical device with shot and excess noise is shown in Figure 10. The 1/f frequency knee, or frequency where the excess noise contribution is equal to that caused by shot and thermal noise, is marked on the graph. Because this noise occurs in the band to which the RF signal has been translated, minimization of its magnitude is particularly important for the direct conversion receiver. The signal and noise spectrum at the mixer output is depicted in Figure 9.

Lastly direct conversion mixers have the unusual requirement that they must operate well when driven from the low input impedance of the antenna or RF preamplifier (optional), ie. 50 Ω or 75 Ω, and loaded by a high impedance at f_{IF}. Because

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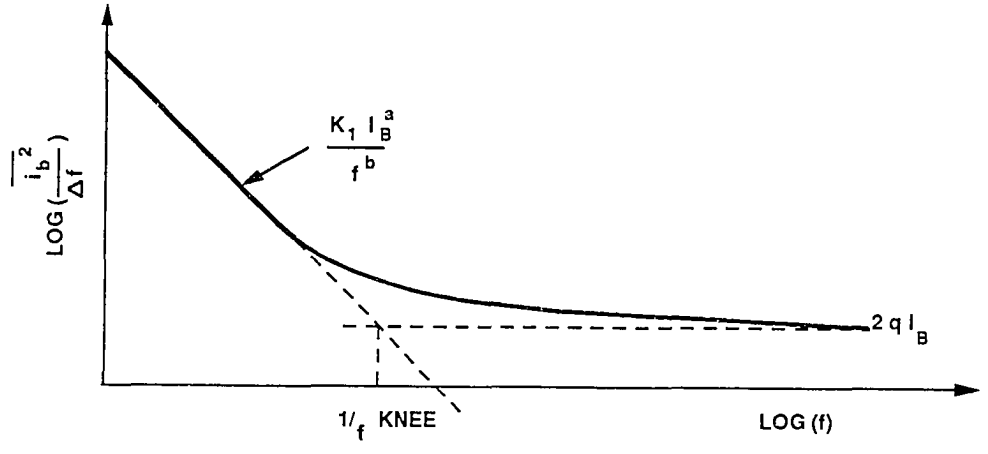


Figure 10: Noise spectrum, due to shot and excess noise, of a typical device.

diode mixers operate best when their source impedance is comparable to their load impedance for reasons discussed in Chapter 4, this represents a design challenge. The mixer must operate into as high a load impedance as possible in order to reduce the noise figure of the subsequent low frequency amplifiers. The optimum source impedance required for low noise operation of a typical bipolar op-amp is on the order of 10 KΩ.

2.3.2 Low Frequency Amplifiers

Silicon bipolar transistors and op-amps are chosen for realization of the low frequency amplifiers. Although these devices are better suited than other types[1], there are several challenging problems arising from their use. First, the $1/f$ frequency knee of these transistors is between 100 Hz and 1 KHz which is within the signal band of this application. Second, the source impedance required for optimum noise performance, $R_{n_{opt}}$, is in the range of 10 - 100 KΩ[33], far higher than the impedances likely

[1]Complementary Metal Oxide Semiconductor (CMOS) can be used to design low noise amplifiers however, as the $1/f$ frequency knee for these devices is typically between 1 KHz and 50 KHz, they must be operated above these frequencies if low noise performance is desired [27]. In addition the source impedances required for minimum noise temperature are far greater than those typical for the direct conversion receiver. $R_{n_{opt}}$ is in the range of 1 - 10 MΩ for a standard CMOS op-amp [33].

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to be presented by the output of an RF mixer. A goal of the work on amplifier design is therefore to identify the noise mechanisms and drive conditions that set the source impedance for minimum noise operation. Then various amplifier configurations can be examined to see which best meets the requirements of the direct conversion receiver. Ideally a standard op-amp circuit may be able to be simply modified, either by selecting a particular input device or by varying the bias applied to the input transistor, in such a way as to optimize noise performance at low source impedances. If not, an amplifier designed specifically for this receiver can be constructed. In either case, determination of the dominant amplifier noise sources at various frequencies within the signal band is necessary so that the final amplifier configuration can be chosen correctly.

A second design criteria for these amplifiers is their gain and stability. The gain of the amplifier stage must be calculated to insure high receiver dynamic range; it cannot be too large in case the power in the adjacent channels, denoted in Fig. 9 by I_1 and I_2, saturates the filter stage. It is difficult to guarantee amplifier stability, particularly if it operates at DC and possesses high gain.

In order to overcome the problems of in-band $1/f$ noise and DC drift arising from all the components in the low-level signal circuits and to insure the stability of the receiver, a DC notch filter will be incorporated into either the active filter or the amplifier. The 'I' and 'Q' channels will then be AC coupled. The amplifier must be optimized for operation with several DC notch filter bandwidths as the lowest required frequency of operation will set its design. The bandwidth of the filter is set by the requirement to guarantee stability without adversely effecting the recovery of the transmitted information as the DC notch filter at baseband effectively removes the signal power previously centered about f_c. Phase lock loop circuitry will need to be implemented upstream from the notch filter. Certain modulation types may be unaffected by the filter's presence, others may require special generation circuits for use with this receiver. For example, techniques developed for fading channels such as transmit tone-in-band can be applied for generation of both analog and digital signals [49].

The DC notch filter must be constructed with a sufficiently narrow bandwidth that

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its impact on the signal spectrum is minimal but large enough that the amplifier can be designed to possess low noise temperature at the lowest remaining signal frequency of interest.

2.3.3 Low Noise Active Filters

These circuits serve to perform the first stage of filtering. Their bandwidth is that of the wanted signal ($BW_{filter} = \frac{BW_{RF}}{2}$). Because they are cascaded by a subsequent filtering stage as shown in Fig. 1 they do not set the receiver selectivity alone but act primarily to reduce the level of the out-of-band interferers so that these signals do not saturate the next filter stage.

To insure that the receiver possesses a high dynamic range, it was decided that for every dB of gain provided in the wanted signal band the power in the adjacent signal band should be reduced by a dB. Thus each gain stage was designed to have a nominal gain of 30 dB and to provide 30 dB of adjacent channel rejection at its output. In typical land mobile systems, the adjacent channel interferer is located 900 MHz away from the edge of the wanted signal band.

Because the receiver's in band signal-to-noise ratio is not yet set, the noise performance of the filter over the wanted signal band is still of importance. The primary constraint on filter performance is therefore to achieve the above gain response while minimizing the amount of added noise. For this reason, the feedback elements must be chosen to optimize the noise temperature performance of the filter. Receiver selectivity will be set by the performance of this active filter and the ensuing CMOS filter.

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Chapter 3

The Mixer Analysis and Design Tool

3.1 Introduction

The next three chapters are concerned with the design of a low conversion loss mixer for the direct conversion receiver. Conversion loss is a measure of the mixer's efficiency in translating the input signal from its original carrier frequency to a specified output frequency. It is defined as the ratio of the carrier power at the input frequency to the carrier power at the output frequency. This chapter begins with a review of past work in mixer analysis and follows with a description of the mixer design tool that has been developed to design the mixers for the direct conversion receiver. Chapter 4 develops the measures that are used to examine these waveforms and establishes the design criteria for low conversion loss optimization. Mixer operation with purely resistive diodes is considered first. Subsequently the degradation in mixer performance is quantified for operation with diodes having substantial barrier capacitance. In Chapter 5, the design tool is used to develop mixer circuits that can take advantage of the diode's nonlinear capacitance to attain performance equal to or superior to that with purely resistive diodes. In all chapters simple mixer circuits are selected as the basis for our analysis and optimization so that issues fundamental to mixer design can be studied. Fortunately this criteria for circuit selection concurs with those of designing

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a mixer with low implementation cost for the direct conversion receiver. This work is therefore confined to the study of single ended and single balanced mixer circuits. A summary of these three chapters can be found in [20].

Section 3.2 summarizes past mixer work and presents the motivation for an alternative design tool. The conventional approach to mixer analysis is rooted in a frequency domain analysis of the diode and mixer circuit and possesses certain drawbacks. On the one hand, the frequency domain problem formulation is a powerful design tool which can be used to understand idealized mixer operation. For instance, given an idealized diode without series resistance or barrier capacitance, it is possible to derive the set of circuit impedances that should be presented to the diode by the circuit at each sideband frequency in order that optimum conversion loss be achieved. However these frequency specific matches are often difficult to implement practically. On the other hand, the frequency domain problem formulation, implemented on a computer, can result in a powerful analysis tool for complex circuits with nonidealized diodes. For example, once a particular mixer circuit has been analyzed for its specific relationship between input and output variables then this technique can predict mixer performance for an arbitrary diode given enough computing power. But each new circuit, single ended, single balanced, or double balanced, requires a separate derivation of the solution as the rearrangement or addition of circuit components imply new relationships between circuit variables. This leaves the designer in a position where, although she can analyze a circuit of arbitrary complexity or specify the circuit matches required for optimum performance with an idealized diode, she will have a difficult time deciphering the route to optimum circuit performance given practical diodes and practical circuit constraints. Our mixer tool seeks to remedy these problems by providing guidelines for mixer design and a framework for circuit optimization capable of working with ideal and nonideal diodes.

The design tool is detailed in Section 3.3. Our approach has been to use a time domain technique for computer-aided mixer analysis and design. This design tool utilizes SPICE to arrive at the steady state solution for the currents and voltages in a mixer circuit. These non-sinusoidal waveforms are studied to understand the

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interaction of diode, circuit, and drive conditions. Criteria are developed to optimize mixer performance, some of which have been derived from the graphical output characteristic of this design tool. Circuit characteristics such as conversion loss, input and output impedances at given frequencies are rapidly calculated by using a Fast Hartley Transform to generate the Fourier transform of the required waveforms. The technique is ideally suited for the study of mixer circuits that are specified by their lumped circuit equivalents rather than by the match they provide at specific frequencies.

Conclusions are given in Section 3.4.

3.2 Motivation for a Time Domain Approach to Mixer Design

A time domain analysis and design technique has been developed for mixers where the circuits are most often visualized in terms of lumped elements rather than as a series of matches at specific frequencies. This approach has proved useful in understanding the interplay of diode and circuit elements and in the design of low conversion loss mixers. The design tool described here differs from other time based analysis in that it is not confined to the use of an ideal diode [32,36], to a particular circuit [3], or a specific ratio of input/output frequencies [42]. It is the first report, to my knowledge, of a general purpose time domain design tool.

The conventional approach to mixer design has been to frame the problem in the frequency domain. This method has proved very useful in the analysis of certain types of mixers and has been well corroborated by experiment. As a consequence, results obtained from the two methods will be compared in Section 4.4. To provide the framework for this comparison and to give some motivation for the development of this tool, the characteristics of the conventional technique will be reviewed here.

The theoretical foundation for mixer analysis was laid out in 1948 by Torrey and Whitmer [67]. They divided the problem into a nonlinear large signal and a linear small signal problem. The large signal problem consists of finding the diode current

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and junction voltage given the bias (DC) and local oscillator (LO) conditions and the mixer circuit, the latter represented by embedding impedances at the LO frequency and its harmonics. The small signal analysis involves the application of linear network theory to calculate conversion loss, input and output impedance by modelling the mixer as a linear multiport network where each port represents a different frequency. The most important of these small signal frequencies are the input signal frequency (RF) and the output difference frequency, $|f_{LO} - f_{RF}|$. The latter frequency is known in heterodyne receiver systems as the intermediate frequency (IF); although $|f_{LO} - f_{RF}|$ in the direct downconversion receiver spans from DC to 1/2 the RF bandwidth, the term of intermediate frequency will be used in this chapter to refer to the mixer output at the difference frequency. This model of the diode and circuit is shown in Figure 11.

Once the large signal problem is solved, the conductance and capacitance waveforms are found, their Fourier coefficients calculated and entered into a conversion matrix. The impedance presented by the circuit at the diode terminals are calculated at each of the small signal frequencies produced by the mixing process and included into the conversion matrix. Current at a particular frequency, or port, can now be related to the voltage at each small signal frequency, or network ports, through the admittance terms of the conversion matrix. Standard network theory is applied to find the conversion loss, input impedance at the signal frequency, f_{RF}, and output impedance at the difference frequency, f_{IF}. The challenges in mixer analysis using this technique have been to find reliable solutions for the large signal nonlinear problem and to formulate the conversion matrix for different mixer circuits.

Central to this method is the view, both for large and small signal analysis, of the diode as an infinite set of signal generators, one at each of the mixer products, and of the circuit as providing an array of narrow band embedding impedances at each of these frequencies.[1] These impedances, reactive and/or resistive, control the amplitude and phase of the currents in the circuit. The large signal problem consists of finding the values of the generators given the embedding impedances at the LO and

[1]The mixer products can be written in terms of the LO and RF frequencies as $k \cdot f_{LO} \pm l \cdot f_{RF}$ where k,l can be any integer.

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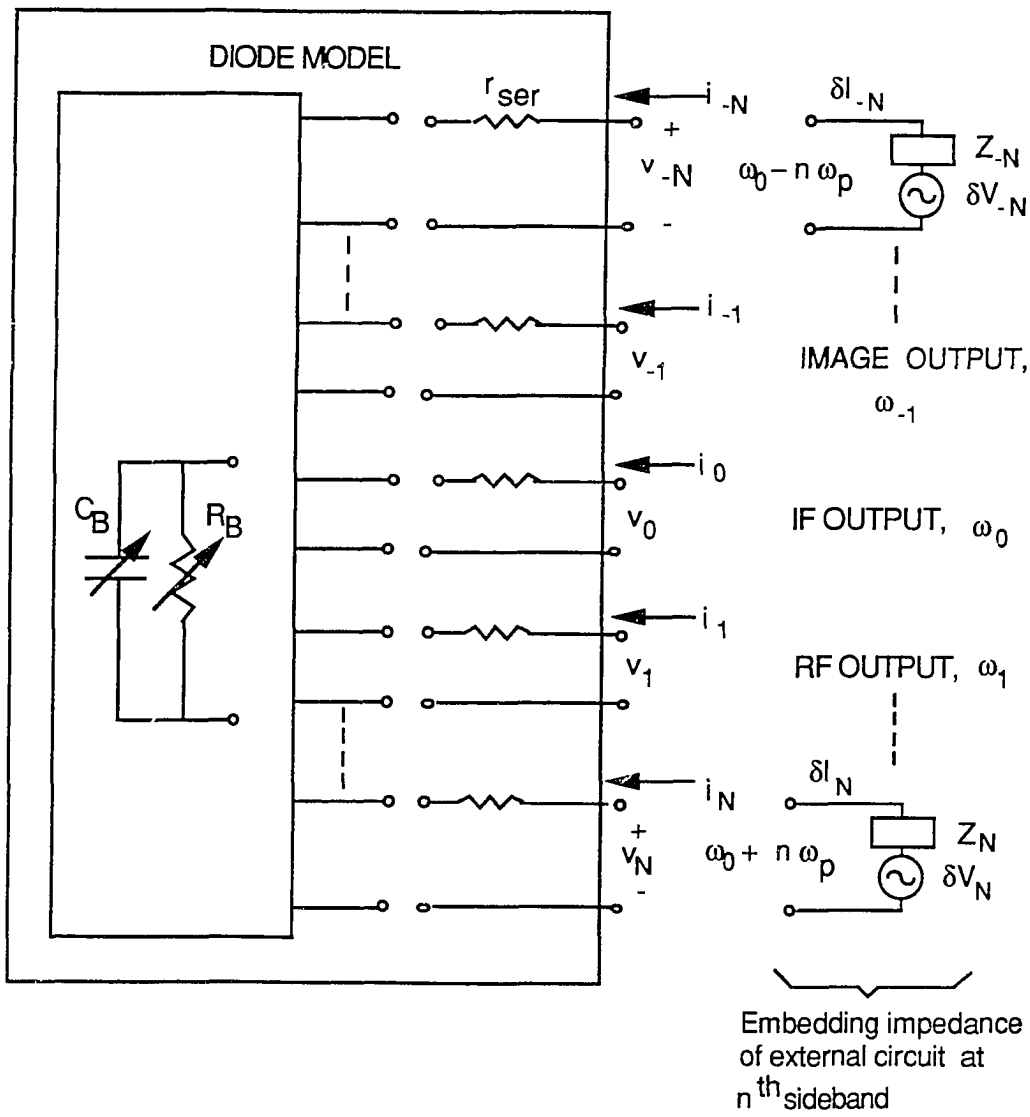


Figure 11: Small signal representation of the mixer as a multifrequency linear multiport network.

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its harmonics. The small signal problem consists of finding the optimum values for the impedances at the small signal, or sideband, frequencies.[2] The art of the designer is to decide how many frequencies she will consider and in cleverly juggling the diode condition and both sets of impedances to maximize the mixer performance.

Prior to the advent of computers, assumptions about the mixer diode and circuit had to be made to find a closed form solution for the large signal problem and to reduce the order of the conversion matrix to a practical number. Torrey and Whitmer assumed the mixer circuit and/or the diode's barrier capacitor short circuited all LO harmonics. They then wrote the diode voltage as the sum of a DC term and a sinusoidal term at f_{LO}. Having done this, the diode current could be expressed in terms of Bessel functions and solved for. The small signal problem complexity was reduced to a manageable level by considering the effects on conversion loss of terminations at the lowest sideband frequencies only, ie. the RF, image and IF frequencies. The image frequency is that frequency that when beat against the LO produces an output at f_{IF}. It is the n = -1 sideband. Postulating that the most important sideband was the image frequency and assuming that the higher sidebands were shorted, the conversion matrix could be reduced to a 3 by 3 matrix. To reduce the numbers of unknown terms in the matrix, they considered a low Q mixer diode - wherein there are no resonant circuits that can differentiate between the signal and the image, nor between the IF and DC. Under these assumptions, they derived conversion loss expressions which were used by many mixer designers up until the 1970's [6,55]. Torrey and Whitmer also found limits for the conversion loss of an ideal, purely resistive, diode mixer to be 3dB for equal terminations at the signal and image frequencies and 0dB when the image frequency was short or open circuited.

The need to increase the complexity of the analytic solution to enable mixer theory to predict performance more closely was brought out by several authors. Barber [6], and, Fleri and Cohen [22] realized that the diode junction voltage could not be expressed as a simple sinusoid due to the effect of spreading resistance and the existence

[2]The sideband frequencies refer to the small signal frequencies located f_{IF} above or below a LO harmonic. They are specified by the subscript n where $f_n = f_{IF} + n \cdot f_{LO}$.

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of the non-linear barrier capacitance. Barber also showed that a sinusoidal conductance did not produce the optimum conductance waveform for minimizing conversion loss. Egami presented an analytic treatment of the large and small signal problems considering an infinite number of LO harmonics and sideband frequencies [17]. To solve the large signal analysis he developed a harmonic balance technique to iteratively solve for the circuit waveforms for a specified number of LO harmonics. Unfortunately, this method assumed constant diode capacitance and his computer program considered only three harmonics of the LO. Saleh analyzed mixers circuits and their optimum conductance waveforms from a theoretical point of view[55]. Modelling the diode as a non-linear resistance only, he showed that the optimum termination for the sideband frequencies was reactive but stressed that the ability to achieve the optimum conversion loss with practical conductance waveforms depended on the method in which each sideband frequency was terminated.

More recently, work in the frequency domain approach to mixer design has concentrated on generating algorithms for faster and reliable convergence of the large signal problem with eight or so LO harmonics included [37,28,31,59] on including the effects of non-linear barrier capacitance into the conversion matrix (considered by Torrey and Whitmer but reintroduced by Held and Kerr [30]); on the study of mixer noise, including shot, thermal and scattering noise, and its inclusion into computer analysis [29]; and on extending this analysis to balanced mixers [44,58] or for any number of diodes [21]. Consequently, theoretical predictions of mixer performance seem now to be in good agreement with experimental results for both the single-ended mixer [38,30,61], and balanced mixer design [58]. In addition, the frequency domain technique has been extended to the analysis of GaAs FET mixers with good results [45].

The frequency domain technique has been described in detail because it provides an excellent analytic framework for the solution of a difficult problem. It works very well in predicting the performance of waveguide mixers when precise matches can be made at specific frequencies or in mixers where the embedding impedances are already known [61]. For this reason it is used in this chapter to corroborate the results generated by our time domain technique, and, in Chapter 5, to compute the

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noise temperature for several mixers.

However, as a design tool, this frequency domain technique has several drawbacks. Most importantly it does not give the designer any insight into the role of the circuit, the relative importance of various terminations, the phasing of energy flow between diode and circuit. Saleh's work produced guidelines on circuit design by examining how close the conversion loss of a given circuit could come to the ideal limit for a given exponential diode. But these guidelines assume a perfect short or open is presented at each sideband frequency and they assume a purely resistive diode. If these conditions are or can not be met, this analytic tool does not point to the direction to be taken nor does it provide the designer with a direction in which to proceed for circuit optimization.

Secondly, it is often difficult to translate the prescribed terminations at each sideband frequency into physical realization. Millimeter wave mixers, where the LO harmonics and RF circuits can be isolated by waveguide or microstrip filters, are ideal candidates for design by this technique. But for lower frequency mixers, UHF or microwave mixers, not only is it often difficult to implement specific matches at a set of frequencies, it is more realistic to think of the design problem in circuit terms.

In the following section a technique is presented that has been developed for the design of UHF and microwave mixers designed to address these design challenges. Working in the time domain, generating extensive plots of the diode and circuit waveforms, it hopes to sharpen the designer's understanding of the mixing process; using SPICE [72], a circuit simulator program, to solve the analytic problem, it forces the designer to think in terms of circuit elements and of designing one matching circuit for the diode; lastly, the development of a quantitative technique for mixer evaluation allows for an optimization procedure to be developed.

Circuit simulation in the time domain has certain advantages: it allows the designer to study the effects of nonlinear barrier capacitance, change diode parameters or package parasitics without having to reformulate the circuit equations; single ended and balanced mixers can be easily analyzed. Indeed, wherever components can be modelled by lumped elements as is often done for MMIC design [53], this technique can be applied.

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Different issues emerge when comparing the two approaches. The problem of convergence is, for the most part, eradicated by the use of a circuit simulator. The accuracy of the solution no longer depends on the number of LO harmonics and sideband frequencies considered but on the setting of the convergence tolerance and the number of samples/sec taken. Practical circuits are now easy to analyze whereas ideal ones with infinite Q's take clever formulation or long computation time [40].

3.3 The Design Tool

The mixer analysis and design technique consists of three parts. First, the circuit is described by its network matrix and SPICE is run to find the time waveforms in the circuit. Secondly, plots are generated of these waveforms and of computed waveforms, such as diode conductance and capacitance. This is necessary for the designer to obtain a physical understanding of the interplay between diode and mixer circuit and see the tradeoffs of bias and drive level. As will be emphasized in Chapter 5, graphical output is a necessary part of a design and optimization tool especially when the diode model includes nonzero barrier capacitance. Thirdly the SPICE data is used as input to a Fortran program. Using it, the diode waveforms are examined, parameters such as diode 'ON' time, or, the proportion of the LO cycle during which the diode conducts, maximum and minimum diode voltages and currents are found. The Fourier transform of certain signals are quickly found with the aid of the Fast Hartley Transform (FHT) [12]. These are used in obtaining an accurate measure of conversion loss, imput and output impedance. The Fourier coefficients of the small signal diode conductance, $g(t)$, and capacitance, $C_B(t)$, waveforms are calculated for subsequent use in computing results using the frequency domain problem formulation.

A flowchart of the tool is shown in Figure 12. Although it may look complex, the analysis of a SPICE run can proceed through the program shown in an automatic fashion with the use of a command file when operating systems such as VMS or UNIX are run.[3] The optimization process for mixer design once a particular circuit has been

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selected is shown in Figure 3 and will be discussed in Section 3.3.5. In this section we provide the motivation for the calculation of the parameters shown and describe their use in the optimization process. The FORTRAN programs, ndfft.for, zout.for, and one of the graphical programs, cjplot.for, are listed in Appendix A.

3.3.1 Mixer Circuit

Figure 13 shows a block diagram of a single-ended diode mixer. The LO is fed through a directional coupler and the bias, if it is necessary, is applied through an RF choke. Matching circuits are shown on the input and output ports of the diode. The mixer depicted will be referred to as a 'Z' mixer, to use Saleh's terminology, but 'Y', 'G', or 'H' mixers may be constructed. A simple circuit realization that will be used to illustrate the operation of this program is shown in Figure 14. The RF and LO sources are shown as current sources with a common source impedance, R_S. Should bias be desired it is applied in parallel with the RF and LO sources and a capacitor, C_S, is added in series with L_S. The output signal is taken as the voltage on the load resistor, R_L. The inductor, L_S, provides a DC and IF return path. The output capacitor, C_{LD}, provides a ground for the RF and LO sources. Thus the diode appears grounded from the signal and LO source point of view as well as from the IF or output port. As seen from the two diode terminals, the circuit appears resistive at all frequencies, including the LO harmonics and sideband frequencies generated by the diode. This mixer circuit will therefore be classified as a *Resistively Matched* ('RM') mixer circuit.

We would like to examine the diode and circuit waveforms and compute certain mixer parameters. Minimization of conversion loss is, of course, an important element of mixer design as is the maximization of the ratio of R_L/R_S for many UHF applications. This ratio reflects the need to match from a RF source impedance in the 50Ω range to an IF amplifier which invariably has a higher source impedance. This circuit can be described by the SPICE file shown below it.

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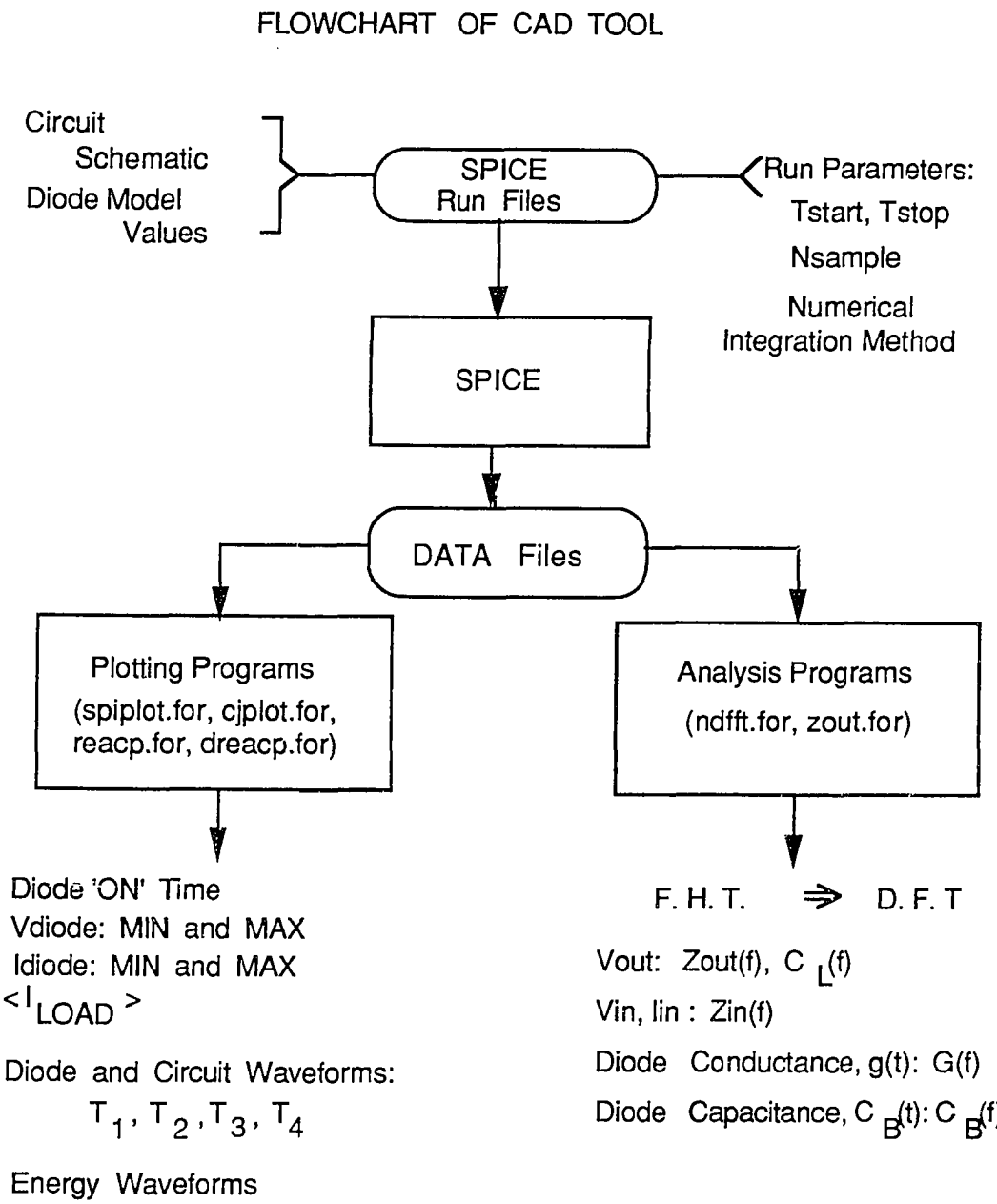


Figure 12: Flowchart of the design tool.

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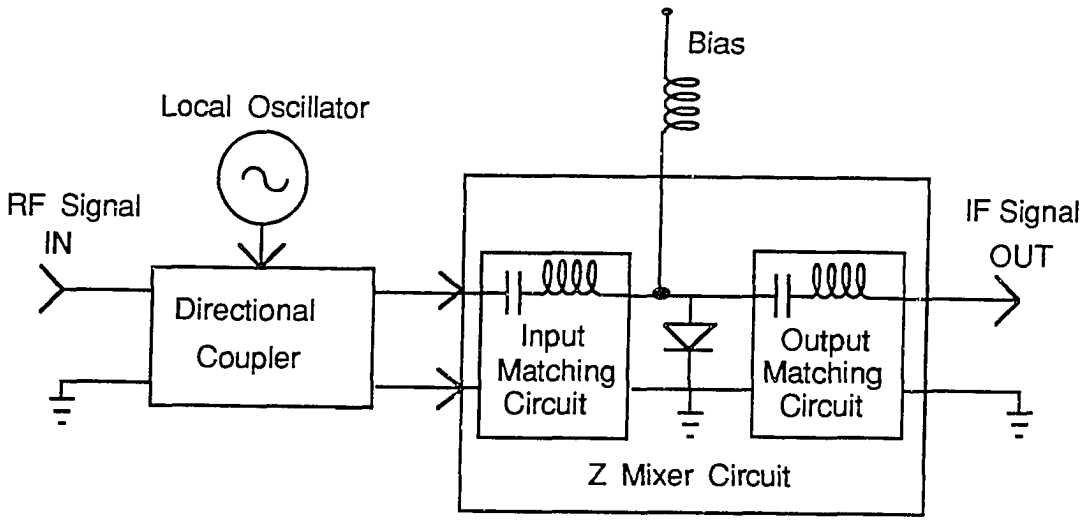
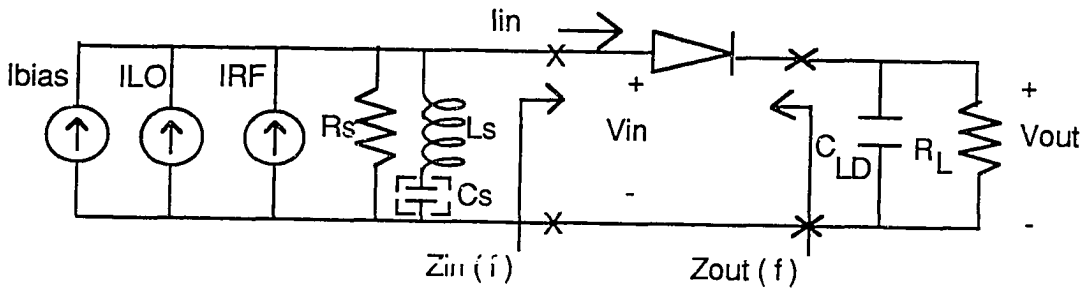


Figure 13: Block diagram of a single ended mixer.

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(a)

```
RESISTIVELY MATCHED S/E MIXER

SINGLE ENDED MIXER
IBIAS 0 21 DC 0.0
VIMB 21 15
ILO 0 7 SIN(0 4.0M 900MEG)
VIM0 7 15
IRF 0 8 SIN(0 .4M 909MEG)
VIMR 8 15
VIMT 15 13
VIM1 13 12
RS 12 0 1000
LS 12 0 1.8UH
VIM2 13 9
VIM3 9 6
D1 6 3 DIODE1
RPD 9 3 5MEG
VIM4 3 23
RL 23 0 1000
VIM6 23 20
CLD 20 0 2.8PF
.MODEL DIODE1 D RS=10.0 IS=1.0E-14 N=1.0 CJO=.001PF VJ=.9 BV=20
.OPTIONS ACCT OPTS  ITL3=10 ITL5=20000 LVLTIM=1 LIMPTS=40000
.TRAN 27.13P .222US .111US
.PRINT TRAN V(3) I(VIM3) V(6,3) I(VIM2) V(13) V(0) V(0) V(0)
* Maximum parameters printed in one row is 8.
.END
```

(b)

Figure 14: *Resistively Matched* mixer: (a) circuit diagram; (b) corresponding SPICE run file ($f_{RF} = 909$ MHz).

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3.3.2 Use of SPICE

SPICE is a circuit simulator program. It was written predominately as an analysis tool for circuit design. It requires a nodal description of the mixer circuit as input. SPICE sets up the integro-differential equations, based on Kirchoff's laws, that represent the mixer circuit as a network. It makes an initial estimate of currents and voltages in the circuit branches and iterates until a solution has been found that satisfies the network equations within a prescribed convergence error. SPICE evaluates the network state from zero time to a user specified final value, stepping along at a internally generated time interval that is varied to insure rapid convergence within prescribed tolerances. The results are printed from a given start time value in user specified time increments, Δt.

Run Parameters

All simulations were performed using SPICE Version 2G-4, run on Helens, a VAX 11-780, at Stanford. Figure 14 shows the SPICE run file for the circuit in Figure 13. The .TRAN statement calls for a transient analysis to be performed from t = 0.0 sec to 0.222μs. The results are to be printed every 27.13ps from 0.111μs to 0.222μs. The trapezoidal numerical integration method was chosen; it is the default method. Trapezoidal integration generally results in reduced program execution time while maintaining accurate results. However certain circuits do not converge when trapezoidal integration is used or produce waveforms with imposed small signal oscillations that can be removed when the simulation timestep is reduced. In these cases the alternate integration method, the Gear method, is a better choice. This method acts as a filter removing the oscillations found in the trapezoidal method. The .OPTIONS statement can be elucidated as follows. The iteration timestep control is used to ensure that the transient analysis would run without generating a timestep too small run time error; this is specified by setting LVLTIM = 1. The default value (LVLTIM = 2) calls for the truncation-error timestep control to be used. For this nonlinear circuit specifying LVLTIM = 2 resulted in a diode current which possessed hysteresis and was highly unsymmetrical when the voltage driving it was symmetrical. ITL3

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sets the lower transient analysis iteration limit. The default value is 4; it has been reset to 10. The circuit solution must converge to the set tolerances within less than 10 iterations before the timestep can be increased. LIMTPS and ITL5 are limits that specify the overall duration of the SPICE run. ITL5 specifies the total number of iterations allowed per transient analysis. LIMPTS sets the total number of points to be printed per analysis. OPTS causes the options chosen to be printed. ACCT causes accounting and run time statistics to be included at the end of a run. This is useful in determining the rapidity with which the simulator is converging upon the solution.

The data from ACCT can be examined to determine if the specified timestep or program tolerances should be changed. Specifically the ratio of NUMTTP to NUMNIT, or, the ratio of the number of timepoints at which the simulator was required to calculate the circuit solution in order to stay within the prescribed accuracy to the total number of iterations taken during the transient analysis is a measure of the simulator's efficiency. It should be less than 8. The number of times the simulator has to take smaller timesteps to stay within convergence, NUMRTP, is a measure of the difficulty of the circuit analysis. If the total number of timepoints at which the simulator calculated the circuit condition, NUMNIT, is 4 or 5 times greater than the number of points requested for output, JTRFLG, then the timestep requested should be decreased or the tolerances increased. For the run file in Figure 14 the ratio of NUMTTP to NUMNIT was 2.9. NUMRTP was 62 and the ratio of NUMTTP to JTRFLG was 2.05. When the timestep specified by the user was made 4 times smaller so that $\Delta t = 6.78$ps, NUMRTP dropped to 1, $\frac{NUMTTP}{NUMNIT}$ and $\frac{NUMTTP}{JTRFLG}$ were equal to 2.0.

To quantize the mixer performance, the Fourier transform of various SPICE generated waveforms must be calculated. Care must be taken in specifying the time increment and the time period, T, so that the Fourier transform can be correctly found. Mixers generate many spurious responses. Since the number of samples/sec $(\frac{1}{\Delta t})$ sets the frequency limit for the Fourier transform $(f_{max} = \frac{1}{2\Delta t})$, Δt must be chosen so that the effect of aliasing, superimposing the spectra from $f_{max} + \Delta t$ on to $f_{max} - \Delta t$, is small in the band of interest, for example from DC to the tenth harmonic

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of the LO. A second consideration is setting Δt to ensure that enough samples are taken at the highest frequency of interest. This guarantees the accuracy with which the phase of that frequency is calculated.

To keep the computation time and file storage requirements low the length of time for the simulation, T, should be no longer than one cycle of the IF. Then the frequency increment of the discrete Hartley transform (DHT) will be equal to the IF frequency ($\Delta f = \frac{1}{T} = f_{IF}$) The initial time should be chosen to allow the transient response of the circuit to have died out. The exact relationship between T and Δt, ($T = N_{sample} \times \Delta t$) must be set so that the number of points taken is a power of 2.

For example, in the run shown in Figure 14, Δt was chosen to that $f_{max} = 20 \cdot f_{LO}$. The power level at the 20th LO harmonic is 92dB below the power at f_{IF}. This choice of Δt resulted in 41 samples/LO cycle or 4 samples at the tenth LO harmonic. The simulation results are recorded for 0.111μs - one cycle of the IF frequency. The number of samples is 4096.

N is quite large. Set much higher the simulation would have become impractical. Its size sets a limit on the ratio of input to output frequencies that can be run straightforwardly. However in many cases results from one mixer input/output frequency ratio can be extended to a different ratio if the same circuit conditions can be created. For instance a model of a short at the input frequency and an open at the output becomes easier to model the greater the difference in frequency. Thus the SPICE results could easily be applied to mixers with greater frequency differences than could be conveniently run. In this example, f_{RF} = 909MHz, f_{IF} = 9MHz. The reactive circuit elements, L_S and C_{LD}, have been chosen to provide as close to a short as possible at f_{IF} and f_{RF}, respectively. The results of this circuit can confidently be extended to f_{IF} = 9KHz or 9Hz.

The mixer results shown in Table 1 can be taken to represent the performance of the circuit in Figure 14(a) operated at the specified frequencies with the given reactive circuit and diode components or taken to represent the performance of this circuit operated at a scaled set of input/output frequencies with similarly scaled reactive components. For example, f_{RF} was set to 505Hz, f_{IF} to 5Hz, L_S to 3.183H, C_{LD} to 5.092μF, the diode capacitance at zero junction voltage, C_{j0}, was scaled to to 1.8

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pF and the transit time to 0.1ns. A comparison of the performance of these two runs is given in Table 1. The nomenclature used in Table 1 will be elaborated on in Section 3.3.3.

Table 1: Performance Comparison of Two Frequency Scaled Mixer Runs

	909 MHz Run pdiod5575	505 Hz Run pdiod557
Conversion Loss	4.33dB	4.33dB
$V_{d_{max}}$, $V_{d_{min}}$	0.72V, -4.34V	0.72V, -4.38V
$I_{d_{max}}$, $I_{d_{min}}$	3.63mA, -24nA	3.66mA, -31nA
$\frac{T_{NL}}{T_{LO}}$, $\frac{T_{TON}}{T_{LO}}$	0.055, 0.45	0.065, 0.46
$Z_{in}(f_{RF})$	1.28 KΩ $\angle -3°$	1.28 $K\Omega$ $\angle -4°$
$Z_{out}(f_{IF})$	1.15KΩ $\angle -7°$	1.1KΩ $\angle -7°$
(R_{L_1}, R_{L_2})	(1.1K, 800Ω)	(1.1K, 800Ω)

When more accuracy in evaluating the higher harmonics is necessary or when more complex circuits are analyzed the number of samples per LO cycle must be increased. For this simple circuit increasing N_{sample} to 16384 points does not change the conversion loss or the estimate of lower sideband frequencies. However the estimate of the phase and magnitude of the fifth and higher harmonics is improved as the sample size increases. The output for both runs is included in Appendix A, the values of the LO harmonics are compared in Table 33 of Appendix A.

Diode Model

SPICE allows one to specify either the diode geometry or model parameters. Several silicon Schottky diodes were used in the mixer simulations. Si Schottky's were chosen over GaAs Schottky's and point contact diodes because of their lower excess noise

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(1/f) power[4]. As the mixer output band will span from DC to half the RF bandwidth and the information band will span from a few hundred Hz above DC to half the RF bandwidth, minimizing the 1/f noise component is key to achieving a low mixer noise temperature over the band of interest. Medium barrier Si Schottky diodes are used in these simulations as they are considered to have lower series resistance and hence provide lower conversion loss than a low barrier device. Both n-type and p-type diodes are simulated; n-type diodes are felt to have lower conversion loss than p-type, however, p-type may generate lower 1/f noise. The advantages of different diode types are detailed in Section A.4 of Appendix A.

The diode model is shown in Figure 15: the spreading, or series, resistance, actually a function of diode current and frequency, is here modelled as a constant; the nonlinear small signal barrier resistor and capacitor are denoted by R_B and C_B; package parasitics, such as L_p and C_p, are shown.

The current in the diode, I_d, can be divided into two components, that in the barrier resistance, I_{d_r}, and that in the barrier capacitance, I_{d_c}:

$$I_d = I_{d_r} + I_{d_c}. \tag{4}$$

These currents can be written as:

$$I_{d_r} = I_S(\exp(\frac{qV_j}{nkT}) - 1), \tag{5}$$

where I_S represents the saturation current of the diode and n is the ideality of the diode, typically close to 1.0 for a Schottky device; and

$$I_{d_c} = C_B \frac{dV_j}{dt} \tag{6}$$

where

$$C_B = \frac{C_{j0}}{(1 - \frac{V_j}{\phi})^M} \tag{7}$$

and ϕ represents the built-in junction voltage. Its coefficient, M, is 1/2 for a linearly graded junction and 1/3 for an abrupt junction.

The diode voltage, V_d, can be written in terms of the junction voltage, V_j, and the voltage drop accross the semiconductor's spreading resistance. This resistance is

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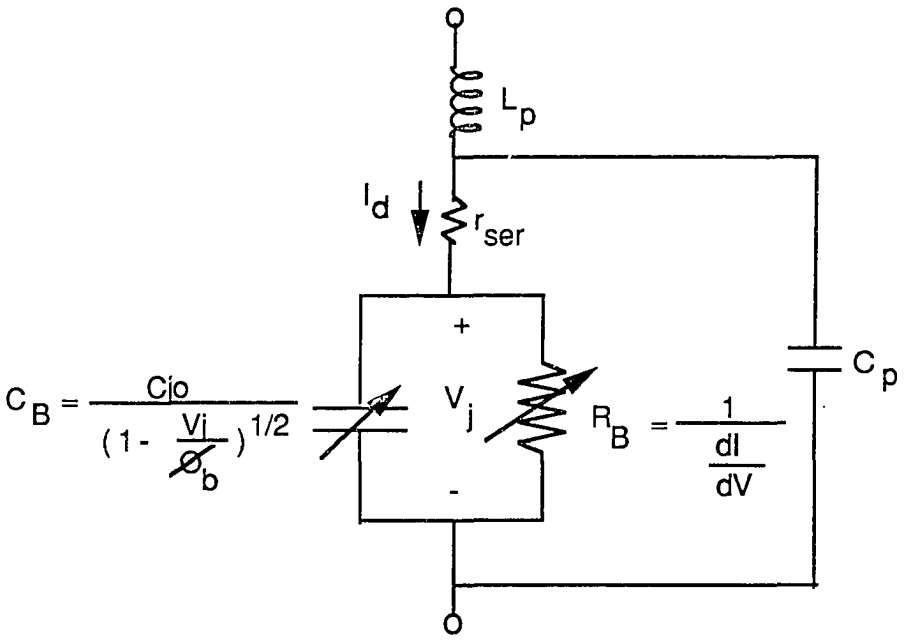


Figure 15: Diode model with package parasitics.

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modelled as the series resistance r_{ser} and is shown in Figure 15. The relationship is given by:

$$V_d = V_j + I_d \times r_{ser}. \tag{8}$$

Table 2 gives the values of the diode model parameters for three devices. The first, DM_1, represents a p-type medium barrier Si Schottky device; the second, DM_2, models a n-type medium barrier Si Schottky device; the model values for DM_3 have been estimated from a specific Si Schottky diode, Toshiba's 1-2J1A. Section A.4 of Appendix A gives diode paramater values developed in mixer literature as well as diode characteristics taken from Nippon Electric Co. and Toshiba. In this section the methods for estimating diode parameters from current-voltage and barrier capacitance-voltage curves are given. The consequent range of diode parameters is used to determine those listed for DM_1 and DM_2. The majority of the simulations have used DM_1 for the device model. DM_2 and DM_3 have been used to check results and verify that the results obtained do not depend on a particular device and circuit but can be achieved with different devices at perhaps different bias and drive levels (as long as all devices have barrier capacitances and series resistances that are reasonably close). DM_1 is used as a purely resistive diode ($C_{j0} = 0.001$pf or, effectively, zero) and as a diode with non-zero barrier capacitance to study the effect on circuit performance and circuit optimization. In Section 4.2 mixer characteristics are examined as C_{j0} is varied from 0.25pF to 1.5pF.

Circuit Model

The circuit shown in Figure 14(a) was chosen as a beginning point for the design of the mixer in the direct downconversion receiver for the following reasons. The load resistance, R_L, was set equal to 1KΩ to model the desired impedance presented by the subsequent amplifier. This is a higher load impedance than is typical for UHF or microwave mixers (50Ω) but it is a very low source impedance for a baseband amplifier operating at frequencies of 10KHz or less. The source resistance, R_S, is set

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Table 2: Diode Parameter Values for Three Si Schottky Diodes Models

	DM_1 p-type	DM_2 n-type	DM_3 Toshiba
Series Resistance, r_{ser}	10Ω	6Ω	10Ω
Saturation Current, I_S	$1.0 \cdot 10^{-14}$A	$1.0 \cdot 10^{-10}$A	$1.0 \cdot 10^{-9}$A
Ideality Factor, n	1.0	1.0	1.04
Barrier Capacitance at Zero Junction Voltage, C_{j0}	0.25pF - 1.5 pF	0.25pF - 1.0 pF	0.6pF
Junction Potential, V_j	0.9V	0.62V	0.8V
Capacitive Coefficient, M	1/2	1/2	1/2
Reverse Breakdown Voltage, V_{RB}	20.0V	20.0V	20.0V

Note. DM_1 was run with n = 1.05 with optimum S/E circuit for $C_{j0} = 0.25pF$ and C_L decreased from 3.13 dB to 3.04 dB (Run *idiod2023*).

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initially equal to R_L.[4]

Ideally the source inductor, L_S, should be chosen to provide a short at f_{IF} and an open at f_{RF}, and, the load capacitor should be selected to provide an open at f_{IF} and a short at f_{RF}. The larger the difference between f_{IF} and f_{RF}, the easier it is to accomplish this. For $f_{RF}/f_{IF} = 10$, as in this simulation, the values of L_S and C_{LD} have been chosen to produce the following source and load impedances. For $L_S = 1.8\mu$H, $Z_S = 995\Omega \ \angle 5°$ at $f_{RF} = 909$ MHz and $Z_S = 101\Omega \ \angle 84°$ at $f_{RF} = 9$ MHz. For $C_{LD} = 2.8$pF, $Z_L = 62\Omega \ \angle -86°$ at $f_{RF} = 909$ MHz and $Z_S = 987\Omega \ \angle -9°$ at f_{RF} = 9 MHz. Identical impedances will be obtained if the RF and IF are decreased by the same factor as L_S and C_{LD} are increased. For the direct downconversion receiver, we would like to design a mixer with $f_{RF} = 909$MHz and $f_{IF} = 9$ KHz. The need for reasonable run times prohibit simulating this wide frequency difference and constrain us to translate the mixer performance results from 9 MHz to 9 KHz. This is possible as the simulated circuit will operate more closely to ideal (ie. provide better opens and shorts) at the lower IF frequency.

The magnitude of the RF signal level has been set to be 1/10 the LO level to permit the RF current in the circuit to be seen on the waveforms plots while disallowing the RF to effect the I-V characteristic of the diode. This assumption has been checked by running SPICE with $I_{RF} = I_{LO}/100$; identical conversion loss, Z_{in} and Z_{out} were obtained. The diode is modelled as having a 5MΩ resistor across it. Although this can be thought of as representing the bulk semiconductor resistance, the resistor was included as a precautionary means to help SPICE converge.

3.3.3 Graphical Interpretation

Several mixer currents and voltages are plotted for each SPICE run. Figure 16 shows the output voltage and diode waveforms for the 'RM' mixer circuit listed in Fig. 14(b). In Figure 16(a) the output voltage, $V_{out}(t)$, is plotted for one IF cycle. Some qualitative information about the mixer operation may be deduced from it: the peak-to-peak variation in the envelope gives a feel for mixer conversion loss; the average value of

[4]Circuits having other source resistances will be discussed in Section 4.2.

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the envelope is a measure of the dc level at the output, and the amplitude of the fluctuations within the envelope indicate the level of LO feedthrough to the output port. When several mixer circuits are run the qualitative difference in voltage levels of the DC, IF and LO signal levels will translate to a difference in power levels at DC, f_{IF} and f_{LO} as long as the circuits all use identical RF drive levels, source and load impedances.

To obtain a quantitative measure of the conversion loss, we must look at the variation of the average current in the load or, equivalently, current in the diode over one LO cycle. Conversion loss can not be calculated from the maximum current flow at a particular point in the LO cycle. The average current establishes the DC and IF Fourier component of the output voltage. Thinking of the output voltage as a sampled waveform, whose valued is measured once every T_{LO}, helps build the analogy between the operation of a complex mixer and that of a simple switching mixer. This analogy will be discussed in Section 21. To observe the diode's operation and to calculate the output voltage component at the IF frequency, $V_{out}(f_{IF})$, the diode voltage and current are plotted at four points along one IF waveform, when the phase difference between the RF and LO is 0°, 90°, 180° and 270° at T_1, T_2, T_3, and T_4, respectively. Figures 16(b) and (c) depict the diode condition when the RF and LO are in-phase and 180° out-of-phase. From the data in these plots, the output voltage at DC and IF can be estimated.

The maximum IF voltage occurs when I_{RF} and I_{LO} are in-phase at time T_1. The average diode current can then be calculated as:

$$\langle I_d(T_1)\rangle = \frac{1}{T_{LO}} \int_{T_1}^{T_1+T_{LO}} I_d(t)dt. \tag{9}$$

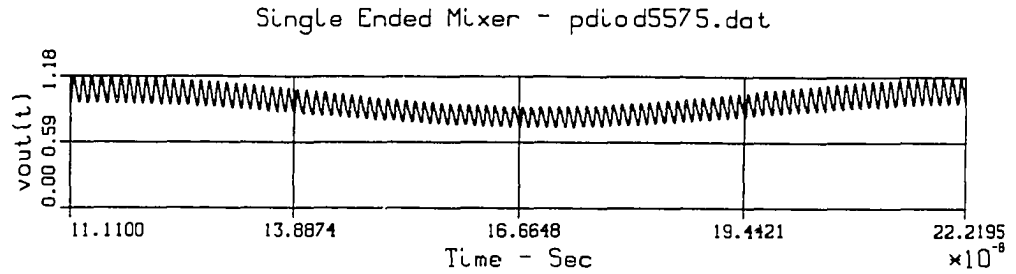
Similarily the minimum IF voltage occurs when I_{RF} and I_{LO} are 180° out-of-phase at T_3, $T_{IF}/2$ seconds after T_1, at which point the average diode current is:

$$\langle I_d(T_3)\rangle = \frac{1}{T_{LO}} \int_{T_3}^{T_3+T_{LO}} I_d(t)dt. \tag{10}$$

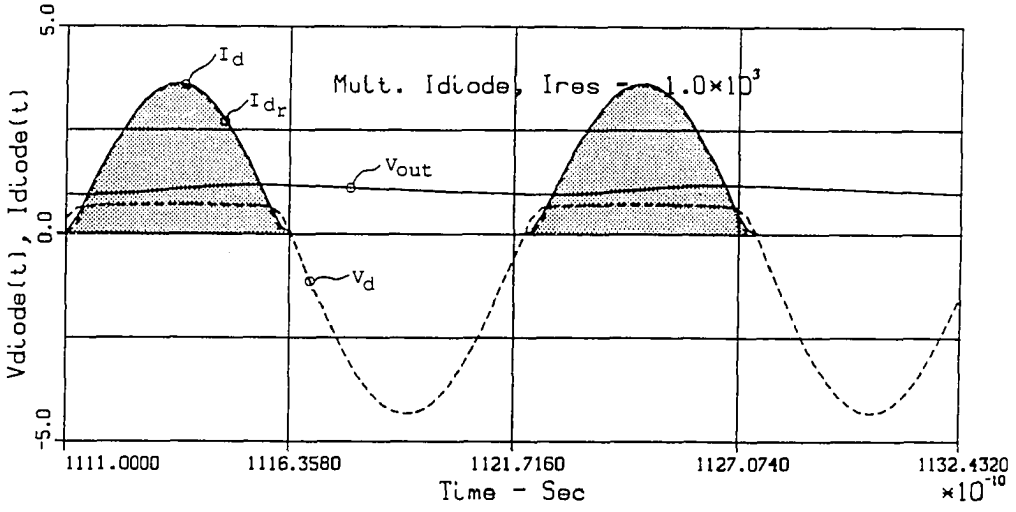
The DC voltage at the output can be written:

$$V_{out}(DC) = \frac{\langle I_d(T_1)\rangle + \langle I_d(T_3)\rangle}{2} R_L; \tag{11}$$

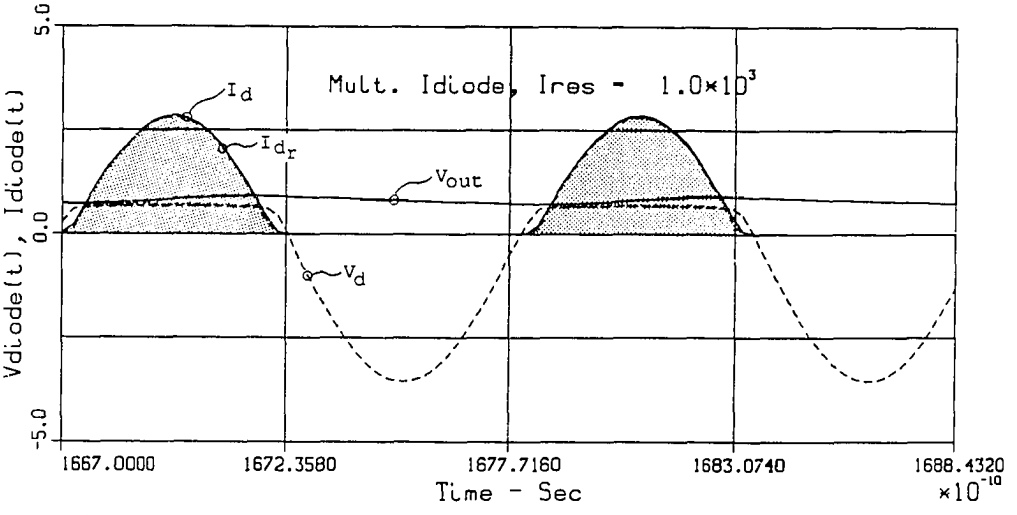
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(a) V_{out} (t) plotted for one cycle of the IF frequency



(b) In-phase diode waveforms



(c) 180° out-of-phase diode waveforms

Figure 16: Performance of a *Resistively Matched* mixer.

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the 0-to-peak IF voltage can be written as:

$$V_{out}(IF) = \frac{\langle I_d(T_1)\rangle - \langle I_d(T_3)\rangle}{2} R_L. \quad (12)$$

The power delivered to the load can be expressed as:

$$P_{load} = \frac{V_{out}^2(IF)}{R_L}.$$

The conversion loss, C_L, can be calculated from P_{load} and the power available to the RF signal source, P_{avs} as follows: $C_L = P_{avs}/P_{load}$. Substituting $P_{avs} = {I_{RF}}^2 R_S/4$, the conversion loss from RF to IF can be written as:

$$C_L(IF) = \frac{{I_{RF}}^2 \times R_S \times R_L}{4 \times V_{out}^2(IF)}. \quad (13)$$

In addition to allowing one to estimate conversion loss, the diode waveforms in Figure 16 give the designer a feel for certain diode parameters that are important in attaining good mixer performance. The 'ON' time of the diode, defined here to be the amount of the LO period that the diode conducts 1μA or more, the maximum and minimum excursions of the diode voltage and current can be found from the graphs.

'ON' time is represented by two numbers. The first, T_{NL}, is the fraction of the LO period that the diode spends in the highly nonlinear portion of the current-voltage curve. The second number, T_{TON}, represents the total amount of the LO period that the diode is turned 'ON'. For example, diode DM_1 is said to be 'ON' when the diode's current is 1μA or greater. When it is 'ON', it may be in the nonlinear region if I_d is between $\{1\mu$A, 0.5mA$\}$ or it may be in the linear region if I_d is greater than 0.5mA. The I-V curves for diodes DM_1, DM_2, and DM_3 are shown in Figure 17. The I-V curves are plotted according to the following equation given the diode parameter value listed in Table 2:

$$V_d = I_s(e^{\frac{-qV_j}{nkT}} - 1) \cdot r_{ser} + V_j \quad (14)$$

Fig. 17(a) depicts more of the 'ON' region, specifically the nonlinear region, of the I-V curves and Fig. 17(b) depicts both the 'ON' and 'OFF' regions of the I-V curves.

The optimum value of parameters similar to T_{NL} and T_{TON} have been discussed in the literature. Saleh and Barber refer to the optimum setting of the diode pulse

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duty ratio, similar to T_{TON}/T_{LO}, for specific mixer circuits [55,6]. Barber analyzes 'Y' mixers only with several image terminations (open, short, and equal to RF termination); he uses Torrey and Whitmer's formulation of conversion loss in terms of the Fourier components of the diode conductance to find the optimum diode pulse duty ratio for minimum conversion loss. Barber concludes that the optimum duty ratio for the 'Y' mixer is less than 10%. Saleh analyzes four mixer circuits and find the optimum diode conductance function for them. His results concur with Barber's for the 'Y' mixer case. In Section 4.2.2 several of these mixer circuits are analyzed with our design tool and the results compared with Saleh and Barber's.

$I_{d_{max}}$ and $V_{d_{max}}$ can be used to determine the level of bias voltage or LO drive required to achieve low conversion loss without excess power consumption. The higher the current in the diode the greater the power lost and noise generated in the spreading resistance. $I_{d_{min}}$ and $V_{d_{min}}$ become interesting when the barrier capacitance is introduced in the diode model. Their role in circuit optimization will become clear in Section 4.3.

The diode and mixer characteristics for the resistively matched mixer shown in Figure 14 are found from these graphical programs and shown below:

$$\text{'ON' Time: } \{T_{NL}, T_{TON}\} = \{0.055\,T_{LO},\ 0.45\,T_{LO}\}$$
$$\{V_{d_{max}},\ V_{d_{min}}\} = \{0.72V,\ -4.34V\}$$
$$\{I_{d_{max}},\ I_{d_{min}}\} = \{3.6mA,\ -24nA\}.$$

Using eqns. 9 and 10 we find:

$$\langle I_d(T_1)\rangle = 1.06mA \text{ and } \langle I_d(T_3)\rangle = 0.82mA.$$

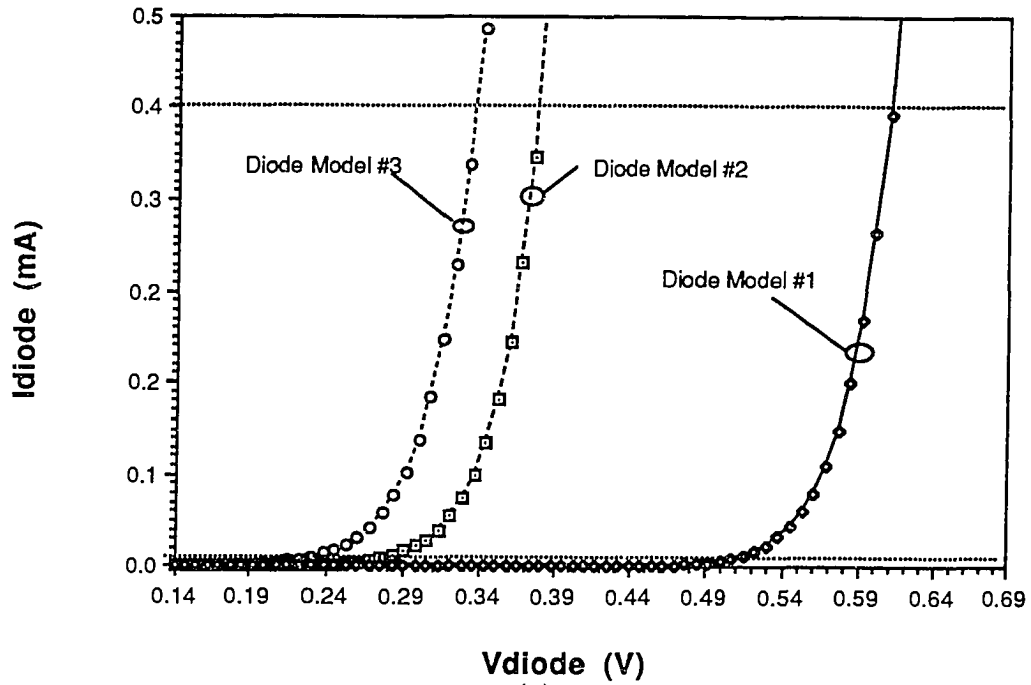
Using $I_{RF} = 0.4mA$ and $R_S = R_L = 1K$ in eqns. 11 and 12, we calculate:

$$V_{out}(DC) = 0.96V \text{ and } V_{out}(IF)_{0-to-peak} = 0.123V.$$

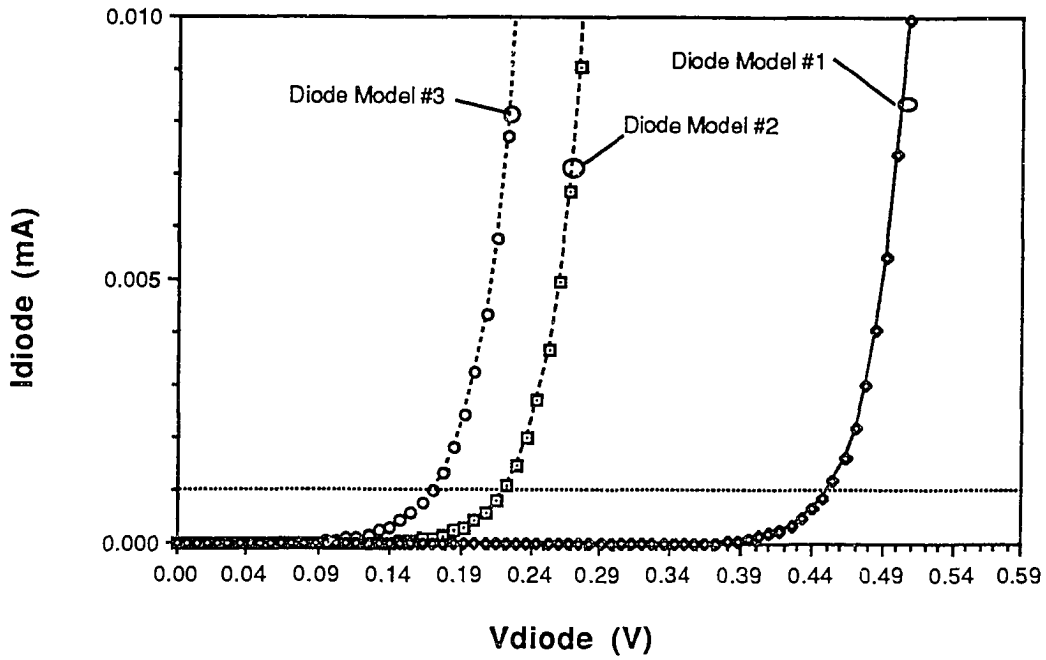
From eqn. 13, the conversion loss is found to be $C_L = 4.22dB$.

These graphically obtained results can be compared with those quantitatively obtained which are listed in Table 1.

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(a)



(b)

Figure 17: Diode I-V curves for DM_1, DM_2 and DM_3: (a) detailing nonlinear region of operation, $1\mu A \leq I_d \leq 0.5mA$; (b) detailing 'OFF' region of operation, $I_d < 1\mu A$.

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The small signal conductance and capacitance waveforms, $g(t)$ and $C_B(t)$, are also plotted when required. They will be discussed in Section 4.2.

By mathematically manipulating the data plotted in Figure 16 the RF current can be examined and the RF component in the diode, R_S, and, L_S studied — $I_{RF} = I_d|_{RF} + I_{R_S}|_{RF} + I_{L_S}|_{RF}$. To minimize conversion loss, all of I_{RF} should flow through the diode to the load hence maximizing $\langle I_d(T_1)\rangle$. The flow of RF current can be examined with the aid of Figure 18. Figure 18(a) shows the results of subtracting the 180° out-of-phase currents from the in-phase currents in the diode, R_S and L_S to obtain only the RF component; these "large-signal" currents are shown in Figure 16. Figure 18(b) shows the results of subtracting the 270° out-of-phase currents from the 90° out-of-phase current in the diode, R_S and L_S to, again, obtain only the RF component. Thus I_{LO} and I_{RF} are in-phase in Fig. 18(a) and 180° out-of-phase in (b). The plots show the RF current and two of its three components. $I_d|_{RF}$ and $I_{R_S}|_{RF}$ are shown; $I_{L_S}|_{RF}$ is left out for clarity. $I_d|_{RF}$ is highlighted by a thicker line and the area under it is shaded. The average current in the diode due to the RF, $\langle I_d|_{RF}\rangle$, is clearly maximized when the LO and RF are in-phase and close to zero when they are 90° out-of-phase. $\langle I_d(T_1)|_{RF}\rangle$ can be expressed as $(\langle I_d(T_1)\rangle - \langle I_d(T_3)\rangle)/2$. From the graph $\langle I_d(T_1)|_{RF}\rangle$ can be found to be 123 μA and $\langle I_d(T_3)|_{RF}\rangle$ is -5 μA. The value of $\langle I_d(T_1)|_{RF}\rangle$ can be used as another means to graphically calculate $V_{out}(IF)_{0-to-peak}$ and C_L with the aid of eqns. 12 and 13. Lastly, Fig. 18 can be used to examine the amount of RF current that is supplied to the diode's non-linear barrier resistor and the amount that is lost to the mixing process through R_S.

3.3.4 Quantitative Assessment of Mixer Performance

The calculation of the spectrum of various waveforms is necessary to evaluate the mixer and to understand how to optimize its performance. The spectum of $V_{out}(t)$, $V_{out}(f)$ is used to quantize the RF energy lost in conversion to sideband frequencies other than f_{IF}, and, to find the amplitude and phase of the output voltage at f_{IF} for a more precise determination of conversion loss. The Fourier coefficient at f_{RF} of the voltage and current at the RF port are used in find the input impedance at f_{RF}. The

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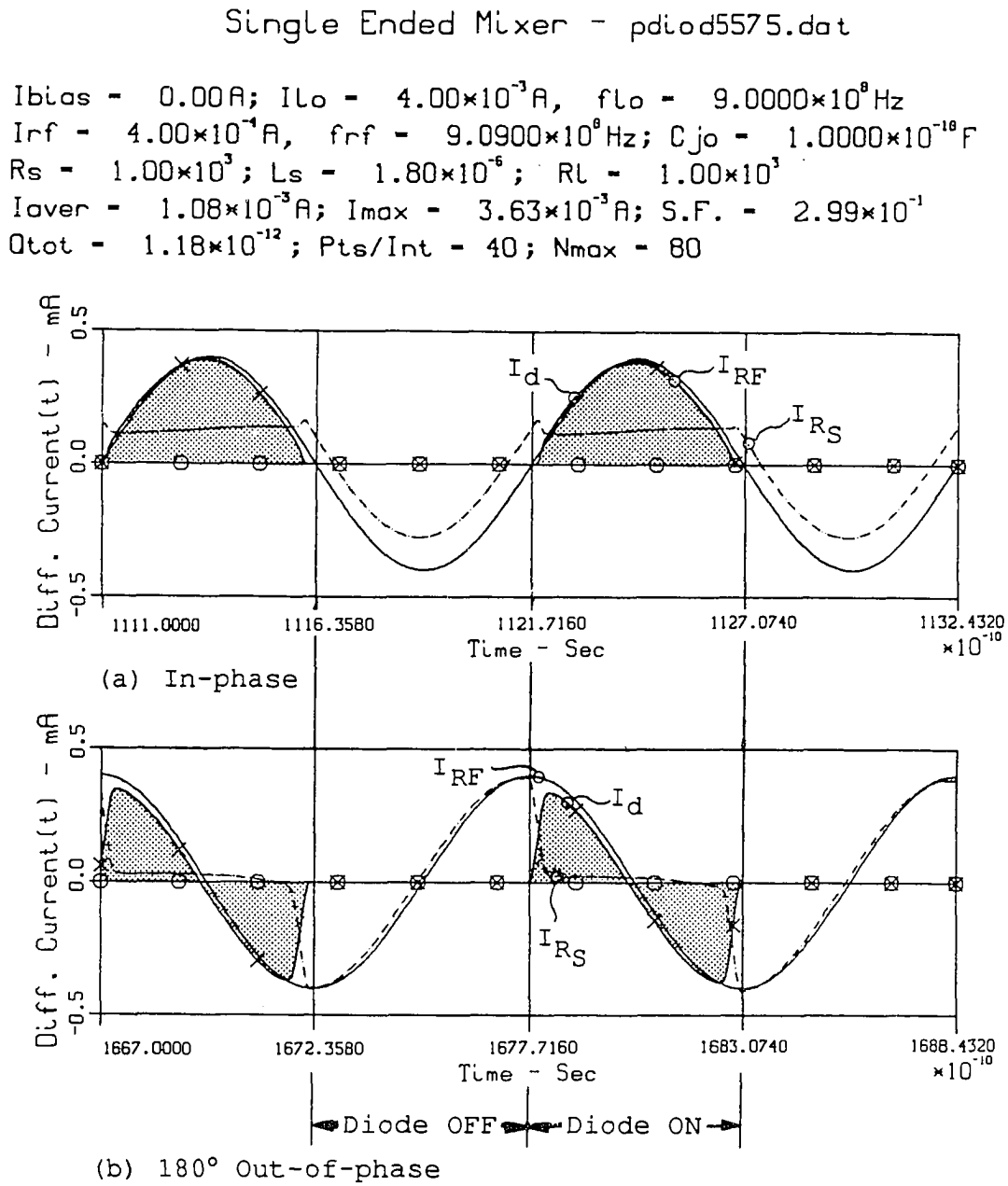


Figure 18: RF current in the diode, R_S and L_S.

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program also finds the Fourier coefficients of the diode voltage and current as well as other spectra for comparison with the frequency domain approach. All spectra are found with the use of the Fast Hartley Transform (FHT) algorithm rather than with the SPICE Fourier analysis program. The latter computes only the first nine harmonics of a specified fundamental frequency. Consequently the ratio of RF to IF frequencies and their ranges are narrowly specified, and the types of mixers and mixer circuits that can be simulated are quite limited. In general, SPICE Fourier analysis is inadequate for use with circuits, such as mixers, that possess a wide frequency response.

The Hartley transform can be used to obtain the Fourier transform of real waveforms [11]. The FHT generates the Discrete Fourier Transform (DFT) of a sequence of real numbers faster than the Fast Fourier Transform (FFT) [12,34].

The Discrete Hartley Transform (DHT), $\mathcal{H}(\nu)$, is defined as follows:

$$\mathcal{H}(\nu) = \frac{1}{N}\sum_{\tau=0}^{N-1} f(\tau)(\cos\frac{2\pi\nu\tau}{N} + \sin\frac{2\pi\nu\tau}{N}) \quad for\ \nu = 0, 1, \cdots, N-1.$$

For our purposes τ represents Δt and ν symbolizes Δf.

The DFT of a discrete real function $f(\tau)$ can be easily expressed in terms of its DHT. To see this, the definition of the DFT of $f(\tau)$, $\mathcal{F}(\nu)$, is shown below and the DHT is rewritten for comparison:

$$\mathcal{F}(\nu) = \frac{1}{N}\sum_{\tau=0}^{N-1} f(\tau)\exp(\frac{-2\pi\nu\tau}{N}) \quad for\ \nu = 0, 1, \cdots, N-1.$$

$$\mathcal{H}(\nu) = \frac{1}{N}\sum_{\tau=0}^{N-1} f(\tau)\cos\frac{2\pi\nu\tau}{N} + \frac{1}{N}\sum_{\tau=0}^{N-1} f(\tau)\sin\frac{2\pi\nu\tau}{N} \quad for\ \nu = 0, 1, \cdots, N-1.$$

Two points are immediately apparent: (1) because $f(\tau)$ is real, the first term of $\mathcal{H}(\nu)$ represents its even part and the second its odd part, defined as:

$$\mathcal{E}_{\mathcal{H}}(\nu) = \frac{\mathcal{H}(\nu) + \mathcal{H}(-\nu)}{2} = \frac{1}{N}\sum_{\tau=0}^{N-1} f(\tau)\cos\frac{2\pi\nu\tau}{N} \quad for\ \nu = 0, 1, \cdots, N-1$$

and

$$\mathcal{O}_{\mathcal{H}}(\nu) = \frac{\mathcal{H}(\nu) - \mathcal{H}(-\nu)}{2} = \frac{1}{N}\sum_{\tau=0}^{N-1} f(\tau)\sin\frac{2\pi\nu\tau}{N} \quad for\ \nu = 0, 1, \cdots, N-1$$

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(2) the DFT is easily expressed in terms of $\mathcal{E}_{\mathcal{H}}(\nu)$ and $\mathcal{O}_{\mathcal{H}}(\nu)$,

$$\mathcal{F}(\nu) = \mathcal{E}_{\mathcal{H}}(\nu) - j\mathcal{O}_{\mathcal{H}}(\nu)$$

To summarize, given N samples of a waveform $f(\tau)$ taken every Δt sec, the FHT returns N values of $\mathcal{H}(\nu)$ spaced by Δf Hz. After decomposing $\mathcal{H}(\nu)$ into its even and odd parts, one arrives at the real and imaginary parts of the Fourier transform of $f(\tau)$.

Figure 19 shows the spectrum of the output voltage for the resistively matched mixer circuit. The rich harmonic output of the mixer is clearly visible as is the leakage of LO and RF sources to the output. The sideband frequencies, as defined on page 30, are labelled according to the subscript n, where $f_n = \mid f_{IF} + nf_{LO} \mid$ [55]. From the FHT calculation, V_{out} at DC and f_{IF} are found to be:

$$V_{out}(DC) = 0.94V$$
$$V_{out}(IF) = V_{out}(f_{IF}) + V_{out}(-f_{IF}) = 0.121V$$

Using Eqn. 13 the accurate conversion loss is found to be 4.33dB. The graphically calculated values are within 5% and 1% of the values computed by the FHT for $V_{out}(DC)$ and $V_{out}(IF)$, respectively.

Although the mixer is a nonlinear circuit for which impedances are not defined, the linear circuit definition for input impedance can be used at frequencies whose power levels are far below that of the driving LO signal as, for example, the sideband frequencies. Signals at these frequencies can be thought of as obeying the circuit equations for a small signal linearized model of the mixer. The FHT of the input voltage and current, as defined in Figure 14, are performed in order to calculate the input impedance at a specific bias and drive condition. The small-signal impedance is then found as:

$$Z_{in}(f) = \frac{\mathcal{F}(V_{in})\mid_f}{\mathcal{F}(Iin)\mid_f}. \tag{15}$$

Knowledge of the input impedance is useful in matching the RF source to the diode. $Z_{in}(f)$ can be controlled, to a certain extent, by the LO drive. For this circuit, $Z_{in}(f_{RF}) = 1.28K\angle -4°$.

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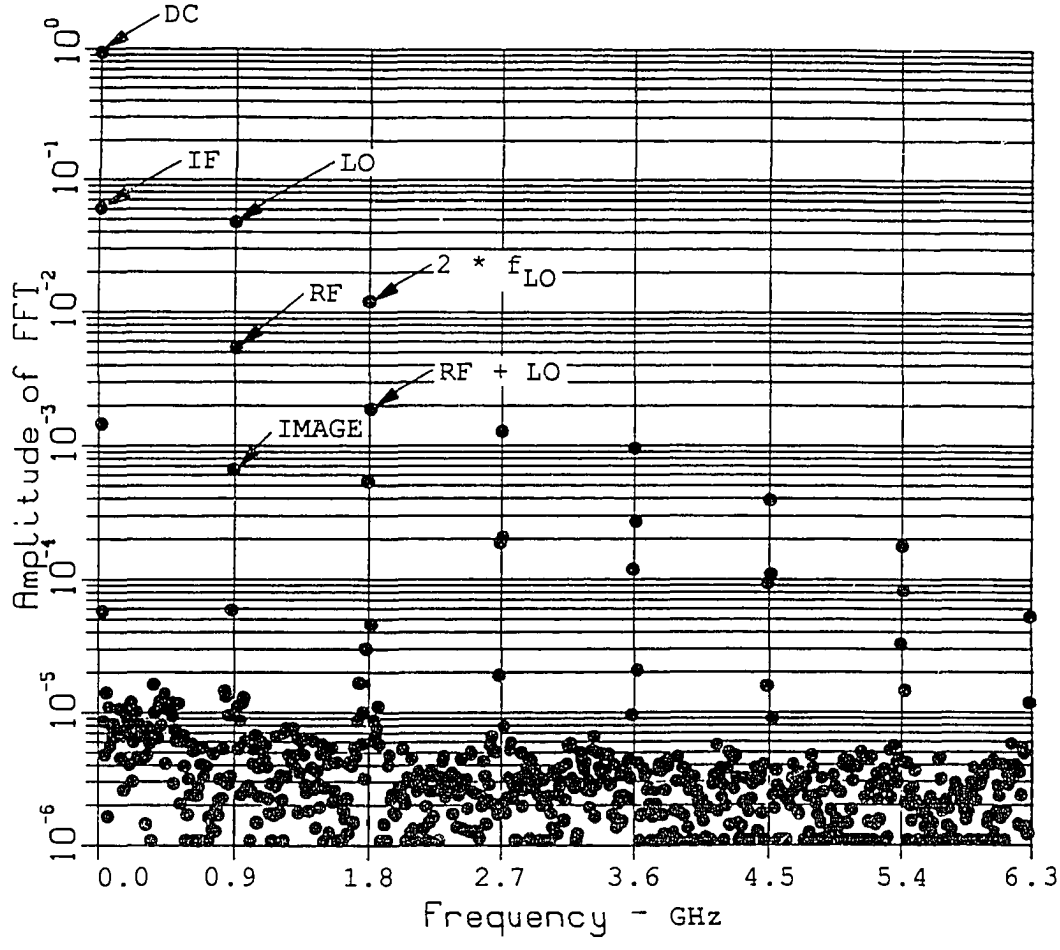


Figure 19: Spectrum of V_{out} - *Resistively Matched* mixer.

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The output impedance of the circuit can be calculated from two SPICE runs which are identical except for the value of the load. This, too, is valid only at frequencies where the nonlinear mixer circuit can be thought of as a linear network. This definition rests on making a Thevenin equivalent circuit for the mixer and is therefore specific to a given bias and drive level. The procedure is outlined in Figure 20.

For a given load impedance, Z_{L_1}, the output voltage at a small signal frequency is found, $V_{out_1}(f)$. The mixer is modelled as a Thevenin voltage source, $V_{thev}(f)$, with a source impedance, $Z_{out}(f)$. The output voltage under this load condition is denoted as $V_{out_1}(f)$. It is written as follows,

$$V_{out_1}(f) = V_{thev}(f) \frac{Z_{L_1}(f)}{Z_{L_1}(f) + Z_{thev}}$$

where $V_{out_1}(f)$ is a complex variable.

The mixer is analyzed under a second load, Z_{L_2}, and its output voltage, $V_{out_2}(f)$, is found. The same Thevenin model for the mixer is assumed to hold for the following equation to correctly predict Z_{out}. The Thevenin equivalent impedance is given below:

$$Z_{thev}(f) = \frac{Z_{L_2}(f) \times Z_{L_1}(f) \times (V_{out_1}(f) - V_{out_2}(f))}{V_{out_2}(f) \times Z_{L_1}(f) - V_{out_1}(f) \times Z_{L_2}(f)} \quad (16)$$

In choosing Z_{L_1} and Z_{L_2}, attention must be paid not to change the bias point of the diode dramatically or the assumptions of the derivation will not hold. The calculation of output impedance, although approximate, is useful in selecting the optimum load for minimization of conversion loss. For the resistively matched mixer shown in Figure 14, varying R_L from 1K to 2K, $Z_{out}(f_{IF}) = 1.1K\angle -8°$.

Both input and output impedance techniques have been tested on linear circuit simulations and found to correctly predict input and output circuit impedances.

In a typical run the spectrum of the voltage and current in the diode are also found; the DC values of V_d and I_d are useful in setting the correct bias and drive condition for a given mixer circuit and for comparison between circuits. The average power in the diode, $P_{av}(f)$, is computed according to the following relation [14]:

$$P_{av}(f) = 1/2\,|V_d(f)|\;\;|I_d(f)|\,\cos(\angle V_d(f) - \angle I_d(f)) \quad (17)$$

and examined to look at energy conversion into the sideband frequencies.

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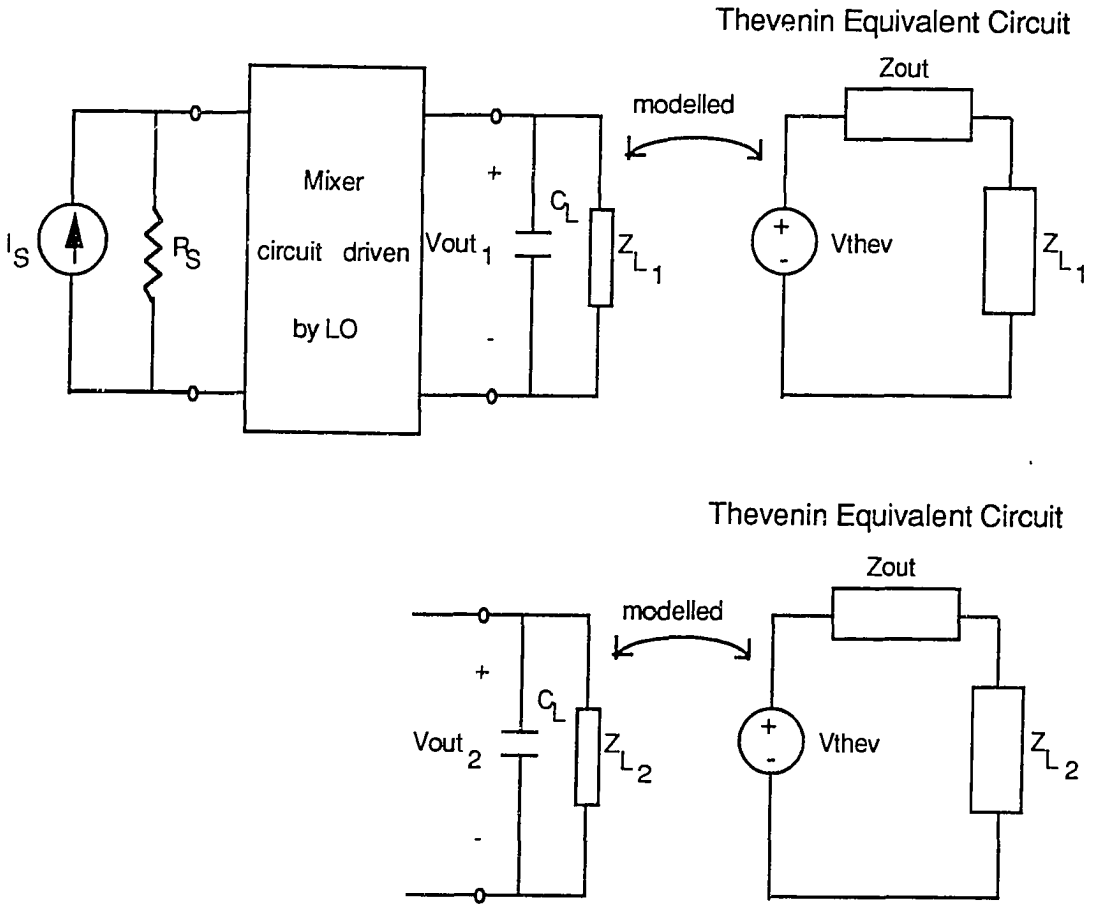


Figure 20: Calculation of $Z_{out}(f)$.

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3.3.5 Optimization Criteria

There are many types of mixer circuits to choose from for any given mixer application. In the following section we shall attempt to classify the performance of some classical mixer circuits for the case of a purely resistive diode mixer. Once a circuit has been chosen, our design tool can be used to optimize its performance by iterating upon the following steps.

First the bias and drive levels are varied to set the optimum diode 'ON' time for the given circuit type. This should be done so as to minimize power consumption. In general the use of a small bias current, enough to bias the diode on the edge of turning on, will reduce the level of LO drive necessary to achieve a minimum C_L. The effect of I_{bias} on mixer noise temperature is unclear: although it increases mixer noise by creating shot and thermal noise in the spreading resistance this may be offset by the decrease in LO generated noise.

Then the load and source impedances are adjusted to achieve desired match and minimize C_L. Mixers, like other RF components, are typically specified to work into prescribed source and load impedances. One design objective is then to ensure that optimum component performance is achieved when these matches are used to load the circuit. Mixer theory has shown that to achieve the lowest conversion loss the load at the IF port should be set to the complex conjugate of the mixer's output impedance but that the same is not true for the source impedance [28,24]. This has been corroborated by our program.

The load impedance can usually be set to the desired out impedance and then varied to find $Z_{out}(f_{IF})$. The load impedance necessary to minimize C_L is equal to $Z^*_{out}(f_{IF})$.[5] The starting source impedance should be set to R_L if a resistive mixer is being run or to the desired source impedance if a mixer diode with non-zero capacitance is being used. Once the first mixer run is performed $Z_{in}(f_{RF})$ can be determined. Z_S can then be set to $Z^*_{in}(f_{RF})$, the mixer circuit rerun and $Z_{out}(f_{RF})$ redetermined.

Minimum conversion loss can be found by iteratively searching for the optimum source impedance while varying the bias and LO source levels to keep T_{ON} at its

[5]The asterisk denotes complex conjugate.

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optimum value and maintaining $Z_L = Z^*_{out}(f_{IF})$. If the required Z_S and Z_L for minimum C_L, $Z_{S_{opt}}$ and $Z_{L_{opt}}$ are then too far from the desired load impedance, one may be able to change I_{bias} and I_{LO} to shift $Z_{S_{opt}}$ and $Z_{L_{opt}}$ closer to their desired driving impedances. In this way one trades off power consumption for conversion loss. If this is not possible, one must trade C_L performance to obtain the necessary matches.

For a purely resistive diode mixer, $Z_{in}(f_{RF})$ and $Z_{out}(f_{IF})$ are mostly resistive and optimum ratios of R_S/R_L exists to achieve $C_{L_{min}}$. It is then relatively easy to optimize C_L performance and meet specifications for input and output load impedances. Once barrier capacitance is introduced in the diode model, Z_{in} is no longer mostly resistive and the iterative process to establish the appropriate matching circuit becomes more complex. The benefits of using graphical output to trace energy flow in the circuit, or, the currents and voltages in the matching structure grow.

This process is detailed in Figure 3. Following these guidelines the performance of the resistively matched mixer can be optimized when different diodes are used. The mixer circuit shown in Figure 14 was optimized for operation with the purely resistive version of diode DM_2.[6] The results are listed in Table 4. Conversion loss of 4.29 dB was realized using DM_2. The main difference in run parameters is the drive level required to set the diode 'ON' time to 0.50 T_{LO}.

The simple resistively matched mixer of Figure 14(a) works quite well: its conversion loss is about 4.3dB for both models used. It has a broadband input match, meaning that the source impedance presented at f_{RF} is identical to that presented at the image frequency. Kelly found that the conversion loss limit for a resistively matched, broadband input, mixer to be 3.92dB for a purely resistive diode mixer [36]. When the higher sidebands are terminated reactively, the conversion loss limit is 3.0dB for a broadband input circuit and 0dB for a circuit that open or short circuits the image frequency. Our circuit, optimized with the above technique, is within 0.4dB of optimum for a resistively matched mixer.

[6]The parameters for DM_2 and DM_3 were taken from Table 2 except C_B which was set to zero.

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Table 3: Iterative Optimization Procedure.

1. Choice of Bias and LO Drive. Set T_{TON} and T_{NL} to their appropriate values for the given mixer circuit type while keeping $I_{d_{max}}$ and $V_{d_{max}}$ within reasonable limits to ensure low power consumption.

   Note. If the diode possesses non-zero C_B, $V_{d_{min}}$ must be greater than -2.0V to produce a highly nonlinear variation in capacitance during one LO cycle.

2. Graphic Check.The graphic output is used to check diode condition and waveforms.

3. Choice of Z_L. Calculate $Z_{out}(f_{IF})$ by comparing V_{out} under two different load conditions. $Z_{L_{opt}}$ is equal to $Z^*_{out}(f_{IF})$. Modify Z_S, I_{bias}, and, I_{LO} if Z_L is outside the desired range of output impedance.

4. Choice of Z_S. Although the optimum Z_S for minimum C_L is not equal to $Z^*_{in}(f_{RF})$, setting $Z_S = Z^*_{in}(f_{RF})$ is a good initial value from which to begin searching for $Z_{S_{opt}}$.

   Note. For purely resistive mixer circuits $Z_{L_{opt}} \simeq R_{Lopt}$, $Z_{S_{opt}} \simeq R_{S_{opt}}$, and, an optimum R_S/R_L exists to achieve $C_{L_{min}}$. Therefore the values of $R_{L_{opt}}$ and $R_{S_{opt}}$ can be chosen to meet imposed design criteria as well as to optimize C_L.

5. Graphic Check.The graphic output is checked to optimize RF energy transfer between the matching elements and diode, and, to set the timing of this transfer correctly with respect to the diode's large signal voltage.

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Table 4: Comparison of Purely Resistive Mixer Circuit with Two Types of Diodes

	DM_1	DM_2
Run	pdiod5575	cdiod181
Circuit Characteristics:		
I_{bias}	0.0 mA	0.0 mA
I_{LO}	4.0 mA	3.0 mA
I_{RF}	0.4 mA	0.3 mA
R_S, R_L	1K, 1K	1K, 1K
Diode Condition:		
$\frac{T_{TON}}{T_{LO}}$	0.45	0.47
$V_{d_{max}}$, $V_{d_{min}}$	0.72V, -4.34V	0.46V, -3.28V
$I_{d_{max}}$, $I_{d_{min}}$	3.6mA, -24nA	2.8mA, -19nA
Circuit Performance:		
$Z_{in}(f_{RF})$	1.28K $\angle -3°$	1.23K $\angle -4°$
C_L	4.33dB	4.29dB

3.4 Conclusion

This chapter describes a computer-aided design tool which has been developed to analyze and optimize the design of practical mixer circuits. The design tool is based on a time domain approach and thus differs from the currently used frequency domain mixer analysis programs. It uses SPICE [72], a circuit simulator program, to arrive at the steady state solution to the network equation. To quantify conversion loss performance and generate small-signal impedances, the Fourier transforms of various voltages and currents are evaluated in a separate program. Rapid calculation of these transforms is made possible through the use of the Hartley transform [12]. Several graphics programs are used to plot the diode and mixer waveforms when the LO and RF are in-phase (T_1), 90° out-of-phase (T_2), and 180° out-of-phase (T_3). Diode characteristics such as the 'ON' time and average current delivered to the load during one LO cycle at T_1, T_2, and T_3 are tabulated. These diode characteristics are useful in assessing the performance of the circuit, in understanding the interaction of the

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diode with the mixer circuit, and in allowing graphical criteria to be established for circuit optimization.

The design tool is thus capable, in theory, of analyzing any mixer circuit whose structure can be specified by elements recognized by SPICE.[7] In practice, run time and convergence considerations limit the analyzed circuits to relatively simple structures. The technique is suited to the optimization of practical UHF circuits where the mixer circuits are composed of discrete elements and where the diode embedding circuit is broadband and frequency non-selective. Such mixers cannot use many of the theoretically reached circuit guidelines - derived principally for purely resistive diode mixers - because they specify that the diode embedding circuit present either short or open-circuits at all sideband frequencies $n \geq 2$. In contrast, mixers designed for operation at higher frequencies can more easily implement these ideal circuits to maximize mixer performance as waveguide structures and quarter-wavelength transmission lines permit the implementation of frequency specific matches. Because UHF mixers cannot take advantage of such matches to optimize performance, the mixer design tool was developed to enhance understanding of the interaction of circuit and diode by obtaining graphical and numerical circuit data and thereby to aid in the development of mixer circuit optimization guidelines.

The majority of other mixer analysis techniques have been based in the frequency domain. They require that the embedding impedances of the mixer circuit be entered into the program, along with the diode characteristics, at a limited set of frequencies spanning from f_{IF} - nf_{LO} to $f_{IF} + nf_{LO}$ where n is typically 4 or 5. These techniques are suited to the analysis of ideal circuits where the optimum match to be presented at each of these frequencies is known or to the evaluation of already designed circuits. Because it is difficult to develop circuit optimization guidelines with these techniques, they serve as better analysis than design tools.

The time domain mixer analysis and design tool presented here has been developed for three reasons: (1) to address problems specific to the design of UHF mixer

[7]While the SPICE used in these simulations, SPICE Version 2G-4, accepts only discrete components as elements, such as resistors, inductors, and capacitors, commercially available versions of SPICE and more recent versions of the public domain SPICE can analyze circuits with transmission lines, spiral inductors, etc.

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design, particularly of the direct conversion type; (2) to give mixer designers both time domain and frequency domain analysis of mixer operation; and (3) to provide new guidelines for mixer optimization.

Several mixer circuits are simulated to show the equivalence of correctly scaled mixer and diode circuits. For example, the direct conversion mixer can be modelled with a f_{RF} of 909 MHz and a f_{LO} of 900 MHz or it can be analyzed assuming a f_{RF} of 505 Hz and a f_{LO} of 500 Hz. As long as the diode elements are scaled according to the model used, identical mixer circuit performance will result. Three diode models for a medium barrier Si Schottky diode are given. The rationale for these models is discussed in Appendix A. Diode model DM_1 is selected as the basic diode for mixer simulations, diode models DM_2 and DM_3 being used occasionally to illustrate the generality of the guidelines.

A simple broadband mixer circuit is analyzed with the design tool and both quantitative and graphical methods are used to calculate its conversion loss. The diode used in this simulation is specified as possessing negligible barrier capacitance at f_{RF}, hence its performance is indicative of that of a purely resistive diode. Because the simulated mixer structure embeds the diode in a circuit that provides a resistive match at all frequencies, the mixer circuit is named a *'Resistively Matched'* or 'RM' circuit. The definition of diode 'ON' time, $Z_{in}(f)$ and $Z_{out}(f)$ are given; their values are calculated for the particular mixer simulated. Simple guidelines for optimization of the 'RM' mixer with a purely resistive diode are given. The conversion loss of the optimized mixer is 4.3 dB. Substitution of diode model DM_2 gives identical performance results after the circuit has been optimization for this diode according to the guidelines. Finally the conversion loss of the 'RM' mixer designed with practical elements using a reasonable diode model is contrasted with that theoretically predicted for a broadband mixer that resistively terminates all sideband frequencies [36] and shown to be 0.4 dB higher.

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Chapter 4

Mixer Design with Purely Resistive Diodes

4.1 Introduction

Chapter 4 concerns the application of the design tool to simple single-ended and single-balanced mixer design in order to gain familiarity with the design tool and to derive the criteria for optimum direct conversion mixer design. First a comparison of low conversion loss mixer designs for purely resistive diodes is performed. Then, the degradation in mixer performance is analyzed when nonlinear barrier capacitance is present, the sources discussed, and simple matching techniques derived and applied to practical mixer design. Finally results obtained using the design tool are compared to those predicted by conventional mixer design techniques.

Section 4.2 concentrates on single-ended mixer design. In it the behavior of an ideal switching mixer is examined in order to develop the analogies between a switching mixer and a purely resistive mixer and to derive theoretical circuit guidelines. These rules are used throughout the mixer study for both ideal resistive diodes and nonideal diodes with resistive and capacitive components. The performance of Saleh's 'Y' and 'Z' mixers circuits are calculated and compared against their ideal performance [55]. A *Resistively Matched* ('RM') circuit is developed and proposed as the starting point for single ended and balanced mixer design. Finally the performance

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of mixer circuits with capacitive diodes is discussed. In Section 4.3 design models for balanced mixers are given and their performance is analyzed for diodes with both resistive and capacitive elements. In Section 4.4 the design tool results are compared with those found by implementing the small-signal analysis developed by Held and Kerr [29] and by running Maas's program DIODEMX [43]. First the predicted performance of the optimized 'Y', 'Z', and 'RM' mixer circuits are compared. Next the effect on mixer circuits of increasing barrier capacitance with and without the addition of matching elements is examined. Finally the noise temperature of the 'RM' mixer for increasing barrier capacitance is given as calculated by DIODEMX. Section 4.5 summarizes the material covered in this chapter and presents our conclusions.

In Chapter 5 the design of low conversion loss mixer circuits with capacitive diodes is discussed. The technique developed relies on barrier capacitance to improve mixer performance though its use as an energy storage element and by parametrically pumping the barrier capacitance to increase the effectiveness of the mixer's frequency conversion process.

4.2 Single-Ended Mixer Design

This section is concerned with some fundamental aspects of mixer design: how to make a simple model of a mixer, how to choose a circuit to embed the diode in, and what differences exist in the performance of a mixer using a diode that possesses series and barrier resistance and one that additionally has barrier capacitance. The first subsection discusses the similarities between an ideal switching mixer and a diode mixer. Here a way of thinking about the mixer is proposed to aid the designer in optimizing mixer performance. This analogy can be used when resistive mixers[1] are analyzed or when a more complete diode model is used. The second subsection deals with the design issues of mixers with exponential diodes.[2] Although actual devices differ greatly from these idealized devices with negligible spreading resistance and

[1] A resistive diode does not have any barrier capacitance. Its current, I_d, and voltage, V_d, can be expressed by $I_d(t) = I_S\,(\exp(\frac{qV_j}{nkT}) - 1)$ and $V_d = V_j + I_d \cdot r_{ser}$.

[2] An exponential diode is a resistive diode that has no series resistance and whose ideality factor, n, is 1.0. Its I-V curve is described by $I_S\,(\exp(\frac{qV_d}{kT}) - 1)$ where $V_d = V_j$.

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barrier capacitance, no circuit guidelines have been derived for these complex devices. Circuits using them have been found to be very difficult to analyze mathematically; it has been impossible to obtain a closed form solution for the network equations. In order to reduce the complexity of the problem and arrive at guidelines for mixer circuits, exponential devices must be assumed. Saleh categorized those mixer circuits that terminate all out-of-band frequencies with a short or an open circuit, and, has found their performance when realized with an exponential diode.

As a starting point in the design of a mixer circuit for the direct conversion receiver design we construct prototypes of two of Saleh's circuits and analyze them with our design tool. This serves as a test of our technique and gives a feel for the difference between the predicted performance of an ideal circuit and the simulated performance of the same circuit when implemented in a practical fashion. Selecting Saleh's 'Y' and 'Z' mixer circuits because their conversion loss performance sets the upper and lower bound for the set of reactively matched circuits, we compare their performance with that of the resistively matched circuit discussed in Section 3.3.

Lastly, we examine the effect of barrier capacitance, C_B, on mixer performance and discuss the use of inductively matching to C_B to minimize the degradation of performance.

4.2.1 The Mixer Viewed as a Switch

One of the easiest ways to think of a mixer is as a multiplier in which the RF signal, $A\ \cos(\omega_{RF}t)$, is multiplied with the LO signal, $\cos(\omega_{LO}t)$, to produce $A/2\ cos(\omega_{diff}t)$ and $A/2\ \cos(\omega_{sum}t)$, the difference and sum frequencies only. A multiplier is difficult to implement at microwave frequencies; however, a switch, which is a square wave multiplier of sorts, can be realized at these frequencies using a diode as the switching element. Examination of the behavior of the switch as a mixer provides a useful analogy for the operation of a practical mixer.

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Mixer Circuit Realized with a Switch

Here we examine the performance of a switch; we develop a measure for conversion loss in terms of the RF current that arrives at the load during the LO cycle in which the RF and LO are in phase; and we predict switch performance for various source and load resistances and switch duty cycles. Figure 21(a) shows a simple switch: the RF source with source resistance, R_S, is connected to a load resistor, R_L, through a switch. The switch is driven between zero and infinite resistance by a periodically varying waveform at the LO frequency. Thinking of the switch as a multiplier, the input waveform is multiplied by (+1,0) as the switch flips from closed to open. The LO and RF waveforms are shown in Fig. 21(b) along with the output waveform, $I_L(t)$, and its averaged value, $\langle I_L(t) \rangle$. As can be seen in the figure, $\langle I_L(t) \rangle$ contains a large frequency component at the difference or IF frequency. Intuitively it seems clear that to maximize the output $\langle I_L(t) \rangle$, the switch should be closed 50% of the LO cycle and that the choice of R_S is arbitrary but that $R_L = R_S$. We can examine this supposition by modelling the circuit mathematically.

Given the duty cycle of the switch, or per cent 'ON' time of the diode, a threshold voltage, V_{ON}, can be established at which the LO voltage, V_{LO}, turns the switch 'ON':

$$V_{ON} = \cos\left(\frac{T_{ON}}{T_{LO}} \times 180°\right) \tag{18}$$

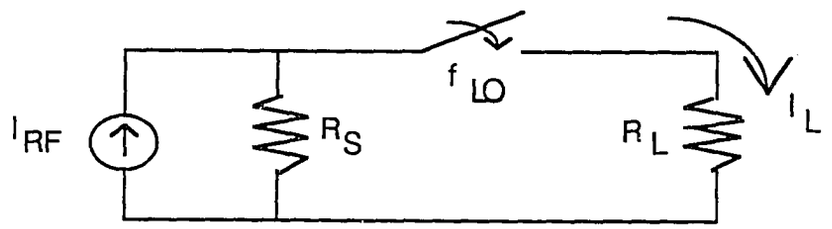
The current in the load can, then, be written as:

$$I_L(t) = I_S(t) \times \frac{R_S}{R_S + R_L}$$

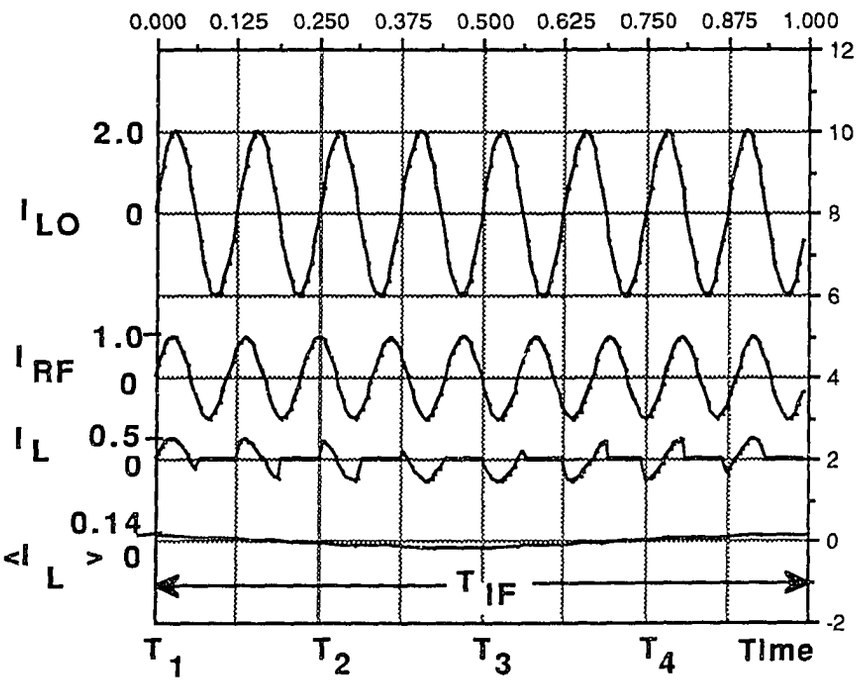
$$I_L(t) = \begin{cases} I_{RF} \sin(\omega_{RF} t) \frac{R_S}{R_S + R_L} & V_{LO} \geq V_{ON} \\ 0 & V_{LO} < V_{ON} \end{cases} \tag{19}$$

Conversion loss can be found with the aid of Figure 21(b). Examining the variations in $I_L(t)$ over one IF cycle we see that the portion of the RF waveform that appears at the output varies as the RF moves through various phase relationships with the LO. Averaging $I_L(t)$ over one LO cycle produces $\langle I_L(t) \rangle$. When the RF and LO are in phase with respect to each other, at time T_1, the RF is positive during

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(a)



(b)

Figure 21: Mixer modelled as a simple switch: (a) circuit diagram; (b) waveforms.

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the entire time the switch is closed. This results in the largest value for $\langle I_L(t) \rangle$. Conversely when the RF and LO are 180° out-of-phase, at time T_3, $\langle I_L \rangle$ acquires its most negative value, equal and opposite to $\langle I_L(T_1) \rangle$. Clearly, the 0-to-peak output voltage at the IF frequency can be written in terms of the average current at T_1:

$$\langle I_L(T_1) \rangle = \frac{1}{T_{LO}} \int_{T_1}^{T_1+T_{LO}} I_L(t) dt$$

$$V_{out}(IF) = \langle I_L(T_1) \rangle \times R_L \tag{20}$$

This argument follows the same lines as that used in Section 3.3.3 to calculate the conversion loss of a mixer from the average value of the diode current when the RF and LO are in and 180° out-of-phase. The conversion loss can be written according to eqn. 13:

$$C_L(IF) = \frac{{I_{RF}}^2 \times R_S \times R_L}{4 \times V_{out}^2(IF)}$$

To minimize C_L we need to maximize $V_{out}(IF)$ or $\langle I_L(T_1) \rangle$. As can be seen in Fig. 21(b), $\langle I_L(T_1) \rangle$ can be maximized by setting the 'ON' time of the switch at $T_{LO}/2$. Then $V_{on} = 0.0$V, and, $I_L(t)$ is non-zero for t between $(0, T_{LO}/2)$. $V_{out}(IF)$ can then be calculated from eqns. 18, 19 and 20:

$$V_{out}(IF) = \frac{1}{T_{LO}} \times \int_0^{T_{LO}/2} I_{RF} \sin(\omega_{RF} t)\, dt \times \frac{R_S R_L}{R_S + R_L}$$

When f_{LO} and f_{RF} are very close to each other (or, $T_{LO} \approx T_{RF}$), as is often true in many microwave mixers applications, one can easily find the optimum 'ON' time and the best value for R_S and R_L for minimum conversion loss:

$$V_{out}(IF) \simeq I_{RF} \times \frac{1}{\pi} \times \frac{R_S R_L}{R_S + R_L}$$

and,

$$C_L(IF) = \frac{\pi^2}{4} \times \frac{(R_S + R_L)^2}{R_S\, R_L} \tag{21}$$

Conversion loss can be maximized by setting $R_S = R_L$ at which point $C_L(IF)$ is independent of R_S:

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$$C_L(IF) = \pi^2 \text{ or } 9.94dB \text{ for } R_S = R_L$$

To investigate the increase in conversion loss when $R_S \neq R_L$, conversion loss is calculated for $\frac{R_S}{R_L} = k$ and $\frac{R_S}{R_L} = \frac{1}{k}$. They are identical:

$$C_L(IF) = \frac{\pi^2}{4}\frac{k+1^2}{k} \text{ for } \frac{R_S}{R_L} = k \text{ or } \frac{R_S}{R_L} = \frac{1}{k} \quad (22)$$

For $R_S/R_L = 1/2$ or 2, $C_L = 10.45dB$ and for $R_S/R_L = 1/5$ or 5, $C_L = 12.50dB$.

The extent to which these conclusions hold when f_{RF} and f_{LO} are not identical can be gauged by submitting the problem to computer evaluation. The load current given by eqn. 19 can be sampled over one IF period and its spectrum calculated using an FFT. Conversion loss can be expressed at any frequency, f, as:

$$C_{L_{SWITCH}}(f) = \frac{I_{RF}^2 \times R_S/4}{I_L^2(f) \times R_L} \quad (23)$$

Using this equation the conversion loss at f_{IF} was calculated for a range of switch 'ON' times, T_{TON}, and various source and load impedances. The results are shown in Figure 22 for $f_{RF} = 909$ MHz and $f_{LO} = 900$ MHz. As predicted, the minimum C_L is achieved when $T_{TON} = 0.50\ T_{LO}$ and when $R_S = R_L$, where R_S is set to an arbitrary value. $C_{L_{min}}$ is calculated to be 9.94dB. $C_{L_{min}}$ is found to be 10.5dB when $R_S = 1/2 \times R_L$ or $2 \times R_L$ and $12.5dB$ when $R_S = 1/5 \times R_L$ or $5 \times R_L$. The values for this value of f_{RF} and f_{LO} are identical to those found assuming $f_{RF} = f_{LO}$.

Conversion loss at frequencies other than f_{IF} can be examined with eqn. 23. For the ideal switching mixer the following properties are observed:

1. $C_L(f_{sum}) = C_L(IF)$ $\quad \forall\ R_S, R_L, T_{TON}$
2. $V_{out}(DC) = 0$ for $T_{TON} = 0.50\,T_{LO}$ $\quad \forall\ R_S, R_L$
3. $V_{out}(IMAGE) = 0$ for $T_{TON} = 0.50\,T_{LO}$ $\quad \forall\ R_S, R_L$

They can be checked against the results for a mixer run.

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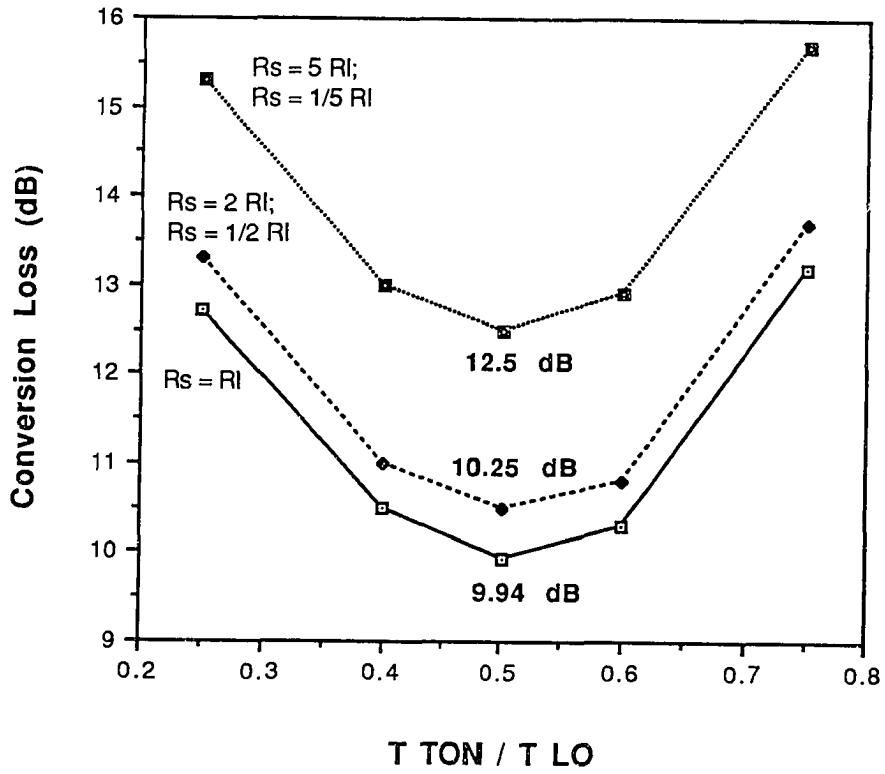


Figure 22: Conversion loss of an ideal switch.

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Mixer Circuit Realized with a Diode

Replacing the switch in Fig. 21(a) by diode DM_1, and adding a LO source to the circuit, the design tool can be run to compare the diode and switch circuit performance and conditions for optimum conversion loss. The results are remarkably similar. Figure 23 shows C_L plotted against LO current for three values of R_S: 50, $1K\Omega$, and $10K\Omega$. We look first at the results of R_S = 1K and 10K. The minimum C_L, which occurs for $R_L = R_S$, in both cases is identical, about 10.25dB, only 0.30dB higher than predicted for the ideal switch. When $R_L = 1/2 \times R_S$, with $R_S = 1K$ or $10K\Omega$, $C_{L_{min}} = 10.6dB$, the switch prediction for this case being 10.5dB. For $R_S = 1K$ and $R_L = 5K$, $C_{L_{min}}$ was found to be 12.6dB, again 0.1dB higher than the switch results.

We now examine the 'ON' time when $C_{L_{min}}$ occurs. 'ON' time, T_{TON}, is represented by T_{NL} and T_{TON}. The first number refers to the fraction of the LO cycle in which the diode is biased in the highly nonlinear portion of its I-V curve and the second is the total fraction of the LO cycle that the diode is turned ON, as defined in Section 3.3.3. Since there are no bias sources in the circuit and the LO source cannot immediately turn the diode on, the 'ON' time will always be less than 0.5 T_{LO}. T_{TON} increases with LO drive. At $C_{L_{min}}$ the 'ON' time is $(0, 0.43)\,T_{LO}$ for the $R_S = R_L = 10K$ case and $(0.09, 0.46)\,T_{LO}$ for the $R_S = R_L = 1K$ case, close to the ideal switch prediction of $0.50\,T_{LO}$. In all of these runs, the level of the output at DC, f_{sum} and f_{image} varied as predicted by the ideal switch.

The case of $R_S = 50\Omega$ differs from the previous two as the diode's spreading resistance, r_{ser}, now 1/5 of R_L, plays a role in setting the minimum C_L. The power dissipated through r_{ser} and the barrier resistance is comparable to the power dissipated in the load. Minimum conversion loss is now 10.9dB - 0.65dB higher than the previous minimum when $R_S = R_L = 1K$ or 10K. T_{ON} is $(0.02, 0.46)\,T_{LO}$. The increase in C_L is difficult to compensate. One might drive the diode harder the time average of the barrier resistance, thus increasing the power available for the conversion process. However, as the spreading resistance increases with LO drive degrading conversion loss, there may be little net improvement.

The effect of 'ON' time on conversion loss for the practical mixer can be examined

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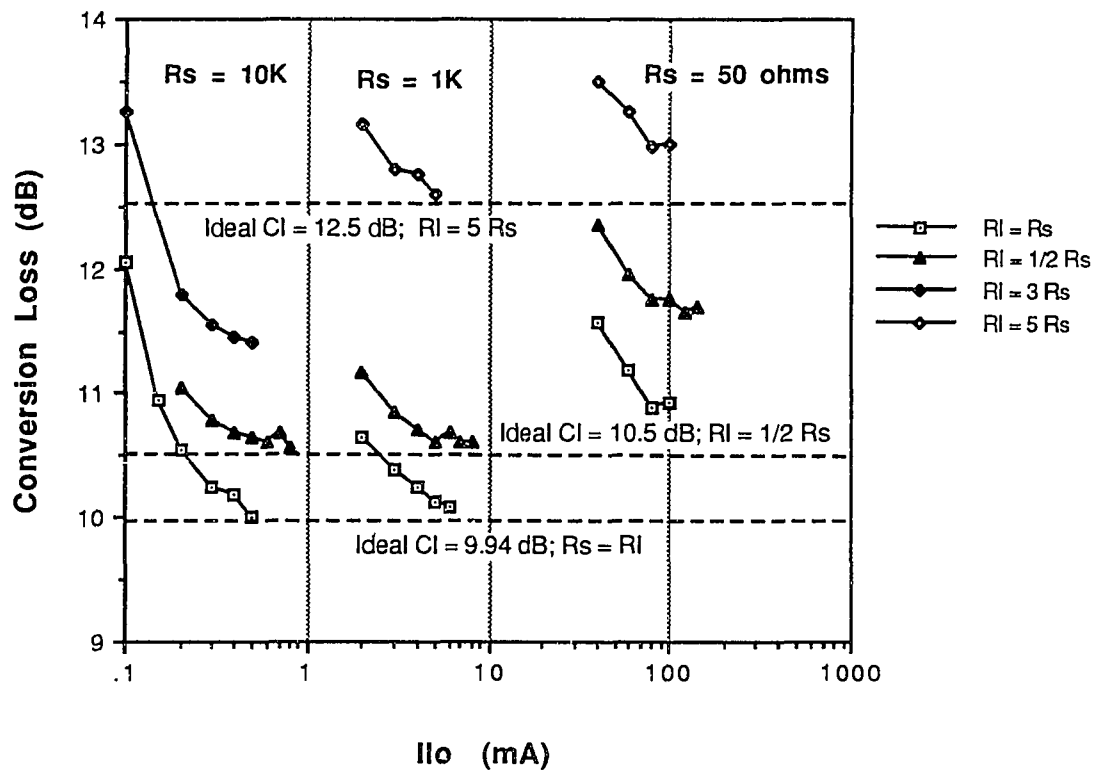


Figure 23: Conversion loss for several values of R_S and R_L.

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if a bias signal is added to the circuit. Without it, the diode will never be turned 'ON' for greater than 0.50 T_{LO}. Although in most practical circuits the bias current is fed to the diode through an RF choke, L_S, as shown in Figure 13, it is easier for SPICE to model the bias supply by placing a DC current source in parallel with the RF and LO sources as shown in Figure 14. A capacitor, C_S, is then placed in series with L_S. This has been specified in the following runs. Figure 24 shows the effect of bias current on conversion loss. For the three curves shown, Ibias is 0, 0.5mA and 1.5mA. The curve, $I_{bias} = 0$ corresponds to that shown in Figure 23 for $R_S = R_L = 1K\Omega$. Adding a bias current of 0.5mA sets the diode on the edge of conduction ($V_d = 0.5V$; $I_d = 2\mu A$) and enables the LO to immediately turn the diode into a fully 'ON' condition. $C_{L_{min}}$ is achieved minimized with a much lower LO drive than used in the non-bias condition. Conversely if the diode is biased well into conduction as in the case of using a 1.5mA bias current then a larger LO drive is required to achieve $C_{L_{min}}$. This effect can best be examined with the aid of Figure 25. The minimum C_L achieved in all three cases is within the error tolerance of the FHT and therefore identical.

In Figure 25 C_L is plotted vs. T_{TON} for the above three cases. Beside each point the value of T_{NL} is listed. We see that optimum conversion loss is achieved when T_{TON} is between 0.45 and 0.55 T_{LO} independent of the bias current used. In the curve corresponding to $I_{bias} = 0$, C_L decreases as I_{LO} increases. Increasing I_{LO} decreases T_{TON} as is intuitively obvious. For the $I_{bias} = 0.5$mA curve, the diode is biased on the edge of conduction and the diode will be 'ON' for $0.5\,T_{LO}$ irrespective of the drive level. However, increasing LO drive causes less time to be spent in the highly nonlinear region, the diode is quickly swept into the fully 'ON' region; conversion loss decreases. Lastly, the curve $I_{bias} = 1.5$mA corresponds to the situation where the diode is biased well into conduction region. Any small LO drive causes T_{ON} immediately to be greater than $0.5\,T_{LO}$. Increasing the LO drive reduces T_{ON} from 0.65 to 0.50 T_{LO} thereby reducing conversion loss. At $C_{L_{min}}$ the 'ON' time for the three cases of no bias, 0.5mA and 1.5mA bias are $(0.09, 0.46)\,T_{LO}$, $(0.16, 0.50)\,T_{LO}$, and $(0.09, 0.56)\,T_{LO}$.

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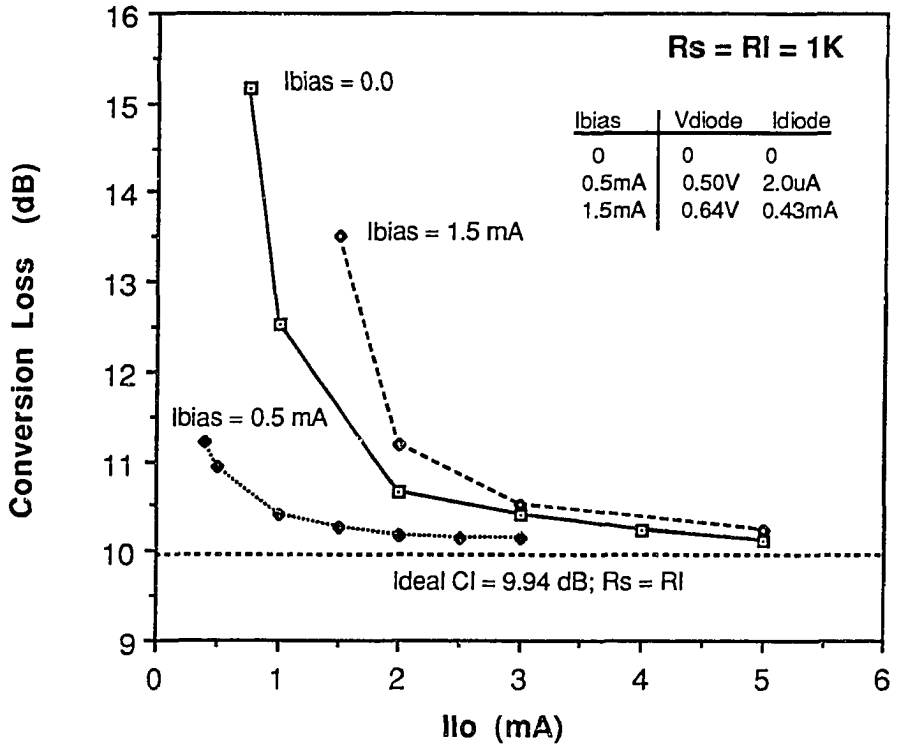


Figure 24: Conversion loss vs. LO drive.

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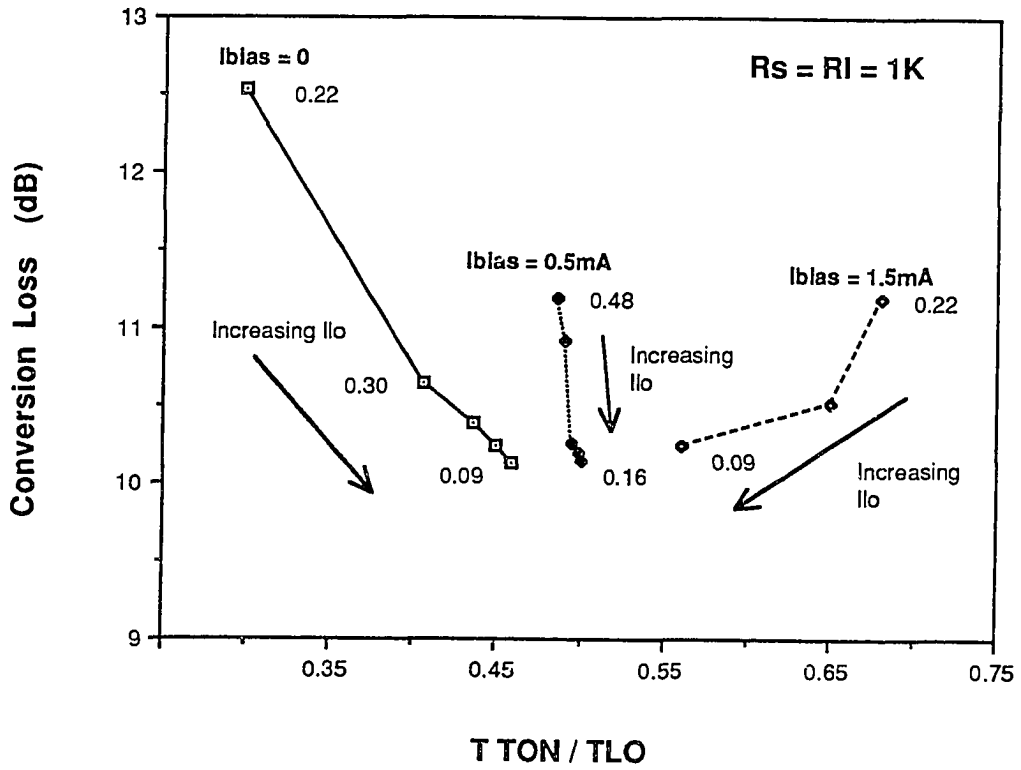


Figure 25: Conversion loss vs. fractional diode 'ON' time.
(The value of T_{NL}/T_{LO} is given alongside the graphed point (T_{TON}/T_{LO} , C_L).)

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Switch Analogy Conclusions

When examining the performance of the switch with regard to maximizing the output at the difference frequency we concluded that $V_{out}(IF)$ is proportional to the RF current that is transferred to the load during one LO cycle when the RF and LO are in phase. Maximizing this average current, $\langle I_d(T_1) \rangle$, minimizes conversion loss. Furthermore we found that this could be accomplished by setting the switch duty cycle to 50% and by using equal R_S and R_L. These conclusions were validated when the ideal switch was replaced by a diode as the mixing element in the circuit. Setting $R_S = R_L$ and $T_{ON} = 0.50\,T_{LO}$ was found to result in minimum conversion loss. C_L then was 0.3dB higher than that predicted when the switch was used. To set $T_{ON} = 0.5\,T_{LO}$ the use of drive and bias currents were considered. The following conclusions are made: 1) $C_{L_{min}}$ will be achieved whenever the combination of I_{bias} and I_{LO} are such that the diode is 'ON' 50% of the LO cycle and this time is spend mostly in the fully conducting region (ie. $T_{NL} \ll T_{TON}$); 2) power consumption will be minimized with the use of bias current if the diode is biased at the edge of conduction; 3) the use of bias current does not change the optimum value of R_L for $C_{L_{min}}$. These observations were found to hold when the source and load impedances were set equal to 50Ω or $10K\Omega$.

Returning to the idea that C_L will be decreased if the RF current transferred to the load can be increased when the LO and RF are in phase, further thought shows two ways in which a reduction of C_L may be attempted. First, $\langle I_L(T_1) \rangle$ would be increased if, when the switch turned 'ON', R_L appeared much smaller than R_S. This can be achieved through the use of frequency selective circuits. This will be the subject of the next section. Second, $\langle I_L(T_1) \rangle$ would increase if the RF current could be transferred to the laod with the opposite phase when the switch were off. If, in a fashion analogous to a balanced rectifier, we could make a mixer with a ± 1 multiplier the average current would double, thereby decreasing C_L by a factor of 4 or 6dB for a mixer where f_{RF} and f_{LO} were very close. The waveform of such a multiplier is shown in Figure 26. Its conversion loss is 3.94dB. It is hard to implement such a circuit. Some configurations of balanced mixers, driven by an LO applied at the center tap of the secondary, produce similar waveforms at their output as the switch with the ± 1

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multiplier. During the LO cycle there is always one diode on; the phase of the RF at the output is either in or out of phase with respect to the RF source depending on which diode is 'ON'. However the conversion loss is unchanged as the RF signal is power split prior to being applied to the diode. Figure 26 seems to demonstrate that if the RF energy present when the diode is 'OFF' can be stored so as to contribute to the output waveform when the diode is 'ON' then conversion loss can be reduced. Ultimately the conversion loss would approach that predicted by Kelly as the limit for resistively matched broadband mixers of 3.92dB with resistive diodes [36]. This idea will be discussed in Chapter 5.

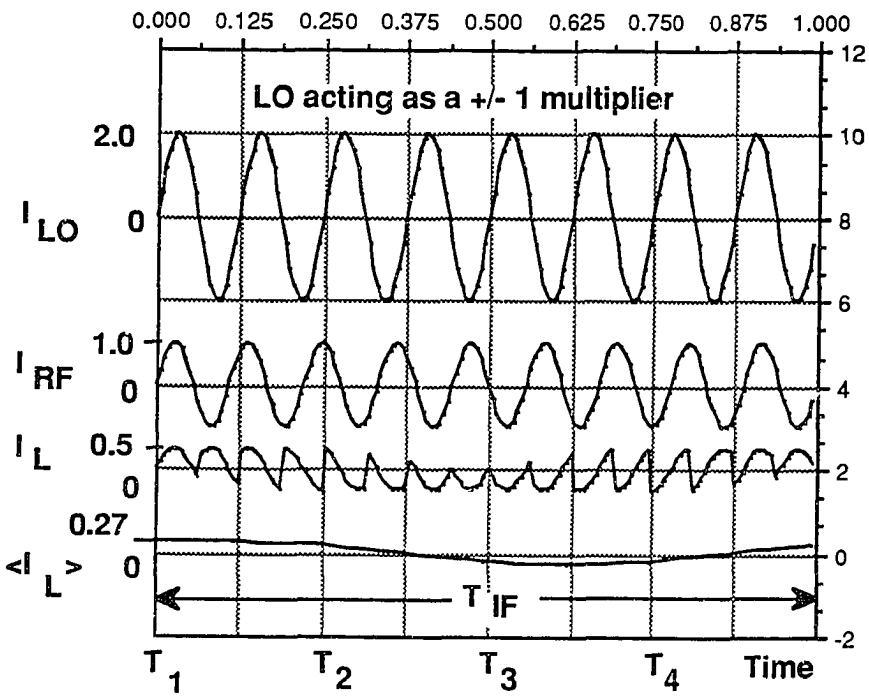


Figure 26: Waveforms of a mixer with ± 1 multiplier.

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4.2.2 Analysis of Three Mixer Circuits: 'Y', 'Z', and 'RM' Mixers

From frequency domain mixer studies, we know the mixer depicted in Figure 14 will not perform very well. Torrey and Whitmer [67] stress the importance of having both RF and LO appear to drive a grounded diode, and, they emphasize that the same condition apply to the generated IF source. Reactively terminating the image and higher order frequencies to achieve low C_L has been repeatedly stated by Egami [17], Saleh [55], and Barber [6].

Saleh categorized mixer circuits according to whether they provided an open or short circuit, as seen from the diode terminals, at each one of the LO harmonics. These circuits were analyzed for use with exponential diode only; the conditions for optimum performance were derived for each circuit type. Although he could not prove that this was the optimum passive embedding network, he postulated that if the time origin could be chosen to make the resistance waveform an even funtion of time then the optimum network should present either an open-circuit or a short-circuit to each of the out-of-band frequencies [56]. The performance of the endless variety of reactively matched circuits fell between the limits set by the 'Z' mixer in which all $n > 1$ sidebands are open circuited, and the 'Y' mixer in which all the $n > 1$ sidebands are short circuited with the 'Z' mixer having the best performance and the 'Y' mixer the worst.

Here we examine the 'Z' and 'Y' mixers with our design tool to understand how they differ and see how the performance of these circuits, implemented practically, compares with their mathematically predicted characteristics. We compare their performance with that of the resistively matched mixer analyzed in Section 3.3.

Description of 'Y', 'Z', and 'RM' Mixer Circuits

The ideal 'Y' mixer configuration is depicted in Figure 27(a). At the RF port L_S and C_S are chosen to resonate at f_{LO}, thus providing infinite impedance at the LO, RF and image frequencies, and a short at all other frequencies. Simularly the output tank circuit, L_L and C_L, resonates at f_{IF}, providing an open circuit at that frequency

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and a short to all others. The effect of this resonant circuits is to embed the diode in a circuit that short-circuits DC and all sidebands above f_{RF}.

The optimized version of our practical realization of a 'Y' mixer is shown in Fig 27(b). There are two differences between this circuit and its ideal counterpart, they lie in the way bias is applied to the diode and in the lack of a resonant circuit at the output port. Insofar as the location of the bias sources both methods succeed in setting bias however the second is easier to analyze with SPICE. However this simplified method of applying bias has a secondary effect of changing the embedding impedance, $Z_{emb}(f)$, presented to the diode at D.C. Without the presence of L_{choke} and L_{LD} the diode's output is no longer shorted to ground. Instead the value of $Z_{emb}(DC)$ is equal to $R_L + j\omega L_S$, or, approximately R_L. Simulations have shown that this does not provide any advantage for conversion loss performance and hence it has been removed to simplify the circuit.

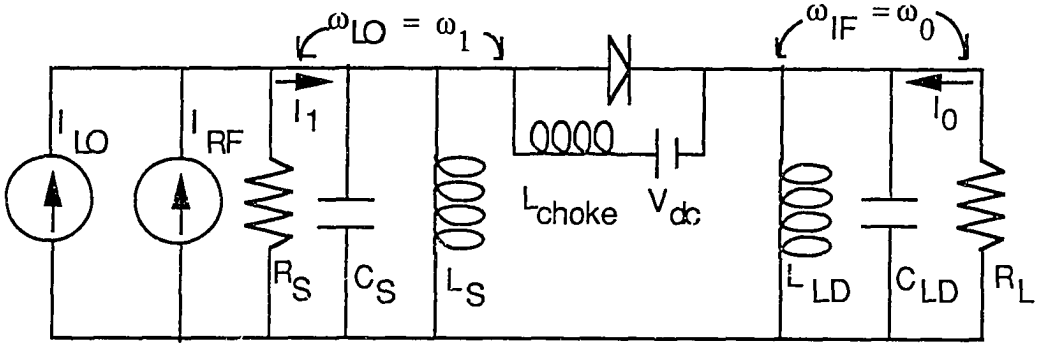
As we are interested in matching the mixer to an IF amplifier with a source impedance in the range of 1-5KΩ as discussed in Chapter 2, the output impedance was set initially at 1KΩ. C_{LD} was chosen so that the output impedance ($R_L \parallel C_{LD}$) could be an effective short at f_{LO}, $Z_{LOAD}(f_{LO}) = R_L/15 \ \angle -86°$. R_S was initially set equal to R_L, L_S and C_S were chosen to resonate at f_{LO} and provide as close to a short as possible at the second LO harmonic. The LO drive was adjusted so as to fully turn the diode 'ON'. Subsequently all matching elements, drive and bias levels were varied to optimize the conversion loss performance of the circuit.

The circuit values of the optimized circuit are listed in Figure 27(b). R_L has been chosen to match $Z^*_{out}(f_{IF})$ which, for a purely resistive diode, is mostly resistive. R_S, L_S, and C_S provide a low C_L source impedance, one which happens to be close to $Z^*_{in}(f_{RF})$[3] though this is not necessarily the condition for minimum C_L. L_S and C_S resonate at 1.04 f_{LO}.

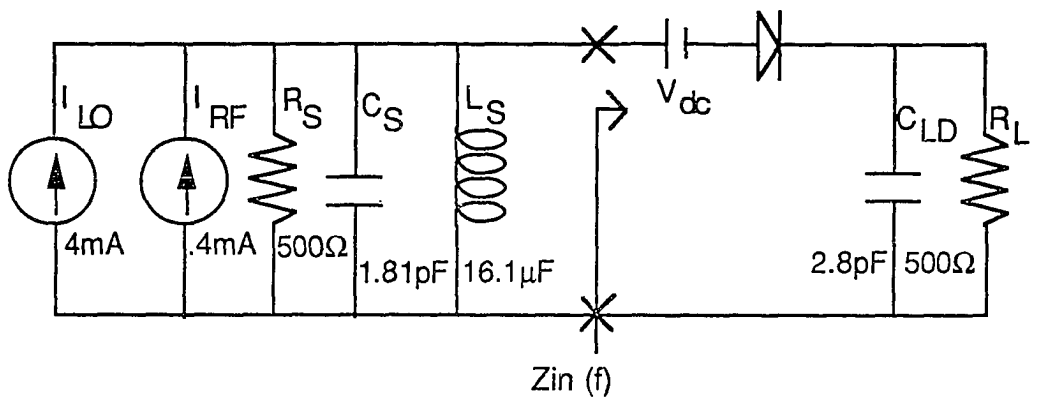
Figure 28 depicts the ideal 'Z' mixer and its practical implementation. The embedding network open circuits all frequencies above f_{RF}. L_S and C_S are chosen to resonate at f_{RF} and L_L and C_{LD} at f_{IF}. Bias is supplied through an RF choke. When realized practically, bias is applied in series with the diode and the tuned circuit at

[3] $Z_{in}(f)$ is defined in Figure 27(b).

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(a)



(b)

Figure 27: Y Mixer: (a) idealized circuit; (b) practical implementation with optimized circuit elements.

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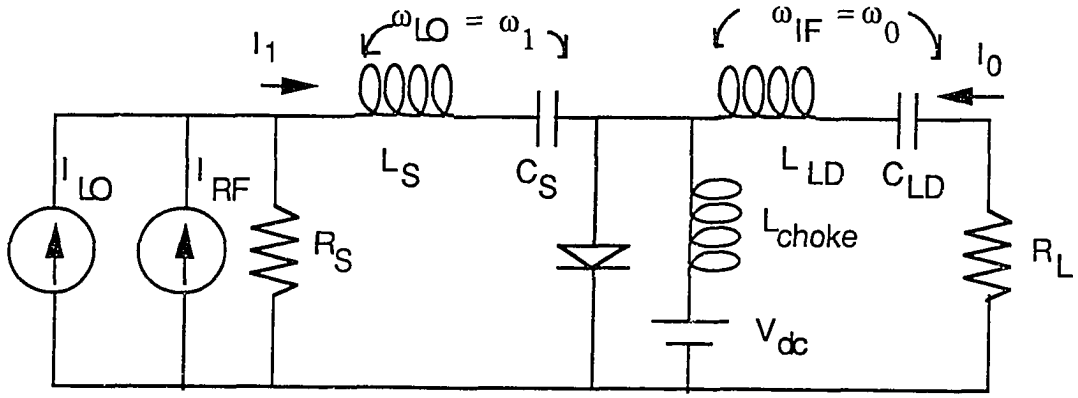
the output is replaced by one reactive element, as was done for the 'Y' mixer. As a result the embedding circuit looks resistive at DC, equal to R_L, and the diode voltage at DC is not zero whereas in the ideal circuit the diode is shorted through the action of the RF choke and $\langle V_d \rangle = 0$ Volts. As with the 'Y' mixer, R_S and R_L were initially set at 1KΩ, L_L was chosen to provide as high an impedance as possible at f_{LO} while affecting the total load impedance $(R_L + j\omega L_L)$ as little as possible at f_{IF}, L_S and C_S were set to resonate at f_{LO} and yield an impedance $10 \cdot R_S$ at the second LO harmonic. The LO drive and bias were set to turn the diode 'ON'. The optimized circuit reflects the use of the iterative design scheme in setting $R_L, Z_S(f_{RF})$ and the appropriate bias and drive conditions for best conversion loss performance.

The 'RM' mixer to be compared with the 'Y' and 'Z' mixers is depicted in Figure 14 in Section 3.3.1. It differs from the switching mixer by the addition of L_S and C_S, consequently the diode appears grounded from the RF and IF port. From the diode point of view the embedding impedances provided by the circuit are resistive at all frequencies.

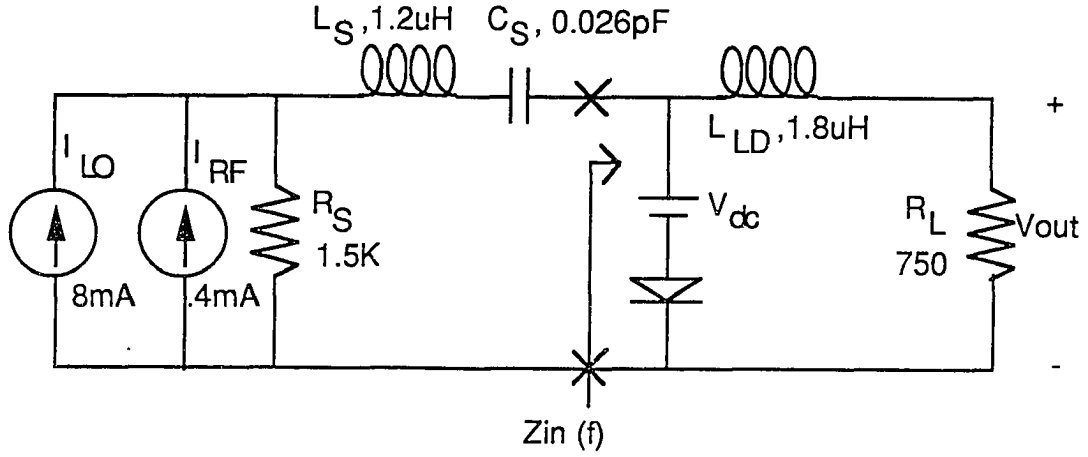
Table 5 lists the characteristics of the idealized 'Y', 'Z', and 'RM' mixers. The performance of the 'Y' mixer has been studied by many other authors including Torrey and Whitmer, Barber and Egami [67,6,17]. Their results concur with Saleh's and are given the table. The expressions for conversion loss, optimum R_S and R_L are Saleh's, as are the entries for the 'Z' mixer. The 'RM' mixer data is based on the results of simulation runs and, therefore, not derived. Immediately visible from the Table is the wide range of attributes spanned by these mixers. Whereas the 'Y' mixer's embedding circuit short circuits the out-of-band frequencies, thus allowing the voltage accross the diode to build up at the LO, RF, IF and image frequency and DC only, the 'Z' mixer, by open-circuiting all out-of-band frequencies, permits current in the diode to flow only at these same frequencies. For the 'RM' mixer no such stipulation holds for V_d or I_d.

Another widely ranging parameter is the 'ON' time of the diode. Barber showed that the optimum conductance waveform, $g(t)$, for an exponential diode in a 'Y' mixer was a rectangular waveform with a very low duty cycle - thus representing a diode that is mostly 'OFF' [6]. Saleh, when looking for the optimum $g(t)$ for the 'Y' mixer,

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(a)



(b)

Figure 28: Z Mixer: (a) idealized circuit; (b) practical implementation with optimized circuit elements.

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Table 5: Characteristics of Ideal 'Y', 'Z', and 'RM' Mixers

	'Y' Mixer	'Z' Mixer	'RM' Mixer
Effect of Embedding Circuit:			
$Z_{emb}(f)$	Short circuit sidebands	Open circuit sidebands	Resist. match sidebands
$V_d(t)$:			
Large signal	$V_{DC} + V_P \cos(\omega_{LO}(t))$	Arbitrary	Arbitrary
Small signal	components at ω_{IF}, $\omega_{RF}, \omega_{image}$ only		
$I_d(t)$:			
Large signal	Arbitrary	$I_{DC} + I_P \cos(\omega_{LO}(t))$	Arbitrary
Small signal		components at ω_{IF}, $\omega_{RF}, \omega_{image}$ only	
Diode Condition:†			
	Mostly OFF	Mostly ON	$T_{ON} \simeq 0.50 \cdot T_{LO}$
Optimized Circuit Characteristics:‡			
Drive Level	$\alpha V_P \gg 1$	$I_P \leq I_{DC} + I_S$	
$R_{S_{opt}}$	$V_P/(\sqrt{2} \cdot I_{DC})$	$2/(\alpha \cdot I_{DC} \cdot b)$	Arbitrary
$R_{L_{opt}}$	$2 \cdot R_{S_{opt}}$	$R_{S_{opt}}/2$	R_S
C_L	$2\,(1 + \sqrt{2}/(\alpha V_P))$	$2\,(1 + 2b)$	
C_L Limit	3.0 dB	3.0 dB	3.92 dB††

†Derived from ideal diode resistance waveform considerations.

‡These circuit conditions and resulting mixer performance have been derived for a broadband mixer with an exponential diode ($r_{ser} = 0$, n = 1, $C_{j0} = 0$) where: $\alpha = q/kT$ and $b = (1 - (\frac{I_P}{I_{DC}+I_{sat}})^2)^{\frac{1}{4}}$ [57].

††From reference [36].

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arrived at the same result, and, when looking for the optimum resistance waveform $r(t)$for the 'Z' mixer, concluded that the optimum $r(t)$ was also rectangular. Its value is mostly held at some low level, ie. 10Ω, with narrow spikes whose maxima were large, ie. 10KΩ. This can be realized by a mostly 'ON' diode. In the case of a 'RM' mixer, the results of the idealized switch would indicate that a 50% duty cycle would be optimum.

Given an exponential diode and an even conductance waveform, Saleh derived criteria for the optimum performance of the 'Y' and 'Z' mixers under certain assumptions about the power range of the LO, easily met in the 'Y' mixer's case but much more limiting in the 'Z' mixer's case. The expressions for conversion loss and optimum impedances are listed in the Table 5 for the specific case of a broadband input circuit, one where the image and RF are terminated identically. For such a circuit, the fundamental limit on conversion loss for both the 'Y' and 'Z' mixer is 3dB, however the 'Z' mixer approaches this limit more rapidly than the 'Y' mixer at any given drive level. Moreover, Saleh found that the performance of any mixer which terminated each out-of-band frequencies in either a short or an open fell between the performance levels set by the 'Z' and 'Y' mixers.

No expression for conversion loss can be derived for the 'RM' mixer. From switching mixer results, $C_{L_{min}}$ is expected given an arbitrary R_S as long as $R_{L_{opt}} = R_S$. The C_L limit specified is Kelly's who found the $C_{L_{min}}$ for a broadband mixer with resistive termination of the out-of-band frequencies to be 3.92dB [36].

Performance of 'Y', 'Z' and 'RM' Mixers

Tables 6 and 7 give the performance of the 'Y', 'Z' and 'RM' mixers optimized with the design tool. Table 6 lists the embedding impedances provided by each of the circuits. Although they do not resemble an absolute short or open at the harmonics of the LO, for the most part they do provide an adequate short or open relative to the match at f_{LO}. At $2 \cdot f_{LO}$ the match is mostly reactive even if its magnitude is not quite that of an open or a short. The effect of these matches can be seen by examining the normalized magnitudes of the Fourier coefficients of V_d and I_d, given in Table 6. Ideally the large signal diode voltage of the 'Y' mixer and the large signal

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diode current of the 'Z' mixer should be represented primarily by a DC component and an LO component. The 'Y' mixer circuit achieves this better than the 'Z' mixer one; however both look quite different than the corresponding Fourier coefficients of the 'RM' mixer. The performance of these prototype circuits is listed in Table 7 and will be discussed below.

The circuit waveforms for these three mixer types are strikingly different. In Figure 29 the diode waveforms, I_d, I_{d_r}, and V_d, are shown. The diode voltage for the 'Y' mixer looks much more sinusoidal than in either of the other two cases, as does the diode current for the 'Z' mixer as predicted in Table 5. The consequences for the 'Z' mixer are drastic as the diode voltage is forced to a large negative value and ramped in a sawtoothed fashion to produce a sinusoidal I_d. From these waveforms it is obvious that, as predicted, the 'Y' mixer is 'OFF' most of the LO cycle whereas the 'Z' mixer is 'ON'. Exactly how much the diodes in these two circuits are 'OFF' or 'ON' can be known from Table 7. From it, T_{TON} is found to be 0.25 T_{LO} and 0.74 T_{LO} for the 'Y' and 'Z' mixers, respectively. These T_{TON} values have been optimized for low C_L, adjusting circuit and bias parameters so that $T_{TON} = 0.50\ T_{LO}$ results in 2dB higher C_L. In the case of the 'RM' mixer, Figure 29 shows that the optimum mixer performance is attained when the diode is 'ON' for half the LO cycle, as expected from the switching mixer analogy. For all three circuits, increasing LO drive reduced conversion loss with, however, decreasing returns after the drive levels specified for these runs.

In Figure 30 the diode small signal conductance, $g(t)$, is shown for the 'Y' and 'RM' mixers and its inverse, the diode resistance, $r(t)$, is plotted for the 'Z' mixer only. $g(t)$ and $r(t)$ are calculated as follows:

$$g(t) = \frac{\Delta I_{d_r}}{\Delta V_j} \tag{24}$$

$$r(t) = \frac{\Delta V_j}{\Delta I_{d_r}} \tag{25}$$

where V_j, defined in Figure 15, is the junction voltage:

$$V_j = V_d - I_d \cdot rser \tag{26}$$

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Table 6: Characteristics of Practically Implemented 'Y', 'Z', and 'RM' Mixers

	'Y' Mixer pdiod569		'Z' Mixer pdiod583		'RM' Mixer pdiod557	
Frequency:	$Z_{embedding}(f)$					
DC	1KΩ	0°	750Ω	0°	1KΩ	0°
f_{IF}	987Ω	-9°	756Ω	7°	987Ω	-3°
f_{LO}	764Ω	33°	1.5KΩ	8°	995Ω	2°
$2 \cdot f_{LO}$	98Ω	-87°	6.7KΩ	83°	998Ω	1°
$3 \cdot f_{LO}$	58Ω	-88°	11.2KΩ	86°	999Ω	1°
$4 \cdot f_{LO}$	42Ω	-89°	15.4KΩ	87°	1KΩ	1°
$5 \cdot f_{LO}$	33Ω	-89°	19.5KΩ	88°	1KΩ	0°
$6 \cdot f_{LO}$	27Ω	-89°	23.6KΩ	88°	1KΩ	0°
Frequency:	$\left\|\frac{V_d(f)}{V_d(DC)}\right\|$ Ideal 'Y' mixer values as 1,1,0,0,0...					
DC	1.0		1.0		1.0	
f_{LO}	2.14		2.48		2.57	
$2 \cdot f_{LO}$	0.17		1.95		0.82	
$3 \cdot f_{LO}$	0.08		1.30		0.13	
$4 \cdot f_{LO}$	0.04		0.72		0.13	
$5 \cdot f_{LO}$	0.02		0.45		0.07	
Frequency:	$\left\|\frac{I_d(f)}{I_d(DC)}\right\|$ Ideal 'Z' mixer values are 1,1,0,0,0...					
DC	1.0		1.0		1.0	
f_{LO}	1.91		1.28		1.63	
$2 \cdot f_{LO}$	1.71		0.22		0.82	
$3 \cdot f_{LO}$	1.39		0.087		0.13	
$4 \cdot f_{LO}$	1.04		0.035		0.13	
$5 \cdot f_{LO}$	0.72		0.017		0.07	

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Table 7: Performance of Practically Implemented 'Y', 'Z', and 'RM' Mixers

	'Y' Mixer pdiod569	'Z' Mixer pdiod583	'RM' Mixer pdiod557
Circuit Characteristics (f_{RF} = 909 MHz):			
I_{Bias}, I_{LO}	0, 4mA	0, 8mA	0, 4mA
R_S, R_L	1K, 1K	1.5K, 750Ω	1K, 1K
L_S, C_S	16.08μH, 1.81pF	1.2μH, 0.026 pF	1.8 μH, 0
L_L or C_L	2.83 pF	1.8 μH	2.83 pF
Diode Condition:			
T_{NL}/T_{LO}, T_{TON}/T_{LO}	0.06, 0.25	0.10, 0.74	0.06, 0.46
$V_{d_{max}}$, $V_{d_{min}}$	0.79V, -2.9V	0.78V, - 20.0V	0.72V, -4.4V
$I_{d_{max}}$, $I_{d_{min}}$	8.1mA, -8.0nA	7.8mA, -10.0μA	3.6mA, -31nA
Circuit Performance:			
C_L	5.0dB	4.25dB	4.33dB
$Z_{in}(f_{RF})$	902Ω -29°	1.3K 33°	1.3K -4°
$Z_{out}(f_{IF})$ (R_{L_1}, R_{L_2})	1.2K -16° (1K, 2K)	734Ω 15° (1K, 750Ω)	1.1K -7° (1.1K, 800Ω)
$Z_S(f_{RF})$	878Ω 29° $(R_S\|j\omega L_S\|j\omega C_S)$	1.5K 5° $(R_L + j\omega L_S + \frac{1}{j\omega C_S})$	995Ω 6° $(R_S\|j\omega L_S)$
$Z_{LOAD}(f_{IF})$	993Ω -9° $(R_L\|j\omega C_{LD})$	757Ω 8° $(R_L + j\omega L_{LD})$	993Ω -9° $(R_L\|j\omega C_{LD})$

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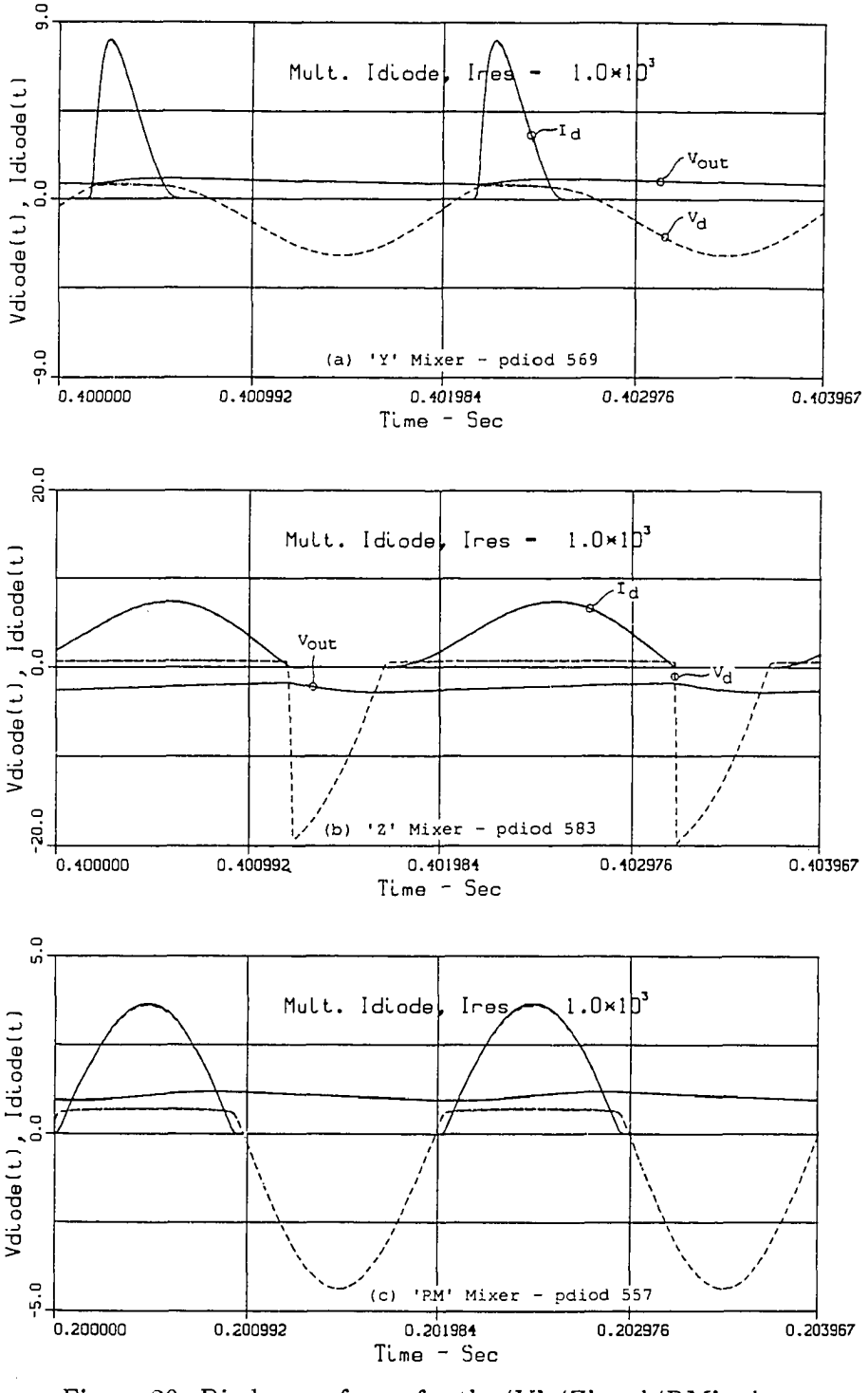


Figure 29: Diode waveforms for the 'Y', 'Z' and 'RM' mixers.

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and, I_{d_r} is as given by eqn. 5 in Section 3.3:

$$I_{d_r} = I_S\,(\exp(\frac{qV_j}{nkT}) - 1).$$

$g(t)$ and $r(t)$ are shown for comparison with the ideal diode waveforms predicted by analysis. As the 'Y' mixer's performance is optimized with a mostly 'OFF' diode, $g(t)$ is expected to be zero for a large portion of the LO cycle and rise to its maximum value ($g_{max} > 1/r_{ser}$) when the diode is 'ON'. Because the 'Z' mixer is optimized when the diode is mostly 'ON' $r(t)$ should stay at a value close to r_{ser} (10Ω) for the majority of T_{LO}, rising rapidly to a very large resistance when the diode is 'OFF'. Lastly the 'RM' mixer has been shown to have the lowest conversion loss when the diode is 'ON' for half of T_{LO}. $g(t)$ is therefore expected to hover about zero for $T_{LO}/2$ and slowly rise to its maximum value ($g(t) < 1/r_{ser}$) as the diode turns 'ON'.

Examination of Figure 30 shows that $g(t)$ and $r(t)$ behave as expected for the three mixer types. The rapid fluctuations in $g(t)$ are the result of dividing small differences and are an artifact of the method used to calculate $g(t)$. It is interested to note that the most unsymmetrical $g(t)$ waveform belongs to the 'Y' mixer which hence cannot be represented as an even function as is typically assumed for mixer analysis. Calculation of diode $g(t)$, and $C_B(t)$, also enables a comparison of mixer performance as predicted by this design tool and as predicted by frequency domain analysis. This is described in Section 4.4.

Comparison of Prototype and Ideal Circuit Performance

The conversion loss of the three mixers is calculated to be 5.0, 4.25 and 4.3dB for the 'Y', 'Z', and 'RM' mixers, respectively. The 'Z' mixer has the lowest C_L, as predicted, and, surprisingly, the 'RM' mixer is not much worse. It is possible that the conversion loss for this mixer would have dropped had a much better open circuit been established at the second LO harmonic. A few other circuits were tried but did not result in improved C_L. The 'Y' and 'Z' mixers are within 2.0 and 1.25dB of their optimum C_L of 3dB whereas the 'RM' mixer is within 0.4dB of its optimum of 3.92dB.

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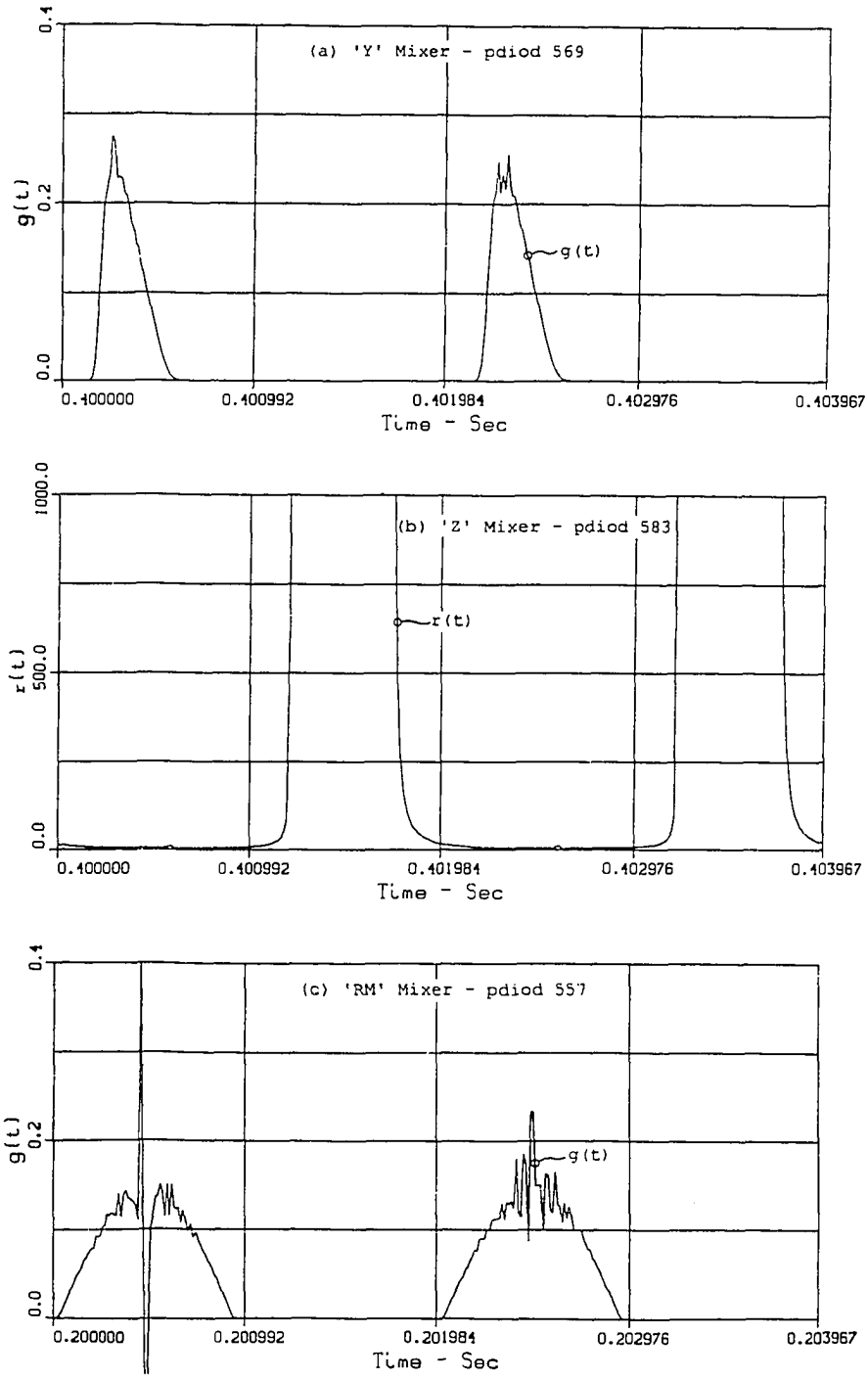


Figure 30: Conductance and resistance waveforms for the 'Y', 'Z', and 'RM' mixers.

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We can compare the simulated mixer results for the practically implemented 'Y' and 'Z' mixers against the calculated performance for idealized 'Y' and 'Z' mixers with exponential diodes listed in Table 5. Using the DC value of V_d at f_{LO}, or V_p, the predicted values for $R_{S_{opt}}$, $R_{L_{opt}}$ and the corresponding C_L can be calculated for the 'Y' mixer. The results are valid if $\alpha V_p \gg 1$ as is the case in the mixer run ($\alpha V_p = 69$). $R_{S_{opt}}$ is found to be 1.5K, $R_{L_{opt}}$ to be 3.0K and the corresponding C_L is 3.1dB.

Mixer simulations for the 'Y' mixer do not exactly corroborate these predictions. As shown in Table 7, minimum C_L is achieved when $R_S = R_L = 1$K, $C_{L_{min}}$ is 5.0dB. When R_L is set equal to $2 \cdot R_S$, the predicted optimal relationship between R_S and R_L, C_L rose to 5.35dB. Using a different set of embedding impedances with $R_S = R_L = 500\Omega$ or $R_S = R_L = 1$K, C_L rose to 5.5dB. When R_S and R_L were set equal to 2K, C_L rose by 1.5dB to 6.5dB. The rise in C_L in the case of $R_S = R_L = 1$K as compared to the minimum C_L run can be attributed to the degradation of this circuit's match to the ideal 'Y' embedding impedances (short-circuiting all frequency above f_{LO}) with respect to those achieved in the optimal mixer run; the latter embedding impedances are shown in Table 6.

The optimum source and load impedance and the corresponding C_L can not be calculated from the large signal driving condition for the 'Z' mixer as the necessary condition $I_P \leq I_{DC} + I_S$ (or, $I_d(f_{LO}) \leq I_d(DC)$) is not met by the simulation run. As shown in Table 6 $|I_d(f_{LO})/I_d(DC)| = 1.28$. Reducing the drive by one fourth did not cause $I_p \leq I_{DC} + I_S$. However the predicted relationship between $R_{L_{opt}}$ and $R_{S_{opt}}$ ($R_{L_{opt}} = R_{S_{opt}}$) was supported by the simulation. When R_L was increased from 750Ω to 1K, C_L increased by 0.1dB to 4.35dB. Simulation results also indicated that specific values of R_S and R_L exist to achieve $C_{L_{min}}$ for when R_S was decreased from 1.5K to 1K and R_L was again set at $R_S/2$, C_L increased from 4.25dB to 6.4dB.

For both the 'Y' mixer and the 'Z' mixer, increasing the LO drive caused C_L to decrease; it reduced T_{TON} for the 'Y' mixer and increased T_{TON} for the 'Z' mixer. Also increased bias voltage could be used to arrive at the same C_L while reducing LO drive.

In conclusion the performance of the 'Y' and 'Z' mixers was found to be close to the predicted characteristics in a qualitative if not quantitative way. The 'ON'

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times differed greatly between mixers, the 'Y' mixer employing a diode 'OFF' 75% of the LO cycle and the 'Z' mixer a diode 'ON' for 25% of the LO cycle. The conversion loss of the 'Z' mixer was 1.25dB away from the 3dB C_L limit, that of the 'Y' mixer was 2dB worse than the conversion loss of the 'Z' mixer when the LO drive caused a roughly 8mA current in both diodes. Both mixers possessed preferred source impedances to achieve $C_{L_{min}}$. The expected relationship between $R_{S_{opt}}$ and $R_{L_{opt}}$ was confirmed through simulation for the 'Z' mixer but not for the 'Y' mixer. The quantitative differences can be explained by the use in the simulations of a diode with series resistance, by the fact that $g(t)$ was not even, hence, not meeting the assumptions of Saleh's derivation, and lastly to the use of a practical circuit over the ideal configuration.

The performance of the 'RM' mixer can be compared against the guidelines for C_L optimization developed for the ideal switching mixer although the two circuits differ due to the inclusion of L_S and C_{LD} in the circuit. These guidelines are shown to hold for optimizing the performance of the 'RM' mixer: C_L is minimized when $T_{TON} \rightarrow 0.50T_{LO}$ and when $R_S = R_L$. Simulation runs for R_S and R_L equal to 10K or 500Ω showed no difference in C_L. When R_S and R_L were set equal to 50Ω, C_L increased to 5.0dB, attributable to the effect of increasing relative power dissipation in the diode resistance as discussed in Section 4.2.1. As for the other mixers studied, increasing the LO drive caused C_L to decrease and bias drive could be traded off for reduced LO drive to achieve the same C_L.

Choice of Mixer Circuit for Basis of Direct Conversion Mixer

Having examined the performance of three prototypes for the direct conversion mixer, Saleh's 'Y' and 'Z' mixers and the *Resistively Matched* mixer of Section 3.3, the conversion loss of the 'Z' and 'RM' mixers were found to be nearly identical. Because the 'RM' circuit is easier to realize and works well with a wide range of source impedances, it is potentially a more versatile mixer. The subsequent mixer work in this chapter will explore the performance of a 'RM' circuit when a diode with barrier capacitance is used and when it is implemented in a balanced configuration.

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4.2.3 Performance of the *Resistively Matched* Mixer - Barrier Capacitance Included in the Diode Model

In this section we examine the performance of mixers when a more complete diode model is used, namely, when the barrier capacitance of the diode is included in the diode model. The capacitance of the diode is varied from 0.25pF to 1.5pF and the resulting degradation of conversion loss is quantized when the diode is placed in a 'RM' circuit. Compensation techniques are discussed to improve mixer performance when barrier capacitance is present.

No general circuit categorization has been completed for mixers using diodes with barrier capacitance. Mania and Stracca compared the performance of 'Z' and 'Y' circuits when a diode with a constant barrier capacitance is used to that obtained when a purely resistive diode is employed. They found that the presence of barrier capacitance caused the mixer's conversion loss to degrade for both mixer types. The deterioration in C_L was so much greater for the 'Z' mixer than the 'Y' mixer that the C_L of the 'Y' mixer became lower than that of the 'Z' mixer for a given capacitance value. This is the inverse of that expected when purely resistive diodes are used. They concluded that the 'Y' mixer possesses a lower conversion loss than the 'Z' mixer - the inverse of the purely resistive case[47]. The increase in conversion loss predicted by Mania and Stracca has been mirrored in most practical mixer work with the result that mixer designers choose devices with as low a C_B as possible.

A typical diode model with barrier capacitance is shown in Figure 15 on page 43. Barrier capacitance, C_B, is included in the model to account for charge storage in the boundary layer between the metal and the semiconductor. As stated in Section 3.3.2, the current in the diode can be written in terms of two components, one resistive, flowing through R_B, and the second capacitive, in C_B.

$$I_d = I_{d_r} + I_{d_c} \tag{27}$$

Rewritting eqns. 5, 6, 7, and 8 for a diode with a linearly graded junction (M = 1/2), we see:

$$I_{d_r} = I_S\,(\exp(\frac{qV_j}{nkT}) - 1)$$

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$$I_{d_c} = C_B \frac{dV_j}{dt}$$

for

$$C_B = \frac{C_{j0}}{(1 - \frac{V_j}{\phi})^{0.5}}$$

and

$$V_d = V_j + I_d \cdot r_{ser}$$

where V_j is the junction potential, I_S is the saturation current, r_{ser} is the series resistance, ϕ is the built-in junction voltage, and, n is the ideality factor of the diode.

Figure 31 shows the variation in C_B as the diode's junction voltage is varied from -2.5V to +0.7V for a diode with a zero-bias barrier capacitance, C_{j0}, of 1.0pF and a built-in potential of 0.9V as used in the diode model DM_1. This voltage excursion represents that of a typical LO source during one cycle. At this drive level, C_B would vary fourfold over one LO cycle. A typical value for C_{j0} for a 1GHz device would be in the range of 0.25 to 2.0pF (see Appendix A). To study the effect of C_B on mixer performance, C_{j0} will be varied from 0.25pF to 1.0pF using diode model DM_1. The mixer circuit used for this analysis will be the 'RM' mixer shown in Figure 14. It has been run with an f_{LO} = 500Hz and f_{RF} = 505Hz using C_{j0} from $0.45\mu F$ to $1.8\mu F$. The results obtained hold for the case of f_{LO} = 900MHz, f_{RF} = 909MHz and C_{j0} varying from 0.25pF to 1.5pF as the frequencies and capacitance are scaled by the same coefficient.

Figure 32 shows the diode waveforms for the 'RM' mixer with C_{j0} = 0.25pF when the LO and RF are in phase. They can be compared against the waveforms in Figure 16 for the same mixer operated with a resistive diode. In the first graph $V_{out}(t)$ is plotted for one cycle of the IF. The large LO feedthrough to the output port can be seen superimposed on the IF signal; comparison with $V_{out}(t)$ in Fig. 16(a) shows the level of LO at the output is far greater than that of a purely resistive mixer as expected from the addition of barrier capacitance to the diode model.

The total diode current, I_d, and its resistive component, I_{d_r}, are plotted along with the diode voltage, V_d, junction voltage, V_j, and output voltage, $V_{out}(t)$, in the second

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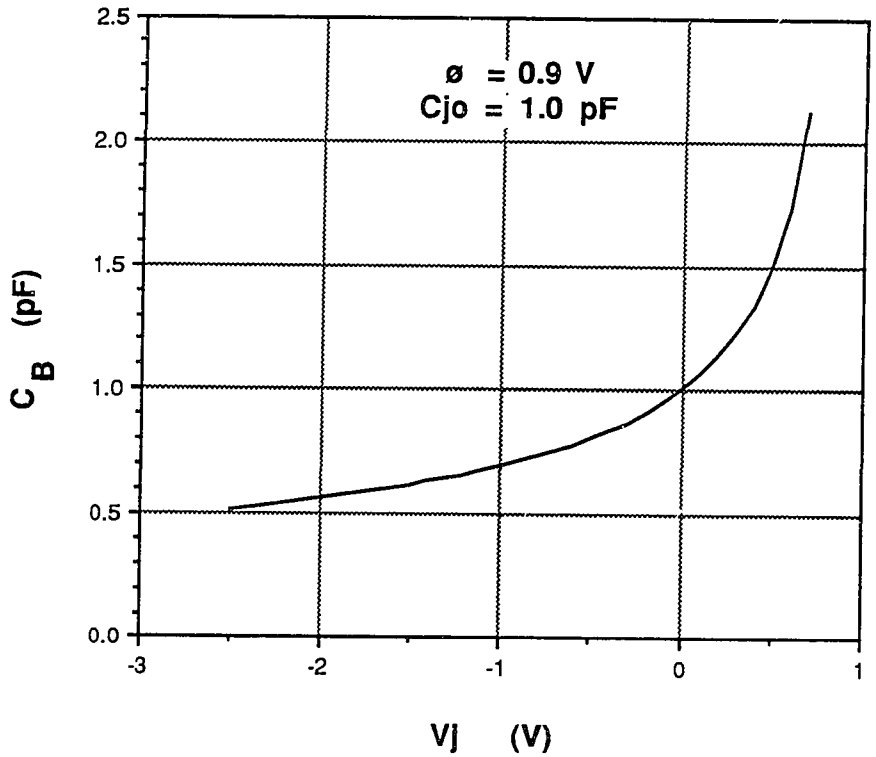


Figure 31: Barrier capacitance vs. diode junction voltage for $C_{j0} = 1\text{pF}$ and $\phi = 0.9V$.

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graph. Although the barrier capacitance is still very small, nearly half of the positive diode current is capacitive. I_d and V_d are found by the program SPICE, V_j and I_{d_r} are calculated using eqns. 8 and 5. I_{d_c} is found by subtracting I_{d_r} from I_d. Comparing Figures 32 and 16, we see the 'ON' time of the diode has been reduced by 20%, that the roll-off of V_d is slower than without C_B, and, that there are greater fluctuations in $V_{out}(t)$. The first observation is an indication that the diode now presents a lower load at the RF port. The second demonstrates that as the diode turns 'OFF', $V_{out}(t)$ discharges through C_B as well as C_{LD}. The last comment signifies that a greater amount of the LO power is now translated to the mixer output due, in part, to the fact that the diode no longer presents infinite impedance to the LO source when it is turned 'OFF'. From the value of average diode current given in the figure when the RF and LO are in- and out-of-phase, conversion loss can be calculated using eqns. 12 and 13. $V_{out}(IF)$ is found to be (0.779mA - 0.563mA)/2×1$K\Omega$, or 0.108V. $C_L(IF)$ can be found by calculating $\frac{(0.4mA)^2 \cdot 1K\Omega \cdot 1K\Omega}{4 \cdot (0.108mA)^2}$. C_L is equal to 3.43 or 5.4dB, within 4% of the value calculated from the FHT.

In the third graph, I_{d_c}, the capacitive component of diode current, is plotted along with C_B and the charge on C_B, Q_{C_B}. The charge is calculated from the definition of C_B.

$$Q_{C_B} = \int C_B \, dV_j \tag{28}$$

Using eqn. 7, we can write:

$$Q_B = -2\, C_{j0}\, \phi\, (1 - \frac{V_j}{\phi})^{0.5}$$

$C_B(t)$ is seen to be a very uneven and nonlinear function; early researchers in mixer analysis who wanted to include barrier capacitance into the conversion loss formula assume that $C_B(t)$ was an even function of time in order to obtain a tractable expression[16,9,18].[4] In this example C_{j0} is 0.45μF (for f_{RF} = 505 Hz), during one cycle of the LO, C_B varies from 0.2 to 0.9μF - from 1/2 to 2 times C_{j0}. Clearly it

[4]It was assumed that $C_B(t)$ could be written as $C_0 + 2C_1 \cos\omega_{LO}t + 2C_2 \cos 2\omega_{LO}t + \ldots$ Since $C_B(t)$ is real and therefore $C_{-n} = C_n^*$, assuming $C_B(t)$ is even implies $C_{-n} = C_n$.

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would be difficult to correctly analyze this problem by replacing C_B by a linear fixed capacitor.

Conversion loss for this run is calculated to be 5.5dB, a 1.2dB increase from the resistive diode case. This degradation in C_L can be understood by realizing that as barrier capacitance increases more charge must be supplied by the LO and RF sources to bring the junction voltage up to the turn-on voltage of the diode. This delay, which decreases the total 'ON' time of the diode during one LO cycle, adversely effects conversion loss in two ways. The first consequence is that the RF current which contributes to charging up C_B is permanently lost to the nonlinear barrier resistance and hence to the frequency conversion process. This occurs because the RF charge stored on C_B when the diode is turning 'ON' is discharged when the diode turns 'OFF' through the source impedance which is primarily resistive. The second effect occurs as the diode is turning 'OFF' and is due to the flow of current from the load to the source through C_B. Thinking of the diode as a switch, one can simplistically understand the increase in conversion loss as due to turning the switch 'ON' for less than half of the LO cycle and to using a leaky switch which conducts in the reverse direction as it is turned 'OFF'. As C_B is increased from zero to 0.25pF in a 'RM' mixer, T_{TON} is reduced from 0.46 T_{LO} to 0.36 T_{LO}.

These two effects can be seen in Figure 33 where the current in the diode, L_S, and, R_S is plotted when the RF and LO are in-phase and in quadrature phase. The RF current in each circuit element is calculated for the in-phase graph by subtracting the current in each element when the RF and LO are in-phase from the current in each element when they are 180° out-of-phase. Similarly the RF current in each element can be calculated for the quadrature graph by subtracting the current in each element when the sources are 90° out-of-phase with that when they are 270° out-of-phase. These currents are known as the differential currents in the circuit elements. The shaded area represents the amount of charge that travelled through the barrier resistance of the diode, thereby contributing to the frequency conversion process. It is also equal to the average diode current (multiplied by T_{LO}) due to the RF source that is delivered to the load during one LO cycle. Comparing these waveforms with those in Figure 18, the degradation in conversion loss is obvious; it can be quantized

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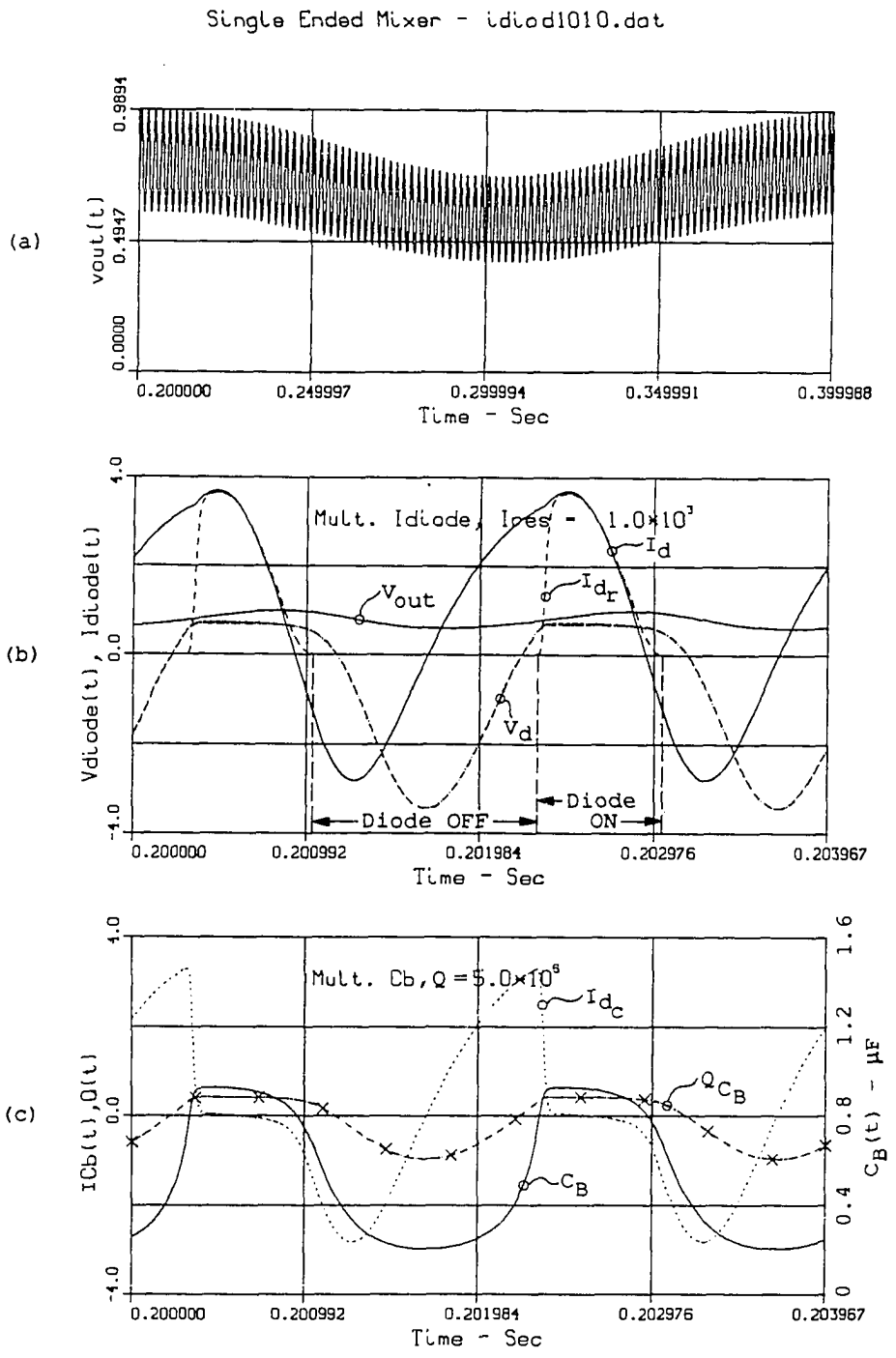


Figure 32: Diode waveforms for a 'RM' mixer with $C_{j0} = 0.25$pF.

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by noticing that:

$$\langle I_{d_{RF}} \rangle |_{C_{j0}=.25pF} = 108\mu A \ < \ \langle I_{d_{RF}} \rangle |_{C_{j0}=.001pF} = 123\mu A,$$

$$\frac{T_{TON}}{T_{LO}} |_{C_{j0}=.25pF} = 0.36 \ < \ \frac{T_{TON}}{T_{LO}} |_{C_{j0}=.001pF} = 0.46.$$

Conversion loss can be calculated in an analogous fashion to that used for the switching mixer by considering the output voltage at f_{IF} to be due to the average diode current due to the RF at T_1. From Figure 33 $\langle I_{d_{RF}}(T_1) \rangle = 108\mu A$ and $\langle I_{d_{RF}}(T_2) \rangle = -4\mu A$. The latter is expected to be close to zero as the average value of V_{out} should ideally be zero then. In fact it is 25 times less than $\langle I_{d_{RF}}(T_1) \rangle$. From $\langle I_{d_{RF}}(T_1) \rangle$, $V_{out}(IF)$ is calculated from eqn. 20 and C_L from eqn. 13. The switch analogy is helpful in stressing that the parameter to be maximized is $\langle I_{d_{RF}}(T_1) \rangle$.

In Figure 34 the conversion loss of the 'RM' mixer in Figure 14 is plotted as the barrier capacitance is increased from 0.25pF to 1.5pF. No circuit compensation has been attempted. The large increase in conversion loss to 22dB when $C_{j0} = 1.0$pF demonstrates the large impact of even small values of barrier capacitance. Mixers at 1GHz use diodes whose barrier capacitance is as high as 1pF; they can be designed to have conversion losses in the 4.5 - 5dB range but adjustments in LO drive, bias, and matching circuits must be made to minimize the degradation caused by the addition of barrier capacitance. The rapid increase in conversion loss with barrier capacitance and the subsequent need for compensation in circuit design explains why mixer designers often choose to work with devices with low barrier capacitance even at the price of higher series resistance.[5]

Table 8 lists the performance of the uncompensated 'RM' mixer circuit as C_{j0} is increased from 0.25 pF to 1.0 pF, no changes have been made in the matching circuit. The effect on diode 'ON' time and $Z_{in}(f_{RF})$ can be seen. T_{TON} drops rapidly as soon as C_{j0} is increased from 0.001pF. $|\ Z_{in}(f_{RF})\ |$ falls as C_{j0} is increased denoting the parallel impedance of C_{j0} and R_B.

[5]A common figure of merit for diodes is the cut-off frequency; it is equal to $\frac{1}{2 \cdot \pi \cdot rser \cdot C_{j0}}$. It is determined principally by the diode's surface area and doping; it reflects the tradeoff between designing for low series resistance and barrier capacitance.

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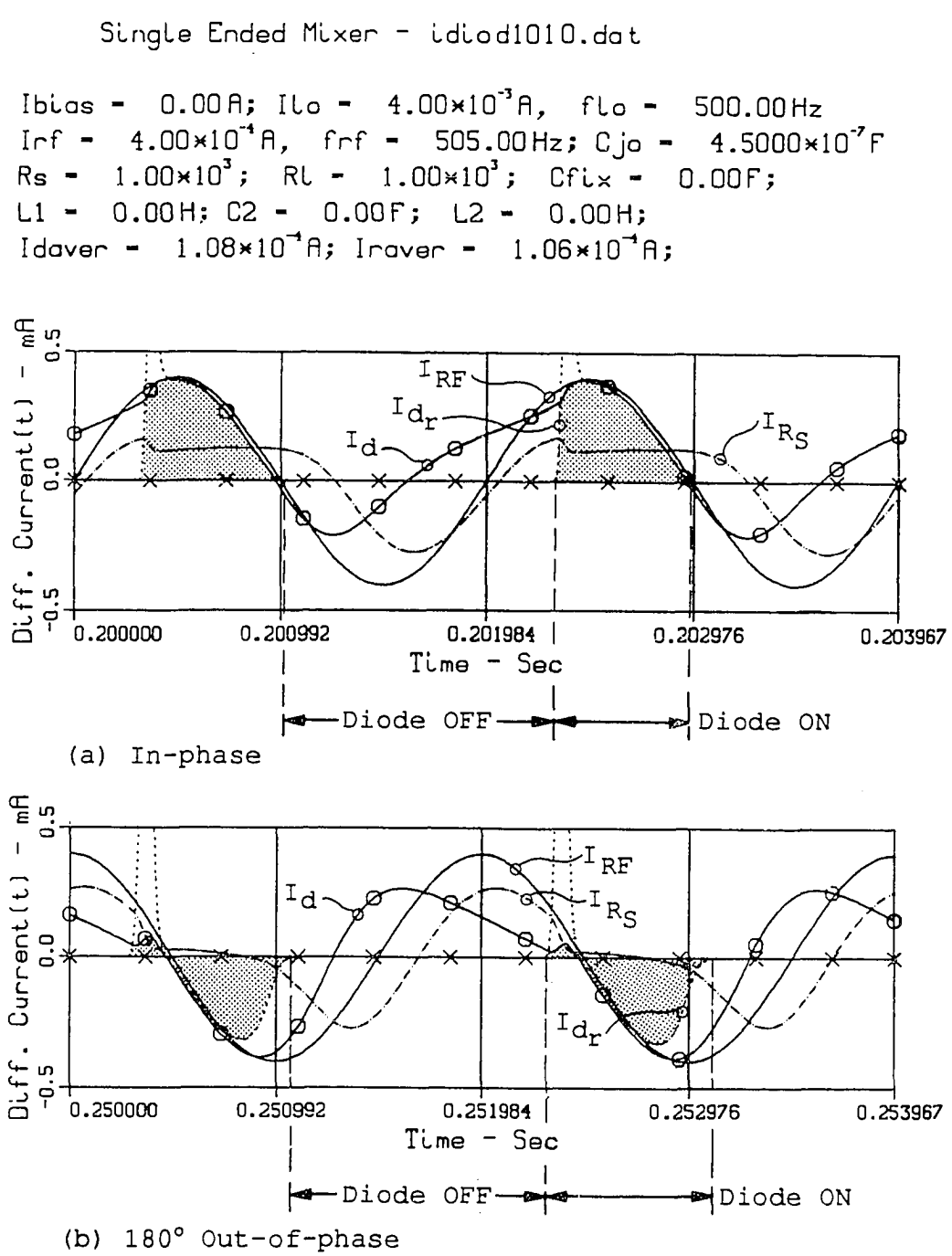


Figure 33: Differential currents in a 'RM' mixer with $C_{j0} = 0.25$pF.

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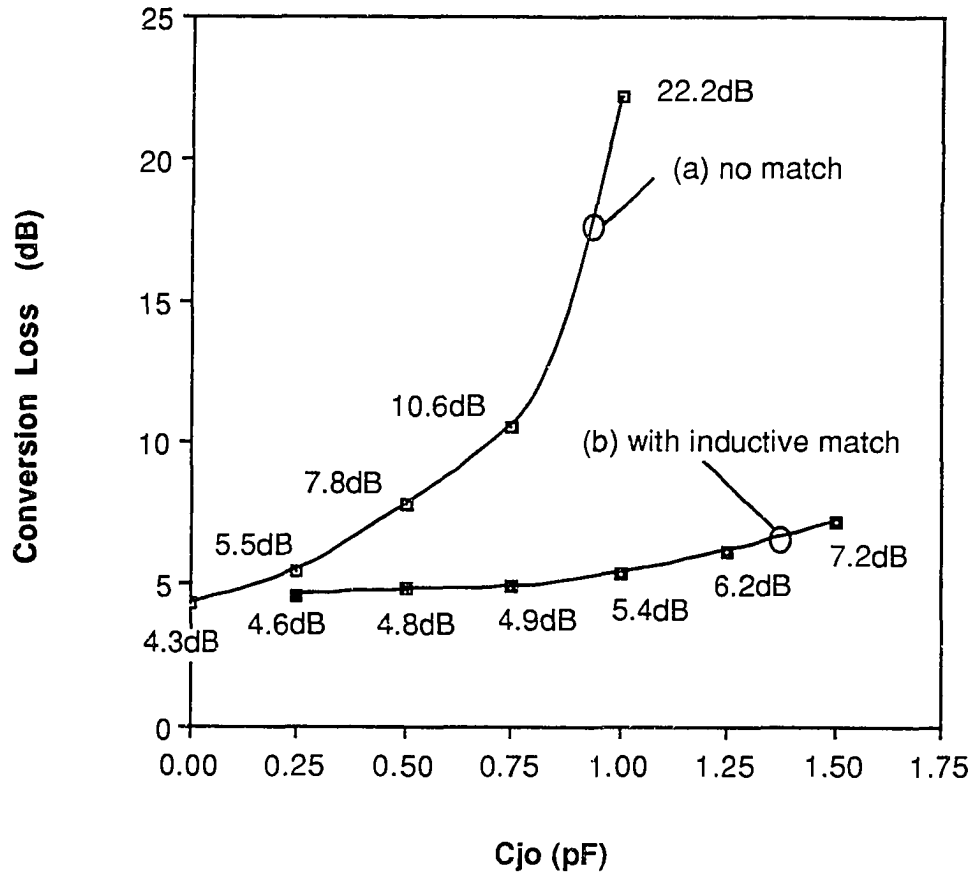


Figure 34: Conversion loss vs. C_{j0}: (a) when no compensation is used; (b) when L_S is optimized for minimum C_L.

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We will now look at the improvement in conversion loss that occurs when the value of the source inductor, L_S, is decreased so that it can be used to resonate out the effect of the barrier capacitance at f_{LO} and thereby match the source to $Z^*_{in}(f_{RF})$ (Refer to Fig. 14; $C_S = 0$.). This has been the approach taken most often in the literature [50,17]; there the effect of the nonlinear barrier capacitance is approximated by replacing it with a constant capacitance equal to C_{j0} or the time averaged value of C_B. As shall be seen in Chapter 5 our design tool can be put to advantage in designing a circuit that utilizes the nonlinearity of the barrier capacitance to improve mixer conversion loss below that of the resistive diode mixer by parametrically pumping the barrier capacitance in the correct phase with respect to the RF source.

The lower curve in Figure 34 shows the improvement in C_L obtained when the value of L_S is optimized to resonate with C_B at f_{LO}. As C_B is varying fourfold over one LO cycle, $L_{S_{opt}}$ must be found by iteration. $L_{S_{opt}}$ has been experimentally found to resonate at f_{LO} with a value of capacitance equal to 0.6 - 0.7 C_{j0}. Conversion loss is then substantially lower than when no compensation is used. For $C_{j0} = 1.0$pF, the 22dB figure for C_L without compensation circuitry drops to 5.4dB, reflecting the fact that a diode with this size of barrier capacitance can be used at 1GHz.

In the lower portion of Table 8 the characteristics of the inductively matched mixer runs are given as C_{j0} is varied from 0 to 1.5 pF. The values of L_S used, the ensuing source impedance, and mixer input impedance are tabulated. Use the appropriate matching structure increases T_{TON} and reduces T_{NL} as expected to generate a lower C_L. $Z_{in}(f_{RF})$ is hardly changed by the addition of the matching inductor. Although the choice of inductor values has been set to optimize C_L, $Z_S(f_{RF})$ falls close to $Z^*_{in}(f_{RF})$.

Conversion loss is a sensitive function of L_S. If L_S is set to resonate with C_{j0} at f_{LO}, the conversion loss improvement is not as substantial: for a barrier capacitance with C_{j0} equal to 0.5, 0.75, and 1.0pF, C_L is then calculated to be 6.5, 8.2, and 10.1dB respectively. These values are 1.7, 3.3, and 4.7dB higher than those obtained when $L_{S_{opt}}$ is used. However, even when the inductive matching is optimized the conversion loss remains higher than that of a purely resistive mixer.

The diode and circuit waveforms of the inductively compensated circuit (when

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Table 8: Performance of the Single Ended Mixer as C_{j0} is Increased

	No Inductive Matching $R_S = 1K,\ R_L = 1K,\ C_{LD} = 2.8pF$						
Run	C_{j0}	L_S	$Z_S(f_{RF})$ $(R_S \parallel L_S)$	$Z_{in}(f_{RF})$	$\frac{T_{NL}}{T_{LO}}$	$\frac{T_{TON}}{T_{LO}}$	C_L
pdiod557	0 pF	1.8μH	995Ω 6°	1.28K -4°	0.06	0.46	4.3 dB
idiod1010	0.25 pF	1.8μH	995Ω 6°	731Ω -60°	0.09	0.36	5.5 dB
idiod1011	0.5 pF	1.8μH	995Ω 6°	444Ω -74°	0.12	0.30	7.8 dB
idiod1012	0.75 pF	1.8μH	995Ω 6°	317Ω -79°	0.17	0.26	10.6 dB
idiod1013	1.0 pF	1.8μH	995Ω 6°	234Ω -84°	0.21	0.21	22.2 dB
	L_S Chosen to Minimize C_L $R_S = 1K,\ R_L = 1K,\ C_{LD} = 2.8pF$						
Run	C_{j0}	$L_{S_{opt}}$	$Z_S(f_{RF})$ $(R_S \parallel L_S)$	$Z_{in}(f_{RF})$	$\frac{T_{NL}}{T_{LO}}$	$\frac{T_{TON}}{T_{LO}}$	C_L
ldiod2362	0.25 pF	0.19μH	745Ω 42°	761Ω -57°	0.08	0.38	4.6 dB
ldiod45	0.5 pF	0.14μH	N.C. †	N.C.	N.C.	N.C.	4.8 dB
ldiod2382	0.75 pF	65.2nH	349Ω 69°	323Ω -77°	0.09	0.31	4.9 dB
ldiod2392	1.0 pF	48.9nH	269Ω 74°	291Ω -79°	0.10	0.30	5.4 dB
ldiod2402	1.25 pF	39.1nH	218Ω 77°	245Ω -81°	0.10	0.29	6.2 dB
ldiod74	1.5 pF	32.6nH	183Ω 79°	211Ω -82°	0.11	0.28	7.2 dB

† Not Calculated.

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the RF and LO are in phase) are shown in Figure 35 for the case when $C_{j0} = 0.25$pF. As shown in Figure 34, setting L_S to resonate with C_B has caused C_L to drop from 5.5dB to 4.6dB.

The first graph depicts $V_{out}(t)$ plotted for one cycle of the IF. In the second graph, the currents in the diode, in R_S, and L_S are plotted along with the total source current. Comparing I_{d_r} in the circuit with that in the uncompensated circuit, shown in Figure 32, the resistive current pulse is wider. The 'ON' time has been increased from $0.36\,T_{LO}$ to $0.38\,T_{LO}$. The last plot shows I_{d_c}, C_B, and Q_{C_B}. The waveforms indicate the diode is turning 'ON' earlier in the LO cycle as a consequence of the inductive match.

In Figure 36 the energy stored in the circuit and in the differential RF currents are plotted. The first graph shows the energy stored in the barrier capacitor, E_{C_B}, and that stored in L_S, E_{L_S}. E_{C_B} and E_{L_S} are calculated as follows:

$$E_{C_B}(t) = \frac{1}{2} \cdot C_B(t) \cdot V_j^2(t) \tag{29}$$

$$E_{L_S}(t) = \frac{1}{2} \cdot L_S \cdot {I_{L_S}}^2(t) \tag{30}$$

One can see the energy alternatively stored in the barrier capacitance and in the matching inductor, typical of a driven resonant circuit. In a parallel RLC circuit energy is traded from inductor to capacitor four times in one LO cycle. The mixer looks similar to a resonant circuit when the diode is 'OFF'. C_{LD} serves to short the diode to ground at f_{LO} and the two reactive elements in the circuit are L_S and C_B. The moment the diode turns 'ON', the phase relationship between I_{L_S} and V_j shifts, and, the energy storage pattern no longer resembles that of a resonant circuit.

The second graph gives the energy in C_B and L_S attributed solely to the RF currents. To calculate this, the differential currents in all reactive elements is found as discussed for Figure 33, these currents, caused by the RF source, are used to find the energy stored in C_B and L_S due solely to the RF source. In this manner, the mixer designer can examine the flow of RF energy through the circuit and the interaction of circuit and diode can be studied. Although these energy patterns can not be observed

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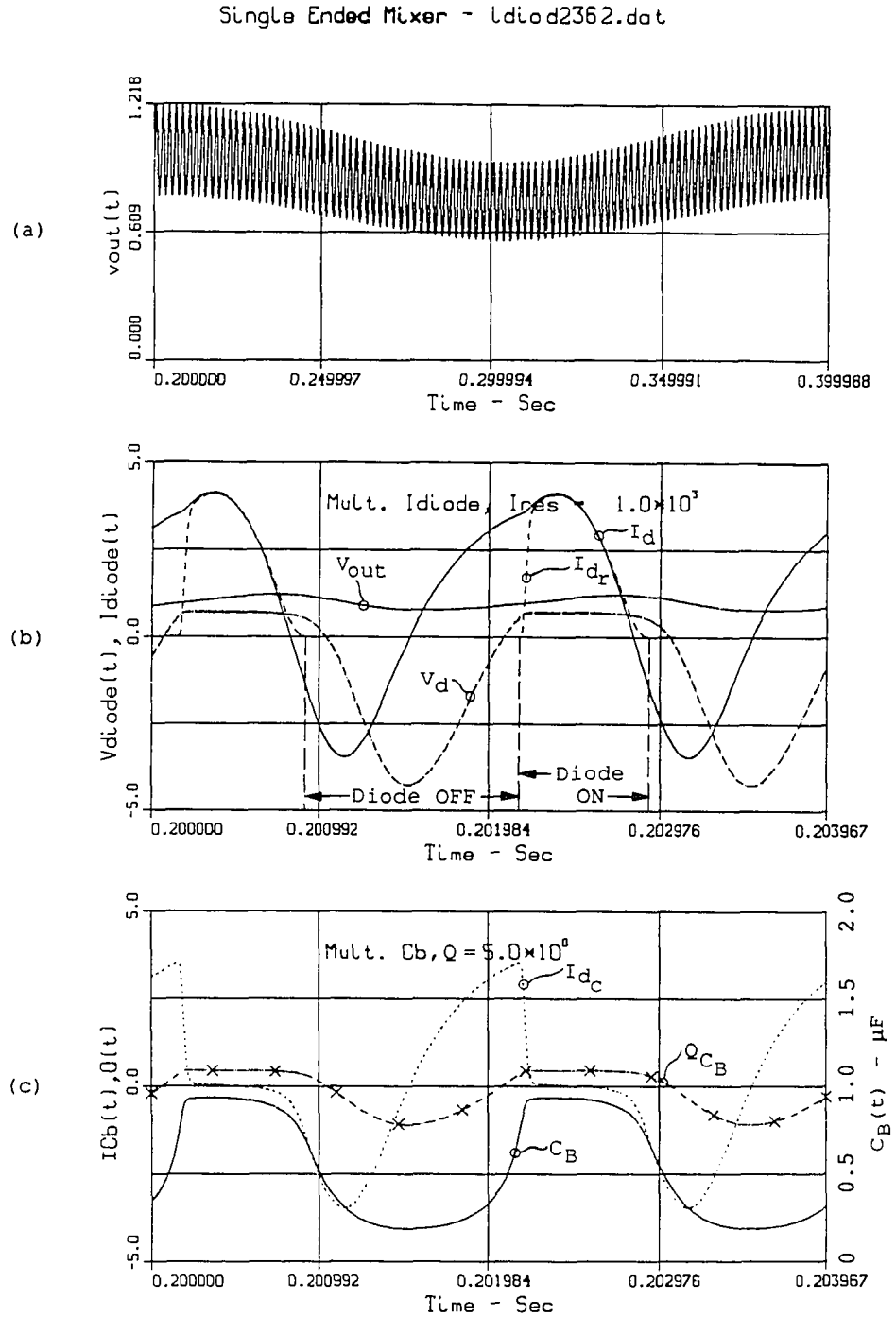


Figure 35: Circuit waveforms in the inductively matched 'RM' mixer with $C_{j0} = 0.25$pF.

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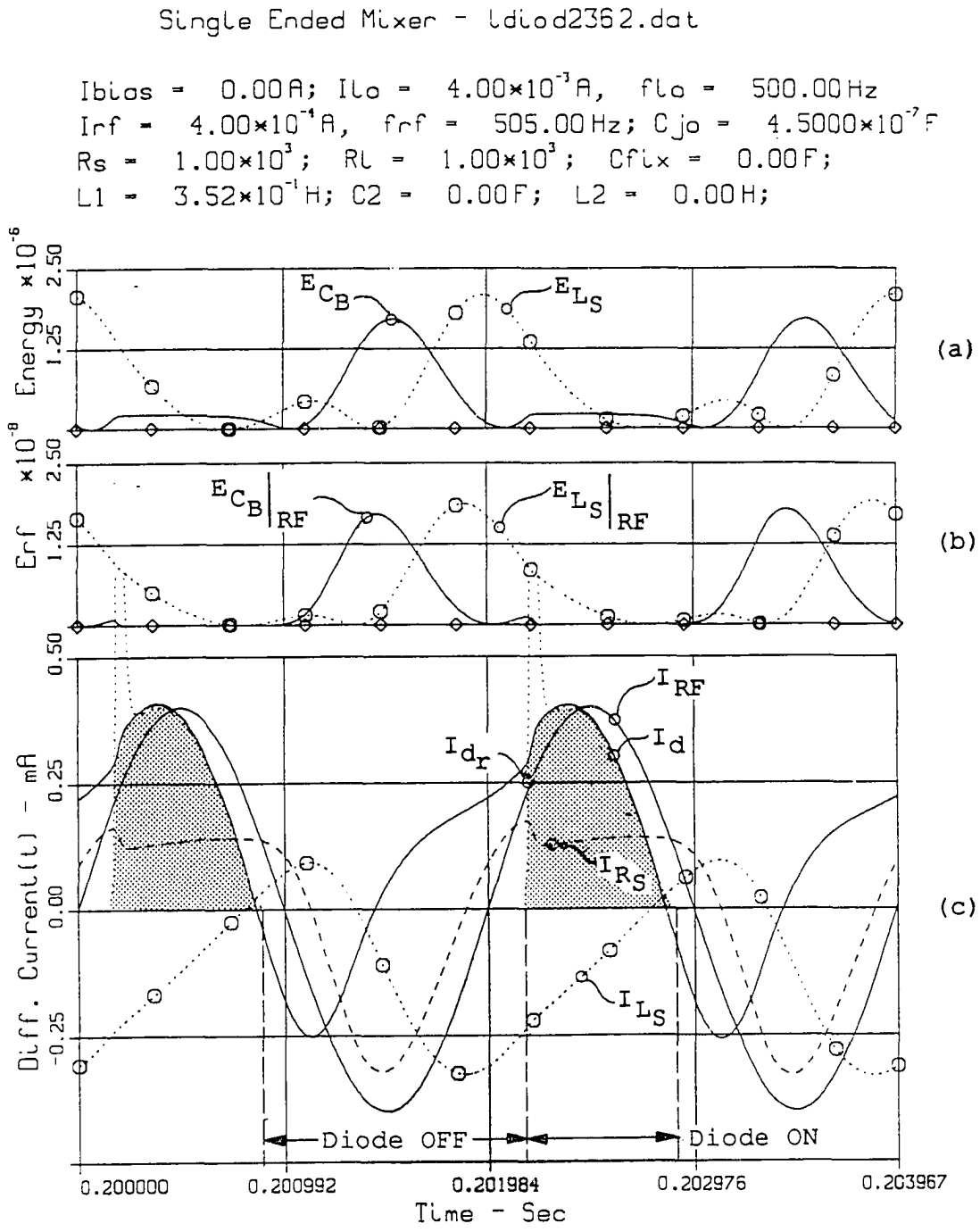


Figure 36: Energy waveforms and differential currents in the inductively matched 'RM' mixer with $C_{j0} = 0.25$pF.

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in a single ended mixer circuit, they are measurable in a balanced mixer as the RF currents are separated from the LO currents at certain points in the circuit.

Lastly the third graph shows the differential currents in the diode, L_S, and, R_S as well as the RF source current.

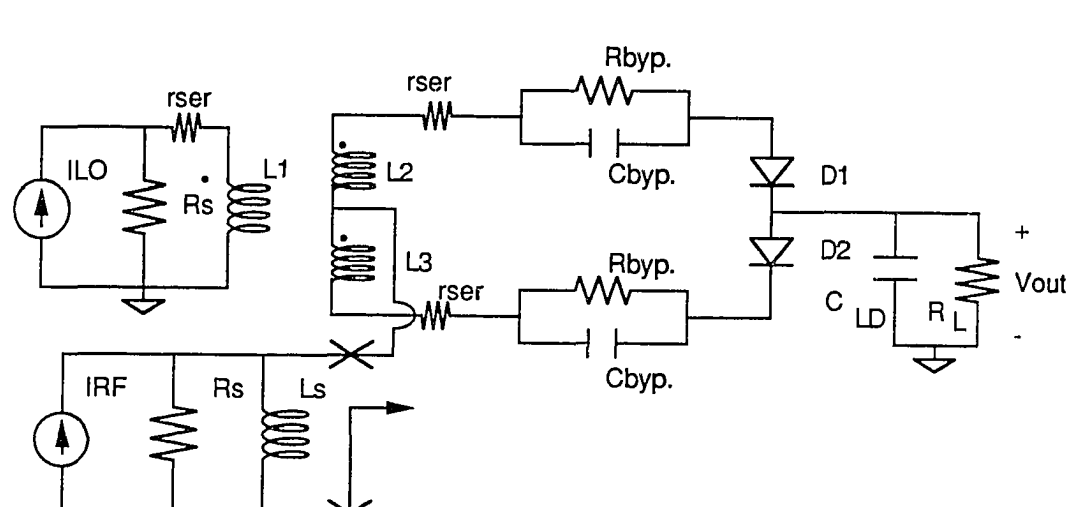
The conversion losses plotted in Figure 34 when inductive matching is used to compensate for the barrier capacitance are not necessarily the lowest conversion loss that can be achieved if R_L and R_S were varied. They are the optimum achievable when L_S, only, is varied. When R_L is optimized to match to $Z_{out}(f_{IF})$, the conversion loss for $C_{j0} = 0.25$pF drops 0.2dB to 4.4dB, for $C_{j0} = 1.0$pF it drops 0.15dB to 5.25dB, and for $C_{j0} = 1.5$pF it drops 0.5dB to 6.7dB. However matching Z_L to $Z^*_{out}(f_{IF})$ and iteratively searching for $Z_{S_{opt}}$ still produces mixer circuits whose C_L is higher than that of the purely resistive circuit.

4.3 Balanced Mixer Design

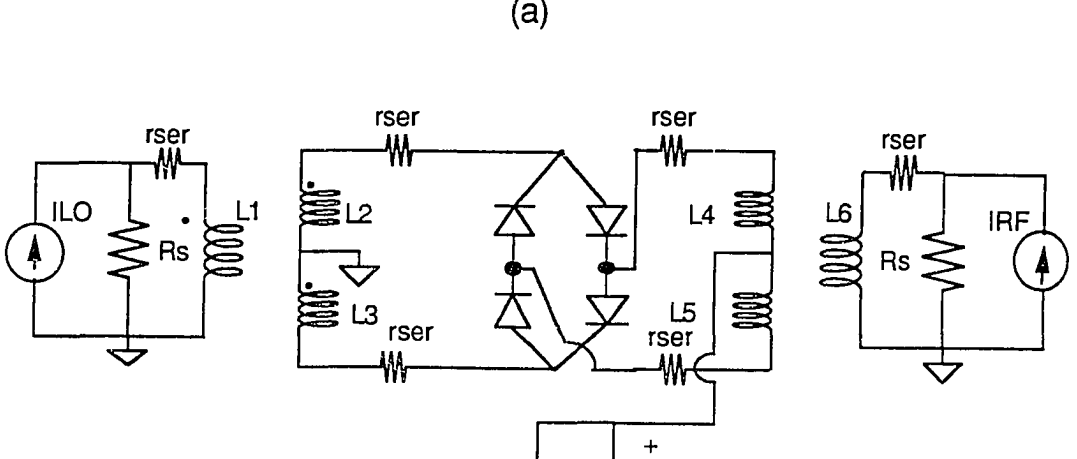
Several balanced mixer realizations are shown in Figure 37. Balanced mixers are employed preferentially over single ended mixers for several reasons: (1) the output port is isolated from the LO source and its harmonics and hence contains less power at DC or any LO harmonics; (2) the amplitude modulated (AM) component of the LO noise is cancelled internally by the balanced circuitry resulting in less noise power in the output signal. However, the use of balanced mixers has two drawbacks: (1) additional circuit elements and active components are required; and (2) a slight degradation in C_L may be incurred due to the losses introduced in the RF signal path by the additional circuitry and to the use of non-identical diodes.

Balanced mixer circuits can be easily modelled for analysis with the design tool described above. Analysis of these circuits can reveal the effects of imperfect balance or dissimilar diodes on mixer performance. In this section the circuit model for a single balanced mixer is first discussed, the corresponding SPICE circuit is then constructed, and the use of the design tool detailed. Differences between the graphical and quantitative output generated for the single ended mixer and single balanced mixer are explained. The optimization criteria outlined in Section 3.3.5 remains

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(a)



(b)

Figure 37: Balanced mixers: (a) single balanced; (b) double balanced.

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unchanged. This is demonstrated by the ensuing analysis, first, of balanced mixers with purely resistive diodes and, subsequently, of balanced mixers with capacitive diodes.

4.3.1 Circuit Description

The single balanced circuit used in the SPICE simulation is shown in Figure 37(a). A double balanced version of this circuit is shown in Fig. 37(b). Double balanced circuits are commonly employed mixer circuits due to their very low VSWRs. A three-winding transformer is used to couple the LO and RF power into the diode as is typical for UHF and microwave mixers.[6] The LO is fed across the primary transformer of the balanced circuit: the diodes, D_1 and D_2, are turned on or off in unison by the LO. When the diode are 'ON', the LO current flows around the loop formed by the diodes, and, if the two diodes are a matched pair, the center tap of the loop, which is the IF port, is at ground. When the diodes are 'OFF', the center tap voltage is floating. Thus the LO is completely isolated from the IF port if the diode are perfectly matched; in practice, 20dB of isolation is typically achieved.

The RF is fed into the common center tap of the secondaries. The small signal circuit, seen from the RF and IF point-of-view, of the single balanced mixer circuit to be analyzed, is drawn in Figure 38. When the diodes are 'ON', the two branches of the secondary circuit appear in parallel. From the RF point-of-view the diodes appear grounded through the load. From the IF perspective, at the output terminals, the diodes appear grounded through the parallel combination of R_S and L_S. In a purely resistive mixer L_S and C_S are identical to those used for a single ended mixer. When the diodes are turned 'OFF' by the negative-going LO, the RF source is loaded R_S and L_S. When the diodes are turned 'ON' by the positive-going LO, the RF signal flows through the diodes to the load. This RF signal travelling in both inductors will not induce a voltage accross the primary if the inductors and their mutual coupling coefficients in the secondary circuit are identical. Infinite isolation would exist from

[6]New versions of SPICE, such as microwave SPICE, support the use of building blocks such as couplers and transmission lines. Using these programs higher frequency or more complex mixers could be analyzed such as image reject or image recovery mixers.

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the RF to the LO port. In practice this is not possible due to non-ideal transformers and to the fact that a positive going RF current in both diodes increases the voltage drop across D_1 but reduces it slightly across D_2 hence making the voltages inequal accross the two secondaries. Typically 20dB isolation is possible between the RF signal and the LO port. No isolation occurs between the RF and IF port. Should isolation from the RF to the IF port be desired, a double balanced mixer is used.

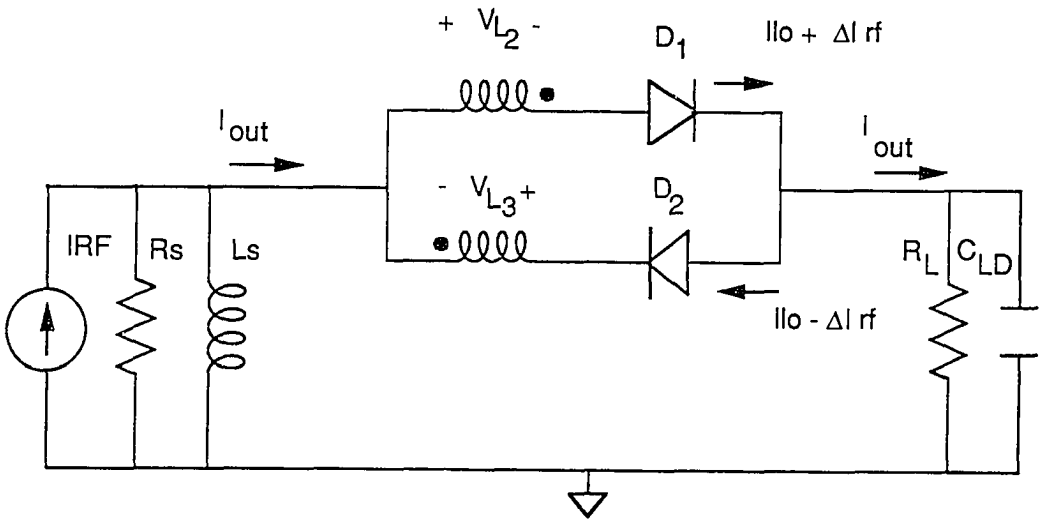


Figure 38: Small signal model of single balanced mixer circuit.

4.3.2 SPICE Model

The SPICE input file and the corresponding circuit are shown in Figure 39. The file is similar to the single ended mixer run file shown in Fig. 14(b), differing principally by the addition of a transformer. The transformer is modelled by a primary, L_1, and two secondaries, L_2 and L_3. Each has a 10Ω resistance, r_L, in series with the windings to model resistive losses in the wire. A capacitor could be set in parallel with each transformer coil to model the stray capacitance in each of the coils; it has not been included in these runs so as not to obfuscate mixer operation by these secondary effects. The values of coil inductance and coupling coefficient have been determined

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through modelling the practical two-winding transformer by non-coupled inductors and ideal transformers.

Transformer Model

Choice of L_1, L_2, L_3, and k. It is well known that a practical transformer, ie. a set of coupled inductors, can be modelled by two non-coupled inductors and one ideal transformer [14]. The circuit shown in Figure 40(a) consisting of two mutually coupled inductors, L_1 and L_2, with coupling coefficient k_{12} can be replaced by the circuit shown in Fig. 40(b) where L_a and L_b are non-coupled inductors and n_1 and n_2 are the number of turns on the primary and secondary, respectively, of an ideal transformer. The correspondance between the two circuits can be found by equating their inductance matrices. The latter relates the magnetic flux, $\vec{\phi}$, and the current, $\vec{I}$, into the two port:

$$\vec{\phi} = \mathbf{L}\,\vec{I}.$$

The inductance matrix, $\mathbf{L}$, for the circuit in Fig. 40(a)is given by

$$\mathbf{L} = \begin{bmatrix} L_1 & k_{12}\sqrt{L_1 L_2} \\ k_{12}\sqrt{L_1 L_2} & L_2 \end{bmatrix}$$

The inductance matrix for the circuit in Fig. 40(b) can be written as

$$\mathbf{L} = \begin{bmatrix} L_a + L_b & \frac{n_2}{n_1} L_b \\ \frac{n_2}{n_1} L_b & \left(\frac{n_2}{n_1}\right)^2 L_b \end{bmatrix},$$

where $V_1' = V_2 \frac{n_1}{n_2}$ and $I_1' = -I_2 \frac{n_2}{n_1}$. The values of L_a, L_b, n_1 and n_2 can be found in terms of L_1, L_2 and k_{12} by equating the two matrices. Equivalence implies:

$$k_{12} = \frac{1}{\sqrt{1 + \frac{L_a}{L_b}}}, \tag{31}$$

$$L_1 = L_a + L_b, \tag{32}$$

$$L_2 = \left(\frac{n_2}{n_1}\right)^2 L_b. \tag{33}$$

The input impedance of the practical transformer can be found in Figure 41(b) to be:

$$Z_{in}(\omega) = j\omega L_a + \left(j\omega L_b \parallel \left(\frac{n_1}{n_2}\right)^2 R_L\right).$$

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```
SINGLE BALANCED MIXER
ILO 0 18 SIN(0 10M 900MHz)
VIM0 18 20
R1 20 0 1000
VIM1 20 15
RL1 15 10 10.0
L1 10 0 5.5UH
L2 30 40 5.5UH
L3 40 45 5.5UH
K1 L1 L2 1.0
K2 L1 L3 1.0
K3 L2 L3 1.0
RL2 30 31 10.0
VBAT1 32 31 -2.0
VIM2 32 35
VIM5 35 37
D1 37 70 DIODE1
RPD1 35 70 5MEG
VBAT2 45 46 -2.0
RL3 46 47 10.0
VIM3 47 49
VIM6 49 48
D2 70 48 DIODE1
RPD2 49 70 5MEG
VIM9 70 72
RL 72 0 1000
CL 72 0 2.8PF
VIM8 42 40
R3 42 0 1000
LS 42 0 1.8UH
VIM7 50 42
IRF 0 50 SIN(0 .4M 909MHz)
 .MODEL DIODE1 D RS=10.0 IS=1.0E-14 N=1.0 CJO=.001PF VJ=.9 BV=20
 .OPTIONS ACCT OPTS ITL3=10 LVLTIM=1 LIMPTS=20000 ITL5=40000
 .TRAN 12.2070327.13PS .222US .111US
 .PRINT TRAN V(70) I(VIM5) V(37,70) I(VIM8) V(40) V(0) V(0) V(0)
* Maximum parameters printed in one row is 8.
 .END
```

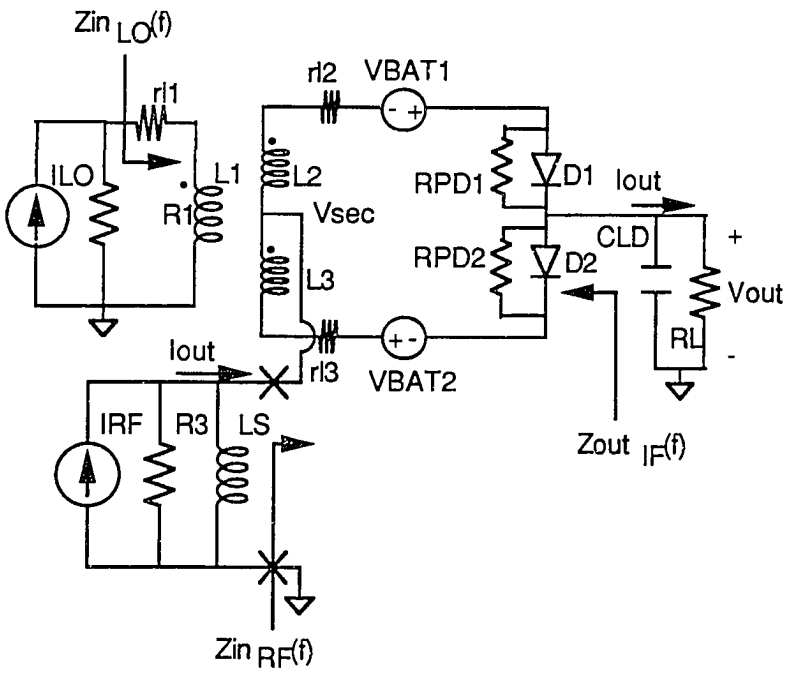


Figure 39: Single balanced mixer: circuit diagram and corresponding SPICE run file.

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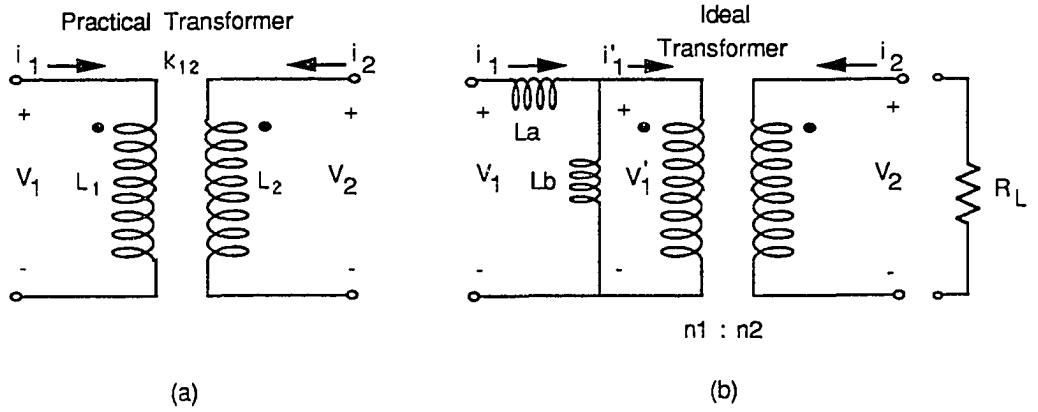


Figure 40: Practical transformer, shown in (a), modelled by non-coupled inductors and an ideal transformer in (b).

To maximize power flow to the load at the output port from the source at a frequency ω, the model in Figure 41(b) allows us to see that L_a should be minimized and L_b chosen so that its impedance is far greater than $(n_1/n_2)^2 R_L$. The values for L_1, L_2, and k_{12} can then be calculated from equations 31, 32, and 33.

Similarly, the transformer used in the balanced mixer in Figure 37 can be modelled by non-coupled inductors and ideal transformers. In Figure 41(a) the practical transformer is shown and in Figure 41(b) its modelled counterpart is given. The inductance matrix, **L**, for the first circuit can be expressed as

$$\mathbf{L} = \begin{bmatrix} L_1 & k_{12}\sqrt{L_1 L_2} & k_{13}\sqrt{L_1 L_3} \\ k_{12}\sqrt{L_1 L_2} & L_2 & k_{23}\sqrt{L_2 L_3} \\ k_{13}\sqrt{L_1 L_3} & k_{23}\sqrt{L_2 L_3} & L_3 \end{bmatrix} \tag{34}$$

and for the latter circuit as

$$\mathbf{L} = \begin{bmatrix} L_b & \frac{n_2}{n_1} L_b & \frac{n_3}{n_1} L_b \\ \frac{n_2}{n_1} L_b & \left(\frac{n_2}{n_1}\right)^2 L_b & \frac{n_2}{n_1}\frac{n_3}{n_1} L_b \\ \frac{n_3}{n_1} L_b & \frac{n_2}{n_1}\frac{n_3}{n_1} L_b & \left(\frac{n_2}{n_1}\right)^2 L_b \end{bmatrix}. \tag{35}$$

The equivalence between circuits holds only for the case $k_{12} = k_{13} = k_{23}$ as the coupling coefficient value is determined by L_a and L_b shown in equation 31. The

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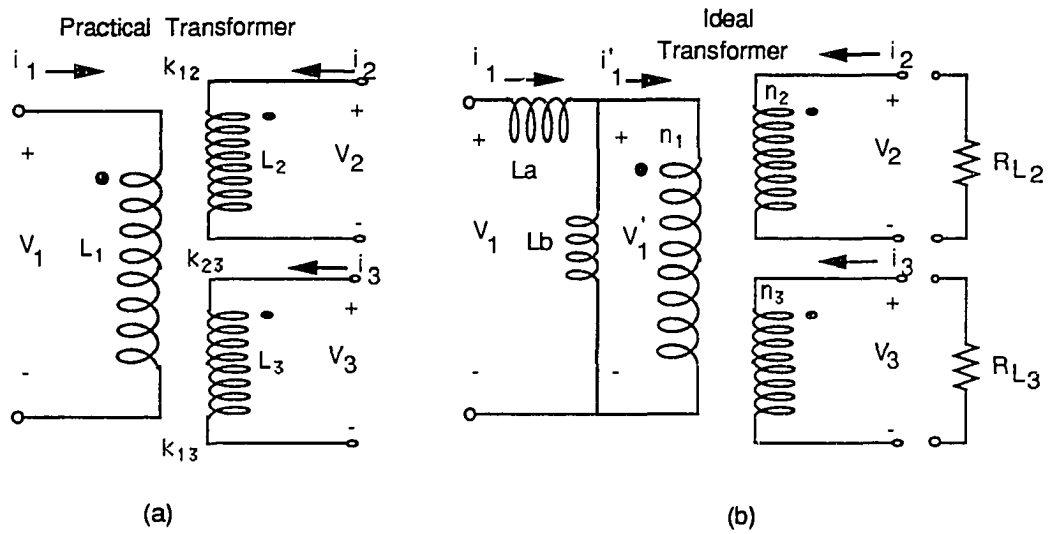


Figure 41: Practical three winding transformer, shown in (a), modelled by two non-coupled inductors and three ideal transformers in (b).

input impedance can be written as

$$Z_{in}(\omega) = j\omega L_a + \left(j\omega L_b \parallel \frac{\left(\frac{n_1}{n_2}\right)^2 R_{L_2} R_{L_3}}{R_{L_3} + \left(\frac{n_3}{n_2}\right)^2 R_{L_2}} \right).$$

The matrix in equation 34 can be simplified to represent a transformer with two secondaries which share a common node such as used in balanced mixer design. Equation 34 is then reduced to

$$\mathbf{L_{Bal}} = \begin{bmatrix} L_1 & k_{12}\sqrt{L_1 L_2} + k_{13}\sqrt{L_1 L_3} \\ k_{12}\sqrt{L_1 L_2} + k_{13}\sqrt{L_1 L_3} & L_{series} \end{bmatrix} \tag{36}$$

where L_{series} is simply the series equivalent of the of the coupled inductors. For the transformer design idealized in Figure 39 where the mutual inductance is positive, L_{series} can be written as

$$L_{series} = L_2 + L_3 + 2k_{23}\sqrt{L_2 L_3}.$$

This transformer can be modelled (for $k_{12} = k_{13} = k_{23}$) by non-coupled inductors and an ideal transformer by reducing equation 35. This is equivalent to replacing

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the two secondaries of the ideal transformer by a coil with $n_2 + n_3$ windings. The inductance matrix for the two port realization of the balanced transformer is given by

$$\mathbf{L_{Bal'}} = \begin{bmatrix} L_a + L_b & \left(\frac{n_2+n_3}{n_1}\right) L_b \\ \left(\frac{n_2+n_3}{n_1}\right) L_b & \left(\frac{n_2+n_3}{n_1}\right)^2 L_b \end{bmatrix}. \tag{37}$$

The input impedance of the balanced transformer as seen from the LO port can then be written as

$$Z_{in_{LO}}(\omega) = j\omega L_a + \left(j\omega L_b \parallel \left(\frac{n_1}{n_2+n_3}\right)^2 R_L\right),$$

for $R_L = R_{L_2} + R_{L_3}$.

The benefit of modelling the balanced transformer by the circuit in Figure 40(b) is that the interaction of L_1, L_2, L_3, and k can be better understood from the simpler transformer model and their values can then be chosen to optimize the circuit's performance. Again, the following condition should be met to maximize the power transfered to the load: $L_a \rightarrow 0$ and $|Z(L_b)| \gg \left(\frac{n_1}{n_2+n_3}\right)^2 R_L$ at f_{LO}. Choosing $n_1 = n_2 = n_3$ and letting $L_a = 0$, we find by equating equations 36 and 37 that

$$\begin{aligned} k &= 1 \\ L_1 &= L_2 = L_3 = L_b. \end{aligned}$$

Considering the highest mixer output impedance attainable to be 10K,

$$L_b \gg \begin{cases} 4\text{H} & \text{for 500Hz operation} \\ 2\mu\text{H} & \text{for 900MHz operation.} \end{cases}$$

Effect of RF current in transformer secondary on LO circuit. If the secondaries have equal inductance and if $k_{13} = k_{12}$ then the effect of the RF curent flowing in L_2 will be to cause a current in the primary of equal magnitude and opposite direction to the current generated by the RF current flowing in L_3. Hence there will be no effect of RF current in L_2 and L_3 on L_1.

Effect of secondaries on RF circuit. As shown in Figure 38 the RF circuit sees the series combination of one of the secondary inductors and one diode in parallel with

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the other secondary inductor and diode. The impedance presented by the parallel combination of the two mutally coupled inductors, each in series with a nonlinear element, is difficult to calculate. However, the parallel combination of two identical, mutually coupled inductors can be written as

$$L_{parallel} = \frac{L_2 L_3 (1 - k_{23}^2)}{L_2 + L_3 - 2k_{23} L_2 L_3}.$$

For $k_{23} = 1$ as modelled in the SPICE run, $L_{parallel} = 0$ because the magnetic flux created by both RF currents runs in the same direction for both secondaries. Therefore it can be simplistically said that, when the diodes are 'ON', the RF circuit sees only the load impedance ($R_L \parallel C_{LD}$), and, when the diodes are 'OFF', the RF circuit is loaded by the source impedance ($R_S \parallel L_S$).

To find the effect of the transformer on both the RF and LO circuits, $Z_{in}(f)$ can be calculated acording to equation 15 from the SPICE run results. The reference planes for $Z_{in}(f)$ at both ports is shown in Figure 39.

Bias Model

Several ways of applying bias in a balanced mixer are shown in Figure 42(a) and (b). Fig. 42(a) depicts the most common way of applying bias; Fig. 42(b) shows a method which takes advantage of the rectification of the LO current in the diode, $\langle I_d \rangle$, to obtain a voltage drop in a bias resistor. This bias resistor is bypassed at the RF by a capacitor. SPICE runs simulate the application of bias by modelling either the circuit in Figure 42(b) or that in Figure 42(c). In fact, the latter is the method used in the simulation run specified in Fig. 39.

The balanced circuit causes a different relationship to exist between circuit elements than in the single ended case and requires special consideration. Summing the voltage around one of the secondary loops, the following relationship arises:

$$\langle V_{L_2} \rangle = \langle V_{r_{L_2}} \rangle + V_{bias} + \langle V_d \rangle + \langle V_{out} \rangle$$

where $\langle\rangle$ refers to the time averaged value over one IF cycle and,

$$\begin{aligned} \langle V_{r_{L_2}} \rangle &= \langle I_d \rangle \cdot r_{L_2} \\ &\rangle\ 0 \end{aligned}$$

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As $\langle V_{out} \rangle$ is the output of a balanced circuit,

$$\langle V_{out} \rangle = 0;$$

similarily $\langle V_{L_2} \rangle$ represents the DC value across an inductor, hence

$$\langle V_{L_2} \rangle = 0.$$

Therefore,

$$V_{bias} = -\langle V_{r_{L_2}} \rangle - \langle V_d \rangle. \tag{38}$$

From Figure 16 V_d is seen to vary from 0.7V to several volts negative depending on the LO drive. $\langle V_d \rangle$ then varies from about -0.5V to -2.0V. In order to bias the diodes in the balanced circuit a similar fashion to those in a single ended circuit a bias voltage must be applied. The level of bias voltage sets the average value of V_d and hence the 'ON' time of both diodes. This will be illustrated in Section 4.3.4.

4.3.3 Application of Design Tool

The design tool, as described in Section 3.3, can be used to analyze the balanced circuits that have been simulated with SPICE. Although the graphical programs shown in the flowchart in Figure 12 must be modified to accomodate the greater number of variables to be plotted, no change in the quantitative mixer analysis is necessary. The Hartley transform is used, as before, to generate the Fourier components of the output voltage and the power delivered to the load at f_{IF} is compared to the available RF input power to find the mixer's conversion loss, as in eqn. 13. The differences in the output of the design tool for single ended and balanced mixer optimization are discussed below.

In Figure 43(a), a plot of V_{out} for one cycle of the IF is shown for the circuit specified in Fig. 39. Immediately visible is the lack of DC voltage and the reduced level of LO feedthrough at the output. This can be verified by examining the spectrum of V_{out} shown in Fig. 43(b). The spectrum was calculated from the Hartley transform of $V_{out}(t)$ as in the single ended case. It is used to evaluate the quantitative performance of the mixer. As in the single ended mixer runs, the simulations have been performed

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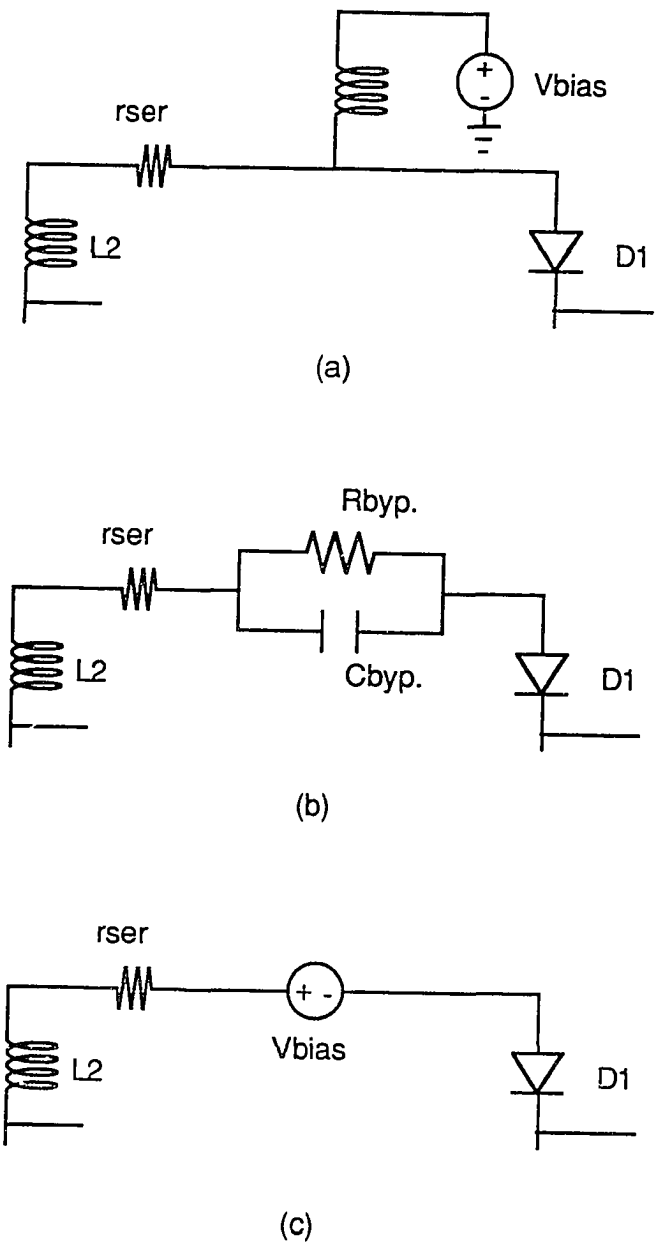


Figure 42: Application of bias in a balanced mixer: (a) through RF choke, (b) using rectified LO current, (c) with a series voltage source.

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with f_{RF} = 909 MHz, f_{LO} = 900 MHz, and, f_{IF} = 9 MHz (or f_{RF} = 505 Hz, f_{LO} = 500 Hz, and, f_{IF} = 5 Hz with all frequency sensitive circuit and diode elements scaled appropriately [7]) to emulate the mixer performance of a direct downconversion receiver. Such receivers operate with the RF and LO frequencies separated by half the RF bandwidth, eg. for transmission of an analog audio signal with 3.1 KHz bandwidth f_{RF} = 909 MHz, f_{LO} = 908.99845 MHz and f_{IF} = 1.55 KHz.

Figure 44 shows four snapshots of the diode and RF waveform when the RF and LO are in-phase, 90°, 180° and 270° out-of-phase. Each plot gives the time variation of five parameters, I_d, V_d, I_{out}, V_{sec} and V_{out}. The current and voltage of the diode D_1 are plotted with a common zero line; it is marked on the left hand side of the graph. One division beneath this zero is the zero line for I_{out}, V_{out}, and V_{sec}; it is marked on the right hand side of the graph. I_{out} represents the RF current flowing into the common secondary node between L_2 and L_3; it is also the current flowing into the output load. V_{sec} is the voltage at this common secondary node. V_{out} is defined, as in the single ended mixer case, as the output voltage at the load, ie. the parallel combination of R_L and C_{LD}. These parameters are shown in the circuit shown in Figure 39.

A balanced mixer possesses certain nodes such as the common secondary node or the output node where the LO voltage is nearly zero. If the circuit is truly balanced, then the LO contribution to the voltage at these nodes is zero. Thus the action of the RF voltage on the circuit is easily visible and the small signal currents and voltages in the RF circuit can be examined without their being swamped by the far greater LO signal. Figure 44 can be used to study the pattern of output current at the four phase relations of the RF and LO. In fact the pattern in I_{out} can be seen to be very similar to that calculated for the ideal switch shown in Figure 21(b); the area underneath I_{out} when the diode is 'ON' has been highlighted to stress this similarity. When the LO and RF are in phase, the positive going RF pulse drives the diode load and appears as the load current. V_{out} is positive and reaches its largest value during this cycle of

[7]The equivalence of frequency scaled circuits and diodes has been confirmed with this design tool by comparing the quantitative performance of scaled mixer circuits and verifying that identical results are obtained. This is discussed in Section 3.3.2.

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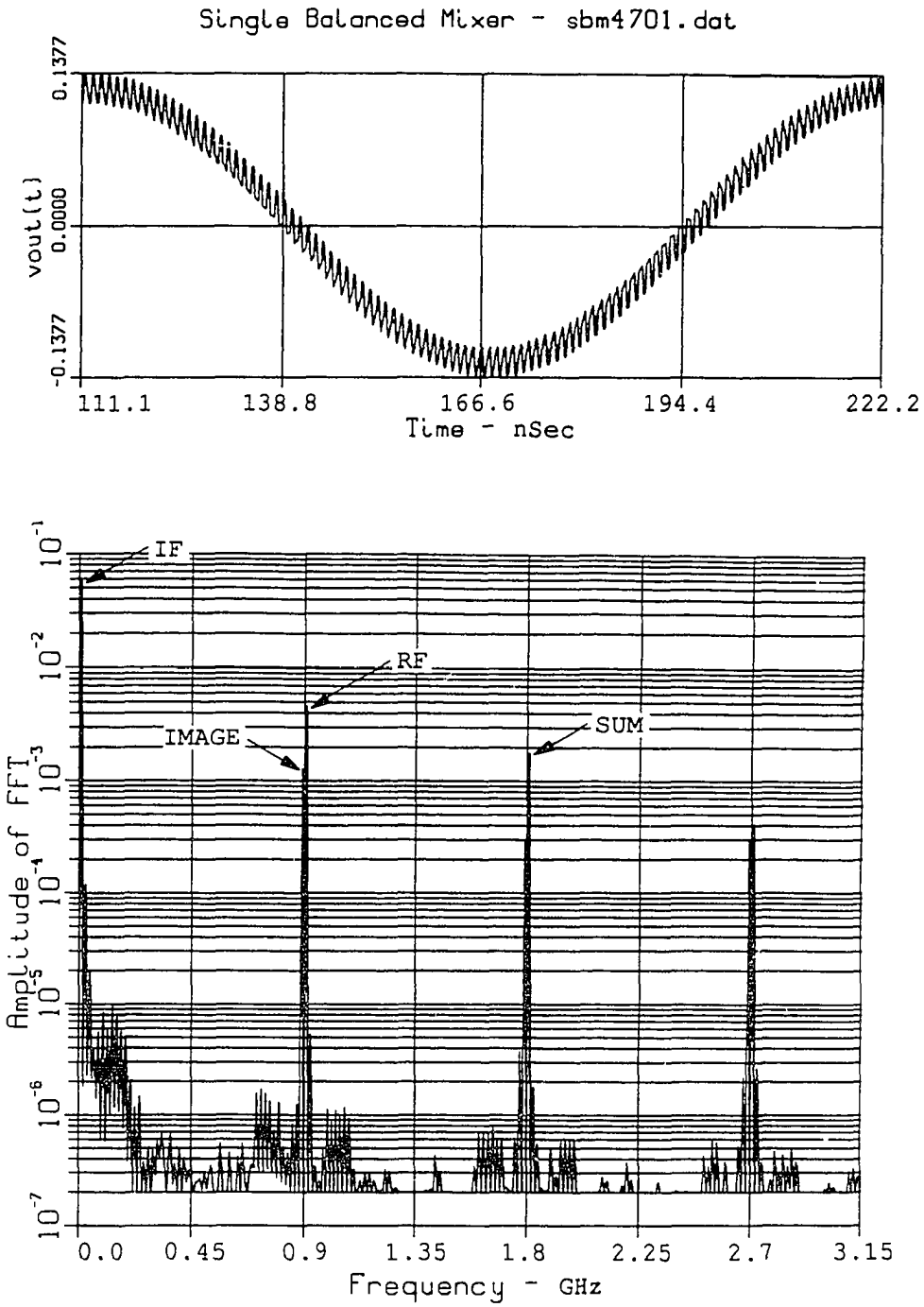


Figure 43: Balanced mixer output voltage: (a) $V_{out}(t)$; (b) $V_{out}(f)$.

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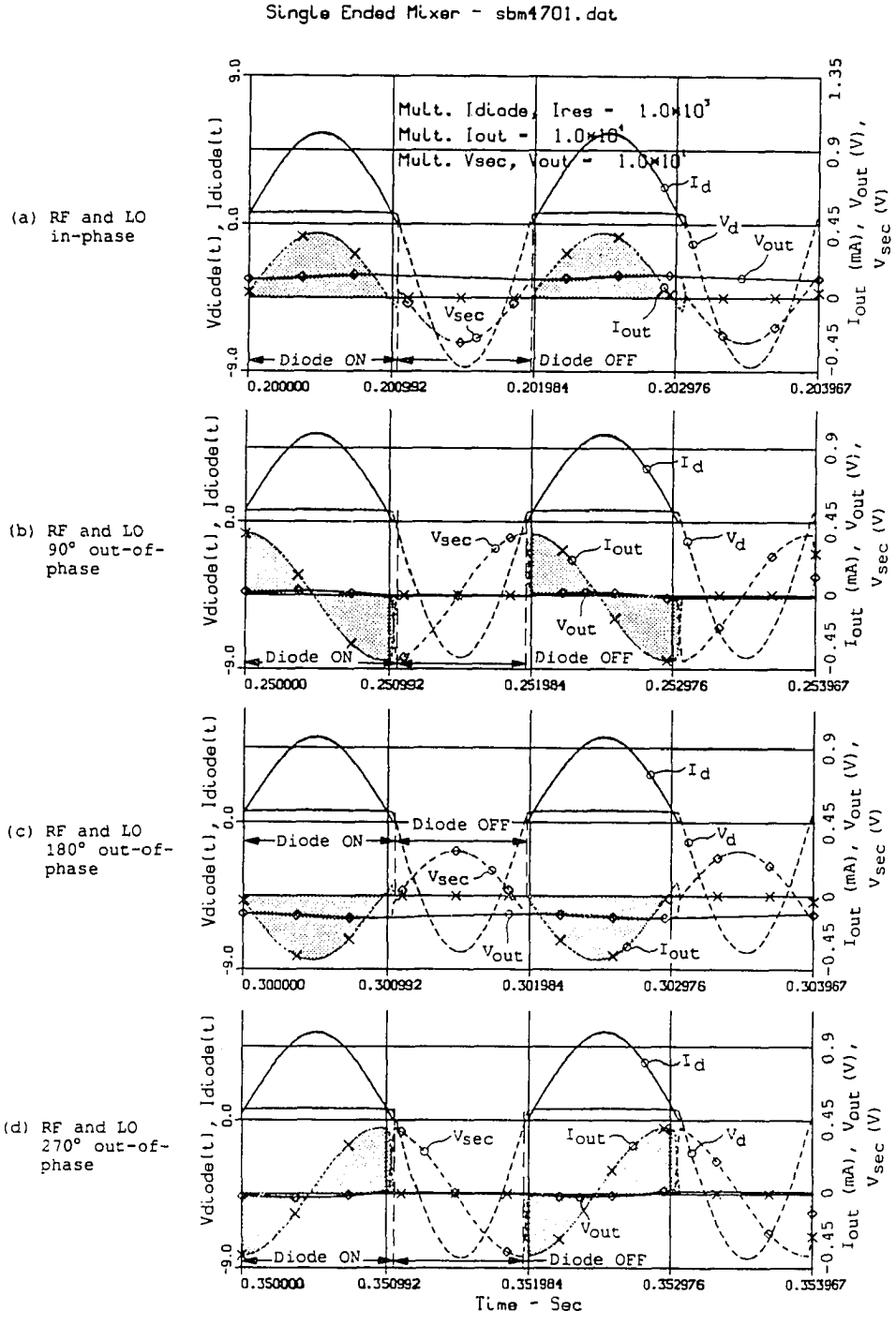


Figure 44: Balanced mixer waveforms for the 'RM' mixer.

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the LO. The RF voltage at V_{sec} is in phase with V_d. It clips when the diodes turn 'ON' and varies sinusoidally when they are 'OFF'. When the LO and RF are 90° out-of-phase the diode remains 'ON' — as V_d is held above zero by the LO voltage — while the RF voltage changes sign, and, again V_{sec} is clipped by V_{out}. The RF current flows into and out of the load during one LO cycle, hence $\langle V_{out} \rangle$ is zero. When the RF and LO are 180° and 270° out-of-phase the patterns repeat themselves although the sign of the output current is reversed. When the RF and LO are out-of-phase the entire negative flowing RF current appears at the load and $\langle V_{out} \rangle$ is driven to its most negative value. The ability to see the RF currents so precisely and to study their path at different moments in the circuit is one of the best characteristics of time domain analysis. It is especially useful for designing complex RF matching circuits, such as those necesary for achieving low C_L when barrier capacitance is included in the diode model.

It is interesting to compare the pattern of RF current in the balanced mixer as the phase difference between the RF and LO varies from 0° to 270° with that obtained in the single-ended mixer. For this purpose, Figure 44 should be compared to Figure 18. In Figure 18, the small-signal current has been calculated by subtracting the total current in the diode at T_3, when the RF and LO are in phase. In this way, the effect of DC currents in the diode can be removed so that only the small-signal current in the diode is visible. In a balanced mixer, when both arms of the mixer are identical as in our simulation, I_{out} and V_{out} possess no DC components and the behavior of the small-signal signals can be easily seen. As in the single ended mixer design case, the mixer performance at f_{IF} can be qualitatively found from the pattern of the small-signal current I_{out}.

First, the diode 'ON' time can be found from Figure 44 – it is expected that C_L decreases as T_{TON}/T_{LO} approaches 0.5 for mixer design with purely resistive diodes. Second, $V_{out}(DC)$, $V_{out}(IF)$ and mixer conversion loss can be calculated from the average output current per LO cycle, I_{out}, taken at T_1, T_2, T_3, and T_4. Following the discussion in Section 3.3.3, the parameters can be written as:

$$V_{out}(DC) = \frac{\langle I_{out}(T_1) \rangle + \langle I_{out}(T_3) \rangle}{2} R_L \qquad (39)$$

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$$V_{out}(IF) = \frac{\langle I_{out}(T_1)\rangle - \langle I_{out}(T_3)\rangle}{2} R_L \quad (40)$$

$$C_L = \frac{I_{RF}^2 R_S R_L}{4V_{out}^2(IF)}. \quad (41)$$

In Figure 44,

$$\langle I_{out}(T_1)\rangle = -\langle I_{out}(T_3)\rangle = 124\mu A \quad \text{and}$$
$$\langle I_{out}(T_2)\rangle = -\langle I_{out}(T_4)\rangle = 15.6\mu A$$

leading to

$$V_{out}(DC) = 0$$

as expected for a well matched balanced mixer. $V_{out}(IF)$ is found to be 124mV which compares well to the value, 123.8mV, calculated from the Fourier transform of $V_{out}(t)$.

4.3.4 Balanced Mixer Performance - Diodes with Barrier Resistance and Capacitance

Performance with Purely Resistive Diodes

The circuit shown in Figure 39 has been optimized in much the same way that the single ended diode was optimized: the bias voltage and LO drive were adjusted so the diode is 'ON' during 50% of the LO cycle; $Z_{in}(f_{RF})$ and $Z_{out}(f_{IF})$ were calculated using equations 15 and 16, respectively, and used to find the optimum output impedance and as a basis for an iterative search for the best RF source impedance. Because of the similar basic structure of both circuits, and the use of identical diodes, the performance of the optimized balanced mixer is expected to be close to that of the optimized single ended mixer. The similarity is brought out by the resemblance of their small-signal time domain performance and quantified by Fourier analysis of their output signals.

Performance parameters for the optimized single ended mixer circuit of Figure 14 and the optimized balanced mixer shown in Figure 39 are listed in Table 9. C_L and diode 'ON' time are nearly identical. $Z_{in}(f_{RF})$ is slightly lower for the balanced mixer to reflect the parallel impedance of two diodes (see Figure 38).

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Table 9: Performance Comparison of the Optimized Purely Resistive S/E Mixer and Its Balanced Counterpart

	Single-Ended pdiod557	Single-Balanced sbm4701
Circuit Characteristics ($f_{RF} = 909$MHz):		
I_{LO}, I_{RF}, I_{bias} or V_{bias}	4mA, 0.4mA, 0mA	10mA, 0.4mA, -2.0V
$R_{S_{RF}}$	1K	1K
$R_{S_{LO}}$	N/A	1K
R_L	1K	1K
L_S, C_{LD}	1.8μH, 2.83pF	1.8μH, 2.83pF
Diode Condition:		
$V_{d_{max}}$, $V_{d_{min}}$	0.72V, -4.38V	0.75V, -8.75V
$I_{d_{max}}$, $I_{d_{min}}$	3.6mA, -31nA	5.56mA, -72nA
$\langle V_d \rangle$	0.945V	-2.0V
$\langle I_d \rangle$	0.945mA	1.8mA
T_{NL}/T_{LO}, T_{TON}/T_{LO}	0.06, 0.46	0.05, 0.54
Circuit Performance:		
$Z_{in}(f_{RF})$	1.28K $-4°$	910Ω $-5°$
$Z_{out}(f_{LO})$	$\sim$ 1K	$\sim$ 1K
C_L	4.33dB	4.17dB

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The differences between single ended and balanced mixers are the level of RF to LO and LO to RF isolation that can be achieved, and the suppression of AM noise from the LO at the output port. The LO to IF isolation and LO harmonics to IF isolation can be seen by comparing the spectrum of the output signal, $V_{out}(f)$, shown in Figure 43(b) to that of the single ended mixer in Figure 19. As expected, the output does not show any power at the LO or any of its harmonics. When diodes with non-identical saturation currents or series resistances are used, the mismatch in both arms of the secondary circuits causes the level of the LO harmonics to rise.

For a purely resistive mixer operating with $f_{RF} \sim f_{LO}$, conversion loss is minimized by ensuring that the diode is 'ON' for half the LO cycle. This guarantees that, when the RF and LO are in phase, the load capacitor will be charged to the greatest extent possible hence causing the largest excursion of the IF voltage at the load. In a balanced mixer, the effect of bias and LO drive on T_{TON} can be clearly seen in the pattern of the load current, I_{out}, and the level of the two can be traded off to set T_{TON} to $0.5T_{LO}$. For a constant drive level, the application of more negative bias levels cause $\langle V_d \rangle$ to become more negative valued as can be seen by equation 38; this can only be affected by reducing the diode 'ON' time. Similarly, at a constant V_{bias}, increasing the LO drive creates large voltage and current swings in the diodes and increses the diodes' 'ON' time.

The effect of V_{bias} on diode 'ON' time, and thereby on the portion of I_{out} that gets transferred to the load, can be seen in Figure 45. In this figure diode and circuit waveforms are plotted for three balanced mixer runs which differ only in the value of V_{bias} used. The plots show mixer operation when the RF and LO are in phase. The output current is shadowed to illustrate the phase of I_{out} at which the diode turns 'ON' and 'OFF'. Although the scales of each plot differ, the amount of time I_{out} is non-zero, corresponding to diode 'ON' time, clearly decreases as V_{bias} is increased from 0.5V to -4.25V. $\langle I_{out} \rangle$ is noted in Table 10 for these runs: it peaks, and conversion loss sinks, as T_{TON} approaches $0.5T_{LO}$. Table 10 lists other performance parameters corresponding to these runs. The last entry shows the effect of changing the LO drive from 10mA to 4mA when a bias voltage of -0.5V is applied. These data show that bias and drive level can be traded off to set T_{TON} to $0.5T_{LO}$ and that this point

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indeed corresponds to $C_{L_{min}}$ as predicted by the ideal switch analogy and verified by the single ended mixer simulations.

Table 10: Performance of a Purely Resistive Balanced Mixer as V_{bias} is Varied

Run	V_{bias}	I_{LO}	$\langle I_{out}(T_1)\rangle$	$\frac{T_{NL}}{T_{LO}}$	$\frac{T_{ON}}{T_{LO}}$	$Z_{in_{RF}}(f_{RF})$	C_L
sbm2701	−0.5V	10mA	113μA	0.048	0.655	561Ω −7°	5.13dB
sbm4701	−2.0V	10mA	124μA	0.046	0.536	910Ω −5°	4.17dB
sbm3701	−3.5V	10mA	122μA	0.046	0.442	1.31K −4°	4.30dB
sbm31021	−4.25V	10mA	118μA	0.050	0.402	1.55K −3°	4.62dB
sbm5701	−0.5V	4mA	124μA	0.116	0.528	965Ω −4°	4.20dB

Balanced Mixers Having Nonzero C_B

Diode capacitance, C_B, can be added to the diode model used in the balanced mixer with similar results as found in the single ended mixer case discussed in Section 4.2.3. When the diode capacitance at zero bias, C_{j0}, is set to 0.25μF in the mixer shown in Figure 39, the mixer waveforms in Figure 46 are obtained at the four moments during the LO cycle when the RF and LO signals are in-phase, 90° out-of-phase, 180° out-of-phase, and 270° out-of-phase. They can be compared against the corresponding mixer waveform at T_1, T_2, T_3, and T_4 for operation with a purely resistive diode as shown in Figure 44.

The diode current is now composed of current flowing through the diode's non-linear resistance, I_{d_r}, and the current flowing the non-linear capacitance I_{d_c}. I_{d_r} is calculated from equation 5 using SPICE data and I_{d_c} is then obtained by subtracting I_{d_r} from I_d. I_d and I_{d_r} are plotted in Figure 46; I_{d_c} must be inferred from the plot. The diode waveforms change dramatically even for low values of barrier capacitance: I_d, which previously had been held at zero for diode voltage less than the turn-on voltage of the diode, $V_{d_{ON}}$, is now somewhat sinusoidal; I_d and V_d are no longer in-phase. I_{out}, as before, is outlined for clarity and the area under it is shaded when the diode is turned 'ON' as can be seen by the non-zero valued I_{d_r}.

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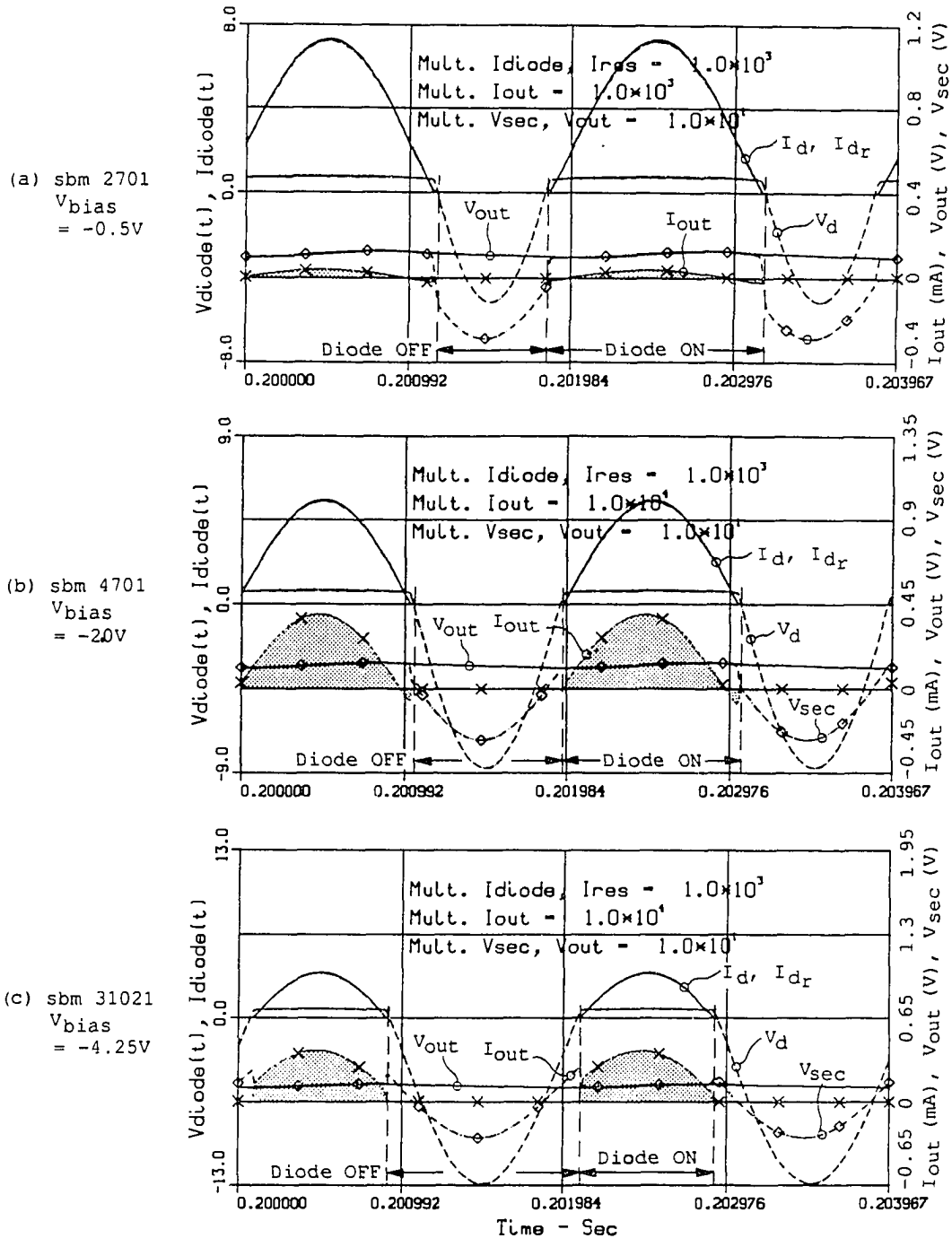
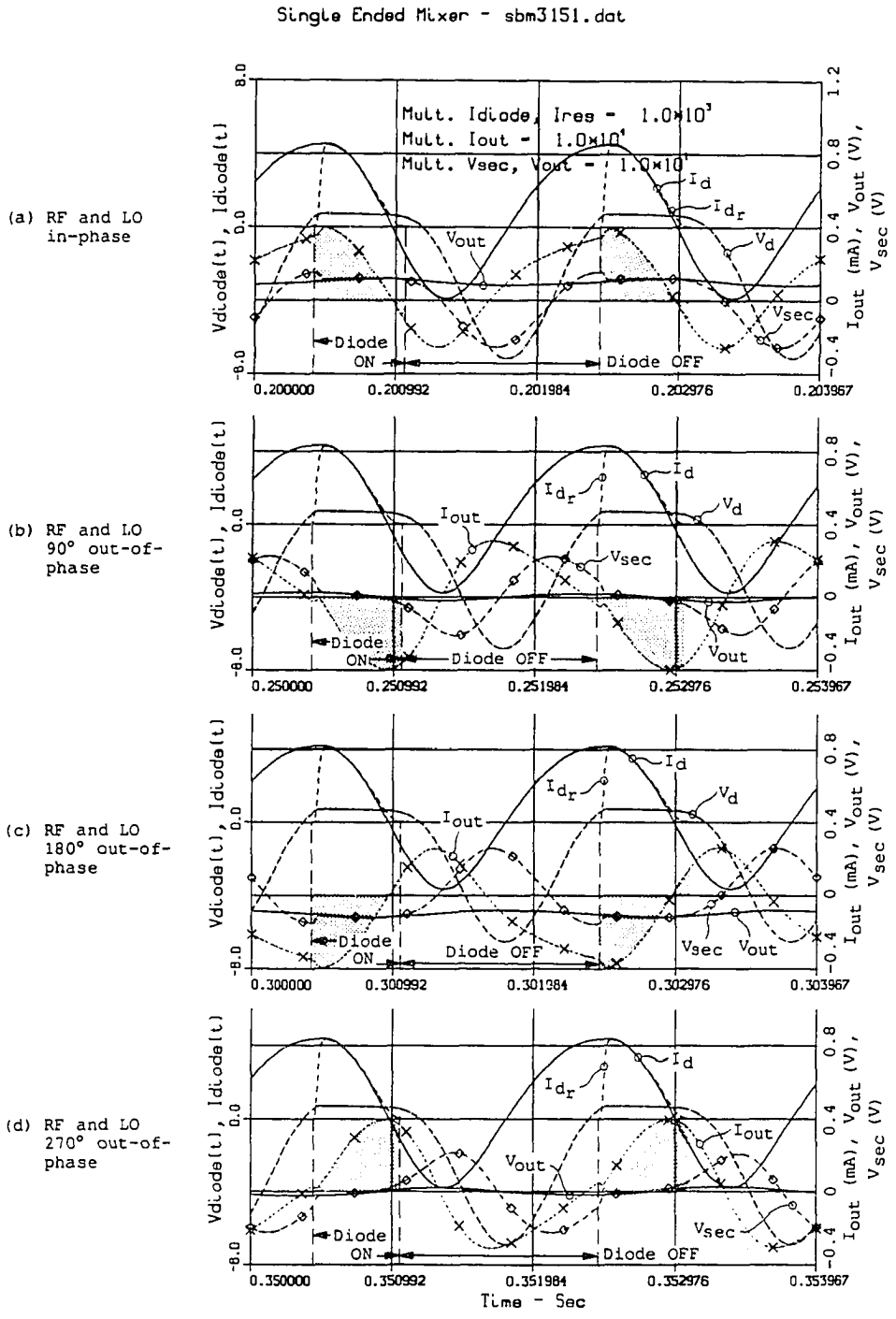


Figure 45: Effect of varying V_{bias} on mixer circuit waveform.

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(a) RF and LO in-phase

(b) RF and LO 90° out-of-phase

(c) RF and LO 180° out-of-phase

(d) RF and LO 270° out-of-phase

Figure 46: Balanced mixer waveforms for diode with $C_{j0} = 0.25$pF.

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The parallel combination of C_B and R_B causes the diode voltage to take longer to build up to $V_{d_{ON}}$ and allows V_d to slowly decrease from $V_{d_{ON}}$, thus reducing the amount of time for substantial current flow through the barrier resistance at both ends of the 'ON' period. For the same bias level and set of circuit components, T_{TON} is reduced from $0.536T_{LO}$ to $0.32T_{LO}$ and $\langle I_{out}(T_1)\rangle$ decreases from 124μA to 101μA with the addition of C_B with $C_{j0} = 0.25$pF. C_L can then be calculated from equations 40 and 41 to increase from 4.15dB to 6.0dB (or found from the Fourier transform of $V_{out}(t)$ to increase from 4.17dB to 6.09dB).

The level of bias voltage and LO drive can again be used to control the 'ON' time of the diode. In Figure 47 the diode waveforms for three mixer runs are plotted corresponding to V_{bias} values of -0.5 to $-4.25V$ for the balanced mixer depicted in Figure 39 with $C_{j0} = 0.25$pF. Now that a capacitor diode is used in the mixer circuit, $\langle I_{out}(T_1)\rangle$ is no longer maximized by setting T_{TON} to $0.5T_{LO}$. Adjusting the window in which the diode current may charge the load impedance to allow only the positive-going RF current to flow at T_1 is no longer acomplished by setting $T_{TON} = 0.5T_{RF} \sim 0.5T_{LO}$ because the diode current now possesses two components, I_{d_r} and I_{d_c}, of which I_{d_r} is the dominant contributor to the frequency conversion process. When capacitive diodes are used, the bias level and LO drive must be iteratively varied to maximize $\langle I_{out}(T_1)\rangle$, or equivalently to maximize the shaded area under I_{out}. Table 11 lists performance parameters for these runs. As can be seen, the level of bias used effects $Z_{in}(f_{RF})$, T_{TON}, and $\langle I_{out}(T_1)\rangle$. $\langle I_{out}(T_1)\rangle$ is greatest when $T_{TON} = 0.32T_{LO}$. The last entry shows the effect of changing the LO drive from 10mA to 4mA when a bias voltage of -0.5V is applied. Notice that, whereas those drive levels produced nearly equivalent conversion loss as $V_{bias} = -2.0$V and $I_{LO} = 10$mA when a purely resistive diode was used in the simulation, they no longer minimize conversion loss when a capacitive diode is used. This stresses the need to iteratively search for the optimum diode bias point.

Figure 48 shows the capacitive diode current I_{d_c}, the barrier capacitance and barrier capacitor charge waveforms associated with the three mixer runs in Figure 47. Comparisons of I_d and I_{d_r} in Figure 47 and I_{d_c} in Figure 48 show that, at any given moment, the current in the diode is predominantly resistive or capacitive but does

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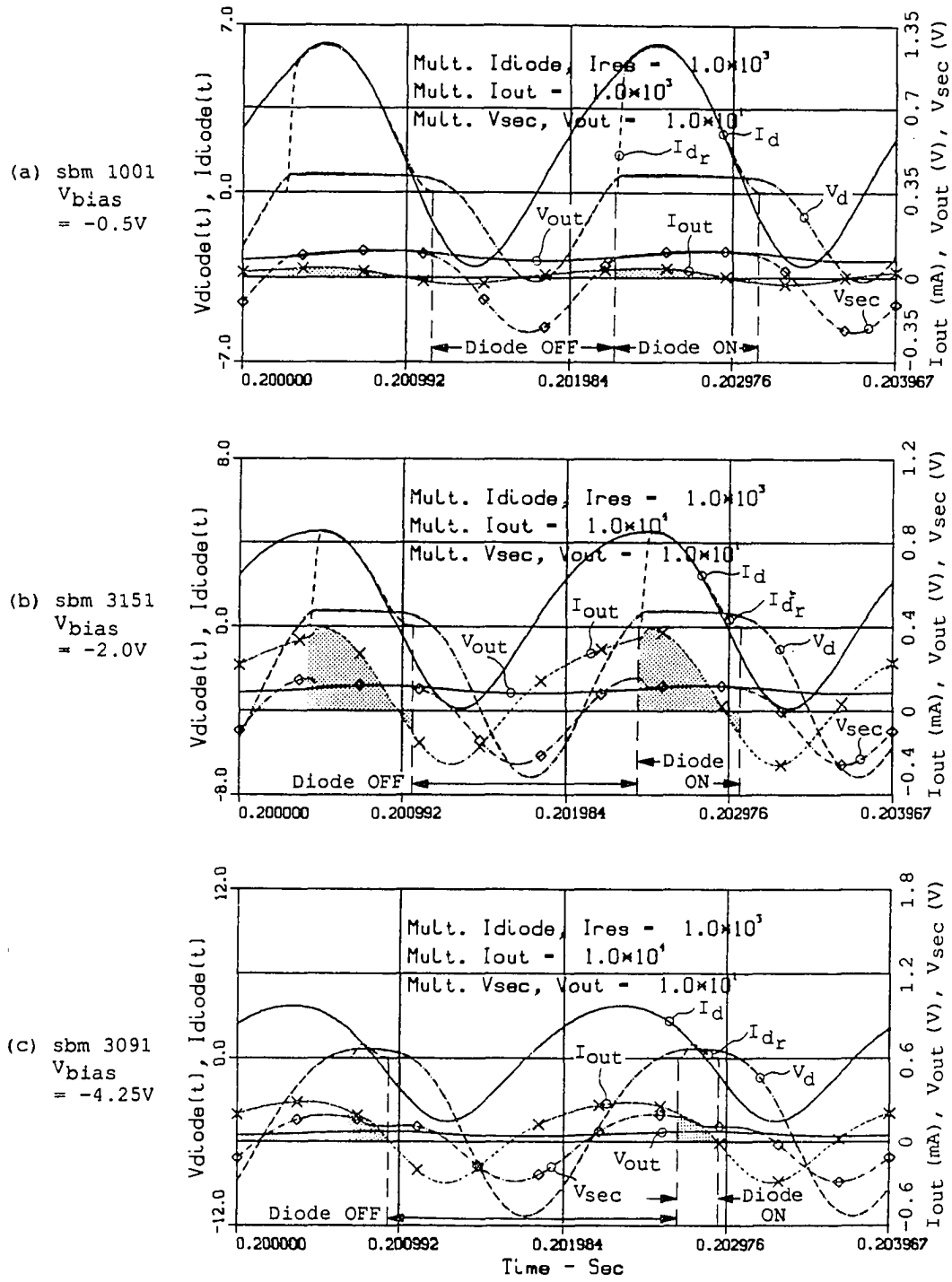


Figure 47: Balanced mixer waveforms with $C_{j0} = 0.25$pF as V_{bias} is varied.

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Table 11: Performance of a Balanced Mixer with $C_{j0} = 0.25$pF as V_{bias} is Varied

Run	V_{bias}	I_{LO}	$\langle I_{out}(T_1)\rangle$	$\frac{T_{NL}}{T_{LO}}$	$\frac{T_{TON}}{T_{LO}}$	$Z_{in_{RF}}(f_{RF})$	C_L
sbm1001	-0.5V	10mA	89.2μA	0.07	0.46	384Ω $-62°$	7.07dB
sbm3151	-2.0V	10mA	101μA	0.07	0.32	565Ω $-67°$	6.09dB
sbm1011	-3.5V	10mA	91.1μA	0.08	0.20	732Ω $-71°$	7.00dB
sbm3091	-4.25V	10mA	57.3μA	0.10	0.12	785Ω $-77°$	10.9dB
sbm1012	-0.5V	4mA	80.9μA	0.17	0.25	474Ω $-75°$	8.00dB

not flow in both elements simultaneously except for cases such as $V_{bias} = -4.25$V, where the diode is hardly turned 'ON'.

The division of RF current between the RF source elements, R_s and L_s, and into the common secondary wire can be seen in Fig. 49. This figure is the balanced mixer counterpart of Fig. 36. In it, the energy and RF currents in the optimally biased balanced mixer run is shown at T_1. In the top graph, the energy in the barier capacitance is plotted acording to equation 29 using SPICE data. Maximum energy storage occurs when the LO drives the voltage accross the non-linear capacitor to its most negative value. In the second graph, I_d and I_{d_r} in D_1 are plotted along with I_{R_s}, I_{L_s}, and I_{out}. (Examination of the balanced mixer's constuction shows that the current flowing into the common secondary node is equal to that flowing into the load impedance.) This plot is useful in studying the transfer of I_{RF} to I_{out}. I_{RF} comprises three currents:

$$I_{RF} = I_{R_s} + I_{L_s} + I_{out},$$

and I_{out} in turn comprises the currents in each of the balanced mixer diodes, D_1 and D_2. To minimize C_L or maximize $\langle I_{out}(T_1)\rangle$, the charge in the positive half cycle of I_{RF} should be transferred to the load. In this case, Figure 49 shows that only half of the positive RF charge is transferred to the load and that, once the diode turns 'ON', $I_{out} \sim I_{RF}$. This type of graph is helpful when matching circuits are used, as the transfer of energy between components during one LO cycle and the division of

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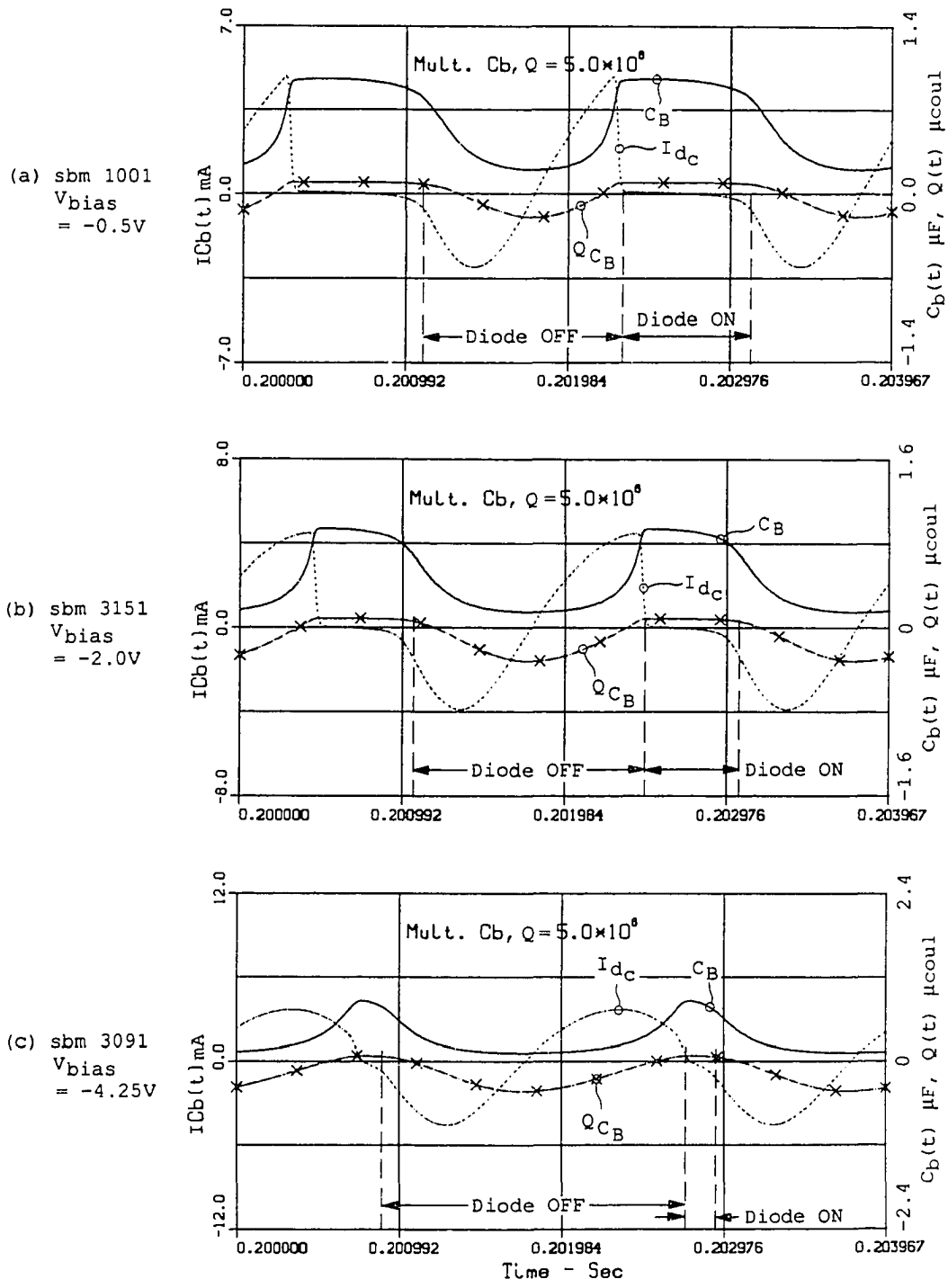


Figure 48: Barrier capacitance, barrier charge, and capacitor current waveforms for the balanced mixer as V_{bias} is varied.

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RF current among matching elements can be studied.

Inductive Matching Used on a Balanced Mixer

An inductive matching circuit can be constructed to completely match the RF source to the mixer impedance at the RF port as was done in the single-ended mixer case. Conversion loss will then be reduced. However, as similar improvements will be obtained as with the single-ended mixer, this technique of optimizing mixer performance will not be discussed here. The use of this time-domain mixer design tool in optimizing single-ended and balanced mixer performance will be addressed in Chapter 5.

Use of Other Diode Models

The balanced mixer in Figure 39 can be run with other diode models and the same optimization criteria used to obtain $C_{L_{min}}$. As an illustration, the diode model DM_3 has been substituted the previously used diode model DM_1 and the new mixer has been optimized. Mixer characteristics and performance for the purely resistive balanced mixer with both diode models are listed in Table 12. The principal difference in mixer operation is that lower bias and drive levels are required to set T_{TON} to $0.5T_{LO}$ due to the higher saturation current of DM_3 (I_s is 10^{-9}A for DM_3 and 10^{-14}A for DM_1). For this reason, the mixer with the lowest conversion loss and lowest drive levels was chosen for comparison against DM_3 (see Table 10). As can be seen from Table 12, both mixers are optimized when $T_{TON} \sim 0.5T_{LO}$ and both possess comparable conversion losses.

4.4 Frequency Domain Technique Results

The mixer performance of 'Y', 'Z', and *Resistively Matched* mixers detailed in this chapter can be compared against predictions obtained by analysis using the conventional frequency domain approach. The comparison has been performed in two ways. Both utilize the same model to represent the small signal operation of the mixer as a multifrequency linear multiport network; this mixer model is shown in Fig. 11.

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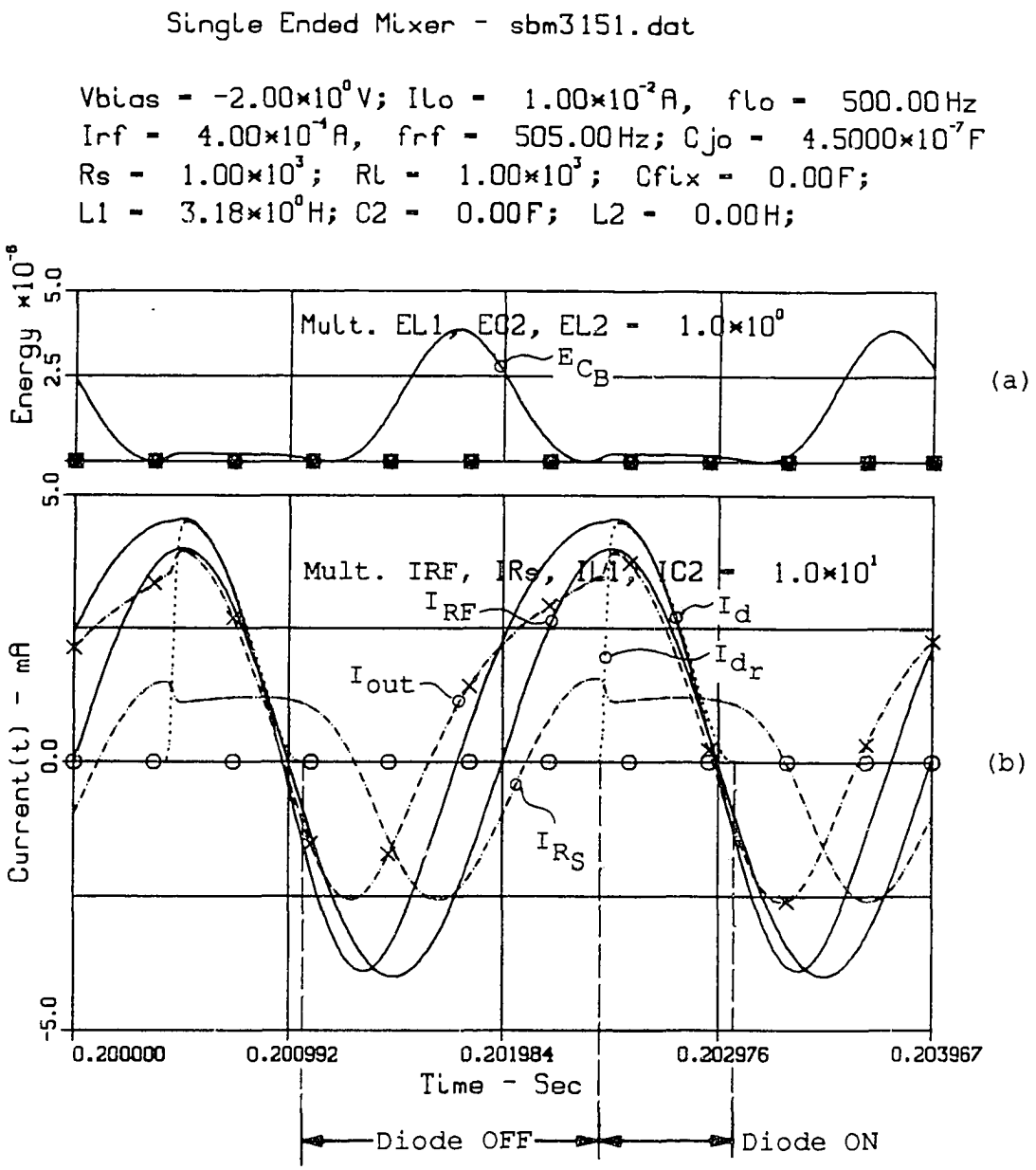


Figure 49: Energy waveforms and RF circuit currents for the balanced mixer with $C_{j0} = 0.25$pF.

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Table 12: Comparison of Purely Resistive Balanced Mixer Circuit with Two Types of Diodes

	DM_1	DM_3
Run	sbm5701	tsbm12
Cicuit Characteristics (f_{RF} = 909MHz):		
V_{bias}	−0.5V	−0.3V
I_{LO}	4mA	2.5mA
I_{RF}	0.4mA	0.1mA
$R_{S_{RF}}$	1K	1K
$R_{S_{LO}}$	1K	1K
R_L	1K	2K
L_S, C_{LD}	1.8μH, 2.83pF	1.8μH, 2.83pF
Diode Condition:		
$V_{d_{max}}$, $V_{d_{min}}$	0.69V, −3.5V	0.36V, −1.59V
$I_{d_{max}}$, $I_{d_{min}}$	2.25mA, −31nA	0.61mA, −9nA
T_{NL}/T_{LO}, T_{TON}/T_{LO}	0.12, 0.53	0.44, 0.46
Circuit Performance:		
$Z_{in}(f_{RF})$	965Ω −4°	1.76K −7°
C_L	4.20dB	4.61dB

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The first approach bypasses the need to solve the large signal mixer problem by using the SPICE generated solution of the diode waveforms in the mixer circuit as input to Held and Kerr's formulation of the mixer conversion loss problem. $I_d(t)$ and $V_d(t)$ are used to calculate the diode conductance, $g(t)$, and capacitance, $C_B(t)$, according to eqns. 24 and 7. The Fourier coefficients, G_k and C_k, of the conductance and capacitance waveforms, respectively, are then computed by the design tool as shown in Fig. 12.

Once the diode conductance and capacitance waveforms can be expressed in terms of their Fourier coefficients:

$$g(t) = \sum_{k=-\infty}^{\infty} G_k \, e^{jk\omega_{LO}t}, \qquad \text{for } G_k = G_k^*,$$

$$C_B(t) = \sum_{k=-\infty}^{\infty} C_k \, e^{jk\omega_{LO}t}, \qquad \text{for } C_k = C_k^*,$$

the large signal problem is solved. The small signal properties of the mixer can then be determined from its nonlinear admittance matrix, Y_{nm}, its series resistance, r_{ser}, and the embedding impedances presented by the circuit at each mixer sideband frequency, $Z_{emb}(f_n)$. Following Held and Kerr's treatment of the problem, the small signal admittance matrix of the nonlinear portion of the diode is first constructed from the Fourier coefficients G_k and C_k; this matrix relates the small signal currents δI_n at sideband frequency f_n to the small signal voltage δV_m at sideband frequency f_m, where n and m are positive or negative integers [29]:

$$\begin{bmatrix} \delta I_N \\ \vdots \\ \delta I_0 \\ \vdots \\ \delta I_{-N} \end{bmatrix} = \begin{bmatrix} Y_{NN} & & Y_{N0} & & Y_{N-N} \\ \vdots & & & & \vdots \\ Y_{0N} & \cdots \; Y_{01} & Y_{00} & Y_{0-1} \; \cdots & Y_{0-N} \\ \vdots & & & & \vdots \\ Y_{-NN} & & Y_{-N0} & & Y_{-N-N} \end{bmatrix} \begin{bmatrix} \delta V_N \\ \vdots \\ \delta V_0 \\ \vdots \\ \delta V_{-N} \end{bmatrix} \tag{42}$$

where

$$Y_{nm} = G_{n-m} + j(\omega_{IF} + n\,\omega_{LO})\, C_{n-m}.$$

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The admittance of the nonlinear portion of the diode is a function of the sideband frequency f_n and the Fourier coefficient of the conductance and capacitance waveforms at the $(n-m)^{th}$ LO harmonic. In practice the order of the matrix is set by the number of sideband frequencies whose embedding impedance is considered to be of importance to the mixer's operation. If k Fourier coefficients are found for the diode's conductance and capacitance, then the embedding impedances at $(2k+1)$ sideband frequencies are needed.

The mixer analysis developed by Torrey and Whitmer long before the advent of large computers calculated mixer performance in a similar fashion. They considered a 3 X 3 diode admittance matrix; this required the Fourier coefficients of $g(t)$ and $C_B(t)$ at DC and f_{LO} and the embedding impedances at f_{RF}, f_{IF} and f_{IMAGE} to predict mixer performance [67]. Because the interaction between the circuit and diode at other mixer frequencies could not be accounted for in their model, the accuracy with which they were able to predict performance depended upon the mixer's construction. More recently Held and Kerr have succeeded in predicting mixer performance at 100 GHz by characterizing their diode with 13 X 13 and 15 X 15 admittance matrices [30].

Once the diode's nonlinear admittance matrix has been found, an augmented admittance matrix that contains the diode's series resistance and the embedding impedances at the $(2k+1)$ sideband frequencies is formed. The small signal voltage sources, δV_n, shown in Fig. 11, are replaced by their Norton equivalents, δI_n, which are connected accross $Z_{emb_n} + r_{ser}$. The augmented matrix relates these small signal currents and voltages at the $2k+1$ sideband frequencies according to:

$$\delta I' = \mathbf{Y}' \, \delta V$$

where

$$\mathbf{Y}' = \mathbf{Y} + \text{diag}\left[\frac{1}{Z_{emb}(f_n) + r_{ser}}\right].$$

From the following definition of mixer conversion loss,

$$C_{L_{HK}} = \frac{\text{Power available from source} Z_{emb}(f_1)}{\text{Power delivered to load } Z_{emb}(f_0)},$$

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Table 13: Comparison of Mixer Conversion Loss for the 'Y', 'Z', and 'RM' Mixers Calculated with Time and Frequency Domain Based Methods

Method	'Y' Mixer pdiod596	'Z' Mixer pdiod583	'RM' Mixer pdiod557
Design Tool:	5.0 dB	4.25 dB	4.33 dB
Frequency Domain Analysis:			
9 X 9 Y Matrix	4.56 dB	4.35 dB	4.28 dB
11 X 11 Y Matrix	4.48 dB	2.8 dB	4.35 dB

Held and Kerr derive C_L of a mixer with a conjugately matched IF port to be

$$C_{L_{HK}} = \frac{1}{4|\ Z'_{01}\ |^2}\ \frac{|\ Z_{emb}(f_0)+r_{ser}\ |^2}{Re[Z_{emb}(f_0)]}\ \frac{|\ Z_{emb}(f_1)+r_{ser}\ |^2}{Re[Z_{emb}(f_1)]}$$

where $\mathbf{Z'} = (\mathrm{Y'})^{-1}$. When $Z_{emb}(f_{IF}) \neq Z^*_{out}(f_{IF})$, the above expression can be corrected as follows:

$$C'_L = C_{L_{HK}} \cdot \frac{|\ Z_{emb}(f_0)+r_{ser}\ |^2}{Re[Z_L]}. \tag{43}$$

Following this procedure conversion loss has been calculated for the optimized 'Y', 'Z', and 'RM' mixers using the program *convhk.for*. The results are given in Table 13 for a 9 X 9 and a 11 X 11 order admittance matrix. Calculation with matrices of different order is done to quantize the sensitivity of these calculations to the number of sideband frequencies used. The agreement between the SPICE generated results and the conversion matrix results are within 0.50dB except for the 'Z' mixer. In that case the 2.8 dB C_L result obtained using frequency domain analysis with the 11 X 11 matrix is $\sim$ 1.5 dB below the results obtained with the 9 X 9 matrix and with the design tool. Analysis of other 'Z' mixers also showed a greater than 1 dB difference in the two matrix order results. It is taken to indicate that a greater number of sideband frequencies were necessary for the results to converge. The difficulty of analyzing the 'Z' mixer is attributable to the characteristically high output embedding impedances that it presents at the LO harmonics (see Table 6).

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The second approach uses Maas' program DIODEMX [43] to solve the large signal and small signal problems. The program finds conversion loss, input and output impedance for a mixer circuit. It determines if the circuit is unconditionally stable and, if so, calculates the maximum available gain. Lastly, it calculates mixer noise temperature. To solve the large signal problem, the embedding impedances at DC and at the LO and its first four harmonics are required. The small signal solution involves manipulating a 9 X 9 admittance matrix similar to the one described above; to do so the embedding impedances at f_n, for n ranging from {-4, 4} must be entered. However, because the algorithm used by DIODEMX to find the solution of the large signal problem calculates a capacitive current in the diode, this program has some difficulty converging for purely resistive mixers. To circumvent this, the diode's large signal current, voltage and capacitance waveforms derived from our design tool can be entered into the program. DIODEMX is then directed to solve only the small signal problem.

Figure 50 shows conversion loss as C_{j0} is varied from 0 to 1.5 pF; C_L is calculated with the design tool as well as with both frequency domain techniques outlined above. When no inductive matching is used, all three methods agree within 0.4 dB except for the results at $C_{j0} = 1$ pF where the design tool, estimated C_L to be 22.2 dB, arrives at an estimate 1.6 dB higher than those of the frequency domain analysis which put the C_L at 20.6 dB and 20.85 dB. As expected conversion loss rises steadily as C_{j0} is increased. When inductive matching is used the three methods differ greatly although the results predicted with both matrix sizes using Held and Kerr's method agree. The design tool predicts a monotonic degradation of C_L as C_{j0} is increased where the other two methods predict non-monotonically increasing C_L's. As these circuits are not fully optimized it is difficult to say with certainty which behavior is more reasonable, however the improvement in C_L as C_{j0} is increased from 0 to 1 pF predicted by both frequency domain analysis contradicts experimentally found trends and is very surprising. It is difficult to speculate whether including higher order LO harmonics in the conductance and capacitance expansions or whether increasing the number of sideband frequencies in the analysis will cause the predicted mixer performance to reflect a more expected trend. This comparison reflects one of the

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advantages of time domain based analysis: once the circuit model has been decided upon, the accuracy to which the small signal voltages and currents are known is set by the voltage and current convergence criteria used by the SPICE program.

Figure 51 gives the single-sideband noise temperature for these mixers as predicted by DIODEMX. Without inductive matching, mixer noise temperature rises from 47 K for the purely resistive mixer to 447 K when $C_{j0} = 0.25$ pF and to 1164 K for $C_{j0} = 1.0$ pF. When inductive matching is used, mixer noise temperature drops to 162 K for $C_{j0} = 0.25$ pF and 348 K for $C_{j0} = 1.0$ pF. This decrease in mixer noise temperature is principally due to the increased mixer performance, ie. lower C_L. According to DIODEMX, the purely resistive diode run, the non-compensated mixer circuit with $C_{j0} = 0.25$ pF, and all of the mixer runs with inductive matching are unconditionally stable.

4.5 Conclusion

This chapter concerns itself primarily with the design of purely resistive diode mixers. These circuits are more tractable to analysis and optimization than those with diodes with barrier capacitance and therefore are examined first. Both single-ended and balanced mixers are simulated with the design tool. Single-ended mixers results are contrasted with those predicted by two frequency domain analysis programs.

The chapter begins with a discussion of a circuit with an ideal switch and its similarity to a diode mixer. The simplicity of the former circuit facilitates the derivation of an expression for conversion loss in terms of the average current in the load during one LO cycle when the RF and LO are in phase $\langle I_L(T_1)\rangle$, the source resistance R_S, and, the load resistance R_L. $\langle I_L(T_1)\rangle$ is shown to be maximized, and correspondingly C_L is minimized, when the switch is closed for half the LO period and when R_S is equal to R_L for arbitrary values of R_L. Minimum C_L is then found to be 10 dB.

The similarity of the switch to a simple diode mixer is borne out via simulation results indicating a mixer conversion loss of 10 dB is attained when the diode 'ON' time is 0.5 T_{LO} for R_S equal to R_L. Bias and LO drive are shown to be interchangeable

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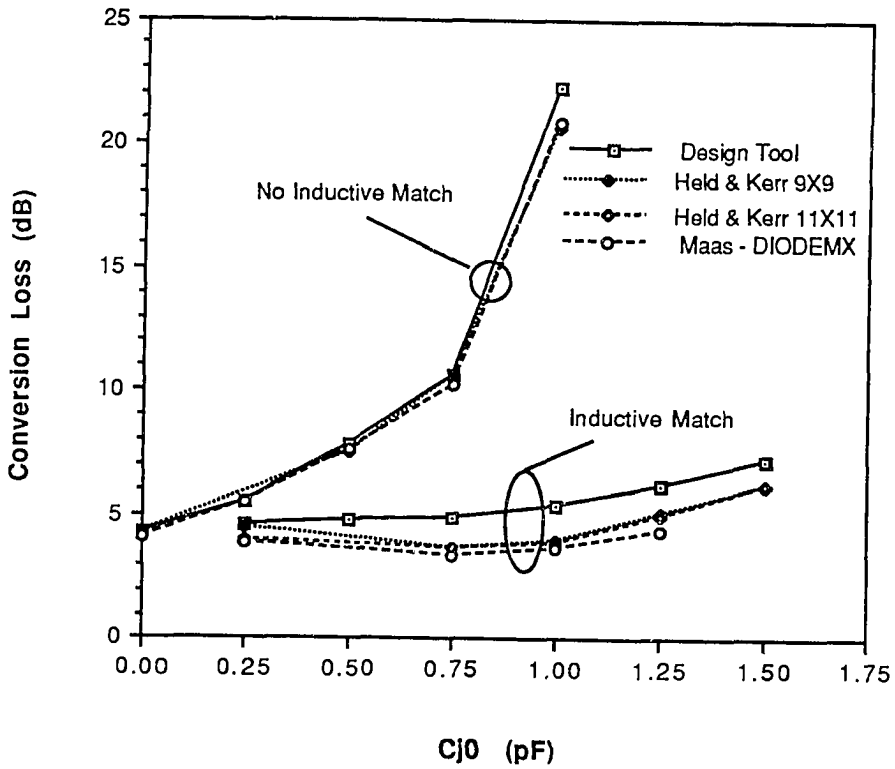


Figure 50: Conversion loss of mixers with capacitive diodes calculated using both time and frequency domain analysis.

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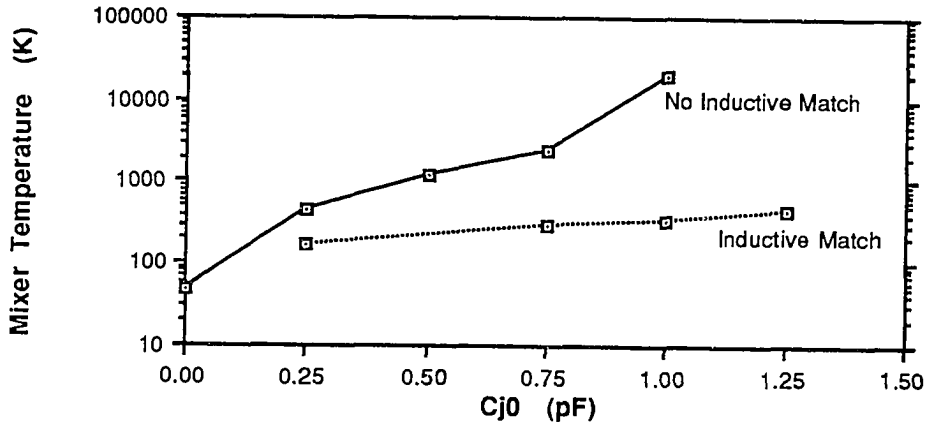


Figure 51: Mixer noise temperature predicted by DIODEMX.

in setting the diode 'ON' time. Although these mixer structures are known to be non-optimal for conversion loss performance, the criteria necessary to minimize conversion loss can be easily studied and the application of these criteria to diode mixer design can be rapidly verified via the design tool.

To find an appropriate circuit to be used as a starting point for the direct conversion mixer study, three mixer circuits are examined: the 'Y' mixer, the 'Z' mixer, and the 'RM' mixer. 'Y' and 'Z' mixers have been studied by many researchers; their names, however, are attributable to Saleh [55]. The 'RM' mixer is defined and analyzed in Chapter 3. The circuits differ in the terminations they provide to the LO harmonics and sideband frequencies $n > 1$. In the 'Y' mixer, these frequencies are terminated in short-circuits; in the 'Z' mixer, they are terminated in open-circuits; and, in the 'RM' mixer, they are resistively terminated. These circuits were analyzed and categorized assuming a broadband match was provided to the diode at f_{LO}, ie. $Z_{emb}(f_{RF}) \approx Z_{emb}(f_{LO}) \approx Z_{emb}(f_{IMAGE})$. The diode was taken to have an exponential I-V curve ($r_{ser} = 0$) and to possess no barrier capacitance. Previous researchers have shown that, when the Fourier coefficients of the diode's waveform can be optimized, the minimum conversion loss achievable with such broadband mixers is 3.0 dB. This should be compared against the minimum C_L of 0 dB attainable when f_{IMAGE} is terminated reactively. When the diode resistance has a pulse shape whose duty cycle

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alone can be varied, Saleh found that the C_L of the 'Z' mixer could more rapidly approach the 3 dB limit than could the C_L of the 'Y' mixer. Kelly found that the C_L limit for broadband mixers which resistively terminate the LO harmonics and sideband frequencies $n > 1$ was 3.9 dB [36]. Evaluation of these mixer circuits thus enables a good initial circuit for subsequent circuit optimization to be chosen. It permits a comparison between projected mixer performance, assuming ideal circuits and exponential diodes, and simulated mixer performance with realistically implemented circuits and purely resistive diodes. Lastly it serves to validate the performance of the design tool.

Simulation and optimization of the 'Y' and 'Z' mixers were performed in this chapter. Agreement between the theoretically derived optimum diode and circuit conditions and that found with the simulation tool is good. The simulated 'Y' mixer, predicted to have lowest C_L when the bias and drive conditions are set so that the duty cycle of the conductance waveform approaches zero, was found to have a minimum conversion loss of 5.0 dB when the diode 'ON' time, T_{TON}, was 0.25 T_{LO}. The 'Z' mixer, predicted to have lowest C_L when the duty cycle of the resistance waveform approaches zero, was found to have a minimum conversion loss of 4.25 dB when T_{TON} was 0.75 T_{LO}. By contrast, the 'RM' mixer, predicted in Chapter 3 to have lowest C_L when the duty cycle of the conductance waveform is 50%, was found to have a minimum C_L of 4.3 dB when T_{TON} was 0.50 T_{LO}. Therefore, as predicted, the 'Z' mixer was found to have a lower C_L than the 'Y' mixer when practical circuits are used.

The embedding impedances provided by the 'Y', 'Z', and, 'RM' circuits to the diode were calculated for the practical circuits and found to have some difficulty in producing the correct match at f_{LO} but to agree well with the ideal matches presented for all frequencies higher than f_{LO}. Because the 'RM' mixer had a comparable performance to the 'Z' mixer, and, because it is easier to implement, the 'RM' circuit was chosen as the starting point for mixer optimization.

The two remaining topics in single-ended mixer design explored in this chapter are the degradation in 'RM' mixer performance once barrier capacitance (C_B) is introduced in the diode model and the conventional circuit techniques used to compensate

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for this degradation. The reasons for increased C_L are shown graphically and quantitatively as the zero bias barrier capacitance, C_{j0}, is varied from 0.25 pF up to 1.5 pF, the maximum expected for a 1 GHz diode. Conventional techniques for matching diodes with non-zero C_B treat C_B as a fixed capacitance of value equal to C_{j0} or $\langle C_B \rangle$. Therefore they do not take advantage of the nonlinearity of C_B as a second frequency conversion element in the diode. Instead the barrier resistance, R_B, is seen as the sole frequency conversion element in the mixer. Standard matching techniques are thus used to set $Z_S(f_{RF}) \approx Z_{in}^*(f_{RF})$ and thereby maximize the power match into R_B. This can be accomplished by inductively matching to $Z_{in}(f_{RF})$. As $C_{L_{min}}$ does not occur exactly as conjugate match is achieved, the value of the inductor must be determined experimentally or, in our case, through repeated simulations.

These simulations resulted in reducing C_L to 4.6 dB for $C_{j0} = 0.25$ pF, to 5.4 dB for $C_{j0} = 1.0$ pF and to 7.2 dB for $C_{j0} = 1.5$ pF. T_{TON} was increased from its pre-match condition to 0.38 T_{LO} for $C_{j0} = 0.25$ pF, to 0.30 T_{LO} for $C_{j0} = 1.0$ pF and to 0.28 T_{LO} for $C_{j0} = 1.5$ pF. It is interesting to note that $C_{L_{min}}$ is no longer achieved by setting R_L equal to R_S. Had the circuits been further optimized, by adjusting bias conditions, LO drive level, and R_L, greater reduction of C_L might have been possible. However these results suffice to explain why designers select diodes with low C_B for applications where good C_L performance is necessary. The C_L degradation predicted via these simulations agrees with the results of earlier researchers who find C_L degradation through straightforward considerations of power lost to R_B due to mismatch losses.

Simulation of balanced mixers is discussed next. Practical transformers are modelled by uncoupled inductors and an ideal transformer to understand their effect on the mixer circuit and arrive at reasonable values for the transformer inductances. Several models are proposed for the application of diode bias. A 'RM' balanced mixer is simulated with a purely resistive diode. The output format of the graphical programs is detailed as it differs from that used for single-ended mixers due to the isolation of RF and LO and the possibility of examining small-signal currents and voltages directly. The similarities between the operation of the purely resistive diode balanced mixer and the idealized switch are examined: the pattern created by the

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average current of the load is shown to exactly mirror that in the ideal switch circuit. Hence the graphical criteria developed for the switch is shown to apply for the balanced mixer design. The balanced mixer output spectrum is shown as devoid of power at any of the LO harmonics for matched diode pairs. The conversion loss for the optimal balanced mixer circuit, expected to be close to the 4.3 dB, is found to be 4.2 dB. Minimum C_L is achieved when T_{TON} is, as expected, 0.50 T_{LO}.

Degradation of mixer performance is shown graphically when C_B is added to the diode model (C_{j0} = 0.25 pF) without concomitant circuit changes. C_L increases from 4.2 dB to 6.1 dB and T_{TON} falls to 0.32 T_{LO}. Attempts to decrease C_L by adjusting the bias and drive levels so as to set T_{TON} to 0.50 T_{LO} are shown to succeed in increasing T_{TON} without reducing C_L. This behavior is graphically demonstrated and explained. Lastly the performance of balanced mixer circuits with purely resistive diodes is shown not to depend on the diode model used.

The chapter concludes with a comparison of the results generated by the mixer design tool and two frequency domain analysis programs based on Held and Kerr's and Maas' work. Held and Kerr formulate the mixer conversion loss problem in terms of the mixer's embedding impedances at the sideband frequencies and the large-signal diode characteristics [29]. Using the Fourier coefficients for the diode's conductance and capacitance as calculated by the design tool, the program *convlhk.for* has been written to find conversion loss based on the Held and Kerr small-signal formulation of the problem. Maas' program DIODEMX was also used to solve the large-signal and small-signal mixer performance problems; it requires as input the diode model and the embedding impedances at the LO harmonics and sideband frequencies [43]. *Convlhk.for* gave the C_L estimate for the 'Y' mixer to be 0.5 dB less than the design tool estimate; for the 'RM' mixer it gave an estimate 0.15 dB less than the design tool estimate. Agreement with the design tool estimate for the 'Z' mixer varied from 0.1 dB to 1.45 dB depending on the order of the admittance matrix considered.

Both programs were used to evaluate the C_L degradation with C_{j0} in the 'RM' mixer with and without the use of inductive matches. When no inductive matching is used, all three methods agree within 0.4 dB except for the results at C_{j0} = 1 pF where the design tool, estimated C_L to be 22.2 dB, arrives at an estimate 1.6 dB

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higher than those of the frequency domain analysis which put the C_L at 20.6 dB and 20.85 dB. When inductive matching is used, the discrepancy between the various methods increase. DIODEMX is used in addition to predict mixer noise temperature. Without inductive matching, mixer noise temperature in the 'RM' mixer rises from 47 K for the purely resistive diode ($C_{j0} = 0.001$ pF) to 447 K when $C_{j0} = 0.25$ pF and to 1164 K for $C_{j0} = 1.0$ pF. When inductive matching is used, mixer noise temperature drops to 162 K for $C_{j0} = 0.25$ pF and 348 K for $C_{j0} = 1.0$ pF. This decrease in mixer noise temperature is principally due to the increased mixer performance, ie. lower C_L. According to DIODEMX, the purely resistive diode run, the non-compensated mixer circuit with $C_{j0} = 0.25$ pF, and, all of the mixer runs with inductive matching are unconditionally stable.

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Chapter 5

Mixer Design with Practical Diodes

5.1 Introduction

In Chapter 3 a computer-aided analysis and design tool, developed for UHF and microwave mixers, was described. It is based on a time domain analysis of the mixer circuit and relies upon examination of the waveforms in the mixer circuit to establish the direction for performance optimization. These traits distinguish it from conventional mixer analysis tools which are based in the frequency domain and offer few directions for optimization. In Chapter 4 the behavior of mixers with purely resistive diodes was examined and their performance compared with that of an ideal switch. Design criteria for minimization of conversion loss were found and successfully applied to optimize resistive mixer performance. Several mixer circuits, described in the literature, which produce reactive terminations at selected mixer sideband frequencies were examined; the results obtained through simulation with the design tool were compared to those analytically derived and found to agree with them. But, despite the extensive treatment of resistive mixers in the literature, most diode mixers operating at frequencies in the UHF range and beyond cannot be assumed to use purely resistive diodes. At these frequencies the diode's nonlinear barrier capacitance no longer presents an infinite impedance to the source and thus significantly impacts

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mixer performance. The effects of non-zero barrier capacitance on mixer conversion loss, input and output impedance were detailed in Chapter 4. Improvements in C_L performance were achieved by modelling C_B as a fixed capacitor and by designing simple circuits to, more or less, conjugately match the source to the imput mixer impedance. Still better performance can be achieved if the nonlinearity of the barrier capacitance is accepted and circuits designed to take advantage of it. This chapter specifically addresses these design issues. In it we delineate why our design tool is ideally suited for solving these complex circuit problems whose solution cannot be satisfactorily derived analytically.

Let us briefly describe the difficulties involved in seeking analytical solutions to mixer design with nonlinear barrier capacitance and resistance. Analysis of mixer operation with a diode possessing nonlinear resistance and nonlinear capacitance is difficult due to the existence of significant power flow in the circuit at many frequencies. Closed form solutions cannot be attained without severely restricting real power flow, ie. assuming the circuit to reactively terminate sideband frequencies and LO harmonics with ideal short or open circuits. The analysis that has been performed rests on a variety of assumptions which, although they are known not to be true, are nevertheless accepted in order to make the problem formulation tractable to analysis. Hence the resultant theoretical predictions for mixer operation with nonzero barrier capacitance have spanned a wide range. Similarly, experimental results, obtained through a variety of different circuit implementations, have covered the gamut of possibilities.

For example, under some conditions the addition of barrier capacitance has been shown to degrade mixer performance, especially conversion loss [50,16], under other circuit and diode conditions conversion loss has been shown to remain constant or decrease to such an extent that conversion gain is possible [41,67]. In this case the resultant mixer is felt to have the potential for instability and to possess a higher noise temperature than possible without significant barrier capacitance.[1] Other researchers [41,15] have arrived at still different results under slightly different conditions: they

[1] Any improvement in C_L would be offset by an increase in temperature such that the use of this mixer as a receiver front-end would not increase receiver sensitivity.

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believe improved conversion loss and noise temperature to be achievable with capacitive diode mixers.

Some of these differences can be attributed to the variety of assumptions made in the theoretical formulation of the problem such as: the number of frequencies that are assumed to couple through the nonlinear device; whether the barrier capacitance is assumed to be fixed rather than nonlinear; whether the spreading resistance is given a nonzero value; and whether the conductance waveform, $g(t)$, and the capacitance waveform, $c(t)$, are assumed to be even functions of time. Unfortunately the impact of these assumptions on predicted performance is not clear. But the need to form simplying assumptions in order to predict mixer performance makes analysis of these mixers an ideal candidate for the application of our design tool. First, because the design tool uses SPICE to iteratively solve the integro-differential equations describing the current flow and voltage in the circuit, the device model and embedding circuit can be changed without reformulating the problem. Second, the addition of spreading resistance and nonlinear barrier capacitance can be easily accomplished. Third, because the design tool calculates time varying signals, information about power flow at a great number of frequencies is available provided the number of sample points per IF cycle is high. Fourth, no assumptions about the diode's characteristics and mixer-diode interaction are necessary. Last, the design tool allows the interaction of circuit and diode to be studied either from a time domain or frequency domain viewpoint in order to obtain insight into and understanding of the mixer's performance.

This chapter discusses mixer performance with diodes having nonlinear capacitance and resistance only. In it the technique developed to optimize mixer performance is detailed. The technique revolves about the development of an energy phasing and storage network that works in tandem with the diode's nonlinear elements to translate RF energy to the output frequency. The circuit takes advantage of the nonlinearity in the barrier capacitance by parametrically pumping it to increase the efficiency of the frequency conversion process. In this manner the degradation in conversion loss characteristic of operation with these diodes is reduced below the levels reported in the previous chapter which were achieved by simply matching to the input of the mixer. The technique takes advantage of the close spacing of f_{RF}

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and f_{LO} and hence is ideally suited to the direct conversion application. The circuit has been developed through the use of the design tool and directed by the guidelines described in the previous chapter.

Single ended and balanced mixers with diodes having barrier capacitances with zero bias values (C_{j0}) of 0.25 pF at 1 GHz have been designed with conversion losses between 2 dB and 3 dB. These mixers have broadband input circuits - meaning that the embedding circuit presents a common match to the diode at f_{RF}, f_{LO} and f_{IMAGE}. These conversion loss values are less than or equal to the 3 dB limit for a broadband mixer with an idealized (exponential) diode when the diode embedding network is reactive at all sidebands of order greater than 2. For diodes with higher C_{j0}'s, e.g. C_{j0} $\sim$ 1 pF, application of this technique results in a single-ended mixer with a conversion loss of 4.25 dB. Both results show that the previously believed levels of degradation of conversion loss performance with increasing C_{j0} need not be tolerated. In addition these time domain circuit results provide a path to understanding the interplay of circuit and diode so that guidelines for optimization of mixer performance with nonzero C_B can be constructed which will operate over a wide range of barrier capacitance values. It is hoped that this technique will also provide a physical understanding for the wide range of results previously obtained when looking at the issue of barrier capacitance on mixer performance.

This chapter comprises eight sections. Section 5.2 discusses mixer performance found by other researchers when C_B is added to the diode model. A discussion of the effect of barrier capacitance on mixer performance and a review of the literature is given. Section 5.3 details the development of the phasing network. Section 5.4 applies this network to single ended mixer designs. Section 5.5 addresses optimization of balanced mixers. In it a phasing network is developed for the RF port circuitry and an LO waveform circuit is designed to maximize the shape of the LO driving waveform. In Section 5.6 several designs for the direct conversion receiver are proposed and their performance detailed. Section 5.7 summarizes the results found and compares them against those reached by other researchers in this field. Because of the central role played by mixer design in this thesis, this chapter concludes in Section 5.8 with proposed directions for future work on the design tool and for the study of mixers

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which take advantage of both diode nonlinear elements, R_B and C_B, to improve mixer performance. A discussion of other candidate mixer circuits for the direct conversion receiver can be found in Chapter 8.

5.2 Prior Mixer Work with Nonlinear Resistive and Reactive Elements

In analyzing the effect of barrier capacitance on mixer conversion loss, most researchers have framed the problem in one of three ways: either (1) by drawing parallels to the behavior of a circuit with a sole nonlinear capacitance; or (2) by modelling the diode as a nonlinear resistor in parallel with a fixed capacitance equal to C_F; or (3) by modelling the problem as a nonlinear resistance in parallel with a nonlinear capacitance. Equivalence between model and circuit increases in this order as does the analytic complexity of the problem. In this section the conclusions found by considering each of these models will be presented. Although not all of this work described is applicable to mixer operation with practical RF diodes, it is necessary to establish the theoretical base for their study. At the conclusion of this chapter our findings for mixer behavior with nonlinear capacitance and the embedding impedance presented by the phasing network to the diode will be juxtaposed against those discussed here.

5.2.1 Single Nonlinear Reactive Element

The behavior of circuits with one nonlinear reactive component, either capacitive or inductive, has been studied for parametric amplifier, modulator, and demodulator applications [10]. Such circuits will be referred to here as NC or NL circuits depending on whether the nonlinear element is a capacitor or an inductor. In 1956 Manley and Rowe derived two independent equations relating the average power at each existing frequency that flowed into a nonlinear reactive component assuming only that the nonlinear element could be represented by a single valued characteristic [48]. The average power, or real power, flowing into the element at the frequency $\pm \mid mf_1 + nf_0 \mid$ was denoted by $W_{m,n}$ where f_1 and f_0 were two applied frequencies that were

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incommensurate and positive. These $W_{m,n}$'s could be interrelated according to the two following equations:

$$\sum_{m=0}^{\infty} \sum_{m=-\infty}^{\infty} \frac{mW_{m,n}}{mf_1 + nf_0} = 0, \tag{44}$$

$$\sum_{m=-\infty}^{\infty} \sum_{m=0}^{\infty} \frac{nW_{m,n}}{mf_1 + nf_0} = 0. \tag{45}$$

The significance of these equations can be understood by considering the nonlinear elements as connected in parallel to an infinite number of generator circuits, each at a unique frequency $mf_1 + nf_0$. Each generator circuit possesses a voltage signal source, a source impedance, and an ideal filter which appears as a short at the generator's frequency and as an open at all other frequencies. All three elements are connected in series. This circuit has many similarities with that of the mixer diode and its embedding circuit. Using this conceptual model, we permit a finite number of non-zero voltage sources to exist. Then eqns. 44 and 45 can be used to find the average power flow into the nonlinear element at each frequency.

In our case we are interested in the performance of a downconverter whose only nonlinear element is a capacitor and where only three frequencies are taken to exist. Two cases can be distinguished for this converter's performance depending on whether the input signal at f_{RF} is greater than f_{LO} or less than f_{LO}; the RF is then denoted by f_{RF+} or f_{RF-}, respectively. The first case is known as the non-inverting demodulator and the second as the inverting demodulator. The relation between the average powers at the three frequencies, f_{RF}, f_{LO} and f_{IF}, can be deduced from eqns. 44 and 45 by taking

$$f_{LO} = f_1,$$

$$f_{RF+} = f_0,$$

and

$$f_{IF} = f_{RF+} - f_{LO}.$$

Then f_{LO} corresponds to $(m = 1,\ n = 0)$, f_{RF+} to $(m = 0,\ n = 1)$ and f_{IF} to $(m = -1,\ n = 1)$. For simplicity the power at these frequencies is denoted by P_{LO},

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P_{RF} and P_{IF}, respectively. Applying the Manley-Rowe power relations, the following relationships are found:

$$\frac{P_{LO}}{f_{LO}} + \frac{P_{RF}}{f_{RF}} = 0, \tag{46}$$

$$\frac{P_{IF}}{f_{IF}} + \frac{P_{RF}}{f_{RF}} = 0. \tag{47}$$

From these equations it can be seen that P_{IF} and P_{RF} are of opposite sign. Since the average power at f_{RF} flows into the nonlinear element (or is positively valued), the average power at f_{IF} and f_{LO} must flow out of the nonlinear element (or be negatively valued). Manley and Rowe found that the rate of power delivered to a specified load impedance to that absorbed by the input to be:

$$\text{Power Gain}|_{No\ Inv.} = \frac{f_{IF}}{f_{LO}}, \tag{48}$$

or less than unity for the non-inverting demodulator.

For the inverting demodulator, corresponding to $f_{LO} > f_{RF}$, the power relations reduce to:

$$\frac{P_{LO}}{f_{LO}} + \frac{P_{RF}}{f_{RF}} = 0, \tag{49}$$

and

$$\frac{P_{IF}}{f_{IF}} - \frac{P_{RF}}{f_{RF}} = 0. \tag{50}$$

Power flows into the device at f_{LO} and flows out at f_{IF} and f_{RF}. The power gain is

$$\text{Power Gain}|_{Inv} = -\frac{f_{IF}}{f_{LO}}. \tag{51}$$

The sign of the power gain shows that the converter is potentially unstable; its gain can be set arbitrarily from 0 to infinity.

The above relations show that three frequency downconverters made from a nonlinear element do not possess very good performance. If $f_{RF} > f_{LO}$, the converter will be stable but its maximum power gain is determined by the ratio of output to input frequency. On the other hand if $f_{RF} < f_{LO}$, then the downconverter can possess higher gain but is extremely unstable. Blackwell and Kotzebue have investigated the

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performance of both types of downconverters and have found stability contours for the inverting type [10].

The problem of designing a stable and high gain downconverter has been examined as well by Adams. He studied the behavior of a nonlinear reactive circuit with four and five frequencies. Signal flow was permitted at f_{LO}, f_{RF} ($f_{RF} > f_{LO}$), f_{IMAGE} and f_{IF}. The image frequency was therefor not terminated reactively. The effect of permitting signal flow at $2f_{LO}$ was investigated. Thus the diode embedding circuit ressembled a 'Y' mixer with the exception that f_{IMAGE} and $2f_{LO}$ were not shorted. Adams concluded that depending on the applied power levels and on the exact expression of the nonlinear reactance, downconversion gain exceeding unity was found with positive input conductance if power flow at $2f_{LO}$ were made possible.

Adams performed a small signal analysis of the mixer by expanding the capacitance into its Fourier coefficients, C_0, C_1, and C_2 at DC, f_{LO}, and $2f_{LO}$, respectively. If power flow at $2f_{LO}$ is not permitted (ie. $C_2 = 0$), the conversion gain at f_{IF} is unlimited but the input resistance is negative and the downconverter is unstable. If power flow at $2f_{LO}$ is permitted ($C_2 \neq 0$), unlimited conversion gain is achievable with positive input resistance at f_{IF} and f_{RF} but negative input resistance at f_{IMAGE}. For the case of no power flow at f_{IMAGE} and $2f_{LO}$, Adams' results reduce to those found by Manley and Rowe [2].

Let us now consider the case of power flow in a circuit containing a nonlinear resistor, R_B, and capacitor, C_B, in parallel. This problem is similar to that facing conventional mixer designers. Here we must distinguish between two types of analysis: one in which C_B is treated as a fixed capacitor C_F, and one in which C_B is modelled as a nonlinear element.

5.2.2 Nonlinear Resistor in Parallel with a Fixed Capacitor

We turn first to the simple case where the diode is taken to have a fixed barrier capacitance of value C_F. The main mixing element is now R_B. C_F is seen as a parasitic whose value is to be minimized as it degrades mixer performance. Mixers constructed with diodes modelled in this way will be referred to here as CF mixers. Mania and Stracca analyze the performance of single-ended mixers in the 'Y' and

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'Z' configurations where f_{IMAGE} is alternatively open or short-circuited. Real power flow (or nonzero average power flow) occurs only at three frequencies, f_{LO}, f_{RF} and f_{IF}. The diode is taken to have a nonzero spreading resistance and is considered to be sinusoidally pumped. They conclude that better performance is achieved with the 'Y' mixer whether the image is open or short-circuited than with the 'Z' mixer [47]. This result is interesting as it is contrary to that found with exponential diodes where 'Z' mixers outperform 'Y' mixers [55]. It is important as it predicts the 'Y' mixer configuration to be superior to the 'Z' configuration when the diode's barrier capacitance is non-negligible.

Other researchers have considered conversion loss to comprise three components [50,60]:

$$C_L = L_0 + L_1 + L_2$$

where L_0 is the broadband conversion loss due to the barrier resistance, L_1 is the loss incurred from the spreading resistance, r_{ser}, and L_2 is the loss due to the barrier capacitance. Their dependance on LO drive level varies: L_0 and L_2 are decreasing functions of LO drive; L_1 increases with increasing LO drive. In this formulation of the problem the capacitance is seen as degrading conversion loss by increasing the power dissipated in r_{ser} due to the shunt signal path through C_F.

5.2.3 Nonlinear Resistor in Parallel with a Nonlinear Capacitor

Finally the case most applicable to practical diode operation can be discussed. Results found are categorized first by the assumptions made and second by chronological order. Mixers with this type of diode will be referred to here as NR-NC mixers.

Three frequency model; 'Y' mixer; $r_{ser} = 0$; $g(t)$ and $c(t)$ even

The assumptions taken here are $r_{ser} = 0$; $c(t)$ and $g(t)$ are even functions; a three frequency model with power flow at f_{RF}, f_{LO} and f_{IF}; the mixer embedding circuit is a 'Y' mixer (ie. all sidebands including f_{IMAGE} are short-circuited as well as all LO

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harmonics). In 1956 Edwards analyzed the mixing performance of two nonlinear elements assuming in addition that both nonlinear elements were pumped in phase [16]. If a conjugate match were made at the signal and IF ports, then a 1 dB improvement in C_L above that of a purely exponential diode could be attained; noise temperature however was predicted to increase. If no conjugate match were established then conversion gain could be achieved but at the expense of negative output impedance and very narrow bandwidth performance. Edwards concluded that the best element for downconverters was a simple nonlinear resistor. Both analysis took f_{IF} to be 1/160 f_{RF}.

In 1964, Becker and Ernst examined the performance of these mixers principally with the goal of understanding mixer operation with high applied LO power [9].[2] They categorized mixer performance for noninverter and inverter operation with two ratios of input to output frequency, $f_{IF} = 1/4\ f_{RF}$ and $f_{IF} = 1/160\ f_{RF}$. They concluded that the non-inverting downconverter ($f_{RF} < f_{LO}$) could support the addition of more barrier capacitance to the diode model prior to obtaining a significant degradation in C_L performance if $f_{IF} = 1/160\ f_{RF}$ than if $f_{IF} = 1/4\ f_{RF}$. In the case of the inverting downconverter ($f_{RF} > f_{LO}$), they found lower values of C_B caused greater degradation in performance than for the non-inverting downconverter for both frequency conversion ratios. In addition the circuit was no longer unconditionally stable.

Four frequency model; broadband 'Y' mixer; $g(t)$ and $c(t)$ even

The following three authors examined the problem of a nonlinear capacitor in parallel with a nonlinear resistor for the case of a broadband four frequency mixer with real power flow at f_{RF}, f_{IF}, f_{IMAGE}, and f_{LO}. The embedding circuit was that of a 'Y' mixer with the exception that f_{IMAGE} was not short-circuited; instead the match at f_{IMAGE} was identical to that at f_{RF}. $g(t)$ and $c(t)$ were taken to be even functions of time.

In 1948 Torrey and Whitmer examined mixer operation for nonzero spreading resistance and found that if r_{ser} were small then conversion gain would be possible.

[2]Becker and Ernst wished to achieve greater mixer dynamic range and reduce intermodulation products by driving the mixer with greater LO power.

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Noise temperature was predicted to rise. If, however, the impedance at f_{IF} was kept positive, then the conversion loss could improve substantially (remaining positive) and the noise temperature would be only slightly degraded from operation without C_B [68]. An experiment by H. Q. North is mentioned in which conversion gain was obtained from a diode mixer.

In 1957 Macpherson examined the performance of a mixer diode with non-zero spreading resistance, nonlinear barrier resistance and nonlinear capacitance [46]. He stressed that the positive effects of barrier capacitance could be realized in mixers without necessarily creating negative IF conductance, ie. if a mixer with a NR-NC diode was unconditionally stable and possessed positive IF conductance it was due to the fact that C_B was not sufficiently nonlinear or that the spreading resistance was too large to create stability problems.

Macpherson did not want to restrict the number of sideband frequencies in his mixer analysis as he believed that the low level sideband signals were necessary to accurately predict low conversion loss performance. But as no solution of his equations was possible without extensive problem simplification, he was forced to accept the same simplifying assumptions that Torrey and Whitmer had adopted. Two cases isolated by Macpherson are of interest to us. One concerned the situation where $r_{ser} = 0$ and equal admittance were applied at f_{RF} and f_{IMAGE}. Regions of negative IF conduction were then associated with arbitrarily high gain. Another case of interest occured when $r_{ser} = 0$ and f_{IMAGE} is short-circuited by the embedding circuit. Then negative IF conductance is found and arbitrarily low conversion loss is possible for operation above a specified frequency.

In 1970 Liechti ranked mixer performance for three mixer circuits, one with a purely resistive circuit, ie. a NR circuit, one with a nonlinear resistor and fixed barrier capacitor, a NR-CF circuit, and lastly one with a nonlinear resistor and nonlinear capacitor in parallel, a NR-NC circuit [41]. For the analysis r_{ser} was set to zero. He concluded that if no bias were applied and if the LO power were kept below 0.2 mW (or $I_{rectified} \leq 0.6$ mA) then the conversion loss performance of the three mixer types could be ordered as follows:

$$C_{L_{NR-NC}} < C_{L_{NR}} < C_{L_{NR-CF}}.$$

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The noise figure performance of these mixers was ranked by:

$$NF_{NR-NC} > NF_{NR-CF} > NF_{NR}.$$

Liechti's experimental results showed that the C_L of a silicon Schottky barrier diode, operated at 3 GHz and driven by a 0.1 mW LO, possessed a lower C_L than its purely resistive counterpart. His theory postulated that this difference in C_L could be as much as 1 dB. The NF of the mixer was unchanged. Liechti's experimental mixer had a C_L of 3.5 dB and a NF of 5.7 dB (including a 1.5 dB IF amplifier NF).

The application of bias permitted the NR-NC mixer to have conversion gain, but the optimum value for R_S became high enough that matching it would cause the circuit bandwidth to become narrow. He also predicted that NF_{NR-NC} would become comparable to NF_{NR}.

'Z' mixer

Lastly we present the experimental results obtained by Dragone in 1972 on a 'Z' mixer (all sideband and $n \geq 2$ harmonic frequencies are open-circuited)[15]. Dragone analyzed the double sideband noise temperature of 'Z' mixers and confirmed his analytic prediction experimentally. Using GaAs diodes ($r_{ser} = 4\Omega$, $C_{j0} = 1.2$ pF) with a bias voltage of 10 V at an f_{LO} of 1.25 GHz and an f_{IF} of 2 MHz, conversion loss and double sideband noise figure were measured for various input matches. The resultant noise figure has a minimum of 0.7 dB and a maximum of 2.3 dB with conversion loss registered in the first case and conversion gain in the latter.

5.2.4 Application of Prior Research to our Design Problem

The work described above can be summarized with regard to the design of direct conversion mixers by considering the effect of using a diode with nonlinear C_B, R_B, and nonzero r_{ser} on three mixer parameters, conversion loss, noise figure and stability. Presentation of the power flow equations derived by Manley and Rowe are necessary in order to understand the importance of including power flow at different frequencies into the analytic formulation of the problem. For, although Manley and

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Rowe initially predicted poor NC mixer performance: conversion loss on the order of f_{IF}/f_{LO} for non-inverting downconverters and arbitrary conversion loss with conditional stability for inverting downconverters, it was understood later that conversion gain with positive conductance could be achieved by a NC mixer. Adams considered the performance of a NC mixer with non-even $c(t)$ with a five frequency model (f_{RF}, f_{IF}, f_{IMAGE}, f_{LO}, and $2f_{LO}$) and demonstrated that conversion gain from circuits with positive real conductance was consistent with the Manley-Rowe equations.

The following researchers concerned themselves with the performance of NR-NC circuits. Edwards, Becker and Ernst considered a three frequency model (f_{RF}, f_{IF}, and f_{LO}). Analyzing a 'Y' mixer they found that the inclusion of small values of C_{j0} did not degrade C_L or destabilize the circuit. In fact, Edwards found that inclusion of C_B might reduce C_L at most by 1 dB but he predicted NF would increase. Torrey, Whitmer, Macpherson and Liechti all examined a broadband 'Y' mixer using a four frequency model (f_{RF}, f_{IF}, f_{IMAGE}, and f_{LO}) and assuming $c(t)$ and $g(t)$ to be even functions of time. The first three found that conversion gain was achievable at the expense of mixer stability. Liechti found that, for low applied LO levels and no applied bias, conversion loss could be improved by as much as 1 dB although NF performance would be degraded compared with the NR mixer. Conversion gain and comparable NF performance to a NR mixer could be achieved without loss of mixer stability if a bias voltage were applied. Liechti's article provides a good comparison of the performance of NR, NR-CF, and NR-NC mixers. Finally Dragone has studied operation of a 'Z' mixer with a shorted image frequency and experimentally confirmed that good conversion performance is possible with low noise temperature.

Because many of the assumptions made by these authors do not hold true for practical mixers (ie. real power flow at a limited number of frequencies, $r_{ser} = 0$, $c(t)$ and $g(t)$ are even), it is difficult to predict the range of possible mixer performance with NR-NC diodes and equally difficult to find design rules to optimize mixer performance. In the remainder of this chapter, we will try to predict practical mixer performance and attempt to develop guidelines for the design of a circuit which improves upon the conversion loss and noise figure achieved by a purely resistive mixer circuit without sacrificing circuit stability. The analytic conclusions developed by the

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preceeding authors and the experimental results found by Torrey, Whitmer, Liechti and Dragone lead one to believe that this may be possible.

5.3 Phasing Network Development

5.3.1 Operation of Ideal Phasing Circuit

In Section 4.2.3 the barrier capacitance was assumed to have a fixed value, $\langle C_B \rangle$ or C_{j0}, in order to conjugately match the source to the diode. An inductor in parallel with R_S was used to provide this match; its value was varied until $C_{L_{min}}$ was reached. In this chapter we would like to take advantage of C_B and its nonlinearity to further reduce C_L using the basic 'RM' circuit derived in Section 4.2.2 as our starting point.

Let us return to the ideal switch analogy to develop a model by which the barrier capacitance can be used to reduce conversion loss. The ideal switch mixer of Fig. 21(a) is modified as follows: a fixed capacitor of value C_F is placed accross the switch; R_L is replaced by the parallel combination of R_L and C_{LD} to reflect the 'RM' circuit design; and an inductor, L_1, is placed in series with the switch-capacitor assembly to inductively match to C_F. The modified switch circuit is depicted in Fig. 52(a). The switch now depicts the impedance presented by the diode's barrier resistance. The diode's barrier capacitance is modelled by a fixed capacitor. In this simplified circuit, the phasing circuit is represented by one element, L_1. For simplicity we assume that $f_{RF} \sim f_{LO} = f_c$ and set L_1 to equal $(1/\omega_c^2\, C_F)$. The current source, I_S, is set equal to $I_{RF}\, cos(\omega_c t)$. V_j corresponds to the voltage accross C_F or the 'diode's' junction voltage.

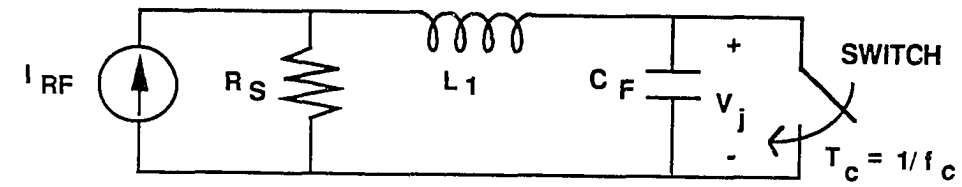
First we consider the circuit's operation without the switch. Then, because L_1 and C_F have been chosen to resonate at ω_c,

$$I_{L_1} = I_S = I_{RF}\, cos(\omega_c t),$$

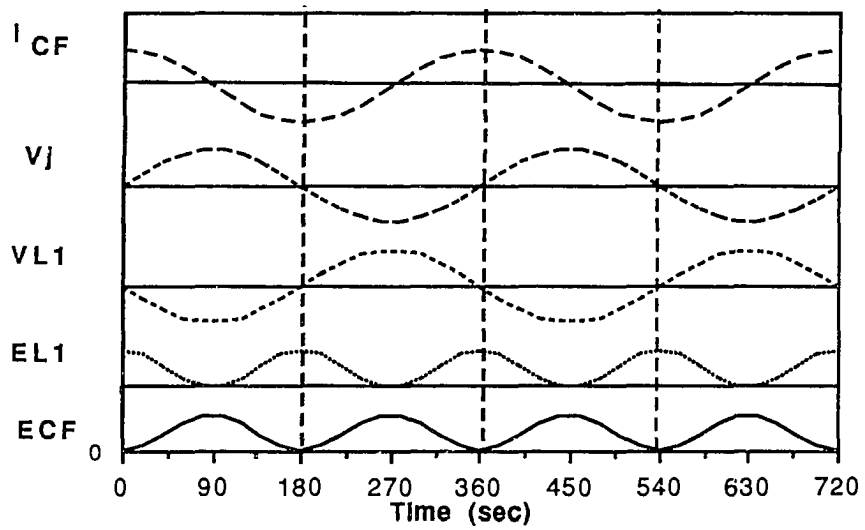
$$V_j = \frac{I_S}{j\omega_c C_F},$$

$$V_{L_1} = -V_j$$

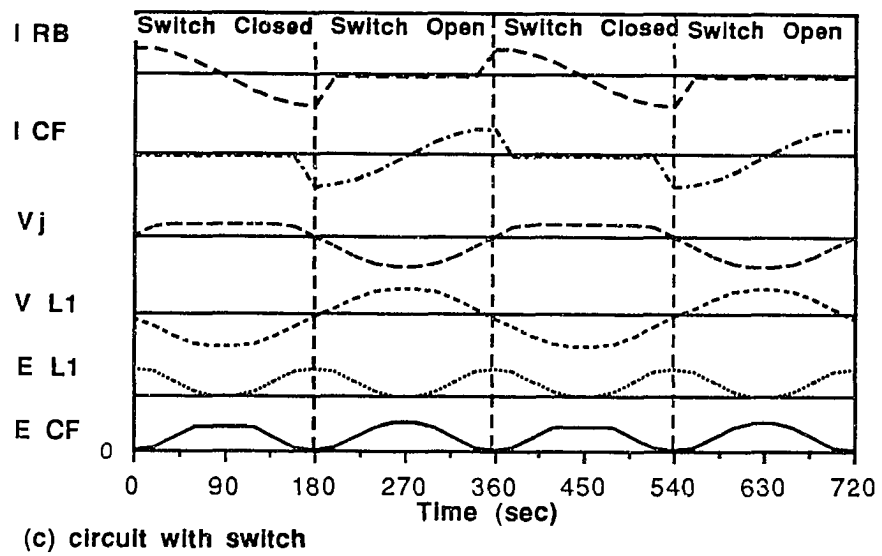
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(a) circuit diagram



(b) circuit without switch



(c) circuit with switch

Figure 52: Derivation of the phasing network - switch analogy.

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and

$$I_{R_S} = 0.$$

The waveforms of I_{C_F}, V_j, V_{L_1} are plotted in Fig. 52(b) along with the energy stored in C_F and L_1. For the resonant circuit, no current travels in R_S and thus $I_{RF} = I_{L_1} = I_{C_F}$. RF energy is built up first in C_F, then L_1, then C_F as time progresses.

Next we consider operation when the switch is in place. The switch is meant to resemble the purely resistive diode, ie. r_{ser} and R_B. The state of the switch, either 'ON' or 'OFF', corresponds to the impedance presented by r_{ser} and R_B, low if the switch is 'ON' and high if it is 'OFF'. The magnitude of the LO sets the state of the switch as it sets the state of the diode in a mixer circuit. The switch period is T_c $(1/\omega_c)$; its duty cycle is shown to be 50%. When the switch is 'ON', the diode is assumed to be conducting through R_B and its junction voltage is taken to be equal or greater than its turn-on voltage. The current in the diode then flows through r_{ser} and R_B. When the switch is 'OFF', no current flows through the purely resistive diode however current flows through C_F. This element is meant to model the diode's barrier capacitance.

The addition of the switch will then cause the following major changes to the circuit waveforms: (1) the voltage accross the switch, V_j, will be zero when the switch is closed, corresponding to the diode's junction voltage having attained the turn-on voltage; (2) I_{C_F}, which was equal to I_S in the resonant circuit, will now be zero when the switch is 'ON' and $I_{C_F} \sim I_S$ when the switch is 'OFF'. The latter implies that the current in the switch will be approximately equal to I_S when the switch is 'ON' and zero when the switch is 'OFF' assuming, as before, that $I_{R_S} = 0$. As will be subsequently shown, this assumption is reasonable to arrive at a rough idea of the circuit's performance.

The waveforms in this circuit are shown in Fig. 52(c) under these assumptions. Shown in the figure are the current in the switch, denoted by I_{R_B}, and that in C_F which in this analogy are roughly equivalent to the currents I_{d_r} and I_{d_c} that one would expect to see in a mixer circuit designed with this phasing circuit. Looking at the energy pattern the following cyclic pattern can be seen in the RF energy: when the switch opens, the RF energy is transferred from L_1 to C_F; at the time when the

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switch begins to close again the RF energy is completly stored in L_1; when the switch is closed the current in the inductor can be passed through the switch (or R_B) to the load. The idea is to use this energy storage pattern so that the maximum RF current is available to course through the switch once it is closed. The goal of the phasing circuit is to set $E_{C_F} = 0$ and $E_{L_1} = E_{L_{1max}}$ when the LO drive closes the switch.

In a real mixer circuit, the voltage and current waveforms are far more complex than those depicted in Fig. 52 however the sequence of events parallels those in the switch. This sequence is detailed in Table 14. In it, the period of the RF signal has been divided in two parts corresponding to whether the voltage accross the diode is negative or positive. The phasing circuit effects on the circuit should possess this pattern when the RF and LO are in-phase. The pattern repeats itself every cycle of the RF: two cycles are shown in the table. First the RF energy pattern in the resonant circuit created by setting $R_B = 0$ is listed, then the pattern when the diode (R_B, $C_B \neq 0$) is in place is given. The goal of the phasing circuit is to coincide the time during which the RF energy is stored in C_B with the 'OFF' time of the diode. Ideally the RF energy, during the cycle in which the RF and LO are in phase, would then flow as follows. As the LO and RF are becoming more negatively valued, the diode would turn 'OFF' and the RF energy would flow into C_B for storage. As the LO and RF become less negative the RF energy would be transferred to L_1 into which component the RF current would flow. When most of the RF energy is transferred to L_1, the LO voltage will reach the diode turn-on voltage and the path to ground through R_B would slowly become more attractive. The stored RF current in L_S would then flow through R_B to ground (or to the parallel impedance formed by R_L and C_{LD}) as the RF and LO voltage reached their maximum positive swings and began decreasing. Once the LO voltage falls below the diode turn-on voltage, the diode would turn 'OFF' and the cycle of RF energy storage would recommence. The structure of this cycle changes slowly as the LO and RF move out-of-phase.

The phasing circuit, now simply composed of the inductor L_S can be placed in series with the diode, as done in the switch model described above, or in parallel with R_S, as done previously in the simple matching circuit. This last method is discussed in Section 4.2.3 (see page 104). Both options are shown in Fig. 53 for the case where

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Table 14: Sequence of Events Orchestrated by Phasing Network
(f_{LO} and f_{RF} in-phase)

Circuit Condition	First RF Cycle		Second RF Cycle	
	0 - $1/2T_{RF}$	$1/2T_{RF}$ - T_{RF}	0 - $1/2T_{RF}$	$1/2T_{RF}$ - T_{RF}
No Diode in Circuit ($C_B = C_F$; $R_B = 0$) RF energy stored in:	C_B	L_1	C_B	L_1
Diode in Circuit (C_B, $R_B \neq 0$)				
V_j	Negative	Positive	Negative	Positive
Diode Condition	OFF	ON	OFF	ON
RF energy stored in:	C_B	$L_S \Rightarrow R_B$	C_B	$L_S \Rightarrow R_B$

the phasing circuit is a single inductor. The series match is chosen over the parallel match as it will enable a lower value of R_S to be used and will allow us to model the application of bias in the circuit easily. This can be seen by considering the values of R_S and L_1 necessary to match to a diode, modelled simply as a parallel combination of $\langle R_B \rangle$ and $\langle C_B \rangle$. In the series case,

$$R_{S_1} = \frac{\langle R_B \rangle}{1 + (\omega_c \langle C_B \rangle \langle R_B \rangle)^2}, \tag{52}$$

and

$$L_{11} = \frac{\langle C_B \rangle (\langle R_B \rangle)^2}{1 + (\omega_c \langle C_B \rangle \langle R_B \rangle)^2}. \tag{53}$$

In the parallel case,

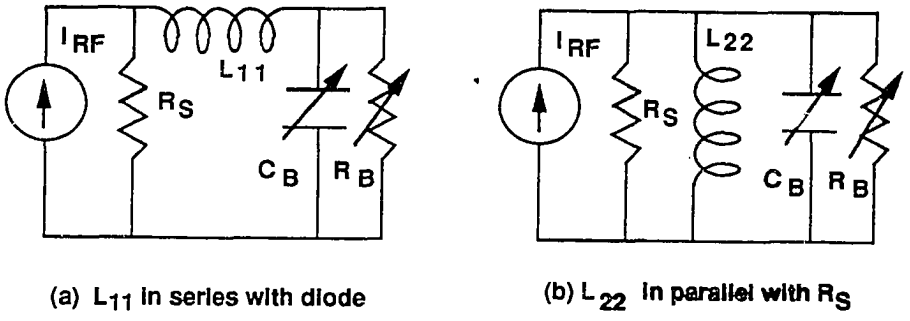
$$R_{S_2} = \langle R_B \rangle, \tag{54}$$

and

$$L_{22} = \frac{1}{\omega_c{}^2 \langle C_B \rangle}. \tag{55}$$

The phasing circuit location resulting in the lowest R_S is chosen for use. This will enable the design of a mixer whose source impedance for best C_L is close to the low impedance of the UHF antenna impedance. It will also facilitate the design of a mixer

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(a) L_{11} in series with diode (b) L_{22} in parallel with R_S

Figure 53: Placement of phasing circuit in a 'RM' mixer.

which can produce high impedance transformations from input to output as required for the direct conversion mixer. Also the use of a series phasing circuit (with L_1 as one of the components) rather than a parallel phasing circuit will allow the application of bias to be modelled by a bias current applied in parallel with I_{RF}. This is far simpler than applying it through an RF choke as would be required if the parallel placement had been chosen.

From these considerations, it has been determined that the phasing circuit will be placed in series with the diode, that its goal is to optimally time the transfer of RF energy from C_B (when the diode is 'OFF') to L_1 (when the diode is just about ready to turn 'ON') and finally to R_B (when the diode is 'ON') during the cycle of the LO when the LO and RF are in-phase. This pattern of energy transfer will change as the phase between the LO and RF change but as minimizing C_L is achieved by maximizing $\langle I_L \rangle$ at T_1, it is the performance of the circuit at during this cycle that concerns us the most. The phasing circuit will not consist simply of L_1, however the raison d'être for the circuit has been derived using this simple model for the phasing circuit.

The effectiveness of the phasing circuit will be gauged by the energy pattern in the circuit, by minimizing I_{R_S}, and by maximizing $\langle I_L(T_1) \rangle$. The key to maintaining this pattern with a real diode and complete mixer circuit is to develop a simple phasing network that will allow the RF energy to be transferred between components as the diode changes state.

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5.3.2 The Design of the Phasing Circuit

The structure of the phasing circuit was developed to incorporate matching to $Z_{in}^{*}(f_{RF})$ as well as to produce the circuit goals described above. The phasing circuit chosen is depicted in Fig. 54. The source inductance, L_S, used to short-circuit the diode and load impedance is not shown. Initial mixer design can be performed without it as R_S is usually much lower than R_L and hence presents a low impedance to the diode at f_{IF}. The criteria for setting the values of R_S, L_1, C_2, and L_2 are:

$$Z_S(f_{RF}) = Z_{in}^{*}(f_{RF}), \tag{56}$$

$$Z_S(f_1) = \infty \tag{57}$$

where $f_1 = 2f_{LO}$ or $3f_{LO}$, and,

$$Z_S(f_2) = 50\Omega \tag{58}$$

where $f_2 = 7f_{LO}$. The values of R_S, L_1, C_2, and L_2 so designed start the iterative procedure of optimizing the mixer circuit. Eqns. 57 and 58 reflect the decision to resistively terminate all high order LO harmonics and high order sidebands as done for the 'RM' mixer. But the lower harmonics and lower frequency sideband power is designed to be reflected back into the nonlinear diode elements for reconversion to the wanted output frequency, f_{IF}. f_1 is arbitrarily set at $2f_{LO}$ and f_2 is set at $7f_{LO}$ for the initial circuit simulation. After the phasing circuit is in place, R_S, L_1, C_2, and L_2 are varied to optimize $Z_S(f_{RF})$, f_1 and f_2.

L_S and C_S are added at the final mixer iteration; they are chosen so that

$$Z_S(f_{IF}) \sim 0.$$

The initial values of the phasing circuit components can be found by expressing the source impedance, $Z_S(\omega)$, in terms of the mixer circuit components. $Z_S(\omega)$, as defined in Fig. 54, can be written as:

$$Z_S(\omega) = R_S + \frac{j\omega L_1(1-\omega^2 L_2 C_2)}{[1-\omega^2 C_2(L_1+L_2)]}.$$

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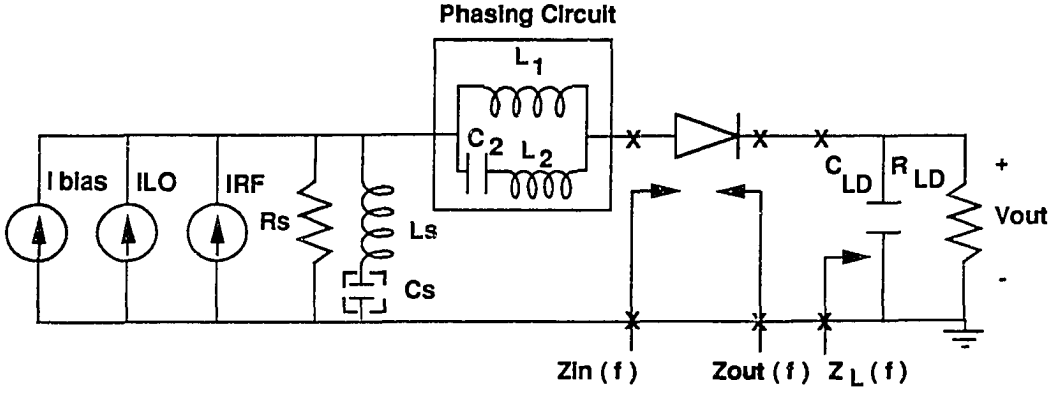


Figure 54: Phasing circuit location in a single-ended mixer.

From this equation f_1 can be determined to be:

$$f_1 = \frac{1}{2\pi\sqrt{C_2(L_1 + L_2)}},$$

at which point $|Z_S(f_1)| = \infty$ and $\angle Z_S(f_1) = 90°$. Similarly f_2 can be given by:

$$f_2 = \frac{1}{2\pi\sqrt{L_2 C_2}}$$

at which point $|Z_S(f_2)| = R_S$ and $\angle Z_S(f_2) = 0°$.

Given an input impedance at f_{RF}, $Z_{in}(f_{RF})$, eqns. 56, 57 and 58 translate into the following requirement on the phasing network elements:

$$R_S = Re\{Z_{in}(f_{RF})\}, \tag{59}$$

$$L_1 = -Im\{Z_{in}(f_{RF})\}\left(1 - \frac{{\omega_{RF}}^2}{\omega_1}\right), \tag{60}$$

$$C_2 = \frac{\left(\frac{\omega_2}{\omega_1}\right)^2 - 1}{{\omega_2}^2 L_1}, \tag{61}$$

$$L_2 = \frac{1}{{\omega_2}^2 C_2}. \tag{62}$$

The component values can be determined once f_1 and f_2 are set and $Z_{in}(f_{RF})$ has been determined or estimated. The value of $Z_{in}(f_{RF})$ used can be taken from the

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simulated results for the mixer run prior to the addition of the matching circuit or from the simple inductive matching circuit run. It is not necessary to have an exact value for $Z_{in}(f_{RF})$ for this initial run as this run is the starting point for a series of phasing circuit simulations and because $Z_{in}(f_{RF})$ varies with the circuit's source impedance. In general f_1 and f_2 are the last parameters iterated as mixer performance is not very sensitive to changes in these values.

5.4 Single Ended Mixer Design

5.4.1 Optimization Strategy

The overall optimization plan consists of several steps, the central core of which are iteratively performed until C_L converges to a minimum value or until the improvement in C_L with each cycle becomes insignificant. At that point the optimization procedure is considered to be completed.

The first step is intended to set a starting point for speedy optimization. In this step, $Z_{in}(f_{RF})$ is estimated from previous runs and a phasing circuit is designed to produce $Z_S(f_{RF}) \sim Z_{in}^*(f_{RF})$ with f_1 and f_2 set to $\sim 2f_{LO}$ and $\sim 7f_{LO}$, respectively. After this run is analyzed, if $Z_{in}^*(f_{RF})$ is not close to $Z_S(f_{RF})$, the run is iterated until this condition is met. The second step involves optimizing the load impedance to minimize C_L (with a concommittant change in C_{LD} if necessary) and adjusting the drive conditions, I_{LO} and I_{bias}. In this step, $|Z_S(f_{RF})|$, $\angle Z_S(f_{RF})$, R_L, I_{bias}, and I_{LO} are optimized. Changes in these variables are repeated until $C_{L_{min}}$ has been found. Then f_1 is varied. It has been experimentally found that further circuit element variation does not improve C_L and thus no need for reiterating $|Z_S(f_{RF})|$, $\angle Z_S(f_{RF})$, R_L, I_{bias}, and I_{LO} exists. Finally f_2 is set to ∞, ie. L_2 is set to 0, to simplify the circuit. For all circuits tested, C_L was either unaffected or reduced by at most 0.2 dB by this move. L_S and C_S are then added to the source impedance as shown in Fig. 14.

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5.4.2 Performance Achieved with a Diode Having C_{j0} = 0.25 pF

First Iteration Cycle - Application of I_{bias}

To examine the optimization procedure and to arrive at guidelines for mixer optimization, the changes in mixer performance arising during the first iterative round will be examined on a mixer with a C_{j0} of 0.25 pF.

The simulation run described in Section 4.2.3 in which C_B was introduced in the diode model without any matching circuit is used as a beginning. C_L was found to be 5.5 dB. Table 8 is used to find $Z_{in}(f_{RF}) = 731\Omega \angle -60°$. The phasing circuit elements are determined by setting $f_1 = 2f_{LO}$, $f_2 = 7.5f_{LO}$ and $Z_S(f_{RF}) = 365\Omega + j633\Omega$. The initial circuit elements are then

$$\begin{aligned} R_S &= 365\Omega, \\ L_1 &= 0.084\mu H, \\ C_2 &= 0.086pF, \\ L_2 &= 6.48nH \end{aligned}$$

for operation at f_{RF} = 909 Hz and f_{LO} = 900 Hz. I_{LO}, R_L, and Z_S are then varied to find the local $C_{L_{min}}$. This results in I_{LO} being increased from 4 mA to 7 mA and R_L increased from 1K to 1.5KΩ. After these changes, the following circuit elements are obtained:

$$\begin{aligned} R_S &= 260\Omega, \\ L_1 &= 0.094\mu H, \\ C_2 &= 0.082pF, \\ L_2 &= 6.77nH. \end{aligned}$$

Figures 55 and 56 show the mixer's large signal and small signal performance, respectively. In Fig. 55(a) one cycle of f_{IF} is given; in Fig. 55(b), $V_d(t)$, $V_{out}(t)$, $I_d(t)$,

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and $I_{d_r}(t)$ are shown; and in Fig. 55(c), $I_{d_c}(t)$, $C_B(t)$, $Q_{C_B}(t)$ are depicted. From this data, the average diode current at T_1, T_2, T_3, and T_4 are calculated to be $711\mu A$, $660\mu A$, $615\mu A$, and $668\mu A$ respectively. Conversion loss can be found from $\langle I_d(T_1)\rangle$ and $\langle I_d(T_3)\rangle$ according to eqns. 12 and 13. T_{NL} and T_{TON} are found to be $0.09T_{LO}$ and $0.34T_{LO}$, respectively. Fourier decomposition of V_{out} can be used to find C_L and $Z_{in}(f_{RF})$: C_L is 4.99 dB and $Z_{in}(f_{RF})$ is calculated to be $861\Omega \angle -72°$.

Application of the phasing circuit and the initial optimization has only reduced C_L by 0.5 dB, however the action of the phasing circuit can be clearly seen in Fig. 56. Fig. 56(a) gives the energy flow in each component due to the LO and RF signals whereas Fig. 56(b) shows the calculated energy flow due to the RF only. (See Section 4.2.3 for details of graph calculation.) Both Fig. 56(a) and 56(b) show the energy is being stored in C_B when the diode is 'OFF', transferred to L_1 prior to the diode turning 'ON', and finally moving to R_B when the diode is 'ON'. Fig. 56(c) can be examined to see the division of RF current among the source components, R_S, L_1, and C_2:

$$I_{RF} = I_{R_S} + I_d$$

$$I_d = I_{L_1} - I_{C_2}$$

When the diode is 'ON', which is only about 1/3 T_{LO}, only 1/2 I_{RF} goes to R_B. The other 1/2 I_{RF} flows in R_S and is lost to the conversion process. The mixer circuit must be optimized to increase the share of I_{RF} that is transferred to the diode when it is 'ON', ie. to increase the current through R_B. To do this, the mixer drive level will now be adjusted to increase T_{TON} while keeping $V_{d_{min}}$ low enough to drive C_B into a highly nonlinear state. This will be accomplished by applying I_{bias} and increasing I_{LO} to keep $V_{d_{min}}$ to -2 or -3 V. The bias could have been adjusted to achieve this condition prior to adding the phasing circuit however it would then have been difficult to assess the correct drive levels to produce the desired energy pattern.

The effect of bias and drive variations on mixer C_L are shown in Fig. 57 where C_L is plotted vs. applied bias for various values I_{LO}. Also plotted is T_{TON}. For each I_{LO} there is a preferred I_{bias} for minimum C_L. As I_{LO} is increased, the optimum I_{bias} increases. This can be easily explained by noting that the I_{bias} currents used are

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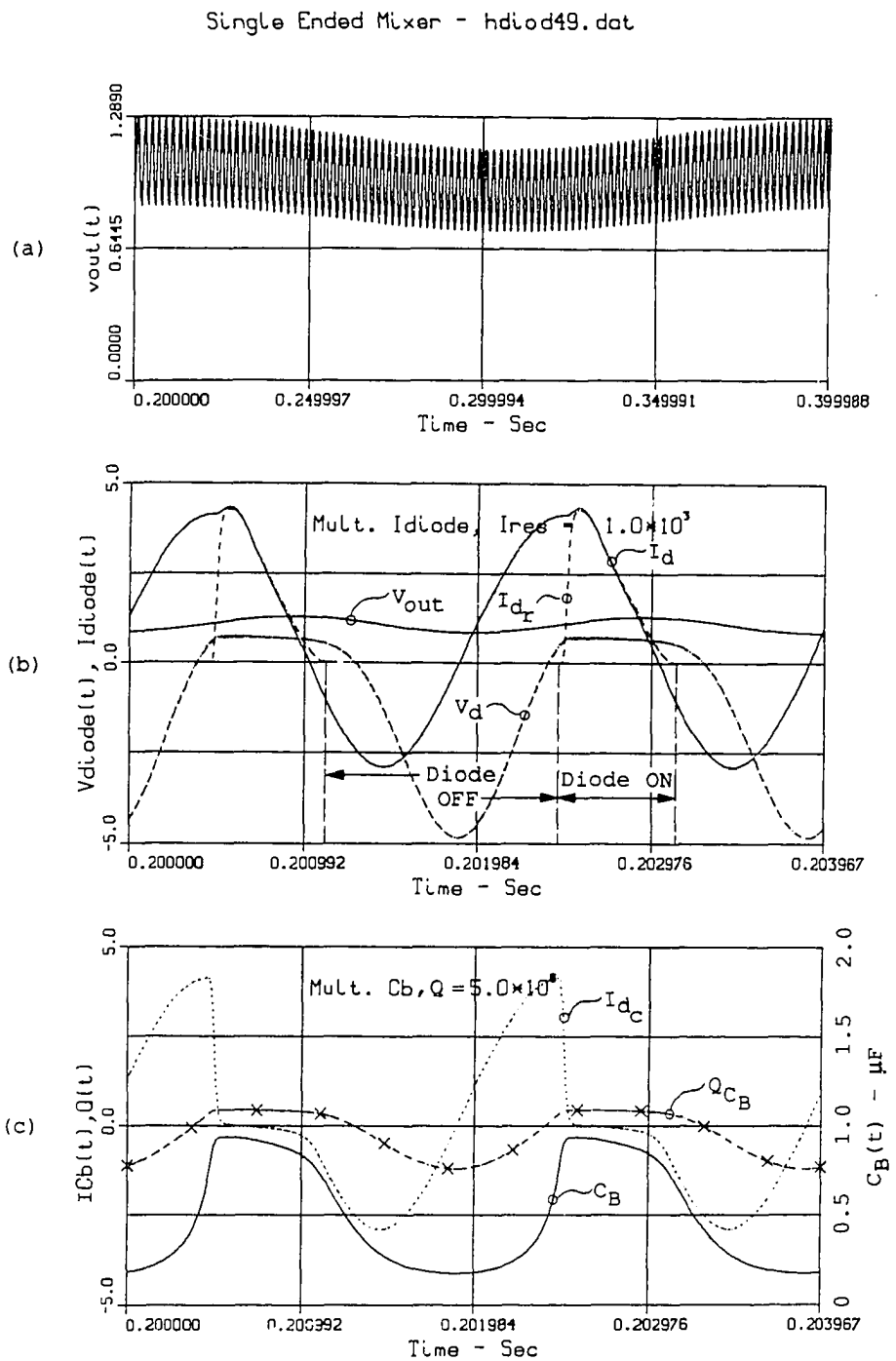


Figure 55: Large-signal waveforms in single-ended mixer - initial phasing circuit in place.

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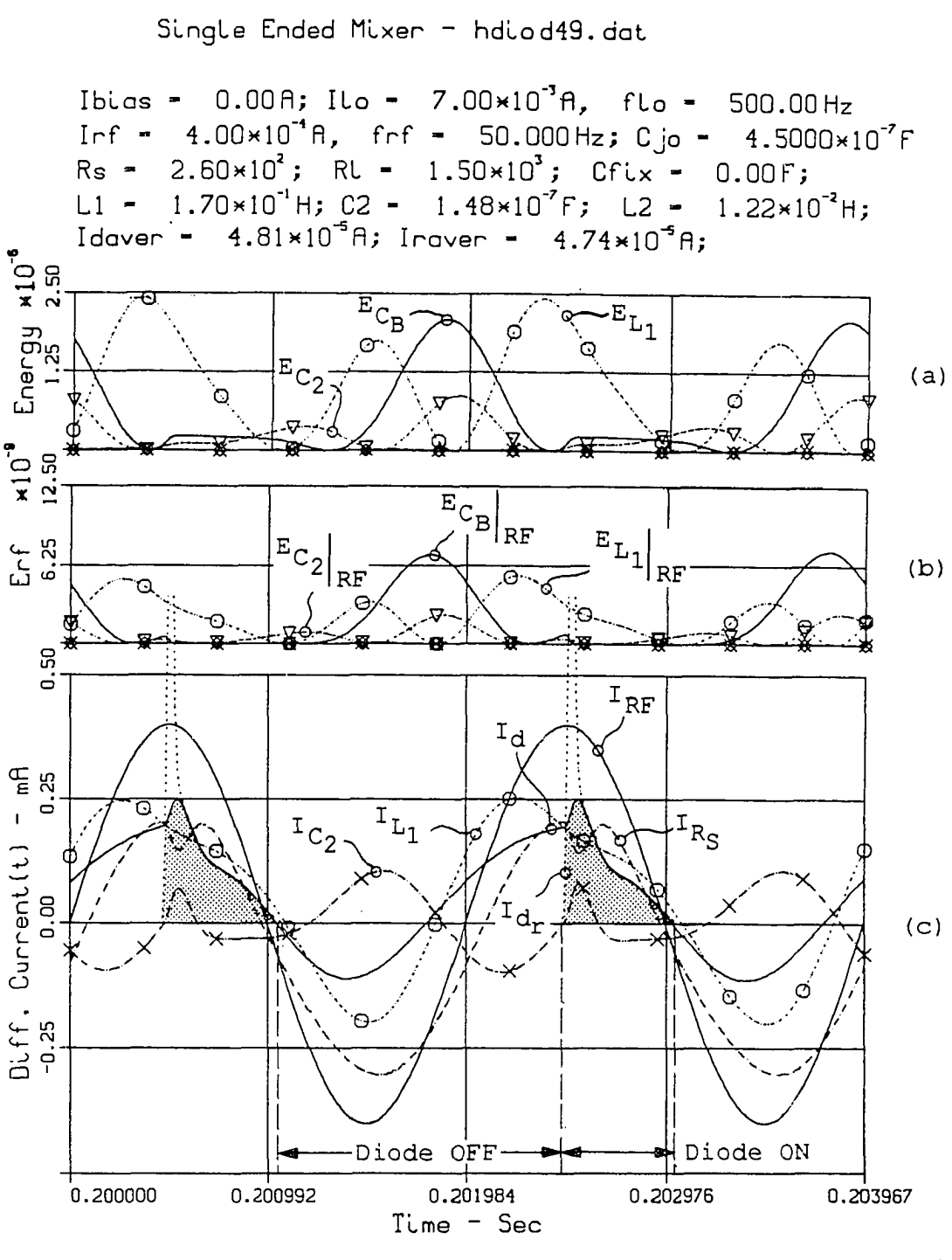


Figure 56: Energy waveforms and small-signal currents in single-ended mixer - initial phasing circuit in place.

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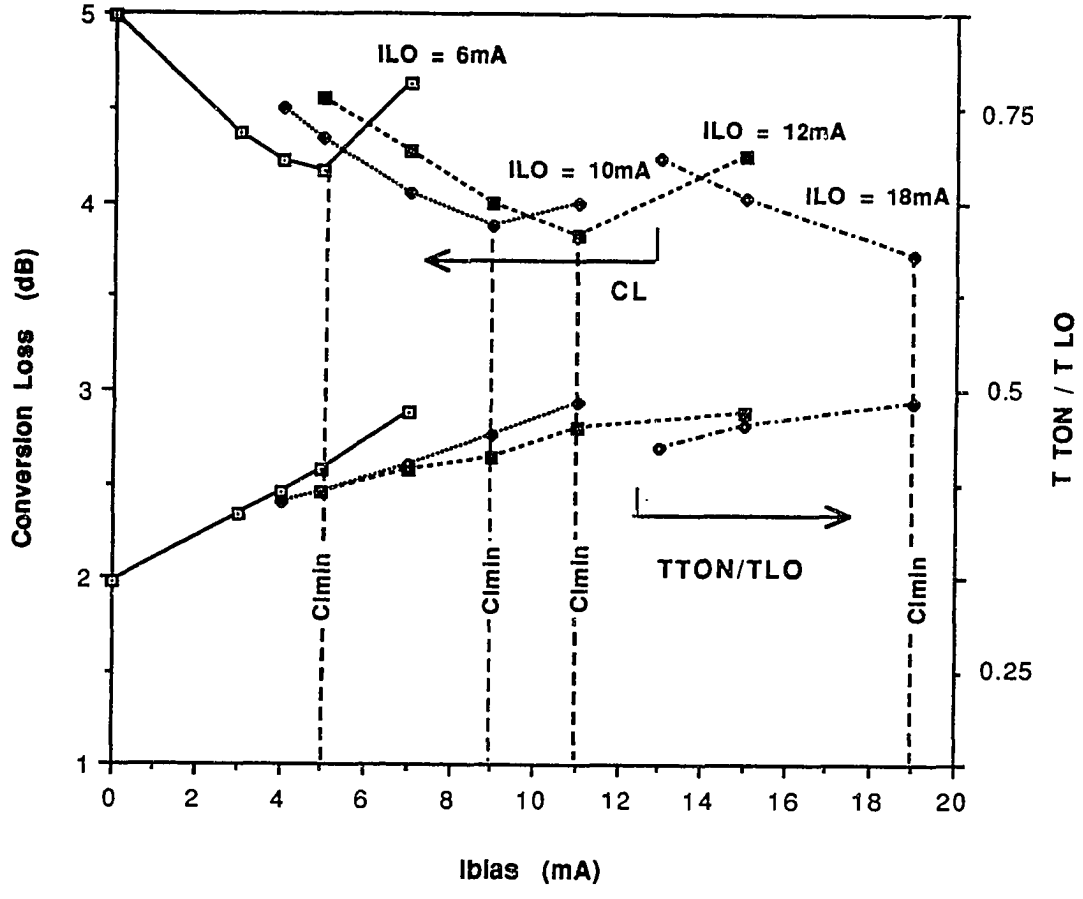


Figure 57: Conversion loss vs. I_{bias} for several values I_{LO}.

enough to keep the diode fully 'ON' and thus increasing I_{LO} is necessary to turn it 'OFF' for $0.5T_{LO}$. The appropriate combination of I_{bias} and I_{LO} causes C_L to drop from 5.0 dB, when I_{bias} = 0mA and I_{LO} = 7mA, to 3.7 dB when I_{bias} = 19mA and I_{LO} = 18mA.

It is interesting to note that although the optimal value for T_{TON} tends to 0.5 T_{LO} for large values of I_{LO}, setting T_{TON} equal to 0.5 T_{LO} at lower values of I_{LO} does not guarantee that $C_{L_{min}}$ will be reached. For example, when I_{LO} is 6mA, $C_{L_{min}}$ is realized with an I_{bias} of 5mA; T_{TON} is then 0.42 T_{LO}, not when I_{bias} necessary to set T_{TON} to 0.50 T_{LO} is used. For large values of I_{bias}, ie. I_{bias} = 19 mA, I_{LO} = 18 mA, T_{TON} approaches 0.5 T_{LO}.

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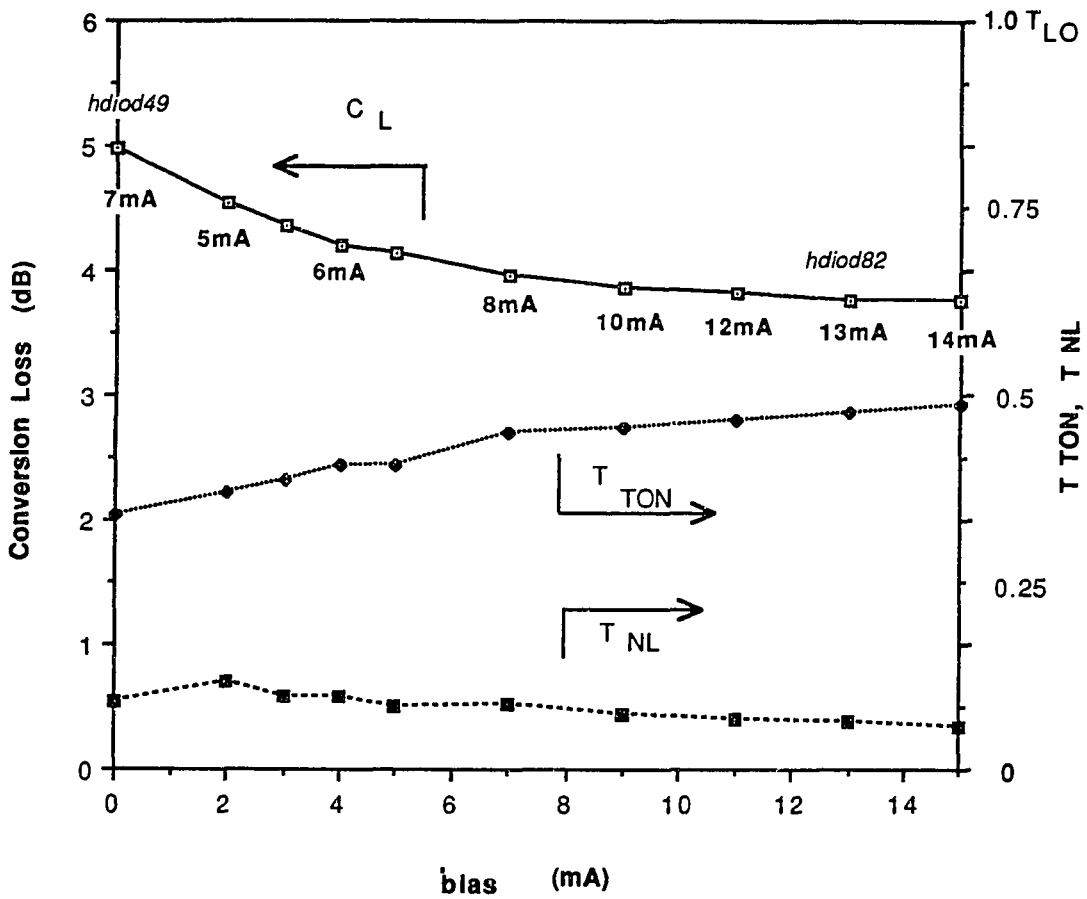


Figure 58: Optimum C_L vs. I_{bias} for various values I_{LO}.

Figure 58 shows the optimum C_L for various values I_{bias}. The value of I_{LO} required to achieve this conversion loss is noted by each point. T_{TON} and T_{NL} are also plotted in Fig. 58. To stress that the phasing circuit is not providing a conjugate match to the diode at f_{RF}, Table 15 gives $Z_{in}(f_{RF})$ at optimum C_L for several values of I_{bias} and I_{LO}. As these runs vary only by the values of I_{bias} and I_{LO}, Z_S remains at 760 Ω at 70°. The names of the SPICE runs to obtain each result are shown beneath the corresponding I_{bias} values. It can be clearly seen that while $\angle Z_S(f_{RF})$ is close to $\angle Z_{in}^*(f_{RF})$, $|Z_S(f_{RF})|$ is not close to $|Z_{in}^*(f_{RF})|$.

A reasonable pair of I_{LO} and I_{bias} must be picked for operation of the mixer. The run *hdiod82* with I_{bias} = 13 mA and I_{LO} = 13 mA possesses a C_L of 3.78 dB which

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Table 15: $Z_{in}(f_{RF})$ at $C_{L_{min}}$ for Several Values of I_{bias} and I_{LO} ($Z_S = 760\Omega \quad \angle 70°$)

Run name	I_{bias}	I_{LO}	C_L	$Z_{in}(f_{RF})$
hdiod49	0 mA	7 mA	4.99 dB	861 Ω -72°
hdiod55	2 mA	5 mA	4.56 dB	730 Ω -72°
hdiod59	3 mA	6 mA	4.37 dB	722 Ω -71°
hdiod62	4 mA	6 mA	4.22 dB	680 Ω -71°
hdiod64	5 mA	8 mA	4.15 dB	716 Ω -70°
hdiod71	7 mA	8 mA	3.98 dB	644 Ω -70°
hdiod74	9 mA	10 mA	3.88 dB	655 Ω -69°
hdiod77	11 mA	12 mA	3.83 dB	667 Ω -69°
hdiod82	13 mA	13 mA	3.78 dB	648 Ω -69°
hdiod84	15 mA	14 mA	3.77 dB	630 Ω -69°

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is fairly close to the optimum achievable with unlimited drive levels. Figures 59 and 60 give the mixer's large signal and small signal performance, respectively.

In Fig. 59(a) one cycle of f_{IF} is given; in Fig. 59(b), $V_d(t)$, $V_{out}(t)$, $I_d(t)$, and $I_{d_r}(t)$ are shown; and in Fig. 59(c), $I_{d_c}(t)$, $C_B(t)$, $Q_{C_B}(t)$ are depicted. The average diode current at T_1, T_2, T_3, and T_4 are calculated to be 2.4 mA, 2.35 mA, 2.29 mA, and 2.35 mA respectively. Conversion loss can be found from $\langle I_d(T_1)\rangle$ and $\langle I_d(T_3)\rangle$ according to eqns. 12 and 13. T_{NL} and T_{TON} are found to be $0.06T_{LO}$ and $0.48T_{LO}$, respectively. Fourier decomposition of V_{out} can be used to find C_L, it is 3.78 dB which is a 1.1 dB improvement from the simulation run for the same mixer structure with no bias current and $I_{LO} = 7$ mA. The nonlinearity of C_B can be gauged from Fig. 59(c) to be slightly greater than for the no I_{bias} case: the variation in C_B has grown from $1.7C_{jo}$ to $1.8C_{jo}$.

Fig. 60 can be examined to see the effect of the higher bias and drive currents on the energy transfer profile and on the distribution of RF current in the circuit components. The RF energy stored in C_B is much greater than before: $6.25 * 10^{-15}$ joules vs. $4.2 * 10^{-15}$ joules previously. The RF energy stored in L_1 is now 6.25 fJ vs. 2.8 fJ previously. I_{d_r} is now greater than 2/3 of I_{RF} when the diode is 'ON'.

Optimization of Phasing Circuit

Following the optimization strategy detailed in Section 5.4.1, the single-ended mixer's conversion loss drops from 3.78 dB when the circuit described in run *hdiod82* is run to 3.1 dB when the final circuit *idiod2022* is simulated. The major changes along this iterative path will be described to illustrate the circuit's sensitivity to changes in $|Z_S|$, $\angle Z_S$, R_L, f_1 and f_2. Tables 16 and 17 list parameters for seven important simulation runs. All circuit elements are given for operation at $f_{RF} = 909$ MHz and $f_{LO} = 900$ MHz. Table 16 covers the first three runs, from the addition of C_B to the diode model to the circuit obtained at the end of the first iterative cycle of the phasing circuit prior to the addition of I_{bias}. All three circuits have been discussed before but are included here for comparison. Table 17 covers the last four runs, from the addition of I_{bias} to the final optimized run. Comments at the end of the table identify the circuit changes that have occured between runs.

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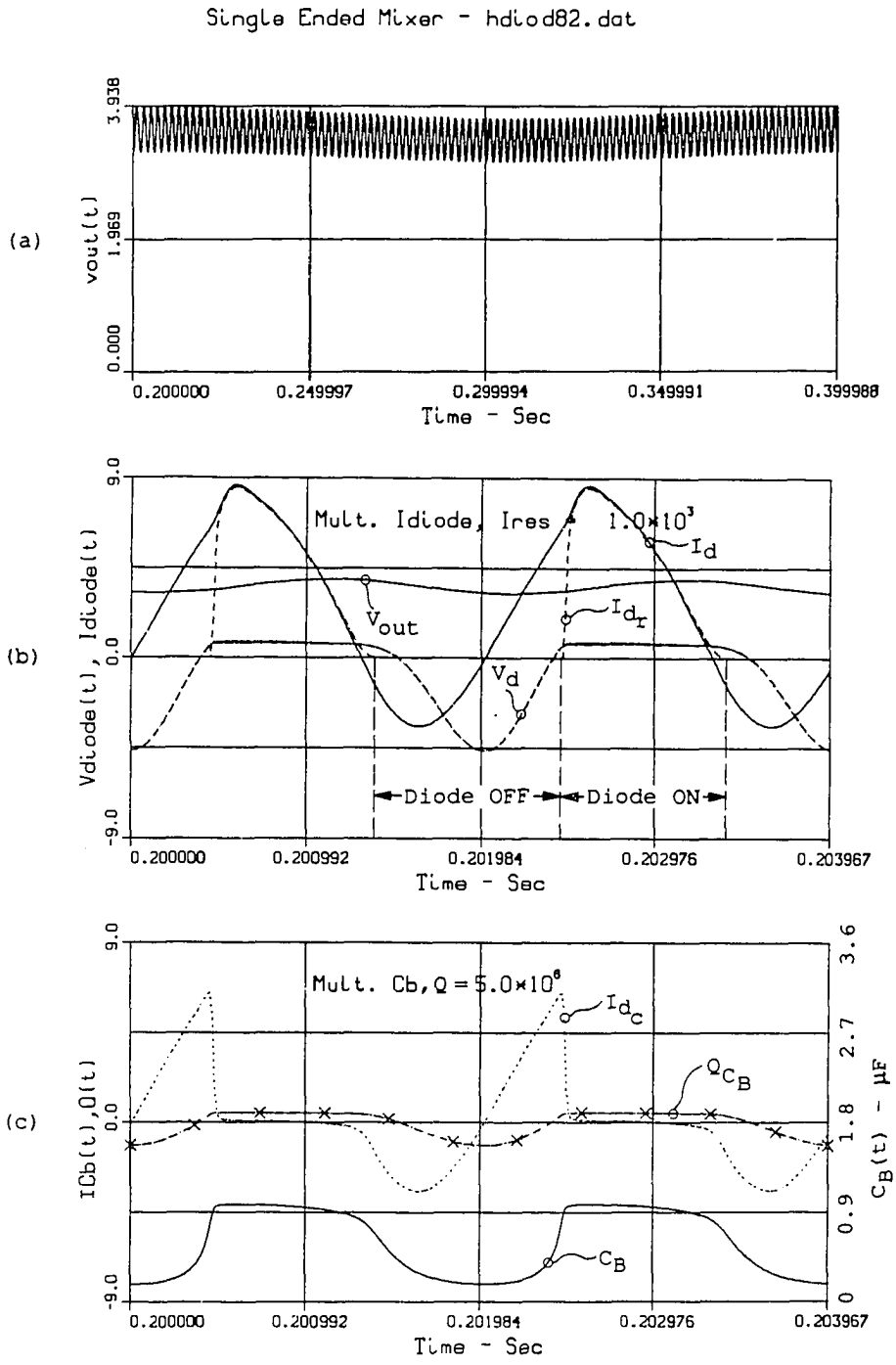


Figure 59: Large-signal waveforms in single-ended mixer - bias optimized for initial phasing circuit.

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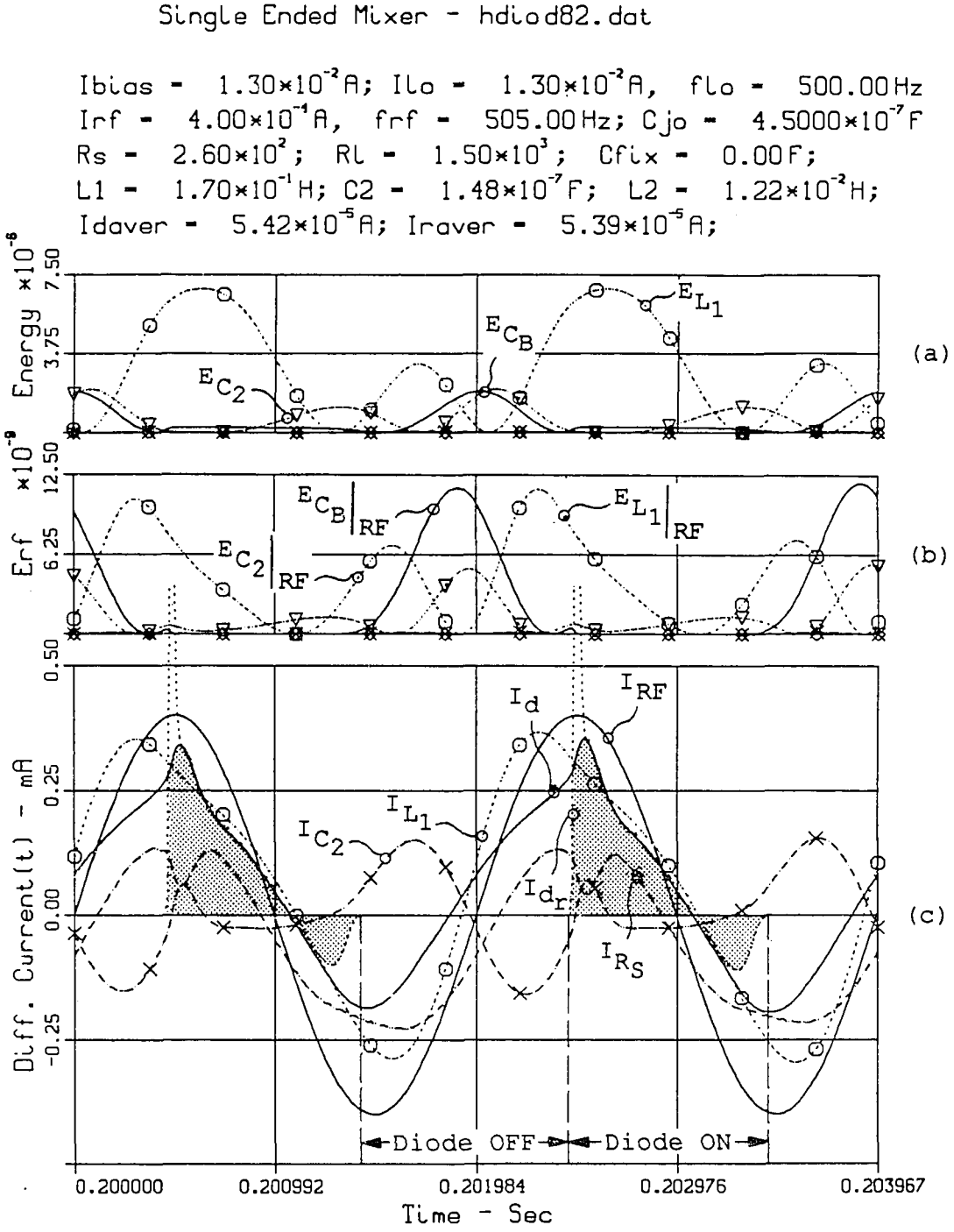


Figure 60: Energy waveforms and small-signal currents in single-ended mixer - bias optimized for initial phasing circuit.

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Table 16: Mixer Performance after Addition of Phasing Circuit
($C_{j0} = 0.25$ pF; $I_{RF} = 0.4$ mA.)

	idiod1010	*idiod2362*	*hdiod49*
Circuit and Drive Condidions:			
I_{bias}, I_{LO}	0, 4mA	0, 4mA	0, 7mA
R_S, R_L	1K, 1K	1K, 1K	260Ω, 1.5K
C_{LD}	2.8 pF	2.8 pF	2.8 pF
L_S, C_S	1.8μH, 0	0.19μH, 0	0, 0
L_1	0	0	0.094μH
C_2, L_2	0, 0	0, 0	0.082pF, 6.77 nH
$Z_S(f_{RF})$	995Ω ∠6°	745Ω ∠42°	760Ω ∠70°
f_1, f_2	N/A†, N/A	N/A, N/A	1.75 GHz, 6.75GHz
Diode Condidions:			
$\frac{T_{NL}}{T_{LO}}$, $\frac{T_{ON}}{T_{LO}}$	0.09, 0.36	0.08, 0.38	0.09, 0.34
$V_{d_{min}}$, $I_{d_{max}}$	-3.4V, 3.7mA	-4.3V, 4.1mA	-4.8V, 4.3mA
$\langle G_B \rangle$	25.9 mmho	33.1 mmho	25.4 mmho
$\langle C_B \rangle$	0.289pF	0.294pF	0.272pF
$\langle I_d(T_1) \rangle$	0.779mA	0.975mA	0.711 mA
$\langle I_d(T_2) \rangle$	0.672mA	0.851mA	0.660 mA
$\langle I_d(T_3) \rangle$	0.563mA	0.945mA	0.615 mA
$\langle I_d(T_4) \rangle$	0.680mA	0.869mA	0.668 mA
Mixer Performance:			
C_L	5.54 dB	4.6 dB	5.00 dB
$Z_{in}(f_{RF})$	731Ω $\angle -60°$	761Ω $\angle -57°$	861Ω $\angle -72°$
$Z_{out}(f_{IF})$	N.C. ‡	N.C.	1.62K ∠1°
Comments:			
	No matching circuit to C_{j0}	Use of parallel inductor,L_S, to match C_B; C_B treated as C_F	1st iteration of phasing circuit ($I_{bias} = 0$)

† Not Applicable.
‡ Not Calculated.

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Table 17: Mixer Sensitivity to Changes in Circuit and Drive Conditions
($C_{j0} = 0.25$ pF; $I_{RF} = 0.4$ mA.)

	hdiod82	*idiod17*	*idiod20*	*idiod2022*
Circuit and Drive Condidions:				
I_{bias}, I_{LO}	13mA, 13mA	13mA, 13mA	13mA, 13mA	13mA, 13mA
R_S, R_L	260Ω, 1.5K	197Ω, 1.5K	197Ω, 1.5K	197Ω, 1.5K
C_{LD}	2.8 pF	2.8 pF	2.8 pF	2.8 pF
L_S, C_S	0, 0	0, 0	0, 0	3.45μH, 88.9pF
L_1	0.094μH	0.117μH	0.116μH	0.116μH
C_2	0.082pF	0.027pF	0.029pF	0.029pF
L_2	6.77nH	12.9nH	0	0
$Z_S(f_{RF})$	760Ω ∠70°	760Ω ∠75°	740Ω ∠82°	770Ω ∠75°
f_1	1.75GHz	2.7GHz	2.7GHz	2.7GHz
f_2	6.75GHz	8.55GHz	∞	∞
Diode Condidions:				
$\frac{T_{NL}}{T_{LO}}$, $\frac{T_{TON}}{T_{LO}}$	0.06, 0.48	0.07, 0.49	0.07, 0.49	0.07, 0.49
$V_{d_{min}}$, $I_{d_{max}}$	-4.6V, 8.6mA	-4.4V, 6.4mA	-4.4V, 6.3mA	-4.4V, 6.3mA
$\langle G_B \rangle$	88.9 mmho	N.C. †	N.C.	71.1 mmho
$\langle C_B \rangle$	0.33pF	N.C.	N.C.	0.33pF
$\langle I_d(T_1) \rangle$	2.40mA	1.93mA	1.93mA	1.93mA
$\langle I_d(T_2) \rangle$	2.35mA	1.88mA	1.88mA	1.88mA
$\langle I_d(T_3) \rangle$	2.29mA	1.83mA	1.83mA	1.83mA
$\langle I_d(T_4) \rangle$	2.35mA	1.89mA	1.88mA	1.88mA
Mixer Performance:				
C_L	3.78 dB	3.43 dB	3.43 dB	3.07 dB
$Z_{in}(f_{RF})$	648Ω ∠ − 69°	675Ω ∠ − 70°	674Ω ∠ − 70°	657Ω ∠ − 70°
$Z_{out}(f_{IF})$	1.25K ∠ − 2°	1.35K ∠ − 2°	1.35K ∠ − 2°	1.35K ∠ − 2°
Comments:				
	First application of bias	Optimize R_L, Z_S, f_1	$f_2 \rightarrow \infty$	Adding L_S and C_S

† Not Calculated.

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In the tables $Z_S(f_{RF})$ and $Z_{in}^*(f_{RF})$ are given to highlight the fact that optimum C_L is not achieved when the source is matched to the complex conjugate of the input impedance. The minimum diode voltage and maximum diode current, $V_{d_{min}}$ and $I_{d_{max}}$, are listed along with the average diode barrier conductance and capacitance, $\langle R_B \rangle$ and $\langle C_B \rangle$, to chart the effect of the circuit and drive level on the diode condition. The latter are obtained from the DC Fourier coefficient of $g(t)$ and $C_B(t)$ [3]. The average value of the diode current at T_1, T_2, T_3, and T_4 are listed for use in calculating C_L with eqns. 12 and 13. The calculated value of $Z_{out}(f_{IF})$ is shown for all the runs for which it has been calculated. Although R_L remains constant in the last four tabulated runs, simulations were performed with other values of R_L to insure that the best performance was achieved with $R_L = 2.5$ K. As can be deduced from observing the values of these four parameters as $C_{L_{min}}$ is approached, the variation is not monotonic. They do not provide a good indication of improved circuit performance. Also listed in the tables are T_{NL} and T_{TON}. T_{TON} remains a good indicator for reducing C_L, $C_{L_{min}}$ being achieved when $T_{TON} \rightarrow 0.5\ T_{LO}$.

Description of Final Circuit

The diode waveforms for the final mixer circuit run *idiod2022* with $C_{j0} = 0.25$ pF are shown in Figures 61 and 62. The energy pattern in Fig. 62 shows transfer of RF energy from C_B, when the diode is 'OFF', to L_1, a moment before the diode is ready to turn 'ON'. This causes I_{L_1} to reach its maximum value just prior to the diode's turning 'ON' and allows the maximum amount of RF current to flow through R_B when the diode is 'ON'. The effect of fine circuit tuning resulting in the C_L of 3.1 dB are difficult to see in the graphical output. When optimizing the circuit performance at this level, the designer must rely on the quantitative measurement of C_L rather than on other circuit parameters. In fact, the single-ended mixer may be able to be further optimized. Optimization was ended in this example when the best performance possible was believed to be reached with the phasing circuit. This

[3]They are calculated as a routine part of the simulation as the Fourier coefficients of these waveforms are needed to compare the mixer performance predicted with our design tool with those using the frequency domain technique as outlined in Section 4.3.

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occured when the amount of C_L improvement for various circuit changes began to fall beneath 0.1 dB.

For all the simulation runs performed, the RF source was set to 0.4 mA, a value high enough to see its effect on the diode waveforms graphically but low enough that its value did not effect the diode's bias conditions. To check the simulation results, mixer performance was reanalyzed with I_{RF} set to $30\mu A$ - no changes in performance were found.

The final optimized circuit is shown in Fig. 63. The element values correspond to $f_{RF} = 909$ MHz and $f_{LO} = 900$ MHz. A microstrip filter may be necessary to realize C_2 (0.03pF) as it has a very low capacitance. The function of the load capacitance is to short out the load impedance at frequencies higher than f_{RF} and to provide an open circuit at f_{IF}. Hence if $f_{IF} \ll 9$ MHz as would be the case with the mobile radio application of the direct conversion receiver, then C_{LD} can be replaced by standard valued capacitance such as a 50 pF capacitor.

Finally we examine the embedding circuit presented to the diode by the phasing circuit and other circuit elements:

$$Z_{emb}(f) = Z_S(f) + Z_L(f)$$

where $Z_S(f)$ and $Z_L(f)$ represent the source and load impedances, respectively, depicted in Fig. 54. The embedding impedances at the selected sideband frequencies are given in Table 18. For frequencies from $2f_{LO}$ to $5f_{LO}$ the mixer circuit provides a very high embedding impedance to the diode, thus ressembling a 'Z' mixer more than a 'Y' mixer although the diode 'ON' time approaches 0.5 T_{LO} unlike the optimum 'Z' mixer.

5.4.3 Performance Achieved with a Diode Having $C_{j0} = 1.0$pF

A circuit has been designed for the single-ended mixer circuit of Fig. 14 with a diode having a barrier capacitance with $C_{j0} = 1.0$ pF in accordance with the design strategy outlined in Section 5.4.1. The optimal circuit is shown in Fig. 64. The improvement

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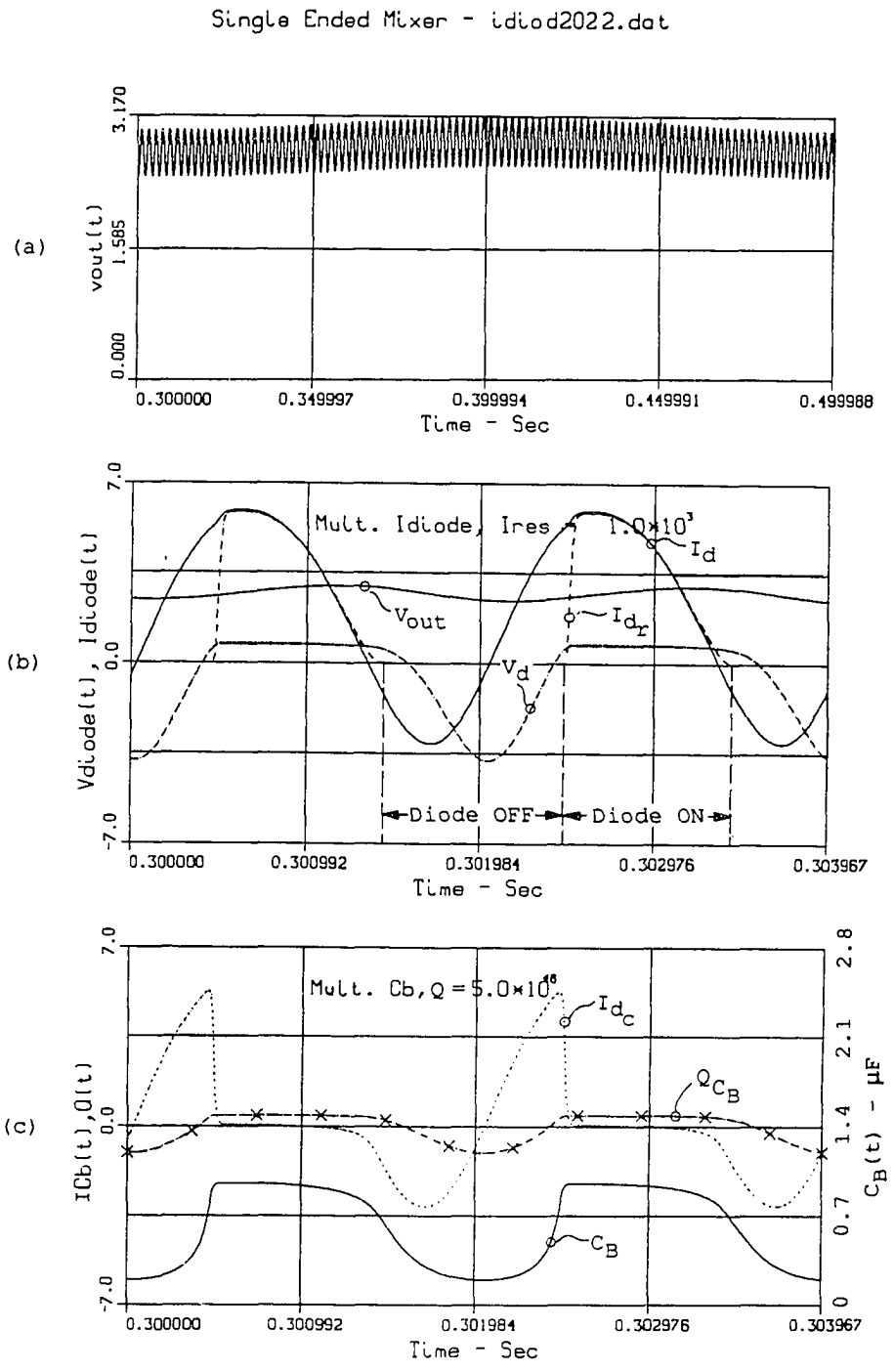


Figure 61: Large-signal waveforms in final single-ended circuit ($C_{j0} = 0.25$ pF).

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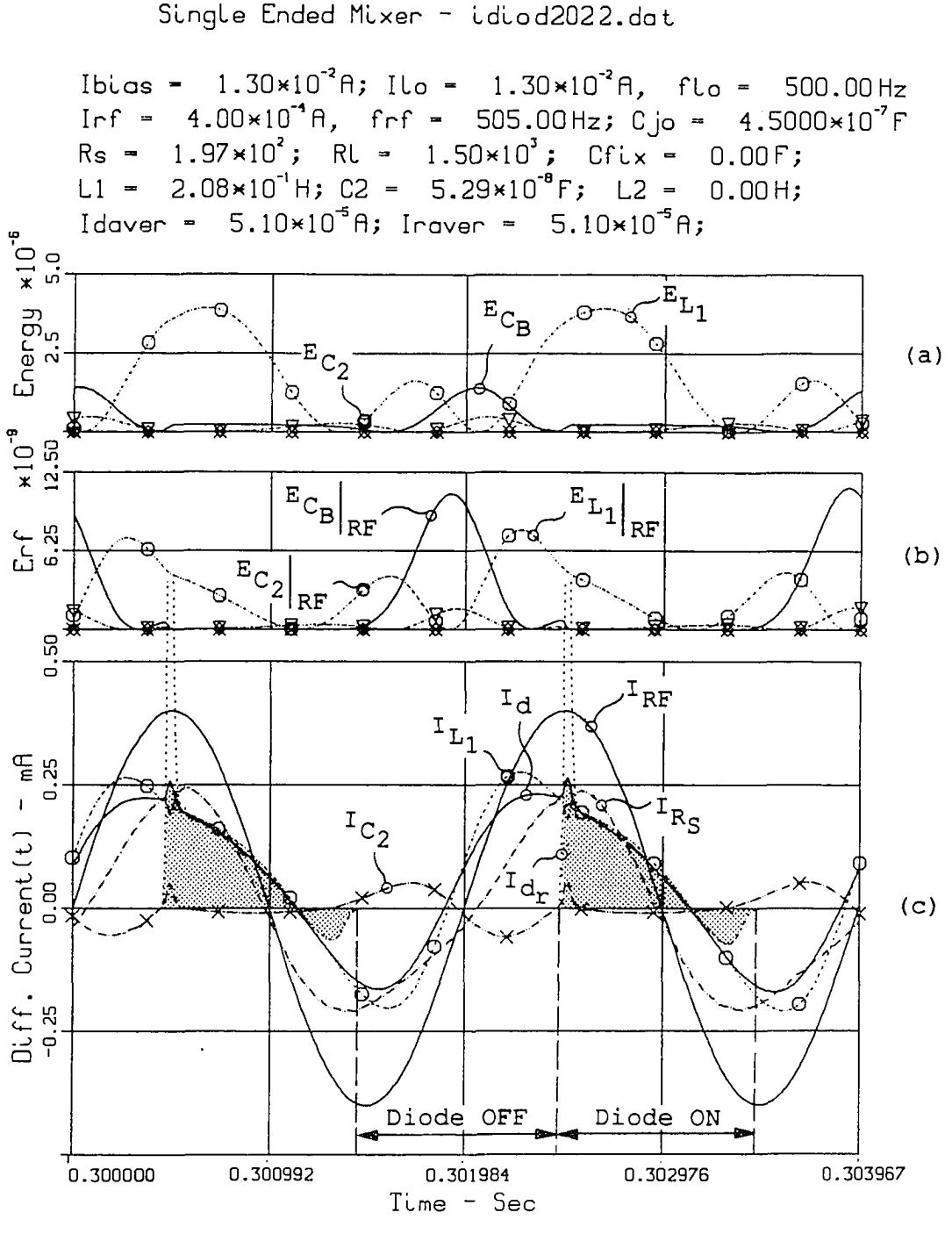


Figure 62: Energy waveforms and small-signal currents in final single-ended circuit ($C_{j0} = 0.25$ pF).

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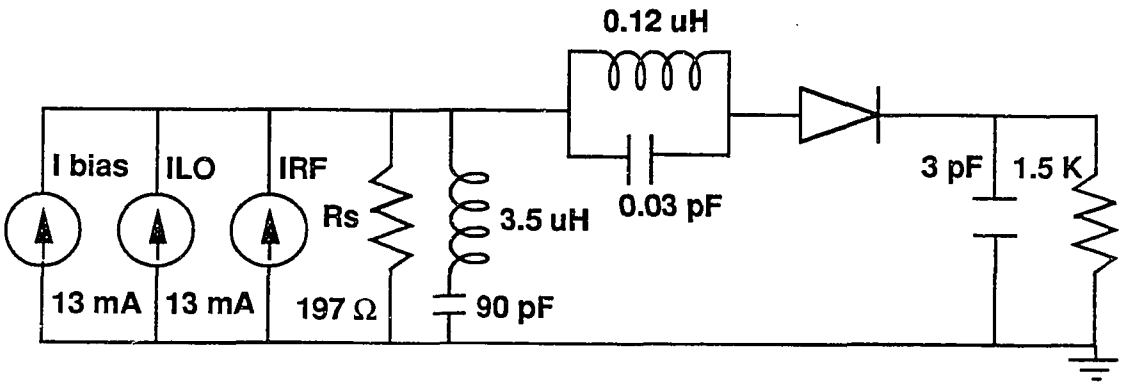


Figure 63: Optimized circuit for the single-ended mixer ($C_{j0} = 0.25$ pF).

Table 18: Embedding Impedances of Final Single Ended Mixer Circuit ($C_{j0} = 0.25$ pF)

Frequency	$Z_{emb}(f)$
DC	1697 Ω
f_{IF}	1420Ω - j 334Ω
f_{RF}	199Ω + j 683Ω
$2f_{LO} + f_{IF}$	197Ω + j 2310Ω
$3f_{LO} + f_{IF}$	197Ω + j 122000Ω
$4f_{LO} + f_{IF}$	197Ω - j 3530Ω
$5f_{LO} + f_{IF}$	197Ω - j 1910Ω

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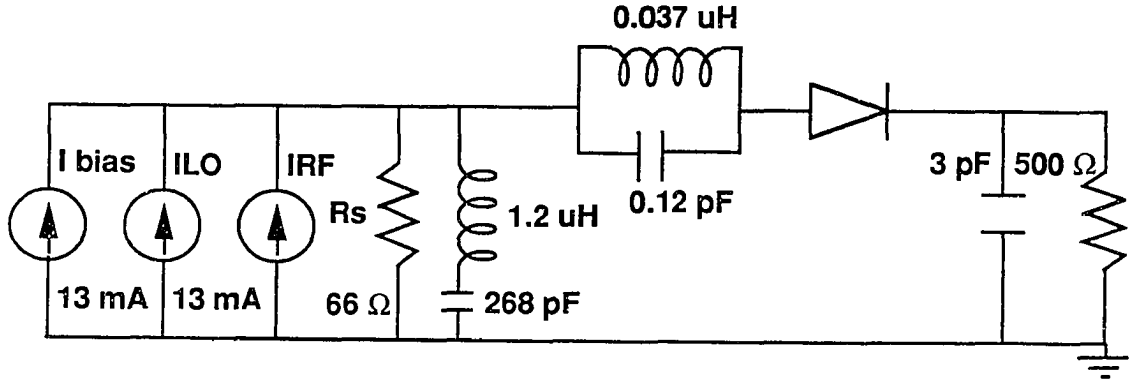


Figure 64: Optimum circuit for the single-ended mixer ($C_{j0} = 1.0$ pF).

due to the addition of the phasing circuit and the appropriate changes in drive and circuit conditions are detailed in Table 19. In it the performance of three mixer runs are compared: (1) *idiod1013* shows the degradation in performance when C_B is added to the diode model and no attempt is made to redesign the purely resistive mixer circuit; (2) *ldiod2392* gives the performance achievable by varying L_S until C_L is minimized; and (3) *cdiod6122* lists the performance obtained when the phasing circuit is utilized.

From Table 19 it can be seen that the source impedance is not chosen to provide a conjugate match to the input impedance - although $Z_S(f_{RF})$ is closer to $Z_{in}^*(f_{RF})$ than in the case of $C_{j0} = 0.25$ pF - and that one of the effects of the phasing network is to open up the window during which the diode conducts through R_B as $T_{TON} \sim 0.42\ T_{LO}$ in the final circuit. Z_{out} is found to be $756\Omega\ \angle 1°$ even though $C_{L_{min}}$ is reached when R_L is 500Ω.

The large signal diode and circuit waveforms are shown in Figure 65. When, in the course of circuit optimization, bias was applied to the diode, I_{RF} was increased from 0.4 mA to 1 mA so that its effect could be seen in the graphical output. C_B can be seen to vary from 2.28 pF to 0.46 pF. The small signal energy and current waveforms are shown in Fig. 66. The transfer of energy from C_B to L_1 and then to R_B can be clearly seen. The pattern is quite similar to that of the final circuit for $C_{j0} = 0.25$ pF

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Table 19: Improvement in Circuit Performance due to the Addition of the Phasing Network

($C_{j0} = 1.0$ pF)

	idiod1013	*idiod2392*	*cdiod6122*
Circuit and Drive Condidions:			
I_{bias}, I_{LO}	0, 4mA	0, 4mA	20mA, 30mA
R_S, R_L	1K, 1K	1K, 1K	66Ω, 500Ω
C_{LD}	2.8pF	2.8pF	2.8pF
L_S, C_S	1.8μH, 0	0.49μH, 0	1.17μH, 0.268nF
L_1	0	0	0.037μH
C_2, L_2	0, 0	0, 0	0.119pF, 0
$Z_S(f_{RF})$	995Ω ∠6°	269Ω ∠74°	259Ω ∠75°
f_1, f_2	N/A†, N/A	N/A, N/A	2.25GHz, ∞
Diode Condidions:			
$\frac{T_{NL}}{T_{LO}}$, $\frac{T_{TON}}{T_{LO}}$	0.21, 0.21	0.10, 0.30	0.07, 0.42
$V_{d_{min}}$, $I_{d_{max}}$	-0.85V, 4.2mA	-3.3V, 9.4mA	-3.5V, 16.5mA
$\langle G_B \rangle$	0.534 mmho	25.6 mmho	125.7 mmho
$\langle C_B \rangle$	1.12pF	1.11pF	1.29pF
$\langle I_d(T_1) \rangle$	29.4μA	0.743mA	3.44mA
$\langle I_d(T_2) \rangle$	7.43μA	0.626mA	3.33mA
$\langle I_d(T_3) \rangle$	-2.96μA	0.515mA	3.22mA
$\langle I_d(T_4) \rangle$	4.80μA	0.645mA	3.33mA
Mixer Performance:			
C_L	22.2 dB	5.4 dB	4.25 dB
$Z_{in}(f_{RF})$	234Ω ∠ − 84°	291Ω ∠ − 79°	243Ω ∠ − 72°
$Z_{out}(f_{IF})$	N.C. ‡	N.C.	756Ω ∠1°
Comments:			
	No matching circuit to C_{j0}	Use of parallel inductor, L_S, to match C_B; C_B treated as C_F	Last iteration of phasing circuit

† Not Applicable.
‡ Not Calculated.

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except that less of the RF current travels through R_B when the diode is 'ON'. There are several differences in the circuit conditions required to reach $C_{L_{min}}$: a higher bias and LO drive are necessary to turn the diode 'ON' for $0.5T_{LO}$. As in the case of C_{j0} = 0.25 pF, higher combinations of I_{LO} and I_{bias} minimized C_L: I_{LO} = 30 mA, I_{bias} = 20 mA was chosen as a reasonable point of operation as the improvement in C_L with increasing bias was decreasing. Conversion loss for this circuit was calculated to be 4.25 dB; this result was corroborated when I_{RF} was reduced to 75μA to model a small-signal level.

The circuit elements for the finalized circuit are given in Fig. 64; they correspond to operation with f_{RF} = 909 MHz and f_{LO} = 900 MHz. Again most of the elements will be easy to realize with lumped components with the exception of C_2 (0.12pF) which may require realization with a microstrip filter. This value of C_2 is larger than that called for with C_{j0} = 0.25 pF and hence should be easier to realize. The value of the load capacitance can be increased according to the ratio of $\frac{f_{RF}}{f_{IF}}$ as the purpose of C_{LD} is to short all frequencies greater than f_{IF}. If $\frac{f_{RF}}{f_{IF}} \sim 100$ as in this example then C_{LD} = 2.8 pF; if $\frac{f_{RF}}{f_{IF}} \geq 10{,}000$ as expected for most direct conversion applications, then C_{LD} can be increased to a more conventional value, eg. 50 pF. Similarly the value used for L_S and C_S depend on the actual ratio of f_{RF} to f_{IF} as their purpose is to provide a short at f_{IF} only. The value of the matching circuit elements, however, are determined by f_{RF} and f_{LO} and do not depend on f_{IF} as they act ot time the storage of RF energy when the LO turns the diode 'ON' and 'OFF'.

Table 20 gives the values of the embedding network created by the phasing circuit and other circuit elements. At frequencies of $2f_{LO}$ and higher, the circuit provides an open-circuit match to the diode similar to the 'Z' mixer. However where a 'Z' mixer is optimized by keeping the diode mostly in the 'ON' state as shown in Table 5, the optimized single-ended mixer possesses minimum C_L when $T_{TON} \rightarrow 0.5T_{LO}$. At very high LO harmonics, the embedding impedance becomes resistive.

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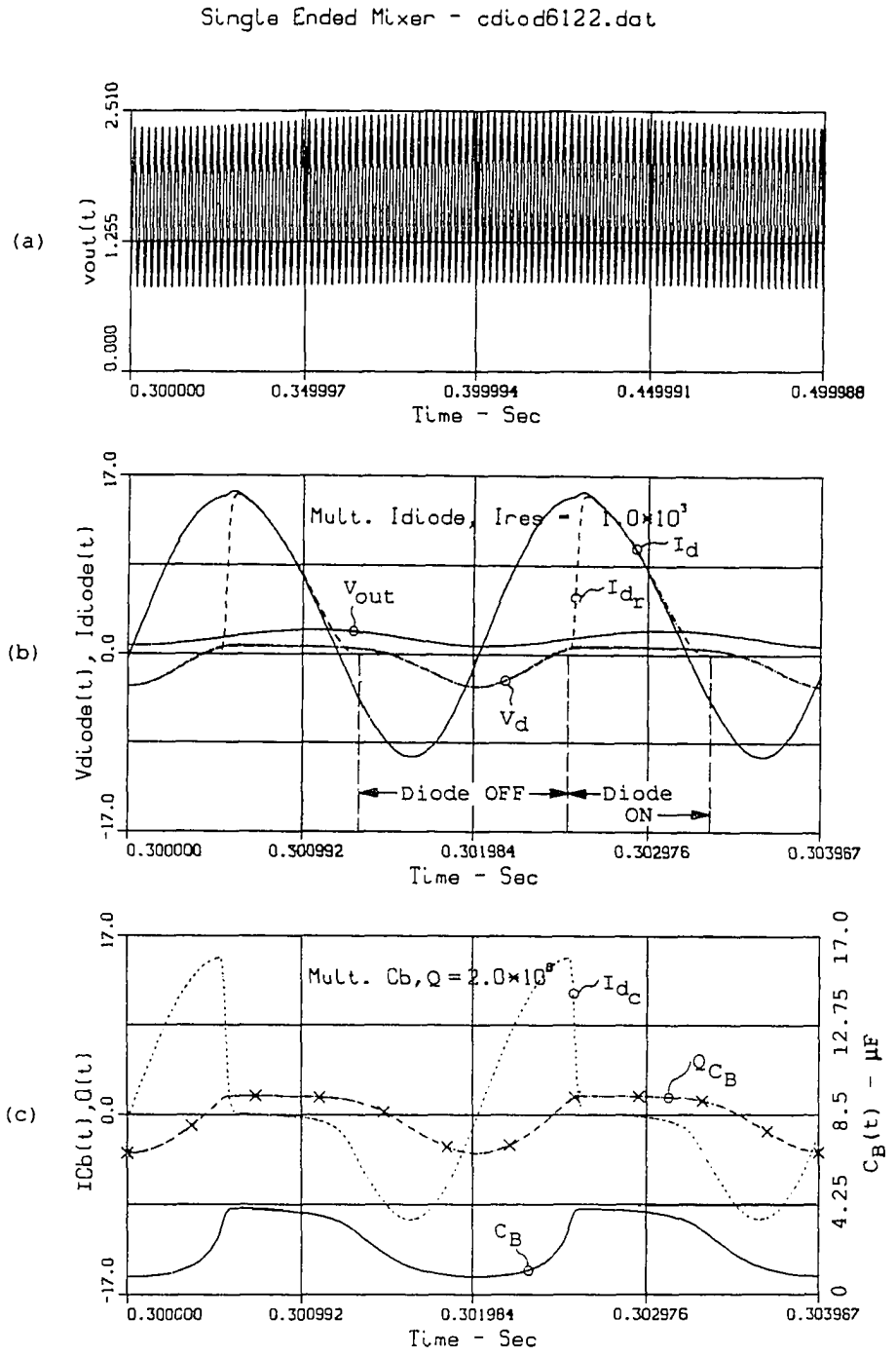


Figure 65: Large-signal waveforms in final single-ended circuit ($C_{j0} = 1.0$ pF).

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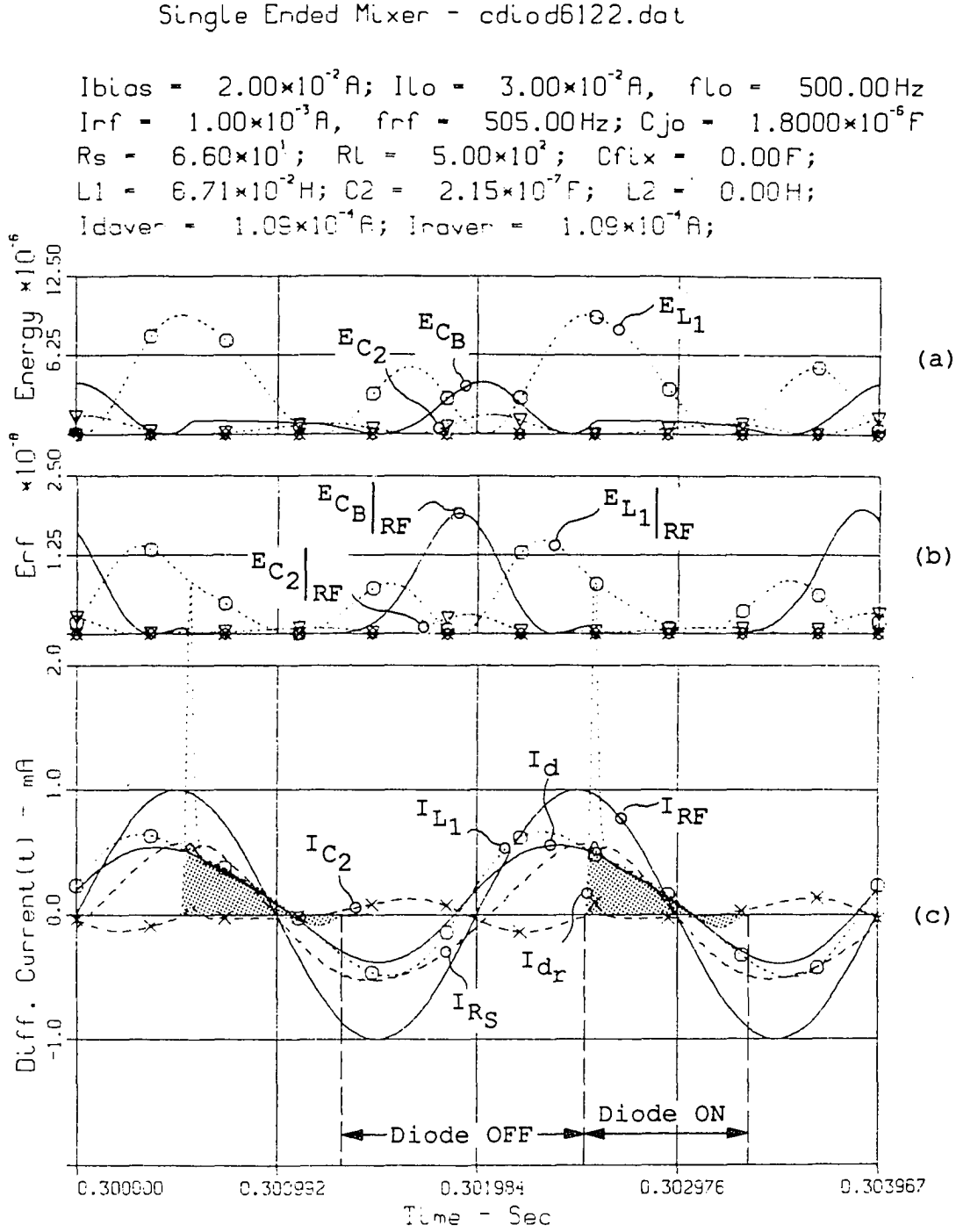


Figure 66: Energy waveforms and small-signal currents in final single-ended circuit ($C_{j0} = 1.0$ pF).

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Table 20: Embedding Impedances of Final Single Ended Mixer Circuit (C_{j0} = 1.0 pF)

Frequency	$Z_{emb}(f)$
DC	566 Ω
f_{IF}	497Ω - j 38Ω
f_{RF}	73Ω + j 189Ω
$2f_{LO} + f_{IF}$	68Ω + j 965Ω
$3f_{LO} + f_{IF}$	67Ω - j 2220Ω
$4f_{LO} + f_{IF}$	66Ω - j 672Ω
$5f_{LC} + f_{IF}$	66Ω -j 423Ω

5.4.4 Performance Improvement due to Nonlinear C_B

In this section, the reasons for the improvement in mixer performance obtained with the phasing circuit will be explored. Here we wish to show that the improvement in C_L is due to the parametric pumping of C_B by the LO source and thus is achievable due to the nonlinearity of C_B with applied voltage as well as to the energy storage capability of C_B. To do this we will replace the current diode model shown in Fig. 67(a) with a diode which possesses a series resistance, r_{ser}, a nonlinear barrier resistance, R_B, and a linear barrier capacitance of fixed value C_F. The model for this theoretical diode is given in Fig. 67(b). The fixed capacitance, C_F, is taken to be in parallel with r_{ser} and R_B, rather than with R_B alone as is the case in a practical diode, to model the performance of a purely resistive diode in parallel with a fixed capacitor. C_F is then used in conjunction with the phasing circuit to minimize C_L.

The diode model is then used in the near-optimal mixer circuit designed for C_{j0} = 0.25 pF. The circuit corresponding to near-optimal run *idiod17* is used for maximum flexibility (L_2 is still in place and hence f_2 can be varied). The resulting C_L and T_{TON} obtained when the diode model of Fig. 67(a) is replaced with that in Fig. 67(b) in this circuit are listed in Table 21. C_F is varied from 0 to 0.36pF.

Although the average value of C_B in the final single-ended mixer circuit is 0.33pF

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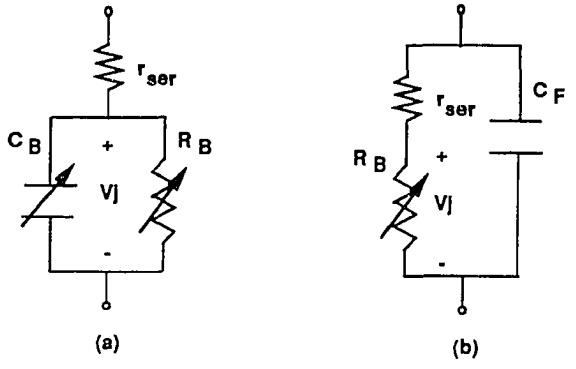


Figure 67: Diode model used to assess parametric improvement due to C_B: (a) practical model, C_B is a nonlinear function of V_j; (b) practical diode replaced by a resistive diode in parallel with C_F.

Table 21: Performance of Near-Optimum Mixer Circuit, *idiod*17, When C_B is Replaced by the Linear Capacitor C_F

	T_{TON}	C_L
Reference Circuit: $C_{j0} = 0.25$ pF	0.49	3.43 dB
C_F:		
0.0 pF	0.72	11.89 dB
0.005 pF	0.70	11.10 dB
0.027 pF	0.64	8.70 dB
0.055 pF	0.59	6.80 dB
0.111 pF	0.52	4.99 dB
0.167 pF	0.48	4.82 dB
0.222 pF	0.46	5.58 dB
0.250 pF	0.45	6.12 dB
0.278 pF	0.45	6.72 dB
0.306 pF	0.45	7.33 dB
0.333 pF	0.45	7.94 dB
0.361 pF	0.45	8.54 dB

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as shown in Table 17, the performance of the new mixer is 4.5 dB higher when C_F is set to $\langle C_B \rangle$. Minimum C_L is achieved in this circuit when C_F is $\sim$ 0.111 - 0.167 pF, then C_L is 4.8 - 5.0 dB and $T_{TON} \sim 0.5T_{LO}$. Two values of C_F are chosen for further circuit optimization, $C_F = 0.167$ pF, that for which $C_{L_{min}}$ is initially observed, and $C_F = 0.333$ pF, that which most resembles performance with $C_B = 0.25$ μF.

Optimization of the mixer circuit with $C_F = 0.167$ pF proceeds as detailed in Section 5.4.1. The conversion loss attained is 4.1 dB – 1 dB higher than that achieved with the non-linear barrier capacitance. The circuit elements for the final circuit are shown in Table 22. The differences between this circuit and that for $C_{j0} = 0.25$ pF are: (1) the lack of bias current necessary to reduce C_L; (2) the slightly higher R_L required, 2.5K vs. 1.5K; and (3) the values of L_1 and C_2. The most striking is the first: in this case reducing the bias from 13mA to 0mA caused C_L to drop by 0.07 dB whereas, when C_{j0} was 0.25 pF, the increase in I_{bias} from 0 to 13mA reduced C_L by over 1 dB.

Figures 68 and 69 show the large signal and small signal waveforms for the optimized single-ended mixer circuit with $C_F = 0.167$ pF. In Fig. 68(c) only the current through C_F is plotted. In Fig. 69 the energy transfer pattern occurs but its effectiveness is much reduced: I_{d_r} is less than half I_{RF} and the RF component of I_{R_S} is much greater than the RF component of I_{d_r}. The conversion loss obtained is 4.09 dB with $I_{RF} = 0.4$ mA; this result has benn checked with that obtained when $I_{RF} = 30\mu$A and found to agree.

A second optimization has been performed for C_F set equal to $\langle C_B \rangle$ in the final mixer run *idiod2022*. C_F is therefore set equal to 0.33pF and the optimization procedure started from the near-optimal circuit *idiod17*. The best conversion loss reached with the linear capacitor is 4.25 dB – 1.2 dB higher than that achieved with the non-linear barrier capacitance. The circuit elements for this final circuit are also shown in Table 22. The major differences between this circuit and that for $C_{j0} = 0.25$ pF lie in the absence of bias, in the use of a slightly higher load impedance ($R_L =$ 2.0 K vs. 1.5 K), and in the design of a phasing circuit optimized to provide a lower source impedance (Z_S is 507Ω $\angle$75° instead of 770Ω $\angle$75°). Examination of Table 22 shows that the diode 'ON' time is severely reduced for both cases involving the fixed

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Table 22: Performance Comparison between Finalized Circuits for a Mixer Diode with $C_{j0} = 0.25$ pF and two Purely Resistive Diodes with $C_F = 0.167$ pF and $C_F = 0.33$ pF

($I_{RF} = 0.4$ mA)

	idiod2022 $C_{j0} = 0.25$ pF	*idiod1492* $C_F = 0.167$ pF	*idiod1672* $C_F = 0.333$ pF
Circuit and Drive Condidions:			
I_{bias}, I_{LO}	13mA, 13mA	0, 13mA	0, 13mA
R_S, R_L	197Ω, 1.5K	197Ω, 2.5K	129Ω, 2K
C_{LD}	2.8pF	2.8pF	2.8pF
L_S, C_S	3.45μH, 88.9pF	3.45μH, 88.9pF	2.29μH, 136.7pF
L_1	0.116μH	0.117μH	0.0767μH
C_2, L_2	0.029pF, 0	0.027pF, 0	0.041pF, 0
$Z_S(f_{RF})$	770Ω ∠75°	770Ω ∠75°	507Ω ∠75°
f_1, f_2	2.7GHz, ∞	2.7 GHz, ∞	2.7GHz, ∞
Diode Condidions:			
$\frac{T_{NL}}{T_{LO}}$, $\frac{T_{TON}}{T_{LO}}$	0.07, 0.49	0.05, 0.31	0.055, 0.27
$V_{d_{min}}$, $I_{d_{max}}$	-4.4V, 6.3mA	-7.95V, 6.3mA	-5.3V, 7.8mA
$\langle G_B \rangle$	71.1 mmho	34.9 mmho	30.4 mmho
$\langle C_B \rangle$	0.33pF	0	0
$\langle I_d(T_1) \rangle$	1.93mA	1.0mA	0.878mA
$\langle I_d(T_2) \rangle$	1.88mA	0.972mA	0.849mA
$\langle I_d(T_3) \rangle$	1.83mA	0.928mA	0.813mA
$\langle I_d(T_4) \rangle$	1.88mA	0.959mA	0.843mA
Mixer Performance:			
C_L	3.07 dB	4.09 dB	4.25 dB
$Z_{in}(f_{RF})$	657Ω ∠ − 70°	826Ω ∠ − 75°	490Ω ∠ − 78°
$Z_{out}(f_{IF})$	1.35K ∠ − 20°	2.45K ∠ − 2°	2.3K ∠ − 8°

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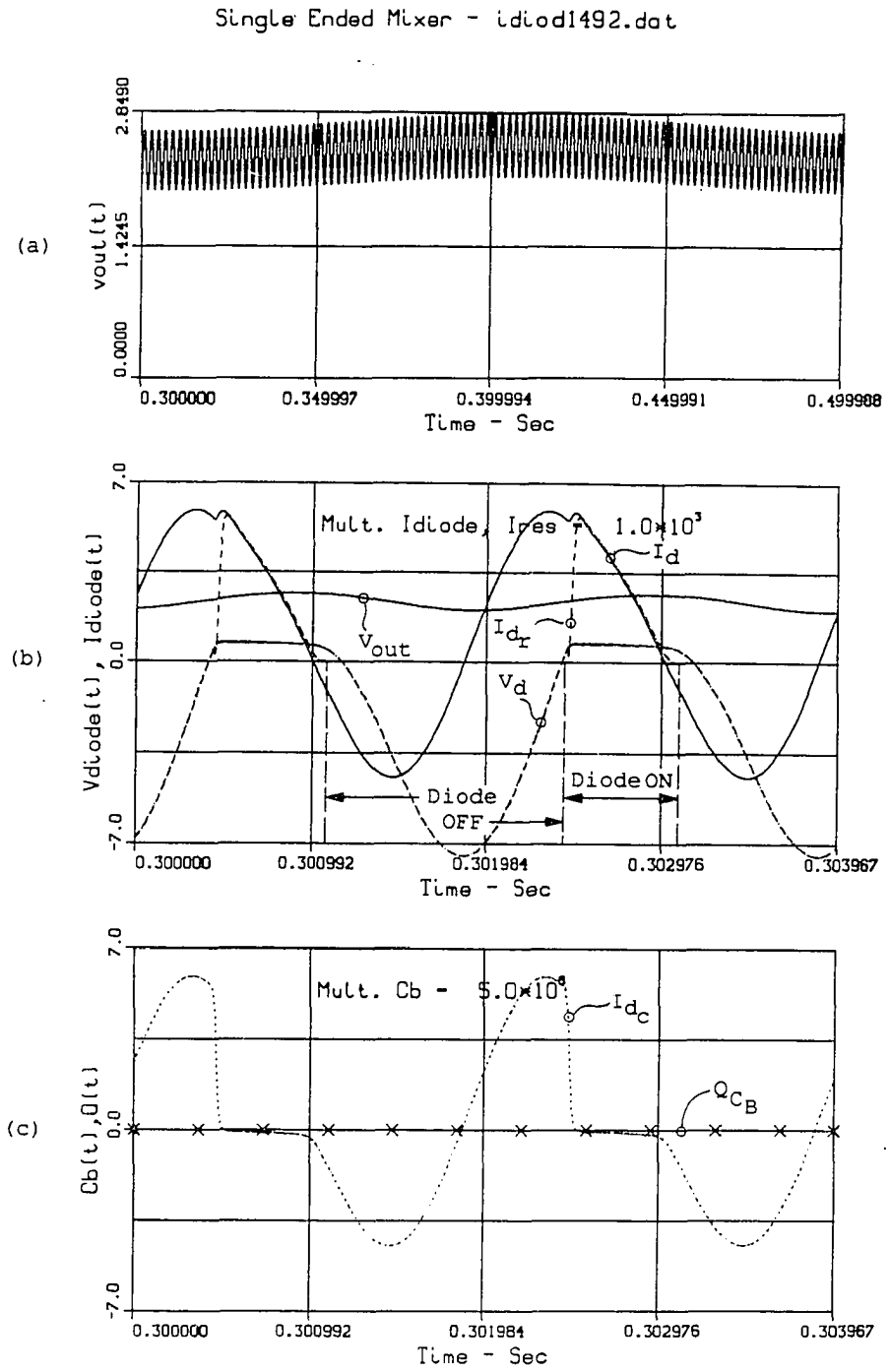


Figure 68: Large-signal waveforms in single-ended test circuit ($C_F = 0.167$ pF).

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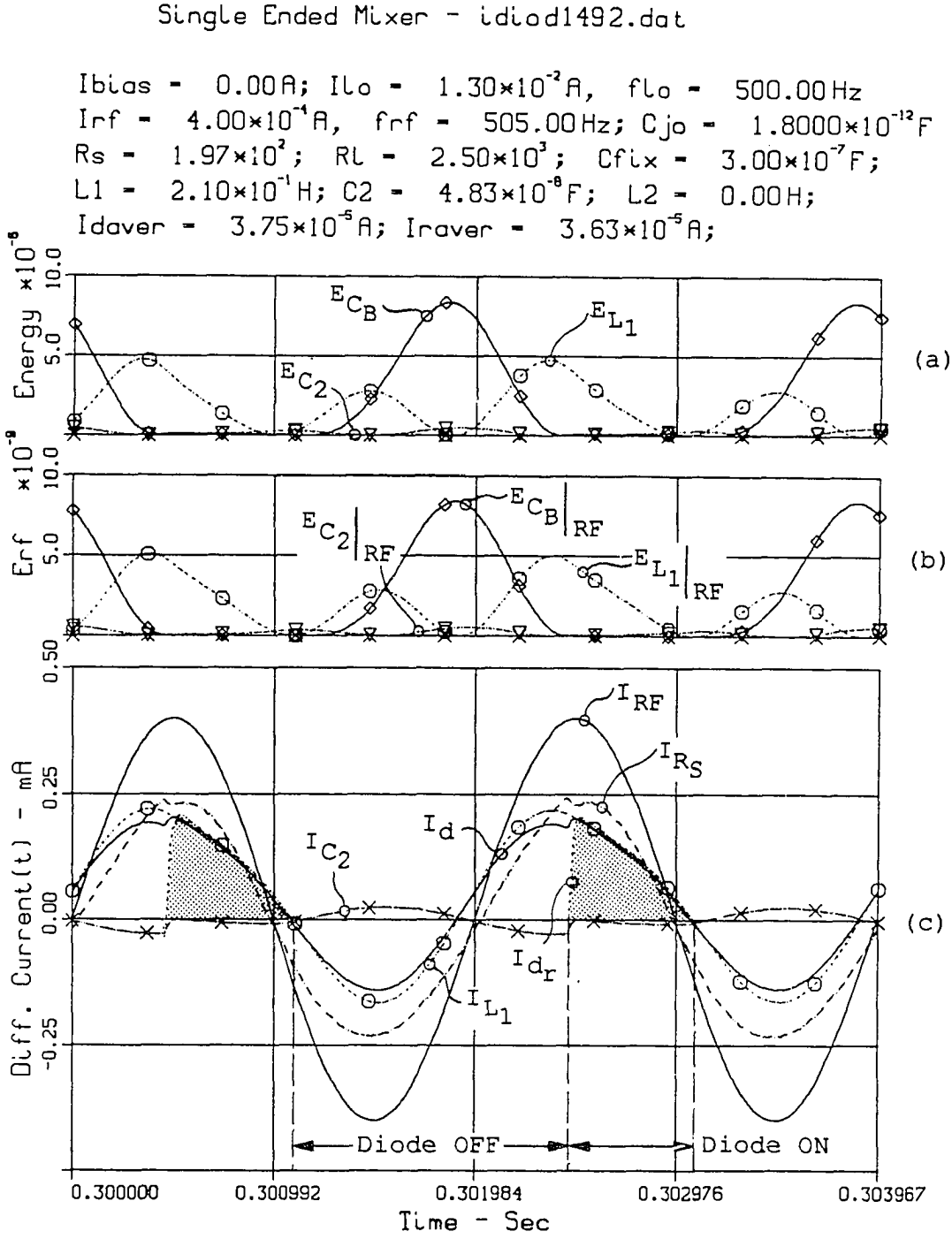


Figure 69: Energy waveforms and small-signal currents in single-ended test circuit ($C_F = 0.167$ pF).

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capacitor. Although the application of bias did increase T_{TON}, C_L was not improved.

Figures 70 and 71 give the large signal and small signal performance. Again Fig. 71 shows the energy transfer pattern and highlights the small T_{TON} diode time. The conversion loss of this mixer is 4.25 dB; this result has been corroborated by setting $I_{RF} = 30\mu$A to insure that the applied RF source is truly small signal. The embedding impedances for both of these circuits are similar to that obtained for C_{j0} = 0.25 pF: harmonics higher than $2f_{LO}$ are open-circuited. Z_{emb} reaches a maximum value at $3f_{LO}$ and slowly tapers off until at high frequencies the embedding impedance equals R_S.

5.4.5 Comparison with Frequency Domain Technique

The frequency domain techniques described in Chapter 3 and illustrated in Chapter 4 apply only to analysis of single-ended mixers. Therefore the results obtained when these techniques are applied to the optimized single-ended circuits with non-zero C_B will be discussed in this subsection prior to the balanced mixer design section. Both the Held and Kerr method, and, Maas' program DIODEMX have been used to estimate the conversion loss of the optimum single-ended mixers derived for C_{j0} = 0.25 pF and C_{j0} = 1.0 pF according to the method detailed in Section 4.4.

The Held and Kerr method has been used to estimate the conversion loss of the C_{j0} = 0.25 pF mixer. *Convhk.for* was run with a 9 X 9 and a 11 X 11 order admittance matrix and the conversion loss estimates were 3.8 dB and 4.3 dB, respectively. DIODEMX predicted a conversion loss of 1.6 dB and a noise temperature of 135 K for this mixer. To do so this program solves a 9 X 9 admittance matrix similar to that of Held and Kerr. These estimates differ significantly between themselves and with the estimate arrived at using our design tool - C_L being 3.1 dB for the optimized single-ended mixer with C_{j0} = 0.25 pF. The fact that the frequency domain estimates lie on either side of the SPICE estimates may indicate the importance of increasing the number of LO harmonics that are used to model the diode's large-signal characteristics and the necessity to include the effect of higher order sideband frequencies in calculating the mixer's performance. (An N X N matrix requires the first (N -

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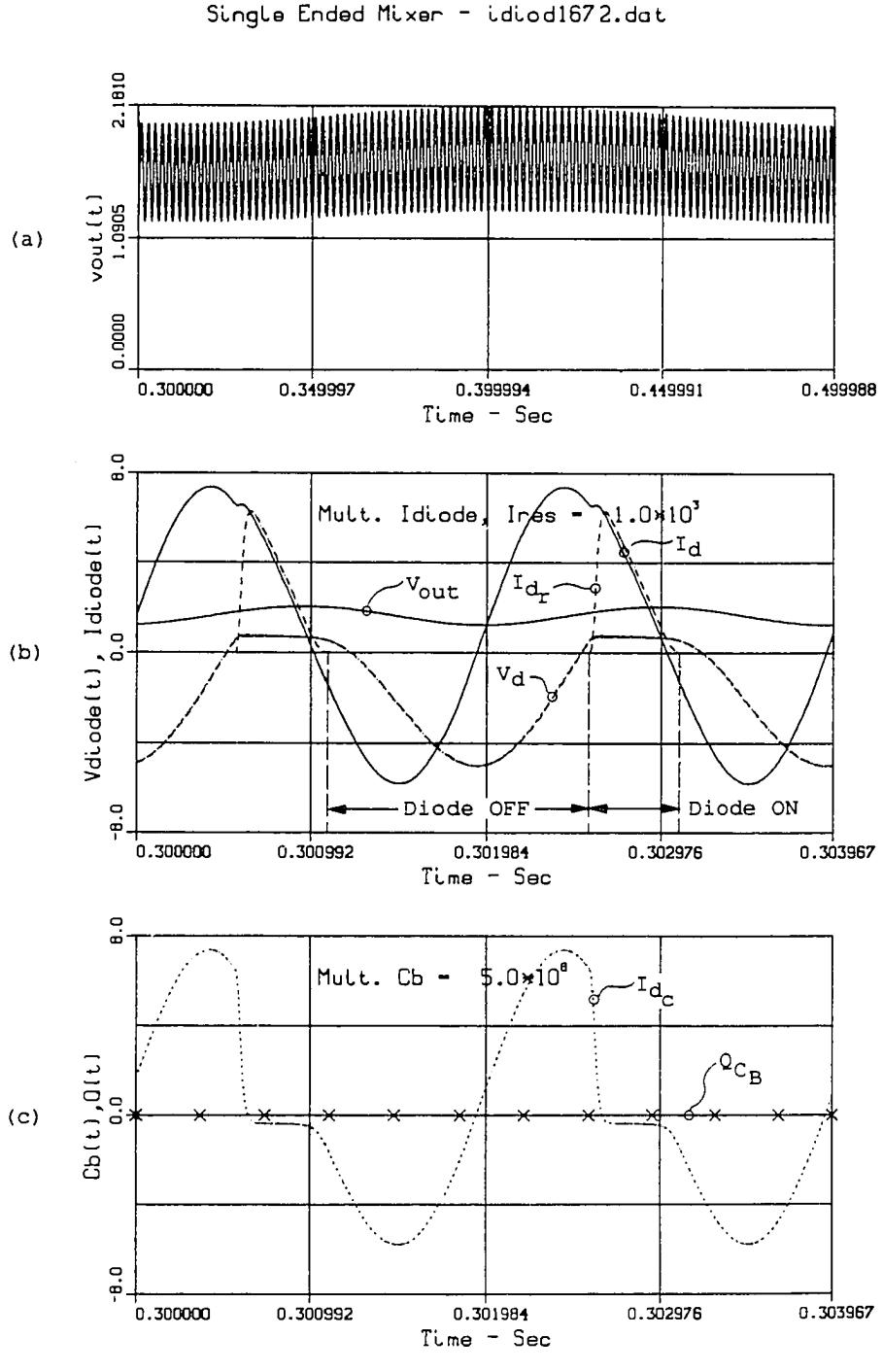


Figure 70: Large-signal waveforms in single-ended test circuit ($C_F = 0.33$ pF).

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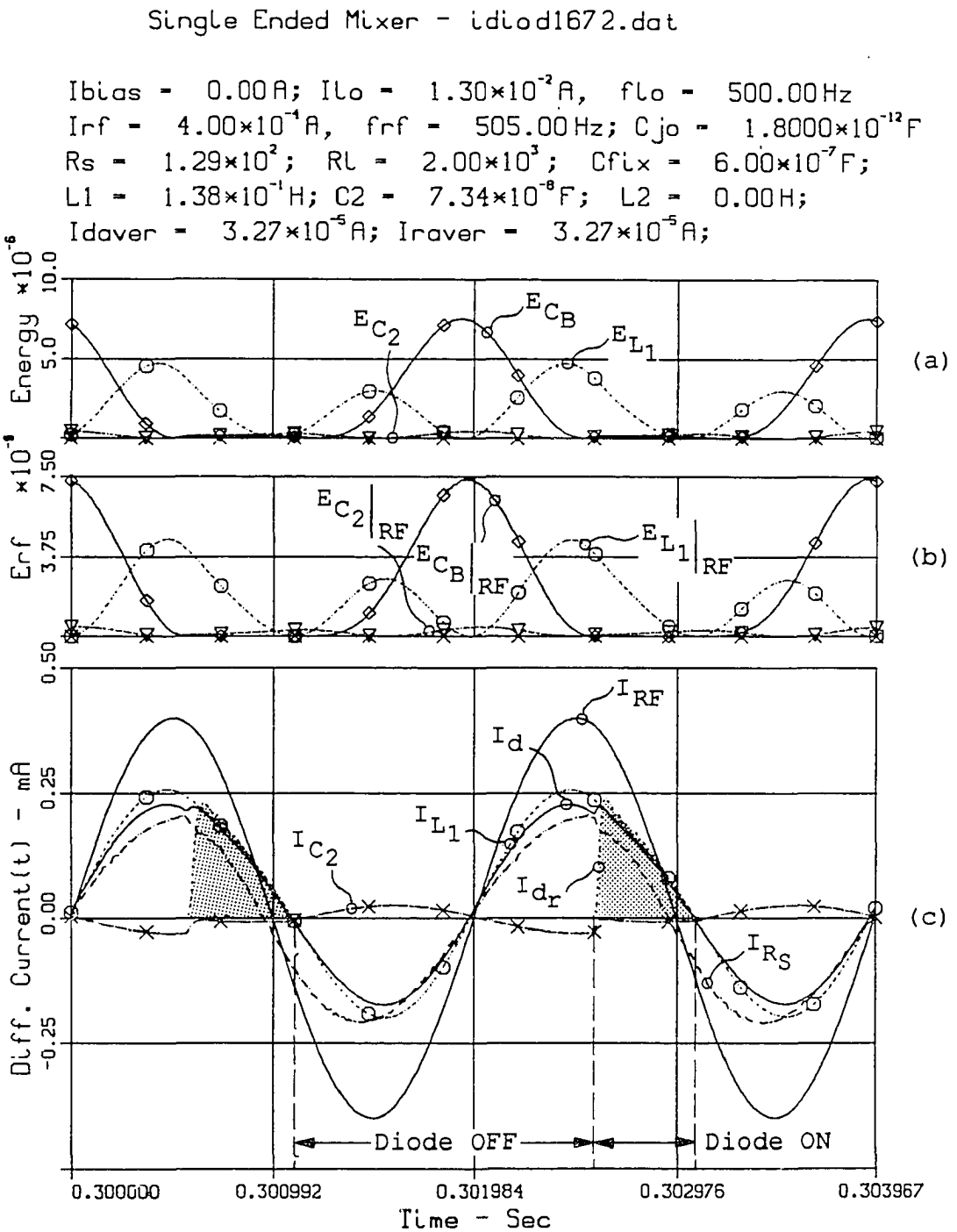


Figure 71: Energy waveforms and small-signal currents in single-ended test circuit ($C_F = 0.33$ pF).

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1)/2 Fourier coefficients of the diode's conductance and capacitance waveforms and the embedding impedance from the $(-\frac{N-1}{2})$th sideband to the $(\frac{N-1}{2})$th sideband. For the matrices employed here, this translates to Fourier coefficients up until the fourth or fifth LO harmonic and embedding impedances at the sideband frequencies about the 4th or 5th LO harmonic.)

When DIODEMX is used to estimate the performance of the single-ended mixer with C_{j0} = 1.0 pF, the mixer is predicted to have a 2.6 dB conversion loss, a noise temperature of 265 K, and to be unconditionally stable. Again, the conversion loss estimate is lower than the SPICE generated result of 4.25 dB obtained with our design tool.

The noise temperature results of both mixers can be compared with those obtained with DIODEMX for the single-ended mixer with inductive matching. The latter are shown in Figure 51 and are 162 K for the C_{j0} = 0.25 pF case and 348 K for the C_{j0} = 1.0 pF case.

It is not possible to apply the noise temperature results generated by DIODEMX to predict the noise performance of the direct conversion mixer for two reasons. First, the lack of agreement between the SPICE generated results and DIODEMX's results for the conversion loss estimate raise the question that the simulation may require analysis of the mixer at a greater number of frequencies. Second, because DIODEMX is generally used to predict the performance of mixers whose f_{IF}'s are at microwave frequencies, this program does not consider the effect of 1/f noise in assessing mixer noise temperature. Therefore DIODEMX's estimates do not apply to mixers operating at low frequencies such as a direct conversion mixer.

The task of predicting mixer noise temperature is one which deserves greater study. It would be interesting to see the effect on mixer noise temperature of using diodes with varying saturation currents and to quantize the effect of 1/f noise. Such estimates require problem formulation in the frequency domain and thus are tractable with current frequency domain techniques. However as our design tool generates the Fourier transform of many mixer waveforms, it too can be used to solve this problem.

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5.5 Single Balanced Mixer Design

5.5.1 Optimization Strategy

As discussed in Section 4.3.2, the introduction of a transformer in the mixer circuit causes certain relationships between circuit variables to appear. First, L_1, which is equal to L_2 and L_3, must be chosen so that $|Z(L_1)| \gg (\frac{n_1}{n_2+n_3})^2 R_L = R_L/4$ at f_{LO} (see 117 for further details). Second, it is necessary to apply a bias voltage for operation with other than very low drive levels. According to eqn. 38, V_{bias} = - $\langle V_{r_{L_2}} \rangle$ - $\langle V_d \rangle$ where $\langle V_{r_{L_2}} \rangle$ is the voltage drop accross the secondary L_2. Third, the isolation of the RF and LO signals at certain points in the mixer mean that separate circuits can be tailored for each signal and optimized to enhance the effect of each source on the conversion process. Specifically this separation allows the designer to create a phasing circuit for the RF signal and a waveform shaping network for the LO signal. Shown in Fig. 72 is the original balanced mixer circuit of Fig. 39 now modified by the addition of the phasing network and the waveform shaping network. These three factors affect the strategy used for optimization of the balanced mixer from that used for the single-ended mixer.

One of the advantages of balanced over single-ended design is that the large signal characteristics of the diode are set by the LO and any circuits at the LO port whereas the small-signal currents can be set by circuits in the RF port only. Because the isolation from LO to RF and vice versa is high, these two effects can be controlled independently.

The optimization process begins as before with an evaluation of $Z_{in}(f_{RF})$ at the RF port. The circuit nodes at which Z_{in} is calculated are shown in Fig. 72. For a given diode state, ie. value of T_{TON}, the input impedance of the balanced mixer is lower than that measured for the single-ended mixer as two diodes are now driven in parallel. Thus $Z_{in}(f_{RF})$ must be evaluated at the RF port from previous balanced runs not from single-ended runs. Similarly the phasing circuit designed for the single-ended mixer can not be used for the balanced mixer: a circuit specific to it must be designed. This difference in $Z_{in}(f_{RF})$ between mixer circuits can be seen by comparing the single-ended mixer results listed in Table 8 with those shown in Table 11 for the

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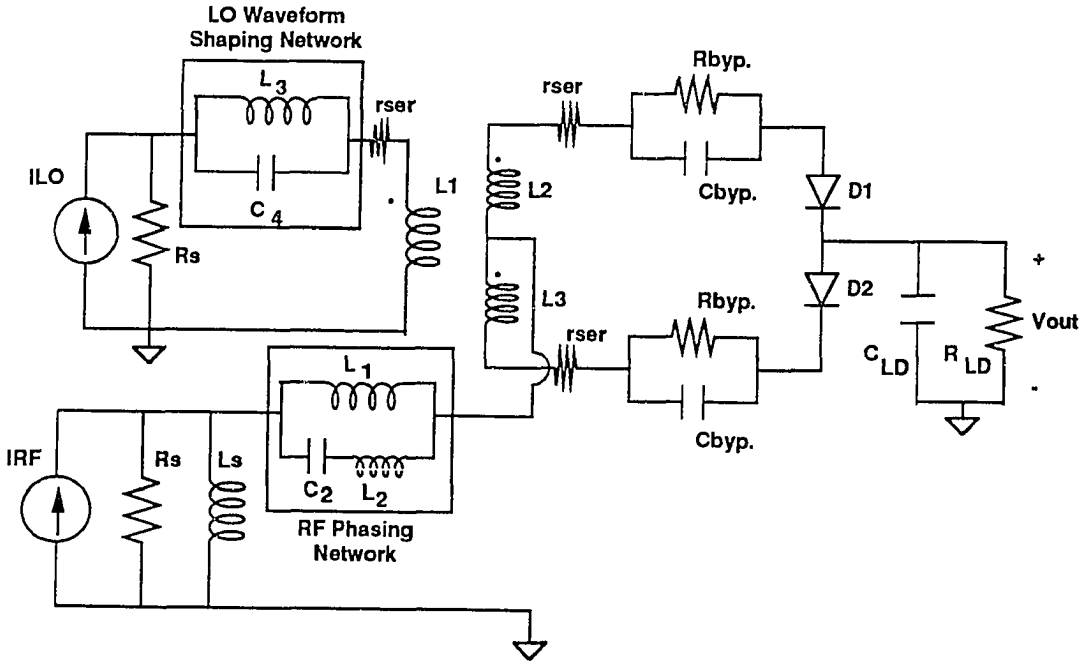


Figure 72: Schematic of the optimized balanced mixer showing the location of the RF phasing network and the LO waveform shaping network.

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balanced mixer. Both circuits have been designed for purely resistive diodes but have been simulated with diode having a $C_{j0} = 0.25$ pF. Comparing $Z_{in}(f_{RF})$ results for comparable 'ON' times, $T_{TON} = 0.38\ T_{LO}$ for the single-ended mixer and $T_{TON} = 0.32\ T_{LO}$ for the balanced mixer, we see that $Z_{in}(f_{RF}) = 761\Omega\ \angle -57°$ for the single-ended mixer and $565\Omega\ \angle -67°$ for the balanced mixer.

Once the starting value for $Z_{in}(f_{RF})$ has been selected from a previous run, a phasing circuit is designed to provide a rough conjugate match to this input impedance. f_1 and f_2 are set as before to $\sim 2f_{LO}$ and $\sim 7f_{LO}$, respectively. The values of R_S, L_1, C_2, and L_2 are calculated from eqns. 59, 60, 61 and 62. This can be considered a good point to begin the iterative search for $C_{L_{min}}$ as long as $Z^*_{in}(f_{RF}) \sim Z_S(f_{RF})$. First the bias voltage is varied, then $|Z_S(f_{RF})|$, $\angle Z_S(f_{RF})$, and R_L are adjusted until a local optimum for C_L is found. Finally f_1 is varied and $f_2 \rightarrow \infty$ by setting L_2 to zero.

Both the transformer's primary and secondaries have a self-inductance of 5.6 μF (for operation at 900 MHz) and a coupling coefficient of 1.0 in all the runs discussed in this thesis. The RF source inductor, L_S, is included in all runs so that $Z_S(DC) = 0$ and $Z_S(f_{RF})$ is very low. This causes the diode's embedding impedances at the small-signal IF sideband frequency and at DC to be approximately equal to R_S. C_S is not used in the balanced circuit because the RF source impedance is very low in comparison with R_L. These last points will be elaborated upon at the end of this section.

When the RF phasing network has been designed and optimized, the LO waveform shaping network is designed. The purpose of this circuit is to optimize the large-signal diode waveforms, $G_B(t)$ and $C_B(t)$ in order to maximize the benefits of the diode's nonlinear characteristics. This network then sets the large-signal diode waveforms so that circuit performance can be enhanced from the parametric pumping of C_B. The initial values for the tank circuit depicted in Fig. 72 are chosen so that L_3 resonates with the diodes' barrier capacitance and so that L_3 and C_4 resonate at $3f_{LO}$. $R_S|_{LO}$ and L_3 can be found from eqns. 52 and 53 assuming that $\langle C_B \rangle \sim C_{j0}/2$ and $\langle R_B \rangle \sim 2R_B$. The latter values take into account that the LO sees the two diodes in series rather than in parallel as seen from the RF port. The starting value can be written

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as:

$$R_S|_{LO} = \frac{2R_B}{1+(\omega_{LO}C_{j0}R_B)^2}, \tag{63}$$

$$L_3 = \frac{C_{j0}R_B^2}{1+(\omega_{LO}C_{j0}R_B)^2}, \tag{64}$$

$$C_3 = \frac{1}{\omega_{LO}^2 L_3}. \tag{65}$$

The optimum values for this resonant circuit are determined by simulations through the evaluation of C_B and ultimately C_L. Once C_L has reached a minimum value or further improvements in C_L with changes in L_3 and C_4 are insignificant, the optimization procedure is considered complete.

5.5.2 Phasing Network Design - $C_{j0} = 0.25$ pF

The performance of the single-balanced mixer with nonzero C_B is charted in Table 11 as V_{bias} is varied. It is evident from this table that C_L is minimized when V_{bias} is -2.0V, however T_{TON} is closest to 0.50 T_{LO} when V_{bias} is -0.5V. Optimization f the single-ended mixer showed that $T_{TON} \rightarrow 0.5\ T_{LO}$ is a condition for reaching $C_{L_{min}}$. Hence we choose to design the source impedance provided by the phasing circuit at f_{RF} to be between these two bias points. Z_S is then set to $435\Omega\ \angle 75°$; f_1 is set to $1.95f_{LO}$ and f_2 to $7.5f_{LO}$. The circuit elements are then:

$$\begin{aligned} R_S|_{RF} &= 109\Omega, \\ L_S &= 0.19\mu H, \\ L_1 &= 0.054\mu H, \\ C_2 &= 0.145pF, \\ L_2 &= 3.85nH, \end{aligned}$$

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for operation at $f_{RF} = 909$ MHz and $f_{LO} = 900$ MHz. After this circuit is simulated, the bias voltage will be varied to minimize C_L.

The large-signal currents, energy waveforms and small-signal currents for this circuit, *sbm600*, are shown in Figures 73 and 74. The conversion loss of the circuit is 5.4 dB, T_{TON} is 0.32 T_{LO} and $Z_{in}(f_{RF})$ is 539 Ω $\angle -71°$. The addition of the phasing circuit without bias optimization has, as in the single-ended case, caused only a small improvement (0.7dB) in C_L. However $Z^*_{in}(f_{RF})$ is close enough to $Z_S(f_{RF})$, measured at the RF port, that this circuit can be used as a starting point. This is especially true given that $Z_S(f_{RF})$ will decrease as V_{bias} is reduced to increase T_{TON}. In Fig. 73(b) I_d, I_{d_r}, V_d are plotted along with I_{out}, V_{sec}, and V_{out}. The first three variables use the left-hand scale of the plot; the last three use the right-hand scale. I_{out} corresponds to the current flowing into the load; it is also equal to the current flowing into the phasing network or to the current flowing into the common node of the secondary. It is a small-signal current only as the LO currents in the load sum to zero if the diodes are well matched, as they are modelled to be. From this figure, $\langle I_{out}(T_1)\rangle$ is found to be 35.7 μA; $\langle I_{out}(T_2)\rangle$, which should be near zero, is found to be -5.5 μA. $V_{out}(f_{IF})$ and C_L can be calculated for this run according to eqns. 40 and 41: they are found to be 35.7 mV and 5.33 dB which compares well with the values calculated by the Fourier transform of $V_{out}(t)$, 35.3 mV and 5.42 dB. This agreement is important as it confirms that the graphical output can be used to guide the C_L optimization of the mixer. Figure 73(c) can be used to find the maximum and minimum excursion of C_B; they are 0.52 pF and 0.076 pF, respectively, representing an variation of 1.78 C_{j0}.

In Fig. 74(a) the total energy due to the LO and RF sources in C_B is plotted along with the energy stored in each of the phasing circuit elements, L_1, C_2, and L_2. The energy stored in the last three components is due solely to the RF source hence these variables must be multiplied by the constant shown in the figure in order to be plotted on the same scale as E_{C_B}. In contrast to the comparable single-ended plots, I_{L_1}, V_{C_2}, and I_{L_2} are known from the SPICE output not calculated from the large-signal currents at T_1 and T_3.

In Fig. 74(b), the total current in the diode, I_d, and the current in R_B, I_{d_r}, are plotted along with the current in each of the phasing circuit elements, I_{L_1}, V_{C_2}, and

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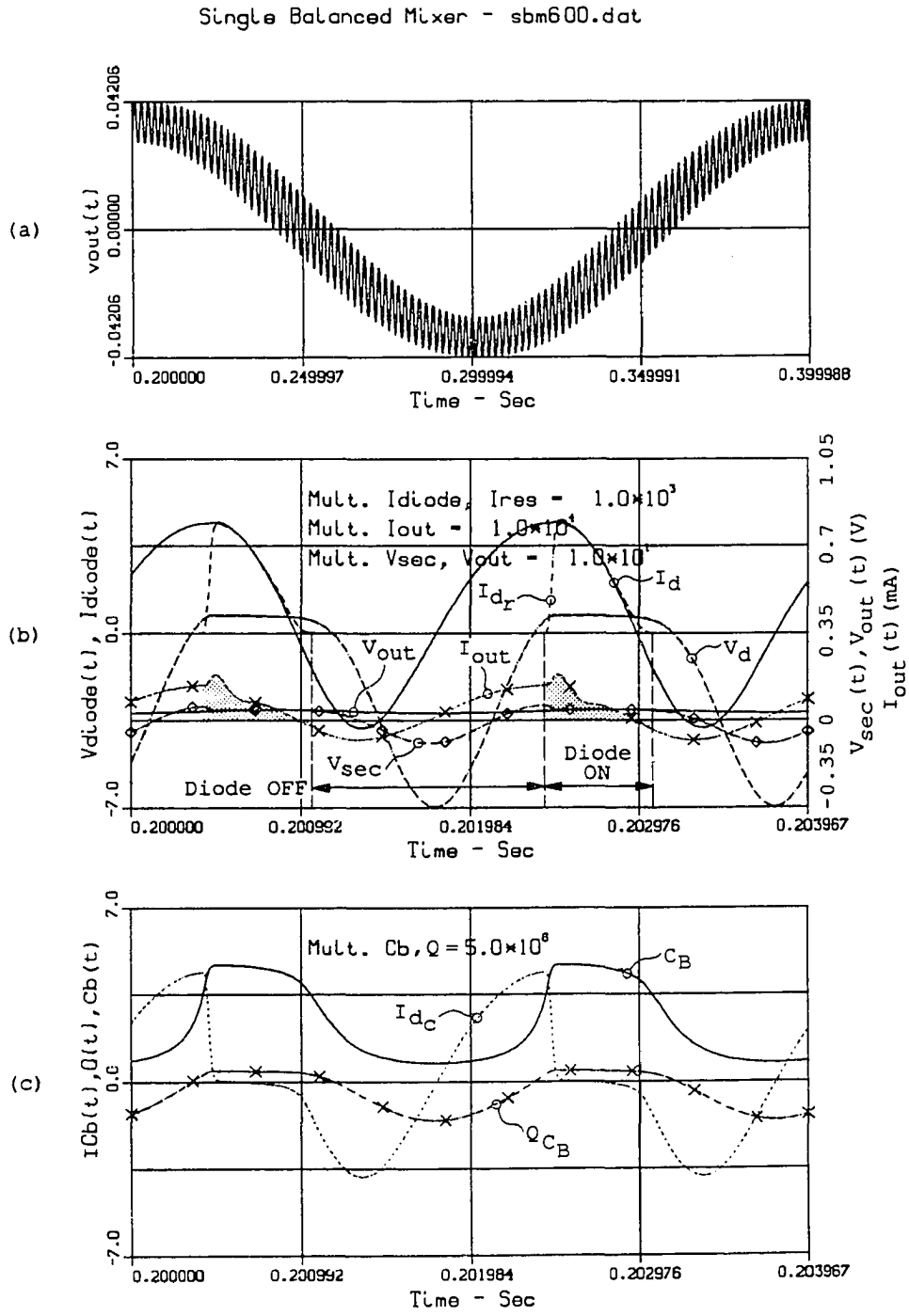


Figure 73: Large-signal waveforms for the balanced mixer - initial phasing circuit in place ($C_{j0} = 0.25$ pF).

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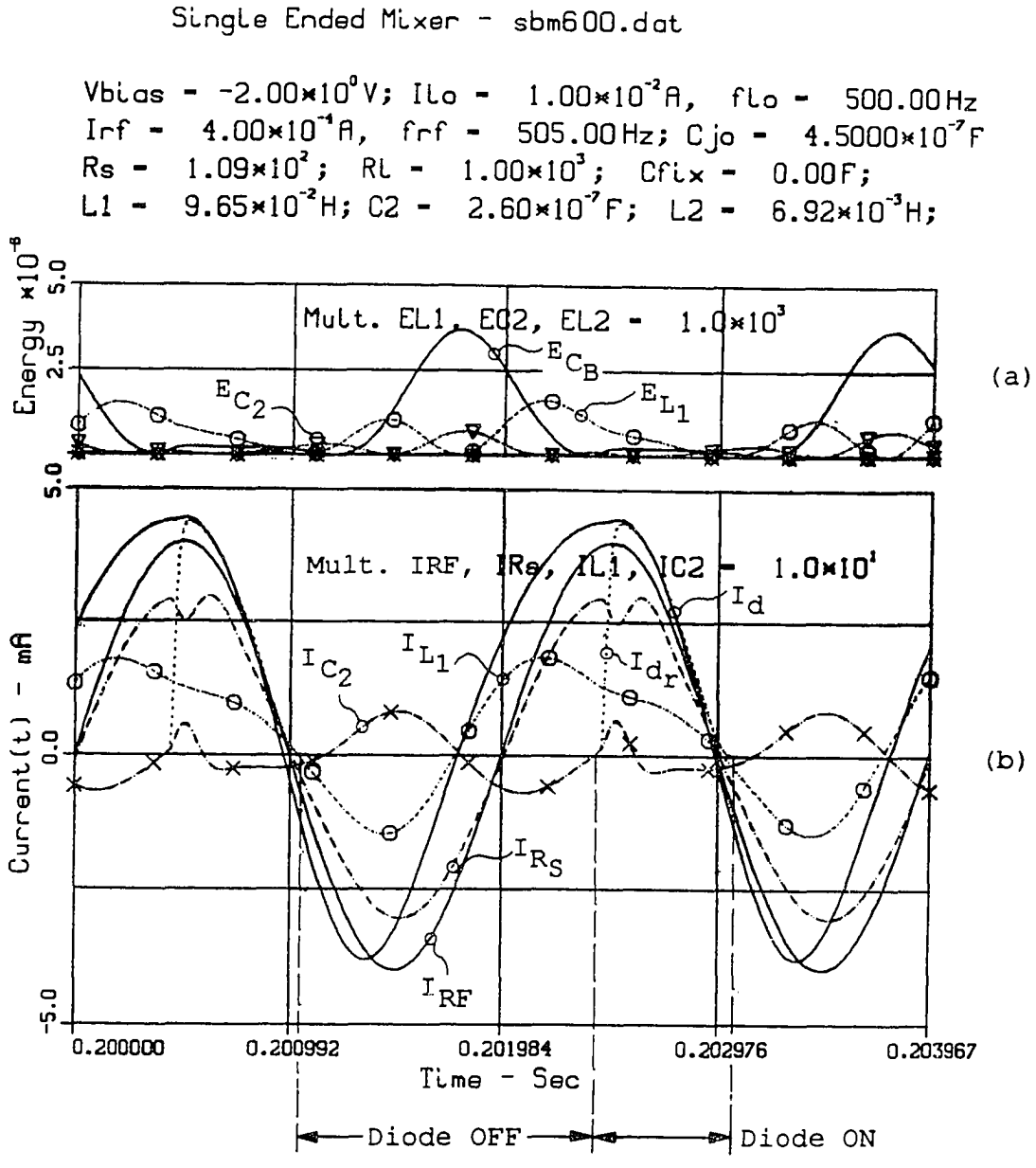


Figure 74: Energy waveforms and RF currents in the balanced mixer - initial phasing circuit in place ($C_{j0} = 0.25$ pF).

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I_{L_2}. In addition I_{R_S} and I_{RF} are shown. Again, in order to plot these five small-signal currents on the same graph as the large-signal currents, they are multiplied by the constant shown on the graph. The variables plotted in this graph differ from those on a typical single-ended mixer, eg. Fig. 56, as there I_{d_r} gave the RF component of the diode current whereas here the entire diode current is plotted. From this figure it can be seen that I_{RF} is being dissipated in R_S, nearly 2/3 of I_{RF} is I_{R_S}. The phase relationship between the large-signal I_d and I_{RF} can also be seen. Ideally I_{RF} should be in phase with I_{L_1}, as shown in Fig. 52, and should lag I_d by 90° as the RF current can then be transferred to L_1 and then to R_B as the diode turns 'ON'. This behavior can be seen in the optimized circuit.

Optimization of V_{bias}

Using the above circuit as a starting point, the bias voltage is varied to increase T_{TON} and reduce C_L. This process is far simpler than with a single-ended mixer as the bias and drive conditions set by I_{LO} and V_{bias} can be set separately from the small-signal circuit conditions. This is due to the separation of the LO and RF circuits. The value of V_{bias} required to set $T_{TON} \rightarrow T_{LO}$ can be immediately ascertained from Table 11 to be -0.5V. The circuit of *sbm600* is then rerun with this bias level. The performance parameters of the resulting circuit, labelled *sbm601*, are shown in Table 23 where they are juxtaposed with those of *sbm600* and the two runs with comparable bias achieved without using any circuit to compensate for C_{j0}. These two runs, taken from Table 11, are labelled *sbm1001* and *sbm3151* for V_{bias} = -0.5 V and -2.0 V, respectively. From this table it can be seen that the diode characteristics are indeed set by the large-signal source: $V_{d_{min}}$, $I_{d_{max}}$, T_{TON}, T_{NL}, and $Z_{in}(f_{RF})$ are nearly identical when the phasing network is in the circuit or absent from it. The effect of the initial phasing circuit and of the bias adjustment are clearly visible: run *sbm601* has a 1.9 dB lower C_L than run *sbm600* and a 2.6 dB lower C_L than the uncompensated balanced mixer with C_{j0} = 0.25 pF.

Figures 75 and 76 show the large-signal currents, energy waveforms and small-signal currents for this circuit, *sbm601*. Comparing Fig. 73(a) and Fig. 75(a) the presence of more high frequency sideband frequencies can be seen; their increased

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Table 23: Balanced Mixer Characteristics vs Circuit and Drive Conditions ($C_{j0} = 0.25$ pF; $I_{RF} = 0.4$ mA.)

	sbm3151	*sbm1001*	*sbm600*	*sbm601*
Circuit and Drive Condidions:				
V_{bias}, I_{LO}	-2.0V, 13mA	-0.5V, 13mA	-2.0V, 13mA	-0.5V, 13mA
$R_S\|_{RF}$, $R_S\|_{LO}$	1K, 1K	1K, 1K	109Ω, 1K	109Ω, 1K
R_L, C_{LD}	1K, 2.8pF	1K, 2.8pF	1K, 2.8pF	1K, 2.8pF
L_S, C_S	1.8μH, 0	1.8μH, 0	0.19μH, 0	0.19μH, 0
L_1	0	0	0.054μH	0.054μH
C_2	0, 0	0, 0	0.145pF	0.145pF
L_2	0	0	3.85nH	3.85nH
$Z_S(f_{RF})$	995Ω ∠6°	995Ω ∠6°	435Ω ∠75°	435Ω ∠75°
f_1	N.A.† N.A.	N.A., N.A.	1.75GHz	1.75GHz
f_2	N.A.	N.A.	6.75GHz	6.75GHz
Diode Condidions:				
$\frac{T_{NL}}{T_{LO}}$, $\frac{T_{TON}}{T_{LO}}$	0.07, 0.32	0.07, 0.46	0.07, 0.32	0.07, 0.46
$V_{d_{min}}$, $I_{d_{max}}$	-7.2V, 4.6mA	-3.7V, 6.2mA	-7.0V, 4.4mA	-3.5V, 6.1mA
$\langle G_B \rangle$	28.6 mmho	65.5 mmho	28.6 mmho	65.5 mmho
$\langle C_B \rangle$	0.26 pF	0.33 pF	0.26 pF	0.33 pF
$\langle I_{out}(T_1) \rangle$	101.0 μA	89.2 μA	35.7 μA	43.9 μA
$\langle I_{out}(T_2) \rangle$	-10.6 μA	-9.8 μA	-5.5 μA	-7.8 μA
Mixer Performance:				
C_L	6.1 dB	7.1 dB	5.4 dB	3.5 dB
$Z_{in}(f_{RF})$	565Ω ∠ − 67°	384Ω ∠ − 62°	539Ω ∠ − 71°	336Ω ∠ − 71°
Comments:				
	No match on RF port; V_{bias} variation.		Initial phasing circuit in place; V_{bias} variation.	

† Not Applicable.

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amplitude can be ascertained from the Fourier components of $vout(t)$. The maximum and minimum excursion of C_B are now found to be 0.53 pF and 0.114 pF; thus causing a variation of 1.67 C_{j0}. From Fig. 76 the change in the relative phase of I_{RF} and I_d can be seen. I_{RF} and I_{L_1}, now more in phase than in the previous circuit, lag 90° behind I_d as desired. The phase of their waveforms now resembles those in Fig. 52 more closely. Also, the amount of I_{RF} that is dissipated in R_S has decreased. Lastly the pattern of energy transfer from C_B to L_1 to R_B can be easily seen in the energy waveforms. Comparison of the energy patterns of *sbm600* and *sbm601* show that the RF energy stored in L_1 has increased from 0.9pJ to 3.25pJ.[4] This indicates that changing the large-signal waveforms, C_B and I_d, has effected the tradeoff of RF energy from C_B to L_1 to R_B and that the interaction of RF storage elements and C_B is effected by the variation in $C_B(t)$. The large increase in E_{L_1} shows that an improvement has been made in the timing of the RF energy transfer.

Final Phasing Circuit

The circuit of *sbm601* is adjusted for $|Z_S(f_{RF})|$, $\angle Z_S(f_{RF})$, R_L and f_1. The resultant circuit, *sbm384*, has the following parameters:

$$\begin{aligned} R_S|_{RF} &= 73\Omega, \\ L_S &= 0.128\mu H, \\ L_1 &= 0.0662\mu H, \\ C_2 &= 0.044pF, \\ L_2 &= 12.6nH, \\ R_L &= 2K, \end{aligned}$$

for operation at f_{RF} = 909 MHz and f_{LO} = 900 MHz. f_1 is $3f_{LO}$ and f_2 is $7.5f_{LO}$. V_{bias} and I_{LO} are still -0.5 V and -2.0 V, respectively. The conversion loss obtained is 2.6 dB, a 0.9 dB improvement over *sbm601*. T_{TON} is 0.50 T_{LO}. The output impedance at the IF port is calculated to be 2.1K $\angle -11°$.

[4]Because the energy stored in C_B is due to both the RF and LO sources, it is not of interest to compare.

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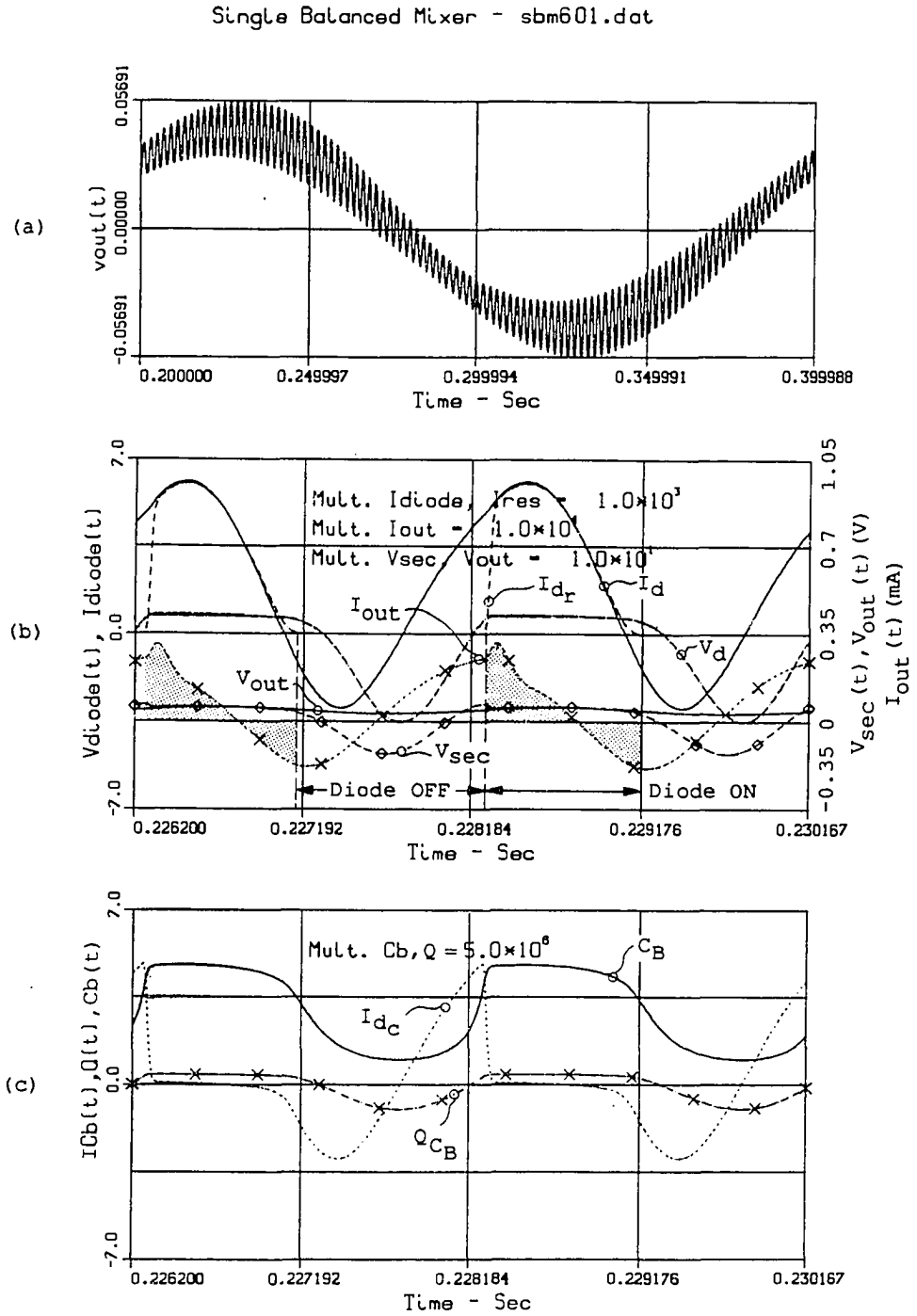


Figure 75: Large-signal waveforms for the balanced mixer - bias optimized for initial phasing circuit.

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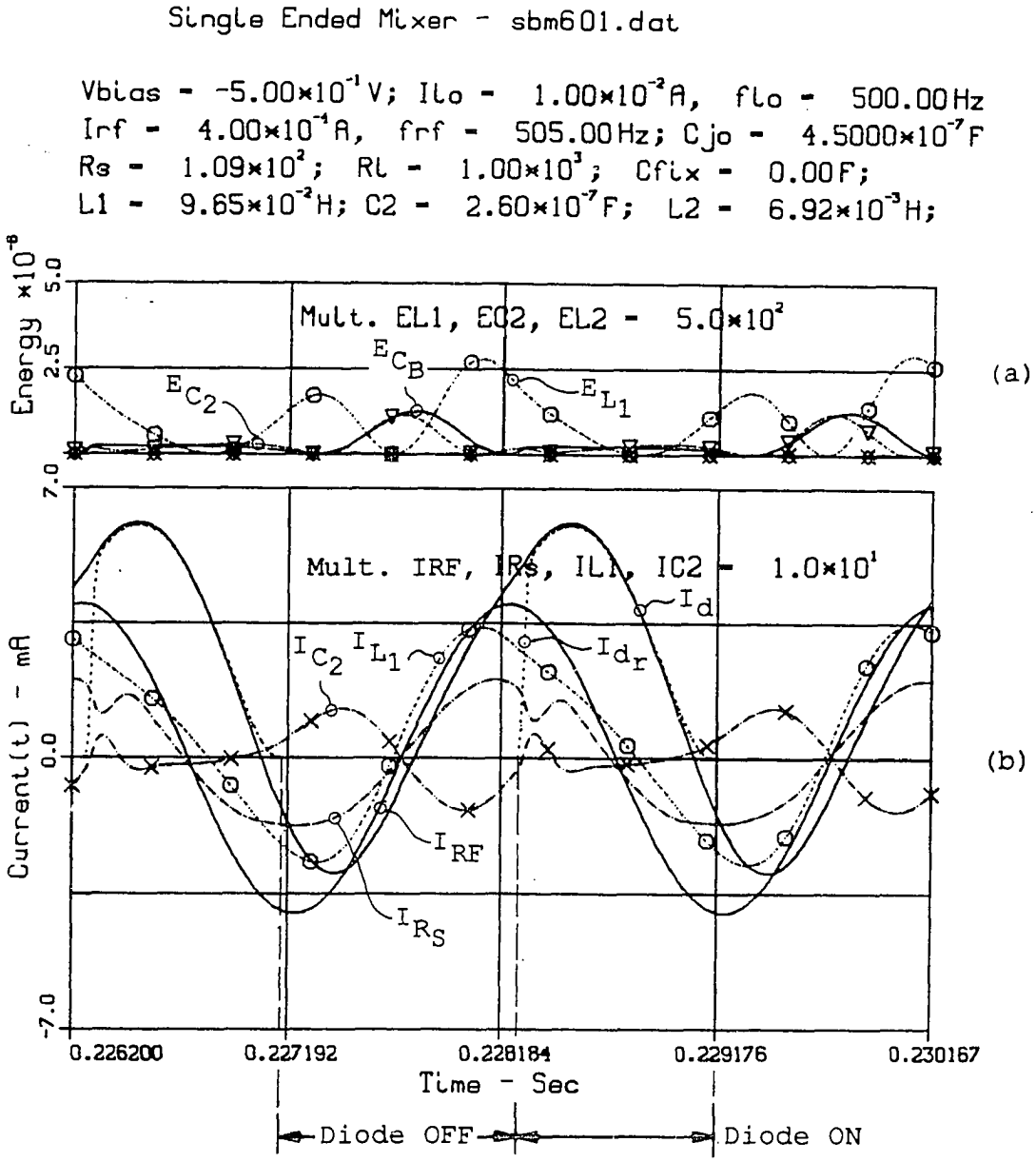


Figure 76: Energy waveforms and RF currents in the balanced mixer - bias optimized for initial phasing circuit.

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Figures 77 and 78 show the large-signal and energy waveforms, and, the RF phasing circuit currents for this run. In the first figure, the barrier capacitance can be seen to vary from 0.54 pf to 0.11 pF, equivalent to a variation of 1.7 C_{j0}. In the second figure, the typical energy patterns can be seen: E_{L_1} reaches a maximum value of 4.8pJ - the highest achieved in the balanced mixer yet. I_{RF} and I_{L_1} are, more or less, in-phase; both lag behing I_d by $\sim 90°$. L_2 can be set to zero, thus forcing f_2 to ∞ without any degradation in C_L.

C_L can be decreased by 0.1 dB by increasing the LO current from 13 mA to 18 mA. This is done in run *sbm386*. In order to maintain $T_{TON} \sim 0.5\ T_{LO}$, V_{bias} must be increased to -0.75 V. The characteristics of runs *sbm384* and *sbm386* are listed in Table 24.

As with the optimized single-ended mixer, the embedding impedances presented to both diodes at the small-signal sideband frequencies by this circuit are resistive at f_{IF}, reactive at frequencies from $2f_{LO} + f_{IF}$ to $6f_{LO} + f_{IF}$, and resistive at very high sideband frequencies. $|\ Z_{emb}(f)\ |$ is highest at $3f_{LO} + f_{IF}$. The circuit model depicted in Figure 38 is used to justify setting:

$$Z_{emb}(f) = Z_S(f)|_{RF\ Port} + Z_L(f)|_{IF\ Port}$$

where the location of $Z_S(f)$ and $Z_L(f)$ are given in Fig. 72.

Use of R_{bypass} and C_{bypass} in applying bias

As discussed in Section 4.3.2 and shown in Fig. 42, the bias voltage used in the SPICE simulation can be replaced in the balanced mixer circuit by a parallel resistor and capacitor. The rectified LO current creates a voltage drop accross R_{bypass} which is bypassed at high frequencies ($\geq f_{RF}$) by C_{bypass}. No conversion loss degradation is found as long as the impedance presented by this parallel combination is very low at f_{RF}. For example, choosing $R_{bypass} = 150\Omega$ and $C_{bypass} = 35$pF caused no significant change in C_L.

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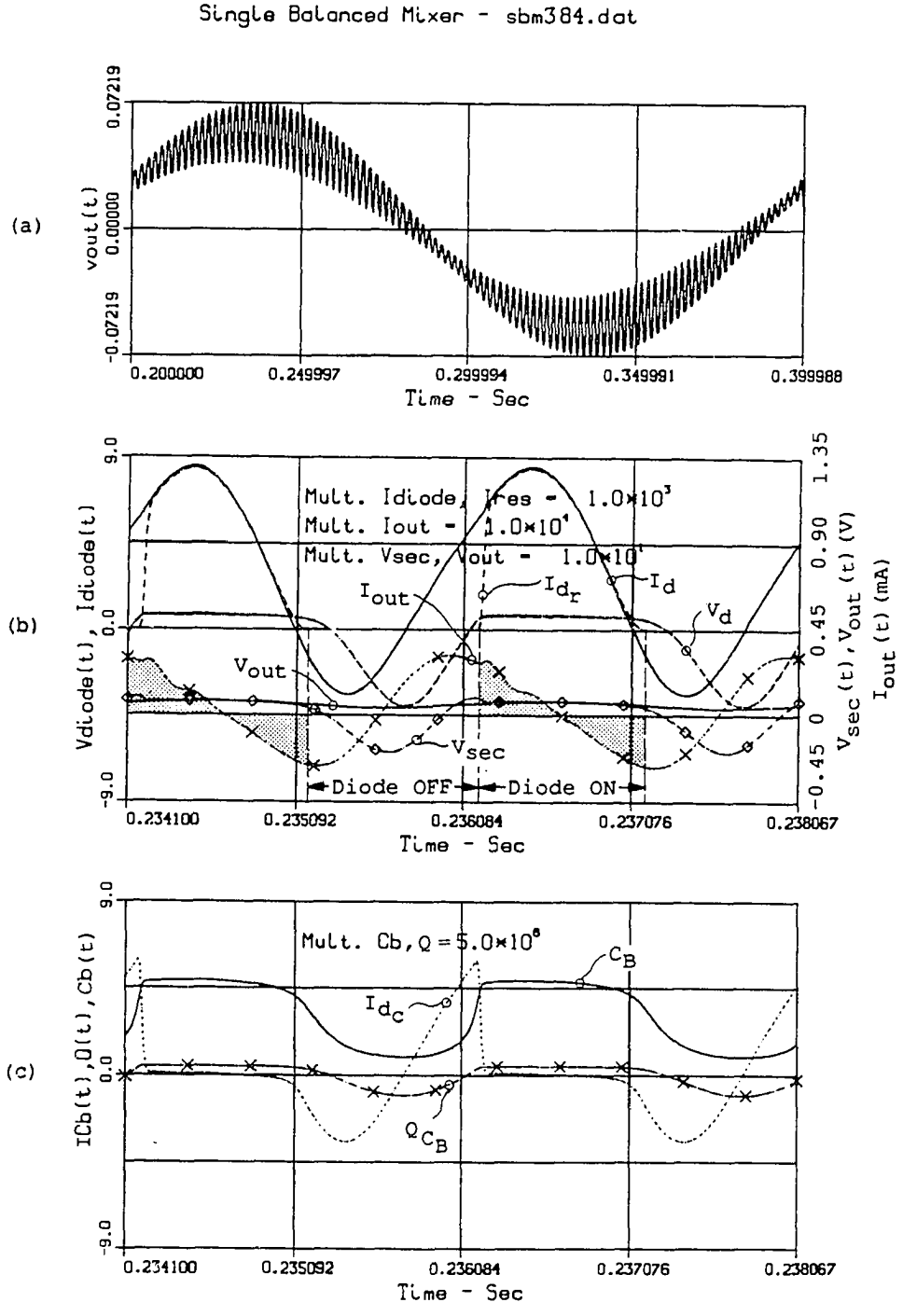


Figure 77: Large-signal waveforms for the balanced mixer - final phasing circuit in place.

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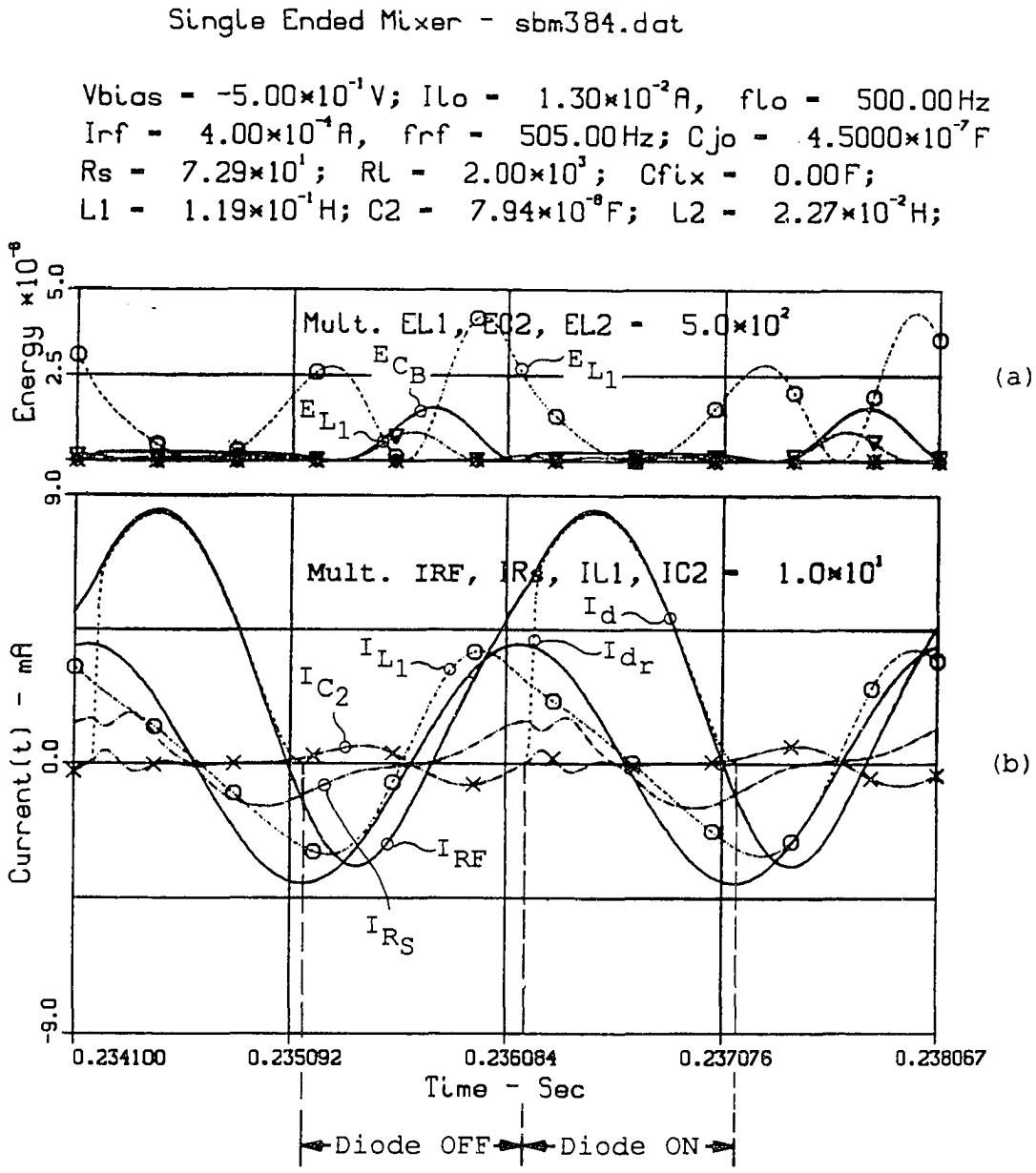


Figure 78: Energy waveforms and RF currents for the balanced mixer - final phasing circuit in place.

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Table 24: Comparison of Balanced Mixer Circuits with Phasing Network and LO Waveform Shaping Network in Place
(C_{j0} = 0.25 pF; I_{RF} = 0.4 mA.)

	sbm384	*sbm386*	*sbm5092*
Circuit and Drive Condidions:			
V_{bias}, I_{LO}	-0.5V, 13mA	-0.75V, 18mA	-0.5V, 13mA
$R_S\|_{RF}$	73Ω	73Ω	73Ω
R_L, C_{LD}	2K, 2.8 pF	2K, 2.8 pF	2K, 2.8 pF
L_S	0.13μH	0.13μH	0.13μH
L_1	0.066μH	0.066μH	0.066μH
C_2, L_2	0.044pF, 12.6nH	0.044pF, 12.6nH	0.044pF, 0.0
$Z_S(f_{RF})$	431Ω ∠80°	431Ω ∠80°	430Ω ∠80° (RF port)
f_1, f_2	2.7 GHz, 3.75GHz	2.7 GHz, 3.75GHz	2.7 GHz, 3.75GHz
$R_S\|_{LO}$	1K	1K	1K
L_3, C_4	0, 0	0, 0	0.083μH, 0.042pF
Diode Condidions:			
$\frac{T_{NL}}{T_{LO}}$, $\frac{T_{ON}}{T_{LO}}$	0.06, 0.50	0.05, 0.53	0.07, 0.51
$V_{d_{min}}$, $I_{d_{max}}$	-4.0V, 8.5mA	-5.5V, 12.3mA	-4.1V, 7.7mA
$\langle G_B \rangle$	102.5 mmho	158.2 mmho	93.8 mmho
$\langle C_B \rangle$	0.346pF	0.355pF	0.346pF
$\langle I_{out}(T_1) \rangle$	27.3μA	27.8μA	28.7μA
$\langle I_{out}(T_2) \rangle$	-9.7μA	-9.3μA	-10.9μA
Mixer Performance:			
C_L	2.66 dB	2.52 dB	2.14 dB
$E_{L_1}(T_1)$	4.8 pJ	5.2 pJ	5.5 pJ
$Z_{in}(f_{RF})$	390Ω ∠ − 79°	395Ω ∠ − 79°	389Ω ∠ − 80°
$Z_{out}(f_{IF})$	2.1K ∠ − 11°	N.C.†	2.1K ∠ − 10°
Comments:			
	Opt. phasing ckt in place.	Opt. phasing ckt in place; variation in V_{bias} and I_{LO}.	Opt. balanced mixer with phasing ckt and LO waveform ckt in place.

† Not Calculated.

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Table 25: Performance of Balanced Mixer Circuit when C_B is Replaced by the Linear Capacitor C_F

	T_{TON}	C_L
Reference Circuit: $C_{j0} = 0.25$ pF	0.53	2.80 dB
C_F:		
0.0 pF	0.69	16.09 dB
0.055 pF	0.62	8.36 dB
0.111 pF	0.56	5.83 dB
0.139 pF	0.54	5.79 dB
0.167 pF	0.52	6.13 dB
0.194 pF	0.51	6.67 dB
0.222 pF	0.49	7.31 dB
0.333 pF	0.43	10.02 dB
0.444 pF	0.39	12.42 dB

Use of Unmatched Diodes

When diodes with differing C_{j0}'s were used in the circuit of run *sbm384*, a 0.2 dB increase in C_L was measured. The C_{j0} value of one diode was 0.25pF, the other was 0.2pF.

Performance Improvement due to C_B

The circuit depicted in run *sbm384* was simulated with a purely resistive diode which had in parallel with it a fixed capacitor, C_F, exactly as was done with the single-ended mixer. The degradation in conversion loss as C_F is varied is listed in Table 25. The best conversion loss is obtained when C_B is replaced by a fixed capacitor of value 0.14pF, assuming that the circuit and bias are unchanged. The conversion loss then is 5.8 dB, 3 dB higher than obtained with the practical diode having $C_{j0} = 0.25$pF.

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5.5.3 Local Oscillator Waveform Shaping Network - C_{j0} = 0.25 pF.

The waveform shaping network is designed to control the large-signal waveforms in the mixer so that the nonlinear barrier capacitance can be driven to optimize the interaction of C_B and the phasing network on the RF port. As this circuit influences the large-signal waveforms it is placed on the LO port as shown in Fig. 72. Eqns. 63, 64, and 65 can be used to calculate the starting circuit for optimization. For this mixer C_{j0} is 0.25 pF and R_B is 500Ω. $R_S|_{LO}$, L_3, and C_4 are then found to be:

$$\begin{aligned} R_S|_{LO} &= 666\Omega, \\ L_3 &= 0.083\mu H, \\ C_4 &= 0.042pF, \end{aligned}$$

for operation at f_{LO} = 909 MHz. This circuit produces a 0.35 dB decrease in C_L when used in conjunction with the phasing circuit and bias conditions of run *sbm384*.

The fully optimized balanced mixer, *sbm5092*, is obtained by increasing $R_S|_{LO}$ to 1K. Variation in L_3 and C_4 from their initial values did not reduce C_L. The source impedance provided by this circuit is given below:

$$Z_S(f) = \begin{cases} 1.1K & \angle 28° & f = f_{LO} \\ 2.0K & \angle 59° & f = 2f_{LO} \\ \infty & \angle 90° & f = 3f_{LO} \\ 2.6K & \angle -68° & f = 4f_{LO}. \end{cases}$$

No changes in the drive conditions or phasing circuit of the initial mixer circuit *sbm384* have been made. The optimized balanced circuit with phasing circuit and waveform shaping network is shown for the case of C_{j0} = 0.25 pF in Fig. 79.

The performance of run *sbm5092* is listed in Table 24. Its conversion loss is 2.1 dB, 0.6 dB lower than that achieved without it. The large-signal waveforms, energy waveforms, and small-signal RF currents can be seen in Figures 80 and 81. From the first figure C_B can be seen to vary from 0.54pF to 0.11pF, which represents a change

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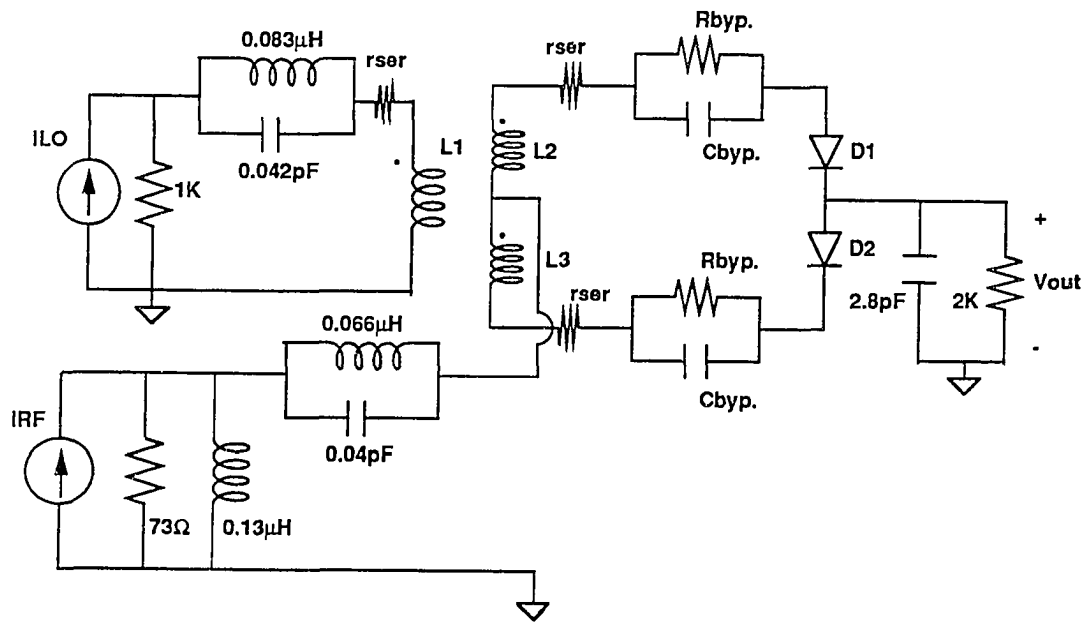


Figure 79: Optimum circuit for the balanced mixer ($C_{j0} = 0.25$pF).

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in C_B equal to 1.7 C_{j0}. From the second figure, the desired energy transfer pattern can be seen: $E_{L_1} = 5.5$pJ, an increase from that achieved without the LO waveform circuit.

As can be seen from the component values in Fig. 79, the balanced mixer circuit elements can be realized with a combination of lumped elements and microstrip elements. The latter are necessary to create C_2 and C_4, the small capacitances required by the RF and LO networks.

5.6 Direct Conversion Mixers

The time domain based mixer design tool has been used to optimize mixer performance, both conversion loss and impedance transformation, with practical mixer diodes having both series resistance and capacitance. Medium barrier p-type Si Schottky diodes are used as they have been characterized as having low 1/f noise. Mixers have been designed with devices whose barrier capacitance at zero bias, C_{jo}, is as great as 1.0 pF; the maximum typically encountered for UHF mixer diodes. Two mixer types have been optimized: single-ended and single-balanced mixers. Figure 82(a) depicts the optimized single-ended mixer. The local oscillator source is applied to the circuit via a directional coupler. The optimized single-balanced mixer is illustrated in Fig. 82(b). Balanced mixers differ from single-ended mixers in several ways: first the output signal has fewer spectral components as it is isolated from the LO source and its harmonics (therfore providing greater isolation of the RF and LO signals at the output port); second the mixer has fewer noise components at its output as the amplitude modulated component of the LO noise is cancelled internally by the balanced circuitry; third good circuit VSWR can be obtained. For these reasons the added circuit elements and active components of balanced mixers are often tolerated.

Table 26 lists the optimized performance of two single-ended mixers with C_{jo} of 0.25pF and 1.0pF and the performance of a single-balanced mixer with a C_{jo} of 0.25pF. Single-ended mixers have a phasing circuit (L_1, C_2) to achieve low C_L; balanced mixers have both phasing circuit (L_1, C_2) for RF signal and driving waveform circuit (L_3, C_4) for LO signal to achieve low C_L.

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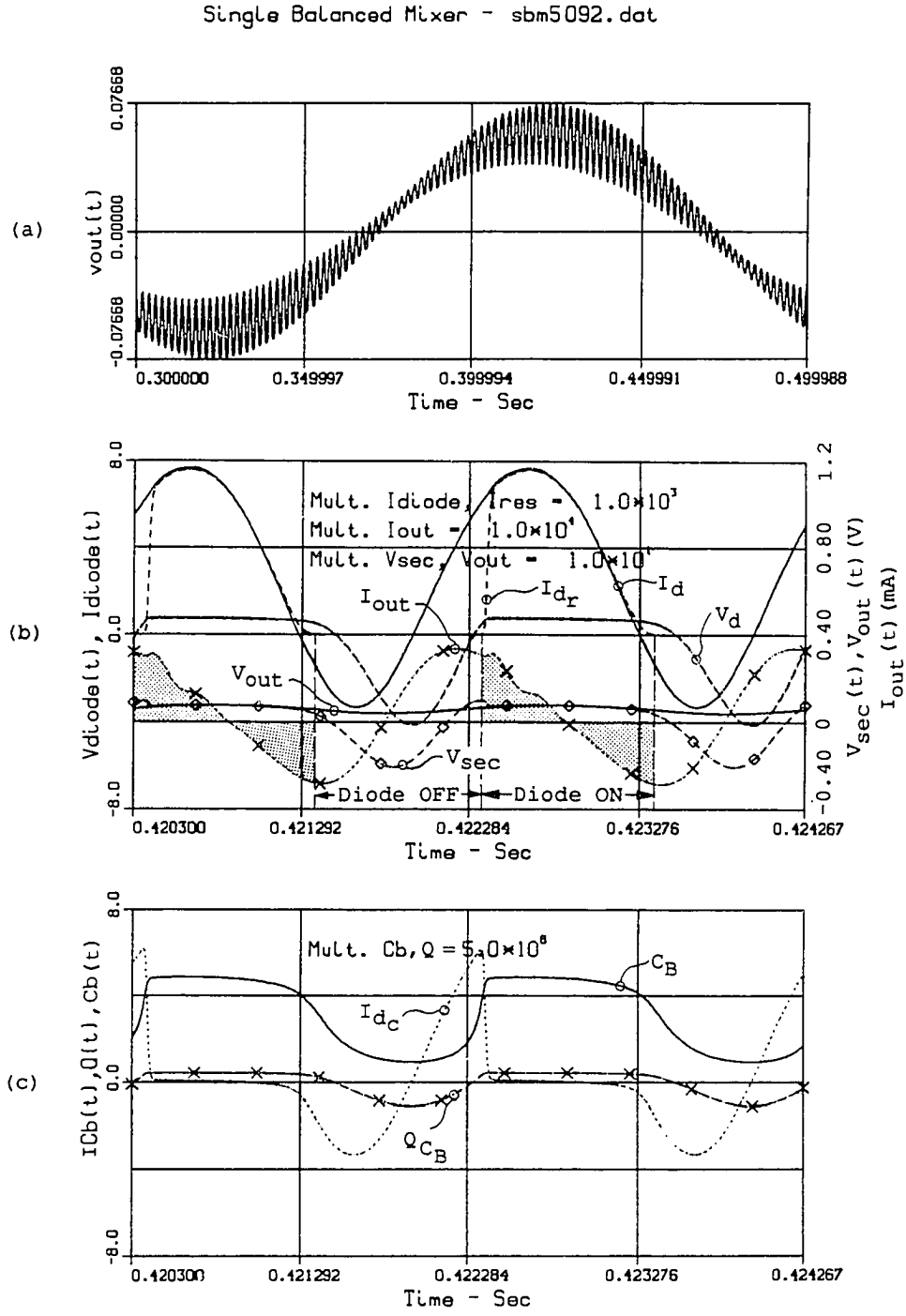


Figure 80: Large-signal waveforms for the final balanced mixer ($C_{j0} = 0.25$ pF).

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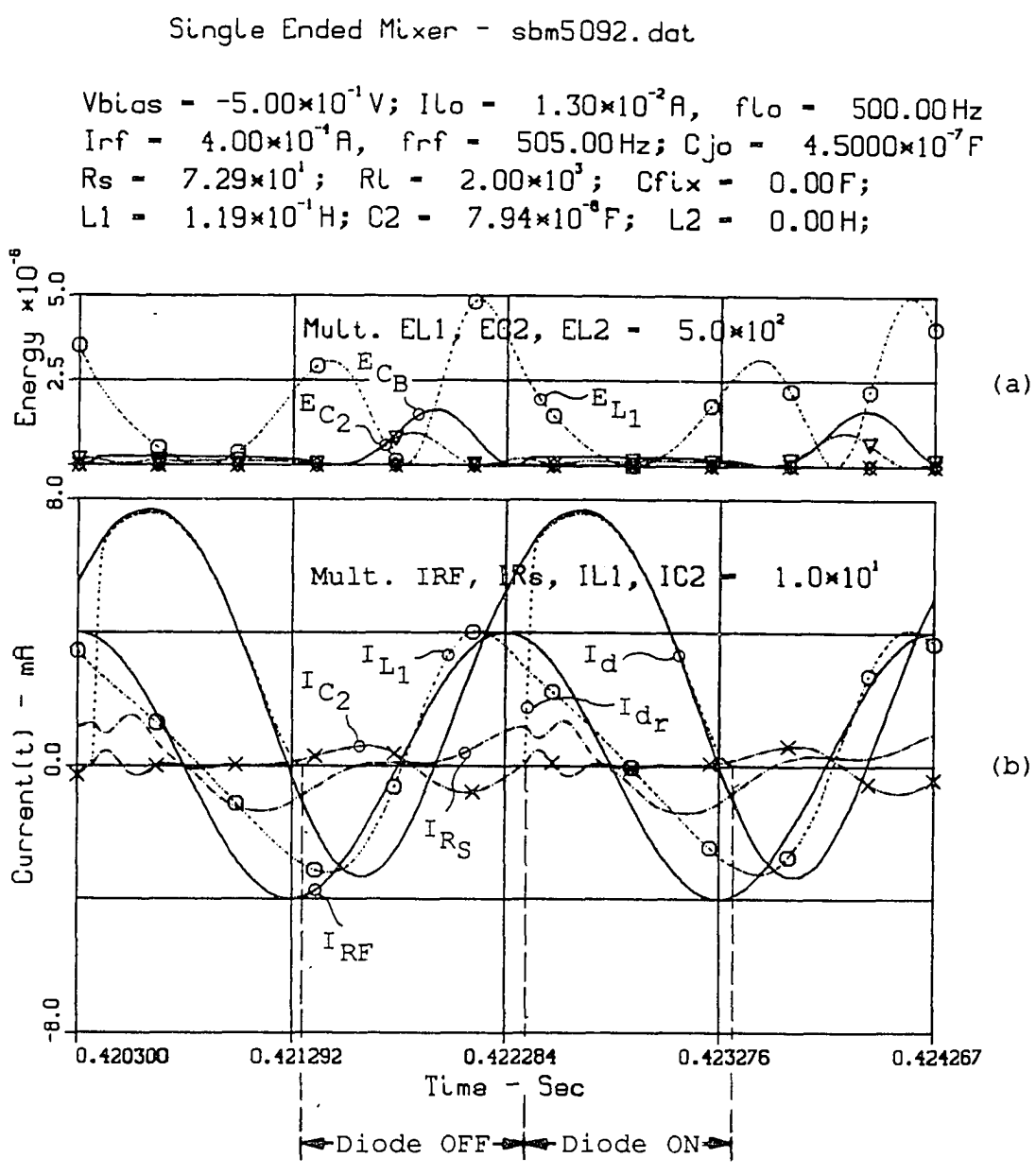
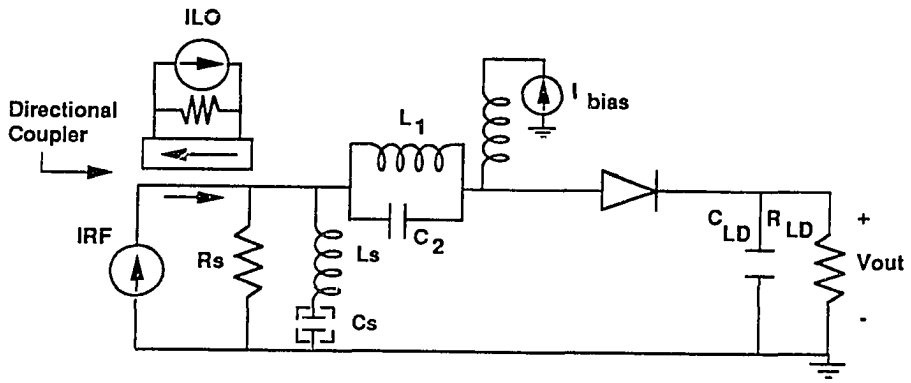
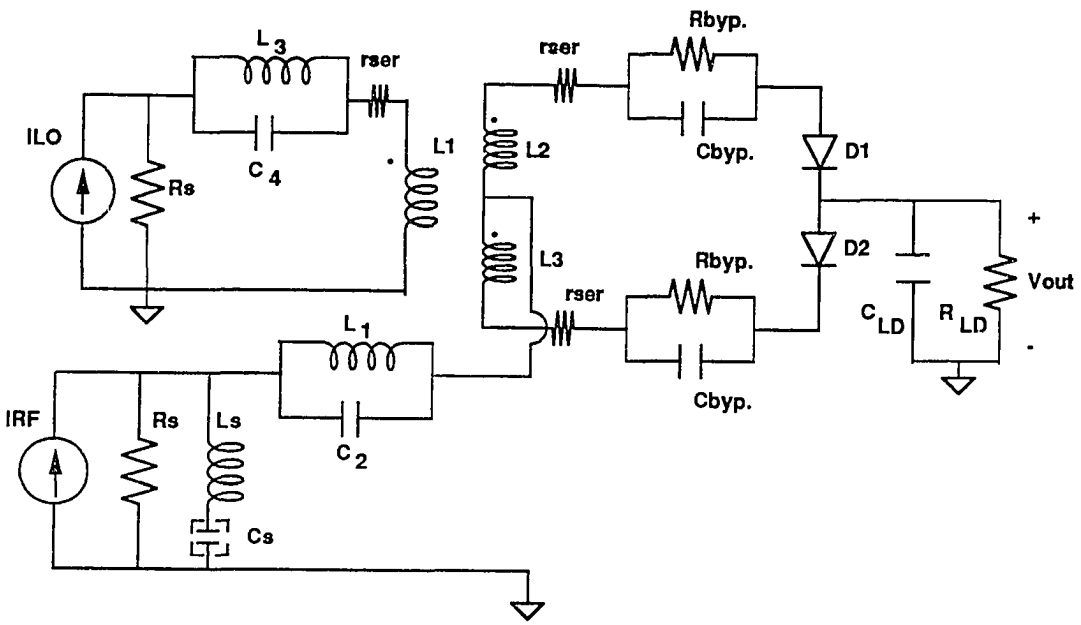


Figure 81: Energy waveforms and RF currents for the final balanced mixer (C_{j0} = 0.25 pF).

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(a) single-ended mixer



(b) single-balanced mixer

Figure 82: Schematics of the two mixer types simulated.

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Noise temperature estimates at the mixer output frequency are based on mixer noise analysis for shot and thermal noise processes as detailed by Maas [43]. Only single-ended mixer noise temperatures can be calculated. The embedding network is assumed to be noiseless. The analysis makes use of the Fourier coefficients of the diode's small signal barrier resistance, $R_B(t)$, and barrier capacitance, $C_B(t)$, to calculate the noise power at the output termination. This method for evaluating mixer noise temperature does not include 1/f noise. The balanced mixer noise temperature has been estimated from Alpha manufacturer's characterization of 1/f diode noise[5] and from estimates of circuit effects on mixer noise. The latter is expected to be low as the mixer circuit parametrically pumps the barrier capacitance to achieve low conversion loss. The worst-case noise temperature for the balanced mixer is believed to be $\approx$ 500 K. Better characterization of mixer noise over frequency remains to be done.

From Table 26 the conversion loss of the balanced mixer can be seen to be lower than that of the single-ended mixer. It is also capable of translating from a lower input impedance (73Ω) to a higher output load impedance (2KΩ).

5.7 Conclusion

This chapter discusses the design of mixers with practical diodes, ie. diodes possessing significant barrier capacitance in addition to series and barrier resistance. Mixer circuits have been designed which will enable lower conversion losses to be reached with diodes having zero bias barrier capacitance, C_{j0}, values $\leq$ 1.0 pF than with a purely resistive diode mixer while simultaneously permitting low mixer noise temperatures to be reached. For operation with diodes having $C_{j0} \leq$ 0.25 pF, single-ended mixers with conversion losses of 3 dB and balanced mixers with conversion losses of 2 dB can be designed. The 1 dB improvement in C_L for the balanced mixer is due to the inherent isolation of the RF and LO ports. This permits the use of a waveform shaping circuit on the LO port in addition to a phasing circuit on the RF port in contrast to the single-ended mixer which can be designed with only the phasing

[5]Correspondance with Stanley Howe of Alpha Industries Inc. in March 1987.

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Table 26: Direct Conversion Mixer Performance

	Single-Ended Mixer		Single-Balanced Mixer
C_{jo}	0.25 pF	1.0 pF	0.25 pF
Bias and LO Drive:			
I_{LO} Bias	13mA	20mA	13mA
Bias	13mA	30mA	-0.5 V
RF source impedance:			
$R_{S_{RF}}$	197 Ω	66 Ω	73 Ω
L_S	3.5 μH	1.2μH	0.13 μH
RF matching circuit:			
L_1	0.11 μH	0.04 μH	0.07 μH
C_2	0.03 pF	0.12 pF	0.04 pF
LO matching circuit:			
L_3	none	none	0.08 μH
C_4	none	none	0.04 pF
Output impedance:			
R_L	1.5 KΩ	500 Ω	2 KΩ
C_{LD}	3 pF	3 pF	3pF
Performance:			
C_L	3.1dB	4.3dB	2.1 dB
$\frac{R_L}{R_{S_{RF}}}$	7.6	7.6	27.4
T_{mixer}	135 K †	265 K †	≈ 500 K

† Estimated from frequency domain analysis program DIODEMX.

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circuit. For operation with diodes having C_{j0} of 1.0 pF, a 4.25 dB conversion loss was achieved for the single-ended mixer. Although a balanced mixer with this C_{j0} has not been designed, there is no reason to believe that the same conversion loss improvement over the single-ended mixer would not be realized.

These low conversion loss results concur with the experimental results obtained by North [67], Liechti [41], and Dragone [15]. North obtained low conversion loss with a 'Y' mixer (LO harmonics and sideband frequencies $n > 1$ terminated in short-circuits); Liechti measured a 3.5 dB conversion loss in a 3 GHz four frequency broadband 'Y' mixer (real power flow at f_{RF}, f_{IF}, f_{IMAGE}, and f_{LO} only); and Dragone designed a 1.25 GHz 'Z' mixer (LO harmonics and sideband frequencies $n > 1$ terminated in open-circuits) which could be tuned to have either a 0.7 dB noise figure with conversion loss or a 2.3 dB noise figure with conversion gain. In comparison, the optimized mixer circuits used in our simulations provide a complex match to the diode at f_{IF} and at the three similar frequencies f_{RF}, f_{LO}, and f_{IMAGE}. They provide a reactive match from $2f_{LO}$ to $5f_{LO}$ and a resistive match at frequencies higher than $6f_{LO}$. Thus the optimal circuit found through simulations with the design tool had some features of a 'Z' mixer and some of a 'RM' mixer depending on the frequency considered. Unlike a 'Z' mixer, however, the diode 'ON' time at $C_{L_{min}}$ was nearly 0.50 T_{LO} for all circuits designed. In addition, because the simulated mixer circuits were implemented with discrete elements, the embedding impedances presented to the diode were never ideal short or open-circuits. The benefit of the design tool is that it allows the designer to optimize the performance of circuits with practical components by following the design guidelines established in Chapters 3, 4 and 5.

The chapter begins with a survey of the literature to assess the predicted effect of C_B on mixer performance. The effect of adding a second frequency conversion element, C_B, to the main conversion element, namely the barrier resistance R_B, varies widely depending on the termination provided to all sideband frequencies. This result was seen both theoretically and experimentally. For the most part, improvements in C_L were thought to coincide with a reduction of circuit stability and increase in mixer noise temperature, although experimental evidence did not always concur.

In order to develop a circuit that can take advantage of the addition of a second

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nonlinear element, we return to the ideal switch analogy. This leads to the development of the phasing circuit which in the single-ended mixer implementation is placed between the source and the diode, and, in the balanced mixer is placed on the RF port prior to the transformer tap. This phasing network takes advantage of C_B to store RF energy when the diode is 'OFF', for subsequent storage in the phasing circuit as the diode changes state, and, finally transferred to R_B when the diode is 'ON'. The phasing circuit acts not only to store the RF energy but also to set the timing of the diode's change from 'ON' to 'OFF' state. Graphical output is instrumental in the design and optimization of this network as it allows the diode state (determined by the large-signal waveforms on the diode) to be seen along with the small-signal waveforms. The advantage of using such a circuit to reduce conversion loss is that it should also lead to a reduction in total noise generated by the diode.

Operation with the phasing circuit allowed for the design of single-ended mixers with C_L's of 3.1 dB for $C_{j0} = 0.25$ pF and 4.25 dB for $C_{j0} = 1.0$ pF. This compares favorably with the 4.3 dB C_L for the optimized 'RM' mixer and the 4.25 dB C_L for the optimized 'Z' mixer - both of which used purely resistive diodes. Moreover it compares well with the 3.9 dB C_L limit predicted for purely resistive diodes in broadband mixer circuits with resistive terminates provided to all out-of-band frequencies. It is just above the 3 dB conversion loss limit for purely resistive diodes in broadband mixers with reactive out-of-band frequency terminations. It confirms other experimental and theoretical findings that C_B can be used to reduce conversion loss rather than to degrade it. This can be seen by comparing the results given in Chapter 4 where C_B is treated as a fixed capacitor and inductive matching is used to optimize C_L. There a C_L of 4.6 dB was achieved for $C_{j0} = 0.25$ pF and 5.4 dB for $C_{j0} = 1.0$ pF.

In order to quantize the improvement due to the nonlinearity of C_B as distinct from that due to its placement in the circuit, C_B is set to 0.001 pF and a fixed capacitor, C_F, is placed in parallel with the diode in the circuit optimized for nonlinear C_B with $C_{j0} = 0.25$ pF. Unfortunately this is the only way to easily determined the impact of nonlinear C_B as all analytic methods require assumptions which may not be valid for practical mixer construction. The value of C_F found to give minimum C_L is 0.167 pF. A single-ended mixer with phasing circuit is then optimized with C_F equal to

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0.167 pF and to 0.33 pF, the value of $\langle C_B \rangle$ in the previously optimized circuit for $C_{j0} = 0.25$ pF. Optimized circuits give a conversion loss of 4.1 dB for $C_F = 0.167$ pF and 4.25 dB for $C_F = 0.33$ pF — about 1 dB higher than that achieved with the nonlinear C_B. Both conversion loss values found are comparable to that achieved with the purely resistive diode. Hence no improvement in C_L should be expected by using the phasing circuit with a capacitor in parallel with a purely resistive diode over a simple 'RM' mixer with the same diode.

The balanced mixer, because of the inherent separation of LO and RF circuits, lends itself to the use of a phasing circuit on the RF port and a waveform shaping network on the LO port. The waveform shaping network optimizes the large-signal driving waveform at the diode and hence effects both the conductance and capacitance diode waveforms. Thus the diode's characterictics can be adjusted independently from the RF waveforms, the latter being optimally timed by the phasing circuit. With only the phasing circuit in place, the conversion loss of the optimized balanced circuit is from 2.7 dB to 2.5 dB depending on the bias and LO voltage used, with greater bias producing lower C_L. Diode 'ON' time is 0.50 T_{LO} and 0.53 T_{LO} where the larger 'ON' time is enduced by the greater bias. As with the single-ended mixer these results are far lower than that achieved with a purely resistive diode mixer.

To assess the effect of the nonlinearity of C_B, C_B is set to 0.001 pF and a fixed capacitor C_F is placed, as before, in parallel with the diode in a balanced circuit whose C_L with $C_{j0} = 0.25$ pF had been 2.8 dB. C_F was varied to minimize C_L. C_L was minimized to 5.8 dB when C_F was set to 0.14 pF. Although no further circuit or bias optimization was performed to reduce the 3 dB differential between circuit performance with C_F and C_B, it is obvious that much of the C_L reduction is due to the nonlinearity of C_B and not to the use of a fixed capacitor in that location in the circuit.

When the waveform shaping circuit is added to the LO circuit and adjusted, the balanced mixer conversion loss falls to 2.1 dB and T_{TON} is 0.51 T_{LO} without any changes having been made in the phasing circuit. The conversion loss of the circuit is then 2 dB below the 4.2 dB achieved for the balanced 'RM' mixer with purely resistive diodes.

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Mixer conversion loss results for both the single-ended and balanced mixers are shown in Figure 83. Improvements in C_L beyond the purely resistive diode mixer are 1 - 2 dB for $C_{j0} = 0.25$ pF depending on whether a single-ended or balanced mixer is implemented. At $C_{j0} = 1.0$ pF only the single-ended mixer has been optimized. There use of the phasing circuit succeeds in reducing the C_L degradation from what it would have been had C_B been treated as a fixed capacitor but it does not succeed in reducing the C_L beyond that achieved with a purely resistive diode mixer. If diodes with C_{j0} greater than 1 pF were used, the same results are expected. As C_{j0} increases it becomes harder to get the improvement brought about by the phasing circuit to override the primary effect of degraded C_L performance caused by reduced T_{TON} and loss of RF power delivered to the load. This underlines the important part that is is the tandem operation of the barrier capacitance and resistance that bring us the improvement in conversion loss over a purely resistive mixer. For large C_B we would find ourselves in a situation not so difficult from a parametric downconverter where the diode is back biased so $R_B >> C_B$ and thus little RF current passes through R_B. The Manley-Rowe equations for an ideal parametric downconverter modelled by a nonlinear capacitor alone then hold [10]. The available power gain is equal to the ratio of the output to input frequencies. This places a lower bound on C_L of $\frac{f_{IF}}{f_{RF}}$ or 20 dB.

In this chapter guidelines for the design of the phasing circuit and the waveform shaping network are given. Their effectiveness is demonstrated by looking at the $E_{L_1}(T_1)$ entry in Table 24 which shows increasing energy stored in the phasing circuit component L_1 for transfer to R_B as the diode turns 'ON'.

Lastly the noise temperature results for the single-ended mixer estimated by the frequency analysis mixer program DIODEMX support the belief that lower noise temperature as well as reduced conversion loss may be achievable with stable mixers by parametrically pumping the barrier capacitance. This program predicted that the 'RM' mixer with a purely resistive diode would have a noise temperature of 47K and that the circuits with inductive matching would have noise temperatures of 162K and 348K for C_{j0} was equal to 0.25 pF and 1.0 pF, respectively. The optimized single-ended mixer circuit noise temperature performance, as predicted by DIODEMX and

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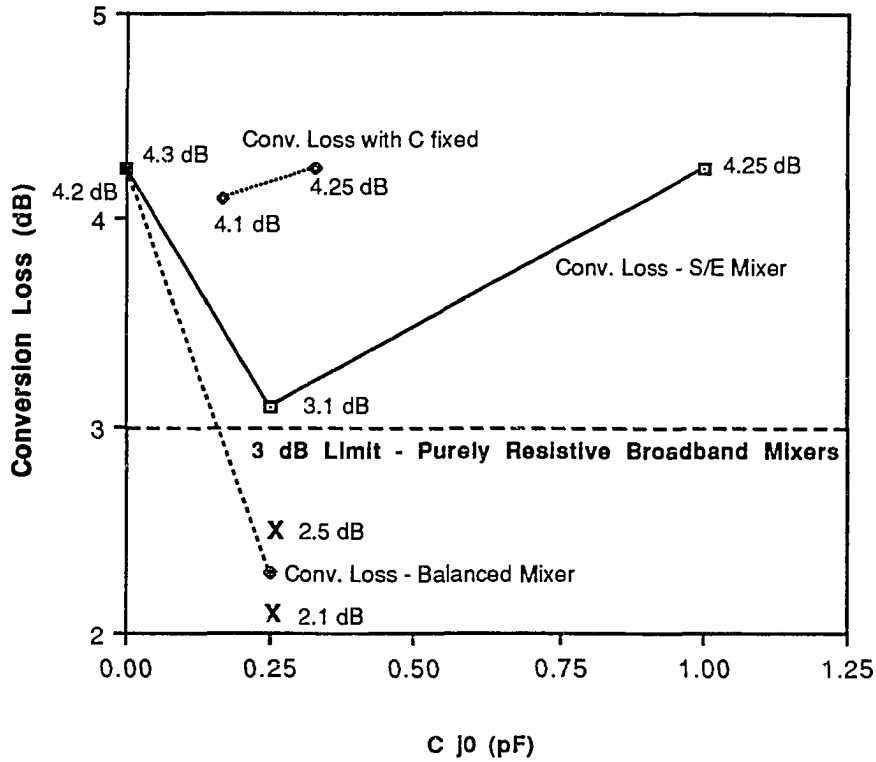


Figure 83: Optimum conversion loss achieved with the design tool.

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discussed in Section 5.4.5, are lower or comparable to those measured when inductive matching is used.

5.8 Areas for Future Mixer Research

This chapter concludes with some suggestions for improving the design tool and with a list of topics for further mixer study. These topics cover areas that are of interest to the design of direct conversion mixers in specific, and, of mixers with diodes having substantial nonlinear resistance and nonlinear capacitance in general. In Chapter 8, other mixer circuits that are good candidates for implementation in the direct conversion receiver are presented.

The power of the design tool could be increased by the addition of several functions. First, the impact on conversion loss due to nonlinear C_B should be assessed more accurately. This task would involve some analytic study and require distinguishing between the charge on C_B due to the RF source or due to the LO source. Then evaluation of the parametric increase in RF due to the pumping of C_B by the LO source would be possible. Second, the design program could also be improved by incorporating Held and Kerr's analysis of mixer noise into the program [29]. This task should not be difficult as the evaluation of mixer noise requires a knowledge of the Fourier coefficients of the diode's conductance and capacitance waveforms, the mixer's embedding impedances, and circuit elements, all of which are already available in the design tool. This feature would be much more valuable if Held and Kerr's noise analysis could be extended to include $1/f$ noise. Last, current optimization of mixer circuits is too laborious and slow. Circuits must be simulated using SPICE and their results analyzed with the design tool prior to submitting another set of circuits for evaluation. This takes a great deal of time which could be reduced if the search process were automated according to the guidelines discussed and if SPICE were running on a faster computer than the presently used VAX 780.

The following topics require further study to ensure that the mixers in Section 5.6 can be successfully used in the direct conversion receiver.

1. Quantitative analysis of the performance degradation due to variations in diode

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parameters within their specified tolerances.

2. Analysis of the effect of diode parasitics on mixer performance.

3. Removal of the matching constraint on the balanced mixer by setting $L_1 \neq L_2$, $k_2 \neq k_3$, $r_{ser_1} \neq r_{ser_1}$. The mixer should be run with D_1 similar to, but not identical to, D_2. In particular the assumption that $k_1 = 1$ allows for perfect isolation of RF to LO on the balanced mixer. It should be replaced by a more realistic value to judge the effects on the phasing and shaping circuit performance.

4. Development of mixer circuits that reduce performance sensitivity to changes in diode parameters, parasitics, and circuit mismatches.

5. Study of the LO drive shaping network to see if further optimization is possible. This may be more feasible if a better assessment of the parametric pumping of C_B is made.

6. Evaluation of the two-tone performance of the mixer to determine its dynamic range.

Once the results of this study are known and the mixer circuit has been designed to minimize the impact on performance due to variations in the diodes, parasitics, or circuit element values, then a direct conversion mixer should be built. If the mixer's frequency of operation is chosen to be in the low UHF range, then it should be possible to measure its waveforms directly on an oscilloscope for comparison with the SPICE predicted signals.

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Chapter 6

Low Noise Amplifier Design

6.1 Introduction

This chapter discusses the design of a low noise amplifier stage for the direct conversion receiver. As delineated in Chapter 2, this amplifier should have a bandwidth nominally spanning DC to half the bandwidth of the RF signal being received. The low frequency cut-off point of the filter will actually be determined by the bandwidth of the DC notch filter required to minimize the $1/f$ noise contribution to the noise in the signal band. As this work considers reception of an ACSB signal of 3.1 KHz bandwidth, the amplifier bandwidth would in this case span from near DC to 1.55 KHz. The amplifier's prime design constraint is that it possess a low noise temperature within its band when driven by the output impedance of the direct conversion mixer. As the mixer's performance has been optimized for an output impedance $\leq$ 2 KΩ, the source impedances under consideration for the direct conversion amplifier must lie near this value. If low noise performance cannot be achieved with such an impedance, then the circuits for both mixer and amplifier will need to be redesigned. The low noise design of the amplifier must take into account then the impedance from which it is being driven, the low frequency range of its operation, and the desire to operate into a high output impedance (10's $K\Omega$) for operation with the active filter. In addition the amplifier must possess acceptable gain to mask the subsequent noise contribution of the active filter.

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The objective of this work is therefore twofold: to identify the proper structure for the amplifier stage (and thereby determine if the mixer design must be reiterated for low noise operation with a higher load impedance), and, to quantify the implications of choice of DC notch filter bandwidth on amplifier design and, hence, on in band amplifier noise temperature.

The first goal requires some elaboration as it is the main objective of this work. To avoid custom design, it would be simplest to use an op-amp for the amplifier stage. However this choice would result in an amplifier with an overly high noise figure as even op-amps designed for low noise operation possess low noise temperatures only when driven by source impedances greater than $10K\Omega$, and, when operated at frequencies higher than 100 Hz – characteristics unlike those called for in this application. To understand if the op-amp's noise performance vs. frequency and optimum source impedance could be matched for this application by adjusting the devices' bias points or a particular circuit element, transistor noise mechanisms are identified and the impact of circuit on amplifier noise temperature is ascertained. In this way, the mechanisms setting the optimum source impedance for minimizing noise temperature, $R_{N_{opt}}$, as well as the frequency dependence of $R_{N_{opt}}$ can be understood and methods for optimizing the op-amp's performance can be found. If, on the other hand, it is necessary to design a specific amplifier stage for the direct conversion receiver, then this work will set the foundation for its choice.

Section 6.2 gives the noise performance of two typical op-amps, the Analog Devices OP-07 and OP-27, as a function of the source impedance used to drive them. In this manner, the degradation in noise figure due to source impedance variation is quantified. In Section 6.3 the performance of the differential amplifier is given and the rationale for choosing it as the building block for the direct conversion amplifier is explained. Section 6.4 details the performance of the proposed direct conversion amplifier stage.

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6.2 Op-Amp Noise Performance

The noise model for an amplifier consists of a current noise source, $\overline{i_i^2}$, across the input and a voltage noise source, $\overline{v_i^2}$, in series with the input to an ideal noiseless amplifier. $\overline{i_i^2}$ and $\overline{v_i^2}$ are defined as a function of frequency. The noise temperature of the amplifier, F_{amp}, is then defined at that frequency as:

$$F_{amp} = 1 + \frac{\overline{v_i^2}}{4kTR_s\Delta f} + \frac{\overline{i_i^2}R_s}{4kT\Delta f}. \tag{66}$$

The optimum R_s for minimum noise temperature, $R_{N_{opt}}$, can be found at the corresponding frequency to be:

$$R_{N_{opt}} = \sqrt{\frac{\overline{v_i^2}}{\overline{i_i^2}}}. \tag{67}$$

An idea of the importance of R_S in setting op-amp noise figure may be obtained by using Eqn. 66 to calculate op-amp noise figure given device noise data $\overline{i_i^2}$ and $\overline{v_i^2}$. The noise performance of the two op-amps, the Analog Devices OP-07 and OP-27, are calculated in this manner. The OP-07 is an ultra-low offset voltage op-amp; the OP-27 is an ultra-low noise precision op-amp. Values for $\overline{i_i^2}$ and $\overline{v_i^2}$ for each device are given in Appendix B.1. The resultant noise figure is plotted in Fig. 84 for operation at 10 Hz and 1 KHz. The noise values plotted correspond to the minimum op-amp noise figure attainable as no feedback around the amplifier is assumed and hence no noise contribution due to the crosscorrelation of $\overline{i_i^2}$ and $\overline{v_i^2}$ has been included in Eqn. 66. Actual op-amps would therefore have slightly higher noise figures. At large R_s, $\overline{v_i^2}$ is the dominant noise source; at low R_s, $\overline{i_i^2}$ dominates. Both op-amps nose figures decrease as frequency increases displaying the effect of $1/f$ noise; the difference between the op-amps' performance is most dramatic for low R_S.

The degradation in noise figure with non-optimum source impedance may be quantized for both op-amps by considering the op-amp noise figure at $R_{N_{opt}}$ and at a source resistor similar to that used with the direct conversion mixer. $R_{N_{opt}}$ is computed from the $\overline{i_i^2}$ and $\overline{v_i^2}$ values given for both devices in Appendix B.1 using eqn. 67. NF_{opt}

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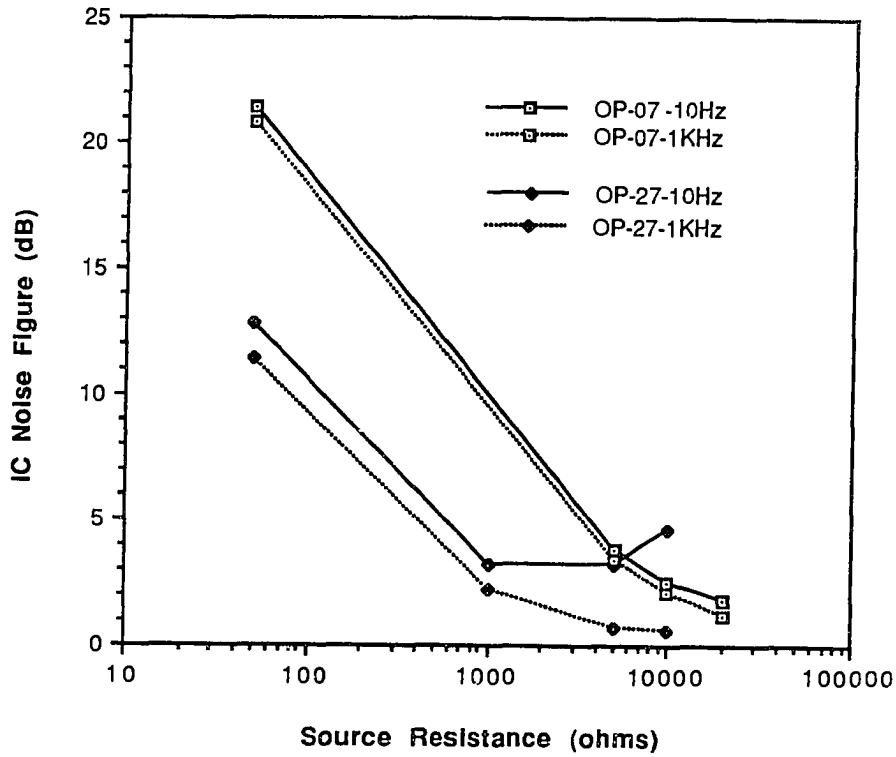


Figure 84: Best case noise figure of the Analog Devices OP-07 and OP-27.

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Table 27: Op-Amp Noise Temperature Degradation with R_S

	OP-07		OP-27	
	NF@$R_{N_{opt}}$	NF@$R_S = 5K$	NF@$R_{N_{opt}}$	NF@$R_S = 5K$
10 Hz	1.6 dB	3.8 dB	2.6 dB	3.2 dB
1 KHz	0.6 dB	3.4 dB	0.6 dB	0.7 dB

is then calculated from eqn. 66. Accordingly $R_{N_{opt}}$ has been calculated for the OP-07 to be 30K at 10Hz and 75K at 1KHz with corresponding noise figures of 1.6dB and 0.6dB, respectively. The OP-27 possesses a $R_{N_{opt}}$ of 2.2K at 10 Hz and 8K at 1KHz with corresponding noise figures of 2.6dB and 0.6dB. The OP-27's noise figure is comparable to that of the OP-07 at 1 KHz and, favorable for this application, utilizes a lower source impedance to achieve minimum noise figure: 8K rather than 75K. However at 10 Hz, the optimum noise figure for the OP-27 is higher than that of the OP-07 although again it requires a lower $R_{N_{opt}}$. Note that $R_{N_{opt}}$ increases as frequency increases due to decreasing $1/f$ noise in $\overline{i_i^2}$.

For comparison with these minimum achievable noise figures, op-amp performance at $R_S = 5$K is taken from Fig. 84 and compared in Table 27 with that obtained when when $R_S = R_{N_{opt}}$. For operation with a R_S of 5K, OP-27 will clearly produce the lowest noise figure at 1 KHz; however the OP-27 is only slightly better than the OP-07 at 10 Hz. The op-amp appropriate for this application clearly depends on the frequency of operation (and hence on the bandwidth of the DC notch filter) and on the source impedance used.

The noise mechanisms that set amplifier performance have been examined in Appendix B to understand the impact of frequency and source resistance on amplifier noise figure, and, to understand if better noise figures are possible for low R_S and low frequencies of operation by correctly choosing the appropriate device and by optimizing its bias and circuit conditions.

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6.3 Differential Amplifier Performance

The differential amplifier has been chosen as the basic building block for the low frequency amplifier. It is composed of two transistors in a common-emitter configuration. The common-emitter configuration has been shown in Appendix B to be the best suited for the direct conversion receiver application due to its performance when driven from a low source impedance and operated into a high load impedance. Three configurations were examined: the common-emitter, the common-base, and the common-collector; all were analyzed for use with a silicon bipolar transistor. The transistor parameters used were modelled after those of the National Semiconductor LM384 superbeta monolithic matched transistor pair. The device model is known as XM_1; its hybrid-π model is given in Appendix B.3. In the appendix, the noise mechanisms that set amplifier noise figure at a given bias and frequency are identified for all three transistor configurations. In addition differential amplifiers have several features that are of interest in this application, the principal one being high common-mode rejection ratio, or, rejection of identical signals appearing at both input ports. This allows the amplifier to be less succeptible to performance changes due to thermal drifts and thus makes their use for low frequency amplifiers desirable [33]. Finally, differential amplifiers are commonly used as input stages for op-amps. Hence analysis of the differential input will permit the understanding of the noise mechanisms that set the op-amp noise temperature and $R_{N_{opt}}$.

A typical three stage low frequency amplifier is shown in Figure 85. The differential amplifier gain stage is outlined. Transistors Q_1 and Q_2 are biased by a transistor current source, created by Q_3 and Q_4. Transistor current sources are more commonly used for op-amp biasing than emitter resistors as they provide increased circuit performance insensitivity to temperature and power supply variations and require less space to realize [25].

The voltage noise source at the input of the differential amplifier, $\overline{v_{N_{in}}^2}$, can be written as:

$$\overline{v_{N_{in}}^2} = \left[\overline{v_{R_S}^2} + \overline{v_{b_1}^2} + (R_S + r_b + R_{E_1})^2 \cdot \overline{i_{b_1}^2}\right.$$

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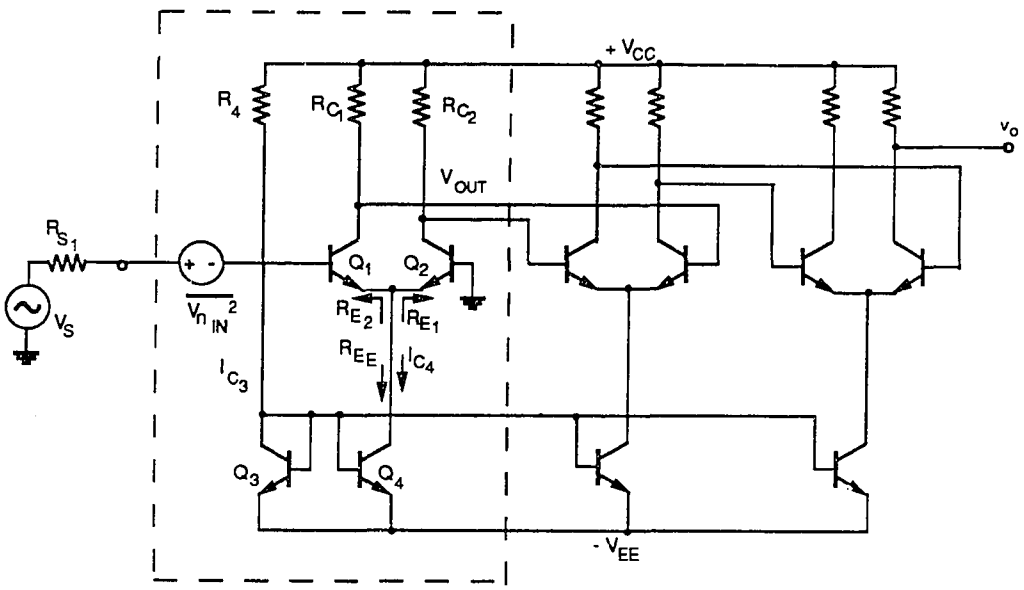


Figure 85: Low frequency amplifier implemented by a cascade of three differential amplifiers. The outlined input differential pair with transistor current source is fundamental gain block studied.

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$$+\left(\frac{R_S+r_b+r_\pi+R_{E_1}}{\beta_o}\right)^2\cdot\overline{i_{c_1}^2}$$
$$+\left(\frac{R_S+r_b+r_\pi+R'_{E_1}(\beta_o+1)}{\beta_o}\right)^2\cdot\overline{i_{R_c}^2}\Bigg]\cdot$$
$$\left(\frac{2r_\pi}{2r_\pi+R_S}\right)$$
$$+\overline{v_{b_2}^2}+(r_b+R_{E_2})^2\cdot\overline{i_{b_2}^2}$$
$$+\left(\frac{r_b+r_\pi+R_{E_2}}{\beta_o}\right)^2\cdot\overline{i_{c_2}^2}$$
$$+\left(\frac{r_b+r_\pi+R'_{E_2}(\beta_o+1)}{\beta_o}\right)^2\cdot\overline{i_{R_c}^2} \qquad (68)$$

where

$$R'_{E_1} = \left(\frac{r_{b_2}+r_{\pi_2}}{\beta_2+1}\right) \parallel R_{EE},$$
$$R'_{E_2} = \left(\frac{R_S+r_{b_1}+r_{\pi_1}}{\beta_1+1}\right) \parallel R_{EE},$$
$$R_{EE} = r_{out_4} = \frac{V_A}{I_{c_4}}.$$

The noise generators, $\overline{v_b^2}$, $\overline{i_b^2}$, $\overline{i_c^2}$, $\overline{v_{R_s}^2}$ and $\overline{i_{R_c}^2}$, are defined by eqns. 85, 86, 87, 88 and 89, respectively in Appendix B.

These equations along with the results obtained in Appendix B from the analysis of the three transistor configurations stress the importance of choosing a device with a low series resistance, r_b, and a high β to minimize $\overline{v_{N_{in}}^2}$. The circuit's performance can be studied when different types of silicon bipolar transistor are used. Of the three types of transistor models described in Appendix B – XM_1, XM_2, and XM_3 – transistor models XM_2 and XM_3 have been used to assess the performance of the differential pair with a current source.[1] Specifically, its performance has been studied

[1]Transistor model XM_2 is based on a small n-p-n transistor used in the input stage of Intersil, Inc.'s op-amp, ICL 8741 [77]. Transistor model XM_3 is a fictitious device having a current gain equal to that of device XM_1, a National Semiconductor LM394 superbeta monolithic matched transistor pair, and a base resistance composed of two elements: a constant resistor equal to 100Ω and a resistor

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for the case where transistors Q_1 - Q_4 are all of the same type, either transistor model XM_2 or XM_3, or where Q_1 and Q_2 are of the low noise type, XM_3, and the current source transistors Q_3 and Q_4 are general purpose transistors, XM_2. To access the lowest noise temperature possible with a differential input, Q_1 and Q_2 were selected to be XM_3 type devices and the active current source was replaced by a large resistor.

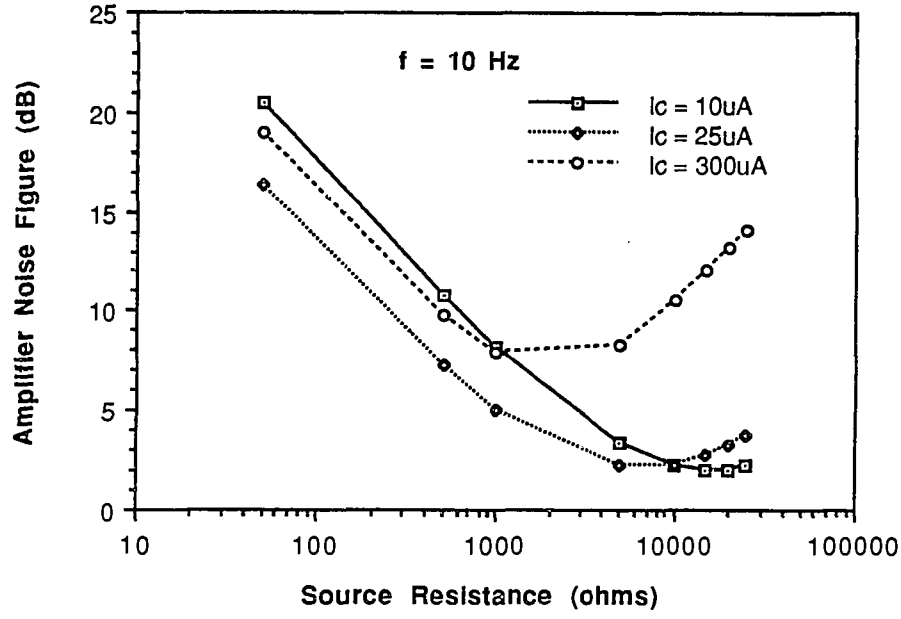
The results presented here assume the use of device model XM_3 for transistors Q_1 - Q_4. Using this device in the outlined circuit shown in Fig. 85, the noise figures shown in Figure 86 are obtained; Fig. 86(a) gives the performance of the differential amplifier at 10 Hz as R_S is varied for collector currents in Q_1 set to 10μA, 25μA, and 300μA, Fig. 86(b) charts performance as a function of R_S and I_C at 1 KHz. The frequency dependance of $I_{C_{opt}}$ and $R_{N_{opt}}$ for minimum noise figure is apparent from Fig. 86. At 10 Hz, NF_{min} is 2.0 dB with $R_{N_{opt}}$ between 15 K and 20 K and a $I_{C_{opt}}$ of 10 μA. At 1 KHz, NF_{min} is 0.4 dB with $R_{N_{opt}}$ between 20 K and 25 K and a $I_{C_{opt}}$ of 25 μA.

The transistor model parameters and differential amplifier analysis can be verified by comparing the results predicted from this work with those measured on op-amps. The results should be roughly equivalent as the op-amp performance will be largely determined by the performance of the input differential stage. As op-amps are typically biased at a I_C of 5 μA to provide high input impedance and low input DC currents, the differential amplifier input stage can be analyzed with Q_1 and Q_2 biased at this current. If Q_1 - Q_4 are modelled by transistor model XM_3, their noise figure performance is found to be roughly equivalent to that of the OP-07; if Q_1 - Q_4 are modelled by XM_2, then the resultant input stage has a similar noise performance as an OP-27.

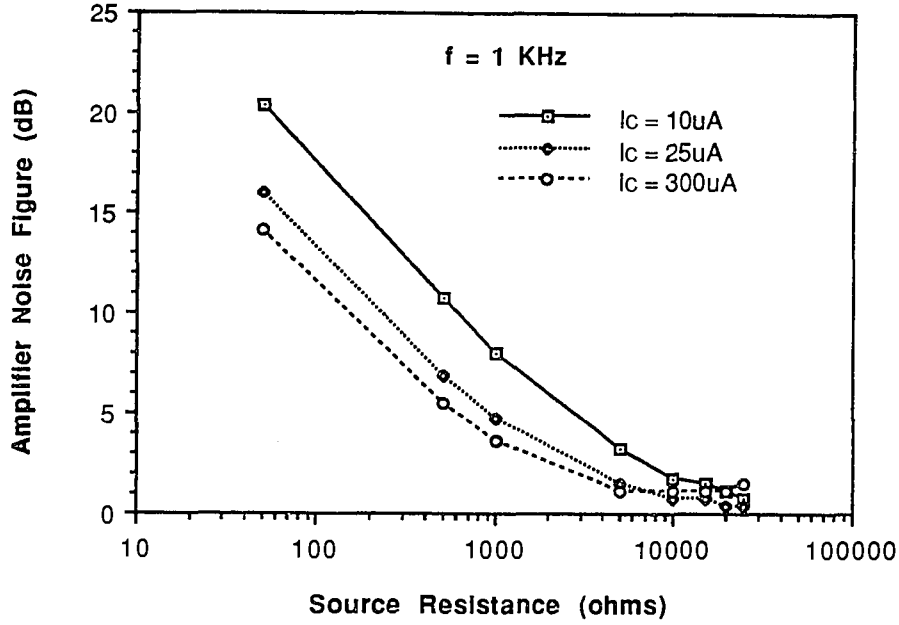
There are several benefits to analyzing the noise performance of the differential stage: first, the mechanisms causing a particular noise performance can be identified; second, particular noise contributions can be minimized to the degree that the appropriate transistor can be found for the application; and third, the transistor bias, or I_C, can be adjusted in order to minimize noise temperature performance at a particular

whose resistance varies with I_C. Both devices have the $1/f$ noise characteristics of the LM394. XM_2 is meant to simulate a general purpose op-amp transistor and XM_3 to simulate a high performance op-amp transistor.

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(a) Performance at 10 Hz



(b) Performance at 1 KHz

Figure 86: Noise figure vs. R_S performance for the differential amplifier shown above.

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R_S or at a particular frequency. Control over this parameter allows the differential stage to be operated at a lower R_S than may be intended when it is used as an input stage for a standard op-amp. Specifically, one can see from Fig. 86 that transistors Q_1 and Q_2 can be operated at a higher bias to reduce the noise figure degradation arising from the use of $R_S \ll R_{N_{opt}}$. For example, at 10 Hz NF is 2.25 dB when a R_S of 5K is used with an I_C of 25 μA (only 0.25dB higher than NF_{min}), or, at 1 KHz NF is 1.0 dB when a R_S of 5K is used with an I_C of 25 μA (0.6dB higher).

6.4 Direct Conversion Amplifier

We propose the use of the differential stage shown in Fig. 85 as the primary building block of the direct conversion amplifier. This input stage can be analyzed according to the previous section treatment when driven by source impedances corresponding to those of the direct conversion mixers whose design is listed in Table 26. Correspondingly, the differential amplifier is analyzed for R_S equal to 500 Ω, 1.5 K and 2.0 K, the optimum load impedances for the two single-ended mixers and the balanced mixer. The required I_C for optimum noise figure are tabulated in Table 28 along with the noise temperature results, the voltage gain G_{amp} of each stage, and the amplifier's output impedance. In the final column the noise figure achieved with the gain stage is compared with NF_{min} (at $R_{N_{opt}}$) given in the previous section.

The large difference in optimum I_C for minimum noise figure is visible as the frequency of operation is varied. $I_{c_{opt}}$ is 25 μA at 10Hz and 0.3 μA at 1KHz. This aids in the determination of the bandwidth of the notch filter. If the notch filter is to be very narrow to minimize signal distortion, eg. 0 - 10 Hz, then the differential amplifier would have to be biased at low currents $\approx$ 25 μA. However if a filter from 0 - 100 Hz can be tolerated then the appropriate bias current to minimize noise would probably be $\approx$ 100 μA. Minimizing current is necessary to conserve power and maintain good performance stability over temperature and power supply fluctuations. The dependance of optimum bias and minimum noise figure on R_S is also illustrated in Table 28. At any of the frequencies the following two trends are observed: (1) the current required to minimize NF_{amp}, $I_{C_{opt}}$, decreases as R_S increases; and (2) NF_{amp}

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Table 28: Gain and Noise Performance of the Gain Stage

R_S	$I_{C_{opt}}$	NF_{amp} @$I_{C_{opt}}$	G_{amp}	R_{out}	NF_{amp} - NF_{min}
f = 10 Hz:					
500 Ω	25 μA	7.2	-50	52K	5.2 dB
1.5 KΩ	25 μA	4.0	-50	52K	2.0 dB
2.0 KΩ	25 μA	3.4	-50	52K	1.4 dB
f = 100 Hz:					
500 Ω	300 μA	5.9	-600	50K	
1.5 KΩ	300 μA	3.2	-600	50K	
2.0 KΩ	100 μA	2.8	-200	51K	
f = 1 KHz:					
500 Ω	1 mA	5.3	-2000	46K	4.9 dB
1.5 KΩ	300 μA	2.8	-600	50K	2.4 dB
2.0 KΩ	300 μA	2.3	-600	50K	1.9 dB

at $I_{C_{opt}}$ decreases as R_S increases.

As the balanced mixer has the best conversion loss, the highest impedance transformation ratio, and, results in the lowest amplifier noise temperature in addition to possessing the benefits inherent in balanced structures, it is chosen as the prototypical direct conversion mixer over the single-ended mixer. The source impedance of the direct conversion amplifier is then 2KΩ. Table 29 gives the performance of the proposed direct conversion stage optimized for use with two types of DC notch filter. For operation with a notch filter from 0 - 10 Hz, the input transistors of the amplifier stage will be biased at 25μA; for operation with notch filters from 0 - 100 Hz, the input transistors of the amplifier stage will be biased at 100μA. The differential mode gain obtained at all frequencies when I_C is equal to 25 μA is -50; the power gain is 24 or 13.8 dB; R_{out} is 52 KΩ. When I_C is equal to 100 μA the differential mode gain is -200, the power gain is 370 or 25.7 dB, and, R_{out} is 51 KΩ. In the last two columns, the noise figure of the amplifier is compared against that achieved at $I_{C_{opt}}$ and against the minimum noise figure, NF_{min}, earlier at 10 Hz and 1 KHz.

The performance of the amplifier stage is thought to be adequate for the direct

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Table 29: Noise Figure of the Gain Block for Operation with Direct Conversion Mixer with Two Types of Notch Filters

Frequency	0 - 10 Hz Notch Filter ($I_C = 25\ \mu$A)			
	NF_{amp}	F_{amp}	NF_{amp} - $NF_{@Ic_{opt}}$	NF_{amp} - NF_{min}
10 Hz	3.4 dB	340 K	0 dB	1.4 dB
100 Hz	3.0 dB	290 K	0.2 dB	
1 KHz	3.0 dB	290 K	0.7 dB	2.6 dB
Frequency	0 - 100 Hz Notch Filter ($I_C = 100\ \mu$A)			
	NF_{amp}	F_{amp}	NF_{amp} - $NF_{@Ic_{opt}}$	NF_{amp} - NF_{min}
10 Hz *	5.5 dB	770 K	2.1 dB	3.5 dB
100 Hz	2.8 dB	270 K	0 dB	
1 KHz	2.5 dB	240 K	0.25 dB	2.1 dB

* The performance at 10Hz is listed for completeness as the notch filter will remove this frequency component from the input of the differential stage.

conversion receiver and hence no further optimization of the direct conversion mixer is necessary. However if further reduction in noise figure were necessary, the current source can be replaced by an emitter resistor, although this will negatively impact the amplifier's performance over temperature.

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Chapter 7

Active Filter Design

7.1 Introduction

A multiple loop feedback filter was chosen as the basis for the active filter; it is depicted in Figure 87. The filter has been analyzed for gain, noise, and, selectivity. Fig. 87(a) shows the design of one op-amp stage. Fig. 87(b) gives the block diagram of the three filter cascade. The op-amp was assumed to be a 741 type op-amp; noise source values for $\overline{v_i^2}$ and $\overline{i_i^2}$ typical of this op-amp were used to calculate the noise performance of the overall filter. The gain of each stage was set to 10 dB in order that the out-of-band or interfering signal power could be reduced prior to saturating any of the stages. All filter stages are assumed to be identical to improve the modularity of the receiver design. Consequently the overall in-band gain shape possesses some roll-off with frequency.

Section 7.2 describes the analysis of the filter for gain and noise and the program designed to calculate filter performance. Based on this analysis, the feedback components of the filter stage are chosen to minimize the filter's noise performance when matched into the output impedance of the gain stage. In Section 7.3 the filter chosen for implementation in the direct conversion receiver is specified and its noise temperature and gain performance are given.

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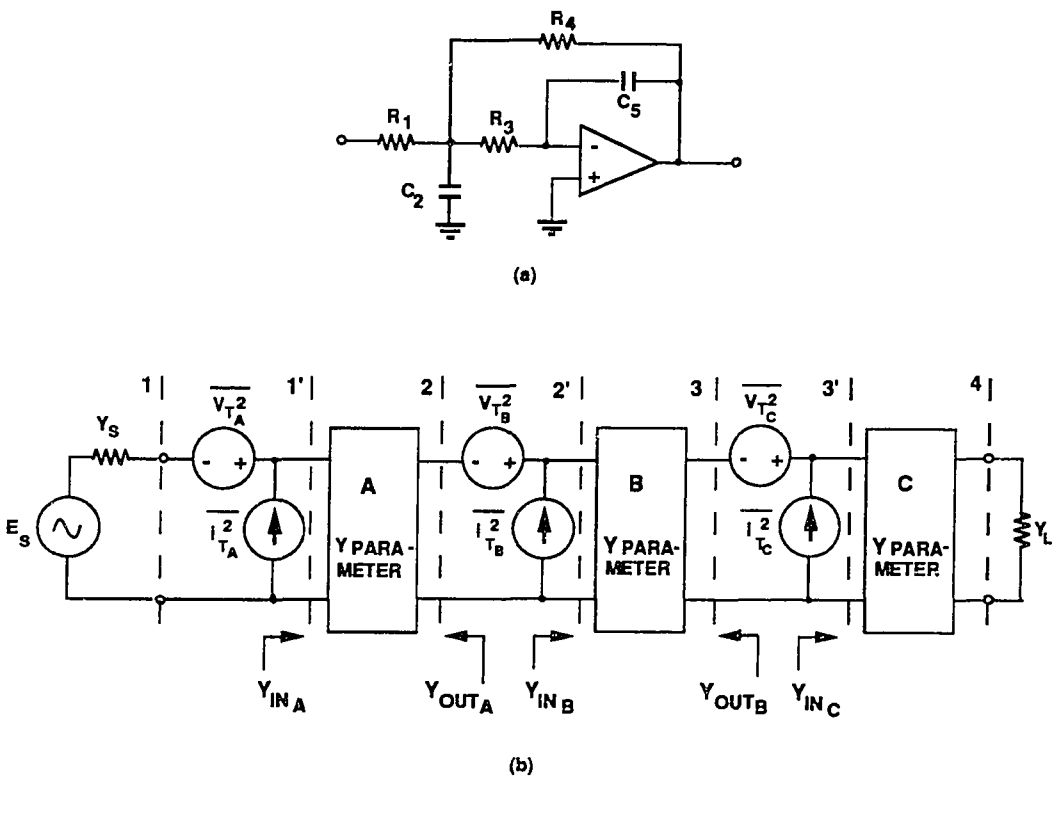


Figure 87: Active filter block diagram: (a) the multiple loop feedback filter stage; (b) the three stage filter cascade.

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7.2 Filter Analysis

The filter stage is specified in terms of its gain in order to find the value of the feedback components. The Y-parameters and the equivalent input noise source characteristics of the filter stage are then computed.[1] The characteristics of the three stage filter are derived by cascading each filter stage two-port. The analysis is carried out by the program *syst.for* whose listing is given in Appendix C. A simple program flowchart is given in Fig. 88. The program calculates filter selectivity by considering the filter's action on three signals in adjacent channels: the wanted signal and two 'interferers' that occupy, at the received RF band, the two RF channels either higher or lower than the wanted signal.

The most interesting features of the program are the method by which signal and noise power is divided into power per frequency bin, the computation of the feedback elements required to achieve a desired filter gain, the calculation of filter Y-parameters, and, lastly, the calculation of the equivalent input filter noise source given the noise characteristics of the op-amp and the filter component noise generators. Once the performance of the filter stage, or 2-port, is specified in terms of its equivalent input noise source and its Y-parameters, the overall filter performance can be easily computed by applying the relationships appropriate to a cascade of identical two ports. The signal and noise voltages can then be tabulated as a function of frequency at each node. Parameters such as signal power in the wanted frequency band (or channel), noise power in the same channel, signal power in adjacent channels, and total noise power over several channel bandwidths can then be found. These parameters allow one to compute the signal-to-noise ratio within the wanted channel and signal-to-noise over the filter bandwidth at each filter node. In this manner, the noise temperature and gain profile of the filter as a function of frequency can be obtained and used to calculate the overall performance of the front-end components of the proposed direct conversion receiver.

The salient features of the filter analysis program and the subroutines that accomplish them will now be described. Division of the input spectrum to the filter

[1]The Y matrix relates the input and output filter stage voltages to the input and output currents.

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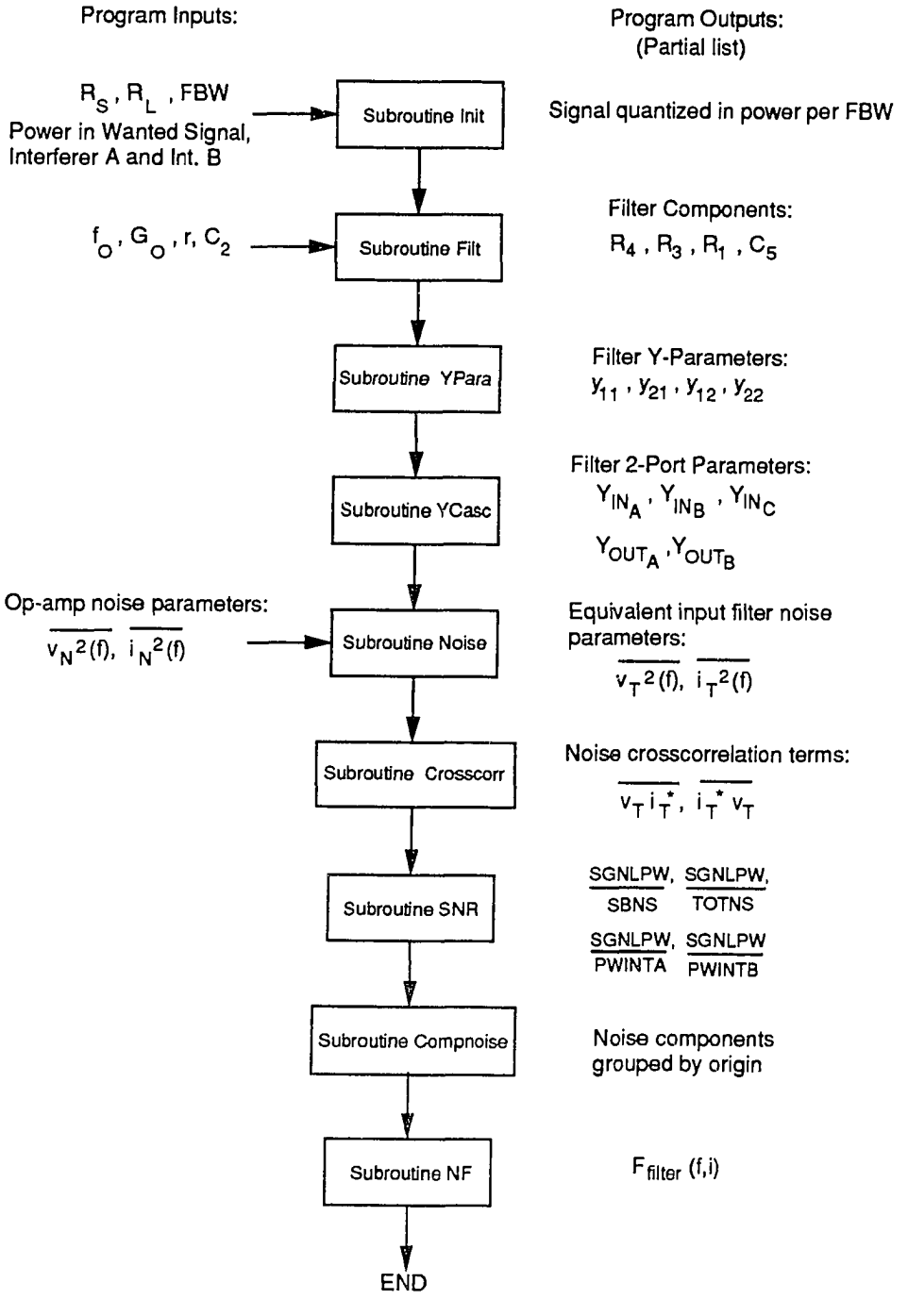


Figure 88: Block diagram of the multiple loop feedback filter program.

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into wanted signal and interferers and calculation of noise power is accomplished by subroutine INIT. The wanted signal, W_S, is taken to extend from FMARK(1) to FMARK(2). The adjacent channel signal, Interferer A or I_A, spans from FMARK(3) to FMARK(4) and the subsequent channel signal, Interferer B or I_B, spans from FMARK(5) to FMARK(6). Filter selectivity is measured by examining the ratio of signal power in the wanted channel to signal power in one of the adjacent channels as all signals pass each stage of the filter. To simulate the reception of ACSB signals with the direct conversion receiver, the RF channel bandwidth of each signal is specified as 3.1 KHz and the guard band between channels is taken to be 900 Hz. The baseband signals therefore span from DC to 1.55 KHz for the wanted signal W_S, from 2.45 KHz to 5.55 KHz for I_A, and from 6.45 KHz to 9.55 KHz for I_B. The power in each channel is entered into this subroutine along with the filter source and load impedance, R_S and R_L, and the highest frequency at which noise calculations are to be made, f_{max} (f_{max} is typically 10 KHz). For this analysis the power of each signal was assumed to be 1nW in a bandwidth of 3.1 KHz (corresponding to 2nW for the wanted signal at baseband whose bandwidth is now 1.55 KHz). The spectrum from DC to f_{max} is then divided into frequency bins of bandwidth FBW (FBW is typically equal to 50 Hz). The signal power in each of the three channels is then converted into a power per FBW Hz. Dividing the spectrum of interest into frequency bins allows us to easily calculate the noise power per frequency bin and hence find the filter noise temperature vs. frequency accurately. Once the signal power/bin and noise power/bin are known the signal-to-noise in each frequency bin can be calculated in a straightforward manner.

The filter component values, R_1, R_3, R_4, and C_5, are calculated for the multiple loop feedback filter stage depicted in Fig. 87(a) given the required gain, G_0, the cut-off frequency f_0 (or angular frequency ω_0), and a value for C_2. This is accomplished by subroutine FILT. First the filter's r_{max} is computed:

$$r_{max} = \frac{1}{2(1+g)}$$

where g is the numeric value of the power gain, ie. $g = 10^{\frac{G_0}{20}}$. A value for r, r less

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than r_{max}, is used to calculate two possible pairs of R_4 and R_3:

$$R_{41} = \left(\frac{1 + \sqrt{1 - r \cdot r_{max}}}{\sqrt{2}\omega_0 C_2 r} \right)$$

and

$$R_{31} = \frac{1}{\omega_0^2 C_2^2 r R_{41}};$$

or,

$$R_{42} = \left(\frac{1 - \sqrt{1 - r \cdot r_{max}}}{\sqrt{2}\omega_0 C_2 r} \right)$$

and

$$R_{32} = \frac{1}{\omega_0^2 C_2^2 r R_{42}}.$$

The R_4,R_3 pair with the smallest difference $\mid R_4 - R_3 \mid$ is chosen to implement the filter. C_5 and R_1 are then calculated according to:

$$C_5 = r C_2,$$

and,

$$R_1 = \frac{R_4}{g}.$$

Subroutine YPARA calculates the Y-parameters of the filter stage given the filter components:

$$\begin{aligned} Y_1 &= \frac{1}{R_1} \\ Y_2 &= j\omega C_2 \\ Y_3 &= \frac{1}{R_3} \\ Y_4 &= \frac{1}{R_4} \\ Y_5 &= j\omega C_5; \end{aligned}$$

and the op-amp Y-parameters:

$$Y_{op-amp} = \begin{bmatrix} y_{11_O} & y_{21_O} \\ y_{12_O} & y_{22_O} \end{bmatrix} = \begin{bmatrix} \frac{1}{r_{in}} & 0 \\ \frac{AOL}{r_o} & \frac{1}{r_o} \end{bmatrix},$$

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where $r_{in} = 2$ MΩ, $r_o = 75$ Ω and the open loop voltage gain, AOL, is 200,000. These three parameter values are typical of the 741 op-amp [26].

The Y-parameters for the filter stage are given as follows:

$$\begin{aligned}
y_{11_T} &= \frac{(Y_2 + Y_3 + Y_4)Y_1Y - Y_3^2Y_1}{D} \\
y_{12_T} &= \frac{-Y_1(Y_4Y + Y_5Y_3)}{D} \\
y_{21_T} &= \frac{Y_3Y_1(y_{21_O} - Y_5) - Y_4Y_1Y}{D} \\
y_{22_T} &= [\,(\,[Y_1 + Y_2 + Y_3 + Y_4]\,Y_5 + Y_3Y_4)\,(y_{21_a} - Y_5) \\
&\quad + \left([Y_1 + Y_2 + Y_3 + Y_4]\,Y - Y_3^2\right)X \\
&\quad - Y_4^2Y - Y_4Y_5Y_3\,] \times \frac{1}{D}
\end{aligned}$$

where $D = (Y_1 + Y_2 + Y_3 + Y_4)Y - Y_3^2$;

$Y = y_{11_O} + Y_3 + Y_5$;

and, $X = y_{22_O} + Y_4 + Y_5$.

Subroutine YCASC calculates the input and output impedance of each filter element as follows:

$$\begin{aligned}
Y_{OUT_A} &= y_{22_T} - \frac{y_{21_T}\,y_{12_T}}{y_{11_T} + Y_L} \\
Y_{OUT_B} &= y_{22_T} - \frac{y_{21_T}\,y_{12_T}}{y_{11_T} + Y_{OUT_A}} \\
Y_{IN_C} &= y_{11_T} - \frac{y_{21_T}\,y_{12_T}}{y_{22_T} + Y_L} \\
Y_{IN_B} &= y_{11_T} - \frac{y_{21_T}\,y_{12_T}}{y_{22_T} + Y_{IN_C}} \\
Y_{IN_A} &= y_{11_T} - \frac{y_{21_T}\,y_{12_T}}{y_{22_T} + Y_{IN_B}}.
\end{aligned}$$

The reference plane for these impedances is shown in Fig. 87(b).

Subroutine NOISE calculates the noise voltage and currents, $\overline{v_n^2}$ and $\overline{i_n^2}$, in each frequency bin, FBW, by integrating the voltage and current noise sources, $\overline{v_i^2}$ and $\overline{i_i^2}$,

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listed in Appendix B.1 for the 741 op-amp over the specific frequency range corresponding to that frequency bin. Whereas $\overline{v_i^2}$ and $\overline{i_i^2}$ are specified in V^2/Hz and A^2/Hz, respectively, $\overline{v_n^2}$ and $\overline{i_n^2}$ are then given in V^2 and A^2, respectively. Noise is generated in the filter stage from the op-amp noise generators and from thermal noise in the resistive components. These noise sources can be referred to the input and replaced by a voltage and current noise source, $\overline{v_T^2}$ and $\overline{i_T^2}$. These noise sources are correlated as they are weighted sums of common noise sources. $\overline{v_T^2}$ and $\overline{i_T^2}$ can be written as:

$$\begin{aligned}
\overline{v_T^2} &= 4kT\,\Delta f\left[R_1\left(1+\frac{R_1}{R_4}\right)+R_3\left(1+\frac{R_1}{R_4}\right)^2+R_3(\omega C_2R_1)^2\right] \\
&\quad +\overline{i_n^2}\left[\left(R_1+R_3\left(1+\frac{R_1}{R_4}\right)\right)^2+\omega^2(C_2R_1R_3)^2\right] \\
&\quad +\overline{v_n^2}\left[\left(1+\frac{R_1}{R_4}+\omega^2R_1R_3C_2C_5\right)^2+\omega^2\left(C_2R_1-C_5\left(R_1+R_3\left(1+\frac{R_1}{R_4}\right)\right)\right)^2\right]; \\
\overline{i_T^2} &= 4kT\,\Delta f\left[\frac{1}{R_4}\left(1+\frac{R_3}{R_4}\right)+R_3(\omega C_2)^2\right] \\
&\quad +\overline{i_n^2}\left[\left(1+\frac{R_3}{R_4}\right)^2+\omega^2C_2^2R_3^2\right] \\
&\quad +\overline{v_n^2}\left[\left(\frac{1}{R_4}+\omega^2R_3C_2C_5\right)^2+\omega^2\left(C_2-C_5\left(1+\frac{R_3}{R_4}\right)\right)^2\right].
\end{aligned}$$

The correlation between the two noise sources is computed by subroutine CROSSCORR. In order to compute the total noise voltage at the output of each filter stage, ie. $\overline{v_{n_{A_{OC}}}^2}$ for filter stage A, it is necessary to find $\overline{v_{T_A}}\,\overline{i_{T_A}^*}$ and $\overline{v_{T_A}^*}\,\overline{i_{T_A}}$. $\overline{v_{n_{A_{OC}}}^2}$ is given by:

$$\overline{v_{n_{A_{OC}}}^2}=\frac{\overline{i_{T_A}^2}}{|\,Y_S\,|^2}+\overline{v_{T_A}^2}+\frac{\overline{i_{T_A}}}{Y_S}\overline{v_{T_A}^*}+\overline{v_{T_A}}\frac{\overline{i_{T_A}^*}}{Y_S}.$$

The noise power can then be calculated at each node according to the following equations:[2]

[2]The total noise at each node is given by $\overline{v_{n_{T_1}}^2}$ for node 1, $\overline{v_{n_{T_2}}^2}$ for node 2, etc.. The noise voltage input to each filter stage is given by $\overline{v_{n_{2_{in}}}^2}$ at node 2, $\overline{v_{n_{3_{in}}}^2}$ at node 3, etc..

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$$
\begin{aligned}
\overline{v_{n_{T_1}}^2} &= \left(\overline{v_{n_{A_{OC}}}^2} + \overline{v_{n_{in_{OC}}}^2}\right) \left|\frac{Y_S}{Y_S + Y_{in_A}}\right|^2 \\
\overline{v_{n_{2_{in}}}^2} &= \overline{v_{n_{T_1}}^2} \left|\frac{y_{21_a}}{y_{22_a} + Y_{L_2}}\right|^2 \\
\overline{v_{n_{T_2}}^2} &= \left(\overline{v_{n_{2_{in}}}^2} + \left(\overline{v_{n_{B_{OC}}}^2}\right) \left|\frac{Y_{OUT_A}}{Y_{OUT_A} + Y_{L_2}}\right|^2\right) \\
\overline{v_{n_{3_{in}}}^2} &= \overline{v_{n_{T_2}}^2} \left|\frac{y_{21_b}}{y_{22_b} + Y_{L_3}}\right|^2 \\
\overline{v_{n_{T_3}}^2} &= \left(\overline{v_{n_{3_{in}}}^2} + \left(\overline{v_{n_{C_{OC}}}^2}\right) \left|\frac{Y_{OUT_B}}{Y_{OUT_B} + Y_{L_3}}\right|^2\right) \\
\overline{v_{n_{4_{in}}}^2} &= \overline{v_{n_{T_3}}^2} \left|\frac{y_{21_c}}{y_{22_c} + Y_{L_4}}\right|^2 + \frac{4kT}{Re(Y_L)}
\end{aligned}
$$

where $\overline{v_{n_{in_{OC}}}^2} = \frac{4kT}{Re(Y_S)}$,

$Y_{L_4} = Y_L$,

$Y_{L_3} = Y_{IN_C}$,

$Y_{L_2} = Y_{IN_B}$;

and where all admittances, Y-parameters, and noise sources are functions of frequency.

The following equations relate the signal voltages along the filter chain. (Note that $V_1 = V_{1'}$, $V_2 = V_{2'}$ and so on.)

$$
\begin{aligned}
V_1 &= \left(\frac{Y_S}{Y_S + Y_{in_A}}\right) E_S \\
V_2 &= \left(\frac{-y_{21_a}}{y_{22_a} + Y_{L_2}}\right) V_1 \\
V_3 &= \left(\frac{-y_{21_b}}{y_{22_b} + Y_{L_3}}\right) V_2 \\
V_4 &= \left(\frac{-y_{21_c}}{y_{22_c} + Y_{L_4}}\right) V_3
\end{aligned}
$$

The power delivered to the load Y_{L_4} (ie. at node 4) in each frequency bin, f , can be expressed as:

$$P_S(f,4) = |V_4|^2 \, Re(Y_L), \tag{69}$$

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$$P_N(f,4) = \overline{v^2_{n_{4_{in}}}}\, Re(Y_L). \quad (70)$$

The power delivered to nodes 2 and 3 can be written similarly where V_4 is replaced by V_2 or V_3 and $\overline{v^2_{n_{4_{in}}}}$ is replaced by $\overline{v^2_{n_{2_{in}}}}$ or $\overline{v^2_{n_{3_{in}}}}$. The noise temperature, $T_{filter}(f,i)$ at node i can then be plotted as a function of frequency, f, using the relation:

$$T_{filter}(f,i) = \frac{P_N(f,i)}{k\,\mathrm{FBW}}.$$

The signal-to-noise, SNR, can be found for a frequency f at node i according to:

$$SNR(f,i) = \frac{P_S(f,i)}{P_N(f,i)}$$

Subroutine SNR calculates the total wanted signal power, $SGNLPW$, the noise power in W_S, $SBNS$, the power in I_A and I_B, $PWINTA$ and $PWINTB$, respectively, and the noise power from DC to f_{max}, $TOTNS$, at each of the nodes 1 - 4. This is accomplished by summing up the signal or noise power, P_S or N_S, given by eqns. 69 and 70, respectively, in each frequency bin from the first bin associated with that signal to the last bin. For example, at node i, these power are given by the following equations:

$$SGNLPW(i) = \sum_{f=M_1}^{M_2} P_S(f,i);$$

$$PWINTA(i) = \sum_{f=M_3}^{M_4} P_S(f,i);$$

$$PWINTB(i) = \sum_{f=M_5}^{M_6} P_S(f,i);$$

$$SBNS(i) = \sum_{f=M_1}^{M_2} P_N(f,i);$$

$$TOTNS(i) = \sum_{f=M_1}^{M_7} P_N(f,i);$$

where M_1 is the bin associated with FMARK(1) (here bin 1), M_2 with FMARK(2) (1.55KHz/FBW), ... and M_7 with f_{max}.

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Subroutine COMPNOISE groups the noise powers at the output of each filter stage according to its source either R_1, R_3, R_4 or op-amp noise generator.

Subroutine NF calculates the noise figure, $f_{filter}(f,i)$, in each frequency bin, f, at each node i according to:

$$f_{filter}(f,i) = \frac{SNR_{input}}{SNR_{output}}.$$

7.3 Direct Conversion Filter

Various choices of feedback elements are made for a gain per filter stage constraint of 10 dB. Filter parameters, r and C_2, are juggled in order to set the optimum source impedance for minimum noise temperature, $R_{N_{opt}}$, to the output impedance of the direct conversion amplifier.[3] As shown in Table 28, the output impedance of the proposed amplifier varies from 46K to 52K depending on the amplifier's bias. Therefore the filter's parameters are adjusted until its $R_{N_{opt}}$ is $\approx$ 50K. The corresponding feedback elements are found to be:

$$\begin{aligned} R_1 &= 23.8K\Omega; \\ C_2 &= 0.0047\mu F; \\ R_3 &= 105.6K\Omega; \\ R_4 &= 75.3K\Omega; \\ C_5 &= 0.00028\mu F. \end{aligned}$$

The performance of the filter stage is shown in Figures 89, 90, 91, and 92. Fig. 89 gives the signal and noise power from DC to 10 KHz at the input to the filter cascade (Node 1). The wanted signal and two interferers can easily be seen. Figures 90 and 91 show the signal and noise power at the input of the remaining two filter stages (Nodes 2 and 3). The performance at the output of the filter chain is shown in Fig. 92. The effect of the filter on the relative powers in W_s, I_A, and I_B can be clearly seen in each figure. The noise power added by each filter stage and its $1/f$ spectral distribution is

[3] $R_{N_{opt}}$ is defined by eqn. 67.

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also clearly evident. The load resistor is assumed to be 10 KΩ (increasing R_L gives better performance).

The following ratios are calculated at each node and shown beside each graph: *SGNLPW/SBNS*, *SGNLPW/TOTNS*, *SGNLPW/PWINTA*, and *SGNLPW/PWINTB*. At the output of the filter cascade, Fig. 92 lists the signal-to-noise ratio in the signal band to be 45.1 dB. The SNR is 44.9 dB in the DC to 10 KHz band. The signal-to-interferer A ratio is 34.5 dB and the signal-to-interferer B ratio is 81.5 dB. As can be seen from Fig. 92, the power level of I_B at the filter output is comparable to the noise power floor. The amount of $1/f$ noise (calculated to within 0.0001 Hz of DC) can be gauged by the following comparison: the average noise temperature in the DC to 1.55 KHz signal band is 88000 K; in the 50 Hz to 1.55 KHz band it is 64000 K.

The filter noise power possesses a very nonlinear spectrum. Figures 93, 94, and 95 show the noise components, computed by subroutine COMPNOISE in *syst.for*, at the output of the 1st, 2nd and final filter stages. The current noise source of the last filter stage is seen to be a major contributor to overall noise. The dominant noise source however is due to the joint noise contribution from the two preceeding stages as shown by the "input term" plot. These plots are used to select the best values of feedback components for the filter stage. Noise performance and filter selectivity are close to optimum with the choice of this source resistance.

Filter noise figure and gain in the signal band are given in Table 30. A comparison of worst-case noise temperatures for the balanced mixer (500 K estimated), the one-stage differential amplifier (770 K max. at 10 Hz when biased at 100 μA) with that of the filter below highlights the magnitude of its noise power over the signal band.

A 1.55 KHz cut-off filter was built along the design of the multiple loop feedback filter stage described above. It was implemented with Burr-Brown UAF 41 IC's [8]. The single stage gain performance was comparable to that of the single stage analyzed above.

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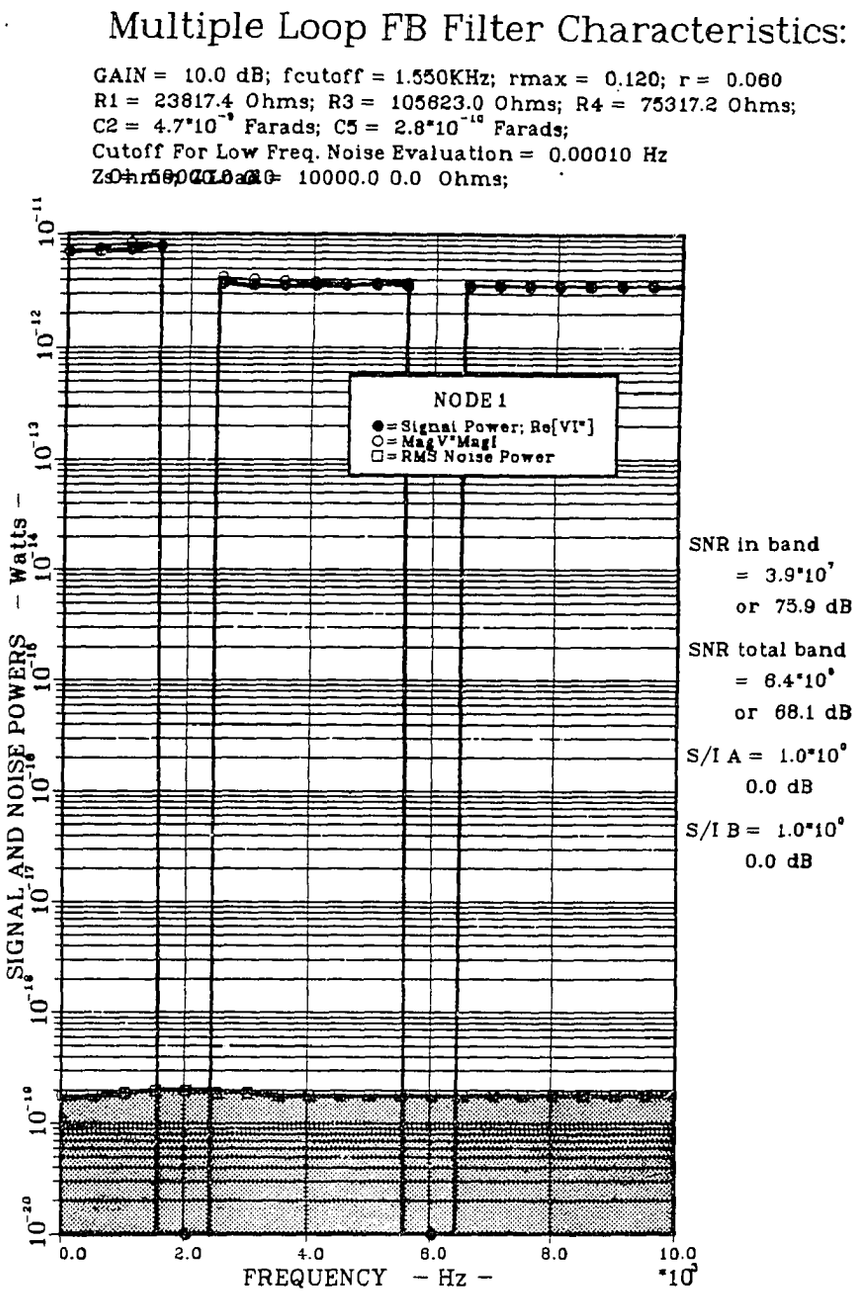


Figure 89: Spectrum at input to filter cascade.

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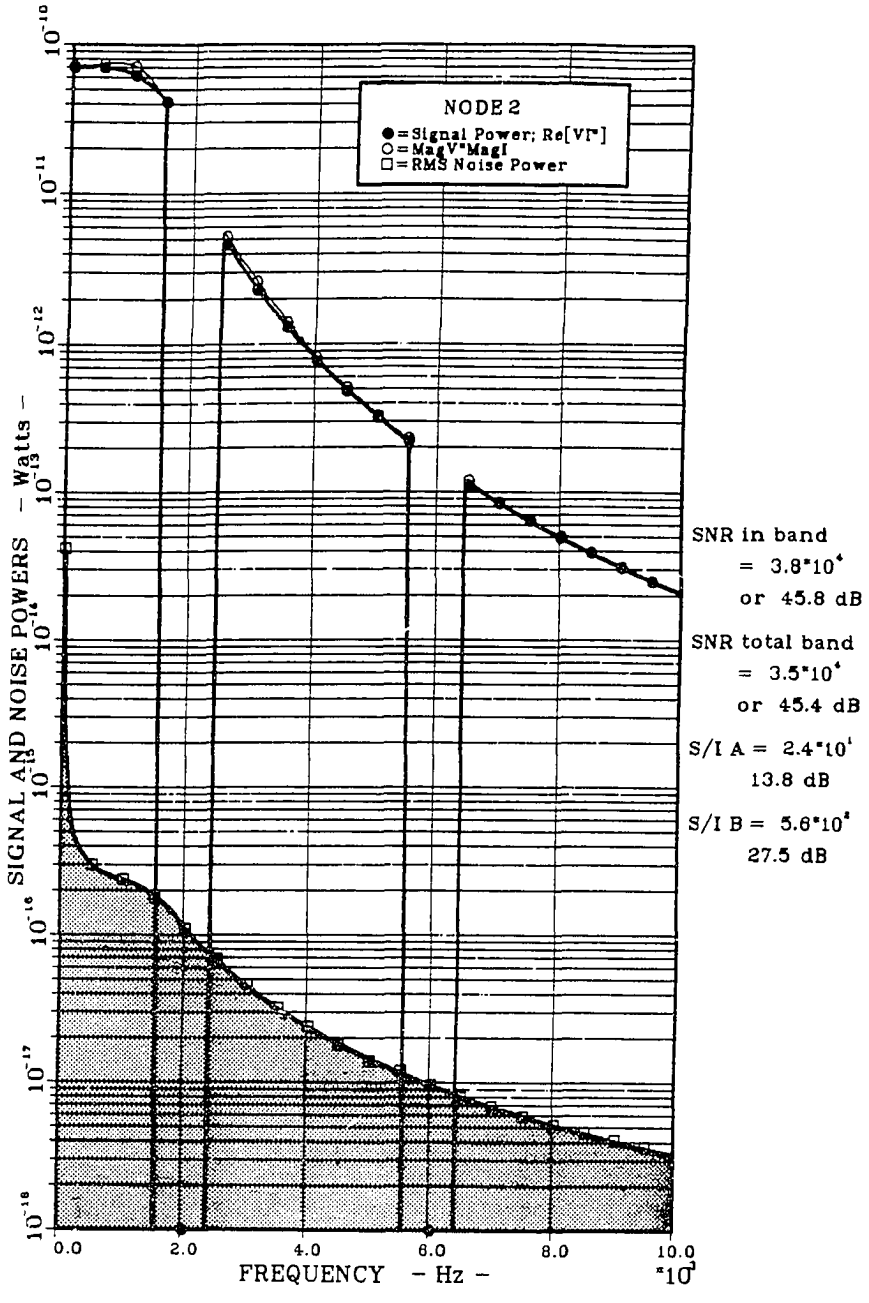


Figure 90: Spectrum at input to 2nd filter stage.

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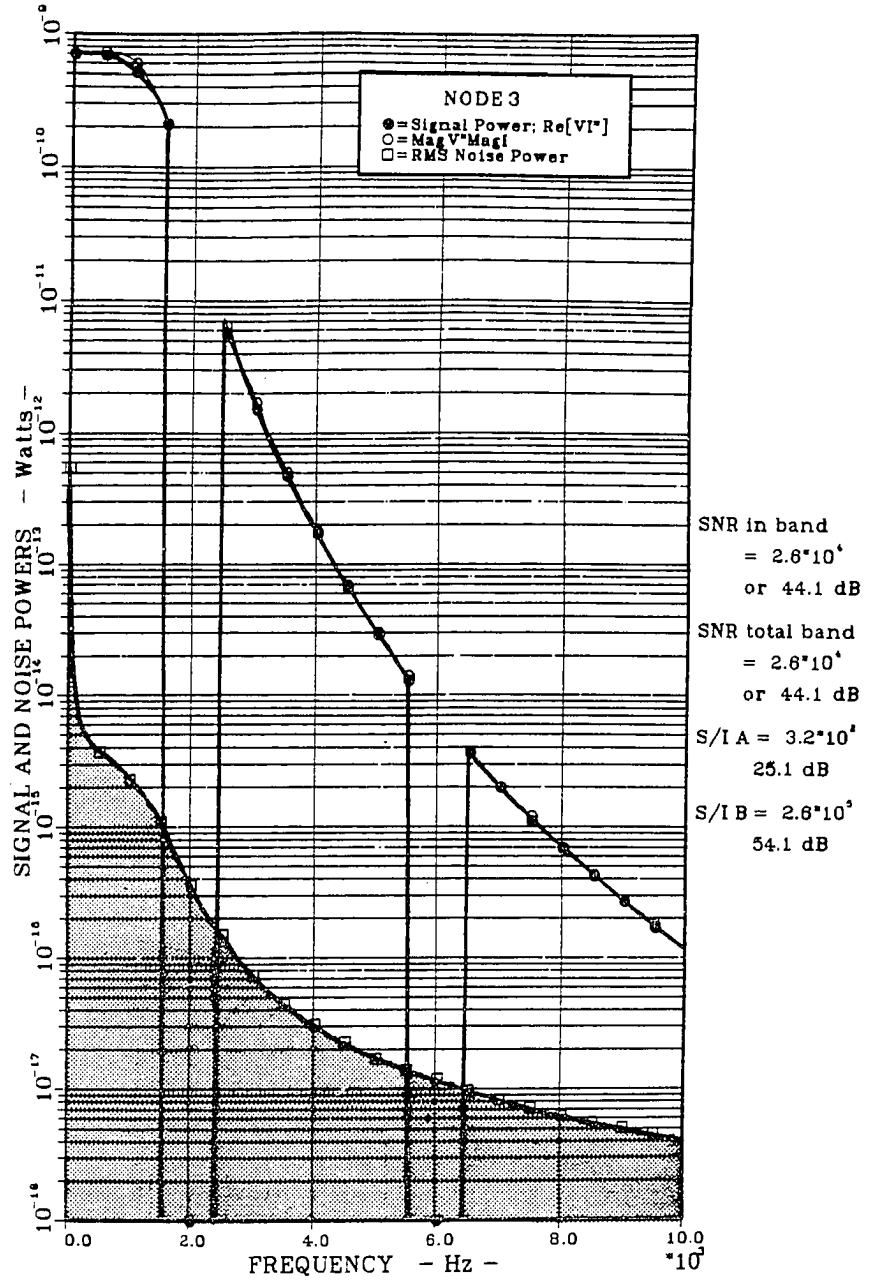


Figure 91: Spectrum at input to 3rd filter stage.

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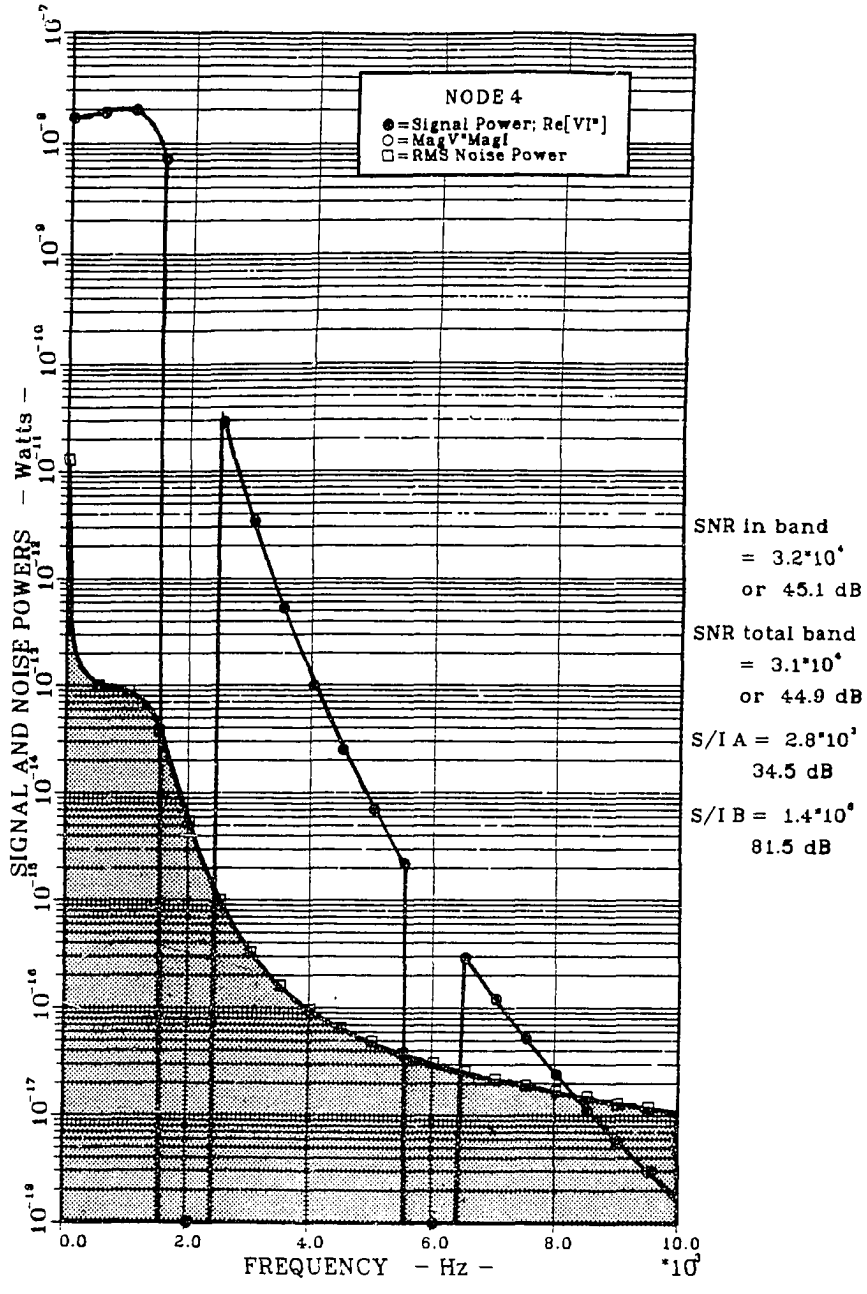


Figure 92: Spectrum at output of filter cascade.

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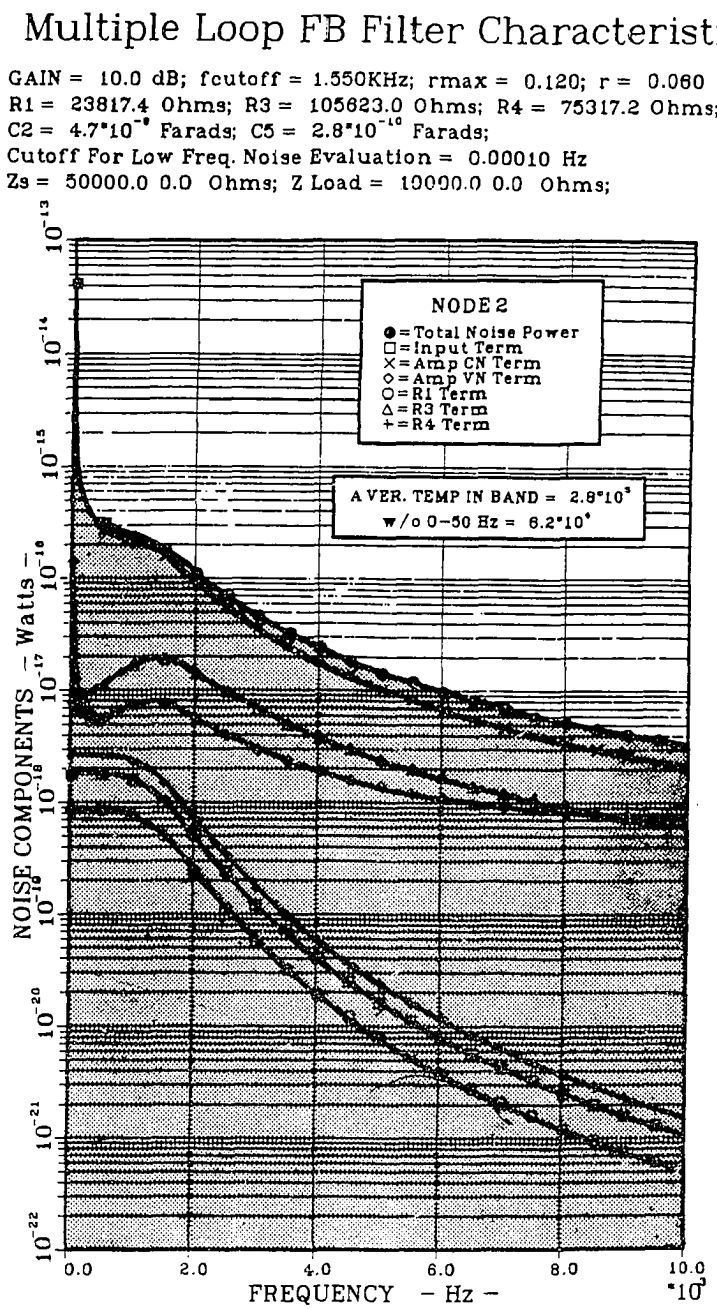


Figure 93: Components of filter noise spectrum at input to 2nd filter stage.

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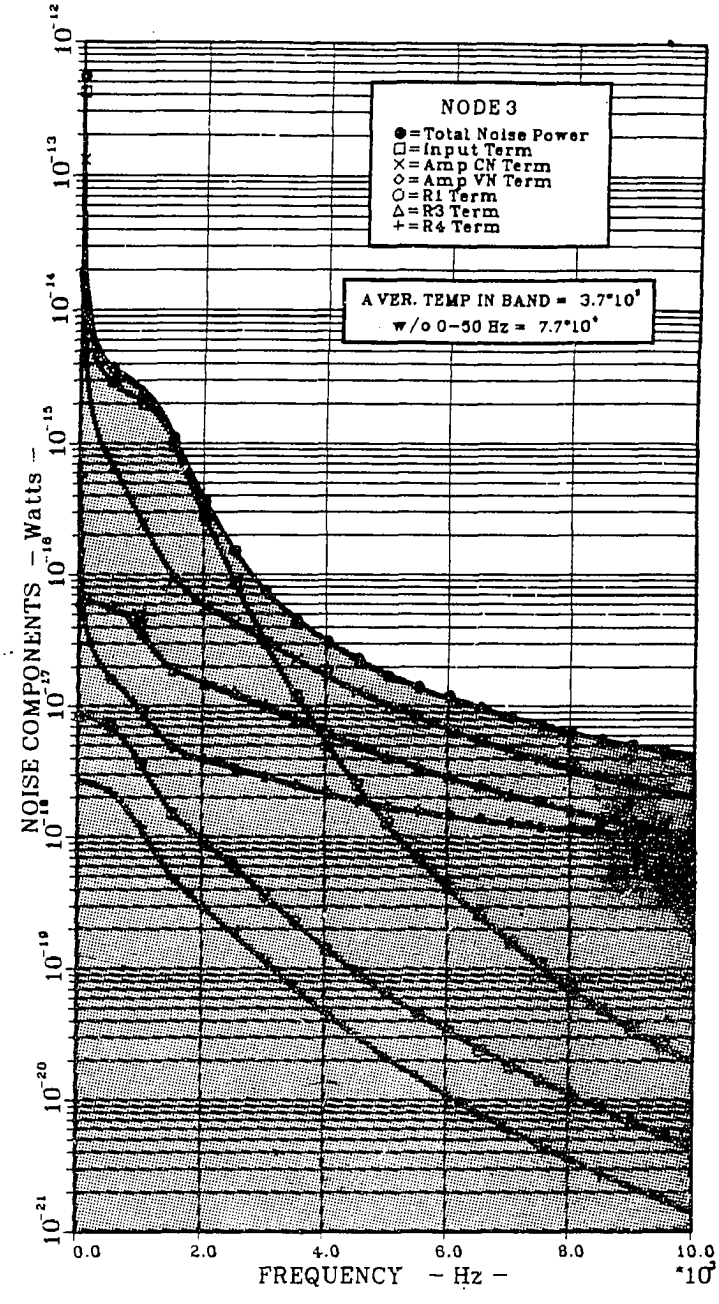


Figure 94: Components of filter noise spectrum at input to 3rd filter stage.

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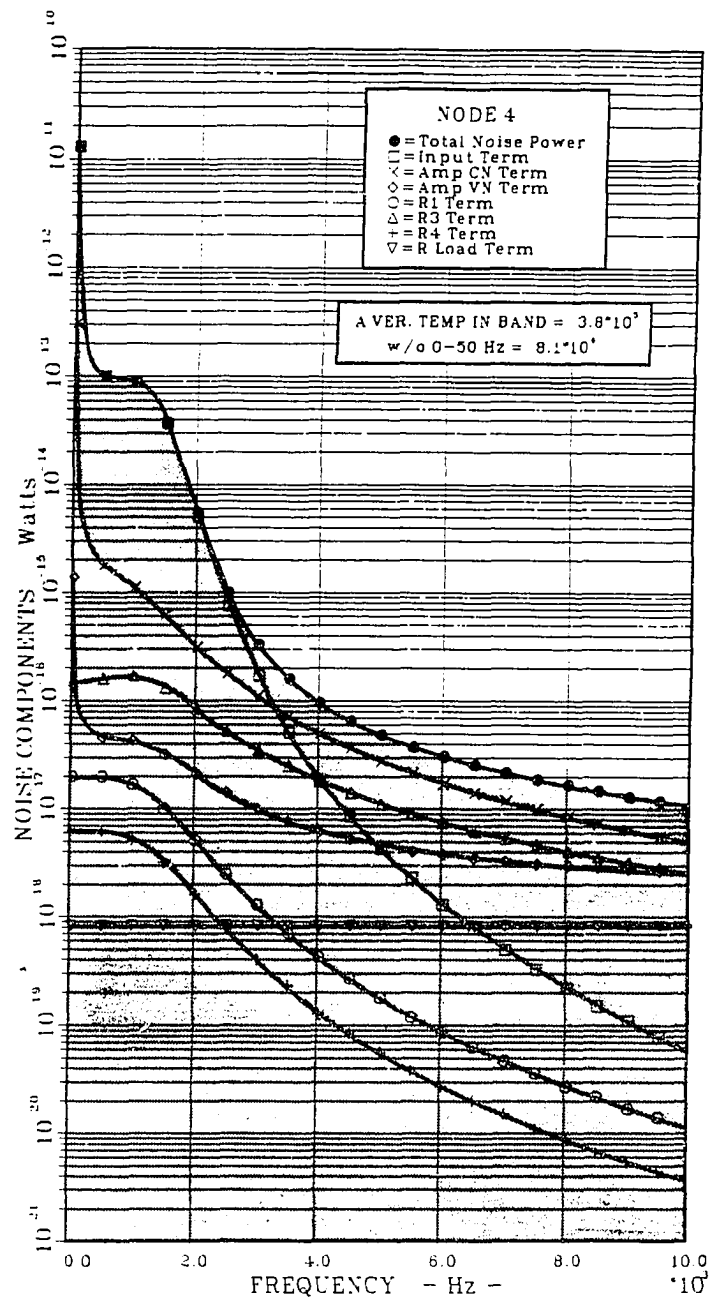


Figure 95: Components of filter noise spectrum at output of filter cascade.

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Table 30: Active Filter Performance

Frequency	Gain	NF_{filter}	F_{filter}
25 Hz	27.2 dB	34.3 dB	770,000 K
525 Hz	27.7 dB	22.3 dB	49,000 K
1025 Hz	27.9 dB	21.9 dB	45,000 K
1525 Hz	23.6 dB	22.7 dB	53,000 K

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Chapter 8

Proposed Direct Conversion Receiver

8.1 Expected Receiver Performance

Receiver gain, noise, and first stage selectivity performance can be calculated from component specifications. Eqns. 1 and 3 can be used to calculate the receiver gain and noise figure. The front-end circuits of the direct conversion receiver consists of the balanced mixer, several gain stages, and the active filter. They have been designed to conjugately match each other. Conversion loss for the balanced mixer is 2.1 dB, its noise temperature has been estimated to have a worst-case value of 500 K. The low frequency amplifier is built from the differential gain stages analyzed above. The fewer gain blocks are used the better dynamic range the receiver will have when adjacent channel signals are present. However several gain blocks may be necessary to reduce the noise contribution of the active filter to the overall receiver noise temperature. Each gain stage has a power gain of 24 (or 13.8 dB) when operated at an I_C of 25 μA and 370 (or 25.7 dB) when operated at an I_C of 100 μA. The noise temperature over frequency of this gain stage is given in Table 29. Operation at 25 μA is employed when a 0 - 10 Hz notch filter is used; operation at 100 μA is employed when a 0 - 100 Hz notch filter is permitted. The active filter noise and temperature performance is given in Table 30; it can attenuate an adjacent channel interferer by 34.5 dB and an

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interferer two channels over by 81.5 dB.

Table 31 gives receiver noise figure and gain performance for operation with a 10 Hz wide notch filter and a 100 Hz wide notch filter. In the former case three stages of gain are necessary to keep the receiver noise figure under 7 dB; in the latter one stage of gain is enough. If the signal characteristics can be designed to operate with a 200 Hz wide notch in their spectrum at f_c, then this is the favored receiver construction.

Table 31: Expected Receiver Gain and Noise Performance

	Notch Filter 0 - 10 Hz Gain Stage biased at 25 μA			
	2 gain stages		3 gain stages	
	10 Hz	1 KHz	10 Hz	1 KHz
Gain	52.7 dB	53.4 dB	66.5 dB	67.2 dB
NF_{rec}	10.9 dB	6.9 dB	7.0 dB	6.5 dB

	Notch Filter 0 - 100 Hz Gain Stage biased at 100 μA	
	1 gain stage	
	10 Hz	1 KHz
Gain	N/A	60.3 dB
NF_{rec}	N/A	6.8 dB

As shown in Fig. 1, receiver selectivity is established by the bipolar op-amp filter in the low-level processing circuits and the CMOS filters in the high-level processing circuits. Overall selectivity, or adjacent channel rejection, is expected to be 70 - 90 dB.

8.2 Conclusion

This thesis has discussed the merits of direct conversion receivers and has identified appropriate applications for its use. We have identified some of the application independent problems and application dependent problems which must be resolved

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in order for this receiver to gain acceptance as an viable alternative to the superheterodyne receiver. We proceed to look at two general application independent problems: the gain and phase match realizable between the 'I' and 'Q' channels in the direct conversion receiver and the design of the front-end components.

Gain and phase match have been assessed by measuring the suppression of the unwanted signal created at the output of the receiver for SSB reception. Infinite suppression is achieved for perfect gain and phase match between channels. The receiver is implemented with discrete components. An RF board contains the input mixers and first local oscillator and a low frequency board contains the remaining components for SSB reception. Suppression levels from 20 dB to 40 dB are measured for CW signal reception at 70 MHz.

The design challenges of the front-end components are identified. These components, RF mixers, low frequency amplifiers, and, low noise active filters, play a more important role in setting receiver performance in a direct conversion receiver than in a heterodyne receiver. These three components set the sensitivity, the dynamic range and, to some degree, the selectivity of the receiver. Design of an RF preamplifier is not considered here as we wish to determine the best sensitivity that can be achieved by taking an integrated approach to the design of the front-end components. In other words, each component is not designed to perform a single function, instead each component is designed to maximize the performance of the overall cascade. Should greater receiver sensitivity be required, this design strategy will insure that a minimum of RF gain be needed.

The majority of the thesis concerns the design of low conversion loss mixers using practical diodes. These diodes therefore differ greatly from the ideal exponential diodes that much of the theoretical mixer work is based upon. Practical diodes have series resistance and barrier capacitance in addition to barrier resistance. In addition package parasitics exist. In order to develop high performance, broadband mixers such as will be necessary for the direct conversion receiver, a computer-aided mixer analysis and design tool has been developed. It is based on a time domain mixer analysis and makes extensive use of graphical plots of the mixer waveforms in order to develop guidelines for optimization of the mixer's conversion loss. This

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combination of graphical and quantitative tools where the optimal mixer circuit is iteratively sought are necessary as it is near-impossible to analytically derive optimal circuit conditions for these diodes.

Using the design tool, RF phasing circuits and LO waveform shaping networks are designed for single-ended and balanced mixers. These mixers have lower conversion losses than mixers optimized to perform with purely resistive diodes. In other words, the existence of a second nonlinear diode element in addition to the diode's nonlinear resistance enhances the mixer's conversion loss. The noise temperature of these mixers is estimated using other mixer analysis programs. It found to be comparable to mixers having the same barrier capacitance designed with conventional techniques. Conversion loss improvement is greatest for small values of barrier capacitance, ie. up to 1 pF, however this barrier capacitance's range is that expected for a 1 GHz diode. The improved performance is interesting because, although it has been experimentally and theoretically predicted by some researchers, it contradicts the expectations of the majority of mixer designers.

Techniques for designing low noise, low frequency, amplifiers which are driven from low source impedances are developed. Noise and gain performance of an active filter is derived in order to optimize its design as well for low noise performance at low frequencies. Circuits for the low noise mixer, amplifier and filter appropriate for the direct conversion receiver are proposed and the ensuing worst-case receiver noise figure and gain are calculated.

Table 32 compares receiver characteristics for the direct conversion receiver against those of a typical mixer front-end heterodyne receiver. The direct conversion receiver possesses better noise figure and selectivity with less complexity and lower cost. The dramatic advantage in selectivity is due to the use of LPF filters realized with bipolar filters and high performance CMOS circuits rather than conventionally designed BPF at various IF frequencies. Although many topics regarding implementation of the direct conversion receiver still remain to be explored, this work will hopefully contribute to the growing awareness of the advantages of this type of receiver architecture and will lead to its implementation at higher frequencies and with a greater number of signal formats.

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Table 32: Comparison of Direct Conversion Receivers and Typical Heterodyne Receivers for Mobile Radio Applications

	Direct Conversion Receiver	Heterodyne Receiver
NF_{rec} (mixer front-end)	7.0 dB	12 dB
Selectivity	70 - 90 dB	60 - 80 dB
Complexity	Simple	High
Cost	Low	High

8.3 Future Work

There remain many interesting topics on the direct conversion receiver to be examined. They can be divided into three categories: those required to validate this component design detailed in this thesis, alternative approaches to component design that can be taken, and topics, outside the scope of this work, which remain to be studied.

In the first category are items concerning the mixer design: (1) experimental confirmation of low conversion loss; (2) theoretical analysis of mixer noise temperature, including $1/f$ noise sources; (3) experimental confirmation of noise temperature. In addition there are the areas of mixer research listed in Chapter 5.

In the second category lie alternative circuits for the direct conversion mixer that use transistors rather than diodes as the nonlinear elements. A possible circuit is the Gilbert multiplier. This circuit has been realized with high frequency silicon bipolar transistors for operation at 1 GHz [65,64]. The structure of this circuit is simple enough that it can be analyzed with the mixer design tool developed here.

Finally there are many topics, some application independent and some application dependent, that remain open for examination. They involve the generation of quadrature signals at 1 GHz, the locking of the local oscillators to the downconverted RF signal, the effect of the notch filter on different modulation types, and the design of demodulation circuits for specific signal formats. Some have been examined by

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other researchers. For example, the possibility of using number controlled oscillators to generate the local oscillator signals was studied in 1984 by Wang [74,73] who concluded that the current prototypes were too expensive and the harmonic content of their output was too rich for mobile radio applications. Alternatives to the use of a notch filter for reducing $1/f$ noise have been proposed by Bateman [7]. This work, which also discusses the application of the direct conversion receiver to mobile radio systems, concludes by favorably comparing the sensitivity and dynamic range of a direct conversion receiver to that of a heterodyne receiver.

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Appendix A

Mixer Appendix

A.1 Output of 'RM' Mixer Simulation Run — $N_{sample} = 4096$

Mixer run *pdiod5575* simulates a single-ended mixer with a resistive diode, DM_1, in a 'RM' circuit. The circuit has been simulated with a sample size of 4096 points taken every 27 psec; the RF frequency is 909MHz with an LO frequency of 900MHz. The first page of each portion of the program is shown. The actual program output contains the Fourier coefficients of the waveforms shown here at a larger number of frequencies.

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```
V1 = 9.440E-01
VNmax+1 = 9.440E-01
Diff = 0.000E+00
          pdiod5575.dat -                    !Run name
     Ibias =    0.000E+00
     Ilo = 4.000E-03 Amps      flo = 9.000E+08 Hz
     Irf = 4.000E-04 Amps      frf = 9.090E+08 Hz
     Rs = 1.000E+03 Ohms      Rl = 1.000E+03 Ohms
Fsample = 3.686E+10           Delta T = 2.713E-11

Fmax = 1.843E+10          Delta F = 8.999E+06


At sample    2 at  8.999E+06 Hz, Amplitude of Vout is  6.076E-02

At sample  202 at  1.809E+09 Hz, Amplitude of Vout is  1.892E-03

At sample 2001 at  1.800E+10 Hz, Amplitude of Vout is  1.466E-06

     % Diff. of IFs =              9.689E+01 %
     Conversion Loss =             3.692E-01    or  -4.328E+00dB
     20*log(V(  2001  )/V(     2)) = -9.235E+01dB

          Vdiode max    0.7247       Vdiode min   -4.3380
          Idiode max  3.629E-03      Idiode min  -2.422E-08

     Diode Condition:
          Voltage          Time/Ttotal
          Vd < 0.50           0.551
       0.50 < Vd < 0.65       0.055
          Vd > 0.65           0.394

          Vd > 0.50           0.449

     Average power consumption in:
                                 Rsource    3.304E-03
                                 Rload      8.949E-04
                                 Diode      6.604E-04
                          Diode and Rload   1.555E-03

     Average power delivered by sources:
                                 Ibias      0.000E+00
                                 Irf        0.000E+00
                                 Ilo        0.000E+00

     Total Source Power:          0.000E+00
     Total Power in Rs, Diode, Rl: 4.859E-03
```


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NO filter used

Sample	Vo	Freq	Mag Freq	Phase
1	9.440E-01	0.000E+00	9.395E-01	0.000E+00
2	9.388E-01	8.999E+06	6.076E-02	-7.689E+00
3	9.392E-01	1.800E+07	1.462E-03	1.644E+02
4	9.451E-01	2.700E+07	5.739E-05	-2.035E+01
5	9.560E-01	3.599E+07	8.613E-06	3.217E+01
6	9.712E-01	4.499E+07	4.804E-06	6.414E+01
99	1.180E+00	8.819E+08	5.886E-05	6.504E+00
100	1.180E+00	8.909E+08	6.634E-04	-1.750E+02
101	1.174E+00	8.999E+08	4.779E-02	-1.675E+02
102	1.163E+00	9.089E+08	5.384E-03	-1.671E+02
103	1.152E+00	9.179E+08	1.107E-05	-1.566E+02
104	1.141E+00	9.269E+08	5.345E-06	-5.490E+01
199	1.005E+00	1.782E+09	3.019E-05	1.028E+02
200	9.958E-01	1.791E+09	5.378E-04	-6.960E+01
201	9.863E-01	1.800E+09	1.211E-02	1.097E+02
202	9.770E-01	1.809E+09	1.892E-03	1.096E+02
203	9.677E-01	1.818E+09	4.570E-05	1.138E+02
204	9.585E-01	1.827E+09	6.180E-06	-1.164E+02
299	1.114E+00	2.682E+09	1.910E-05	1.975E+01
300	1.134E+00	2.691E+09	1.880E-04	-1.569E+02
301	1.150E+00	2.700E+09	1.284E-03	2.784E+01
302	1.163E+00	2.709E+09	2.076E-04	2.666E+01
303	1.171E+00	2.718E+09	7.877E-06	2.191E+01
304	1.174E+00	2.727E+09	2.160E-06	9.198E+01
399	1.040E+00	3.581E+09	9.578E-06	1.315E+02
400	1.030E+00	3.590E+09	1.188E-04	-4.963E+01
401	1.020E+00	3.599E+09	9.562E-04	1.274E+02
402	1.011E+00	3.608E+09	2.722E-04	1.274E+02
403	1.001E+00	3.617E+09	2.080E-05	1.359E+02
404	9.915E-01	3.626E+09	4.177E-06	-9.976E+01
499	9.901E-01	4.481E+09	1.585E-05	2.856E+01
500	1.013E+00	4.490E+09	9.333E-05	-1.359E+02
501	1.036E+00	4.499E+09	3.900E-04	4.673E+01
502	1.060E+00	4.508E+09	1.097E-04	4.678E+01
503	1.083E+00	4.517E+09	9.027E-06	4.774E+01
504	1.104E+00	4.526E+09	2.380E-06	1.502E+02
599	1.066E+00	5.381E+09	4.464E-06	1.498E+02
600	1.056E+00	5.390E+09	3.267E-05	-2.936E+01
601	1.046E+00	5.399E+09	1.788E-04	1.441E+02
602	1.036E+00	5.408E+09	8.214E-05	1.442E+02
603	1.026E+00	5.417E+09	1.462E-05	1.453E+02
604	1.016E+00	5.426E+09	2.095E-06	5.901E+01
699	9.013E-01	6.281E+09	1.179E-05	5.572E+01
700	9.077E-01	6.290E+09	5.249E-05	-1.215E+02
701	9.187E-01	6.299E+09	1.595E-04	6.650E+01

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pdiod5575.dat - !Run name
Ibias = 0.000E+00
Ilo = 4.000E-03 Amps flo = 9.000E+08 Hz
Irf = 4.000E-04 Amps frf = 9.090E+08 Hz
Rs = 1.000E+03 Ohms Rl = 1.000E+03 Ohms
Fsample = 3.686E+10 Delta T = 2.713E-11

Fmax = 1.843E+10 Delta F = 8.999E+06

FFT of Vdiode - NO filter used

Sample	Real Vd	Im Vd	Freq	Mag Freq	Phase
1	3.583E-01	0.00	0.000E+00	9.383E-01	1.800E+02
2	6.227E-01	0.00	8.999E+06	6.009E-02	1.781E+02
100	6.689E-01	0.00	8.909E+08	1.022E-02	8.799E+01
101	6.404E-01	0.00	8.999E+08	1.208E+00	-8.498E+01
102	4.006E-01	0.00	9.089E+08	1.107E-01	-8.563E+01
200	-3.025E+00	0.00	1.791E+09	1.712E-02	-1.691E+02
201	-2.518E+00	0.00	1.800E+09	3.862E-01	1.018E+01
202	-1.952E+00	0.00	1.809E+09	6.046E-02	9.959E+00
301	7.115E-01	0.00	2.700E+09	6.115E-02	-7.603E+01
401	-4.159E+00	0.00	3.599E+09	6.029E-02	1.955E+01
501	7.224E-01	0.00	4.499E+09	3.048E-02	-6.570E+01
601	-3.741E+00	0.00	5.399E+09	1.664E-02	2.829E+01
701	6.944E-01	0.00	6.299E+09	1.693E-02	-5.575E+01
801	-1.508E+00	0.00	7.199E+09	4.149E-03	3.383E+01
901	3.011E-02	0.00	8.099E+09	9.448E-03	-4.625E+01
1001	6.540E-01	0.00	8.999E+09	3.825E-04	-4.659E+01

FFT of Idiode - NO filter used

Sample	Real Id	Im Id	Freq	Mag Freq	Phase
1	8.212E-06	0.00	0.000E+00	9.398E-04	0.000E+00
2	3.961E-04	0.00	8.999E+06	6.165E-05	1.406E+00
100	1.130E-03	0.00	8.909E+08	1.063E-05	-9.256E+01
101	5.261E-04	0.00	8.999E+08	7.687E-04	-8.541E+01
102	1.053E-04	0.00	9.089E+08	8.747E-05	-8.500E+01
200	7.517E-09	0.00	1.791E+09	1.719E-05	9.769E+00
201	9.279E-09	0.00	1.800E+09	3.879E-04	-1.709E+02
202	1.121E-08	0.00	1.809E+09	6.072E-05	-1.710E+02
301	2.892E-03	0.00	2.700E+09	6.133E-05	1.033E+02
401	1.663E-09	0.00	3.599E+09	6.050E-05	-1.609E+02
501	3.492E-03	0.00	4.499E+09	3.056E-05	1.139E+02
601	-5.591E-09	0.00	5.399E+09	1.670E-05	-1.520E+02
701	2.068E-03	0.00	6.299E+09	1.696E-05	1.240E+02

Pav(f) in Diode - No Filter

Sample	Freq	Pav in Diode
1	0.000E+00	-1.764E-03
2	8.999E+06	-7.396E-06
100	8.909E+08	-2.172E-07
101	8.999E+08	1.858E-03
102	9.089E+08	1.937E-05
200	1.791E+09	-5.886E-07

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pdiod5575.dat - !Run name
Ibias = 0.000E+00
Ilo = 4.000E-03 Amps flo = 9.000E+08 Hz
Irf = 4.000E-04 Amps frf = 9.090E+08 Hz
Rs = 1.000E+03 Ohms Rl = 1.000E+03 Ohms
Fsample = 3.686E+10 Delta T = 2.713E-11

Fmax = 1.843E+10 Delta F = 8.999E+06

FFT of Vin - NO filter used

Sample	Real Vin	Im Vin	Freq	Mag Freq	Phase
1	1.302E+00	0.00	0.000E+00	1.172E-03	0.000E+00
2	1.561E+00	0.00	8.999E+06	6.091E-03	-8.843E+01
100	1.849E+00	0.00	8.909E+08	1.016E-02	9.176E+01
101	1.814E+00	0.00	8.999E+08	1.216E+00	-8.721E+01
102	1.564E+00	0.00	9.089E+08	1.116E-01	-8.837E+01
200	-2.029E+00	0.00	1.791E+09	1.705E-02	-1.673E+02
201	-1.531E+00	0.00	1.800E+09	3.844E-01	1.196E+01
202	-9.750E-01	0.00	1.809E+09	6.018E-02	1.173E+01
301	1.862E+00	0.00	2.700E+09	6.085E-02	-7.485E+01
401	-3.138E+00	0.00	3.599E+09	6.001E-02	2.042E+01
501	1.759E+00	0.00	4.499E+09	3.034E-02	-6.502E+01
601	-2.695E+00	0.00	5.399E+09	1.656E-02	2.886E+01

FFT of Iin - NO filter used

Sample	Real Iin	Im Iin	Freq	Mag Freq	Phase
1	8.284E-06	0.00	0.000E+00	9.397E-04	0.000E+00
2	3.962E-04	0.00	8.999E+06	6.163E-05	1.407E+00
100	1.130E-03	0.00	8.909E+08	1.062E-05	-9.255E+01
101	5.262E-04	0.00	8.999E+08	7.690E-04	-8.541E+01
102	1.054E-04	0.00	9.089E+08	8.749E-05	-8.500E+01
200	-5.975E-07	0.00	1.791E+09	1.719E-05	9.764E+00
201	-4.943E-07	0.00	1.800E+09	3.878E-04	-1.709E+02
202	-3.792E-07	0.00	1.809E+09	6.070E-05	-1.710E+02
301	2.892E-03	0.00	2.700E+09	6.132E-05	1.033E+02
401	-8.300E-07	0.00	3.599E+09	6.048E-05	-1.609E+02
501	3.492E-03	0.00	4.499E+09	3.055E-05	1.139E+02
601	-7.537E-07	0.00	5.399E+09	1.669E-05	-1.520E+02

Zin(f) - No Filter

Sample	Freq	Mag Freq	Phase
1	0.000E+00	1.247E+00	0.000E+00
2	8.999E+06	9.883E+01	-8.984E+01
3	1.800E+07	2.019E+02	2.637E+02
4	2.700E+07	7.574E+02	-1.291E+02
5	3.599E+07	2.582E+03	7.189E+01
6	4.499E+07	2.775E+03	1.034E+01
100	8.909E+08	9.567E+02	1.843E+02
101	8.999E+08	1.581E+03	-1.797E+00
102	9.089E+08	1.276E+03	-3.362E+00
103	9.179E+08	2.203E+03	1.584E+02

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pdiod5575.dat - !Run name
Ibias = 0.000E+00
Ilo = 4.000E-03 Amps flo = 9.000E+08 Hz
Irf = 4.000E-04 Amps frf = 9.090E+08 Hz
Rs = 1.000E+03 Ohms Rl = 1.000E+03 Ohms
Fsample = 3.686E+10 Delta T = 2.713E-11

Fmax = 1.843E+10 Delta F = 8.999E+06

Gdiode(f) - No Filter

Sample	Real gd	Im gd	Freq	Mag Freq	Phase
1	1.489E-03	0.00	0.000E+00	3.542E-02	0.000E+00
2	1.489E-03	0.00	8.999E+06	2.590E-03	-2.796E+00
100	5.209E-02	0.00	8.909E+08	6.632E-04	-8.202E+01
101	2.689E-02	0.00	8.999E+08	2.937E-02	-8.962E+01
102	1.786E-03	0.00	9.089E+08	3.593E-03	-9.238E+01
200	3.805E-09	0.00	1.791E+09	4.507E-04	-1.026E+01
201	3.475E-09	0.00	1.800E+09	1.561E-02	-1.793E+02
202	3.412E-09	0.00	1.809E+09	2.653E-03	1.765E+02
301	1.177E-01	0.00	2.700E+09	3.159E-03	9.055E+01
401	1.450E-08	0.00	3.599E+09	2.161E-03	-1.790E+02
501	1.300E-01	0.00	4.499E+09	1.414E-03	8.742E+01
601	-4.902E-09	0.00	5.399E+09	7.321E-04	-1.644E+02
701	6.876E-02	0.00	6.299E+09	1.169E-03	1.008E+02
801	-6.010E-09	0.00	7.199E+09	3.295E-04	3.024E+01
901	6.885E-09	0.00	8.099E+09	3.175E-04	5.885E+01
1001	3.655E-02	0.00	8.999E+09	2.317E-04	-8.594E+01

Sample	gdiode	Freq	Mag Freq	Phase
1	1.489E-03	0.000E+00	3.542E-02	0.000E+00
2	1.489E-03	8.999E+06	2.590E-03	-2.796E+00
3	1.699E-02	1.800E+07	2.725E-04	3.861E+01
4	4.503E-02	2.700E+07	2.848E-04	1.236E+02
5	6.773E-02	3.599E+07	2.084E-04	-1.556E+02
6	8.797E-02	4.499E+07	3.266E-05	8.431E+01
7	1.048E-01	5.399E+07	1.507E-04	1.379E+02
8	1.201E-01	6.299E+07	3.019E-04	1.602E+02
9	1.294E-01	7.199E+07	1.523E-04	-1.229E+02
10	1.386E-01	8.099E+07	1.778E-04	-8.274E+01
11	1.353E-01	8.999E+07	2.737E-05	-2.801E+01
12	1.500E-01	9.899E+07	1.331E-04	-1.194E+02
13	1.238E-01	1.080E+08	2.228E-04	-1.315E+01
14	1.248E-01	1.170E+08	3.528E-04	2.971E+01
15	1.132E-01	1.260E+08	2.882E-04	7.642E+01
16	9.565E-02	1.350E+08	1.237E-04	9.836E+01
17	7.612E-02	1.440E+08	9.461E-05	5.938E+01
18	5.512E-02	1.530E+08	2.231E-04	8.341E+01
19	3.008E-02	1.620E+08	1.979E-04	-1.613E+02
20	2.512E-03	1.710E+08	2.496E-04	-1.108E+02
21	3.027E-04	1.800E+08	2.213E-04	-4.694E+01
22	4.789E-10	1.890E+08	1.015E-04	-5.650E+01
23	-7.453E-09	1.980E+08	1.917E-04	-5.605E+01

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A.2 Output of 'RM' Mixer Simulation Run — $N_{sample} = 16384$

Mixer run *pdiod5573* simulates a single-ended mixer with a resistive diode, DM_1, in a 'RM' circuit. The circuit has been simulated with a sample size of 16384 points taken every 6.7 psec; the RF frequency is 909MHz with an LO frequency of 900MHz. The first page of each portion of the program is shown. The actual program output contains the Fourier coefficients of the waveforms shown here at a larger number of frequencies.

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```
V1 = 9.444E-01
VNmax+1 = 9.444E-01
Diff = 0.000E+00
          pdiod5573.dat

      Ibias =   0.000E+00
      Ilo = 0.400E-02 Amps      flo =900.0 Hz
      Irf = 0.400E-03 Amps      frf =909.0 Hz
      Rs = 1000.0 Ohms      Rl = 1000.0 Ohms
Fsample =                    Delta T = 6.782E-12

Fmax =                       Delta F =


At sample    2 at            Hz, Amplitude of Vout is  6.075E-02

At sample  202 at            Hz, Amplitude of Vout is  1.900E-03

At sample 5101 at            Hz, Amplitude of Vout is  8.955E-07

     % Diff. of IFs =              96.873 %
     Conversion Loss =            0.36905  or   -4.33dB
     20*log(V(25500)/V(100)) =     0.00dB

          Vdiode max    0.7252       Vdiode min   -4.3770
          Idiode max  3.658E-03      Idiode min  -2.956E-08

     Diode Condition:
          Voltage          Time/Ttotal
          Vd < 0.50           0.540
    0.50 < Vd < 0.65          0.066
          Vd > 0.65           0.394

          Vd > 0.50           0.460

     Average power consumption in:
                                Rsource     3.343E-03
                                Rload       9.053E-04
                                Diode       6.653E-04
                          Diode and Rload   1.571E-03

     Average power delivered by sources:
                                Ibias       0.000E+00
                                Irf         0.000E+00
                                Ilo         0.000E+00

     Total Source Power:          0.000E+00
     Total Power in Rs, Diode, Rl: 4.914E-03
```


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NO filter used

Sample	Vo	Freq	Mag Freq	Phase
1	9.444E-01	0.000E+00	9.449E-01	0.000E+00
2	9.424E-01	9.000E+06	6.075E-02	2.111E+01
3	9.407E-01	1.800E+07	1.429E-03	-1.381E+02
4	9.395E-01	2.700E+07	6.634E-05	6.301E+01
5	9.385E-01	3.600E+07	2.610E-06	-1.040E+02
6	9.380E-01	4.500E+07	5.718E-07	6.579E+01
99	1.103E+00	8.820E+08	4.942E-05	-5.559E+01
100	1.100E+00	8.910E+08	6.479E-04	1.538E+02
101	1.097E+00	9.000E+08	4.828E-02	-1.707E+02
102	1.095E+00	9.090E+08	5.411E-03	-1.413E+02
103	1.092E+00	9.180E+08	1.590E-05	-1.165E+02
104	1.089E+00	9.270E+08	5.787E-07	1.438E+02
199	1.043E+00	1.782E+09	3.798E-05	4.740E+01
200	1.049E+00	1.791E+09	5.535E-04	-1.044E+02
201	1.055E+00	1.800E+09	1.225E-02	1.032E+02
202	1.061E+00	1.809E+09	1.900E-03	1.320E+02
203	1.067E+00	1.818E+09	4.796E-05	1.597E+02
204	1.073E+00	1.827E+09	1.494E-06	3.041E+01
299	1.008E+00	2.682E+09	2.219E-05	-4.403E+01
300	1.005E+00	2.691E+09	1.872E-04	1.672E+02
301	1.003E+00	2.700E+09	1.296E-03	1.743E+01
302	1.001E+00	2.709E+09	2.064E-04	4.379E+01
303	9.982E-01	2.718E+09	5.430E-06	6.066E+01
304	9.959E-01	2.727E+09	9.280E-07	1.708E+01
399	1.168E+00	3.582E+09	1.330E-05	6.265E+01
400	1.166E+00	3.591E+09	1.261E-04	-9.262E+01
401	1.164E+00	3.600E+09	9.820E-04	1.147E+02
402	1.162E+00	3.609E+09	2.757E-04	1.437E+02
403	1.159E+00	3.618E+09	2.444E-05	1.704E+02
404	1.156E+00	3.627E+09	2.418E-06	-1.592E+02
499	9.297E-01	4.482E+09	1.619E-05	-3.168E+01
500	9.301E-01	4.491E+09	9.703E-05	1.795E+02
501	9.309E-01	4.500E+09	3.988E-04	2.985E+01
502	9.320E-01	4.509E+09	1.097E-04	5.743E+01
503	9.334E-01	4.518E+09	8.082E-06	7.827E+01
504	9.352E-01	4.527E+09	8.810E-07	-1.110E+01
599	1.069E+00	5.382E+09	4.763E-06	8.351E+01
600	1.066E+00	5.391E+09	3.615E-05	-7.804E+01
601	1.064E+00	5.400E+09	1.906E-04	1.263E+02
602	1.061E+00	5.409E+09	8.326E-05	1.561E+02
603	1.059E+00	5.418E+09	1.288E-05	-1.740E+02
604	1.056E+00	5.427E+09	5.144E-07	1.669E+02
699	1.084E+00	6.282E+09	1.248E-05	-1.644E+01
700	1.090E+00	6.291E+09	5.642E-05	-1.665E+02
701	1.095E+00	6.300E+09	1.666E-04	4.134E+01

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Ibias = 0.000E+00
Ilo = 0.400E-02 Amps flo =900.0 Hz
Irf = 0.400E-03 Amps frf =909.0 Hz
Rs = 1000.0 Ohms Rl = 1000.0 Ohms

FFT of Vdiode - NO filter used

Sample	Real Vd	Im Vd	Freq	Mag Freq	Phase
1	5.374E-01	0.00	0.000E+00	9.449E-01	1.800E+02
2	5.986E-01	0.00	9.000E+06	6.070E-02	-1.531E+02
100	-3.082E+00	0.00	8.910E+08	1.023E-02	6.129E+01
101	-3.197E+00	0.00	9.000E+08	1.216E+00	-8.497E+01
102	-3.307E+00	0.00	9.090E+08	1.115E-01	-5.687E+01
200	7.238E-01	0.00	1.791E+09	1.761E-02	1.626E+02
201	7.241E-01	0.00	1.800E+09	3.918E-01	1.028E+01
202	7.242E-01	0.00	1.809E+09	6.109E-02	3.906E+01
301	-3.428E+00	0.00	2.700E+09	6.217E-02	-7.637E+01
401	6.305E-01	0.00	3.600E+09	6.289E-02	1.997E+01
501	6.734E-01	0.00	4.500E+09	3.197E-02	-6.618E+01
601	-3.950E+00	0.00	5.400E+09	1.829E-02	2.981E+01
701	7.205E-01	0.00	6.300E+09	1.862E-02	-5.624E+01

FFT of Idiode - NO filter used

Sample	Real Id	Im Id	Freq	Mag Freq	Phase
1	1.411E-05	0.00	0.000E+00	9.451E-04	0.000E+00
2	1.158E-04	0.00	9.000E+06	6.154E-05	3.020E+01
100	-8.416E-09	0.00	8.910E+08	1.029E-05	-1.208E+02
101	-7.974E-09	0.00	9.000E+08	7.744E-04	-8.536E+01
102	-7.540E-09	0.00	9.090E+08	8.768E-05	-5.597E+01
200	3.578E-03	0.00	1.791E+09	1.765E-05	-1.850E+01
201	3.590E-03	0.00	1.800E+09	3.927E-04	-1.708E+02
202	3.596E-03	0.00	1.809E+09	6.123E-05	-1.420E+02
301	6.533E-09	0.00	2.700E+09	6.226E-05	1.029E+02
401	3.399E-04	0.00	3.600E+09	6.296E-05	-1.606E+02
501	1.252E-03	0.00	4.500E+09	3.200E-05	1.134E+02
601	-4.264E-09	0.00	5.400E+09	1.831E-05	-1.505E+02
701	3.383E-03	0.00	6.300E+09	1.864E-05	1.235E+02

Pav(f) in Diode - No Filter

Sample	Freq	Pav in Diode
1	0.000E+00	-1.786E-03
2	9.000E+06	-7.458E-06
100	8.910E+08	-2.104E-07
101	9.000E+08	1.884E-03
102	9.090E+08	1.955E-05
200	1.791E+09	-6.214E-07

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pdiod5573.dat

Ibias = 0.000E+00
Ilo = 0.400E-02 Amps flo =900.0 Hz
Irf = 0.400E-03 Amps frf =909.0 Hz
Rs = 1000.0 Ohms Rl = 1000.0 Ohms

FFT of Vin - NO filter used

Sample	Real Vin	Im Vin	Freq	Mag Freq	Phase
1	1.482E+00	0.00	0.000E+00	1.453E-06	0.000E+00
2	1.541E+00	0.00	9.000E+06	6.119E-03	-6.551E+01
100	-1.982E+00	0.00	8.910E+08	1.022E-02	6.492E+01
101	-2.099E+00	0.00	9.000E+08	1.221E+00	-8.722E+01
102	-2.212E+00	0.00	9.090E+08	1.122E-01	-5.962E+01
200	1.773E+00	0.00	1.791E+09	1.759E-02	1.644E+02
201	1.779E+00	0.00	1.800E+09	3.914E-01	1.207E+01
202	1.785E+00	0.00	1.809E+09	6.102E-02	4.085E+01
301	-2.425E+00	0.00	2.700E+09	6.210E-02	-7.518E+01
401	1.794E+00	0.00	3.600E+09	6.281E-02	2.086E+01
501	1.604E+00	0.00	4.500E+09	3.193E-02	-6.547E+01
601	-2.887E+00	0.00	5.400E+09	1.827E-02	3.040E+01

FFT of Iin - NO filter used

Sample	Real Iin	Im Iin	Freq	Mag Freq	Phase
1	1.422E-05	0.00	0.000E+00	9.449E-04	0.000E+00
2	1.159E-04	0.00	9.000E+06	6.153E-05	3.020E+01
100	-6.249E-07	0.00	8.910E+08	1.029E-05	-1.208E+02
101	-6.473E-07	0.00	9.000E+08	7.747E-04	-8.536E+01
102	-6.689E-07	0.00	9.090E+08	8.770E-05	-5.597E+01
200	3.578E-03	0.00	1.791E+09	1.765E-05	-1.850E+01
201	3.590E-03	0.00	1.800E+09	3.926E-04	-1.708E+02
202	3.596E-03	0.00	1.809E+09	6.122E-05	-1.420E+02
301	-6.790E-07	0.00	2.700E+09	6.225E-05	1.029E+02
401	3.400E-04	0.00	3.600E+09	6.295E-05	-1.606E+02
501	1.252E-03	0.00	4.500E+09	3.200E-05	1.134E+02
601	-7.943E-07	0.00	5.400E+09	1.831E-05	-1.505E+02

Zin(f) - No Filter

Sample	Freq	Mag Freq	Phase
1	0.000E+00	1.538E-03	0.000E+00
2	9.000E+06	9.946E+01	-9.571E+01
3	1.800E+07	1.939E+02	2.589E+02
4	2.700E+07	2.726E+02	-1.108E+02
5	3.600E+07	3.393E+02	5.944E+01
6	4.500E+07	2.000E+03	1.455E+02
100	8.910E+08	9.930E+02	1.858E+02
101	9.000E+08	1.576E+03	-1.870E+00
102	9.090E+08	1.279E+03	-3.649E+00

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pdiod5573.dat

Ibias = 0.000E+00
Ilo = 0.400E-02 Amps flo =900.0 Hz
Irf = 0.400E-03 Amps frf =909.0 Hz
Rs = 1000.0 Ohms Rl = 1000.0 Ohms

gdiode(f) - No Filter

Sample	Real gd	Im gd	Freq	Mag Freq	Phase
1	1.690E-03	0.00	0.000E+00	3.637E-02	0.000E+00
2	1.690E-03	0.00	9.000E+06	2.331E-03	3.239E+01
100	-3.773E-09	0.00	8.910E+08	4.059E-04	-1.388E+02
101	-3.843E-09	0.00	9.000E+08	2.978E-02	-8.642E+01
102	-3.945E-09	0.00	9.090E+08	3.310E-03	-5.599E+01
200	1.728E-01	0.00	1.791E+09	6.946E-04	-8.754E+00
201	6.666E-02	0.00	1.800E+09	1.502E-02	-1.728E+02
202	1.500E-01	0.00	1.809E+09	2.257E-03	-1.433E+02
301	4.194E-09	0.00	2.700E+09	2.192E-03	1.012E+02
401	1.589E-02	0.00	3.600E+09	2.735E-03	-1.669E+02
501	4.557E-02	0.00	4.500E+09	1.606E-03	1.041E+02
	45E-09	0.00	5.400E+09	3.455E-04	-1.343E+02
701	1.593E-01	0.00	6.300E+09	3.437E-04	1.417E+02
801	3.519E-09	0.00	7.200E+09	6.673E-04	-1.649E+02
901	-8.913E-09	0.00	8.100E+09	9.358E-04	1.119E+02
1001	8.750E-02	0.00	9.000E+09	5.208E-04	1.485E+01

Sample	gdiode	Freq	Mag Freq	Phase
1	1.690E-03	0.000E+00	3.637E-02	0.000E+00
2	1.690E-03	9.000E+06	2.331E-03	3.239E+01
3	6.320E-03	1.800E+07	2.681E-04	6.571E+01
4	1.224E-02	2.700E+07	1.520E-04	-1.637E+02
5	1.823E-02	3.600E+07	2.471E-04	-1.385E+02
6	2.379E-02	4.500E+07	2.115E-04	-1.643E+01
7	2.979E-02	5.400E+07	2.975E-04	-7.845E+01
8	3.592E-02	6.300E+07	5.925E-05	5.163E+01
9	4.156E-02	7.200E+07	1.595E-04	-4.364E+01
10	4.706E-02	8.100E+07	5.131E-05	-8.044E+01
11	5.108E-02	9.000E+07	2.157E-04	-1.259E+02
12	5.768E-02	9.900E+07	1.857E-04	-9.225E+00
13	6.355E-02	1.080E+08	1.807E-04	-3.577E+01
14	7.112E-02	1.170E+08	3.000E-04	1.287E+02
15	7.127E-02	1.260E+08	1.056E-04	5.447E+01
16	7.683E-02	1.350E+08	3.296E-04	-1.658E+02
17	8.841E-02	1.440E+08	2.021E-04	-9.283E+01

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A.3 Comparison of the LO Harmonic Amplitudes in a Mixer Circuit

All mixer simulation runs used to obtain mixer performance data were performed with N_{sample}, the number of sample points per LO cycle, set to 16384. Such a sample size guarantees that the interaction of the high sideband frequencies, $n > 5$, with the circuit are correctly evaluated. The differences in the value of the Fourier coefficient of these high order harmonics can easily be seen in Table 33 where the output of the design tool is compared for N_{sample} set to 2^{12} and 2^{14}. The difference in the phase estimate given by the two sample sizes is 10° for $3f_{LO}$ and 28° for $9f_{LO}$; the percent difference in the amplitude estimate is less than 1% at $3f_{LO}$ and 10% at $9f_{LO}$. Use of $N_{sample} = 16384$ translates into 18 samples at $9f_{LO}$. It is necessary to use such high sample rates to ensure correct mixer simulation.

A.4 UHF and Microwave Diode Characteristics — Development of Diode Models Used in Mixer Simulation

The diode model parameters for DM_1, DM_2 and DM_3 are based on typical S_i Schottky diode values for a p-type device, an n-type device and on a specific diode model, respectively. The parameters values for DM_1 and DM_2 were chosen from estimates found in the literature for p- and n-type devices. Schottky devices were chosen for the UHF (3-3000 MHz) direct downconversion mixer application over pn diodes as Schottky's have been shown to have a lower flicker (1/f) noise [4]. S_i Schottky's were chosen over GaAs Schottky's for the same reason. As the mixer output spans from a few hundred Hz above DC to half the RF bandwidth minimization of 1/f noise is important to achieve a low mixer temperature over the entire output frequency band.

Table 34 lists four researchers estimates for n-type S_i Schottky diode parameters.

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Table 33: Comparison of the LO Harmonic Amplitudes in a Mixer Circuit Simulated with Two Sample Sizes.

Harmonic $n \cdot f_{LO}$	$N_{sample} = 4096$ *pdiod5575*		$N_{sample} = 16384$ *pdiod5573*	
	Samples per $T_{n \cdot f_{LO}}$	Harmonic Amplitude and Phase	Samples per $T_{n \cdot f_{LO}}$	Harmonic Amplitude and Phase
f_{LO}	41	$4.8 \times 10^{-2} \quad \angle -167°$	164	$4.8 \times 10^{-2} \quad \angle -171°$
$2 \cdot f_{LO}$	20	$1.2 \times 10^{-2} \quad \angle +110°$	82	$1.2 \times 10^{-2} \quad \angle +103°$
$3 \cdot f_{LO}$	13.6	$1.28 \times 10^{-3} \quad \angle +28°$	54.7	$1.29 \times 10^{-3} \quad \angle +17°$
$4 \cdot f_{LO}$	10	$9.6 \times 10^{-4} \quad \angle +127°$	41	$9.8 \times 10^{-4} \quad \angle +115°$
$5 \cdot f_{LO}$	8.2	$3.9 \times 10^{-4} \quad \angle +47°$	32.8	$4.0 \times 10^{-4} \quad \angle +30°$
$6 \cdot f_{LO}$	6.8	$1.79 \times 10^{-4} \quad \angle +144°$	27.3	$1.9 \times 10^{-4} \quad \angle +126°$
$7 \cdot f_{LO}$	5.8	$1.59 \times 10^{-4} \quad \angle +66°$	23.4	$1.67 \times 10^{-4} \quad \angle +41°$
$8 \cdot f_{LO}$	5	$3.51 \times 10^{-5} \quad \angle +157°$	20.5	$4.02 \times 10^{-5} \quad \angle +137°$
$9 \cdot f_{LO}$	4.6	$6.85 \times 10^{-5} \quad \angle +82°$	18.2	$7.65 \times 10^{-5} \quad \angle +54°$

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The results are tabulated according to the frequency of operation of the mixer designed with each device. Table 35 gives the manufacturer specification for S_i Schottky diodes from Nippon Electric Co. [52] and Toshiba [69].

Four NEC devices parameters are shown corresponding to a low barrier and medium barrier n-type device and a low barrier and medium barrier p-type device. NEC believes p-type devices to have lower 1/f noise than n-type devices. P-type devices are recommended for applications where low output frequencies are required such as video detectors and doppler radar mixers. N-type devices are recommended for applications requiring low series resistance. Regardless of device type the low barrier devices possess a lower impedance than the medium barrier devices and hence are useful in wideband mixer applications; medium barrier devices have greater dynamic range [52].

In Table 35 the ideality factor for the NEC diode has been taken to be 1.0, the saturation current has been calculated from the forward current, I_F, and forward voltage, V_F pair according to:

$$I_S = \frac{I_F}{(e^{\frac{qV_F}{kT}} - 1)}. \tag{71}$$

The NEC specification of total capacitance (diode and package), C_T, at various diode voltage values is given.

The ideality factor, saturation current, series resistance, barrier capacitance at zero applied voltage, and, package capacitance for the Toshiba diode have been calculated from the manufacturer's curves for $I-V$ and C_T-V following the technique described in [35] as this device is the basis for DM_3. To estimate the first two parameters, n and I_S, two values of diode current, I_{d_1} and I_{d_2}, are chosen a decade apart. The corresponding diode voltages, V_{d_1} and V_{d_2}, are noted. I_{d_1} and I_{d_2} can be written in terms of the diode junction voltage V_{j1} and V_{j2} as follows:

$$I_{d_1} = I_S\,(e^{\frac{qV_{j1}}{nkT}} - 1) \tag{72}$$

$$I_{d_2} = I_S\,(e^{\frac{qV_{j2}}{nkT}} - 1) \tag{73}$$

Choosing $I_{d_1} >> I_S$ and $I_{d_2} >> I_S$, the current ratio I_{d_2}/I_{d_1} can be approximated in

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Table 34: S_i Schottky Diode Models Taken from Mixer Literature

Reference:	Liechti[41] 1970	Schuppert[59] 1086	Cerniglia [13] 1968	Akaike [3] 1977
Device:	Hewlett-Packard HP5082-2511	Alpha DMF5817A beam lead package	n-type beam lead package	n-type
Frequency of Operation:	3 GHz	2-4 GHz‡	9.4 GHz	120 GHz
Diode Parameters:				
I_S	$9.6{\cdot}10^{-9}$A	$5{\cdot}10^{-8}$A	$1{\cdot}10^{-9}$A	$1.4{\cdot}10^{-14}$A
n	1.04	1.08	1.06	1.1
r_{ser}	3.4Ω(@10mA)	2.5Ω	10Ω(@1mA)	17Ω
C_{j0}	0.56pF	0.25pF	0.21pF	0.03pF
M	0.5	0.5	0.5	0.3
ϕ	0.51†	0.60V	0.615V	0.85V
V_{RB}	N.G.*	N.G.	7-8V @ 10μA	N.G.
Package Characteristics:				
C_p	N.G.	0.1pF	0.05pF	N.G.
L_p	N.G.	0.1nH	N.G.	

†Liechti found that the C_T vs reverse voltage curve could be approximated by the M and ϕ values given above for $0 \leq V_R < \phi$ and by M = 0.233 and ϕ = 0.20V for -5V $\leq V_R \leq 0$.
‡The diode package has been designed for operation for 1.5GHz to 12.75 GHz.
* Not Given.

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Table 35: Selected NEC and Toshiba S_i Schottky Diode Parameters

Device	NEC - ND 4000 Series				Toshiba
	p-type device		n-type device		
	low barrier	medium barrier	low barrier	medium barrier	
Manufacturer: Part No.	ND4781	ND4132	ND4991	ND 4431	1-2J1A
EIAJ No.	1SS78	N.G.†	1SS16	1SS43	1SS239
Frequency of Operation	4 GHz	26 GHz	3 GHz	3 GHz	UHF/VHF/ CATV
Diode Parameters:					
I_F	1mA	1mA	1mA	1mA	
V_F	200mV	420mV	190mV	350mV	
I_S‡	$4.5{\cdot}10^{-7}$A	$9.6{\cdot}10^{-11}$A	$6.6{\cdot}10^{-7}$A	$1.4{\cdot}10^{-9}$A	$1.0{\cdot}10^{-9}$A
n‡	1.0	1.0	1.0	1.0	1.04
r_{ser}	N.G.	N.G.	N.G.	N.G.	6Ω
C_T	0.4pF @-0.2V	0.08-0.20pF @ 0V	0.7pF @ -0.2V	0.9pF @0V	0.8pF @0V
C_{j0}‡	N.G.	N.G.	N.G.	N.G.	0.6pF
C_p‡	N.G.	N.G.	N.G.	N.G.	0.2pF
ϕ	N.G.	N.G.	N.G.	N.G.	0.8V
V_{RB}	5-6V @100μA	3-7V @10μA	3V @100μA	10-20V @10μA	10-20V @10μA*

†Not Given.
‡See text for calculation.
*Estimated from current vs. reverse voltage curve and data point at 5V @10nA.

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terms of the difference in junctions voltage $\Delta V_j = V_{j2} - V_{j1}$:

$$\frac{I_{d_2}}{I_{d_1}} \simeq e^{\frac{q\Delta V_j}{nkT}} \tag{74}$$

As I_{d_2} and I_{d_1} have been chosen to differ by a decade, the following expression can be used to find n:

$$1 = \frac{q\Delta V_j}{nkT} \log 10(e) \tag{75}$$

When I-V curve of the Toshiba diode 1-2J1A is used to select values for I_{d_1}, V_{d_1} and I_{d_2}, V_{d_2}, n is found to be 1.04 and I_S is estimated at $1.0{\cdot}10^{-9}$A.

The series resistance can be found from:

$$r_{ser} = \frac{\Delta V_d}{\Delta I_d} \tag{76}$$

For the Toshiba diode, it is estimated to be 6Ω.

The values of C_{j0}, C_p and ϕ can be found from C_T - V curves given by the diode manufacturer. C_T can be written as:

$$C_T(V_d) = \frac{C_{j0}}{(1 - \frac{V_d}{\phi})^M} + C_p \tag{77}$$

Assuming M to be equal to 1/2, a plot of $1/(C_T - C_p)^2$ vs V_d should result in a straight line whose x-axis intercept is ϕ and whose y-axis intercept can be used to find C_{j0}. Various choices of C_p were used to plot $1/(C_T - C_p)^2$. The best straight line approximation occurred for $C_p = 0.2$pF whereupon $C_{j0} = 0.6$pF and $\phi = 0.8$V.

DM_1 was chosen to represent a medium barrier p-type S_i Schottky diode. This was thought to be the best device choice to guarantee low 1/f noise. DM_1 is modelled after the p-type device shown in Table 35.

DM_2 was chosen to represent a medium barrier n-type S_i Schottky diode. This device was thought to give the lowest conversion loss at frequencies above the 1/f knee of the device (10-100 kHz). DM_2 is modelled after the n-type devices shown in Table 34 and 35. Both DM_1 and DM_2 were selected to be medium barrier devices in order to obtain a mixer with good dynamic range.

DM_3 was taken to be the Toshiba 1-2J1A. It is modelled exactly according to the specifications given in Table 35 with the exception that the diode resistance, r_{ser}, has been raised from 6Ω to 10Ω as this was felt to be a more typical value.

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A.5 Program Listings

This section contains the listings for the FORTRAN programs used to evaluate the simulation data generated by SPICE. They are shown in Figure 12 of Chapter 3. The programs, *ndfft.for*, *zout.for*, and *cjplot.for*, are listed consecutively.

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ndfft.for

```
c                              NDFFT.for
c
c       NDFFT.for performs a FAST HARTLEY TRANSFORM on SPICE diode data
c       Smoothing is done, if desired, by a cos filter.
c       Written on February 13, 1986 by Polly Estabrook

c       This program is set up so that the following values are assumed:
c               One cycle of Fif  =   Time interval to be FHT 'ed
c                       lrf
c                       flo = nlo * fif
c                       frf = nrf * fif
c                       rs and rl
c                       nmax
c               In subroutine data no changes to delta t or t(1)

c       Output to be saved (printed with polly.ml) is on:
c               FOR022.DAT for Vload(f),Gdiod(f),Zdiod(f),and FFT(voc/isc)
c               FOR023.DAT for Gdiod(f) - small-signal admittance -
c                                       - records selected points
c               FOR024.DAT for Cbarrier(f) - small-signal capacitance -
c                                       - records selected points
c               FOR025.DAT for Pav(f) -  Records selected points
c               FOR026.DAT for Zin(f) -  Records selected points
c               FOR027.DAT for Zload(f) - Records nmax/8 points
c               FOR029.DAT for Vload(f) - Records selected points
c               FOR031.DAT for Zin(f) at diode for a BALANCED MIXER (as
c                       opposed to Zin(f) at RF PORT) - Records selected points
c
c       Output to be plotted with macfplt.for is on:
c               FOR011.DAT for FFT data:
c                               Vload,Gdiod,Zdiod,FFT(voc/isc)
c                                - Records nmax/8 points -

        complex x(20000,2)
        complex zo(20000)
        complex zwt(20000)

c       Complex numbers used for FFT subroutine. FHT is a purely
c       real version of the Fourier transform.

        dimension ffht(20000),ftest(20000)
        dimension y(20000),vo(20000),vwt(20000),vdiod(20000),vjunc(20000)
        dimension cdiod(20000),cvar4(20000),vin(20000),cvar1(20000)
        dimension ccap(20000), cres(20000)
        dimension gdiod(20000),cbar(20000),zdiod(20000),zin(20000),tout(20000)
        dimension csc(20000),cvar2(20000),cvar3(20000),cvar5(20000)
        dimension rft(20000),cft(20000),eft(20000),pft(20000)
        dimension veft(20000),vpft(20000),ceft(20000),cpft(20000)
        dimension zeft(20000),zpft(20000),dpwr(20000)
        dimension fr(20000),t(20000)
        dimension ititle(80)
        dimension kk(20),istart(10)

        data x/40000*(0.0,0.0)/
        data zo/20000*(0.0,0.0)/
        data zwt/20000*(0.0,0.0)/
        data y/20000*0.0/

        open (unit=34,file='test.dat',status='old',readonly)
c       open (unit=36,file='isc.dat',status='old',readonly)

c       This program reads Spice generated data from the file tran.dat
c       and writes x(t) and its FFT on FOR011.dat.

        pi = 3.1415926

        type 71
71      format(5x,'Enter Circuit Name, eg. Single Ended Mixer')
        read(5,72) (ititle(i),i=1,80)
72      format(80a1)

        type 86
86      format(5x,'Enter Source and Load Resistance, Rs and Rl',
     1  2x, 'in Kohms:', /,10x, 'eg. 10,10')
        accept *, rrs,rrl

        Rs = rrs*1000.0
        Rl = rrl*1000.0

        type 73
73      format(5x,'Enter Ibias, Ilo, and Irf in mA, nlo, nrf and fdown',
     1          2x,/,5x,'*** nlo = flo/fdown;  nrf = frf/fdown;',
     1          2x,'nrf = nlo + 1 ***')
        accept *, cbma, cloma, crfma, fnlo, fnrf, fdown

        cbias = cbma * 1.0*10.0**-3
        clo = cloma * 1.0*10.0**-3
        crf = crfma * 1.0*10.0**-3

        nlo = int(fnlo)
        nrf = int(fnrf)
        flo = nlo*fdown
        frf = nrf*fdown

        write(6,74) (ititle(i),i = 1,80)

C       1ST WRITE TO FILE FOR011.DAT

        write(11,74) (ititle(i),i = 1,80)
74      format(15x,80a1)

        write(6,75) cbias,clo,flo,crf,frf,rs,rl
75      format(10x,'Ibias =',1pe12.3,/,10x,'Ilo =',1pe10.3,
     1  1x,'Amps',5x,'flo =',1pe10.3,1x,'Hz',/,
     1  10x,'Irf =',1pe10.3,1x,'Amps',5x,'frf =',1pe10.3,1x,'Hr',/,
     1  10x,'Rs =',1pe10.3,1x,'Ohms',5x,'Rl =',1pe10.3,1x,'Ohms')

C       2ND WRITE TO FILE FOR011.DAT

        write(11,76) cbias,clo,flo,crf,frf
76      format(5x,5(1pe10.3,2x))

        write(11,78) rs,rl
78      format(5x,2(1pe10.3,2x))

        type 3
3       format(5x,'Enter Nmax, 64 min')
        accept *,nmax

c       nmax = 1024

        rser = 10.0
        cmat = 1.0*10.0**-14

        type 77
77      format(5x,'Enter Cjo and Cfixed in uF, ie. 1.0E-06, .30')
        accept *, cjjo,ccfix
```


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ndfft.for

```
      cjo = cjjo * 10.0**-6
      cfix = ccfix * 10.0**-6

c     cjo = .45*10.0**-6
c     bktoq = .026

      qcharge = 1.6*10.0**-19
      bk = 1.38 * 10.0**-23

      temp = 300

      bktoq = bk*temp/qcharge

      aphi = .9
      call data(nmax,clo,t,vo,cdiod,
     1     vdiod,cvar4,vin,cvar5,cvar1,cvar2,cvar3,cac,delt)

      call avpw(nmax,vo,cdiod,vdiod,cvar4,
     1          vin,cvar1,cvar2,cvar3,rs,rl,
     1          apwra,apwr1,apwd,apwdr1,apwlb,apwlrf,apwlio)

      call diostate(nmax,t,cdiod,vdiod,cmax,cmin,vmax,vmin,
     1              con,tcrf,tlin,tcon)

      fsamp = 1.0/delt
      delf = fsamp/nmax
      fmax = fsamp/2

135   write(6,135) fsamp,delt
      format(5x,'Fsample =',1pe10.3,10x,'Delta T =',1pe10.3)

140   write(6,140) fmax,delf
      format(5x,/,5x,'Fmax =',1pe10.3,10x,'Delta F =',1pe10.3,/)

c     enter data into x(1,1)

209   continue

200   type 200
      format(5x,'Which function do you want to FFT?',/,
     1 10x,'vload, Cdiode, Cbarrier, Fav Diode, Zin, Zload, Zin(diode) -
     1          balanced mixer.',/,
     1 10x,'vload, gdiode, vdiode, (voc/isc), Zin, Zload.',
     1  2x,'Type <1,2,3,4,5,6,7>.')
      accept *,fans

c     In calculating Fav Diode we find vdiode, therefore it can be removed
c     from the list of variables to be chosen.

c     fans = 1
      if (fans.LE.1) go to 216
      if (fans.EQ.2) go to 212
      if (fans.EQ.3) go to 213
      if (fans.EQ.4) go to 221
      if (fans.EQ.5) go to 217
      if (fans.EQ.6) go to 218
      if (fans.GE.7) go to 208

216   continue
      write(22,74) (ititle(i),i = 1,80)
      write(22,75) cbias,clo,flo,crf,frf,rs,rl
      write(22,135) fsamp,delf
      write(22,140) fmax,delf

      write(29,74) (ititle(i),i = 1,80)
      write(29,75) cbias,clo,flo,crf,frf,rs,rl
      write(29,135) fsamp,delt
      write(29,140) fmax,delf

      go to 219

212   continue
      write(23,74) (ititle(i),i = 1,80)
      write(23,75) cbias,clo,flo,crf,frf,rs,rl
      write(23,135) fsamp,delt
      write(23,140) fmax,delf

      go to 219

213   continue
      write(24,74) (ititle(i),i = 1,80)
      write(24,75) cbias,clo,flo,crf,frf,rs,rl
      write(24,135) fsamp,delt
      write(24,140) fmax,delf
      go to 219

221   continue
      write(25,74) (ititle(i),i = 1,80)
      write(25,75) cbias,clo,flo,crf,frf,rs,rl
      write(25,135) fsamp,delt
      write(25,140) fmax,delf
      go to 219

217   continue
      write(26,74) (ititle(i),i = 1,80)
      write(26,75) cbias,clo,flo,crf,frf,rs,rl
      write(26,135) fsamp,delt
      write(26,140) fmax,delf
      go to 219

218   continue
      write(27,74) (ititle(i),i = 1,80)
      write(27,75) cbias,clo,flo,crf,frf,rs,rl
      write(27,135) fsamp,delt
      write(27,140) fmax,delf
      go to 219

208   continue
      write(31,74) (ititle(i),i = 1,80)
      write(31,'/,'5) cbias,clo,flo,crf,frf,rs,rl
      write(31,135) fsamp,delt
      write(31,110) fmax,delf

219   continue

      if (fans.LE.1) go to 205
      if (fans.EQ.2) go to 210
      if (fans.EQ.3) go to 202
      if (fans.EQ.4) go to 204
      if (fans.EQ.5) go to 203
      if (fans.EQ.6) go to 206
      if (fans.GE.7) go to 207

c     For calculation of Zout - cvar4(1) MUST be cstot(1)
      .
205   continue
      do 11 i = 1,nmax
      ax = vo(i)
```

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ndfft.for

```
      bx = y(1)
      zo(1) = cmplx(ax,bx)
      continue
      go to 215

210   continue
      if (cfix.gt.0.0) go to 2210
      do 2211 i = 1,nmax
      vrser = cdlod(i) * rser
      vjunc(i) = vdlod(i) - vrser
      vratio = vjunc(i)/bktoq
      cres(i) = cap * (exp(vratio) - 1.0)
2211  continue
      if (cjo.gt.1.0E-12) go to 2215
c     The following is for the case of a purely resistive mixer
      vthres = 1.0*10.0**-06
      do 211 i = 2,nmax
      k = i - 1
      diffv = vjunc(i) - vjunc(k)
      diff(i - cdlod(i) - cdlod(k)
      vtst = abs(diffv)
      if (vtst.LE.vthres) go to 237
      qdlod(i) = diff(/diffv
      go to 236
237   qdlod(i) = qdlod(k)
236   continue
      ax = qdlod(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
211   continue
      qdlod(i) = qdlod(2)
      zo(i) = zo(2)
      go to 2270

2215  continue
c     For the case of cfix = 0 but non-zero Cjo.
      do 2220 i = 2,nmax
      k = i - 1
      diffv = vjunc(i) - vjunc(k)
      diff(i - cres(i) - cres(k)
      vtst = abs(diffv)
      if (vtst.LE.vthres) go to 2237
      qdlod(i) = diff(/diffv
      go to 2236
2237  qdlod(i) = qdlod(k)
2236  continue
      ax = qdlod(i)
      bx = y(i)
2220  continue
      qdlod(i) = qdlod(2)
      zo(i) = zo(2)
      go to 2270

2210  continue
c     For cfixed non-zero. I must estimate icapacitor so as to find
c     iresistive diode and vjunction.
      do 2225 i = 2,nmax
      k = i - 1
      ccap(i) = cfix * (vdlod(i) - vdlod(k)
      cres(i) = cdlod(i) - ccap(i)
      vrser = cres(i) * rser
      vjunc(i) = vdlod(i) - vrser
2225  continue
      vthres = 1.0*10.0**-06
      do 2245 i = 2,nmax
      k = i - 1
      diffv = vjunc(i) - vjunc(k)
      diff(i - cres(i) - cres(k)
      vtst = abs(diffv)
      if (vtst.LE.vthres) go to 2247
      qdlod(i) = diff(/diffv
      go to 2246
2247  qdlod(i) = qdlod(k)
2246  continue
      ax = qdlod(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
2245  continue
      qdlod(2) = qdlod(3)
      qdlod(1) = qdlod(3)
      zo(2) = zo(3)
      zo(1) = zo(3)

2270  continue
c     ------------------------------------------------------------
c     End of the g(t) calculations: 3 ways depending on purely resistive,
c     non-linear Cjo, or Cjo modelled as a fixed Capacitor.
c     ------------------------------------------------------------
      go to 215

202   continue
      if (cfix.gt.0.0) go to 2250
c     For cases where no cfixed
      do 201 i = 1,nmax
      zdlod(i) = abs(vdlod(i)/cdlod(i))
      vrser = cdlod(i)*rser
      vjunc(i) = vdlod(i) - vrser
      fac = 1 - (vjunc(i)/aphi)
      cbar(i) = cjo/(sqrt(fac))
      ax = cbar(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
201   continue
      go to 2265

2250  continue
c     For non-zero Cfixed
      do 2260 i = 1,nmax
      fac = 1 - (vdlod(i)/aphi)
      cbar(i) = cjo/(sqrt(fac))
      ax = cbar(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
2260  continue
2265  continue

      go to 215

c     ------------------------------------------------------------
c     For calculation of zout - cvar4(i) MUST be calculated
c     For use to get FFT(voc/isc)
c     ------------------------------------------------------------
c204  continue
      do 214 i = 1,nmax
      voc = cvar4(i)*rs
      zout(i) = voc/csc(i)
      ax = zout(i)
```


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ndfft.for

```
c       bx = y(i)
c       zo(i) = cmplx(ax,bx)
c214    continue
c       go to 215


215     continue


c-------------------------------------------------------------------
c
c       For use with cos filter
c
c-------------------------------------------------------------------
c
c       do 15 i = 1,nmax
c       ax = vwt(i)
c       bx = y(i)
c       zwt(i) = cmplx(ax,bx)
c15     continue

c       type 21
c21     format(5x,'Do you want to use smoothing filter? yes,no <0,1>')
c       accept *, ans

c       if(ans) 23,23,25

c23     continue
c       do 33 i = 1,nmax
c       x(i,1) = zwt(i)
c33     continue
c       write(6,29)
c       write(22,29)
c29     format(25x,'Cos filter used on data')
c       go to 27

c25     continue

ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

c       do 35 i = 1,nmax
c       x(i,1) = zo(i)
c35     continue

        do 36 i = 1,nmax
        ftest(i) = real(zo(i))
36      continue

27      continue

C       The fft routine included in this program can only handle
c       4096 points.
c       The program now calls the Fourier_Hartley Transform, FHT, to
c       which the program must be linked. This transform handles
c       from 16 to 1048,576 (2**20) points.

c       call fft(x,nmax,-1)

c       need scaling factor for width of pulse

c       do 20 i = 1,nmax
c       rft(i)= real(x(i,1))
c       cft(i) = aimag(x(i,1))
c       eft(i) = sqrt(rft(i)**2+cft(i)**2)/nmax
c       pft(i) = atan(cft(i)/rft(i))
c20     continue


c       ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

        call fht(ftest,nmax)

        ffht(1) = ftest(1)/(nmax**.5)
        rft(1) = (ftest(1) + ftest(1))/(2*(nmax**.5))
        cft(1) = 0
        eft(1) = (sqrt(rft(1)**2 + cft(1)**2))
        do 22 i= 2,nmax
        k = i-2
        ffht(i) = ftest(i)/(nmax**.5)
        rft(i) = (ftest(i) + ftest(nmax - k))/(2*(nmax**.5))
        cft(i) = (ftest(i) - ftest(nmax - k))/(2*(nmax**.5))
        eft(i) = (sqrt(rft(i)**2 + cft(i)**2))
22      continue

c       do 702 i = 1,nmax
c       write(6,705) i , t(i), vo(i),ffht(i), rft(i),cft(i),eft(i)
c705    format(2x,15,6(1x,1pe9.2))
c702    continue

        do 91 i =1,nmax
        if (rft(i).gt.1.0E-09) go to 92
        temp  = -1.0*rft(i)
        if (temp.gt.1.0E-09) go to 92
        if (cft(i).gt.1.0E-09) go to 93
        temp = -1.0*cft(i)
        if (temp.gt.1.0E-09) go to 94
        pft(i) = 5.0
        go to 95
93      pft(i) = -90.0
        go to 95
94      pft(i) = 90.0
        go to 95
92      radan = atan2(-cft(i),rft(i))
        pft(i) = (180.0/pi) * radan
95      continue
91      continue

        if (fans.LE.1) go to 41
        if (fans.EQ.2) go to 225
        if (fans.EQ.3) go to 305

c       if (fans.GE.4) go to 350
c       Above line to be used if calculating FFT(voc/isc)

41      continue

        fif1 = frf - flo
        fif2 = flo + frf
        flon = 51.0 * flo

        fif10 = fif1 - delf
        fif11 = fif1 + delf
        fif20 = fif2 - delf
        fif21 = fif2 + delf
        flon0 = flon - delf
        flon1 = flon + delf

        type *, fif1,fif10,fif11,fif2,fif20,fif21,flon,flon0,flon1
```


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ndfft.for

```
      do 600 i =1,nmax
      fr(i) = (i-1)*delf
      if (ifr(i)-fmax) 190,190,193
193   k = i - (nmax/2) - 1
      fr(i) = -1.0*(fmax-(k*delf))
190   continue
      if (ifr(i).GT.fif10.AND.fr(i).LT.fif11) iif1=i
      if (ifr(i).GT.fif20.AND.fr(i).LT.fif21) iif2=i
      if (ifr(i).GT.fif00.AND.fr(i).LT.fif01) iif3=i
600   continue

      iif1=2
      iif2=202

c     1st sample is dc, fif = iif1
c     2nd sample is delf, iif = 1005 = faum = iif2
c     202nd sample is (202-1)*delf = 1005 = faum = iif2
c     The last sample we want corresponds to the highest harmonic
c           of the LO that we get out of this choice of Nmax:
c                 Frequency of interest = INT(fmax/flo) * flo = flomax
c                       Sample of interest = INT((flomax/delf) + 1

      nlomax = int(fmax/flo)
      flomax = nlomax * flo

      iif3 = int(flomax/delf) + 1

      fr(iif1) = (iif1-1)*delf
      fr(iif2) = (iif2-1)*delf
      fr(iif3) = (iif3-1)*delf

c
c     type *, iif1,iif2,iif3,fr(iif1),fr(iif2),fr(iif3)
      write(6,723)
c723  format(5x, 'Enter iif1,iif2,iif3')
      accept *, iif1,iif2,iif3

      diffif = 100.0*(efc(iif3)-efc(iif2))/efc(iif1)
      convl = 16.0*(efc(iif1)**2)/(cerf**2)*rs*rl)
      convdb = 10.0*alog10(convl)
      xratio = efc(iif3)/efc(iif1)
      ratio = 20.0*alog10(xratio)

      write(6,720) iif1,fr(iif1),efc(iif1)
      write(22,720) iif1,fr(iif1),efc(iif1)
      write(29,720) iif1,fr(iif1),efc(iif1)
720   format(1x,/,5x,'At sample',i5,' at',
     1     1x,1pe10.3,' Hz, Amplitude of Vout is ',1pe10.3)

      write(6,730) iif2,fr(iif2),efc(iif2)
      write(22,730) iif2,fr(iif2),efc(iif2)
      write(29,730) iif2,fr(iif2),efc(iif2)
730   format(1x,/,5x,'At sample',i5,' at',
     1     1x,1pe10.3,' Hz, Amplitude of Vout is ',1pe10.3)

      write(6,740) iif3,fr(iif3),efc(iif3)
      write(22,740) iif3,fr(iif3),efc(iif3)
      write(29,740) iif3,fr(iif3),efc(iif3)
740   format(1x,/,5x,'At sample',i5,' at',
     1     1x,1pe10.3,' Hz, Amplitude of Vout is ', 1pe10.3)

      write(6,700) diffif,convl,convdb,iif2,iif1,ratio
      write(22,700) diffif,convl,convdb,iif2,iif1,ratio
      write(29,700) diffif,convl,convdb,iif2,iif1,ratio

700   format(1x,/,10x,'% Diff. of IFs = ',t40,1pe10.3,' %',
     1     1x,/,10x,'Conversion Loss = ',t40,1pe10.3,
     1     2x,'  or  ',1pe10.3,'dB',1x,/,10x,'20*log(V(',i6,
     1     2x,'))/V(',i6,')) = ',1pe10.3,'dB')

      write(6,760) vmax,vmin,cmax,cmin
      write(22,760) vmax,vmin,cmax,cmin
      write(29,760) vmax,vmin,cmax,cmin
760   format(1x,/,15x,'Vdiode max',t28,f8.4,7x,'Vdiode min',
     1     5x,'Idiode min',  t55,1pe10.3)

      write(6,770) toff,ton,tlin,ttot
      write(22,770) toff,ton,tlin,ttot
      write(29,770) toff,ton,tlin,ttot
770   format(1x,/,10x,'Diode Condition:',/,15x,'Voltage',
     1     1x,t32,'Time/Total',/,15x,'Vd < 0.50',t35,f5.3,
     1     1x,/,12x,'0.50 < Vd < 0.65',t35,f5.3,
     1     1x,/,15x,'Vd > 0.65',t35,f5.3,
     1     1x,/,15x,'Vd > 0.50',t35,f5.3)

      write(6,750) aprs,aprl,apd,apdrl
      write(22,750) aprs,aprl,apd,apdrl
      write(29,750) aprs,aprl,apd,apdrl
750   format(1x,/,10x,'Average power consumption in:',
     1     1x,/,t40,'Rsource',t50,1pe10.3,
     1     1x,/,t40,'Rload',t50,1pe10.3,
     1     1x,/,t40,'Diode',t50,1pe10.3,
     1     1x,/,t30,'Diode and Rload',t50,1pe10.3)

      write(6,780) apwlb,apwlrf,apwllo
      write(22,780) apwlb,apwlrf,apwllo
      write(29,780) apwlb,apwlrf,apwllo
780   format(1x,/,10x,'Average power delivered by sources:',
     1     1x,/,t40,'Iblas',t50,1pe10.3,
     1     1x,/,t40,'Irf',t50,1pe10.3,
     1     1x,/,t40,'Ilo',t50,1pe10.3)

      totpwd = apwlb + apwlrf + apwllo
      totpwr = aprs + aprl + apd

      write(6,790) totpwd,totpwr
      write(22,790) totpwd,totpwr
      write(29,790) totpwd,totpwr
790   format(1x,/,10x,'Total Source Power:',t40,1pe10.3,
     1     1x,/,10x,'Total Power in Rs, Diode, Rl:',t40,1pe10.3)

      write(6,31)
      write(22,31)
      write(29,31)
31    format(1x,/,25x,'NO filter used')

      continue
57    write(6,155)
      write(22,155)
      write(29,155)
155   format(1x,'Sample',6x,'Vo',7x,'Vdiode',6x,'Idiode',
     1     8x,'Freq',6x,'Rad Freq',5x,'Phase')

      do 125 i = 1,nmax/8
      write(22,100) i,vol(i),vdiod(i),cdiod(i),fr(i),efc(i),pfc(i)
```

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```
100     format(2x,15,6(2x,1pe10.3))
125     continue

        do 185 i = 1, 14
        write(6,195) i,vo(i),vdiod(i),cdiod(i),fr(i),eft(i),pft(i)
195     format(2x,15,6(2x,1pe10.3))
185     continue

        istart(1) = 1
        do 127 i = 2,10
        istart(i) = (i-1)*nlo - 1
127     continue

        do 128 k = 1,10
        istop = istart(k) + 5
        do 126 i = istart(k),istop
        write(29,195) i,vo(i),vdiod(i),cdiod(i),fr(i),eft(i),pft(i)
126     continue
128     continue

c       In the above way, we get data out from 1-10; 10points around n*flo;

        n2max = nmax/2

        do 129 i = iif3 - 5, iif3 + 5
        write(29,195) i,vo(i),vdiod(i),cdiod(i),fr(i),eft(i),pft(i)
129     continue

        do 131 i = n2max - 5, n2max + 5
        write(29,195) i,vo(i),vdiod(i),cdiod(i),fr(i),eft(i),pft(i)
131     continue

C       3RD WRITING ON FILE FOR011.DAT
c       writing on disk 11 to be read by fplot.for
c       which will plot the sampled time signal and
c       the amplitude and phase of FFT

        write(11,160) nmax, delf,delt
160     format(5x,16,e12.3,2x,e15.4)

ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c               Use with Cos filter
c
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

c       if(ans) 81,81,83
c81     continue
c       do 170 i =1,nmax
c       write(11,175) t(i),vdiod(i),vwt(i),fr(i),eft(i),pft(i)
c175    format(5x,1pe16.6,2(1pe10.3,2x),e12.3,2(2x,1pe10.3))
c170    continue
c       go to 85

c83     continue

ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

        do 145 i = 1,nmax/16
        write(11,165) t(i),vo(i),vdiod(i),fr(i),eft(i),pft(i)
165     format(5x,1pe16.6,2(1pe10.3,2x),e12.3,2(2x,1pe10.3))
145     continue
        go to 230
```

ndfft.for

6

```
c-----------------------------------------------------------------------
c       fans = 2
225     continue

c       Calculation of Gdiode - small-signal admittance

        kk(1) = 1
        kk(2) = 2
        kk(3) = nlo
        kk(4) = nlo + 1
        kk(5) = nlo + 2
        kk(6) = 2*nlo
        kk(7) = 2*nlo + 1
        kk(8) = 2*nlo + 2
        kk(9) = 3*nlo + 1
        kk(10) = 4*nlo + 1
        kk(11) = 5*nlo + 1
        kk(12) = 6*nlo + 1
        kk(13) = 7*nlo + 1
        kk(14) = 8*nlo + 1
        kk(15) = 9*nlo + 1
        kk(16) = 10*nlo + 1


        write(6,3531)
        write(23,3531)
3531    format(25x,'Gdiode(f) - No Filter')

        write(6,3555)
        write(23,3555)
3555    format(1x,'Sample',5x,'Real gd',2x,'Im gd'
     1          5x,'Freq',6x,'Mag Freq',6x,'Phase')

        do 3585 j = 1,16
        i = kk(j)
        fr(i) = (i-1)*delf
        if (fr(i)-fmax) 3590,3590,3593
3593    k = i - nmax/2 - 1
        fr(i) = -1.0*(fmax-(k*delf))
3590    continue
        write(6,3595) i,zo(i),fr(i),eft(i),pft(i)
        write(23,3595) i,zo(i),fr(i),eft(i),pft(i)
3595    format(2x,i5,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
3585    continue


        write(23,3556)
3556    format(1x,'Sample',6x,'Vjunc',6x,'Ires diode',3x,'gdiode',
     1          6x,'Freq',6x,'Mag Freq',6x,'Phase')


        do 3552 i = 1,180
        fr(i) = (i-1)*delf
        if (fr(i)-fmax) 3566,3566,3561
3561    k = i - nmax/2 - 1
        fr(i) = -1.0*(fmax-(k*delf))
3566    continue
        write(23,3501) i,vjunc(i),cres(i),gdiod(i),fr(i),eft(i),pft(i)
3501    format(2x,i5,6(2x,1pe10.3))
3552    continue
        .
        do 3553 i = 98,105
        fr(i) = (i-1)*delf
        write(23,3501) i,vjunc(i),cres(i),gdiod(i),fr(i),eft(i),pft(i)
```


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fbound.for

```
3553  continue
      do 3554 i = 199,205
      fr(i) = (i-1)*delf
      write(23,3501) i,vjunc(1),cres(1),gdiod(1),fr(i),efc(i),pfc(i)
3554  continue

      do 3559 i = 299,305
      fr(i) = (i-1)*delf
      write(23,3501) i,vjunc(1),cres(1),gdiod(1),fr(i),efc(i),pfc(i)
3559  continue

      do 3557 i = 399,405
      fr(i) = (i-1)*delf
      write(23,3501) i,vjunc(1),cres(1),gdiod(1),fr(i),efc(i),pfc(i)
3557  continue

      do 3558 i = 499,505
      fr(i) = (i-1)*delf
      write(23,3501) i,vjunc(1),cres(1),gdiod(1),fr(i),efc(i),pfc(i)
3558  continue

C     3RD WRITING ON FILE FOR011.DAT
c     writing on disk 11 to be read by fplot.for
c     which will plot the sampled time signal and
c     the amplitude and phase of FFT

      do 235 i = 1,nmax/16
      write(11,240) i,(i),gdiod(1),fr(i),efc(i),pfc(i)
240   format(5x,ipe16.6,2(1pe10.3,2x),e12.5,2(2x,1pe10.3))
235   continue
      go to 230
c-------------------------------------------------------------------
c     fans = 3
c-------------------------------------------------------------------
305   continue
c     Calculation of Cbarrier- small-signal capacitance (dQ/dV)

      kk(1) = 1
      kk(2) = 2
      kk(3) = nlo
      kk(4) = nlo + 1
      kk(5) = nlo + 2
      kk(6) = 2*nlo + 1
      kk(7) = 2*nlo + 2
      kk(8) = 2*nlo + 1
      kk(9) = 3*nlo + 1
      kk(10) = 4*nlo + 1
      kk(11) = 5*nlo + 1
      kk(12) = 6*nlo + 1
      kk(13) = 7*nlo + 1
      kk(14) = 8*nlo + 1
      kk(15) = 9*nlo + 1
      kk(16) = 10*nlo + 1

      write(6,1131)
      write(24,1131)
1131  format(25x,'Cbarrier(f) - No Filter')

      write(6,1132) cjo,rser,csat,sphi,bktoq
      write(24,1132) cjo,rser,csat,sphi,bktoq
```

ndfft.for

```
1137  format(15x,'Cjo =',1pe10.3,
     1       2x,/,15x,'series =',1pe10.3,15x,'is =',1pe10.3,
     1       2x,/,15x,'phi =',1pe10.3,14x,'kT/q =',1pe10.3)

      write(6,1155)
      write(24,1155)
1155  format(1x,'Sample',5x,'Real Cb',2x,'Im Cb'
     1       5x,'Freq',6x,'Mag Freq',6x,'Phase')

      do 1185 j = 1,16
      k = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1190,1190,1193
1193  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1190  continue
      write(6,1195) i,zo(i),fr(i),efc(i),pfc(i)
      write(24,1195) i,zo(i),fr(i),efc(i),pfc(i)
1195  format(2x,i5,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
1185  continue

      write(24,1156)
1156  format(1x,'Sample',7x,'Vjunc',5x,'Cbarrier',
     1       5x,'Freq',6x,'Mag Freq',6x,'Phase')

      do 1152 i = 1,180
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1166,1166,1161
1161  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1166  continue
      write(24,1101) i,vjunc(1),cbar(1),fr(i),efc(i),pfc(i)
1101  format(2x,i5,5(2x,1pe10.3))
1152  continue

      do 1153 i = 98,105
      fr(i) = (i-1)*delf
      write(24,1101) i,vjunc(1),cbar(1),fr(i),efc(i),pfc(i)
1153  continue

      do 1154 i = 199,205
      fr(i) = (i-1)*delf
      write(24,1101) i,vjunc(1),cbar(1),fr(i),efc(i),pfc(i)
1154  continue

      do 1159 i = 299,305
      fr(i) = (i-1)*delf
      write(24,1101) i,vjunc(1),cbar(1),fr(i),efc(i),pfc(i)
1159  continue

      do 1157 i = 399,405
      fr(i) = (i-1)*delf
      write(24,1101) i,vjunc(1),cbar(1),fr(i),efc(i),pfc(i)
1157  continue

      do 1158 i = 499,505
      fr(i) = (i-1)*delf
      write(24,1101) i,vjunc(1),cbar(1),fr(i),efc(i),pfc(i)
1158  continue

C     3RD WRITING ON FILE FOR011.DAT
```


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ndfft.for

```
c       writing on disk 11 to be read by fplot.for
c       which will plot the sampled time signal and
c       the amplitude and phase of FFT

      write(11,1125) nmax, delf,delt
1125  format(5x,i6,e12.3,2x,e15.4)

      do 310 i = 1,nmax/16
      write(11,315) t(i),cbar(i),yjunc(i),fr(i),efr(i),pfr(i)
315   format(5x,1pe16.6,2(1pe10.3,2x),e12.3,2(2x,1pe10.3))
310   continue
      go to 230
c-----------------------------------------------------------------
c       fans = 4

c       NOT used NOW. For use for calculating FFT(woc/isc)

c350  continue
c     do 360 i = 1,nmax/16
c     write(11,365) t(i),zout(i),cvar4(i),fr(i),efr(i),pfr(i)
c365  format(5x,1pe16.6,2(1pe10.3,2x),e12.3,2(2x,1pe10.3))
c360  continue
c     go to 230
c-----------------------------------------------------------------
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c85     continue
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

c       fans = 4

c-----------------------------------------------------------------
c
c       For calculation of Average Power in the Diode
c             Pav(i) = 1/2 * Vmag(i) * Imag(i) * cos(<V - <I)
c
c                      1. Find FFT of vdiode
c
c-----------------------------------------------------------------

204   continue
      kk(1) = 1
      kk(2) = 2
      kk(3) = nlo
      kk(4) = nlo + 1
      kk(5) = nlo + 2
      kk(6) = 2*nlo
      kk(7) = 2*nlo + 1
      kk(8) = 2*nlo + 2
      kk(9) = 3*nlo + 1
      kk(10) = 4*nlo + 1
      kk(11) = 5*nlo + 1
      kk(12) = 6*nlo + 1
      kk(13) = 7*nlo + 1
      kk(14) = 8*nlo + 1
      kk(15) = 9*nlo + 1
      kk(16) = 10*nlo + 1

      do 1313 i = 1,nmax
      ax = vdiod(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
1313  continue

      do 1336 i = 1,nmax
      x(i,1) = zo(i)
      ftest(i) = real(zo(i))
1336  continue
      write(6,1331)
      write(25,1331)
1331  format(25x,'FFT of Vdiode - NO filter used')

c-----------------------------------------------------------------
      call fft(x,nmax,-1)

c     need scaling factor for width of pulse

      do 1320 i = 1,nmax
      rfc(i)= real(x(i,1))
      cfc(i) = aimag(x(i,1))
      vofc(i) = sqrt(rfc(i)**2+cfc(i)**2)/nmax
      vpfc(i) = atan(cfc(i)/rfc(i))
1320  continue
c-----------------------------------------------------------------

      call fht(ftest,nmax)

      fht(1) = ftest(1)/(nmax**.5)
      rfc(1) = (ftest(1) + ftest(1))/(2*(nmax**.5))
      cfc(1) = 0
      vofc(1) = (sqrt(rfc(1)**2 + cfc(1)**2)
      do 1222 i= 2,nmax
      k = i-2
      fht(i) = ftest(i)/(nmax**.5)
      rfc(i) = (ftest(i) + ftest(nmax - k))/(2*(nmax**.5))
      cfc(i) = (ftest(i) - ftest(nmax - k))/(2*(nmax**.5))
1222  vofc(i) = (sqrt(rfc(i)**2 + cfc(i)**2))
      continue

      do 1319 i =1,nmax
      if (rfc(i).gt.1.0E-09) go to 1329
      temp = -1.0*rfc(i)
      if (temp.gt.1.0E-09) go to 1329
      if (cfc(i).gt.1.0*10**-9) go to 1324
      temp = -1.0*cfc(i)
      if (temp.gt.1.0*10.0**-9) go to 1323
      vpfc(i) = 5.0
      go to 1326
1324  vpfc(i) = -90.0
      go to 1326
1323  vpfc(i) = 90.0
      go to 1326
1329  radan = atan2(-cfc(i),rfc(i))
      vpfc(i) = (180.0/pi) * radan
1326  continue
1319  continue

      write(6,1355)
      write(25,1355)
1355  format(1x,'Sample',5x,'Real Vd',2x,'Im Vd',
     1    5x,'Freq',6x,'Mag Freq',6x,'Phase')

      do 1352 j = 1,16
```


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ndfft.for

```
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1366,1366,1361
1361  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1366  continue
      write(25,1301) i,zo(i),fr(i),veft(i),vpft(i)
1301  format(2x,15,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
1352  continue

      do 1385 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1390,1390,1393
1393  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1390  continue
      write(6,1395) i,zo(i),fr(i),veft(i),vpft(i)
1395  format(2x,15,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
1385  continue

c-----------------------------------------------------------------------
c
c                2. Find FFT of Idiode, cdiod
c
c-----------------------------------------------------------------------

      do 1413 i = 1,nmax
      ax = cdiod(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
1413  continue

      do 1436 i = 1,nmax
c     x(i,1) = zo(i)
      ftest(i) = real(zo(i))
1436  continue
      write(6,1431)
      write(25,1431)
1431  format(25x,'FFT of Idiode - NO filter used')
c-----------------------------------------------------------

c     call fft(x,nmax,-1)

c     need scaling factor for width of pulse

c     do 1420 i = 1,nmax
c     rft(i)= real(x(i,1))
c     cft(i) = aimag(x(i,1))
c     ceft(i) = sqrt(rft(i)**2+cft(i)**2)/nmax
c     cpft(i) = atan(cft(i)/rft(i))
c1420 continue
c-----------------------------------------------------------

      call fht(ftest,nmax)

      ffht(1) = ftest(1)/(nmax**.5)
      rft(1) = (ftest(1) + ftest(1))/(2*(nmax**.5))
      cft(1) = 0
      ceft(1) = (sqrt(rft(1)**2 + cft(1)**2))
      do 1422 i= 2,nmax
      k = i-2
      ffht(i) = ftest(i)/(nmax**.5)
      rft(i) = (ftest(i) + ftest(nmax - k))/(2*(nmax**.5))
      cft(i) = (ftest(i) - ftest(nmax - k))/(2*(nmax**.5))
      ceft(i) = (sqrt(rft(i)**2 + cft(i)**2))
1422  continue

      do 1419 i =1,nmax
      if (rft(i).gt.1.0E-09) go to 1429
      temp  = -1.0*rft(i)
      if (temp.gt.1.0E-09) go to 1429
      if (cft(i).gt.1.0*10**-9) go to 1424
      temp = -1.0*cft(i)
      if (temp.gt.1.0*10.0**-9) go to 1423
      cpft(i) = 5.0
      go to 1426
1424  cpft(i) = -90.0
      go to 1426
1423  cpft(i) = 90.0
      go to 1426
1429  radan = atan2(-cft(i),rft(i))
      cpft(i) = (180.0/pi) * radan
1426  continue
1419  continue

      write(6,1455)
      write(25,1455)
1455  format(1x,'Sample',5x,'Real Id',2x,'Im Id',
     1   5x,'Freq',6x,'Mag Freq',6x,'Phase')

      do 1452 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1466,1466,1461
1461  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1466  continue
      write(25,1401) i,zo(i),fr(i),ceft(i),cpft(i)
1401  format(2x,15,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
1452  continue

      do 1485 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1490,1490,1493
1493  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1490  continue
      write(6,1495) i,zo(i),fr(i),ceft(i),cpft(i)
1495  format(2x,15,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
1485  continue

cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c           Calculation of Pav:
c                   Pav(f) = Re(Instantaneous Power at f)
c                   Pav(f) = Re(v(t)*i(t))  where v(t),i(t) are at freq. f
c
c                   Pav(f) = 1/2 * Vmag(f) * Imag(f) * cos(<V - <I)
c         * where Vmag and Imag are Vdiod(500) + Vdiod(-500)
c
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
```

9

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ndfft.for

```
      do 1505 i = 1,nmax
      angle = vpfc(i) - cpfc(1)
      cosa = cos(angle)
      dpwr(i) = 0.5*(2.0*vefr(i)**2.0*cefc(i))*cosa
1505  continue

      write(6,1531)
      write(25,1531)
1531  format(25x,'Pav(f) in Diode - No Filter')

      write(6,1555)
      write(25,1555)
1555  format(6x,'Sample',4x,'Freq',6x,'Pav in Diode')

      do 1585 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1590,1590,1593
1593  fr(i) = nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1590  continue
      write(6,1595) i,fr(i),dpwr(i)
      write(25,1595) i,fr(i),dpwr(i)
1595  format(1x,i10,2(2x,1pe10.3))
1585  continue

      write(25,1556)
1556  format(2x,/,/,6x,'Sample',4x,'Freq',6x,'Pav in Diode')

      do 1552 i = 1,10
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1566,1566,1561
1561  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1566  continue
      write(25,1501) i,fr(i),dpwr(i)
1501  format(1x,i10,2(2x,1pe10.3))
1552  continue

      do 1553 i = 98,105
      fr(i) = (i-1)*delf
      write(25,1501) i,fr(i),dpwr(i)
1553  continue

      do 1554 i = 199,205
      fr(i) = (i-1)*delf
      write(25,1501) i,fr(i),dpwr(i)
1554  continue

      do 1559 i = 299,305
      fr(i) = (i-1)*delf
      write(25,1501) i,fr(i),dpwr(i)
1559  continue

      do 1557 i = 399,405
      fr(i) = (i-1)*delf
      write(25,1501) i,fr(i),dpwr(i)
1557  continue

      do 1558 i = 499,505
      fr(i) = (i-1)*delf
      write(25,1501) i,fr(i),dpwr(i)
1558  continue
```

10

```
C     3RD WRITING ON FILE FOR011.DAT
C     writing on disk 11 to be read by fplot.for
C     which will plot the sampled time signal and
C     the amplitude and phase of FFT
C
      write(11,1506) nmax, delf,delt
1506  format(5x,i6,e12.3,2x,e15.4)

      do 1530 i = 1,nmax
      write(11,1535) t(i),vdiod(i),cdiod(i),fr(i),dpwr(i)
1535  format(5x,1pe16.6,2(1pe10.3,2x),e12.3,2x,1pe10.3)
1530  continue

cccccccccccccccccccccccccccccccccccccccccccccccccccccccc

      End of Pav in Diode

cccccccccccccccccccccccccccccccccccccccccccccccccccccccc
cccccccccccccccccccccccccccccccccccccccccccccccccccccccc
cccccccccccccccccccccccccccccccccccccccccccccccccccccccc
      go to 230

c-------------------------------------------------------

      For calculation of zin
      1. Find FFT of vin

c-------------------------------------------------------

203   continue
      kk(1) = 1
      kk(2) = 2
      kk(3) = nlo
      kk(4) = nlo + 1
      kk(5) = nlo + 2
      kk(6) = 2*nlo
      kk(7) = 2*nlo + 1
      kk(8) = 2*nlo + 2
      kk(9) = 3*nlo + 1
      kk(10) = 4*nlo + 1
      kk(11) = 5*nlo + 1
      kk(12) = 6*nlo + 1
      kk(13) = 7*nlo + 1
      kk(14) = 8*nlo + 1
      kk(15) = 9*nlo + 1
      kk(16) = 10*nlo + 1

      do 313 i = 1,nmax
      ax = vin(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
313   continue

      do 336 i = 1,nmax
      x(i,1) = zo(i)
      fzero(i) = real(zo(i))
336   continue
      write(6,331)
      write(26,331)
331   format(25x,'FFT of Vin - NO filter used')
```


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ndfft.for

```
c-----------------------------------------------------------------------
c       call fft(x,nmax,-1)

c       need scaling factor for width of pulse

c       do 320 i = 1,nmax
c       rft(i)= real(x(i,1))
c       cft(i) = aimag(x(i,1))
c       veft(i) = sqrt(rft(i)**2+cft(i)**2)/nmax
c       vpft(i) = atan(cft(i)/rft(i))
c320    continue

c-------------------------------------------------------------

        call fht(ftest,nmax)

        ffht(1) = ftest(1)/(nmax**.5)
        rft(1) = (ftest(1) + ftest(1))/(2*(nmax**.5))
        cft(1) = 0
        veft(1) = (sqrt(rft(1)**2 + cft(1)**2))
        do 222 i= 2,nmax
        k = i-2
        ffht(i) = ftest(i)/(nmax**.5)
        rft(i) = (ftest(i) + ftest(nmax - k))/(2*(nmax**.5))
        cft(i) = (ftest(i) - ftest(nmax - k))/(2*(nmax**.5))
        veft(i) = (sqrt(rft(i)**2 + cft(i)**2))
222     continue

        do 319 i =1,nmax
        if (rft(i).gt.1.0E-09) go to 329
        temp  = -1.0*rft(i)
        if (temp.gt.1.0E-09) go to 329
        if (cft(i).gt.1.0*10**-9) go to 324
        temp = -1.0*cft(i)
        if (temp.gt.1.0*10.0**-9) go to 323
        vpft(i) = 5.0
        go to 326
324     vpft(i) = -90.0
        go to 326
323     vpft(i) = 90.0
        go to 326
329     radan = atan2(-cft(i),rft(i))
        vpft(i) = (180.0/pi) * radan
326     continue
319     continue

        write(6,355)
        write(26,355)
355     format(1x,'Sample',4x,'Real Vin',2x,'Im Vin',
     1     4x,'Freq',6x,'Mag Freq',6x,'Phase')


        do 352 j = 1,16
        i = kk(j)
        fr(i) = (i-1)*delf
        if (fr(i)-fmax) 366,366,361
361     k = i - nmax/2 - 1
        fr(i) = -1.0*(fmax-(k*delf))
366     continue
        write(26,301) i,zo(i),fr(i),veft(i),vpft(i)
301     format(2x,i5,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
352     continue

        do 385 j = 1,16
        i = kk(j)
        fr(i) = (i-1)*delf
        if (fr(i)-fmax) 390,390,393
393     k = i - nmax/2 - 1
        fr(i) = -1.0*(fmax-(k*delf))
390     continue
        write(6,395) i,zo(i),fr(i),veft(i),vpft(i)
395     format(2x,i5,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
385     continue


c-----------------------------------------------------------------------
c
c                       2. Find FFT of cin
c
c-----------------------------------------------------------------------

c       cvar4(i) MUST be cin

        do 413 i = 1,nmax
        ax = cvar4(i)
        bx = y(i)
        zo(i) = cmplx(ax,bx)
413     continue

        do 436 i = 1,nmax
c       x(i,1) = zo(i)
        ftest(i) = real(zo(i))
436     continue
        write(6,431)
        write(26,431)
431     format(25x,'FFT of Iin - NO filter used')

c-------------------------------------------------------------

c       call fft(x,nmax,-1)

c       need scaling factor for width of pulse

c       do 420 i = 1,nmax
c       rft(i)= real(x(i,1))
c       cft(i) = aimag(x(i,1))
c       ceft(i) = sqrt(rft(i)**2+cft(i)**2)/nmax
c       cpft(i) = atan(cft(i)/rft(i))
c420    continue

c-------------------------------------------------------------

        call fht(ftest,nmax)

        ffht(1) = ftest(1)/(nmax**.5)
        rft(1) = (ftest(1) + ftest(1))/(2*(nmax**.5))
        cft(1) = 0
        ceft(1) = (sqrt(rft(1)**2 + cft(1)**2))
        do 422 i= 2,nmax
        k = i-2
        ffht(i) = ftest(i)/(nmax**.5)
        rft(i) = (ftest(i) + ftest(nmax - k))/(2*(nmax**.5))
        cft(i) = (ftest(i) - ftest(nmax - k))/(2*(nmax**.5))
        ceft(i) = (sqrt(rft(i)**2 + cft(i)**2))
422     continue

        do 419 i =1,nmax
        if (rft(i).gt.1.0E-09) go to 429
```


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ndfft.for

```
      temp = -1.0*rft(i)
      if (temp.gt.1.0E-09) go to 429
      if (cft(i).gt.1.0*10**-9) go to 424
      temp = -1.0*cft(i)
      if (temp.gt.1.0*10.0**-9) go to 423
      cpft(i) = 5.0
      go to 426
424   cpft(i) = -90.0
      go to 426
423   cpft(i) = 90.0
      go to 426
429   radan = atan2(-cft(i),rft(i))
      cpft(i) = (180.0/pi) * radan
426   continue
419   continue

      write(6,455)
      write(26,455)
455   format(1x,'Sample',4x,'Real Iin',2x,'Im Iin',
     1   4x,'Freq',6x,'Mag Freq',6x,'Phase')


      do 452 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 466,466,461
461   k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
466   continue
      write(26,401) i,zo(i),fr(i),ceft(i),cpft(i)
401   format(2x,15,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
452   continue

      do 485 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 490,490,493
493   k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
490   continue
      write(6,495) i,zo(i),fr(i),ceft(i),cpft(i)
495   format(2x,15,3x,1pe10.3,1x,f4.2,3(2x,1pe10.3))
485   continue

cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c              Calculation of Zin = FFT(vin)/FFT(cin)
c
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

      do 505 i = 1,nmax
      if (ceft(i).GT.1.0*10**-12) go to 510
      zeft(i) = 100.0*10.0**3
      go to 507
510   zeft(i) = veft(i)/ceft(i)
507   zpft(i) = vpft(i) - cpft(i)
505   continue

      write(6,531)
      write(26,531)
531   format(25x,'Zin(f) - No Filter')


      write(6,555)
      write(26,555)
555   format(6x,'Sample',4x,'Freq',6x,'Mag Freq',3x,'Phase')

      do 552 i = 1,10
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 566,566,565
565   k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
566   continue
      write(26,501) i,fr(i),zeft(i),zpft(i)
501   format(1x,110,3(2x,1pe10.3))
552   continue

      do 560 i = 98,105
      fr(i) = (i-1)*delf
      write(26,501) i,fr(i),zeft(i),zpft(i)
560   continue

      do 561 i = 199,205
      fr(i) = (i-1)*delf
      write(26,501) i,fr(i),zeft(i),zpft(i)
561   continue

      do 562 i = 299,305
      fr(i) = (i-1)*delf
      write(26,501) i,fr(i),zeft(i),zpft(i)
562   continue

      do 563 i = 399,405
      fr(i) = (i-1)*delf
      write(26,501) i,fr(i),zeft(i),zpft(i)
563   continue

      do 564 i = 499,505
      fr(i) = (i-1)*delf
      write(26,501) i,fr(i),zeft(i),zpft(i)
564   continue

      do 585 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 590,590,593
593   k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
590   continue
      write(6,595) i,fr(i),zeft(i),zpft(i)
595   format(1x,110,3(2x,1pe10.3))
585   continue


c      3RD WRITING ON FILE FOR011.DAT
c      writing on disk 11 to be read by fplot.for
c      which will plot the sampled time signal and
c      the amplitude and phase of FFT

c      write(11,506) nmax, delf,delt
c506   format(5x,16,e12.3,2x,e15.4)

c      do 530 i = 1,nmax
c      write(11,535) t(i),zin(i),vin(i),fr(i),zeft(i),zpft(i)
c535   format(5x,1pe16.6,2(1pe10.3,2x),e12.3,2(2x,1pe10.3))
c530   continue
```

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ndfft.for

```
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c                       End of zin
c
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
        go to 230


c-------------------------------------------------------------------------------
c
c       For calculation of zload
c                       1. Find FFT of vload
c
c-------------------------------------------------------------------------------


206     continue

        kk(1) = 1
        kk(2) = 2
        kk(3) = nlo
        kk(4) = nlo + 1
        kk(5) = nlo + 2
        kk(6) = 2*nlo
        kk(7) = 2*nlo + 1
        kk(8) = 2*nlo + 2
        kk(9) = 3*nlo + 1
        kk(10) = 4*nlo + 1
        kk(11) = 5*nlo + 1
        kk(12) = 6*nlo + 1
        kk(13) = 7*nlo + 1
        kk(14) = 8*nlo + 1
        kk(15) = 9*nlo + 1
        kk(16) = 10*nlo + 1

        do 813 i = 1,nmax
        ax = vo(i)
        bx = y(i)
        zo(i) = cmplx(ax,bx)
813     continue

        do 836 i = 1,nmax
c       x(i,1) = zo(i)
        ftest(i) = real(zo(i))
836     continue
        write(6,831)
        write(27,831)
831     format(25x,'FFT of Vload - NO filter used')

ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c       call fft(x,nmax,-1)

c       need scaling factor for width of pulse

c       do 820 i = 1,nmax
c       rft(i)= real(x(i,1))
c       cft(i) = aimag(x(i,1))
c       veft(i) = sqrt(rft(i)**2+cft(i)**2)/nmax
c       radan = atan2(cft(i),rft(i))
c       vpft(i) = (180.0/pi) * radan
c820    continue
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

        call fht(ftest,nmax)

        ffht(1) = ftest(1)/(nmax**.5)
        rft(1) = (ftest(1) + ftest(1))/(2*(nmax**.5))
        cft(1) = 0
        veft(1) = (sqrt(rft(1)**2 + cft(1)**2))
        do 822 i= 2,nmax
        k = i-2
        ffht(i) = ftest(i)/(nmax**.5)
        rft(i) = (ftest(i) + ftest(nmax - k))/(2*(nmax**.5))
        cft(i) = (ftest(i) - ftest(nmax - k))/(2*(nmax**.5))
        veft(i) = (sqrt(rft(i)**2 + cft(i)**2))
822     continue

        do 819 i =1,nmax
        if (rft(i).gt.1.0E-09) go to 829
        temp  = -1.0*rft(i)
        if (temp.gt.1.0E-09) go to 829
        if (cft(i).gt.1.0*10**-9) go to 824
        temp = -1.0*cft(i)
        if (temp.gt.1.0*10.0**-9) go to 823
        vpft(i) = 5.0
        go to 826
824     vpft(i) = -90.0
        go to 826
823     vpft(i) = 90.0
        go to 826
829     radan = atan2(-cft(i),rft(i))
        vpft(i) = (180.0/pi) * radan
826     continue
819     continue

        write(6,855)
        write(27,855)
855     format(1x,'Sample',4x,'Real Vo',3x,'Im Vo',
     1     5x,'Freq',6x,'Mag Freq',4x,'Phase')


        do 852 j = 1,16
        i = kk(j)
        fr(i) = (i-1)*delf
        if (fr(i)-fmax) 866,866,861
861     k = i - nmax/2 - 1
        fr(i) = -1.0*(fmax-(k*delf))
866     continue
        write(27,801) i,zo(i),fr(i),veft(i),vpft(i)
801     format(2x,i5,3x,1pe10.3,1x,f4.2,
     1    2x,1pe10.3,2x,1pe10.3,2x,1pe10.3)
852     continue

        do 885 j = 1,16
        i = kk(j)
        fr(i) = (i-1)*delf
        if (fr(i)-fmax) 890,890,898
898     k = i - nmax/2 - 1
        fr(i) = -1.0*(fmax-(k*delf))
890     continue
        write(6,895) i,zo(i),fr(i),veft(i),vpft(i)
895     format(2x,i5,3x,1pe10.3,1x,f4.2,
     1    2x,1pe10.3,2x,1pe10.3,2x,1pe10.3)
885     continue


c-------------------------------------------------------------------------------
c
```


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ndfft.for 14

```
c
c                    2. Find FFT of cload, total current in the load
c-----------------------------------------------------------------------
c     cvars(i) MUST be cload, total current in the load
      do 913 i = 1,nmax
      ax = cvars(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
913   continue
      do 936 i = 1,nmax
      x(i,1) = zo(i)
c     ftest(i) = real(zo(i))
936   continue
      write(6,93:)
      write(27,931)
931   format(25x,'FFT of Iload - NO filter used')
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c     call fft(x,nmax,-1)
c
c     Need scaling factor for width of pulse
c
      do 920 i = 1, nmax
      fft(i) = real(x(i,1))
c     cft(i) = aimag(x(i,1))
c     ceft(i) = sqrt(fft(i)**2+cft(i)**2)/nmax
c     radan = atan2(cft(i),fft(i))
c     cpft(i) = (180.0/pi) * radan
c920  continue
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
      call fht(ftest,nmax)
      fft(1) = ftest(1)/(nmax**.5)
      fft(i) = (ftest(i) + ftest(i))/(2*(nmax**.5)
      cft(1) = 0
      ceft(1) = (sqrt(fft(1)**2 + cft(1)**2))
      do 922 i= 2,nmax
      k = i-2
      fht(i) = ftest(i)/(nmax**.5)
      fft(i) = (ftest(i) + ftest(nmax - k))/(2*(nmax**.5))
      cft(i) = (ftest(i) - ftest(nmax - k))/(2*(nmax**.5))
      ceft(i) = (sqrt(fft(i)**2 + cft(i)**2))
922   continue

      do 919 i =1,nmax
      if (fft(i).gt.1.0E-09) go to 929
      temp = -1.0*fft(i)
      if (temp.gt.1.0E-09) go to 929
      temp = -1.0*cft(i)
      if (temp.gt.1.0*10.0**-9) go to 924
      if (temp.gt.1.0*10.0**-9) go to 923
      cpft(i) = 5.0
      go to 926
924   cpft(i) = -90.0
      go to 926
923   cpft(i) = 90.0
      go to 926
929   radan = atan2(-cft(i),fft(i))
      cpft(i) = (180.0/pi) * radan
926   continue
919   continue
      write(6,955)
      write(27,955)
955   format(1x,'Sample',4x,'Real Vo',3x,'Im Vo',
     1   5x,'Freq',6x,'Mag Freq',4x,'Phase')

      do 952 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 966,966,961
961   k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
966   continue
      write(27,901) i,zo(i),fr(i),ceft(i),cpft(i)
901   format(2x,i5,3x,1pe10.3,1x,f4.2,
     1   2x,1pe10.3,2x,1pe10.3,2x,1pe10.3)
952   continue

      do 985 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 990,990,993
993   k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
990   continue
      write(6,995) i,zo(i),fr(i),ceft(i),cpft(i)
995   format(2x,i5,3x,1pe10.3,1x,f4.2,
     1   2x,1pe10.3,2x,1pe10.3,2x,1pe10.3)
      continue
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c                    Calculation of Zload = FFT(Vload)/FFT(Iload)
c
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

      do 1005 i = 1,nmax
      if (ceft(i).gt.1.0*10**-12) go to 1010
      zeft(i) = 100.0*10.0**3
      go to 1007
1010  zeft(i) = veft(i)/ceft(i)
1007  zpft(i) = vpft(i) - cpft(i)
1005  continue
      write(6,1031)
      write(27,1031)
1031  format(25x,'Zload(f) - No Filter')
      write(6,1055)
      write(27,1055)
1055  format(6x,'Sample',4x,'Freq',6x,'Mag Freq',5x,'Phase')

      do 1052 i = 1,nmax/8
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1066,1066,1061
1061  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1066  continue
      write(27,1001) i,fr(i),zeft(i),zpft(i)
1001  format(1x,110,3(2x,1pe10.3))
1052  continue
```

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ndfft.for

```
      do 1085 j = 1,16
      i = kk(j)
      fr(i) = (i-1)*delf
      if (fr(i)-fmax) 1090,1090,1093
1093  k = i - nmax/2 - 1
      fr(i) = -1.0*(fmax-(k*delf))
1090  continue
      write(6,1095) i,fr(i),zeft(i),zpft(i)
1095  format(1x,i10,3(2x,1pe10.3))
1085  continue

C     3RD WRITING ON FILE FOR011.DAT
C     writing on disk 11 to be read by fplot.for
C     which will plot the sampled time signal and
C     the amplitude and phase of FFT

      write(11,1006) nmax, delf,delt
c1006 format(5x,i6,e12.3,2x,e15.4)

c     do 1030 i = 1,nmax
c     write(11,1035) t(i),zin(i),vin(i),fr(i),zeft(i),zpft(i)
c1035 format(5x,1pe16.6,2(1pe10.3,2x),e12.3,2(2x,1pe10.3))
c1030 continue

ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

c
c                End of Zload
c
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

c-----------------------------------------------------------------------
c
c     For calculation of zin at diode
c          Useful for a BALANCED MIXER
c               1. Find FFT of vin
c
c-----------------------------------------------------------------------
207   continue
      kk(1) = 1
      kk(2) = 2
      kk(3) = nlo
      kk(4) = nlo + 1
      kk(5) = nlo + 2
      kk(6) = 2*nlo
      kk(7) = 2*nlo + 1
      kk(8) = 2*nlo + 2
      kk(9) = 3*nlo + 1
      kk(10) = 4*nlo + 1
      kk(11) = 5*nlo + 1
      kk(12) = 6*nlo + 1
      kk(13) = 7*nlo + 1
      kk(14) = 8*nlo + 1
      kk(15) = 9*nlo + 1
      kk(16) = 10*nlo + 1
      do 2313 i = 1,nmax
      ax = vdiod(i) + vo(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
2313  continue

      do 2336 i = 1,nmax
      x(i,1) = zo(i)
      ftest(i) = real(zo(i))
2336  continue
      write(6,2331)
      write(31,2331)
2331  format(25x,'FFT of Vd+Vout - NO filter used')

c-----------------------------------------------------------------------
      call fft(x,nmax,-1)
c     need scaling factor for width of pulse

      do 2320 i = 1,nmax
      cft(i) = real(x(i,1))
      cft(i) = aimag(x(i,1))
      veft(i) = sqrt(cft(i)**2+cft(i)**2)/nmax
      vpft(i) = atan(cft(i)/cft(i))
c2320 continue
c-----------------------------------------------------------------------

      call fht(ftest,nmax)

      fht(1) = ftest(1)/(nmax**.5)
      rft(1) = (ftest(1) + ftest(1))/(2*(nmax**.5))
      cft(1) = 0
      veft(1) = (sqrt(rft(1)**2 + cft(1)**2))
      do 2222 i= 2,nmax
      k = i-2
      fht(i) = ftest(i)/(nmax**.5)
      rft(i) = ((ftest(i) + ftest(nmax - k))/(2*(nmax**.5))
      cft(i) = (ftest(i) - ftest(nmax - k))/(2*(nmax**.5))
      veft(i) = (sqrt(rft(i)**2 + cft(i)**2))
2222  continue

      do 2319 i =1,nmax
      if (rft(i).gt.1.0E-09) go to 2329
      temp = -1.0*rft(i)
      if (temp.gt.1.0E-09) go to 2329
      if (cft(i).gt.1.0*10**-9) go to 2324
      temp = -1.0*cft(i)
      if (temp.gt.1.0*10.0**-9) go to 2323
      vpft(i) = 5.0
      go to 2326
2324  vpft(i) = -90.0
      go to 2326
2323  vpft(i) = 90.0
      go to 2326
2329  radan = atan2(-cft(i),rft(i))
      vpft(i) = (180.0/pi) * radan
2326  continue
2319  continue

      write(6,2355)
      write(31,2355)
2355  format(11x,'Sample',4x,'Real Vd+Vout',2x,'Im Vd+Vout',
     1     4x,'Freq',6x,'Mag Freq',6x,'Phase')
```


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[redacted]

ndfft.for

```
      do 2352 j = 1,16
      l = kk(j)
      fr(l) = (l-1)*delf
      if (fr(l)-fmax) 2366,2366,2361
2361  k = l - nmax/2 - 1
      fr(l) = -1.0*(fmax-(k*delf))
2366  continue
      write(31,2301) l,zo(l),fr(l),vpfc(l),ypfc(l)
2301  format(2x,i5,3x,ipe10.3,1x,f4.2,3(2x,ipe10.3))
2352  continue

      do 2385 j = 1,16
      l = kk(j)
      fr(l) = (l-1)*delf
      if (fr(l)-fmax) 2390,2390,2393
2393  k = l - nmax/2 - 1
      fr(l) = -1.0*(fmax-(k*delf))
2390  continue
      write(6,2395) l,zo(l),fr(l),vpfc(l),ypfc(l)
2395  format(2x,i5,3x,ipe10.3,1x,f4.2,3(2x,ipe10.3))
2385  continue

c-----------------------------------------------------------------
c
c                    2. Find FFT of cdiod
c
c-----------------------------------------------------------------

      do 2413 i = 1,nmax
      ax = cdiod(i)
      bx = y(i)
      zo(i) = cmplx(ax,bx)
2413  continue

      do 2436 i = 1,nmax
c     x(i,1) = zo(i)
      freqc(i) = real(zo(i))
2436  continue
      write(6,2431)
      write(31,2431)
2431  format(25x,'FFT of idiode - NO filter used')

c-----------------------------------------------------------------

c     call fft(x,nmax,-1)

c     need scaling factor for width of pulse

c     do 2420 i = 1,nmax
c     rfc(i)= real(x(i,1))
c     cfc(i) = aimag(x(i,1))
c     cpfc(i) = sqrt(rfc(i)**2+cfc(i)**2)/nmax
c     cpfc(i) = atan(cfc(i)/rfc(i))
c2420 continue

c-----------------------------------------------------------------

      call fht(freqc,nmax)

      fft(1) = freqc(1)/(nmax**.5)
      rfc(1) = (freqc(1) + freqc(1))/(2*(nmax**.5))
      cfc(1) = 0
      cefc(1) = (sqrt(rfc(1)**2 + cfc(1)**2))
      do 2422 i = 2,nmax
      k = i-2
      fht(i) = freqc(i)/(nmax**.5)
      rfc(i) = (freqc(i) + freqc(nmax - k))/(2*(nmax**.5))
      cfc(i) = (freqc(i) - freqc(nmax - k))/(2*(nmax**.5))
2422  cefc(i) = (sqrt(rfc(i)**2 + cfc(i)**2))
      do 2419 i =1,nmax
      if (rfc(i).gt.1.0E-09) go to 2429
      temp = -1.0*rfc(i)
      if (temp.gt.1.0E-09) go to 2429
      if (cfc(i).gt.1.0*10**-9) go to 2424
      temp = -1.0*cfc(i)
      if (temp.gt.1.0*10.0**-9) go to 2423
      cpfc(i) = 5.0
      go to 2426
2424  cpfc(i) = -90.0
      go to 2426
2423  cpfc(i) = 90.0
      go to 2426
2429  radan = atan2(-cfc(i),rfc(i))
      cpfc(i) = (180.0/pi) * radan
2426  continue
2419  continue

      write(6,2455)
      write(31,2455)
2455  format(1x,'Sample',4x,'Real Idiode',2x,'Im Idiode',
     1       4x,'Freq',6x,'Mag Freq',6x,'Phase')

      do 2452 j = 1,16
      l = kk(j)
      fr(l) = (l-1)*delf
      if (fr(l)-fmax) 2466,2466,2461
2461  k = l - nmax/2 - 1
      fr(l) = -1.0*(fmax-(k*delf))
2466  continue
      write(31,2401) l,zo(l),fr(l),cefc(l),cpfc(l)
2401  format(2x,i5,3x,ipe10.3,1x,f4.2,3(2x,ipe10.3))
2452  continue

      do 2485 j = 1,16
      l = kk(j)
      fr(l) = (l-1)*delf
      if (fr(l)-fmax) 2490,2490,2493
2493  k = l - nmax/2 - 1
      fr(l) = -1.0*(fmax-(k*delf))
2490  continue
      write(6,2495) l,zo(l),fr(l),cefc(l),cpfc(l)
2495  format(2x,i5,3x,ipe10.3,1x,f4.2,3(2x,ipe10.3))
2485  continue

ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c                  Calculation of Zin = FFT(vdiode+vout)/FFT(idiode)
c                                       at diode
c
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

      do 2505 i = 1,nmax
      if (cefc(i).GT.1.0*10**-12) go to 2510
```


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```
        zeft(i) = 100.0*10.0**3
        go to 2507
2510    zeft(i) = veft(i)/ceft(i)
2507    zpft(i) = vpft(i) - cpft(i)
2505    continue

        write(6,2531)
        write(31,2531)
2531    format(25x,'Zin(f) at diode - No Filter')


        write(6,2555)
        write(31,2555)
2555    format(6x,'Sample',4x,'Freq',6x,'Mag Freq',3x,'Phase')

        do 2552 i = 1,10
        fr(i) = (i-1)*delf
        if (fr(i)-fmax) 2566,2566,2565
2565    k = i - nmax/2 - 1
        fr(i) = -1.0*(fmax-(k*delf))
2566    continue
        write(31,2501) i,fr(i),zeft(i),zpft(i)
2501    format(1x,i10,3(2x,1pe10.3))
2552    continue

        do 2560 i = 98,105
        fr(i) = (i-1)*delf
        write(31,2501) i,fr(i),zeft(i),zpft(i)
2560    continue

        do 2561 i = 199,205
        fr(i) = (i-1)*delf
        write(31,2501) i,fr(i),zeft(i),zpft(i)
2561    continue

        do 2562 i = 299,305
        fr(i) = (i-1)*delf
        write(31,2501) i,fr(i),zeft(i),zpft(i)
2562    continue

        do 2563 i = 399,405
        fr(i) = (i-1)*delf
        write(31,2501) i,fr(i),zeft(i),zpft(i)
2563    continue

        do 2564 i = 499,505
        fr(i) = (i-1)*delf
        write(31,2501) i,fr(i),zeft(i),zpft(i)
2564    continue

        do 2585 j = 1,16
        i = kk(j)
        fr(i) = (i-1)*delf
        if (fr(i)-fmax) 2590,2590,2593
2593    k = i - nmax/2 - 1
        fr(i) = -1.0*(fmax-(k*delf))
2590    continue
        write(6,2595) i,fr(i),zeft(i),zpft(i)
2595    format(1x,i10,3(2x,1pe10.3))
2585    continue


c       3RD WRITING ON FILE FOR011.DAT
c       writing on disk 11 to be read by fplot.for
```

ndfft.for

```
c       which will plot the sampled time signal and
c       the amplitude and phase of FFT

c       write(11,2506) nmax, delf,delt
c2506   format(5x,i6,e12.3,2x,e15.4)


c       do 2530 i = 1,nmax
c       write(11,2535) t(i),zin(i),vin(i),fr(i),zeft(i),zpft(i)
c2535   format(5x,1pe16.6,2(1pe10.3,2x),e12.3,2(2x,1pe10.3))
c2530   continue

ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c                       End of Zin
c
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
        go to 230



230     continue

        write(6,260)
260     format(5x,'Do you want to get another FFT or EXIT?',
     1    5x,/,15x,'<FFT or EXIT>?  Type <0,1>')
        accept *, finans

        if (finans.LE.0) go to 209

        close(24)


        stop
        end




        subroutine data(nmax,clo,t,vo,cdiod,
     1          vdiod,cvar4,vin,cvar5,cvar1,cvar2,cvar3,csc,delt)

        dimension idum(80)
        dimension vo(20000),t(20000),vdiod(20000),cdiod(20000)
        dimension cvar4(20000),vin(20000),cvar1(20000),cvar2(20000)
        dimension cvar3(20000),cvar5(20000)
        dimension tt(20000),coc(20000),csc(20000),deltc(20000)
        dimension wt(20000),vwt(20000)

c       do 2 i = 1, number of lines want to skip
c       read(34,9) idum(80)
c9      format(1x,80a1)
c2      continue

        do 3 i = 1,nmax+1
        read(34,5) t(i),vo(i),cdiod(i),vdiod(i),cvar4(i),vin(i),
c     1          cvar1(i),cvar2(i),cvar3(i)
     1          cvar5(i),cvar2(i),cvar3(i)
5       format(1x,1pe9.3,4x,1pe10.3,7(2x,1pe10.3))
c5      format(1x,1pe10.3,4x,1pe12.5,2x,1pe12.5)
3       continue

        write(6,17) t(i),vo(i),cdiod(i),vdiod(i),cvar4(i),vin(i),
     1          cvar5(i),cvar2(i),cvar3(i)
```


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ndfft.for

```
      write(22,117) t(1),vo(1),cdlod(1),vdlod(1),cvar4(1),vin(1),
     1    cvar5(1),cvar2(1),cvar3(1)
      write(29,17) t(1),vo(1),cdlod(1),vdlod(1),cvar4(1),vin(1),
     1    cvar5(1),cvar2(1),cvar3(1)
17    format(2x,1pe10.3,4x,4(1pe10.3,2x),/,4x,4(1pe10.3,2x))

      write(6,19) t(nmax),vo(nmax),cdlod(nmax),vdlod(nmax),cvar4(nmax),
     1    vin(nmax),cvar5(nmax),cvar2(nmax),cvar3(nmax)
      write(22,19) t(nmax),vo(nmax),cdlod(nmax),vdlod(nmax),cvar4(nmax),
     1    vin(nmax),cvar5(nmax),cvar2(nmax),cvar3(nmax)
      write(29,19) t(nmax),vo(nmax),cdlod(nmax),vdlod(nmax),cvar4(nmax),
     1    vin(nmax),cvar5(nmax),cvar2(nmax),cvar3(nmax)
19    format(2x,1pe10.3,4x,4(1pe10.3,2x),/,4x,4(1pe10.3,2x))

c     check that vo(1) - vo(nmax+1)

      diff - vo(1)-vo(nmax+1)
      write(6,11) vo(1),vo(nmax+1),diff
      write(22,11) vo(1),vo(nmax+1),diff
      write(29,11) vo(1),vo(nmax+1),diff
11    format(5x,'Vl =',1pe10.3,/,5x,'VNmax+1 =',1pe10.3,/,
     1  5x,'Diff =',1pe10.3)

c     find delta T

      delt = (t(nmax)-t(1))/(nmax-1)
      write(6,21)delt
c21   format(5x,'Delta t calculated is ',1pe10.3,
c    1   1x,/,1x,'Do you want to change value? yes,no:<0,1>')
c     accept *, tans

      tans - 1

      If (tans.GE.1.0) go to  30

      write(6,33)
33    format(5x,'Enter exact value')
      accept *,delt
30    continue
      type *,delt

c     write(6,22) t(1),t(nmax)
c22   format(5x,'T(1) is ',1pe10.3,8x,'T(nmax) is',1pe10.3,
c    1   1x,/,1x,'Do you want to change value of T(1)? yes,no:<0,1>')
c     accept *, tans2

      tans2 - 1

      If (tans2.GE.1.0) go to 40
      write(6,43)
43    format(5x,'Enter exact value of T(1)')
      accept *,t(1)
40    continue
      type *,t(1)


c     do 103 i - 1,nmax+1
c105  read(36,105) tt(i),coc(i),csc(i)
c     format(1x,1pe9.3,4x,1pe10.3,2x,1pe10.3)
c103  continue

c     write(6,117) tt(1),coc(1),csc(1)
```



```
c     write(22,117) tt(1),coc(1),csc(1)
c117  format(2x,1pe10.3,4x,2(1pe10.3,2x))

c     find delta T of this second run

      deltt = (tt(nmax)-tt(1))/(nmax-1)
      write(6,121)deltt
c121  format(5x,'New Delta t calculated is ',1pe10.3,
     1   1x,/,1x,'Do you want to change value? yes,no:<0,1>')
c     accept *, tans

c     If (tans.GE.1.0) go to  130

c133  write(6,133)
      format(5x,'Enter exact value')
      accept *,deltt
      continue
c130  type *,deltt

c     check that coc and cstor are close - where cstor(1) IS cvar4(1)

      close - clo/100.0

      do 175 i - 1,nmax
      deltc(i) - abs(cvar4(1) - coc(i)
      If (deltc(i).GT.close) go to 180
      go to 185
c180  continue
      write(6,192)
      write(6,192)
c192  format(10x,'I',8x,'Delt Current,')

      write(6,187) i,deltc(i)
c187  write(22,187) i,deltc(i)
c185  format(10x,i5,5x,1pe10.3)
c175  continue

      do 25 i - 2,nmax
      k - i-1
25    t(i) - t(i) + k*deltt
      continue

      deltf - 1.0/(deltt*nmax)

c     to reduce sidebands and ensure that vo(1)-vo(nmax+1)-0
c     we pass the data through a cos filter

      pi - 3.1415926
      do 23 i - 1,nmax+1
      k - i-2
      ttime - k*deltt
      wt(i) - (pi/2.0)*sin(pi*deltf*ttime)
      vwt(i) - vo(1) * wt(i)
23    continue


c     check that vwt(1) - vwt(nmax+1)

      diff - vwt(1)-vwt(nmax+1)
      write(6,27) vwt(1),vwt(nmax+1),diff
      write(22,27) vwt(1),vwt(nmax+1),diff
c27   format(5x,'Vwt1 =',1pe10.3,/,5x,'VwtNmax+1 =',1pe10.3,/,
     1   5x,'Diff =',1pe10.3)
c
```

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```
      return
      end


      subroutine avpw(nmax,vo,cdiod,vdiod,cvar4,vin,
     1          cvar1,cvar2,cvar3,rs,rl,
     1          apwrs,apwrl,apwd,apwdrl,apwib,apwirf,apwilo)


c     calculates average power consumed by resistors and diode

      dimension vo(20000),cdiod(20000),vdiod(20000),cvar4(20000)
      dimension vin(20000),cvar1(20000)
      dimension cvar2(20000),cvar3(20000)

      apwrs = 0
      apwrl = 0
      apwd = 0
      apwib = 0
      apwirf = 0
      apwilo = 0

c     Variable named cvar1, here, is really ibias.
c     For the case of series inductor, cvar2, is Voltage
c                    from source to diode

      do 150 i = 1,nmax
      vrs = vin(i) + cvar2(i)
      apwrs = (vrs**2)/rs + apwrs
c     apwrs = (vin(i)**2)/rs + apwrs
      apwrl = (vo(i)**2)/rl + apwrl
      apwd = cdiod(i)*vdiod(i) + apwd
      apwib = (cvar1(i)*vin(i)) + apwib
      apwirf = (cvar2(i)*vin(i)) + apwirf
      apwilo = (cvar3(i)*vin(i)) + apwilo
150   continue


      apwrs = apwrs/nmax
      apwrl = apwrl/nmax
      apwd = apwd/nmax
      apwdrl = apwd + apwrl

      apwib = apwib/nmax
      apwirf = apwirf/nmax
      apwilo = apwilo/nmax

      return
      end


      subroutine diostate(nmax,t,cdiod,vdiod,cmax,cmin,vmax,vmin,
     1            ton,toff,tlin,tton)

      dimension t(20000),cdiod(20000),vdiod(20000)

      cmax = cdiod(1)
      do 300 i = 2,nmax
      if (cdiod(i).le.cmax) go to 310
      cmax = cdiod(i)
310   continue
300   continue
```

ndfft.for

```
      cmin = cdiod(1)
      do 305 i = 2,nmax
      if (cdiod(i).ge.cmin) go to 315
      cmin = cdiod(i)
315   continue
305   continue

      vmax = vdiod(1)
      do 350 i = 2,nmax
      if (vdiod(i).le.vmax) go to 360
      vmax = vdiod(i)
360   continue
350   continue

      vmin = vdiod(1)
      do 355 i = 2,nmax
      if (vdiod(i).ge.vmin) go to 365
      vmin = vdiod(i)
365   continue
355   continue

      delt = (t(nmax)-t(1))/(nmax-1)

c     type *, t(nmax), t(1)
c     type *, delt

      ton = 0.0
      toff = 0.0
      tlin = 0.0
      do 400 i = 1,nmax
      if(vdiod(i).lt.0.50) toff=delt+toff
      if(vdiod(i).ge.0.50.AND.vdiod(i).le.0.65) ton=delt+ton
      if(vdiod(i).gt.0.65) tlin=delt+tlin
400   continue

      ttotal = t(nmax) - t(1)
      ton = (ton/ttotal)
      toff = (toff/ttotal)
      tlin = (tlin/ttotal)
      tton = ton + tlin

      return
      end

      subroutine fft (x,nsamp,signl)
c
c  fast fourier transform routine
c
c  emaciation in time
c  input, output in normal order, not calculated in place
c  for flow graph, see Oppenheim and Schaefer, fig. 6.13
c
c  calling sequence:
c       x = complex data (20000 pts. max)
c          data goes into x(n,1)
c          results come back in x(n,1)
c          x(n,2) is used as a working register
c   nsamp = no. of points (N)
c   signl = type of transform (integer)
c       -1 => forward transform
c       +1 => inverse transform (normalizes by N)
c
      complex x(nsamp,2),w(10000),z,cmplx
```


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ndfft.for

```
      Integer r,sign1
c
c     set up constants
c
      n=nsamp
      n2=n/2
      fltn=float(n)
      lnsam=alog(fltn)/alog(2.)
      ph12n=6.28318531/fltn
c
c     set up complex exponentials
c
      do 5 m=1,n2
        w(m) = cexp(cmplx(0., (m-1)*sign1*ph12n))
5     continue
c
c     and away we go
c
      do 3 j=1,lnsam
      n2j=n/(2**j)
      nr=n2j
      nl=(2**j)/2
      do 2 l=1,nl
        ln2j=(l-1)*n2j
        m=ln2j+1
        do 2 r=1,nr
c
c     subscript jockeying
c
          isub=r+ln2j
          isub1=r+ln2j+2
          isub2=isub1+n2j
          isub3=isub1n2
c
c     basic butterfly calculation -> intermediate array
c
          z=w(m)*x(isub2,1)
          x(isub2,2)=x(isub),1)+z
          x(isub3,2)=x(isub),1)-z
2     continue
c
c     update source array
c
      do 3 r=1,n
        x(r,1)=x(r,2)
3     continue
c
c     divide by N for inverse transform
c
      if(sign1.lt.0) return
      do 4 r=1,n
        x(r,1)=x(r,1)/fltn
4     continue
      return
      end
```


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zout.for

```
C                              ZOUT.FOR
C
C     This program calculates Zout from output of DFFT.for
C     for 2 spice runs.
C     Output of DFFT.for - for022.dat -
C     must be stored in Z1.DAT AND Z2.DAT
C
      complex zout(5000)
      complex zv1(5000), zv2(5000), zi1(5000), zi2(5000)
      complex znum,zden,yload1,yload2
C
      dimension vo(5000),vdiod(5000),cdiod(5000)
C
      dimension ltit1(132), ltit2(132)
      dimension ltrash(132)
      dimension idum1(132),idum2(132)
      dimension k(5000), kk(10)
      dimension fr(5000),eft1(5000),pft1(5000)
      dimension eft2(5000),pft2(5000)
      dimension rev1(5000),cmv1(5000)
      dimension rev2(5000),cmv2(5000)
      dimension rmout(5000),rpout(5000)
C
      open(unit=24,file='z1.dat',status='old',readonly)
      open(unit=26,file='z2.dat',status='old',readonly)
C
c     type 105
c105  format(5x,'How many points do you want read?',
c    1   1x,'(More than 506 rec. for ifkeep).',/,10x,'Enter nfreq')
c     accept *,nfreq
      nfreq = 510
C
c     type 108
c108  format(5x,'Enter number of lines to be skipped')
c     accept *,nline
      nline=46
C
c     this lines are to be skipped
      do 103 j = 1,7
      read(24,104) (ltrash(i),i=1,132)
104   format(132a1)
103   continue
C
      read(24,112) (ltit1(i),i=1,132)
112   format(132a1)
C
      write(6,113) (ltit1(i),i=1,80)
      write(28,113) (ltit1(i),i=1,80)
113   format(132a1)
C
      do 110 j = 1,nline
      read(24,109) (idum1(i),i=1,132)
109   format(132a1)
      if (j.gt.4) go to 165
      write(6,111) (idum1(i),i=1,80)
      write(28,111) (idum1(i),i=1,80)
111   format(80a1)
165   continue
110   continue
C
      do 115 i=1,nfreq
      read(24,120) k(i),vo(i),vdiod(i),cdiod(i),fr(i),eft1(i),pft1(i)
120   format(2x,i5,3(2x,1pe10.3),
     1   2x,1pe10.2,2x,1pe10.3,2x,1pe10.3)
115   continue
C
      do 125 j = 1,3
      write(6,130) k(i),vo(i),vdiod(i),cdiod(i),fr(i),eft1(i),pft1(i)
130   format(2x,i5,3(2x,1pe10.3),
     1   2x,1pe10.2,2x,1pe10.3,2x,1pe10.3)
125   continue
C
c     this lines are to be skipped
      do 203 j = 1,7
      read(26,204) (ltrash(i),i=1,132)
204   format(132a1)
203   continue
C
      read(26,212) (ltit2(i),i=1,132)
212   format(132a1)
C
      write(6,213) (ltit2(i),i=1,80)
      write(28,213) (ltit2(i),i=1,80)
213   format(1x,/,80a1)
C
      do 210 j = 1,nline
      read(26,209) (idum2(i),i=1,132)
209   format(132a1)
      if (j.gt.4) go to 265
      write(6,211) (idum2(i),i=1,80)
      write(28,211) (idum2(i),i=1,80)
211   format(80a1)
265   continue
210   continue
C
      do 215 i=1,nfreq
      read(26,220) k(i),vo(i),vdiod(i),cdiod(i),fr(i),eft2(i),pft2(i)
220   format(2x,i5,3(2x,1pe10.3),
     1   2x,1pe10.2,2x,1pe10.3,2x,1pe10.3)
215   continue
C
      do 225 i = 1,2
      write(6,230) k(i),vo(i),vdiod(i),cdiod(i),fr(i),eft2(i),pft2(i)
230   format(2x,i5,3(2x,1pe10.3),
     1   2x,1pe10.2,2x,1pe10.3,2x,1pe10.3)
225   continue
C
      type 107
107   format(2x,/,5x,'Enter R11 and R12 in ohms')
      accept *, r11, r12
C
      type 135
135   format(2x,/,5x,'Enter cload1 and cload2 in UF:',
     1   5x,/,15x,'ie. 5.092 or 0')
      accept *, cc11,cc12
C
      y11 = 1/r11
      y12 = 1/r12
      c11 = cc11* 10.0**-6
      c12 = cc12 * 10.0**-6
C
      pi = 3:141592654
C
      do 320 i = 1, nfreq
      xc1 = 2 * pi * fr(i) * c11
```

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```
      xc2 = 2 * pi * fr(i) * c12
      yload1 = cmplx(y11,xc1)
      yload2 = cmplx(y12,xc2)
      z11(i) = 1/yload1
      z12(i) = 1/yload2
320   continue

      do 305 i = 1,nfreq
      if (eft1(i).le.1.0*10.0**-15) go to 310
      if (eft2(i).le.1.0*10.0**-15) go to 310
      rev1(i) = eft1(i)*cosd(pft1(i))
      cmv1(i) = eft1(i)*sind(pft1(i))
      rev2(i) = eft2(i)*cosd(pft2(i))
      cmv2(i) = eft2(i)*sind(pft2(i))
      zv1(i) = cmplx(rev1(i),cmv1(i))
      zv2(i) = cmplx(rev2(i),cmv2(i))
      znum = z11(i)*z12(i)*(zv1(i)-zv2(i))
      zden = z11(i)*zv2(i)-z12(i)*zv1(i)
      zout(i) = znum/zden
      rmout(i) = cabs(zout(i))
      rrout = real(zout(i))
      crout = aimag(zout(i))
      radan = atan2(crout,rrout)
      rpout(i) = (180.0/pi) * radan
      go to 315
310   zout(i) = cmplx(0.0,0.0)
      rmout(i) = 0.0
      rpout(i) = 0.0
315   continue
305   continue

c     write(6,405) (itit1(i),i=1,80)
c     write(28,405) (itit1(i),i=1,80)
c405  format(15x,30a1)

c     write(6,450)
c     write(28,450)
c450  format(25x,'and')

c     write(6,410) (itit2(i),i=1,80)
c     write(28,410) (itit2(i),i=1,80)
c410  format(15x,30a1)

      write(6,409) r11,r12
      write(28,409) r11,r12
409   format(1x,/,10x,'R11 =',f10.2,6x,'R12 =',f10.2)

      write(6,419) c11,c12
      write(28,419) c11,c12
419   format(1x,/,10x,'Cload1 =',1pe10.3,6x,'Cload2 =',1pe10.3)

      write(6,415)
      write(28,415)
415   format(1x,/,1x,'Sample',6x,'Freq',5x,'V1(f)',4x,'Ph(f)',4x,'V2(f)',
     1          4x,'Ph(f)',4x,'Mag Zout',5x,'Phase')


      kk(1) = 2
      kk(2) = 202
      kk(3) = 102
      kk(4) = 101

      do 455 j = 1,4
      i = kk(j)
```

zout.for

```
      write(6,465) i,fr(i),eft1(i),pft1(i),eft2(i),pft2(i),rmout(i),rpout(i)
465   format(1x,17,1x,1pe10.3,1x,4(1x,1pe8.1),1x,1pe10.3,1x,0pf7.2)
455   continue

      do 420 i = 1,10
      write(28,425) i,fr(i),eft1(i),pft1(i),eft2(i),pft2(i),rmout(i),rpout(i)
425   format(1x,17,1x,1pe10.3,1x,4(1x,1pe8.1),2(1x,1pe10.3))
420   continue

      do 430 j = 1,5
      nstart = (j*100) - 1
      nstop = nstart + 6
      do 435 i = nstart,nstop
      write(28,425) i,fr(i),eft1(i),pft1(i),eft2(i),pft2(i),rmout(i),rpout(i)
435   continue
430   continue

      close(24)
      close(26)


      stop
      end
```


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cjplot.for

```
c                    CJPLOT.FOR

      dimension idum(80),ititle(80)
      dimension vo(4,1000), vdiod(4,1000), cdiod(4,1000)
      dimension vvar3(4,1000)
      dimension t1(1000), t2(1000), t3(1000), t4(1000)
      dimension ymax(4), ymin(4)
      dimension cvar4(1000),cvar1(1000),cvar2(1000)
      dimension cvar3(1000),cstot(1000),cvar5(1000)

      dimension xvar1(1000),xvar2(1000),xvar3(1000)
      dimension xvar4(1000),xvar5(1000),xvar6(1000)
      dimension nstart(4),istart(4),istop(4),idelt(4)
      dimension cdmax(4),qint(4),cavar(4)
      dimension vomax(4),vomin(4),vbat(4)
      dimension af(4),qo(4)
      dimension iintg(4),kintg(4),vjtr1(4),vjtr2(4)

      dimension vj(4,1000),cres(4,1000),ccap(4,1000)
      dimension cbar(4,1000),qcalc(4,1000),qintg(4,1000)
      dimension qic(4,1000), qco(4), qcao(4)

      dimension ccalc(1000),cintg(1000),cic(1000)
      dimension craver(4),crmax(4),sfr(4)
      dimension pdiod(4,1000),pload(4,1000),pmax(4),pmin(4)

      dimension big(6),small(6),bg(6),sm(6)
      dimension y2max(4),y2min(4)

      character*60 MSGLN
      integer*4 imsgln(15)
      character*4 MSGARY(15), name

      open (unit=24,file='m1.dat',status='old',readonly)
      open (unit=25,file='m2.dat',status='old',readonly)
      open (unit=26,file='m3.dat',status='old',readonly)
      open (unit=27,file='m4.dat',status='old',readonly)

      type 71
71    format(5x,'Enter Circuit Name and Run Characteristics')
      read(5,72) (ititle(i),i=1,80)
72    format(80a1)

      type 35
35    format(5x,'Enter Circuit Name ie. ldiod1.dat  $,',
     1         1x,/,20x,'END WITH $   !!!')
      read(5,37) MSGLN
37    format(a60)

      type 86
86    format(5x,'Enter Source and Load Resistance, Rs and Rl',
     1  2x, 'in Kohms:', /,10x, 'eg. 10,10')
      accept *, rrs,rrl

      Rs = rrs*1000.0
      Rl = rrl*1000.0

      type 80
80    format(5x, 'Enter Reactance Value, eg. .318E-06, or 0.0')
      accept *, xreac

c     xreac  = 0.0

      type 73
```

```
73    format(5x,'Enter Ibias on diode, Ilo,and Irf in mA,',
     1  2x,'flo and frf in Hz,',/,1x,' eg. 0,2,.01,500,600')
      accept *, cbma,cloma,crfma,flo,frf

      cbias = cbma * 1.0*10.0**-3
      clo = cloma * 1.0*10.0**-3
      crf = crfma * 1.0*10.0**-3

      type 21
21    format(5x,'Enter diode parameters: rs, Isat, n, phi.',
     1         2x,/,15x,'ie 10.0, 1.0E-14, 1.0, .9')
      accept *, rser, csat, fideal, sphi

c     rser = 10.0
c     csat = 1.0*10.0**-14

      type 74
74    format(5x,'Enter Cjo in UF, ie. .45 or 1.8E-06')
      accept *, cjjo

      cjo = cjjo * 10.0**-6

c     cjo = .45*10.0**-6
c     bktoq = .026

      qcharge = 1.6*10.0**-19
      bk = 1.38 * 10.0**-23

      temp = 300

      bktoq = bk*temp/qcharge

      sphi = .9

      nmax = 500

      nfile = 326

      do 7 i = 1,nfile+1
      read(24,4) t1(i),vo(1,i),cdiod(1,i),vdiod(1,i),cvar4(i),vvar3(1,i),
     1         cvar5(i),cvar1(i),cvar2(i)
      read(25,4) t2(i),vo(2,i),cdiod(2,i),vdiod(2,i),cvar4(i),vvar3(2,i),
     1         cvar5(i),cvar1(i),cvar2(i)
      read(26,4) t3(i),vo(3,i),cdiod(3,i),vdiod(3,i),cvar4(i),vvar3(3,i),
     1         cvar5(i),cvar1(i),cvar2(i)
      read(27,4) t4(i),vo(4,i),cdiod(4,i),vdiod(4,i),cvar4(i),vvar3(4,i),
     1         cvar5(i),cvar1(i),cvar2(i)
4     format(1x,1pe9.3,4x,1pe10.3,7(2x,1pe10.3))
7     continue


      write(6,81) t1(1),vo(1,1),cdiod(1,1),vdiod(1,1),cvar4(1),vvar3(1,1),
     1         cvar5(1),cvar1(1),cvar2(1)
c     1         cvar1(1),cvar2(1),cvar3(1)
      write(6,81) t1(nfile),vo(1,nfile),cdiod(1,nfile),vdiod(1,nfile),
     1         cvar4(nfile),vvar3(1,nfile),cvar5(nfile),cvar1(nfile),
     1         cvar2(nfile)
81    format(2x,1pe10.3,4x,1pe10.3,7(2x,1pe10.3))


c     find delta T

      delt = (t1(nfile)-t1(1))/(nfile-1)
      write(6,22)delt
```


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cjplot.for

```
22      format(5x,'Delta t calculated is ',1pe10.3)

        delt = 12.20703125*10.0**-6
c     1     2x,/,2x,'Enter exact value')
c       accept *, delt
        type *, delt

c       write(6,22) t(1),t(nfile)
c22     format(5x,'T(1) is ',1pe10.3,8x,'T(nfile) is',1pe10.3,
c     1    1x,/,1x,'Do you want to change value? yes,no:<0,1>')
c       accept *, tans2

        tans2 = 1

        if (tans2.GE.1.0) go to 40
        write(6,43)
43      format(5x,'Enter exact value of T(1)')
        accept *,t1(1)
40      continue
c       type *,t1(1)

        do 25 i = 2,nfile
        k = i-1
        t1(i) = t1(1) + k*delt
        t2(i) = t2(1) + k*delt
        t3(i) = t3(1) + k*delt
        t4(i) = t4(1) + k*delt
25      continue

c       delf = 1.0/(delt*nfile)

        pi = 3.14159266


c       Calculating cdiode: Idiode max in cycle, cdmax
c                           sums current over taver, qint
c                           average positive value, caver = qint/ptav*delt


        taulo = 1/flo
        taurf = 1/frf
        taver = taulo
        ptav = taver/delt
        iptav = int(ptav)

        type *, ptav, iptav

c       SETTING NMAX FOR THE GRAPHS

        nmax = 2* iptav

c       vvar3 = vdiode + vload = "vin" used for calculating zin for
c               series L matching circuit. We want to calculate the
c               average value of vvar3 because that is equal to the
c               Battery Voltage required to bias the diode.
c                       Vbatt  depends on LO drive and Bias level on diode


        do 400 j = 1,4

        vomax(j) = 0.0
        do 403 i = 1, iptav+1
        if(vo(j,i).gt.vomax(j)) go to 405
        go to 407
405     vomax(j) = vo(j,i)
407     continue
403     continue

        vomin(j) = vomax(j)
        do 404 i = 1, iptav+1
        if (vo(j,i).lt.vomin(j)) go to 406
        go to 408
406     vomin(j) = vo(j,i)
408     continue
404     continue

        cdm = 0.0
        do 415 i = 1,iptav+1
        if (cdiod(j,i).gt.cdm) go to 420
        go to 425
420     cdm = cdiod(j,i)
425     continue
415     continue
        cdmax(j) = cdm

        cwtot = 0.0
        do 430 i = 1,iptav
        cwtot = cdiod(j,i) + cwtot
430     continue

        vbatot=0.0
        do 413 i=1, iptav
        vbatot = vvar3(j,i) + vbatot
413     continue

        qint(j) = cwtot * delt
        caver(j) = qint(j)/(iptav * delt)
        sf(j) = caver(j)/cdmax(j)
        vbat(j) = vbatot/iptav

400     continue

c       END of DO LOOP for calculating cdiode conditions

        write(30,455) (ititle(i),i=1,80)
455     format(15x,80a1)

        write(30,452) cjo, temp, bktoq
452     format(2x,/,5x,'cjo = ',1pe10.2,2x,'Temp = ',0pf6.1,2x,
     1          'kt/q = ',0pf10.7)

        write(6,450)
        write(30,450)
450     format(2x,/,6x,'vomax',6x,'vomin',5x,'Iaver',6x,'Idmax',
     1          7x,'Sh.F.',7x,'Qint',5x,'Vbattery')

        do 460 j = 1,4
        write(6,465) vomax(j),vomin(j),caver(j),cdmax(j),sf(j),qint(j),
     1          vbat(j)
        write(30,465) vomax(j),vomin(j),caver(j),cdmax(j),sf(j),qint(j),
     1          vbat(j)
465     format(3x,7(1pe10.2,1x))
460     continue

c       Now we calculate current in resistive part of diode, current in
c               capacitive part of diode, using:
c                               Idiode = Is (exp(qVj/nkt) - 1)
c               where csat = Is, fideal = n, ideality factor
```

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cjplot.for

```
c
c                    We calculate:      Cb - Cjo/(sqrt(1- Vj/ph10)
c                                         Q - CV
c                    and                Qintq - Iredt + Qo
c
      do 435 j - 1,4

      do 440 i - 1,nmax
      vrser - cdlod(j,i)*rser
      vj(j,i) - vdlod(j,i) - vrser
      vratio - vj(j,i)/(ideal*bxtoq)
      cres(j,i) - csat*(exp(vratio)-1.0)
      ccap(j,i) - cdlod(j,i) - cres(j,i)
      fac - 1 - (vj(j,i)/sphi)
      cbar(j,i) - cjo/(sqrt(fac)
      qcalc(j,i) - -2.0 * cjo * sphi * sqrt(fac)
440   continue

      qintq(j,1) - ccap(j,1) * delt
      do 445 i - 2,nmax
      k - i-1
      qintq(j,i) - ccap(j,i) * delt + qintq(j,k)
445   continue

      qlc(j,1) - 0.0
      do 447 i - 2,nmax
      k - i-1
      delv - vj(j,i) - vj(j,k)
      qlc(j,i) - cbar(j,i)*delv + qlc(j,k)
447   continue

435   continue

c     Find constant of integration for qintq. We want to find time at
c     which vjunction is zero (sample - ilintq(j)), find qintq at
c     that time (qintq(j,ilintq(j)) - qo(j)) and find a new qintq(j,i)
c     (qintq(j,i) - qintq(j,i) - qo(j)). This new qintq(j,i) will
c     be 0.0 when vjunction is 0.0 as it should be.

      nend - int(iptav/2) + int(iptav/10)

      write(6,730) nend
      write(30,730) nend
730   format(5x,/,15x,'Constant of Integration, Qo(j):',5x,/,
     1   2x,'Looking for sign change of vjunction over',15,'  points.')

      do 725 j - 1,4

      vjstart - vj(j,1)
      if(vjstart.GE.0.0) go to 700

c     vjstart is -. Looking for where goes +.
      do 703 i - 2,nend
      k - i + 1
      if(vj(j,i).LE.0.0.AND.vj(j,k).GE.0.0) go to 708
      go to 711
708   ilintq(j) - i
711   continue
703   continue
      go to 713

700   continue
c     vjstart is +. Looking for where goes -.
      do 705 i - 2,nend
      k - i + 1
      if(vj(j,i).GE.0.0.AND.vj(j,k).LE.0.0) go to 710
      go to 715
710   ilintq(j) - i
715   continue
705   continue

713   continue
      klntq(j) - ilintq(j) + 1
      i1 - ilintq(j)
      i2 - klntq(j)
      vjtr1(j) - vj(j,i1)
      vjtr2(j) - vj(j,i2)
      qo(j) - qintq(j,i1)
      qco(j) - qlc(j,i1)
      qcao(j) - qcalc(j,i1)

725   continue

      write(30,735)
735   format(2x,'Plot',3x,'ilntq',2x,'vj(ilntq)',3x,'klntq',
     1   2x,'vj(klntq)',5x,'Qlc',7x,'Qco',7x,'Qcalco')

      do 740 j - 1,4
      write(30,745) j,ilntq(j),vjtr1(j),klntq(j),vjtr2(j),qo(j),
     1   qco(j),qcao(j)
745   format(2x,i5,2x,i5,ipe10.2,2x,i5,2x,ipe10.2,3(1x,ipe10.2))
740   continue

c     Subtract integration factor, Qo, from qintq.

      do 755 j - 1,4
      do 750 i - 1,nmax
      qintq(j,i) - qintq(j,i) - qo(j)
      qlc(j,i) - qlc(j,i) - qco(j)
      qcalc(j,i) - qcalc(j,i) - qcao(j)
750   continue
755   continue

      write(30,470)
470   format(2x,/,2x,'Sample',4x,'Time',6x,'Vdiode',5x,'Vjunc',
     1   6x,'Idiode',6x,'Ires',7x,'Icap')

      do 473 i - 1,20
      write(30,472) i,t1(i),vdlod(i,1),vj(i,1),cdlod(i,1),cres(i,1),
     1   ccap(i,1)
472   format(2x,i5,1x,ipe11.4,1x,5(ipe10.2,1x))
473   continue

      do 480 i - 30,50
      write(30,482) i,t1(i),vdlod(i,1),vj(i,1),cdlod(i,1),cres(i,1),
     1   ccap(i,1)
c482  format(2x,i5,1x,ipe11.4,1x,5(ipe10.2,1x))
c480  continue

c     do 484 i - 80,110
c     write(30,486) i,t1(i),vdlod(i,1),vj(i,1),cdlod(i,1),cres(i,1),
c    1   ccap(i,1)
c486  format(2x,i5,1x,ipe11.4,1x,5(ipe10.2,1x))
c484  continue
```

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cjplot.for

```
c              do 488 i = 110,130
c              write(30,489) i,t1(i),vdlod(i,1),vj(i,1),cdlod(i,1),cres(i,1),
c     1              ccap(i,1)
c489           format(2x,i5,1x,1pe11.4,1x,5(1pe10.2,1x))
c488           continue

               write(30,475)
475            format(/2x,'Sample',4x,'Time',5x,'Cbarrier',4x,'Vjunc',
     1              7x,'Qcalc',6x,'Qintq',7x,'Qic')

               do 476 i = 1,20
               write(30,478) i,t1(i),cbar(1,i),vj(i,1),qcalc(1,i),qintq(1,i),qic(1,i)
478            format(2x,i5,1x,1pe11.4,1x,5(1pe10.2,1x))
476            continue

               do 490 i = 30,50
               write(30,491) i,t1(i),cbar(1,i),vj(i,1),qcalc(1,i),qintq(1,i),qic(1,i)
c491           format(2x,i5,1x,1pe11.4,1x,5(1pe10.2,1x))
c490           continue

               do 493 i = 80,110
               write(30,495) i,t1(i),cbar(1,i),vj(i,1),qcalc(1,i),qintq(1,i),qic(1,i)
c495           format(2x,i5,1x,1pe11.4,1x,5(1pe10.2,1x))
c493           continue

               do 497 i = 110,130
               write(30,498) i,t1(i),cbar(1,i),vj(i,1),qcalc(1,i),qintq(1,i),qic(1,i)
c498           format(2x,i5,1x,1pe11.4,1x,5(1pe10.2,1x))
c497           continue

               Compare current into capacitor from qcalc, qintegrated(from icap),
               qintegrated from Cb,qic, with icapacitor, ccap

               ccalc(1) = 0.0
               clntq(1) = 0.0
               cic(1) = 0.0
               do 760 i = 2,nmax
               k = i - 1
               ccalc(i) = (qcalc(i,1) - qcalc(1,k))/delt
               clntq(i) = (qintq(i,1) - qintq(1,k))/delt
               cic(i) = (qic(i,1) - qic(1,k))/delt
760            continue

               write(30,765)
765            format(/2x,'Sample',4x,'Time',6x,'Icalc',6x,'Intq',
     1              7x,'Iic',7x,'Icap')

               do 767 i = 1,20
               write(30,768) i,t1(i),ccalc(i),clntq(i),cic(i),ccap(i,1)
768            format(2x,i5,1x,1pe11.4,1x,4(1pe10.2,1x))
767            continue

               do 769 i = 30,50
               write(30,770) i,t1(i),ccalc(i),clntq(i),cic(i),ccap(i,1)
c770           format(2x,i5,1x,1pe11.4,1x,4(1pe10.2,1x))
c769           continue

               do 772 i = 80,110
               write(30,773) i,t1(i),ccalc(i),clntq(i),cic(i),ccap(i,1)
c773           format(2x,i5,1x,1pe11.4,1x,4(1pe10.2,1x))
c772           continue

               do 774 i = 110,130
               write(30,775) i,t1(i),ccalc(i),clntq(i),cic(i),ccap(i,1)
c775           format(2x,i5,1x,1pe11.4,1x,4(1pe10.2,1x))
c774           continue

c              Finding limits for 1st plot, pdlod and ploa

               do 501 j = 1,4

               do 504 i = 1,nmax
               pdlod(j,i) = cdlod(j,i) * vdlod(j,i)
               ploa(j,i) = cdlod(j,i) * vo(j,i)
504            continue

501            continue

               do 506 j = 1,4
               plarge = pdlod(j,1)
               do 500 i = 2,nmax
               if (pdlod(j,i).le.plarge) go to 510
               plarge = pdlod(j,i)
510            continue
500            continue

               psmall = pdlod(j,1)
               do 505 i = 2,nmax
               if (pdlod(j,i).ge.psmall) go to 515
               psmall = pdlod(j,i)
515            continue
505            continue

               olarge = ploa(j,1)
               do 502 i = 2,nmax
               if (ploa(j,i).le.olarge) go to 512
               olarge = ploa(j,i)
512            continue
502            continue

               osmall = ploa(j,1)
               do 503 i = 2,nmax
               if (ploa(j,i).ge.osmall) go to 513
               osmall = ploa(j,i)
513            continue
503            continue

               if (olarge.ge.plarge) go to 516
               pbig = plarge
               go to 517
516            pbig = olarge
517            continue

               if (osmall.le.psmall) go to 518
               plit = psmall
               go to 519
518            plit = osmall
519            continue

               pmax(j) = pbig
               pmin(j) = plit

506            continue

c              We have now found pmax and pmin for all four curves. Now we need
c              to find absolute max and min for all curves so as to
c              plot them all on the same scales.
```


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cjplot.for

```
      ptmax = pmax(1)
      do 563 j = 2,4
      if (ptmax.ge.pmax(j)) go to 560
      ptmax = pmax(j)
560   continue
563   continue

      ptmin = pmin(1)
      do 565 j = 2,4
      if (ptmin.le.pmin(j)) go to 562
      ptmin = pmin(j)
562   continue
565   continue

      write(6,581) ptmax,ptmin
      write(30,581) ptmax, ptmin
581   format(5x, 'ptmax is',f10.5,5x,/,5x,'ptmin is',f10.5)
c     1        5x,/,10x,'Enter ptmax (ptmin = -ptmax):')
c     accept *, ptmax

c     ptmin = -1.0*ptmax

      psmax = ptmax
      pmmin = sqrt((ptmin**2))
      if(psmax.ge.pmmin) go to 582
      psmax = pmmin
582   continue

      expon = alog10(psmax)
      ipower = int(expon)
      ptmax = 1.0*10.0**(ipower)
      ptmin = - ptmax

      write(30,583) ptmax,ptmin
583   format(5x, 'Scale max, ptmax, is',1pe10.2,
     1        5x,/,5x,'Scale min, ptmin, is', 1pe10.2)

c     Finding ymax and ymin for all plots for diode voltages and currents.

      cmult = 1000
      do 307 i = 1,nmax
      cdiod(1,i) = cmult * cdiod(1,i)
      cdiod(2,i) = cmult * cdiod(2,i)
      cdiod(3,i) = cmult * cdiod(3,i)
      cdiod(4,i) = cmult * cdiod(4,i)
307   continue

      do 306 j = 1,4
      big(1) = vo(j,1)
      do 300 i = 2,nmax
      if (vo(j,i).le.big(1)) go to 310
      big(1) = vo(j,i)
310   continue
300   continue

      small(1) = vo(j,1)
      do 305 i = 2,nmax
      if (vo(j,i).ge.small(1)) go to 315
      small(1) = vo(j,i)
315   continue
305   continue

      big(3) = vdiod(j,1)
      do 302 i = 2,nmax
      if (vdiod(j,i).le.big(3)) go to 312
      big(3) = vdiod(j,i)
312   continue
302   continue

      small(3) = vdiod(j,1)
      do 303 i = 2,nmax
      if (vdiod(j,i).ge.small(3)) go to 313
      small(3) = vdiod(j,i)
313   continue
303   continue

      big(2) = cdiod(j,1)
      do 320 i = 2,nmax
      if (cdiod(j,i).le.big(2)) go to 330
      big(2) = cdiod(j,i)
330   continue
320   continue

      small(2) = cdiod(j,1)
      do 325 i = 2,nmax
      if (cdiod(j,i).ge.small(2)) go to 335
      small(2) = cdiod(j,i)
335   continue
325   continue

      big(4) = vj(j,1)
      do 370 i = 2,nmax
      if (vj(j,i).le.big(4)) go to 373
      big(4) = vj(j,i)
373   continue
370   continue

      small(4) = vj(j,1)
      do 375 i = 2,nmax
      if (vj(j,i).ge.small(4)) go to 378
      small(4) = vj(j,i)
378   continue
375   continue

      big(5) = cres(j,1)
      do 380 i = 2,nmax
      if (cres(j,i).le.big(5)) go to 383
      big(5) = cres(j,i)
383   continue
380   continue

      small(5) = cres(j,1)
      do 385 i = 2,nmax
      if (cres(j,i).ge.small(5)) go to 388
      small(5) = cres(j,i)
388   continue
385   continue

      write(30,390) j
390   format(5x,/,25x,'Plot',15,/,
     1        10x,'Vload(max,min)',18x,'Vdiod(max,min)')
      write(30,389) big(1),small(1),big(3),small(3)
389   format(5x,2(1pe10.2,2x),5x,2(1pe10.2,2x))

      write(30,391)
391   format(6x,'Idiod(max,min) in mA',18x,'Vjunc(max,min)')
      write(30,392) big(2),small(2),big(4),small(4)
392   format(5x,2(1pe10.2,2x),5x,2(1pe10.2,2x))
```


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cjplot.for

```
      write(30,395)
395   format(10x,'Iresimax,min)')
      write(30,396) biq(5),small(5)
396   format(5x,2(1pe10.2,2x),5x,2(1pe10.2,2x))

c     vo is characterized by biq(1), small(1)
c     vdiod     "    "    by biq(3), small(3)
c     cdiod     "    "    by biq(2), small(2)
c     vjunction "    "    by biq(4), small(4)
c     Iresistor "    "    by biq(5), small(5)

      biqq = biq(1)
      do 316 k = 2,5
      if (biqq.go.biq(k)) go to 317
      biqq = biq(k)
317   continue
316   continue

      ssmall = small(1)
      do 318 k = 2,5
      if (ssmall.le.small(k)) go to 319
      ssmall = small(k)
319   continue
318   continue

      ymax(j) = biqq
      ymin(j) = ssmall

306   continue

c     We have now found ymax and ymin for all four curves. Now we need
c                to find absolute max and min for all curves so as to
c                plot them all on the same scales.

      ytmax = ymax(1)
      do 363 j = 2,4
      if (ytmax.ge.ymax(j)) go to 360
      ytmax = ymax(j)
360   continue
363   continue

      ytmin = ymin(1)
      do 365 j = 2,4
      if (ytmin.le.ymin(j)) go to 362
      ytmin = ymin(j)
362   continue
365   continue

      write(6,381) ytmax,ytmin
381   format(5x,'ytmax is',f10.5,5x,/,5x,'ytmin is',f10.5)
     1       5x,/,10x,'Enter ytmax (ytmin = -1.0*ytmax):')
      accept *, ytmax

      ytmax = int(ytmax) + 1.0
      ytmin = -1.0 * ytmax

      do 606 j = 1,4
      bq(1) = ccap(j,1)
      do 600 i = 2,nmax
      if (ccap(j,i).le.bq(1)) go to 610
      bq(1) = ccap(j,i)
610   continue
600   continue

      sm(1) =ccap(j,1)
      do 605 i = 2,nmax
      if (ccap(j,i).ge.sm(1)) go to 615
      sm(1) = ccap(j,i)
615   continue
605   continue

      bq(2) = cbar(j,1)
      do 602 i = 2,nmax
      if (cbar(j,i).le.bq(2)) go to 612
      bq(2) = cbar(j,i)
612   continue
602   continue

      sm(2) = cbar(j,1)
      do 603 i = 2,nmax
      if (cbar(j,i).ge.sm(2)) go to 613
      sm(2) = cbar(j,i)
613   continue
603   continue

      bq(3) = qlc(j,1)
      do 620 i = 2,nmax
      if (qcalc(j,i).le.bq(3)) go to 630
      bq(3) = qcalc(j,i)
630   continue
620   continue

      sm(3) = qlc(j,1)
      do 625 i = 2,nmax
      if (qcalc(j,i).ge.sm(3)) go to 635
      sm(3) = qcalc(j,i)
635   continue
625   continue

      bq(4) = vj(j,1)
      do 670 i = 2,nmax
      if (vj(j,i).le.bq(4)) go to 673
      bq(4) = vj(j,i)
673   continue
670   continue

      sm(4) = vj(j,1)
      do 675 i = 2,nmax
      if (vj(j,i).ge.sm(4)) go to 678
      sm(4) = vj(j,i)
678   continue
675   continue

      bq(5) = qlntq(j,1)
      do 680 i = 2,nmax
      if (qlntq(j,i).le.bq(5)) go to 683
      bq(5) = qlntq(j,i)
683   continue
680   continue

      sm(5) = qlntq(j,1)
      do 685 i = 2,nmax
      if (qlntq(j,i).ge.sm(5)) go to 688
      sm(5) = qlntq(j,i)
688   continue
685   continue
```

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cjplot.for

```
      write(30,690) j
690   format(5x,/,25x,'Plot',i5,/,
     1       10x,'Icap(max,min)',18x,'Charlie(max,min)')
      write(30,689) bq(1),sm(1),bq(2),sm(2)
689   format(5x,2(1pe10.2,2x),5x,2(1pe10.2,2x))

      write(30,691)
691   format(10x,'Qic(max,min)',18x,'Vjunc(max,min)')
      write(30,692) bq(3),sm(3),bq(4),sm(4)
692   format(5x,2(1pe10.2,2x),5x,2(1pe10.2,2x))

      write(30,695)
695   format(5x,'Qintegrated(max,min)')
      write(30,696) bq(5),sm(5)
696   format(5x,2(1pe10.2,2x),5x,2(1pe10.2,2x))

c     ccap is characterized by bq(1), sm(1)
c     char     "       "    "  bq(2), sm(2)
c     qic      "       "    "  bq(3), sm(3)
c     vjunction "      "    "  bq(4), sm(4)
c     qintegrated "    "    "  bq(5), sm(5)

      bigar = bq(1)
      do 616 k = 2,5
      if (bigar.ge.bq(k)) go to 617
      bigar = bq(k)
617   continue
616   continue

      smaler = sm(1)
      do 618 k = 2,5
      if (smaler.le.sm(k)) go to 619
      smaler = sm(k)
619   continue
618   continue

      y2max(j) = bigar
      y2min(j) = smaler

606   continue

      CALL MSGLINE(MSGLN,NL,MSGARY)

13    write(6,13)
      format(5x,'Where do you want to plot: Versatec,Canon,Mac Screen?',
     1     2x,/,10x,'Type 1,2,3')
c     accept *, ntype

      ntype = 2

      if (ntype-2) 11,12,14

11    CALL VRSTEC(0,0,0)
      GO TO 16
12    CALL IMP300('TIME.IMP',0,0,0,0)
      GO TO 16
14    CALL TK4014(4800,0)
c14   CALL REGIS(1,0)
c     Regis is used with Rainbow Graphics Board
16    CONTINUE

      CALL RESET ('ALL')

      CALL BASALF('I/CSTD')

      CALL MIXALF('STAND')

      XPAGE=8.5
      YPAGE=11.0

      CALL PAGE(XPAGE,YPAGE)

c     plotting 4th plot: title section

      x04 = 0.5
      y04 = 9.0

      CALL PHYSOR(X04,Y04)

      XLENGT = XPAGE - X04 - 0.5
      YWIDTH = YPAGE - Y04

      CALL AREA2D(XLENGT,YWIDTH)

      HITE = 0.13
      CALL HEIGHT(HITE)

      XTIT = 1.75
      YTIT = YWIDTH - 0.5

c     CALL LSTORY(ITITLE,1,XTIT,YTIT)

      CALL MESSAG(' (S)INGLE (E)NDED (M)IXER - S',100,XTIT,YTIT)

      HITE = 0.11
      CALL HEIGHT(HITE)

      name = maqary(1)
      CALL MESSAG(NREF(NAME),4,'ABUT','ABUT')

      if (nl.le.1) go to 31

      do 33 i = 2,nl
      name = maqary(i)
      CALL MESSAG(NREF(NAME),4,'ABUT','ABUT')
33    continue

31    continue

      XM1 = 0.5
      YM1 = YTIT - 4.0*HITE

      CALL MESSAG(' (I)BIAS - $',100,XM1,YM1)
      CALL REALNO(CBIAS,-2,'ABUT','ABUT')
      CALL MESSAG(' (A): (I)LD - $',100,'ABUT','ABUT')
      CALL REALNO(CLD,-2,'ABUT','ABUT')
      CALL MESSAG(' (A),  FID - $',100,'ABUT','ABUT')
      CALL REALNO(FLD,105,'ABUT','ABUT')
      CALL MESSAG(' (B)2$',100,'ABUT','ABUT')

      YM2 = YM1 - 2.0*HITE

      CALL MESSAG(' (I)RF - $',100,XM1,YM2)
      CALL REALNO(CRF,-2,'ABUT','ABUT')
      CALL MESSAG(' (A),  FRF - $',100,'ABUT','ABUT')
      CALL REALNO(FRF,105,'ABUT','ABUT')
      CALL MESSAG(' (B)2: (C)jo - $',100,'ABUT','ABUT')
      CALL REALNO(cjo,-4,'ABUT','ABUT')
      CALL MESSAG(' (F) $',100,'ABUT','ABUT')
```


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cjplot.for

```
      XM3 = 0.5
      YM3 = YM2 -2.0*HITE
      CALL MESSAG('(R)S = $',100,XM3,YM3)
      CALL REALNO(RS,-2,'ABUT','ABUT')
      CALL MESSAG('; (L)s = $',100,'ABUT','ABUT')
      CALL REALNO(Xread,-2,'ABUT','ABUT')
      CALL MESSAG('; (R)L = $',100,'ABUT','ABUT')
      CALL REALNO(RL,-2,'ABUT','ABUT')
      CALL MESSAG('$',100,'ABUT','ABUT')
C
      XM4 = 0.5
      YM4 = YM3 -2.0*HITE
      CALL MESSAG('(I)aver = $',100,XM4,YM4)
      CALL REALNO(Caver(1),-2,'ABUT','ABUT')
      CALL MESSAG('(A); (I)max = $',100,'ABUT','ABUT')
      CALL REALNO(Cdmax(1),-2,'ABUT','ABUT')
      CALL MESSAG('(A); (S.F.) = $',100,'ABUT','ABUT')
      CALL REALNO(Sf(1),-2,'ABUT','ABUT')
      CALL MESSAG('; $',100,'ABUT','ABUT')
C
      XM5 = 0.5
      YM5 = YM4 -2.0*HITE
      CALL MESSAG('(Q)tot = $',100,XM5,YM5)
      CALL REALNO(Qint(1),-2,'ABUT','ABUT')
      CALL MESSAG('; (P)ts/(I)nt = $',100,'ABUT','ABUT')
      CALL INTNO(Ipav,'ABUT','ABUT')
      CALL MESSAG('; (N)max = $',100,'ABUT','ABUT')
      CALL INTNO(nmax,'ABUT','ABUT')
C
      XM8 = 0.5
      YM8 = YM7 -2.0*HITE
      CALL MESSAG('(V)omax = $',100,XM8,YM8)
      CALL REALNO(Vomax(1),-2,'ABUT','ABUT')
      CALL MESSAG('(V); (V)omin = $',100,'ABUT','ABUT')
      CALL REALNO(Vomin(1),-2,'ABUT','ABUT')
      CALL MESSAG('(V) $',100,'ABUT','ABUT')
C
      CALL ENDGR(0)
C
C     plotting 3rd plot: Diode power vs. time
C
      HITE = 0.13
      CALL HEIGHT(HITE)
      XO3 = 1.0
      YO3 = 8.0
      CALL PHYSOR(XO3,YO3)
      XLENGT = XPAGE - XO3 - 0.75
      YWIDTH = YO4 - YO3
      CALL AREA2D(XLENGT,YWIDTH)
      CALL YNAME('(P)ower(it(i))$',100)
      XORIG= T1(1)
      XSTP = (T1(NMAX)-T1(1))/4
      XMAX =  T1(NMAX)
      YSTP = (pmax-pmin)/2.0
      WRITE(5,15) XORIG,XSTP,XMAX,PTMIN,YSTP,PTMAX
15    FORMAT(2X,3(1PE10.3),3(E10.2))
      do 83 i = 1,501
      xvar1(i) = pdiod(i,1)
      xvar2(i) = pload(i,1)
83    continue
      CALL YAXEND('NOFIRST')
      IIH = 0
      CALL GRAF(XORIG,XSTP,XMAX,PTMIN,YSTP,PTMAX)
      CALL CURVE(T1,XVAR1,NMAX,IIH)
      CALL DOT
      CALL CURVE(T1,XVAR2,NMAX,IIH)
      CALL RESET('DOT')
      CALL GRID (1,1)
C
      end of graph
      CALL RESET('YAXEND')
      CALL ENDGR(0)
C
C     plotting 1st plot: Diode parameters vs. time
      HITE = 0.13
      CALL HEIGHT(HITE)
      XO1 = 1.0
      YO1 = 4.65
      CALL PHYSOR(XO1,YO1)
      XLENGT = XPAGE - XO1 - 0.75
      YWIDTH = YO3 - YO1 - 0.2
      CALL AREA2D(XLENGT,YWIDTH)
      CALL XNAME('(T)ime - (Sec)$',100)
      CALL YNAME('(V)diode(I(I)), (I)diode(it(I))$',100)
      XORIG= T1(1)
      XSTP = (T1(NMAX)-T1(1))/4
      XMAX =  T1(NMAX)
      ystp = (ptmax-ptmin)/2.0
      WRITE(5,15) XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX
C15   FORMAT(2X,3(1PE10.3),3(E10.2))
C     calpd was previously multiplied by cmult, now cres by cmult
      do 90 i = 1,501
      xvar1(i) = vd(i,1)
      xvar2(i) = vdiod(i,1)
      xvar3(i) = vj(i,1)
      xvar4(i) = cdiod(i,1)
      xvar5(i) = cres(i,1) * cmult
90    continue
      HITE = 0.13
      CALL HEIGHT(HITE)
```


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cjplot.for

```
      XMESS = XO1 + 1.0
      YMESS = YWIDTH - 0.5
      CALL MESSAG('(M)ult. (1)diode, (1)res - S',100,XMESS,YMESS)
      CALL REALNO(cmult,-1,'ABUT','ABUT')
      HITE = 0.13
      CALL HEIGHT(HITE)

C
      CALL MARKER(4)
      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX)
      CALL CURVE(T1,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T1,XVAR2,NMAX,IIM)
      CALL DASH
      CALL CURVE(T1,XVAR3,NMAX,IIM)
      CALL RESET ('DASH')
      CALL CURVE(T1,XVAR4,NMAX,IIM)
      CALL DASH
      CALL CURVE(T1,XVAR5,NMAX,IIM)
      CALL RESET ('DASH')
      CALL GRID (1,2)

C     end of graph

      CALL ENDGR(0)

C
C     plotting 2nd plot on 1st page - current and voltages in
C                                     the barrier capacitor

      XO2 = 1.0
      YO2 = 0.8

      CALL PHYSOR(XO2,YO2)

      XLENGT = XPAGE - XO2 - 0.75
      YWIDTH = YO1 - YO2 - 0.7
      CALL AREA2D(XLENGT,YWIDTH)

      CALL XNAME('(T)ime - (S)ecs',100)
      CALL YNAME('(C)b((1)(0),(Q) ((1)(0)S',100)

      XORIG= T1(1)
      XSTP = (T1(NMAX)-T1(1))/4
      XMAX = T1(NMAX)

      ystp = (ytmax-ytmin)/2.0
      ystp = (int(stp*1)/2

C
C     Using same limits as previous graph as long < idiode
C     hoping that qlncq and Qcalc are small, and Cb small

C     WRITE(5,15) XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX
C15   FORMAT(2X,3(1PE10.3),3(E10.2))

      cbmult = 2.0 * 10.0**6

      do 91 i = 1,501
      xvar1(i) = cbar(1,i) * cbmult
      xvar2(i) = qlncq(1,i) * 10.0**6
      xvar3(i) = qcalc(1,i) * 10.0**6
      xvar4(i) = ccap(1,i) * 10.0**3
      xvar5(i) = vj(1,i)
      xvar6(i) = qic(1,i) * 10.0**6
91    continue

      HITE = 0.13
      CALL HEIGHT(HITE)
      XMESS = XO1 + 1.0
      YMESS = YWIDTH - 0.5
      CALL MESSAG('(M)ult. (C)b - S',100,XMESS,YMESS)
      CALL REALNO(cmult,-1,'ABUT','ABUT')
      HITE = 0.13
      CALL HEIGHT(HITE)

      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX)
      CALL CURVE(T1,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T1,XVAR4,NMAX,IIM)
      CALL DASH
      CALL CURVE(T1,XVAR5,NMAX,IIM)
      CALL MARKER(6)
      IIM = 30
      CALL DOT
      CALL CURVE(T1,XVAR2,NMAX,IIM)
      CALL MARKER(4)
      CALL DASH
      CALL CURVE(T1,XVAR3,NMAX,IIM)
      CALL RESET ('DASH')
      CALL MARKER(1)
      CALL CURVE(T1,XVAR6,NMAX,IIM)
      CALL GRID (1,2)

C     end of graph
      CALL RESET('ALL')
      CALL ENDPL(0)

C     3rd page: 3rd plot

      CALL BASALF('L/CSTD')
      CALL MIXALF('STAND')

C     plotting title section

      XO4 = 0.5
      YO4 = 9.0

      CALL PHYSOR(XO4,YO4)

      XLENGT = XPAGE - XO4 - 0.5
      YWIDTH = YPAGE - YO4

      CALL AREA2D(XLENGT,YWIDTH)

      HITE = 0.13
      CALL HEIGHT(HITE)

      XTIT = 1.75
      YTIT = YWIDTH - 0.5

      CALL LSTORY(ITITLE,1,XTIT,YTIT)

C
```

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```
      CALL MESSAG(' (S)INGLE (E)NDED (M)IXER - $',100,XTIT,YTIT)

      HITE = 0.11
      CALL HEIGHT(HITE)

      name = msgary(1)
      CALL MESSAG(%REF(NAME),4,'ABUT','ABUT')

      If (ni.le.1) go to 32

      do 34 i = 2,ni
      name = msgary(i)
      CALL MESSAG(%REF(NAME),4,'ABUT','ABUT')
34    continue

32    continue

      HITE = 0.13
      CALL HEIGHT(HITE)

      XM1 = 0.5
      YM1 = YTIT - 4.0*HITE

      CALL MESSAG(' (I)aver = $',100,XM1,YM1)
      CALL REALNO(caver(3),-2,'ABUT','ABUT')
      CALL MESSAG(' (A); (I)max = $',100,'ABUT','ABUT')
      CALL REALNO(cdmax(3),-2,'ABUT','ABUT')
      CALL MESSAG(' (A); (S.F.) = $',100,'ABUT','ABUT')
      CALL REALNO(sf(3),-2,'ABUT','ABUT')
c     CALL MESSAG('; $',100,'ABUT','ABUT')

      XM2 = 0.5
      YM2 = YM1 -2.0*HITE

      CALL MESSAG(' (Q)tot = $',100,XM2,YM2)
      CALL REALNO(qint(3),-2,'ABUT','ABUT')
      CALL MESSAG('; (P)ts/(I)nt = $',100,'ABUT','ABUT')
      CALL INTNO(iptav,'ABUT','ABUT')
      CALL MESSAG('; (N)max = $',100,'ABUT','ABUT')
      CALL INTNO(nmax,'ABUT','ABUT')

      XM3 = 0.5
      YM3 = YM2 -2.0*HITE

      CALL MESSAG(' (V)omax = $',100,XM3,YM3)
      CALL REALNO(vomax(3),-2,'ABUT','ABUT')
      CALL MESSAG(' (V); (V)omin = $',100,'ABUT','ABUT')
      CALL REALNO(vomin(3),-2,'ABUT','ABUT')
      CALL MESSAG(' (V); (I)d*(V)o)aver = $',100,'ABUT','ABUT')
      CALL REALNO(vbat(3),-2,'ABUT','ABUT')
      CALL MESSAG(' (V) $',100,'ABUT','ABUT')

      CALL ENDGR(0)

c     plotting 3rd plot: Diode power vs. time

      HITE = 0.13
      CALL HEIGHT(HITE)

      x03 = 1.0
      y03 = 8.0

      CALL PHYSOR(X03,Y03)

      XLENGT = XPAGE - X03 - 0.75
      YWIDTH = Y04 - Y03
      CALL AREA2D(XLENGT,YWIDTH)

      CALL YNAME(' (P)ower(()t())$',100)

      XORIG= T3(1)
      XSTP = (T3(NMAX)-T3(1))/4
      XMAX =  T3(NMAX)

      ystp = (ptmax-ptmin)/2.0

C     WRITE(5,15) XORIG,XSTP,XMAX,PTMIN,YSTP,PTMAX
C15   FORMAT(2X,3(1PE10.3),3(E10.2))

      do 87 i = 1,501
      xvar1(i) = pdiod(3,i)
      xvar2(i) = pload(3,i)
87    continue

      CALL YAXEND('NOFIRST')
      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,PTMIN,YSTP,PTMAX)
      CALL CURVE(T3,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T3,XVAR2,NMAX,IIM)
      CALL RESET ('DOT')
      CALL GRID (1,1)

C     end of graph

      CALL RESET('YAXEND')
      CALL ENDGR(0)

c     plotting 1st graph on 3rd page

      HITE = 0.13
      CALL HEIGHT(HITE)

      X01 = 1.0
      Y01 = 4.65

      CALL PHYSOR(X01,Y01)

      XLENGT = XPAGE - X01 - 0.75
      YWIDTH = Y03 - Y01 - 0.2
      CALL AREA2D(XLENGT,YWIDTH)

      CALL XNAME(' (T)ime - (S)ec$',100)
      CALL YNAME(' (V)diode(()t()), (I)diode(()t())$',100)

      XORIG= T3(1)
      XSTP = (T3(NMAX)-T3(1))/4
      XMAX =  T3(NMAX)

      ystp = (ytmax-ytmin)/2.0
      do 94 i = 1,501
      xvar1(i) = vo(3,i)
      xvar2(i) = vdiod(3,i)
      xvar3(i) = vj(3,i)
      xvar4(i) = cdiod(3,i)
      xvar5(i) = cres(3,i) * cmult
94    continue
```


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cjplot.for

```
      HITE = 0.13
      CALL HEIGHT(HITE)
      XHESS = XO1 + 1.0
      YHESS = YWIDTH - 0.5
      CALL MESSAG('(H)ult. (I)diode, (I)res - S',100,XHESS,YHESS)
      CALL REALNO(cbmult,-1,'ABUT','ABUT')
      HITE = 0.13
      CALL HEIGHT(HITE)

C
      CALL MARKER(4)
      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,YTHIN,YSTP,YTMAX)
      CALL CURVE(T3,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T3,XVAR2,NMAX,IIM)
      CALL DASH
      CALL CURVE(T3,XVAR3,NMAX,IIM)
      CALL RESET ('DASH')
      CALL CURVE(T3,XVAR4,NMAX,IIM)
      CALL DASH
      CALL CURVE(T3,XVAR5,NMAX,IIM)
      CALL RESET ('DASH')
      CALL GRID (1,2)

C     end of graph

      CALL ENDGR(0)

C     plotting 2nd plot on 3rd page - Current and Voltages in
C                                     the barrier Capacitor

      XO2 = 1.0
      YO2 = 0.8

      CALL PHYSOR(XO2,YO2)

      XLENGT = XPAGE - XO2 - 0.75
      YWIDTH = YO1 - YO2 - 0.7
      CALL AREAZD(XLENGT,YWIDTH)

      CALL XNAME('(T)ime - (S)ec$',100)
      CALL YNAME('(C)b((t()),(Q)((t())$',100)

      XORIG= T3(1)
      XSTP = (T3(NMAX)-T3(1))/4
      XMAX = T3(NMAX)

      ystp = (ymax-ymin)/2.0
      ystp = (int(stp)+1)/2

C
C15   WRITE(5,15) XORIG,XSTP,XMAX,YTHIN,YSTP,YTMAX
      FORMAT(2X,3(1PE10.3),3(E10.2))

      cbmult = 2.0 * 10.0**6

      do 95 I = 1,501
      xvar1(I) = cbar(3,I) * cbmult
      xvar2(I) = qincg(3,I) * 10.0**6
      xvar3(I) = qcalc(3,I) * 10.0**6
      xvar4(I) = dcap(3,I) * 10.0**3
      xvar5(I) = v3(3,I)
      xvar6(I) = qlc(3,I) * 10.0**6
95    continue

      HITE = 0.13
      CALL HEIGHT(HITE)
      XHESS = XO1 + 1.0
      YHESS = YWIDTH - 0.5
      CALL MESSAG('(H)ult. (C)b = S',100,XHESS,YHESS)
      CALL REALNO(cbmult,-1,'ABUT','ABUT')
      HITE = 0.13
      CALL HEIGHT(HITE)

      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,YTHIN,YSTP,YTMAX)
      CALL CURVE(T3,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T3,XVAR4,NMAX,IIM)
      CALL DASH
      CALL CURVE(T3,XVAR5,NMAX,IIM)
      CALL MARKER(6)
      IIM = 30
      CALL DOT
      CALL CURVE(T3,XVAR2,NMAX,IIM)
      CALL MARKER(4)
      CALL DASH
      CALL CURVE(T3,XVAR3,NMAX,IIM)
      CALL RESET ('DASH')
      CALL MARKER(1)
      CALL CURVE(T3,XVAR6,NMAX,IIM)
      CALL GRID (1,2)

C     end of graph

      CALL RESET('ALL')
      CALL ENDPL(0)

C     go to 700

C     2nd Page: 2nd plot

      CALL BASALF('L/CSTD')
      CALL MIXALF('STAND')

      XPAGE=8.5
      YPAGE=11.0

      CALL PAGE(XPAGE,YPAGE)

C     plotting 4th plot: title section

      X04 = 0.5
      Y04 = 9.0

      CALL PHYSOR(X04,Y04)

      XLENGT = XPAGE - X04 - 0.5
      YWIDTH = YPAGE - Y04

      CALL AREAZD(XLENGT,YWIDTH)

      HITE =.13
      CALL HEIGHT(HITE)

      XTIT = 1.75
```

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cjplot.for

```
      YTIT = YWIDTH - 0.5

c     CALL ISTORY(ITITLE,1,XTIT,YTIT)

      CALL MESSAG('(S)INGLE (E)NDED (M)IXER - $',100,XTIT,YTIT)
      HITE = 0.11
      CALL HEIGHT(HITE)

      name = nsgary(1)
      CALL MESSAG(&REF(NAME),4,'ABUT','ABUT')

      If (nl.le.1) go to 36

      do 38 i = 2,n1
      name = nsgary(i)
      CALL MESSAG(&REF(NAME),4,'ABUT','ABUT')
38    continue

36    continue

      HITE = 0.13
      CALL HEIGHT(HITE)

      XM1 = 0.5
      YM1 = YTIT - 4.0*HITE

      CALL MESSAG('(l)ayer - $',100,XM1,YM1)
      CALL REALNO(layer(2),-2,'ABUT','ABUT')
      CALL MESSAG('(A); (l)max = $',100,'ABUT','ABUT')
      CALL REALNO(cdmax(2),-2,'ABUT','ABUT')
      CALL MESSAG('(A); (S.F.) = $',100,'ABUT','ABUT')
      CALL REALNO(sf(2),-2,'ABUT','ABUT')
      CALL MESSAG('; S',100,'ABUT','ABUT')

c     XM2 = 0.5
      YM2 = YM1 -2.0*HITE

      CALL MESSAG('(D)ot - $',100,XM2,YM2)
      CALL REALNO(dinc(2),-2,'ABUT','ABUT')
      CALL MESSAG('; (P)ts/(l)ne - $',100,'ABUT','ABUT')
      CALL INTNO(ptsv,'ABUT','ABUT')
      CALL MESSAG('; (N)max = $',100,'ABUT','ABUT')
      CALL INTNO(nmax,'ABUT','ABUT')

      XM3 = 0.5
      YM3 = YM2 -2.0*HITE

      CALL MESSAG('(V)dmax = $',100,XM3,YM3)
      CALL REALNO(vdmax(2),-2,'ABUT','ABUT')
      CALL MESSAG('(V); (V)dmin = $',100,'ABUT','ABUT')
      CALL REALNO(vdmin(2),-2,'ABUT','ABUT')
      CALL MESSAG('(V); (l)(V)d*(V)o(l)ayer - $',100,'ABUT','ABUT')
      CALL REALNO(vbat(2),-2,'ABUT','ABUT')
      CALL MESSAG('(V) S',100,'ABUT','ABUT')

      CALL ENDGR(0)

c     plotting 3rd plot: Diode power vs. time

      HITE = 0.13
      CALL HEIGHT(HITE)

      x03 = 1.0

      y03 = 8.0

      CALL PHYSOR(X03,Y03)

      XLENGT = XPAGE - X03 - 0.75
      YWIDTH = Y04 - Y03
      CALL AREA2D(XLENGT,YWIDTH)

      CALL YNAME('(P)ower((l)t(l))$',100)

      XORIG= T2(1)
      XSTP = (T2(NMAX)-T2(1))/4
      XMAX = T2(NMAX)

      ystp = (ptmax-ptmin)/2.0

C     WRITE(5,15) XORIG,XSTP,XMAX,PTMIN,YSTP,PTMAX
C15   FORMAT(2X,3(1PE10.3),3(E10.2))

      do 85 i = 1,501
      xvar1(i) = pdiod(2,i)
      xvar2(i) = pload(2,i)
85    continue

      CALL YAXEND('NOFIRST')
      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,PTMIN,YSTP,PTMAX)
      CALL CURVE(T2,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T2,XVAR2,NMAX,IIM)
      CALL RESET('DOT')
      CALL GRID (1,1)

c     end of graph

      CALL RESET('YAXEND')
      CALL ENDGR(0)

c     plotting 1st graph on 2nd page

      HITE = 0.13
      CALL HEIGHT(HITE)
      X01 = 1.0
      Y01 = 4.65

      CALL PHYSOR(X01,Y01)

      XLENGT = XPAGE - X01 - 0.75
      YWIDTH = Y03 - Y01 - 0.2
      CALL AREA2D(XLENGT,YWIDTH)

      CALL XNAME('(T)ime - (S)ecS',100)
      CALL YNAME('(V)diode((l)t(l)),(l)diode((l)t(l))$',100)

      XORIG= T2(1)
      XSTP = (T2(NMAX)-T2(1))/4
      XMAX = T2(NMAX)

      ystp = (ytmax-ytmin)/2.0

      do 92 i = 1,501
      xvar1(i) = vo1(2,i)
      xvar2(i) = vdiod(2,i)
```


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cjplot.for

```
      xvar3(i) = vj(2,i)
      xvar4(i) = cdiod(2,i)
      xvar5(i) = cres(2,i) * cmult
92    continue

      HITE = 0.13
      CALL HEIGHT(HITE)
      XMESS = XO1 + 1.0
      YMESS = YWIDTH - 0.5
      CALL MESSAG('(M)ult. (i)diode, (I)res - $',100,XMESS,YMESS)
      CALL REALNO(cmult,-1,'ABUT','ABUT')
      HITE = 0.13
      CALL HEIGHT(HITE)

C     CALL MARKER(4)
      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX)
      CALL CURVE(T2,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T2,XVAR2,NMAX,IIM)
      CALL DASH
      CALL CURVE(T2,XVAR3,NMAX,IIM)
      CALL RESET ('DASH')
      CALL CURVE(T2,XVAR4,NMAX,IIM)
      CALL DASH
      CALL CURVE(T2,XVAR5,NMAX,IIM)
      CALL RESET ('DASH')
      CALL GRID (1,2)

C     end of graph

      CALL ENDGR(0)

C     plotting 2nd plot on 2nd page - Current and Voltages in
C                    the barrier Capacitor

      XO2 = 1.0
      YO2 = 0.8

      CALL PHYSOR(XO2,YO2)

      XLENGT = XPAGE - XO2 - 0.75
      YWIDTH = YO1 - YO2 - 0.7
      CALL AREA2D(XLENGT,YWIDTH)

      CALL XNAME(' (T)ime - (S)ecs',100)
      CALL YNAME(' (C)ib(i)t(I), (Q)(i)t(i)s',100)

      XORIG= T2(1)
      XSTP = (T2(NMAX)-T2(1))/4
      XMAX = T2(NMAX)

      ystp = (ymax-ymin)/2.0
      ystp = (int(stp)+1)/2

C     WRITE(5,15) XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX
C15   FORMAT(2X,3(1PE10.3),3(E10.2))

      cmult = 2.0 * 10.0**6

      do 93 i = 1,501
      xvar1(i) = cbar(2,i) * cmult
      xvar2(i) = qintq(2,i) * 10.0**6
      xvar3(i) = qreal(2,i) * 10.0**6
      xvar4(i) = ccap(2,i) * 10.0**3
      xvar5(i) = vj(2,i)
      xvar6(i) = qic(2,i) * 10.0**6
93    continue

      HITE = 0.13
      CALL HEIGHT(HITE)
      XMESS = XO1 + 1.0
      YMESS = YWIDTH - 0.5
      CALL MESSAG('(M)ult., (C)ib - $',100,XMESS,YMESS)
      CALL REALNO(cmult,-1,'ABUT','ABUT')
      HITE = 0.13
      CALL HEIGHT(HITE)

      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX)
      CALL CURVE(T2,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T2,XVAR4,NMAX,IIM)
      CALL DASH
      CALL CURVE(T2,XVAR5,NMAX,IIM)
      CALL MARKER(6)
      IIM = 30
      CALL DOT
      CALL CURVE(T2,XVAR2,NMAX,IIM)
      CALL MARKER(4)
      CALL DASH
      CALL CURVE(T2,XVAR3,NMAX,IIM)
      CALL RESET ('DASH')
      CALL MARKER(1)
      CALL CURVE(T2,XVAR6,NMAX,IIM)
      CALL GRID (1,2)

C     end of graph

      CALL RESET('ALL')
      CALL ENDPL(0)

C     4th page: 4th and last plot
C     plotting 4th plot: title section

      CALL BASALF('L/GSTD')
      CALL MIXALF('STAND')

      XPAGE=8.5
      YPAGE=11.0

      CALL PAGE(XPAGE,YPAGE)

      x04 = 0.5
      y04 = 9.0

      CALL PHYSOR(X04,Y04)

      XLENGT = XPAGE - X04 - 0.5
      YWIDTH = YPAGE - Y04

      CALL AREA2D(XLENGT,YWIDTH)

      HITE = .13
      CALL HEIGHT(HITE)
```


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cjplot.for

```
      XTIT = 1.75
      YTIT = YWIDTH - 0.5

c     CALL LSTORY(ITITLE,1,XTIT,YTIT)

      CALL MESSAG('(S)INGLE (E)NDED (M)IXER - $',100,XTIT,YTIT)

      HITE = 0.11
      CALL HEIGHT(HITE)

      name = msqary(1)
      CALL MESSAG(NAME(name),4,'ABUT','ABUT')

      if (n1.le.1) go to 39

      do 41 i = 2,n1
      name = msqary(i)
      CALL MESSAG(NAME(name),4,'ABUT','ABUT')
41    continue

39    continue

      HITE = 0.13
      CALL HEIGHT(HITE)

      XM1 = 0.5
      YM1 = YTIT - 4.0*HITE

      CALL MESSAG('(I)aver = $',100,XM1,YM1)
      CALL REALNO(caver(4),-2,'ABUT','ABUT')
      CALL MESSAG('(A); (I)max = $',100,'ABUT','ABUT')
      CALL REALNO(cdmax(4),-2,'ABUT','ABUT')
      CALL MESSAG('(A); (S,F) = $',100,'ABUT','ABUT')
      CALL REALNO(is(4),-2,'ABUT','ABUT')
      CALL MESSAG('; $',100,'ABUT','ABUT')

c     XM2 = 0.5
      YM2 = YM1 -2.0*HITE

      CALL MESSAG('(O)tot - $',100,XM2,YM2)
      CALL REALNO(qint(4),-2,'ABUT','ABUT')
      CALL MESSAG('; (P)ts/(I)nt = $',100,'ABUT','ABUT')
      CALL INTNO(ipav,'ABUT','ABUT')
      CALL MESSAG('; (N)max = $',100,'ABUT','ABUT')
      CALL INTNO(nmax,'ABUT','ABUT')

      XM3 = 0.5
      YM3 = YM2 -2.0*HITE

      CALL MESSAG('(V)omax = $',100,XM3,YM3)
      CALL REALNO(vomax(4),-2,'ABUT','ABUT')
      CALL MESSAG('(V); (V)omin = $',100,'ABUT','ABUT')
      CALL REALNO(vomin(4),-2,'ABUT','ABUT')
      CALL MESSAG('(V); (I)(V)d*(V)o(I)aver = $',100,'ABUT','ABUT')
      CALL REALNO(vbat(4),-2,'ABUT','ABUT')
      CALL MESSAG('(V) $',100,'ABUT','ABUT')

      CALL ENDGR(0)

c     plotting 3rd plot: Diode power vs. time

      HITE = 0.13
      CALL HEIGHT(HITE)

      x03 = 1.0
      y03 = 8.0

      CALL PHYSOR(X03,Y03)

      XLENGT = XPAGE - x03 - 0.75
      YWIDTH = Y04 - Y03
      CALL AREA2D(XLENGT,YWIDTH)

      CALL YNAME('(P)ower((it()$',100)

      XORIG= T4(1)
      XSTP = (T4(NMAX)-T4(1))/4
      XMAX = T4(NMAX)

      ystp = (ptmax-ptmin)/2.0

C     WRITE(5,15) XORIG,XSTP,XMAX,PTMIN,YSTP,PTMAX
C15   FORMAT(2X,3(1PE10.3),3(E10.2))

      do 89 i = 1,501
      xvar1(i) = pdiod(4,i)
      xvar2(i) = pload(4,i)
89    continue

      CALL YAXEND('NOFIRST')
      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,PTMIN,YSTP,PTMAX)
      CALL CURVE(T4,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T4,XVAR2,NMAX,IIM)
      CALL RESET('DOT')
      CALL GRID (1,1)

c     end of graph

      CALL RESET('YAXEND')
      CALL ENDGR(0)

c     plotting 1st graph on 4th page

      HITE = 0.13
      CALL HEIGHT(HITE)

      XO1 = 1.0
      YO1 = 4.65

      CALL PHYSOR(XO1,YO1)

      XLENGT = XPAGE - XO1 - 0.75
      YWIDTH = YO3 - YO1 - 0.2
      CALL AREA2D(XLENGT,YWIDTH)

      CALL XNAME('(T)ime - (Sec$',100)
      CALL YNAME('(V)diode((it()),(I)diode((it()$',100)

      XORIG= T4(1)
      XSTP = (T4(NMAX)-T4(1))/4
      XMAX = T4(NMAX)
      .
      ystp = (ymax-ymin)/2.0

      do 96 i = 1,501
```


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cjplot.for

15

```
      xvar1(1) = vo(4,1)
      xvar2(1) = vdiod(4,1)
      xvar3(1) = vj(4,1)
      xvar4(1) = cdiod(4,1)
      xvar5(1) = cres(4,1) * cmult
96    continue

      HITE = 0.13
      CALL HEIGHT(HITE)
      XMESS = X01 + 1.0
      YMESS = YWIDTH - 0.5
      CALL MESSAG(' (M)ult. (I)diode, (I)res = 5',100,XMESS,YMESS)
      CALL REALNO(cmult,-1,'ABUT','ABUT')
      HITE = 0.13
      CALL HEIGHT(HITE)


C     CALL MARKER(4)
      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX)
      CALL CURVE(T4,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T4,XVAR2,NMAX,IIM)
      CALL DASH
      CALL CURVE(T4,XVAR3,NMAX,IIM)
      CALL RESET ('DASH')
      CALL CURVE(T4,XVAR4,NMAX,IIM)
      CALL DASH
      CALL CURVE(T4,XVAR5,NMAX,IIM)
      CALL RESET ('DASH')
      CALL GRID (1,2)

C     end of graph

      CALL ENDGR(0)

C     plotting 2nd plot on 1st page - Current and Voltages in
c                    the barrier Capacitor

      X02 = 1.0
      Y02 = 0.8

      CALL PHYSOR(X02,Y02)

      XLENGT = XPAGE - X02 - 0.75
      YWIDTH = Y01 - Y02 - 0.7
      CALL AREA2D(XLENGT,YWIDTH)

      CALL XNAME(' (T)ime - (S)ec$',100)
      CALL YNAME(' (C)b(()t()), (Q)(()t())$',100)

      XORIG= T4(1)
      XSTP = (T4(NMAX)-T4(1))/4
      XMAX =  T4(NMAX)

      ystp = (ytmax-ytmin)/2.0
c     ystp = (int(stp)+1)/2


C     WRITE(5,15) XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX
C15   FORMAT(2X,3(1PE10.3),3(E10.2))

      cbmult = 2.0 * 10.0**6
```

```
      do 97 i = 1,501
      xvar1(1) = cbar(4,i) * cbmult
      xvar2(1) = qintg(4,i) * 10.0**6
      xvar3(1) = qcalc(4,i) * 10.0**6
      xvar4(1) = ccap(4,i) * 10.0**3
      xvar5(1) = vj(4,i)
      xvar6(1) = qic(4,i) * 10.0**6
97    continue

      HITE = 0.13
      CALL HEIGHT(HITE)
      XMESS = X01 + 1.0
      YMESS = YWIDTH - 0.5
      CALL MESSAG(' (M)ult. (C)b = 5',100,XMESS,YMESS)
      CALL REALNO(cbmult,-1,'ABUT','ABUT')
      HITE = 0.13
      CALL HEIGHT(HITE)

      IIM = 0
      CALL GRAF(XORIG,XSTP,XMAX,YTMIN,YSTP,YTMAX)
      CALL CURVE(T4,XVAR1,NMAX,IIM)
      CALL DOT
      CALL CURVE(T4,XVAR4,NMAX,IIM)
      CALL DASH
C     CALL CURVE(T4,XVAR5,NMAX,IIM)
      CALL MARKER(6)
      IIM = 30
      CALL DOT
      CALL CURVE(T4,XVAR2,NMAX,IIM)
      CALL MARKER(4)
      CALL DASH
      CALL CURVE(T4,XVAR3,NMAX,IIM)
      CALL RESET ('DASH')
      CALL MARKER(1)
      CALL CURVE(T4,XVAR6,NMAX,IIM)
      CALL GRID (1,2)

C     end of graph

      CALL RESET('ALL')
      CALL ENDPL(0)


c700  continue

      CALL DONEPL


      STOP
      END


ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

      SUBROUTINE MSGLINE(MSGLN,NI,MSGARY)

C     INPUT:
C     MSGLN   UP TO 60 CHARACTER LINE
C     OUTPUT:
C     NI      # OF 4-CHARACTER WORDS IN THE MESSAGE
C     MSGARY- ARRAY HOLDING THE MESSAGE IN 4-CHAR. WORDS

      character*60 MSGLN
      integer*4 imsgln(15)
```


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cjplot.for

```
      character*4 MSGARY(15)

      NCHR=0
      I=1
   80 IF( MSGLN(I:I) .EQ. ':') GO TO 100
      NCHR=NCHR+1
      I=I+1
      GO TO 80

  100 IF(MOD(NCHR,4) .EQ. 0) THEN
          NI=NCHR/4
          DO 105 I=1,NI
              II=4*(I-1)+1
              READ(MSGLN(II:II+3),159)IMSGLN(I)
  105     CONTINUE
      ELSE
          NI=NCHR/4 + 1
          DO 115 I=1,NI-1
              II=4*(I-1)+1
              READ(MSGLN(II:II+3),159)IMSGLN(I)
  115     CONTINUE
          READ(MSGLN(4*(NI-1)+1:NCHR),159)IMSGLN(NI)
      END IF

      DO 120 I=1,NI
          WRITE(MSGARY(I),159)IMSGLN(I)
  120 CONTINUE

      RETURN

  159 FORMAT(A4)

      END
```


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Appendix B

Amplifier Appendix

B.1 Op-amp Noise Parameters

Table 36 gives the input voltage and current noise sources, $\overline{v_i^2}$ and $\overline{i_i^2}$, for the Analog Devices OP-07 and OP-27 and for a generic 741 op-amp. The AD-07 is an ultra-low offset voltage op-amp similar to the μA714 and μA725 from Fairchild; the AD-27 is an ultra-low noise precision op-amp; the 741 op-amp is a general purpose industry standard op-amp [1].

The values of $\overline{v_i^2}$ and $\overline{i_i^2}$ are given at only three frequencies in the data catalog for the Analog Devices op-amps: 10 Hz, 100 Hz and 1 KHz for the OP-07 and 10 Hz, 30 Hz, and 1KHz for the OP-27.

B.2 Performance Expressions for Three Transistor Configurations: CE, CB, and CC

B.2.1 Gain Expressions

The performance of three transistor building blocks has been analyzed in order to understand which configuration will best meet the needs of the direct conversion receiver's amplifier: operation from a low R_S into high R_L, low $1/f$ noise, good overall noise performance, and acceptable gain. The three transistor configurations that have

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Table 36: Op-Amp Noise Models

Frequency	$\overline{v_i^2}$ (V^2/Hz)		
	OP-07	OP-27	741
≤ 0.01 Hz			$6.0 * 10^{-12}$
1 Hz			$6.0 * 10^{-14}$
10 Hz	$1.1 * 10^{-16}$	$1.2 * 10^{-17}$	$6.0 * 10^{-15}$
30 Hz		$9.6 * 10^{-18}$	$6.0 * 10^{-15}$
100 Hz	$1.0 * 10^{-16}$		$1.1 * 10^{-15}$
500 Hz			$5.0 * 10^{-16}$
1 KHz	$9.2 * 10^{-17}$	$9.0 * 10^{-18}$	$4.4 * 10^{-16}$
5 KHz			$4.0 * 10^{-16}$
10 KHz			$4.0 * 10^{-16}$

Frequency	$\overline{i_i^2}$ (A^2/Hz)		
	OP-07	OP-27	741
≤ 0.01 Hz			$9.8 * 10^{-20}$
1 Hz			$7.8 * 10^{-22}$
10 Hz	$1.0 * 10^{-25}$	$2.9 * 10^{-24}$	$6.9 * 10^{-23}$
30 Hz		$1.0 * 10^{-24}$	$6.9 * 10^{-23}$
100 Hz	$2.0 * 10^{-26}$		$6.2 * 10^{-24}$
500 Hz			$1.4 * 10^{-24}$
1 KHz	$1.4 * 10^{-26}$	$1.6 * 10^{-25}$	$8.3 * 10^{-25}$
5 KHz			$3.7 * 10^{-25}$
10 KHz			$3.0 * 10^{-25}$

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been examined are the common-emitter block (CE), the common-base block (CB), and the common-collector, or emitter-follower, block (CC). Table 37 gives the circuit diagram for each transistor configuration and their small signal, hybrid-π, models.

Y parameters have been used to model the three transistor configurations. **Y** parameters relate the input two port waveforms, I_1 and V_1, to the output two port waveforms, I_2 and V_2, in the following way:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}.$$

The voltage gain V_2/V_1, current gain I_2/I_1, input admittance Y_{in}, and output admittance Y_{out} can then be found from the **Y** parameters and the source and load admittances, Y_S and Y_L respectively, as given below:

$$A_V = \frac{V_2}{V_1} = \frac{-y_{21}}{y_{22} + y_L}, \tag{78}$$

$$A_I = \frac{I_2}{I_1} = \frac{y_{21} Y_L}{D_Y + y_{11} Y_L}, \tag{79}$$

$$Y_{in} = y_{11} - \left(\frac{y_{12} y_{21}}{y_{22} + Y_S} \right), \tag{80}$$

$$Y_{out} = y_{22} - \left(\frac{y_{12} y_{21}}{y_{11} + Y_S} \right), \tag{81}$$

where D_Y is the determinant of **Y**.

Other parameters of interest are A_{VS}, the voltage gain from the source to the load:

$$A_{VS} = \frac{V_{out}}{V_S}, \tag{82}$$

the available power gain, APG, defined as

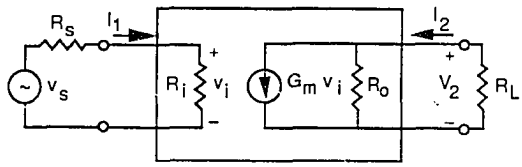
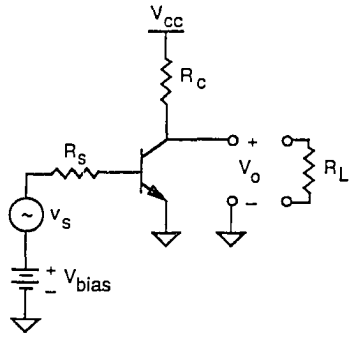
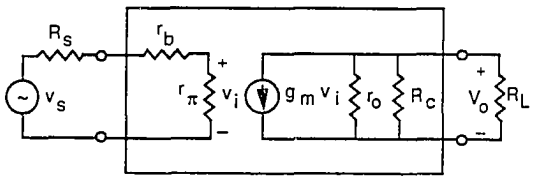
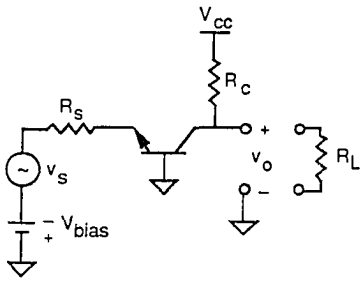
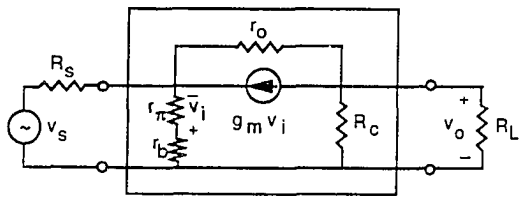
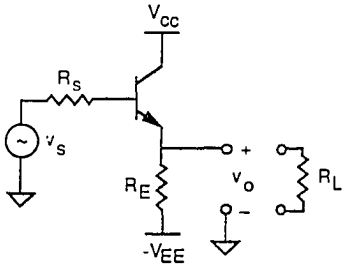
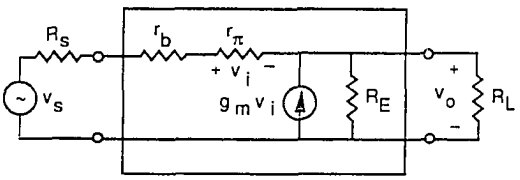
$$APG = \frac{\text{Power delivered to load}}{\text{Power available from the source}}, \tag{83}$$

which can be found from A_{VS} as follows:

$$APG = A_{VS}^2 \frac{4R_S}{R_L},$$

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Table 37: CE, CB, and CC Amplifier Configurations and Small Signal Models

	CIRCUIT	BASIC TWO PORT CIRCUIT MODEL
		
CE		 $R_i = r_b + r_\pi$ $R_o = r_o \parallel R_c$ $G_m = g_m \cdot \left(\frac{1}{1 + r_b/r_\pi}\right)$
CB		 $R_i = \frac{\alpha_o}{g_m}\left(1 + \frac{r_b}{r_\pi}\right)$ $R_o \sim R_c$ $G_m = -g_m \left(\frac{1}{1 + r_b/r_\pi}\right)$
CC	 $R_{LT} = R_L \parallel R_E$	 $R_i = r_\pi + r_b + R_{LT}(\beta_o + 1)$ $R_o = \frac{(r_\pi + r_b + R_s) R_E}{(1 + \beta_o) R_E + (R_s + r_\pi + r_b)}$

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and the available power gain under matched conditions, *APGM*. In general *APG* and *APGM* are complex functions of the small signal transistor models and their circuits, however under certain conditions they can be easily expressed in terms of the circuit's **Y** parameters. If the **Y** parameters are independent of Y_L, the condition on Y_L for power match is:

$$Y_L = \sqrt{\frac{R_i}{R_o} D_Y}; \tag{84}$$

and if the two port can be modelled by

$$\mathbf{Y} = \begin{bmatrix} \frac{1}{R_i} & 0 \\ G_m & \frac{1}{R_o} \end{bmatrix}$$

as the CE and CB amplifier configurations can, then A_V and A_I can be expressed as:

$$\begin{aligned} A_V &= -G_m (R_o \parallel R_L), \\ A_I &= G_m (R_o \parallel R_L) \frac{R_i}{R_L}. \end{aligned}$$

The available power gain under matched conditions can be calculated from eqn. 84. It occurs for $R_L = R_o$. *APGM* is then found to be:

$$APGM = \frac{G_m^2 R_i R_o}{4}.$$

The **Y** parameters for the three transistor configurations are shown in Table 38. Also listed are the voltage and current gains, A_V and A_I, the squared voltage gain, A_{VS}, the output impedance for conjugate match to R_o, $R_{L_{opt}}$, and the available power gain under matched conditions, *APGM*.

B.2.2 Noise Temperature Expressions

The total noise voltage at the output of each transistor can be written in terms of three transistor noise generators. They are the voltage noise source due to thermal noise in the base resistance r_b: $\overline{v_b^2}$; the current noise source representing the excess or $1/f$ noise and shot noise due to the base current I_B: $\overline{i_b^2}$; and the current noise source representing the shot noise caused by the collector current I_C: $\overline{i_c^2}$. These noise sources can be written in terms of the hybrid-π transistor model parameters as follows:

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Table 38: **Y** Parameters and Circuit Performance Relations for the Three Amplifier Configurations

	Y Parameter	Circuit Performance
CE	$\begin{bmatrix} \frac{1}{r_b+r_\pi} & 0 \\ \frac{g_m}{1+\frac{r_b}{r_\pi}} & \frac{1}{r_o\|R_c} \end{bmatrix}$	$A_V = \frac{-g_m r_\pi R_o\|R_L}{r_\pi+r_b}$ $A_I = \frac{g_m r_\pi R_o\|R_L}{R_L}$ $A_{VS}^2 = \left(\frac{g_m r_\pi R_o\|R_L}{r_\pi+r_b+R_S}\right)^2$ $R_{L_{opt}} = R_o$ $APGM = \frac{(g_m r_\pi)^2 r_o\|R_L}{4(r_b+r_\pi)}$
CB	$\begin{bmatrix} \frac{g_m}{\alpha_o(1+\frac{r_b}{r_\pi})} & 0 \\ \frac{-g_m}{1+\frac{r_b}{r_\pi}} & \frac{1}{R_c} \end{bmatrix}$	$A_V = \frac{g_m r_\pi R_C\|R_L}{r_\pi+r_b}$ $A_I = \frac{-\beta_0}{1+\beta_0}\frac{R_C\|R_L}{R_L}$ $A_{VS}^2 = \left(\frac{g_m r_\pi R_o\|R_L}{R_S(1+g_m r_\pi)+r_b+r_\pi}\right)^2$ $R_{L_{opt}} = R_o$ $APGM = \frac{(g_m r_\pi)^2 R_C}{4(1+\beta_o)(r_b+r_\pi)}$
CC	$\begin{bmatrix} \frac{1}{r_b+r_\pi} & \frac{-1}{r_b+r_\pi} \\ \frac{-(\beta_o+1)}{r_b+r_\pi} & \frac{(\beta_o+1)}{r_b+r_\pi}+\frac{1}{R_E} \end{bmatrix}$	$A_V = \frac{R_{LT}(\beta_o+1)}{r_\pi+r_b+R_{LT}(\beta_o+1)}$ $A_I = \frac{-R_{LT}(\beta_o+1)}{R_L}$ $A_{VS}^2 = \left(\frac{1}{1+\frac{R_S+r_\pi+r_b}{R_{LT}(\beta_o+1)}}\right)^2$ $R_{L_{opt}} = R_o$ $A_I A_V = \frac{-R_{LT}(\beta_o+1)}{R_L}\left(\frac{1}{1+\frac{r_\pi+r_b}{R_{LT}(\beta_o+1)}}\right)$

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$$\overline{v_b^2} = 4kTr_b\,\Delta f \quad \text{in } \frac{V^2}{Hz}, \tag{85}$$

$$\overline{i_b^2} = \frac{K_1 I_B^a}{f^b} + 2qI_B\,\Delta f \quad \text{in } \frac{A^2}{Hz}, \tag{86}$$

$$\overline{i_c^2} = 2qI_C\,\Delta f \quad \text{in } \frac{A^2}{Hz} \tag{87}$$

where the values for K_1, a, and b are device dependent; a ranges from 0.5 to 2.0 and b is approximately 1.0 for silicon bipolar transistors. Note that the term due to burst noise in $\overline{i_b^2}$ is not included.

The noise generated by the source and collector resistors, R_S and R_C respectively, in the amplifier circuit can be written in terms of a noise voltage source or a current source as:

$$\overline{v_{R_S}^2} = 4kTR_S\,\Delta f \quad \text{in } \frac{V^2}{Hz}, \tag{88}$$

or,

$$\overline{i_{R_C}^2} = \frac{4kT}{R_C}\,\Delta f \quad \text{in } \frac{A^2}{Hz}. \tag{89}$$

B.3 Transistor Models

Three transistor models are used in this analysis; the models are denoted by XM_1, XM_2, and XM_3. The transistor models differ in the absolute values given for r_b and β_0 and in the manner in which these parameters vary with I_C. All models use the same characterization for the $1/f$ noise: $K_1 = 4 * 10^{-14}$, $a = 1.3$, and $b = 1.2$. These values are based on the noise performance of the National Semiconductor LM394, a superbeta monolithic matched transistor pair [33]. The differences in r_b and β_0 for the transistor models are shown in Table 39.

Once values for transistor parameters r_b, β_0, and V_A (the Early voltage) are set for a given I_C, the following relationships can be used to calculate the remaining hybrid-π parameters, g_m, r_π, and r_o:

$$g_m = \frac{qI_C}{kT}, \tag{90}$$

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Table 39: Bipolar Transistor Models

	XM_1	XM_2		XM_3	
I_C	β_0	r_b	β_0	r_b	β_0
0.001mA	N.C.†	670Ω	23.8	350Ω	380
0.01mA	500	670Ω	75.3	350Ω	480
0.025mA	N.C.	670Ω	119.1	245Ω	510
0.1mA	600	540Ω	220	120Ω	600
0.3mA	N.C.	368.5Ω	290	100Ω	630
1.0mA	700	234.5Ω	232	100Ω	700
4.0mA	750	N.C.	N.C.	N.C.	N.C.
5.0mA	N.C.	70Ω	46.4	100Ω	760
10.0mA	800	50Ω	43.5	100Ω	800

† Not Calculated.

$$r_\pi = \frac{\beta_0}{g_m}, \tag{91}$$

$$r_o = \frac{V_A}{I_C}, \tag{92}$$

where q is the charge on the electron ($1.6 * 10^{-19}$ coulomb), k is Boltzmann's constant ($1.38 * 10^{-23}$ joules/Kelvins) and T is the transistor temperature.

Transistor model XM_1 is based on the National Semiconductor LM394 with r_b assumed to be a constant. The values shown for β_0 in Table 39 and the value of V_A have been calculated from the device **H** parameters given in the data sheets. These can be related to the hybrid-π parameters as shown below:

$$\mathbf{H} = \begin{bmatrix} h_{ie} & h_{re} \\ h_{fe} & h_{oe} \end{bmatrix} = \begin{bmatrix} r_b + r_\pi & 0 \\ \beta_0 & \frac{1}{r_o} \end{bmatrix}.$$

From the device data V_A is found to be 100V and a reasonable value taken for r_b. r_b is taken to be 50Ω [25]. It can be set to 500Ω to see the effect of increased base resistance.

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Transistor model XM_2 is based on a small n-p-n transistor used in the input stage of Intersil, Inc.'s op-amp, ICL 8741 [77]. Transistor model XM_3 is a fictitious device having a current gain equal to that of device XM_1, a National Semiconductor LM394 superbeta monolithic matched transistor pair, and a base resistance composed of two elements: a constant resistor equal to 100Ω and a resistor whose resistance varies with I_C. XM_2 is meant to simulate a general purpose op-amp transistor and XM_3 to simulate a high performance op-amp transistor.

These transistor models are used throughout the amplifier work to model the performance of the ultra-low noise op-amps and the general purpose op-amps. This allows our models to be compared against the performance of other amplifier circuits. For example, when a differential pair with a current source is modelled as consisting of four XM_2 transistors biased at a collector current of 5μA, the resulting noise performance is very similar to that of the OP-07. When the transistors are taken to be XM_3 devices biased at 5μA, their noise performance is roughly equivalent to that of an OP-27.

B.4 Performance of the CE, CB, and CC Transistor Configurations using Transistor Model XM_1

B.4.1 Gain, R_{in}, and R_{out}

Figure 96, 97, and 98 show R_{in}, R_{out} and ${A_{VS}}^2$ as a function of I_C for a transistor amplifier in the CE, CB and CC configuration, respectively. Transistor parameters, r_b and β_0, have been varied as shown and resultant values of R_{in}, R_{out} and ${A_{VS}}^2$ have been found. These new values have been plotted whenever there is a significant change in one of these parameters. R_{in} and R_{out} are given in Table 37 and ${A_{VS}}^2$ is given in Table 38 for the three configurations.

For the CE configuration R_{in} approaches r_π as r_b is $\leq r_\pi$ and $R_{out} \sim R_C$. R_{in} is plotted for two values of β. For the CB configuration R_{out} can be seen to be

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comparable to R_C for the range of I_C values plotted. In the CC configuration the equations for R_{in}, R_{out}, and ${A_{VS}}^2$ simplify to:

$$R_{in} = \begin{cases} \frac{\beta_0 v_T}{I_C} & R_{LT} < \frac{v_T}{I_C} \\ R_{LT}\beta_0 & R_{LT} > \frac{v_T}{I_C} \end{cases},$$

$$R_{out} \sim \begin{cases} \frac{r_\pi}{\beta_0} = \frac{v_T}{I_C} & R_E < \frac{v_T}{I_C} \\ R_E & R_E > \frac{v_T}{I_C} \end{cases},$$

$$A_{VS} \sim \frac{1}{1 + \frac{v_T}{I_C R_{LT}}}.$$

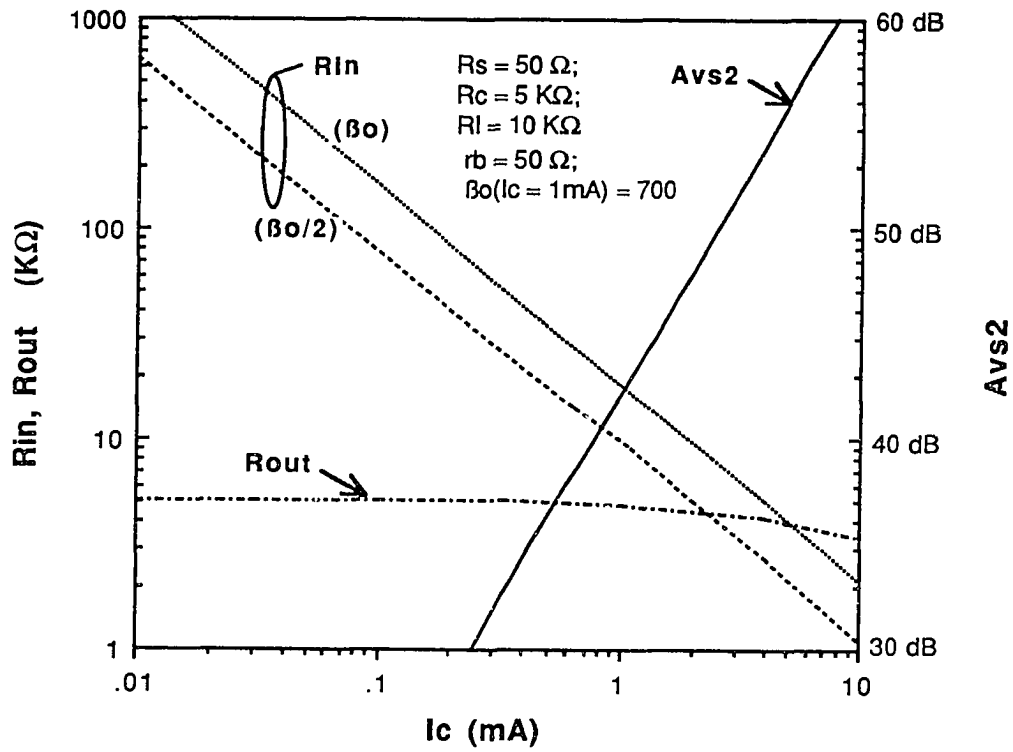


Figure 96: R_{in}, R_{out} and ${A_{VS}}^2$ vs. I_C for a CE Amplifier.

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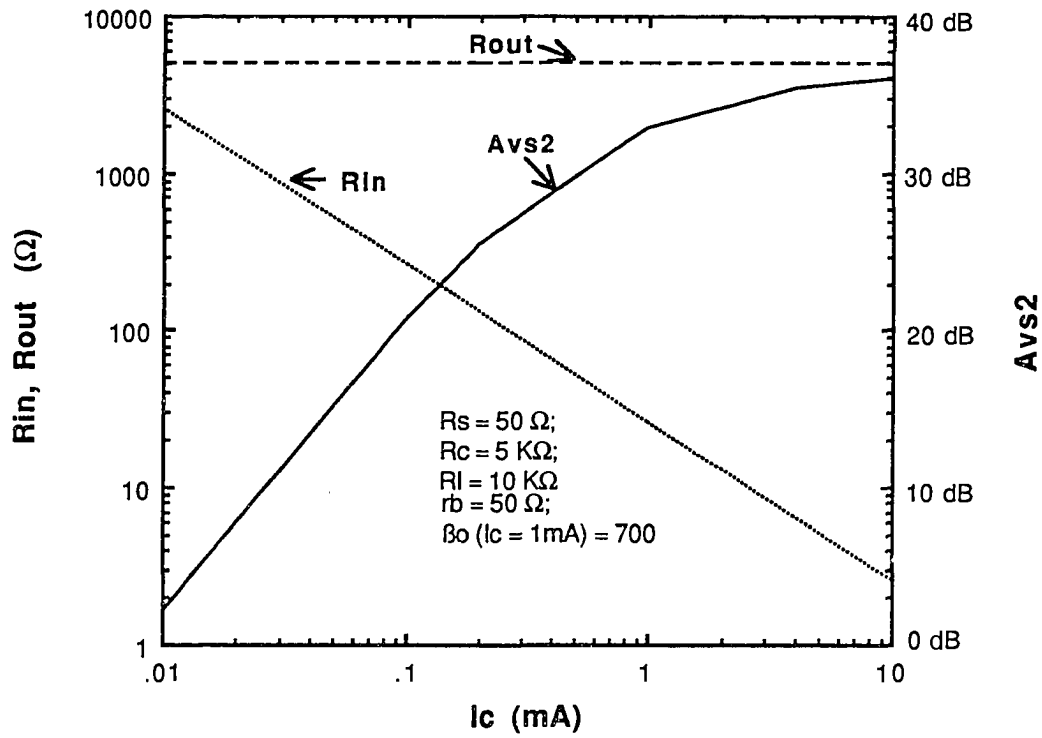


Figure 97: R_{in}, R_{out} and $A_{VS}{}^2$ vs. I_C for a CB Amplifier.

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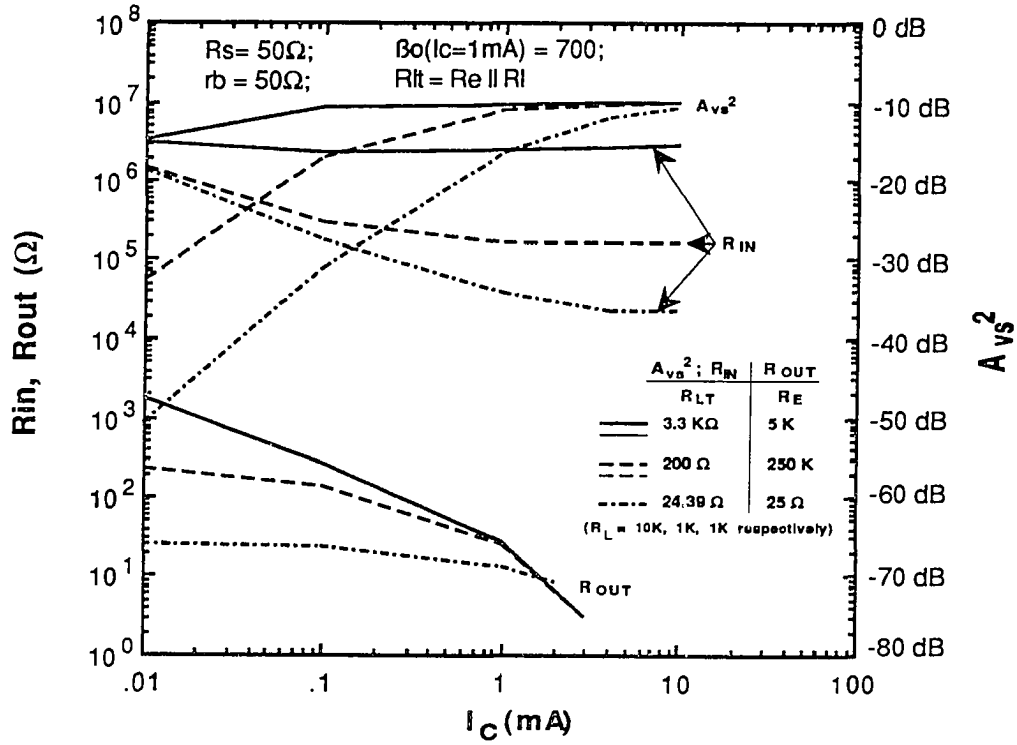


Figure 98: R_{in}, R_{out} and $A_{VS}{}^2$ vs. I_C for a CC Amplifier.

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In the specific case of CC we see that because we have direct feedback from output to input through r_π, R_{in} depends on R_{LT}, and R_{out} depends on R_S. Thus in this case we plot R_{in}, R_{out} and ${A_{VS}}^2$ while varying R_E and R_L.

Insofar as these three parameters depend on transistor parameters r_b and β_0, we find that none depend strongly on r_b and only R_{in} depends on β_0 ($R_{in} \sim (R_e \parallel R_L) \cdot \beta_0$, for large values of I_C).

The choice of appropriate amplifier configuration, either CE, CB, or CC, depends on the source impedance presented to the amplifier, ie. the load impedance presented by the direct conversion receiver mixer. This sets R_{in}. Table 40 summarizes the performance of the three amplifier types in terms of the possible driving impedances and optimal amplifier load impedances.

Table 40: Circuit Characteristics for the Three Amplifier Configurations

Amplifier Configuration	R_{in} @ $I_C = I_{mA}$	R_{out} @ $I_C = I_{mA}$
CE	$\sim$10KΩ	$= R_c \sim$ 5K
CB	20Ω	$= R_c \sim$ 5K
CC	$\geq$ 30KΩ	20Ω

Available power gain obtained under matched output conditions ($R_L = R_{out}$), $APGM$, can be written as:

$$\begin{aligned} APGM|_{CE} &= \left(\frac{g_m \cdot r_\pi}{r_\pi + r_b + R_S}\right)^2 \cdot \left(\frac{1}{2}R_0\right)^2 \cdot \frac{4R_S}{R_0} \\ &= \left(\frac{g_m \cdot r_\pi}{r_\pi + r_b + R_S}\right)^2 \cdot R_0 \cdot R_S, \end{aligned}$$

$$APGM|_{CB} = \left(\frac{g_m \cdot r_\pi}{R_S(1 + g_m \cdot r_\pi) + r_b + r_\pi}\right)^2 \cdot R_0 \cdot R_S,$$

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$$APGM|_{CC} = (\beta_0 + 1)^2 \frac{R_{out} \cdot R_S}{(R_S + r_b + r_\pi)^2}.$$

Rewritting $APGM$ substituting transistor parameters for R_{out}:

$$APGM = \begin{cases} \frac{\beta_0^2 \cdot R_S \cdot (r_0 \| R_c)}{(R_S + r_b + r_\pi)^2} & CE \\ \frac{\beta_0^2 \cdot R_S \cdot R_c}{(R_S(1+\beta_0) + r_b + r_\pi)^2} & CB \\ \frac{(\beta_0+1)^2 \cdot R_S \cdot R_E}{(R_S + r_\pi + r_b) \cdot (R_S + r_\pi + r_b + R_E(1+\beta_0))} & CC \end{cases}$$

APG and $APGM$ are plotted in Figure 99 for all three amplifier configurations as a function of I_C. The behavior of $APGM$ for the three amplifier configurations can be compared by approximating the above expressions. The following is then obtained: for CE with R_L set to R_{out} ($R_{out} = (r_0 \parallel R_C)$)

$$\begin{aligned} APGM &\simeq \frac{\beta_0^2 \cdot R_S \cdot r_0 \parallel R_C}{r\pi^2}, \\ &\simeq \frac{I_C^2}{V_T^2} \cdot R_S \cdot (r_0 \parallel R_C); \end{aligned}$$

for CB with R_L set to R_{out} ($R_{out} = \simeq R_C$)

$$\begin{aligned} APGM &\simeq \frac{\beta_0^2 \cdot R_S \cdot R_C}{(R_S \cdot \beta_0 + \beta_0/g_m)^2}, \\ &\simeq \frac{I_C^2 \cdot R_S \cdot R_C}{V_T^2 \cdot (1 + R_S g_m)^2}; \end{aligned}$$

for CC with R_L set to R_{out} ($R_{out} = \frac{(r_\pi + R_S + r_b) \cdot R_E}{(1+\beta_0)R_E + (R_S + r_\pi + r_b)}$)

$$\begin{aligned} APGM &\simeq \frac{\beta_0^2 \cdot R_S \cdot R_E}{r_\pi(r_\pi + R_E r_\pi g_m)}, \\ &\simeq \frac{I_C^2 \cdot R_S \cdot R_E}{V_T^2(1 + R_E g_m)}. \end{aligned}$$

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From Figure 99 it can be clearly seen that for low I_C (I_C such that $g_m \cdot R_E \ll 1$) APGM for CE and CB are nearly identical, that for CC is $\approx 10^{-4}$ times lower when R_E is 5 K and more than 200 times lower for R_E equal to 25 Ω, ie. the larger R_E in the CC configuration, the larger the APGM. For higher I_C, the APGM of CC becomes closer to that of CB, while the APGM of CE is nearly 100 times that of CB.

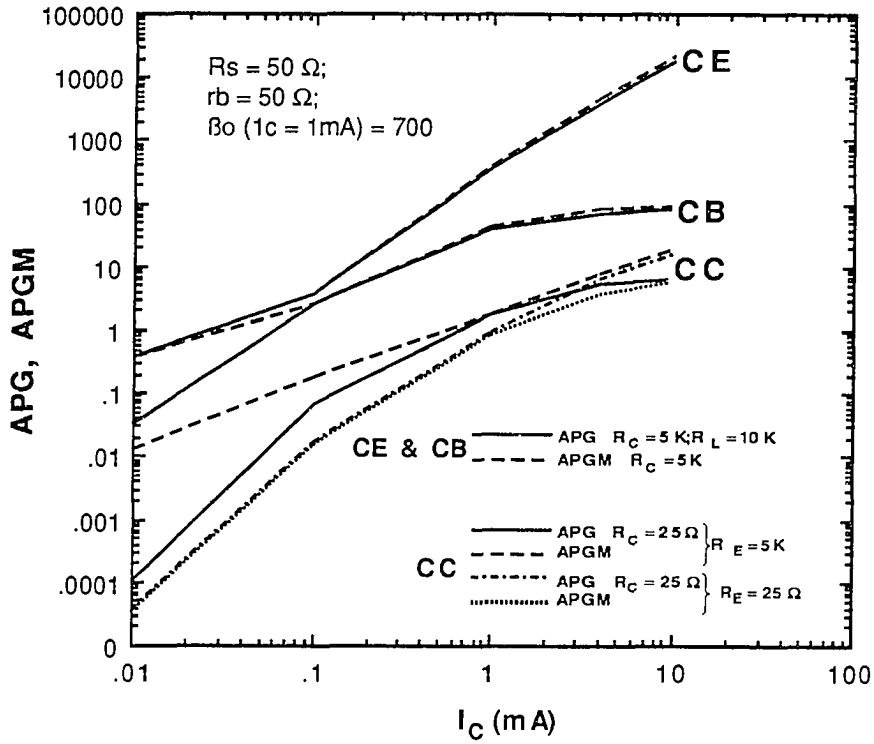


Figure 99: APG and APGM vs. I_C for CE, CB, and CC amplifier configurations.

B.4.2 Noise Temperature Performance

Based on the noise model given in the previous section, the output noise voltages can be written as follows for the three amplifier configurations: for the CE configuration

$$\frac{\overline{v_0^2}}{\Delta f} = \left(\frac{g_m R_{LT} r_\pi}{R_S + r_b + r_\pi}\right)^2 \cdot \left[\overline{v_s^2} + \overline{v_b^2} + (R_S + r_b)^2\,\overline{i_b^2} + \left(\frac{R_S + r_b + r_\pi}{g_m r_\pi}\right)^2 \overline{i_c^2}\right.$$

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$$+\left(\frac{R_S+r_b+r_\pi}{g_m r_\pi}\right)^2 \overline{i_{R_{LT}}^2}\Big];$$

for the CB configuration

$$\frac{\overline{v_0^2}}{\Delta f} = \left(\frac{g_m R_{LT} r_\pi}{R_S(1+g_m r_\pi)+r_b+r_\pi}\right)^2 \cdot \Big[\overline{v_s^2}+\overline{v_b^2}+(R_S+r_b)^2\,\overline{i_b^2} + \left(\frac{R_S+r_b+r_\pi}{g_m r_\pi}\right)^2 \overline{i_c^2} + \left(\frac{R_S(1+g_m r_\pi)+r_b+r_\pi}{g_m r_\pi}\right)^2 \overline{i_{R_{LT}}^2}\Big];$$

for the CC configuration

$$\frac{\overline{v_0^2}}{\Delta f} = \left(\frac{1}{1+\frac{R_S+r_\pi+r_b}{R_{LT}(\beta_0+1)}}\right)^2 \cdot \Big[\overline{v_s^2}+\overline{v_b^2}+\left(\frac{\beta_0(R_S+r_b)-r_\pi}{\beta_0+1}\right)^2 \overline{i_b^2} + \left(\frac{R_S+r_b+r_\pi}{\beta_0+1}\right)^2 \overline{i_c^2} + \left(\frac{R_S+r_\pi+r_b}{\beta_0+1}\right)^2 \overline{i_{R_{LT}}^2}\Big].$$

As the first term represents signal gain $\left(\frac{v_0}{v_s} = A_{Vs}\right)$ we can express the noise performance of these three amplifiers in terms of noise added at the input through the use of Eqns. 93 and 94:

$$\frac{\overline{v_0^2}}{\Delta f} = A_{Vs}^2 \cdot \overline{v_{n_{in}}^2}, \tag{93}$$

where

$$\overline{v_{n_{in}^2}} = \overline{v_s^2} + \overline{v_a^2}, \tag{94}$$

$\overline{v_s^2}$ is the input noise voltage and $\overline{v_a^2}$ is the noise added by the amplifier. The meaning behind this equation is depicted in Figure 100.

Comparing input noise voltage for the three configurations we note that (a) the contribution to output noise voltage due to $\overline{v_b^2}$ is identical to that of input noise source

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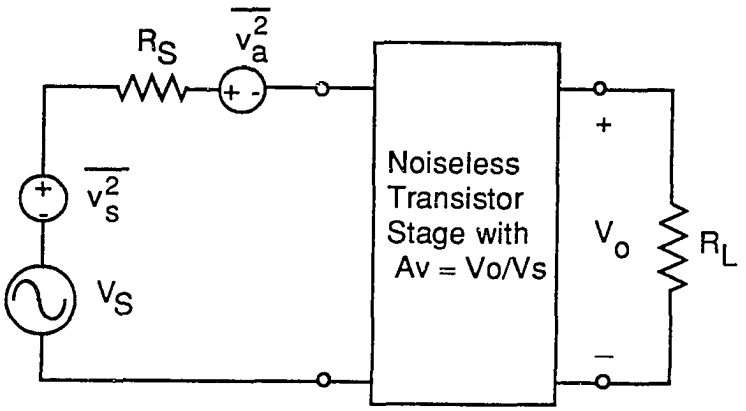


Figure 100: Noise sources of amplifier referred to the input of an ideal noiseless transistor stage.

for all transistor configurations; and (b) the noise contributions from $\overline{v_s^2}$, $\overline{v_b^2}$, $\overline{i_b^2}$, $\overline{i_c^2}$ to CE and CB are identical. The input noise of CE and CB differs only in $\overline{i_{R_{LT}}^2}$ term where the contribution of CB is slightly lower for the CE configuration.

We can plot $\overline{v_a^2}$ of each amplifier in terms of the effective noise temperature of each of the noise sources referred to the input:

$$\overline{v_a^2} = \overline{v_b^2} + K_b\overline{i_b^2} + K_c\overline{i_c^2} + K_L\overline{i_{R_{LT}}^2}$$

where each noise voltage sources, working into R_S, can be expressed as $\overline{v_i^2} = 4KT_iR_S$. Thus the individual noise contribution can be plotted in terms of their equivalent input voltage (or $V/\sqrt{Hz}$) (in which case the minimum detectable signal $v_{s_{min}} \sim \sqrt{\overline{v_s^2} + \overline{v_a^2}}$) or in terms of their effective noise temperature.

Since receiver performance is often expressed in terms of equivalent input temperature which can be easily related to noise figure via:

$$F = 1 + \frac{T_{amp}}{T}$$

where T is the physical temperature of R_S, commonly 290 K, we will plot the contributions of each transistor and the thermal noise source due to R_S in terms of their equivalent temperature:

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$$T_{added} = T_{\overline{v_b^2}} + T_{\overline{i_b^2}} + T_{\overline{i_c^2}} + T_{\overline{i_{R_{LT}}^2}}.$$

This can be expressed for each amplifier type as follows. For the CE configuration, T_{added} can be written as:

$$T_{added} = \frac{\overline{v_b^2}}{4kR_S} + \frac{(R_S + r_b)^2}{4kR_S}\,\overline{i_b^2} + \left(\frac{R_S + r_b + r_\pi}{g_m r_\pi}\right)^2 \frac{\overline{i_c^2}}{4kR_S}$$

$$+\left(\frac{R_S + r_b + r_\pi}{g_m r_\pi}\right)^2 \frac{\overline{i_{R_{LT}}^2}}{4kR_S}.$$

Using the definitions of $\overline{v_b^2}$, $\overline{i_b^2}$, $\overline{i_c^2}$ and $\overline{i_{R_{LT}}^2}$, T_{added} can be written for all three transistor configurations by the following equations. For the CE configuration, T_{added} can be expressed as:

$$T_{added} = T \cdot \frac{r_b}{R_S} + \frac{(R_S + r_b)^2}{4kR_S}\left[\frac{K_1 I_B^a}{f^b} + 2qI_B\right] + \left(\frac{R_S + r_b + r_\pi}{g_m r_\pi}\right)^2 \frac{2qI_C}{4kR_S}$$

$$+ \left(\frac{R_S + r_b + r_\pi}{g_m r_\pi}\right)^2 \frac{T}{R_S \cdot R_{LT}}.$$

For the CB configuration, T_{added} can be expressed as:

$$T_{added} = T \cdot \frac{r_b}{R_S} + \frac{(R_S + r_b)^2}{4kR_S}\left[\frac{K_1 I_B^a}{f^b} + 2qI_B\right] + \left(\frac{R_S + r_b + r_\pi}{g_m r_\pi}\right)^2 \frac{2qI_C}{4kR_S}$$

$$+ \left(\frac{R_S(1 + g_m r_\pi) + r_b + r_\pi}{g_m r_\pi}\right)^2 \frac{T}{R_S \cdot R_{LT}}.$$

For the CC configuration, T_{added} can be expressed as:

$$T_{added} = T \cdot \frac{r_b}{R_S} + \frac{1}{4kR_S}\left(\frac{\beta_0(R_S + r_b) - r_\pi}{\beta_0 + 1}\right)^2 \left[\frac{K_1 I_B^a}{f^b} + 2qI_B\right]$$

$$+ \left(\frac{R_S + r_b + r_\pi}{\beta_0 + 1}\right)^2 \frac{2qI_C}{4kR_S} + \left(\frac{R_S + r_\pi + r_b}{\beta_0 + 1}\right)^2 \frac{T}{R_S \cdot R_{LT}}.$$

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The above equations involve the following transistor parameters: r_b, r_π, g_m, β_0, I_C, I_B, a, b, K_1. Once K_1, a, and b are specified, the magnitude of $1/f$ noise is given as a function of I_B and frequency. Once r_b, I_C, and $\beta_0(I_C)$ are given, g_m, r_π, and r_o can be found from eqns. 90, 91 and 92. The equivalent noise temperature due to each noise generator, $T_{\overline{i_b^2}}$, $T_{\overline{i_b^2}}$, $T_{\overline{i_c^2}}$, $T_{\overline{i^2_{R_{LT}}}}$ and their sum T_{added}, can be plotted vs I_C for all three transistor types. $T_{\overline{v_b^2}}$, ... , T_{added} are plotted for two values of r_b as $\overline{v_b^2}$ determines T_{min}. Plots of these noise temperature components are shown in Figures 101, 102 and 103 for the three amplifier configurations.

Discussion

Noise performance results can be studied by looking at the magnitude of T_{added} for all three configurations, by determining the dominant noise contribution to T_{added} at various values of I_C, by examining the effect of changes in certain transistor parameters on T_{added}, and lastly by quantifying the importance of $1/f$ noise contribution to $\overline{i_b^2}$. Each of these topics is examined below separately.

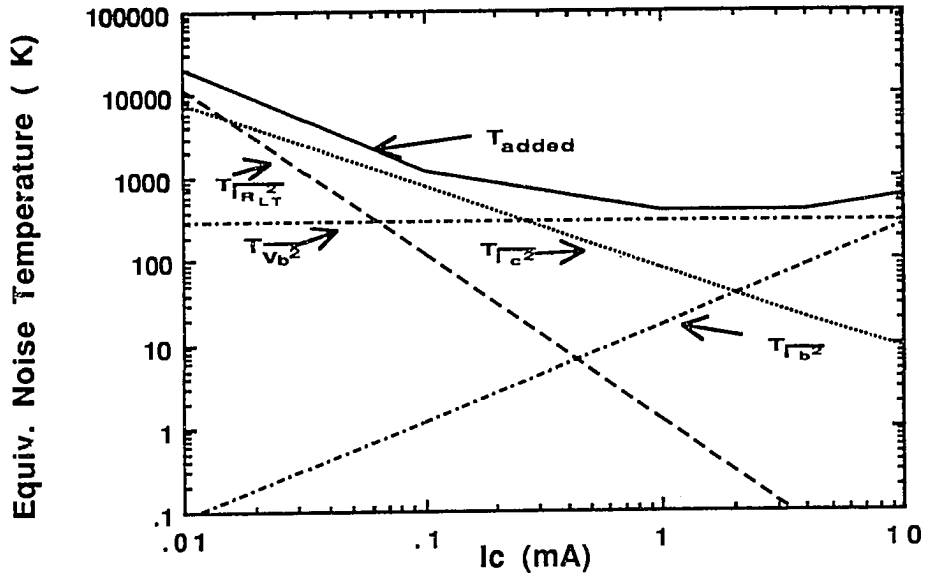
Comparison between transistor types. 1. T_{added} is nearly identical for all three configurations. This can be seen from the above equations as the dominant terms in T_{added} are nearly identical, i.e. $\overline{v_b^2}$, $\overline{i_b^2}$.

2. CE and CB differ only in $T_{\overline{i^2_{R_{LT}}}}$, because A_{V_s} flattens out as I_C increases for the CB transistor but not for the CE transistor. This is elaborated upon later. The effect of $\overline{i_{R^2_{LT}}}$ is greater for the CB than the CE configuration at high currents. This can also be thought of in terms of the higher current gain CE vs CB. The lack of CB current gain causes current at output to be referred to the input current with unity loss.

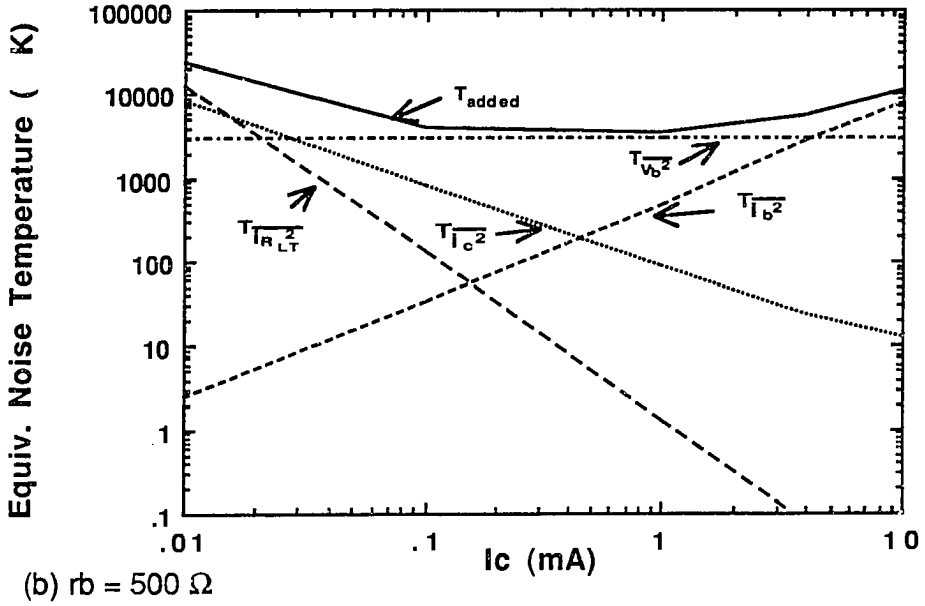
3. CC differs from both CE and CB in the magnitude of the $T_{\overline{i_b^2}}$ term. This is due to the feedback in r_π.

Dominant contributor to T_{added} as I_C is varied. The dominant noise contributor to T_{added} depends on the operating value of I_C. This is shown in Table 41.

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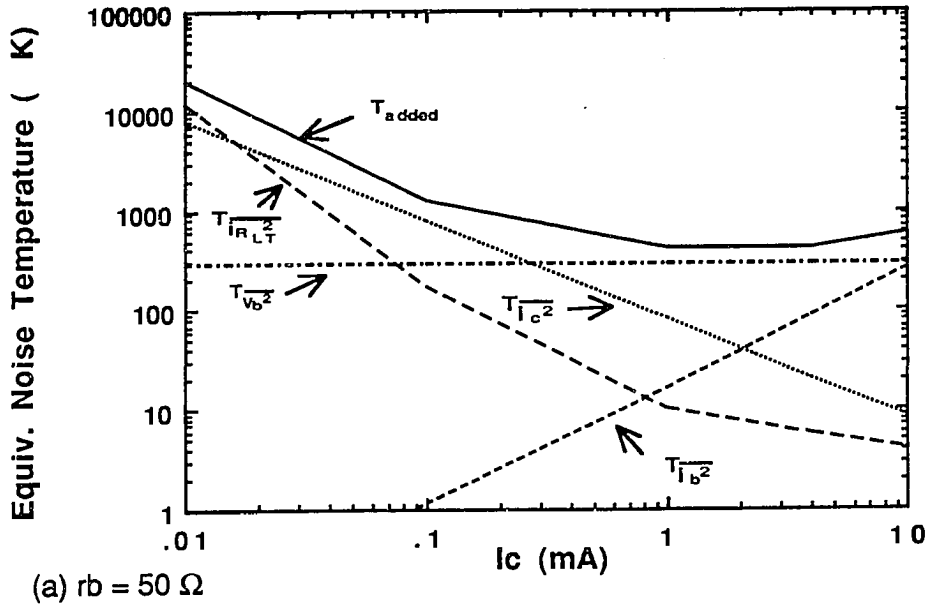
(a) rb = 50 Ω



(b) rb = 500 Ω

Figure 101: Equivalent noise temperature at 100 Hz at the input of a CE amplifier ($R_S = 50\Omega$; $R_C = 5\text{K}\Omega$; $R_L = 10\text{K}\Omega$; $\beta_0(I_C = 1\text{mA}) = 700$).

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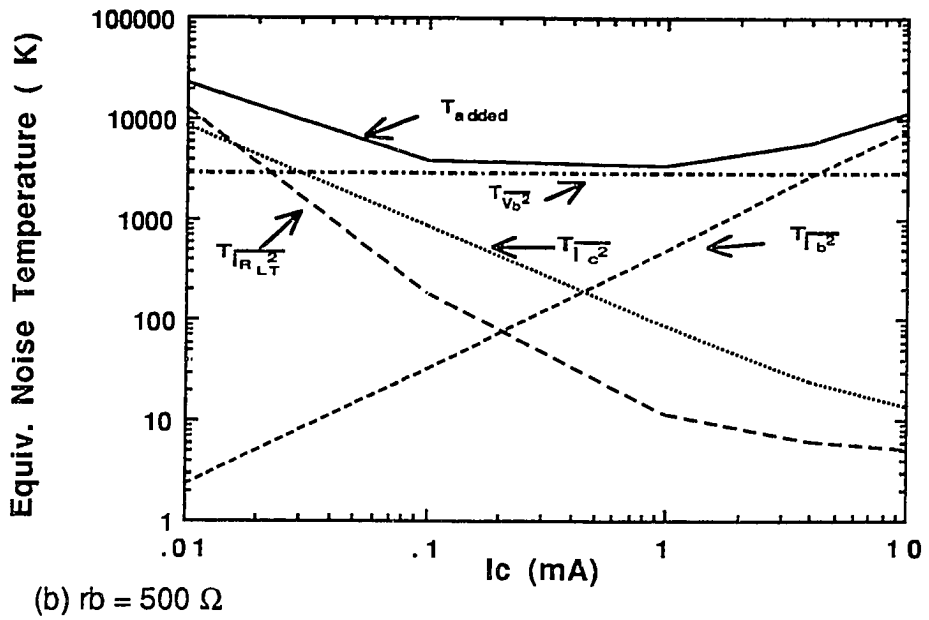
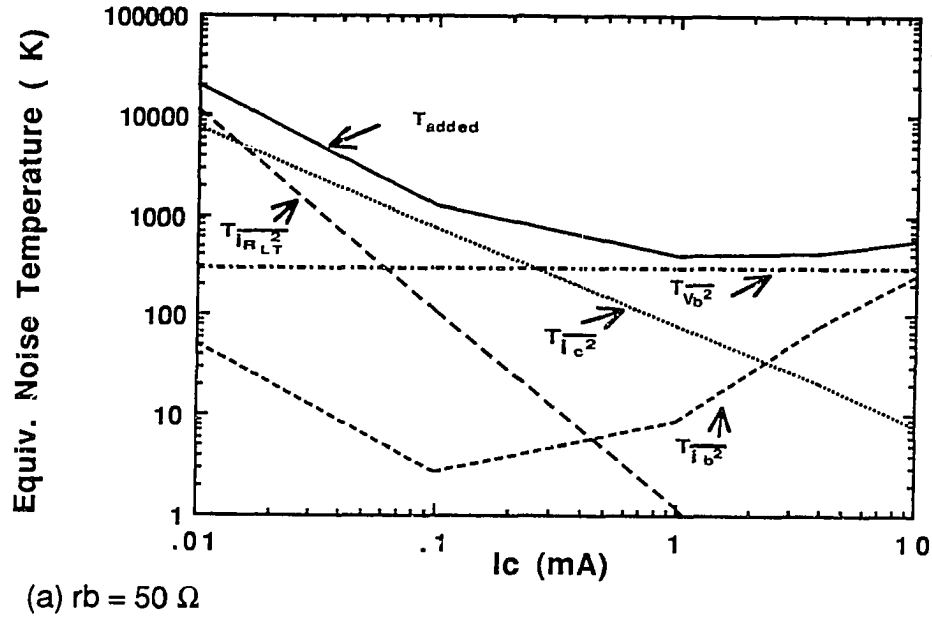
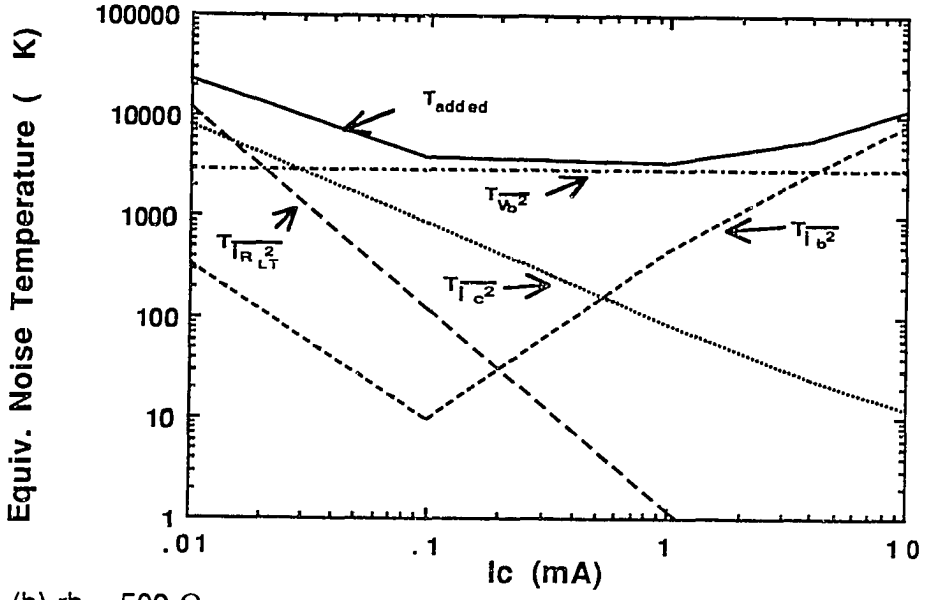


Figure 102: Equivalent noise temperature at 100 Hz at the input of a CB amplifier ($R_S = 50\Omega$; $R_C = 5\text{K}\Omega$; $R_L = 10\text{K}\Omega$; $\beta_0(I_C = 1\text{mA}) = 700$).

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(a) rb = 50 Ω



(b) rb = 500 Ω

Figure 103: Equivalent noise temperature at 100 Hz at the input of a CC amplifier ($R_S = 50\Omega$; $R_C = 5\text{K}\Omega$; $R_L = 10\text{K}\Omega$; $\beta_0(I_C = 1\text{mA}) = 700$).

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Table 41: Main Contributors to T_{added} for Various Regimes of I_C

I_C	Main Contributor	Reasons
$< 500\mu$A	$T_{\overline{i_c^2}}$, $T_{\overline{i_{R_{LT}}^2}}$	Low gain at low I_C's. Output noise referred to input > noise caused by input source.
0.5mA $\leq I_C \leq$ 5mA	$T_{\overline{v_b^2}}$	$\overline{v_b^2}$ quantifies thermal noise in r_b. Since r_b is always in series with the input signal, its contribution is added directly to incoming noise.
$> 5mA$	$T_{\overline{i_b^2}}$	$\overline{i_b^2} \alpha \frac{K_1 I_B^a}{f^b} + 2qI_B$. Therefore as $I_C \uparrow, I_B \uparrow$ and $T_{\overline{i_b^2}}$ grows. For freq < 1/f knee the 1/f noise is greater than the shot noise contribution.

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Variations in Transistor Parameters on T_{added}. The available transistor parameters in a simple hybrid-π model are $r_b, r_\pi, g_m, \beta_0, r_0$. As mentioned earlier, r_π, g_m and r_0 can be found from β_0 and I_C. β_0 is, however, a function of I_C. Therefore $\beta_0(I_C)$ and r_b can be varied to see the effect on T_{added}.

1. Variations in r_b. Anticipating the importance of $\overline{v_b}$ in setting the minimum noise temperature we have plotted all equivalent temperatures for $r_b = 50\Omega$ and $r_b = 500\Omega$. Effect of $\uparrow r_b$ is to $\uparrow T_{added}$ and to widen the range of I_C over which $T_{added} \sim T_{added_{min}}$.

2. Variations in β_0. This effect is shown in Figure 104. Here $\beta_1 = 100 \; \forall \; I_C$; $\beta_2 = f(I_C)$; and $\beta_3 = 2\beta_2$. β_3 is given by that of transistor model XM_1 in Table 39.

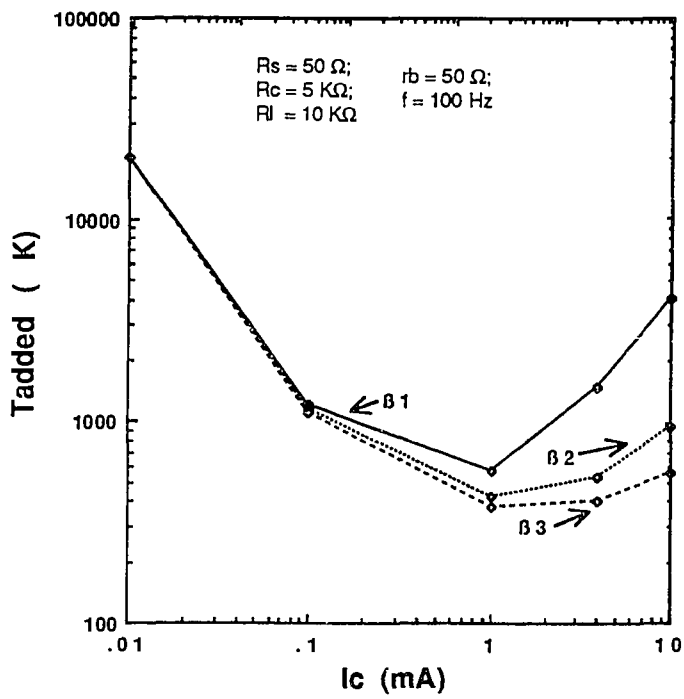


Figure 104: Sensitivity of T_{added} to variations in β_0.

T_{added} is fairly insensitive to change in β_0; at I_C= 1mA, a decrease in β_0 from 700 to 350 causes an increase in T_{added} from 390K to 420K. This can be easily explained by looking at the three regimes of I_C.

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(a) Small I_C : $I_C < 0.5mA$. $T_{added} \neq f(\beta_0)$.

For the CE transistor configuration, T_{added} can be written as:

$$\begin{aligned} T_{added} &\sim T_{\overline{i_c^2}} + T_{\overline{i^2_{R_{LT}}}}, \\ &= \left(\frac{R_S + r_b + r_\pi}{g_m r_\pi}\right) \frac{1}{4kR_S} \left(2qI_C + \frac{4kT}{R_{LT}}\right), \\ &\sim \frac{1}{g_m}\left(\frac{2qI_C}{4kR_S} + \frac{T}{R_S \cdot R_{LT}}\right) \qquad \text{for } r_\pi > R_S + r_b, \\ &\sim \frac{I_C}{V_T}\left(\frac{2qI_C}{4kR_S} + \frac{T}{R_S R_{LT}}\right) \qquad \text{for } g_m = \frac{I_C}{V_T}. \end{aligned}$$

(b) I_C regimes 2 and 3 can be combined: $I_C > 0.5mA$.

For CE and CB amplifiers:

$$\begin{aligned} T_{added} &\simeq T_{\overline{v_b^2}} + T_{\overline{i_b^2}} \\ &= T \cdot \frac{r_b}{R_S} + \frac{(R_S + r_b)^2}{4kR_S}\left[\frac{K_1 I_B^a}{f^b} + 2qI_B\right]. \end{aligned}$$

The first term is generally the dominant term, that is, when β is large enough such that $I_B = I_C/\beta_F$ is small. However when β becomes low enough such that $T_{\overline{i_b^2}} \sim T_{\overline{v_b^2}}$, then Regime 2 becomes dominated by $T_{\overline{i_b^2}}$ as Regime 3 in general is. The impact of β_0 variation is negligible as long as β_0 is large enough that $I_B < 10\mu A$. If $I_0 > 10\mu A$ then $T_{\overline{i_b^2}}$ quickly becomes the dominant term in T_{added}. This lead us to a closer examination of $T_{\overline{i_b^2}}$ or $\overline{i_b^2}$ which is composed of flicker noise and shot noise.

Role of $T_{\overline{i_b^2}}$; importance of $1/f$ noise. Figure 105 shows the equivalent temperature due to $\overline{i_b^2}$ referred to the input of the transistor (for CE and CB configurations). $T_{\overline{i_b^2}}$ is plotted over frequencies from 10 Hz to 10 KHz for values of I_B from $0.01\mu A$ to $10\mu A$. R_S is assumed to be 50Ω and r_b is taken to be 50Ω. This transistor has a $1/f$ knee, or frequency beyond which $1/f$ noise is not the dominant source of noise, of $\sim$ 1 KHz to 5 KHz depending on I_B. From 10 KHz on the shot noise in I_B dominates

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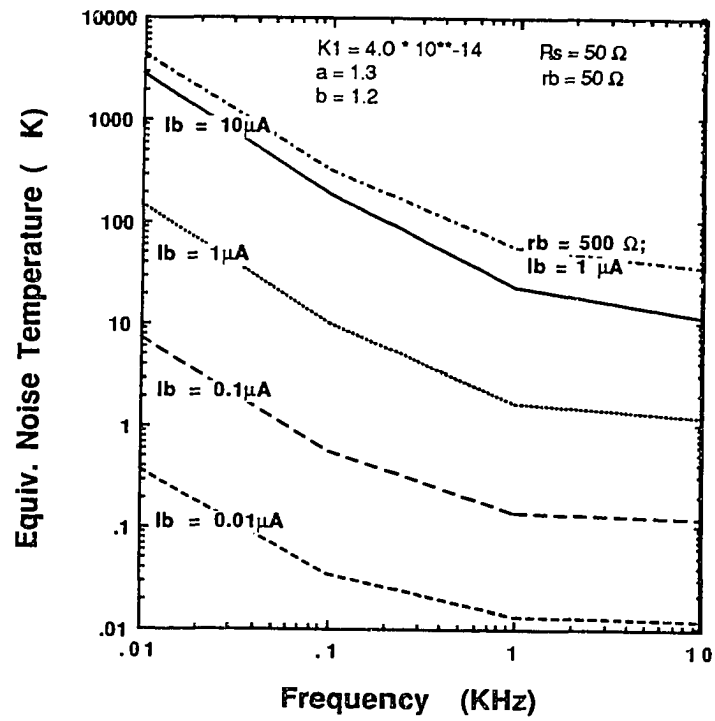


Figure 105: $T_{\frac{i_n^2}{i_b^2}}$ plotted vs. frequency for several values of I_B.

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as the major source of noise. In the dashed line is plotted $T_{\overline{i_b^2}}$ for $I_B = 1\mu A$ and $r_b = 500\Omega$. Once again, the importance of keeping r_b low is seen.

In Figure 106 $T_{\overline{i_b^2}}$ and T_{added} are plotted vs I_C at three frequencies, f=10 Hz, 100 Hz and 1KHz for a CE amplifier. Thus we see that at 1 KHz, the $1/f$ noise contribution to T_{added} is negligible even at I_C=10mA, whereas at 10 Hz, $T_{\overline{i_b^2}}$ is on the order of $T_{\overline{v_b^2}}$ by $I_C = 0.3mA$ and becomes the dominates source of noise by $I_C = 3mA$.

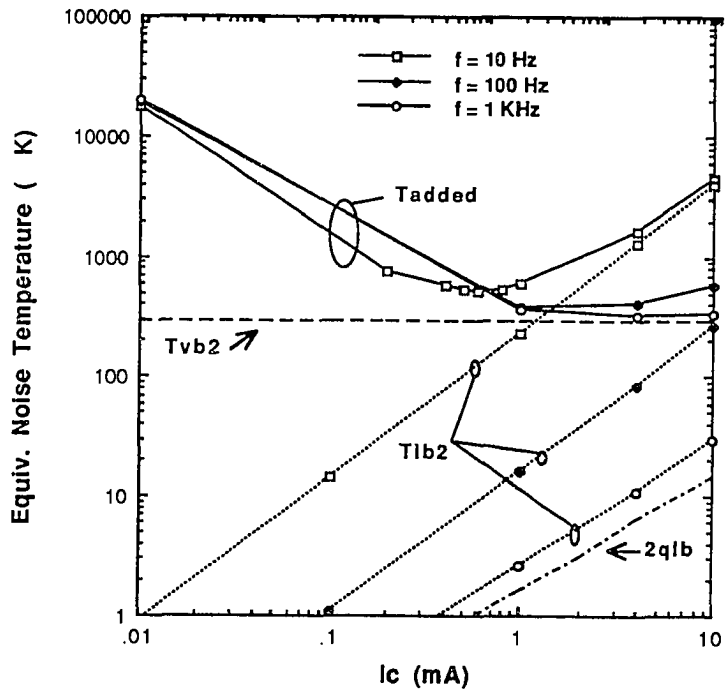


Figure 106: T_{added} and $T_{\overline{i_b^2}}$ vs. frequency for several values of I_B.

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B.4.3 Noise Temperature Performance For Various Sources and Load Impedances - Optimum Source and Load Conditions

Figures 107, 108, and 109 show amplifier temperature for several values of R_S where Figures 101, 102, and 103 of Section B.4.2 gave the equivalent noise temperatures for the CE, CB, and CC configurations when driven by a 50Ω source. The minimum noise temperature is achieved at a value of I_C where the equivalent temperature due to the thermal noise of r_b is the dominant contributor to the overall amplifier temperature.

As the source impedance is increased, we begin to see several trends in the value and makeup of the amplifier's equivalent temperature: (1) T_{amp} decreases; (2) the value of I_C where T_{amp} is minimized decreases; (3) the contribution to T_{amp} from i_b^2 grows. Eventually as R_S grows, $T_{\overline{i_b^2}} > T_{\overline{r_b^2}}$. As R_S increases, $T_{\overline{i^2_{R_L}}}$ and, to a lesser extent, $T_{\overline{i_c^2}}$ dominates T_{amp}.

To achieve low amplifier noise temperatures at low I_C the dominant contribution to T_{amp}, $T_{\overline{i^2_{R_L}}}$, must be kept small. The requirements on R_{bias} and R_L to keep $T_{\overline{i^2_{R_L}}}$ of the same order of magnitude as the other components of T_{amp} depend on which transistor configuration is being used as will be seen next.

Figure 107 shows the noise temperature of a CE amplifier driven by source resistances of 50Ω, 5K, and 20K. Note that $T_{\overline{i^2_{R_L}}}$ is the dominant noise source only when $R_S \geq 20$K at which point I_C (for $T_{amp_{min}}$) $\sim 10\mu$A. Table 42 lists the noise contributions to total temperature. As R_S increases, the transistor can be operated at lower I_C's while keeping T_{amp} at a minimum. Eventually, the noise of the load dominates T_{amp} due to the low power gain of the amplifier. As R_{in} of the CE amplifier increases with decreasing I_C, we continue to get power match on the input of the device, although the actual power gain is proportional to I_C, as shown in Figure 96.

Figure 108 shows the noise temperature of a CB amplifier driven by two source resistances, $R_S = 50\Omega$ and $R_S = 5$K. The noise of the load and bias resistors are dominant noise sources at low I_C; to minimize this circuit contribution both resistors must be increased. Note that $T_{\overline{i^2_{R_{LT}}}}$ is the dominant noise source at T_{min} for $R_S \geq 5$K irrespective of R_C and R_L. Increasing R_S does not decrease the value of I_C at T_{min}.

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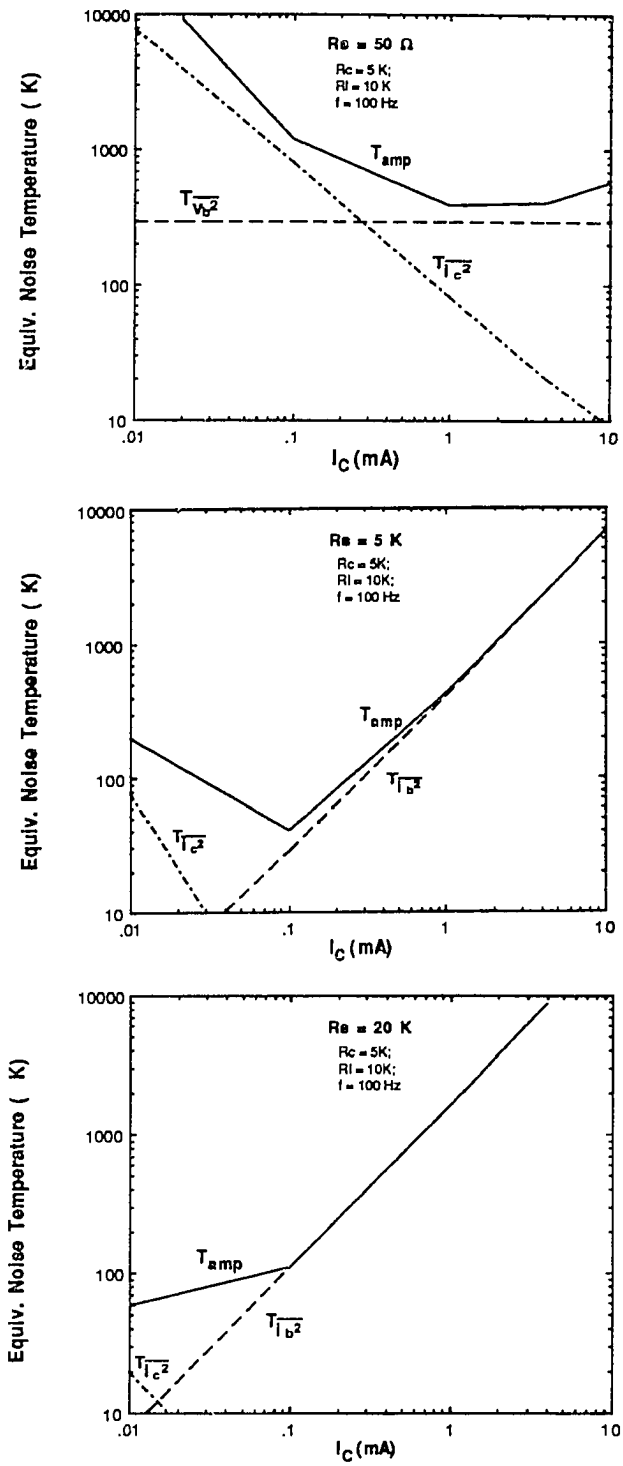


Figure 107: T_{added} vs. I_C for several values of R_S for a CE amplifier.

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Table 42: Noise Temperature Contributors for a CE Amplifier

R_S	T_{min}	$I_{C_{opt}}$	Dominant Noise Contributors
50Ω	380K	1mA	$T_{\overline{r_b^2}} = 290\text{K}$; $T_{\overline{i_c^2}} = 80\text{K}$
5K	40K	0.1mA	$T_{\overline{i_b^2}} = 28\text{K}$; $T_{\overline{i_c^2}} = 8.4\text{K}$; $T_{\overline{r_b^2}} = 2.9\text{K}$
20K	59K	10μA	$T_{\overline{i_{R_L}^2}} = 30\text{K}$; $T_{\overline{i_c^2}} = 20\text{K}$

Table 43 lists the major contributors to the noise temperature of a CB amplifier and brings out a problem with the use of the CB amplifier. To minimize the amplifier temperature, high values of R_C (high V_{CC}) must be used, in addition we have the choice of keeping the load resistor large or the noise contribution due to the second stage amplifier low.

Table 43: Noise Temperature Contributors for a CB Amplifier

R_S	R_C	R_L	T_{min}	$I_{C_{opt}}$	Dominant Noise Contributors
50Ω	5K	10K	400K	1mA	$T_{\overline{r_b^2}} = 290\text{K}$; $T_{\overline{i_c^2}} = 79\text{K}$
5K	5K	10K	520K	0.1mA	$T_{\overline{i_{R_L}^2}} = 480\text{K}$; $T_{\overline{i_b^2}} = 28\text{K}$
5K	20K	20K	200K	0.1mA	$T_{\overline{i_{R_L}^2}} = 160\text{K}$; $T_{\overline{i_b^2}} = 28\text{K}$

Figure 109 plots the noise temperature of a CC amplifier driven by $R_S = 50\Omega$, 5K, and 20K. Here also the bias and load resistors must have large values in order that T_{amp} be determined by the device and not the circuit. Here note that for all R_S, $T_{\overline{i_{R_{LT}}^2}}$ and $T_{\overline{i_b^2}}$ are the two dominant noise sources at T_{min}. By increasing R_E and R_L, $T_{\overline{i_{R_{LT}}^2}}$ can be reduced, enabling T_{amp} to decrease as R_S is increased. Table 44 lists the major contributors to the noise temperature of the CC amplifier. The value of R_E and R_L required to minimize their contribution are very reasonable. The choice of 26Ω for R_L was intended to maximize power gain as shown in Figure 99. For $R_E = 5\text{K}$ and $I_C = 1\text{mA}$, R_{out} is 30Ω as shown in Figure 98. Therefore, setting $R_L = R_{out}$

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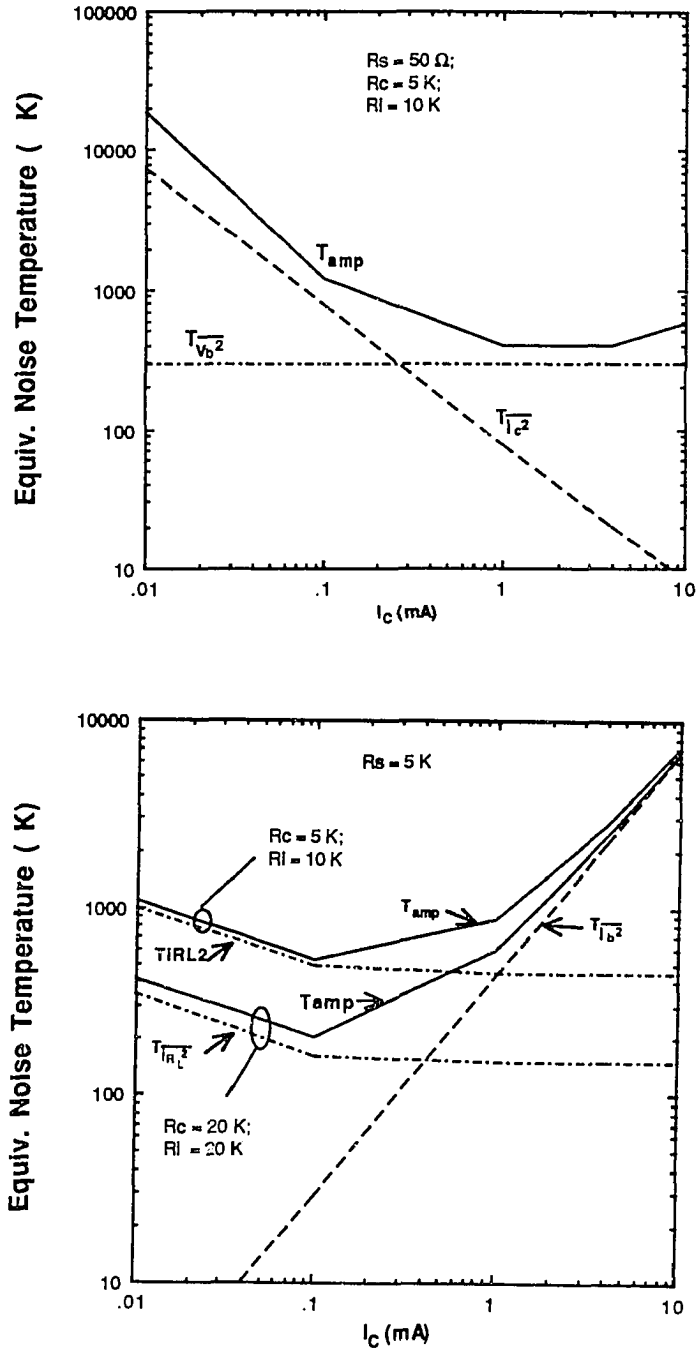


Figure 108: T_{added} vs. I_C for several values of R_S for a CB amplifier.

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Table 44: Noise Temperature Contributors for a CC Amplifier

R_S	R_E	R_L	T_{min}	$I_{C_{opt}}$	Dominant Noise Contributors
50Ω	5K	26Ω	400K	4mA	$T_{\overline{r_b^2}} = 290\text{K}$; $T_{\overline{i_b^2}} = 76\text{K}$
5K	1K	26Ω	200K	0.1mA	$T_{\overline{i_{R_L}^2}} = 160\text{K}$; $T_{\overline{i_b^2}} = 25\text{K}$
5K	5K	5K	38K	0.1mA	$T_{\overline{i_b^2}} = 25\text{K}$; $T_{\overline{i_c^2}} = 8.3\text{K}$
20K	5K	5K	67K	$10\mu A$	$T_{\overline{i_{R_L}^2}} = 40\text{K}$; $T_{\overline{i_c^2}} = 20\text{K}$

maximizes the power delivered to the load. If R_L is indeed a resistor and not the input to a CB transistor, its noise contribution will swamp T_{amp}.

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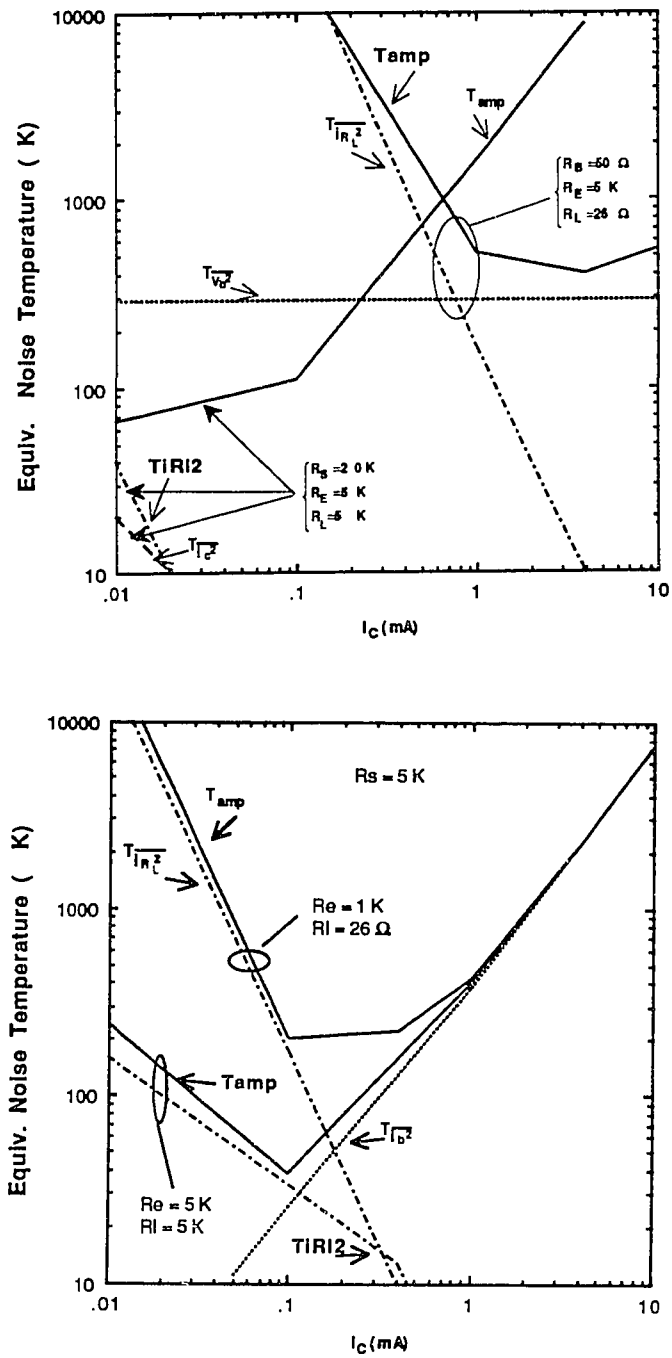


Figure 109: T_{added} vs. I_C for several values of R_S for a CC amplifier.

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Appendix C

Filter Appendix

C.1 Program Listing

A listing of the filter analysis program *syst.for* follows.

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```
c                       SYST.FOR
        IMPLICIT COMPLEX (Y)


c       ARRAYS CREATED BY SUBROUTINE INIT
        DIMENSION FR(200), SIGNL(200), H(6)

c       ARRAYS CREATED BY YPARA
        DIMENSION YA(2,2), YT(2,2,200)

c       ARRAYS CREATED BY YCASC
        DIMENSION VDIVSA(200), VDIVAB(200), VDIVBC(200)
        DIMENSION VGAINA(200), VGAINB(200), VGAINC(200)
        DIMENSION YINA(200),YINB(200),YINC(200)
        DIMENSION YOUTA(200),YOUTB(200)

c       ARRAYS CREATED BY NOISE
        DIMENSION VN2(200),CN2(200)
        DIMENSION VN2VV(200),CN2AA(200),VT2(200),CT2(200)
        DIMENSION VFILT(200),CFILT(200)
        DIMENSION QVR1(200),QVR3(200),QVR4(200),QVCN(200),QVVN(200)
        DIMENSION QCR3(200),QCR4(200),QCCN(200),QCVN(200)

c       ARRAYS CREATED BY CROSSCORR
        DIMENSION CTVCF(200,3)
        DIMENSION QVCR3(200,3),QVCR4(200,3),QVCCN(200,3),QVCVN(200,3)
        DIMENSION VNTOT(200,3)

c       ARRAYS CREATED IN THE MAIN PROGRAM
        DIMENSION Vv1(200),vv2(200),vv3(200),vv4(200)

        DIMENSION YSRCE(200,3)
        DIMENSION VTFILTA(200),VTFILTB(200),VTFILTC(200)
        DIMENSION VSRCE(200), VLOAD(200)

        dimension vnt1(200),vnt2(200),vnt3(200)
        dimension vn1in(200),vn2in(200),vn3in(200),vn4in(200)

        DIMENSION PWSG(200,4),PWNS(200,4),VIMAG(200,4)
        DIMENSION FTOT(200,3),TOTNF(200,3),TEMPTOT(200,3)
        DIMENSION TEMPAV(4),TEMPMB(4)


c       ARRAYS USED FOR TESTING MAIN PROGRAM
        DIMENSION VRA(200),VRB(200),VRC(200)
        DIMENSION VNB(200),VNC(200)


cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c       VARIABLES USED:
c               REAL: VNSRCE,VNLD,
c                     FBW
c
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc


        CHARACTER FNAME*10
        WRITE(5,18)
18      FORMAT(T5,'ENTER OUTPUT DATA FILENAME.')
        READ (6,50) FNAME
50      FORMAT(A10)
```



```
        OPEN(UNIT=8, STATUS='NEW', FILE=FNAME)
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c       UNIT 10 WILL BE USED TO STORE ALL PWSG,PWNS DATA TO BE
c               PLOTTED WITH DISSPLA USING PWRPLOT.FOR
c       UNIT 11 --- NOISE DATA   PLOTTED WITH NOISEPLOT.FOR
c       UNIT 12 --- VV1,..VV4 AND VN1IN,VN4IN   WITH VVVNPLOT.FOR
c       UNIT 13 --- TERMR1,TERMR3 ... TERMIN   WITH COMPLOT.FOR and LINPLOT
c       UNIT 14 --- FILTER DATA, NOISE DATA (CUTLF), SNR DATA TO BE USED
c                   IN RUNNING TRYPLOT.FOR WHICH OUTPUTS TO DISSPLA
c                   BOXED OFF AREAS, LEYENDS, ETC.
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

        WRITE(5,210)
        WRITE(8,210)
210     FORMAT(20X,'BASEBAND SYSTEM ANALYSIS')

        CALL INIT(NUMF,YS,YLD,FR,SIGNL,FBW,H)


        CALL FILT(FO,HO,R1,R3,R4,C2,C5)
c               Number 1 write statement to units 10,11,13,14
c                   filter data


        CALL YPARA(FR,NUMF,R1,R3,R4,C2,C5,YA,YT)


        CALL YCASC(YT,YS,YLD,NUMF,FR,VGAINA,VGAINB,VGAINC,VDIVSA,
     1   VDIVAB,VDIVBC,YINA,YINB,YINC,YOUTA,YOUTB)


        WRITE(10,25) NUMF,YS,YLD
        WRITE(11,25) NUMF,YS,YLD
        WRITE(12,25) NUMF,YS,YLD
        WRITE(13,25) NUMF,YS,YLD
25      FORMAT(5X,I5,5X,E10.2,2X,E10.2,5X,E10.2,2X,E10.2)
c               Number 2 write statement to units 10,11,12,13



        DO 145 K = 1, NUMF

        VV1(K) = SIGNL(K) * VDIVSA(K)
        VV2(K) = VV1(K) * VGAINA(K)
        VV3(K) = VV2(K) * VGAINB(K)
        VV4(K) = VV3(K) * VGAINC(K)

145     CONTINUE


        CALL NOISE(R1,R3,R4,C2,C5,FR,FBW,NUMF,VN2,CN2,
     1      VN2VV,CN2AA,VT2,CT2,CFILT,VFILT,
     1      QVR1,QVR3,QVR4,QVCN,QVVN,QCR3,QCR4,QCCN,QCVN)
c                   Number 3 write statement to Units 10,11,13,14
c                       cutoff for low freq. noise evaluation CUTLF

        DO 215 I = 1, NUMF
        YSRCE(I,1) = YS
        YSRCE(I,2) = YOUTA(I)
        YSRCE(I,3) = YOUTB(I)
215     CONTINUE
```


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syst.for

```
      CALL CROSSCORR(YSRCE,R1,R3,R4,C2,C3,FR,NUMF,FBW,
     1     VN2,CN2,VN2VV,CN2AA,VT2,CT2,CTVCF,
     1     QVCR3,QVCR4,QVCCN,QVCVN,VNTOT)

      DO 220 I = 1, NUMF
      VTFILTA(I) = CFILT(I)/(CABS(YSRCE(I,1))**2)+VFILT(I)+CTVCF(I,1)
      VTFILTB(I) = CFILT(I)/(CABS(YSRCE(I,2))**2)+VFILT(I)+CTVCF(I,2)
      VTFILTC(I) = CFILT(I)/(CABS(YSRCE(I,3))**2)+VFILT(I)+CTVCF(I,3)
  220 CONTINUE

      FKT = 1.66 * (10.0**-20)
      VNSRCE = FKT/REAL(YS)
      VNLD = FKT/REAL(YLD)

      DO 147 K = 1,NUMF
      VSRCE(K) = VNSRCE * FBW
      VLOAD(K) = VNLD * FBW
  147 CONTINUE

      DO 150 K = 1, NUMF

      VN1IN(K) = VSRCE(K) * VDIVSA(K)
      VN1(K) = VN1IN(K) + (VTFILTA(K) * VDIVSA(K))
      VN2IN(K) = VN1(K) * VGAINA(K)
      VN2(K) = VN2IN(K) + (VTFILTB(K) * VDIVAB(K))
      VN3IN(K) = VN2(K) * VGAINB(K)
      VN3(K) = VN3IN(K) + (VTFILTC(K) * VDIVBC(K))
      VN4IN(K) = (VN3(K) * VGAINC(K)) + VLOAD(K)

  150 CONTINUE

      WRITE(5,300)
      WRITE(8,300)
  300 FORMAT(5X,/,5X,'Freq',6X,'Vsrce',6X,'Vload',
     1    4X,'VTFILTA',4X,'VTFILTB',4X,'VTFILTC')

      DO 302 K = 1,NUMF,20
      write(5,301) FR(K),VSRCE(K),VLOAD(K),VTFILTA(K),
     1    VTFILTB(K),VTFILTC(K)
      write(8,301) FR(K),VSRCE(K),VLOAD(K),VTFILTA(K),
     1    VTFILTB(K),VTFILTC(K)
  301 FORMAT(1X,F6.1,3X,5(E9.2,2X))
  302 CONTINUE

C     WRITING ON UNIT 11 TO BE READ BY NOISEPLOT.FOR
C           4th write statement for unit 11.

      DO 304 K =1,NUMF
      WRITE(11,303) FR(K),VN1(K),VN2IN(K)
  303 FORMAT(2X,F9.2,2(2X,E10.2))
  304 CONTINUE

      write(5,305)
      WRITE(8,305)
  305 FORMAT(5X,/,5X,'Frequency',8x,'VV1',8x,'VN1IN')

      write(5,310) (FR(K),VV1(K),VN1IN(K),K=1,NUMF,20)
      write(8,310) (FR(K),VV1(K),VN1IN(K),K=1,NUMF,20)
  310 FORMAT(2X,F9.2,5X,E10.2,5X,E10.2)

      WRITE(5,315)
      WRITE(8,315)
  315 FORMAT(5X,/,5X,'Frequency',8x,'VV2',8x,'VN2IN',8X,'YINB')

      write(5,320) (FR(K),VV2(K),VN2IN(K),YINB(K),K=1,NUMF,20)
      write(8,320) (FR(K),VV2(K),VN2IN(K),YINB(K),K=1,NUMF,20)
  320 FORMAT(2X,F9.2,5X,E10.2,5X,E10.2,3X,E10.2,E10.2)

      WRITE(5,325)
      WRITE(8,325)
  325 FORMAT(5X,/,5X,'Frequency',8x,'VV3',8x,'VN3IN',8x,'YINC')

      write(5,330) (FR(K),VV3(K),VN3IN(K), YINC(K),K=1,NUMF,20)
      write(8,330) (FR(K),VV3(K),VN3IN(K), YINC(K),K=1,NUMF,20)
  330 FORMAT(2X,F9.2,5X,E10.2,5X,E10.2,E10.2)

      WRITE(5,335)
      WRITE(8,335)
  335 FORMAT(5X,/,5X,'Frequency',8x,'VV4',10x,'VN4IN')

      write(5,340) (FR(K),VV4(K),VN4IN(K),K=1,NUMF,20)
      write(8,340) (FR(K),VV4(K),VN4IN(K),K=1,NUMF,20)
  340 FORMAT(2X,F9.2,5X,E10.2,5X,E10.2)

C     WRITING ON UNIT 12 TO BE READ BY VVVNPLOT.FOR

      DO 345 K = 1,NUMF
      WRITE(12,350) FR(K),VV1(K),VN1IN(K)
  350 FORMAT(5X,F9.2,2X,E10.2,2X,E10.2)
  345 CONTINUE

      DO 355 K = 1,NUMF
      WRITE(12,360) FR(K),VV2(K),VN2IN(K)
  360 FORMAT(5X,F9.2,2X,E10.2,2X,E10.2)
  355 CONTINUE

      DO 365 K = 1,NUMF
      WRITE(12,370) FR(K),VV3(K),VN3IN(K)
  370 FORMAT(5X,F9.2,2X,E10.2,2X,E10.2)
  365 CONTINUE

      DO 375 K = 1,NUMF
      WRITE(12,380) FR(K),VV4(K),VN4IN(K)
  380 FORMAT(5X,F9.2,2X,E10.2,2X,E10.2)
  375 CONTINUE

      DO 385 K = 1,31
      VRA(K) = VV2(K)/VV1(K)
      VRB(K) = VV3(K)/VV2(K)
      VRC(K) = VV4(K)/VV3(K)
      VNB(K) = VN3IN(K)/VN2IN(K)
      VNC(K) = VN4IN(K)/VN3IN(K)
  385 CONTINUE

      WRITE(5,390)
      WRITE(8,390)
  390 FORMAT(5X,/,5X,'FREQ',7X,'VRA',8X,'VRB',8X,'VRC',
     1    8X,'VNB',8X,'VNC')

      DO 392 K = 1,31
      WRITE(5,395) FR(K),VRA(K),VRB(K),VRC(K),VNB(K),VNC(K)
      WRITE(8,395) FR(K),VRA(K),VRB(K),VRC(K),VNB(K),VNC(K)
  395 FORMAT(1X,F6.1,3X,5(E9.2,2X))
  392 CONTINUE
```


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syst.for

```
      VV1TOT = 0.0
      VV2TOT = 0.0
      VV3TOT = 0.0
      VV4TOT = 0.0
      VN1TOT = 0.0
      VN2TOT = 0.0
      VN3TOT = 0.0
      VN4TOT = 0.0

      MSTART = M(1)
      MSTOP = M(2)

      DO 383 K = MSTART,MSTOP
      VV1TOT = VV1(K) + VV1TOT
      VV2TOT = VV2(K) + VV2TOT
      VV3TOT = VV3(K) + VV3TOT
      VV4TOT = VV4(K) + VV4TOT
      VN1TOT = VN1IN(K) + VN1TOT
      VN2TOT = VN2IN(K) + VN2TOT
      VN3TOT = VN3IN(K) + VN3TOT
      VN4TOT = VN4IN(K) + VN4TOT
383   CONTINUE

      VNR1 = VV1TOT/VN1TOT
      VNR2 = VV2TOT/VN2TOT
      VNR3 = VV3TOT/VN3TOT
      VNR4 = VV4TOT/VN4TOT

      WRITE(5,387)
      WRITE(8,387)
387   FORMAT(5X,/,T28,3X,'NODE 1',6X,'NODE 2',6X,'NODE 3',6X,'NODE 4')

      WRITE(5,388) VV1TOT,VV2TOT,VV3TOT,VV4TOT
      WRITE(8,388) VV1TOT,VV2TOT,VV3TOT,VV4TOT
388   FORMAT(2X,'TOT. VOLTS SQRD',T28,4(E10.2,2X))

      WRITE(5,389) VN1TOT,VN2TOT,VN3TOT,VN4TOT
      WRITE(8,389) VN1TOT,VN2TOT,VN3TOT,VN4TOT
389   FORMAT(2X,'TOT. NOISE VOLTS SQRD',T28,4(E10.2,2X))

      WRITE(5,391) VNR1,VNR2,VNR3,VNR4
      WRITE(8,391) VNR1,VNR2,VNR3,VNR4
391   FORMAT(2X,'VNR',T28,4(E10.2,2X))

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C     WE NOW CALCULATE THE SIGNAL POWER AT EACH FREQ. K AND AT
C     EACH NODE, N, AND STORE IT IN A 2 X 2 ARRAY, PMSG(K,N) OR
C     PMSG(200,4).
C     THE SAME IS DONE FOR THE NOISE POWER AT EACH FREQ.,K, AND
C     AT EACH NODE, N. IT IS STORED IN PMNS(K,N).
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

      DO 400 K = 1,NUMF

      PMSG(K,1) = VV1(K) * REAL(YINA(K))
      PMSG(K,2) = VV2(K) * REAL(YINB(K))
      PMSG(K,3) = VV3(K) * REAL(YINC(K))
      PMSG(K,4) = VV4(K) * REAL(YLD)

      VINAG(K,1) = VV1(K) * CABS(YINA(K))
      VINAG(K,2) = VV2(K) * CABS(YINB(K))
      VINAG(K,3) = VV3(K) * CABS(YINC(K))
      VINAG(K,4) = VV4(K) * CABS(YLD)

      PMNS(K,1) = VN1IN(K) * REAL(YINA(K))
      PMNS(K,2) = VN2IN(K) * REAL(YINB(K))
      PMNS(K,3) = VN3IN(K) * REAL(YINC(K))
      PMNS(K,4) = VN4IN(K) * REAL(YLD)

400   CONTINUE

      DO 415 I = 2,4
      DO 410 K = 1,NUMF
      PIRATIO = PMSG(K,I)/PMNS(K,I)
      PRATIO = PMSG(K,I)/PMNS(K,I)

      IF(PRATIO) 405,405,407

405   FTOT(K,I) = 1.0*(10.0**10.0)
      GO TO 408
407   FTOT(K,I) = PIRATIO/PRATIO
408   TOTNF(K,I) = 10.0 * ALOG10(FTOT(K,I))
      TEMPTOT(K,I) = (FTOT(K,I)-1.0) * 290.0
410   CONTINUE
415   CONTINUE

      MSTART = M(1)
      MSTOP = M(2)
      MDIFF = MSTOP - MSTART

      DO 450 I = 2,4
      TTAVER = 0.0

      DO 420 K = MSTART,MSTOP
      TTAVER = TEMPTOT(K,I) + TTAVER
420   CONTINUE

      TEMPAV(I) = TTAVER/MDIFF
      TEMPHB(I) = (TTAVER - TEMPTOT(MSTART,I))/(MDIFF - 1)
450   CONTINUE

      WRITE(5,500)
      WRITE(8,500)
      FORMAT(5X,/,T23,'Node 1',t52,'Node 2')
500

      write(5,505)
      write(8,505)
      format(5x,/,4x,'Frequency',5x,'PMSG',7x,'PMNS',11x,'PMSG',
     1   7x,'PMNS')
505

      DO 515 K = 1,NUMF,20
      WRITE(5,510) FR(K),PMSG(K,1),PMNS(K,1),PMSG(K,2),PMNS(K,2)
      WRITE(8,510) FR(K),PMSG(K,1),PMNS(K,1),PMSG(K,2),PMNS(K,2)
      FORMAT(2X,F9.2,2X,E10.2,2X,E10.2,5X,E10.2,2X,E10.2)
510   CONTINUE
515

      WRITE(5,520)
      WRITE(8,520)
      FORMAT(5X,/,T23,'Node 3',t52,'Node 4')
520

      write(5,525)
      write(8,525)
      format(5x,/,4x,'Frequency',5x,'PMSG',7x,'PMNS',11x,'PMSG',
525
```

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```
     1   7X,'PWNS')

         DO 535 K = 1,NUMF,20
         WRITE(5,530) FR(K),PWSG(K,3),PWNS(K,3),PWSG(K,4),PWNS(K,4)
         WRITE(8,530) FR(K),PWSG(K,3),PWNS(K,3),PWSG(K,4),PWNS(K,4)
530      FORMAT(2X,F9.2,2X,E10.2,2X,E10.2,5X,E10.2,2X,E10.2)
535      CONTINUE


         WRITE(5,550)
         WRITE(8,550)
550      FORMAT(5X,/,4X,'Frequency',3X,'VIMAG(1)',3X,'VIMAG(2)',
     1    7X,'VIMAG(3)',3X,'VIMAG(4)')

         DO 555 K = 1,NUMF,20
         WRITE(5,560) FR(K),VIMAG(K,1),VIMAG(K,2),VIMAG(K,3),VIMAG(K,4)
         WRITE(8,560) FR(K),VIMAG(K,1),VIMAG(K,2),VIMAG(K,3),VIMAG(K,4)
560      FORMAT(2X,F9.2,2X,E10.2,2X,E10.2,5X,E10.2,2X,E10.2)
555      CONTINUE


         DO 620 I = 2,4
         WRITE(5,625) I
         WRITE(8,625) I
625      FORMAT(5X,/,5X,/,40X,'MODE ',I2)

         WRITE(5,600)
         WRITE(8,600)
600      FORMAT(5X,'FREQUENCY',12X,'FTOTAL',15X,'TOT NF',
     1          10X,'TEMP TOT')

         DO 605 K = 1,NUMF,10
         WRITE(5,610) FR(K),FTOT(K,I),TOTNF(K,I),TEMPTOT(K,I)
         WRITE(8,610) FR(K),FTOT(K,I),TOTNF(K,I),TEMPTOT(K,I)
610      FORMAT(5X,F9.2,9X,E10.2,9X,F10.2,9X,E10.2)
605      CONTINUE

         WRITE(5,615) TEMPAV(I),TEMPHB(I)
         WRITE(8,615) TEMPAV(I),TEMPHB(I)
615      FORMAT(5X,/,15X,'AVERAGE TEMP. IN BAND = ',E10.2,/,
     1          15X,'AVERAGE TEMP. (w/o 0-50 Hz) = ',E10.2)

620      CONTINUE


C        WRITING ON UNIT 10 TO BE READ BY PWRPLOT.FOR
C                3rd write statement on unit 10.

         DO 518 K = 1,NUMF
         WRITE(10,513) FR(K),PWSG(K,1),PWNS(K,1),PWSG(K,2),PWNS(K,2)
513      FORMAT(2X,F9.2,2X,E10.2,2X,E10.2,5X,E10.2,2X,E10.2)
518      CONTINUE

         DO 540 K = 1,NUMF
         WRITE(10,545) FR(K),PWSG(K,3),PWNS(K,3),PWSG(K,4),PWNS(K,4)
545      FORMAT(2X,F9.2,2X,E10.2,2X,E10.2,5X,E10.2,2X,E10.2)
540      CONTINUE

         DO 580 K = 1,NUMF
         WRITE(10,585) FR(K),VIMAG(K,1),VIMAG(K,2),VIMAG(K,3),VIMAG(K,4)
585      FORMAT(2X,F9.2,2X,E10.2,2X,E10.2,5X,E10.2,2X,E10.2)
580      CONTINUE
```

syst.for

```
C        WRITING ON UNIT 13 TO BE READ BY COMPLOT
C                number 4 write statement to unit 13 (complot.for)
         DO 590 I = 2,4
         WRITE(13,595) TEMPAV(I),TEMPHB(I)
595      FORMAT(5X,E10.2,5X,E10.2)
590      CONTINUE


         CALL SNR(NUMF,FR,M,PWSG,PWNS)
C                Number 4 write statement to unit 10.

         CALL COMPNOISE(NUMF,FR,FBW,YSRCE,YLD,VSRCE,VLOAD,YOUTA,
     1    YOUTB,YINB,YINC,VGAINA,VGAINB,VGAINC,VDIVSA,VOIVAB,VDIVBC,
     1    QVR1,QVR3,QVR4,QVCN,QVVN,QCR3,QCR4,QCCN,QCVN,CN2AA,VN2VV,
     1    QVCR3,QVCR4,QVCCN,QVCVN)
C                Number 5 write statement to unit 13 (Complot.for).

         CALL NF(NUMF,FR,M,YSRCE,VNTOT,VGAINA,VGAINB,VGAINC,
     1          YINA,YINB,YINC)



         STOP
         END



         SUBROUTINE INIT(NUMF,YS,YLD,FR,SIGNL,FBW,M)

         IMPLICIT COMPLEX (Y)
         DIMENSION FMARK(6),M(6),PD(6)
         DIMENSION FR(200),SIGNL(200)

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C        THIS DIMENSIONS ALL ARRAYS WHICH DEPEND ON NUMF:
C                the number of frequencies
C
C        VARIABLES USED:
C                FBW - BANDWIDTH OF EACH SAMPLE
C                FMAX - MAX FREQ WISHED TO BE EVALUATED
C                NUMFB - MAX NUMBER OF FREQ, IE. MAX ARRAY SIZE ALLOWED
C                NUMFA - MAX NUMBER OF FREQ'S NECESSARY TO INCLUDE
C                        FMAX.
C                NUMF - ARRAY SIZE SET
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

         WRITE(5,213)
         WRITE(8,213)
213      FORMAT(5X,/,20X,'POWER INITIALIZATION')

         TYPE 200
200      FORMAT(5X,'ENTER RS AND RLD IN OHMS:')
         ACCEPT *, RS, RLD

C        RS = 50.0
C        RLD = 10000.0

         GS = 1.0/RS
         BS = 0.0
         GLD = 1.0/RLD
```

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syst.for


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      BLD = 0.0
      YS = CMPLX(GS,BS)
      YLD = CMPLX(GLD,BLD)

      WRITE(5,203) RS,RLD
      WRITE(8,203) RS,RLD
203   FORMAT(5X,/,15X,'Rs =',F8.2,5X,'Rload =',F10.2)


C     TYPE 680
C680  FORMAT(5X,'ENTER BANDWIDTH OF EACH BIN, FBW:')
C     ACCEPT *, FBW

C     TYPE 681
C681  FORMAT(5X,'ENTER FMAX:')
C     ACCEPT *, FMAX

      FBW = 50.0

      FMAX = 9550.0

      FCSTART = FBW/2.0

      FINTMA = (FMAX - FCSTART)/FBW
      INTMA = INT(FINTMA)
      DIFFA = FINTMA - INTMA
      IF(DIFFA - 0.5) 670,670,675
670   NUMFA = INTMA + 1
      GO TO 678
675   NUMFA = INTMA + 2
678   CONTINUE

      NUMFB = 200
      NUMF = MIN0(NUMFA,NUMFB)
      FCSTOP = FBW * (NUMF - 1)   +  FCSTART
      BANDEND = FCSTOP + (0.5 * FBW)

      WRITE(5,692) FBW
      WRITE(8,692) FBW
692   FORMAT(5X,/,5X,'WARNING:',2X,'THREE MARKS CANNOT BE CONTAINED IN',
    1   1X,'A BIN OF WIDTH',F9.2)

C     TYPE 690
C690  FORMAT(5X,'ENTER THE BEGIN. AND END OF 3 SIGNALS:',/,
C   1    5X,'EG: 0,1550,2450,5550,6450,9550')
C     ACCEPT *, FMARK(1),FMARK(2),FMARK(3),FMARK(4),FMARK(5),FMARK(6)

      FMARK(1) =    0.0
      FMARK(2) = 1550.0
      FMARK(3) = 2450.0
      FMARK(4) = 5550.0
      FMARK(5) = 6450.0
      FMARK(6) = 9550.0

C     FMARK(1) SETS THE BAND BEGINNING AND END FOR EACH SIGNAL




CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C     VARIABLES USED:
C             REAL:    FINTMA,DIFFA
C                      RS,BS,GS,RLD,BLD,GLD,
C                      PWIN,PINTA,PINTB,PCS1,PCS2
C                      BWS,BWA,BWB,BWCS1,BWCS2
C                      FBW,FMAX,FCSTOP,BANDEND
C                      FRW,RANGE,DIFF
C                      STARTB,DELTA,ENDBIN,EPSILON,GAMMA
C                      PDF,PDR
C             COMPLEX: YS,YLD
C             INTEGERS:INTMA
C                      NUMFA,NUMFB,NUMF
C                      IRANGE,IBIN,MSTART,MSTOP,MBEG
C             ARRAYS:  DIMENSIONED ABOVE
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC



      TYPE 205
205   FORMAT(5X,'ENTER WANTED SIGNAL POWER,INTERFERER A POWER,',
    1  1x,'INTERFERER B POWER, IN *MICRO*watts. ')
      ACCEPT *, PPWIN, PPINTA,PPINTB

      PWIN = PPWIN * (10.0**-6)
      PINTA = PPINTA * (10.0**-6)
      PINTB = PPINTB * (10.0**-6)

      BWS = FMARK(2) - FMARK(1)
      BWA = FMARK(4) - FMARK(3)
      BWB = FMARK(6) - FMARK(5)

      PCS1 = 0.0
      PCS2 = 0.0
      BWCS1 = FMARK(3) - FMARK(2)
      BWCS2 = FMARK(5) - FMARK(4)

      PD(1) = PWIN/BWS
      PD(2) = PCS1/BWCS1
      PD(3) = PINTA/BWA
      PD(4) = PCS2/BWCS2
      PD(5) = PINTB/BWB


CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C     THE INITIAL POWER AND BANDWIDTHS HAVE BEEN ENTERED
C     THE ARRAY PD(1) CONTAINS THE POWER DENSITY (WATTS/HZ) FOR EACH
C             SIGNAL TYPE:
C                     WANTED SIGNAL
C                     CHANNEL SPACE 1
C                     INTERFERER A
C                     CHANNEL SPACE 2
C                     INTERFERER B
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

      DO 700 K = 1,NUMF
      FR(K) = FBW * (K-1) + FCSTART
700   CONTINUE

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C     THE FREQUENCY ARRAY - FR(K) - CONTAINS THE CENTER FREQUENCIES OF
C             EACH SAMPLE ( OR BIN) INTO WHICH WE SHALL DIVIDE THE
```


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syst.for 6

```
C              SPECTRUM.
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

C       WE NOW CALCULATE THE BIN NUMBER - OR FREQ SAMPLE- INTO
C               WHICH THESE FMARK'S FALL

        DO 710 I = 1,6

        FRW = FMARK(I)
        RANGE = (FRW - FCSTART)/FBW
        IRANGE = INT(RANGE)
        DIFF = RANGE - IRANGE
        IF(DIFF - 0.5) 715,715,720
715     IBIN = IRANGE + 1
        GO TO 730
720     IBIN = IRANGE + 2
730     CONTINUE
        H(I) = IBIN

710     CONTINUE

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C       FMARK(1) IS IN BIN H(1) = 1 - OR FREQ SAMPLE 1
C
C       FMARK(6) IS IN BIN H(6)
C
C       WE USE THIS TO CALCULATE THE POWER DENSITY AT THE BAND BEGINNING
C               AND END - WHERE WE HAVE  A CHANGE FROM PD(1) TO PD(2)
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

        DO 740 I = 1,5,2
        MAR = H(I)
        ENDBIN = FR(MAR) + (FBW/2.0)
        EPSILON = ENDBIN - FMARK(I)
        SIGNL(MAR) = (PD(I) * EPSILON)/ REAL(YS)
740     CONTINUE

        DO 735 I = 2,6,2
        MAR = H(I)
        STARTB = FR(MAR) - (FBW/2.0)
        DELTA = FMARK(I) - STARTB
        J = I - 1
        SIGNL(MAR) = PD(J) * DELTA / REAL(YS)
735     CONTINUE

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C       TO CALCULATE THE CORRECT VOLTAGE SQRD LEVEL IF ONE SIGNAL
C               RISES AND FALLS IN THE SAME BIN.
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

        DO 741 I = 1,5,2
        J = I + 1
        IF (H(I).EQ.H(J)) GO TO 742
        GO TO 744
742     MAR = H(I)
        GAMMA = FMARK(J) - FMARK(I)
        SIGNL(MAR) = (PD(I) * GAMMA)/REAL(YS)
744     CONTINUE
741     CONTINUE

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C       TO CALCULATE THE CORRECT VOLTAGE SQRD IF 2 SIGNALS:
C               ONE FALLS
C               NEXT RISES
C                       IN THE SAME BIN
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

        DO 736 I = 2,4
        K = I + 1
        IF (H(I).EQ.H(K)) GO TO 738
        GO TO 737
738     MAR = H(I)

C       POWER DENSITY DUE TO FALLING EDGE

        STARTB = FR(MAR) - (FBW/2.0)
        DELTA = FMARK(I) - STARTB
        J = I - 1
        PDF = PD(J) * DELTA

C       POWER DENSITY DUE TO RISING EDGE

        ENDBIN = FR(MAR) + (FBW/2.0)
        EPSILON = ENDBIN - FMARK(K)
        PDR = (PD(K) * EPSILON)

        SIGNL(MAR) = (PDF + PDR)/REAL(YS)
737     CONTINUE
736     CONTINUE

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C       NOW WE HAVE CALCULATED THE SIGNAL IN VOLTS SQRD AT THE BAND
C               EDGES.
C       WE NOW LOAD THE SIGNAL LEVEL IN VOLTS * VOLTS AT EACH OF
C               THE FREQUENCIES - FR(K),  K NOT A BAND EDGE
C       WE MUST TAKE INTO ACCOUNT THE DIFFERENT POWER DENSITIES
C               ACCORDING TO THE DIFFERENT SIGNAL LEVELS, FOR
C               THIS REASON WE DIVIDE THE DO LOOP INTO
C               6 REGIONS:
C                       1       TO      H(1) - 1
C                   H(1)+1      TO      H(2) - 1
C                   H(2)+1      TO      H(3) - 1
C                   H(3)+1      TO      H(4) - 1
C                   H(4)+1      TO      H(5) - 1
C                   H(5)+1      TO      H(6) - 1
C
C                       THE FIRST CASE IS NECESSARY
C               to handle the case where H(1)- the rising edge
C               edge of the wanted signal is not in the first
C               bin, and therefore SIGNL(1) has not been
C               found, we must set all SIGNL(I)  I less than H(1)
C               (the bin number of the rising edge, FMARK(1) )
C               or I from 1 to H(1) - 1 to  0.0
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
```

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```
      MBEG = M(1) - 1
      DO 745 I = 1, MBEG
      SIGNL(I) = 0.0
745   CONTINUE


      DO 750 I = 1,5

      MSTART = M(I) + 1
      J = I + 1
      MSTOP = M(J) - 1

      DO 755 K = MSTART,MSTOP
      SIGNL(K) = PD(I) * FBW / REAL(YS)
755   CONTINUE

750   CONTINUE


      WRITE(5,215)
      WRITE(8,215)
215   FORMAT(5X,/,5X,'BASEBAND SPECTRUM (0 - 10KHZ) will be',
     1  1x,' represented by signal and noise',/,5X,'levels at the',
     1  1x,' carrier frequencies given below.')

      write(5,220)pwin,bws
      write(8,220)PWIN,BWS
220   FORMAT(5X,/,5X,'Wanted Signal:',T25,'PWIN =',E10.2,T44,'Watts',
     1  4X,' BWs =',f9.2,2x,'Hz')

      WRITE(5,235) PSC1,BWCS1
      WRITE(8,235) PSC1,BWCS1
235   FORMAT(5X,/,5X,'Channel Space:',T25,'PSC1 =',E10.2,T44,'Watts',
     1  4X,' BWCS1 =',f9.2,2x,'Hz')

      WRITE(5,245) PINTA,BWA
      WRITE(8,245) PINTA,BWA
245   FORMAT(5X,/,5X,'Interferer A:',T25,'PINTA =',E10.2,T44,'Watts',
     1    4x,' BWa =',f9.2,2x,'Hz')

      WRITE(5,260) PSC2,BWCS2
      WRITE(8,260) PSC2,BWCS2
260   FORMAT(5X,/,5X,'Channel Space:',T25,'PSC2 =',E10.2,T44,'Watts',
     1  4X,' BWCS2 =',f9.2,2x,'Hz')

      WRITE(5,270) PINTB,BWB
      WRITE(8,270) PINTB,BWB
270   FORMAT(5X,/,5x,'Interferer B:',T25,'PINTB =',E10.2,T44,'Watts',
     1    4x,' BWb =',f9.2,2x,'Hz')



      WRITE(5,800) FBW,FCSTART
      WRITE(8,800) FBW,FCSTART
800   FORMAT(5X,/,5X,'FBW =',F9.2,3X,'FCSTART =',F9.2)

      WRITE(5,805) FMAX, FCSTOP
      WRITE(8,805) FMAX, FCSTOP
805   FORMAT(5X,'FMAX =',F9.2,3X,'FCSTOP =',F9.2)

      WRITE(5,810) BANDEND,NUMF
      WRITE(8,810) BANDEND,NUMF
810   FORMAT(5X,'BANDEND =',F9.2,3X,'NUMBER OF FREQ. =', I5)
```

syst.for

7

```
      WRITE(5,815)
      WRITE(8,815)
815   FORMAT(5X,/,8X,'FMARKER',10X,'BIN (M(I))')

      WRITE(5,820) ((FMARK(I),M(I)),I=1,6)
      WRITE(8,820) ((FMARK(I),M(I)),I=1,6)
820   FORMAT(5X,F9.2,10X,I5)

      WRITE(5,825)
      WRITE(8,825)
825   FORMAT(5X,/,2X,'SIGNAL(1-20)',3X,'SIGNAL(21-40)',
     1    3X,'SIGNAL(41-60)',3X,'SIGNAL(61-80)',3X,'SIGNAL(81-100)')

      WRITE(5,830) ((SIGNL(K)),K=1,NUMF)
      WRITE(8,830) ((SIGNL(K)),K=1,NUMF)
830   FORMAT(2X,5(E10.2,6X))

      RETURN
      END



      SUBROUTINE FILT(FO,HO,R1,R3,R4,C2,C5)

ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
C
C       VARIABLES USED:
C               FO,HO,H,RMAX,R,C2M,C2,K,A,F,FF,R41,R42,R31,R32,D1,D2
C               R4,R3,R1,C5
C
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc

      WRITE(5,100)
      WRITE(8,100)
100   format(5X,/,20x,'Multiple Loop Feedback Filter Program:',/)

      type 105
105   format(5x,'Enter cutoff frequency fo in KHz and Gain in 20log dB.')
      accept *,fo,ho

C     FO = 1.550
C     HO = 10.0

      wo = 2 * 3.1415 * fo * 1000
      h = 10.0 ** (ho/20.0)
      rmax = 1/(2*(1+h))
      write(5,110) rmax
      write(8,110) rmax
110   format(t5,'rmax is',3x,F10.5,/)

      type 120
120   format(1x,'Enter r (smaller than rmax), and C2 in microfarads.')
      accept *, r, C2m

C     R = .06
C     C2M = .0047

      C2 = C2m * (10.0 ** -6.0)
      k = (wo*C2* SQRT(r))** -1
      a = SQRT(2.0)
      f = 4.0*r*(1+h)/(a**2.0)
      ff = a/(2.0*wo*C2*r)
      R41 = FF * (1 + SQRT(1-f))
      R42 = FF * (1 - SQRT(1-f))
```


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```
      R31 = 1/(wo*wo*R41*r*C2*C2)
      R32 = 1/(wo*wo*R42*r*C2*C2)

      write(5,130)
      write(8,130)
130   format(t5,'Pick the set whose values are closest to each other.')
      write (5,140) R41,R31,R42,R32
      write (8,140) R41,R31,R42,R32
140   format(t5,2(E8.2,5x),'or',5x,2(E8.2,5x),/)

      D1 = R41 - R31
      D2 = R42 - R32
      IF (D1-D2) 123,125,125
123   R4 = R41
      R3 = R31
      GO TO 127
125   R4 = R42
      R3 = R32
127   CONTINUE

      C5 = r*C2
      R1 = R4/h

      write(5,160)
      write(8,160)
160   format(t8,'fo',15x,'ho',14x,'rmax',14x,'r')
      write(5,170) fo,ho,rmax,r
      write(8,170) fo,ho,rmax,r
170   format(t5,f8.5,8x,f8.2,10x,f8.6,10x,f8.6,/)
      write(5,180)
      write(8,180)
180   format(t8,'R4',15x,'R3',14x,'R1',14x,'C2',14x,'C5')
      write(5,190) R4,R3,R1,C2,C5
      write(8,190) R4,R3,R1,C2,C5
190   format(t5,f9.1,7x,f9.1,7x,f9.1,7x,2(E8.2,9x),/,/)

cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c
c     NOW WE HAVE CALCULATED THE RESISTORS REQUIRED FOR THE FILTER.
c
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc


c     WRITING ON UNITS 10,11,13,14 TO BE READ BY PWRPLOT.FOR
c                                                NOISEPLOT.FOR
c                                                COMPLOT.FOR
c                                                TRYPLOT.FOR


      write(10,200) fo,ho,rmax,r
      write(11,200) fo,ho,rmax,r
      write(13,200) fo,ho,rmax,r
      write(14,200) fo,ho,rmax,r
200   format(t5,f8.5,8x,f8.2,10x,f8.6,10x,f8.6,/)

      write(10,210) R4,R3,R1,C2,C5
      write(11,210) R4,R3,R1,C2,C5
      write(13,210) R4,R3,R1,C2,C5
      write(14,210) R4,R3,R1,C2,C5
210   format(t5,f9.1,7x,f9.1,7x,f9.1,7x,2(E8.2,8x),/,/)


      RETURN
```

syst.for

```
      END



      SUBROUTINE YPARA(FR,NUMF,R1,R3,R4,C2,C5,YA,YT)


      IMPLICIT COMPLEX (Y)
      DIMENSION FR(200), YA(2,2), YT(2,2,200)
      DIMENSION GA(2,2),BA(2,2)
      DIMENSION GL(200),BL(200),YL(200)


cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c                THIS IS Y PARAMETER PROGRAM - GIVEN R1,R3,R4,C2,C5        c
c                                                                          c
c       VARIABLES USED:                                                    c
c               REAL: ZIN, AOL,ZO, GA(i,j), BA(i,j)
c                     R1,R3,R4,C2,C5, GL(i), BL(i)
c                     GG,BB,FR(200),WW
c               COMPLEX: YA(i,j), YL(i), YY, YX, Y1234, Y234, YDEN,
c                     YNUM22, YT(i,j,k)
c
c       INPUT VARIABLES:
c               FNAME = THE NAME OF OUTPUT FILE
c               R1,R3,R4,C2,C5    FOR THE MULTIPLE LOOP FEEDBACK FILTER
c               FR(i) =  THE FREQUENCIES AT WHICH THE FILTER'S Y PARA WILL BE
c                        CALCULATED.
c
c       HIDDEN VARIABLES (given a value in program):
c               AMPLIFIER CHARACTERISTICS:
c                        ZIN, AOL(open loop voltage gain) and ZO
c
c       CALCULATED VARIABLES: YL(1) ....YL(5) FROM R1,....C5.
c
c       OUTPUT VARIABLES:
c               AMPLIFIER Y PARAMETERS -- YA(1,1) = GA(1,1) + j BA(1,1)
c                        and so on for ya(i,j)
c               FILTER Y PARAMETERS  --  YT(i,j,k) for which formulas are
c                        given. K designates the frequency, Fr(k), at
c                        the y parameters are calculated.
c
cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc


      ZIN = 2000000.0
      AOL = 200000.0
      ZO = 75.0

      GA(1,1) = 1/ZIN
      BA(1,1) = 0.0
      GA(1,2) = 0.0
      BA(1,2) = 0.0
      GA(2,1) = AOL/ZO
      BA(2,1) = 0.0
      GA(2,2) = 1/ZO
      BA(2,2) = 0.0

      write(5,12)
      write(8,12)
12    FORMAT(5X,/,/,5X,'Y PARAMETER CALCULATION FOR MULTIPLE LOOP FEEDBACK',
```


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syst.for 9

```
      1   ' FILTER:')

          DO 22 I = 1,2
          DO 32 J = 1,2
          GG = GA(I,J)
          BB = BA(I,J)
          YA(I,J) = CMPLX(GG,BB)
32        CONTINUE
22        CONTINUE

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C         THIS LOADS THE VALUES OF THE COMPLEX Y-PARAMETERS FOR THE BASIC       C
C         AMPLIFIER WHICH WILL BE USED IN THE FILTER.                           C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

          WRITE(5,24)
          WRITE(8,24)
24        FORMAT(5X,/,/,20X,'AMPLIFIER BLOCK Y-PARAMETERS',/)

          WRITE(5,42)  ((I,J,YA(I,J), J=1,2),I=1,2)
          WRITE(8,42)  ((I,J,YA(I,J), J=1,2),I=1,2)
42        FORMAT(5X,'YA(',I1,',',I2,')=',3X,E10.2,E10.2,10X,'YA(',I1,
      1   ',',I2,')=',3X,E10.2,E10.2)


          WRITE(5,28)
          WRITE(8,28)
28        FORMAT(5X,/,20X,'FILTER BLOCK Y-PARAMETERS')

          DO 26 K = 1,NUMF

          WW = 2.0 * 3.1415 * FR(K)

          GL(1) = 1.0/R1
          BL(1) = 0.0
          GL(2) = 0.0
          BL(2) = WW * C2
          GL(3) = 1.0/R3
          BL(3) = 0.0
          GL(4) = 1.0/R4
          BL(4) = 0.0
          GL(5) = 0.0
          BL(5) = WW * C5


          DO 36 I = 1,5
          GG = GL(I)
          BB = BL(I)
          YL(I) = CMPLX(GG,BB)
C         WRITE(5,1000) YL(I)
C         WRITE(8,1000) YL(I)
C1000     FORMAT (5X, 'YL(I) =', E10.2,E10.2)
36        CONTINUE

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C         THIS LOADS THE VALUES OF THE COMPLEX Y-PARAMETERS FOR THE FEEDBACK    C
C         ELEMENTS OF THE FILTER, YL(I).
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

          YY = YA(1,1) + YL(3) + YL(5)
          YX = YA(2,2) + YL(4) + YL(5)
          Y1234 = YL(1) + YL(2) + YL(3) + YL(4)
          Y234 = YL(2) + YL(3) + YL(4)
          YDEN = Y1234 * YY  -  YL(3) * YL(3)

C         WRITE(5,1005) YY,YX,Y1234,Y234,YDEN
C         WRITE(8,1005) YY,YX,Y1234,Y234,YDEN
C1005     FORMAT(5X,4(E12.2),/,5X,4(E12.2),/.5X,2(E12.2),/)


          YT(1,1,K) = (Y234 * YY - YL(3)*YL(3)) * YL(1)/ YDEN
          YT(1,2,K) = -YL(1) * (YL(4)*YY + YL(5)*YL(3))/ YDEN
          YT(2,1,K) = ((YL(3) *(YA(2,1) - YL(5))) - YL(4)*YY ) * YL(1)/YDEN

          YNUM22 = (Y1234*YL(5) + YL(3)*YL(4))*(YA(2,1) - YL(5))
      1            + (Y1234*YY - YL(3)*YL(3)) * YX
      1            + YL(4)*YL(4)*YY   -    YL(4)*YL(5)*YL(3)

          YT(2,2,K) = YNUM22/YDEN

26        CONTINUE


          DO 60 K = 1,NUMF,20

          WRITE(5,38) FR(K)
          WRITE(8,38) FR(K)
38        FORMAT(5X,/,/,5X,'FREQUENCY =',F10.2,3X,'HZ')

          WRITE(5,48) ((I,J,K,YT(I,J,K), J=1,2),I=1,2)
          WRITE(8,48) ((I,J,K,YT(I,J,K), J=1,2),I=1,2)
48        FORMAT(5X,'YT(',I1,',',I1,',',I3,')=',3X,E10.2,E10.2,5X,'YT(',I1,
      1   ',',I1,',',I3,')=',3X,E10.2,E10.2)

60        CONTINUE

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C         NOW WE HAVE CALCULATED ALL THE Y-PARAMETERS OF THE FILTER
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

          RETURN
          END





          SUBROUTINE YCASC(YT,YS,YLD,NUMF,FR,VGAINA,VGAINB,VGAINC,VDIVSA,
      1     VDIVAB,VDIVBC,YINA,YINB,YINC,YOUTA,YOUTB)


          IMPLICIT COMPLEX (Y)
          DIMENSION YT(2,2,200), FR(200)
          DIMENSION YOUTA(200), YOUTB(200), YINA(200), YINB(200), YINC(200)
          DIMENSION VDIVSA(200), VDIVAB(200), VDIVBC(200)
          DIMENSION VGAINA(200), VGAINB(200), VGAINC(200)


CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C         THIS SUBROUTINE IS GIVEN YS,YLD, AND THE Y-PARAMETERS OF THE FILTER
C         NETWORK AT A MAXIMUM OF 12 (ACTUALLY NUMF) FREQUENCIES.
```


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```
C                IT THEN CALCULATES THE VOLTAGE GAIN SQUARED OF EACH FILTER,
C       OF WHICH THERE ARE A MAXIMUM OF 3,  AND THE VOLTAGE DIVIDER OF EACH
C       SOURCE.
C                        VARIABLES: THOSE DIMENSIONED AND YS,YLD.
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC


        DO 205 K-1,NUMF

        YOUTA(K) - YT(2,2,K) -((YT(1,2,K)*YT(2,1,K))/(YT(1,1,K) + YS))
        YOUTB(K) - YT(2,2,K) -((YT(1,2,K)*YT(2,1,K))/(YT(1,1,K) + YOUTA(K)))
        YINC(K)  - YT(1,1,K) - ((YT(1,2,K)*YT(2,1,K))/(YT(2,2,K) + YLD))
        YINB(K)  - YT(1,1,K) - ((YT(1,2,K)*YT(2,1,K))/(YT(2,2,K) + YINC(K)))
        YINA(K)  - YT(1,1,K) - ((YT(1,2,K)*YT(2,1,K))/(YT(2,2,K) + YINB(K)))

        VDIVSA(K) - CABS(YS/(YS+ YINA(K)))**2
        VDIVAB(K) - CABS(YOUTA(K)/(YOUTA(K) +YINB(K)))**2
        VDIVBC(K) - CABS(YOUTB(K)/(YOUTB(K) +YINC(K)))**2

        VGAINA(K) - CABS(YT(2,1,K)/(YT(2,2,K) + YINB(K)))**2
        VGAINB(K) - CABS(YT(2,1,K)/(YT(2,2,K) + YINC(K)))**2
        VGAINC(K) - CABS(YT(2,1,K)/(YT(2,2,K) + YLD))**2

205     CONTINUE

        WRITE(5,210)
        WRITE(8,210)
210     FORMAT(5X,/,5X,'Frequency',12x,'YoutA',17x,'YoutB')

        write(5,215)((FR(K),YOUTA(K),YOUTB(K)),K-1,NUMF,20)
        write(8,215)((FR(K),YOUTA(K),YOUTB(K)),K-1,NUMF,20)
215     FORMAT(2X,F9.2,5X,E10.2,E10.2,5X,E10.2,E10.2)

        WRITE(5,220)
        WRITE(8,220)
220     FORMAT(5X,/,5X,'Frequency',10x,'YinA',16x,'YinB',16x,'YinC')

        write(5,225)((FR(K),YINA(K),YINB(K),YINC(K)),K-1,NUMF,20)
        write(8,225)((FR(K),YINA(K),YINB(K),YINC(K)),K-1,NUMF,20)
225     FORMAT(2X,F9.2,3X,E10.2,E10.2,3X,E10.2,E10.2,3X,E10.2,E10.2)

        WRITE(5,230)
        WRITE(8,230)
230     FORMAT(5X,/,5X,'Frequency',12x;'VDIVSA',14X,'VDIVAB',14X,'VDIVBC')

        WRITE(5,235)((FR(K),VDIVSA(K),VDIVAB(K),VDIVBC(K)),K-1,NUMF,20)
        WRITE(8,235)((FR(K),VDIVSA(K),VDIVAB(K),VDIVBC(K)),K-1,NUMF,20)
235     FORMAT(5X,F9.2,9X,E10.2,10X,E10.2,10X,E10.2)

        WRITE(5,240)
        WRITE(8,240)
240     FORMAT(5X,/,5X,'Frequency',12x,'VGAINA',14X,'VGAINB',14X,'VGAINC')

        WRITE(5,245)((FR(K),VGAINA(K),VGAINB(K),VGAINC(K)),K-1,NUMF,20)
        WRITE(8,245)((FR(K),VGAINA(K),VGAINB(K),VGAINC(K)),K-1,NUMF,20)
245     FORMAT(5X,F9.2,9X,E10.2,10X,E10.2,10X,E10.2)


        RETURN
        END
```

syst.for

10

```
        SUBROUTINE NOISE(R1,R3,R4,C2,C5,FR,.BW,NUMF,VN2,CN2,
     1      VN2VV,CN2AA,VT2,CT2,CFILT,VFILT,
     1      QVR1,QVR3,QVR4,QVCN,QVVN,QCR3,QCR4,QCCN,QCVN)


        DIMENSION FR(200)

        DIMENSION QVR1(200),QVR3(200),QVR4(200),QVCN(200),QVVN(200)
        DIMENSION QCR3(200),QCR4(200),QCCN(200),QCVN(200)
        DIMENSION vfr1(200),vfr3(200),vfr4(200),vfcn(200),vfvn(200)
        DIMENSION cfr3(200),cfr4(200),cfcn(200),cfvn(200)

        DIMENSION VN2(200),CN2(200),VT2(200),CT2(200)
        DIMENSION CN2AA(200),VN2VV(200),CFILT(200),VFILT(200)

        DIMENSION VN2GAIN(200),CN2GAIN(200)
        DIMENSION RSNOPT(200),FOPT(200)


CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C       WE CALCULATE THE EQUIVALENT NOISE VOLTAGE, VT2(I), AND
C       NOISE CURRENT, CT2(I), GIVEN THE OP-AMP NOISE VOLTAGE, VN2(I),
C       AND NOISE CURRENT, CN2(I), AND THE RESISTOR VALUES.
C               VARIABLES USED:
C                       REAL: R1,R3,R4,C2,C5
C                             RR1,RR3
C                             ZAR3,ZBR3,ZC,ZD,ZE,ZF,ZG
C                             XAR3,XBR3,XC,XD,XE,XF,XG
C                             NUMF,FBW,CUTLF
C                             YS,GS,BS
C                       REAL ARRAYS:
C                             FBW(200)
C                             VN2(3),CN2(3),VT2(3),CT2(3)
C                             QM1(3),QM2(3),QM3(3),QM4(3),QM5(3),QM6(3)
C                             RSNOPT(3), FOPT(3)
C                             VN2VV(200),CN2AA(200),CFILT(200),VFILT(200)
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC


C       vn2(1) - 1.7  * (10.0**-13)
C       vn2(2) - 1.3  * (10.0**-14)
C       vn2(3) - 1.0  * (10.0**-15)
C       vn2(4) - 4.8  * (10.0**-16)
C       vn2(5) - 4.25 * (10.0**-16)
C       vn2(6) - 4.1  * (10.0**-16)
C       vn2(7) - 4.05 * (10.0**-16)
C       vn2(8) - 4.0  * (10.0**-16)
C       vn2(9) - 4.0  * (10.0**-16)
C       vn2(10) - 4.0 * (10.0**-16)
C       vn2(11) - 4.0 * (10.0**-16)


C       cn2(1) - 1.71 * (10.0**-21)
C       cn2(2) - 1.46 * (10.0**-22)
C       cn2(3) - 5.91 * (10.0**-24)
C       cn2(4) - 1.16 * (10.0**-24)
C       cn2(5) - 7.07 * (10.0**-25)
C       cn2(6) - 5.10 * (10.0**-25)
C       cn2(7) - 4.42 * (10.0**-25)
C       cn2(8) - 3.88 * (10.0**-25)
```


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```
C       cn2(9) = 3.53 * (10.0**-25)
C       cn2(10) = 3.4 * (10.0**-25)
C       cn2(11) = 3.2 * (10.0**-25)

      TYPE 200
200   FORMAT(5X,'ENTER LOW FREQUENCY CUTOFF FOR NOISE CALCULATIONS')
      ACCEPT *, CUTLF

      DO 300 K = 1, NUMF

      FB = FR(K) + FBW/2.0
      FA = FR(K) - FBW/2.0
      IF (FA.LE.0.0) GO TO 304
      GO TO 308
304   FA = CUTLF
308   CONTINUE

      IF(FR(K).LE.0.01) GO TO 310
      IF(FR(K).LE.30.0) GO TO 320
      IF(FR(K).LE.300.0) GO TO 330
      IF(FR(K).LE.500.0) GO TO 340
      IF(FR(K).LE.2000.0) GO TO 350
      IF(FR(K).LE.10000.0) GO TO 360
      VN2(K) = 4.0 * (10.0**-16)
      VN2VV(K) = 4.0 * (10.0**-16) * FBW
      CN2AA(K) = 3.0 * (10.0**-25) * FBW
      GO TO 380
310   VN2(K) = 6.00 * (10.0**-12)
      CN2(K) = 9.78 * (10.0**-20)
      VN2VV(K) = 6.00 * (10.0**-12) * FBW
      CN2AA(K) = 9.78 * (10.0**-20) * FBW
      GO TO 380
320   VN2(K) = 6.00 * (10.0**-14)/(FR(K)**1.0)
      CN2(K) = 7.77 * (10.0**-21)/(FR(K)**1.05)
      VN2VV(K) = 6.00 * (10.0**-14)*(ALOG(FB) - ALOG(FA))
      CN2AA(K) = (7.77/0.05) * (10.0**-22)*(FA**-0.05 - FB**-0.05)
      GO TO 380
330   VN2(K) = 1.07 * (10.0**-14)/(FR(K)**0.493)
      CN2(K) = 7.77 * (10.0**-22)/(FR(K)**1.05)
      VN2VV(K) = (1.07/0.507) * (10.0**-14)* (FB**.507 - FA**.507)
      CN2AA(K) = (7.77/0.05) * (10.0**-22)*(FB**-0.05 - FB**-0.05)
      GO TO 380
340   VN2(K) = 1.07 * (10.0**-14)/(FR(K)**0.493)
      CN2(K) = 1.29 * (10.0**-22)/(FR(K)**0.731)
      VN2VV(K) = (1.07/0.507) * (10.0**-14)* (FB**.507 - FA**.507)
      CN2AA(K) = (1.29/0.269) * (10.0**-22)*(FB**0.269 - FA**0.269)
      GO TO 380
350   VN2(K) = 1.35 * (10.0**-15)/(FR(K)**0.161)
      CN2(K) = 1.29 * (10.0**-22)/(FR(K)**0.731)
      VN2VV(K) = (1.35/0.839) * (10.0**-15) * (FB**0.839 - FA**0.839)
      CN2AA(K) = (1.29/0.269) * (10.0**-22)*(FB**0.269 - FA**0.269)
      GO TO 380
360   VN2(K) = 4.0 * (10.0**-16)
      CN2(K) = 5.58 * (10.0**-24)/(FR(K)**0.317)
      VN2VV(K) = 4.0 * (10.0**-16) * FBW
      CN2AA(K) = (5.58/0.683) * (10.0**-24)*(FB**0.683 - FA**0.683)
      GO TO 380
380   CONTINUE

300   CONTINUE
```


syst.for

```
C
C       VN2VV(K) AND CN2AA(K) ARE THE VALUES OF VN2(K) AND CN2(K)
C       INTEGRATED FROM FB TO FA. THIS SHOULD REPRESENT A GOOD
C       APPROXIMATION TO THE TRUE VALUE OF NOISE POWER IN THAT
C       BAND AS LONG AS FBW IS ENTIRELY IN THE NOISE REGION THAT
C       FR(K) FALLS IN.

        rf1 = 1 + (R1/R4)
        rf3 = 1 + (R3/R4)

        zar3 = r3*rf1*rf1
        zbr3 = ((c2*c1)**2)*r3
        zc = r1 + r3*rf1
        zd = c2*r1*r3
        ze = rf1
        zf = r1*r3*c2*c5
        zg = C2*r1 - c5*r3*rf1

C       write(5,485) za,zb,zc
C       write(8,485) za,zb,zc
C       write(5,488) zd,ze,zf,zg
C       write(8,488) zd,ze,zf,zg
C485    format(t5,//,t5,3(E10.2,5x))
C488    format(t5,//,t5,3(E10.2,5x))

        xar3 = r3/(r4**2)
        xbr3 = c2*c2*r3
        xc = rf3
        xd = c2*r3
        xe = 1/r4
        xf = r3*c2*c5
        xg = c2 - rf3*c5

C       write(5,480) za,zb,xc
C       write(8,480) za,zb,xc
C       write(5,482) zd,ze,xf,xg
C       write(8,482) zd,ze,xf,xg
C480    format(t5,//,t5,3(E10.2,5x))
C482    format(t5,//,t5,3(E10.2,5x))

        fkt = 1.66 * (10.0**-20)

        do 500 i = 1,NUMF

        w = 2.0 * 3.1415 * FR(i)

        qvr1(i) = r1
        qvr3(i) = zar3 + w*w*zbr3
        qvr4(i) = r1*r1/r4
        qvcn(i) = zc*zc + (zd*w)**2
        qvvn(i) = (ze + w*w*zf)**2 + (w*zg)**2

        qcr3(i) = xar3 + w*w*xbr3
        qcr4(i) = 1/r4
        qccn(i) = xc*xc + (xd*w)**2
        qcvn(i) = (xe + w*w*xf)**2 + (w*xg)**2

500     continue

        do 510 i = 1, NUMF
```


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```
      vfr1(i) = fkt * qvr1(i)
      vfr3(i) = fkt * qvr3(i)
      vfr4(i) = fkt * qvr4(i)
      vfcn(i) = cn2(i) * qvcn(i)
      vfvn(i) = vn2(i) * qvvn(i)

      cfr3(i) = fkt * qcr3(i)
      cfr4(i) = fkt * qcr4(i)
      cfcn(i) = cn2(i)*qccn(i)
      cfvn(i) = vn2(i)*qcvn(i)

      vt2(i) = vfr1(i)+vfr3(i)+vfr4(i)+vfcn(i)+vfvn(i)
      ct2(i) = cfr3(i)+cfr4(i)+cfcn(i)+cfvn(i)

      VFILT(i) = fkt * FBW * (qvr1(i) + qvr3(i) + qvr4(i))
     1                + CN2AA(i)*qvcn(i) + VN2VV(i)*qvvn(i)
      CFILT(i) = fkt * FBW * (qcr3(i) + qcr4(i))
     1                + CN2AA(i)*qccn(i) + VN2VV(i)*qcvn(i)

      VN2GAIN(I) = VT2(I)/VN2(I)
      CN2GAIN(I) = CT2(I)/CN2(I)

      RSNOPT(i) = sqrt(vt2(i)/ct2(i))
      fopt(i) = 1 + ((2.0*vt2(i))/(fkt*rsnopt(i)))

510   continue



      write(5,525)
      write(8,525)
525   format(t5,/,t5,'Total Voltage Noise Squared Calculation - vt2':)
C     write(5,550)
C     write(8,550)
C550  format(t4,'Freq',8x,'H1(4kt)',11x,'H2(cn2)',11x,'H3(vn2)')

C     do 600 I = 1,NUMF,20
C     write(5,650) fr(i),qm1(i),qm2(i),qm3(i)
C     write(8,650) fr(i),qm1(i),qm2(i),qm3(i)
C650  format(t4,f6.1,3x,3(E9.2,9x))
C600  continue

      write(5,530)
      write(8,530)
530   format(t4,'Freq',9x,'VFR1',13X,'VFR3',13X,'VFR4')

      DO 560 I = 1, NUMF,20
      WRITE(5,570) FR(I),VFR1(I),VFR3(I),VFR4(I)
      WRITE(8,570) FR(I),VFR1(I),VFR3(I),VFR4(I)
570   FORMAT(T4,F6.1,3X,3(E9.2,9X))
560   CONTINUE

      WRITE(5,575)
      WRITE(8,575)
575   FORMAT(T4,'Freq',9X,'VFCN',13X,'VFVN',13X,'VT2')

      DO 580 I = 1, NUMF,20
      WRITE(5,590) FR(I),VFCN(I),VFVN(I),VT2(I)
      WRITE(8,590) FR(I),VFCN(I),VFVN(I),VT2(I)
590   FORMAT(T4,F6.1,3X,3(E9.2,9X))
580   CONTINUE
```

```
      write(5,725)
      write(8,725)
725   format(t5,/,t5,'Total Current Noise Squared Calculation - ct2':)
C     write(5,750)
C     write(8,750)
C750  format(t4,'Freq',8x,'H4(4kt)',11x,'H5(cn2)',11x,'H6(vn2)')

C     do 800 I = 1,NUMF
C     write(5,850) fr(i),qm4(i),qm5(i),qm6(i)
C     write(8,850) fr(i),qm4(i),qm5(i),qm6(i)
C850  format(t4,f6.1,3x,3(E9.2,9x))
C800  continue

      write(5,730)
      write(8,730)
730   format(t4,'Freq',9x,'CFR3',13X,'CFR4')

      DO 760 I = 1, NUMF,20
      WRITE(5,770) FR(I),CFR3(I),CFR4(I)
      WRITE(8,770) FR(I),CFR3(I),CFR4(I)
770   FORMAT(T4,F6.1,3X,2(E9.2,9X))
760   CONTINUE

      WRITE(5,775)
      WRITE(8,775)
775   FORMAT(T4,'Freq',9X,'CFCN',13X,'CFVN',13X,'CT2')

      DO 780 I = 1, NUMF,20
      WRITE(5,790) FR(I),CFCN(I),CFVN(I),CT2(I)
      WRITE(8,790) FR(I),CFCN(I),CFVN(I),CT2(I)
790   FORMAT(T4,F6.1,3X,3(E9.2,9X))
780   CONTINUE


      write(5,900)
      write(8,900)
900   format(t5,/,/,25X,'4kt = 1.66 * 10**-20 V*A/Hz')

      write(5,910)
      write(8,910)
910   format(t4,/,t5,'Freq',5x,'cn2(A2/Hz)',5x,'vn2(V2/Hz)',
     1   5x,'ct2(A2/Hz)',5x,'vt2(V2/Hz)')

      do 930 I=1,NUMF,20
      write(5,950) fr(i), cn2(i),vn2(i),ct2(i),vt2(i)
      write(8,950) fr(i), cn2(i),vn2(i),ct2(i),vt2(i)
950   format(t4,f6.1,3x,4(E9.2,6x))
930   continue

C     WRITE(5,955)
C     WRITE(8,955)
C955  FORMAT(T4,/,T5,'Freq',6x,'cn2gain',8x,'vn2gain')

C     do 905 I = 1,NUMF,20
C     write(5,908) fr(i),cn2gain(i),vn2gain(i)
C     write(8,908) fr(i),cn2gain(i),vn2gain(i)
C908  format(t4,f6.1,3x,2(E9.2,6x))
C905  continue

      WRITE(5,915) CUTLF
      WRITE(8,915) CUTLF
915   FORMAT(5X,/,10X,'LOW FREQ. CUTOFF FOR NOISE CALCULATIONS = ',
     1   1X,F10.7)
```

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```
      write(5,985)
      write(8,985)
985   format(t4,/,t5,'Freq',5x,'CN2AA(A2)',6x,'VN2VV(V2)',
    1   6x,'CFILT(A2)',6X,'VFILT(V2)')

      DO 990 I = 1,NUMF,20
      WRITE(5,995) FR(I),CN2AA(I),VN2VV(I),CFILT(I),VFILT(I)
      WRITE(8,995) FR(I),CN2AA(I),VN2VV(I),CFILT(I),VFILT(I)
995   FORMAT(t4,f6.1,3x,4(E9.2,6x))
990   CONTINUE


      WRITE(5,946)
      WRITE(8,946)
946   FORMAT(T4,/,25X,'ASSUMING VT2 AND CT2 ARE UNCORRELATED:')

      write(5,945)
      write(8,945)
945   format(t4,/,t5,'Freq',6x,'Rsnopt',9x,'Fopt',9x,'NF(dB)')

      do 920 i=1,NUMF,20
      fodb = 10.0 * alog10(fopt(i))
      write(5,940) fr(i),rsnopt(i),fopt(i),fodb
      write(8,940) fr(i),rsnopt(i),fopt(i),fodb
940   format(t4,f6.1,3x,3(E9.2,6x))
920   continue

C     WRITING TO UNIT 11 TO BE READ BY NOISEPLOT.FOR

      DO 935 I = 1,NUMF
      write(11,937) fr(i), cn2(i),vn2(i),ct2(i),vt2(i)
937   format(t4,f6.1,3x,4(E9.2,6x))
935   CONTINUE

      DO 960 I = 1,NUMF
      write(11,970) fr(i),cn2gain(i),vn2gain(i)
970   format(t4,f6.1,3x,2(E9.2,6x))
960   CONTINUE

      DO 965 I = 1, NUMF
      WRITE(11,969) fr(i), CN2AA(i),VN2VV(i),CFILT(i),VFILT(i)
969   format(t4,f6.1,3x,4(E9.2,6x))
965   CONTINUE

      DO 975 I=1,NUMF
      fodb = 10.0 * alog10(fopt(i))
      write(11,980) fr(i),rsnopt(i),fopt(i),fodb
980   format(t4,f6.1,3x,3(E9.2,6x))
975   CONTINUE

C     WRITING ON UNIT 10,11,13,14 TO BE READ BY PWRPLOT.FOR
C                                               NOISEPLOT.FOR
C                                               COMPLOT.FOR
C                                               TRIAL.FOR

      WRITE(10,997) CUTLF
      WRITE(11,997) CUTLF
      WRITE(13,997) CUTLF
      WRITE(14,997) CUTLF
997   FORMAT(25X,F10.7)

      RETURN
      END
```

syst.for

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```
      SUBROUTINE CROSSCORR(YSRCE,R1,R3,R4,C2,C5,FR,NUMF,FBW,
    1   VN2,CN2,VN2VV,CN2AA,VT2,CT2,CTVCF,
    1   QVCR3,QVCR4,QVCCN,QVCVN,VNTOT)


      IMPLICIT COMPLEX (Y)
      DIMENSION FR(200)
      DIMENSION YSRCE(200,3)
      DIMENSION RSRCE(3),XSRCE(3)
      DIMENSION VN2(200),CN2(200),VN2VV(200),CN2AA(200)
      DIMENSION VT2(200),CT2(200)

      DIMENSION CTVC(200),CRATIO(200)

      DIMENSION xtr3(200),xtr4(200),xtcn(200),xtvn(200)
      DIMENSION VNTOT(200,3)

      DIMENSION CTVCF(200,3),QVCR3(200,3),QVCR4(200,3)
      DIMENSION QVCCN(200,3),QVCVN(200,3)

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C     VARIABLES USED:  FKT,YSRCE,RS,XS
C                      war3,wbr3,wcr3,wdr4,wc,wd,we,wf,wg,wh,wi,wj
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

      FKT = 1.66 * (10.0**-20)

      rr1 = 1 + (R1/R4)
      rr3 = 1 + (R3/R4)

      war3 = rr1/(r3*r4)
      wbr3 = (c2**2) * r1/r3
      wcr3 = c2/r3
      wdr4 = r1/r4
      wc = r3*rr3 + r1*rr3*rr3
      wd = ((c2*r3)**2) * r1
      we = c2*r3*r3
      wf = (r4+r1)/(r4**2)
      wg = c2*c2*r1 - c5*c5*r3*rr3  + ((c5*rr3)**2)*r1
    1        - 2.0*c2*c5*r1
      wh = ((c2*c5*r3)**2)/r1
      wi = c5 - c2
      wj = c2 * ((c5*r3)**2)


      DO 210 K = 1,3

      WRITE(5,200) K,YSRCE(1,K)
      WRITE(8,200) K,YSRCE(1,K)
200   FORMAT(5X,/,25X,'YSRCE(1,',I3,') = ', E9.2,2X,E9.2)

      do 205 i = 1, NUMF

      RSRCE(K) =   REAL(YSRCE(I,K))/(CABS(YSRCE(I,K))**2)
      XSRCE(K) = -AIMAG(YSRCE(I,K))/(CABS(YSRCE(I,K))**2)

      w = 2.0 * 3.1415 * FR(i)

      qvcr3(i,k) = -1.0 * (war3+w*w*wbr3) * rsrce(k)  + w*wcr3*xsrce(k)
```


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```
      qvcr4(i,k) = wdr4*rsrce(k)
      qvccn(i,k) = (wc + w*w*wd) * rsrce(k) - w*we*xsrce(k)
      qvcvn(i,k) = (wf + w*w*wg + (w**4)*wh) * rsrce(k)
     1              + (w*wi - (w**3)*wj) * xsrce(k)

      ctvcf(i,k) = fkt * (qvcr3(i,k) + qvcr4(i,k)) * FBW *2.0
     1      + CN2AA(i)*qvccn(i,k)*2.0 + VN2VV(i)*qvcvn(i,k)*2.0

205   continue
210   CONTINUE

      DO 260 K = 1,3

      DO 250 I = 1, NUMF

      xtr3(i) = fkt * qvcr3(i,k) * 2.0
      xtr4(i) = fkt * qvcr4(i,k) * 2.0
      xtcn(i) = cn2(i)*qvccn(i,k) * 2.0
      xtvn(i) = vn2(i)*qvcvn(i,k) * 2.0
      ctvc(i) = xtr3(i)+xtr4(i)+xtcn(i)+xtvn(i)

      VNTOT(I,K) = (CT2(I)/CABS(YSRCE(I,K))**2)+VT2(I)+CTVC(I)
      CRATIO(I) = CTVC(I)*CABS(YSRCE(I,K))/(SQRT(VT2(I)*CT2(I))*2.0)
250   CONTINUE

      write(5,220)
      write(8,220)
220   format(5x,/,t5,'Freq',7x,'XTR3',7X,'XTR4',7X,'XTCN',
     1  7X,'XTVN',7X,'CTVC')

      do 240 i = 1, NUMF,20
      write(5,230) fr(i),xtr3(i),xtr4(i),xtcn(i),xtvn(i),ctvc(i)
      write(8,230) fr(i),xtr3(i),xtr4(i),xtcn(i),xtvn(i),ctvc(i)
230   format(t4,f6.1,3x,5(e9.2,2x))
240   continue

      WRITE(5,1003)
      WRITE(8,1003)
1003  FORMAT(5X,/,T5,'Freq',7x,'CTVCF',7X,'CrossTermVC',
     1    5X,'CRATIO',7X,'VNTOT(VV/Hz)')

      DO 1005 I = 1,NUMF,20
      WRITE(5,1010) FR(I),CTVCF(I,K),CTVC(I),CRATIO(I),VNTOT(I,K)
      WRITE(8,1010) FR(I),CTVCF(I,K),CTVC(I),CRATIO(I),VNTOT(I,K)
1010  FORMAT(T4,F6.1,5X,4(E9.2,5X))
1005  CONTINUE

260   CONTINUE

      RETURN
      END



      SUBROUTINE SNR(NUMF,FR,M,PWSG,PWNS)

      DIMENSION FR(200)
      DIMENSION M(6)
      DIMENSION PWSG(200,4),PWNS(200,4)

      DIMENSION SGNLPW(4),SBNS(4)
      DIMENSION PWINTA(4),PWINTB(4)
      DIMENSION TOTNS(4)
```

syst.for

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```
      DIMENSION SNRINB(4),SNRTB(4),SINTAR(4),SINTBR(4)

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
C     CALCULATES TOTAL SIGNAL POWER, SGNLPW(N), AT NODE N.
C               SIGNAL BAND NOISE POWER, SBNS(N), AT NODE N.
C               TOTAL INTERFERER A POWER, PWINTA(N), AT NODE N.
C               TOTAL INTERFERER B POWER, PWINTB(N), AT NODE N.
C               TOTAL NOISE POWER - 0 TO 9550 HZ -  TOTNS(N)
C                                       AT NODE N.
C
C     VARIABLES USED: NUMF AND THOSE DIMENSIONED.
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC


      DO 405 N = 1,4

      SGNLPW(N) = 0.0
      SBNS(N) = 0.0
      MSTART = M(1)
      MSTOP = M(2)

      DO 410 K = MSTART,MSTOP
      SGNLPW(N) = PWSG(K,N) + SGNLPW(N)
      SBNS(N) = PWNS(K,N) + SBNS(N)
410   CONTINUE

405   CONTINUE


      DO 415 N = 1,4

      PWINTA(N) = 0.0
      MSTART = M(3)
      MSTOP = M(4)

      DO 420 K = MSTART,MSTOP
      PWINTA(N) = PWSG(K,N) + PWINTA(N)
420   CONTINUE

415   CONTINUE



      DO 425 N = 1,4

      PWINTB(N) = 0.0
      MSTART = M(5)
      MSTOP = M(6)

      DO 430 K = MSTART,MSTOP
      PWINTB(N) = PWSG(K,N) + PWINTB(N)
430   CONTINUE

425   CONTINUE


      DO 440 N = 1,4

      TOTNS(N) = 0.0

      DO 445 K = 1,NUMF
      TOTNS(N) = PWNS(K,N) + TOTNS(N)
```

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```
445   CONTINUE

440   CONTINUE

      DO 450 N = 1,4
      SNRINB(N) = SGNLPW(N)/SBNS(N)
      SNRTB(N)  = SGNLPW(N)/TOTNS(N)
      SINTAR(N) = SGNLPW(N)/PWINTA(N)
      SINTBR(N) = SGNLPW(N)/PWINTB(N)
450   CONTINUE

      WRITE(5,550)
      WRITE(8,550)
550   FORMAT(5X,/,T28,3X,'Node 1',6x,'Node 2',6x,'Node 3',6x,'Node 4')

      write(5,555) ((sgnlpw(n)),n=1,4)
      write(8,555) ((sgnlpw(n)),n=1,4)
555   FORMAT(2X,'Wanted Signal Power',T28,4(e10.2,2X))

      write(5,560) ((pwinta(n)),n=1,4)
      write(8,560) ((pwinta(n)),n=1,4)
560   FORMAT(2X,'Interferer A Power',T28,4(e10.2,2X))

      write(5,565) ((pwintb(n)),n=1,4)
      write(8,565) ((pwintb(n)),n=1,4)
565   FORMAT(2X,'Interferer B Power',T28,4(e10.2,2X))

      write(5,570) ((totns(n)),n=1,4)
      write(8,570) ((totns(n)),n=1,4)
570   FORMAT(2X,'Total Noise(0-9550)',T28,4(e10.2,2X))

      write(5,575) ((sbns(n)),n=1,4)
      write(8,575) ((sbns(n)),n=1,4)
575   FORMAT(2X,'Noise In Signal Band',T28,4(e10.2,2X))

      WRITE(5,580) ((SNRINB(N)),N=1,4)
      WRITE(8,580) ((SNRINB(N)),N=1,4)
580   FORMAT(2X,/,2X,'SNR (In Band)',T28,4(E10.2,2X))

      WRITE(5,585) ((SNRTB(N)),N=1,4)
      WRITE(8,505) ((SNRTB(N)),N=1,4)
585   FORMAT(2X,'SNR (Total Band)',T28,4(E10.2,2X))

      WRITE(5,590) ((SINTAR(N)),N=1,4)
      WRITE(8,590) ((SINTAR(N)),N=1,4)
590   FORMAT(2X,'Signal Power to Int. A',T28,4(E10.2,2X))

      WRITE(5,595) ((SINTBR(N)),N=1,4)
      WRITE(8,595) ((SINTBR(N)),N=1,4)
595   FORMAT(2X,'Signal Power to Int. B',T28,4(E10.2,2X))

C     WRITING ON UNIT 10,14 TO BE READ BY PWRPLOT.FOR
C                                          TRIAL.FOR

      WRITE(10,600) ((SNRINB(N)),N=1,4)
      WRITE(14,600) ((SNRINB(N)),N=1,4)
600   FORMAT(4(E10.2,2X))

      WRITE(10,605) ((SNRTB(N)),N=1,4)
      WRITE(14,605) ((SNRTB(N)),N=1,4)
605   FORMAT(4(E10.2,2X))

      WRITE(10,610) ((SINTAR(N)),N=1,4)
      WRITE(14,610) ((SINTAR(N)),N=1,4)
610   FORMAT(4(E10.2,2X))

      WRITE(10,615) ((SINTBR(N)),N=1,4)
      WRITE(14,615) ((SINTBR(N)),N=1,4)
615   FORMAT(4(E10.2,2X))

      return
      end

      SUBROUTINE COMPNOISE(NUMF,FR,FBW,YSRCE,YLD,VSRCE,VLOAD,YOUTA,
     1  YOUTB,YINB,YINC,VGAINA,VGAINB,VGAINC,VDIVSA,VDIVAB,VDIVBC,
     1  QVR1,QVR3,QVR4,QVCN,QVVN,QCR3,QCR4,QCCN,QCVN,CN2AA,VN2VV,
     1  QVCR3,QVCR4,QVCCN,QVCVN)

      IMPLICIT COMPLEX (Y)

C     ARRAYS CREATED BY SUBROUTINE INIT
      DIMENSION FR(200)

C     ARRAYS CREATED BY YCASC
      DIMENSION VDIVSA(200), VDIVAB(200), VDIVBC(200)
      DIMENSION VGAINA(200), VGAINB(200), VGAINC(200)
      DIMENSION YINB(200),YINC(200)
      DIMENSION YOUTA(200),YOUTB(200)

C     ARRAYS CREATED BY NOISE
      DIMENSION VN2VV(200),CN2AA(200)
      DIMENSION QVR1(200),QVR3(200),QVR4(200),QVCN(200),QVVN(200)
      DIMENSION QCR3(200),QCR4(200),QCCN(200),QCVN(200)

C     ARRAYS CREATED BY CROSSCORR
      DIMENSION QVCR3(200,3),QVCR4(200,3),QVCCN(200,3),QVCVN(200,3)

C     ARRAYS CREATED IN THE MAIN PROGRAM
      DIMENSION YSRCE(200,3)
      DIMENSION VSRCE(200), VLOAD(200)

C     ARRAYS CREATED BY THIS SUBROUTINE
      DIMENSION CPR1(200,3),CPR3(200,3),CPR4(200,3)
      DIMENSION CPCN(200,3),CPVN(200,3)
      DIMENSION VTFTER(200,3),VVRY(200,3)
      DIMENSION TERMR1(200,4),TERMR3(200,4),TERMR4(200,4)
      DIMENSION TERMCN(200,4),TERMVN(200,4),TERMIN(200,4)
      DIMENSION TERMOUT(200),PNOISE(200,4)

C     CONSTANTS USED: FFACTR,FBW,FKT,SSOURC

cccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
C
C     THIS PROGRAM CALCULATES TOTAL NOISE VOLTAGE OF FILTERS A,B,C
C     (VTFTER(200,3) SAME AS VTFILTA,VTFILTB,VTFILTC) IN V*V
C     AND TOTAL NOISE POWER IN WATTS AT EACH NODE: PNOISE(200,3)
C     (SAME AS PWNS(200,3))
C
C             IT DOES NOT CALCULATE V*V/HZ OR A*A/HZ
C
```


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```
C       INPUTS ARE VN2VV (VN2 integrated over a BW, FBW) and
C               CN2AA (CN2 integrated over a BW, FBW)
C
C       FOR COMPARISON WITH PREVIOUS CALCULATION, COMPARE:
C                       VTFTER(200,1) = VTFILTA
C                       VTFTER(200,2) = VTFILTB
C                       VTFTER(200,3) = VTFILTC
C               AND     PNOISE(200,3) = PWNS(200,3)
C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

        FKT = 1.66 * (10.0**-20)
        FFACTR = FKT * FBW

        DO 600 K = 1,3
        DO 610 I = 1,NUMF

        SSOURC = CABS(YSRCE(I,K))**2
        CPR1(I,K) = QVR1(I)
        CPR3(I,K) = QVR3(I) + (QCR3(I)/SSOURC) + 2.0*QVCR3(I,K)
        CPR4(I,K) = QVR4(I) + (QCR4(I)/SSOURC) + 2.0*QVCR4(I,K)
        CPCN(I,K) = QVCN(I) + (QCCN(I)/SSOURC) + 2.0*QVCCN(I,K)
        CPVN(I,K) = QVVN(I) + (QCVN(I)/SSOURC) + 2.0*QVCVN(I,K)

        VTFTER(I,K) = (CPR1(I,K) + CPR3(I,K) + CPR4(I,K)) * FFACTR
     1                + CPCN(I,K) * CN2AA(I) + CPVN(I,K) * VN2VV(I)

610     CONTINUE
600     CONTINUE

        DO 620 I = 1,NUMF
        VVRY(I,1) = VDIVSA(I) * VGAINA(I) * REAL(YINB(I))
        VVRY(I,2) = VDIVAB(I) * VGAINB(I) * REAL(YINC(I))
        VVRY(I,3) = VDIVBC(I) * VGAINC(I) * REAL(YLD)
620     CONTINUE

        DO 630 K = 1,3
        DO 640 I = 1,NUMF
        J = K+1

        TERMR1(I,J) = CPR1(I,K) * FFACTR * VVRY(I,K)
        TERMR3(I,J) = CPR3(I,K) * FFACTR * VVRY(I,K)
        TERMR4(I,J) = CPR4(I,K) * FFACTR * VVRY(I,K)
        TERMCN(I,J) = CPCN(I,K) * CN2AA(I) * VVRY(I,K)
        TERMVN(I,J) = CPVN(I,K) * VN2VV(I) * VVRY(I,K)

640     CONTINUE
630     CONTINUE

        DO 650 I = 1,NUMF
        TERMIN(I,2) = VSRCE(I) * VVRY(I,1)
        PNOISE(I,2) = TERMIN(I,2) + TERMR1(I,2) + TERMR3(I,2)
     1      + TERMR4(I,2) + TERMCN(I,2) + TERMVN(I,2)

        TERMIN(I,3) = PNOISE(I,2)*VVRY(I,2)/(VDIVAB(I)*REAL(YINB(I)))

        PNOISE(I,3) = TERMIN(I,3) + TERMR1(I,3) + TERMR3(I,3)
     1      + TERMR4(I,3) + TERMCN(I,3) + TERMVN(I,3)

        TERMIN(I,4) = PNOISE(I,3)*VVRY(I,3)/(VDIVBC(I)*REAL(YINC(I)))

        TERMOUT(I) = VLOAD(I) * REAL(YLD)

        PNOISE(I,4) = TERMIN(I,4) + TERMR1(I,4) + TERMR3(I,4)
     1      + TERMR4(I,4) + TERMCN(I,4) + TERMVN(I,4) + TERMOUT(I)

650     CONTINUE

        WRITE(5,710) FKT,FFACTR
        WRITE(8,710) FKT,FFACTR
710     FORMAT(T5,/,T29,'4KT = ',E10.2,3X,'V*A/Hz',/,
     1     T25,'4KT*FBW = ',E10.2,3X,'WATTS')

        DO 715 K = 1,3

        WRITE(5,720) K,K,K,K,K
        WRITE(8,720) K,K,K,K,K
720     FORMAT(T5,/,T5,'FREQ',4X,'CPR1(',I1,')',4X,'CPR3(',I1,')',
     1     4X,'CPR4(',I1,')',4X,'CPCN(',I1,')',4X,'CPVN(',I1,')')

        DO 725 I = 1,NUMF,20
        WRITE(5,730) FR(I),CPR1(I,K),CPR3(I,K),CPR4(I,K),
     1        CPCN(I,K),CPVN(I,K)
        WRITE(8,730) FR(I),CPR1(I,K),CPR3(I,K),CPR4(I,K),
     1        CPCN(I,K),CPVN(I,K)
730     FORMAT(T4,F6.1,3X,5(E9.2,4X))

725     CONTINUE
715     CONTINUE

        WRITE(5,735)
        WRITE(8,735)
735     FORMAT(5X,/,5X,'FREQUENCY',11X,'VTFTERA',12X,'VTFTERB',
     1    12X,'VTFTERC')

        DO 740 I = 1,NUMF,20
        WRITE(5,745) FR(I),VTFTER(I,1),VTFTER(I,2),VTFTER(I,3)
        WRITE(8,745) FR(I),VTFTER(I,1),VTFTER(I,2),VTFTER(I,3)
745     FORMAT(5X,F9.2,9X,E10.2,9X,E10.2,9X,E10.2)
740     CONTINUE

        WRITE(5,750)
        WRITE(8,750)
750     FORMAT(5X,/,5X,'FREQUENCY',11X,'VVRY(1,1)',10X,'VVRY(1,2)',
     1       10X,'VVRY(1,3)')

        DO 755 I = 1,NUMF,20
        WRITE(5,760) FR(I),VVRY(I,1),VVRY(I,2),VVRY(I,3)
        WRITE(8,760) FR(I),VVRY(I,1),VVRY(I,2),VVRY(I,3)
760     FORMAT(5X,F9.2,9X,E10.2,9X,E10.2,9X,E10.2)
755     CONTINUE

        DO 763 K = 2,4
        WRITE(5,765) K,K,K,K,K
        WRITE(8,765) K,K,K,K,K
765     FORMAT(5X,/,5X,'FREQ',3X,'TERMR1(',I1,')',2X,'TERMR3(',I1,
     1    ')',2X,'TERMR4(',I1,')',2X,'TERMCN(',I1,')',2X,'TERMVN(',
     1    I1,')')

        DO 770 I = 1,NUMF,20
        WRITE(5,775) FR(I),TERMR1(I,K),TERMR3(I,K),TERMR4(I,K),
     1    TERMCN(I,K),TERMVN(I,K)
        WRITE(8,775) FR(I),TERMR1(I,K),TERMR3(I,K),TERMR4(I,K),
     1    TERMCN(I,K),TERMVN(I,K)
775     FORMAT(T4,F6.1,3X,5(E9.2,4X))
```


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```
      CONTINUE
      CONTINUE

      WRITE(5,778)
      WRITE(8,778)
778   FORMAT(5X,/,5X,'FREQ',4X,'TERMIN(1,2)',3X,'TERMIN(1,3)',
     1   3X,'TERMIN(1,4)',3X,'TERMOUT(1)',)

      DO 780 I = 1,NUMF,20
      WRITE(5,785) FR(I),TERMIN(I,2),TERMIN(I,3),TERMIN(I,4),TERMOUT(I)
      WRITE(8,785) FR(I),TERMIN(I,2),TERMIN(I,3),TERMIN(I,4),TERMOUT(I)
785   FORMAT(4X,F6.1,3X,4(E9.2,5X))
780   CONTINUE

      WRITE(5,790)
      WRITE(8,790)
790   FORMAT(5X,/,'I',5X,'FREQ',5X,'PNOISE(1,2)',3X,'PNOISE(1,3)',
     1   3X,'PNOISE(1,4)',)

      DO 795 I = 1,NUMF,20
      WRITE(5,798) FR(I),PNOISE(I,2),PNOISE(I,3),PNOISE(I,4)
      WRITE(8,798) FR(I),PNOISE(I,2),PNOISE(I,3),PNOISE(I,4)
798   FORMAT(4X,F6.1,3X,3(E9.2,5X))
795   CONTINUE

C
C     WRITING ON UNIT 13 TO BE READ BY COMPLOT.FOR
C           4th Write statement to unit 13 (Complot.for).

      DO 930 K = 2,4
      DO 920 I = 1,NUMF
      WRITE(13,910) FR(I),TERMR1(I,K),TERMR3(I,K),TERMR4(I,K),
     1   TERMCN(I,K),TERMVH(I,K)
910   FORMAT(F4.1,F6.1,3X,5(E9.2,1X))
920   CONTINUE
930   CONTINUE

      DO 946 I = 1,NUMF
      WRITE(13,945) FR(I),TERMIN(I,2),TERMIN(I,3),TERMIN(I,4),TERMOUT(I)
945   FORMAT(4X,F6.1,3X,4(E9.2,5X))
940   CONTINUE

      WRITE(13,955) FR(I),PNOISE(I,2),PNOISE(I,3),PNOISE(I,4)
955   FORMAT(4X,F6.1,3X,3(E9.2,5X))
950   CONTINUE

      DO 950 I = 1,NUMF
      WRITE(13,955) FR(I),PNOISE(I,2),PNOISE(I,3),PNOISE(I,4)
955   FORMAT(4X,F6.1,3X,3(E9.2,5X))
950   CONTINUE

      RETURN
      END

      SUBROUTINE NF(NUMF,FR,M,YS,VNTOT,VGAINA,VGAINB,VGAINC,
     1   YINA,YINB,YINC)

      IMPLICIT COMPLEX (Y)

      COMPLEX ZSRCE

C     ARRAYS PASSED BY MAIN PROGRAM
      DIMENSION FR(200),M(6)
      DIMENSION VNTOT(200,3)
      DIMENSION VGAINA(200),VGAINB(200),VGAINC(200)
      DIMENSION YINA(200),YINB(200),YINC(200)

C     ARRAYS CREATED BY THIS PROGRAM
      DIMENSION FAFILT(200),FBFILT(200),FCFILT(200)
      DIMENSION FCASC(200),CASCNF(200),TCASC(200)

      FKT = 1.68*(10.0**-20)

      DO 100 I = 1,NUMF

      FAFILT(I) = 1 + (VNTOT(I,1)*REAL(YS)/FKT)
      FBFILT(I) = 1 + (VNTOT(I,2)*REAL(YS)/FKT)
      FCFILT(I) = 1 + (VNTOT(I,3)*REAL(YS)/FKT)
      RATIO1 = REAL(YINA(I))/REAL(YINB(I))
      RATIO2 = REAL(YINA(I))/REAL(YINC(I))
      FTERM2 = (FBFILT(I) - 1.0) * RATIO1/VGAINA(I)*VGAINB(I)
      FTERM3 = (FCFILT(I) - 1.0) * RATIO2/(VGAINA(I)*VGAINB(I))

      FCASC(I) = FAFILT(I) + FTERM2 + FTERM3
      CASCNF(I) = 10.0 * ALOG10(FCASC(I))
      TCASC(I) = (FCASC(I) - 1.0) * 290.0

100   CONTINUE

      MSTART = M(1)
      MSTOP = M(2)
      TTAVER = 0.0

      DO 105 I = MSTART,MSTOP
      TTAVER = TCASC(I) + TTAVER
105   CONTINUE

      MDIFF = MSTOP - MSTART
      TAVER = TTAVER/MDIFF
      TMID = (TTAVER - TCASC(MSTART))/(MDIFF - 1)

      WRITE(5,200)
      WRITE(8,200)
200   FORMAT(5X,/,5X,'FREQUENCY',12X,'FAFILT',13X,'FBFILT',
     1   13X,'FCFILT')

      DO 205 I = 1,NUMF,10
      WRITE(5,210) FR(I),FAFILT(I),FBFILT(I),FCFILT(I)
      WRITE(8,210) FR(I),FAFILT(I),FBFILT(I),FCFILT(I)
210   FORMAT(5X,F9.2,3(9X,E10.2))
205   CONTINUE

      WRITE(5,215)
      WRITE(8,215)
215   FORMAT(5X,/,5X,'FREQENCY',12X,'TCASC',14X,'CASCNF(dB)',
     1   8X,'TCASC(deg K)',)

      DO 220 I = 1,NUMF,10
      WRITE(5,225) FR(I),TCASC(I),CASCNF(I),TCASC(I)
      WRITE(8,225) FR(I),TCASC(I),CASCNF(I),TCASC(I)
225   FORMAT(5X,F9.2,9X,E10.2,9X,F10.2,9X,E10.2)
220   CONTINUE

      WRITE(5,230) TAVER,TMID
      WRITE(8,230) TAVER,TMID
230   FORMAT(5X,/,15X,'AVERAGE TEMP. IN BAND - ',E10.2,/,
     1   15X,'AVERAGE TEMP. (W/O 0-50 HZ) - ',E10.2)

      RETURN
      END
```

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Glossary

Mixer Terminology

Mixer Circuit Nomenclature

'Z' mixer circuit that provides an open circuit at the diode terminals to all mixer generated frequencies except at f_{RF} and f_{IF}.

'Y' mixer circuit that provides an open circuit at the diode terminals to all mixer operated frequencies except f_{RF} and f_{IF}.

'H' mixer circuit that provides an open circuit to all odd order sideband frequencies and a short circuit to all even order sideband frequencies.

'G' mixer circuit that provides an open circuit to a short order sideband frequencies and an open circuit to all even order sideband frequencies.

'RM' resistive mixer. This mixer circuit provides a resistive termination to all mixer generated frequencies including f_{RF} and f_{IF}.

Broadband mixer circuit is one that provides the same match to the diode at f_{RF}, f_{LO}, and f_{IMAGE}.

Frequency Domain Terminology

f_n sideband, or small-signal, frequencies generated by mixer; $f_n = f_{IF} + nf_{LO}$ where n can be a positive or negative integer.

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f_{RF}, **RF** radio frequency or signal frequency at the input of the downconverting mixer (n sideband = 1).

f_{IF}, **IF** intermediate frequency at the output of the downconverting mixer (n sideband = 0).

f_{LO}, **LO** local oscillator frequency. It is chosen so that f_{RF} - $f_{LO} = f_{IF}$.

f_{IMAGE} image frequency, it is that frequency that when beaten against f_{LO} produces f_{IF} i.e., f_{LO} - $f_{IMAGE} = f_{IF}$ (n sideband = -1).

T_{LO} period of local oscillator signal, $T_{LO} = \frac{1}{f_{LO}}$.

$Z_{emb}(f)$ embedding impedance established by the mixer circuit at diode terminals at the frequency f.

Mixer Circuit

I_{LO} current source at LO frequency; it models the LO source.

I_{RF} current source at RF frequency; it models the RF input signal.

I_{bias} dc current source; it models the application of bias in the mixer circuit.

$Z_S(f)$ source impedance presented to the diode by the preceeding component in the application the output impedance of the antenna. $Z_S(f)$ may be given to the mixer designer as a specification or it may be a design parameter under their control:

R_S source resistor,

L_S source inductor,

C_S source capacitor (see Fig. 14(a)).

$Z_L(f)$ load impedance presented to the diode by following receiver component:

C_{LD} load capacitor,

R_L load resistor.

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$V_{in}(t)$ voltage at the input terminals to mixer circuit (see Fig. 14(a)).

$I_{in}(t)$ current at the input terminals to mixer circuit (see Fig. 14(a)).

$Z_{in}(f)$ input impedance at the small signal frequency f. It is typically of interest to know $Zin(f_{RF})$; $Zin(f_{RF}) \triangleq \frac{\mathcal{F}(Vin)|f_{RF}}{\mathcal{F}(Iin)|f_{RF}}$.

$Z_{out}(f)$ output impedance at small signal frequency f. It is typically of interest to know $Z_{out}(f_{IF})$. This can be determined by finding the Thevenin equivalent of the mixer circuit at a given LO drive and bias level.

Mixer Analysis Terms

$V_{d_{max}}$, $V_{d_{min}}$ maximum and minimum excursion of diode voltage.

$V_{d_{ON}}$ turn-on voltage of the diode, ie. the voltage at which the dominant component of the diode current is resistive.

$I_{d_{max}}$, $I_{d_{min}}$ maximum and minimum excursion of diode current.

'ON' Time portion of the LO period that the diode is turned 'ON' ie. that non-zero current is travelling across the diode barrier resistance. It is somewhat arbitrarily set to be $I_d \geq 1\mu A$. 'ON' time is specified by two numbers. One, T_{NL}/T_{LO}, determines the amount of 'ON' time spent in the diode's highly nonlinear region, the other, T_{TON}/T_{LO}, gives the total percent of the LO period that the diode is 'ON'.

$\frac{T_{NL}}{T_{LO}}$ portion of LO period that $1\mu A \leq I_d \leq 0.5$mA.

$\frac{T_{TON}}{T_{LO}}$ portion of LO period that $I_d \geq 1\mu A$.

T_1 moment when RF and LO source are in phase.

T_2 moment when RF and LO are 90° out of phase.

T_3 moment when RF and LO are 180° out of phase.

T_4 moment when RF and LO are 270° out of phase.

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$< I_d(T_1) >$ average diode current during one LO cycle centered at T_1.

$< I_d(T_3) >$ average diode current during one LO cycle centered at T_3.

$< I_d(T_1)|_{RF} >$ average diode current during one LO cycle centered at T_1 due to the RF source.

$< I_d(T_3)|_{RF} >$ average diode current during one LO cycle centerd at T_3 due to the RF source.

$V_{out}(IF)$ Fourier component of $V_{out}(t)$ at f_{IF}.

$C_L(f)$ mixer conversion loss at the frequency f. Conversion loss is defined to be the ratio of available power from the RF source to the power delivered to the load at the frequency f, $P_{AVS}(f_{RF})/P_{load}(f)$. In this thesis we are interested in $C_L(f_{IF})$.

P_{load} power delivered to the load resistance. It is defined to be equal to $V_{out}^2(IF)/R_L$.

$R_{S_{opt}}$ optimum R_S to achieve minimum $C_L(f_{IF})$.

$R_{L_{opt}}$ optimum R_L to achieve minimum $C_L(f_{IF})$.

Balanced Mixer Terms

V_{bias} DC bias voltage applied in series with each diode in a balanced mixer to model the application of bias. In a practical circuit this is accomplished either by applying bias through an RF choke or by rectification of the LO current.

I_{out} current flowing into the common secondary node between L_2 and L_3. It is also the current flowing into the load impedance, R_L and C_{LD}.

V_{sec} voltage at the common secondary node between L_2 and L_3.

$Z_{in_{RF}}(f)$ input impedance at the RF port at the small signal frequency f.

$Z_{in_{LO}}(f)$ input impedance at the LO port at the small signal frequency f.

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Diode Terminology

Diode Nomenclature

Resistive diode. A resistive diode is a diode that does not have any barrier capacitance. Its current, I_d, and voltage, V_d, can be expressed by $I_d(t) = I_S\ exp(\frac{qV_j}{nkT} - 1)$ and $V_d = V_j + I_d \cdot r_{ser}$.

Exponential diode. An exponential diode is a resistive diode that has no series resistance and whose ideality factor is 1.0. Its current - voltage curve is described by $I_S\ (exp(\frac{qV_d}{kT}) - 1)$ where $V_d = V_j$.

Diode Model

DM_1 diode model corresponding to a medium barrier p-type S_i Schottky diode.

DM_2 diode model corresponding to an NEC; a medium barrier n-type S_i Schottky diode.

DM_3 diode model corresponding to a Toshiba 1-2J1A, a S_i Schottky diode.

I_S diode saturation current.

n ideality function.

ϕ built-in junction voltage.

M capacitive coefficient.

C_{j0} zero-bias barrier capacitance.

r_{ser} series diode resistance.

V_{RB} reverse breakdown voltage.

T_T transit time.

R_B barrier resistance.

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C_B barrier capacitance.

I_d diode current; I_d is composed of two diode currents, that which flows through the barrier resistance and that which flows through the barrier capacitance:

I_{d_r} resistive diode current,

I_{d_c} capacitive diode current.

V_d diode voltage; V_d is the sum of two voltages, the function voltage or that accross the barrier resistance or capacitance and that accross the diode's series resistance:

V_j junction voltage.

L_p parasitic inductance due to diode package.

C_p parasitic capacitance due to diode package.

Amplifier Terminology

Amplifier Circuit Nomenclature

CE a common-emitter amplifier.

CB a common-base amplifier.

CC a common-collector amplifier.

LM-394 is a National Semiconductor superbeta monolithic matched transistor pair.

741 is a general purpose industry standard op-amp.

OP-07 is the Analog Devices ultra-low offset voltage op-amp.

OP-27 is the Analog Devices ultra-low noise precision op-amp.

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Amplifier Terms

A_{VS} is the voltage gain from source to output. Its value depends on the impedance of the load.

APG is the available power gain of the amplifier. Its value depends on the impedance of the load.

APGM is the available power gain of the amplifier under matched conditions.

Transistor Model

The hybrid-π model of the transistor is shown in Table 37. Some of the small-signal elements defined below are depicted in it.

g_m incremental transconductance, $g_m = \frac{qI_C}{kT}$.

β incremental common-emitter short-circuit current gain.

β_0 low frequency value of β, $\beta_0 = g_m\ r_\pi$.

β_F large signal forward-injection common-emitter short-circuit current gain.

r_π incremental resistance from base to emitter.

r_b incremental base resistance.

r_o incremental output resistance, $r_o = \frac{V_A}{I_C}$.

C_π incremental capacitance equal to the sum of the base-charging capacitance and that of the emitter junction.

C_μ incremental feedback capacitance.

V_A Early voltage, typical values for integrated circuit transistors are 50 - 100 V.

f_T frequency where the short-circuit common-emitter current gain falls to unity.

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The direct conversion receiver: Analysis and design of the front-end components

Estabrook, Polly

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ABSTRACT (ENGLISH)

This thesis discusses the design of a direct conversion receiver. This receiver architecture is intended for applications where single channel reception with low cost compact transceivers is desired. The issues of achievable gain and phase match between the receiver's 'I' and 'Q' channel and the design of receiver front-end components are specifically addressed. Designs for a low conversion loss RF mixer whose input frequency is 1GHz or lower, a low frequency (DC to 100's KHz) low noise amplifier, and a low frequency low noise active filter stage are developed and analyzed.

A mixer analysis and design tool has been developed to study the design of low conversion loss mixers with practical diodes, ie. ones having series resistance, barrier resistance, and barrier capacitance. Low levels of barrier capacitance are shown to improve mixer conversion loss over that of a purely resistive diode mixer. Simulation results predict the conversion loss of the direct conversion single-ended mixer to be 3.1dB and that of the balanced mixer to be 2.1dB; both mixers utilize diodes having a barrier capacitance of 0.25pF.

Low frequency amplifier design is performed by analyzing the noise performance of a typical bipolar op-amp input stage. Dominant noise sources are identified; noise temperature is optimized for operation at low frequencies and for low source resistances by selection of the input device and by bias adjustment. Noise figure is estimated to be 3.4dB at 10 Hz and 2.5dB at 1KHz when the amplifier is driven by a source impedance of 2KΩ.

An active filter stage consisting of a cascade of three identical multiple loop feedback filter stages is analyzed by considering the noise contributions of the op-amp and the resistive feedback elements in each stage. Feedback components are chosen to ensure good noise performance when cascaded by the direct conversion amplifier and to provide acceptable in-band gain and adjacent channel rejection. A filter gain of 30dB is realized with an adjacent channel rejection of 34dB and a subsequent channel rejection of 81dB; filter noise figure ranges from 34dB at 25Hz to 22dB at 1KHz.

The expected performance of the direct conversion receiver can be computed from the performance of each of the front-end components. This receiver is found to perform as well as or better than a conventional super-heterodyne receiver with a mixer front-end. It is expected to have smaller volume, lower weight and power consumption, and, to be more versatile than receivers with heterodyne architectures.

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▼FOLIO JSON


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▼Circulation rules

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material-type: book
location-location: SAL3-STACKS
=> loan: 1qtr-3renew-7daygrace
=> request: Allow All
=> notice: Default notice
=> overdue: 3.00/21.00 recall overdue fine
=> lost-item: $75 lost fee
(line 175)
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https://searchworks.stanford.edu/view/1356111,1356111,SPEC-SAL3-U-ARCHIVES,36105049106524,Available,any,any,any,,,RUMSEY-MAP or SPEC-COLL or HILA or CLASSICS,,No loan,
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Responsibility	by Polly Estabrook.
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Physical description	xix, 396 leaves, bound.

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Creators/Contributors

Author/Creator
Estabrook, Polly.

Contributor
Stanford University. Department of Electrical Engineering.

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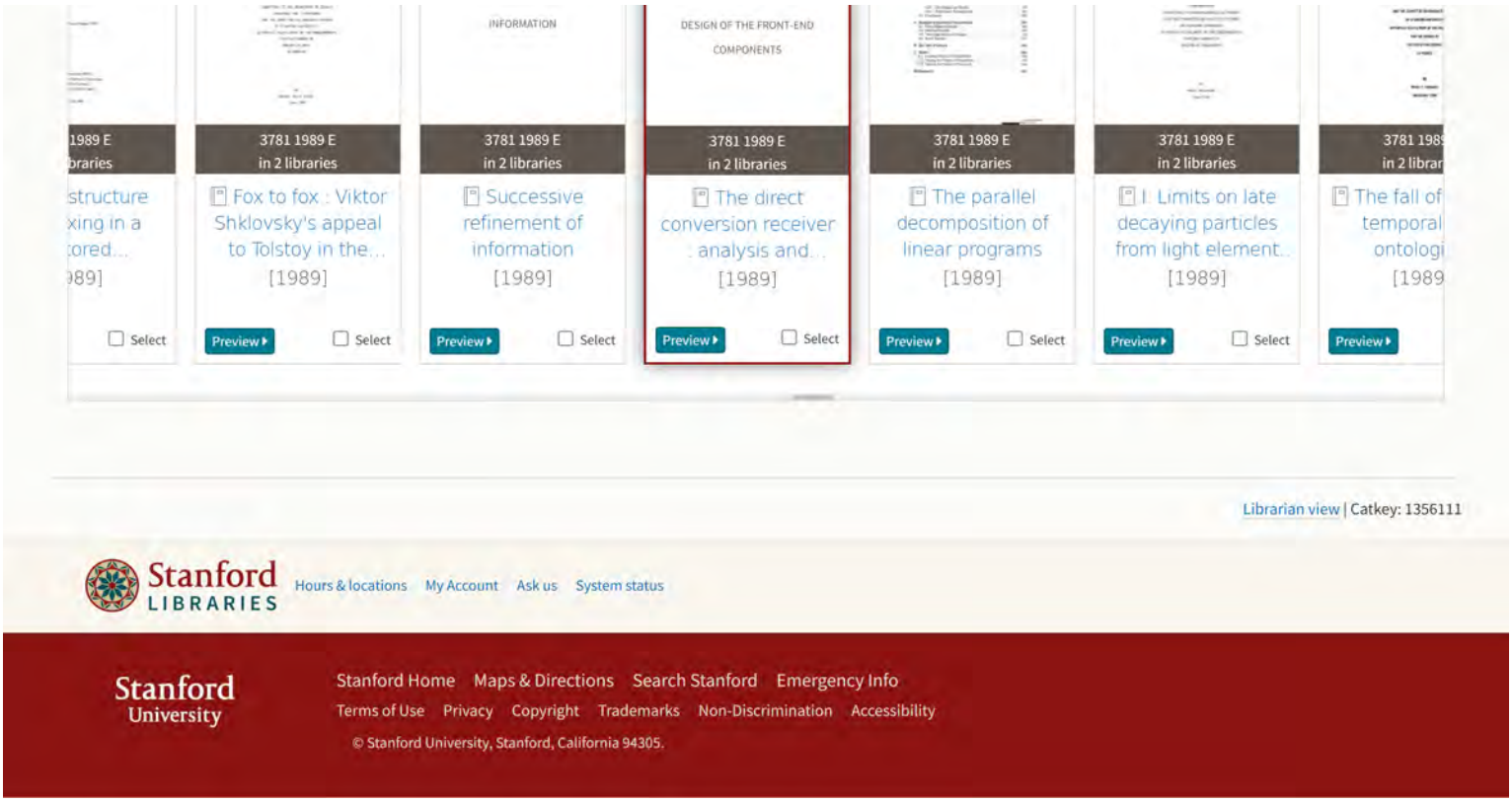
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246     3#$aGateway to new concepts in vehicular technology
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300     ##$a2 v. (901 p.) : $bill. ; $c28 cm.
500     ##$a"IEEE catalog no. 89CH2739-1."
504     ##$aIncludes bibliographical references.
533     ##$aMicrofiche. $bNew York, N.Y., Piscataway, N.J. : $cInstitute of Electrical and Electronics Engineers, $d1989. $e10 microfiche
599     31$aPaper copy donated by Nortel Networks, April 1999.
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Other title	Gateway to new concepts in vehicular technology
Creator/Contributor	IEEE Vehicular Technology Conference (39th : 1989 San Francisco, Calif.) Vehicular Technology Society Institute of Electrical and Electronics Engineers. Santa Clara Valley Section Vehicular Technology Society. San Francisco Bay Area Chapter.
Subjects	Electronics in transportation Mobile communication systems Artificial satellites in telecommunication
Identifier	OCLC : (OCoLC)20047104
Publisher	New York : Institute of Electrical and Electronics Engineers ; Piscataway, N.J. : Order from IEEE Service Center
Creation date	c1989
Format	2 v. (901 p.) : ill. ; 28 cm.
General notes	"IEEE catalog no. 89CH2739-1." Includes bibliographical references.


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245 10 1988 IEEE MTT International Microwave Symposium digest :
       |bMay  25-27, 1988, Marriott Marquis Hotel, Jacob Javits
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260 0  New York :|bInstitute of Electrical and Electronics
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