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This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 C.F.R. § 1.53(c).

Docket Number: 1744.0630000

Type a plus sign (+) inside this box ☐

+

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TITLE OF THE INVENTION (280 Characters Maximum)

**Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology**

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ENCLOSED APPLICATION PARTS (check all that apply)

- ☒ Specification Number of pages: 50
☐ Other: Authorization to Treat a Reply as Incorporating an
☒ Claims Number of pages: 2 Extension of Time under 37 C.F.R. § 1.136(a)(3)(in duplicate)
☒ Drawings Number of sheets: 120
☐ Two return postcards

Method Of Payment (check one)

- ☐ Our Check No. _____ is enclosed to cover the Provisional filing fees.
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The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No

☐ Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

Signature:

Michael O. Lee

Date:

8/4/99

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(if appropriate)

☐ Additional inventors are being named on separately numbered sheets attached hereto.

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

jc670 U.S. PTO



08/04/99

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August 4, 1999

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Washington, D.C. 20231

Box Provisional Application

Express Mail Label No. TB851567178US

Re: U.S. Provisional Patent Application
Appl. No. (to be assigned); Filed: (herewith)
For: **Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology**
Inventors: Sorrells *et al.*
Our Ref: 1744.0630000

Sir:

The following documents are being submitted herewith for appropriate action by the U.S. Patent and Trademark Office:

1. U.S. Provisional Patent Application entitled:

**Wireless Local Area Network (WLAN) Using
Universal Frequency Translation Technology**

and naming as inventors:

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Robert W. Cook
Richard C. Looke
Charley D. Moses, Jr.
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Assistant Commissioner for Patents
August 3, 1999
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the application consisting of:

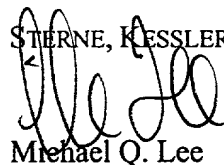
- (a) A Provisional Application for Patent Cover Sheet;
 - (b) A specification containing 53 total pages:
 - (i) 50 pages of description prior to any claims;
 - (ii) 2 pages of claims (1-10 claims); and
 - (iii) a one-page abstract;
 - (c) 20 sheets of drawings: (Figures A-102);
2. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3) (*in duplicate*);
3. Two (2) return postcards.

It is respectfully requested that the two attached postcards be stamped with the filing date and unofficial application number and returned as soon as possible.

This application is being filed under 37 C.F.R. § 1.53(b), without Declaration or filing fee.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Michael Q. Lee
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SKGF Rev. 5/21/99 mac

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Sorrells *et al.*

Appl. No. (to be assigned)

Filed: (herewith)

For: **Wireless Local Area Network
(WLAN) Using Universal
Frequency Translation
Technology**

Art Unit: (to be assigned)

Examiner: (to be assigned)

Atty. Docket: 1744.0630000

Assistant Commissioner for Patents
Washington, D.C. 20231

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Date of Deposit: August 4, 1999 (8/4/99)

I hereby certify that the following attached papers:

1. PTO Cover Letter;
2. Provisional Application Cover Sheet;
3. U.S. Utility Application consisting of 50 pages of Specification, 2 pages of Claims, a one (1) page abstract; and 120 sheets of drawings: (Figures 1A-102);
4. Authorization to Treat a Reply as Incorporating an Extension of Time under 37 C.F.R. § 1.136(a)(3) (in duplicate); and
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are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Commissioner for Patents and Trademarks, Washington, D.C. 20231, or to the Assistant Commissioner for Patents, at the same address.

Michael O. Lee, Reg. No. 35,239
(Printed name of person mailing paper or fee)

(Signature)

Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology

Cross-Reference to Other Applications

The following applications of common assignee are related to the present application, and are
5 herein incorporated by reference in their entireties:

"Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022,
filed October 21, 1998.

"Method and System for Down-Converting Electromagnetic Signals Having Optimized
Switch Structures," Ser. No. 09/293,095, filed April 16, 1999.

10 "Method and System for Down-Converting Electromagnetic Signals Including Resonant
Structures for Enhanced Energy Transfer," Ser. No. 09/293,342, filed April 16, 1999.

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21,
1998.

15 "Method and System for Frequency Up-Conversion Having Optimized Switch Structures,"
Ser. No. 09/293,097, filed April 16, 1999.

"Method and System for Frequency Up-Conversion with a Variety of Transmitter
Configurations," Ser. No. 09/293,580, filed April 16, 1999.

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998.

"Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed October 21, 1998.

5 "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," Ser. No. 09/293,283, filed April 16, 1999.

"Universal Frequency Translation, and Applications of Same," Ser. No. 09/176,027, filed October 21, 1998.

"Applications of Universal Frequency Translation," Ser. No. 09/261,129, filed March 3, 1999.

Background of the Invention

Field of the Invention

The present invention is generally related to frequency translation, and applications of same.

Related Art

5 Various communication components exist for performing frequency down-conversion, frequency up-conversion, and filtering. Also, schemes exist for signal reception in the face of potential jamming signals.

Summary of the Invention

10 The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

15 Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost character(s) and/or digit(s) in the corresponding reference number.

Brief Description of the Figures

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. 1A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention;

FIG. 1D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 2 is a block diagram of a universal frequency translation (UFT) module according to an alternative embodiment of the invention;

FIG. 3 is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 4 is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 5 is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention;

FIGS. 6A-6I illustrate example waveforms used to describe the operation of the UFU module;

FIG. 7 illustrates a UFT module used in a receiver according to an embodiment of the invention;

FIG. 8 illustrates a UFT module used in a transmitter according to an embodiment of the invention;

FIG. 9 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using a UFT module of the invention;

FIG. 10 illustrates a transceiver according to an embodiment of the invention;

FIG. 11 illustrates a transceiver according to an alternative embodiment of the invention;

FIG. 12 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention;

FIG. 13 illustrates a UFT module used in a unified down-conversion and filtering (UDF) module according to an embodiment of the invention;

FIG. 14 illustrates an example receiver implemented using a UDF module according to an embodiment of the invention;

FIGS. 15A-15F illustrate example applications of the UDF module according to embodiments of the invention;

FIG. 16 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention, wherein the receiver may be further implemented using one or more UFD modules of the invention;

FIG. 17 illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention;

FIG. 18 is a table of example values at nodes in the UDF module of FIG. 17;

FIG. 19 is a detailed diagram of an example UDF module according to an embodiment of the invention;

FIGS. 20A and 20A-1 are example aliasing modules according to embodiments of the invention;

FIGS. 20B-20F are example waveforms used to describe the operation of the aliasing modules of FIGS. 20A and 20A-1;

FIG. 21 illustrates an enhanced signal reception system according to an embodiment of the invention;

FIGS. 22A-22F are example waveforms used to describe the system of FIG. 21;

FIG. 23A illustrates an example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23B and 23C are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 23D illustrates another example transmitter in an enhanced signal reception system according to an embodiment of the invention;

5 FIGS. 23E and 23F are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 24A illustrates an example receiver in an enhanced signal reception system according to an embodiment of the invention;

10 FIGS. 24B-24J are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 25 illustrates a block diagram of an example computer network;

FIG. 26 illustrates a block diagram of an example computer network;

FIG. 27 illustrates a block diagram of an example wireless interface;

15 FIG. 28 illustrates an example heterodyne implementation of the wireless interface illustrated in FIG. 27;

FIG. 29 illustrates an example in-phase/quadrature-phase (I/Q) heterodyne implementation of the interface illustrated in FIG. 27;

FIG. 30 illustrates an example high level block diagram of the interface illustrated in FIG. 27, in accordance with the present invention;

20 FIG. 31 illustrates a example block diagram of the interface illustrated in FIG. 29, in accordance with the invention;

FIG. 32 illustrates an example I/Q implementation of the interface illustrated in FIG.31;

FIGS. 33-38 illustrate example environments encompassed by the invention;

25 FIG. 39 illustrates a block diagram of a WLAN interface according to an embodiment of the invention;

FIG. 40 illustrates a WLAN receiver according to an embodiment of the invention;

FIG. 41 illustrates a WLAN transmitter according to an embodiment of the invention;

FIGS. 42-44 are example implementations of a WLAN interface;

FIGS. 45, 46A, and 46B relate to an example MAC interface for an example WLAN interface embodiment;

FIGS. 47, 48, 49A, and 49B relate to an example demodulator/modulator facilitation module
5 for an example WLAN interface embodiment;

FIGS. 50, 51, 52A, and 52B relate to an example alternate demodulator/modulator facilitation module for an example WLAN interface embodiment;

FIGS. 53 and 54 relate to an example receiver for an example WLAN interface embodiment;

FIGS. 55, 56A, and 56B relate to an example synthesizer for an example WLAN interface
10 embodiment;

FIGS. 57, 58, 59, 60, 61A, and 61B relate to an example transmitter for an example WLAN interface embodiment;

FIGS. 62 and 63 relate to an example motherboard for an example WLAN interface
15 embodiment;

FIGS. 64, 65, and 66 relate to example LNAs for an example WLAN interface embodiment;

FIGS. 67-101 illustrate test results for an example WLAN interface embodiment of the
invention; and

FIG. 102 is an example PCMCIA test bed assembly for a WLAN interface according to an
embodiment of the invention.

Detailed Description of the Preferred Embodiments

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 - 6.1.2 Example Modifications
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7. Conclusions

1. *Universal Frequency Translation*

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

FIG. 1A illustrates a universal frequency translation (UFT) module 102 according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

As indicated by the example of FIG. 1A, some embodiments of the UFT module 102 include three ports (nodes), designated in FIG. 1A as Port 1, Port 2, and Port 3. Other UFT embodiments include other than three ports.

Generally, the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module 102 (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

An example embodiment of the UFT module 103 is generally illustrated in FIG. 1B. Generally, the UFT module 103 includes a switch 106 controlled by a control signal 108. The switch 106 is said to be a controlled switch.

As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. 2 illustrates an example UFT module 202. The example UFT module 202 includes a diode 204 having two ports, designated as Port 1 and Port 2/3. This embodiment does not include a third port, as indicated by the dotted line around the "Port 3" label.

The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

For example, a UFT module 115 can be used in a universal frequency down-conversion (UFD) module 114, an example of which is shown in FIG. 1C. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

As another example, as shown in FIG. 1D, a UFT module 117 can be used in a universal frequency up-conversion (UFU) module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal.

These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2. *Frequency Down-Conversion*

The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in co-pending U.S. Patent Application entitled "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, the full disclosure of which is incorporated herein by reference. A relevant portion of the above mentioned patent application is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. 20A illustrates an aliasing module 2000 (also called a universal frequency down-conversion module) for down-conversion using a universal frequency translation (UFT) module 2002

which down-converts an EM input signal 2004. In particular embodiments, aliasing module 2000 includes a switch 2008 and a capacitor 2010. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 20A-1), the capacitor 2010 is in series with the input signal 2004 and the switch 2008 is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module 2000 with UFT module 2002 can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal 2004.

In one implementation, aliasing module 2000 down-converts the input signal 2004 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 2000 down-converts the input signal 2004 to a demodulated baseband signal. In yet another implementation, the input signal 2004 is a frequency modulated (FM) signal, and the aliasing module 2000 down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal 2006 includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 2004. In this embodiment, the control signal 2006 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 2004. Preferably, the frequency of control signal 2006 is much less than the input signal 2004.

A train of pulses 2018 as shown in FIG. 20D controls the switch 2008 to alias the input signal 2004 with the control signal 2006 to generate a down-converted output signal 2012. More specifically, in an embodiment, switch 2008 closes on a first edge of each pulse 2020 of FIG. 20D and opens on a second edge of each pulse. When the switch 2008 is closed, the input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal to the capacitor 2010. The charge stored during successive pulses forms down-converted output signal 2012.

Exemplary waveforms are shown in FIGS. 20B-20F.

FIG. 20B illustrates an analog amplitude modulated (AM) carrier signal 2014 that is an example of input signal 2004. For illustrative purposes, in FIG. 20C, an analog AM carrier signal portion 2016 illustrates a portion of the analog AM carrier signal 2014 on an expanded time scale. The analog AM carrier signal portion 2016 illustrates the analog AM carrier signal 2014 from time t_0 to time t_1 .

FIG. 20D illustrates an exemplary aliasing signal 2018 that is an example of control signal 2006. Aliasing signal 2018 is on approximately the same time scale as the analog AM carrier signal portion 2016. In the example shown in FIG. 20D, the aliasing signal 2018 includes a train of pulses 2020 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 2020 repeat at an aliasing rate, or pulse repetition rate of aliasing signal 2018. The aliasing rate is determined as described below, and further described in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000.

As noted above, the train of pulses 2020 (i.e., control signal 2006) control the switch 2008 to alias the analog AM carrier signal 2016 (i.e., input signal 2004) at the aliasing rate of the aliasing signal 2018. Specifically, in this embodiment, the switch 2008 closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch 2008 is closed, input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal 2004 to the capacitor 2010. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 2022 form down-converted signal portion 2024 (FIG. 20E) that corresponds to the analog AM carrier signal portion 2016 (FIG. 20C) and the train of pulses 2020 (FIG. 20D). The charge stored during successive under-samples of AM carrier signal 2014 form the down-converted signal 2024 (FIG. 20E) that is an example of down-converted output signal 2012 (FIG. 20A). In FIG. 20F, a demodulated baseband signal 2026 represents the demodulated baseband signal 2024 after filtering on a compressed time scale. As illustrated, down-converted signal 2026 has

substantially the same "amplitude envelope" as AM carrier signal 2014. Therefore, FIGS. 20B-20F illustrate down-conversion of AM carrier signal 2014.

The waveforms shown in FIGS. 20B-20F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No.09/176,022, Attorney Docket Number 1744.0010000.

The aliasing rate of control signal 2006 determines whether the input signal 2004 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 2004, the aliasing rate of the control signal 2006, and the down-converted output signal 2012 are illustrated below:

$$\begin{aligned} (\text{Freq. of input signal 2004}) &= n \cdot (\text{Freq. of control signal 2006}) \pm \\ &(\text{Freq. of down-converted output signal 2012}) \end{aligned}$$

For the examples contained herein, only the "+" condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal 2004 (e.g., $n = 0.5, 1, 2, 3, \dots$).

When the aliasing rate of control signal 2006 is off-set from the frequency of input signal 2004, or off-set from a harmonic or sub-harmonic thereof, input signal 2004 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 2004. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal 2006 would be calculated as follows:

$$\begin{aligned} (\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n &= \text{Freq}_{\text{control}} \\ (901 \text{ MHz} - 1 \text{ MHz})/n &= 900/n \end{aligned}$$

For $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 would be substantially equal to 1.8 GHz, 900 MHz, 450 MHz, 300 MHz, 225 MHz, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signals, and exemplary methods and systems thereof, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000.

Alternatively, when the aliasing rate of the control signal 2006 is substantially equal to the frequency of the input signal 2004, or substantially equal to a harmonic or sub-harmonic thereof, input signal 2004 is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-sampling pulses occur at the same point of subsequent cycles of the input signal 2004. As a result, the under-samples form a constant output baseband signal. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHz input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 2006 would be calculated as follows:

$$\begin{aligned} (\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n &= \text{Freq}_{\text{control}} \\ (900 \text{ MHz} - 0 \text{ MHz})/n &= 900 \text{ MHz}/n \end{aligned}$$

For $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHz, 450 MHz, 300 MHz, 225 MHz, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. _09/176,022, Attorney
5 Docket Number 1744.0010000.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1 + F_2) \div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal 2006 would be calculated as follows:

$$\begin{aligned} \text{Frequency of the input} &= (F_1 + F_2) \div 2 \\ &= (899 \text{ MHZ} + 901 \text{ MHZ}) \div 2 \\ &= 900 \text{ MHZ} \end{aligned}$$

Frequency of the down-converted signal = 0 (i.e., baseband)

$$\begin{aligned} (\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n &= \text{Freq}_{\text{control}} \\ (900 \text{ MHZ} - 0 \text{ MHZ})/n &= 900 \text{ MHZ}/n \end{aligned}$$

For $n = 0.5, 1, 2, 3$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2 .

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHz and F_2 equal to 901 MHz, to an ASK signal, the aliasing rate of the control signal 2006 should be substantially equal to:

$$(900 \text{ MHz} - 0 \text{ MHz})/n = 900 \text{ MHz}/n, \text{ or}$$

$$(901 \text{ MHz} - 0 \text{ MHz})/n = 901 \text{ MHz}/n.$$

For the former case of $900 \text{ MHz}/n$, and for $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHz, 450 MHz, 300 MHz, 225 MHz, etc. For the latter case of $901 \text{ MHz}/n$, and for $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.802 GHz, 901 MHz, 450.5 MHz, 300.333 MHz, 225.25 MHz, etc. The frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHz).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000.

In an embodiment, the pulses of the control signal 2006 have negligible apertures that tend towards zero. This makes the UFT module 2002 a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal 2006 have non-negligible apertures that tend away from zero. This makes the UFT module 2002 a lower input impedance device. This allows the lower input impedance of the UFT module 2002 to be substantially matched with a source impedance of the input signal 2004. This also improves the energy transfer from the input signal 2004

to the down-converted output signal 2012, and hence the efficiency and signal to noise (s/n) ratio of UFT module 2002.

Exemplary systems and methods for generating and optimizing the control signal 2006, and for otherwise improving energy transfer and s/n ratio, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000.

3. *Frequency Up-Conversion*

The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

An example frequency up-conversion system 300 is illustrated in FIG. 3. The frequency up-conversion system 300 is now described.

An input signal 302 (designated as "Control Signal" in FIG. 3) is accepted by a switch module 304. For purposes of example only, assume that the input signal 302 is a FM input signal 606, an example of which is shown in FIG. 6C. FM input signal 606 may have been generated by modulating information signal 602 onto oscillating signal 604 (FIGS. 6A and 6B). It should be understood that the invention is not limited to this embodiment. The information signal 602 can be analog, digital, or any combination thereof, and any modulation scheme can be used.

The output of switch module 304 is a harmonically rich signal 306, shown for example in FIG. 6D as a harmonically rich signal 608. The harmonically rich signal 608 has a continuous and periodic waveform.

FIG. 6E is an expanded view of two sections of harmonically rich signal 608, section 610 and section 612. The harmonically rich signal 608 may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a

similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

Harmonically rich signal 608 is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal 608. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. 6F and FIG. 6G show separately the sinusoidal components making up the first, third, and fifth harmonics of section 610 and section 612. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal 608 is shown as a square wave, there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. 6H.

The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal 306 and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal 306. According to an embodiment of the invention, the input signal 606 may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

A filter 308 filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal 310, shown for example as a filtered output signal 614 in FIG. 6I.

FIG. 4 illustrates an example universal frequency up-conversion (UFU) module 401. The UFU module 401 includes an example switch module 304, which comprises a bias signal 402, a resistor or impedance 404, a universal frequency translator (UFT) 450, and a ground 408. The UFT 450 includes a switch 406. The input signal 302 (designated as "Control Signal" in FIG. 4) controls the switch 406 in the UFT 450, and causes it to close and open. Harmonically rich signal 306 is generated at a node 405 located between the resistor or impedance 404 and the switch 406.

Also in FIG. 4, it can be seen that an example filter 308 is comprised of a capacitor 410 and an inductor 412 shunted to a ground 414. The filter is designed to filter out the undesired harmonics of harmonically rich signal 306.

The invention is not limited to the UFU embodiment shown in FIG. 4.

For example, in an alternate embodiment shown in FIG. 5, an unshaped input signal 501 is routed to a pulse shaping module 502. The pulse shaping module 502 modifies the unshaped input signal 501 to generate a (modified) input signal 302 (designated as the "Control Signal" in FIG. 5).
5 The input signal 302 is routed to the switch module 304, which operates in the manner described above. Also, the filter 308 of FIG. 5 operates in the manner described above.

The purpose of the pulse shaping module 502 is to define the pulse width of the input signal 302. Recall that the input signal 302 controls the opening and closing of the switch 406 in switch module 304. During such operation, the pulse width of the input signal 302 establishes the pulse width of the harmonically rich signal 306. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal 306 are a function of at least the pulse width of the harmonically rich signal 306. As such, the pulse width of the input signal 302 contributes to setting the relative amplitudes of the harmonics of harmonically rich signal 306.
10

Further details of up-conversion as described in this section are presented in pending U.S. application "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, incorporated herein by reference in its entirety.
15

4. *Enhanced Signal Reception*

The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same.

Referring to FIG. 21, transmitter 2104 accepts a modulating baseband signal 2102 and generates (transmitted) redundant spectrums 2106a-n, which are sent over communications medium 2108. Receiver 2112 recovers a demodulated baseband signal 2114 from (received) redundant spectrums 2110a-n. Demodulated baseband signal 2114 is representative of the modulating baseband signal 2102, where the level of similarity between the modulating baseband signal 2114 and the
20 modulating baseband signal 2102 is application dependent.
25

Modulating baseband signal 2102 is preferably any information signal desired for transmission and/or reception. An example modulating baseband signal 2202 is illustrated in FIG. 22A, and has an associated modulating baseband spectrum 2204 and image spectrum 2203 that are illustrated in FIG. 22B. Modulating baseband signal 2202 is illustrated as an analog signal in FIG. 22a, but could also be a digital signal, or combination thereof. Modulating baseband signal 2202 could be a voltage (or current) characterization of any number of real world occurrences, including for example and without limitation, the voltage (or current) representation for a voice signal.

Each transmitted redundant spectrum 2106a-n contains the necessary information to substantially reconstruct the modulating baseband signal 2102. In other words, each redundant spectrum 2106a-n contains the necessary amplitude, phase, and frequency information to reconstruct the modulating baseband signal 2102.

FIG. 22C illustrates example transmitted redundant spectrums 2206b-d. Transmitted redundant spectrums 2206b-d are illustrated to contain three redundant spectrums for illustration purposes only. Any number of redundant spectrums could be generated and transmitted as will be explained in following discussions.

Transmitted redundant spectrums 2206b-d are centered at f_1 , with a frequency spacing f_2 between adjacent spectrums. Frequencies f_1 and f_2 are dynamically adjustable in real-time as will be shown below. FIG. 22D illustrates an alternate embodiment, where redundant spectrums 2208c,d are centered on unmodulated oscillating signal 2209 at f_1 (Hz). Oscillating signal 2209 may be suppressed if desired using, for example, phasing techniques or filtering techniques. Transmitted redundant spectrums are preferably above baseband frequencies as is represented by break 2205 in the frequency axis of FIGS. 22C and 22D.

Received redundant spectrums 2110a-n are substantially similar to transmitted redundant spectrums 2106a-n, except for the changes introduced by the communications medium 2108. Such changes can include but are not limited to signal attenuation, and signal interference. FIG. 22E illustrates example received redundant spectrums 2210b-d. Received redundant spectrums 2210b-d are substantially similar to transmitted redundant spectrums 2206b-d, except that redundant spectrum

2210c includes an undesired jamming signal spectrum 2211 in order to illustrate some advantages of the present invention. Jamming signal spectrum 2211 is a frequency spectrum associated with a jamming signal. For purposes of this invention, a "jamming signal" refers to any unwanted signal, regardless of origin, that may interfere with the proper reception and reconstruction of an intended signal. Furthermore, the jamming signal is not limited to tones as depicted by spectrum 2211, and can have any spectral shape, as will be understood by those skilled in the art(s).

As stated above, demodulated baseband signal 2114 is extracted from one or more of received redundant spectrums 2210b-d. FIG. 22F illustrates example demodulated baseband signal 2212 that is, in this example, substantially similar to modulating baseband signal 2202 (FIG. 22A); where in practice, the degree of similarity is application dependent.

An advantage of the present invention should now be apparent. The recovery of modulating baseband signal 2202 can be accomplished by receiver 2112 in spite of the fact that high strength jamming signal(s) (e.g. jamming signal spectrum 2211) exist on the communications medium. The intended baseband signal can be recovered because multiple redundant spectrums are transmitted, where each redundant spectrum carries the necessary information to reconstruct the baseband signal. At the destination, the redundant spectrums are isolated from each other so that the baseband signal can be recovered even if one or more of the redundant spectrums are corrupted by a jamming signal.

Transmitter 2104 will now be explored in greater detail. FIG. 23A illustrates transmitter 2301, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2206b-d. Transmitter 2301 includes generator 2303, optional spectrum processing module 2304, and optional medium interface module 2320. Generator 2303 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

Transmitter 2301 operates as follows. First oscillator 2302 and second oscillator 2309 generate a first oscillating signal 2305 and second oscillating signal 2312, respectively. First stage modulator 2306 modulates first oscillating signal 2305 with modulating baseband signal 2202, resulting in modulated signal 2308. First stage modulator 2306 may implement any type of

modulation including but not limited to: amplitude modulation, frequency modulation, phase modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates modulated signal 2308 with second oscillating signal 2312, resulting in multiple redundant spectrums 2206a-n shown in FIG. 23B. Second stage modulator 2310 is preferably a phase modulator, or a frequency modulator, although other types of modulation may be implemented including but not limited to amplitude modulation. Each redundant spectrum 2206a-n contains the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal 2202.

Redundant spectrums 2206a-n are substantially centered around f_1 , which is the characteristic frequency of first oscillating signal 2305. Also, each redundant spectrum 2206a-n (except for 2206c) is offset from f_1 by approximately a multiple of f_2 (Hz), where f_2 is the frequency of the second oscillating signal 2312. Thus, each redundant spectrum 2206a-n is offset from an adjacent redundant spectrum by f_2 (Hz). This allows the spacing between adjacent redundant spectrums to be adjusted (or tuned) by changing f_2 that is associated with second oscillator 2309. Adjusting the spacing between adjacent redundant spectrums allows for dynamic real-time tuning of the bandwidth occupied by redundant spectrums 2206a-n.

In one embodiment, the number of redundant spectrums 2206a-n generated by transmitter 2301 is arbitrary and may be unlimited as indicated by the "a-n" designation for redundant spectrums 2206a-n. However, a typical communications medium will have a physical and/or administrative limitations (i.e. FCC regulations) that restrict the number of redundant spectrums that can be practically transmitted over the communications medium. Also, there may be other reasons to limit the number of redundant spectrums transmitted. Therefore, preferably, the transmitter 2301 will include an optional spectrum processing module 2304 to process the redundant spectrums 2206a-n prior to transmission over communications medium 2108.

In one embodiment, spectrum processing module 2304 includes a filter with a passband 2207 (FIG. 23C) to select redundant spectrums 2206b-d for transmission. This will substantially limit the frequency bandwidth occupied by the redundant spectrums to the passband 2207. In one embodiment,

spectrum processing module 2304 also up converts redundant spectrums and/or amplifies redundant spectrums prior to transmission over the communications medium 2108. Finally, medium interface module 2320 transmits redundant spectrums over the communications medium 2108. In one embodiment, communications medium 2108 is an over-the-air link and medium interface module 2320 is an antenna. Other embodiments for communications medium 2108 and medium interface module 2320 will be understood based on the teachings contained herein.

FIG. 23D illustrates transmitter 2321, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2208c-d and unmodulated spectrum 2209. Transmitter 2321 includes generator 2311, spectrum processing module 2304, and (optional) medium interface module 2320. Generator 2311 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

As shown in FIG. 23D, many of the components in transmitter 2321 are similar to those in transmitter 2301. However, in this embodiment, modulating baseband signal 2202 modulates second oscillating signal 2312. Transmitter 2321 operates as follows. First stage modulator 2306 modulates second oscillating signal 2312 with modulating baseband signal 2202, resulting in modulated signal 2322. As described earlier, first stage modulator 2306 can effect any type of modulation including but not limited to: amplitude modulation frequency modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates first oscillating signal 2304 with modulated signal 2322, resulting in redundant spectrums 2208a-n, as shown in FIG. 23E. Second stage modulator 2310 is preferably a phase or frequency modulator, although other modulators could be used including but not limited to an amplitude modulator.

Redundant spectrums 2208a-n are centered on unmodulated spectrum 2209 (at f_1 Hz), and adjacent spectrums are separated by f_2 Hz. The number of redundant spectrums 2208a-n generated by generator 2311 is arbitrary and unlimited, similar to spectrums 2206a-n discussed above. Therefore, optional spectrum processing module 2304 may also include a filter with passband 2325 to select, for example, spectrums 2208c,d for transmission over communications medium 2108. In addition, optional spectrum processing module 2304 may also include a filter (such as a bandstop

filter) to attenuate unmodulated spectrum 2209. Alternatively, unmodulated spectrum 2209 may be attenuated by using phasing techniques during redundant spectrum generation. Finally, (optional) medium interface module 2320 transmits redundant spectrums 2208c,d over communications medium 2108.

5 Receiver 2112 will now be explored in greater detail to illustrate recovery of a demodulated baseband signal from received redundant spectrums. FIG. 24A illustrates receiver 2430, which is one embodiment of receiver 2112. Receiver 2430 includes optional medium interface module 2402, down-converter 2404, spectrum isolation module 2408, and data extraction module 2414. Spectrum isolation module 2408 includes filters 2410a-c. Data extraction module 2414 includes demodulators 2416a-c, error check modules 2420a-c, and arbitration module 2424. Receiver 2430 will be discussed in relation to the signal diagrams in FIGS. 24B-24J.

10 In one embodiment, optional medium interface module 2402 receives redundant spectrums 2210b-d (FIG. 22E, and FIG. 24B). Each redundant spectrum 2210b-d includes the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal used to generate the redundant spectrums. However, in the present example, spectrum 2210c also contains jamming signal 2211, which may interfere with the recovery of a baseband signal from spectrum 2210c. Down-converter 2404 down-converts received redundant spectrums 2210b-d to lower intermediate frequencies, resulting in redundant spectrums 2406a-c (FIG. 24C). Jamming signal 2211 is also down-converted to jamming signal 2407, as it is contained within redundant spectrum 2406b. Spectrum isolation module 2408 includes filters 2410a-c that isolate redundant spectrums 2406a-c from each other (FIGS. 24D-24F, respectively). Demodulators 2416a-c independently demodulate spectrums 2406a-c, resulting in demodulated baseband signals 2418a-c, respectively (FIGS. 24G-24I). Error check modules 2420a-c analyze demodulated baseband signal 2418a-c to detect any errors. In one embodiment, each error check module 2420a-c sets an error flag 2422a-c whenever an error is detected in a demodulated baseband signal. Arbitration module 2424 accepts the demodulated baseband signals and associated error flags, and selects a substantially error-free demodulated baseband signal (FIG. 24J). In one embodiment, the substantially error-free

demodulated baseband signal will be substantially similar to the modulating baseband signal used to generate the received redundant spectrums, where the degree of similarity is application dependent.

Referring to FIGS. 24G-I, arbitration module 2424 will select either demodulated baseband signal 2418a or 2418c, because error check module 2420b will set the error flag 2422b that is associated with demodulated baseband signal 2418b.

The error detection schemes implemented by the error detection modules include but are not limited to: cyclic redundancy check (CRC) and parity check for digital signals, and various error detections schemes for analog signal.

Further details of enhanced signal reception as described in this section are presented in pending U.S. application "Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998, incorporated herein by reference in its entirety.

5. *Unified Down-Conversion and Filtering*

The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

FIG. 17 is a conceptual block diagram of a UDF module 1702 according to an embodiment of the present invention. The UDF module 1702 performs at least frequency translation and frequency selectivity.

The effect achieved by the UDF module 1702 is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module 1702 effectively performs input filtering.

According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals 1704 received by the UDF module 1702 are at radio frequencies. The UDF module 1702 effectively operates to input filter these RF input signals 1704. Specifically, in these embodiments, the UDF module 1702 effectively performs input, channel select filtering of the RF input signal 1704. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module 1702 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module 1702 includes a frequency translator 1708. The frequency translator 1708 conceptually represents that portion of the UDF module 1702 that performs frequency translation (down conversion).

The UDF module 1702 also conceptually includes an apparent input filter 1706 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1706 represents that portion of the UDF module 1702 that performs input filtering.

In practice, the input filtering operation performed by the UDF module 1702 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter 1706 is herein referred to as an "apparent" input filter 1706.

The UDF module 1702 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1702. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1702 can be designed with a filter center frequency f_c on the order of 900
5 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where
10 Q factor as discussed herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_c of the UDF module 1702 can be electrically adjusted, either statically or dynamically.

Also, the UDF module 1702 can be designed to amplify input signals.

Further, the UDF module 1702 can be implemented without large resistors, capacitors, or
15 inductors. Also, the UDF module 1702 does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1702 is friendly to integrated circuit design techniques and processes.

The features and advantages exhibited by the UDF module 1702 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation.
20 Specifically, according to the present invention, the UDF module 1702 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

According to embodiments of the present invention, the UDF module generates an output
25 signal from an input signal using samples/instances of the input signal and samples/instances of the output signal.

More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

Next, the input sample is held (that is, delayed).

Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

FIG. 19 illustrates an example implementation of the unified down-converting and filtering (UDF) module 1922. The UDF module 1922 performs the frequency translation operation and the frequency selectivity operation in an integrated, unified manner as described above, and as further described below.

In the example of FIG. 19, the frequency selectivity operation performed by the UDF module 1922 comprises a band-pass filtering operation according to EQ. 1, below, which is an example representation of a band-pass filtering transfer function.

$$VO = \alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \quad \text{EQ. 1}$$

It should be noted, however, that the invention is not limited to band-pass filtering. Instead, the invention effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof. As will be appreciated, there are many representations of any given filter type. The invention is applicable to these filter representations. Thus, EQ. 1 is referred to herein for illustrative purposes only, and is not limiting.

The UDF module 1922 includes a down-convert and delay module 1924, first and second delay modules 1928 and 1930, first and second scaling modules 1932 and 1934, an output sample and hold module 1936, and an (optional) output smoothing module 1938. Other embodiments of the UDF module will have these components in different configurations, and/or a subset of these components, and/or additional components. For example, and without limitation, in the configuration shown in FIG. 19, the output smoothing module 1938 is optional.

As further described below, in the example of FIG. 19, the down-convert and delay module 1924 and the first and second delay modules 1928 and 1930 include switches that are controlled by a clock having two phases, ϕ_1 and ϕ_2 . ϕ_1 and ϕ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low.

Preferably, each of these switches closes on a rising edge of ϕ_1 or ϕ_2 , and opens on the next corresponding falling edge of ϕ_1 or ϕ_2 . However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. 19, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module 1924 is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The example UDF module 1922 has a filter center frequency of 900.2 MHZ and a filter bandwidth of 570 KHz. The pass band of the UDF module 1922 is on the order of 899.915 MHZ to 900.485 MHZ. The Q factor of the UDF module 1922 is approximately 1879 (i.e., 900.2 MHZ divided by 570 KHz).

5 The operation of the UDF module 1922 shall now be described with reference to a Table 1802 (FIG. 18) that indicates example values at nodes in the UDF module 1922 at a number of consecutive time increments. It is assumed in Table 1802 that the UDF module 1922 begins operating at time $t-1$. As indicated below, the UDF module 1922 reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

10 At the rising edge of ϕ_1 at time $t-1$, a switch 1950 in the down-convert and delay module 1924 closes. This allows a capacitor 1952 to charge to the current value of an input signal, VI_{t-1} , such that node 1902 is at VI_{t-1} . This is indicated by cell 1804 in FIG. 18. In effect, the combination of the switch 1950 and the capacitor 1952 in the down-convert and delay module 1924 operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor 1952 represents an instance of a down-converted image of the input signal VI .

15 The manner in which the down-convert and delay module 1924 performs frequency down-conversion is further described elsewhere in this application, and is additionally described in pending U.S. application "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, which is herein incorporated by reference in its entirety.

20 Also at the rising edge of ϕ_1 at time $t-1$, a switch 1958 in the first delay module 1928 closes, allowing a capacitor 1960 to charge to VO_{t-1} , such that node 1906 is at VO_{t-1} . This is indicated by cell 1806 in Table 1802. (In practice, VO_{t-1} is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

Also at the rising edge of ϕ_1 at time $t-1$, a switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to a value stored in a capacitor 1964. At this time, however, the value in capacitor 1964 is undefined, so the value in capacitor 1968 is undefined. This is indicated by cell 1807 in table 1802.

5 At the rising edge of ϕ_2 at time $t-1$, a switch 1954 in the down-convert and delay module 1924 closes, allowing a capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_{t-1} , such that node 1904 is at VI_{t-1} . This is indicated by cell 1810 in Table 1802.

10 The UDF module 1922 may optionally include a unity gain module 1990A between capacitors 1952 and 1956. The unity gain module 1990A operates as a current source to enable capacitor 1956 to charge without draining the charge from capacitor 1952. For a similar reason, the UDF module 1922 may include other unity gain modules 1990B-1990G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules 1990A-1990G are optional. The structure and operation of the unity gain modules 1990 will be apparent to persons skilled in the
15 relevant art(s).

Also at the rising edge of ϕ_2 at time $t-1$, a switch 1962 in the first delay module 1928 closes, allowing a capacitor 1964 to charge to the level of the capacitor 1960. Accordingly, the capacitor 1964 charges to VO_{t-1} , such that node 1908 is at VO_{t-1} . This is indicated by cell 1814 in Table 1802.

20 Also at the rising edge of ϕ_2 at time $t-1$, a switch 1970 in the second delay module 1930 closes, allowing a capacitor 1972 to charge to a value stored in a capacitor 1968. At this time, however, the value in capacitor 1968 is undefined, so the value in capacitor 1972 is undefined. This is indicated by cell 1815 in table 1802.

25 At time t , at the rising edge of ϕ_1 , the switch 1950 in the down-convert and delay module 1924 closes. This allows the capacitor 1952 to charge to VI_t , such that node 1902 is at VI_t . This is indicated in cell 1816 of Table 1802.

Also at the rising edge of ϕ_1 at time t , the switch 1958 in the first delay module 1928 closes, thereby allowing the capacitor 1960 to charge to VO_t . Accordingly, node 1906 is at VO_t . This is indicated in cell 1820 in Table 1802.

Further at the rising edge of ϕ_1 at time t , the switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to the level of the capacitor 1964. Therefore, the capacitor 1968 charges to VO_{t-1} , such that node 1910 is at VO_{t-1} . This is indicated by cell 1824 in Table 1802.

At the rising edge of ϕ_2 at time t , the switch 1954 in the down-convert and delay module 1924 closes, allowing the capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_t , such that node 1904 is at VI_t . This is indicated by cell 1828 in Table 1802.

Also at the rising edge of ϕ_2 at time t , the switch 1962 in the first delay module 1928 closes, allowing the capacitor 1964 to charge to the level in the capacitor 1960. Therefore, the capacitor 1964 charges to VO_t , such that node 1908 is at VO_t . This is indicated by cell 1832 in Table 1802.

Further at the rising edge of ϕ_2 at time t , the switch 1970 in the second delay module 1930 closes, allowing the capacitor 1972 in the second delay module 1930 to charge to the level of the capacitor 1968 in the second delay module 1930. Therefore, the capacitor 1972 charges to VO_{t-1} , such that node 1912 is at VO_{t-1} . This is indicated in cell 1836 of FIG. 18.

At time $t+1$, at the rising edge of ϕ_1 , the switch 1950 in the down-convert and delay module 1924 closes, allowing the capacitor 1952 to charge to VI_{t+1} . Therefore, node 1902 is at VI_{t+1} , as indicated by cell 1838 of Table 1802.

Also at the rising edge of ϕ_1 at time $t+1$, the switch 1958 in the first delay module 1928 closes, allowing the capacitor 1960 to charge to VO_{t+1} . Accordingly, node 1906 is at VO_{t+1} , as indicated by cell 1842 in Table 1802.

Further at the rising edge of ϕ_1 at time $t+1$, the switch 1966 in the second delay module 1930 closes, allowing the capacitor 1968 to charge to the level of the capacitor 1964. Accordingly, the capacitor 1968 charges to VO_t , as indicated by cell 1846 of Table 1802.

In the example of FIG. 19, the first scaling module 1932 scales the value at node 1908 (i.e., the output of the first delay module 1928) by a scaling factor of -0.1. Accordingly, the value present at node 1914 at time $t+1$ is $-0.1 * VO_t$. Similarly, the second scaling module 1934 scales the value present at node 1912 (i.e., the output of the second scaling module 1930) by a scaling factor of -0.8. Accordingly, the value present at node 1916 is $-0.8 * VO_{t-1}$ at time $t+1$.

At time $t+1$, the values at the inputs of the summer 1926 are: VI_t at node 1904, $-0.1 * VO_t$ at node 1914, and $-0.8 * VO_{t-1}$ at node 1916 (in the example of FIG. 19, the values at nodes 1914 and 1916 are summed by a second summer 1925, and this sum is presented to the summer 1926). Accordingly, at time $t+1$, the summer generates a signal equal to $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$.

At the rising edge of ϕ_1 at time $t+1$, a switch 1991 in the output sample and hold module 1936 closes, thereby allowing a capacitor 1992 to charge to VO_{t+1} . Accordingly, the capacitor 1992 charges to VO_{t+1} , which is equal to the sum generated by the adder 1926. As just noted, this value is equal to: $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$. This is indicated in cell 1850 of Table 1802. This value is presented to the optional output smoothing module 1938, which smooths the signal to thereby generate the instance of the output signal VO_{t+1} . It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. 1.

Further details of unified down-conversion and filtering as described in this section are presented in pending U.S. application "Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed October 21, 1998, incorporated herein by reference in its entirety.

6. *Example Application Embodiments of the Invention*

As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

Example applications of the UFT module were described above. In particular, frequency down-conversion, frequency up-conversion, enhanced signal reception, and unified down-conversion

and filtering applications of the UFT module were summarized above, and are further described below. These applications of the UFT module are discussed herein for illustrative purposes. The invention is not limited to these example applications. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s), based on the teachings contained herein.

5 For example, the present invention can be used in applications that involve frequency down-conversion. This is shown in FIG. 1C, for example, where an example UFT module 115 is used in a down-conversion module 114. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal. This is also shown in FIG. 7, for example, where an example UFT module 706 is part of a down-conversion module 704, which is part of a receiver 702.

10 The present invention can be used in applications that involve frequency up-conversion. This is shown in FIG. 1D, for example, where an example UFT module 117 is used in a frequency up-conversion module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal. This is also shown in FIG. 8, for example, where an example UFT module 806 is part of up-conversion module 804, which is part of a transmitter 802.

15 The present invention can be used in environments having one or more transmitters 902 and one or more receivers 906, as illustrated in FIG. 9. In such environments, one or more of the transmitters 902 may be implemented using a UFT module, as shown for example in FIG. 8. Also, one or more of the receivers 906 may be implemented using a UFT module, as shown for example in FIG. 7.

20 The invention can be used to implement a transceiver. An example transceiver 1002 is illustrated in FIG. 10. The transceiver 1002 includes a transmitter 1004 and a receiver 1008. Either the transmitter 1004 or the receiver 1008 can be implemented using a UFT module. Alternatively, the transmitter 1004 can be implemented using a UFT module 1006, and the receiver 1008 can be implemented using a UFT module 1010. This embodiment is shown in FIG. 10.

25 Another transceiver embodiment according to the invention is shown in FIG. 11. In this transceiver 1102, the transmitter 1104 and the receiver 1108 are implemented using a single UFT module 1106. In other words, the transmitter 1104 and the receiver 1108 share a UFT module 1106.

As described elsewhere in this application, the invention is directed to methods and systems for enhanced signal reception (ESR). Various ESR embodiments include an ESR module (transmit) in a transmitter 1202, and an ESR module (receive) in a receiver 1210. An example ESR embodiment configured in this manner is illustrated in FIG. 12.

5 The ESR module (transmit) 1204 includes a frequency up-conversion module 1206. Some embodiments of this frequency up-conversion module 1206 may be implemented using a UFT module, such as that shown in FIG. 1D.

10 The ESR module (receive) 1212 includes a frequency down-conversion module 1214. Some embodiments of this frequency down-conversion module 1214 may be implemented using a UFT module, such as that shown in FIG. 1C.

15 As described elsewhere in this application, the invention is directed to methods and systems for unified down-conversion and filtering (UDF). An example unified down-conversion and filtering module 1302 is illustrated in FIG. 13. The unified down-conversion and filtering module 1302 includes a frequency down-conversion module 1304 and a filtering module 1306. According to the invention, the frequency down-conversion module 1304 and the filtering module 1306 are implemented using a UFT module 1308, as indicated in FIG. 13.

20 Unified down-conversion and filtering according to the invention is useful in applications involving filtering and/or frequency down-conversion. This is depicted, for example, in FIGS. 15A-15F. FIGS. 15A-15C indicate that unified down-conversion and filtering according to the invention is useful in applications where filtering precedes, follows, or both precedes and follows frequency down-conversion. FIG. 15D indicates that a unified down-conversion and filtering module 1524 according to the invention can be utilized as a filter 1522 (i.e., where the extent of frequency down-conversion by the down-converter in the unified down-conversion and filtering module 1524 is minimized). FIG. 15E indicates that a unified down-conversion and filtering module 1528 according to the invention can be utilized as a down-converter 1526 (i.e., where the filter in the unified down-conversion and filtering module 1528 passes substantially all frequencies). FIG. 15F illustrates that the unified down-conversion and filtering module 1532 can be used as an amplifier. It is noted that

one or more UDF modules can be used in applications that involve at least one or more of filtering, frequency translation, and amplification.

For example, receivers, which typically perform filtering, down-conversion, and filtering operations, can be implemented using one or more unified down-conversion and filtering modules.

5 This is illustrated, for example, in FIG. 14.

The methods and systems of unified down-conversion and filtering of the invention have many other applications. For example, as discussed herein, the enhanced signal reception (ESR) module (receive) operates to down-convert a signal containing a plurality of spectrums. The ESR module (receive) also operates to isolate the spectrums in the down-converted signal, where such isolation is implemented via filtering in some embodiments. According to embodiments of the invention, the ESR module (receive) is implemented using one or more unified down-conversion and filtering (UDF) modules. This is illustrated, for example, in FIG. 16. In the example of FIG. 16, one or more of the UDF modules 1610, 1612, 1614 operates to down-convert a received signal. The UDF modules 1610, 1612, 1614 also operate to filter the down-converted signal so as to isolate the spectrum(s) contained therein. As noted above, the UDF modules 1610, 1612, 1614 are implemented using the universal frequency translation (UFT) modules of the invention.

The invention is not limited to the applications of the UFT module described above. For example, and without limitation, subsets of the applications (methods and/or structures) described herein (and others that would be apparent to persons skilled in the relevant art(s) based on the herein teachings) can be associated to form useful combinations.

For example, transmitters and receivers are two applications of the UFT module. FIG. 10 illustrates a transceiver 1002 that is formed by combining these two applications of the UFT module, i.e., by combining a transmitter 1004 with a receiver 1008.

Also, ESR (enhanced signal reception) and unified down-conversion and filtering are two other applications of the UFT module. FIG. 16 illustrates an example where ESR and unified down-conversion and filtering are combined to form a modified enhanced signal reception system.

The invention is not limited to the example applications of the UFT module discussed herein. Also, the invention is not limited to the example combinations of applications of the UFT module discussed herein. These examples were provided for illustrative purposes only, and are not limiting. Other applications and combinations of such applications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion; (4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals.

Additional example applications are described below.

6.1 Data Communication

The invention is directed to data communication among data processing devices. For example, and without limitation, the invention is directed to computer networks such as, for example, local area networks (LANs), wide area networks (WANs), including wireless LANs (WLANs) and wireless WANs, modulator/demodulators (modems), including wireless modems, etc.

FIG. 25 illustrates an example environment 2502 wherein computers 2504, 2512, and 2526 communicate with one another via a computer network 2534. In the example of FIG. 25, computer 2504 is communicating with the network 2534 via a wired link, whereas computers 2512 and 2526 are communicating with the network 2534 via wireless links.

In the teachings contained herein, for illustrative purposes, a link may be designated as being a wired link or a wireless link. Such designations are for example purposes only, and are not limiting. A link designated as being wireless may alternatively be wired. Similarly, a link designated as being wired may alternatively be wireless. This is applicable throughout the entire application.

The computers 2504, 2512 and 2526 each include an interface 2506, 2514, and 2528, respectively, for communicating with the network 2534. The interfaces 2506, 2514, and 2528 include

transmitters 2508, 2516, and 2530 respectively. Also, the interfaces 2506, 2514 and 2528 include receivers 2510, 2518, and 2532 respectively. In embodiments of the invention, the transmitters 2508, 2516 and 2530 are implemented using UFT modules for performing frequency up-conversion operations (see, for example, FIG. 8). In embodiments, the receivers 2510, 2518 and 2532 are implemented using UFT modules for performing frequency down-conversion operations (see, for example, FIG. 7).

As noted above, the computers 2512 and 2526 interact with the network 2534 via wireless links. In embodiments of the invention, the interfaces 2514, 2528 in computers 2512, 2526 represent modulator/demodulators (modems).

In embodiments, the network 2534 includes an interface or modem 2520 for communicating with the modems 2514, 2528 in the computers 2512, 2526. In embodiments, the interface 2520 includes a transmitter 2522, and a receiver 2524. Either or both of the transmitter 2522, and the receiver 2524 are implemented using UFT modules for performing frequency translation operations (see, for example, FIGS. 7 and 8).

In alternative embodiments, one or more of the interfaces 2506, 2514, 2520, and 2528 are implemented using transceivers that employ one or more UFT modules for performing frequency translation operations (see, for example, FIGS. 10 and 11).

FIG. 26 illustrates another example data communication embodiment 2602. Each of a plurality of computers 2604, 2612, 2614 and 2616 includes an interface, such as an interface 2606 shown in the computer 2604. It should be understood that the other computers 2612, 2614, 2616 also include an interface such as an interface 2606. The computers 2604, 2612, 2614 and 2616 communicate with each other via interfaces 2606 and wireless or wired links, thereby collectively representing a data communication network.

The interfaces 2606 may represent any computer interface or port, such as but not limited to a high speed internal interface, a wireless serial port, a wireless PS2 port, a wireless USB port, PCMCIA port, etc.

The interface 2606 includes a transmitter 2608 and a receiver 2610. In embodiments of the invention, either or both of the transmitter 2608 and the receiver 2610 are implemented using UFT modules for frequency up-conversion and down-conversion (see, for example, FIGS. 7 and 8). Alternatively, the interfaces 2806 can be implemented using a transceiver having one or more UFT modules for performing frequency translation operations (see, for example, FIGS. 10 and 11).

FIGS. 33-38 illustrate other scenarios envisioned and encompassed by the invention. FIG. 33 illustrates a data processing environment 3302 wherein a wired network, such as an Ethernet network 3304, is linked to another network, such as a WLAN 3306, via a wireless link 3308. The wireless link 3308 is established via interfaces 3310, 3312 which are preferably implemented using universal frequency translation modules.

The invention includes multiple networks linked together. The invention also envisions wireless networks conforming to any known or custom standard or specification. This is shown in FIG. 34, for example, where any combination of WLANs conforming to any WLAN standard or configuration, such as IEEE 802.11, any cellular telephone standard or specification, any type of radio links, any custom standard or specification, etc., can be implemented using the universal frequency translation technology described herein. Also, any combination of these networks may be coupled together, as illustrated in FIG. 34.

The invention supports WLANs that are located in one or multiple buildings, as shown in FIGS. 35 and 36. The invention also supports WLANs that are located in an area including and external to one or more buildings, as shown in FIG. 37. In fact, the invention is directed to networks that cover any defined geographical area, as shown in FIG. 38. In the embodiments described above, wireless links are preferably established using WLAN interfaces as described herein.

6.1.1. Example Implementations: Interfaces, Wireless Modems, Wireless LANs, etc.

The present invention is now described as implemented in an interface, such as a wireless modem, which can be utilized to implement a wireless local area network (WLAN) or wireless wide area network (WWAN), for example. In an embodiment, the present invention is implemented in a WLAN to support IEEE WLAN Standard 802.11, but this embodiment is mentioned for illustrative purposes only. The invention is not limited to this standard.

Conventional wireless modems are described in, for example, U.S. Patent 5,764,693, titled, "Wireless Radio Modem with Minimal Inter-Device RF Interference," incorporated herein by reference in its entirety. The present invention replaces a substantial portion of conventional wireless modems with one or more universal frequency translators (UFTs). The resultant improved wireless modem consumes less power than conventional wireless modems and is easier and less expensive to design and build. A wireless modem in accordance with the present invention can be implemented in a PC-MCIA card or within a main housing of a computer, for example.

FIG. 27 illustrates an example block diagram of a computer system 2710, which can be wirelessly coupled to a LAN, as illustrated in FIGS. 25 and 26. The computer system 2710 includes an interface 2714 and an antenna 2712. The interface 2714 includes a transmitter module 2716 that receives information from a digital signal processor (DSP) 2720, and modulates and up-converts the information for transmission from the antenna 2712. The interface 2714 also includes a receiver module 2718 that receives modulated carrier signals via the antenna 2712. The receiver module 2718 down-converts and demodulates the modulated carrier signals to baseband information, and provides the baseband information to the DSP 2720. The DSP 2720 can include a central processing unit (CPU) and other components of the computer 2712. Conventionally, the interface 2714 is implemented with heterodyne components.

FIG. 28 illustrates an example interface 2810 implemented with heterodyne components. The interface 2810 includes a transmitter module 2812 and a receiver module 2824. The receiver module 2824 includes an RF section 2830, one or more IF sections 2828, a demodulator section 2826, an optional analog to digital (A/D) converter 2834, and a frequency generator/synthesizer 2832. The transmitter module 2812 includes an optional digital to analog (D/A) converter 2822, a modulator

section 2818, one or more IF sections 2816, an RF section 2814, and a frequency generator/synthesizer 2820. Operation of the interface 2810 will be apparent to one skilled in the relevant art(s), based on the description herein.

FIG. 29 illustrates an example in-phase/quadrature-phase (I/Q) interface 2910 implemented with heterodyne components. I/Q implementations allow two channels of information to be communicated on a carrier signal and thus can be utilized to increase data transmission.

The interface 2910 includes a transmitter module 2912 and a receiver module 2934. The receiver module 2934 includes an RF section 2936, one or more IF sections 2938, an I/Q demodulator section 2940, an optional A/D converter 2944, and a frequency generator/synthesizer 2942. The I/Q demodulator section 2940 includes a signal splitter 2946, mixers 2948, and a phase shifter 2950. The signal splitter 2946 provides a received signal to the mixers 2948. The phase shifter 2950 operates the mixers 2948 ninety degrees out of phase with one another to generate I and Q information channels 2952 and 2954, respectively, which are provided to a DSP 2956 through the optional A/D converter 2944.

The transmitter module 2912 includes an optional D/A converter 2922, an I/Q modulator section 2918, one or more IF sections 2916, an RF section 2914, and a frequency generator/synthesizer 2920. The I/Q modulator section 2918 includes mixers 2924, a phase shifter 2926, and a signal combiner 2928. The phase shifter 2926 operates the mixers 2924 ninety degrees out of phase with one another to generate I and Q modulated information signals 2930 and 2932, respectively, which are combined by the signal combiner 2928. The IF section(s) 2916 and RF section 2914 up-convert the combined I and Q modulated information signals 2930 and 2932 to RF for transmission by the antenna, in a manner well known in the relevant art(s).

Heterodyne implementations, such as those illustrated in FIGS. 28 and 29, are expensive and difficult to design, manufacture and tune. In accordance with the present invention, therefore, the interface 2714 (FIG. 27) is preferably implemented with one or more universal frequency translation (UFT) modules, such as the UFT module 102 (FIG. 1A). Thus previously described benefits of the present invention are obtained in wireless modems, WLANs, etc.

FIG. 30 illustrates an example block diagram embodiment of the interface 2714 that is associated with a computer or any other data processing device. In FIG. 30, the receiver module 2718 includes a universal frequency down-converter (UFD) module 3014 and an optional analog to digital (A/D) converter 3016, which converts an analog output from the UFD 3014 to a digital format for the DSP 2720. The transmitter module 2716 includes an optional modulator 3012 and a universal frequency up-converter (UFU) module 3010. The optional modulator 3012 can be a variety of types of modulators, including conventional modulators. Alternatively, the UFU module 3010 includes modulator functionality. The example implementation of FIG. 30 operates substantially as described above and in co-pending U.S. Patent Applications titled, "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, and "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998.

FIG. 31 illustrates an example implementation of the interface 2714 illustrated in FIG. 30, wherein the receiver UFD 3014 includes a UFT module 3112, and the transmitter UFU 3010 includes a universal frequency translation (UFT) module 3110. This example implementation operates substantially as described above and in co-pending U.S. Patent Applications titled, "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, and "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998.

FIG. 32 illustrates an example I/Q implementation of the interface module 2710. Other I/Q implementations are also contemplated and are within the scope of the present invention.

In the example of FIG. 32, the receiver UFD module 3014 includes a signal divider 3228 that provides a received I/Q modulated carrier signal 3230 between a third UFT module 3224 and a fourth UFT module 3226. A phase shifter 3232, illustrated here as a 90 degree phase shifter, controls the third and fourth UFT modules 3224 and 3226 to operate 90 degrees out of phase with one another. As a result, the third and fourth UFT modules 3224 and 3226 down-convert and demodulate the received I/Q modulated carrier signal 3230, and output I and Q channels 3234 and 3236, respectively, which are provided to the DSP 2720 through the optional A/D converter 3016.

In the example of FIG. 32, the transmitter UFU module 3010 includes first and second UFT modules 3212 and 3214 and a phase shifter 3210, which is illustrated here as a 90 degree phase shifter. The phase shifter 3210 receives a lower frequency modulated carrier signal 3238 from the modulator 3012. The phase shifter 3210 controls the first and second UFT modules 3212 and 3214 to operate 90 degrees out of phase with one another. The first and second UFT modules 3212 and 3214 up-convert the lower frequency modulated carrier signal 3238, which are output as higher frequency modulated I and Q carrier channels 3218 and 3220, respectively. A signal combiner 3216 combines the higher frequency modulated I and Q carrier channels 3218 and 3220 into a single higher frequency modulated I/Q carrier signal 3222 for transmitting by the antenna 2712.

The example implementations of the interfaces described above, and variations thereof, can also be used to implement network interfaces, such as the network interface 2520 illustrated in FIG. 25.

6.1.2. Example Modifications

The RF modem applications, WLAN applications, etc., described herein, can be modified by incorporating one or more of the enhanced signal reception (ESR) techniques described herein. Use of ESR embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The RF modem applications, WLAN applications, etc., described herein can be enhanced by incorporating one or more of the unified down-conversion and filtering (UDF) techniques described herein. Use of UDF embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.2. Other Example Applications

The application embodiments described above are provided for purposes of illustration. These applications and embodiments are not intended to limit the invention. Alternate and additional applications and embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, such alternate and additional applications and embodiments include combinations of those described above. Such combinations will be apparent to persons skilled in the relevant art(s) based on the herein teachings.

6.3. *Example WLAN Implementation Embodiments*

6.3.1. *Architecture*

FIG. 39 is a block diagram of a WLAN interface 3902 (also referred to as a WLAN modem herein) according to an embodiment of the invention. The WLAN interface/modem 3902 includes an antenna 3904, a low noise amplifier or power amplifier (LNA/PA) 3904, a receiver 3906, a transmitter 3910, a control signal generator 3908, a demodulator/modulator facilitation module 3912, and a media access controller (MAC) interface 3914. The MAC interface 3914 couples the WLAN interface/modem 3902 to a computer 3916 or other data processing device. The computer 3916 preferably includes a MAC 3918.

The WLAN interface/modem 3902 represents a transmit and receive application that utilizes the universal frequency translation technology described herein. It also represents a zero IF (or direct-to-data) WLAN architecture.

The WLAN interface/modem 3902 also represents a vector modulator and a vector demodulator using the universal frequency translation (UFT) technology described herein. Use of the UFT technology enhances the flexibility of the WLAN application (i.e., makes it universal).

In the embodiment shown in FIG. 39, the WLAN interface/modem 3902 is compliant with WLAN standard IEEE 802.11. However, the invention is not limited to this standard. The invention

is applicable to any communication standard or specification, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein. Any modifications to the invention to operate with other standards or specifications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

5 In the embodiment shown in FIG. 39, the WLAN interface/modem 3902 provides half duplex communication. However, the invention is not limited to this communication mode. The invention is applicable and directed to other communication modes, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

10 In the embodiment shown in FIG. 39, the modulation/demodulation performed by the WLAN interface/modem 3902 is preferably direct sequence spread spectrum QPSK (quadrature phase shift keying) with differential encoding. However, the invention is not limited to this modulation/demodulation mode. The invention is applicable and directed to other modulation and demodulation modes, such as but not limited to those described herein, as well as frequency hopping according to IEEE 802.11, OFDM (orthogonal frequency division multiplexing), as well as others.
15 These modulation/demodulation modes will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

The operation of the WLAN interface/modem 3902 when receiving shall now be described.

20 Signals 3922 received by the antenna 3904 are amplified by the LNA/PA 3904. The amplified signals 3924 are down-converted and demodulated by the receiver 3906. The receiver 3906 outputs I signal 3926 and Q signal 3928.

25 FIG. 40 illustrates an example receiver 3906 according to an embodiment of the invention. It is noted that the receiver 3906 shown in FIG. 40 represents a vector modulator. The "receiving" function performed by the WLAN interface/modem 3902 can be considered to be all processing performed by the WLAN interface/modem 3902 from the LNA/PA 3904 to generation of baseband information.

Signal 3924 is split by a 90 degree splitter 4001 to produce an I signal 4006A and Q signal 4006B that are preferably 90 degrees apart in phase. I and Q signals 4006A, 4006B are down-

converted by UFD (universal frequency down-conversion) modules 4002A, 4002B. The UDF modules 4002A, 4002B output down-converted I and Q signals 3926, 3928. The UFD modules 4002A, 4002B each includes at least one UFT (universal frequency translation) module 4004A. UFD and UFT modules are described above.

5 The demodulator/modulator facilitation module 3912 receives the I and Q signals 3926, 3928. The demodulator/modulator facilitation module 3912 amplifies and filters the I and Q signals 3926, 3928. The demodulator/modulator facilitation module 3912 also performs automatic gain control (AGC) functions. The AGC function is coupled with the universal frequency translation technology described herein. The demodulator/modulator facilitation module 3912 outputs processed I and Q
10 signals 3930, 3932.

 The MAC interface 3914 receives the processed I and Q signals 3930, 3932. The MAC interface 3914 preferably includes a baseband processor. The MAC interface 3914 preferably performs functions such as combining the I and Q signals 3930, 3932, and arranging the data according to the protocol/file format being used. Other functions performed by the MAC interface
15 3914 and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The MAC interface 3914 outputs the baseband information signal, which is received and processed by the computer 3916 in an implementation and application specific manner.

 In the example embodiment of FIG. 39, the demodulation function is distributed among the
20 receiver 3906, the demodulator/modulator facilitation module 3912, and a baseband processor contained in the MAC interface 3914. The functions collectively performed by these components include, but are not limited to, despread the information, differentially decoding the information, tracking the carrier phase, descrambling, recreating the data clock, and combining the I and Q signals. The invention is not limited to this arrangement. These demodulation-type functions can be
25 centralized in a single component, or distributed in other ways.

 The operation of the WLAN interface/modem 3902 when transmitting shall now be described.

A baseband information signal 3936 is received by the MAC interface 3914 from the computer 3916. The MAC interface 3914 preferably performs functions such as splitting the baseband information signal to form I and Q signals 3930, 3932, and arranging the data according to the protocol/file format being used. Other functions performed by the MAC interface 3914 and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The demodulator/modulator facilitation module 3912 filters and amplifies the I and Q signals 3930, 3932. The demodulator/modulator facilitation module 3912 outputs processed I and Q signals 3942, 3944. Preferably, at least some filtering and/or amplifying components in the demodulator/modulator facilitation module 3912 are used for both the transmit and receive paths.

The transmitter 3910 up-converts the processed I and Q signals 3942, 3944, and combines the up-converted I and Q signals. This up-converted/combined signal is amplified by the LNA/PA 3904, and then transmitted via the antenna 3904.

FIG. 41 illustrates an example transmitter 3910 according to an embodiment of the invention. The device in FIG. 41 can also be called a vector modulator. The "transmit" function performed by the WLAN interface/modem 3902 can be considered to be all processing performed by the WLAN interface/modem 3902 from receipt of baseband information through the LNA/PA 3904.

I and Q signals 3942, 3944 are received by UFU (universal frequency up-conversion) modules 4102A, 4102B. The UFU modules 4102A, 4102B each includes at least one UFT module 4104A, 4104B. The UFU modules 4102A, 4102B up-convert I and Q signals 3942, 3944. The UFU modules 4102A, 4102B output up-converted I and Q signals 4106, 4108. The 90 degree combiner 4110 effectively phase shifts either the I signal 4106 or the Q signal 4108 by 90 degrees, and then combines the phase shifted signal with the unshifted signal to generate a combined, up-converted I/Q signal 3946.

In the example embodiment of FIG. 39, the modulation function is distributed among the transmitter 3910, the demodulator/modulator facilitation module 3912, and a baseband processor contained in the MAC interface 3914. The functions collectively performed by these components

include, but are not limited to, differentially encoding data, splitting the baseband information signal into I and Q signals, scrambling data, and data spreading. The invention is not limited to this arrangement. These modulation-type functions can be centralized in a single component, or distributed in other ways.

5 The components in the WLAN interface/modem 3902 are preferably controlled by the MAC interface 3914 in operation with the MAC 3918 in the computer 3916. This is represented by the distributed control arrow 3940 in FIG. 39. Such control includes setting the frequency, data rate, whether receiving or transmitting, and other communication characteristics/modes that will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

10 FIG. 42 illustrates an example implementation of the WLAN interface/modem 3902. It is noted that in this implementation example, the MAC interface 3914 is located on a different board. FIG. 62 is an example motherboard corresponding to FIG. 42. FIG. 63 is an example bill-of-materials (BOM) list for the motherboard of FIG. 62. This and other implementations are provided herein for example purposes only. Other implementations will be apparent to persons skilled in the relevant art(s), and the invention is directed to such other implementations.

15 FIG. 102 illustrates an alternate example PCMCIA test bed assembly for a WLAN interface/modem 3902 according to an embodiment of the invention. In this embodiment, the baseband processor 10202 is separate from the MAC interface 3914.

20 In some applications, it is desired to separate the receive path and the transmit path. FIG. 43 illustrates an example receive implementation, and FIG. 44 illustrates an example transmit implementation.

6.3.2. Receiver

 An example implementation of the receiver 3906 (vector demodulator) is shown in FIG. 53. An example BOM list for the receiver 3906 of FIG. 53 is shown in FIG. 54.

6.3.3. Transmitter

An example implementation of the transmitter 3910 (vector modulator) is shown in FIGS. 57-60. The data conditioning interfaces 5802 in FIG. 58 effectively pre-process the I and Q signals 3942, 3944 before being received by the UFU modules 4102. An example BOM list for the transmitter 3910 of FIGS. 57-60 is shown in FIGS. 61A and 61B.

6.3.4. Demodulator/Modulator Facilitation Module

An example demodulator/modulator facilitation module 3912 is shown in FIGS. 47 and 48. A corresponding BOM list is shown in FIGS. 49A and 49B.

An alternate example demodulator/modulator facilitation module 3912 is shown in FIGS. 50 and 51. A corresponding BOM list is shown in FIGS. 52A and 52B.

6.3.5. MAC Interface

An example MAC interface 3914 is shown in FIG. 45. A corresponding BOM list is shown in FIGS. 46A and 46B.

6.3.6. Control Signal Generator - Synthesizer

In an embodiment, the control signal generator 3908 is preferably implemented using a synthesizer. An example synthesizer is shown in FIG. 55. A corresponding BOM list is shown in FIGS. 56A and 56B.

6.3.7. LNA/PA

An example LNA/PA 3904 is shown in FIGS. 64 and 65. A corresponding BOM list is shown in FIG. 66.

6.3.8. Test Results

Test results relating to the operation of the WLAN interface/modem 3902 are shown in FIGS. 67-94. FIGS. 95-100 relate to IIP2 and IIP3, and FIG. 101 relates to power consumption.

7. Conclusions

Example implementations of the systems and components of the invention have been described herein. As noted elsewhere, these example implementations have been described for illustrative purposes only, and are not limiting. Other implementation embodiments are possible and covered by the invention, such as but not limited to software and software/hardware implementations of the systems and components of the invention. Such implementation embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

While various application embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What Is Claimed Is:

1. A wireless modem apparatus, comprising:
a universal frequency up-converter(UFU) module; and
a universal frequency down-converter (UFD) module.
2. The apparatus according to claim 1, wherein said UFU module comprises a first universal frequency translation (UFT) module.
3. The apparatus according to claim 2, wherein said UFU module further comprises a second UFT module, wherein said first and second UFT modules are configured to modulate and up-convert information signals to in-phase and quadrature-phase channels.
4. The apparatus according to claim 1, wherein said UFD comprises a third universal frequency translation (UFT) module.
5. The apparatus according to claim 4, wherein said UFD further comprises a fourth UFT module, wherein said third and fourth UFT modules are configured to down-convert and demodulate in-phase and quadrature-phase components of a received signal.
6. A computer apparatus, comprising:
an antenna;
a data processing device; and
a wireless interface coupled between said antenna and said data processing device, said wireless interface including;
a universal frequency up-converter(UFU) module, and
a universal frequency down-converter (UFD) module.

- 1 7. The apparatus according to claim 6, wherein said UFU module comprises a first universal
2 frequency translation (UFT) module.
- 1 8. The apparatus according to claim 7, wherein said UFU module further comprises a second
2 UFT module, wherein said first and second UFT modules are configured to modulate and up-
3 convert information signals to in-phase and quadrature-phase channels.
- 1 9. The apparatus according to claim 6, wherein said UFD comprises a third universal frequency
2 translation (UFT) module.
- 1 10. The apparatus according to claim 9, wherein said UFD further comprises a fourth UFT
2 module, wherein said third and fourth UFT modules are configured to down-convert and
3 demodulate in-phase and quadrature-phase components of a received signal.

Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology

Abstract

Frequency translation and applications of same are described herein, including RF modem and wireless local area access (WLAN) applications. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

C:\Work\Matters\1744\Trip\WLAN application\17440630000.app

080499

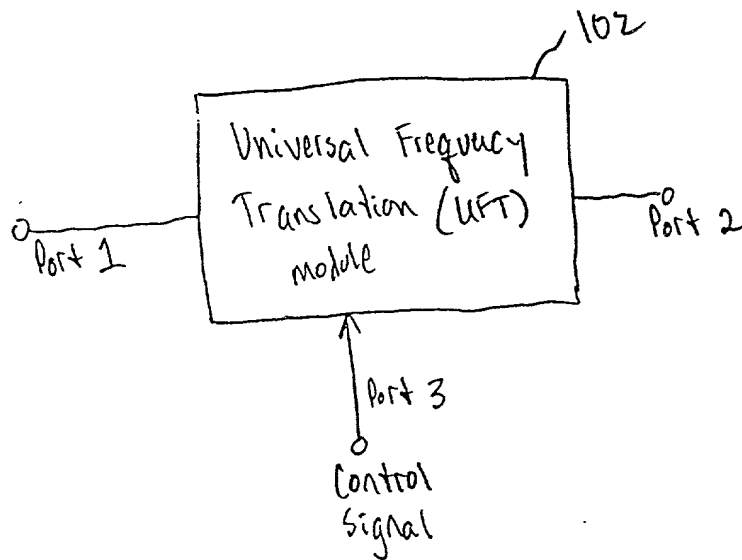


FIG. 1A

FIG. 1B

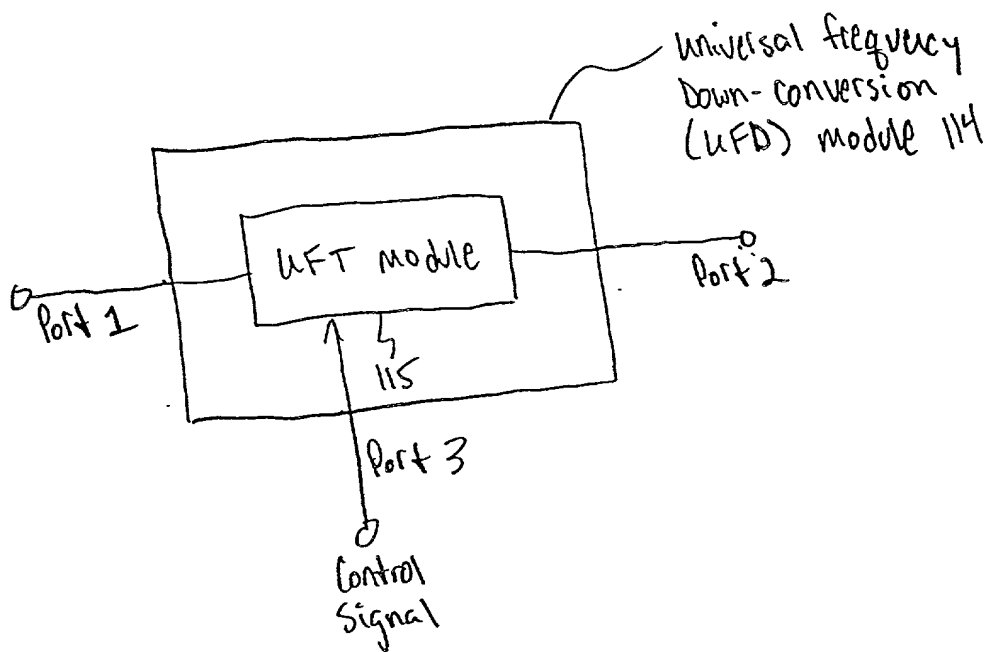


FIG. 1C

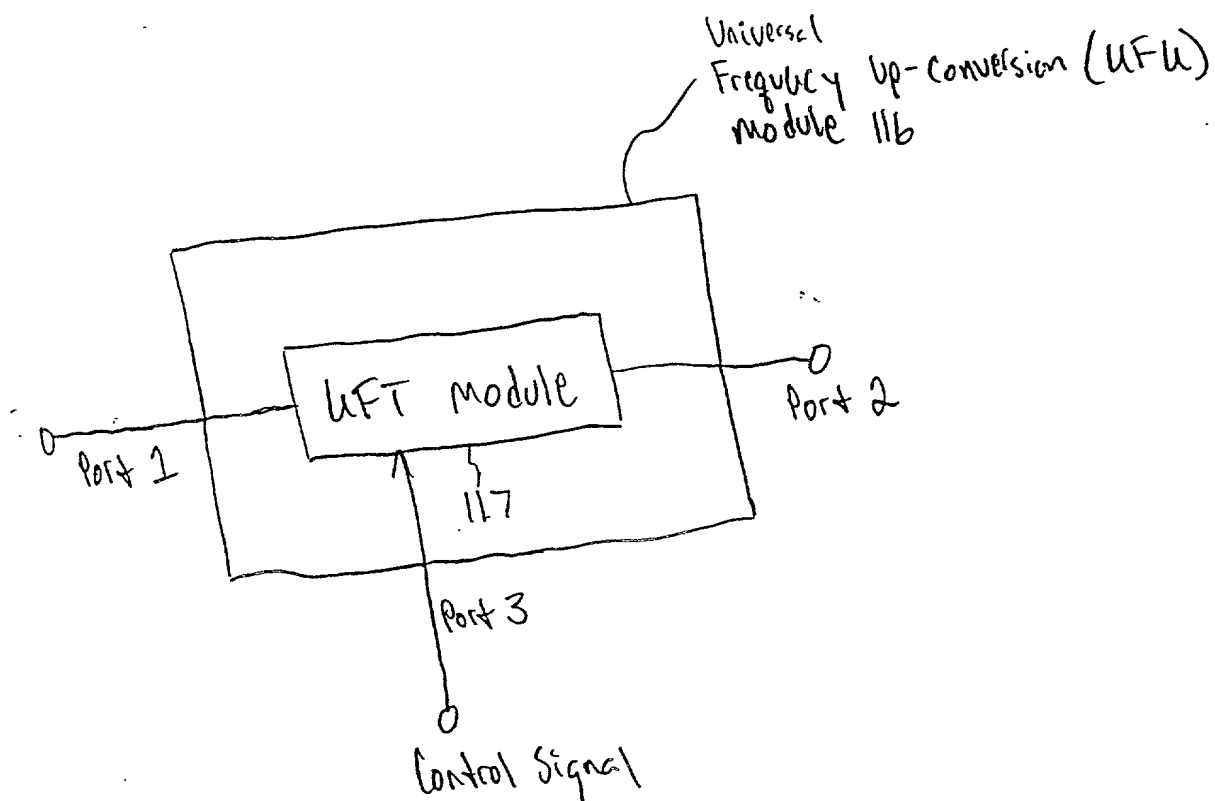


FIG. 1D

Control Signal

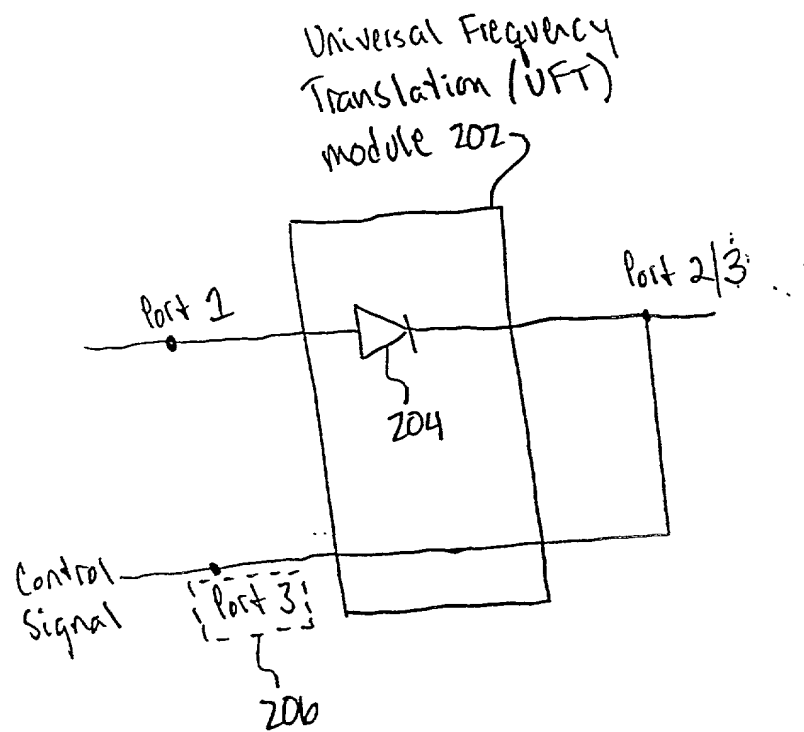


FIG. 2

Universal Frequency
Up-Conversion (UFU) module 300

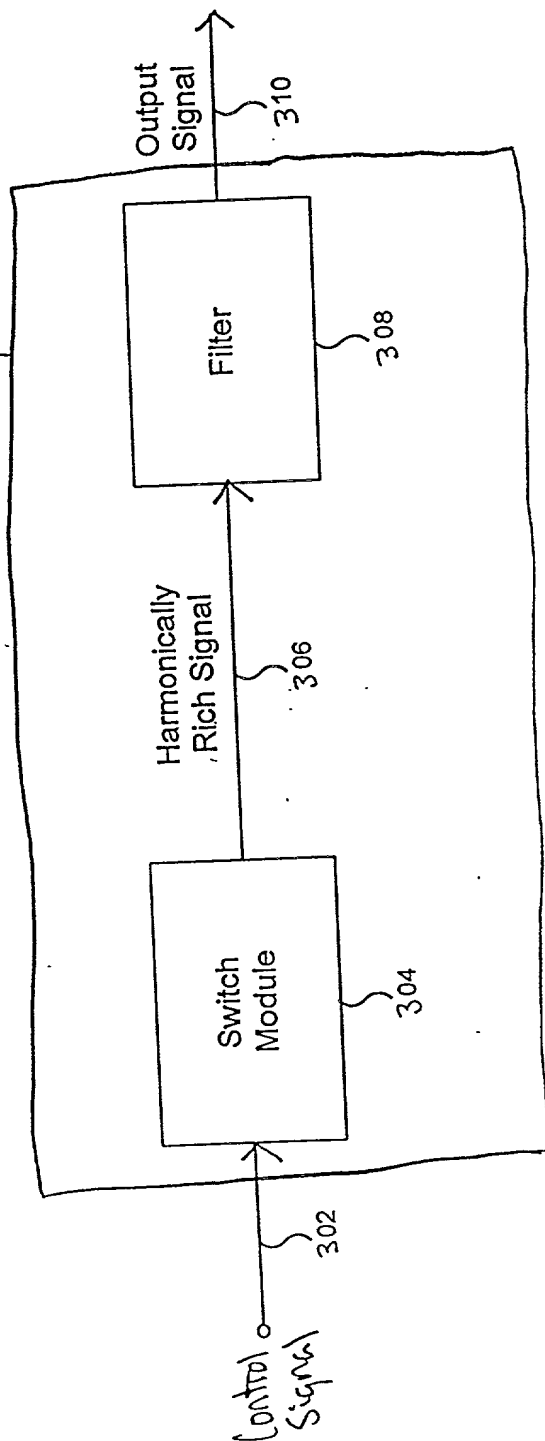


FIG. 3

Universal Frequency
Up-Conversion (UFC) module 401

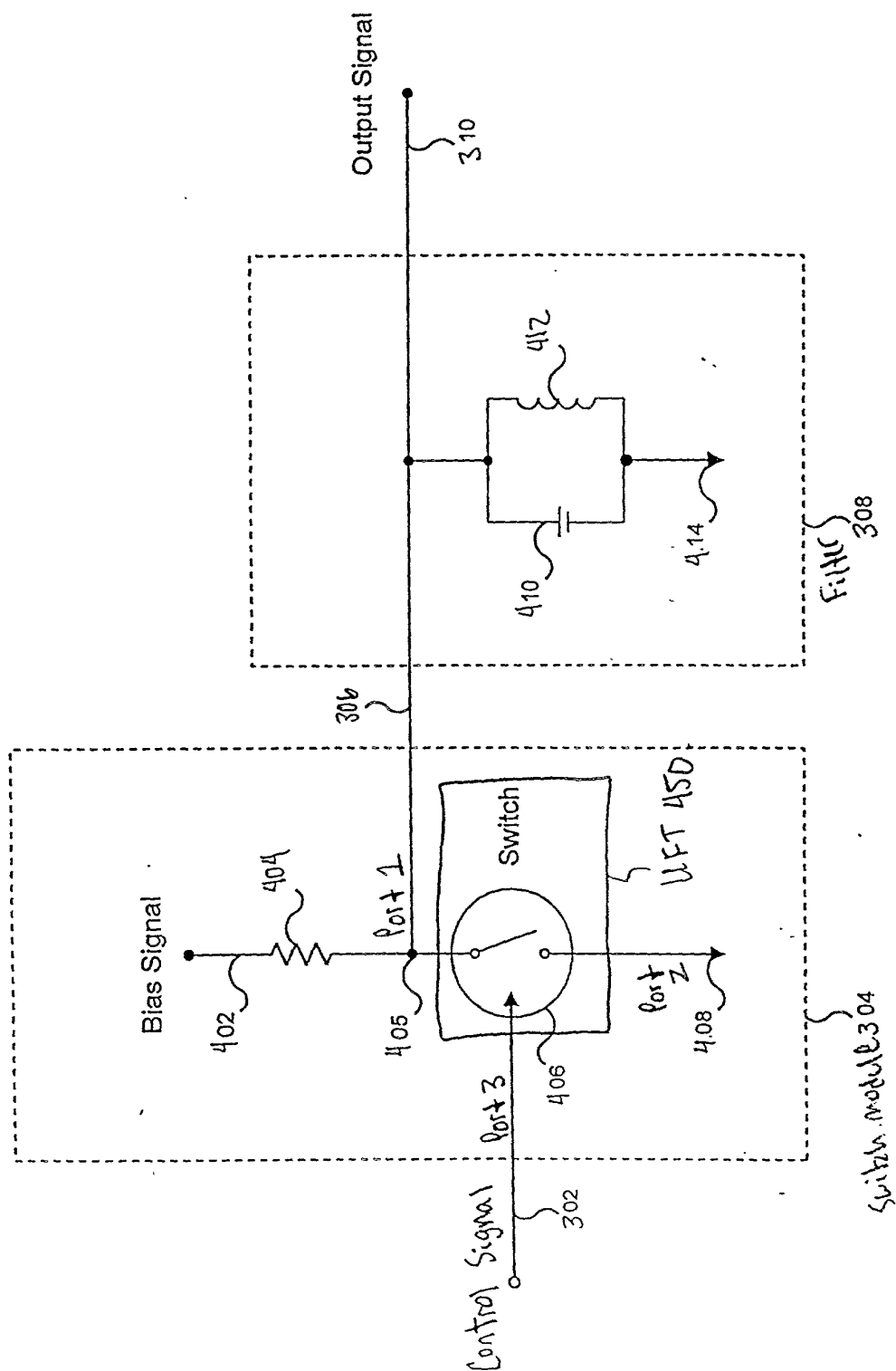


FIG. 4

Universal Frequency
 up-conversion
 (UFU) module 590

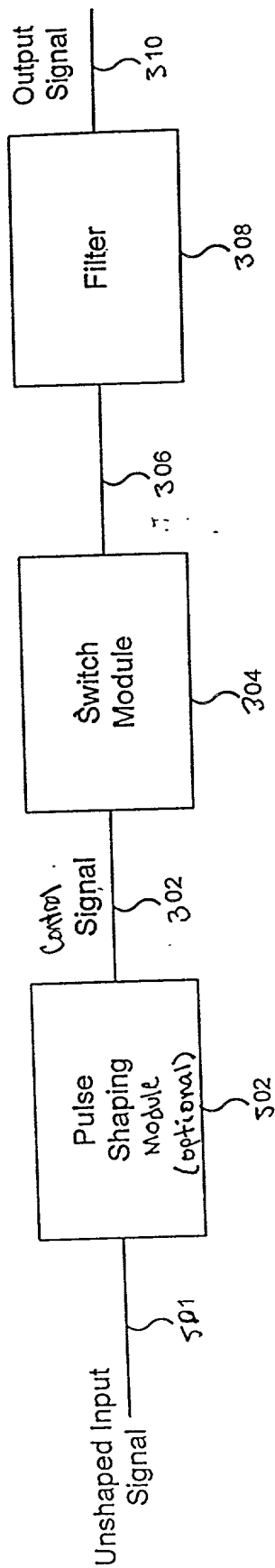


FIG. 5

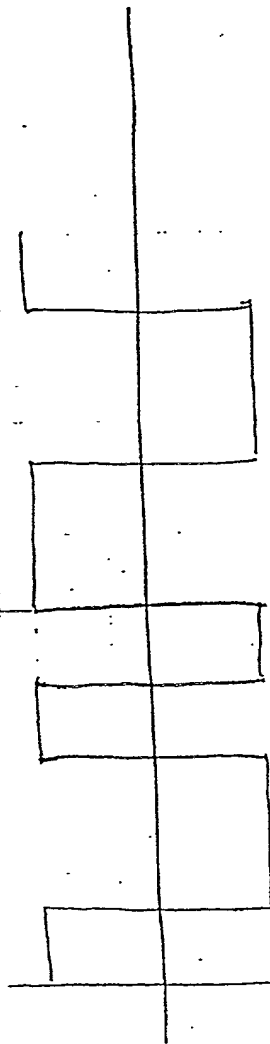


Fig. 6A

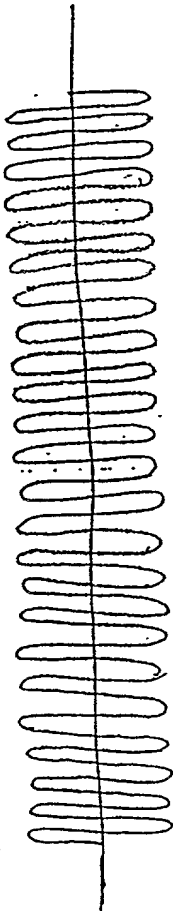


Fig: 18

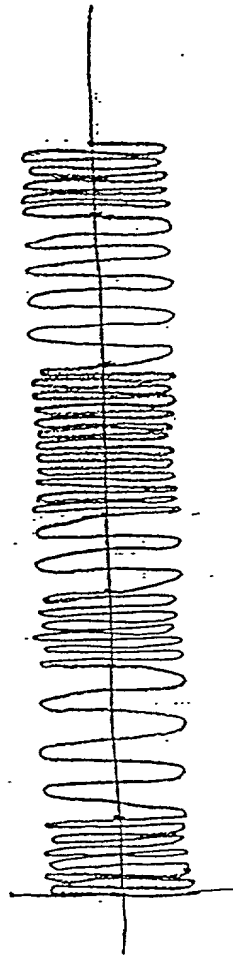


FIG. 6C



File 60

2017.11.11

Fig. 6

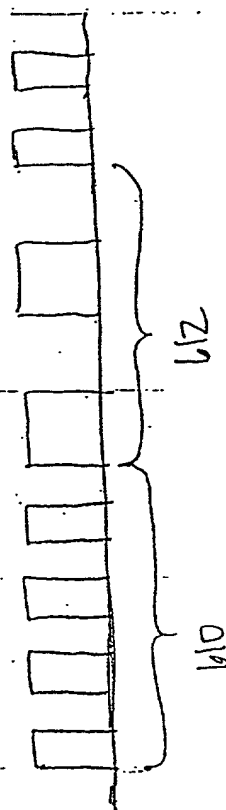
INFORMATION
SIGNAL
602

OSCILLATING
SIGNAL
6.04

FREQUENCY MODULATED
INPUT SIGNAL

804
HARMONICALLY
RICH SIGNAL
(SHOWN AS SQUARE WAVE)

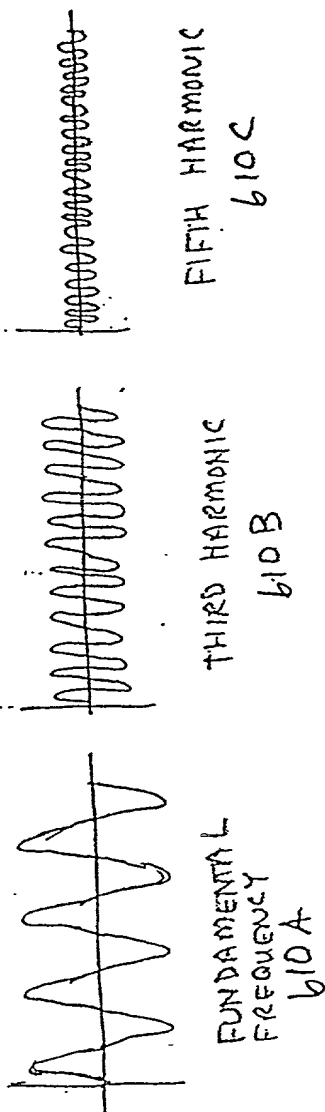
EXPANDED VIEW OF
HARMONICALLY RICH
SIGNAL 608



12
13
14
15
16
17
18

99
100
101
102

HARMONICS OF
SIGNAL 610
(SHOWN SEPARATELY)



HARMONICS OF
SIGNAL $u(t)$
(SHOWN SEPARATELY)

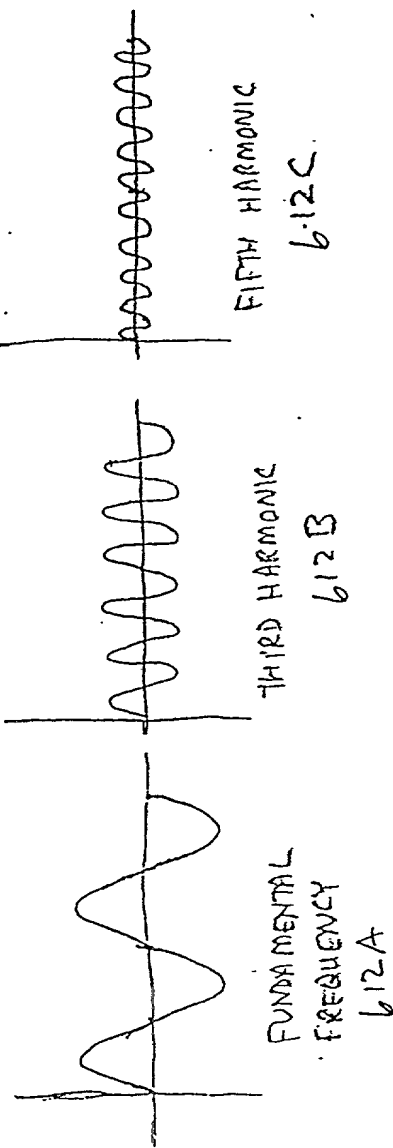
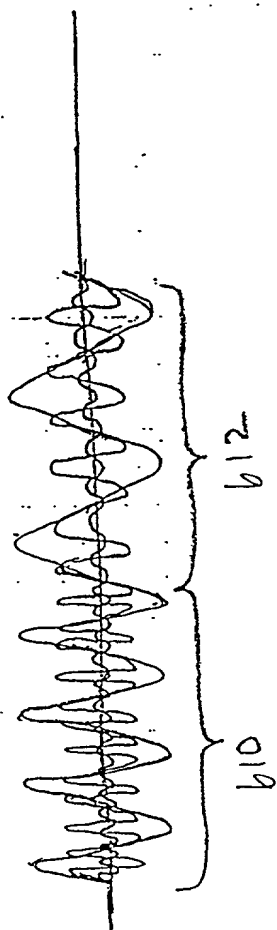


FIG. 6 (cont)

HARMONICS OF
SIGNALS SAID AND:
612 (SHOWN
SIMULTANEOUSLY BUT
NOT SUMMED)



第 5 頁

Page 68 of 177

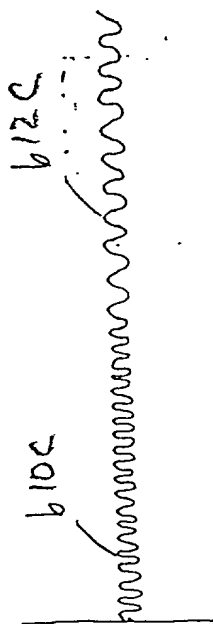


Fig. 6T

FIG-6 (cont)

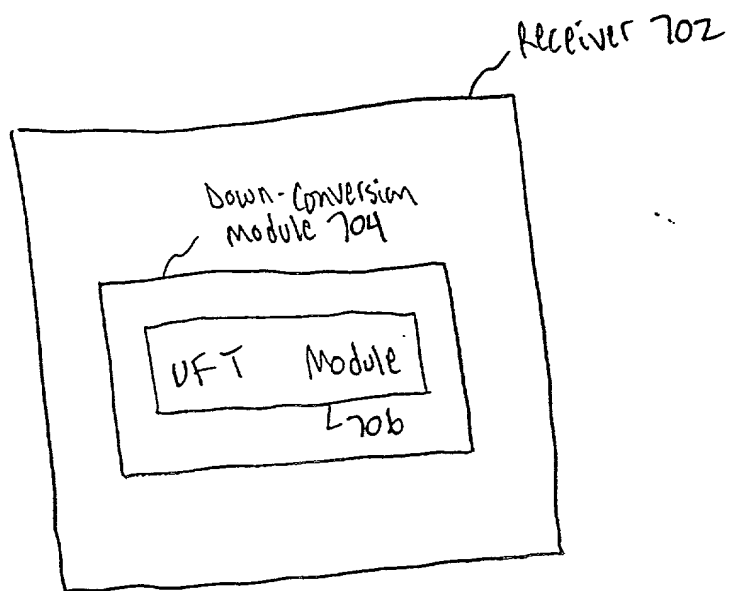


FIG. 7

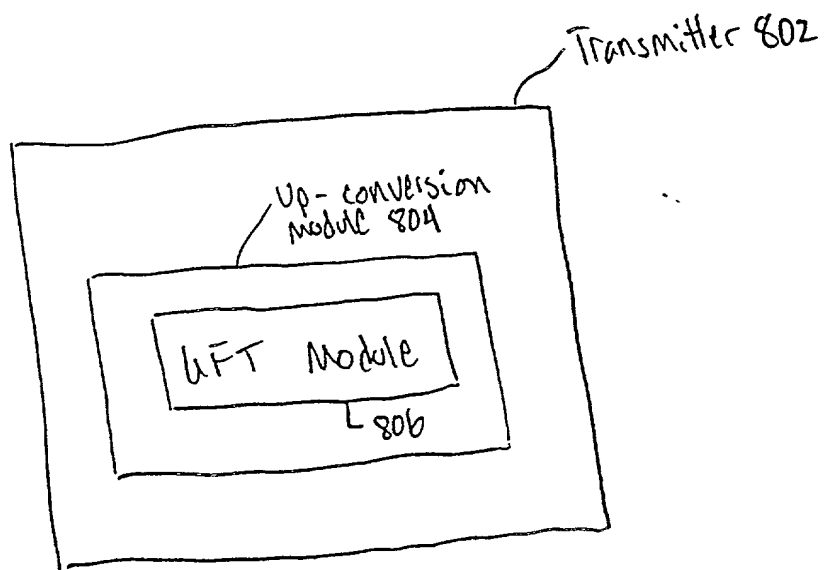


FIG. 8

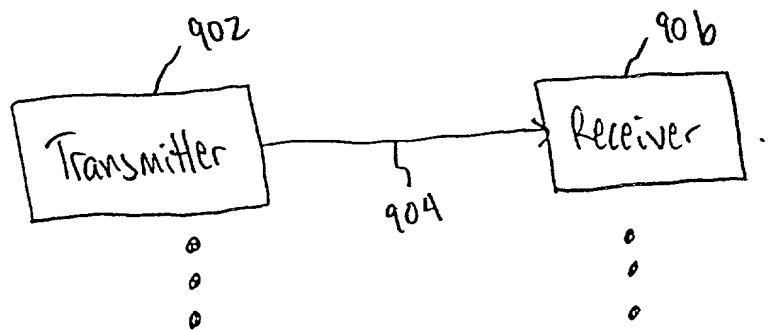
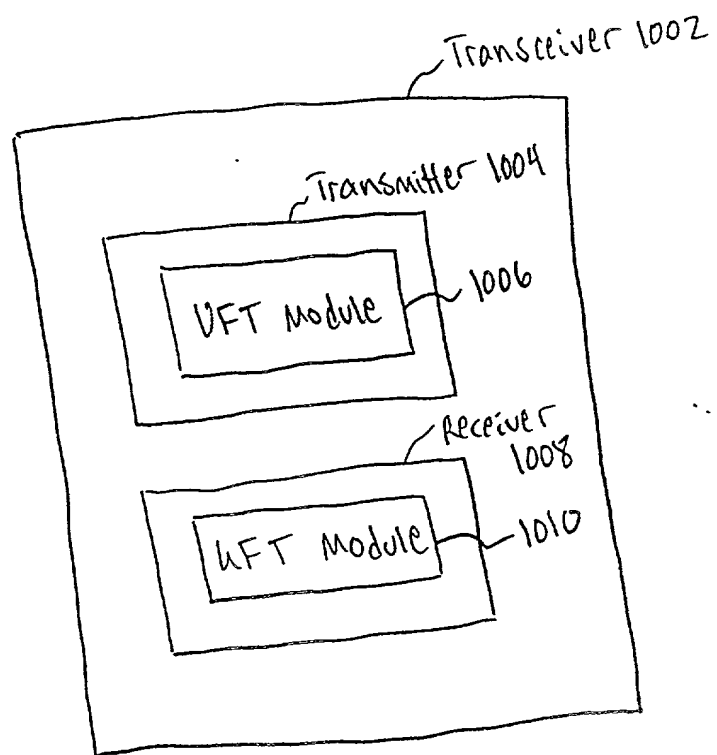


FIG. 9



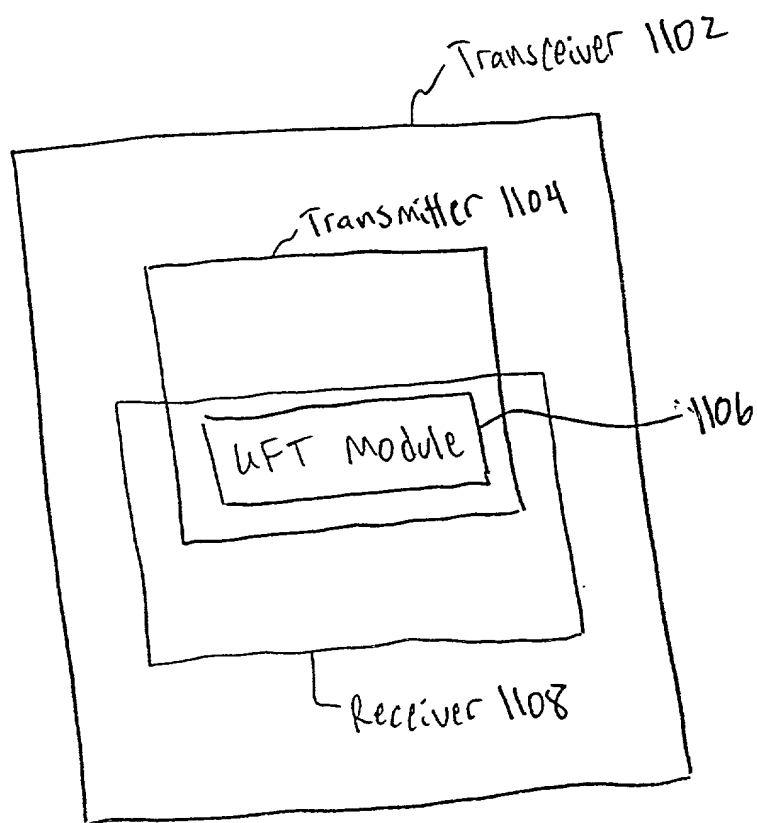


FIG. 11

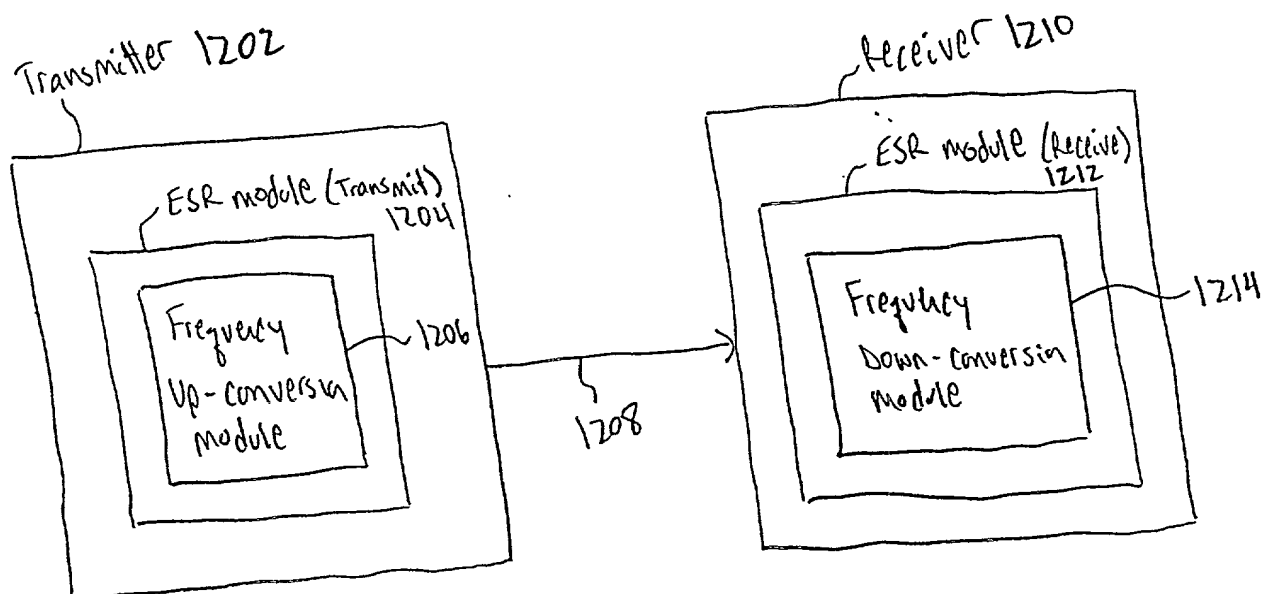


FIG. 12

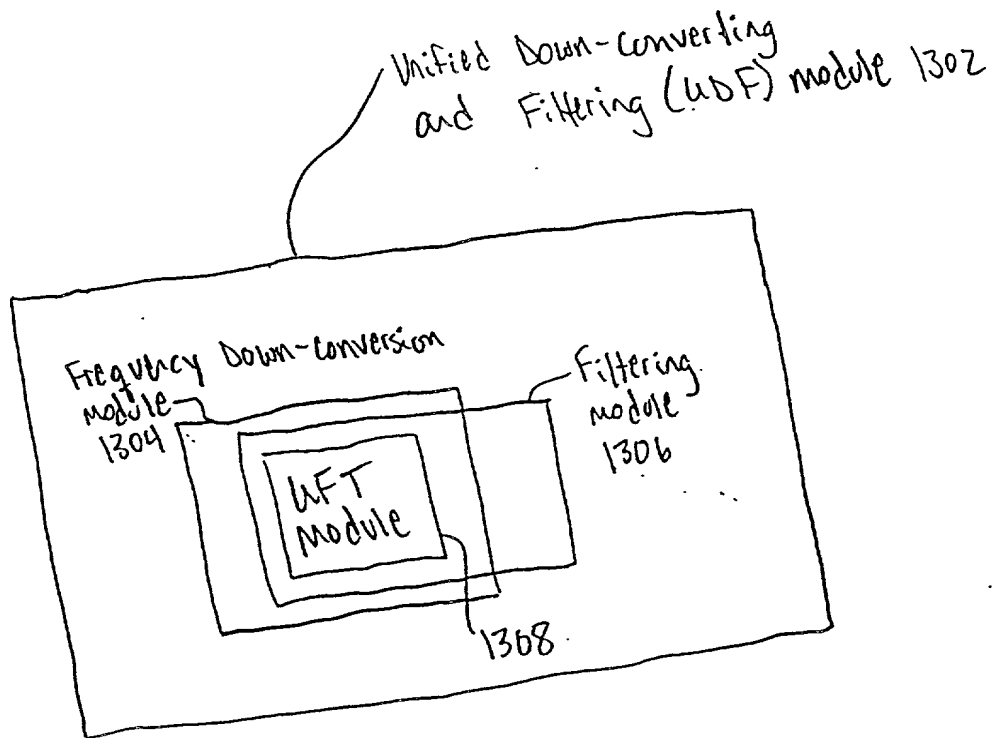


FIG. 13

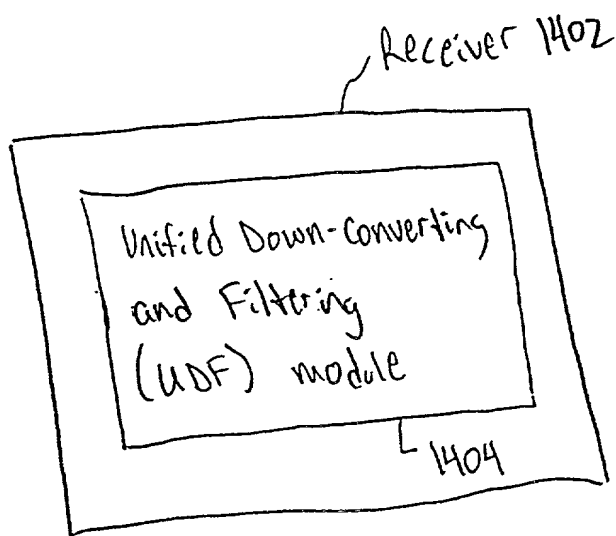


FIG. 14

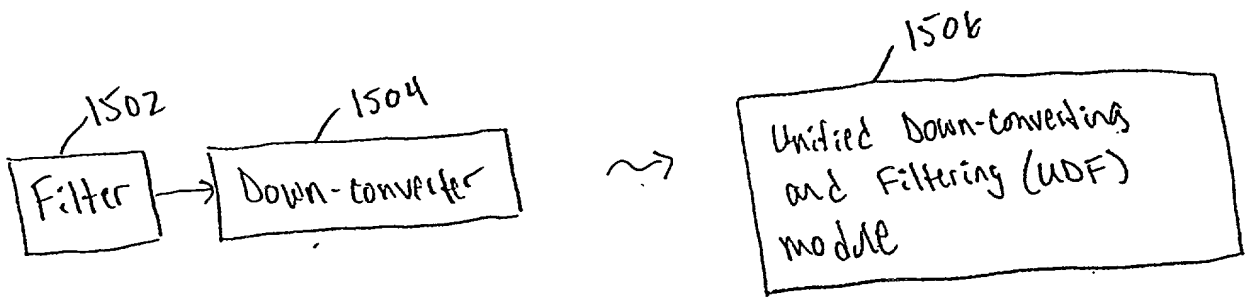


FIG. 15A

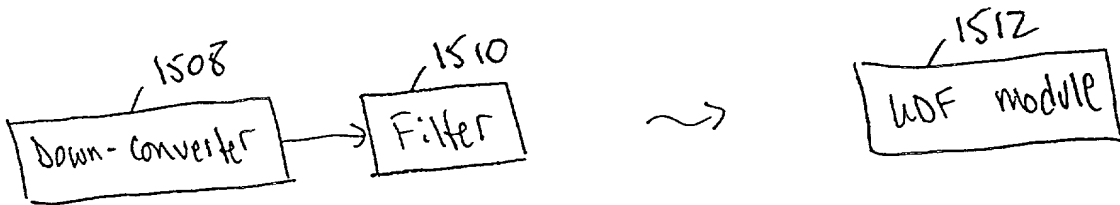


FIG. 15B

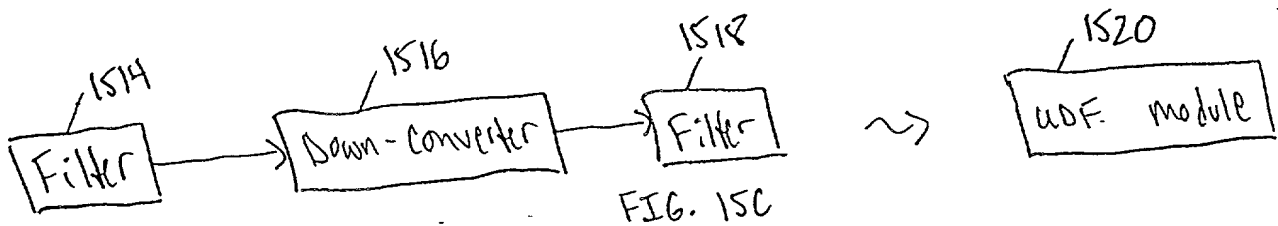


FIG. 15C

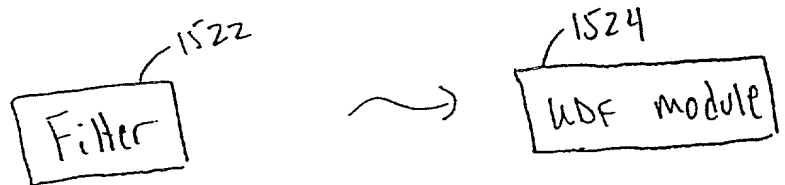


FIG. 15D



FIG. 15E

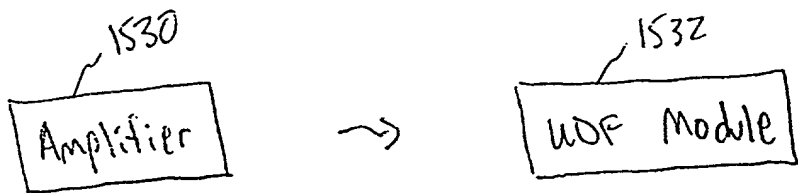


FIG. 15F

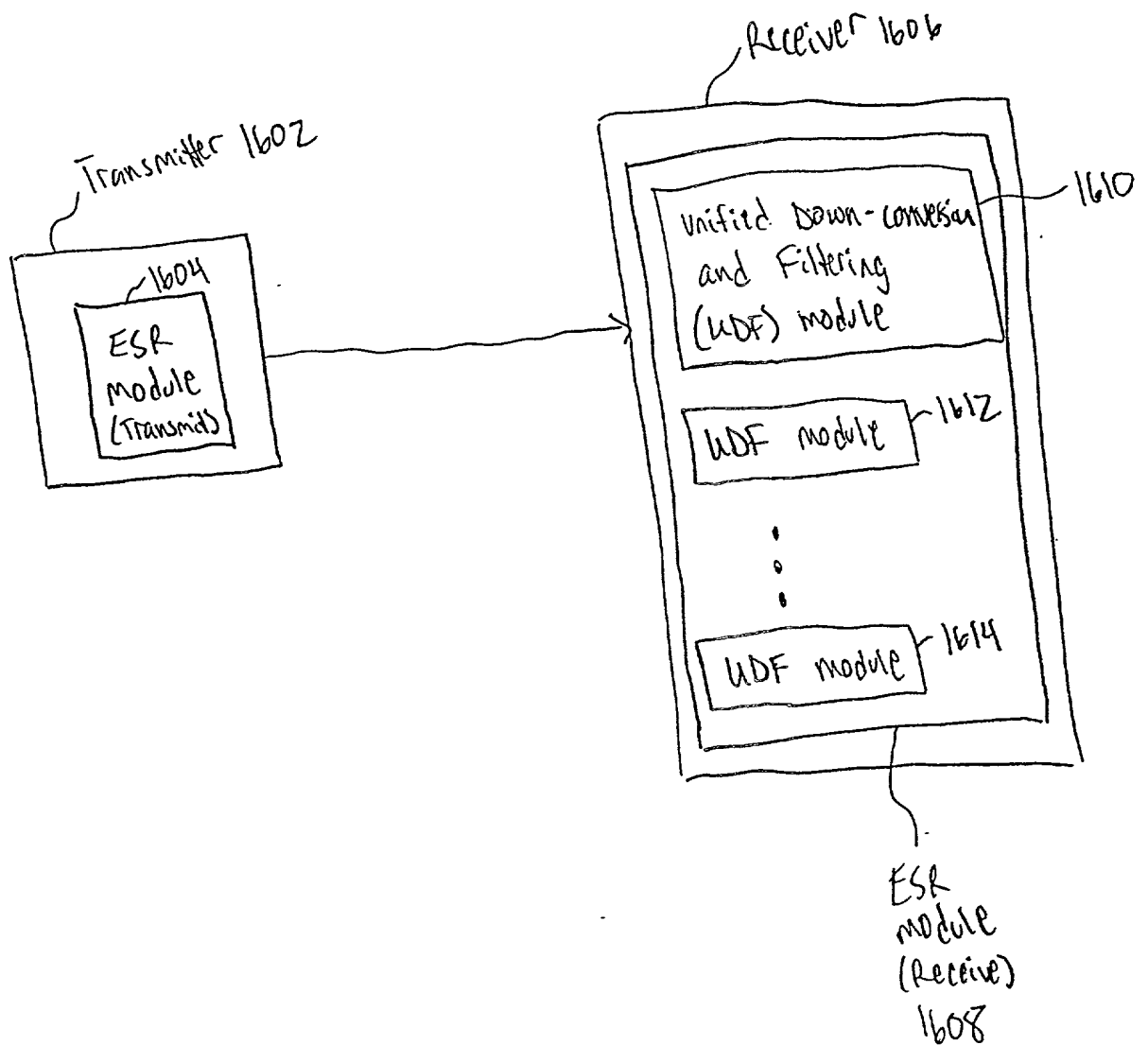


FIG. 16

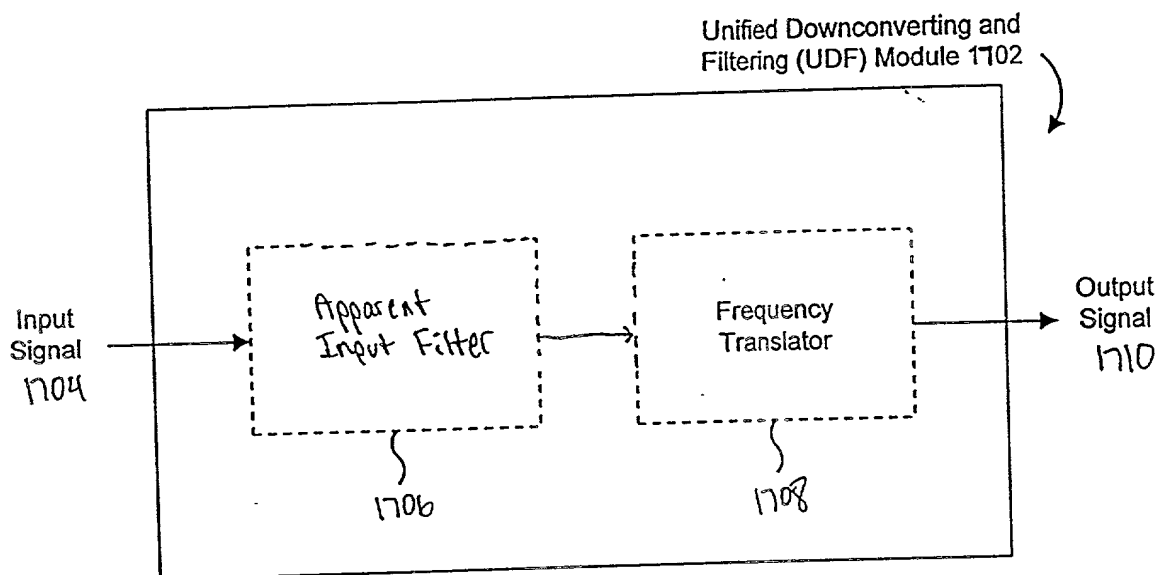
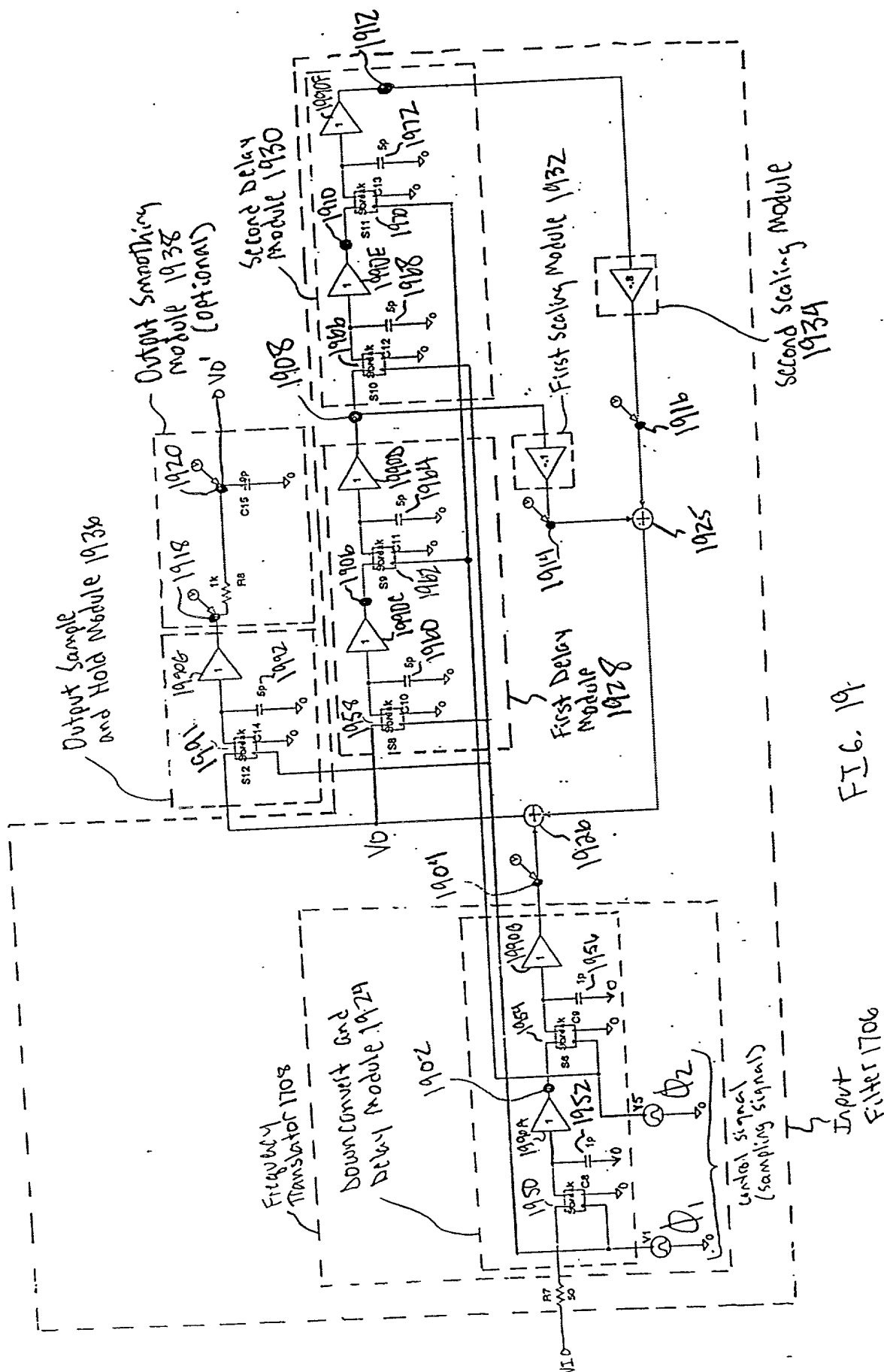


FIG. 17

1802

Time Node	t-1 (rising edge of ϕ_1)	t-1 (rising edge of ϕ_2)	t (rising edge of ϕ_1)	t (rising edge of ϕ_2)	t+1 (rising edge of ϕ_1)
1902	VI_{t-1} 1804	VI_{t-1} 1808	VI_t 1816	VI_t 1826	VI_{t+1} 1838
1904	—	VI_{t-1} 1810	VI_{t-1} 1818	VI_t 1828	VI_t 1840
1906	VO_{t-1} 1806	VO_{t-1} 1812	VO_t 1820	VO_t 1830	VO_{t+1} 1842
1908	—	VO_{t-1} 1814	VO_{t-1} 1822	VO_t 1832	VO_t 1844
1910	— 1807	—	VO_{t-1} 1824	VO_{t-1} 1834	VO_t 1846
1912	—	— 1815	—	VO_{t-1} 1836	VO_{t-1} 1848
1918	—	—	—	—	VI_t 1850 0.1 * VO_t 0.8 * VO_{t-1}

FIG. 18



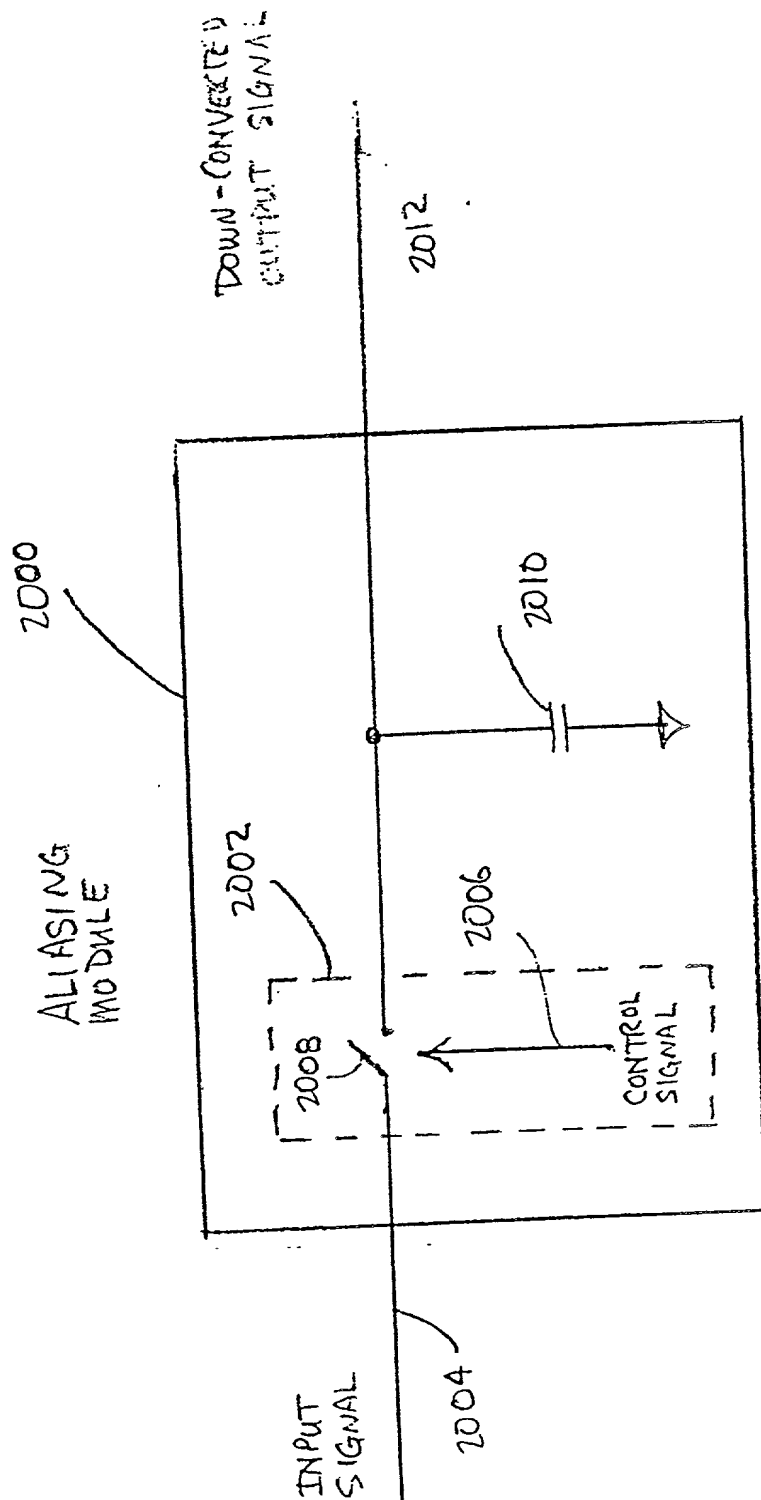


FIG. 20A

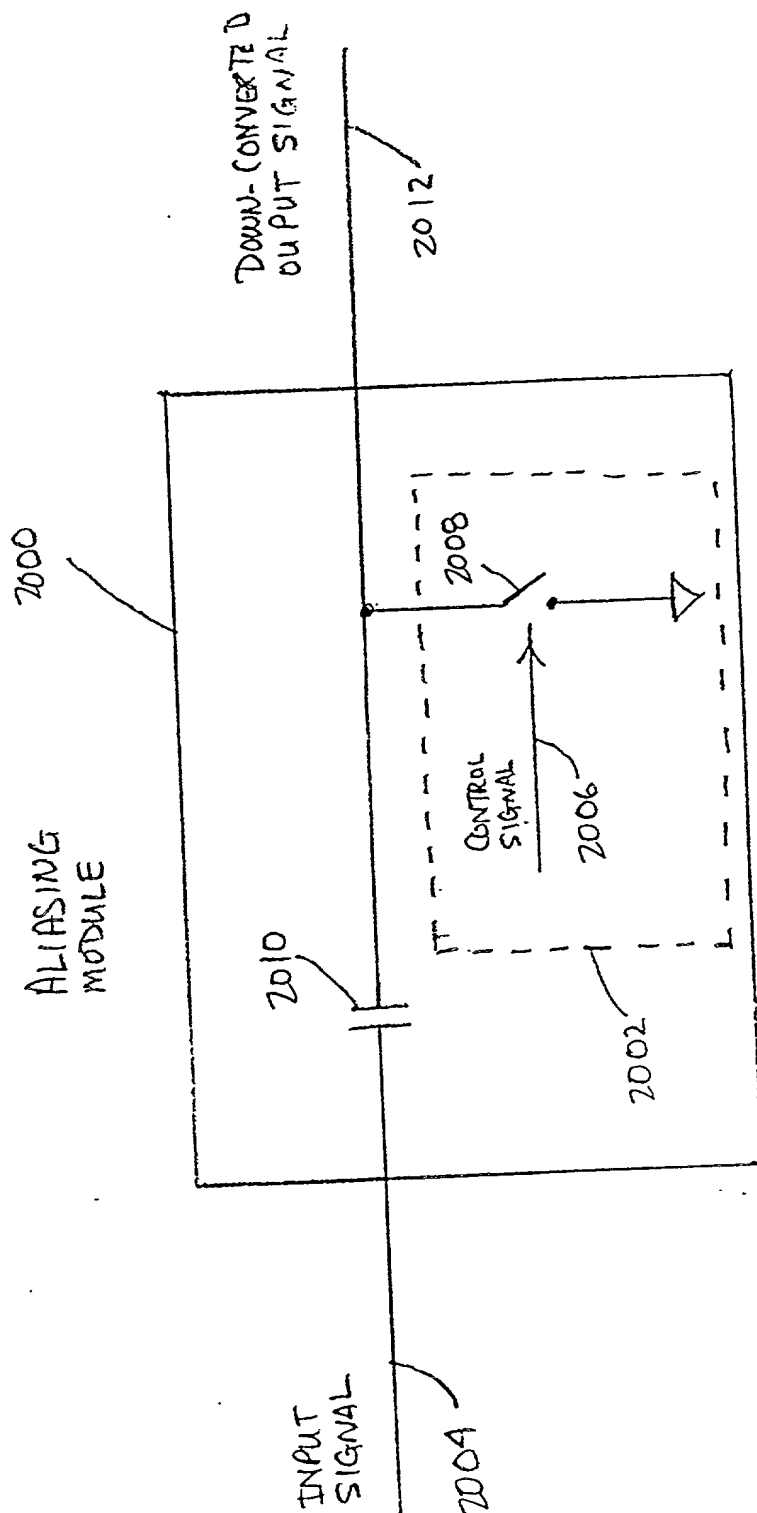


FIG. 20A-1

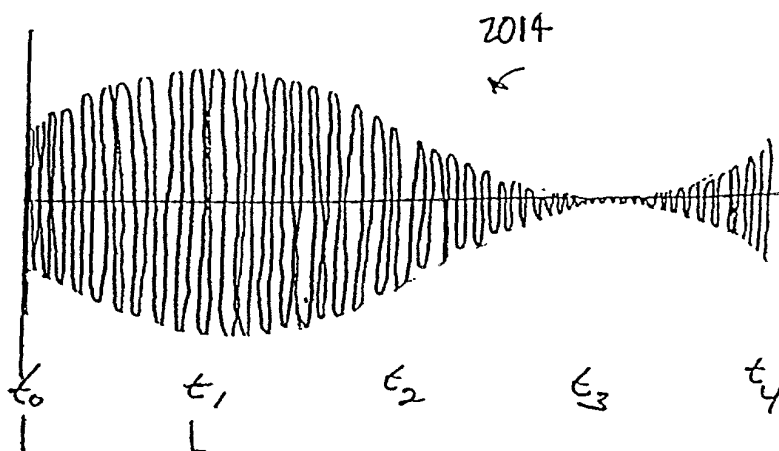


FIG. 20B

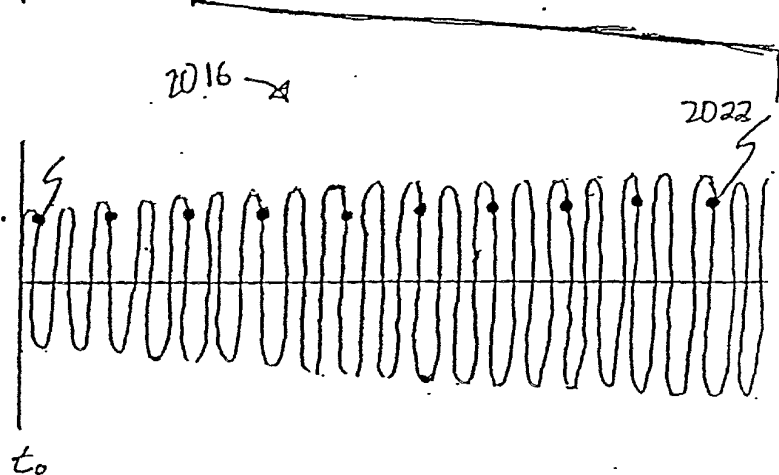


FIG. 20C

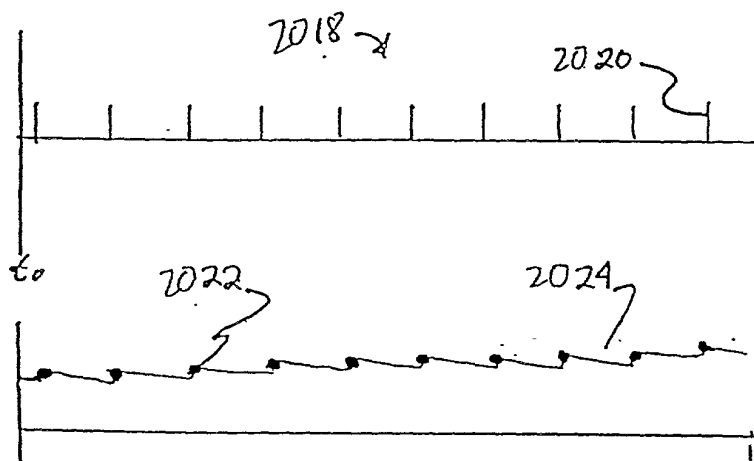


FIG. 20D

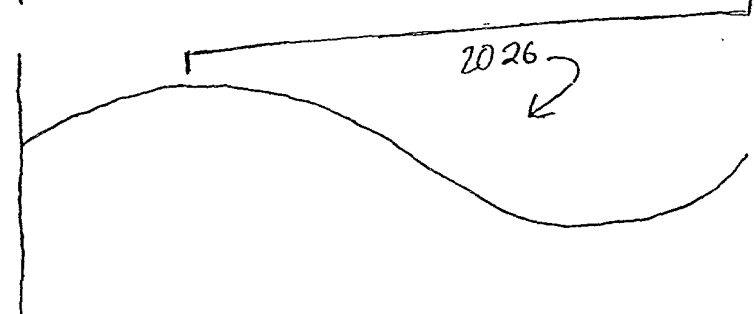


FIG. 20E

FIG. 20F

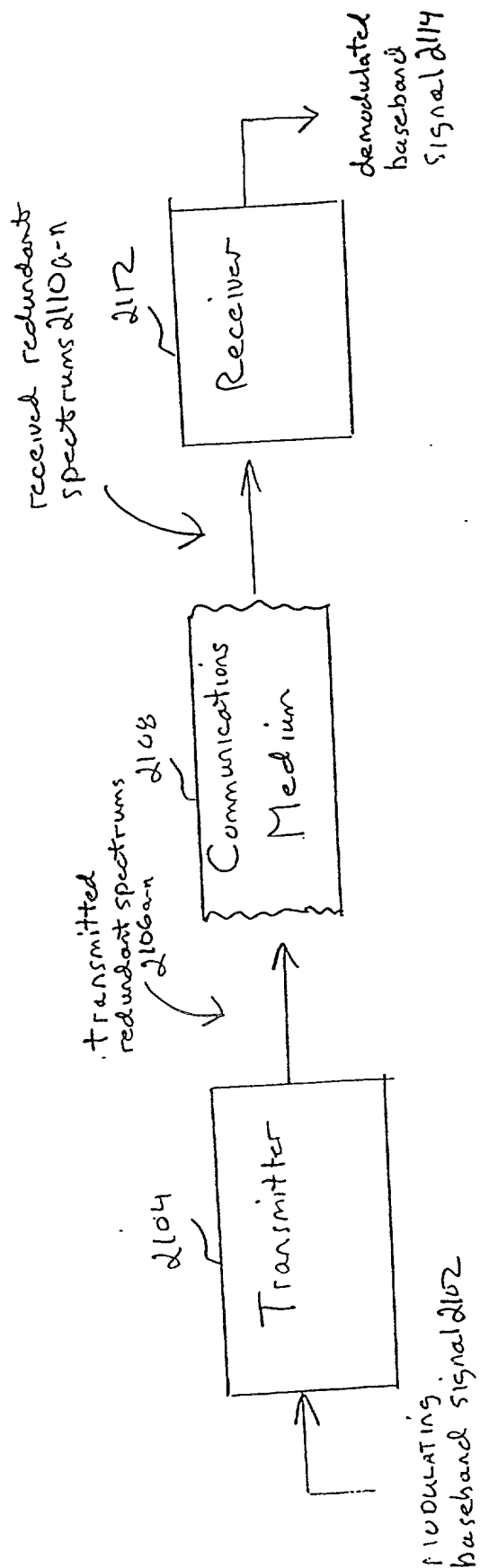


Fig. 21

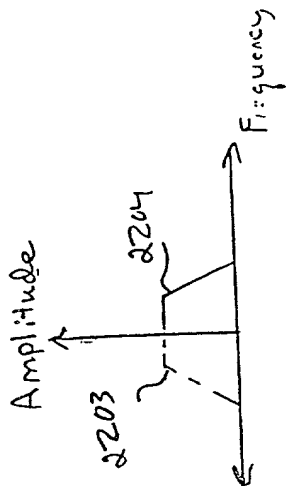


Fig. 22B

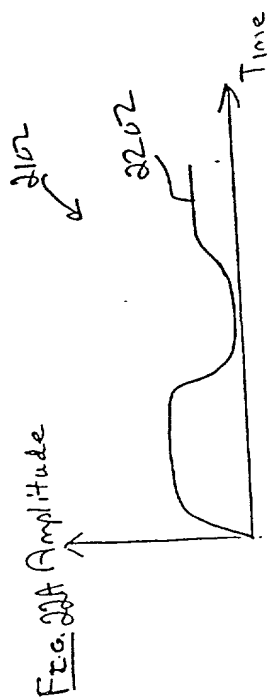


Fig. 22A

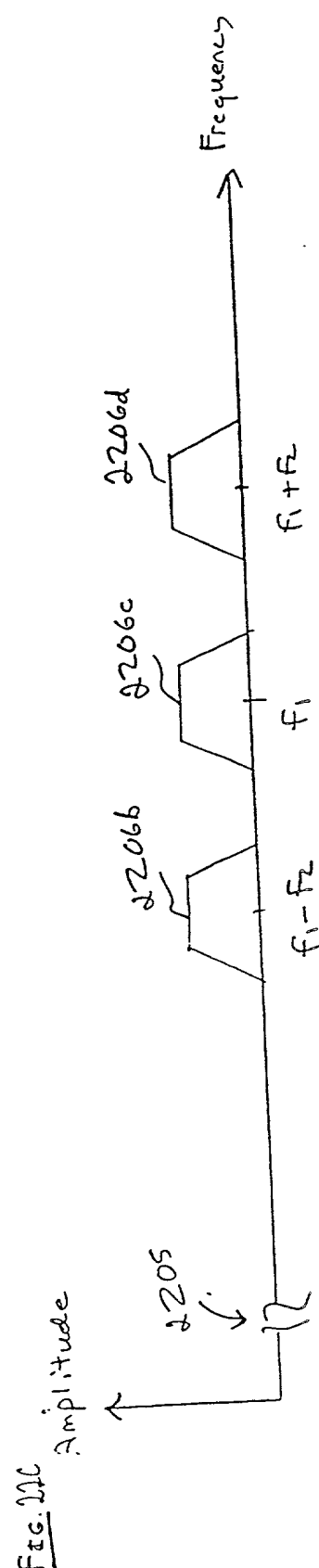


Fig. 22C

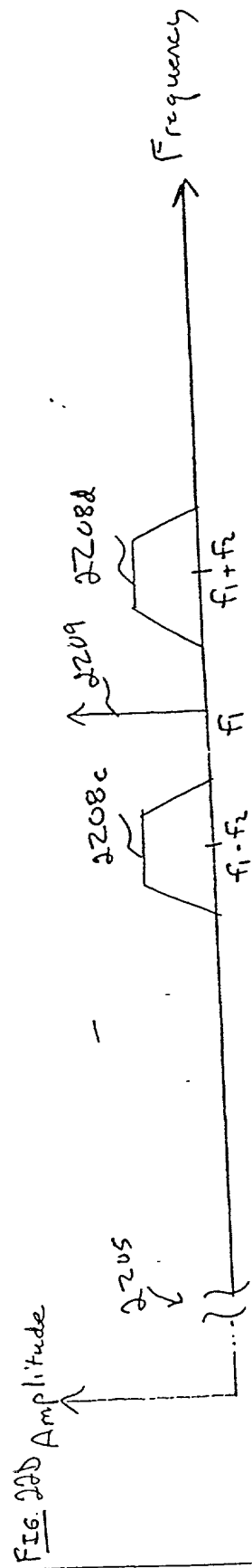
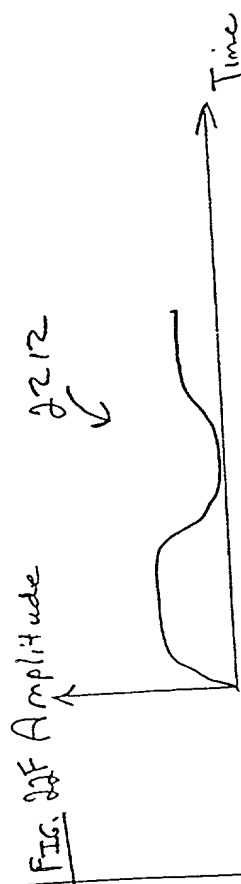
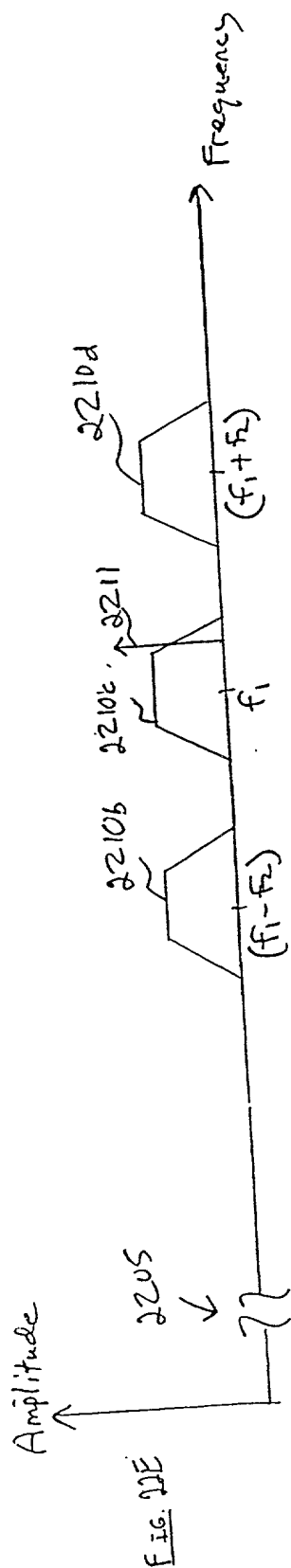


Fig. 22D



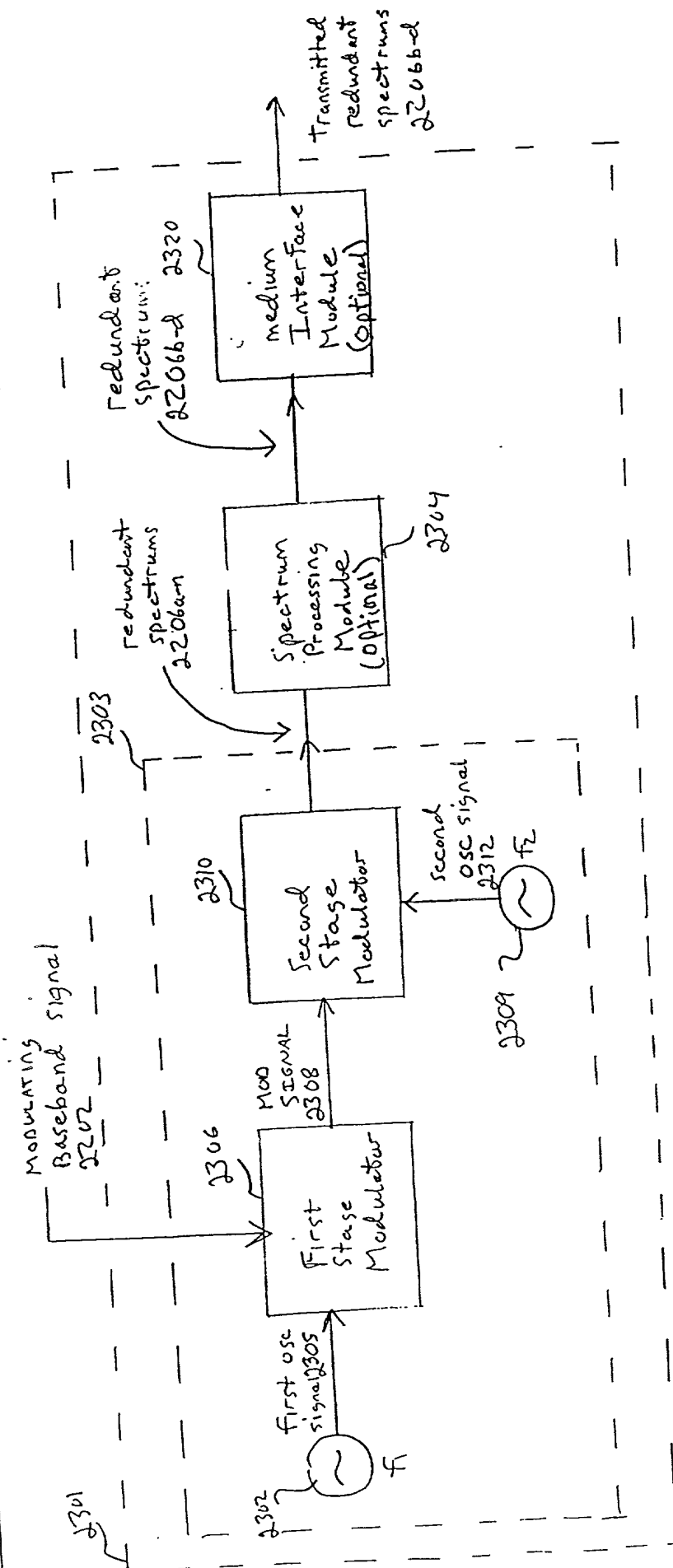


FIG. 23A

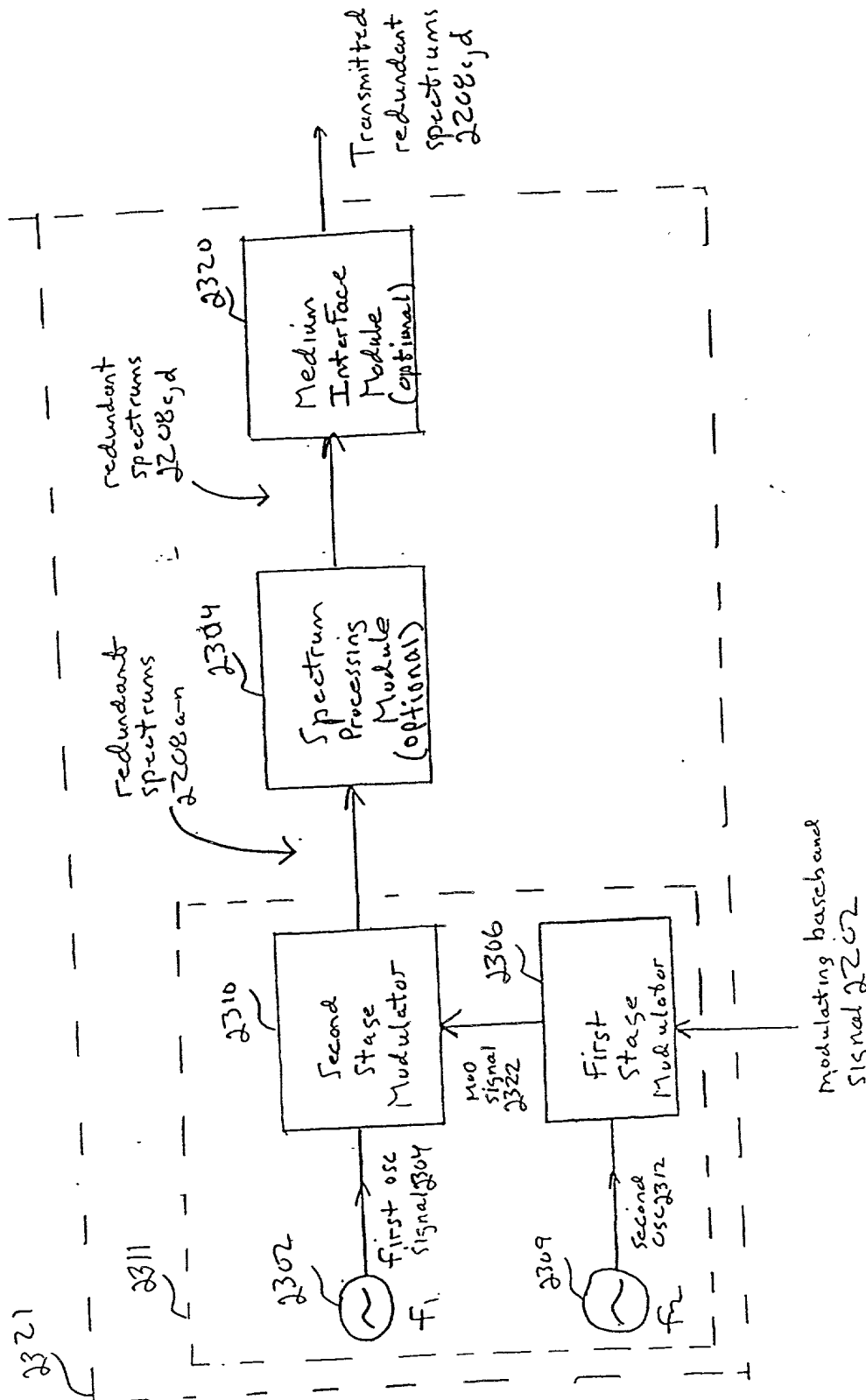


FIG. 23D

FIG. 23E

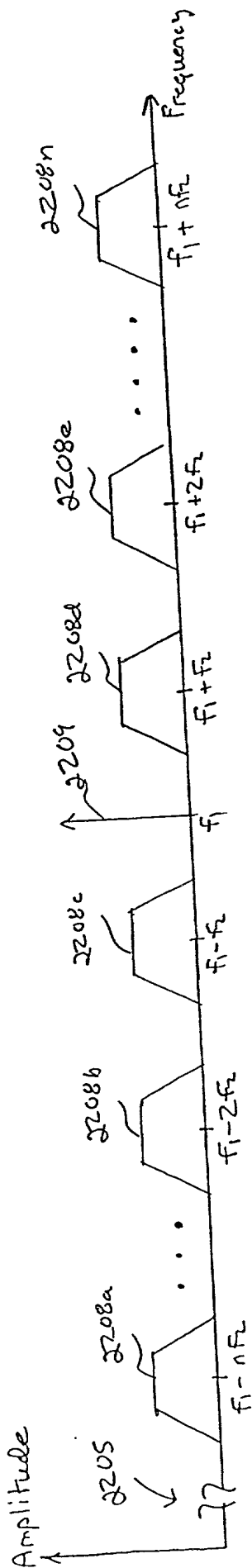
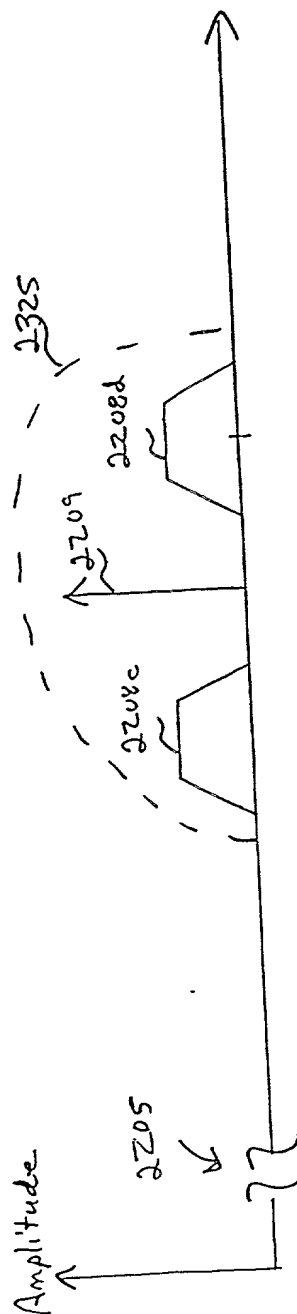


FIG. 23F



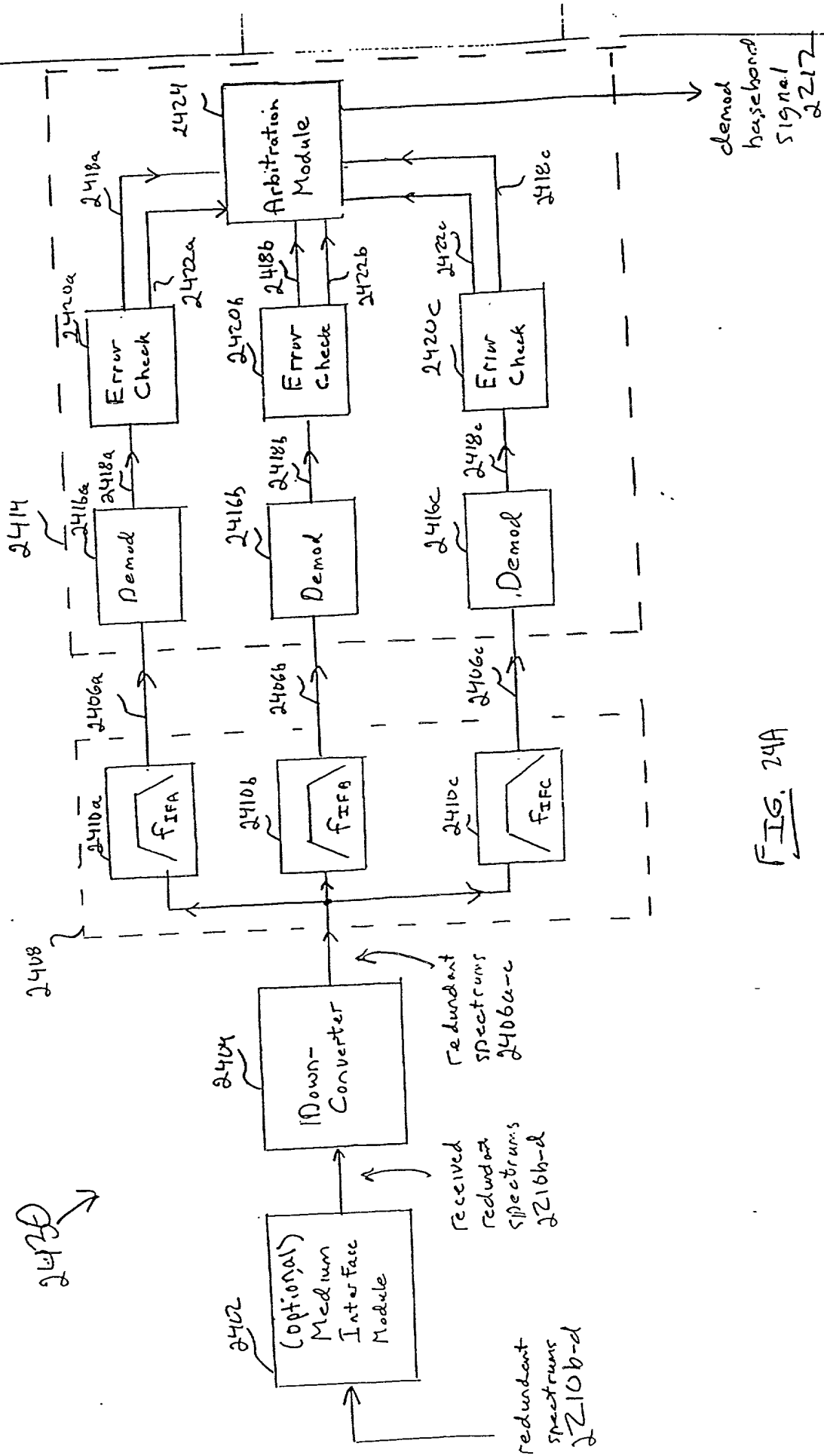
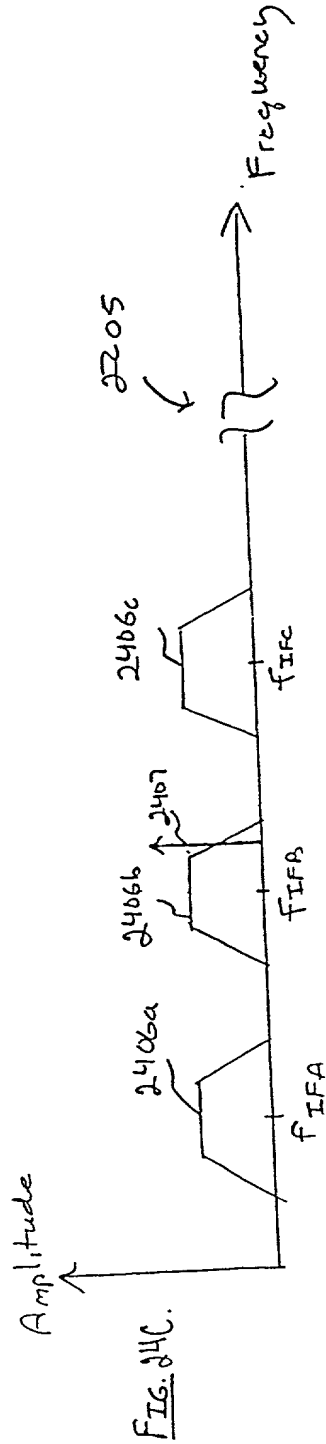
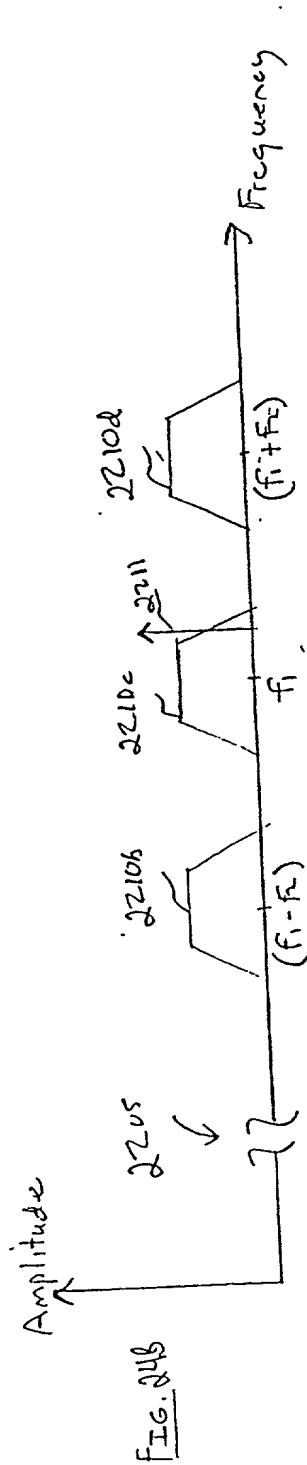
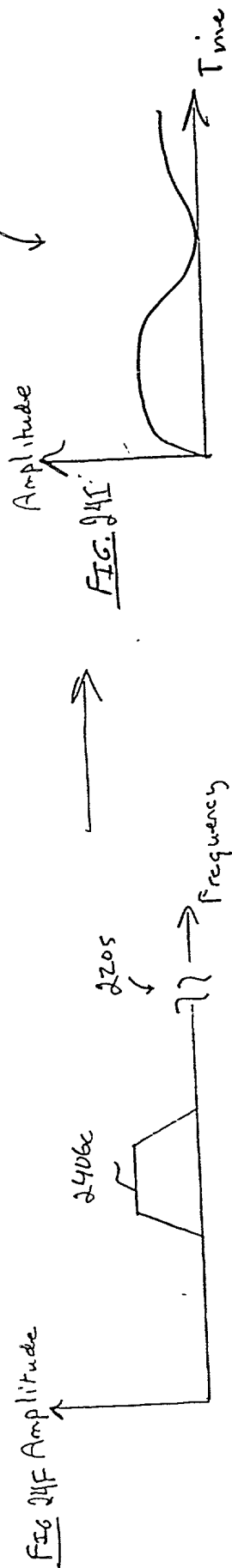
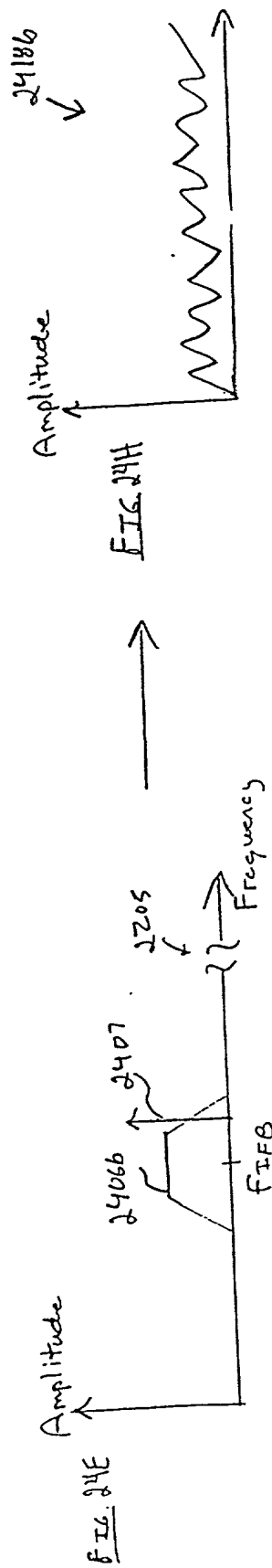
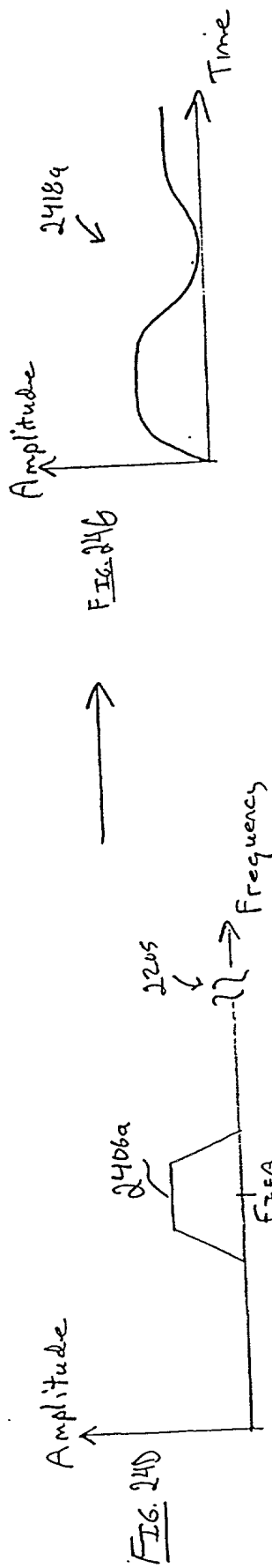


FIG. 24A





42-381 50 SHEETS 1/2" X 1/2" 5 SQUARE
 42-382 100 SHEETS 1/2" X 1/2" 5 SQUARE
 42-383 200 SHEETS 1/2" X 1/2" 5 SQUARE
 42-384 500 SHEETS 1/2" X 1/2" 5 SQUARE
 42-385 1000 SHEETS 1/2" X 1/2" 5 SQUARE
 42-386 200 RECYCLED WHITE 5 SQUARE
 42-387 200 RECYCLED WHITE 5 SQUARE
 MADE IN U.S.A.

"Cotton" Brand
 100% Cotton

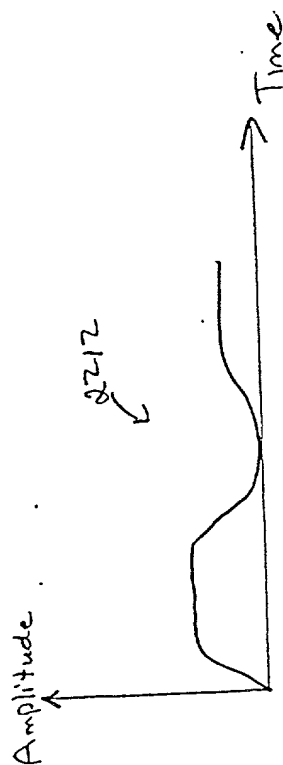


FIG. 245

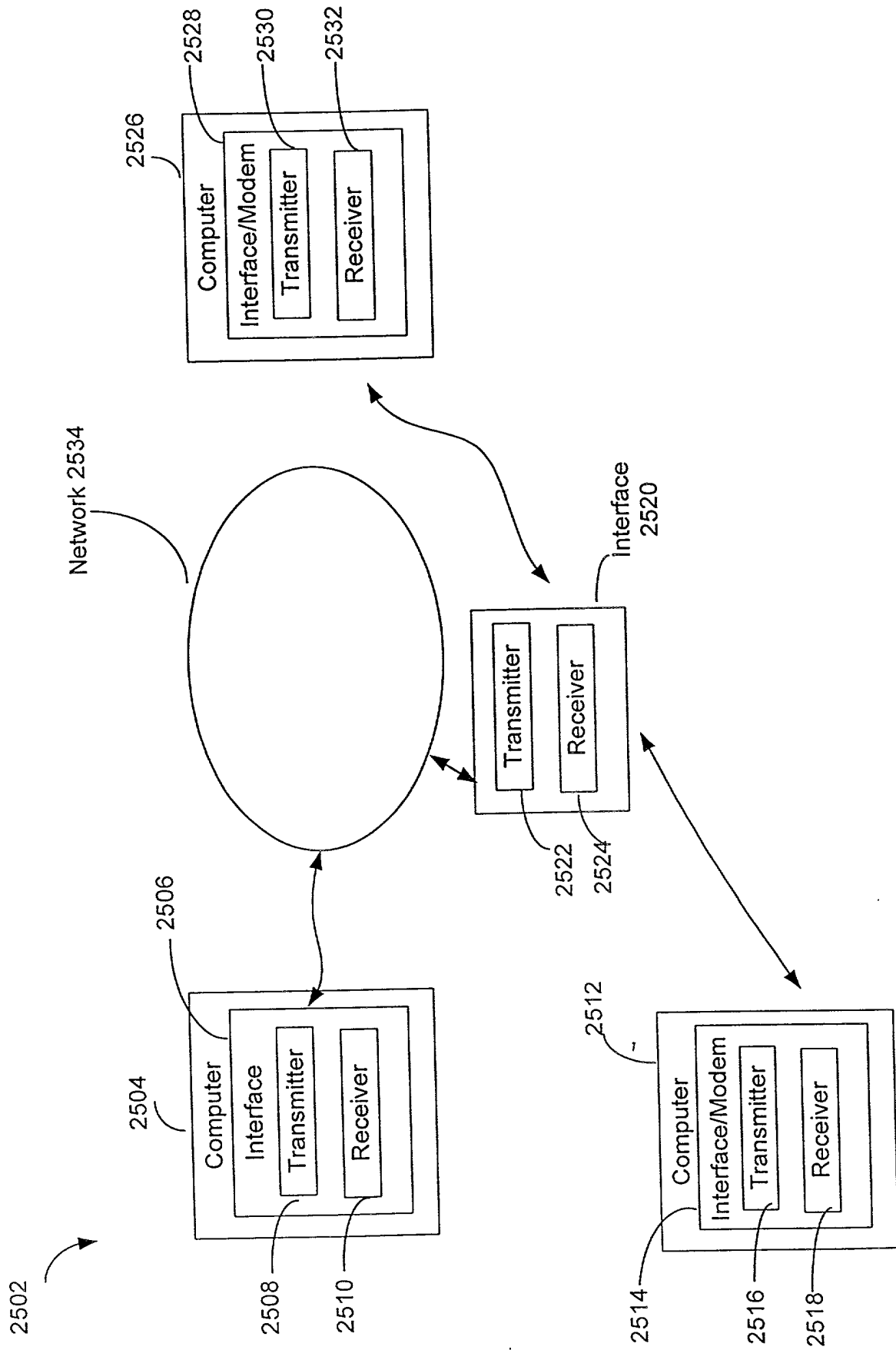


FIG. 25

2606

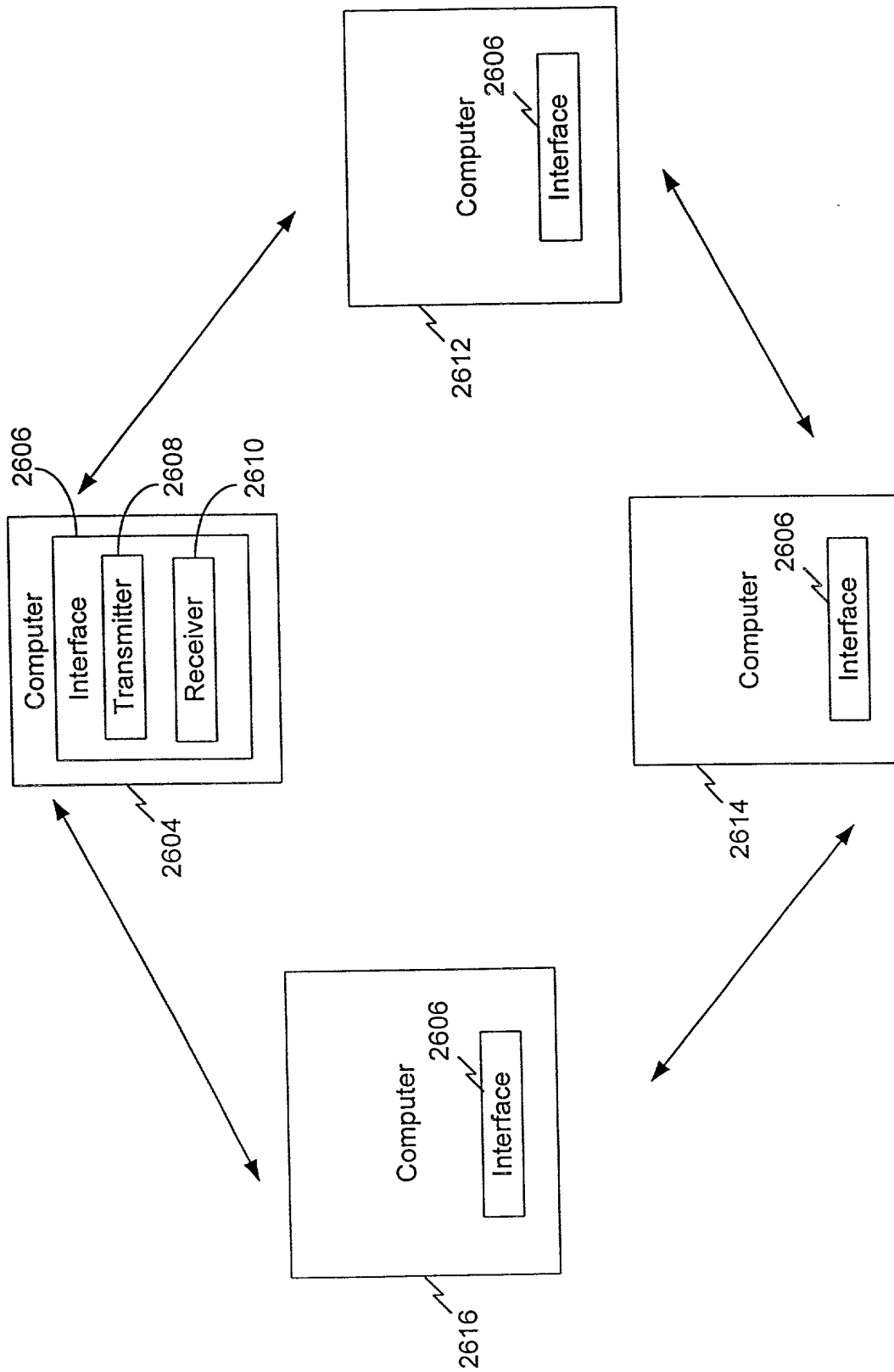


FIG. 26

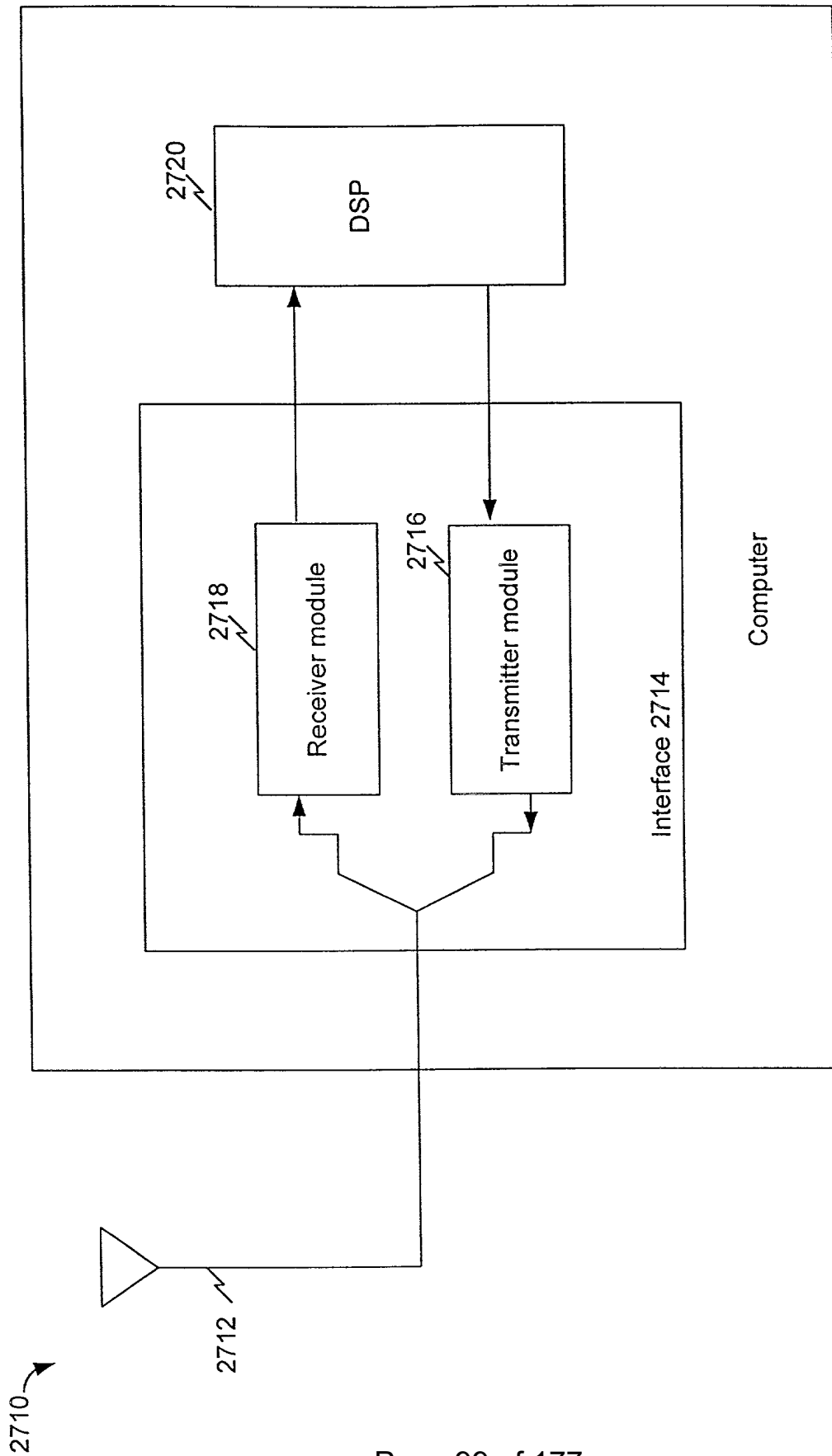
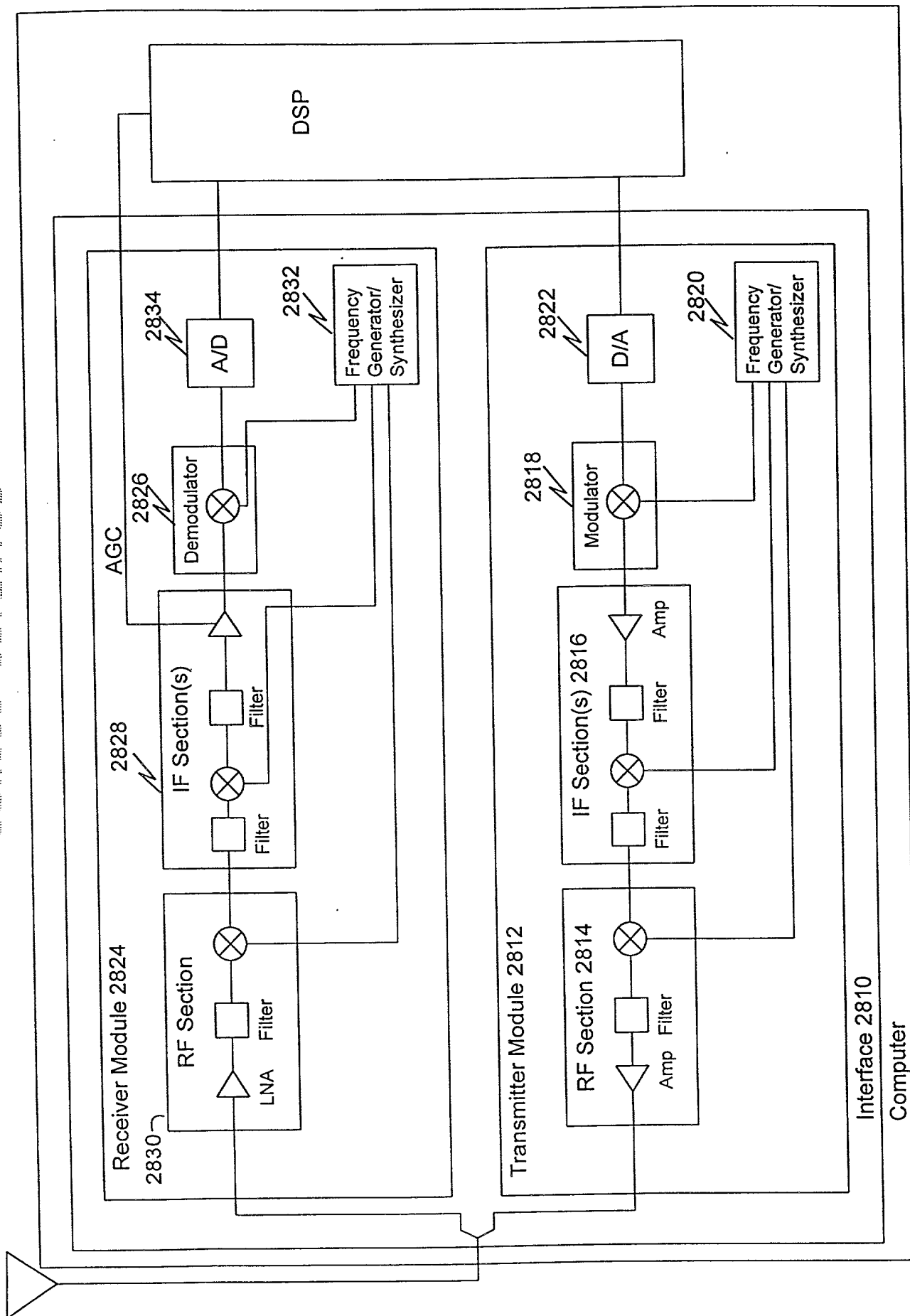


FIG. 27



Heterodyne Implementation

FIG. 28

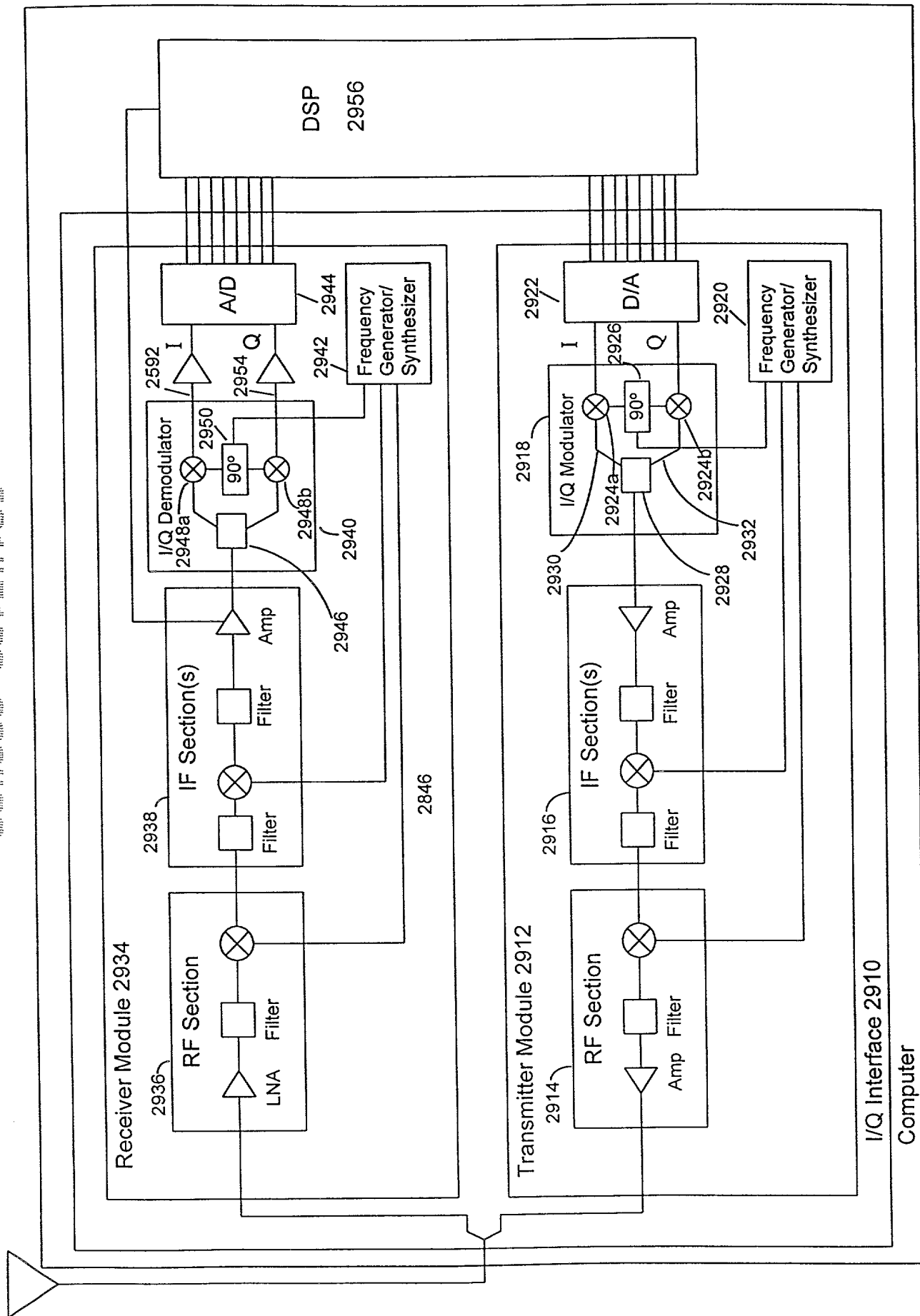


FIG. 29

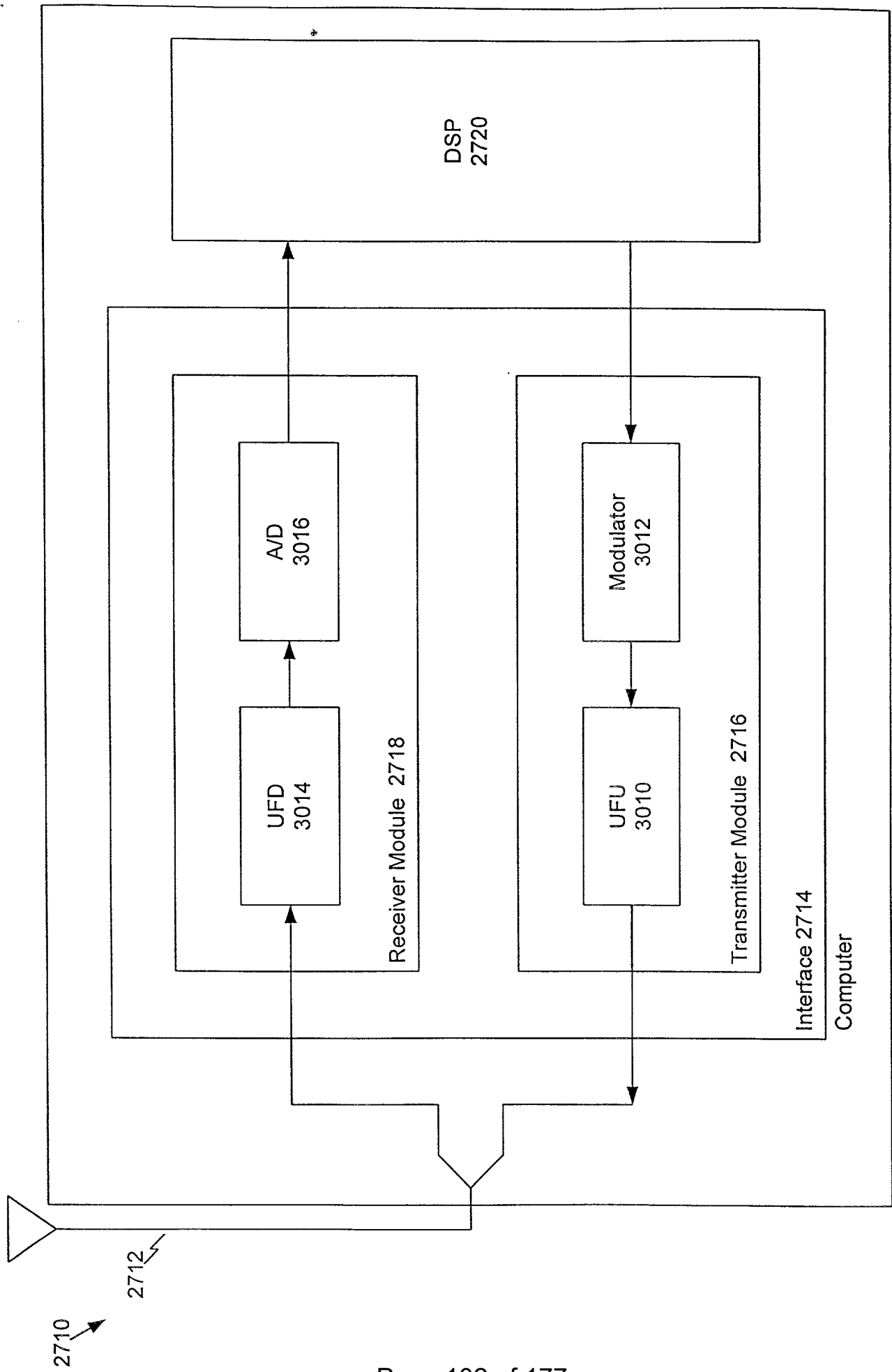


FIG. 30

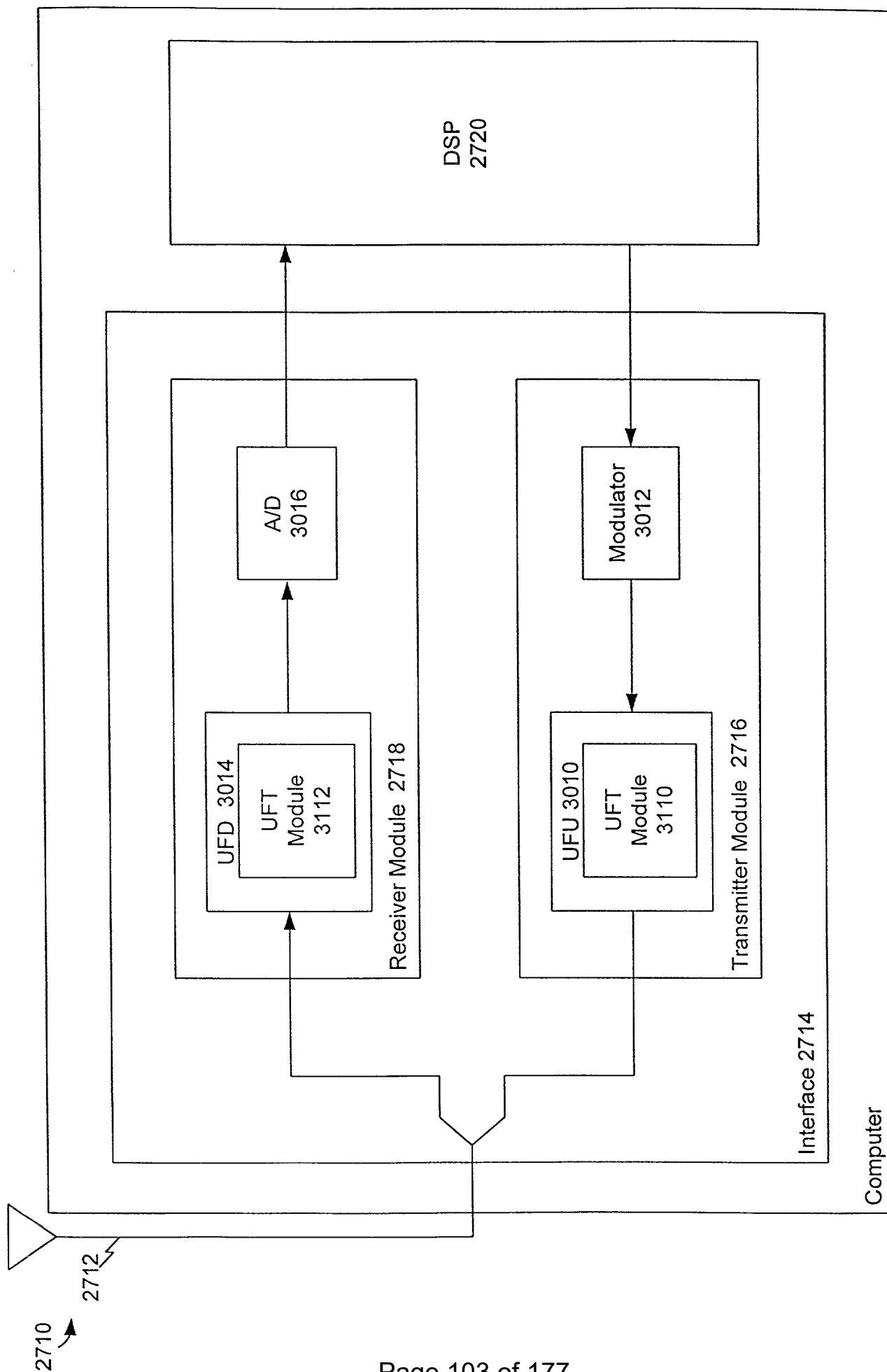


FIG. 31

2710 →

Computer

Transceiver 2714

2712

Receiver Module 2718

UFD 3014

I

3224

UFT

3228

0°

3232

Q

3226

UFT

3236

A/D

3016

3234

DSP

2720

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3220

D/A

3012

3238

Transmitter Module 2716

UFU 3010

3218

0°

3216

Q

3220

90°

3210

UFT

3214

3212

3238

D/A

3012

3234

3236

3230

3222

3218

UFT

3212

90°

3210

UFT

3214

3302
↓

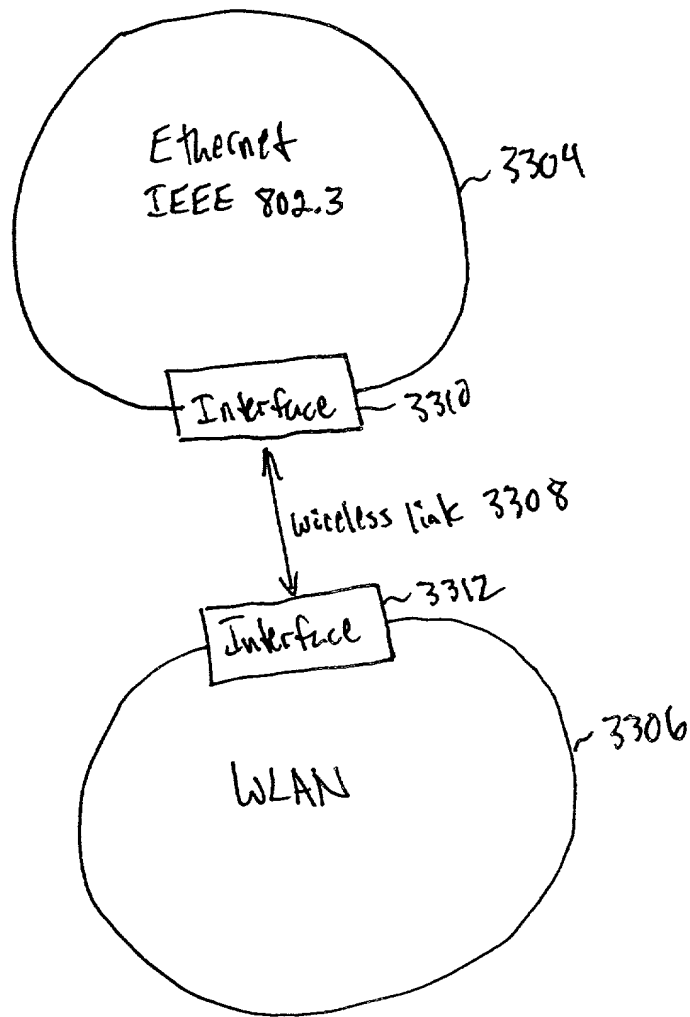


FIG. 33

3402
↓

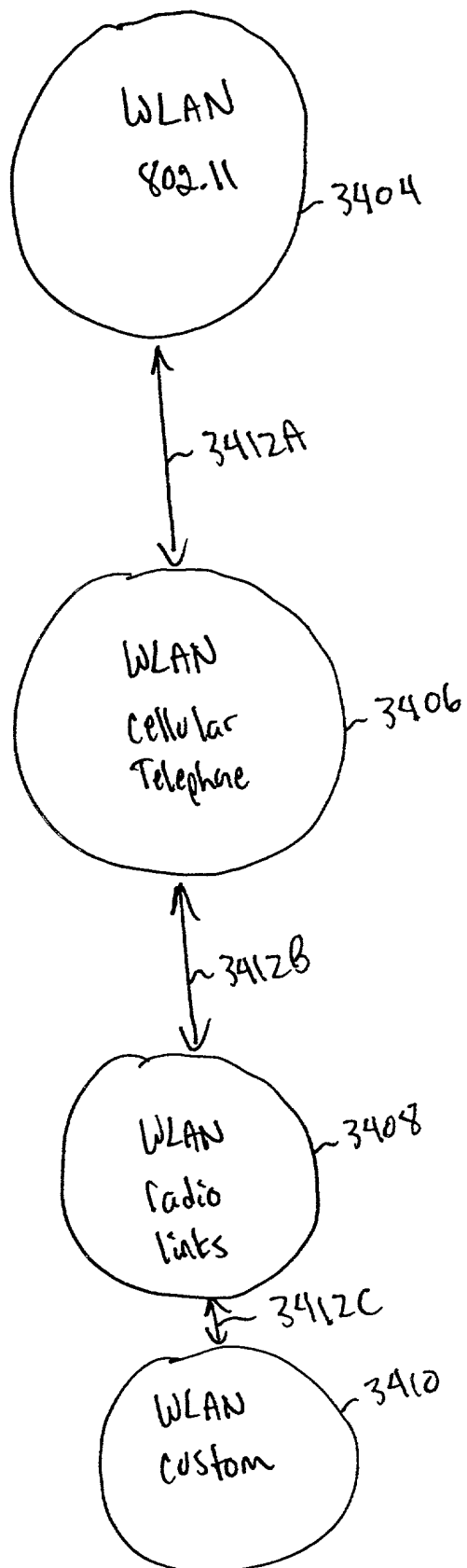
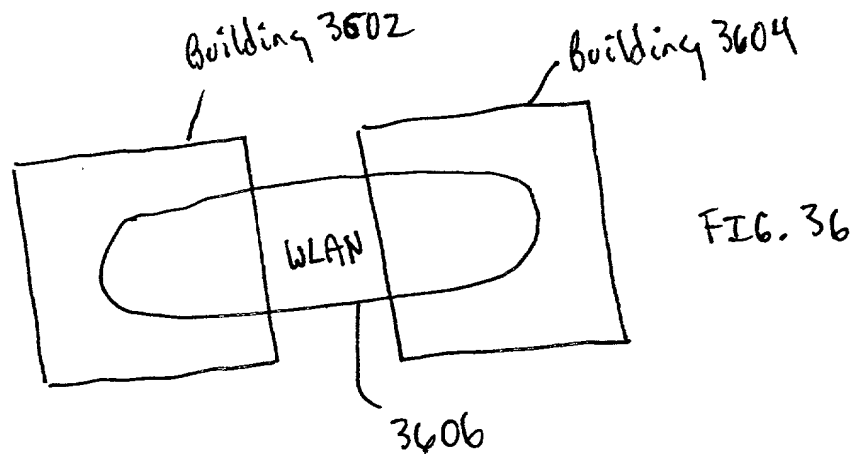
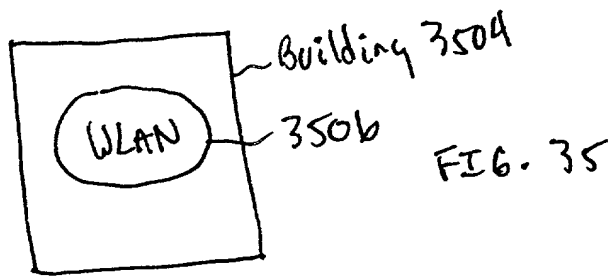


FIG. 34

3502



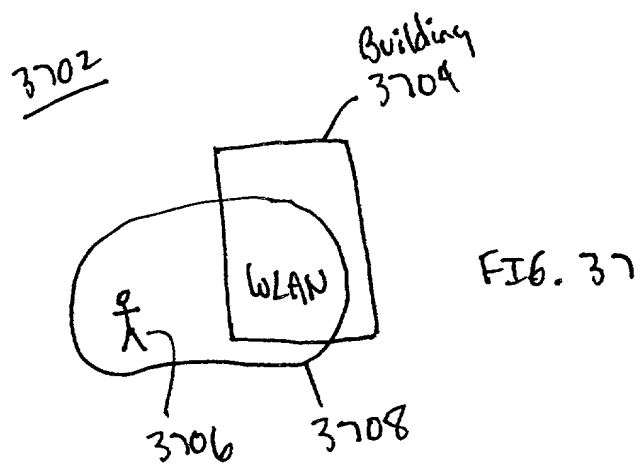


FIG. 38

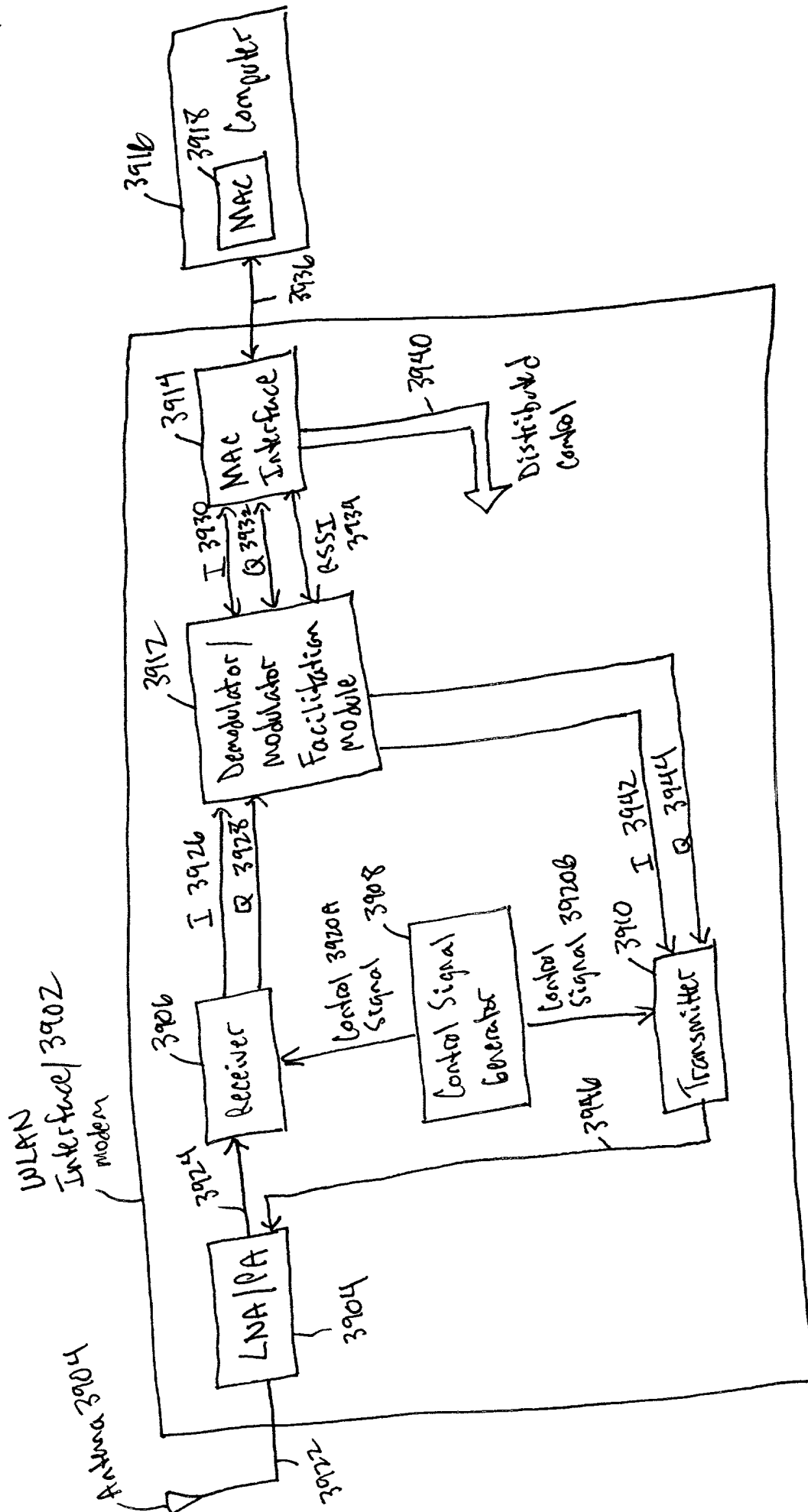


FIG. 39

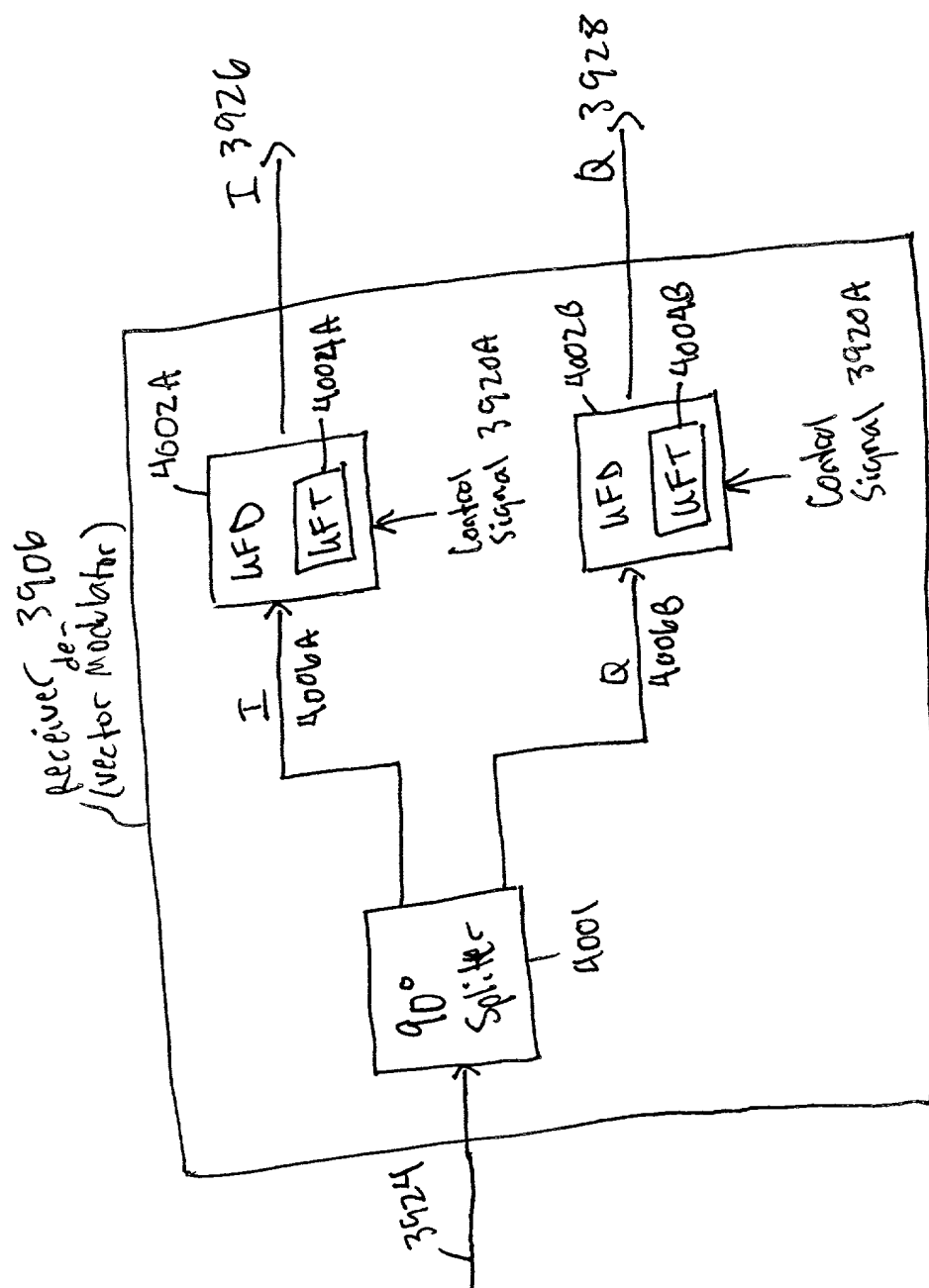


FIG. 40

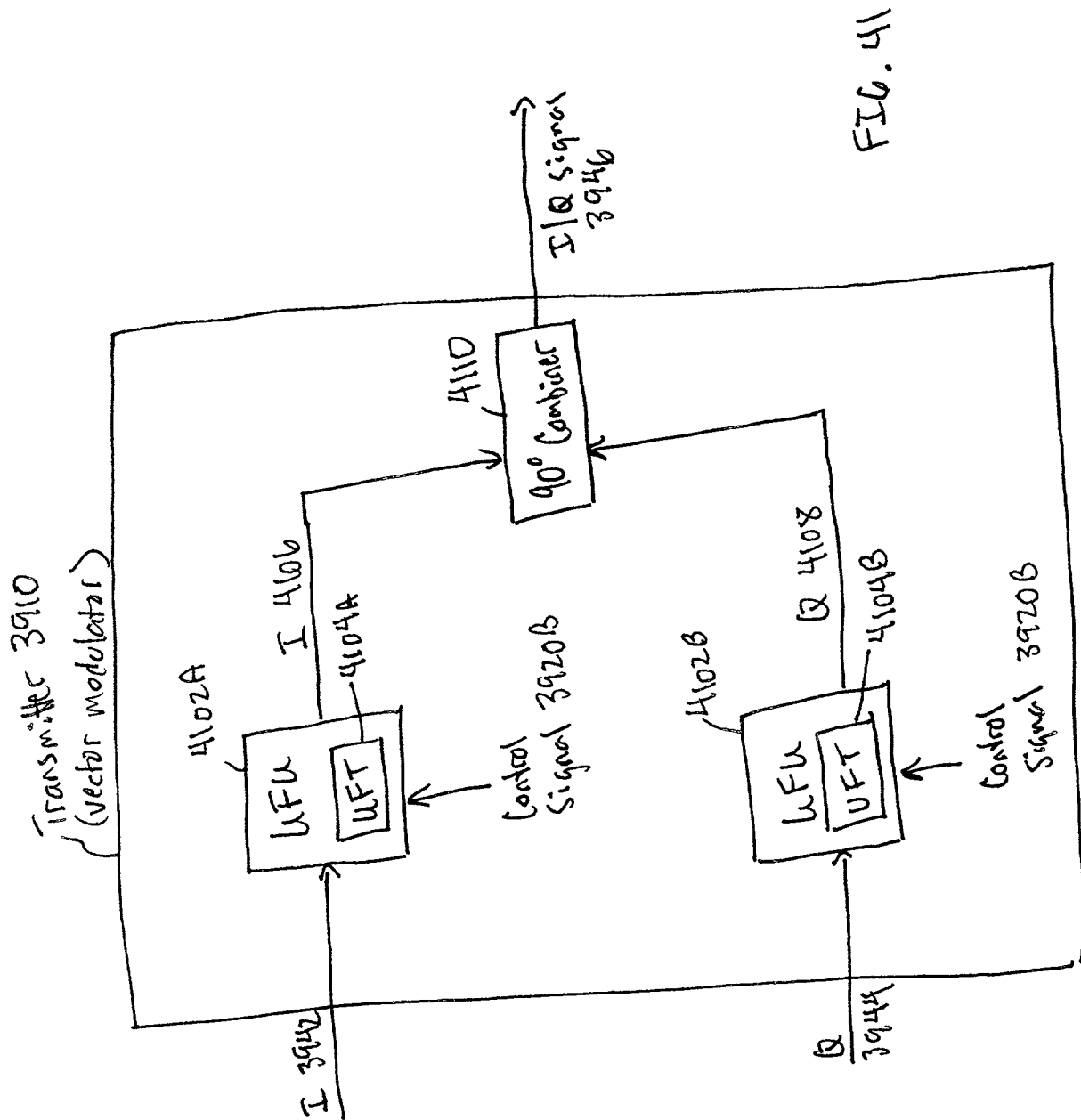
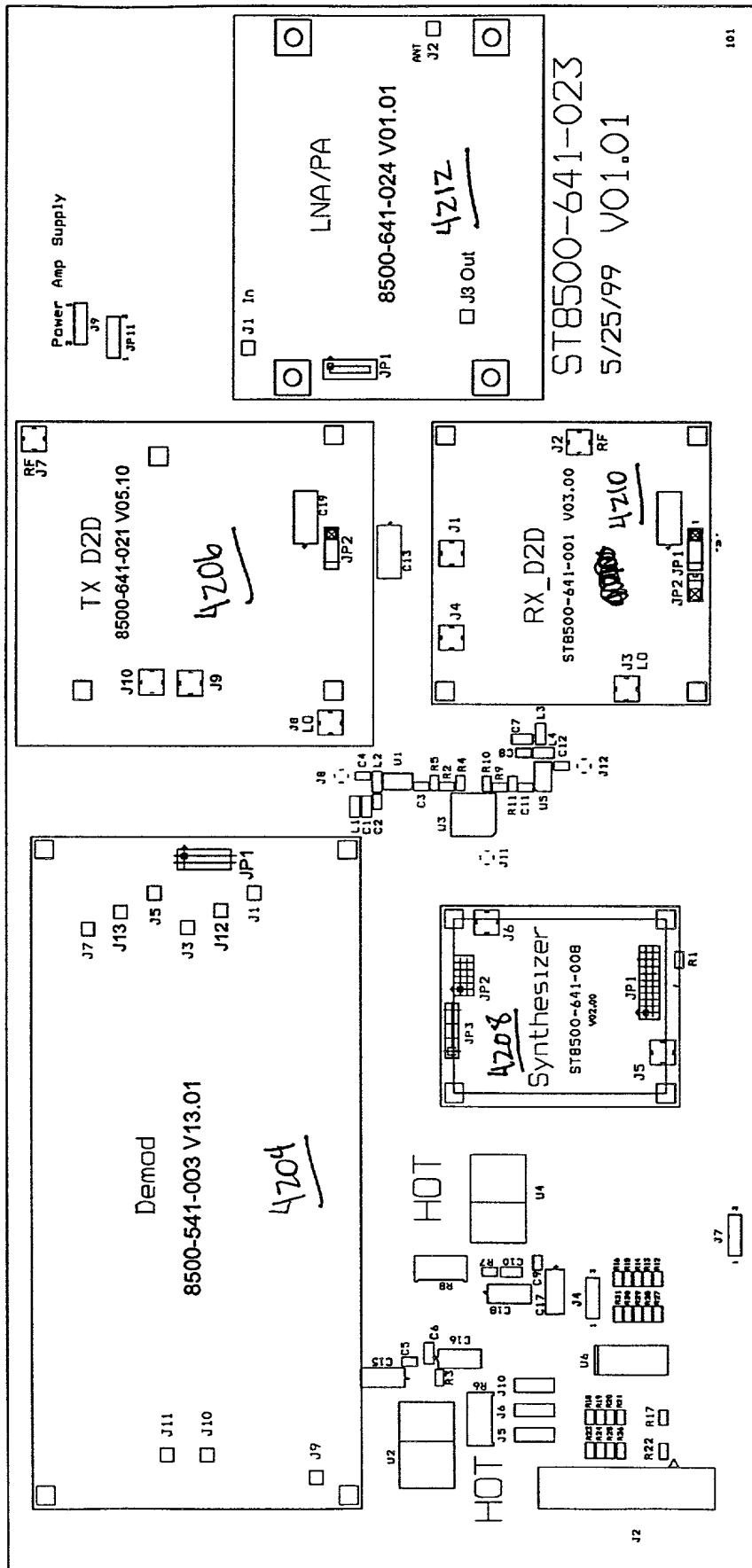


FIG. 41

4202



Signal Technologies, Inc.
ST8500-641-023 V01.01
May 25, 1999

T/R

FIG. 42

Demod

8500-541-003 V11.01

Synthesizer

ST8500-641-008 V02.00

RX_D2D

ST8500-641-001 V03.00

LNA/PA

8500-641-014 V01.01 (rx only)

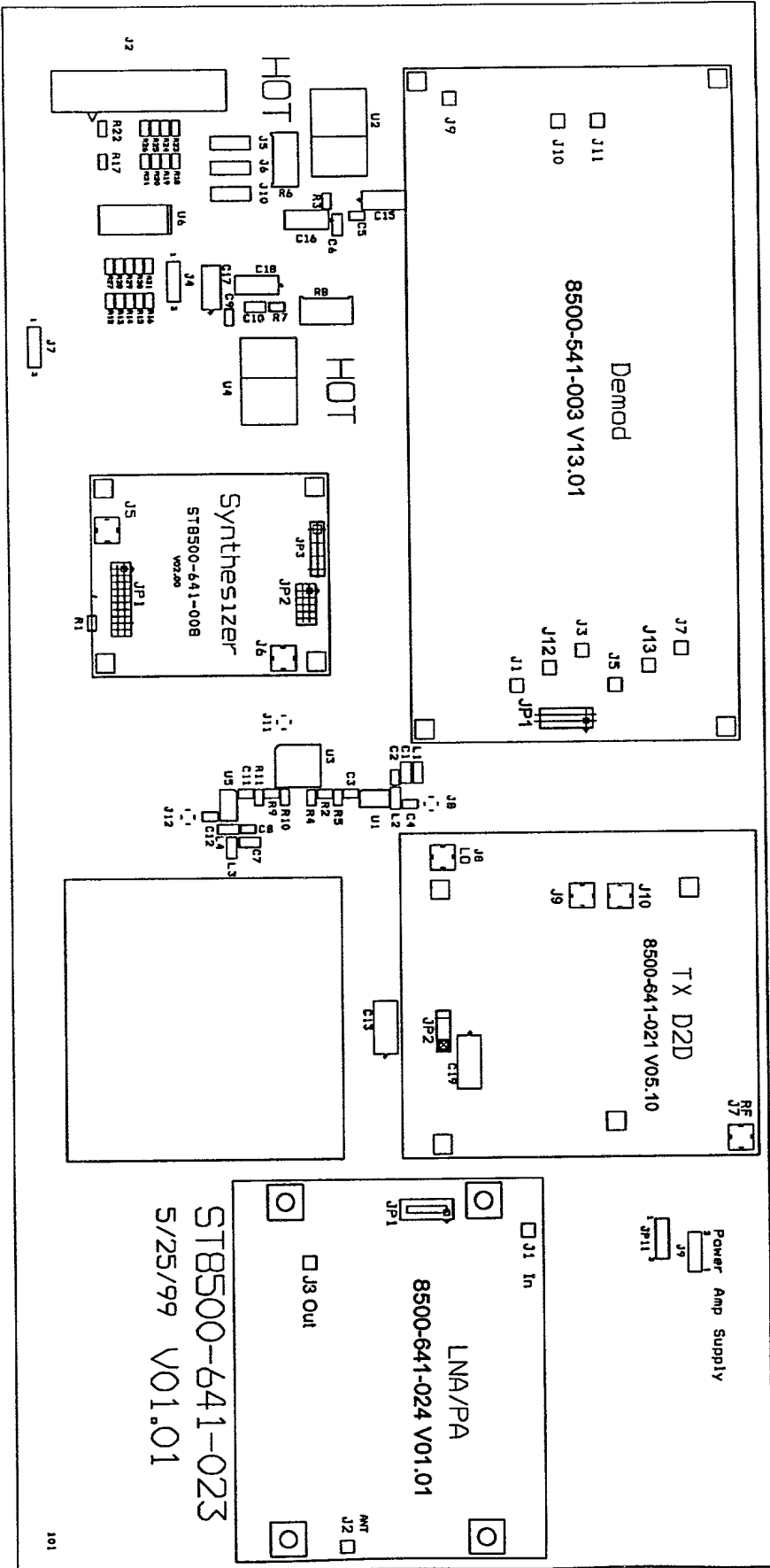
8500-641-024 V01.01

Power Amp Supply

5/25/99 V01.01

FI 6.43

4462

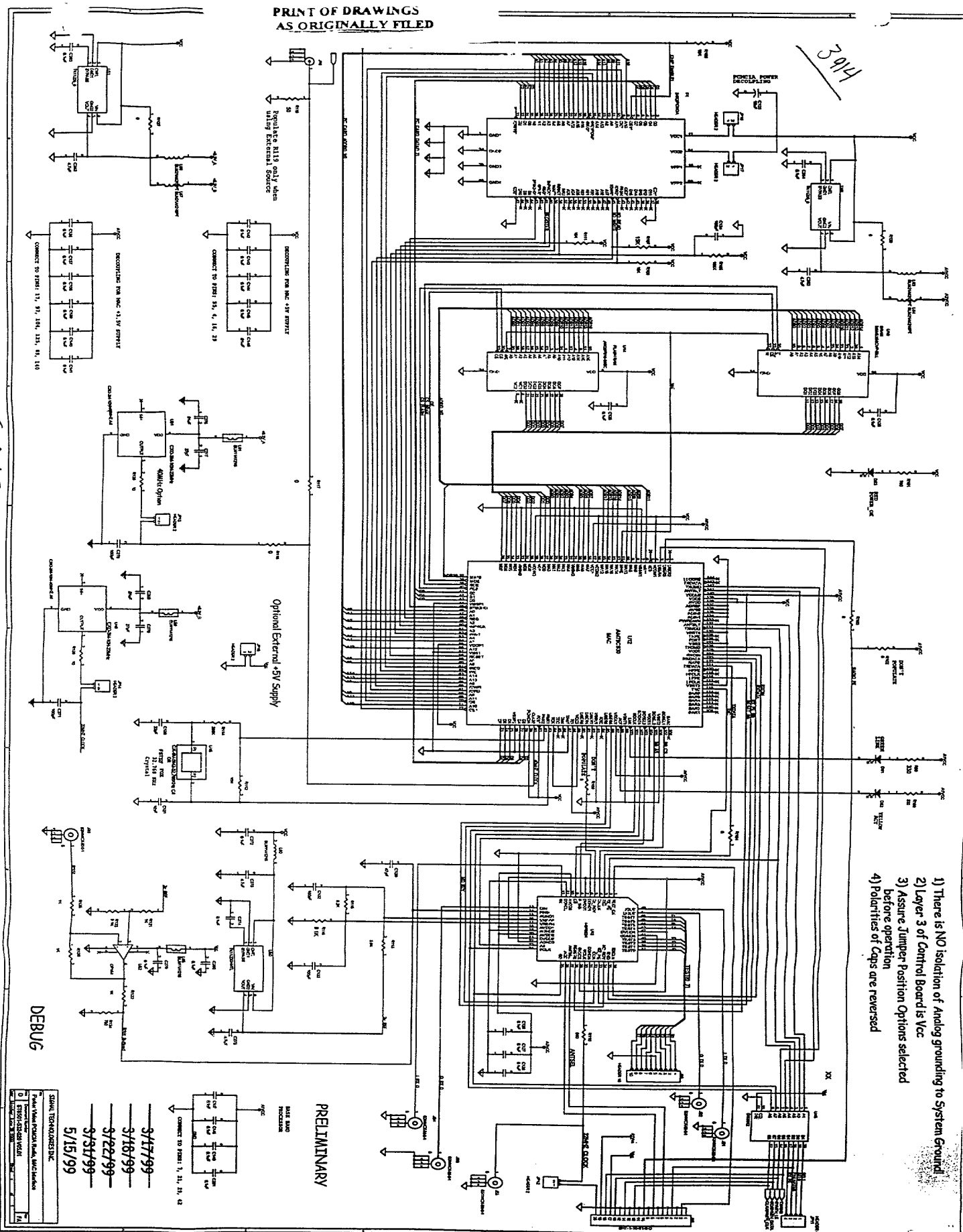


Signal Technologies, Inc.
ST8500-641-023 V01.01
May 25, 1999

Transmit Only

FIG. 44

3014



- 1) There is NO isolation of Analog grounding to System Ground
- 2) Layer 3 of Control Board is Vcc
- 3) Assume Jumper Position Options selected before operation
- 4) Polarities of Caps are reversed

PRELIMINARY

SIGNAL TECHNOLOGIES INC.	
Part Number	3/17/99
Revision	3/18/99
Drawn By	3/22/99
Checked By	3/31/99
Released By	5/15/99

60447120 1180499

PARK VISION PCMCIA CONTROLLER BOM

Item	Quantity	Reference	Part Description	Part Number	Manufacturer
1	1	C123	10uF CAP 6032, Tantalum,20%	TAJT106K010R	Kemet
2	3	C263, C273, C275, C282	4.7uF CAP 6032,Tantalum,20%	T491A475M006AS	Kemet
3	25	C120, C125, C126, C127, C128, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C147, C148, C149, C264, C272, C274, C279, C280, C281, C283	0.1uF CAP 0603,X7R,10% GRM39X7R104K050AD	GRM39X7R104K050AD	Murata
4	3	C146, C269, C276	.01uF CAP 0603,X7R,10%	GRM39X7R103K050AD	Murata
5	5	C124, C132, C133, C271, C278	100pF CAP 0603,X7R,10%	GRM39COG101K050AD	Murata
6	1	C129	47pF CAP 0603,X7R,10%	GRM39COG470J100AD	Murata
7	2	C270, C277	27pF CAP 0603,X7R,10%	GRM39COG270K050AD	Murata
8	1	C130	22pF CAP 0603,X7R,10%	GRM39COG220K050AD	Murata
9	1	C131	10pF CAP 0603,X7R,10%	GRM39COG100D050AD	Murata
10	1	DS1	LED, Green	597-3311-420	Dialight
11	1	DS2	LED Yellow	597-3401-420	Dialight
12	1	DS3	LED Red	597-3111-420	Dialight
13	6	JP12, JP13, JP14, JP15, JP16, JP17	Connector HEADER 2Pin	2MS-19-33-01	Specialty Electronics
14	1	JP11	Connector HEADER 4Pin	100VH/TM1SQW.100/4	BLKCON
15	7	J16, J20, J21, J22, J23, J24, J25	Connector 82MMCX	82MMCX-50-0-1	Huber/Shuner
16	1	J18	Connector Header10	TMS-110-01-G-S	samtec
17	1	J19	Connector with Ejector	EHT-1-10-01-S-D	samtec
18	1	P1	Connector 34X2PCMCIA	DICMJ-68S-SPC-M08	ITT Canon
19	7	L59, L60, L61, L63, L64, L65, L66	Ferrite Bead	BLM11A121S	Murata
20					
21	1	R112	10M, Resistor, 0603, 5%	ERJ-3GSYJ394V	Panasonic
22	1	R114	390K, Resistor, 0603, 5%	ERJ-3GSYJ104V	Panasonic
23	1	R105	100K, Resistor, 0603, 5%	ERJ-3GSYJ153V	Panasonic
24	4	R106, R107, R108, R111	15K, Resistor, 0603, 5%	ERJ-3GSYJ912V	Panasonic
25	1	R116	9.1K, Resistor, 0603, 5%	ERJ-3GSYJ822V	Panasonic
26	1	R115	8.2K, Resistor, 0603, 5%	ERJ-3GSYJ392V	Panasonic
27	1	R113	3.9K, Resistor, 0603, 5%	ERJ-3GSYJ751V	Panasonic
28	1	R101	750, Resistor, 0603, 5%	ERJ-3GSYJ561V	Panasonic
29	1	R110	560, Resistor, 0603, 5%	ERJ-3GSYJ331V	Panasonic
30	2	R99, R100	330, Resistor, 0603, 5%	ERJ-3GSYJ331V	Panasonic

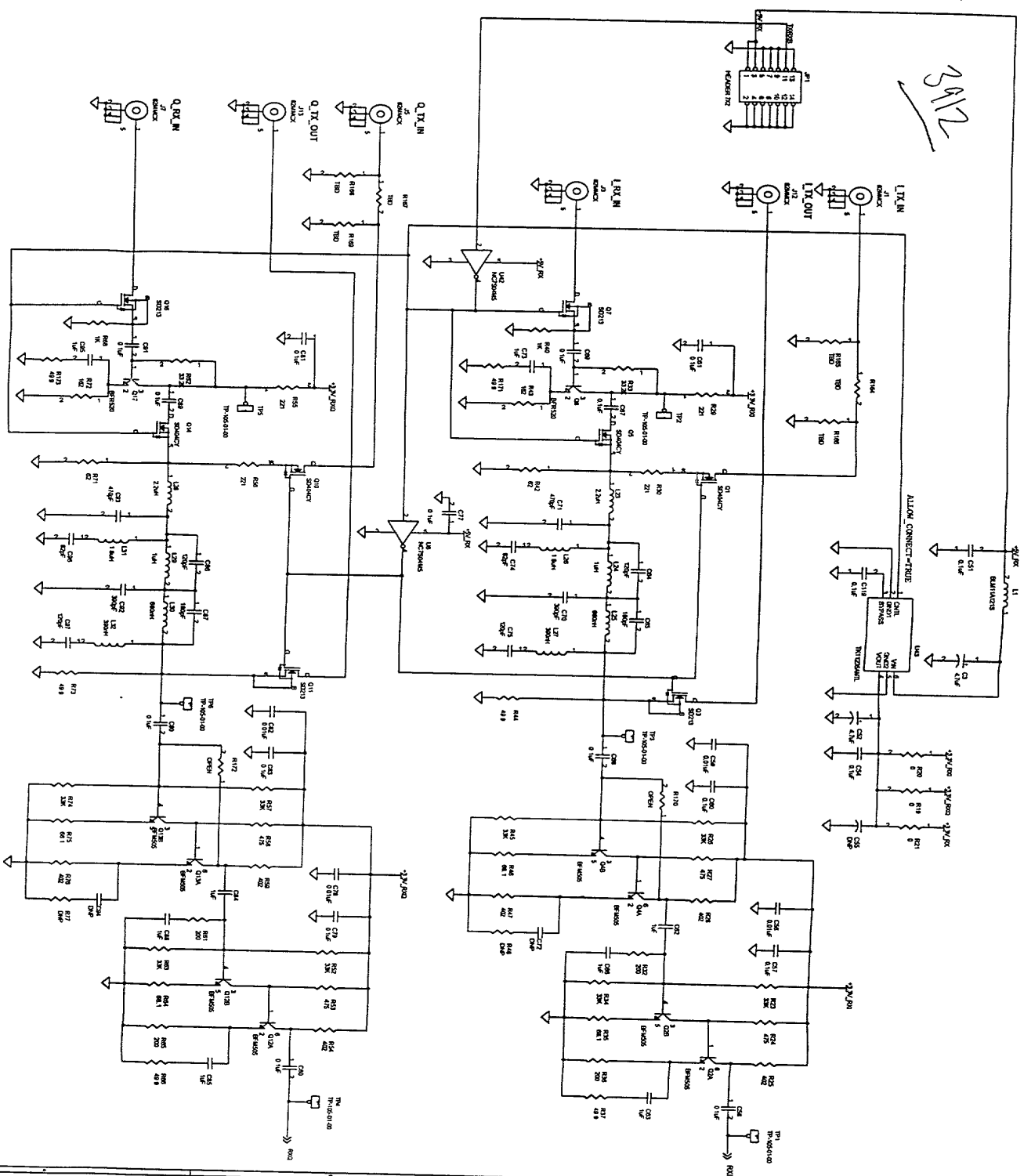
FIG. 46A

31	1	R119	50 , Resistor, 0603, f	ERJ-3GSYJ500V	Panasonic
32	2	R128, R129	10 , Resistor, 0603, b.	ERJ-3GSYJ100V	Panasonic
33	8	R102, R103, R104, R109, R117, R118, R120, R127	0, Resistor, 0603, 5%	RM732Z1J000ZT	ERJ-KOA
34	6	R121, R122, R123, R124, R125, R126	TBD, Resistor, 0603, 5%	3GSYJ000V	Panasonic
35	1	U10		R	Panasonic
36	1	U12	SRAM	KM62256DLTG-5L	Samsung
37	1	U13	MAC	M5M5256CVP-55LL	Mitsubishi
38	1	U14	Baseband Processor	AM79C930	AMD
39	1	U15	FLASH RAM	HFA3842 A1	Harris
40	2	U45	32 KHz Crystal	AM29F010-55EC	AMD
41	1	U48	Bus Buffer	CX-6V-SM2-32.768KHz C/I	Statek
42	1	U49	Regulator 3.5 V	DS3862	National
43	1	U50	22MHz Oscillator	TK11235BMC	TOKO
44	1	U51	2 Volt Reference	FOX F3346-22MHz	FOX
			40MHz Oscillator	TK11220BMC	TOKO
				CXO-M-10N-40MHz A/I	Statek

FIG. 46B

3412

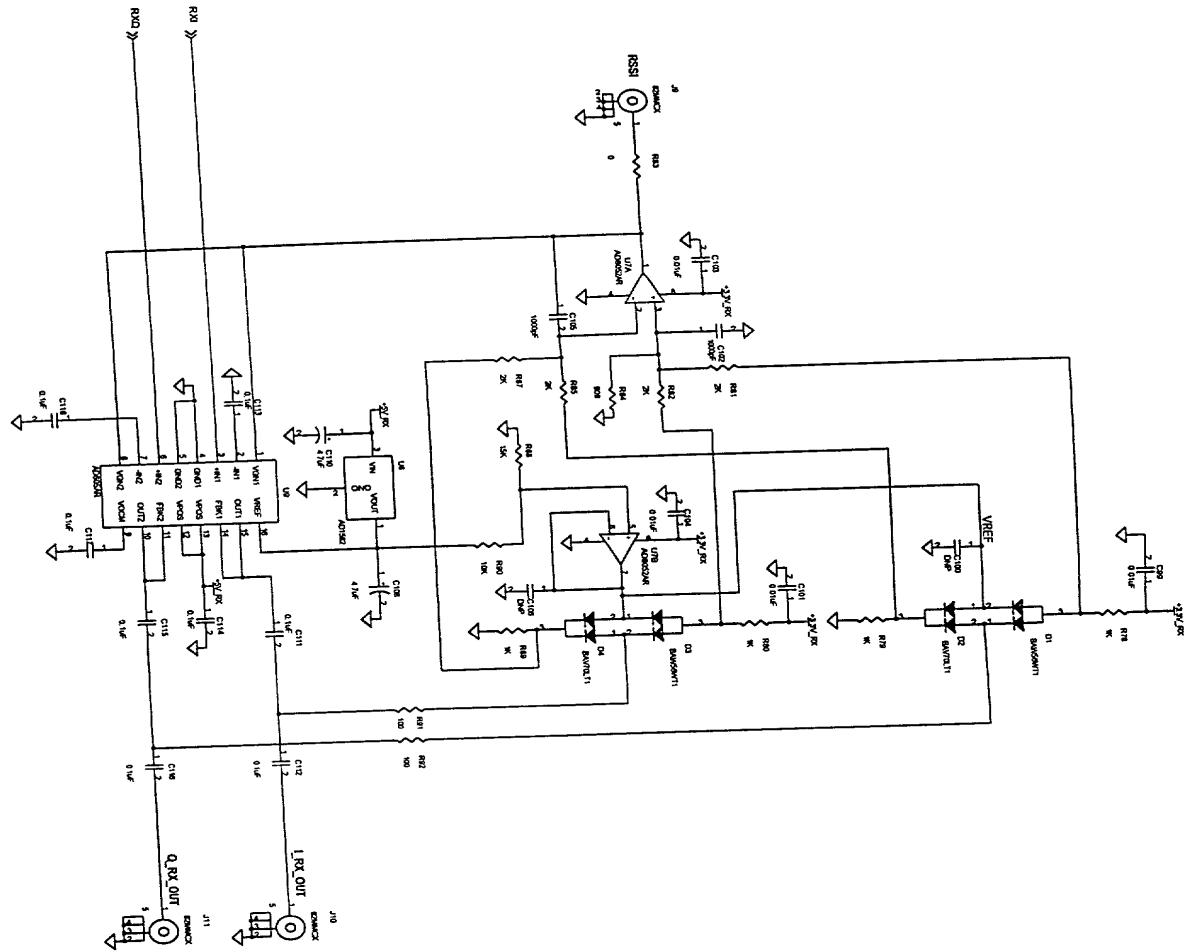
FIG. 47



SIGNAL TECHNOLOGIES INC.	
STP-Radio Vision PCMCIA Radio Demod	
Document Number	
STP-R90-92-003 V14.00	
Rev	1
DATE	10/1/92
BY	N

30/12

FIG. 48



SIGNAL TECHNOLOGIES INC	
100	STP-Patent Vision PIVOLUX Road, Dorset
101	Document Number
102	STP000-003 V14.00
103	Version
104	1.0
105	Sheet
106	2
107	of
108	3
109	Rev
110	N

SIGNAL TECHNOLOGIES INC.

July: Page1

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	4	C3,C52,C108,C110	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61, C67,C68,C69,C77,C79,C80, C81,C83,C89,C90,C91,C111, C112,C113,C114,C115,C116, C117,C118,C119	0.1uF	GRM39Y5V104Z016	Murata
3	1	C55	DNP	T491A475K006AS	KEMET
4	8	C56,C59,C78,C82,C99,C101, C103,C104	0.01uF	GRM39X7R103K050	Murata
5	8	C62,C63,C66,C73,C84,C85, C88,C95	1uF	GRM40Y5V105Z016	Murata
6	4	C64,C75,C86,C97	120pF	GRM39COG121J050	Murata
7	2	C65,C87	180pF	GRM39COG181J050	Murata
8	2	C70,C92	390pF	GRM39COG391J050	Murata
9	2	C71,C93	470pF	GRM39COG471J050	Murata
10	2	C72,C94	DNP	GRM40Y5V105Z016	Murata
11	2	C74,C96	82pF	GRM39COG820J050	Murata
12	2	C100,C106	DNP	DNP	Murata
13	2	C105,C102	1000pF	GRM39COG102K050	Murata
14	2	D3,D1	BAW56WT1	BAW56WT1	Motorola
15	2	D4,D2	BAV70LT1	BAV70LT1	Motorola
16	1	JP1	HEADER 7X2	FTSH-107-02-L-D	Samtec
17	9	J1,J3,J5,J7,J9,J10,J11, J12,J13	82MMCX	82MMCX-50-0-1	Suhner
18	1	L1	BLM11A121S	BLM11A121S	Murata
19	2	L23,L28	2.2uH	LQG21N2R2K10	Murata
20	2	L29,L24	1uH	LQG21N1R0K10	Murata
21	2	L30,L25	680nH	LQG21NR68K10	Murata
22	2	L26,L31	1.8uH	LQG21N1R8K10	Murata
23	2	L32,L27	390nH	LQG21NR39K10	Murata
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	Calogic
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	Philips
26	4	Q3,Q7,Q11,Q16	SD213	SD213	Calogic
27	2	Q17,Q8	BFR520	BFR520	Philips
28	4	R19,R20,R21,R83	0	ERJ3GSY0R00	Panasonic
29	8	R23,R26,R34,R45,R52,R57, R63,R74	33K	ERJ3GSYJ333	Panasonic
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	Panasonic
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	Panasonic
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	Panasonic
33	2	R32,R61	200	ERJ3GSYJ201	Panasonic
34	2	R33,R62	33.2K	ERJ3GSYJ333	Panasonic
	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	Panasonic

FIG. 49A

36	2	R36,R65	200	ERJ3EKF2000	Panasonic
7	6	R37,R44,R66,R73,R171, R173	49.9	ERJ3EKF49R9	Panasonic
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	Panasonic
39	2	R42,R71	62	ERJ3GSYJ620	Panasonic
40	2	R43,R72	162	ERJ3EKF1620	Panasonic
41	2	R77,R48	DNP	ERJ3GSYJ330	Panasonic
42	4	R81,R82,R85,R87	2K	ERJ3EKF2001	Panasonic
43	1	R84	909	ERJ3EKF9090	Panasonic
44	1	R88	15K	ERJ3EKF1502	Panasonic
45	1	R90	10K	ERJ3EKF1002	Panasonic
46	2	R91,R92	100	ERJ3EKF1000	Panasonic
47	6	R164,R165,R166,R167,R168, R169	TBD		Panasonic
48	2	R170,R172	OPEN		Panasonic
49	6	TP1,TP2,TP3,TP4,TP5,TP6	TP-105-01-00		
50	2	U42,U6	NC7S04M5	NC7S04M5	National Semiconductor
51	1	U7	AD8052AR	AD8052AR	Analog Devices
52	1	U8	AD1582	AD1582	Analog Devices
53	1	U9	AD605AR	AD605AR	Analog Devices
54	1	U43	TK11235AMTL	TK11235BM	Toko

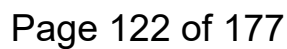
55

1

Board

8500.541.003 V13.01

FIG. 49B





FT6.51

Page 123 of 177

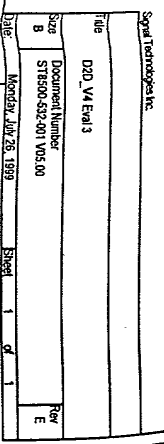
SIGNAL TECHNOLOGIES INC.

Page1

Bill Of Materials July 27,1999 11:20:09

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	3	C3,C52,C55	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61, C67,C68,C69,C77,C79,C80, C81,C83,C89,C90,C91,C111, C112,C113,C114,C115,C116, C117,C118,C119	0.1uF	GRM39Y5V104Z016	Murata
3	8	C56,C59,C78,C82,C99,C101, C103,C104	0.01uF	GRM39X7R103K050	Murata
4	10	C62,C63,C66,C72,C73,C84, C85,C88,C94,C95	1uF	GRM40Y5V105Z016	Murata
5	4	C64,C75,C86,C97	120pF	GRM39COG121J050	Murata
6	2	C87,C65	180pF	GRM39COG181J050	Murata
7	2	C70,C92	390pF	GRM39COG391J050	Murata
8	2	C71,C93	470pF	GRM39COG471J050	Murata
9	2	C96,C74	82pF	GRM39COG820J050	Murata
10	5	C100,C102,C105,C106,C107	100pF	GRM39COG101K050	Murata
*1	1	C108	1uF		
	1	C110	4.7uF		
13	2	D3,D1	BAW56WT1	BAW56WT1	Motorola
14	2	D4,D2	BAV70LT1	BAV70LT1	Motorola
15	2	JP2,JP1	HEADER 7X2		
16	6	J1,J3,J5,J7,J10,J11	82MMCX	142-0701-231	Johnson
17	1	J9	82MMCX	82MMCX-50-0-1	Suhner
18	1	L1	BLM11A121S	BLM11A121S	Murata
19	2	L28,L23	2.2uH	LQG21N2R2K10	Murata
20	2	L24,L29	1uH	LQG21N1R0K10	Murata
21	2	L30,L25	680nH	LQG21NR68K10	Murata
22	2	L26,L31	1.8uH	LQG21N1R8K10	Murata
23	2	L27,L32	390nH	LQG21NR39K10	Murata
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	Calogic
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	Philips
26	4	Q3,Q7,Q11,Q16	SD213	SD213	Calogic
27	2	Q17,Q8	BFR520	BFR505	Philips
28	5	R19,R20,R21,R171,R173	0		
29	8	R23,R26,R34,R45,R52,R57, R63,R74	33K	ERJ3GSYJ333	Panasonic
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	Panasonic
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	Panasonic
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	Panasonic
33	2	R32,R61	200	ERJ3GSYJ201	Panasonic
34	2	R33,R62	33.2K	ERJ3GSYJ333	Panasonic
	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	Panasonic
	2	R36,R65	200	ERJ3EKF2000	Panasonic

FIG. 52A



Signal Technologies Inc.

July Page1

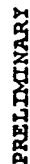
Item	Quantity	Reference	Part	Part Number	Manufacturer
1	10	C/R7,C/R15,C16,C17,C18, C19,C21,C22,C23,C24	0.1uF	GRM39Y5V104Z016	Murata
2	6	C1,C3,C6,C8,C9,C12	22pF	GRM39COG220J050	Murata
3	3	C2,C4,C11	0.1uF	GRM39X7R104K016	Murata
4	2	C5,C15	47pF	GRM39COG470J050	Murata
5	2	C10,C7	1000pF	GRM39X7R102K050	Murata
6	1	C13	100pF	GRM39X7R101J050	Murata
7	1	C14	3pF	GRM40COG030B50V	Murata
8	2	C20,C25	1uF	GRM40Y5V105Z016	Murata
9	1	JP1	69190-403	69190-403	BERG
10	1	JP2	69190-402	69190-402	BERG
11	4	J1,J2,J3,J4	82MMCX-50-0-1	82MMCX-50-0-1	Suhner
12	2	L3,L1	DNP	L	TOKO
13	2	L4,L2	4.7nH	LL1608-F4N7K	TOKO
14	1	L5	15nH	LL2012FH15NJ	TOKO
15	1	L6	DNP	DNP	TOKO
16	2	Q1,Q2	BFR520	BFR520	Philips
17	2	R1,R3	2K	ERJ3GSYJ202	Panasonic
18	1	R2	51	ERJ3GSYJ510	Panasonic
19	2	R4,R12	221	ERJ3EKF2210	Panasonic
20	6	R5,R6,R8,R13,R14,R16	33.2K	ERJ3EKF3322	Panasonic
21	2	R9,R17	DNP	ERJ3EKF1001	Panasonic
22	2	R10,R18	249	ERJ3EKF2490	Panasonic
23	2	R11,R19	10	ERJ3GSYJ100	Panasonic
24	1	U1	D2D_V4	D2D_V4	Parker Vision
25	1	U2	1X603	1X603	Anaren
26	1	U3	AD8032AR	AD8032AR	Analog Devices

27 1

Based

ST8500.6A1.001 V03.00

FIG. 54



SYNTHESIZER	ST8500-532
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FT. S.S.

MAY 26, 1961

12/8

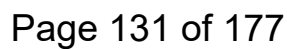
FIG. 56A

32	1	R14	220	Resistor, 220 ohm, 5%, 0603	ERJ3GSYJ221	Panasonic
33	1	R15	DNP	Resistor, zero ohm, 0603	ERJ3GSY0R00	Panasonic
34	2	R18,R19	DNP	Resistor, 91 ohm, 5%, 0603	ERJ3GSYJ910	Panasonic
35	1	R36	TBD	Resistor, zero ohm, 0603	ERJ3GSY0R00	Panasonic
36	1	R37	DNP	Resistor, , , 0603		Panasonic
37	1	TP1	Test Point			
38	1	U1	PE3282A	IC, Synthesizer	PE3282A	Peregrine
39	1	U2	CXO-3M-10N-40MHz	Xtal Osc, 40MHz	CXO-3M-10N-40MHZ A/I	Statek
40	1	U4	TK11233AMTL	Voltage Regulator, 3.5V	TK11235BM	Toko
41	1	U5	74125	IC, BUFFER	MC74LCX125DT	Motorola
42	1	U6	UPC1678GV	IC, RF Amplifier	UPC1678GV	NEC

43 1 STB500.641.00B Board

V02.00

FIG. 56B



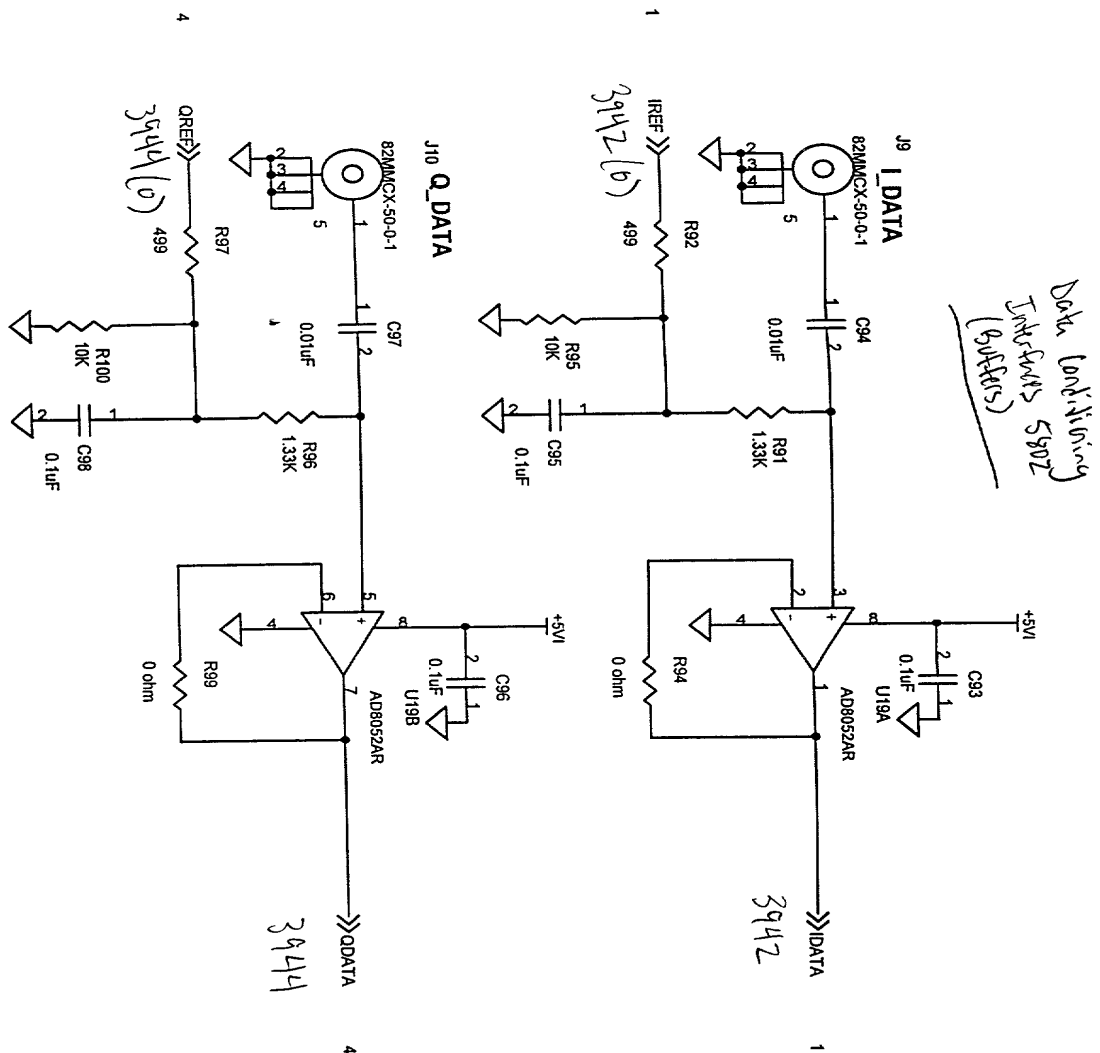


FIG. 58

50447129.000400

Signal Technologies Inc.

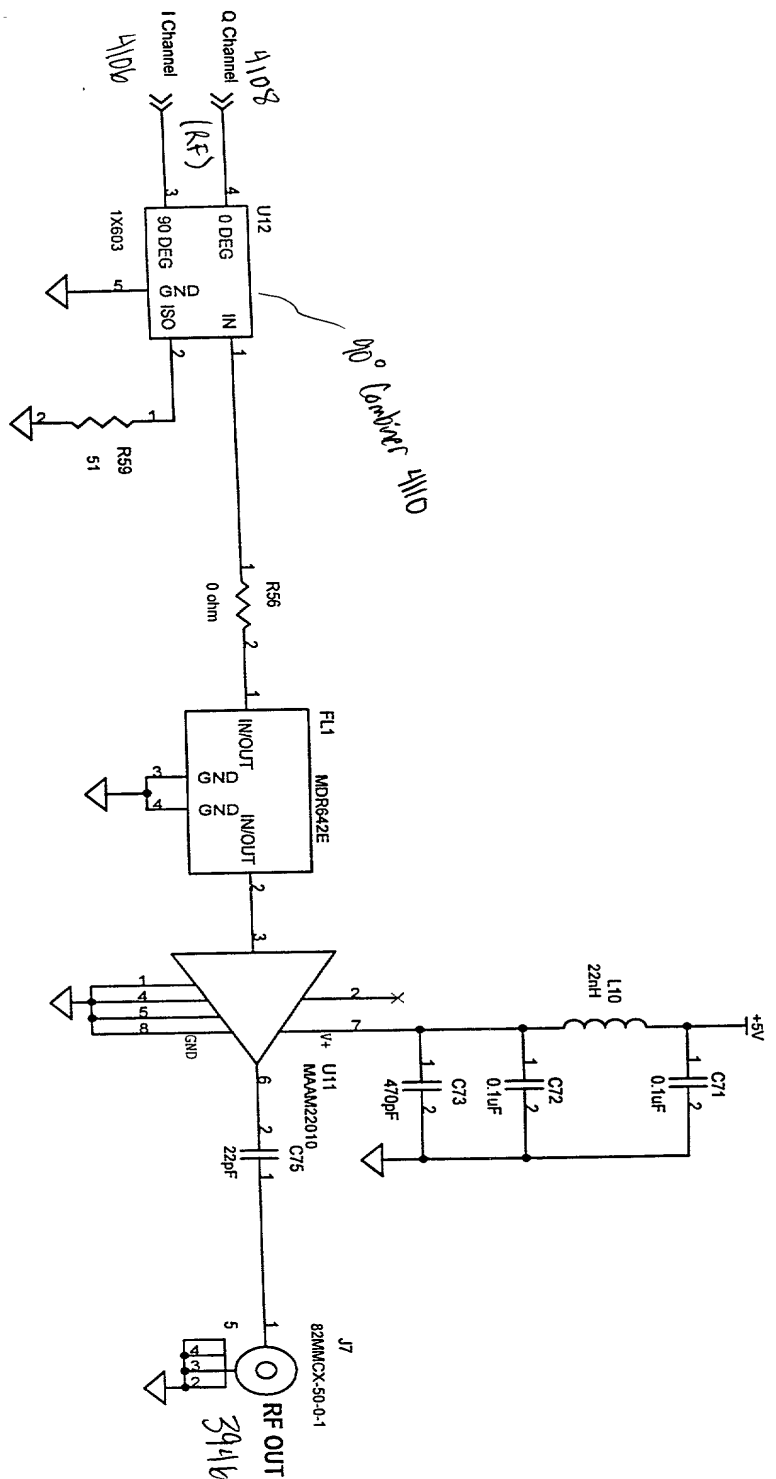
Title OPSK I and Q INPUTS

Size Document Number
A ST8500-532-021 V06.00

Date Monday, July 26, 1999

Sheet 2 of 4

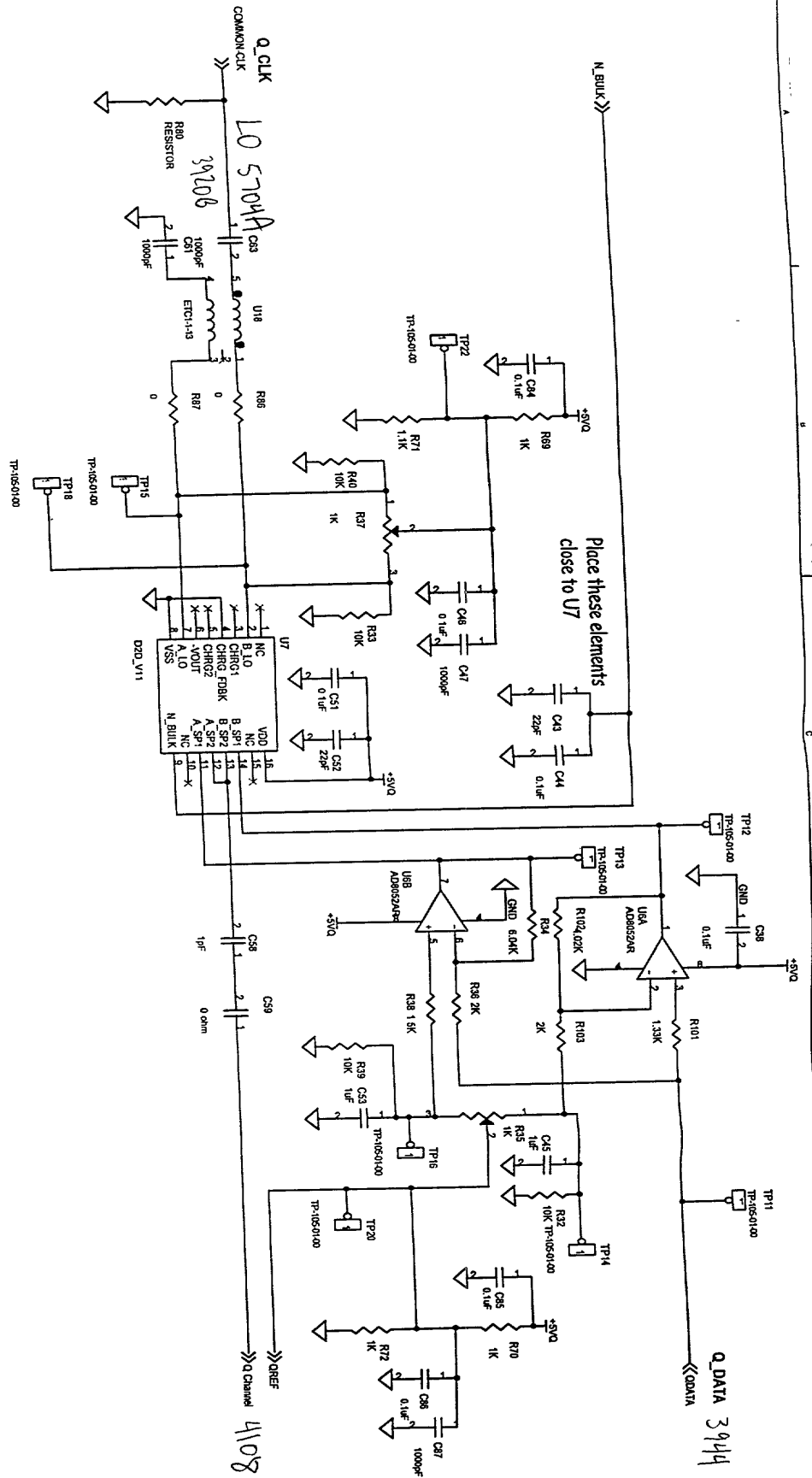
Rev F



FL6.59

60447420-1000499

Signal Technologies Inc.	
Title	Combiner / RF Out
Size	Document Number
A	ST8500-532-021 V06.00
Date:	Monday, July 26, 1999
Sheet	3 of 4
Rev	F



Signal Technologies Inc.

Page1

Bill Of Materials July 27,1999 9:51:54

Item	Quantity	Reference	Part	Part Number	Manufacturer
1	21	C3,C6,C8,C10,C14,C38,C44, C46,C51,C71,C72,C77,C78, C79,C84,C85,C86,C93,C95, C96,C98	0.1uF	GRM39X7R104K016	Murata
2	6	C5,C7,C15,C43,C52,C75	22pF	GRM39COG220J050	Murata
3	5	C9,C16,C45,C53,C89	1uF	GRM40Y5V105Z016	Murata
4	8	C11,C23,C25,C47,C61,C63, C80,C87	1000pF	GRM39X7R102K050	Murata
5	2	C58,C21	1pF	GRM39COG010B50V	Murata
6	2	C82,C33	4.7uF	T491A475K006AS	KEMET
7	2	C59,C35	0 ohm	GRM39COGxxx50V	Murata
8	1	C73	470pF	GRM39COG471J050	Murata
9	1	C83	1uF	T491A105M016AS	Kemet
10	3	C90,C91,C92	100pF	ECU-V1H101JCV	
11	2	C94,C97	0.01uF	GRM39X7R103K016	Murata
12	1	FL1	MDR642E	MDR642E	Soshin
13	1	JP1	Shunt	69190-402	BERG
14	1	JP2	69190-403	69190-403	BERG
15	4	J7,J8,J9,J10	82MMCX-50-0-1	82MMCX-50-0-1	Suhner
16	1	L10	22nH	LL1608-F22NK	Coilcraft
17	1	L12	BLM11A121S	BLM11A121S	Murata
18	1	L13	330nH	LL2012-FR33K	
19	10	R5,R6,R12,R13,R32,R33, R39,R40,R95,R100	10K	ERJ3EKF1002	Panasonic
20	2	R34,R7	6.04K	ERJ3EKF6041	Panasonic
21	4	R8,R10,R35,R37	1K	3224W-1-102	Bourns
22	4	R9,R36,R90,R103	2K	ERJ3EKF2001	Panasonic
23	2	R38,R11	1.5K	ERJ3EKF1501	Panasonic
24	3	R56,R94,R99	0 ohm	ERJ3GSY0R00	Panasonic
25	1	R59	51	ERJ3GSYJ510	Panasonic
26	7	R60,R61,R62,R84,R85,R86, R87	0	ERJ3GSY0R00	Panasonic
27	6	R63,R64,R66,R69,R70,R72	1K	ERJ3EKF1001	Panasonic
28	2	R71,R65	1.1K	ERJ3EKF1101	Panasonic
29	2	R80,R79	RESISTOR		
30	3	R81,R82,R83	R		
31	4	R88,R91,R96,R101	1.33K	ERJ3EKF1331	Panasonic
32	2	R102,R89	4.02K	ERJ3EKF4021	Panasonic
33	2	R92,R97	499	ERJ3EKF4990	Panasonic
34	19	TP1,TP2,TP3,TP4,TP5,TP6,	TP-105-01-00		

FIG. b1A

		TP8,TP9,TP11,TP12,TP13,			
		TP14,TP15,TP16,TP18,TP19,			
		TP20,TP21,TP22			
35	3	U1,U6,U19	AD8052AR	AD8052AR	Analog Devices
36	2	U7,U2	D2D_V11	D2D_V11	Parker Vision
37	1	U11	MAAM22010	MAAM22010	MACOM
38	1	U12	1X603	1X603	Anaren
39	1	U14	AD1582	AD1582	Analog Devices
40	1	U15	UPG1678	UPG1678GV	NEC
41	1	U16	ADP-2-10-75	ADP-2-10-75	Mini-Circuits

42 1

BOARD

B500.641.021 V05.10

FIG. 61B

From PCMCIA Connector Ribbon

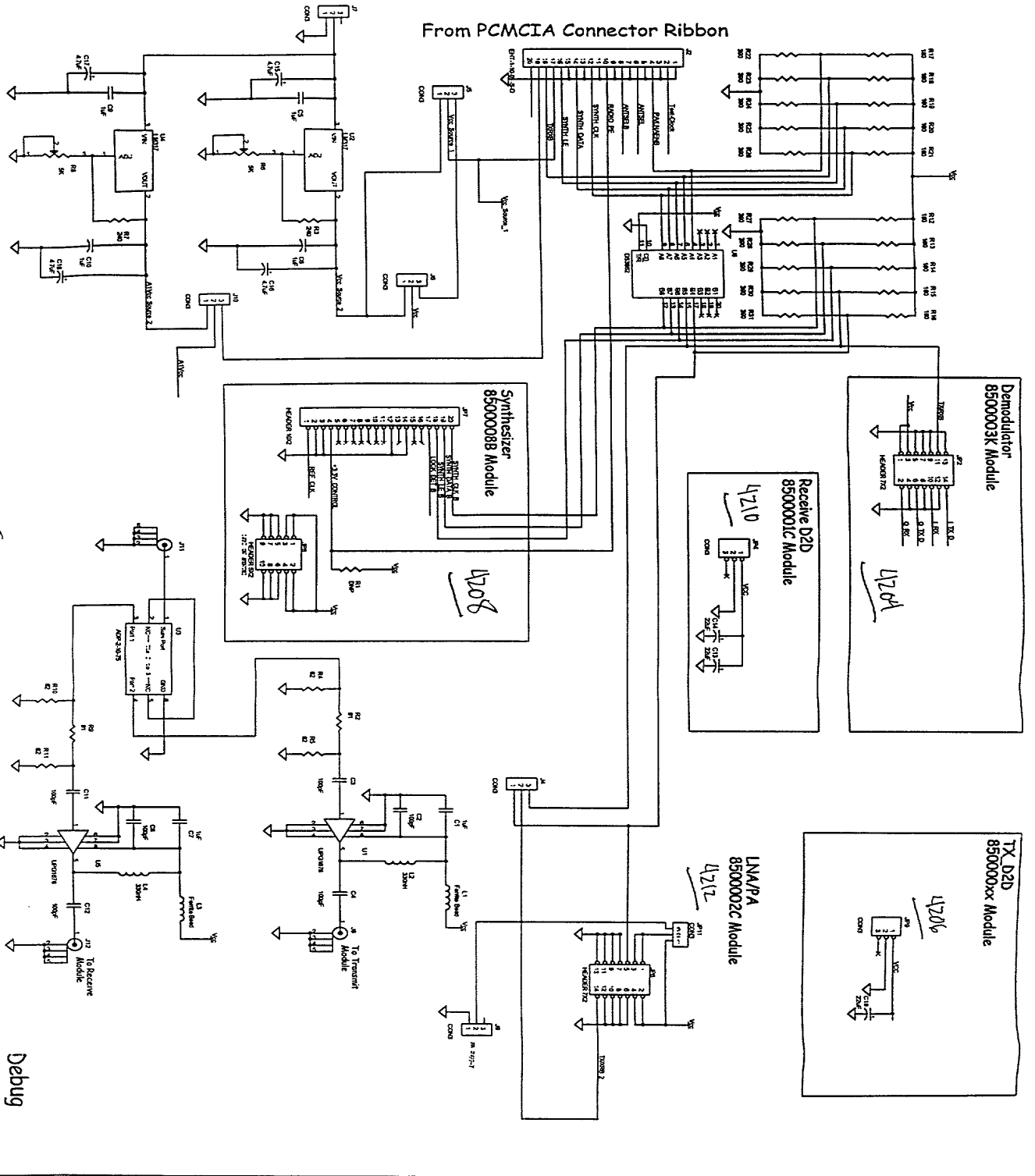
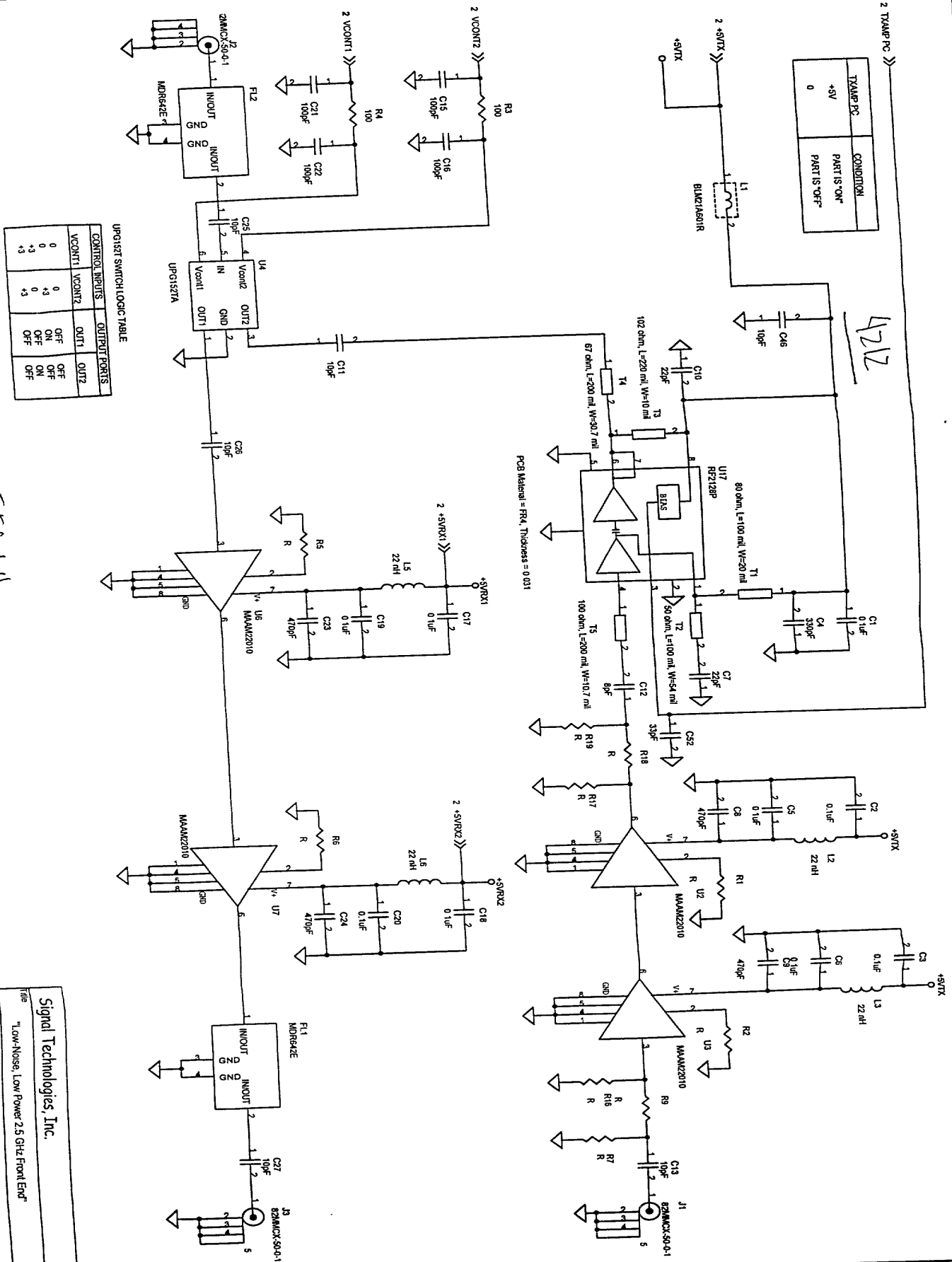


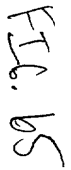
FIG. 62

MOTHER BOARD FOR PCMCIA TEST BED

Debug

50447129-000000

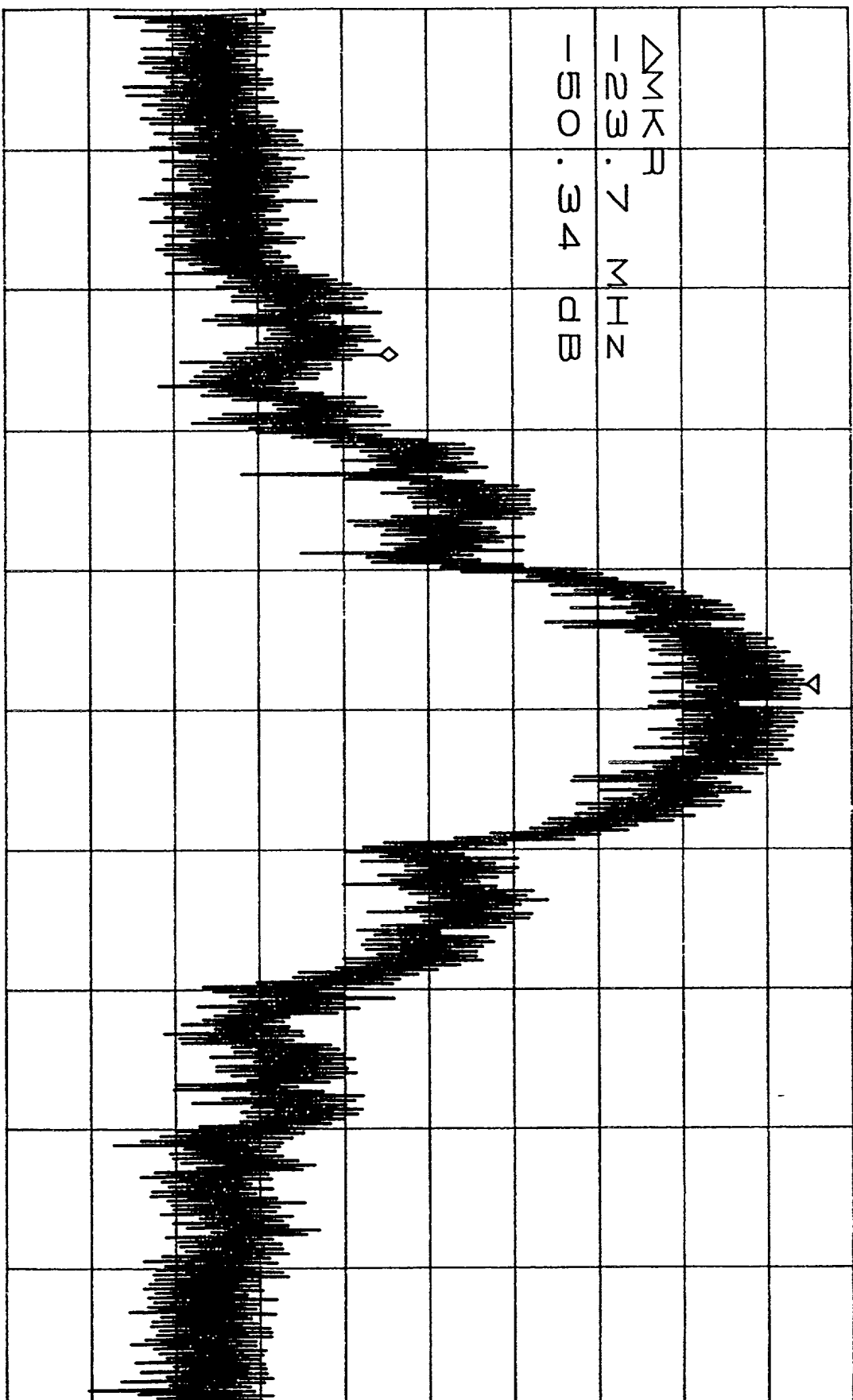


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Aug 1992 08:10:14.70 VOM (211.35, 4=12.6 dBm) TX #1 #00566

FIG. 68

*ATTEN 20dB
RL 5.0dBm 10dB/ Δ MKR -50.34dB



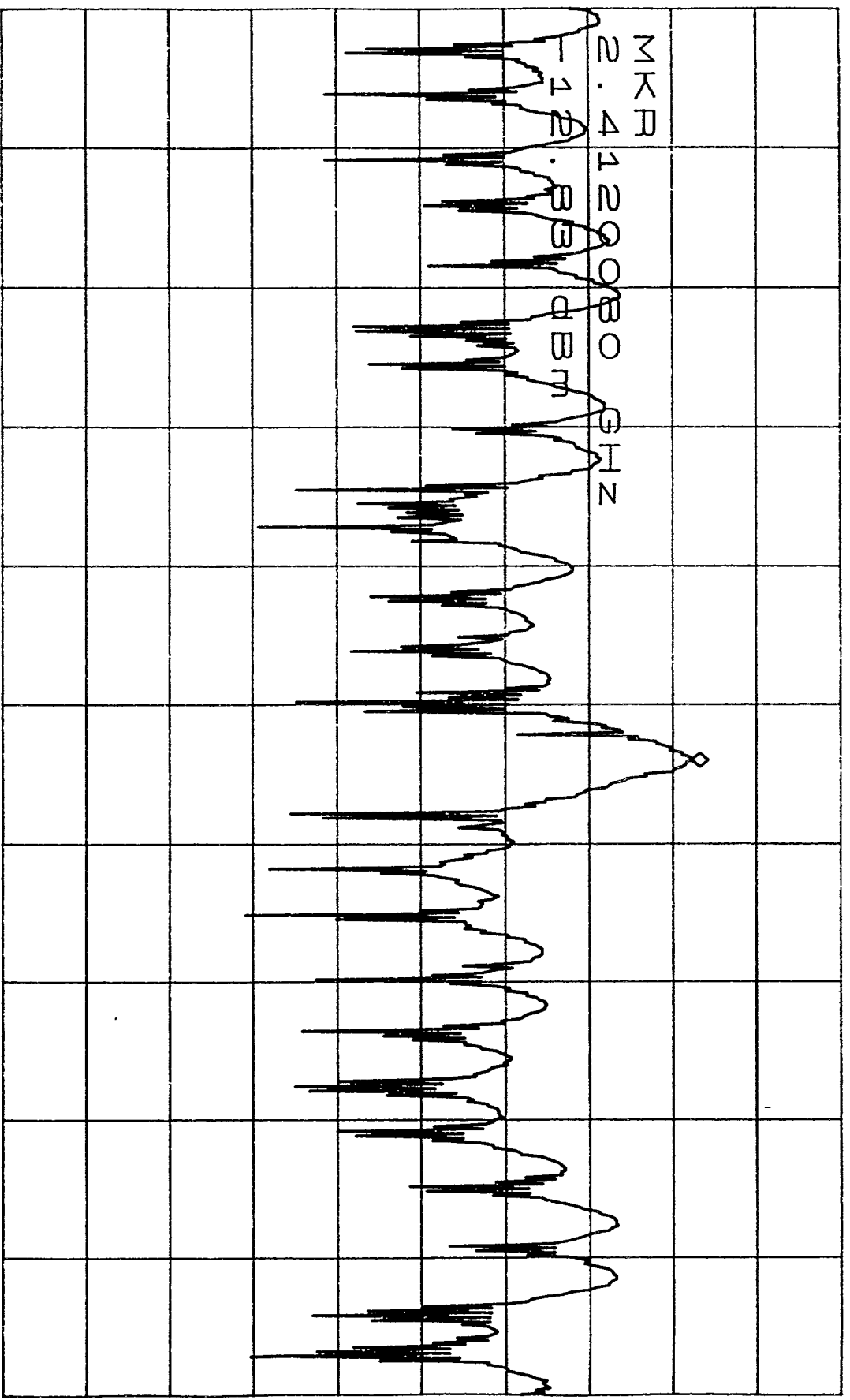
CENTER 2.4120GHz SPAN 100.0MHz
*RBW 100kHz *VBW 30kHz SWP 84.0ms

50447429.000000

2.412000 GHz $\Delta f = 14.72 \text{ dBm}$ ($\Delta f = 11.35 \text{ dBm}$, $I = 12.21 \text{ dBm}$) TX #1 #00568

FIG 69

*ATTEN 20dB
 RL 5.0dBm
 10dB/
 MKR -12.83dBm
 2.4120080GHz



CENTER 2.412000GHz
 RBW 3.0KHz
 *VBW 30KHz
 SPAN 200.0KHz
 SWP 67.0ns

50.447429 - 0.000000

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99

*ATTEN 20DB
RL 5.0DBM
10DB/
-134.10MHZ

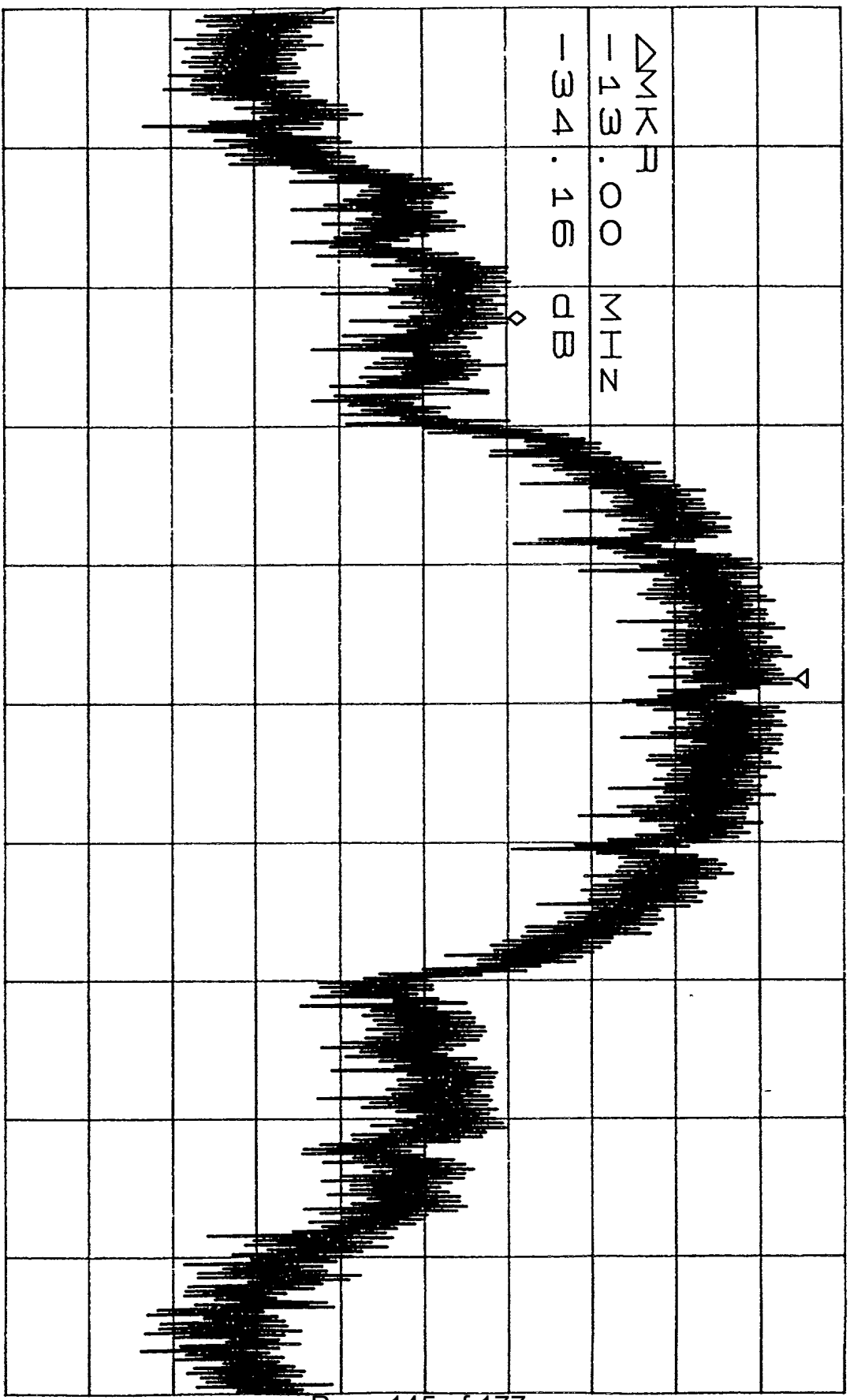


Fig 70

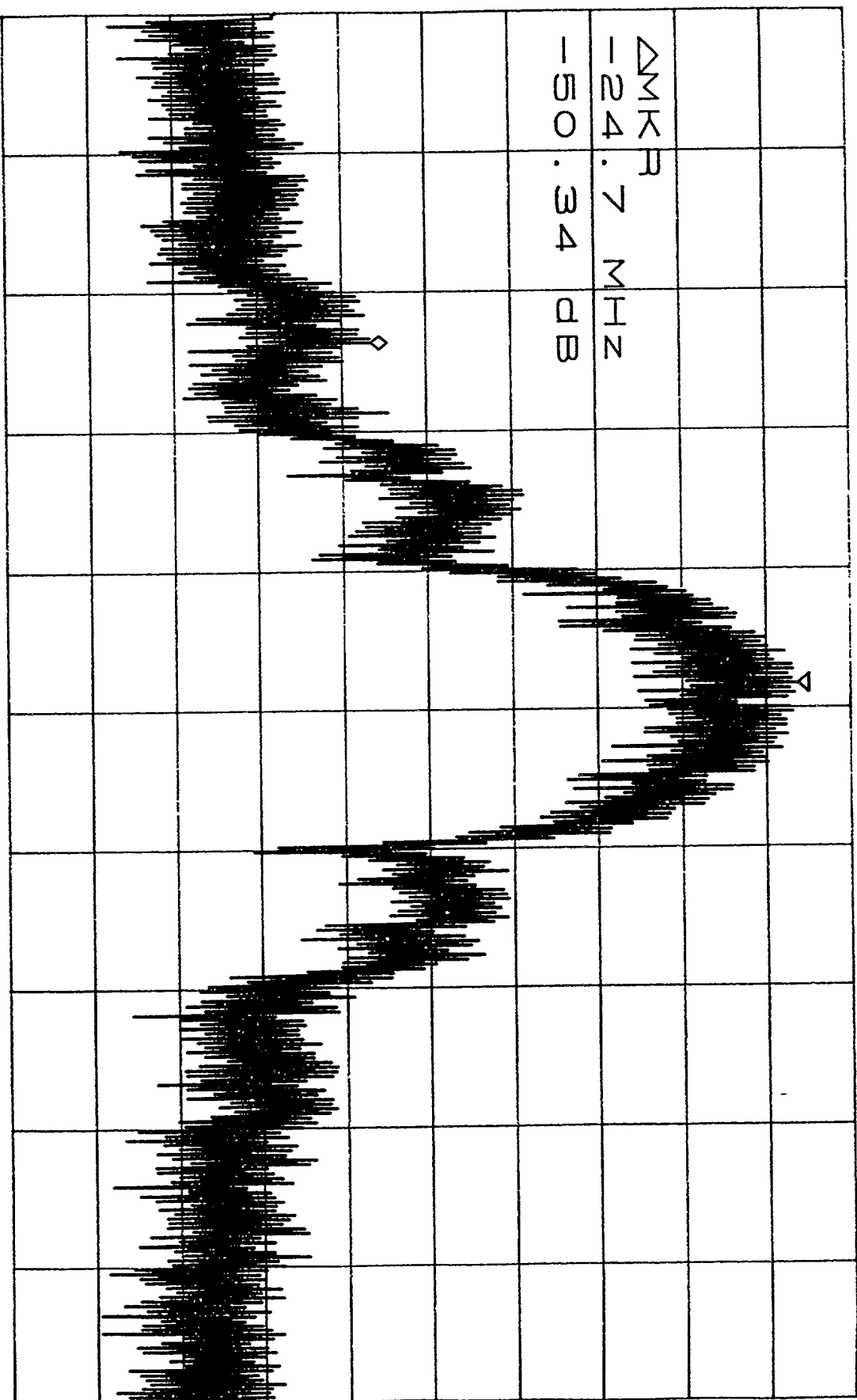
CENTER 2.43200GHZ
*RBW 100KHZ
*VBW 30KHZ
SPAN 50.00MHZ
SMP 50.0MS

13447429.1344499

Amplitude: 10.7 dBm (2 = 10.5 dBm, 1 = 11.3 dBm) TX #5 4 00568

FIG. 71

*ATTEN 20dB
RL 5.0dBm
10dB/
ΔMKR -50.34dB



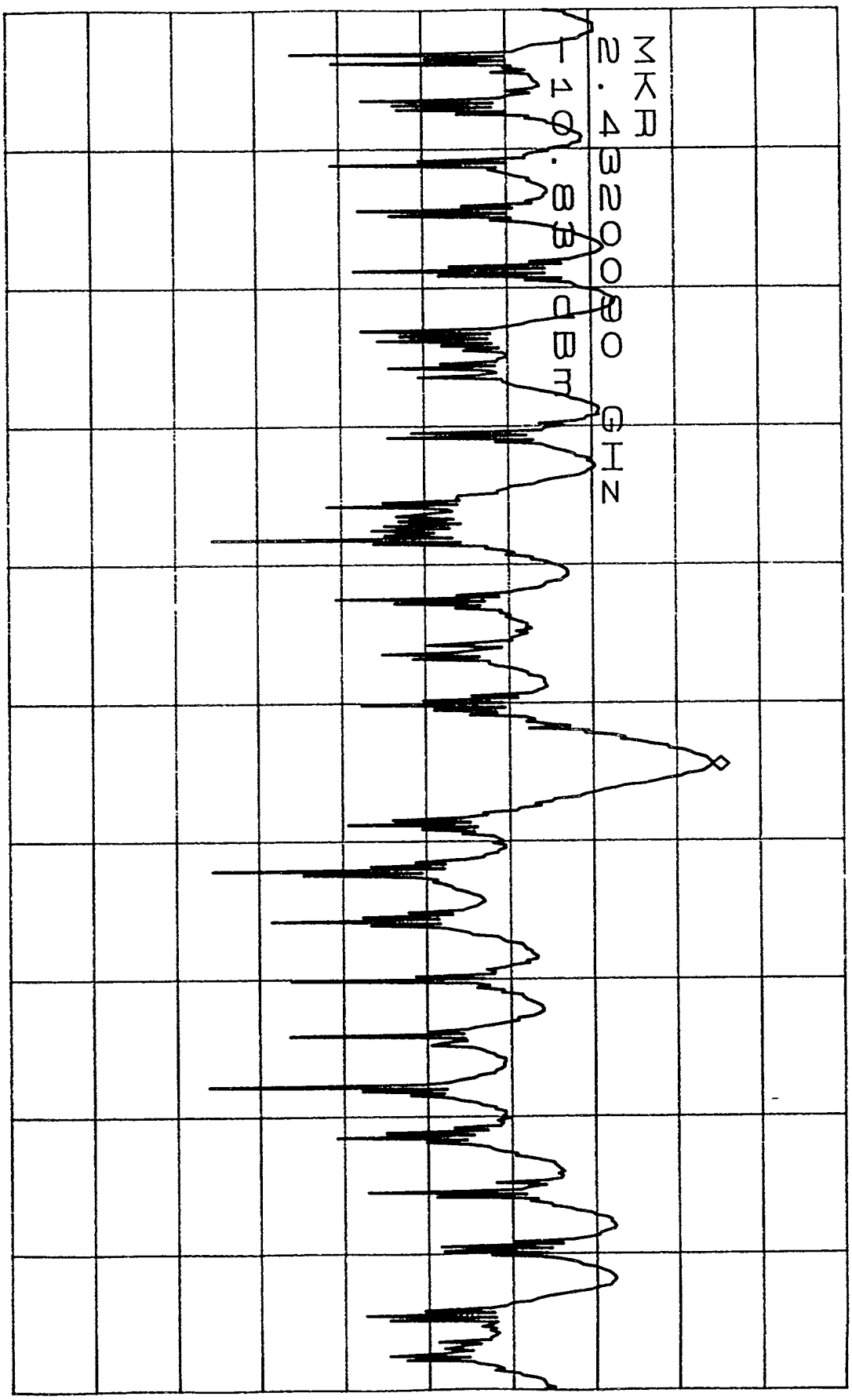
CENTER 2.43206GHz
*RBW 100KHz *VBW 30KHz
SPAN 100.0MHz
SMP 84.0ms

60447429 020449

2.4320090GHz, L = 11.35dBm, TX #5 400568

FIG. 72

*ATTEN 20dB
 RL 5.00dBm
 10dB/
 MKR -10.83dBm
 2.4320090GHz



CENTER 2.432000GHz
 RBW 3.0KHz
 *VBW 30KHz
 SPAN 200.0KHz
 SWP 67.0FS

63447423 030449

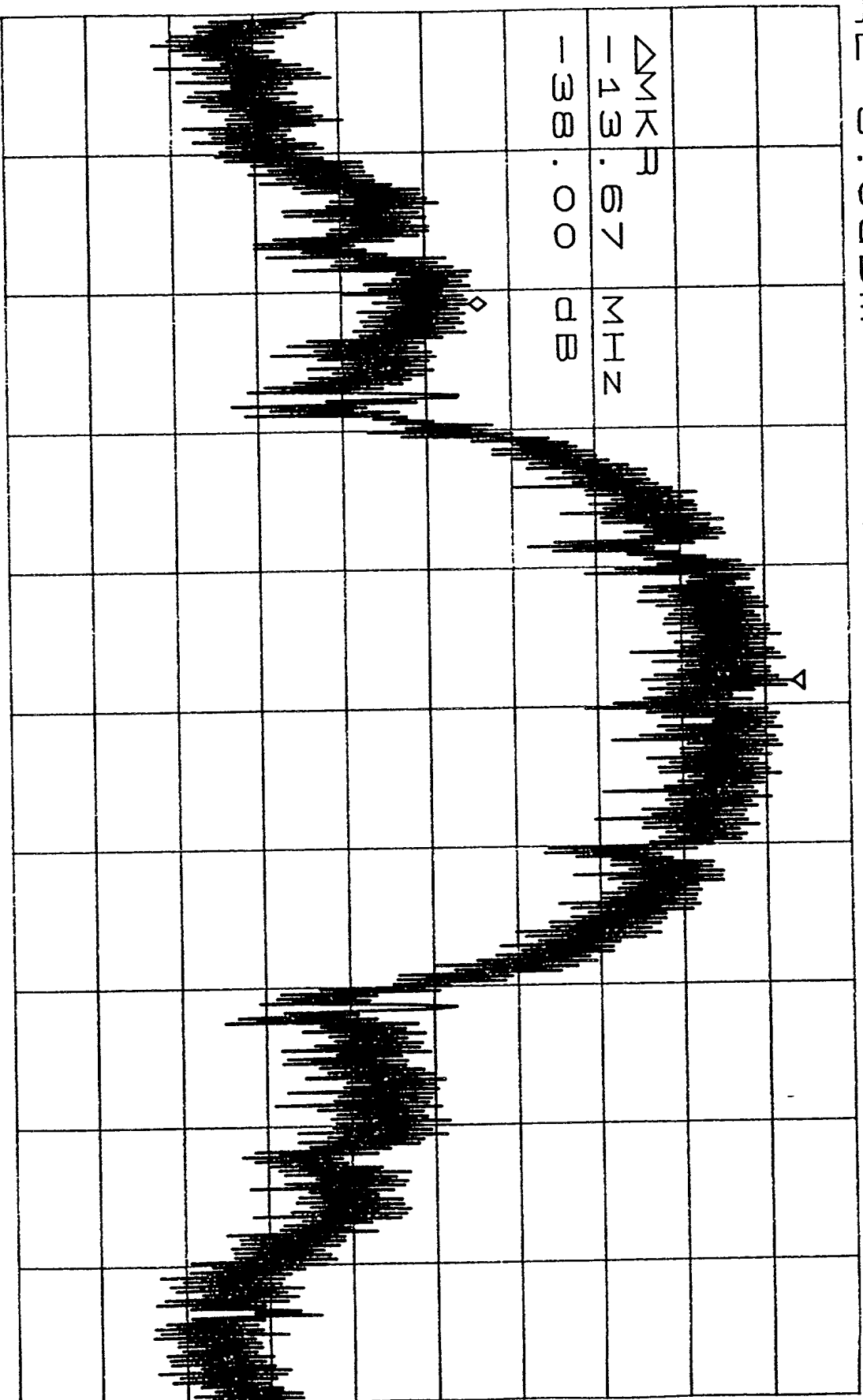
FIG. 73

$\lambda = 1999$ $P_0 = 12.8 \text{ dBm}$ ($G = 9.4 \text{ dBm}$, $I = 10.0$ m) $T_X = 11$ 70568

*ATTEN 20dB
RL 5.00dB

10dB/

$\Delta \text{MKR} - 38.00 \text{ dB}$
 $- 13.67 \text{ MHz}$



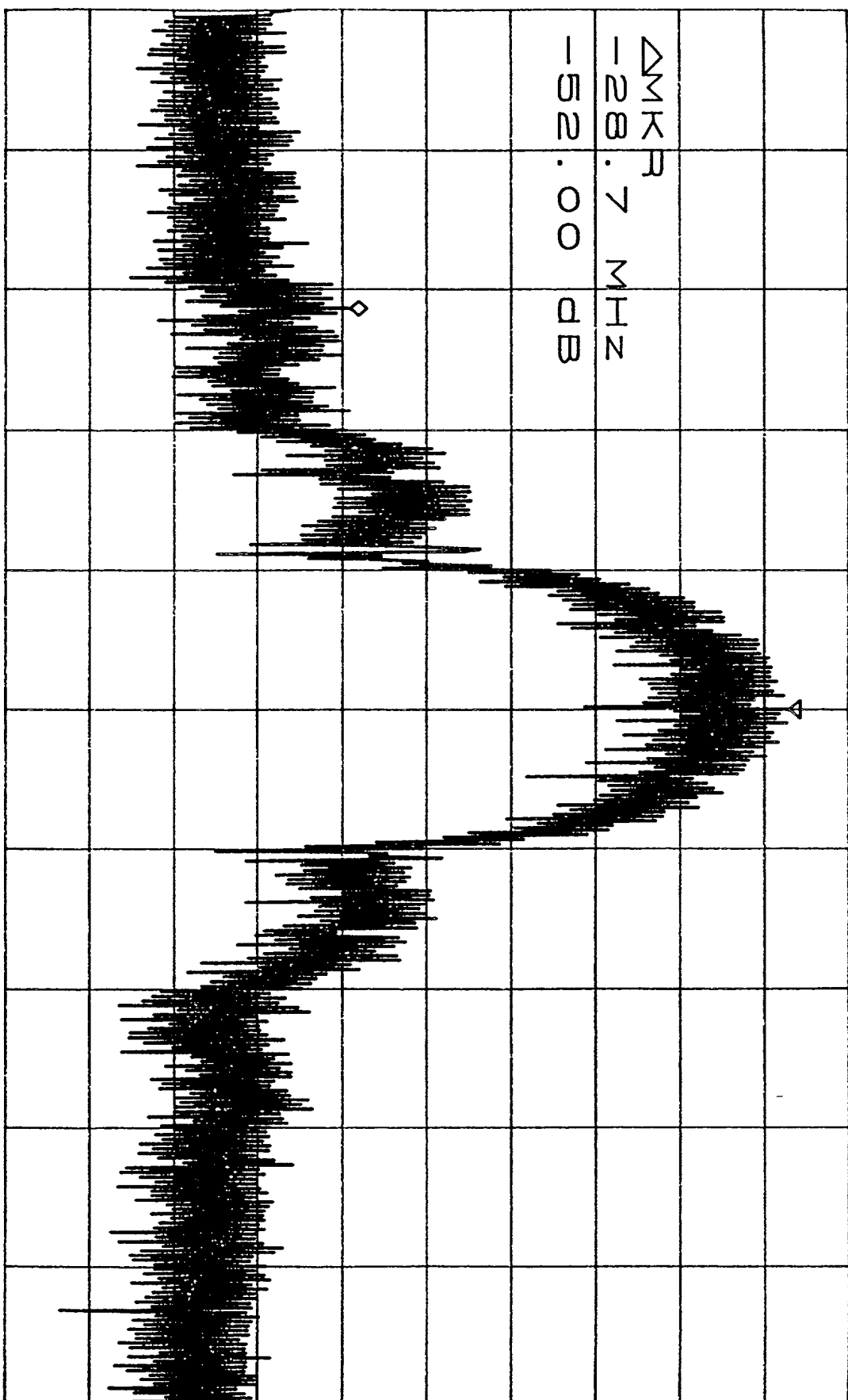
CENTER 2.46200GHz SPAN 50.00MHz
*RBW 100Hz *VBW 30Hz SWP 50.0ms

63447429.083449

2 / 1999 $P_0 = 12.9 \text{ dBm}$ ($Q = 9.4 \text{ dBm}$, $\bar{I} = 10.0 \text{ dB}$) $\backslash$ TX # 11 # 00568

*ATTEN 20dB RL 5.0dBm 10dB/ $\Delta \text{MKR} - 52.00 \text{ dB}$

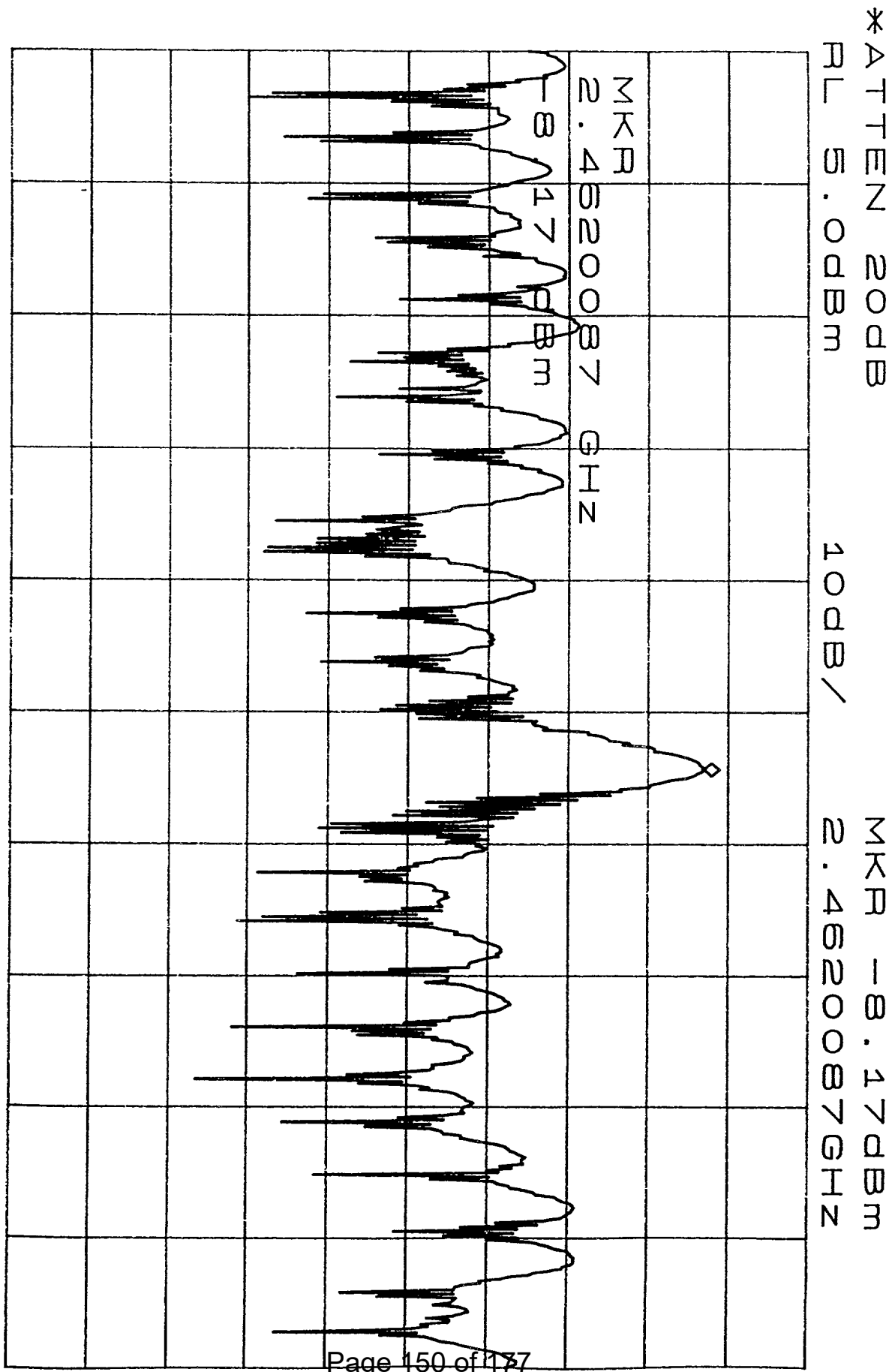
FIG. 74



CENTER 2.4620GHz *RBW 100kHz *VBW 30kHz SPAN 100.0MHz
 *RBW 100kHz *VBW 30kHz SMD 84.0ms

2 Aug 1999 $P_0 = 12.8 \text{ dBm}$ ($G = 9.4 \text{ dBm}$, $I = 10.0 \text{ dBm}$) TX#11 #00568

FIG. 75

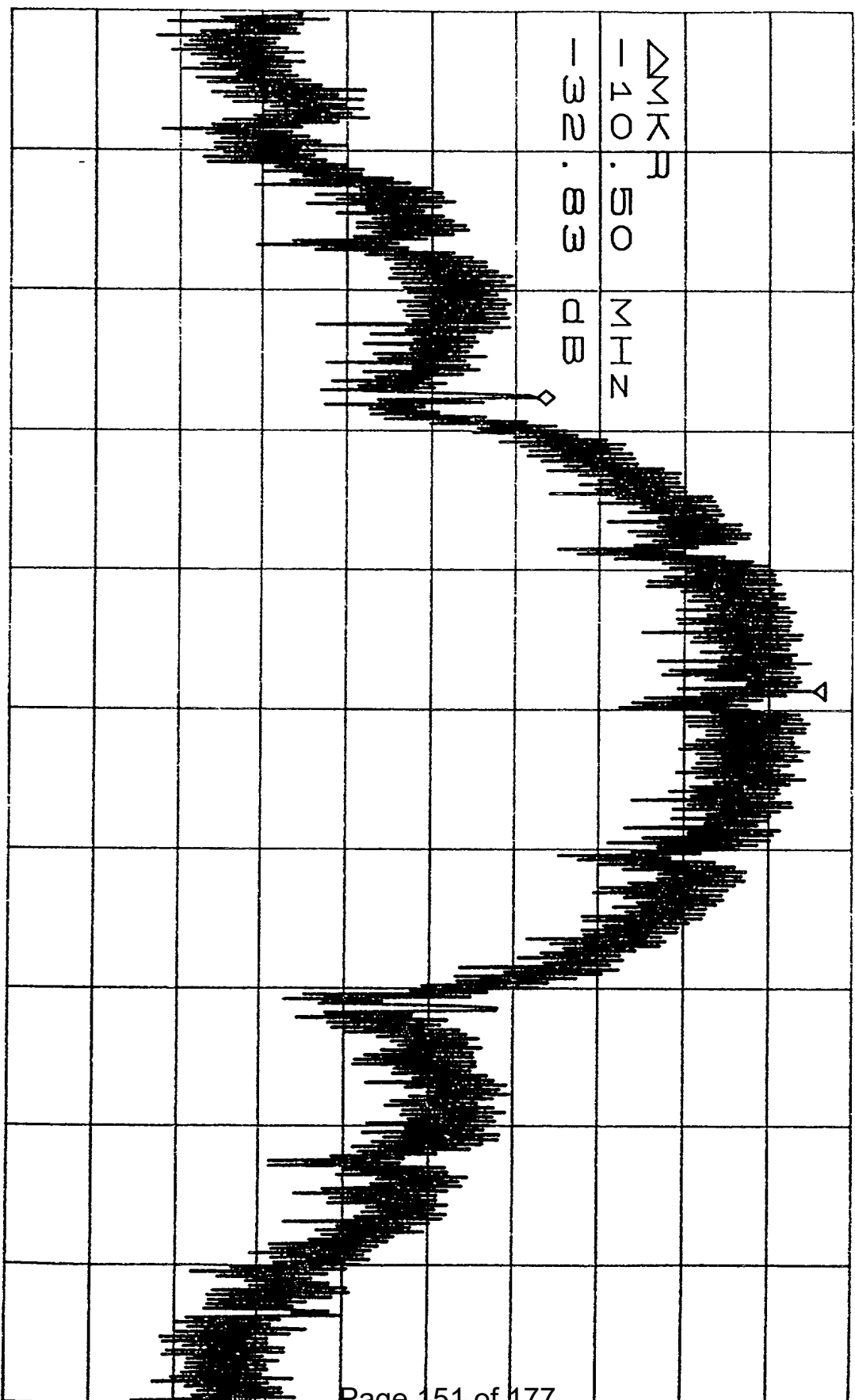


CENTER 2.46200087GHZ
 RBW 3.0KHZ *VBW 30KHZ
 SPAN 200.0KHZ
 SWP 67.0ms
 10.447429 - 10.4499

Aug 1995 10:00:00 AM, L = 14.000000, CH#1 TX#2 #00570

FIG. 76

*ATTEN 20dB
 RL 5.00dB
 10dB/
 ΔMKR -32.83dB



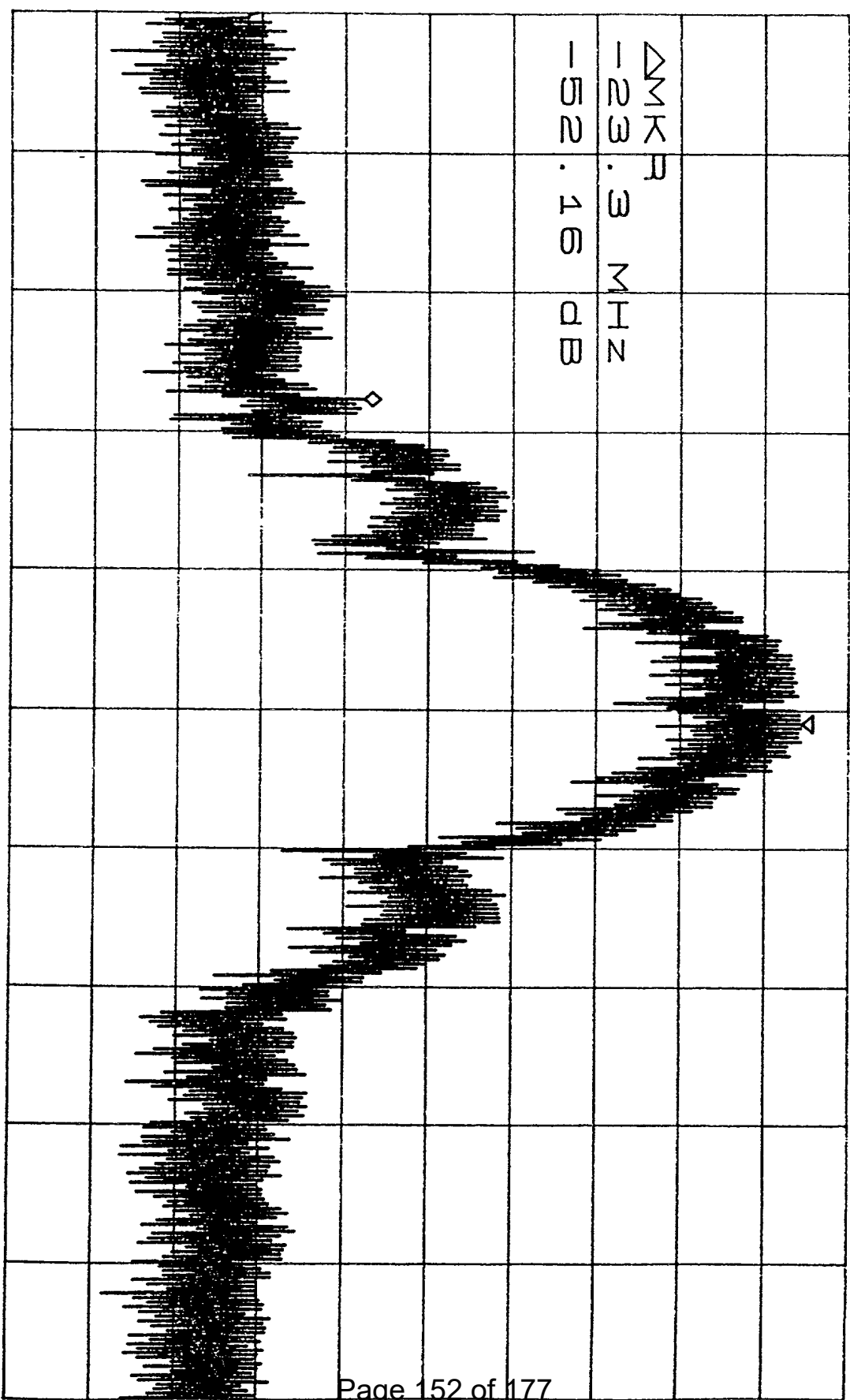
CENTER 2.412000GHZ
 *RBW 100KHZ
 *VBW 30KHZ
 SPAN 50.000MHZ
 SWP 50.00ms

SEP 14 1995 10:00:00 AM

2 Aug 1988 15:17:28 (Q=11.7dBm, I=12.6dBm) CH#1 TX#2 #00570

FIG. 77

*ATTEN 20dB
 RL 5.0dBm
 10dB/
 ΔMKR -52.16dB



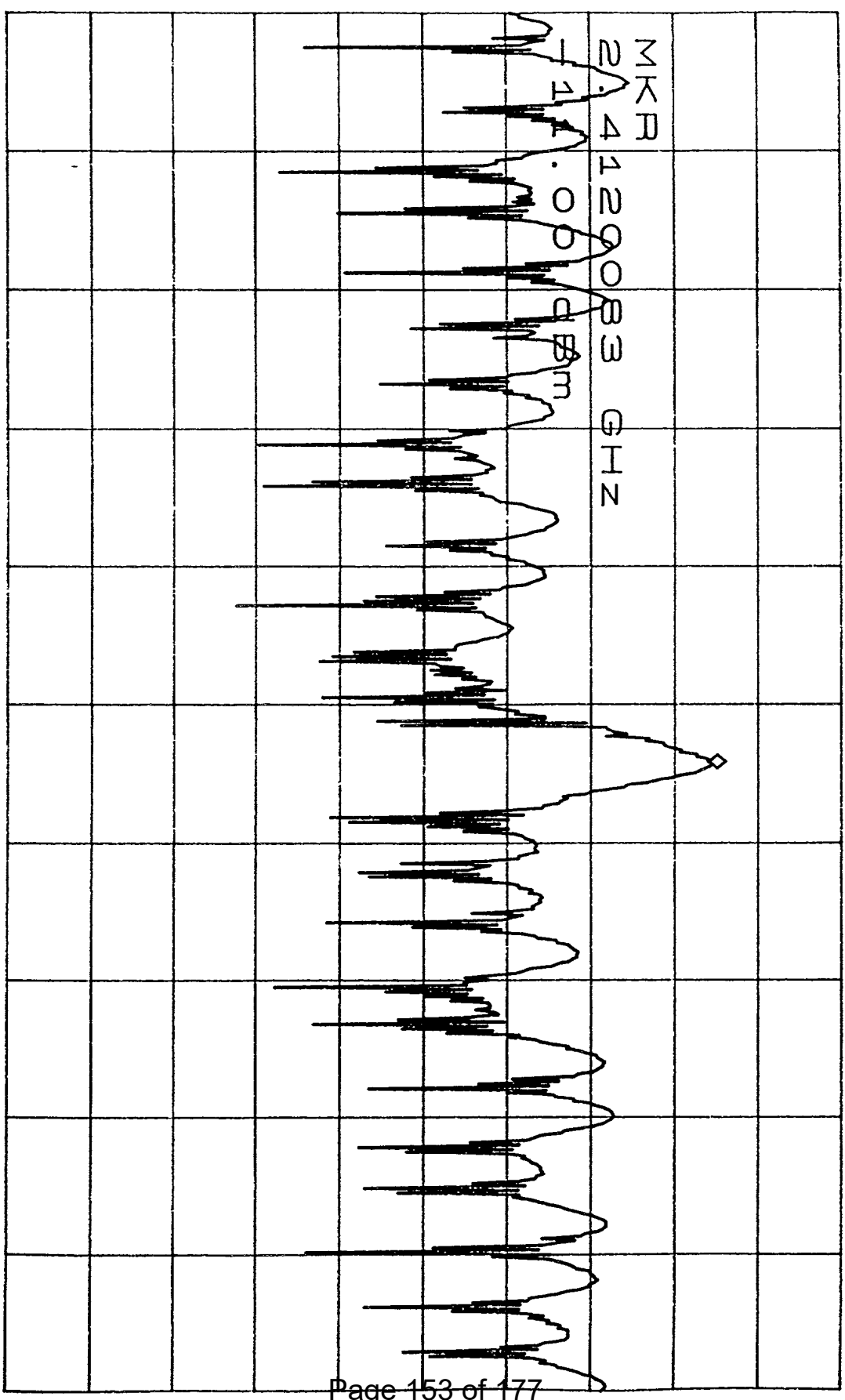
CENTER 2.4120GHz
 *RBW 100kHz
 *VBW 30kHz
 SPAN 100.0MHz
 SWP 84.0ms

68447429.080499

2.4120083 GHz 10 dBm 2.4120083 GHz 10 dBm 2.4120083 GHz 10 dBm

FIG. 78

*ATTEN 20dB
RL 5.0dBm
10dB/
MKR -11.00dBm
2.4120083GHz

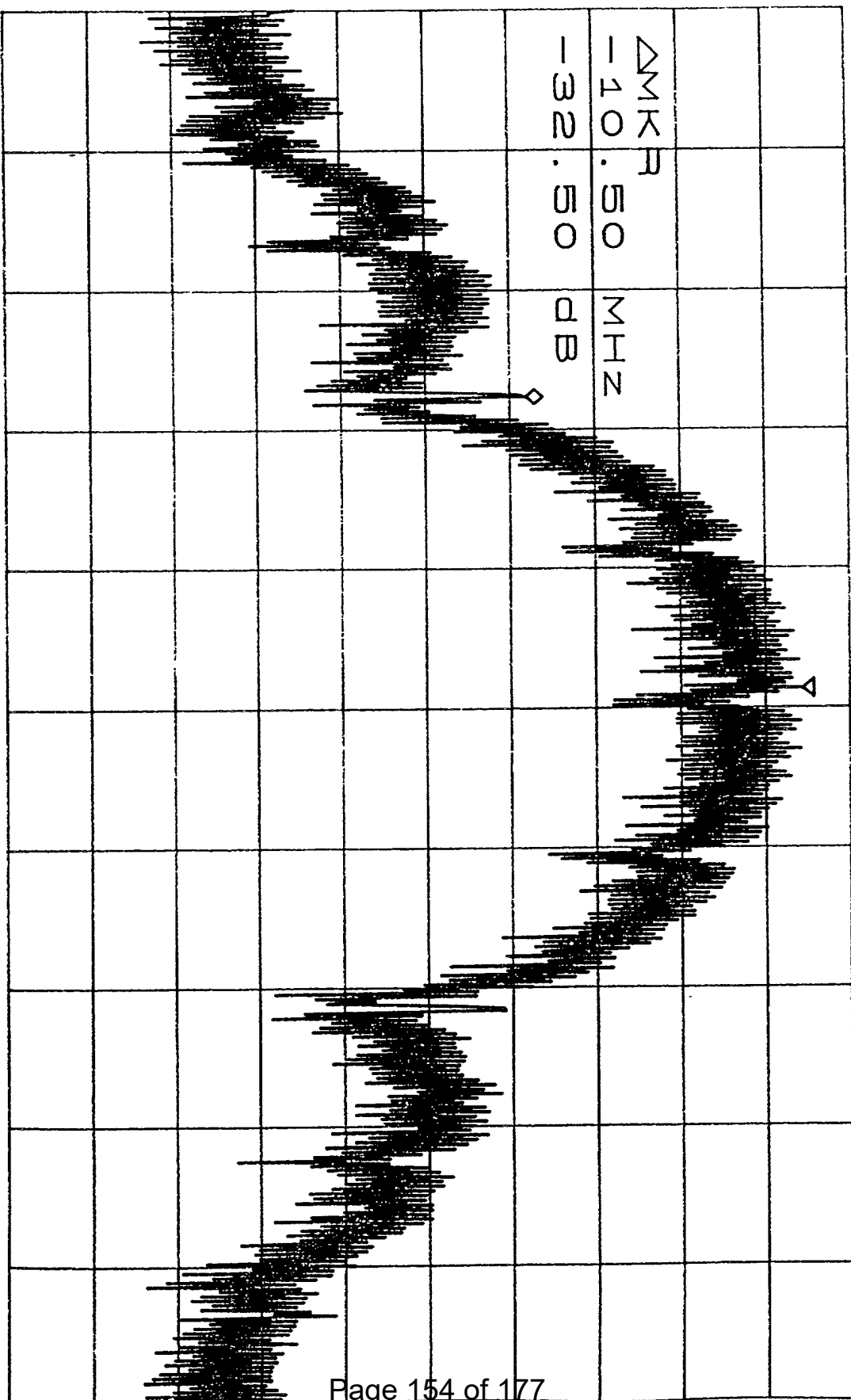


CENTER 2.4120000GHz
RBW 3.0KHz
*VBW 30KHz
SPAN 200.0KHz
SMP 67.0ms

CH #5 1KHz #00570

FIG. 79

*ATTEN 20dB
RL 5.0dBm 10dB/ Δ MR 132.50dB

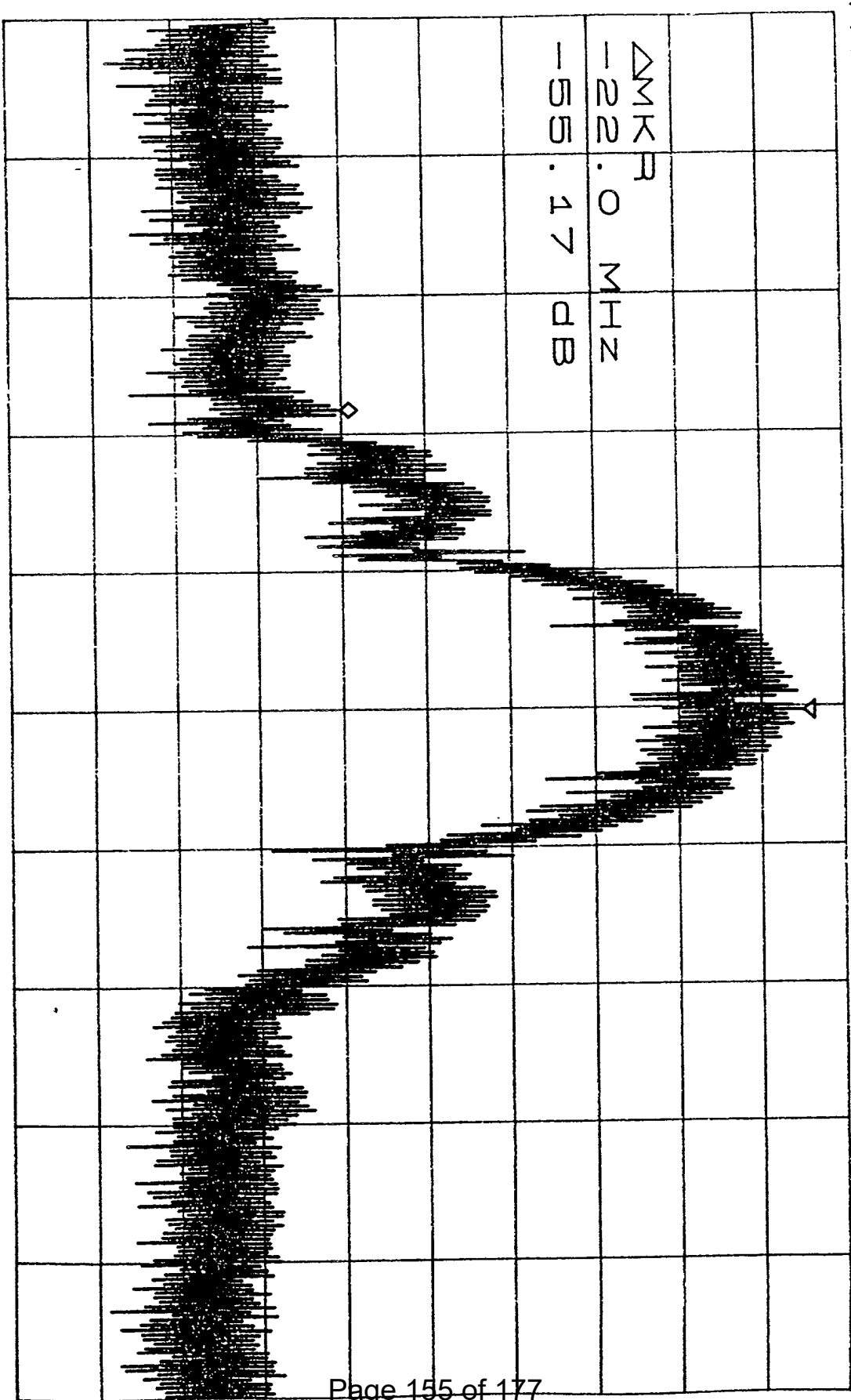


CENTER 2.43200GHz SPAN 50.00MHz
*RBW 100KHz *VBW 30KHz SWP 50.0ms

2. 11/18/1995 10:14.4 dBm CLK: 11.6 dBm, L: 12.0 dBm) CH#5 TX#2 #00510

FIG 80

*ATTEN 20dB
 RL 5.0dBm
 10dB/
 -22.0MHz
 ΔMKR -55.17dB

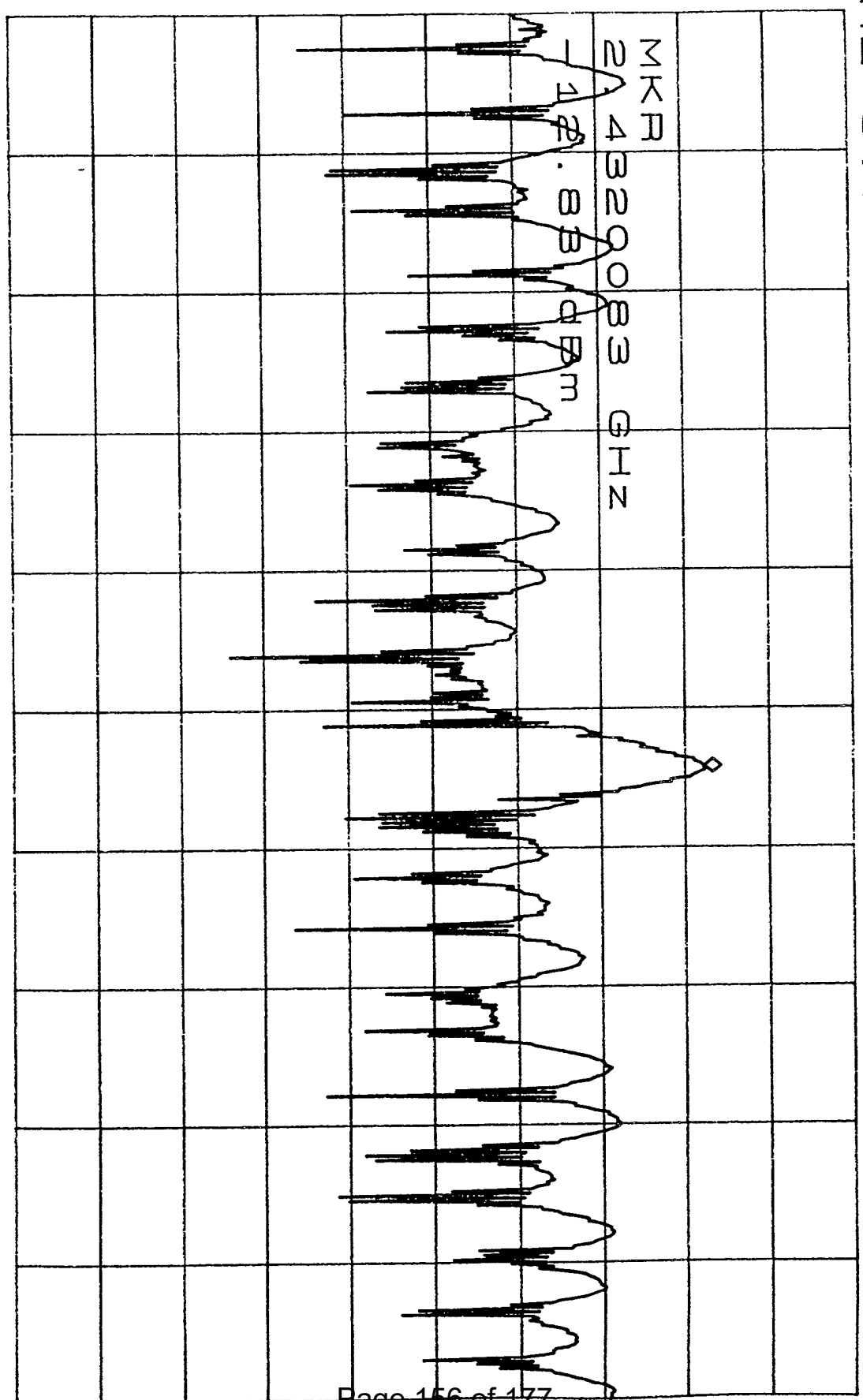


CENTER 2.4320GHz
 *RBW 100kHz
 *VBW 30kHz
 SPAN 100.0MHz
 SWP 84.0ms

my test is in the 100 MHz to 1 GHz range (CH#5 FX#2 400520)

FIG. 81

*ATTEN 20dB
RL 5.0dBm
10dB/
MKR -12.83dBm
2.4320083GHz



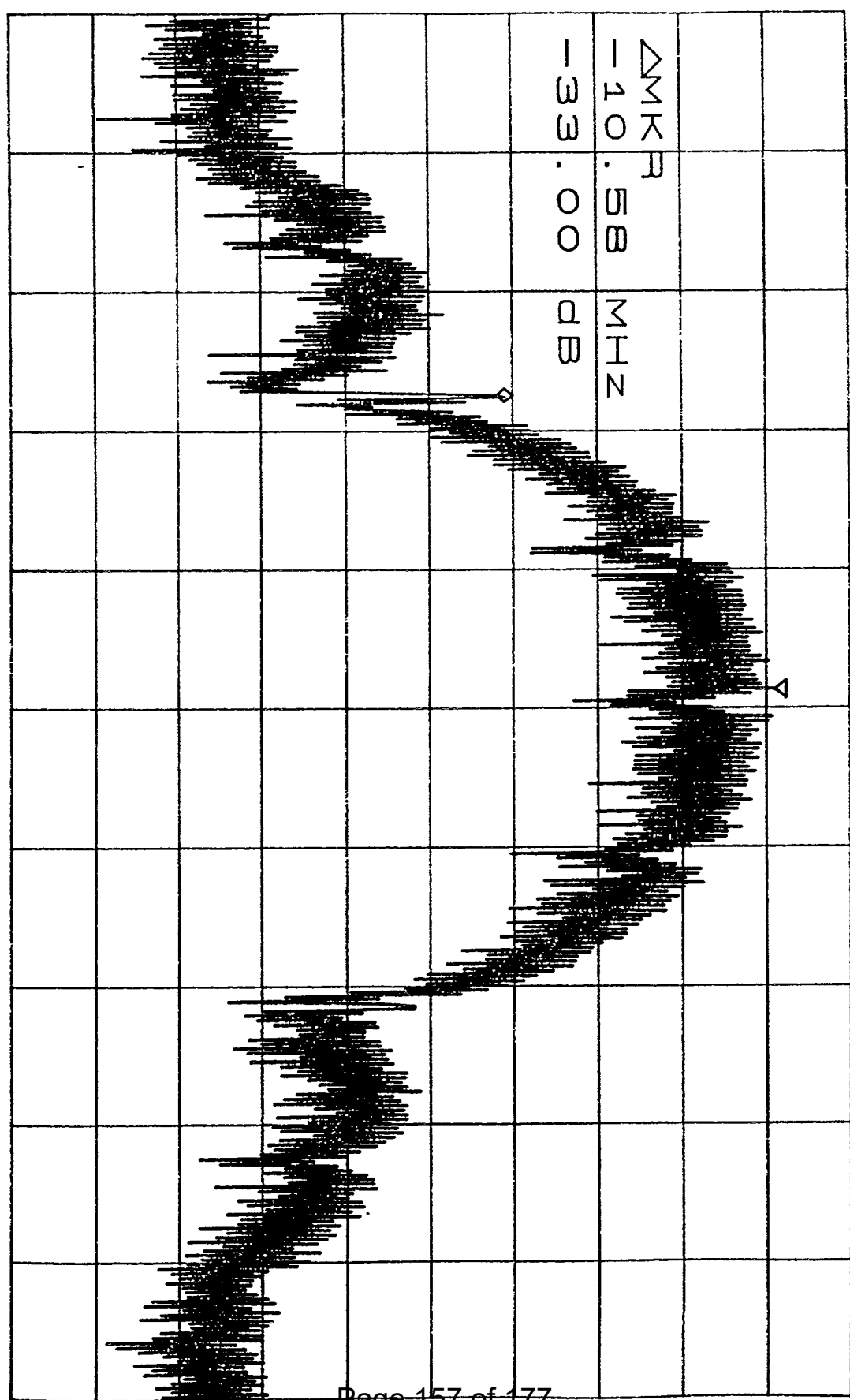
CENTER 2.4320000GHz
SPAN 200.0KHz
RBW 3.0KHz
SMP 67.0ms

63447429 03040403

Aug 1988 to 12/19/88 (approx) CH#11 TX#2 #00576

FIG. 82

*ATTEN 20dB
 RL 5.00dB
 10dB/
 -10.58MHz
 ΔMKR -33.00dB



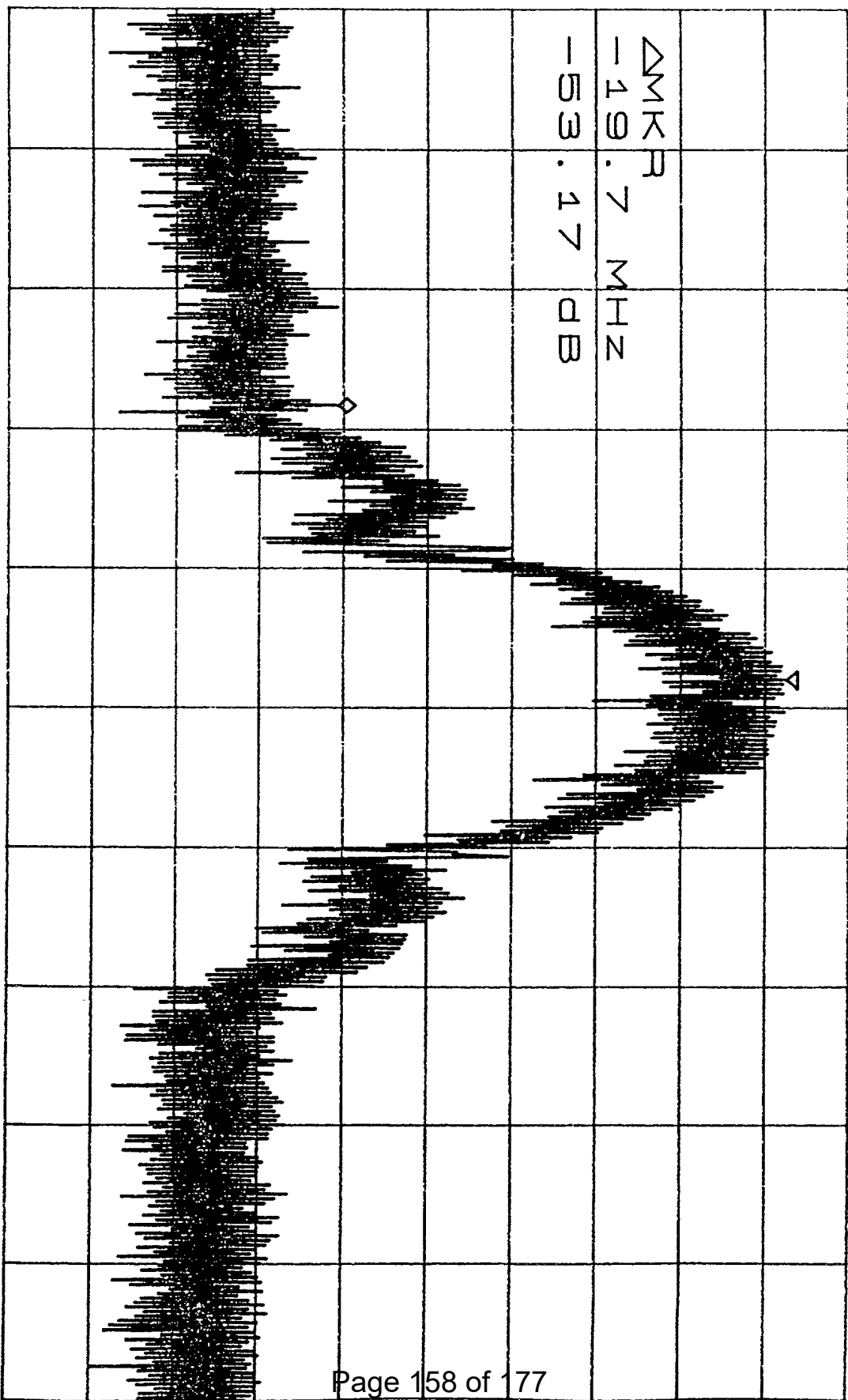
CENTER 2.46200GHz
 *RBW 100KHz
 *VBW 30KHz
 SPAN 50.00MHz
 SWP 50.0ms

50347429.000000

freq 149.5 MHz = 13.26 dBm (Q = 7.75 dBm, I = 10.7 dBm) CH #11 TX #2 #00570

FIG. 83

*ATTEN 20 DB
RL 5.0 DBM
10 DB/
-19.7 MHz



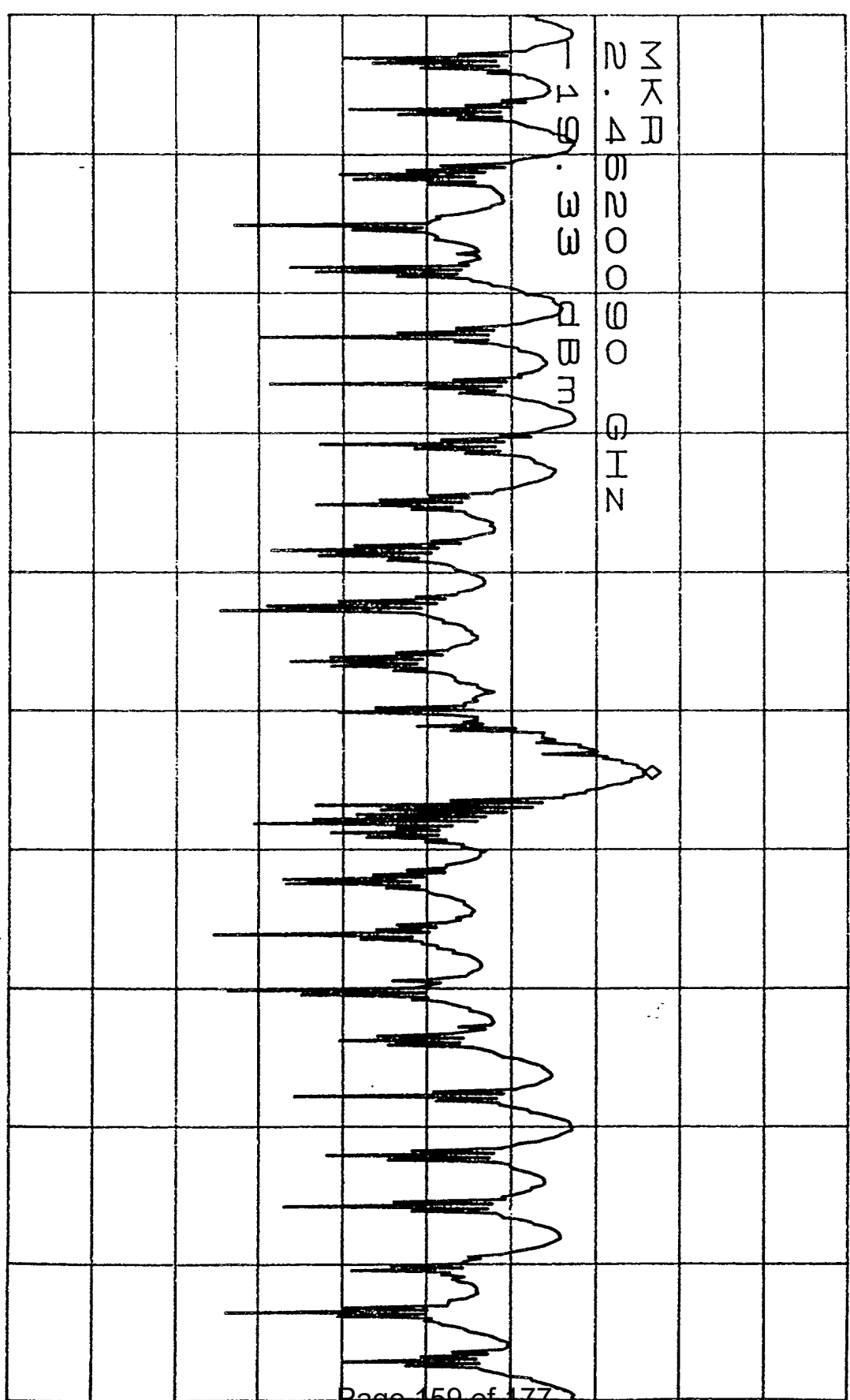
CENTER 2.4620 GHz
*RBW 100 KHz
*VBW 30 KHz
SPAN 100.0 MHz
SWP 84.0 MHz

50 149.5 MHz

2 Aug 1998, f₀ = 13.26 GHz (L₀ = 8.59 dBm, I = 10.7 dBm) CH #1 TX #2 #00570

FIG. 84

*ATTEN 20dB
 RL 5.0dBm
 10dB/
 MKR -19.33dBm
 2.4620090GHz



CENTER 2.4620000GHz
 RBW 3.0KHz *VBW 30KHz
 SPAN 200.0KHz
 SWP 67.0ms
 13.26 GHz

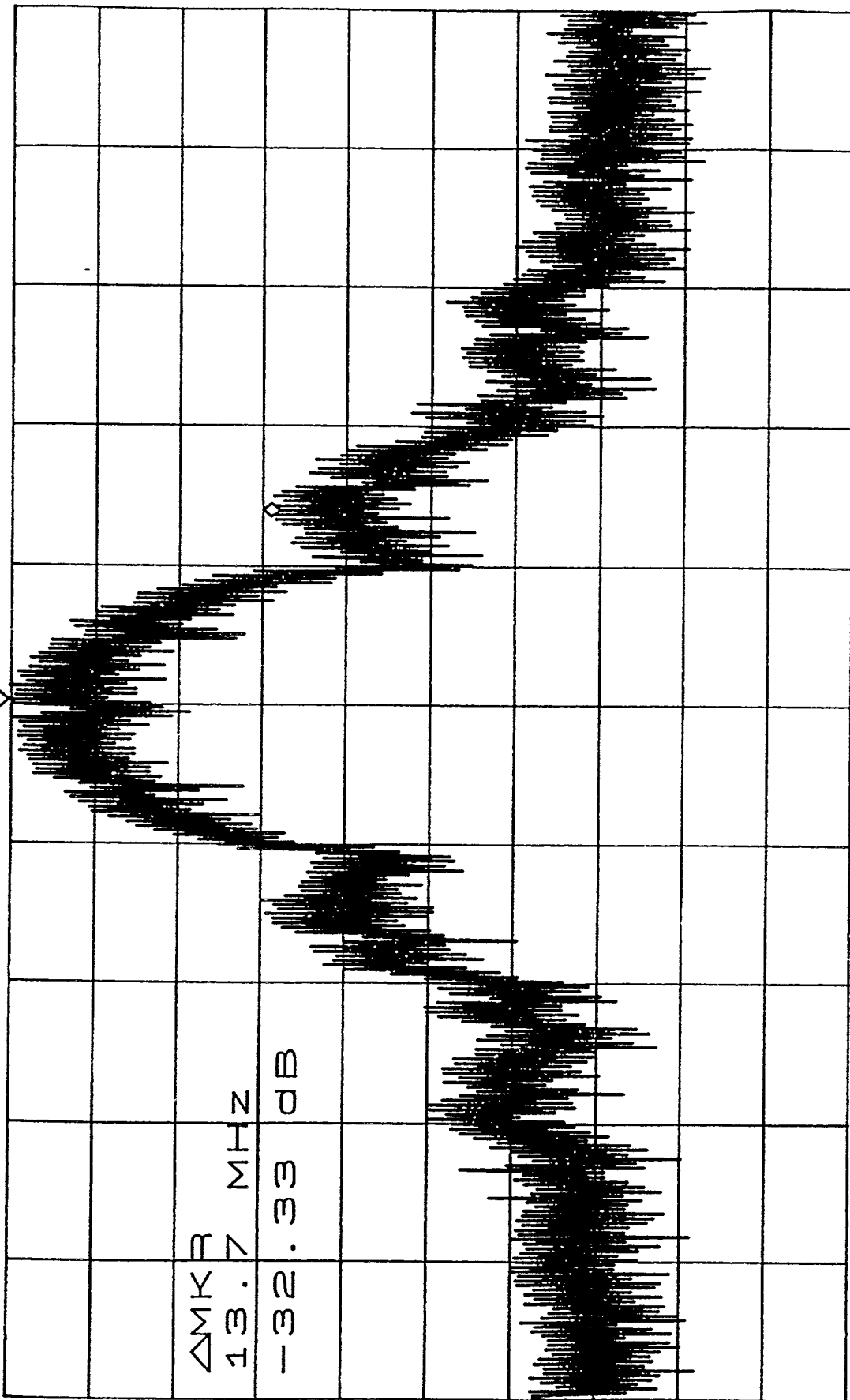
7/24/99 CW#1 P₀=15.1dBm (315 Hz BW Removal) 24.45 dB TX

*ATTEN 20dB

RL 0dBm

ΔMKR -32.33dB

10dB/Δ 13.7MHz



CENTER 2.4120GHz

*PRBW 100KHZ

*VBW 30KHZ

SPAN 100.0MHz

SWP 84.0ms

FIG. 85

7/22/99 C445 B. 12345678 (RF2126 PA AFTER RF2126 / 3dB AND BETWEEN 80500021E & 818500024)
 60403030 60403030 60403030 60403030 60403030 60403030 60403030 60403030 60403030 60403030
 *ATTEN 20dB
 RL 10.0dBm 10dB /
 ΔMKR -34.50dB
 -15.3MHz

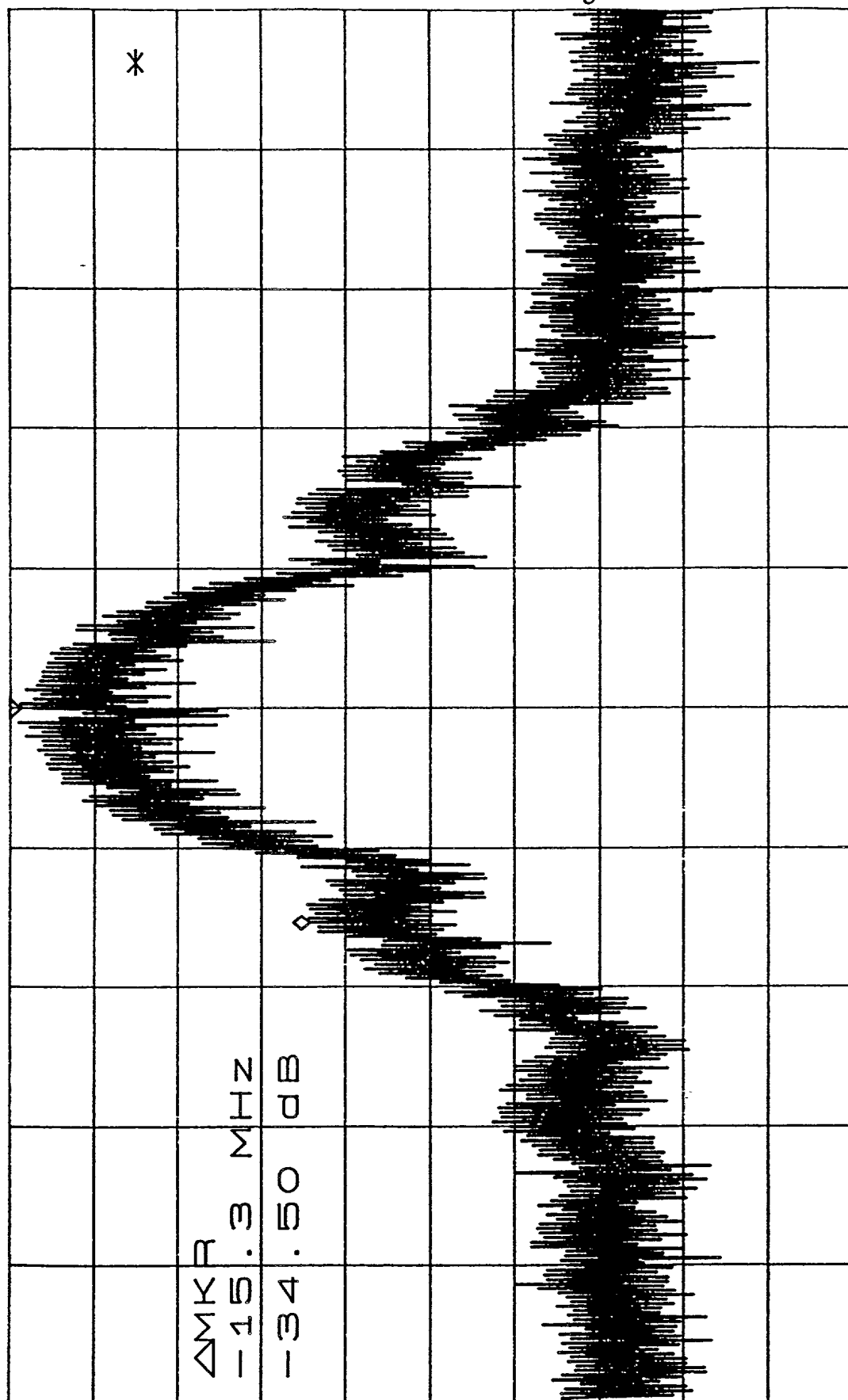


FIG. 86

CENTER 2.4320GHZ
 *RBW 100KHZ *VBW 30KHZ
 SPAN 100.0MHZ
 SWP 84.0ms

FIG. 87

7/22/99 CH15 F2: 14.6dBm (313 PPS Reduced) CENTER FREQ 2440.5 D2D TX

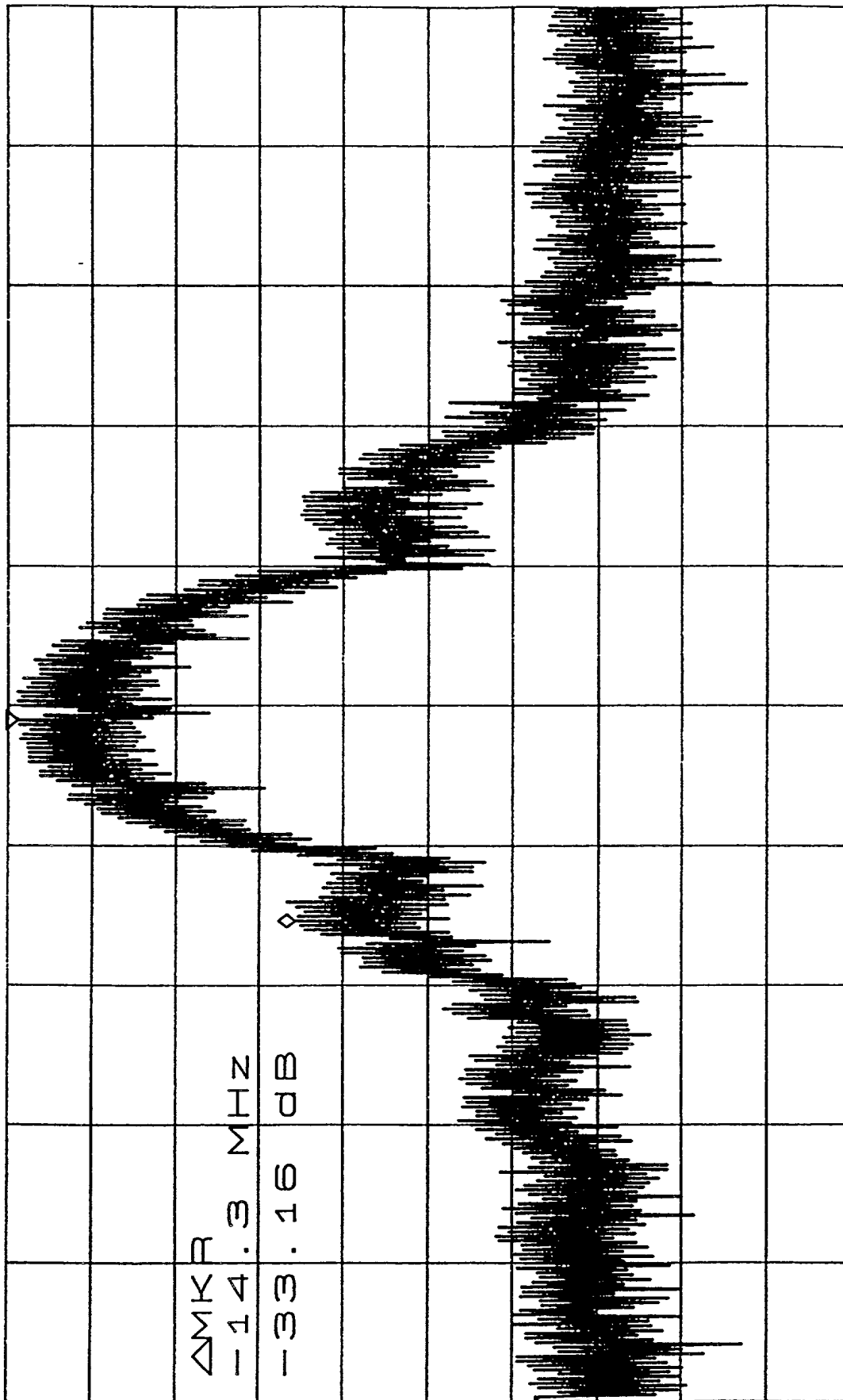
*ATTEN 20dB

ΔMKR -33.16dB

RL 0dBm

10dB/

-14.3MHz



ΔMKR
-14.3 MHz
-33.16 dB

CENTER 2.4320GHz

SPAN 100.0MHz

*RRBW 100KHz

*VBW 30KHz

SWP 84.0ms

4/2/99 CN#1 P₀ = 12.3dBm

POWER OFF 320 TX

*ATTEN 20dB
RL 0dBm
ΔMKR -55.83dB
-28.0MHz

10dB/

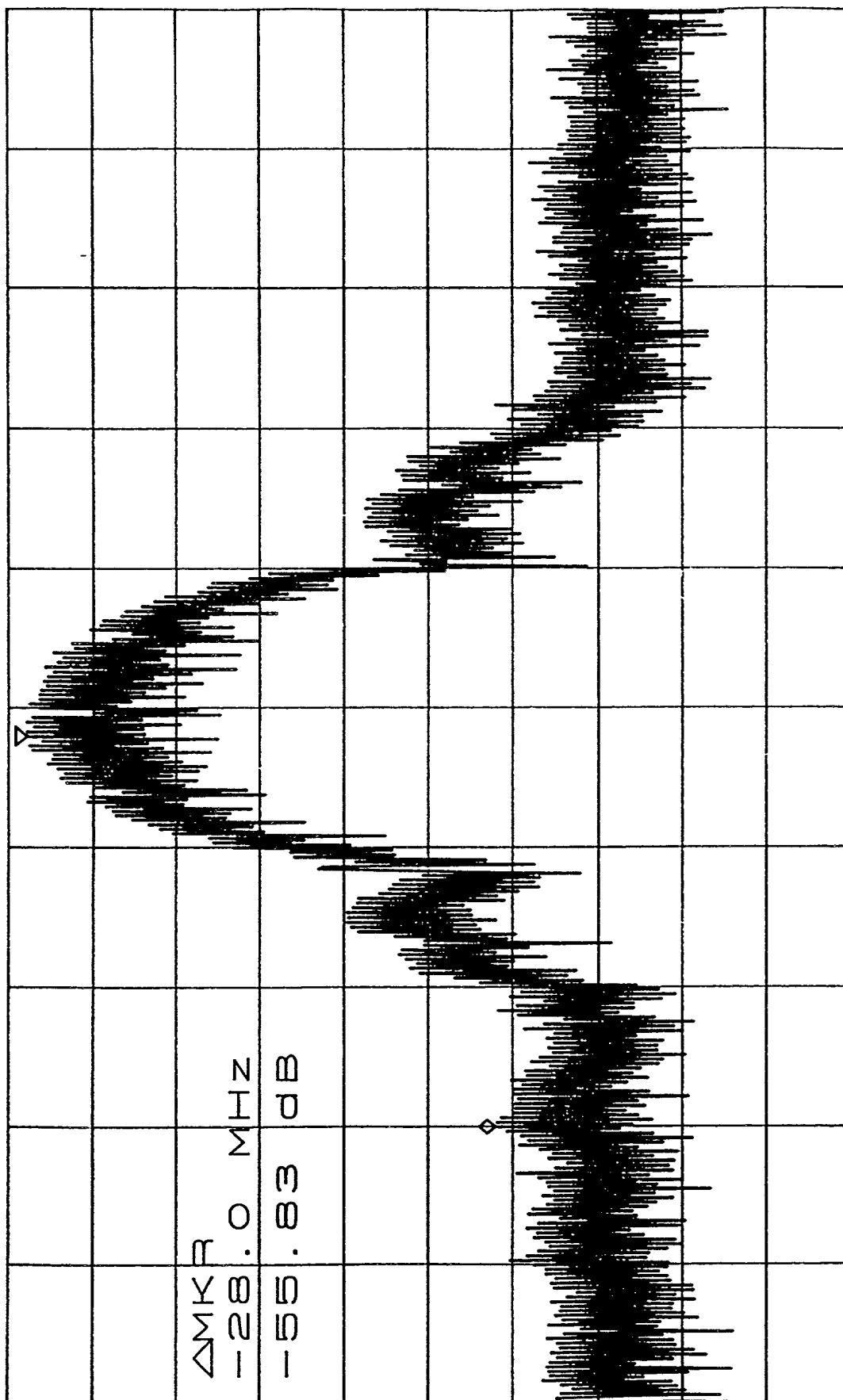
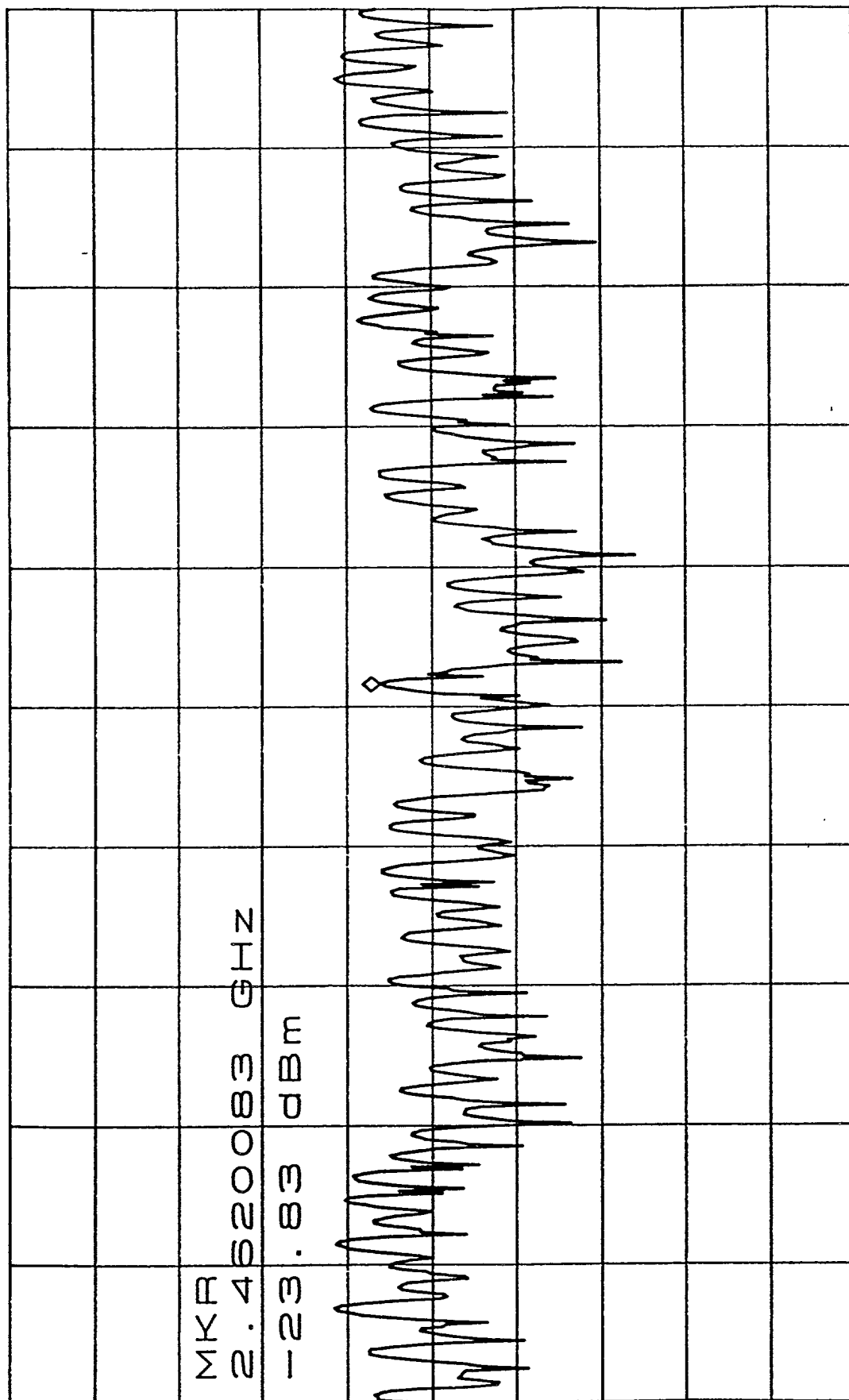


FIG. 88

7/23/99

100B/2.46200836HN



NYO. 3 MB

SECTION 404

ENTERED OFF AIR 7/23/99

ATTEN 30dB
RL 20.0dBm

MKR -12.00dBm
2.4120083GHz

10dB/

CENTER
2.4120000 GHz

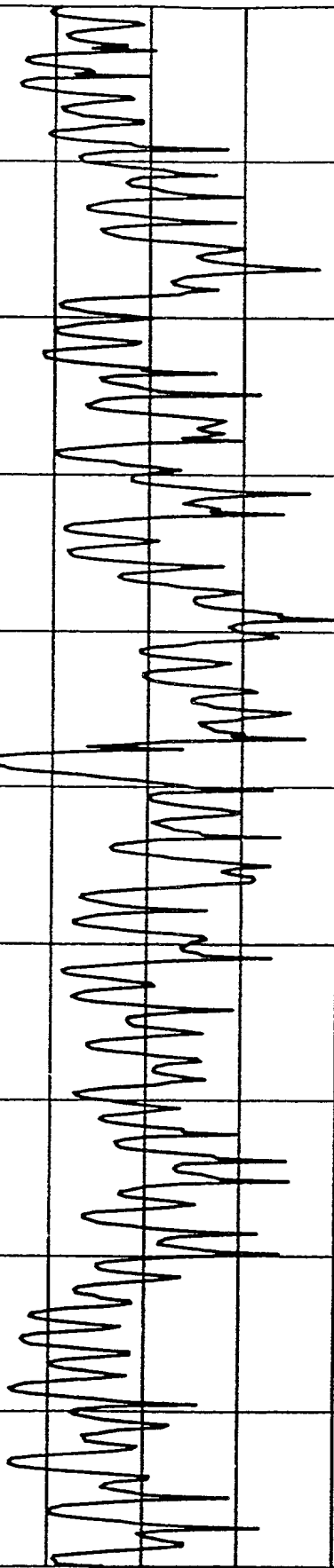


FIG. 91

CENTER 2.4120000GHz SPAN 500.0KHz
RBW 3.0KHz VBW 3.0KHz SWP 140ms

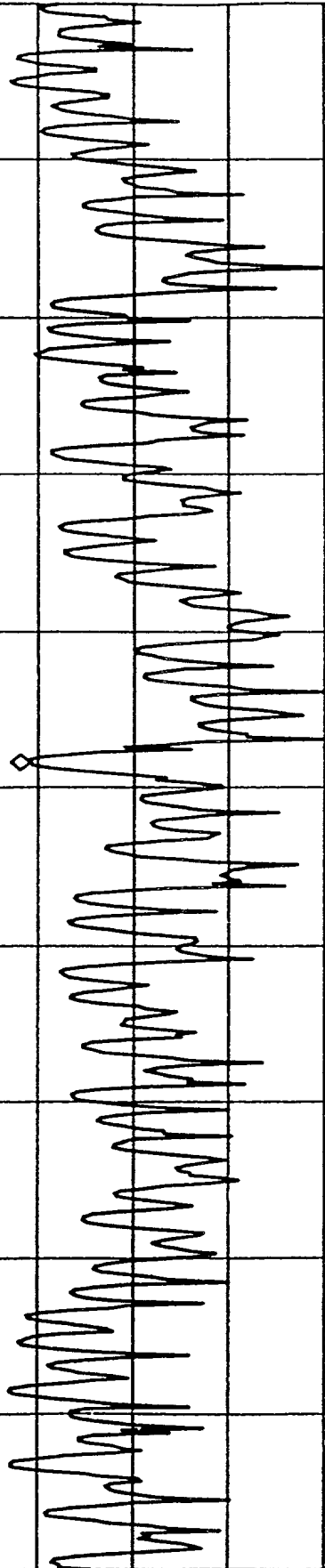
b2b TX 7/23/99

7/23/94

ΣΥΝΕΧΕΙΑ

100B/2.4320083GIN

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NIGOOO

NIYO. 3 MB >

SECRET

FIG. 92

Temperature: 27.0

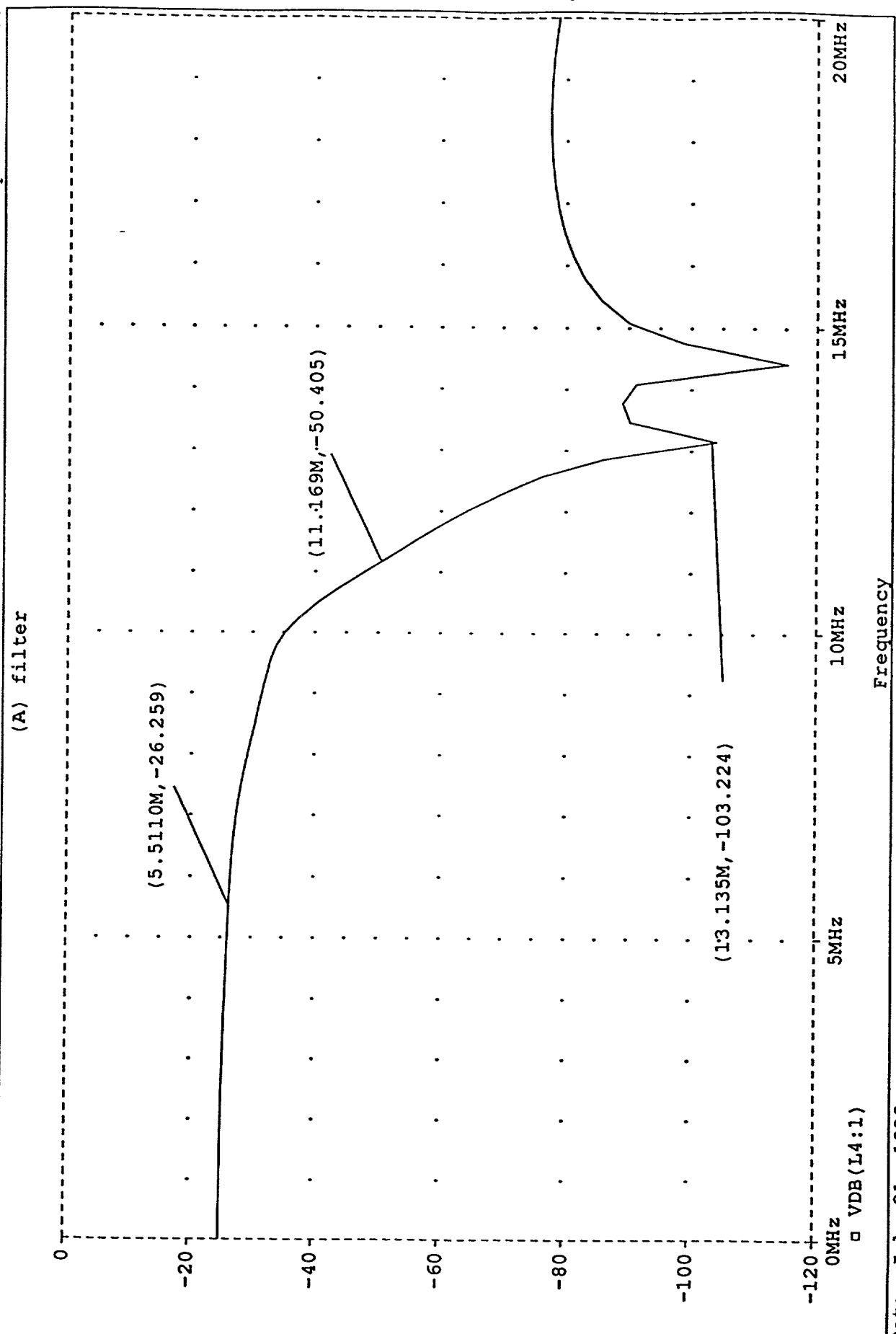


FIG. 94

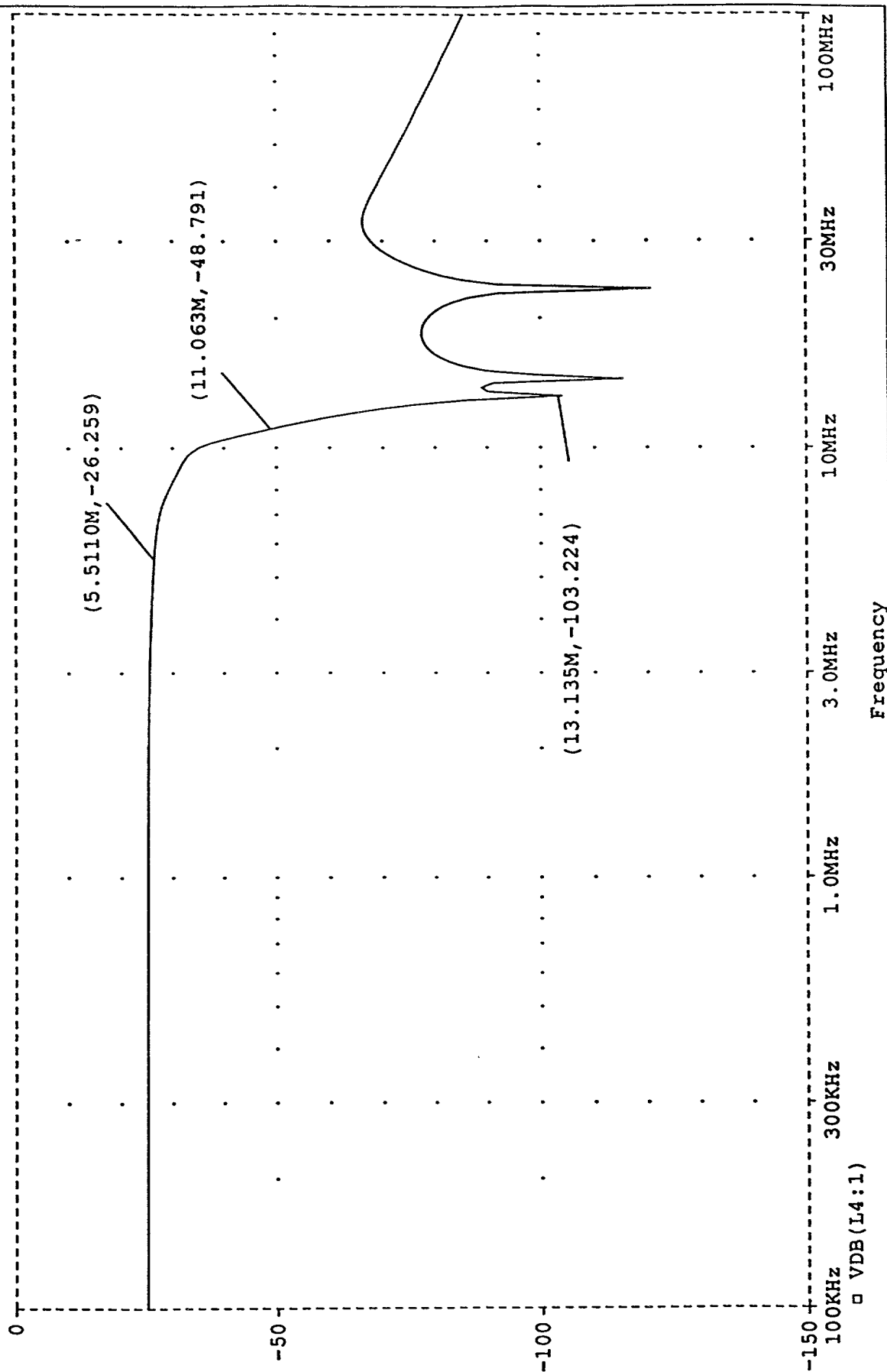
Cellular Base Station

* C:\MSim_8\Projects\CELLS\VECTOR_DEMOD\filter.sch

Date/Time run: 07/21/99 12:15:33

Temperature: 27.0

(A) filter



Date: July 21, 1999

Page 1

Time: 12:17:32

$S_{if} \#2 = 2433.4 \text{ MHz}$ (-17dBm) $S_{if} \#1 = 2433.4 \text{ MHz}$ (-17dBm) $S_{if} \#3 = 2433.4 \text{ MHz}$
 J2 2 CHANNEL

ATTN 20dB VAVG 80 ΔMKR -51.00dB
 RL 10.00dBm 10dB/ -200kHz

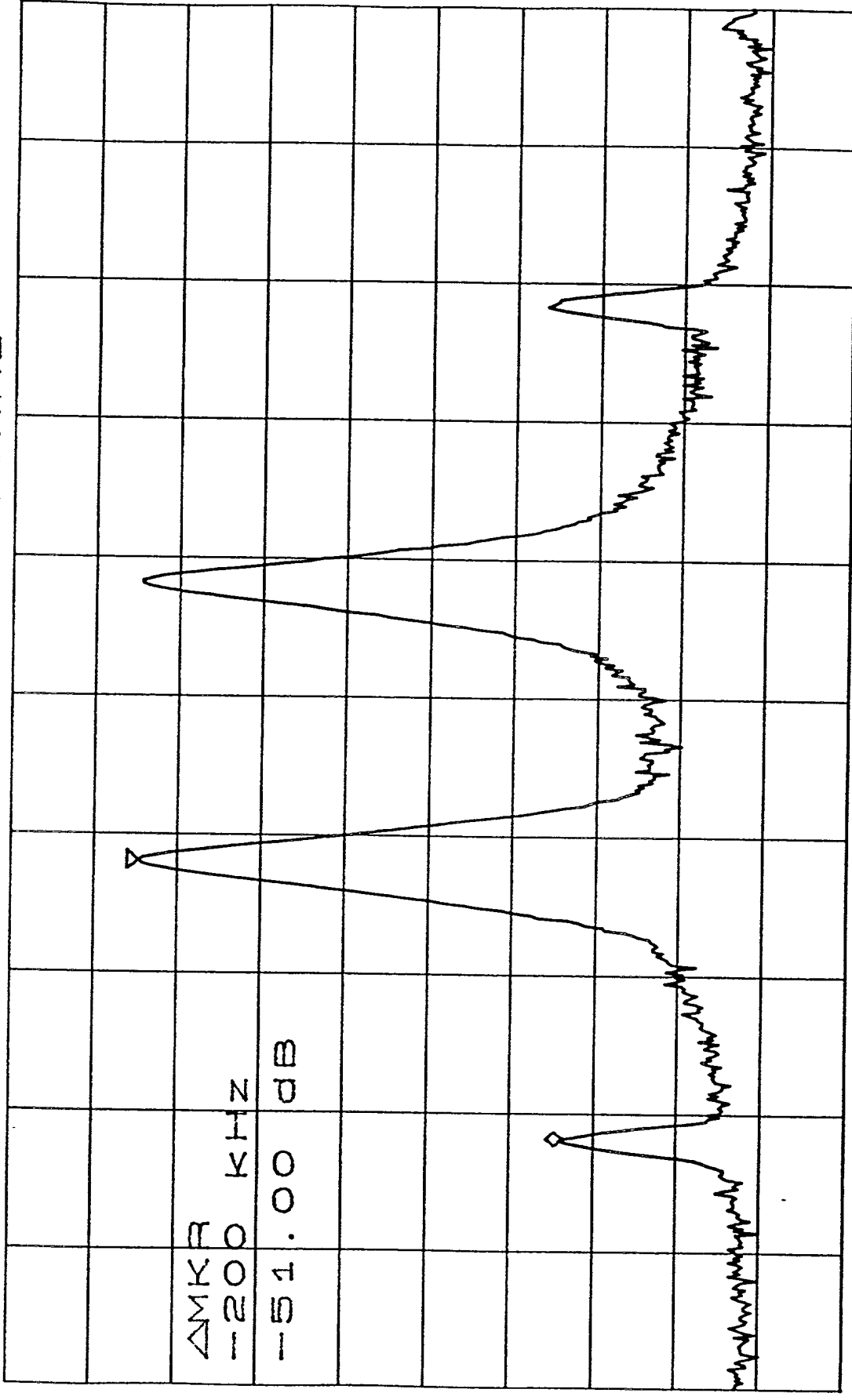
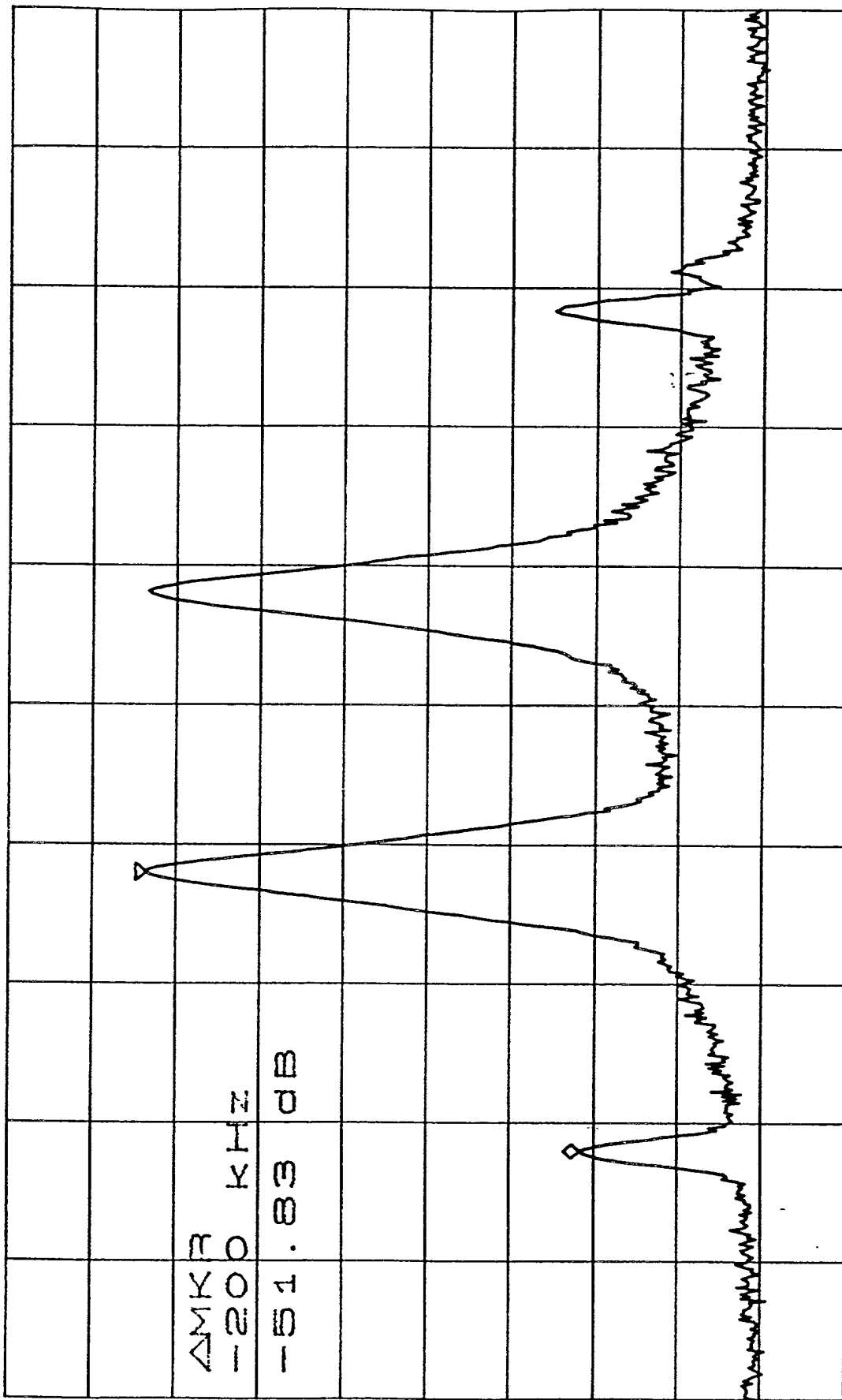


FIG. 95

CENTER 1.300MHZ SPAN 1.000MHZ
 RBW 10KHZ VBW 10KHZ SWP 50ms

28 #1 = 14142 (-17dBm) 570-20-641-001 103.001
 8y #2 = 2453.4142 (-17dBm) 570-20-641-001 103.001
 INPUT PPS = +28.9dB

ATTN 20dB VAVG 88 AMKR -51.83dB
 RL 10.00dBm 10dB/ -200KHz

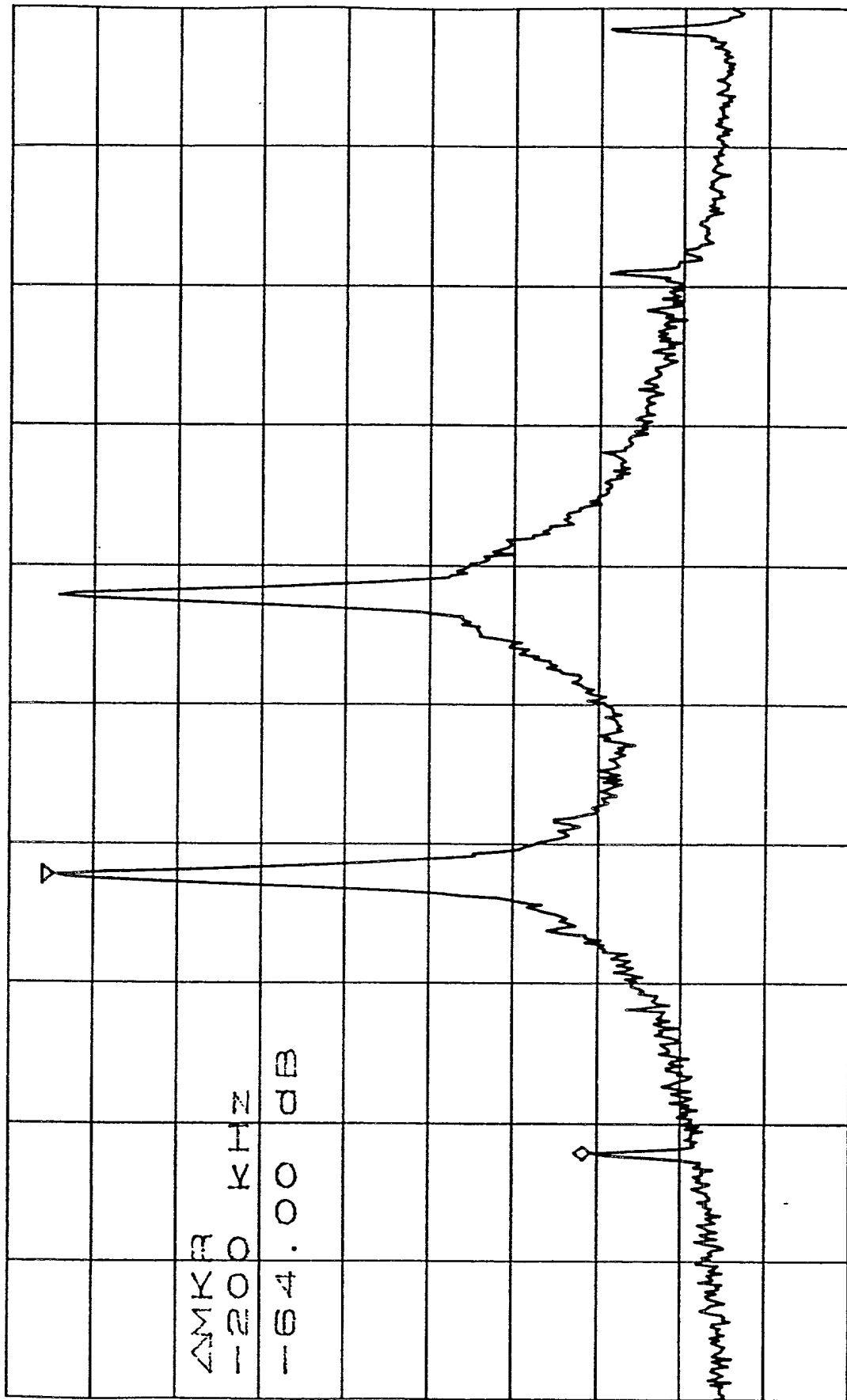


CENTER 1.300MHZ SPAN 1.000MHZ
 RBW 10KHz VBW 10KHz SWP 50ms

sig #1 = 2453.2 MHz (-27 dBm) 10 July 1999
 sig #2 = 2453.4 MHz (-27 dBm) 10 July 1999
 J4 = 2 CHANNEL

ATTN 10dB VAVG 51 ΔMKR -64.00dB
 RL -10.00dB 10dB/ -200KHz

ΔMKR
 -200 KHz
 -64.00 dB

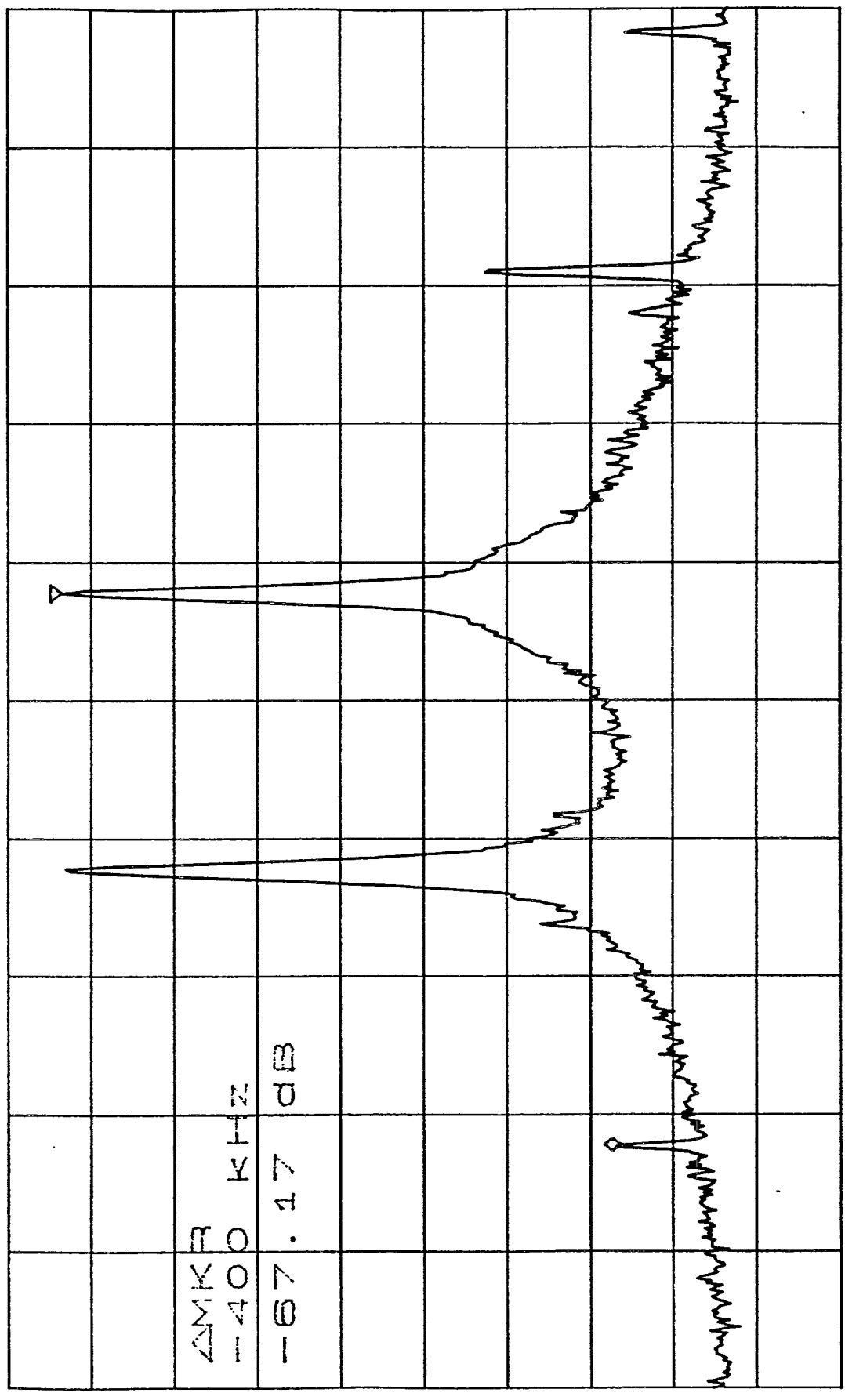


CENTER 1.300MHz SPAN 1.000MHz
 *RBW 3.0KHz VBW 3.0KHz SWP 300ms

FIG. 97

2641 2433.4 MHz (-27dBm) 685000041.001 003.01
 Input 11P3 = +1.585dBm
 J1 = I CHANNEL

ATTEN 10dB VVVS TO 10dB 100YIN
 RL -10.00dB 10dB 100YIN



CENTER 1.000MHz SPAN 1.000MHz
 MARKER 3.00MHz VERT. 3.00dB

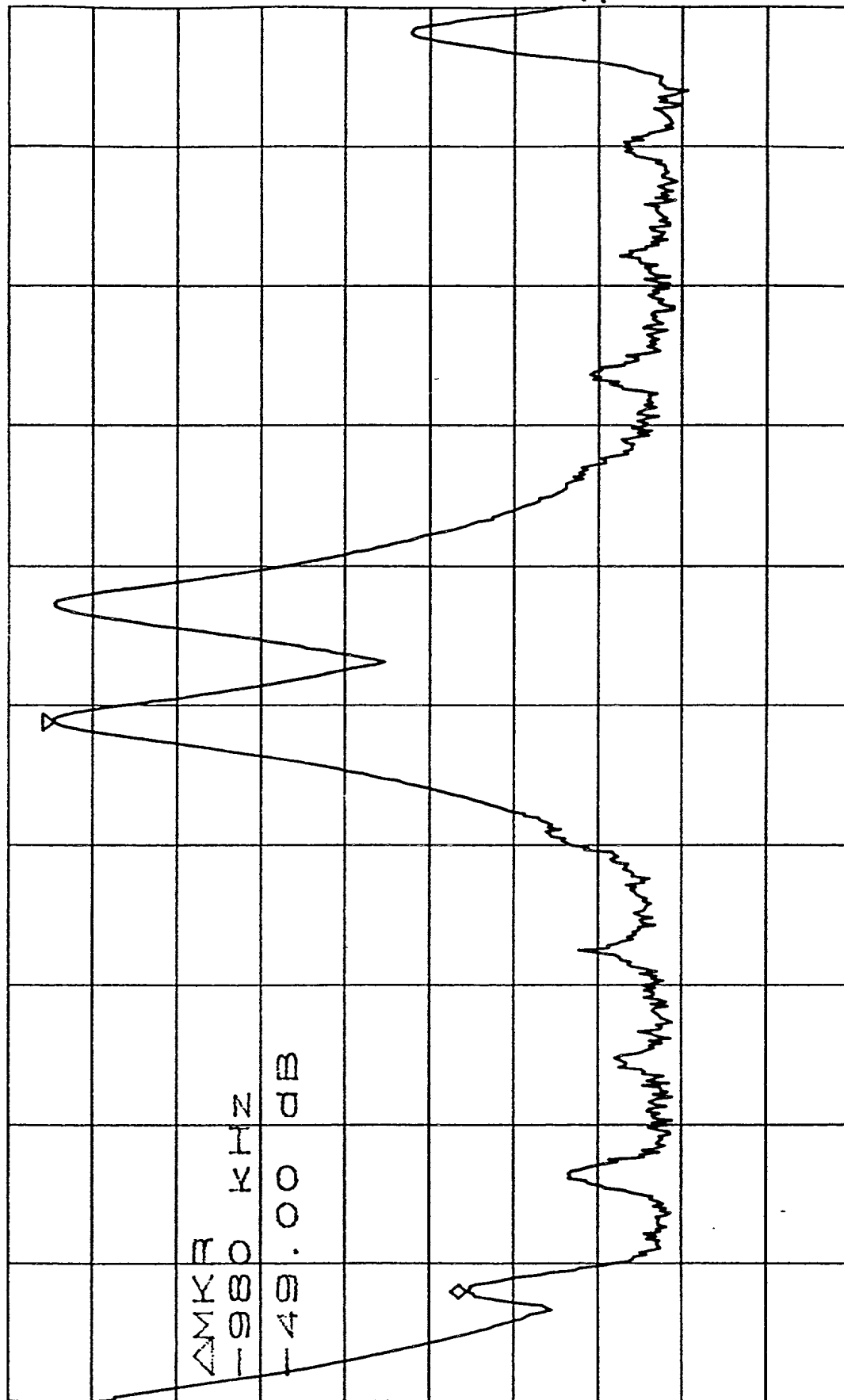
Sig #1 = 2433.5 MHz (-21.00m input) 13 JULY 1998

Sig #2 = 2433.4 MHz (-27dBm input) 578500 04:00:00 03.01

input 11P2, +2: 3m

SA = 2 CHANNEL

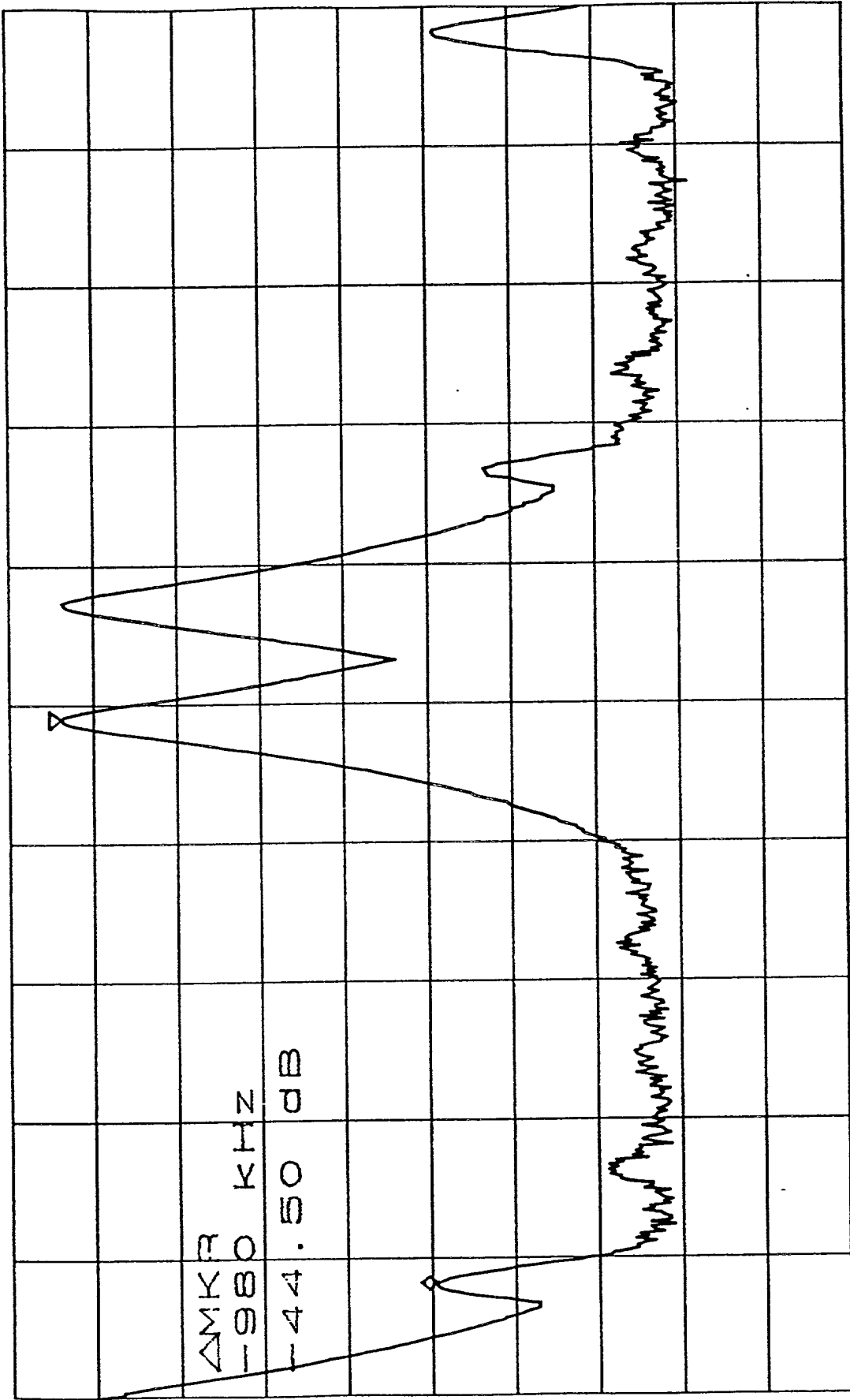
ATTEN 10dB VAVG 100 MKR -49.00dB
RL -10.00dB 10dB/ -980KHz



CENTER 1.200MHZ SPAN 2.400MHZ
RBW 30KHZ VBW 30KHZ SWP 50ms

Sig #1 = 2453.4 MHz (-41.0 dBm input) 10 JULY 1984
 Sig #2 = 2453.4 MHz (-41.0 dBm input) 10 JULY 1984
 J1 = 1 CHANNEL

ATTN 10dB VAVG 46 ΔMKR -44.50dB
 RL -10.00dB 10dB/ -980KHZ



CENTER 1.200MHZ SPAN 2.400MHZ
 RBW 30KHZ VEBW 30KHZ SWP 50ms

FIG. 101

TX TEST BED

<u>Board</u>	<u>Current Consumption (mA)</u>	<u>Voltage</u>
ST8500-641-021E	112.8	5
ST8500-641-024	75	5
ST8500-641-003	0	0
ST8500-641-008	41	5
ST8500-641-023	280	7.5
Total	508.8 (513 measured)	

3902

FIG. 102

SIGNAL TECHNOLOGIES INC.			
Title			
PCMCIA TEST BED Assembly			
Doc Number	ST8500-912-027	Rev	A
Doc	8	Rev	1
Date	Tuesday, August 03, 1999	Sheet	1 of 1

