2022-1548

IN THE UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

PARKERVISION, INC.,

Appellant,

v.

INTEL CORPORATION,

Appellee.

On Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board In Proceeding No. IPR2020-01265

BRIEF OF APPELLANT PARKERVISION, INC.

Ronald M. Daignault*
Chandran B. Iyer
Jason S. Charkow*
Richard Juang*
DAIGNAULT IYER LLP
8618 Westwood Center Drive, Suite 150
Vienna, Virginia 22182
rdaignault@daignaultiyer.com
cbiyer@daignaultiyer.com
jcharkow@daignaultiyer.com
rjuang@daignaultiyer.com
**Not admitted in Virginia*

Counsel for Appellant ParkerVision, Inc.

July 15, 2022

PATENT CLAIM AT ISSUE

U.S. Patent No. 7,110,444 B1, Claim 3:

3. A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

wherein said first and said second frequency down-conversion modules each comprise a switch and a storage element.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF INTEREST

Case Number 22-1548

Short Case Caption ParkerVision, Inc. v. Intel Corporation

Filing Party/Entity ParkerVision, Inc.

Instructions: Complete each section of the form. In answering items 2 and 3, be specific as to which represented entities the answers apply; lack of specificity may result in non-compliance. **Please enter only one item per box; attach additional pages as needed and check the relevant box**. Counsel must immediately file an amended Certificate of Interest if information changes. Fed. Cir. R. 47.4(b).

I certify the following information and any attached sheets are accurate and complete to the best of my knowledge.

Date: 04/04/2022

Signature: Ronald M. Daignault

Name: Ronald M. Daingault

1. Represented Entities. Fed. Cir. R. 47.4(a)(1).	**2. Real Party in Interest.** Fed. Cir. R. 47.4(a)(2).	**3. Parent Corporations and Stockholders.** Fed. Cir. R. 47.4(a)(3).
Provide the full names of all entities represented by undersigned counsel in this case.	Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities. ☑ None/Not Applicable	Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities. ☑ None/Not Applicable
ParkerVision, Inc.		

☐ Additional pages attached

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

☐ None/Not Applicable ☐ Additional pages attached

Stephanie Mandir		

5. Related Cases. Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case. Fed. Cir. R. 47.4(a)(5). See also Fed. Cir. R. 47.5(b).

☐ None/Not Applicable ☐ Additional pages attached

ParkerVision, Inc. v. Hisense Co., Ltd. et al WDTX-6-20-cv-00870	LG Electronics, Inc. v. ParkerVision, Inc. PTAB-IPR2022-00245	
ParkerVision, Inc. v. ZyXEL Communications Corporation WDTX-6-20-cv-01010		
ParkerVision, Inc. v. LG Electronics, Inc. WDTX-6-21-cv-00520		

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

☑ None/Not Applicable ☐ Additional pages attached

TABLE OF CONTENTS

PATENT CLAIM AT ISSUE

CERTIFICATE OF INTEREST

TABLE OF CONTENTS i

TABLE OF AUTHORITIES iv

STATEMENT OF RELATED CASES vi

JURISDICTIONAL STATEMENT 1

STATEMENT OF THE ISSUES 1

STATEMENT OF THE CASE 2

I. OVERVIEW OF WIRELESS TECHNOLOGY 2

A. Wired Communications 2

B. Wireless Communications 3

C. Frequency. 4

D. Up-conversion. 5

E. Down-conversion. 6

II. CONCEPTS RELATED TO WIRELESS TECHNOLOGY. 7

A. Basic circuit concepts. 7

B. Circuit diagrams. 9

1. Transistors. 10

2. Capacitors 11

3. Resistor. 11

4. Differential amplifier. 12

C. Electrical load. 12

III. VOLTAGE SAMPLING V. ENERGY SAMPLING. 13

A. Sample-and-hold (*voltage* sampling). 13

B. Energy Sampling. 15

C. Key take-aways. 16

IV. THE ’444 PATENT. 17

A. Overview. 17

B. The patent discloses two *fundamental different and competing* systems for down-conversion. 23

1. Energy transfer (energy sampling). 25

2. Sample-and-hold (voltage sampling). 30

V. PRIOR ART REFERENCES. 34

VI. PROCEDURAL HISTORY. 49

A. Intel’s Petition. 49

B. Patent Owner Response. 50

C. Intel’s Reply. 51

D. ParkerVision’s Sur-Reply. 51

E. Intel’s motion to exclude. 52

SUMMARY OF THE ARGUMENT 52

ARGUMENT 53

VII. STANDARDS OF REVIEW 53

VIII. PTAB’S INVALIDATION OF CLAIM 3 WAS IMPROPER BECAUSE IT IS BASED ON AN INCORRECT CONSTRUCTION OF “STORAGE ELEMENT.” 54

A. The Board’s construction of “storage element” is wrong. 54

1. The intrinsic evidence supports ParkerVision's construction. .55

2. The Board's construction is technically and legally wrong.....59

3. ParkerVision's prior arguments do not support the Board's construction. 62

B. Under the proper construction, Tayloe does not disclose a "storage element." 63

IX. THE BOARD ERRED BY BASING ITS UNPATENTABILITY DECISION ON THEORIES NOT PRESENTED IN THE PETITION. 64

X. THE BOARD ABUSED ITS DISCRETION BY STRIKING ARGUMENTS PROPERLY RAISED IN PARKERVISION'S SUR-REPLY. 66

A. ParkerVision's Sur-Reply arguments did not "proceed in a new direction." 67

B. The arguments in ParkerVision's Sur-Reply properly respond to Intel's Reply. 70

C. The portions of ParkerVision's Sur-Reply the Board struck demonstrated that Tayloe did not disclose a "storage element" 71

XI. TAYLOE DOES *NOT* DISCLOSE ELEMENTS THAT STORE "NON-NEGLIGIBLE ENERGY." 72

CONCLUSION 77

ADDENDUM Appx1

CERTIFICATE OF COMPLIANCE

TABLE OF AUTHORITIES

Page(s)

Cases

Apple Inc. v. Andrea Elecs. Corp.,
949 F.3d 697 (Fed. Cir. 2020) 55

Baxalta Inc. v. Genentech, Inc.
972 F.3d 1341 (Fed. Cir. 2020) 60

Belden Inc. v. Berk-Tek LLC,
805 F.3d 1064 (Fed Cir. 2015) 64

Dell Inc. v. Acceleron, LLC,
818 F.3d 1293 (Fed. Cir. 2016) 64

Ericsson Inc. v. Intellectual Ventures I LLC,
901 F.3d 1374 (Fed. Cir. 2018) 68

Intelligent Bio-Systems, Inc. v. Illumina Cambridge, Ltd.,
821 F.3d 1359 (Fed. Cir. 2016) 64, 65, 66

LG Elecs. Inc. v. Immervision, Inc.,
Case No. 21-2037, 2022 U.S. App. LEXIS 18948
(Fed. Cir. July 11, 2022).....53

In re NuVasive, Inc.,
841 F.3d 966 (Fed. Cir. 2016) 64

OSI Pharms., LLC v. Apotex Inc.,
939 F.3d 1375 (Fed. Cir. 2019) 53

ParkerVision, Inc. v. Hisense Co., Ltd. et al.,
Case No. WDTX-6-20-cv-00870
(W. D. Tex. Oct. 29, 2021).....54

ParkerVision, Inc. v. LG Electronics, Inc.,
Case No. 6:21-cv-00520-ADA (W.D. Tex., June 21, 2022).....60

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005) 62

SAS Institute Inc. v. Iancu,
138 S.Ct. 1348 (2018).....65, 66

Univ. of Strathclyde v. Clear-Vu Lighting LLC,
17 F.4th 155 (Fed. Cir. 2021) 53

Vidstream LLC v. Twitter, Inc.,
981 F.3d 1060 (Fed. Cir. 2020) 53, 54

Statutes

28 U.S.C. § 1295(a)(4)(A) 1

35 U.S.C. § 6.....1

35 U.S.C. § 103(a) 34

35 U.S.C. § 141(c) 1

35 U.S.C. § 312(a)(3).....64

35 U.S.C. § 319.....1

Other Authorities

37 C.F.R. § 42.23(b) 65, 67

https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf 67

STATEMENT OF RELATED CASES

No appeal in or from the same proceedings in the United States Patent and Trademark Office Patent Trial and Appeal Board ("PTAB" or "Board") was previously before this Court or any other appellate court. ParkerVision, Inc. ("ParkerVision" or "Appellant") has asserted U.S. Patent No. 7,110,444 ("the '444 patent") in the following district court cases:

- *ParkerVision, Inc. v. Intel Corp.*, Case No. 6:20-cv-00108-ADA (W.D. Tex.);
- *ParkerVision, Inc. v. TCL Indus. Holdings Co. et al.*, Case No. 6:20-cv-00945-ADA (W.D. Tex.);
- *ParkerVision, Inc. v. Hisense Co., Ltd. et al.*, Case No. 6:20-cv-00870-ADA (W.D. Tex.);
- *ParkerVision, Inc. v. LG Elecs., Inc.*, Case No. 6:21-cv-00520-ADA (W.D. Tex.);

The '444 patent is currently involved in the following proceedings before the United States Patent and Trademark Office Patent Trial and Appeal Board ("PTAB"):

- *TCL Industries Holdings Co., Ltd. et al. v. ParkerVision, Inc.*, Case No. IPR2021-00990 (PTAB);

- *LG Elecs. Inc. v. ParkerVision, Inc.*, Case No. IPR2022-00245 (PTAB) (joined with IPR2021-00990) (collectively no. IPR2021-00990 and IPR2022-00245 are referred to as "the TCL IPR").

ParkerVision submits that the PTAB's Final Written Decision in the TCL IPR referenced above, which is expected to issue on or before November 22, 2022 and any subsequent appeal thereof, will directly affect or be directly affected by this Court's decision in this appeal.

JURISDICTIONAL STATEMENT

The PTAB had jurisdiction over the petition for *inter partes* review ("Petition") brought by Intel Corporation ("Intel") under 35 U.S.C. § 6 that is the subject of this appeal: IPR2020-01265. The PTAB issued its Final Written Decision in IPR2020-01265 on January 21, 2022. Appx1. Appellant ParkerVision timely filed a notice of appeal on March 18, 2022. Appx1273. This Court has jurisdiction under 35 U.S.C. § 141(c) and 319 and 28 U.S.C. § 1295(a)(4)(A).

STATEMENT OF THE ISSUES

1. Whether the PTAB erred by invalidating claim 3 of the '444 patent based on an incorrect claim construction of "storage element," where the PTAB failed to consider the complete disclosure of the patent specification.

2. Whether the PTAB erred when it based its unpatentability decision on theories not presented in the Petition but, instead, were raised for the first time in Intel's Reply.

3. Whether the PTAB abused its discretion by striking arguments properly raised in Patent Owner's Sur-Reply in response to newly raised arguments in Intel's Reply.

4. Whether the PTAB erred by invalidating claim 3 of the '444 patent under the PTAB's claim construction of "storage element" (which stores non-

negligible amounts of energy) where the prior art reference the Board relied on discloses "holding elements" (which hold *negligible* amounts of energy).

STATEMENT OF THE CASE

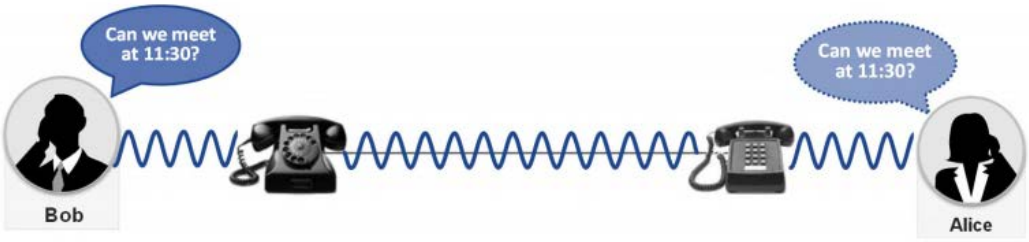
This case is an appeal of the PTAB's Final Written Decision ("FWD") in IPR2020-01265, which challenged claim 3 of the '444 patent.

I. OVERVIEW OF WIRELESS TECHNOLOGY.

The '444 patent relates to wireless communication and, more particularly, to frequency up-conversion and down-conversion of electromagnetic (EM) signals. Appx5349(¶ 26).

A. Wired Communications.

Traditional wired communications networks transmit audio signals over wire lines by converting audio signals to electrical signals and back to audio signals. Appx5349(¶ 27).



When Bob speaks into a phone, Bob's phone converts his voice (low frequency audio signals) into electrical signals. Electrical signals are transmitted over wires to Alice's phone, which converts the electrical signals back into audio signals so that Alice can hear Bob's voice. Appx5349-5350(¶ 28).

B. Wireless Communications.

Similar to wired communications, in wireless communications, low frequency audio signals are converted into electrical signals. But instead of travelling through wires, the signals are transmitted through air as radio waves (electromagnetic (EM) waves). Appx5350(¶ 29).



As shown above, wireless devices use high radio frequency (RF) signals (e.g., above 300 MHz (red)) because high frequency signals can carry more information and because high frequency antennas can physically fit within small devices such as cellular phones. Appx5350(¶ 30).

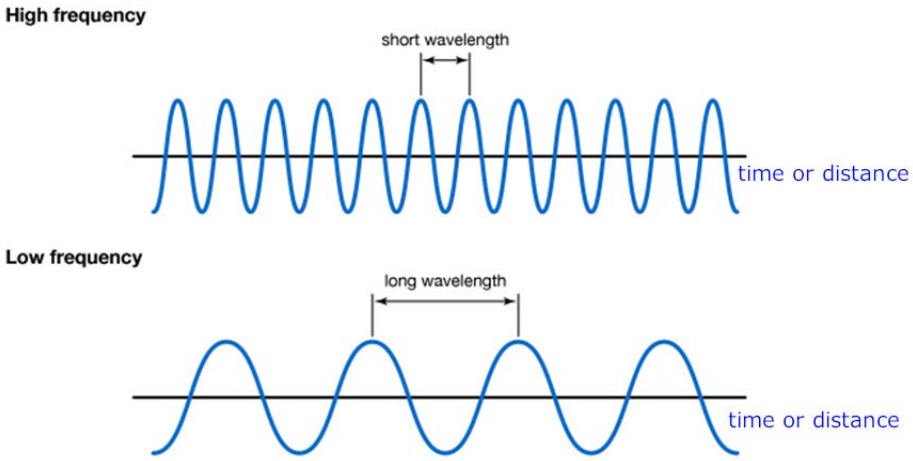


In a wireless communication, when Bob speaks into his cell phone, Bob's cell phone converts his voice (low frequency audio signals) into a high frequency

RF signal. The RF signal is transmitted over the air to Alice's cell phone. Alice's cell phone then converts the RF signal back into a low frequency audio signal and Alice can hear Bob's voice. Appx5350-5351(¶ 31).

C. Frequency.

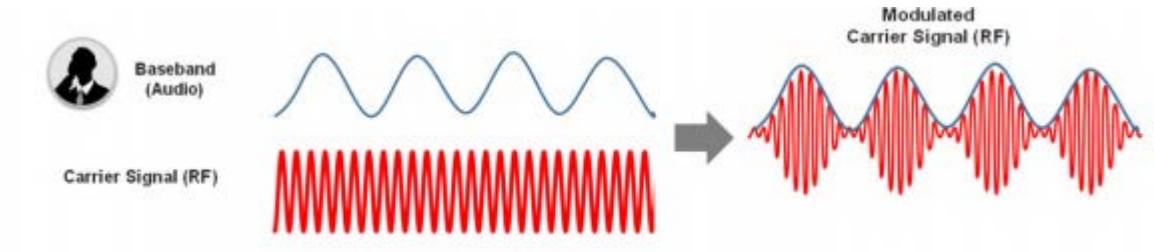
Frequency is the number of cycles of a wave per unit time (second). Appx5351(¶ 32).



As shown above, a high frequency signal has more cycles of a wave per second than a low frequency signal. Notably, the frequency of an audio wave can be one thousand cycles per second whereas the frequency of a radio wave can be one billion cycles per second. Appx5351(¶ 33).

D. Up-conversion.

To transmit an audio signal over air, a wireless device must transform the audio signal to an RF signal. Because the RF signal is used to carry the information in the audio signal, the RF signal is referred to as a "carrier signal." And since audio waves are at a low frequency, they are referred to as "baseband," a "baseband signal" or at a "baseband frequency." Appx5351-5352(¶ 34).



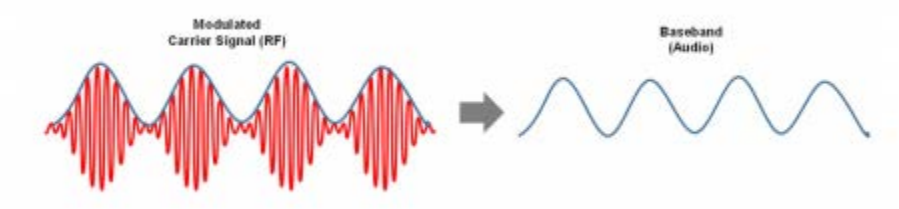
To transport the baseband signal (e.g., audio signal), the transmitting wireless device (e.g., Bob's cell phone) modifies the carrier (RF) signal. As shown above, the baseband signal is impressed upon the carrier signal (above left), thereby modulating/changing the shape of the carrier signal to approximate the shape of the baseband (audio) signal (above right).[1] The modified signal is referred to as a "modulated carrier signal." The process is referred to as "up-conversion" because the low frequency signal is being up-converted to a high frequency signal. Appx5352(¶ 35); *see also* Appx5373(¶¶ 103-104), Appx5373-5374(¶ 105).

[1] This type of modification is referred to as amplitude modulation. But other types of modulation can be used. Appx5352(¶ 35 n.1).

E. Down-conversion.

In order for the receiving wireless device (e.g., Alice's cell phone) to recover the baseband (audio) signal (and the information that it carries) from the modulated carrier signal, the receiving wireless device must transform the modulated carrier signal back to a baseband signal (e.g., audio signal). This process is referred to as "demodulation" or "down-conversion" because a high frequency signal is being down-converted to a low frequency signal. Appx5352-5353(¶ 36); Appx5377(¶ 113).

Demodulation is the inverse of modulation and results in the extraction of the baseband signal from the modulated carrier signal. Appx5377(¶ 114).



As shown above, "down-conversion" is the process by which the baseband (audio) signal is recovered from the carrier signal. Down-conversion is the subject of claim 3 of the '444 patent. Appx5353(¶ 37).

Today, a receiver can down-convert from an RF signal to a baseband signal in one-stage or multiple-stages. In a one-stage configuration, the RF signal is directly converted to a baseband signal. This is referred to as direct down-conversion. In a multiple-stage configuration, the RF signal is first down-converted

to an intermediate frequency (IF) signal, which is then down-converted to a baseband signal. Appx5379(¶ 120).

At the time of the invention of the ’444 patent, in the late 1990s through March 2000, however, direct down-conversion was not well developed. At that time, receivers generally used multiple-stage conversion. There was, however, significant research and development dedicated to finding ways to accomplishing direct down-conversion using a single conversion stage. Many companies failed in this endeavor and the solutions that were developed had significant technical and practical limitations. Appx5379-5380(¶ 121).

II. CONCEPTS RELATED TO WIRELESS TECHNOLOGY.

A. Basic circuit concepts.

RF signals are created using electronic circuits. To understand circuits, it is important to understand the concepts of charge, voltage, current, energy, power, resistance and impedance. Appx5356(¶ 43).

Charge: In a circuit, there are two physical types of charge – positive charge and negative charge. Protons have a positive charge (+) and electrons have a negative charge (–). Appx5356(¶ 44).

Circuits operate based on the movement of electrons and the movement of charge transfers energy. Charge may build up to establish a voltage signal. Here, a voltage signal refers to information that is almost entirely conveyed as a voltage.

Alternatively, the movement of charge, the rate of which is current, may itself be the signal. Appx5357(¶ 47).

Voltage: Voltage is the difference in an electron's potential energy, per unit charge, between two points. In other words, voltage is the amount of potential (electrical) energy available, per unit charge. Negative charges (electrons) are pulled towards higher voltages, while positive charges (protons) are pulled towards lower voltages. Appx5357(¶ 48).

Electric current: An electric current is the movement/flow of charge in a circuit (in a conductor or into, out of, or through an electrical component). Current (the net rate of movement of positive charges) flows from positive voltage to negative voltage. Appx5358(¶ 49).

Electric energy: Electric energy is energy that results from the movement of a charge in a circuit. The faster the charges move and the more charges that move, the more energy they carry. The only way to transfer energy is by transferring charge. So, movement of a charge indicates movement of energy. Appx5358(¶ 50).

Energy is not the same as voltage. Energy and voltage are used in circuits in *different ways*. Appx5359(¶ 53).

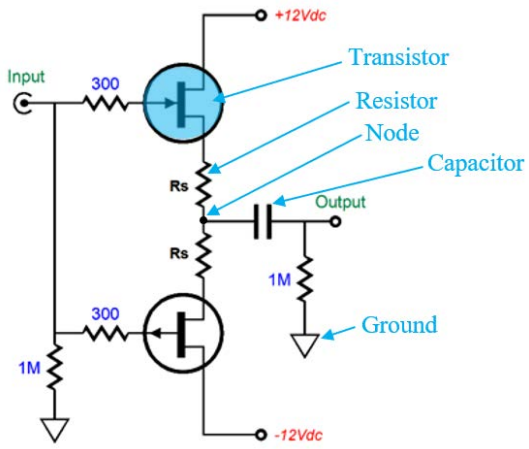
Power: Power is the amount of energy transferred per unit time. Power is the average rate at which energy is transferred by charges. Appx5359(¶ 54).

Resistance: Resistance is a measure of the difficulty of passing an electric current through a conductor. Appx5359(¶ 55).

Impedance: Impedance is the measure of the opposition that a circuit presents to a current when a voltage is applied. Impedance is related to, but not the same as, resistance. Resistance is one component of impedance. In addition, impedance describes the ability of a circuit element to store and/or return electrical energy (referred to as reactance). A circuit component with high resistance has high impedance. Appx5359-5360(¶ 56).

B. Circuit diagrams.

Circuit designers/engineers use circuit diagrams to illustrate how circuit elements are connected together. Appx5362(¶ 64).



The exemplary circuit diagram above shows various circuit elements connected together by wires/traces (shown by lines). Transistors, capacitors, and resistors shown in the diagram are described below.[2] Appx5363(¶ 65).

Each circuit element has a particular effect(s) on voltage, current, charge, and energy. By combining circuit elements in different numbers and/or ways and using circuit elements that have certain values, circuit designers/engineers can create circuits that perform a wide variety of different functions. Appx5363(¶ 66).

1. Transistors.

A transistor is a semiconductor device used to switch or amplify electronic signals and electrical power. A transistor has at least three terminals for connection to an external circuit. Key to the functionality of a transistor is that a controlling voltage or current at one terminal can control a current between two of the other terminals. Appx5363(¶ 67).

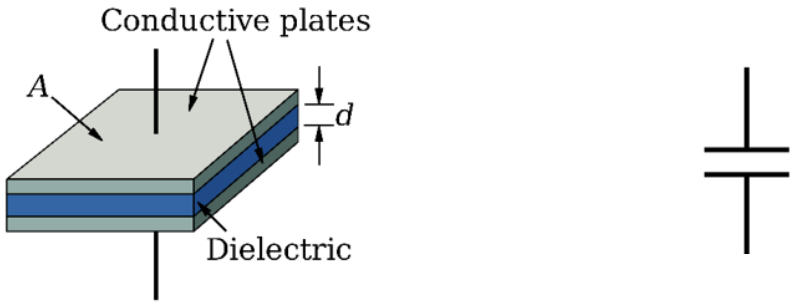
Whether a transistor is used as a switch or performs another function depends on the signals applied to the terminals of the transistor, and on the circuit in which the transistor is located. Appx5363-5364(¶ 68).

---

[2] "Ground" (shown as an upside-down triangle) is a connection to a fixed potential which is defined as zero volts and a "node" (shown as a dot) is a location where three or more wires/leads come together. Appx5363(¶ 65).

2. Capacitors.

A capacitor is a circuit element used to store (accumulate) energy. A capacitor stores electric charge in an electric field by separating charges over a distance. Appx5364(¶ 72).



As shown above left, a capacitor is constructed with two conductive (metal) plates with a dielectric (or air) separating the plates by a distance *d*. The dielectric/air does not allow current to pass. Appx5365(¶ 75). The symbol for one type of capacitor is shown above right. Appx5364-5365(¶ 73).

A capacitor can be used in *different ways* within a circuit. In particular, the capacitance of a capacitor and the electric elements connected to a capacitor dictate how the capacitor operates in a circuit. Appx5367(¶ 83)

3. Resistor.

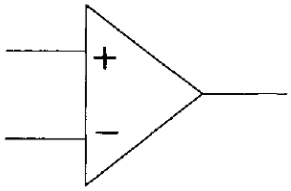
A resistor is a circuit element that introduces resistance into a circuit. The symbol for one type of resistor is shown below. Appx5367(¶ 84).



Resistors are used, for example, to reduce current flow, adjust signal levels, divide voltages, bias active elements, and terminate transmission lines. Appx5367(¶ 85).

4. Differential amplifier.

A differential amplifier is an electrical element that amplifies voltage or current. It has two input terminals and either one or two output terminals. The symbol for a single-output differential amplifier is shown below. Appx5358(¶¶ 88-89).



C. Electrical load.

An electrical load is an electrical element or portion of a circuit that absorbs power and converts it into a desired form. Appx5274. Whereas a power source supplies energy, a load extracts/uses energy. For example, a resistor is a type of load and a differential amplifier is another type of load. Appx5369(¶ 92).

Connecting a load to a capacitor affects the operation of the capacitor and, thus, the way the capacitor is used in a circuit. Appx5369(¶ 91).

There are high impedance loads and low impedance loads. A high impedance load inhibits current from moving in a circuit and absorbs very little

electrical energy. A low impedance load provides little constraint to current moving in a circuit and absorbs electrical energy. Thus, a low impedance load must have a low resistance, whereas a load with a high resistance is a high impedance load. Appx5369-5370(¶ 93).

Since a load is connected to the output of other circuitry, the circuitry (e.g., capacitor, source, transistors) is said to be driving the load (when substantial current flows from the circuitry to the load). For example, when circuitry is connected to a low impedance load, the circuitry is said to be driving a low impedance load. Appx5370(¶ 94).

III. VOLTAGE SAMPLING V. ENERGY SAMPLING.

The ’444 patent discloses only two systems/technologies – voltage sampling and energy sampling. The difference between these technologies is critical to understanding why Intel’s prior art fails to invalidate claim 3.

Claim 3 covers only *energy* sampling. On the other hand, Tayloe (Intel’s main prior art reference) pertains to *voltage* sampling. But energy sampling and voltage sampling are *fundamentally different and competing* systems. And these differences are why Intel’s prior art fails to disclose the claimed “*storage* element.”

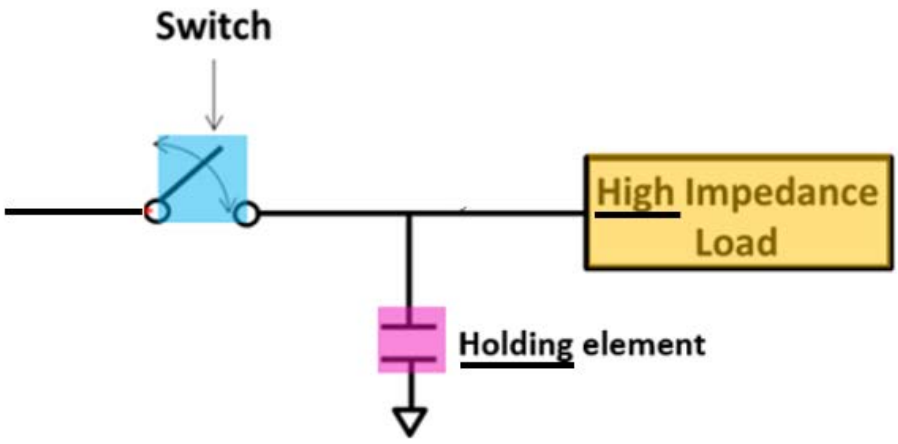
A. Sample-and-hold (*voltage* sampling).

At the time of the’444 patent invention, in the late 1990s through March 2000, a technology being considered for direct down-conversion (to recover the

baseband signal directly from the RF signal without using IF) was sample-and-hold (*voltage* sampling). There are different types of sample-and-hold (*voltage* sampling) systems. Appx5387-5388(¶¶ 141-144).

All such systems, however, attempted to replicate the *voltage* of the RF signal with as little distortion as possible. In the late 1990s through March 2000, it was thought that the best (and most accurate) way to replicate the *voltage* of the RF signal, while distorting the RF signal as little as possible, was to sample the voltage of the RF signal itself. Based on numerous *readings* of the *voltage*, sample-and-hold (*voltage* sampling) systems could derive a baseband signal (which is a representation of the baseband signal sent from a transmitting device). Appx5387-5388(¶142).

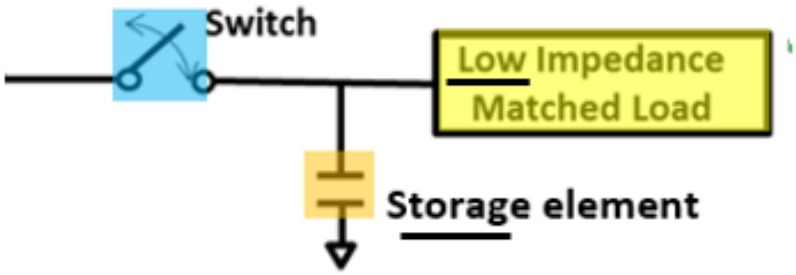
The diagram below illustrates an exemplary sample-and-hold (*voltage* sampling) system.



As shown above, a sample-and-hold (*voltage* sampling) system includes a switch (blue), a holding element (capacitor) (pink) coupled to ground, and a *high* impedance load (orange). The '444 patent specifically *reserves* the term "*holding*" module/element to refer to an element (e.g., capacitor) used in a sample-and-hold (voltage sampling) system because, as discussed in Section IV.B.2 below, the use of a *high* impedance load causes the capacitor to *hold* energy (i.e., *prevent* energy in the capacitor from being discharged to form the down-converted signal – the discharged energy itself does not becomes part of the down-converted signal). Appx5389-5390(¶ 146); Appx5387-5394; Appx5401-5402; Appx5417-5421.

B. Energy Sampling.

The diagram below illustrates ParkerVision's implementation of an energy transfer (*energy* sampling) system for radio communications. *See, e.g.*, Appx5394(¶ 156); Appx5402(¶ 176).



ParkerVision's energy transfer (energy sampling) system includes a switch (blue), a *storage* element (capacitor) (orange) coupled to ground, and a *low* impedance load (yellow). Using a *low* impedance load is significant in the design

of ParkerVision's inventive energy transfer (energy sampling) system. Appx5395(¶ 159).

The '444 patent specifically *reserves* the term "*storage*" module/element to refer to an element (e.g., capacitor) used in an energy sampling system because, as discussed below, the use of a *low* impedance load enables the capacitor to *store* energy and subsequently *discharge* the energy to form the baseband signal (i.e., the discharged energy itself becomes part of the baseband signal). The ability to store and discharge energy to form the down-converted signal is critical to ParkerVision's invention. Appx5395-5396(¶ 160); Appx5394-5402; Appx5412-5417; *see also* Section IV.B.1 below.

C. Key take-aways.

What is critical to understand is that while both energy sampling and voltage sampling use similar components (e.g., switches, capacitors and loads), these components are used in different *ways* in a circuit to create a desired result. Appx5401-5402(¶ 173).

But the *way* in which the components are used is significant. Whereas a voltage sampling circuit discards energy without using the energy in the down-converted signal (thereby wasting energy), an energy sampling circuit discharges energy into a load so that the energy itself becomes part of the down-converted signal. *Id.*

Though the Board acknowledged the differences between these two systems as described throughout the specification, it then improperly ignored them.

IV. THE '444 PATENT.

A. Overview.

The '444 patent relates to a system and method to up-convert and down-convert an electromagnetic signal (radio frequency signal). Appx447(2:20-22, 25-28; Appx451(9:27-29); *see also* Appx5387-5394; Appx5401-5402; Appx5417-5421. Since claim 3 relates to down-conversion, this section focuses on down-conversion.

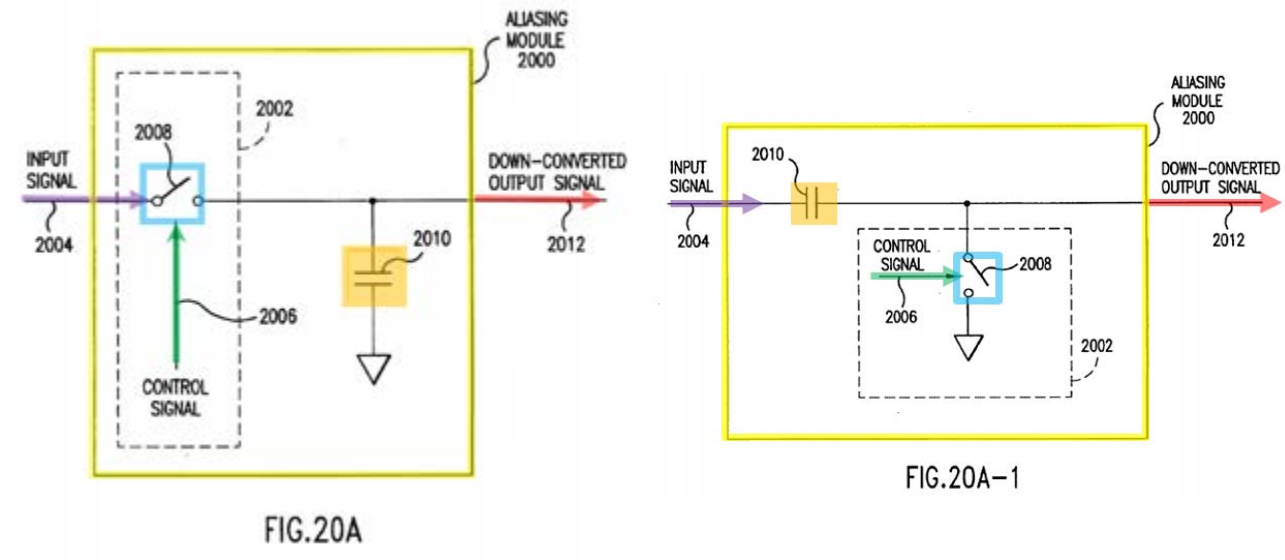


Figure 20A (above left) shows the basic configuration of a universal frequency down-conversion (UFD) module, which is also referred to as an aliasing module. Appx451(9:43-48). Aliasing (UFD) module 2000 (yellow) includes (1) a universal frequency translation (UFT) module 2002 (implemented as a switch 2008

(blue) with a control signal 2006 (green) for controlling the switch) and (2) a capacitor 2010 (orange) for storing and discharging energy. *Id.* The switch receives an input signal 2004 (purple arrow), processes the signal as discussed below, and outputs a down-converted output signal 2012 (red arrow). *Id.* at 9:61-10:20. In this configuration, the switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to e.g., ground. *Id.* at 9:49-53.

Figure 20A-1 (above right) shows an alternative configuration of the universal frequency down-conversion (UFD) module of Figure 20A. In Figure 20A-1, the capacitor 2010 is in series with the input signal 2004 and the switch 2008 is shunted to e.g., ground. *Id.* at 9:53-57.

Nevertheless, the configurations of Figures 20A and 20A-1 operate in the same way. Appx5404(¶ 180).

The ’444 patent discloses various embodiments of receivers into which the aliasing module of Figures 20A and 20A-1 can be incorporated, such as, for example, into the receiver 7000 of Figures 70A and 70A-1.

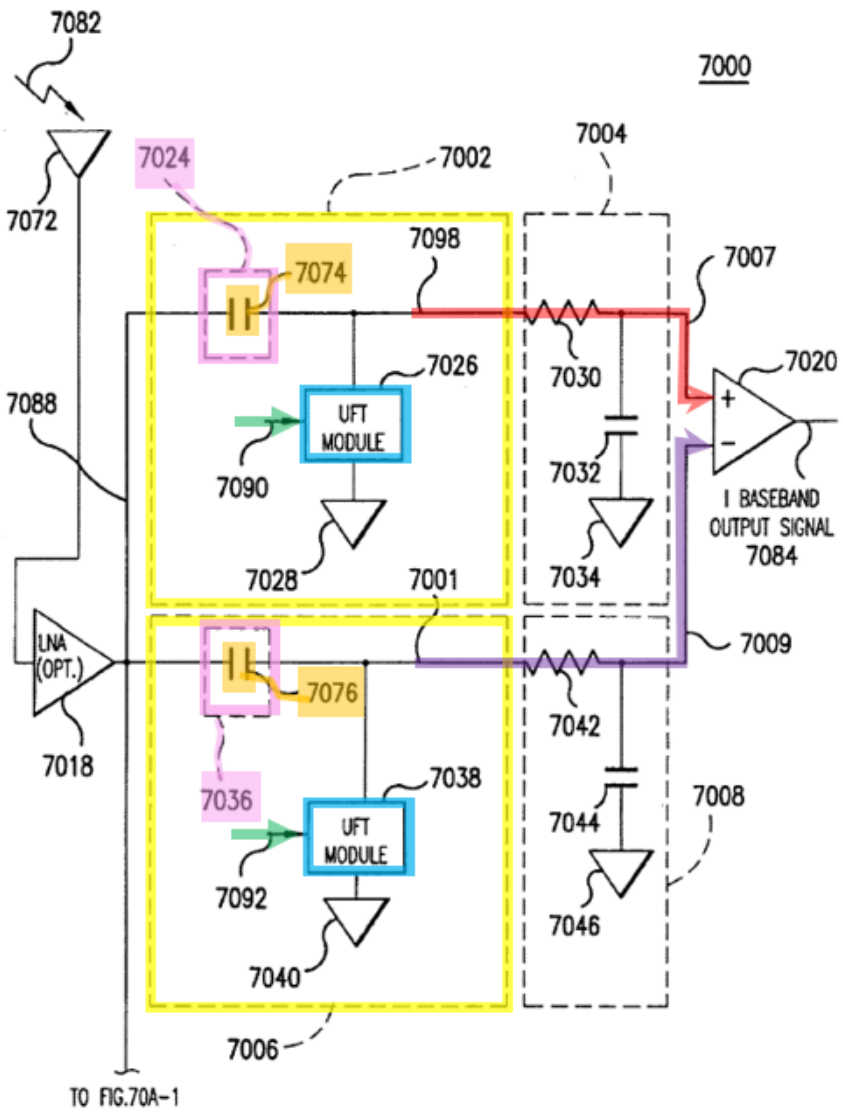


FIG.70A

Figures 70A and 70A-1 illustrate an exemplary I/Q modulation receiver 7000. Appx464(35:36-50). Figure 70A illustrates the portion of the receiver 7000 that handles the I-phase signal and Figure 70A-1 (now shown) illustrates the portion of the receiver 7000 that handles the Q-phase signal. The receiver 7000

receives, down-converts, and demodulates an I/Q modulated RF input signal 7082. *Id.* at 35:51-54.

RF input signal 7082 comprises a first and second information signal that are I/Q modulated onto an RF carrier signal. Appx464(35:54-56). I baseband output signal 7084 (Figure 70A) comprises the first baseband information signal and Q baseband output signal 7086 (Figure 70A-1) comprises the second baseband information signal. *Id.* at 35:56-59.

In particular, antenna 7072 receives I/Q modulated RF input signal 7082, which is sent to a low noise amplifier (LNA) 7018. Appx464(35:60-62). The LNA 7018 amplifies I/Q modulated RF input signal 7082 and sends the amplified I/Q signal 7088 to UFD modules 7002, 7006 (Figure 70A) and UFD modules 7010, 7014 (Figure 70A-1). Appx464(35:62-65); Appx464(36:33-34); Appx465(37:21-22, 57-58).

Other than processing signals with different phase shifts, Figures 70A and 70A-1 operate the same and, thus, the operation of the circuits will be explained in the context of Figure 70A. Figure 70A (above) includes aliasing (UFD) modules 7002, 7006 (yellow) (aliasing modules having the configuration as shown in Figure 20A-1). The UFD modules 7002, 7006 (yellow) include UFT modules 7026, 7038 (blue), respectively, which can include a switch such as shown in Figure 20A-1. Appx464(36:3-7, 38-42). The UFD modules 7002, 7006 also include storage

modules 7024, 7036 (another name for "storage element"). Appx464(36:3-5, 38-40). The specification specifically refers to and identifies storage modules 7024, 7036 (pink) separately from capacitors 7074, 7076 (orange) respectively. Appx464(36:14-15, 50-51).

A switch in the UFT module 7026 is turned ON (closes) and OFF (opens) based on a control signal 7090 (green). Appx464(36:5-7). As the switch opens and closes, a down-converted signal (I output signal 7098) is formed. *See* Section VI.B.1 below; Appx464(36:7-11). The I output signal 7098 may be received by a filter 7004 (which is optional), which filters the signal. Appx464(36:19-32).

Similarly, a switch in the UFT module 7038 is turned ON (closes) and OFF (opens) based on a control signal 7092 (green). Appx464(36:40-42). As the switch opens and closes, a down-converted signal (inverted I output signal 7001) is formed. *See* Section VI.B.1 below; Appx464(36:42-47). The inverted I output signal 7001 may be received by a filter 7008 (which is optional), which filters the signal. Appx464-465(36:55-37:2).

As shown by the red arrow, UFD module 7002 (yellow) outputs an I output signal 7098, which can be filtered to produce a filtered I output signal 7007. As shown by the purple arrow, UFD module 7006 (yellow) outputs an inverted I output signal 7001, which can be filtered to produce a filtered inverted I output signal 7009. Regardless of whether a filter is used, the I output signal and inverted

I output signal are sent to a subtractor module (differential amplifier 7020). The differential amplifier 7020 subtracts the inverted I output signal from the I output signal, amplifies the result, and outputs I baseband output signal 7084. Appx465(37:3-8).

Figures 67A, 67B, 68A, 68B, 69A, 69B, 70Q, 70S, 70S-1 illustrate other receiver embodiments using the aliasing modules of Figures 20A and 20A-1 (although, in certain embodiments, a UFT module can also be implemented as FETs such as shown in Figures 69A, 69B and 70S, 70S-1. Appx464(35:29-35); Appx466(40:65-67).

Similar to Figures 70A and 70A-1, Figures 67A, 67B, 68A, 68B, 69A, 69B, 70Q, 70S, 70S-1 also refer to storage modules 6704A, 6704B, 7024, 7036, 7048, 7060 separately from capacitors. *See*, *e.g.*, Appx463(34:17-30).

The reason the ’444 patent describes a “storage” module/element and a capacitor separately is because a capacitor used as a “storage” module/element is a *specific* implementation where a capacitor is used as an element of an *energy* transfer (*energy* sampling) system (where energy itself becomes part of the baseband/down-converted signal). *See* Section VI.B.1 below.

In other words, whether a capacitor is a “storage” module/element depends on the way in which the capacitor is being used. Just because a capacitor is being used does not mean the capacitor is a “storage” module/element. As discussed in

Section IV.B.2 below, a capacitor(s) is a "holding" module/element when used in a sample-and-hold (*voltage* sampling) system (where voltage readings are used for down-converting a signal).

The Board ignores this critical detail and distinction in its FWD and the import this has to the analysis of "storage element" of claim 3 and Intel's prior art references.

The specification of the '444 patent specifically states that the details regarding the aliasing (UFD) module and down-conversion are set forth in U.S. Patent No. 6,061,551 ("the '551 patent"). Appx5066-5271. Thus, a POSITA would look to and review the '551 patent in order to further his/her understanding of the technology of the '444 patent. Appx5409-5410(¶ 194).

B. The patent discloses two *fundamental different and competing* systems for down-conversion.

The '551 patent and, thus, the '444 patent, goes into great detail regarding the difference between "storage" module/element (which the '551 patent explains is an element of an *energy* transfer (*energy* sampling) system) and a "holding" module/element (which the '551 patent explains is an element of a sample-and-hold (*voltage* sampling) system). Appx5410(¶ 195).

The '551 patent and, thus, the '444 patent discloses two systems for down-conversion: (1) *energy* transfer (i.e., *energy* sampling) and (2) sample-and-hold (i.e., *voltage* sampling). Appx5410(¶ 196). Challenged claim 3 of the '444 patent is

directed to *energy* transfer because the claim uses a term that the patentees *reserved* specifically to connote energy transfer – "*storage* element." *Id.* The patent draws a sharp contrast between a "storage" module/element, which connotes energy transfer (energy sampling), and a "holding" module/element, which connotes sample-and-hold (voltage sampling). *See, e.g.*, Appx5234(66:55-67).

Indeed, as discussed above, energy transfer (energy sampling) and sample-and-hold (voltage sampling) are distinctly different technologies. In energy transfer, the down-converted signal includes the *energy*[3] from the RF signal; in sample-and-hold, the down-converted signal is derived from reading discrete points of *voltage* of the RF signal. *Compare* Appx5234-5235(66:33-68:15) (describing an energy transfer system) *with* Appx5228-5229(54:45-55:29) (describing a sample and hold system). Though energy transfer and sample/hold both result in down-converted signals, an energy transfer system results in a higher quality baseband signal and, therefore, allows for wireless devices with fewer components, reduced size and cost, and increased battery life. Appx5232(62:60-63, 66:34-54); Appx5410-5411(¶ 197).

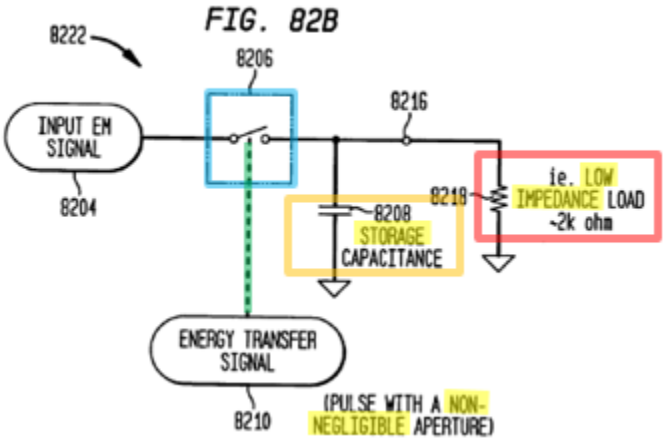
[3] Energy and voltage are not the same thing.

As disclosed in the ’551 patent (and, thus, the ’444 patent), the following table identifies some key features that distinguish energy transfer (i.e., energy sampling) from sample-and-hold (i.e., voltage sampling).

Energy Transfer (*Energy* Sampling)	**Sample and Hold (*Voltage* Sampling)**
Non-negligible sampling aperture	Negligible sampling aperture
“*Storage*” module	“*Holding*” module
Low impedance load	*High* impedance load
Down-converted signal includes the *energy* transferred from the RF signal to the load (i.e., energy sent to the load makes up the down-converted signal)	Down-converted signal is based on discrete *voltage* measurements of the RF signal

1. Energy transfer (*energy* sampling).

Figure 82B of the ’551 patent (below) illustrates an *energy* transfer (*energy* sampling) system, which would be incorporated into a transceiver chip of a wireless device. Appx5412(¶ 199).

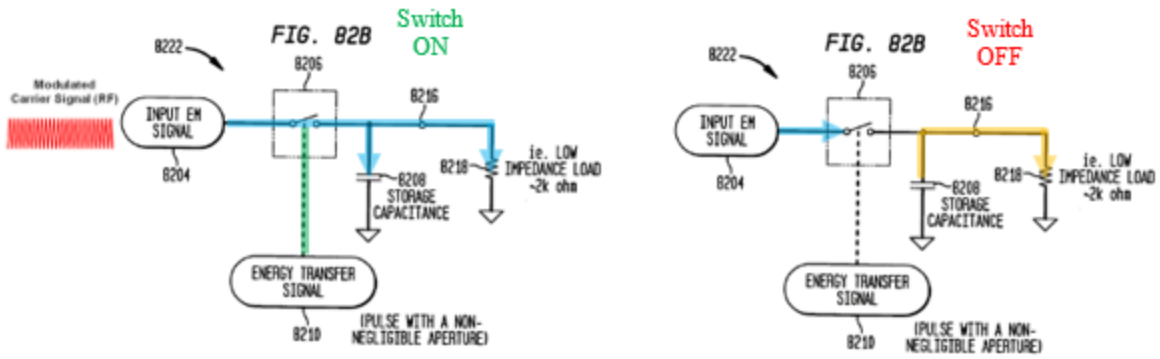


The system includes a switch 8206 (blue), a control signal 8210 (green) for controlling the switch, a “*storage*” capacitor 8208 (orange) for storing *and*

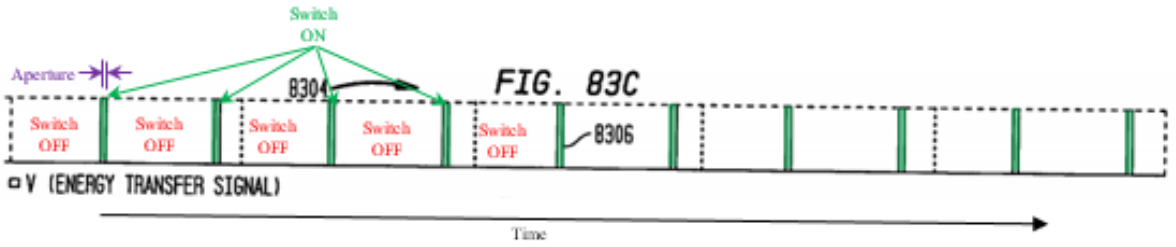
discharging energy, and a *low* impedance load (red).[4] Notably, there are several *key* features (yellow highlights) that distinguish an energy transfer system from sample-and-hold. In particular, an energy transfer system uses (1) a control signal having a pulse with a *non*-negligible aperture/duration, and (2) a "*storage*" capacitor for storing *and discharging non*-negligible amounts of energy for driving a *low* impedance load.[5] Indeed, *low* impedance is what enables a "storage" capacitor to discharge its energy when the switch is OFF (open). If the impedance were high, the "storage" capacitor could *not* discharge sufficient energy for the system to perform energy transfer (energy sampling) and form a down-converted signal from energy transferred to the low impedance load. Appx5412-5413(¶ 200).

[4] All emphasis has been added unless otherwise noted.

[5] Unlike a battery that produces energy, a load is an electrical component (e.g., resistor) that consumes energy (similar to how a light bulb consumes energy). Impedance refers to the opposition that a component presents to the flow of electrical current. A low impedance load is an electrical component that consumes energy and provides low resistance to the flow of current. Appx5413(¶ 200 n.11).



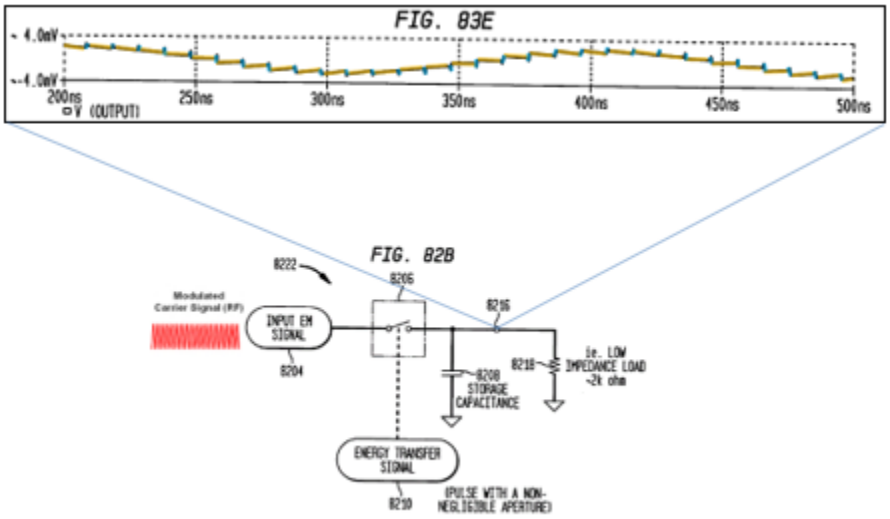
The annotations in Figure 82B above illustrate how an energy transfer system down-converts a high frequency input EM signal 8204 (e.g., modulated carrier signal (red)) to a baseband signal. In particular, down-conversion occurs by repetitively opening and closing the switch 8206. Appx5413-5414(¶ 201).



As shown in Figure 83C above, the switch is turned ON (closed) by sending a pulse 8306 (green) to the switch. The switch is kept ON (kept closed) for the duration of the pulse (i.e., a *non*-negligible aperture (purple) of the pulse). As shown by the repetitive pulses 8306, this opening and closing of the switch repeats continuously over time. Appx5414(¶ 202).

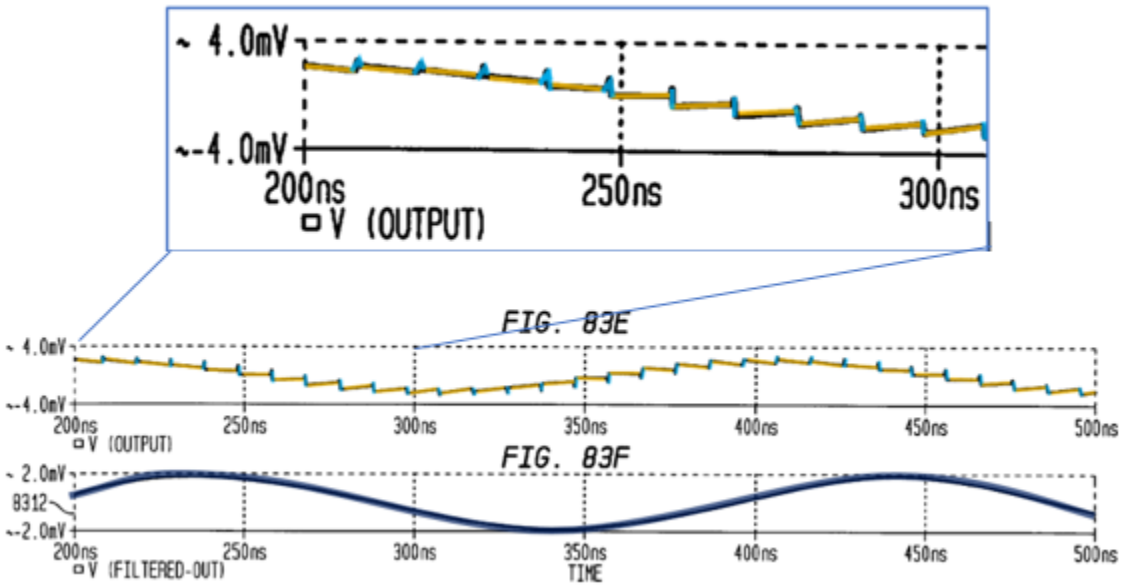
As shown in Figure 82B above (left), when the switch is ON (during the aperture), a portion of the input EM signal 8204 (blue) passes to the "storage"

capacitor 8208 and the low impendence load 8218. When the pulse 8306 (green) stops, the switch is turned OFF (opened), and the input EM signal is prevented from passing through the switch. Since the load is *low* impedance, when the switch is OFF (opened), as shown in Figure 82B above (right), energy (orange) stored in the "storage" capacitor 8208 is discharged to the low impedance load 8218. For this reason, the "storage" capacitor is said to "drive the load." Appx5235(67:42-46); Appx5414-5415(¶ 203).



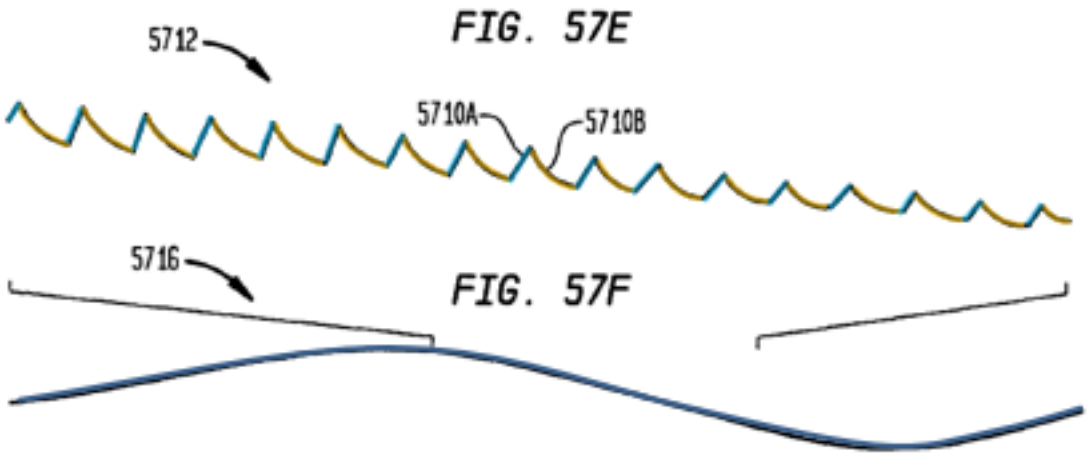
The repetitive opening and closing of the switch results in the waveform (blue/orange) shown above in Figure 83E at terminal 8216. The waveform is made up of energy (blue) from the EM signal and discharged energy (orange) from the "storage" capacitor. Indeed, the discharged energy (orange) from the "storage" capacitor is essential. Without the discharged energy, the waveform of Figure 83E would be incomplete (the orange portions would be missing), thereby producing a

degraded and/or unusable signal that could not be properly processed by a receiving wireless device. Appx5415-5416(¶ 204).



As shown above, the waveform of Figure 83E is filtered to create a smooth waveform (dark blue) as shown in Figure 83F. Appx5235(68:2-4). The smooth waveform is the baseband (audio) signal that was sent from the transmitting wireless device (e.g., Bob's cell). The baseband signal can be processed by the receiving wireless device (e.g., Alice's cell) and Alice can hear Bob's voice. Appx5416 (¶ 205).

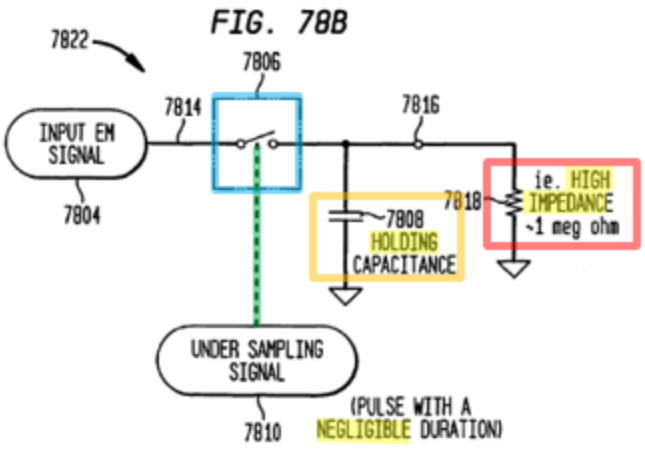
The figures below illustrate a close-up view of another embodiment of a down-converted signal in an energy transfer system. Appx5416-5417(¶ 206).



Figures 57E shows a segment 5712 of the down-converted signal 5716 of Figure 57F. The down-converted signal of Figure 57E is made up of *two* portions - portion 5710A (i.e., energy (blue) from the EM signal) and portion 5710B (i.e., discharged energy (orange) from the "storage" capacitor). Appx5244(85:48-58); Appx5417(¶ 207).

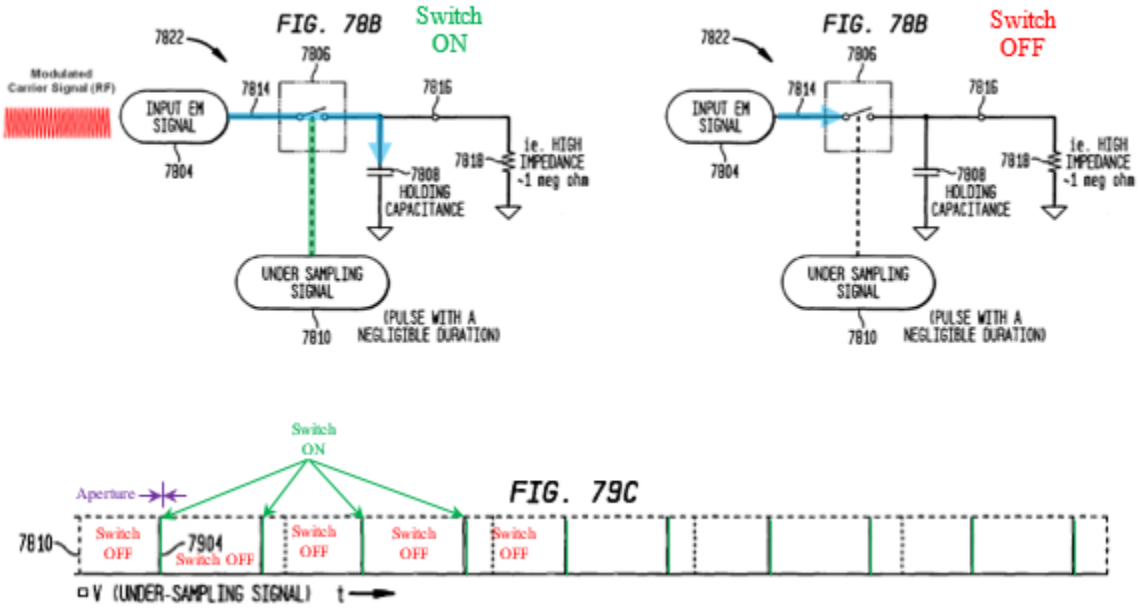
2. Sample-and-hold (*voltage* sampling).

Figure 78B of the '551 patent illustrates a sample-and-hold (*voltage* sampling) system. Appx5417-5418(¶ 208).



The system includes a switch 7806 (blue), a control signal 7810 (green) for controlling the switch, a "holding" capacitor 7808 (orange) for *holding* a voltage across the capacitor, and a *high* impedance load (red). Unlike an energy transfer system, a sample and hold system uses (1) a control signal having a pulse with a *negligible* aperture/duration, (2) a "holding" capacitor for *holding* a constant voltage across the capacitor and (3) a *high* impedance load (yellow highlights). The capacitor is referred to as a "holding" capacitor because, unlike the "storage" capacitor in an energy transfer system, a "holding" capacitor does *not* discharge any significant energy to the load. Indeed, the *high* impedance load is specifically included to *prevent* the holding capacitor from discharging energy, which would degrade the discrete voltage measurements and adversely affect the system performing sample and hold (voltage sampling). Appx5418-5419(¶ 209).

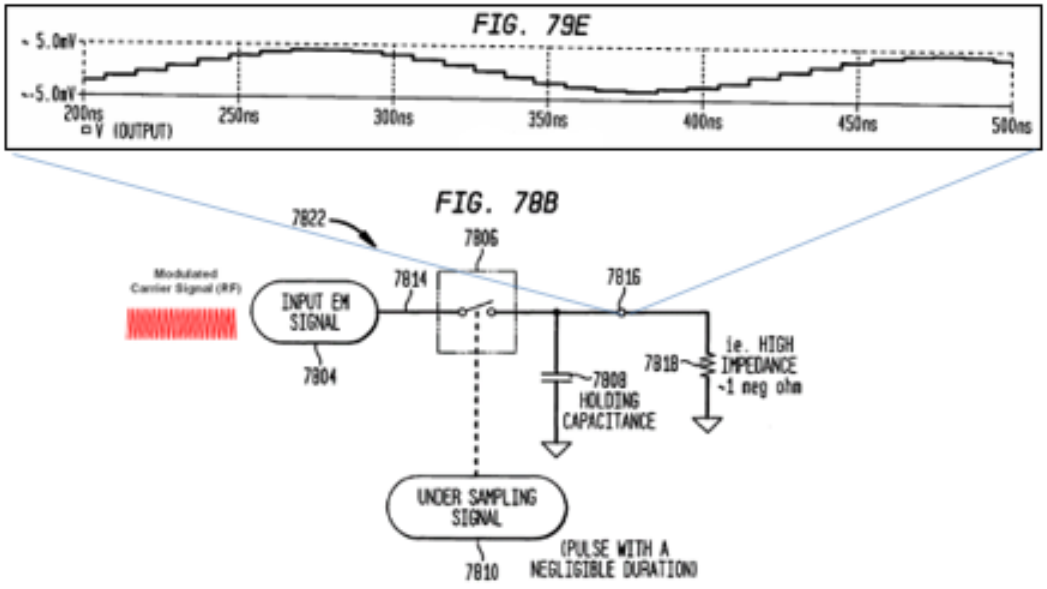
The annotations in Figure 78B (below) illustrate how a sample and hold system down-converts a high frequency input EM signal 7804 (e.g., modulated carrier signal (red)) to a baseband signal. Appx5419(¶ 210).



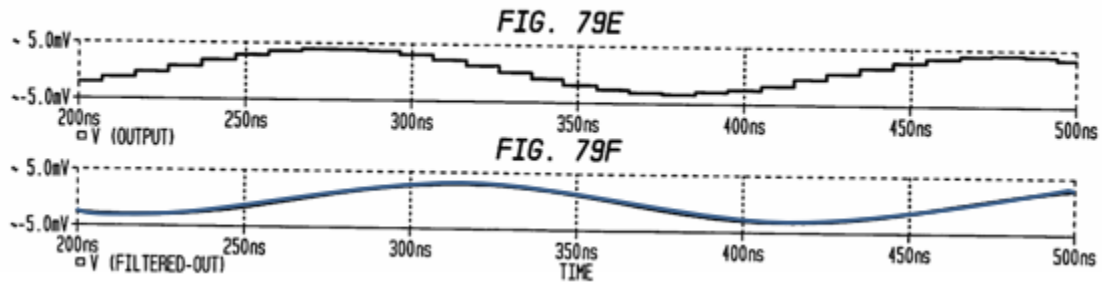
As shown in Figure 79C (above), the switch is turned ON (closed) by sending a pulse 7904 (green vertical line) of an extremely short/negligible duration to the switch. Thus, the aperture (purple) of a pulse is referred to as a *negligible* aperture because the pulse width "tend[s] toward zero time." Appx5233(63:45-47). As shown by the repetitive pulses 7904, this opening and closing of the switch repeats continuously over time. Appx5419(¶ 211).

As shown in Figure 78B above, when the switch is ON (closed) (during the aperture), the EM signal 7804 (blue) is sent to the "holding" capacitor 7808. When the pulse 7904 (green) stops, the switch is turned OFF (opened). But unlike energy

transfer (energy sampling), since sample-and-hold uses a *high* impedance load, when the switch is OFF (opened), there is *high* resistance to the flow of current and, thus, the "holding" capacitor holds a constant voltage value. Because there is no significant energy discharge between pulses, the terminal 7816 maintains a constant voltage value until the next pulse. Appx5233(64:21-26). The voltage value serves as the "sample" of a discrete voltage value that the system uses to recover the baseband signal. In particular, the system uses each discrete change (increase/decrease) in the *voltage* value over time to recover the baseband. This is unlike energy transfer (energy sampling) which uses the *energy* from the input EM signal provided to a low impedance load to recover the baseband. Appx5419-5420(¶ 212).



As shown in Figure 79E (above), sample-and-hold produces a voltage wave with a stair step pattern. The vertical part of the step represents the "sample" of the voltage value which occurs at the time of pulse 7904. The horizontal portion of the step represents the "holding" of that voltage value until the next pulse when the next sample of voltage is taken. Appx5233(64:26-30); Appx5420-5421(¶ 213).



As shown above, the waveform of Figure 79E is filtered to create a smooth waveform (dark blue) as shown in Figure 79F. Appx5233(64:32-34). The smooth waveform is the baseband (audio) signal that was sent from the transmitting wireless device (e.g., Bob's cell). The baseband signal can be processed by the receiving wireless device (e.g., Alice's cell) and Alice can hear Bob's voice. Appx5421(¶ 214).

V. PRIOR ART REFERENCES.

Intel's petition challenged claim 3 under 35 U.S.C. § 103(a) in view of U.S. Patent No. 6,230,000 ("Tayloe") and a Texas Instruments Datasheet for

SN74CBT3253 DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER ("TI Datasheet") (collectively "Ground I")[6].

Tayloe was filed October 15, 1998. At this time, other than non-sampling mixing (e.g., heterodyning), the radio (cellular/wireless) industry was focused on *voltage* sampling solutions for direct down-conversion of RF signals. Appx5432(¶ 240).

Tayloe discloses a *voltage* sampling system for direct down-conversion of an RF signal. Because Tayloe is a *voltage* sampling system, Tayloe does *not* disclose the use of the claimed "*storage* elements" (a term *reserved* for elements of an *energy* transfer (*energy* sampling) system). Instead, Tayloe uses "*holding*" elements which is the term the '444 patent uses to describe elements (e.g., capacitors) of a *voltage* sampling system. Appx54322(¶ 241).

Notably, the word "voltage" is used throughout the Tayloe specification to describe how the circuits disclosed in Tayloe operate. Indeed, a POSITA would understand that *all* of the concepts taught in Tayloe relate to the use of *voltage* and *voltage* sampling to perform down-conversion of an RF signal. The word "energy"

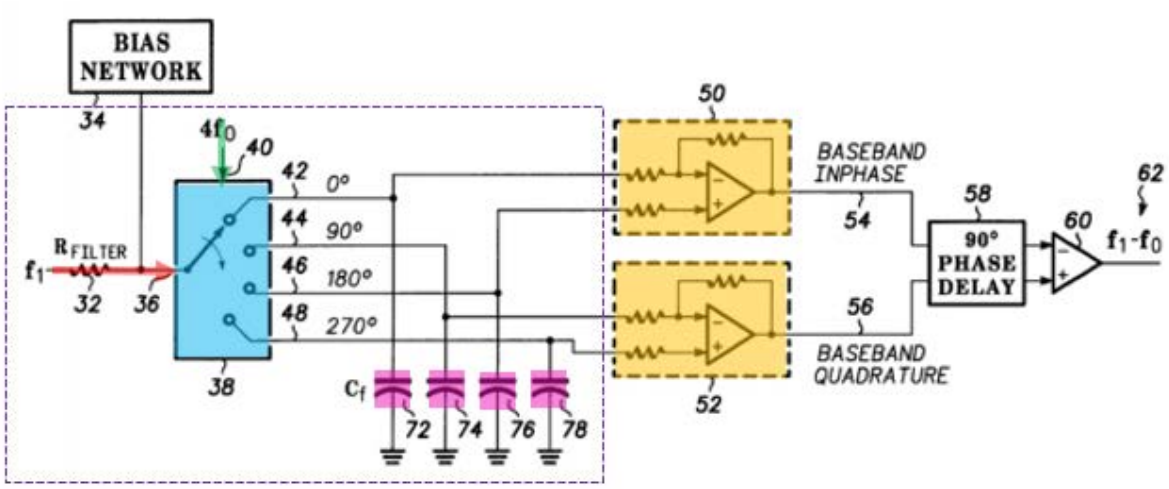
---

[6] The Board did not reach a decision on Ground II of Intel's Petition, Tayloe in view of U.S. Patent No. 4,985,647 ("Kawada"). Appx65. Thus, the scope of this appeal is focused on Ground I.

does *not* appear anywhere in Tayloe *nor* would a POSITA understand Tayloe to disclose, teach or suggest the use of *energy* or *energy* sampling to perform down-conversion of an RF signal. Appx5432-5433(¶ 242).

The "Background of the Invention" section of Tayloe begins by discussing direct down-conversion of RF signals and the problem associated with existing solutions. Appx2698(Figs. 1, 2); Appx2701(1:10-45). Tayloe proposes a method and apparatus that purportedly solves the problem. Appx5433(¶ 243).

Tayloe discloses a product detector (part of a down-converter) for converting an RF signal to a baseband signal using a switch, which samples an RF signal (waveform) during periods of the RF signal. Appx2697(Abstract). "The samples are integrated over time to produce an average *voltage* . . . ." *Id*. According to Tayloe, the "average *voltage*" is the baseband (down-converted) signal. *Id.;* Appx5433(¶ 244).



30 FIG. 3

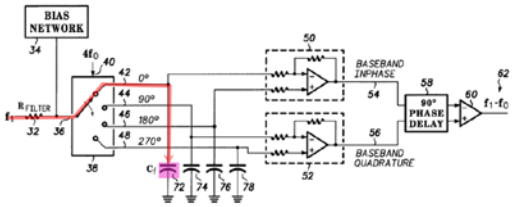
Figure 3 of Tayloe discloses a receiver 30 having a commutating switch 38 (blue), capacitors 72, 74, 76, 78 (pink), and summing amplifiers 50, 52 (orange). Appx2701(2:6-12). Tayloe refers to the area in the purple dashed box as the "product detector" or "Tayloe Product Detector." Appx2702(3:1-4); *see also* Appx5434(¶ 245).

An RF or IF signal f_1 (red arrow) is sent from a radio frequency source to resistor R_{FILTER} 32, which forms a filter when combined with the capacitors 72, 74, 76, 78. Appx2701(2:13-15). The input signal f_1 (red arrow) is subsequently received by the commutating switch 38 (blue). *Id*. at 2:16-17; Appx5434(¶ 246).

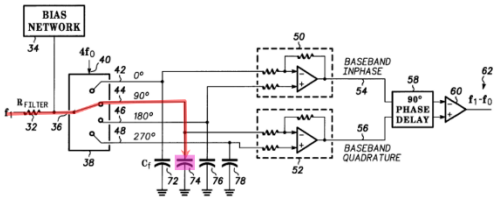
The commutating switch 38 has one input 36 and four outputs 42, 44, 46, 48. Appx2701(2:17-18). Upon receiving a control signal (green) at control input 40, the commutating switch 38 can move to one of four different positions: (1) at time

T1, the commutating switch 38 connects input 36 to output 42, (2) at time T2, the commutating switch 38 connects input 36 to output 44; (3) at time T3, the commutating switch 38 connects input 36 to output 46, and (4) at time T4, the commutating switch 38 connects input 36 to output 48. *Id*. at 2:18-26; Appx5434(¶ 247).

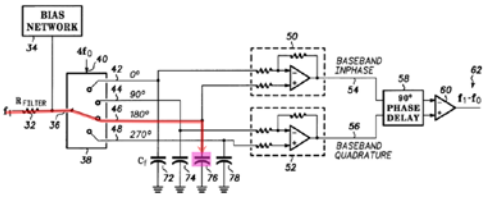
The input 36 is switched to each of the four outputs 42, 44, 46, 48 substantially once during each period of the input signal f_1. Appx2701(2:24-26). The commutating switch 38 remains closed at each of the four outputs for 90 degrees or less of the input signal f_1. Appx2702(3:27-31); Appx5434-5435(¶ 248).



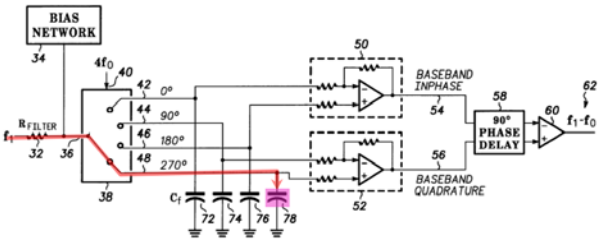
30 FIG. 3



30 FIG. 3



30 FIG. 3

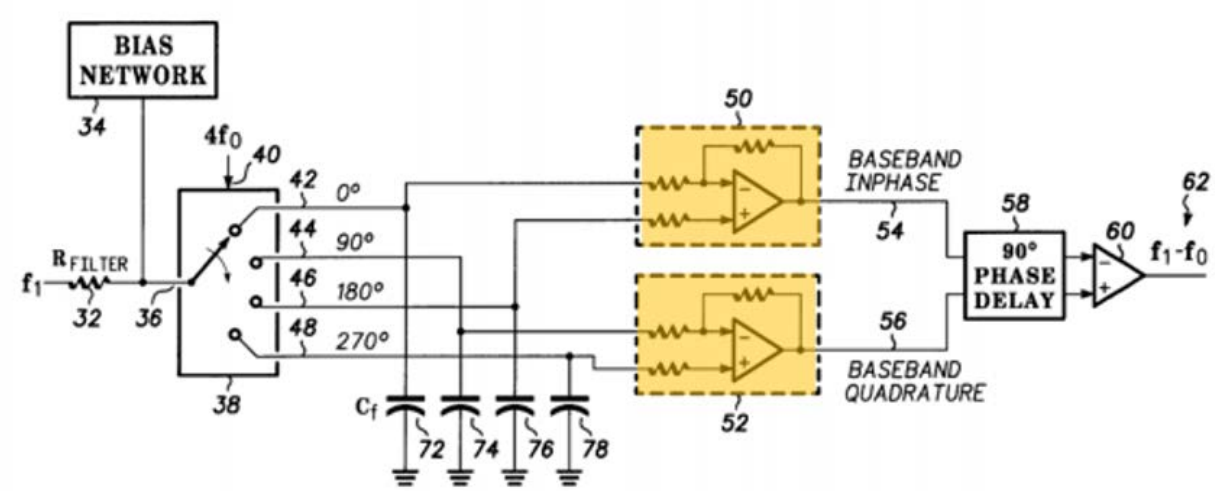


30 FIG. 3

As shown in the figures above, during the time that the commutating switch 38 connects input signal 36 to output 42 (top left), charge builds up on capacitor 72. When the commutating switch 38 connects input signal 36 to output 44 (top right), charge builds up on capacitor 74. When the commutating switch 38

connects input signal 36 to output 46 (bottom left), charge builds up on capacitor 76. When the commutating switch 38 connects input signal 36 to output 48 (bottom right), charge builds up on capacitor 78. Appx2701(2:32-38); Appx5435(¶ 249).

In particular, "[a]s commutating switch 38 cycles through the four outputs, capacitors 72-78 charge to *voltage values* substantially equal to the average value of the input signal during their respective quadrants." Appx2701(2:38-41). According to Tayloe, each of the capacitors function as a separate integrator, which each integrate a separate quarter wave of the input signal f_1. *Id*. at 2:40-43; Appx5435-5436(¶ 250).



30 FIG. 3

As shown above in Figure 3, "the outputs of commutating switch 38 are input to summing amplifiers 50 and 52. Summing amplifier 50 differentially sums

the 0 degree output and the 180 degree output, thereby producing baseband in-phase signal 54. Summing amplifier 52 differentially sums the 90 degree output and the 270 degree output, thereby producing baseband quadrature signal 56." Appx2701(2:56-61); Appx5436-5437(¶ 251).

Figure 4 of Tayloe illustrates how the system uses the input signal f_1 to determine the *voltage* to which to charge each capacitor. Figure 4 shows a waveform 100 includes a signal 125 corresponding to input signal f_1. Appx2702(3:40-42).

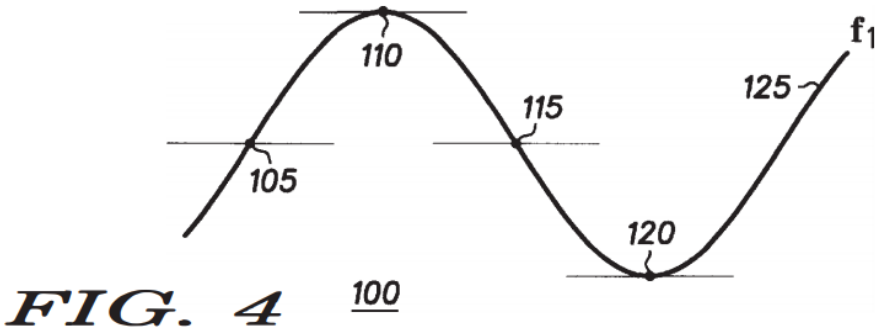


FIG. 4

As shown in Figure 4: "Point 105 represents the *voltage* to which capacitor 72 (FIG. 3) charges. Likewise, point 110 represents the *voltage* to which capacitor 74 charges, point 115 represents the *voltage* to which capacitor 76 charges, and point 120 represents the *voltage* to which capacitor 78 charges." *Id*. at 3:43-48; Appx5437(¶ 253).

According to Tayloe, outputs 42, 44, 46, 48 represent average values of the input signal f_1 during quarter waves of a period. Appx2701(2:45-54).[7] In other words, the points 105, 110, 115, 120 in Figure 4 represent the average value of *voltage* at 0°, 90°, 180°, 270°, respectively, of the input signal f_1. Thus, the capacitors 72, 74, 76, 78 are charging to the average *voltage* as shown by points 105, 110, 115, 120, respectively. Appx5437-5438(¶ 254). *See also* Appx2702(3:44-48); Appx5438(¶ 256).

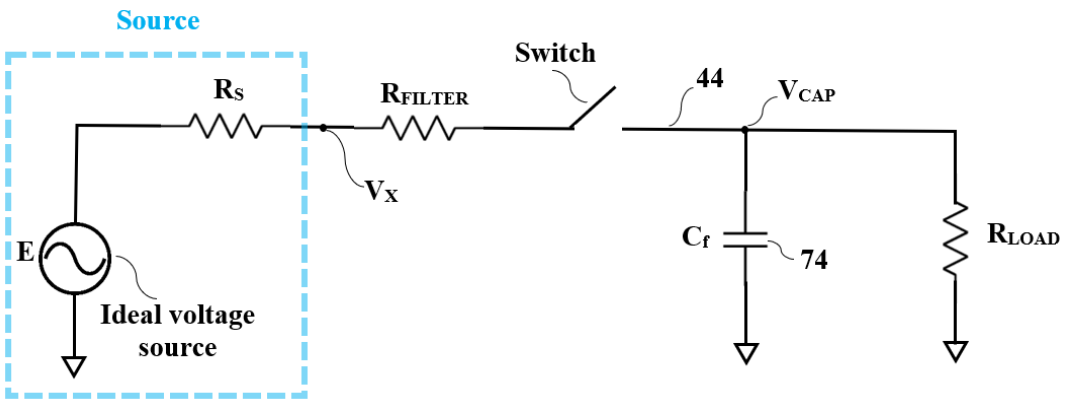
Accordingly, a POSITA would understand that Tayloe is a *voltage* sampling system, which uses a *high* impedance load. The *high* impedance load causes each capacitor of Tayloe to *hold* energy (i.e., *prevent* energy in the capacitor from being discharged to form the down-converted signal) when it is not connected to input 36, so that an accurate voltage across each capacitor can be determined. As the energy is being held, the system determines the voltage across the capacitor (i.e., the voltage level). At the next sampling interval (i.e., when the capacitor is again connected to input 36), the voltage on the capacitor will charge to the next average voltage value. Using multiple voltage readings, the system derives a baseband

[7] Tayloe's use of 25% of the input signal (one quarter of the wave) does not indicate or imply energy transfer. *See* Appx5438(¶254 n. 13).

signal (which is a representation of the original baseband signal sent from the transmitting device).[8] Appx5439-5440(¶ 257).

In order to demonstrate that Tayloe is a *voltage* sampling system, which uses a *high* impedance load, a circuit diagram (below) illustrates a single path of Figure 3 (output 44, capacitor 74 and summing amplifier 52). The analysis below, however, applies to all other paths (and other outputs and capacitors and summing amplifier 54) of Figure 3. Appx5440(¶ 258).

The radio frequency source (shown in the dashed blue box below) is what a POSITA would use to represent the input signal f_1. Appx5440(¶ 259).

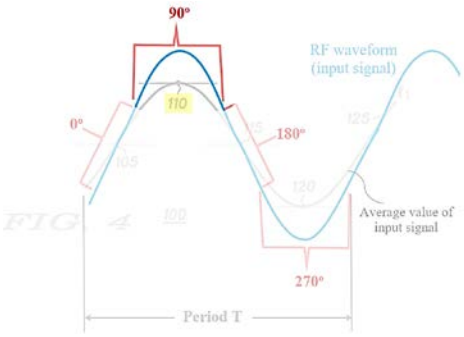


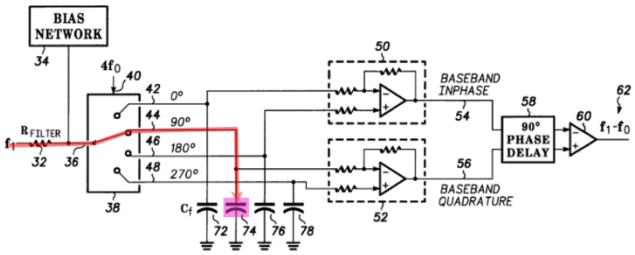
As shown above, a POSITA would model a radio frequency source as having an ideal voltage source and a resistance R_S. Appx5440-5441(¶ 260); *see also* Appx5328-5329; Appx5332; Appx5333-5335.

---

[8] If needed, energy in the capacitor will leave the capacitor and be dissipated in R_{FILTER} 32.

Based on Tayloe's disclosure, R_{LOAD} is ideally infinite so that no current (no energy) flows into R_{LOAD} (i.e., no energy will be discharged to the summing amplifier 52). Although in the real world, as discussed below, R_{LOAD} would be a very *high* value in order for the system of Tayloe to work and, thus, R_{LOAD} is a *high* impedance load. Appx5441(¶ 261).





30 FIG. 3

As shown above right (red path), when the commutating switch 38 closes during the 90° phase of the input signal f_1 (i.e., when the input 36 of the switch is connected to the output 44), capacitor 74 charges to the average *voltage* of the input signal f_1 during the second quarter-wave of the cycle, i.e. at the 90° phase. As shown above left, the average voltage at the 90° phase is represented by point 110 (yellow). Appx2701(2:47-49); Appx2702(4:45-46). When the commutating switch 38 moves to the next phase (the 180° phase), the input 36 of the switch 38 is disconnected from the output 44 (the switch is open for the path (red path)) and the voltage on capacitor 74 is held constant until the switch closes again at the next 90° phase (i.e., the next time the input 36 of the switch is connected to the output

44). The analysis above applies to each path and capacitor. Appx5441-5442(¶ 262).

For the average voltage to be held constant, the voltage on capacitor 74 should not change when the switch is open for the red path. Otherwise, the voltage on capacitor 74 would not be maintained as the average voltage of point 110 and the system could not derive the baseband signal. Appx5442(¶ 263).

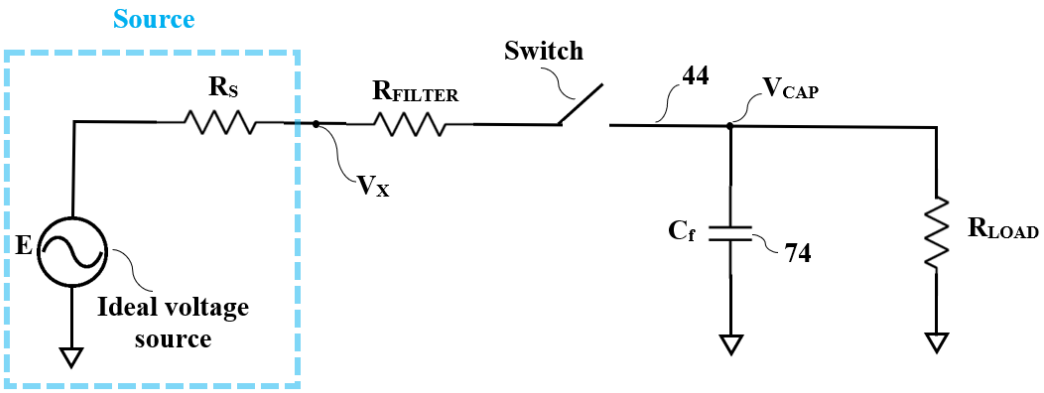
A POSITA knows that for the voltage on the capacitor 74 to equal the average voltage represented by point 110, there is only a small amount of current and, thus, only a small amount of energy flowing through R_{FILTER} 32. And in order for the voltage on the capacitor 74 to equal the average voltage represented by point 110 and be held constant, R_{LOAD} must be very high. Otherwise, current would continuously flow through R_{FILTER} to R_{LOAD}. If current flows through $R_{FILTER,}$ there would be a voltage drop across R_{FILTER} and the voltage on the capacitor, V_{CAP}, could not approximate the average value of the voltage at f_1, V_x, as required by Tayloe. Since Tayloe states that the voltage on the capacitor is the average value of the voltage at f_1, R_{LOAD} must be a *high*-impedance load to prevent the voltage drop across R_{FILTER}. Appx5442-5443(¶ 264).

In view of the forgoing, each summing amplifier 52, 54 must be a *high* impedance load, which will cause the capacitors to *hold* the voltage. In other words, the *high* impedance load *prevents* energy in the capacitor from being

discharged to form the down-converted signal. This demonstrates that Tayloe is a *voltage* sampling system. Appx5443(¶ 265).

Moreover, there is additional evidence that Tayloe is a *voltage* sampling system. In particular, Tayloe asserts that "[o]ne advantage [of the Tayloe Product Detector of Figure 3] is low conversion loss." Appx2702(3:5-6). Tayloe then states that "[t]he Tayloe Product Detector can exhibit less than 1 dB of conversion loss." *Id*. at 3:6-7; Appx5443(¶ 266).

As shown below, this 1 dB conversion loss refers to a *voltage* conversion loss. This voltage conversion loss is the loss of voltage from the output of the radio frequency source to the voltage across the capacitors. Again, capacitor 74 and the average voltage represented by point 110 (which will be referred to as V_{110}) are used to illustrate this point. The analysis below, however, applies to all other paths (and other outputs and capacitors and summing amplifier 54) of Figure 3. Appx5443-5444(¶ 267).

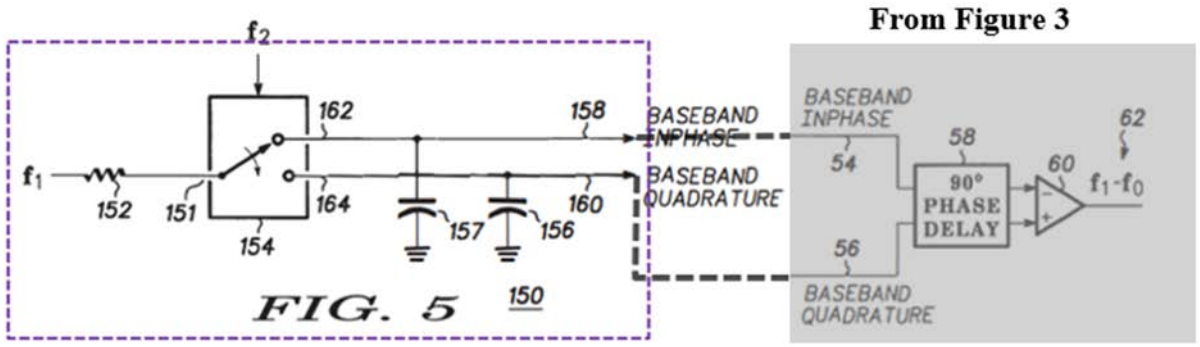


For the 90° path, the voltage conversion loss C_{Lv} is calculated using the following formula. $C_{Lv} = V_{CAP} / V_{110}$. In an ideal circuit, the resistance of the switch (R_{SWITCH}) is 0 ohms, R_{LOAD} is equal to infinite ohms and C_{Lv} equals 1. Appx5444(¶ 268).

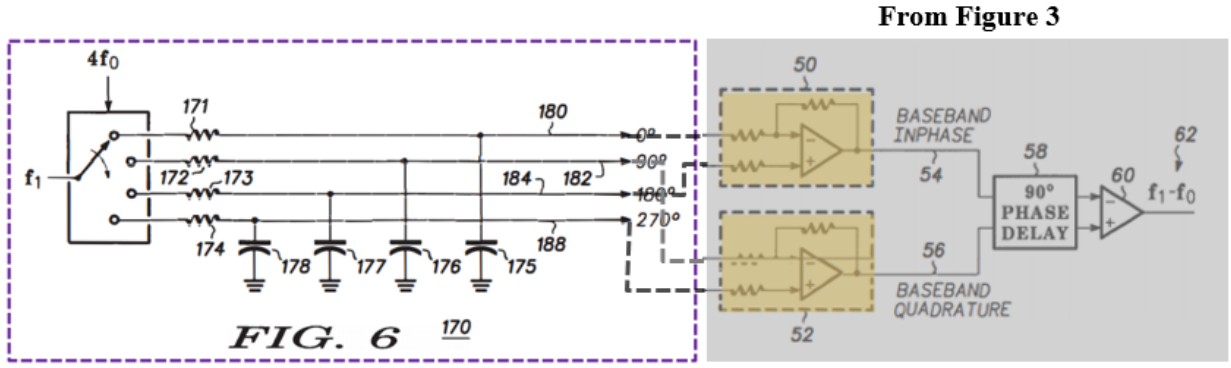
Radio engineers, however, express ratios in decibels, so the formula for conversion loss in decibels is: $C_{Lv}(dB) = -20 \times \log(V_{CAP} / V_{110})$. In an ideal Tayloe circuit, $V_{CAP} = V_{110}$ and $C_{Lv}(dB)$ is equal to 0 dB. Appx5444(¶ 269).

In the real world, however, R_{SWITCH} will not be 0 ohms and R_{LOAD} will not be infinite ohms. So V_{CAP} will be slightly less than V_{110} as long as R_{SWITCH} is very small and R_{LOAD} is very large. For example, if V_{CAP} = 89% of V_{110}, the non-ideal voltage conversion loss will be $C_{Lv} = (V_{CAP} / V_{110}) = 0.89$. In decibels the voltage conversion loss is $C_{Lv}(dB) = -20 \times \log(V_{CAP} / V_{110}) = -20 \times \log(0.89) = 1$ dB. So if R_{SWITCH} is closer to zero ohms and R_{LOAD} is closer to infinity, the voltage conversion loss will be "less than 1 dB" of conversion loss just as Tayloe claims. Appx2702(3:6-7); Appx5444(¶ 270).

In view of the foregoing, Figure 3 of Tayloe is operating as a *voltage* sampling system, ***not*** as an energy transfer (energy sampling) system. Thus, the capacitors 72, 74, 76, 78 are all "holding" elements, not "storage elements" as set forth in claim 3 of the '444 patent. Appx5444-5445(¶ 271).



As shown above, Figure 5 of Tayloe discloses an alternative embodiment of a product detector 150 (purple dashed box). Appx2702(4:9-15). According to Tayloe, "[p]roduct detector 150 can be substituted into direct conversion receiver 30 (FIG. 3)" (*id.* at 4:42-44) and the only difference between Figure 3 and Figure 5 is that Figure 5 only has two outputs. *Id.* at 4:13-15. The circuit of Figure 5 works the same as the circuit of Figure 3 with regards to holding the average voltages on the capacitors and the analysis of Figure 3 above would apply to Figure 5. Appx5445(¶ 272).



As shown above, Figure 6 of Tayloe discloses another alternative embodiment of a product detector 170 (purple dashed box). Appx2702(4:46-49).

As shown above, a POSITA would understand that Figure 6 would be connected to the summing amplifier 50, 52 just like Figure 3. Appx5446(¶ 274).

The circuit of Figure 6 works the same as Figure 3 with regard to holding the average voltages on the capacitors 175, 176, 177, 178 and the analysis of Figure 3 above applies to Figure 6. Appx5446-5447(¶ 275).

Moreover, with regard to Figure 6, Tayloe clearly focuses on *voltage* and how *voltage* is controlled by the combination of the capacitor and resistor. Appx2702(4:49-57). The summing amplifiers 50, 52 and/or other circuitry to the right of the capacitors 175, 176, 177, 178 is a *high* impedance load to each capacitor, which is a characteristic of a *voltage* sampling system. Appx5447(¶ 276).

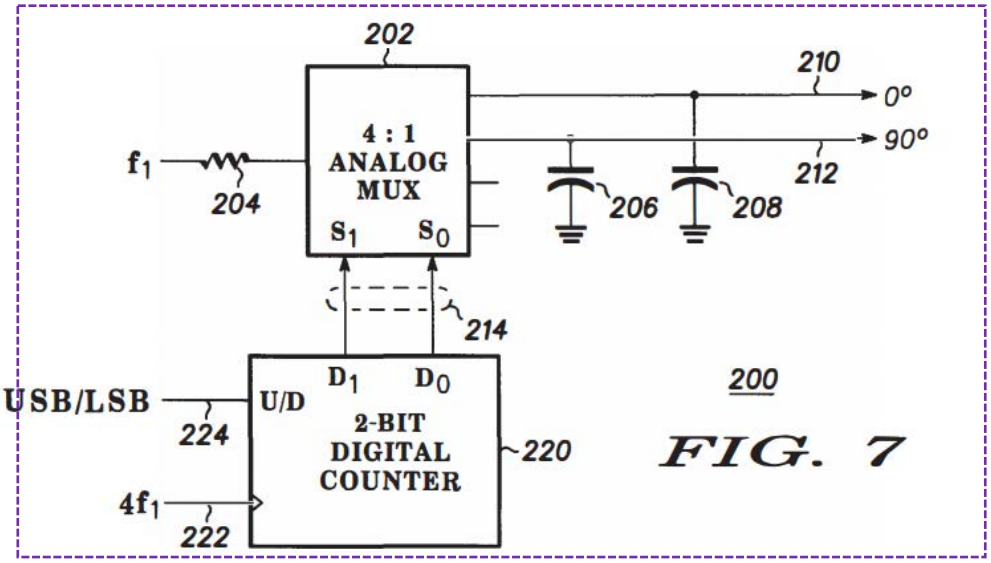


FIG. 7

As shown above, Figure 7 of Tayloe discloses another alternative embodiment of a product detector (purple dashed box). Appx2703(5:1-2). Since

Tayloe refers to Figure 7 as the product detector and Tayloe explains that the receiver design of Figure 7 is "the *same* as direct conversion receiver 30 (FIG. 3)" (other than the analog MUX 202 and a digital counter 220) (*id.* at 5:31-34), a POSITA would understand that if only two outputs 210, 212 are being used, those outputs are connected to summing amplifier 60 (of Figure 3). Appx5448(¶ 278).

Moreover, a POSITA would understand that if output 210, output 212, as well as 180° and 270° outputs are being used, Figure 7 would be connected to the summing amplifier 50, 52 just like Figure 3. Appx5448(¶ 279).

The circuit of Figure 7 works the same as Figures 3 and 5 (depending on how many outputs are used) with regard to holding the average voltages on the capacitors 206, 208 (as well as capacitors for the 180° and 270° paths) and the analysis of Figures 3 and 5 above applies to Figure 7. Appx5449(¶ 280).

In view of the foregoing, Figures 5, 6 and 7 of Tayloe are operating as a *voltage* sampling system. Thus, the capacitors in these figures are all "holding" elements, not "storage elements" as set forth in claim 3. Appx5449(¶ 281).

VI. PROCEDURAL HISTORY.

A. Intel's Petition.

Intel filed its Petition on July 13, 2020. The Petition alleged that claim 3 was obvious in view of Tayloe and the TI Datasheet. Appx563-567. In applying Tayloe, the Petition asserted that capacitors 72, 74, 76, and 78 of Tayloe were the

claimed "storage element." Intel did not propose "storage element" as a term for construction and merely asserted that "[a] capacitor is a well-known storage element." Appx565. That was the entirety of Intel's basis for arguing that Tayloe met this claim element.

Further, the Petition made no mention at all of "non-negligible" amounts of energy or whether a Tayloe capacitor stores "non-negligible" amounts of energy.

The Board instituted the IPR proceeding on January 28, 2021.

B. Patent Owner Response.

On May 11, 2021, ParkerVision filed its Patent Owner Response ("POR"). Adopting the construction of the U.S. District Court for the Western District of Texas ("District Court"), ParkerVision proposed construing "storage element" as "an element of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal." Appx727-728; Appx757-762; Appx770-774.

ParkerVision asserted that claim 3 was patentable over Tayloe, because Tayloe was a voltage sampling system (which the patent describes as using "holding" elements that hold *negligible* amounts of energy) and, thus, the Tayloe capacitors were "holding" elements, not the claimed "storage" element. Appx726-727; Appx796-799.

C. Intel's Reply.

Intel filed its Reply on August 5, 2021. For the first time, Intel provided a construction of "storage element." In doing so, Intel agreed that a "storage element" stores "non-negligible" amounts of energy.[9] Appx821-827. Intel then argued, for the first time, that a Tayloe capacitor stores non-negligible amounts of energy and disclosed *new* evidence –providing an energy calculation and pointing to the size of Tayloe's capacitors. *See e.g.*, Appx830.

D. ParkerVision's Sur-Reply.

On September 14, 2021, ParkerVision filed its Patent Owner Sur-Reply ("POSR"). ParkerVision pointed out that the District Court considered and reaffirmed its construction of "storage element" in another litigation. Appx873-877. Moreover, based on the positions contained in its POR, ParkerVision refuted the arguments in Intel's Reply and explained why (1) the capacitors of Tayloe only hold negligible amounts of energy, and (2) the "operational amplifier" of Tayloe is a high impedance load. Appx866-877.

---

[9] In asserting that the construction of "storage" element is not limited to an element of an "energy transfer system," Intel made the same claim construction arguments to the Board that the District Court previously rejected.

In particular, ParkerVision used a set of calculations in its POSR, demonstrating that the claimed storage elements stored non-negligible amounts of energy (nearly 60% of the available energy) relative to the input signal, while Tayloe's capacitors only held negligible amounts of energy (nearly zero). Appx877-889.

E. Intel's motion to exclude.

On October 7, 2021, Intel moved to exclude portions of the POSR, alleging that it violated PTAB procedural rules and was unfairly prejudicial to Intel. Appx936-953. ParkerVision opposed Intel's motion.

In a pre-hearing conference on October 27, 2021, the Board excluded portions of the POSR related to ParkerVision's arguments that Tayloe capacitors do not store "non-negligible" amounts of energy. Appx55-56.

The parties conducted oral argument on November 1, 2021.

SUMMARY OF THE ARGUMENT

The PTAB's claim construction of "storage element" is wrong. Thus, the PTAB erred in finding claim 3 invalid in view of that erroneous construction. But even if the PTAB's construction were correct—which it is not—the PTAB still erred in finding claim 3 invalid, because the prior art does not disclose elements that store non-negligible amounts of energy from an input EM signal.

Further, the PTAB erred by basing its patentability decision on theories not presented in the Petition but instead, were raised for the first time (and based on new evidence) in Intel's Reply.

Finally, the PTAB abused its discretion by excluding certain arguments in the POSR. Contrary to PTAB's finding, Patent Owner's arguments were based on positions in its POR and responded to newly-raised arguments in Intel's Reply.

ARGUMENT

VII. STANDARDS OF REVIEW.

Obviousness is a legal question based on underlying findings of fact. *Univ. of Strathclyde v. Clear-Vu Lighting LLC*, 17 F.4th 155, 160 (Fed. Cir. 2021). The Court reviews the Board's ultimate obviousness determination de novo and underlying factual findings for substantial evidence. *LG Elecs. Inc. v. Immervision, Inc.*, Case No. 21-2037, 2022 U.S. App. LEXIS 18948, at *11 (Fed. Cir. July 11, 2022). "The substantial evidence standard asks 'whether a reasonable fact finder could have arrived at the agency's decision.'" *OSI Pharms., LLC v. Apotex Inc.*, 939 F.3d 1375, 1381–82 (Fed. Cir. 2019) (quoting *In re Gartside*, 203 F.3d 1305, 1312 (Fed. Cir. 2000)).

"The PTAB's evidentiary rulings are reviewed on the standard of abuse of discretion." *Vidstream LLC v. Twitter, Inc.*, 981 F.3d 1060, 1064 (Fed. Cir. 2020) (citing *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1078 (Fed Cir. 2015)). "Abuse

of discretion arises if the ruling: '(1) is clearly unreasonable, arbitrary, or fanciful; (2) is based on an erroneous conclusion of law; (3) rests on clearly erroneous fact findings; or (4) follows from a record that contains no evidence on which the Board could rationally base its decision.'" *Vidstream*, 981 F.3d at 1064 (quoting *Chen v. Bouchard*, 347 F.3d 1299, 1307 (Fed. Cir. 2003)).

VIII. PTAB'S INVALIDATION OF CLAIM 3 WAS IMPROPER BECAUSE IT IS BASED ON AN INCORRECT CONSTRUCTION OF "STORAGE ELEMENT."

A. The Board's construction of "storage element" is wrong.

Claim 3 includes the term "storage element." Before the PTAB's FWD, the District Court already considered and construed this term on *three* separate occasions in litigations against Intel, TCL, and Hisense. The District Court consistently maintained its construction (which ParkerVision adopted as its proposed construction in the IPR) — "an element of an *energy transfer system* that stores non-negligible amounts of energy from an input electromagnetic signal." Appx5310-5311; Appx4949; *ParkerVision, Inc. v. Hisense Co., Ltd. et al.*, Case No. WDTX-6-20-cv-00870, D.I. 51 at 5 (W. D. Tex. Oct. 29, 2021).

The Board considered the ***exact*** same arguments that Intel twice made to the District Court (and the court twice rejected). And despite being aware of the District Court's construction, the Board afforded no deference to the District Court and expressly rejected its construction. Instead, the Board found that "one of

ordinary skill in the art would understand 'storage element' to mean 'an element of a *system* that stores non-negligible amounts of energy from an input EM signal.'" Appx41. The Board's finding and rationale are wrong.

1. The intrinsic evidence supports ParkerVision's construction.

"*Storage* element" is a claim term reserved exclusively for a component of an energy transfer (energy sampling) system. On the other hand, a "holding" element is a term reserved exclusively for a component of a voltage sampling system. The patent specification distinguishes clearly between the two. Thus, a "storage" element must be construed in a way that distinguishes it from a "holding" element.[10] The distinctions between a "storage" element in an energy transfer system and a "holding" element in a sample-and-hold/voltage sampling system are spelled out in the patent specification. Yet, this is what the Board ignores.

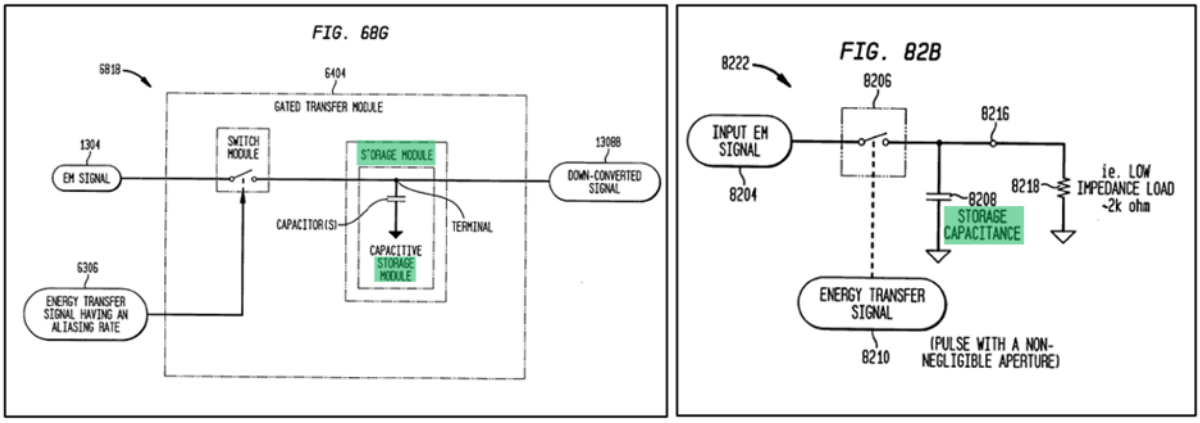
---

[10] *See Apple Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 708 (Fed. Cir. 2020) ("As we have held, '[when] the patent describes multiple embodiments, every claim does not need to cover every embodiment. This is particularly true [when] the plain language of a limitation of the claim does not appear to cover that embodiment.'").

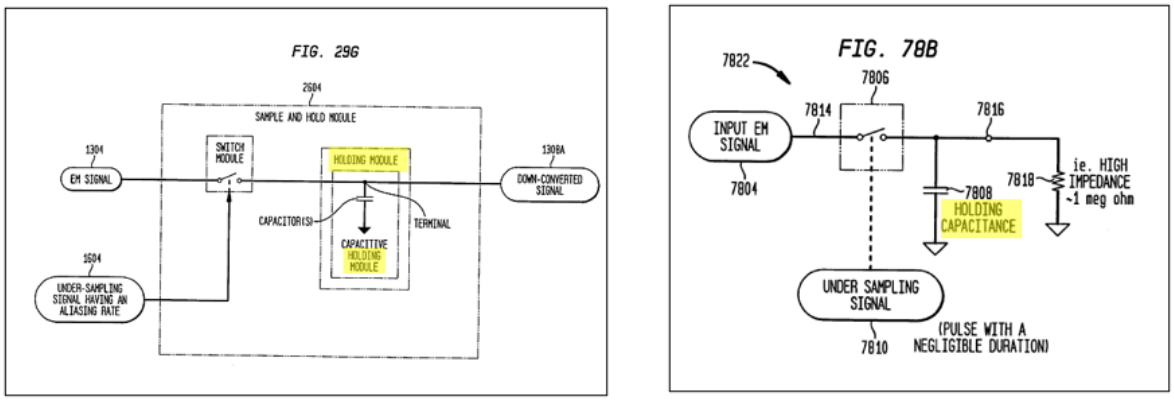
The Board agrees that a "storage" element "stores non-negligible amounts of energy from an input electromagnetic (EM) signal." But this feature alone does not distinguish a "storage" element from a "holding" element. There is a key distinguishing feature—the "storage" element is part "of an energy transfer system."

Unlike an energy *transfer* system which, as the name implies, uses a low impedance load to *transfer* (discharge) non-negligible amounts of energy, a sample-and-hold (voltage sampling system) uses a high impedance load to *hold* (i.e., not transfer/discharge) voltage/charge. In other words, whereas a "storage" element stores energy for subsequent transfers/discharges of energy, a "holding" element is "holding a voltage value." Appx771. Indeed, the specification specifically calls out driving a low impedance load as a "benefit" of an energy transfer system. Appx5235(67:37-46). Without a "storage" element driving a low impedance load, sufficient energy could not be transferred/discharged from the "storage" element in order to recover a down-converted signal from an input EM signal. Thus, the specification is clear that the term "storage" element is specific to an "energy transfer system" and a "holding" element is specific to a sample-and-hold/voltage sampling system.

In addition to the textual description in the specification, this distinction between "storage" and "holding" elements is readily apparent in the patent figures.



Energy transfer system



Sample and hold system

For example, as shown in Figures 68G and 82B above, when discussing an energy transfer system, the specification uses the term "storage" module/capacitance (green). *See also* Appx5149(Figs 65); Appx5153-5155(Figs. 68A-G); Appx5161(Fig. 74); Appx5173(Figs. 82A-82B); Appx5189(Fig. 95). But as Figures 29G and 78B show above, when discussing a sample-and-hold system, the specification uses the term "holding" module/capacitance (yellow). *See also id*.

at Appx5097(Fig. 24A); Appx5101(Fig. 27); Appx5103-5105(Figs. 29A-G); Appx5121(Fig. 42); Appx5149(Fig. 65); Appx5169(Figs. 78A-78B).

Moreover, the patents include a section entitled "0.1.2 Introduction to *Energy Transfer*", which states:

> FIG. 82A illustrates an exemplary *energy transfer system* 8202 for down-converting an input EM signal 8204. The *energy transfer system* 8202 includes a switching module 8206 and a *storage module* illustrated as a *storage* capacitance 8208. The terms *storage module and storage capacitance*, as used herein, are *distinguishable* from the terms *holding module and holding capacitance*, respectively. *Holding modules and holding capacitances*, as used above, *identify systems* that store negligible amounts of energy from an under-sampled input EM signal with the *intent of 'holding' a voltage value*. *Storage modules and storage capacitances, on the other hand, refer to systems* that store non-negligible amounts of energy from an input EM signal.

Appx5234(66:55-67); *see also* Appx5228-5231(54:20-59:19) (sample-and-hold systems); Appx5234-5235(66:35-68:15); Appx5250-5252(97:39-101:32) (energy transfer systems).

Notably, the Board recognized that there are only two systems disclosed in the patent: (1) energy transfer and (2) under-sampling. Appx33-34. The Board also acknowledged that a "holding module" is "expressly link[ed]" to an under-sampling system. Appx37 ("The above-quoted paragraph of the '551 patent

expressly links 'holding module' to an under-sampling method, by expressly including the phrase 'from an under-sampled input EM signal."). Logically, if there are only two systems and a "holding" element is only used in an "under-sampling" system, then, consistent with ParkerVision's construction, a "storage" element must necessarily be an element of an energy transfer system.

Indeed, as previously discussed, the specification makes it clear that "storage" elements are inseparably intertwined with energy transfer systems.

2. The Board's construction is technically and legally wrong.

The Board's construction incorrectly omits the fact that, based on the patent's disclosure, a storage element is a component of an "energy transfer system." In particular, the Board points to a single sentence from the specification (shown in the passage in red above) and asserts that this one sentence, standing alone, is enough to define "storage element." The Board asserts that the last sentence (in red above) is lexicography and ignores the specification's full description.

But this last sentence is *not* a lexicographic definition of storage element. The sentence is comparative, not definitional.

In particular, the entire passage quoted above focuses on characteristics of *systems*. Specifically, the passage states that holding and storage modules/capacitances "identify"/ "refer to" *systems* that have certain

characteristics—storing negligible or non-negligible amounts of energy. When read in context, this passage describes the operation of an element in an energy transfer system (i.e., the "storage capacitance" and "storage module") as compared to the operation of the corresponding element in a sample-and-hold/voltage sampling system (i.e., the "holding capacitance" and "holding module"). The Board's reliance on, and misreading of the last sentence (in red above), is not only wrong but *cannot* negate the entirety of the specification's teachings regarding "storage element." *See, e.g., Baxalta Inc. v. Genentech, Inc.* 972 F.3d 1341, 1346-47 (Fed. Cir. 2020).

Notably, in its FWD, the Board expressly qualified its claim construction analysis, stating that while the Board had considered the District Court's claim construction "to the extent possible on the record before us," "the district court's claim construction is set forth in a chart format without providing the benefit of the district court's informed analysis as to how that construction was determined," and that "the lack of explanation is particularly of note here because the district court did not adopt either party's proposed construction in full." Appx31.

But the District Court has now provided the guidance the Board was looking for. Appx5877-5921 (*ParkerVision, Inc. v. LG Electronics, Inc.*, Case No. 6:21-cv-00520-ADA, D.I. 55 (W.D. Tex., June 21, 2022)). The District Court's decision

confirms for a *fourth* time[11] that the Board and Intel's construction for "storage element" is incorrect.

In particular, in a *recent* a claim construction order, Magistrate Judge Gilliland construed "storage element" consistent with ParkerVision's (and the District Court's prior constructions) and *expressly* disagreed with the Board's construction. The court held "the PTAB incorrectly put too much weight and focus on the alleged definitional sentence while also incorrectly ignoring teachings found throughout the specification." Appx5895.

Specifically, the court analyzed the single sentence that the Board relied upon, finding that it did not "rise[] to the 'exacting standards' necessary for lexicography" because, *inter alia*, the language of the sentence itself references additional context of the technical disclosure. Appx5892 (quoting *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014)). The court further found that, given the technical context, a POSITA "would likely understand that the storage capacitance's place and role in an electrical system—and not any inherent property of the storage capacitance itself—is why the storage

[11] The Western District of Texas has construed the "storage element" term in *four* separate cases, three of which specifically involved claim 3 of the '444 patent, and *each time*, the district court limited term to "an energy transfer system."

capacitance[/element] only stores a non-negligible amount of energy from an input EM signal." Appx5892-5893. And in the context of the passage as a whole, "a POSITA would understand this snippet as describing that one can identify whether a system is an energy transfer system or a sample-and-hold system based on how the capacitor operates within the system and/or its size (for a given input EM signal, sampling aperture, and load impedance)." Appx5893.

The court also found that the specification as a whole provides "definitive confirmation that the patentees did not intend for the [] sentence [in question] to be a lexicographical statement," because the specification repeatedly compares storage elements "in the context of an energy transfer system" with holding elements "in the context of a sample-and-hold system." The court concluded that the patentees did not "clearly express an intent' to [define] the term," but rather simply contrast the operation of the capacitor in an energy transfer system with the capacitor in a sample-and-hold system. Appx5894.

3. ParkerVision's prior arguments do not support the Board's construction.

The Board relies on ParkerVision's proposed construction of "storage module" in IPR2014-00948 from 2014 as supporting its determination that the patentees acted as lexicographers. Appx39. But as this Court is aware, in 2014, the USPTO used the broadest reasonable interpretation (BRI) standard for construing terms—a different standard than the one federal courts use under *Phillips v. AWH*

Corp., 415 F.3d 1303 (Fed. Cir. 2005) and its progeny. Indeed, in 2018, the USPTO eliminated the BRI standard and harmonized the USPTO standard with the standard federal courts use.

Further, the Board implies that during the IPR, ParkerVision conceded that the last sentence (in red above) alone is lexicography. But the Board is wrong. ParkerVision did no such thing. More specifically, the Board points to ParkerVision's statement that "[t]he Specification provides an explicit definition that supports this construction." Appx39. The Board fails to mention that when ParkerVision made these statements, ParkerVision pointed to the same passage quoted above *in its entirety*, *not* merely the last sentence in red.

For the reasons set forth above, "storage element" should be construed as "an element of an *energy transfer system* that stores non-negligible amounts of energy from an input electromagnetic signal." The Court should therefore reverse the Board's decision and remand for further proceedings based on the correct construction.

B. Under the proper construction, Tayloe does not disclose a "storage element."

As discussed in above, a "storage element" is an element of an "energy transfer system." Tayloe discloses a voltage sampling system; thus, the Tayloe capacitors are not elements of an energy transfer system. *See* Section V. Moreover, as discussed in Section XI below, Tayloe capacitors do not store non-negligible

amounts of energy. Under the proper construction, claim 3 is not obvious in view of Tayloe.

IX. THE BOARD ERRED BY BASING ITS UNPATENTABILITY DECISION ON THEORIES NOT PRESENTED IN THE PETITION.

The Board may not base its patentability decision on evidence and theories not presented in the Petition. *See Dell Inc. v. Acceleron, LLC*, 818 F.3d 1293, 1301 (Fed. Cir. 2016). Yet, that is what the Board did here.

A patent owner must be given adequate notice of the unpatentability theories and evidence it faces, so that it may rebut those theories and evidence in its Patent Owner Response. *Id.; Belden, Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1080 (Fed. Cir. 2015). Indeed, 35 U.S.C. § 312(a)(3) requires that all of the Petitioner's arguments and evidence must be presented "with particularity" in the petition. *Intelligent Bio-Systems, Inc. v. Illumina Cambridge, Ltd*., 821 F.3d 1359, 1369 (Fed. Cir. 2016). This is because "[u]nlike district court litigation—where parties have greater freedom to revise and develop their arguments over time and in response to newly discovered material—the expedited nature of IPRs bring with it an obligation for petitioners to make their case in their petition to institute." *Id.;* see *also In re NuVasive, Inc*., 841 F.3d 966, 969-73 (Fed. Cir. 2016).

The Board, however, invalidated claim 3 in view of Tayloe based on an untimely disclosed theory that was not presented in Intel's Petition. The Board's determination of unpatentability was therefore improper and should be reversed.

In particular, Intel's Petition did not provide a construction of "storage element." Moreover, Intel merely identified a "storage element" as capacitor 72, 76 in Tayloe and stated that "[a] capacitor is a well-known storage element" Appx564-566. This is all that Intel said as to this claim element.

Then, for the first time in its Reply, Intel defined "storage element" as "an element that stores a nonnegligible amount of energy from an input electromagnetic (EM) signal," and addressed Tayloe capacitors storing non-negligible amounts of energy. Appx831-838. In doing so, Intel submitted new evidence – a supplemental declaration from Intel's expert, Dr. Subramanian, newly "analyzing the amount of energy stored by Tayloe's capacitors." Appx4769-4774.

A reply, however, "may only respond to arguments raised in the . . . patent owner response . . . ." 37 C.F.R. § 42.23(b). *See Intelligent Bio-Systems*, 821 F.3d at 1366, 1369-70 (affirming the Board's finding that the petitioner "ran afoul of § 42.23(b) by presenting a new argument for the first time in its reply brief"); *SAS Institute Inc. v. Iancu*, 138 S.Ct. 1348 (2018).

By arguing (and presenting never before disclosed evidence) that capacitors in Tayloe "store non-negligible amounts of energy," Intel proceeded in a new direction with a new approach compared to the positions it took in the Petition.

Based on Intel's impermissible new theory, the Board determined that "Tayloe's capacitors 72–78 teach the recited 'storage element' because Petitioner

establishes sufficiently that Tayloe's capacitors are 'element[s] of a system that store[] non-negligible amounts of energy from an input EM signal.' Appx57. The Board relied on Dr. Subramanian's newly-disclosed analysis discussing the size of the capacitor and including an equation for calculating the amount of energy that a capacitor stores.

Intel had no basis whatsoever and zero record evidence in its Petition to show that Tayloe's capacitors store non-negligible amounts of energy. For this reason alone, Intel's Petition failed to meet its burden. The Petition was completely silent as to whether a Tayloe capacitor stores "non-negligible" amounts of energy. Appx566-567. This lapse cannot be fixed in a reply. But this is what the Board allowed Intel to do.

Because Intel's new theory and Subramanian analysis are untimely, the Board's reliance on them is improper. Indeed, the Board should not have considered them at all. *Intelligent Bio-Systems*, 821 F.3d at 1366, 1369-70; *see also*, *SAS Institute Inc. v. Iancu*, 138 S.Ct. 1348 (2018).

X. THE BOARD ABUSED ITS DISCRETION BY STRIKING ARGUMENTS PROPERLY RAISED IN PARKERVISION'S SUR-REPLY.

To make the matter worse, the Board abused its discretion by striking the very portions of ParkerVision's Sur-Reply that addressed Intel's newly-raised arguments.

A sur-reply, however, is supposed to afford a patent owner the opportunity to respond to arguments raised in the corresponding reply. 37 C.F.R. § 42.23(b). "In most cases, the Board is capable of identifying new issues or belatedly presented evidence . . . and disregarding any new issues or belatedly presented evidence . . . ." Consolidated TPG, 80.[12] "As such, striking the entirety or a portion of a party's brief is an exceptional remedy that the Board expects will be granted rarely." *Id.*

Here, the Board's "exceptional remedy" of striking portions of ParkerVision's Sur-Reply is wholly unjustified and should be reversed. Contrary to the Board's assertion, the arguments presented in ParkerVision's Sur-Reply did not introduce a "new theory" nor "proceed in a new direction with a new approach." Instead, ParkerVision's Sur-Reply arguments properly built on arguments already in its POR and responded to arguments and evidence raised, for the first time, in Intel's Reply.

A. ParkerVision's Sur-Reply arguments did not "proceed in a new direction."

ParkerVision's Sur-Reply does not contain any "new theory." Rather, the arguments in ParkerVision's Sur-Reply are simply an expansion of previously

[12] *See* https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf

argued rationale, which this Court has deemed permissible. *See Ericsson Inc. v. Intellectual Ventures I LLC*, 901 F.3d 1374 (Fed. Cir. 2018).

The Board justified excluding ParkerVision's arguments by alleging "Patent Owner did not assert, in its Patent Owner Response, that Tayloe's capacitors did not teach a 'storage element' because they did not *store a non-negligible amount of energy*." S*ee* Appx68. But that is incorrect.

In the POR, ParkerVision argued that Tayloe did not disclose the claimed "storage element" under ParkerVision's construction. *See* Appx5451(¶ 287) ("none of the capacitors in Tayloe is an "element of an energy transfer system that *stores non-negligible amounts of energy* from an input electromagnetic signal.").

In particular, ParkerVision argued that Tayloe is a voltage sampling system—a *fundamentally different and competing* technology to energy transfer (energy sampling). *See* Appx743; Appx778. As ParkerVision pointed out, Tayloe uses "holding elements" which is the term the '444 patent uses to describe elements (such as capacitors) of a *voltage sampling system* that "store *negligible amounts of energy* from an under-sampled input EM signal with the intent of 'holding' a voltage value." Appx771; Appx797.

The POR noted that the '444 patent draws a sharp contrast between a "storage" element, which connotes energy transfer (energy sampling), and a "holding" element, which connotes sample-and-hold/voltage sampling. Appx755.

The POR also provided a detailed explanation of the differences between energy transfer (energy sampling) and sample-and-hold. To that end, ParkerVision noted that while a "storage" capacitor of an energy transfer system stores and discharges non-negligible amounts of energy, Appx757, a "holding" capacitor of a sample-and-hold/voltage sampling system holds a constant voltage across the capacitor and does not discharge any significant energy to the load. Appx763.

Moreover, ParkerVision analyzed the Tayloe circuit and explained that the capacitors in Tayloe hold *negligible* amounts of energy. When discussing Tayloe, for example, ParkerVision noted that "[a]s commutating switch 38 cycles through the four outputs, capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants." Appx781. ParkerVision then explained that:

> A POSITA knows that for the voltage on the capacitor 74 to equal the average voltage represented by [the input signal], there is only a small amount of current and, thus, *only a small amount of energy* flowing through RFILTER 32. . . . *If current flows through* R_{FILTER}, there would be a voltage drop across R_{FILTER} and the voltage on the capacitor, V_{CAP}, could not approximate the average value of the voltage at f_1, V_x, as required by Tayloe.

Appx787-788. In other words, the POR asserted that there is no (or negligible) amounts of energy flowing through R_{FILTER}. Thus, logically, there is no (or negligible) amounts of energy, reaching Tayloe's capacitors. Otherwise (if there

was non-negligible energy flow through R_{FILTER}), there would be a voltage drop across R_{FILTER}, and the voltage on the capacitors in Tayloe could not approximate the average voltage value of the input signal – which is how Tayloe describes its capacitors working.

The excluded portions of ParkerVision's Sur-Reply merely built on these POR arguments. Because the Board overlooked these arguments, its exclusion of these arguments was improper.

B. The arguments in ParkerVision's Sur-Reply properly respond to Intel's Reply.

Moreover, the arguments in the Sur-Reply are proper because they are in direct response to new arguments in Intel's Reply.

Intel attempted to prove through *calculations* by its expert in its Reply that the capacitors of Tayloe stored non-negligible amounts of energy. Appx57; Appx4773-4774(¶ 12).

To address Dr. Subramanian's (and Intel's) new evidence/theories, ParkerVision's counsel took the deposition of Dr. Subramanian on September 10, 2021. As part of that examination, ParkerVision's counsel probed the issue of energy transfer (and the amount of energy stored by capacitors) through well-known concepts and equations—equations that were absent from Dr. Subramanian's analysis. Appx5503-5527; Appx5553-5608. ParkerVision then used these equations in its Sur-Reply to directly contradict and underscore the

deficiencies in Dr. Subramanian's approach. In particular, ParkerVision explained why Intel's theory was predicated on an incorrect assumption of the meaning of "non-negligible" energy—an assumption that was entirely untethered the '444 patent disclosures. ParkerVision's methodology for determining non-negligible energy was, therefore, offered in direct response to the methodology that Intel advanced (improperly) for the first time in its Reply.

C. The portions of ParkerVision's Sur-Reply the Board struck demonstrated that Tayloe did not disclose a "storage element"

ParkerVision's Sur-Reply demonstrated through mathematical proofs that the claimed storage elements stored non-negligible amounts of energy (nearly 60% of the available energy) relative to the input signal, while Tayloe's capacitors only held negligible amounts of energy (nearly zero). Appx877-889. In his deposition, Dr. Subramanian confirmed that ParkerVision's calculations (not present in Dr. Subramanian's Reply Declaration) were appropriate for a proper determination of energy storage by a capacitor in a circuit like Tayloe. Appx5553-5608. By striking this calculation, the only evidence the Board considered on this issue was the *new* evidence that Dr. Subramanian provided in Intel's Reply, which merely pointed to the size of the capacitors (which says nothing about whether the capacitors are actually storing non-negligible amounts of energy) and inappropriately relied on a simplistic equation for calculating the amount of energy that a capacitor stores based on the amount of work needed to charge the capacitor to a particular voltage

level (which does not take into account Tayloe's circuit configuration). Appx4770; Appx4773-4774.

Had the Board not struck ParkerVision's Sur-Reply arguments, the Board would have had to consider ParkerVision's sound mathematical proofs that Dr. Subramanian verified at his deposition.

Unlike the Board and Intel, who improperly considered Tayloe's capacitors in isolation, ParkerVision's energy calculations considered the capacitors in the context of Tayloe's actual circuit configuration, And ParkerVision's calculations show that Tayloe's capacitors hold only negligible amounts of energy (a fraction of a percentage). Notably, ParkerVision's mathematical proofs are consistent with the fact that Tayloe is a voltage sampling system (see Section V above), which uses capacitors as holding elements that hold *negligible* amounts of energy. Accordingly, Tayloe cannot render claim 3 of the '444 patent obvious. Because the Board abused its discretion in excluding Patent Owner's arguments and evidence, the Board's decision should be reversed and remanded.

XI. TAYLOE DOES *NOT* DISCLOSE ELEMENTS THAT STORE "NON-NEGLIGIBLE ENERGY."

Even if this Court determines that Intel's Reply arguments are timely (which, as discussed above, they are not), they are insufficient to meet Petitioner's burden of proof. Appx864; Appx878; Appx880. ParkerVision's expert specifically

noted that "in order to understand the operation of a circuit, one must view a circuit as a whole." Appx5401(¶172). Dr. Steer further explained:

> One cannot simply look at *individual components* of the circuit. This is because the same components used in different circuits can be used in different ways depending on the value of the component (e.g., resistor with low or high resistance, capacitor with low or high capacitance) and/or the other components in the circuit.

Appx5401-5402 (¶¶ 172-173).

Yet, this is exactly what Intel did in its Reply. Contrary to the Board's assertion that Petitioner's analysis considers "the specific components/ configuration of [Tayloe's] system," Appx58, Intel failed to properly consider the system of Tayloe's circuit as a whole. Instead, as ParkerVision asserted in its Sur-Reply, Intel provides only a superficial analysis of Tayloe's capacitors that does not reflect how the capacitors/circuits of Tayloe actually operate. Appx864, Appx880. Because the Board based its unpatentability decision on Intel's cursory analysis, it is improper and should be reversed.

As discussed above, for the first time in its Reply, Intel argued that Tayloe's capacitors "store non-negligible amounts of energy." Appx829. To supports its new position, Intel relied on new evidence: (1) the size of Tayloe's capacitors; (2) Tayloe's disclosure describing the capacitors as "integrating the input signal," and (3) a calculation that Intel's expert set forth in a supplemental declaration that

calculates the amount of energy that a capacitor stores based on the amount of work needed to charge the capacitor to a particular voltage level. The Board cited exclusively to this evidence to support its determination that Tayloe met the "storage element" limitation.

But on its face Intel's support is limited to an analysis of only an individual component—a capacitor. Neither Intel nor the Board analyzes any other circuit component, let alone the Tayloe circuit in its entirety, when determining whether the Tayloe capacitors store "non-negligible amounts of energy." Without that additional analysis, Intel (and the Board) performed, at best, a cursory and incomplete review of Tayloe. This is not substantial evidence.

Indeed, the arguments and evidence set forth in Intel's Reply (and the Board's decision) fail to give insight into the actual operation of Tayloe's capacitors. First, Intel argued that because Tayloe's capacitors are tens of thousands of times larger than the capacitors in the energy transfer embodiments of the '551 patent, they are capable of storing non-negligible amounts of energy. Appx882. But the inquiry is not whether a capacitor "is capable" of storing non-negligible amounts of energy," but rather whether it actually does. The question is, do Tayloe's capacitors *actually* store a non-negligible amount of energy? *See Ball Aerosol & Specialty Container, Inc. v. Ltd. Brands*, Inc., 555 F.3d 984, 994-95 (Fed. Cir. 2009) ("[Patent owner's] reliance on cases that found infringement by

accused products that were reasonably capable of operating in an infringing manner is misplaced, since that line of cases is relevant only to claim language that specifies that the claim is drawn to capability." (internal citations omitted)).

A proper analysis of Tayloe's circuit, which ParkerVision performed and is discussed above, demonstrates that Tayloe's capacitors do not. In fact, the size of Tayloe's capacitors says nothing about whether the capacitors are actually storing non-negligible amounts of energy. Instead, the size of Tayloe's capacitors was selected to form a filter. Appx5434(¶ 246). As set forth in Tayloe, each capacitor operates with a resistor to form a low-pass filter. Appx2701(2:14-15); Appx2702(3:21-22). A low pass filter filters out signals at a frequency higher than a cutoff frequency and passes signals at a frequency lower than the cutoff frequency. Tayloe uses a higher capacitance, because the higher the capacitance, the lower the cutoff frequency, which makes for a better low pass filter.

Second, the Board's reliance on Intel's assertion that "Tayloe describes the capacitors as integrating the input signal, which indicates an accumulation of energy and matches the '551 patent's description of a storage module's operation" (Appx830) is incorrect. In fact, the word "energy" does not appear anywhere in Tayloe nor would a POSITA understand Tayloe to disclose, teach or suggest the use of energy or energy sampling to perform down-conversion of an RF signal. Appx778. As explained in the POR, Tayloe discloses a voltage sampling system

that seeks to accurately represent the "voltage values substantially equal to the average value of the input signal during their respective quadrants." Appx781. Tayloe does this by integrating the input signal and holding the voltage value on a capacitor. Appx870, n.4. Unlike voltage sampling, the '551 patent explains that energy sampling systems cannot accurately represent the voltage of the input signal because a non-negligible amount of energy in the storage element is being transferred to a low impedance load, even between samples. Appx870, n.4.

Third, the Board's/Intel's reliance on Dr. Subramanian's storage calculation as proving the "quantity of energy stored on Tayloe's capacitors is plainly non-negligible" is misplaced. *See* Appx831. The energy formula, by itself, fails to take Tayloe's configuration into account. Instead, it merely provides the maximum amount of energy that <u>*can be*</u> stored (not that it *actually* is stored) in a capacitor given a source voltage. The portions of ParkerVision's Sur-Reply, which the Board improperly excluded, further demonstrate the errors in Dr. Subramanian's analysis. *See* Appx884-885 (utilizing the same formula with accurate variables).

Intel (and the Board's) evidence fails to prove Tayloe's capacitors store non-negligible amounts of energy because they simply do not. Instead, and as explained above, Tayloe discloses a voltage sampling system that uses "holding" elements to "store *negligible amounts of energy* from an under-sampled input EM signal with the intent of 'holding' a voltage value." Appx771; Appx797.

CONCLUSION

For all of the reasons set forth above, the Board's decision and judgment must be reversed and vacated, and/or remanded.

July 15, 2022

Respectfully submitted,

/s/ Ronald M. Daignault
Ronald M. Daignault*
Chandran B. Iyer
Jason S. Charkow*
Richard Juang*
DAIGNAULT IYER LLP
8618 Westwood Center Drive, Suite 150
Vienna, Virginia 22182
rdaignault@daignaultiyer.com
cbiyer@daignaultiyer.com
jcharkow@daignaultiyer.com
rjuang@daignaultiyer.com
**Not admitted in Virginia*

Counsel for Appellant ParkerVision, Inc.

ADDENDUM

Trials@uspto.gov
571-272-7822

Paper 44
Date: January 21, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PARKERVISION, INC.,
Patent Owner.

IPR2020-01265
Patent 7,110,444 B1

Before MICHAEL R. ZECHER, BART A. GERSTENBLITH, and IFTIKHAR AHMED, *Administrative Patent Judges*.

GERSTENBLITH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Non-Disclaimed Challenged Claim Unpatentable
Granting Petitioner's Request to Exclude Improper Arguments
Raised in Patent Owner's Sur-reply
Granting Petitioner's Motion to Exclude
Denying Petitioner's Motion to Seal
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background

Intel Corporation ("Petitioner") filed a Petition (Paper 3, "Pet.") requesting institution of *inter partes* review of claims 1, 3, and 5 of U.S. Patent No. 7,110,444 B1 (Ex. 1001, "the '444 patent"). ParkerVision, Inc. ("Patent Owner") filed an Amended Preliminary Response (Paper 9).[1] Applying the standard set forth in 35 U.S.C. § 314(a), we instituted an *inter partes* review as to all claims and grounds set forth in the Petition. Paper 10 ("Inst. Dec.").

After institution, Patent Owner filed a Patent Owner Response (Paper 18, "PO Resp."), Petitioner filed a Reply to Patent Owner's Response (Paper 21, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 26, "PO Sur-reply"). Additionally, Petitioner filed a Motion to Exclude Exhibit 2022 (Paper 34, "Mot. Exc."), Patent Owner filed an Opposition to Petitioner's Motion to Exclude (Paper 36, "Opp."), and Petitioner filed a Reply in Support of its Motion to Exclude (Paper 37, "Mot. Reply"). With our prior

[1] Patent Owner filed a timely Preliminary Response on November 23, 2020 (Paper 8), and, a day later, filed the Amended Preliminary Response. The Notice of Filing Date Accorded to Petition and Time for Filing Patent Owner Preliminary Response (Paper 4) was entered August 21, 2020. A preliminary response was thus due by November 23, 2020 (November 21st and 22nd fell on a weekend). Patent Owner should have requested authorization from the Board prior to filing its Amended Preliminary Response. Nonetheless, despite Patent Owner's failure to request authorization, we exercised our discretion under 37 C.F.R. § 42.5(b) to waive, by one day, the timing requirement under 37 C.F.R. § 42.107(b) because (1) Petitioner has not asserted that the additional day resulted in any prejudice to Petitioner and (2) the Amended Preliminary Response appears to be nearly identical to the timely filed Preliminary Response. Paper 10 ("Inst. Dec."), 2 n.1.

authorization (Paper 31, "Order"), Petitioner filed an Identification of Improper New Evidence and Arguments in [Patent Owner's] Sur-Reply (Paper 32, "Petitioner's Identification") and Patent Owner filed a Response to Petitioner's Identification (Paper 35, "Patent Owner's Response to Identification"). Petitioner also filed an unopposed Motion to Seal Exhibit 1029, which is the deposition transcript of Michael Steer, Ph.D. (Paper 22, "Mot. Seal").

Additionally, Patent Owner filed a Notice of Statutory Disclaimer (Paper 40, "Patent Owner's Disclaimer Notice") to which Patent Owner attached a copy of its disclaimer under 37 C.F.R. § 1.321(a), wherein Patent Owner disclaimed claims 1 and 5 of the '444 patent (Paper 40, Ex. A). Patent Owner's disclaimer effectively eliminated claims 1 and 5 from the '444 patent, leaving the patent as if those claims never existed. *See Sanofi-Aventis U.S., LLC v. Dr. Reddy's Labs., Inc.*, 933 F.3d 1367, 1373 (Fed. Cir. 2019) (noting that disclaiming claims effectively eliminates those claims from the patent as though the disclaimed claims had never existed (internal quotations and citations omitted)); *see also Asetek Danmark A/S v. CoolIT Sys., Inc.*, IPR2020-00747, Paper 42 at 6 (PTAB Sept. 30, 2021) (determining that a statutory disclaimer removed a disclaimed claim from an *inter partes* review proceeding). Thus, claims 1 and 5 are no longer part of this proceeding.

At Petitioner's request, we held a pre-hearing conference on October 26, 2021, during which we addressed, *inter alia*, Petitioner's Motion to Exclude and related briefing, Petitioner's Identification and Patent Owner's Response to Identification, and Petitioner's Motion to Seal. Each is addressed in more detail below. An oral hearing was held on November 1,

2021, and a copy of the transcript was entered in the record. Paper 42 ("Tr.").

We have jurisdiction pursuant to 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 as to the patentability of claim 3, the sole claim remaining in the trial. Petitioner bears the burden of proving unpatentability of the challenged claim. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must prove unpatentability by a preponderance of the evidence. *See* 35 U.S.C. § 316(e) (2018); 37 C.F.R. § 42.1(d) (2019). Having reviewed the arguments and the supporting evidence, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 3 of the '444 patent is unpatentable.

B. Related Proceedings

Petitioner and Patent Owner identify the following related matter: *ParkerVision, Inc. v. Intel Corp.*, No. 6:20-cv-108-ADA (W.D. Tex.) ("the related litigation"). Pet. 7; Paper 5 (Patent Owner's Mandatory Notices), 2. Patent Owner also states that the '444 patent is asserted in *ParkerVision, Inc. v. TCL Technology Group Corp.*, No. 5:20–cv-01030-GW-SHK (C.D. Cal.). Paper 5, 2. In addition, Petitioner filed a petition challenging several claims of U.S. Patent No. 7,539,474 B2, which is related to the '444 patent, in IPR2020-01302.

C. Real Parties in Interest

Petitioner identifies Intel Corporation as the real party in interest. Pet. 7. Patent Owner identifies ParkerVision, Inc. as the real party in interest. Paper 5, 2.

D. The Asserted Grounds of Unpatentability and Declaration Evidence

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged[2]	35 U.S.C. §[3]	Reference(s)/Basis
3	103(a)	Tayloe,[4] TI Datasheet[5]
3	103(a)	Tayloe, Kawada[6]

Pet. 10. Petitioner supports its challenge with two declarations by Vivek Subramanian, Ph.D., one submitted with the Petition (Ex. 1002 (Declaration of Vivek Subramanian, Ph.D.)) and the other submitted with Petitioner's Reply (Ex. 1030 (Reply Declaration of Vivek Subramanian, Ph.D.)), and a Declaration of Maureen M. Honeycutt (Ex. 1019). Patent Owner supports its arguments with a Declaration of Michael Steer, Ph.D. (Ex. 2021).

---

[2] Claim 3 is the sole challenged claim remaining in the case following Patent Owner's disclaimer of claims 1 and 5.

[3] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the '444 patent has an effective filing date before March 16, 2013, we apply the pre-AIA versions of the statutory bases for unpatentability.

[4] U.S. Patent No. 6,230,000 B1, issued May 8, 2001 (Ex. 1004, "Tayloe").

[5] SN74CBT3253 Dual 1-of-4 FET Multiplexer/Demultiplexer (rev. ed. May 1998) (Ex. 1005, "TI Datasheet"). Petitioner refers to this exhibit, in at least one instance, as "SN74CBT3253D." Pet. 9. The exhibit itself, however, does not include the letter "D" in the product number. Ex. 1005. Petitioner explains that "the 'D' in the product number refers simply to a packaging option" (Pet. 38 n.5), which is confirmed by the description on the first page stating "Package Options Include Plastic Small-Outline (D)." Ex. 1005, 1. Neither party asserts that the packaging option results in a difference of any significance to the issues before us.

[6] U.S. Patent No. 4,985,647, issued January 15, 1991 (Ex. 1008, "Kawada").

E. The '444 Patent

The '444 patent is directed to "a wireless local area network (WLAN) that includes one or more WLAN devices (also called stations, terminals, access points, client devices, or infrastructure devices) for effecting wireless communications over the WLAN." Ex. 1001, 2:10–14. The '444 patent explains that "[t]he WLAN device includes at least an antenna, a receiver, and a transmitter . . . . The WLAN receiver includes at least one universal frequency translation module that frequency down-converts a received electromagnetic (EM) signal." *Id.* at 2:14–22.

Figure 70A is reproduced below:

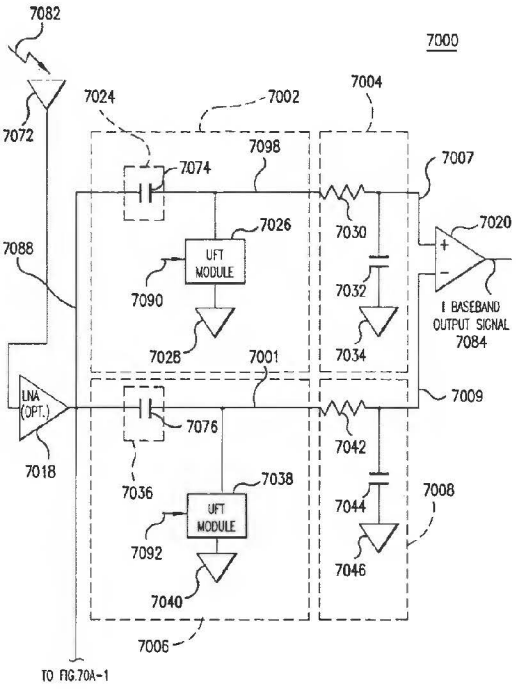


FIG.70A

Figure 70A of the '444 patent "illustrates an IQ receiver having shunt UFT [universal frequency translation] modules." Ex. 1001, 5:34–35. The '444 patent explains that "I/Q modulation receiver 7000 receives, down-

converts, and demodulates a[n] I/Q modulated RF input signal 7082 to an I baseband output signal 7084, and a Q baseband output signal 7086." *Id.* at 35:51–54; *see id.* at 35:60–62 (Antenna 7072 receives and outputs I/Q modulated RF input signal 7082.). The '444 patent states that, "[w]hen present, LNA 7018 amplifies I/Q modulated RF input signal 7082, and outputs amplified I/Q signal 7088." *Id.* at 35:62–64. Thereafter, "[f]irst UFD [universal frequency down-conversion] module 7002, receives amplified I/Q signal 7088. . . . [,] down-converts the I-phase signal portion of amplified input I/Q signal 7088 according to an I control signal 7090. . . . [, and] outputs an I output signal 7098." *Id.* at 35:65–36:2. Similarly, UFD module 7006 "receives amplified I/Q signal 7088[,]" "down-converts the inverted I-phase signal portion of amplified input I/Q signal 7088 according to an inverted I control signal 7092[,]" and "outputs an inverted I output signal 7001." *Id.* at 36:33–37. Thereafter, "[f]irst differential amplifier 7020 receives filtered I output signal 7007 . . . . subtracts filtered inverted I output signal 7009 from filtered I output signal 7007, amplifies the result, and outputs I baseband output signal 7084." *Id.* at 37:3–8.

The '444 patent's first and second UFD modules in Figure 70A include capacitors 7074 and 7076, respectively, and UFT modules 7026 and 7038, respectively. *See* Ex. 1001, 36:3–5 (first UFD module 7002 comprises first storage module 7024 and first UFT module 7026), 36:14–15 (first storage module 7024 comprises first capacitor 7074), 36:38–40 (second UFD module 7006 comprises second storage module 7036 and second UFT module 7038), 36:50–51 (second storage module 7036 comprises second capacitor 7076).

Figure 1B is reproduced below:

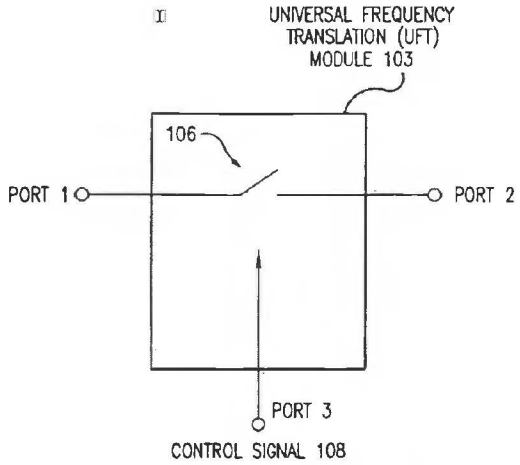


FIG. 1B

Figure 1B of the '444 patent "is a more detailed diagram of a universal frequency translation (UFT) module." *Id.* at 2:56–58. The '444 patent explains that, "[g]enerally, the UFT module 103 includes a switch 106 controlled by a control circuit 108." *Id.* at 8:62–64 (noting that switch 106 is referred to as a controlled switch); *see id.* at 36:5–7 (first UFT module, shown in Figure 70A, contains a switch that opens and closes as a function of I control signal 7090), 36:40–42 (second UFT module, also shown in Figure 70A, contains a switch that opens and closes as a function of inverted I control signal 7092).

The '444 patent includes two alternative configurations of switches and capacitors in UFD modules (Ex. 1001, 9:43–57), as shown in Figures 20A and 20A-1 reproduced below:

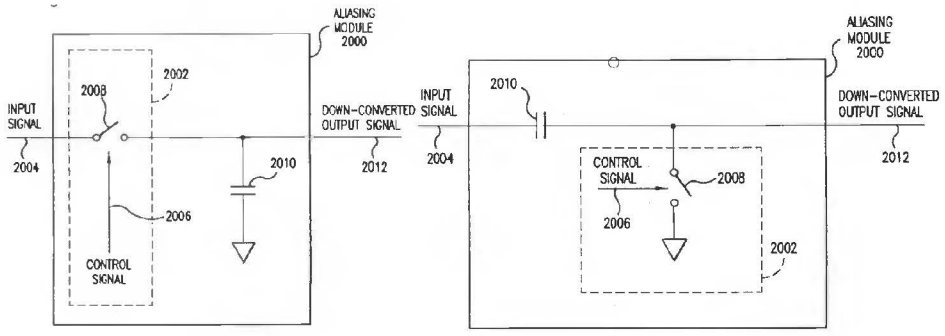


FIG.20A FIG.20A-1

Figures 20A and 20A-1 of the '444 patent "are example aliasing modules." *Id.* at 3:50–51. The '444 patent explains that, in Figure 20A, switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to ground; in Figure 20A-1, however, capacitor 2010 is in series with input signal 2004 and switch 2008 is shunted to ground. *Id.* at 9:48–57 (also noting that "[t]he electronic alignment of the circuit components is flexible").

The '444 patent states that "[t]he down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in" U.S. Patent No. 6,061,551 ("the '551 patent"), "the full disclosure of which is incorporated herein by reference." Ex. 1001, 9:32–38. And, the '444 patent further states that "[d]own-conversion utilizing a UFD module (also called an aliasing module) is further described in the" '551 patent. *Id.* at 34:54–58.

F. Illustrative Claim

Claim 3, the sole claim remaining in this proceeding, is illustrative of the claimed subject matter and reproduced below with Petitioner's bracketing added for reference:

> 3. [3 preamble] A wireless modem apparatus, comprising:
>
> [3A] a receiver for frequency down-converting an input signal including,
>
> [3B] a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;
>
> [3C] a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and
>
> [3D] a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;
>
> [3E] wherein said first and said second frequency down-conversion modules each comprise a switch and a storage element.

Ex. 1001, 61:1–18.

G. Level of Ordinary Skill in the Art

Petitioner, supported by Dr. Subramanian's testimony, proposes that a person of ordinary skill in the art at the time of the invention would have had "at least a bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of RF circuit design." Pet. 47 (citing Ex. 1002 ¶ 25). Petitioner explains that "[l]ess work experience may

be compensated by a higher level of education, such as a master's degree." *Id.* (citing Ex. 1002 ¶ 25).

In the Institution Decision, we noted that Patent Owner had not expressed a position on the level of ordinary skill in the art in the Preliminary Response, and, on the preliminary record, we adopted Petitioner's unopposed position, finding it consistent with the level of ordinary skill in the art reflected by the '444 patent and the prior art of record. Inst. Dec. 9 (citing *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978)).

In the Patent Owner Response, Patent Owner, supported by Dr. Steer's testimony, proposes that a person of ordinary skill in the art at the time of the invention would have

> (a) a Bachelor of Science degree in electrical or computer engineering (or a related academic field), and at least two (2) additional years of work experience in the design and development of radio frequency circuits and/or systems, or (b) at least five (5) years of work experience and training in the design and development of radio frequency circuits and/or systems.

PO Resp. 4 (citing Ex. 2021 ¶ 24). Neither Patent Owner nor Dr. Steer explains why their proposal materially differs from that proposed by Petitioner.

Patent Owner's option (a) is substantially the same as Petitioner's proposal—both require a bachelor's degree in the same or a related subject and two additional years of related work experience. Patent Owner's option (b) adds an additional option based on work experience in lieu of a formal degree. Patent Owner's option (b), however, is consistent with

Dr. Subramanian's testimony, which states "[l]ess work experience may be compensated by a higher level of education, such as a master's degree, *and vice versa*." Ex. 1002 ¶ 25 (emphasis added). It is not clear why Petitioner's proposal, as set forth in the Petition, did not include the additional option of providing greater work experience in compensation for a lower level of education.

Neither party contends that the differences in proposals affect the outcome of this proceeding and we do not find that they do. Nonetheless, on the full record before us, we find that our identification of the level of ordinary skill in art in the Institution Decision as well as Patent Owner's option (b) are supported by the prior art of record, the '444 patent, and the opinions of Drs. Subramanian and Steer (which, as discussed above, recognize that additional work experience can compensate for the lack of a formal degree). Accordingly, we modify our preliminary finding to include option (b) from Patent Owner's proposal. Thus, we find that one of ordinary skill in the art would have at least a bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of RF circuit design, or at least five years of work experience and training in the design and development of RF circuits and/or systems. We also find that less work experience may be compensated by a higher level of education, such as a master's degree.

II. CLAIM CONSTRUCTION

In this *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claims in a civil action under 35 U.S.C. § 282(b). *See* 37 C.F.R. § 42.100(b) (2019). The claim construction standard includes construing claims in accordance with

the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art at the time of the invention. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc). In construing claims in accordance with their ordinary and customary meaning, we take into account the specification and prosecution history. *Phillips*, 415 F.3d at 1315–17.

If the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor's lexicography governs." *Phillips*, 415 F.3d at 1316 (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). Another exception to the general rule that claims are given their ordinary and customary meaning is "when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Uship Intellectual Props., LLC v. United States*, 714 F.3d 1311, 1313 (Fed. Cir. 2013) (quoting *Thorner v. Sony Computer Entm't Am., LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)).

Additionally, only terms that are in controversy need to be construed, and these need be construed only to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that "only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy"); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs.* in the context of an *inter partes* review).

A. "storage element"[7]

In the Institution Decision, we did not construe any claim terms expressly because none of the terms were in dispute. Inst. Dec. 10 (citation omitted). In the briefing following institution, Patent Owner proposed a construction for the term "storage element," *see, e.g.*, PO Resp. 2–4, 45–59, and it became clear that the parties dispute the meaning of the term. Additionally, because many of Patent Owner's arguments hinge on the meaning of this term, its proper construction is important to address the issues presented in this proceeding. Further, the parties' arguments rely, almost exclusively, on disclosures in the '551 patent, incorporated by reference into the '444 patent. Accordingly, we address the parties' arguments and proposed constructions.

1. The Parties' Arguments

In the Petition, Petitioner does not propose a construction for "storage element," but does assert that each "storage element" is taught by Tayloe's capacitors, illustrated in Tayloe's Figure 3. Pet. 75–78 (citations omitted). Petitioner contends that "[a] capacitor is a well-known storage element, and in fact, the '444 patent embodiment discloses a capacitor as the storage element." *Id.* at 77 (citations omitted).

In the Patent Owner Response, Patent Owner notes that the district court construed "storage element" in the related litigation as "an element of

[7] The parties agree that the terms "storage element" and "storage module" are synonymous. *See* PO Resp. 27 (noting that "storage module" is "another name for 'storage element'"); Pet. Reply 10 n.2 ("The '551 patent uses the term 'storage ***module***,' whereas challenged claim 3 uses 'storage ***element***.' As [Patent Owner] appears to admit (*e.g.*, [PO Resp.] 46), 'storage module' and 'storage element' are synonymous.").

an *energy transfer system* that stores non-negligible amounts of energy from an input electromagnetic signal." PO Resp. 45; *see also id.* at 3–4 (citing Ex. 2012 (Document 75, Claim Construction Order), 5). Patent Owner contends that the district court previously considered the construction of "storage element" proposed by Petitioner in that forum—"an element that stores a non-negligible amount of energy from an input electromagnetic (EM) signal." *Id.* at 46. Patent Owner asserts that the district court included the phrase "of an energy transfer system" from Patent Owner's proposed construction "to distinguish a 'storage element' (an element of an *energy transfer* system) from a 'holding element' (an element of a sample and hold system – the type of element used in [Petitioner's] primary prior art reference, Tayloe)." *Id.*

Patent Owner contends that the '444 patent (based on the incorporated '551 patent disclosure) teaches two different systems: (1) a "sample-and-hold" or "voltage sampling" system and (2) an "energy transfer" or "energy sampling" system. PO Resp. 19, 21; *see also id.* at 31 (citing Ex. 2021 ¶ 196). Patent Owner asserts that a sample-and-hold system includes (1) a switch, (2) a *holding* element, and (3) a *high* impedance load. *Id.* at 20. Patent Owner contends,

> The '444 patent specifically *reserves* the term "*holding*" module/element to refer to an element (e.g., capacitor) used in a sample-and-hold (voltage sampling) system because . . . the use of a *high* impedance load causes the capacitor to *hold* energy (i.e., *prevent* energy in the capacitor from being discharged to form the down-converted signal – the discharged energy itself does not become part of the down-converted signal).

Id. (citing Ex. 2021 ¶ 146). In contrast, Patent Owner contends that an energy transfer system includes (1) a switch, (2) a *storage* element, and (3) a *low* impedance load. *Id.* at 21. Patent Owner asserts,

> The '444 patent specifically *reserves* the term "*storage*" module/element to refer to an element (e.g., capacitor) used in an energy sampling system because . . . the use of a *low* impedance load enables the capacitor to *store* energy and subsequently *discharge* the energy to form the baseband signal (i.e., the discharged energy itself becomes part of the baseband signal).

Id. at 22 (citing Ex. 2021 ¶ 160).

Patent Owner contends that "[w]hat is critical to understand is that while both energy sampling and voltage sampling use similar components (e.g., switches, capacitors and loads), these components are used in different *ways* in a circuit to create a desired result." PO Resp. 22 (citing Ex. 2021 ¶ 173). Patent Owner asserts that "the *way* in which the components are used is significant and make these systems *fundamentally different and competing* systems." *Id.* In particular, Patent Owner contends that "[w]hereas a voltage sampling circuit discards energy without using the energy in the down-converted signal (thereby wasting energy), an energy sampling circuit discharges energy into a load so that the energy itself becomes part of the down-converted signal." *Id.* (citing Ex. 2021 ¶ 173). Patent Owner argues that "[t]hese differences . . . [are] why claim 3 of the '444 patent specifically recites '*storage* element' (an element of an *energy* transfer (*energy* sampling) system) instead of '*holding* element' (an element of a sample-and-hold (*voltage* sampling) system)." *Id.*; *see id.* at 31 ("Challenged claim 3 of the '444 patent is directed to *energy* transfer because it uses a term that the patentees *reserved* specifically to connote

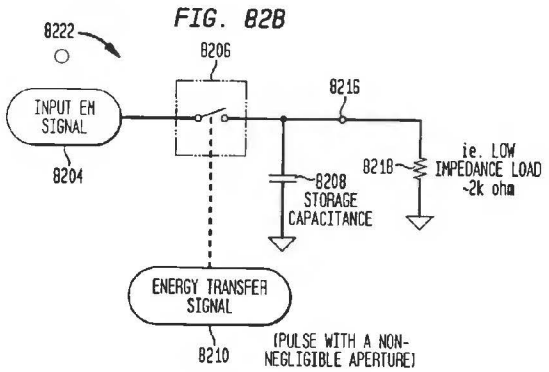
energy transfer – '*storage* element.'") (citing Ex. 2021 ¶ 196). Patent Owner asserts that "[t]he different terms distinguish between the *different* function/operation of the capacitors and *different* type of loads used with the capacitors." *Id.* Patent Owner further explains, "[i]n other words, whether a capacitor is a 'storage' module/element depends on the way in which the capacitor is being used. Just because a capacitor is being used does not mean that the capacitor is a 'storage' module/element." *Id.* at 29.

Patent Owner includes the following table that it contends "identifies key features that distinguish energy transfer (i.e., energy sampling) from sample-and-hold (i.e., voltage sampling)" systems:

Energy Transfer (*Energy* Sampling)	**Sample and Hold (*Voltage* Sampling)**
Non-negligible sampling aperture	Negligible sampling aperture
"*Storage*" module	"*Holding*" module
Low impedance load	*High* impedance load
Down-converted signal includes the *energy* transferred from the RF signal to the load (i.e., energy sent to the load makes up the down-converted signal)	Down-converted signal is based on discrete *voltage* measurements of the RF signal

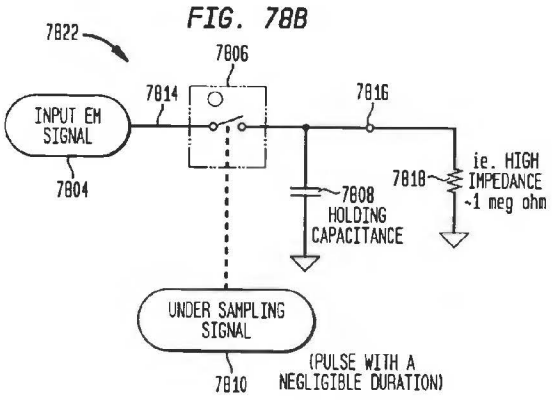
PO Resp. 32 (footnote omitted).

Relying on Figure 82B of the '551 patent, reproduced below, Patent Owner explains the operation of an energy transfer (energy sampling) system.



Ex. 2007, Fig. 82B; *see* PO Resp. 33. Figure 82B of the '551 patent illustrates an exemplary energy transfer system. Ex. 2007, 7:47–48. According to Patent Owner, "an energy transfer system uses (1) a control signal having a pulse with a *non*-negligible aperture/duration, and (2) a '*storage*' capacitor for storing *and discharging non*-negligible amounts of energy for driving a *low* impedance load." PO Resp. 33–34. Patent Owner asserts that, "[i]f the impedance were high, the 'storage' capacitor could *not* discharge sufficient energy for the system to perform energy transfer (energy sampling) and form a down-converted signal from energy transferred to the low impedance load." *Id.* at 34 (citing Ex. 2021 ¶ 200). Patent Owner provides further explanation as to how it contends an energy transfer system functions, based on the teachings of the '551 patent, to produce the baseband signal sent from a transmitting device. *Id.* at 33–38 (citations omitted).

In comparison, Patent Owner relies on Figure 78B of the '551 patent, reproduced below, to explain the operation of a sample-and-hold system.



Ex. 2007, Fig. 78B; *see* PO Resp. 39. Figure 78B of the '551 patent illustrates an exemplary embodiment of an under-sampling system. Ex. 2007, 7:36–37. According to Patent Owner, "a sample and hold system uses (1) a control signal having a pulse with a *negligible* aperture/duration, (2) a 'holding' capacitor for *holding* a constant voltage across the capacitor and (3) a *high* impedance load." PO Resp. 39. Patent Owner asserts that the capacitor is referred to as a "holding" capacitor "because, unlike the 'storage' capacitor in an energy transfer system, a 'holding' capacitor does *not* discharge any significant energy to the load." *Id.* Patent Owner contends that "the *high* impedance load is specifically included to *prevent* the holding capacitor from discharging energy, which would degrade the discrete voltage measurements and adversely affect the system performing sample and hold (voltage sampling)." *Id.* (citing Ex. 2021 ¶ 209). Patent Owner provides further explanation as to how it contends a sample and hold system functions, based on the teachings of the '551 patent, to produce the baseband signal sent from a transmitting device. *Id.* at 38–42 (citations omitted).

Patent Owner contends that "[a] '*storage* element' (or 'storage module') is a term reserved exclusively for a component of an energy

transfer (*energy* sampling) system" whereas "a 'holding' module/element is a term reserved exclusively for a component of a sample-and-hold (*voltage* sampling) system." PO Resp. 46. Therefore, Patent Owner asserts that "an energy 'storage' module/element must be construed in a way that distinguishes it from a 'holding' module/element." *Id.* (citations omitted).

Patent Owner argues that the specification of the '551 patent "is clear that the term 'storage' module/element is specific to an '*energy transfer system*' and a 'holding' module/element, as the name implies, is specific to a sample-and-*hold* (voltage sampling) system." PO Resp. 47. In particular, Patent Owner relies on the following paragraph of the '551 patent:

> FIG. 82A illustrates an exemplary energy transfer system 8202 for down-converting an input EM signal 8204. The energy transfer system 8202 includes a switching module 8206 and a storage module illustrated as a storage capacitance 8208. The terms storage module and storage capacitance, as used herein, are distinguishable from the terms holding module and holding capacitance, respectively. Holding modules and holding capacitances, as used above, identify systems that store negligible amounts of energy from an under-sampled input EM signal with the intent of "holding" a voltage value. Storage modules and storage capacitances, on the other hand, refer to systems that store non-negligible amounts of energy from an input EM signal.

Ex. 2007, 66:55–67, *quoted in* PO Resp. 47. Patent Owner also relies on the '551 patent's use of "storage" in Figures 68G and 82B compared to the use of "holding" in Figures 29G and 78B. PO Resp. 48–49 (comparing "*STORAGE* MODULE" and "CAPACITIVE *STORAGE* MODULE" in Figure 68G and "*STORAGE* CAPACITANCE" in Figure 82B to "*HOLDING* MODULE" and "CAPACITIVE *HOLDING* MODULE" in

Figure 29G and "*HOLDING* CAPACITANCE" in Figure 78B (emphases added)).

Patent Owner contends that "[a] storage element is synonymous with a *low* impedance load. Indeed, a *low* impedance load is what makes a module a 'storage' module/element as opposed to a 'holding' module/element." PO Resp. 49. Patent Owner asserts that "a *low* impedance load provides little resistance to electrical current and, thus, energy can be transferred/discharged from a 'storage' module/element. This unique feature of an energy transfer system is what enables the 'storage' module/element to drive a low impedance load." *Id.* In contrast, Patent Owner argues that, if "a load is *high* impedance, there would be high resistance to current and the module would 'hold' a voltage. In other words, with a *high* impedance load, the module would be a 'holding' module/element, *not* a 'storage' module/element." *Id.* As further support for its argument, Patent Owner points to the following statement in the '551 patent, which notes that a benefit of energy transfer system 8202 is driving a low impedance load:

> Another benefit of the energy transfer system 8202 is that the non-negligible amounts of transferred energy permit the energy transfer system 8202 to effectively drive loads that would otherwise be classified as low impedance loads in under-sampling systems and conventional sampling systems. In other words, the nonnegligible amounts of transferred energy ensure that, even for lower impedance loads, the storage capacitance 8208 accepts and maintains sufficient energy or charge to drive the load 8202.

Ex. 2007, 67:37–46, *quoted in* PO Resp. 49–50. Patent Owner asserts that "[w]ithout a 'storage' module/element driving a *low* impedance load, sufficient energy could <u>not</u> be transferred/discharged from the 'storage'

module/element in order to recover a down-converted signal from an input EM signal. In such a case, the module/element would be a 'holding' module/element." PO Resp. 50.

Petitioner contests Patent Owner's characterization of the '444 and '551 patents as well as Patent Owner's construction of "storage element." *See, e.g.*, Pet. Reply 4–16. We discuss both patents, as we did with respect to Patent Owner's argument, because the distinction informs as to how the parties understand these two patents and, specifically, claim 3 of the '444 patent. With respect to the characterization of the patents, Petitioner relies on a portion of the Summary of the Invention of the '551 patent, which states:

> Briefly stated, the present invention is directed to methods, systems, and apparatuses *for down-converting an electromagnetic (EM) signal by aliasing the EM signal*, and applications thereof. Generally, the invention operates by receiving an EM signal. The invention also receives an aliasing signal having an aliasing rate. The invention aliases the EM signal according to the aliasing signal to down-convert the EM signal. *The term aliasing, as used herein and as covered by the invention refers to both down-converting an EM signal by under-sampling the EM signal at an aliasing rate, and down-converting an EM signal by transferring energy from the EM signal at the aliasing rate.*

Ex. 2007, 2:53–65 (emphases added), *quoted in* Pet. Reply 5–6.

Relying on the above-disclosure from the '551 patent, Petitioner explains that "aliasing" refers to down-converting an EM signal by (1) under-sampling the EM signal at an aliasing rate and (2) transferring energy from the EM signal at the aliasing rate. Pet. Reply 6 (citing Ex. 2007, 2:60–65, 20:7–11, 21:4–7). Additionally, Petitioner points to the Table of Contents in the '551 patent and, specifically, the Overview of the

Invention section that organizes its discussion around these two concepts as well as Figure 45A, which shows a Venn diagram in which "UNDERSAMPLING" and "TRANSFERRING ENERGY" are shown as subsets of "ALIASING." *Id.* at 6–8 (citing Ex. 2007, 9:1–21, 20:63–21:2, Fig. 45A). Further, Petitioner points to an express statement by Patent Owner in a previous *inter partes* review (IPR2014-00948), where Patent Owner stated that the '551 patent describes "***two sampling mechanisms***: (1) ***under-sampling***; and (2) ***energy transfer***." *Id.* at 8 (citing Ex. 1031 (Patent Owner's Response to Petition in IPR2014-00948, Paper 25), 17).[8]

Petitioner contends that neither patent (the '444 patent or the '551 patent) refers to "energy sampling" or "voltage sampling," and neither refers to "any sample of 'energy'" measured in units of energy, such as joules. Pet. Reply 8–9. Rather, Petitioner asserts that "the down-converted waveforms for all embodiments—including those that [Patent Owner] identifies as 'energy transfer' embodiments—show samples measured in units of voltage ('millivolts' or 'mV')." *Id.* (citing Ex. 2007, Figs. 83E–83F). Thus, Petitioner argues that Patent Owner's characterization is incorrect because the distinction in the '551 patent is not between "energy sampling" and "voltage sampling"; rather, the distinction is between "under-sampling" and "energy transfer." *See, e.g.*, *id.* at 4–5 (citations omitted).

[8] The patent-at-issue in IPR2014-00948 also incorporates the '551 patent by reference, and, thus, the argument there also was based on the '551 patent. *See, e.g.*, Ex. 1031, 3 n.1 (noting incorporation of the '551 patent by reference).

With respect to the construction of "storage element," Petitioner proposes that it be construed to mean "an element that stores a nonnegligible amount of energy from an input electromagnetic (EM) signal." Pet. Reply 10. Petitioner contends that its proposed construction expressly tracks the definition provided in the '551 patent for "storage element," which the parties agree is synonymous with "storage module." *Id.*; *see id.* at 10 n.2. In particular, Petitioner asserts that the '551 patent states: "***Storage modules . . . refer to systems that store non-negligible amounts of energy from an input EM signal***." *Id.* (quoting Ex. 2007, 66:65–67). Petitioner notes that the '551 patent also states that "the 'goal of the storage modules' is 'to ***store non-negligible amounts of energy*** transferred from the EM signal'" and that the patent "specifically distinguishes ***storage*** elements from ***holding*** elements on this basis." *Id.* at 10–11 (quoting Ex. 2007, 66:59–67 ("***Holding modules*** . . . identify systems that ***store negligible amounts of energy*** from an under-sampled input EM signal with the intent of 'holding' a voltage value. ***Storage modules*** . . . on the other hand, refer to systems that ***store non-negligible amounts of energy*** from an input EM signal.")). Thus, Petitioner contends "'storage element' should be construed accordingly." *Id.* at 11 (citation omitted).

Additionally, Petitioner points to IPR2014-00948, where Petitioner asserts that Patent Owner argued "a storage module" should be construed to mean "an apparatus that stores non-negligible amounts of energy from the carrier signal." Pet. Reply 11 (citing Ex. 1032 (Patent Owner's Preliminary Response in IPR2014-00948, Paper 7), 37). Petitioner also notes that Patent Owner argued that the '551 patent "***explicitly defines a storage module***." *Id.* (citing Ex. 1032, 21). And, Petitioner further argues that the Board relied

upon Patent Owner's statement in the institution decision in that proceeding. *Id.* at 11–12 (citing Ex. 1033 (Decision, Institution of *Inter Partes* Review, Paper 8), 10).

Addressing Patent Owner's proposed construction in this proceeding, Petitioner asserts that Patent Owner seeks to modify the definition provided in the '551 patent by including a requirement that the "storage element" be part of "an ***energy transfer system***." Pet. Reply 12 (citing PO Resp. 45). Petitioner notes that Patent Owner "then interprets this proposed construction as requiring a further limitation—the system must have a low-impedance load." *Id.* (citing PO Resp. 32, 46–50).

Petitioner responds with three primary points. First, Petitioner points to Patent Owner's express statement, from IPR2014-00948, that the '551 patent "explicitly defines" this term, but Petitioner notes that "of an energy transfer system" does not appear in the definition. Pet. Reply 12 (citing Ex. 1032, 21). Petitioner contends that Patent Owner's proposal "should be rejected for this reason alone." *Id.* (citation omitted). Second, Petitioner asserts that Patent Owner's "rationale for its construction—the supposed distinction between 'energy sampling' and 'voltage sampling'—is not grounded in the patent." *Id.* And, third, that the '551 patent does not define a storage module as part of an energy transfer system; rather, it "merely discloses an embodiment of 'an exemplary energy transfer system.'" *Id.* at 12–13 (citing Ex. 2007, 66:55–67). And, "the rest of the passage directly supports [Petitioner's] proposed construction" by reciting that storage modules "refer to systems that store non-negligible amounts of

energy from an input EM signal." *Id.* at 13 (internal quotation and emphasis omitted).[9]

In its Sur-reply, Patent Owner responds to Petitioner's discussion of the characterization of the '444 and '551 patents as well as the construction of "storage element." PO Sur-reply 8–14. With respect to the characterization of these two patents, Patent Owner contends that "[u]nlike [Patent Owner], who focuses on how the technology actually works, [Petitioner] relies on a *naming convention* used in the patent to push a *flawed* narrative – one that has *twice* been rejected by the" same district court. PO Sur-reply 8 (citing Pet. Reply 2–3, 6–8). Patent Owner asserts that "[t]he fact that the patent does not use the terms 'voltage sampling' and 'energy sampling' verbatim is beside the point."[10] *Id.* at 9. Patent Owner argues that the '444 patent "relates to the use of *sampling* to down-convert a signal and teaches *only* <u>*two*</u> things that can be sampled to down-convert a signal: (1) voltage and (2) flow of energy over time." *Id.* Voltage, Patent Owner asserts, "is sampled by taking and holding input voltage values (using a 'holding' element)," whereas "energy is sampled by transferring non-negligible amounts of energy from an input signal." *Id.* (citing Ex. 2007,

---

[9] Petitioner also notes that, although Figures 68G and 82B "show a 'storage module' or 'storage capacitance' in an 'energy transfer' embodiment, . . . neither figure ***defines*** a storage module as an element of an 'energy transfer system'—any more than they suggest that a switch or resistor (also shown) should be defined as such an element." Pet. Reply 13 n.3.

[10] Patent Owner contends that "[e]nergy cannot be measured directly. Instead a measurement (voltage or its inverse, current) needs to be taken from which energy can be derived." PO Sur-reply 9 n.6. Thus, Patent Owner argues that Petitioner's identification of Figures 83E–F of the '551 patent, which plot measurements of voltage over time, "is of no moment." *Id.*

62:27–30). Patent Owner explains that this is the reason it refers to the two systems as voltage sampling and energy sampling. *Id.* at 10.

With respect to the construction of "storage element," Patent Owner contends that the '551 patent "states that the 'energy transfer' system uses 'a storage module' that 'stores non-negligible amounts of energy,' whereas the 'under-sampling (i.e., sample-and-hold) system utilizes a 'holding module' that 'stores negligible amounts of energy.'" PO Sur-reply 10–11 (quoting Ex. 2007, 66:55–67). Thus, Patent Owner asserts that "there should be no dispute that 'energy transfer system' should be included in the construction as [Patent Owner] proposes." *Id.* at 11.

Patent Owner contends that Petitioner fails to provide any "substantive technical arguments based on the intrinsic evidence as to why including 'an element of an energy transfer system' is technically incorrect. Instead, [Petitioner] points to a single sentence from the specification . . . and asserts that this passage is enough to define the 'storage' element." PO Sur-reply 11. Discussing the same paragraph quoted above from Petitioner's Reply, Patent Owner contends that the paragraph "is describing a 'storage' module/element in the context of an energy transfer system . . ., which is the only type of system that has a 'storage' module/element. Indeed, this passage is found in the section entitled '0.1.2 Introduction to *Energy Transfer*.'" *Id.* at 12 (quoting Ex. 2007, 66:33) (citing Ex. 2007, 66:55–37). Thus, Patent Owner asserts there is no basis to argue against including "energy transfer system" in the meaning of "storage element." *Id.*

Patent Owner argues that inclusion of "energy transfer system" in the meaning of "storage element" is appropriate because (1) Petitioner admits there are only two systems disclosed—energy transfer and under-sampling

(PO Sur-reply 12 (citing Pet. Reply 6)), and (2) the '444 patent (via incorporation of the '551 patent) states that a "storage" element is only used in an energy transfer system (*id.* (citing Ex. 2007, 66:55–59)). Patent Owner contends, "[l]ogically, if there are only two systems and a 'storage' element is only used in an energy transfer system, then a 'storage' module/element must necessarily be an element of an energy transfer system." *Id.* Patent Owner argues that "the specification makes it clear that 'storage' modules/elements are inseparably intertwined with energy transfer systems." *Id.* (citing PO Resp. 46–50).

Additionally, Patent Owner asserts that its arguments in IPR2014-00948 were based on the broadest reasonable interpretation standard used by the Board at that time, not the standard currently employed by the Board, which matches the standard used in federal courts under 35 U.S.C. § 282(b). PO Sur-reply 12–13. In particular, Patent Owner contends that it focused on the single-sentence highlighted by Petitioner because of the claim construction standard at that time, whereas the current claim construction standard, "requires considering more than just the" one sentence, which Patent Owner asserts its proposed construction now does. *Id.* at 13.

Further, Patent Owner asserts that "a 'low impedance load' goes to the heart of what makes an element, a 'storage' element (used in energy sampling) as opposed to a 'holding' element (used in voltage sampling/sample-and-hold)." PO Sur-reply 13. Patent Owner contends that "[u]nlike a low impedance load, a high impedance load causes an element to 'hold' energy, making it a 'holding' element, not a 'storage' element." *Id.* Patent Owner asserts that "[t]his is the reason the specification specially makes a point to say that a 'holding' modules/elements hold 'negligible

amounts of energy . . . *with the intent of 'holding' a voltage value.*'" *Id.* (quoting Ex. 2007, 66:63–65). Patent Owner argues that "the way in which 'holding' modules/elements 'hold' a voltage value is by using a high impedance load." *Id.* at 14 (citing Ex. 2021 ¶ 148). Patent Owner asserts that loads can either be high or low—"it is a binary choice"—and "because a 'storage' module/element is not using a high impedance load, it must necessarily be using a low impedance load." *Id.* (citing Ex. 2007, 67:32–33). Patent Owner also remarks that "the specification states that in energy transfer systems driving a low impedance load *is* a benefit" meaning "it *necessarily* occurs." *Id.* (citing Ex. 2007, 67:37–42).

2. Analysis

We begin with a discussion of the timing of the parties' proposed constructions and interplay between this proceeding and the related litigation because the parties include aspects of both in their briefing here. Petitioner's Reply, in particular, sets forth an accurate timeline, which we repeat here along with additional details.

- July 2020 – Petitioner files the instant Petition, but does not propose an express construction for "storage element" (*see* Paper 4 (Notice of Filing Date Accorded to Petition and Time for Filing Patent Owner Preliminary Response), 1);
- September 2020 – the parties identify terms for construction in the related litigation, but neither party includes "storage element" (*see* Ex. 1034 (Patent Owner's Identification of Proposed Claim Terms for Construction); Ex. 1035 (Petitioner's Proposed Claim Terms));
- Late September 2020 – the parties modify their identification of terms for construction in the related litigation and Petitioner

includes "storage element" as recited in the '444 patent (Ex. 1036 (Petitioner's Proposed Claim Constructions));

- October 2020 – the parties exchange proposed constructions for the terms identified in the related litigation (Pet. Reply 14);
- January 2021 – the district court issues a claim construction order construing "storage element" as "an element of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal" (*see* Paper 12 (Petitioner's Supplemental Notice Regarding Claim Construction), Ex. 2012 (Claim Construction Order in the related litigation), 5);
- May 2021 – Patent Owner files its Patent Owner Response and proposes an express construction for "storage element";
- July 2021 – the district court issues a claim construction order in a different case (Case No. W-20-CV-00562-ADA) construing "storage module" in a related patent as "a module of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal *for driving a low impedance load*" (Ex. 1038 (Claim Construction Order in Case No. W-20-CV-00562-ADA), 2 (emphasis added));
- August 2021 – Petitioner files its Reply;
- September 2021 – Patent Owner files its Sur-reply;
- October 2021 – the district court issues an amended construction of "storage module" in Case No. W-20-CV-00562-ADA, deleting the recitation of "for driving a low impedance load" from its previous construction and, thus, harmonizing its constructions (*see* Paper 39

(Petitioner's Supplemental Notice Regarding Claim Construction), 2–3); and

- October 2021 – a district court-appointed Special Master recommends, in other litigation involving claim 3 of the '444 patent, construing "storage element" consistent with the district court's construction of "an element of an energy transfer system that stores nonnegligible amounts of energy from an input electromagnetic signal" (*see* Paper 41 (Patent Owner's Supplemental Notice Regarding Claim Construction), 2)).

As the above-sequence reflects, the most-current construction of "storage element" by the district court is "an element of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal." *See* Paper 12; Ex. 2012, 5. As set forth in 37 C.F.R. § 42.100(b), we consider "[a]ny prior claim construction determination concerning a term of the claim in a civil action . . . that is timely made of record." We have done so to the extent possible on the record before us. In particular, the district court's claim construction is set forth in a chart format without providing the benefit of the district court's informed analysis as to how that construction was determined. The lack of explanation is particularly of note here because the district court did not adopt either party's proposed construction in full; rather, the court accepted parts of each party's proposal. As reflected in the chart below, the district court accepted that "storage element" is limited to "an energy transfer system" by including that phrase in the court's final construction, but did not accept Patent Owner's inclusion of the phrase "for driving a low impedance load."

Term	Patent Owner's Proposed Construction	Petitioner's Proposed Construction	District Court's Final Construction
"storage element"	"an element *of an energy transfer system* that stores non-negligible amounts of energy from an input electromagnetic signal *for driving a low impedance load*"	"an element that stores a nonnegligible amount of energy from an input electromagnetic (EM) signal"	"an element *of an energy transfer system* that stores non-negligible amounts of energy from an input electromagnetic signal"

See Ex. 1026, 5 (emphases added). We consider the district court's construction as we analyze the meaning of "storage element" based on the complete record before us.

As reflected in the arguments above, Patent Owner's proposed construction in this proceeding matches the district court's final construction in the related litigation. Petitioner, however, presents the same construction here that it proposed in the related litigation. The parties' proposed constructions in this proceeding are reflected in the chart below.

Term	Patent Owner's Proposed Construction	Petitioner's Proposed Construction
"storage element"	"an element *of an energy transfer system* that stores non-negligible amounts of energy from an input electromagnetic signal"	"an element that stores a nonnegligible amount of energy from an input electromagnetic (EM) signal"

See, e.g., PO Resp. 4 (emphasis altered); Pet. Reply 10 (emphasis added).

We begin with the plain language of claim 3. Claim 3, as reproduced above, is directed to "[a] wireless modem apparatus, comprising a receiver for frequency down-converting an input signal." Ex. 1001, 61:1–3. Claim 3 recites several structural requirements of the claimed receiver including "a

first frequency down-conversion module," "a second frequency down-conversion module," and "a subtractor module." *Id.* at 61:4–15. Claim 3 further recites two structural requirements of the first and second frequency down-conversion modules—"a switch and a storage element." *Id.* at 61:16–18. Neither party contends that the claim language itself informs as to the meaning of "storage element" beyond the words "storage" and "element." The term "energy transfer" is not recited in claim 3 and neither party points to *other* language in claim 3 (aside from "storage element") to argue that the claim must be understood to require an energy transfer system.

Turning to the Specification of the '444 patent, the parties agree that it has little significance apart from its incorporation of the '551 patent by reference. *See, e.g.*, Ex. 1001, 9:30–38. Aside from incorporating the '551 patent, the parties do not rely on the Specification of the '444 patent to inform as to the meaning of "storage element." Thus, our focus is on the specification of the '551 patent.

Despite their differences, the parties' discussions of the '551 patent (as reflected above) are similar. For example, it is undisputed that the '551 patent teaches "down-converting an electromagnetic (EM) signal by aliasing the EM signal" and that "[t]he term aliasing, as used [therein], refers to both down-converting an EM signal by under-sampling the EM signal at an aliasing rate, and down-converting an EM signal by transferring energy from the EM signal at the aliasing rate." Ex. 2007, code (57). Despite Patent Owner's use of the phrases "voltage sampling" and "energy sampling," the parties agree (as do we) that the '551 patent expressly describes these two methods as "under-sampling" and "energy transfer."

It is clear from the '551 patent's "Table of Contents" that the specification is structured to provide an overview of the invention and then include different sections addressing "Under-Sampling" and "Energy Transfer." *See, e.g.*, Ex. 2007, cols. 9–13 (Table of Contents). It is in section "0.1.2 Introduction to Energy Transfer" where the parties primarily focus their arguments. We find this section particularly noteworthy and informative. This section begins by comparing an energy transfer system to an under-sampling system. In making the comparison, the '551 patent specifically focuses on what it refers to as "an energy transfer signal" compared to "an under-sampling signal": "In an embodiment, the present invention transfers energy from an EM signal *by utilizing an energy transfer signal instead of an under-sampling signal*." *Id.* at 66:34–36. The '551 patent continues to describe the comparison: "Unlike under-sampling signals that have negligible aperture pulses, the energy transfer signal includes a train of pulses having non-negligible apertures that tend away from zero." *Id.* at 66:36–39. The '551 patent explains that "this"—the train of pulses having non-negligible apertures that tend away from zero—"provides more time to transfer energy from an EM input signal." *Id.* at 66:39–40. By these statements, the '551 patent provides a direct link between (a) using of a train of pulses having non-negligible apertures that tend away from zero and (b) the result of providing more time to transfer energy.

The '551 patent also lists several benefits flowing from using a train of pulses having non-negligible apertures that tend away from zero, including (1) "that the input impedance of the system is reduced so that practical impedance matching circuits can be implemented to further

improve energy transfer and thus overall efficiency," (2) "[t]he non-negligible transferred energy significantly improves the signal to noise ratio and sensitivity to very small signals, as well as permitting the down-converted signal to drive lower impedance loads unassisted," (3) "[s]ignals that especially benefit include low power ones typified by RF signals," and (4) "[o]ne benefit of a non-negligible aperture is that phase noise within the energy transfer signal does not have as drastic of an effect on the down-converted output signal as under-sampling signal phase noise or conventional sampling signal phase noise does on their respective outputs." Ex. 2007, 66:40–54.

Turning to what we consider a critical paragraph and disclosure of the '551 patent (Ex. 2007, 66:55–67), the patent precisely explains the use of the term "storage module," which, as noted above, the parties agree is synonymous with "storage element." The first sentence states that Figure 82A, reproduced below, "illustrates an exemplary energy transfer system 8202 for down-converting an input EM signal." Ex. 2007, 66:55–56.

FIG. 82A

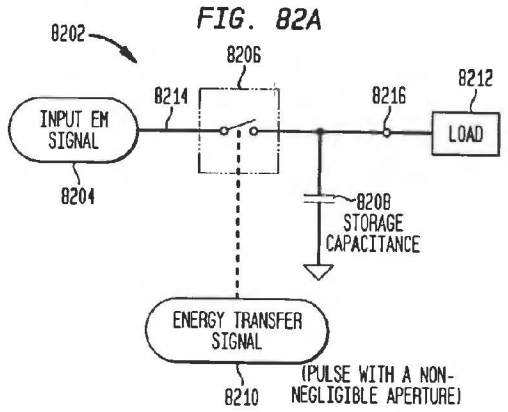


Figure 82A illustrates an exemplary energy transfer system. *Id.* at 7:47–48. The '551 patent explains that "[t]he energy transfer system 8202 includes a

switching module 8206 and a storage module illustrated as a storage capacitance 8208." *Id.* at 66:56–59. Critically, the '551 patent states:

> The terms storage module and storage capacitance, as used herein, are distinguishable from the terms holding module and holding capacitance, respectively. Holding modules and holding capacitances, as used above, identify systems that store negligible amounts of energy from an under-sampled input EM signal with the intent of "holding" a voltage value. *Storage modules and storage capacitances, on the other hand, refer to systems that store non-negligible amounts of energy from an input EM signal.*

Id. at 66:59–67 (emphasis added).

This portion of the '551 patent specification provides a lexicographic definition of the systems to which the terms refer. In particular, "holding modules" "identify systems that store negligible amounts of energy from an under-sampled input EM signal with the intent of 'holding' a voltage value" whereas "storage modules" "*refer* to systems that store non-negligible amounts of energy from an input EM signal." *Id.* (emphasis added). Because the parties agree that "storage element" and "storage module" are synonymous, we determine that the patentees acted as their own lexicographers and deliberately defined the systems to which "storage element" refers as "systems that store non-negligible amounts of energy from an input EM signal." *Id.* As reflected in the parties' proposed constructions above, the parties also agree that the meaning of "storage element" includes the term "element." Thus, applying the lexicographic definition of the systems to which "storage element" refers, we determine that one of ordinary skill in the art would have understood "storage element" to mean "an element of a system that stores non-negligible amounts of energy from an input EM signal."

We do not agree with Patent Owner that "system" should be limited to "energy transfer system." Critically, if the patentees wanted to limit the term "storage element" beyond the express definition of the systems to which the term refers, it was incumbent upon the patentees to do so; *and they did not*. The aspect chosen by the patentees to provide the critical distinction between "storage element" and "holding element"[11] is not whether one refers to "an energy transfer system"; rather, it is the clause that follows the word "system" and there are two choices provided by the patentees—(1) "systems that store negligible amounts of energy from an under-sampled input EM signal with the intent of 'holding' a voltage value," and (2) "systems that store non-negligible amounts of energy from an input EM signal." That is how the patentees specifically set forth the distinction between the terms and that is the distinction we express in the construction of "storage element."

We recognize that the parties vigorously dispute the construction of "storage element" and that the patentees' definition in the '551 patent is different than the district court's construction. We also recognize that the parties agree that only two methods of down-converting an EM signal are disclosed in the '551 patent—(1) under-sampling and (2) energy transfer. The above-quoted paragraph of the '551 patent expressly links "holding module" to an under-sampling method, by expressly including the phrase "from an under-sampled input EM signal." But, the '551 patent does not include the phrase "energy transfer system" in its definition of the systems to

[11] The patentees specifically refer to "storage module" and "holding module," which as we indicate above are synonymous with "storage element" and "holding element."

which "storage element" refers. Rather, the '551 patent, as explained above, expressly defines "storage elements" as referring to "systems that store non-negligible amounts of energy from an input EM signal." Thus, to the extent a system stores non-negligible amounts of energy from an input EM signal, it would be within the scope of the express lexicographic meaning of "storage module" whether or not it is *also* an energy transfer system. The "naming convention" that Patent Owner complains of is the patentees' own lexicographic definition. It is not appropriate to re-write a definition expressly set forth in the patent simply because an assignee complains that the definition does not focus on "how the technology actually works." *Contra* PO Sur-reply 8 (citations omitted). As the United States Court of Appeals for the Federal Circuit has repeatedly stated, "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Phillips*, 415 F.3d at 1316 (citation omitted).[12]

[12] Patent Owner's attempt to read "energy transfer" into the meaning of "storage element" is not insignificant. In particular, Patent Owner asserts that four "key features" distinguish energy transfer systems and the implication of Patent Owner's argument is that, if "energy transfer" were read into the meaning of "storage element," then all four "key features" would also be read into the meaning of the claim term—(1) non-negligible sampling aperture; (2) storage module; (3) low impedance load; and (4) down-converted signal includes the energy transferred from the RF signal to the load (i.e., energy sent to the load makes up the down-converted signal). *See* PO Resp. 32 (chart listing "key features" of energy transfer systems). We need not decide whether "energy transfer" requires any of the four alleged "key features" because we do not limit the patentees' lexicographic definition to "energy transfer" systems.

Additionally, we note that Patent Owner proposed a construction for "storage module" in IPR2014-00948 that did not include the phrase "energy transfer system." In particular, relying on the same disclosures of the '551 patent, Patent Owner proposed that "storage module" (in a related patent claim) "be construed to mean 'an apparatus that stores non-negligible amounts of energy from the carrier signal.'" Ex. 1032, 21–22. Patent Owner now argues that its proposed construction of "storage module" in IPR2014-00948 is inconsequential because, at that time, the Board applied the broadest reasonable interpretation standard in claim construction and Patent Owner's proposed construction was, therefore, broader than what it now proposes. PO Sur-reply 12–13. We do not agree with Patent Owner's attempt to distinguish its prior argument from IPR2014-00948 on the basis that it applied a different claim construction standard because Patent Owner clearly stated that "[t]he Specification *provides an explicit definition* that supports this construction" and that "[t]he incorporated *'551 Specification explicitly defines a storage module and draws the distinction between storage modules and holding modules*." Ex. 1032, 21 (emphases added). These statements by Patent Owner confirm that Patent Owner understood *its own '551 patent* to (a) provide *an explicit definition* of "storage module" and (b) draw a distinction between storage modules and holding modules. The steps of claim construction, whether applying the broadest reasonable interpretation standard or the standard used in federal courts under 35 U.S.C. § 282(b), include "look[ing] to the specification to see if it provides a definition for claim terms." *In re ICON Health and Fitness, Inc.*, 496 F.3d 1374, 1379 (Fed. Cir. 2007) (applying the broadest reasonable interpretation standard); *see Phillips*, 415 F.3d at 1316 (applying the standard used in

federal courts and stating that "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs.") (citation omitted). Thus, Patent Owner's acknowledgement that the '551 patent provides an explicit definition of "storage module" directly supports our determination that the patentees acted as lexicographers, which the case law confirms controls.

Neither party relies upon the prosecution history of the '444 patent or any related patent. And, we do not find the prosecution history informative as to the disputed aspect of the meaning of "storage element" (i.e., whether "energy transfer" should be read into the claim). *See generally* Ex. 1003 (prosecution history of the '444 patent).

Turning to extrinsic evidence,[13] Patent Owner, as reflected above, argues that Dr. Steer agreed with its proposed construction, whereas Dr. Subramanian did not offer an express opinion on the meaning of "storage element." Although we have considered Dr. Steer's testimony, we find it "less significant than the intrinsic record in determining the legally operative meaning of" "storage element." *Phillips*, 415 F.3d at 1317 (internal quotations and citations omitted). In particular, we are cognizant of the Federal Circuit's guidance that we "should discount any expert

[13] Although, in the Petition, Petitioner initially relied on two dictionary definitions of a "capacitor" in support of its analysis that Tayloe's capacitor teaches the recited "storage element" (*see* Pet. 77 (citing Ex. 1014 (Microsoft Press Computer Dictionary (2d ed. 1994)) (defining "capacitor"); Ex. 1015 (IBM Dictionary of Computing (10th ed. 1994)) (defining "capacitor"))), neither party relies upon a dictionary definition in support of their proposed constructions of "storage element."

testimony that is clearly at odds with the claim construction mandated by . . . the written description." *Id.* at 1318 (internal quotation and citation omitted). In this instance, we find that Dr. Steer's testimony is clearly at odds with the lexicographic definition provided in the '551 patent because the definition does not include "energy transfer" in the meaning of "storage element." In particular, Dr. Steer (and Patent Owner) seek to read an additional limitation of "energy transfer" into the definition of "storage element" provided by the specification. Therefore, although we appreciate and recognize Dr. Steer's discussion of the "background on the technology at issue" and "how [the] invention works," we do not find that his testimony trumps the express definition provided in the specification. *See id.* ("extrinsic evidence in the form of expert testimony can be useful to a court for a variety of purposes," including, *inter alia*, "to provide background on the technology at issue" or "to explain how an invention works") (citations omitted).

Based on our review of the complete record before us, including the intrinsic and extrinsic evidence, we determine that one of ordinary skill in the art would understand "storage element" to mean "an element of a system that stores non-negligible amounts of energy from an input EM signal."

B. Other Claim Terms

Petitioner presents two other claim terms recited in claim 3 for construction—"frequency down-conversion module" and "subtractor module." Pet. 28–31. And, Patent Owner presents an additional term for construction in its Patent Owner Response—"switch." PO Resp. 45. In its Reply, Petitioner notes that Patent Owner does not argue that the combinations of prior art asserted by Petitioner lack any of these elements,

and, therefore, there is no need for us to construe the terms. Pet. Reply 16–18. Patent Owner does not appear to address these terms in its Sur-reply. *See generally* PO Sur-reply.

We decline to construe these additional terms because their constructions are not necessary to resolve the present controversy between the parties. *See Vivid Techs.*, 200 F.3d at 803 (holding that "only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy"); *Nidec Motor Corp.*, 868 F.3d at 1017 (citing *Vivid Techs.* in the context of an *inter partes* review).

III. ANALYSIS

A. Legal Standards – Obviousness

The U.S. Supreme Court set forth the framework for applying the statutory language of 35 U.S.C. § 103 in *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966):

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.

The Supreme Court explained in *KSR International Co. v. Teleflex Inc.* that

> [o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion

> claimed by the patent at issue. To facilitate review, this analysis should be made explicit.

550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.")).

"Whether an ordinarily skilled artisan would have been motivated to modify the teachings of a reference is a question of fact." *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1327 (Fed. Cir. 2016) (citations omitted). "[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan 'would have had a reasonable expectation of success from doing so.'" *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

B. Obviousness over Tayloe and TI Datasheet

Petitioner asserts the combination of Tayloe and TI Datasheet would have rendered the subject matter of claim 3 obvious to one of ordinary skill in the art at the time of the invention. Pet. 43–47 (discussing motivation to combine), 47–78 (discussing the application of the art to claim 3).

1. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is set forth above. *See supra* § I.G.

2. Scope and Content of the Prior Art

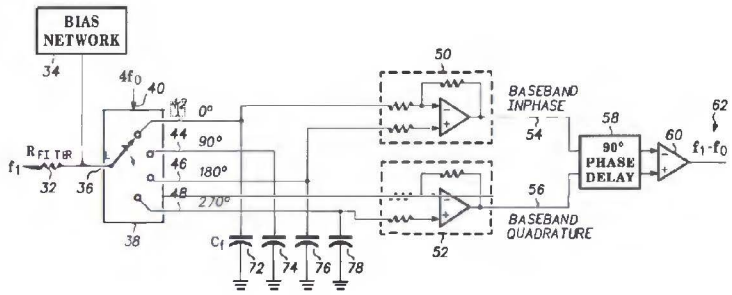
a. Tayloe

Tayloe is directed to a direct conversion receiver (also referred to as a "product detector") "for converting a signal to baseband." Ex. 1004, code (57); *see id.* at 1:51–52 (describing Figure 3). Tayloe explains that its direct conversion receiver

> includes a commutating switch which serves to sample an RF waveform four times per period at the RF frequency. The samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees. The average voltage at 0 degrees is the baseband in-phase signal . . . .

Id. at code (57). Tayloe discloses that, "[a]lternatively, to increase gain, the 0 degree average can be differentially summed with the 180 degree average to form the baseband in-phase signal . . . ." *Id.* Tayloe states that "[d]irect conversion receivers are desirable in part because they convert signals of interest directly to baseband (or near zero hertz) from a radio frequency (RF) or an intermediate frequency (IF)." *Id.* at 1:10–13.

Tayloe's Figure 3 is reproduced below:



30 FIG. 3

Tayloe's Figure 3 "shows a direct conversion receiver." Ex. 1004, 1:51–52. Tayloe discloses the following regarding the operation of the direct conversion receiver shown in the Figure 3:

> [A]n RF or IR signal f_1 is received at resistor 32. . . . After passing through resistor 32, the input signal is received by commutating switch 38 at input 36. Commutating switch 38 switches input 36 to outputs 42, 44, 46, and 48. The rate at which commutating switch 38 operates is controlled by a signal present at control input 40. In the preferred embodiment as shown in FIG. 3, the control signal input to control input 40 is substantially equal to four times the local oscillator frequency that would exist in a simple direct conversion receiver. As a result, input 36 is switched to each of the four outputs substantially once during each period of the input signal f_1.
>
> In the preferred embodiment, commutating switch 38 remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal. In alternate embodiments, commutating switch 38 remains closed at each of the four outputs for less than 90 degrees.
>
> During the time that commutating switch 38 connects input 36 to output 42, charge builds up on capacitor 72. Likewise, during the time commutating switch 38 connects input 36 to output 44, charge builds up on capacitor 74. The same principle holds true for capacitors 76 and 78 when commutating switch 38 connects input 36 to outputs 46 and 48 respectively. As commutating switch 38 cycles through the four outputs, capacitors 72–78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants. . . .
>
> Output 42 represents the average value of the input signal during the first quarter wave of the period, and is termed the 0 degree output. Output 44 represents the average value of the input signal during the second quarter wave of the period, and is termed the 90 degree output. Output 46 represents the average value of the input signal during the third quarter wave of the period, and is termed the 180 degree output. Output 48 represents the average value of the input signal during the fourth quarter wave of the period, and is termed the 270 degree output.

Id. at 2:13–55.

Tayloe describes the following regarding summing amplifiers 50 and 52:

> The outputs of commutating switch 38 are input to summing amplifiers 50 and 52. Summing amplifier 50 differentially sums the 0 degree output [42] and the 180 degree output [46], thereby producing baseband in-phase signal 54. Summing amplifier 52 differentially sums the 90 degree output and the 270 degree output, thereby producing baseband quadrature signal 56. Baseband in-phase signal 54 and baseband quadrature signal 56 are input to phase delay 58 which shifts the phase of baseband quadrature signal 56 by 90 degrees relative to baseband in-phase signal 54. The resulting signals are then summed by summing amplifier 60 to produce the signal of interest 62.

Ex. 1004, 2:56–67. Summing amplifiers 50, 52, and 60 show "+" and "-" input ports. *Id.* at Fig. 3.

Tayloe's Figure 4 is reproduced below:

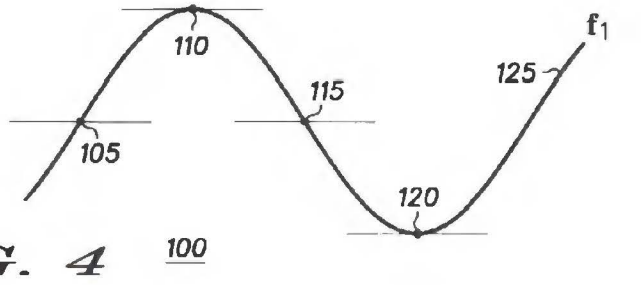


FIG. 4

Tayloe's Figure 4 "shows a waveform." Ex. 1004, 1:53–54. Tayloe explains the following regarding Figure 4:

> Waveform 100 includes signal 125 which corresponds to the input signal f_1. Superimposed on signal 125 are points 105, 110, 115, and 120. Point 105 represents the voltage to which capacitor 72 (FIG. 3) charges. Likewise, point 110 represents the voltage to which capacitor 74 charges, point 115 represents the voltage to which capacitor 76 charges, and point 120 represents the voltage to which capacitor 78 charges.

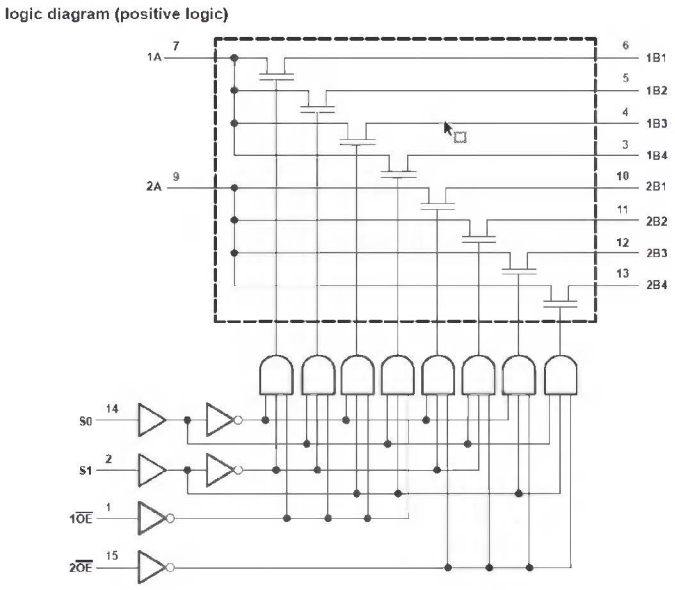
Id. at 3:40–48.

Tayloe further discloses the equipment used to achieve its stated experimental results, explaining: "A direct conversion receiver which utilizes a Tayloe Product Detector has been built. The receiver design is the same as direct conversion receiver 30 (FIG. 3) utilizing an analog multiplexer and a digital counter as shown in FIG. 7. The analog multiplexer is a Texas Instruments SN74BCT3253D." Ex. 1004, 5:32–37.

b. TI Datasheet

TI Datasheet is directed to SN74CBT3253, a "dual 1-of-4 high-speed [transistor-transistor logic]-compatible [field-effect transistor] multiplexer/demultiplexer." Ex. 1005, 1. TI Datasheet states "[t]he low on-state resistance of the switch allows connections to be made with minimal propagation delay." *Id.*

TI Datasheet includes the following figure:



The above figure illustrates a logic diagram (positive logic). Ex. 1005, 2. TI Datasheet explains "1$\overline{OE}$, 2$\overline{OE}$, S0, and S1 select the appropriate output for the A-input data." *Id.* at 1.

3. Differences Between the Prior Art and Claim 3; Motivation to Modify

a. Uncontested Elements of Claim 3

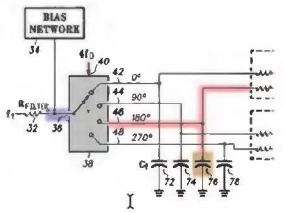
For elements [3preamble] and [3A]–[3D], Petitioner relies upon its arguments and evidence presented with respect to its challenge to claim 1. Pet. 74–75 (referring to elements of claim 1) (citing Ex. 1002 ¶¶ 148–149). In the Patent Owner Response, Patent Owner does not contest Petitioner's showing with respect to these elements; rather, Patent Owner's argument is focused entirely on whether the combination of Tayloe and TI Datasheet teaches or suggests the "storage element" recited in element [3E]. *See, e.g.*, PO Resp. 53–70 (contending that Tayloe discloses capacitors that are "holding" elements and not "storage" elements because Tayloe teaches (1) a voltage sampling system and (2) a high impedance load), 72–74 (contending that Tayloe does not teach "storage elements" because "the capacitors of Tayloe are *not* elements of 'an energy transfer system'" and there is "no teaching, suggestion, or motivation in Tayloe to use *energy* sampling to down-convert a signal").

We have reviewed Petitioner's arguments and evidence in support thereof as to how the combination of Tayloe and TI Datasheet teaches or suggests elements [3preamble] and [3A]–[3D]. *See* Pet. 74–75 (addressing claim 3), 43–47 (addressing motivation to combine Tayloe and TI Datasheet as well as reasonable expectation of success), 47–69 (addressing claim elements [1preamble] and [1A]–[1D]). We find Petitioner's arguments persuasive and supported sufficiently on the complete record before us, and, therefore, we adopt them as our own findings. Accordingly, for the reasons explained by Petitioner, we find that the combination of Tayloe and TI Datasheet teaches or suggests elements [3preamble] and 3[A]–3[D].

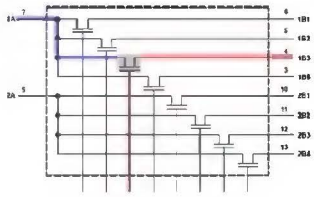
b. Element [3E]

i. The Parties' Arguments

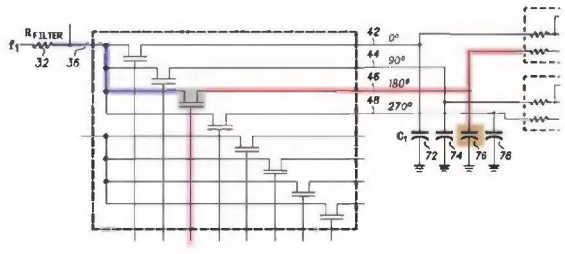
Element [3E] recites "wherein said first and said second frequency down-conversion modules each comprise a switch and a storage element." Ex. 1001, 61:16–18.[14] Petitioner contends that "Tayloe in view of TI Datasheet discloses this limitation." Pet. 75. In particular, and with reference to several annotated figures reproduced below, Petitioner asserts that "the combination of Tayloe and TI [D]atasheet teaches a first frequency down-conversion module (for Tayloe's 180° output 46 (red)) comprising a first switch (TI Datasheet's transistor (gray)) and a first capacitor (Tayloe's capacitor 76 (brown))." *Id.* at 75–76 (citing Ex. 1002 ¶ 150).



Ex. 1004-Tayloe
Fig. 3



Ex. 1005-TI
Datasheet. 2



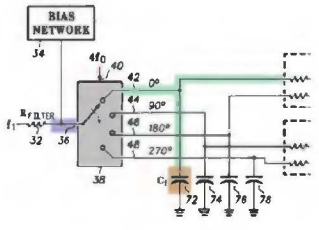
Combined Teachings

Id. at 76. Petitioner's annotated figures, shown above, include (1) Tayloe's Figure 3, (2) a portion of TI Datasheet's "logic diagram (positive logic),"

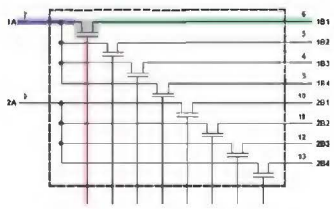
[14] Even though some of the discussion below refers to a "storage element," we recognize that element [3E] recites that the first and second frequency down-conversion modules *each* comprise a storage element.

and (3) a figure prepared by Petitioner showing the "Combined Teachings." *Id.* Petitioner added several colors to highlight various aspects of the figures, shown above. *Id.*

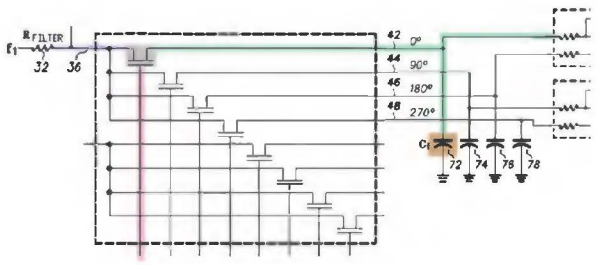
Similar to its analysis of the recited "first frequency down-conversion module" and, again, with reference to several annotated figures reproduced below, Petitioner contends that the combination of Tayloe and TI Datasheet also "teaches a second frequency down-conversion module (for Tayloe's 0° output 42 (green)) comprising a second switch (TI Datasheet's transistor (gray)) and a second capacitor (Tayloe's capacitor 72 (brown))[]." Pet. 76–77 (citing Ex. 1002 ¶ 151).



Ex. 1004-Tayloe
Fig. 3



Ex. 1005-TI
Datasheet. 2



Combined Teachings

Id. at 77. Petitioner's annotated figures, shown above, include (1) Tayloe's Figure 3, (2) a portion of TI Datasheet's "logic diagram (positive logic)," and (3) a figure prepared by Petitioner showing the "Combined Teachings."

Id. Petitioner added several colors to highlight various aspects of the figures, shown above. *Id.*

Additionally, Petitioner asserts that "[a] capacitor is a well-known storage element, and in fact, the '444 patent embodiment discloses a capacitor as the storage element." Pet. 77 (citing Ex. 1001, 34:22–23, 36:14–15; Ex. 1014; Ex. 1015; Ex. 1002 ¶ 152).

In the Patent Owner Response, Patent Owner asserts that the capacitors in Tayloe "are not '*storage*' elements' because the capacitors of Tayloe are *not* elements of 'an *energy* transfer system.'" PO Resp. 73. In contrast, Patent Owner asserts that "Tayloe is a *voltage* sampling system – a *fundamentally different and competing* technology to energy transfer (energy sampling). As such, the capacitors in Tayloe are '*holding* elements' (a term *reserved* by the '444 patent for elements of a sample-and-hold (voltage sampling) system." *Id.*

Additionally, Patent Owner contends that "there is no teaching, suggestion, or motivation in Tayloe to use *energy* sampling to down-convert a signal." PO Resp. 73 (citing Ex. 2021 ¶ 283). Rather, according to Patent Owner, "the opposite is true. All teaching, suggestion, and motivation in Tayloe demonstrates that Tayloe only relates to a *sample-and-hold* (*voltage* sampling) system." *Id.* (citing Ex. 2021 ¶ 283; PO Resp. § VIII.A); *see id.* (noting that "Tayloe consistently refers to voltage and voltage sampling concepts for down-conversion") (citing Ex. 2021 ¶ 242). Patent Owner contends that "the term 'energy' does not appear anywhere in Tayloe[,] nor would a [person of ordinary skill in the art] understand Tayloe as teaching or suggesting use of energy sampling for down-conversion." *Id.* (citing Ex. 2021 ¶ 242).

Patent Owner asserts that "whether a capacitor is a '*storage* element' depends on the *way* in which the capacitor is being used in a circuit." PO Resp. 74 (citing Ex. 2021 ¶ 193). Patent Owner argues that Petitioner "ignores that capacitors are used in different ways in Tayloe and claim 3 of the '444 patent." *Id.* (citing Ex. 2021 ¶ 172). Patent Owner explains as follows:

> Whereas the high impedance load in a sample-and-hold (voltage sampling) system (as in Tayloe) causes a capacitor to *hold* energy (i.e., *prevent* energy in the capacitor from being discharged to form the down-converted signal), the *low* impedance load in an energy transfer (energy sampling) system (as in claim 3) has the opposite effect. Ex. 2021 ¶168. A low impedance load enables a capacitor to *store* energy and then *discharge* the stored energy in between samples to form the down-converted signal (i.e., the discharged energy itself becomes part of the down-converted signal). Ex. 2021 ¶¶168, 173. The way in which capacitors are used in energy transfer (energy sampling) systems results in such systems having significant benefits that were not recognized by a [person of ordinary skill in the art] at the time of the invention of the '444 patent. Ex. 2021 ¶169.

PO Resp. 74.

Further, Patent Owner contends that "it would not have been obvious to a [person of ordinary skill in the art] to replace the voltage sampling configuration of Tayloe with an energy sampling configuration." PO Resp. 74 (citing Ex. 2021 ¶ 288). Patent Owner asserts, "[t]here are numerous secondary considerations of non-obviousness demonstrating that such a dramatic modification of Tayloe was not envisioned by a [person of ordinary skill in the art] at the time of the invention of the '444 patent."[15] *Id.*

[15] Patent Owner's assertions of secondary considerations of non-obviousness are addressed below. *See infra* § III.B.4.

at 74–75 (citing Ex. 2021 ¶¶ 228–239). Patent Owner argues that "to get the invention of the '444 patent using Tayloe, one would have to *ignore* all of the disclosure in Tayloe, *abandon* all of the teachings and suggestions of Tayloe, and *ignore* the state-of-the-art for direct down-conversion at the time of the invention of the '444 patent." *Id.* at 75 (citing Ex. 2021 ¶ 289). Patent Owner asserts that "one would have to use hindsight (knowledge of the '444 patent) to modify Tayloe to use a *low* impedance load and *energy* sampling to get to the invention of claim 3 of the '444 patent." *Id.* (citing Ex. 2021 ¶ 289). And, Patent Owner contends "secondary considerations demonstrate that the invention of claim 3 of the '444 patent was not obvious in view of Tayloe." *Id.* (citing Ex. 2021 ¶¶ 228–239, 289).

With respect to TI Datasheet, Patent Owner asserts that it "merely describes a possible switch configuration for use with Tayloe. But the TI [D]atasheet does not change the fundamental nature of Tayloe as a *voltage* sampling system using 'holding' modules/elements. As such, the TI Datasheet does not cure the deficiencies of Tayloe." PO Resp. 75 (citing Ex. 2021 ¶ 291).

In its Reply, Petitioner contends that Patent Owner's "sole validity argument for claim 3 is that Tayloe does not disclose a 'storage element' under [Patent Owner's] proposed construction of the term. There is no dispute that under [Petitioner's] (proper) construction, Tayloe discloses the 'storage element.'"[16] Pet. Reply 18.

[16] Petitioner also asserts that "even under [Patent Owner's] proposed construction, Tayloe discloses a 'storage element.'" Pet. Reply 18; *see id.* at 20–27. We need not reach these arguments because we do not adopt Patent Owner's proposed construction of "storage element."

Petitioner contends that "Tayloe clearly discloses that its capacitors 72–78 store non-negligible amounts of energy from the input signal." Pet. Reply 19. Petitioner asserts that Tayloe's capacitors are "***tens of thousands of times*** larger than the capacitors in the energy transfer embodiments of the '551 patent." *Id.* (*comparing* Ex. 1004, 5:50–52 (Tayloe's capacitors at 0.3 microfarads (or 300,000 picofarads (pF))), *with* Ex. 2007, 67:22–25 (disclosing *storage* capacitance 8208 at 18pF)). Petitioner explains that Tayloe teaches (1) its capacitors charge to the average level of the input signal (*id.* (citing Pet. 32–33; Ex. 1004, 2:33–45, 4:28–45)), and (2) its capacitors integrate the input signal, which Petitioner asserts "indicates an accumulation of energy and matches the '551 patent's description of a storage module's operation" (*id.* at 19–20 (citing Ex. 1004, 4:46–47, 2:42–44; Ex. 2007, claims 198–202)). Thus, Petitioner asserts that "[t]he quantity of energy stored on Tayloe's capacitors is plainly non-negligible." *Id.* at 20 (citing Ex. 1030 ¶¶ 6–14).

From a high level, Patent Owner's Sur-reply raises the following arguments: (1) Tayloe's capacitors only hold a negligible amount of energy from an input EM signal (PO Sur-reply 1), (2) "storage element" should be construed such that it is limited to an "energy transfer system" (*id.* at 2), (3) an "energy transfer system" should be limited to driving a low impedance load (*id.* at 2–3), and (4) Tayloe discloses a high impedance load, not a low impedance load (*id.* at 3).

ii. Discussion

To begin, we agree with Petitioner that the arguments asserted in Patent Owner's Response, and Dr. Steer's testimony in support thereof, are entirely dependent upon Patent Owner's proposed construction of "storage

element," which we do not adopt. Therefore, our focus below is on the arguments raised in Patent Owner's Sur-reply, which either respond to Petitioner's arguments or raise new arguments that we have excluded (as explained below).

Addressing Patent Owner's Sur-reply arguments slightly out of order, the second, third, and fourth arguments are each directed to Patent Owner's proposed construction of "storage element," which we do not adopt. In particular, as noted above, those arguments focus on various aspects that Patent Owner contends are required by an "energy transfer system," including whether "storage element" should be limited thereto, whether a low impedance load is required, and whether Tayloe discloses a low impedance load. *See, e.g.*, PO Sur-reply 2–3. Those arguments do not address Petitioner's challenge when "storage element" is construed as we have here, in accordance with the lexicographic definition provided in the '551 patent.[17] Thus, we focus below on Patent Owner's arguments in response to Petitioner's assertion that Tayloe teaches a "storage element," as we construe the term.

Turning back to Patent Owner's first argument (whether Tayloe's capacitors hold a negligible or non-negligible amount of energy from an input EM signal), that argument includes positions that were first raised in the Sur-reply, which, as discussed further below, we determined are

[17] Patent Owner's argument also includes its contention that Dr. Subramanian allegedly admitted that Tayloe's operational amplifiers are high impedance loads. *See* PO Sur-reply 3–6 (addressing whether Tayloe teaches high or low impedance loads). That argument by Patent Owner also is directed to Patent Owner's claim construction position, which we do not adopt.

impermissible under our Rules and, therefore, excluded from consideration in this proceeding. *See infra* § III.D; *see also* Tr. 6:24–7:23 (reiterating the ruling made during the pre-hearing conference). Also, as discussed below, our exclusion includes Exhibit 2022 because it was filed in violation of 37 C.F.R. § 42.23(b) and in support of Patent Owner's improperly asserted sure-reply arguments. In light of that ruling, we limit our discussion of Patent Owner's first argument to the arguments that are not excluded.[18]

Patent Owner contends that the "[t]he capacitors of Tayloe . . . only hold a *negligible* . . . amount of energy from an input EM signal." PO Sur-reply 1. Patent Owner asserts that "[h]ow much energy is stored depends on the specific components/configuration of a system."[19] *Id.* Although somewhat intertwined with its claim construction argument, Patent Owner also contends that, "[s]ince Tayloe is simply capturing a voltage measurement, a Tayloe capacitor only holds *negligible* amounts of energy . . . ." *Id.* at 7. Further, Patent Owner argues that, "for the first time in its Reply, [Petitioner] focuses on the size of Tayloe's capacitor and that Tayloe's capacitors accumulate energy over time." *Id.* at 17 (citing Pet. Reply 19). Patent Owner asserts that "this superficial analysis provides no

[18] As discussed herein, not all of Patent Owner's arguments as to whether Tayloe discloses capacitors that hold a non-negligible amount of energy from an input EM signal were excluded. That specific delineation is discussed *infra* and also is set forth clearly in Petitioner's Identification.
[19] This argument by Patent Owner also responds to Petitioner's alternative position that Tayloe teaches an "energy transfer system" (under Patent Owner's proposed construction of "storage element") because Tayloe discloses a control signal with non-negligible aperture widths. *See* PO Sur-reply 1.

insight into whether a Tayloe capacitor stores *non*-negligible amounts of energy."[20] *Id.*

Based on the full record before us, we find Petitioner's argument and evidence persuasive to show that Tayloe's capacitors 72–78 teach the recited "storage element" because Petitioner establishes sufficiently that Tayloe's capacitors are "element[s] of a system that store[] non-negligible amounts of energy from an input EM signal." In particular, we find Dr. Subramanian's testimony persuasive to show that "the amount of energy stored in one of Tayloe's capacitors 72-78 is . . . 0.6 μJ (microjoules)" and that one of ordinary skill in the art "would [have understood] that this quantity is a significant amount of energy in the context of a down-conversion system such as that disclosed in Tayloe." Ex. 1030 ¶ 12 (citing Ex. 1004, 5:38–41, 5:49–52); *see id.* ¶ 13 ("the energy transferred is distinguishable from noise" and "is also not minor or inconsequential but rather is important for the formation of the down-converted signal in Tayloe").

Additionally, Dr. Subramanian's testimony and Tayloe's disclosure supports Petitioner's arguments that (a) Tayloe's capacitors are "***tens of thousands of times*** larger than the capacitors in the energy transfer embodiments of the '551 patent" (Pet. Reply 19 (*comparing* Ex. 1004, 5:50–52 (Tayloe's capacitors at 0.3 microfarads (or 300,000 picofarads (pF))), *with* Ex. 2007, 67:22–25 (disclosing *storage* capacitance 8208 at 18pF)); (b) Tayloe's capacitors charge to the average level of the input signal (*id.* (citing Pet. 32–33; Ex. 1004, 2:33–45, 4:28–45)); and (c) Tayloe's capacitors integrate the input signal, which "indicates an accumulation of

[20] The remainder of Patent Owner's Sur-reply arguments are either directed to its incorrect claim construction position or are excluded.

energy and matches the '551 patent's description of a storage module's operation" (*id.* at 19–20 (citing Ex. 1004, 4:46–47, 2:42–44; Ex. 2007, claims 198–202)).

Patent Owner's arguments that remain for our consideration, as noted above, do not detract from Petitioner's arguments and evidence (particularly Dr. Subramanian's testimony in support thereof) because Patent Owner does not identify any deficiencies therein that would lead us to find otherwise. In particular, Petitioner's analysis considers "the specific components/ configuration of [Tayloe's] system" (as Patent Owner asserts a proper analysis should), and we do not agree that Petitioner's analysis is "superficial" and "provides no insight into whether a Tayloe capacitor stores *non*-negligible amounts of energy" (as Patent Owner contends), for the reasons explained above.

Further, Petitioner sets forth a reason with rational underpinning as to why one of ordinary skill in the art would have been motivated to combine Tayloe and TI Datasheet with a reasonable expectation of success. *See, e.g.*, Pet. 43–47. Although we address Patent Owner's arguments of alleged objective indicia of nonobviousness below, Patent Owner does not challenge, specifically, Petitioner's argument and evidence with respect to motivation to combine the teachings of Tayloe and TI Datasheet or reasonable expectation of success in so doing.[21] We find Petitioner's analysis persuasive and adopt it as our own findings. *See id.*

[21] As discussed below, Patent Owner asserts that it would not have been obvious to replace the voltage sampling configuration of Tayloe with an energy sampling configuration; Patent Owner, however, does not argue that one of ordinary skill in the art would not have combined Tayloe and TI Datasheet. *See, e.g.*, PO Resp. 74–75 (citations omitted).

Accordingly, we find that the combination of Tayloe and TI Datasheet teaches or suggests element 3[E] and that one of ordinary skill in the art would have had a reason with rational underpinning to combine the teachings as proposed with a reasonable expectation of success.

4. Objective Indicia of Nonobviousness

Patent Owner asserts that "it would not have been obvious to a [person of ordinary skill in the art] to replace the voltage sampling configuration of Tayloe with an energy sampling configuration." PO Resp. 74 (citing Ex. 2021 ¶ 288). Patent Owner contends that "[t]here are numerous secondary considerations of non-obviousness demonstrating that such a dramatic modification of Tayloe was not envisioned by a [person of ordinary skill in the art] at the time of the invention of the '444 patent." *Id.* at 74–75 (citing Ex. 2021 ¶¶ 228–239); *see id.* at 75 ("In addition, secondary considerations demonstrate that the invention of claim 3 of the '444 patent was not obvious in view of Tayloe.").

Petitioner raises several arguments in its Reply responding to Patent Owner, including: (1) that Patent Owner improperly incorporates Dr. Steer's testimony by reference without discussing any substance of the cited paragraphs in the Patent Owner Response in violation of 37 C.F.R. § 42.6(a)(3), which prohibits incorporation by reference (Pet. Reply 28); and (2) that, even if considered, Dr. Steer's testimony is "conclusory and factually unsupported" because he "cites no evidence other than his unsupported, subjective opinions," "fails to name a single commercial product practicing the purported invention," asserts "various alleged unexpected results from energy transfer systems . . . but cites no evidence to support his assertion that energy transfer systems yield ***any*** of these results"

and "does not tie any alleged secondary consideration to claim 3's purported invention," thus failing to "establish a nexus between the alleged secondary considerations and the claimed invention" (*id.* at 29–30 (citations omitted)).

Although not required, we note that Patent Owner does not address objective indicia of nonobviousness in its Sur-reply.

Objective indicia of nonobviousness are "only relevant to the obviousness inquiry 'if there is a nexus between the claimed invention and the [objective indicia of nonobviousness].'" *In re Affinity Labs of Tex., LLC*, 856 F.3d 883, 901 (Fed. Cir. 2017) (quoting *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1312 (Fed. Cir. 2006)). For objective indicia of nonobviousness to be accorded substantial weight, their proponent must establish a nexus between the evidence and the merits of the claimed invention. *ClassCo, Inc., v. Apple, Inc.*, 838 F.3d 1214, 1220 (Fed. Cir. 2016). "[T]here is no nexus unless the evidence presented is 'reasonably commensurate with the scope of the claims.'" *Id.* (quoting *Rambus Inc. v. Rea*, 731 F.3d 1248, 1257 (Fed. Cir. 2013)).

A patentee is entitled to a presumption of nexus "when the patentee shows that the asserted objective evidence is tied to a specific product and that product 'embodies the claimed features, and is coextensive with them.'" *Fox Factory, Inc. v. SRAM, LLC*, 944 F.3d 1366, 1373 (Fed. Cir. 2019) (quoting *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1072 (Fed. Cir. 2018) (quoting *Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 229 F.3d 1120, 1130 (Fed. Cir. 2000))); *Lectrosonics, Inc. v. Zaxcom, Inc.*, IPR2018-01129, Paper 33, 32 (PTAB Jan. 24, 2020) (precedential, designated Apr. 14, 2020). On the other hand, a patentee is not entitled to a presumption of nexus if the patented invention is only a component of a

commercially successful machine or process. *Fox Factory*, 944 F.3d at 1373 (reaffirming the importance of the "coextensiveness" requirement).

"[T]he purpose of the coextensiveness requirement is to ensure that nexus is only presumed when the product tied to the evidence of secondary considerations 'is the invention disclosed and claimed.'" *Fox Factory*, 944 F.3d at 1374 (quoting *Demaco Corp. v. F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 1392 (Fed. Cir. 1988)). "[T]he degree of correspondence between a product and a patent claim falls along a spectrum. At one end of the spectrum lies perfect or near perfect correspondence. At the other end lies no or very little correspondence." *Id.* "A patent claim is not coextensive with a product that includes a 'critical' unclaimed feature that is claimed by a different patent and that materially impacts the product's functionality." *Id.* at 1375.

However, "[a] finding that a presumption of nexus is inappropriate does not end the inquiry into secondary considerations." *Fox Factory*, 944 F.3d at 1375. "To the contrary, the patent owner is still afforded an opportunity to prove nexus by showing that the evidence of secondary considerations is the 'direct result of the unique characteristics of the claimed invention.'" *Id.* at 1373–74 (quoting *In re Huang*, 100 F.3d 135, 140 (Fed. Cir. 1996)). "Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, there is no nexus to the merits of the claimed invention," meaning that "there must be a nexus to some aspect of the claim not already in the prior art." *In re Kao*, 639 F.3d 1057, 1068–69 (Fed. Cir. 2011) (emphasis in original). On the other hand, there is no requirement that "objective evidence must be tied exclusively to claim elements that are not disclosed in

a particular prior art reference in order for that evidence to carry substantial weight." *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1331 (Fed. Cir. 2016). A patent owner may show, for example, "that it is the claimed combination as a whole that serves as a nexus for the objective evidence; proof of nexus is not limited to only when objective evidence is tied to the supposedly 'new' feature(s)." *Id.* at 1330.

Ultimately, the fact finder must weigh the objective indicia evidence presented in the context of whether the claimed invention, as a whole, would have been obvious to a skilled artisan. *WBIP*, 829 F.3d at 1331–32. Once the patentee has presented a prima facie case of nexus, the burden of coming forward with evidence in rebuttal shifts to the challenger "to adduce evidence to show that the commercial success was due to extraneous factors other than the patented invention." *Demaco*, 851 F.2d at 1393.

Here, we first note that Patent Owner's arguments as to objective indicia appear to be based on modifying Tayloe to replace what Patent Owner refers to as "the voltage sampling configuration of Tayloe" with "an energy sampling configuration." PO Resp. 74. That modification, however, is not proposed by Petitioner and does not form the basis for our findings herein. Rather, as we discuss above, we decline to construe "storage element" as limited to an "energy transfer system." *See supra* § II.A.2. Thus, in large part, Patent Owner's arguments as to nonobviousness do not respond to Petitioner's arguments and evidence discussed above. Nor does Patent Owner specifically contest Petitioner's arguments and evidence that one of ordinary skill in the art would have had a reason with rational underpinning to combine Tayloe and TI Datasheet with a reasonable expectation of success in so doing, as we discussed above.

Nonetheless, even assuming that all or some of Patent Owner's arguments and Dr. Steer's testimony are directed to the combination of Tayloe and TI Datasheet proposed by Petitioner, Patent Owner's arguments and evidence fail for each of the reasons identified by Petitioner. In particular, Patent Owner's argument consists of two sentences that do no more than assert the phrase "secondary considerations" without providing any explanation or reason in support. *See* PO Resp. 74–75 (quoted in our discussion above). Instead, Patent Owner cites to twelve paragraphs of Dr. Steer's Declaration. *See id.* at 75 (citing Ex. 2021 ¶¶ 228–239). This is precisely the type of incorporation by reference that is prohibited by 37 C.F.R. § 42.6(a)(3), which states "[a]rguments must not be incorporated by reference from one document into another document." *See* Consolidated Trial Practice Guide November 2019, 35–36 ("CTPG") (*available at* https://www.uspto.gov/TrialPracticeGuideConsolidated) ("Thus, *parties that incorporate expert testimony by reference* in their petitions, motions, or replies without providing explanation of such testimony risk having the testimony not considered by the Board." (emphasis added) (citing *Cisco Sys., Inc. v. C-Cation Techs., LLC*, IPR2014-00454, Paper 12 (PTAB Aug. 29, 2014) (informative))). Thus, Patent Owner's failure—to provide any explanation or reason in support of its bare assertion of objective indicia—is a basis, in and of itself, for us not to consider Patent Owner's evidence of nonobviousness. *See* 37 C.F.R. § 42.6(a)(3); CTPG 35–36.

Nonetheless, even if we were to overlook Patent Owner's failure and assume that the entire twelve paragraphs of Dr. Steer's testimony were included in the Patent Owner Response, the evidence of nonobviousness remains insufficient to "be accorded substantial weight" because Patent

Owner fails to "establish a nexus between the evidence and the merits of the claimed invention." *ClassCo*, 838 F.3d at 1220. In particular, neither Patent Owner nor Dr. Steer makes any attempt to establish nexus with the elements recited in claim 3 based on a presumption of co-extensiveness or otherwise. Each instance in which Dr. Steer mentions claim 3, he only ties the discussion to energy transfer systems or energy sampling in general, which is based on Patent Owner's proposed claim construction that we do not adopt. *See, e.g.*, Ex. 1022 ¶¶ 229 ("energy transfer (energy sampling) system – of claim 3"), 230 ("energy sampling as set forth in claim 3"), 233 ("[u]sing energy sampling . . . as set forth in claim 3"), 234 ("energy sampling as set forth in claim 3"), 235 (same), 236 (same), 237 ("using the energy transfer (energy sampling) system of claim 3"), 238 (same), 239 ("energy sampling system as set forth in claim 3"). Thus, we find that Patent Owner fails to establish that a presumption of nexus is warranted and similarly fails to establish nexus absent the presumption. Accordingly, for the reasons above, Patent Owner has not satisfied its burden to establish nexus. *See WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1359 (Fed. Cir. 1999) (patent owner "bears the burden of showing that a nexus exists").

Nonetheless, in spite of the above failures, we consider Patent Owner's weak evidence of nonobviousness in our weighing of the *Graham* factors below.

5. Weighing the Graham Factors

"Once all relevant facts are found, the ultimate legal determination [of obviousness] involves the weighing of the fact findings to conclude whether the claimed combination would have been obvious to an ordinary artisan."

Arctic Cat, 876 F.3d at 1361. On balance, considering the complete record before us and for the reasons explained above, the evidence of obviousness is very strong and the evidence of nonobviousness, which includes Patent Owner's objective evidence of nonobviousness, is very weak. As a result of that balancing we determine that Petitioner has established by a preponderance of the evidence that the combination of Tayloe and TI Datasheet would have rendered the subject matter of claim 3 obvious to one of ordinary skill in the art at the time of the invention.

C. Obviousness over Tayloe and Kawada

Petitioner also contends the combined teachings of Tayloe and Kawada would have rendered the subject matter of claim 3 of the '444 patent obvious to one of ordinary skill in the art at the time of the invention. Pet. 43–47 (discussing motivation to combine), 78–81 (discussing the application of the art to claim 3). Because Petitioner's challenge based on the combination of Tayloe and TI Datasheet is dispositive as to claim 3, we need not reach this additional asserted ground. *See SAS Inst. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding that a petitioner "is entitled to a final written decision addressing all of the claims it has challenged"); *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App'x 984, 990 (Fed. Cir. 2020) (nonprecedential) (stating that the "Board need not address issues that are not necessary to the resolution of the proceeding," such as "alternative arguments with respect to claims [the Board] found unpatentable on other grounds"); *cf. In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009) (not reaching other grounds of unpatentability after affirming a ground based on anticipation); *see also Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (An administrative agency is at liberty to reach

a decision based on a dispositive issue because doing so "can not only save the parties, the [agency], and [the reviewing] court unnecessary cost and effort," but "can greatly ease the burden on [an agency] commonly faced with a . . . proceeding involving numerous complex issues and required by statute to reach its conclusion within rigid time limits."); *SK Hynix Inc. v. Netlist, Inc.*, IPR2017-00692, Paper 25 at 40 (PTAB July 5, 2018) (determining all challenged claims to be unpatentable and not addressing additional grounds).

D. Petitioner's Identification of Arguments Improperly Raised in a Sur-Reply

As noted above, we held a conference call to discuss Petitioner's request to file a motion to strike Exhibit 2022 as well as portions of Patent Owner's Sur-reply. *See* Order. As set forth in our Order, we authorized (1) Petitioner to address the propriety of Patent Owner filing Exhibit 2022 with its Sur-reply and (2) in lieu of a motion to strike, Petitioner to file a chart including the page and line numbers for each portion of Patent Owner's Sur-reply that Petitioner contends exceeds the proper scope for a sur-reply and for Patent Owner to file a corresponding chart in response. *See id.* at 2–5. Thereafter, Petitioner filed Petitioner's Identification (Paper 32) and Patent Owner filed Patent Owner's Response to Identification (Paper 35).[22]

At Petitioner's request, we held a pre-hearing conference to discuss, *inter alia*, Petitioner's Identification and Patent Owner's Response to Identification. In particular, Petitioner explained that Patent Owner did not assert, in the Patent Owner Response, that Tayloe's capacitors did not store a

[22] Petitioner also filed a Motion to Exclude Exhibit 2022. *See infra* § III.E.

non-negligible amount of energy; rather, Patent Owner's arguments as to whether Tayloe discloses a "storage element" were directed to other aspects of Patent Owner's proposed construction of "storage element," including whether Tayloe discloses an "energy transfer system" and a low impedance load. In contrast, Petitioner asserted that Patent Owner's arguments—that "'non-negligible' is *relative to* the available power (i.e., amount of energy available from the input EM signal)" (PO Sur-reply 15), and which segues to most of the portions of the Sur-reply identified in Petitioner's Identification—were not raised in Patent Owner's Response and are raised, improperly, for the first time in the Sur-reply.

Patent Owner responded by arguing, *inter alia*, that its Sur-reply arguments were properly raised to respond to Petitioner's arguments, first raised in the Reply, in which Petitioner argued that Tayloe's capacitors stored a non-negligible amount of energy. Additionally, Patent Owner asserted that it had previously raised the argument—that "non-negligible" is relative to available power—in its Patent Owner Response. *See, e.g.*, Paper 35, 3 (citing "Paper 18 (Response) at . . . 47:40–48:2 . . . .").[23]

The moving party "has the burden of proof to establish that it is entitled to the requested relief." 37 C.F.R. § 42.20(c). "A sur-reply may only respond to arguments raised in the corresponding reply and may not be accompanied by new evidence other than deposition transcripts of the cross-examination of any reply witness." 37 C.F.R. § 42.23(b); *see* Consolidated TPG at 74 ("*'Respond,' in the context of 37 C.F.R. § 42.23(b), does not mean proceed in a new direction with a new approach as compared to the*

[23] We reviewed each citation provided by Patent Owner, but particularly call out 47:40–48:2 for reasons discussed below.

positions taken in a prior filing." (emphasis added)). The portions of Patent Owner's Sur-reply identified in Petitioner's Identification proceed in a new direction with a new approach as compared to the positions taken in Patent Owner's Response, and, therefore, are impermissible for a sur-reply.

First, we agree with Petitioner that Patent Owner did not assert, in its Patent Owner Response, that Tayloe's capacitors did not teach a "storage element" because they did not store a non-negligible amount of energy. In no instance is that assertion raised in Patent Owner's Response. *See generally* PO Resp. None of Patent Owner's citations in its Response to Petitioner's Identification reflect any argument even remotely raising this issue.

Second and relatedly, it also is clear that Patent Owner did not assert in its Patent Owner Response that to determine whether an element stores "non-negligible" amounts of energy, the available power must be determined and compared. *See* PO Sur-reply 15. Patent Owner's Response to Petitioner's Identification cites, *inter alia*, to page 48, line 2, of the Patent Owner Response. Paper 35, 3. During the pre-hearing conference, Patent Owner emphasized this citation as evidencing that Patent Owner had previously asserted this argument in its Patent Owner Response. In the Patent Owner Response, this citation follows a block quote of the paragraph of the '551 patent that is the centerpiece of the claim construction arguments regarding the meaning of "storage element" (and is reproduced in our claim construction discussion above). *See* PO Resp. 47–48. Patent Owner quotes the paragraph in the context of its arguments distinguishing energy transfer systems and sample-and-hold systems. *See id.* The citation following the block quote reads as follows: "Ex. 2007 at 66:56-67; *see also id.* at 54:20-

59:19 (discussing sample and hold systems); 66:35-68:15, 97:39-101:32 (discussing energy transfer systems)." PO Resp. 48. Patent Owner identified the most relevant portion of this citation as column 68, lines 1 through 15. Nothing from this portion (or any other portion) of the Patent Owner Response expressly or impliedly states the argument raised in the Sur-reply. Additionally, even if the citation *could have* supported the argument raised in Patent Owner's Sur-reply, that argument would have had to be raised in Patent Owner's Response, which it was not.[24] The citations on line 2 of page 48 of Patent Owner's Response, which span six columns of text of the '551 patent, fail to sufficiently raise the specific argument asserted in the Sur-reply.

Third, the discussion that follows this critical segue in Patent Owner's Sur-reply continues this line of argument and includes pages of arguments and calculations not asserted previously in the Patent Owner Response, and clearly proceeds in a new direction with a new approach as compared to the positions actually asserted in the Patent Owner Response. Our discussion of Exhibit 2022 (in the context of Petitioner's Motion to Exclude, below) is similarly reflective of this new argument as that exhibit, which constitutes new evidence, was filed with Patent Owner's Sur-reply in violation of 37 C.F.R. § 42.23(b).

Fourth, one of the reasons that a sur-reply may not raise arguments that proceed in a new direction with a new approach is because Petitioner does not have an opportunity to respond thereto. Patent Owner asserts that it

[24] We need not and do not decide whether the citation supports Patent Owner's Sur-reply argument because the argument was raised, improperly, in the Sur-reply in the first instance.

was merely responding to Petitioner's Reply. But, it was Patent Owner's Response that first asserted the meaning of "storage element" that included the phrase "non-negligible amount of energy," and Patent Owner *could have* asserted that Tayloe was distinguishable on this basis, *but did not do so*.

Additionally, if Patent Owner believed Petitioner's Reply raised an issue that was inappropriate for a reply brief or that Patent Owner needed a greater opportunity to respond beyond that provided by our Rules (e.g., to include new argument and evidence in its Sur-reply), it was incumbent upon Patent Owner to contact us and request authorization for an exception to the Rules. *Patent Owner did not do so*. Patent Owner did not request that its Sur-reply be permitted to include arguments and evidence that would otherwise be impermissible in a sur-reply.

As noted above, the parties' arguments and our ruling thereon were made during the pre-hearing conference and our ruling was reiterated at the start of the oral hearing. Here, we include the positions expressed by the parties and our basis for finding that Petitioner satisfied its burden to show that it is entitled to the relief requested so that the record is complete. For each of these reasons,[25] we granted Petitioner's request to exclude the portions of Patent Owner's Sur-reply identified in Petitioner's Identification

[25] We also find that Patent Owner waived these arguments by not raising them in the Patent Owner Response. *See* Paper 11 (Scheduling Order), 8 ("Patent Owner is cautioned that any arguments not raised in the response may be deemed waived."); *see also In re NuVasive, Inc.*, 842 F.3d 1376, 1381 (Fed. Cir. 2016) (determining that an argument not raised in a patent owner response was waived).

and we do not consider those portions of the Sur-reply in reaching this Final Written Decision.[26]

E. Petitioner's Motion to Exclude

Following a timely objection (*see* Paper 27), Petitioner moves to exclude Exhibit 2022 pursuant to 37 C.F.R. § 42.64(c) because the exhibit (1) is "untimely and improper pursuant to 37 C.F.R. § 42.23(b)" and the Consolidated TPG and (2) is unfairly prejudicial under Federal Rule of Evidence 403. Mot. Exc. 1.

First, Petitioner contends the exhibit is untimely and procedurally improper because it was first introduced and filed with Patent Owner's Sur-reply, in violation of our Rules. Mot. Exc. 2 (citing 37 C.F.R. § 42.23(b); Consolidated TPG at 73). Petitioner asserts that Exhibit 2022 raises "complicated calculations . . . at a point when Petitioner cannot fully respond—after the time when Petitioner could respond with expert testimony or a written response. Forcing Petitioner to address these calculations during an oral hearing without the benefit of briefing or expert testimony will significantly prejudice Petitioner." *Id.* at 2–3.

Second, Petitioner contends that Exhibit 2022 should be excluded under Federal Rule of Evidence 403 because it is an attorney-prepared document, contains unsupported assumptions and calculation errors, is not supported by expert testimony, lacks the necessary factual foundation to

[26] Patent Owner's Demonstrative Exhibits (Ex. 2029) include discussion of the arguments we exclude from the Sur-reply. Even though demonstrative exhibits are not evidence, we have not considered the excluded arguments referenced therein.

make it relevant, and thus "any purported relevance . . . is substantially outweighed by the unfair prejudice and confusion it creates." Mot. Exc. 3.

In its Opposition, Patent Owner asserts that "Exhibit 2022 is timely, compliant with PTAB procedure, and poses no undue prejudice." Opp. 2. First, regarding timeliness, Patent Owner asserts that it introduced Exhibit 2022 "[t]o address Dr. Subramanian's (and [Petitioner's]) additional theories" through the cross-examination of Dr. Subramanian and the use of the exhibit, which Patent Owner contends includes "well-known calculations and mathematical equations." *Id.* at 5. Thus, Patent Owner argues that "Exhibit 2022 was not belatedly introduced, but is simply used as deposition testimony submitted in rebuttal of issues raised by [Petitioner/Petitioner's] expert in its Reply." *Id.* at 6.

Second, Patent Owner contends that Petitioner is not prejudiced by the inclusion of Exhibit 2022. Opp. 6. Patent Owner asserts that Petitioner's "prejudice argument rests on the false notion that [Patent Owner's] Exhibit 2022 is improper." *Id.* Patent Owner argues that in any given case, "one party submits the final brief" and the other party is not prejudiced just because that party is not the one that gets the final word. *Id.* Additionally, Patent Owner asserts that Dr. Subramanian first addressed the application of the construction of "storage element" to Tayloe in his Reply Declaration, and, therefore, Patent Owner was "entitled to impeach Dr. Subramanian's analysis" during his deposition. *Id.* at 6–7. Further, Patent Owner asserts that the filing of Exhibit 2022 does not violate 37 C.F.R. § 42.23(b) because the exhibit is cited "in conjunction with Dr. Subramanian's deposition testimony, which [Patent Owner] elicited in accordance with [the] Trial Practice Guide." *Id.* at 8; *see id.* at 8–9 (also asserting that Patent Owner

argued that Tayloe's capacitors do not store non-negligible amounts of energy in the Patent Owner Response).

Third, Patent Owner asserts that Exhibit 2022 should not be excluded pursuant to Federal Rule of Evidence 403 because the probative value clearly outweighs any risk of unfair prejudice. Opp. 10. To the contrary, Patent Owner contends that "excluding Exhibit 2022 prejudices [Patent Owner] and unfairly deprives it of proper rebuttal evidence." *Id.*

In its Reply in Support of Its Motion to Exclude, Petitioner responds to Patent Owner's arguments, contending (1) that "Exhibit 2022 is improper 'new evidence' that would take the trial 'in a new direction with a new approach'" because Patent Owner did not assert the positions for which it relies on Exhibit 2022 in its Patent Owner Response (Mot. Reply 1–4); (2) Patent Owner could have, but did not, question Dr. Subramanian about the calculations set forth in his Reply Declaration (*id.* at 4–5); and (3) that Exhibit 2022 contains multiple errors and unsupported assumptions that support Petitioner's argument of exclusion because of unfair prejudice pursuant to Federal Rule of Evidence 403 (*id.* at 5).

Petitioner, as the "moving party," "has the burden of proof to establish that it is entitled to the requested relief." 37 C.F.R. § 42.20. As set forth above, 37 C.F.R. § 42.23(b) specifies, in relevant part, that "[a] sur-reply may only respond to arguments raised in the corresponding reply and *may not be accompanied by new evidence* other than deposition transcripts of the cross-examination of any reply witness." 37 C.F.R. § 42.23(b) (emphasis added). The Consolidated TPG repeats the above-quoted language of the rule and also explains that

> [s]ur-replies should only respond to arguments made in reply briefs, comment on reply declaration testimony, or point to cross-examination testimony. As noted above, a sur-reply may address the institution decision if necessary to respond to the petitioner's reply. This sur-reply practice essentially replaces the previous practice of filing observations on cross-examination testimony.

Consolidated TPG at 73–74. Accordingly, Rule 42.23(b) provides a blanket prohibition on a patentee filing new exhibits (other than deposition transcripts of the cross-examination of any reply witness) with a sur-reply, as Patent Owner has done here.

Additionally, Exhibit 2022 is used by Patent Owner to raise new arguments in the Sur-reply that we exclude above. As our discussion above reflects, the new arguments based on this exhibit are improper under our Rules. Petitioner would undoubtedly be prejudiced by the admission of Exhibit 2022 for precisely the reasons explained by Petitioner (and reiterated above). In particular, the Rules prohibit new evidence (other than deposition transcripts of the cross-examination of any reply witness) with a sur-reply for this exact reason—because Petitioner lacks an opportunity to respond to new evidence submitted with a sur-reply.[27]

Patent Owner's complaints that it would be prejudiced by the exclusion of the exhibit are (1) unfounded because Patent Owner had the opportunity to cross-examine Dr. Subramanian as to the opinions set forth in his Reply Declaration and (2) only the result of Patent Owner's own actions or inaction. Specifically, at no point (even belatedly) did Patent Owner seek

[27] Contrary to Patent Owner's argument, this is not a question of who gets the last word; rather, this is a question of whether a party can submit *new evidence* with its last word, which Rule 42.23(b) specifically prohibits.

authorization to file new evidence (such as Exhibit 2022) with its Sur-reply. Had Patent Owner requested to do so in a timely manner, we could have considered Patent Owner's arguments of potential prejudice and determined whether Patent Owner should have been permitted to file the exhibit along with providing an opportunity for Petitioner to respond. But, Patent Owner *did not so request* and, thus, we do not agree with Patent Owner's assertions of unfair prejudice.

Further, even though not expressly argued by Patent Owner, we similarly do not find it in the interests of justice to maintain this exhibit in the case file. Even though Exhibit 2022 was used during Dr. Subramanian's deposition, each of Patent Owner's arguments thereon is excluded as improper sur-reply argument. Thus, there is no basis upon which inclusion of the exhibit is warranted.

Accordingly, we grant Petitioner's Motion to Exclude pursuant to 37 C.F.R. § 42.23(b).[28,29]

F. Petitioner's Motion to Seal

Petitioner filed an unopposed Motion to Seal Exhibit 1029, the deposition transcript of Dr. Steer. Mot. Seal. Petitioner explains that it "seeks to seal Dr. Steer's deposition transcript because, during the deposition, Patent Owner . . . designated the [t]ranscript as 'confidential' under the terms of the PTAB's default Protective Order." *Id.* at 1. Petitioner

[28] In light of our determination, we need not also decide whether Federal Rule of Evidence 403 provides an independent basis for exclusion.
[29] Patent Owner's Demonstrative Exhibits (Ex. 2029) include discussion of excluded Exhibit 2022. Even though demonstrative exhibits are not evidence, we have not considered the portions of the demonstratives referencing that exhibit.

explains that Patent Owner sought to seal the deposition transcript because of Dr. Steer's "testimony revealing alleged confidential information about his work for [Patent Owner]." *Id.* Petitioner also states that Patent Owner asserts good cause exists to seal the deposition transcript, although Petitioner expressly "takes no position as to the propriety of this designation . . . and reserves the right to challenge such designation." *Id.*

Petitioner's Motion to Seal was discussed during the pre-hearing conference. Without elaborating on the details of the discussion, we indicated that, as presented, the Motion is insufficient to justify sealing the entirety of the deposition transcript. Additionally, we explained that we intended to deny the Motion, but we provided Patent Owner an opportunity to file a new motion to seal with a protective order (which was not filed with Petitioner's Motion to Seal) if Patent Owner maintained its desire to seal a portion of the deposition transcript.[30] On November 18, 2021, Patent Owner emailed the Board to report that Patent Owner "does not intend to designate any portions of Dr. Michael Steer's deposition transcript as confidential, and therefore will not file" a new motion to seal. Ex. 3002 (Email from S. Mandir, dated Nov. 18, 2021). Patent Owner indicates, "[a]ccordingly, . . . Dr. Steer's deposition transcript (filed as Exhibit 1029 in IPR2020-01265 . . .) can be unsealed." *Id.*

In light of our discussion at the pre-hearing conference and Patent Owner's representation that it no longer intends to designate any portion of Dr. Steer's deposition transcript as confidential, we deny Petitioner's Motion to Seal and unseal Exhibit 1029.

---

[30] There was no basis provided to seal the entirety of the deposition transcript.

IV. SUMMARY[31]

For the reasons discussed above, Petitioner has demonstrated, by a preponderance of the evidence, that claim 3 of the '444 patent is unpatentable. Additionally, we exclude from consideration the portions of Patent Owner's Sur-reply identified in Petitioner's Identification (Paper 32), we grant Petitioner's Motion to Exclude (Paper 34) and exclude Exhibit 2022, and we deny Petitioner's Motion to Seal (Paper 22) and unseal Exhibit 1029.

Our conclusions regarding claim 3 are summarized below:

Claims Challenged	35 U.S.C. §	Reference(s) /Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
3	103(a)	Tayloe, TI Datasheet	3	
3	103(a)[32]	Tayloe, Kawada		
Overall Outcome			3	

[31] Should Patent Owner wish to pursue amendment of claim 3 in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[32] As explained above, because Petitioner's challenge based on the combination of Tayloe and TI Datasheet is dispositive as to claim 3, we do not reach this asserted ground. *See supra* § III.C.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claim 3 of U.S. Patent No. 7,110,444 B1 is determined to be unpatentable;

FURTHER ORDERED that the portions of Patent Owner's Sur-reply (Paper 26) identified in Petitioner's Identification (Paper 32) are excluded;

FURTHER ORDERED that Petitioner's Motion to Exclude (Paper 34) is *granted* and Exhibit 2022 is excluded;

FURTHER ORDERED that Petitioner's Motion to Seal (Paper 22) is *denied* and Exhibit 1029 is unsealed; and

FURTHER ORDERED that, because this a Final Written Decision, parties to this proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-01265
Patent 7,110,444 B1

For PETITIONER:

Grant K. Rowan
Haixia Lin
Brian Lambson
Michael J. Summersgill
Todd C. Zubler
WILMER CUTLER PICKERING HALE AND DORR LLP
grant.rowan@wilmerhale.com
haixia.lin@wilmerhale.com
brian.lambson@wilmerhale.com
Michael.summersgill@wilmerhale.com
todd.zubler@wilmerhale.com
WH-ParkerVision-IPRs@wilmerhale.com

For PATENT OWNER:

Jason S. Charkow
Chandran B. Iyer
Stephanie R. Mandir
Richard Juang
Kevin H. Sprenger
DAIGNAULT IYER LLP
jcharkow@daignaultiyer.com
cbiyer@daignaultiyer.com
smandir@daignaultiyer.com
rjuang@daignaultiyer.com
ksprenger@daignaultiyer.com

US007110444B1

(12) **United States Patent**
Sorrells et al.

(10) **Patent No.: US 7,110,444 B1**
(45) **Date of Patent: Sep. 19, 2006**

(54) **WIRELESS LOCAL AREA NETWORK (WLAN) USING UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY INCLUDING MULTI-PHASE EMBODIMENTS AND CIRCUIT IMPLEMENTATIONS**

(75) Inventors: **David F. Sorrells**, Middleburg, FL (US); **Michael J. Bultman**, Jacksonville, FL (US); **Robert W. Cook**, Switzerland, FL (US); **Richard C. Looke**, Jacksonville, FL (US); **Charley D. Moses, Jr.**, Jacksonville, FL (US); **Gregory S. Rawlins**, Lake Mary, FL (US); **Michael W. Rawlins**, Lake Mary, FL (US)

(73) Assignee: **ParkerVision, Inc.**, Jacksonville, FL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1111 days.

(21) Appl. No.: **09/632,856**

(22) Filed: **Aug. 4, 2000**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/525,615, filed on Mar. 14, 2000, and a continuation-in-part of application No. 09/526,041, filed on Mar. 14, 2000.
(60) Provisional application No. 60/147,129, filed on Aug. 4, 1999.

(51) **Int. Cl.**
H04L 5/16 (2006.01)

(52) **U.S. Cl.** **375/222**; 375/328; 455/137

(58) **Field of Classification Search** 375/222, 375/328, 324, 349; 455/131, 137, 150.1, 455/189.1, 190.1, 313, 323, 326
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2,057,613 A 10/1936 Gardner 250/8
2,241,078 A 5/1941 Vreeland 179/15

(Continued)

FOREIGN PATENT DOCUMENTS

DE 35 41 031 A1 5/1986
DE 42 37 692 C1 3/1994

(Continued)

OTHER PUBLICATIONS

English Translation of German Patent Publication No. DE 196 48 915 A1, 10 pp.

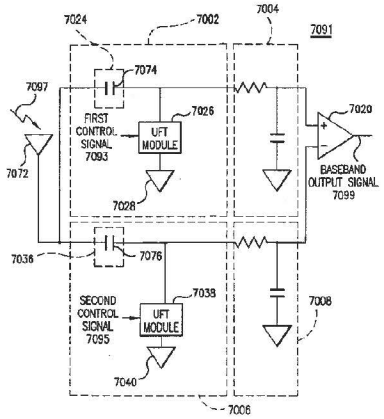
(Continued)

Primary Examiner Chieh M. Fan
Assistant Examiner—Kevin Kim
(74) *Attorney, Agent, or Firm*—Sterne, Kessler, Goldstein & Fox P.L.L.C.

(57) **ABSTRACT**

Frequency translation and applications of the same are described herein, including RF modem and wireless local area network (WLAN) applications. In embodiments, the WLAN invention includes an antenna, an LNA/PA module, a receiver, a transmitter, a control signal generator, a demodulation/modulation facilitation module, and a MAC interface. The WLAN receiver includes at least one universal frequency translation module that frequency down-converts a received EM signal. In embodiments, the UFT based receiver is configured in a multi-phase embodiment to reduce or eliminate re-radiation that is caused by DC offset. The WLAN transmitter includes at least one universal frequency translation module that frequency up-converts a baseband signal in preparation for transmission over the wireless LAN. In embodiments, the UFT based transmitter is configured in a differential and multi-phase embodiment to reduce carrier insertion and spectral growth.

32 Claims, 349 Drawing Sheets



INTEL 1001

U.S. PATENT DOCUMENTS

2,270,385	A	1/1942	Skillman	179/15
2,283,575	A	5/1942	Roberts	250/6
2,358,152	A	9/1944	Earp	179/171.5
2,410,350	A	10/1946	Labin et al.	179/15
2,451,430	A	10/1948	Barone	250/8
2,462,069	A	2/1949	Chatterjea et al.	250/17
2,462,181	A	2/1949	Grosslfinger	250/17
2,472,798	A	6/1949	Fredenall	178/44
2,497,859	A	2/1950	Boughtwood et al.	250/8
2,499,279	A	2/1950	Peterson	332/41
2,802,208	A	8/1957	Hobbs	343/176
2,985,875	A	5/1961	Grisdale et al.	343/100
3,023,309	A	2/1962	Foulkes	250/17
3,069,679	A	12/1962	Sweeney et al.	343/200
3,104,393	A	9/1963	Vogelman	343/200
3,114,106	A	12/1963	Mcmaus	325/56
3,118,117	A	1/1964	King et al.	332/22
3,226,643	A	12/1965	McNair	325/40
3,246,084	A	4/1966	Kryter	
3,258,694	A	6/1966	Shepard	325/145
3,383,598	A	5/1968	Sanders	325/163
3,384,822	A	5/1968	Miyagi	325/30
3,454,718	A	7/1969	Perreault	178/66
3,523,291	A	8/1970	Pierret	340/347
3,548,342	A	12/1970	Maxey	332/9
3,555,428	A	1/1971	Perreault	325/320
3,614,627	A	10/1971	Runyan et al.	
3,617,892	A	11/1971	Hawley et al.	325/145
3,621,402	A	11/1971	Gardner	328/37
3,622,885	A	11/1971	Oberdorf et al.	325/40
3,623,160	A	11/1971	Giles et al.	340/347 DA
3,626,417	A	12/1971	Gilbert	343/203
3,629,696	A	12/1971	Bartelink	324/57 R
3,662,268	A	5/1972	Gans et al.	325/56
3,689,841	A	9/1972	Bello et al.	325/39
3,702,440	A	11/1972	Moore	
3,714,577	A	1/1973	Hayes	325/145
3,716,730	A	2/1973	Cemy, Jr.	307/295
3,717,844	A	2/1973	Barret et al.	340/5 R
3,735,048	A	5/1973	Tomsa et al.	179/15 BM
3,736,513	A	5/1973	Wilson	
3,767,984	A	10/1973	Shinoda et al.	
3,806,811	A	4/1974	Thompson	325/146
3,852,530	A	12/1974	Shen	
3,868,601	A	2/1975	MacAfee	332/45
3,940,697	A	2/1976	Morgan	
3,949,300	A	4/1976	Sadler	325/31
3,967,202	A	6/1976	Batz	325/31
3,980,945	A	9/1976	Bickford et al.	325/30
3,987,280	A	10/1976	Bauer	235/150.53
3,991,277	A	11/1976	Hirata	179/15 FD
4,003,002	A	1/1977	Snijders et al.	332/10
4,013,966	A	3/1977	Campbell	325/363
4,016,366	A	4/1977	Kurata	
4,017,798	A	4/1977	Gordy et al.	325/42
4,019,140	A	4/1977	Swerdlow	322/65
4,032,847	A	6/1977	Unkauf	325/323
4,035,732	A	7/1977	Lohrmann	325/446
4,045,740	A	8/1977	Baker	
4,047,121	A	9/1977	Campbell	331/76
4,051,475	A	9/1977	Campbell	343/180
4,066,841	A	1/1978	Young	178/66 R
4,066,919	A	1/1978	Huntington	307/353
4,080,573	A	3/1978	Howell	325/439
4,081,748	A	3/1978	Batz	325/56
4,115,737	A	9/1978	Hongu et al.	
4,130,765	A	12/1978	Arakelian et al.	307/220 R
4,130,806	A	12/1978	Van Gerwen et al.	325/487
4,132,952	A	1/1979	Hongu et al.	
4,142,155	A	2/1979	Adachi	325/47
4,170,764	A	10/1979	Salz et al.	332/17
4,204,171	A	5/1980	Sutphin, Jr.	328/167
4,210,872	A	7/1980	Gregorian	330/9
4,220,977	A	9/1980	Yamanaka	
4,245,355	A	1/1981	Pascoe et al.	455/326
4,250,458	A	2/1981	Richmond et al.	
4,253,066	A	2/1981	Fisher et al.	329/50
4,253,067	A	2/1981	Caples et al.	329/110
4,253,069	A	2/1981	Nossek	330/107
4,308,614	A	12/1981	Fisher et al.	370/119
4,320,361	A	3/1982	Kikkert	332/16 R
4,320,536	A	3/1982	Dietrich	455/325
4,334,324	A	6/1982	Hoover	455/333
4,346,477	A	8/1982	Gordy	455/257
4,355,401	A	10/1982	Ikoma et al.	375/5
4,356,558	A	10/1982	Owen et al.	364/724
4,360,867	A	11/1982	Gonda	363/158
4,363,132	A	12/1982	Collin	455/52
4,365,217	A	12/1982	Berger et al.	333/165
4,369,522	A	1/1983	Cerny, Jr. et al.	455/333
4,370,572	A	1/1983	Cosand et al.	307/353
4,384,357	A	5/1983	deBuda et al.	
4,389,579	A	6/1983	Stein	307/353
4,392,255	A	7/1983	Del Giudice	455/328
4,393,395	A	7/1983	Hacke et al.	358/23
4,430,629	A	2/1984	Betzl et al.	333/165
4,441,080	A	4/1984	Saari	
4,446,438	A	5/1984	Chang et al.	328/127
4,456,990	A	6/1984	Fisher et al.	370/119
4,470,145	A	9/1984	Williams	
4,472,785	A	9/1984	Kasuga	364/718
4,479,226	A	10/1984	Prabhu et al.	375/1
4,481,490	A	11/1984	Huntley	332/41
4,481,642	A	11/1984	Hanson	375/9
4,483,017	A	11/1984	Hampel et al.	382/17
4,484,143	A	11/1984	French et al.	329/50
4,485,488	A	11/1984	Houdart	455/327
4,488,119	A	12/1984	Marshall	
4,504,803	A	3/1985	Lee et al.	332/31 R
4,510,467	A	4/1985	Chang et al.	
4,517,519	A	5/1985	Mukaiyama	329/126
4,517,520	A	5/1985	Ogawa	329/145
4,518,935	A	5/1985	van Roermund	333/173
4,521,892	A	6/1985	Vance et al.	375/88
4,563,773	A	1/1986	Dixon, Jr. et al.	455/327
4,577,157	A	3/1986	Reed	329/50
4,583,239	A	4/1986	Vance	375/94
4,591,736	A	5/1986	Hirao et al.	307/267
4,602,220	A	7/1986	Kurihara	331/19
4,603,300	A	7/1986	Welles, II et al.	329/50
4,612,464	A	9/1986	Ishikawa et al.	307/496
4,612,518	A	9/1986	Gans et al.	332/21
4,616,191	A	10/1986	Galani et al.	331/4
4,621,217	A	11/1986	Saxe et al.	315/1
4,628,517	A	12/1986	Schwarz et al.	375/40
4,633,510	A	12/1986	Suzuki et al.	
4,634,998	A	1/1987	Crawford	331/1 A
4,648,021	A	3/1987	Alberkrack	363/157
4,651,034	A	3/1987	Sato	307/556
4,653,117	A	3/1987	Heck	455/209
4,660,164	A	4/1987	Leibowitz	
4,675,882	A	6/1987	Lillie et al.	375/80
4,688,253	A	8/1987	Gumm	381/7
4,716,376	A	12/1987	Daudelin	329/107
4,716,388	A	12/1987	Jacobs	333/173
4,718,113	A	1/1988	Rother et al.	455/209
4,726,041	A	2/1988	Prohaska et al.	375/91
4,733,403	A	3/1988	Simone	375/103
4,734,591	A	3/1988	Ichitsubo	307/219.1
4,737,969	A	4/1988	Steel et al.	375/67
4,740,675	A	4/1988	Brosnan et al.	

4,743,858	A		5/1988	Everard 330/10
4,745,463	A		5/1988	Lu 358/23
4,751,468	A		6/1988	Agoston 328/133
4,757,538	A		7/1988	Zink 381/7
4,761,798	A		8/1988	Griswold, Jr. et al.
4,768,187	A		8/1988	Marshall 370/69.1
4,769,612	A		9/1988	Tamakoshi et al. 328/167
4,772,853	A		9/1988	Hart
4,785,463	A		11/1988	Janc et al. 375/1
4,791,584	A		12/1988	Greivenkamp, Jr. 364/525
4,801,823	A		1/1989	Yokoyama 307/353
4,806,790	A		2/1989	Sone 307/353
4,810,904	A		3/1989	Crawford 307/353
4,810,976	A		3/1989	Cowley et al. ..... 331/117 R
4,811,362	A		3/1989	Yester, Jr. et al. 375/75
4,816,704	A		3/1989	Fiori, Jr. 307/519
4,819,252	A		4/1989	Christopher 375/122
4,833,445	A		5/1989	Buchele 341/118
4,841,265	A		6/1989	Watanabe et al. 333/194
4,855,894	A		8/1989	Asahi et al. 363/157
4,857,928	A		8/1989	Gailus et al.
4,862,121	A		8/1989	Hochschild et al. 333/173
4,868,654	A		9/1989	Juri et al. 358/133
4,873,492	A		10/1989	Myer
4,943,974	A		7/1990	Motamedi 375/1
4,972,436	A		11/1990	Halim et al.
5,012,245	A		4/1991	Scott et al.
5,016,242	A		5/1991	Tang
5,058,107	A		10/1991	Stone et al.
5,083,050	A		1/1992	Vasile 307/529
5,091,921	A		2/1992	Minami 375/88
5,095,533	A		3/1992	Loper et al. 455/245
5,095,536	A		3/1992	Loper 455/324
5,111,152	A		5/1992	Makino 329/300
5,113,094	A		5/1992	Horiguchi et al. 307/529
5,113,129	A		5/1992	Hughes 323/316
5,115,409	A		5/1992	Stepp 364/841
5,122,765	A		6/1992	Pataut 332/105
5,124,592	A		6/1992	Hagino 307/520
5,126,682	A		6/1992	Weinberg et al. 329/304
5,136,267	A		8/1992	Cabot 333/174
5,140,705	A		8/1992	Kosuga 455/318
5,150,124	A		9/1992	Moore et al. 342/68
5,151,661	A		9/1992	Caldwell et al. 328/14
5,157,687	A		10/1992	Tymes 375/1
5,159,710	A		10/1992	Cusdin 455/304
5,170,414	A		12/1992	Silvian 375/59
5,172,070	A		12/1992	Hiraiwa et al. 329/304
5,179,731	A	*	1/1993	Trankle et al.
5,191,459	A		3/1993	Thompson et al. 359/133
5,204,642	A		4/1993	Asghar et al. 331/135
5,212,827	A		5/1993	Meszko et al. 455/219
5,214,787	A		5/1993	Karkota, Jr. 455/3.2
5,218,562	A		6/1993	Basehore et al.
5,220,583	A		6/1993	Solomon 375/82
5,220,680	A		6/1993	Lee 455/102
5,222,144	A		6/1993	Whikehart 381/15
5,230,097	A		7/1993	Currie et al. 455/226.1
5,239,496	A		8/1993	Vancraeynest
5,239,686	A		8/1993	Downey 455/78
5,241,561	A		8/1993	Barnard 375/1
5,249,203	A		9/1993	Loper 375/97
5,251,218	A		10/1993	Fujisawa et al. 370/120
5,251,232	A		10/1993	Nonami 375/5
5,260,970	A		11/1993	Henry et al. 375/10
5,260,973	A		11/1993	Watanabe
5,263,194	A		11/1993	Ragan 455/316
5,263,196	A		11/1993	Jasper 455/324
5,267,023	A		11/1993	Kawasaki 358/23
5,278,826	A		1/1994	Murphy et al. 370/76
5,282,023	A		1/1994	Scarpa 358/36
5,282,222	A		1/1994	Fattouche et al.
5,287,516	A		2/1994	Schaub 375/88
5,293,398	A		3/1994	Hamao et al. 375/1
5,303,417	A		4/1994	Laws 455/314
5,307,517	A		4/1994	Rich 455/306
5,315,583	A		5/1994	Murphy et al. 370/18
5,319,799	A		6/1994	Morita 455/78
5,321,852	A		6/1994	Seong 455/182.1
5,325,204	A		6/1994	Scarpa 348/607
5,337,014	A		8/1994	Regunathan et al. 324/613
5,339,054	A		8/1994	Taguchi 332/100
5,339,459	A		8/1994	Schiltz et al. 455/333
5,345,239	A		9/1994	Madni et al.
5,353,306	A		10/1994	Yamamoto 375/14
5,355,114	A		10/1994	Sutterlin et al. ..... 340/310 A
5,361,408	A		11/1994	Watanabe et al. 455/324
5,369,404	A		11/1994	Galton 341/143
5,369,789	A		11/1994	Kosugi et al.
5,369,800	A		11/1994	Takagi et al. 455/59
5,375,146	A		12/1994	Chalmers 375/103
5,379,040	A		1/1995	Mizomoto et al. 341/143
5,379,141	A		1/1995	Thompson et al. 359/125
5,388,063	A		2/1995	Takatori et al. 364/724.17
5,389,839	A		2/1995	Heck
5,390,364	A		2/1995	Webster et al. 455/52.3
5,400,084	A		3/1995	Scarpa 348/624
5,404,127	A		4/1995	Lee et al. 340/310.02
5,410,541	A		4/1995	Hotto 370/76
5,410,743	A		4/1995	Seely et al. 455/326
5,412,352	A		5/1995	Graham 332/103
5,416,449	A		5/1995	Joshi
5,416,803	A		5/1995	Janer 375/324
5,422,909	A		6/1995	Love et al.
5,422,913	A		6/1995	Wilkinson 375/347
5,423,082	A		6/1995	Cygan et al. 375/126
5,428,638	A		6/1995	Cioffi et al. 375/224
5,428,640	A		6/1995	Townley 375/257
5,434,546	A		7/1995	Palmer 332/151
5,438,329	A		8/1995	Gastouniotis et al.
5,438,692	A		8/1995	Mohindra 455/324
5,440,311	A		8/1995	Gallagher et al.
5,444,415	A		8/1995	Dent et al. 329/302
5,444,416	A		8/1995	Ishikawa et al. 329/341
5,444,865	A		8/1995	Heck et al. 455/86
5,446,421	A		8/1995	Kechkaylo 332/100
5,446,422	A		8/1995	Mattila et al. 332/103
5,448,602	A		9/1995	Ohmori et al. 375/347
5,451,899	A		9/1995	Lawton 329/302
5,454,007	A		9/1995	Dutta 375/322
5,454,009	A		9/1995	Fruit et al. 372/202
5,463,356	A		10/1995	Palmer 332/117
5,463,357	A		10/1995	Hobden 332/151
5,465,071	A		11/1995	Kobayashi et al. 329/315
5,465,410	A		11/1995	Hiben et al. 455/266
5,465,415	A		11/1995	Bien 455/326
5,465,418	A		11/1995	Zhou et al. 455/332
5,471,162	A		11/1995	McEwan 327/92
5,471,665	A		11/1995	Pace et al.
5,479,120	A		12/1995	McEwan 327/91
5,479,447	A		12/1995	Chow et al. 375/260
5,481,570	A		1/1996	Winters
5,483,193	A		1/1996	Kennedy et al. 329/300
5,483,549	A		1/1996	Weinberg et al. 375/200
5,483,600	A		1/1996	Werrbach
5,483,691	A		1/1996	Heck et al. 455/234.2
5,483,695	A		1/1996	Pardoen
5,490,173	A		2/1996	Whikehart et al. 375/316
5,490,176	A	*	2/1996	Peltier
5,493,581	A		2/1996	Young et al. 375/350
5,493,721	A		2/1996	Reis 455/339
5,495,200	A		2/1996	Kwan et al. 327/554

5,495,202	A	2/1996	Hsu	327/113
5,495,500	A	2/1996	Jovanovich et al.	375/206
5,499,267	A	3/1996	Ohe et al.	375/206
5,500,758	A	3/1996	Thompson et al.	359/189
5,513,389	A	4/1996	Reeser et al.	455/311
5,515,014	A	5/1996	Troutman	332/178
5,517,688	A	5/1996	Fajen et al.	455/333
5,519,890	A	5/1996	Pinckley	455/307
5,523,719	A	6/1996	Longo et al.	327/557
5,523,726	A	6/1996	Kroeger et al.	332/103
5,523,760	A	6/1996	McEwan	342/89
5,539,770	A	7/1996	Ishigaki	375/206
5,555,453	A	9/1996	Kajimoto et al.	455/266
5,557,641	A	9/1996	Weinberg	375/295
5,557,642	A	9/1996	Williams	375/316
5,563,550	A	10/1996	Toth	329/347
5,564,097	A	10/1996	Swanke	
5,574,755	A	11/1996	Persico	375/295
5,579,341	A	11/1996	Smith et al.	375/267
5,579,347	A	11/1996	Lindquist et al.	375/346
5,584,068	A	12/1996	Mohindra	455/324
5,589,793	A	12/1996	Kassapian	
5,592,131	A	1/1997	Labreche et al.	332/103
5,600,680	A	2/1997	Mishima et al.	
5,602,847	A	2/1997	Pagano et al.	370/484
5,602,868	A	2/1997	Wilson	375/219
5,604,592	A	2/1997	Kotidis et al.	356/357
5,604,732	A	2/1997	Kim et al.	370/342
5,606,731	A	2/1997	Pace et al.	
5,608,531	A	3/1997	Honda et al.	386/1
5,610,946	A	3/1997	Tanaka et al.	375/269
RE35,494	E	4/1997	Nicollini	327/554
5,617,451	A	4/1997	Mimura et al.	375/340
5,619,538	A	4/1997	Sempel et al.	375/328
5,621,455	A	4/1997	Rogers et al.	348/6
5,628,055	A	5/1997	Stein	455/89
5,630,227	A	5/1997	Bella et al.	455/324
5,633,815	A	5/1997	Young	
5,636,140	A	6/1997	Lee et al.	
5,638,396	A	6/1997	Klimek	372/92
5,640,415	A	6/1997	Pandula	375/202
5,640,424	A	6/1997	Banavong et al.	375/319
5,640,428	A	6/1997	Abe et al.	375/334
5,640,698	A	6/1997	Shen et al.	455/323
5,648,985	A	7/1997	Bjerede et al.	375/219
5,650,785	A	7/1997	Rodal	342/357
5,661,424	A	8/1997	Tang	327/105
5,663,878	A	9/1997	Walker	363/159
5,663,986	A	9/1997	Striffler	375/260
5,668,836	A	9/1997	Smith et al.	375/316
5,675,392	A	10/1997	Nayebi et al.	348/584
5,678,220	A	10/1997	Fournier	455/302
5,678,226	A	10/1997	Li et al.	
5,680,078	A	10/1997	Ariie	332/178
5,680,418	A	10/1997	Croft et al.	375/346
5,682,099	A	10/1997	Thompson et al.	
5,689,413	A	11/1997	Jaramillo et al.	363/146
5,694,096	A	12/1997	Ushiroku et al.	333/195
5,697,074	A	12/1997	Makikallio et al.	
5,699,006	A	12/1997	Zele et al.	327/341
5,705,949	A	1/1998	Alelyunas et al.	329/304
5,705,955	A	1/1998	Freeburg et al.	331/14
5,710,992	A	1/1998	Sawada et al.	
5,710,998	A	1/1998	Opas	455/324
5,714,910	A	2/1998	Skoczen et al.	331/3
5,715,281	A	2/1998	Bly, deceased et al.	375/344
5,721,514	A	2/1998	Crockett et al.	331/3
5,724,002	A	3/1998	Hulick	329/361
5,724,653	A	3/1998	Baker et al.	455/296
5,729,577	A	3/1998	Chen	375/334
5,729,829	A	3/1998	Talwar et al.	455/63
5,732,333	A	3/1998	Cox et al.	455/126
5,736,895	A	4/1998	Yu et al.	327/554
5,737,035	A	4/1998	Rotzoll	348/725
5,742,189	A	4/1998	Yoshida et al.	327/113
5,745,846	A	4/1998	Myer et al.	
5,748,683	A	5/1998	Smith et al.	375/347
5,751,154	A	5/1998	Tsugai	
5,757,858	A	5/1998	Black et al.	
5,757,870	A	5/1998	Miya et al.	375/367
RE35,829	E	6/1998	Sanderford, Jr.	375/200
5,760,629	A	6/1998	Urabe et al.	
5,760,632	A	6/1998	Kawakami et al.	
5,760,645	A	6/1998	Comte et al.	329/304
5,764,087	A	6/1998	Clark	327/105
5,767,726	A	6/1998	Wang	327/356
5,768,118	A	6/1998	Faulk et al.	363/72
5,768,323	A	6/1998	Kroeger et al.	375/355
5,770,985	A	6/1998	Ushiroku et al.	333/193
5,771,442	A	6/1998	Wang et al.	455/93
5,777,692	A	7/1998	Ghosh	348/725
5,777,771	A	7/1998	Smith	359/180
5,778,022	A	7/1998	Walley	375/206
5,784,689	A	7/1998	Kobaysahi	
5,786,844	A	7/1998	Rogers et al.	348/6
5,790,587	A	8/1998	Smith et al.	
5,793,801	A	8/1998	Fertner	375/219
5,793,817	A	8/1998	Wilson	
5,793,818	A	8/1998	Claydon et al.	375/326
5,801,654	A	9/1998	Traylor	341/144
5,802,463	A	9/1998	Zuckerman	455/208
5,809,060	A	9/1998	Cafarella et al.	375/206
5,812,546	A	9/1998	Zhou et al.	370/342
5,818,582	A	10/1998	Fernandez et al.	356/318
5,818,869	A	10/1998	Miya et al.	375/206
5,825,254	A	10/1998	Lee	331/25
5,834,979	A	11/1998	Yatsuka	
5,834,985	A	11/1998	Sundeg.ang.rd	332/100
5,841,324	A	11/1998	Williams	331/17
5,841,811	A	11/1998	Song	375/235
5,844,449	A	12/1998	Abeno et al.	332/105
5,859,878	A	1/1999	Phillips et al.	375/316
5,864,754	A	1/1999	Hotto	455/280
5,870,670	A	2/1999	Ripley et al.	
5,872,446	A	2/1999	Cranford, Jr. et al.	323/315
5,881,375	A	3/1999	Bonds	455/118
5,883,548	A	3/1999	Assard et al.	329/306
5,892,380	A	4/1999	Quist	327/172
5,894,239	A	4/1999	Bonaccio et al.	327/176
5,894,496	A	4/1999	Jones	455/126
5,896,304	A	4/1999	Tiemann et al.	
5,896,562	A	4/1999	Heinonen	455/76
5,898,912	A	4/1999	Heck et al.	
5,900,747	A	5/1999	Brauns	327/9
5,901,054	A	5/1999	Leu et al.	363/41
5,901,187	A	5/1999	Iinuma	375/347
5,901,344	A	5/1999	Opas	455/76
5,901,347	A	5/1999	Chambers et al.	455/234.1
5,901,348	A	5/1999	Bang et al.	455/254
5,901,349	A	5/1999	Guegnaud et al.	455/302
5,903,178	A	5/1999	Miyatsuji et al.	327/308
5,903,187	A	5/1999	Claverie et al.	329/342
5,903,196	A	5/1999	Salvi et al.	331/16
5,903,421	A	5/1999	Furutani et al.	361/58
5,903,553	A	5/1999	Sakamoto et al.	370/338
5,903,595	A	5/1999	Suzuki	375/207
5,903,609	A	5/1999	Kool et al.	375/261
5,903,827	A	5/1999	Kennan et al.	455/326
5,903,854	A	5/1999	Abe et al.	455/575
5,905,449	A	5/1999	Tsubouchi et al.	340/925.69
5,907,149	A	5/1999	Marckini	235/487
5,907,197	A	5/1999	Faulk	307/119

5,909,447	A		6/1999	Cox et al.	370/508
5,911,116	A		6/1999	Nosswitz	455/83
5,911,123	A		6/1999	Shaffer et al.	455/554
5,914,622	A		6/1999	Inoue	327/172
5,915,278	A		6/1999	Mallick	73/658
5,920,199	A		7/1999	Sauer	324/678
5,926,065	A		7/1999	Wakai et al.	329/304
5,926,513	A		7/1999	Suominen et al.	
5,933,467	A		8/1999	Sehier et al.	375/350
5,937,013	A		8/1999	Lam et al.	
5,943,370	A		8/1999	Smith	375/334
5,945,660	A		8/1999	Nakasuji et al.	235/462.46
5,949,827	A		9/1999	DeLuca et al.	
5,952,895	A		9/1999	McCune, Jr. et al.	332/128
5,953,642	A		9/1999	Feldtkeller et al.	455/195.1
5,955,992	A		9/1999	Shattil	
5,959,850	A		9/1999	Lim	363/17
5,960,033	A		9/1999	Shibano et al.	375/207
5,970,053	A	*	10/1999	Schick et al.	
5,982,315	A		11/1999	Bazarjani et al.	
5,995,030	A		11/1999	Cabler	
5,999,561	A	*	12/1999	Naden et al.	
6,005,903	A		12/1999	Mendelovicz	
6,011,435	A		1/2000	Takeyabu et al.	
6,014,176	A		1/2000	Nayebi et al.	
6,014,551	A		1/2000	Pesola et al.	
6,018,262	A		1/2000	Noro et al.	
6,018,553	A	*	1/2000	Sanielevici et al.	375/334
6,026,286	A		2/2000	Long	
6,028,887	A		2/2000	Harrison et al.	375/206
6,031,217	A		2/2000	Aswell et al.	
6,041,073	A		3/2000	Davidovici et al.	375/148
6,047,026	A		4/2000	Chao et al.	
6,049,573	A		4/2000	Song	
6,049,706	A		4/2000	Cook et al.	455/313
6,054,889	A		4/2000	Kobayashi	327/357
6,061,551	A		5/2000	Sorrells et al.	455/118
6,061,555	A		5/2000	Bultman et al.	455/313
6,064,054	A		5/2000	Waczynski et al.	
6,067,329	A		5/2000	Kato et al.	
6,073,001	A		6/2000	Sokoler	
6,076,015	A		6/2000	Hartley et al.	
6,078,630	A	*	6/2000	Prasanna	
6,081,691	A		6/2000	Renard et al.	455/12.1
6,084,465	A		7/2000	Dasgupta	
6,084,922	A		7/2000	Zhou et al.	375/316
6,085,073	A		7/2000	Palermo et al.	
6,091,939	A		7/2000	Banh	455/102
6,091,940	A		7/2000	Sorrells et al.	455/118
6,091,941	A		7/2000	Moriyama et al.	455/126
6,094,084	A		7/2000	Abou-Allam et al.	
6,098,046	A		8/2000	Cooper et al.	
6,098,886	A		8/2000	Swift et al.	235/472.1
6,121,819	A		9/2000	Traylor	327/326
6,125,271	A		9/2000	Rowland, Jr.	455/313
6,144,236	A		11/2000	Vice et al.	327/113
6,144,331	A		11/2000	Jiang	
6,144,846	A		11/2000	Durec	455/323
6,147,340	A		11/2000	Levy	250/214 R
6,147,763	A		11/2000	Steinlechner	356/484
6,150,890	A		11/2000	Damgaard et al.	331/14
6,151,354	A		11/2000	Abbey	
6,160,280	A		12/2000	Bonn et al.	
6,169,733	B1		1/2001	Lee	
6,175,728	B1		1/2001	Mitama	455/323
6,178,319	B1		1/2001	Kashima	
6,204,789	B1		3/2001	Nagata	
6,215,475	B1		4/2001	Meyerson et al.	345/173
6,225,848	B1		5/2001	Tilley et al.	
6,230,000	B1		5/2001	Tayloe	
6,266,518	B1		7/2001	Sorrells et al.	455/118
6,307,894	B1		10/2001	Eidson et al.	
6,313,685	B1		11/2001	Rabii	
6,314,279	B1		11/2001	Mohindra	
6,317,589	B1	*	11/2001	Nash	455/245.2
6,321,073	B1		11/2001	Luz et al.	
6,327,313	B1		12/2001	Traylor et al.	
6,330,244	B1		12/2001	Swartz et al.	
6,335,656	B1		1/2002	Goldfarb et al.	
6,353,735	B1		3/2002	Sorrells et al.	455/118
6,363,262	B1		3/2002	McNicol	
6,366,622	B1		4/2002	Brown et al.	
6,370,371	B1		4/2002	Sorrells et al.	455/323
6,400,963	B1		6/2002	Glockler et al.	
6,421,534	B1		7/2002	Cook et al.	
6,459,721	B1		10/2002	Mochizuki et al.	
6,516,185	B1		2/2003	MacNally	
6,531,979	B1		3/2003	Hynes	
6,542,722	B1		4/2003	Sorrells et al.	
6,560,301	B1		5/2003	Cook et al.	
6,580,902	B1		6/2003	Sorrells et al.	
6,600,795	B1		7/2003	Ohta et al.	
6,600,911	B1	*	7/2003	Morishige et al.	
6,608,647	B1		8/2003	King	
6,611,569	B1		8/2003	Schier et al.	
6,634,555	B1		10/2003	Sorrells et al.	
6,647,250	B1		11/2003	Bultman et al.	
6,686,879	B1	*	2/2004	Shattil	
6,687,493	B1		2/2004	Sorrells et al.	
6,690,232	B1		2/2004	Ueno et al.	
6,694,128	B1		2/2004	Sorrells et al.	
6,697,603	B1		2/2004	Lovinggood et al.	
6,704,549	B1	*	3/2004	Sorrells et al.	
6,704,558	B1	*	3/2004	Sorrells et al.	

FOREIGN PATENT DOCUMENTS

DE	196 27 640	A1	1/1997
DE	196 48 915	A1	6/1998
DE	197 35 798	C1	7/1998
EP	0 035 166	A1	9/1981
EP	0 099 265	A1	1/1984
EP	0 087 336	B1	7/1986
EP	0 254 844	A2	2/1988
EP	0 193 899	B1	6/1990
EP	0 380 351	A2	8/1990
EP	0 380 351	A3	2/1991
EP	0 411 840	A2	2/1991
EP	0 423 718	A2	4/1991
EP	0 411 840	A3	7/1991
EP	0 485 095	A1	5/1992
EP	0 423 718	A3	8/1992
EP	0 512 748	A2	11/1992
EP	0 529 836	A1	3/1993
EP	0 548 542	A1	6/1993
EP	0 512 748	A3	7/1993
EP	0 087 336	A1	8/1993
EP	0 560 228	A1	9/1993
EP	0 632 288	A2	1/1995
EP	0 632 577	A1	1/1995
EP	0 643 477	A2	3/1995
EP	0 643 477	A3	3/1995
EP	0 411 840	B1	10/1995
EP	0 696 854	A1	2/1996
EP	0 632 288	A3	7/1996
EP	0 732 803	A1	9/1996
EP	0 486 095	B1	2/1997
EP	0 782 275	A2	7/1997
EP	0 785 635	A1	7/1997
EP	0 789 449	A2	8/1997
EP	0 795 955	A3	9/1997
EP	0 795 955	A2	9/1997
EP	0 795 978	A2	9/1997

EP	0 817 369	A2	1/1998
EP	0 817 369	A3	1/1998
EP	0 837 565	A1	4/1998
EP	0 862 274	A1	9/1998
EP	0 874 499	A2	10/1998
EP	0 512 748	B1	11/1998
EP	0 877 476	A1	11/1998
EP	0 977 341	A	2/2000
FR	2 245 130		4/1975
FR	2 669 787	A1	5/1992
FR	2 743 231	A1	7/1997
GB	2 161 344	A	1/1986
GB	2 215 945	A	9/1989
GB	2 324 919	A	11/1998
JP	56-114451		9/1981
JP	59-144249		8/1984
JP	60-130203		7/1985
JP	61-30821		2/1986
JP	63-54002		3/1988
JP	2-39632		2/1990
JP	2-131629		5/1990
JP	2-276351		11/1990
JP	5-327356		12/1993
JP	8-32556		2/1996
JP	8-139524		5/1996
JP	9-36664		2/1997
WO	WO 80/01633	A1	8/1980
WO	WO 91/18445	A1	11/1991
WO	WO 94/05087	A1	3/1994
WO	WO 95/01006	A1	1/1995
WO	WO 96/02977	A1	2/1996
WO	WO 96/08078	A1	3/1996
WO	WO 96/39750	A1	12/1996
WO	WO 97/08839	A3	3/1997
WO	WO 97/08839	A2	3/1997
WO	WO 97/38490	A1	10/1997
WO	WO 98/00953	A1	1/1998
WO	WO 98/21201	A1	6/1998
WO	WO 98/40968	A3	9/1998
WO	WO 98/40968	A2	9/1998
WO	WO 99/23755	A1	5/1999
WO	WO 00/31659	A1	6/2000

OTHER PUBLICATIONS

Aghvami, H. et al., "Land Mobile Satellites Using the Highly Elliptic Orbits The UK T SAT Mobile Payload," *Fourth International Conference on Satellite Systems for Mobile Communications and Navigation,* , IEE, pp. 147–153 (Oct. 17–19, 1988).

Akers, N. P. et al., "RF Sampling Gates: a Brief Review," *IEE Proceedings,* IEE, vol. 133, Part A, No. 1, pp. 45–49 (Jan. 1986).

Al–Ahmad, H.A.M. et al., "Doppler Frequency Correction for a Non–Geostationary Communications Satellite. Techniques for CERS and T–SAT, " *Electronics Division Colloquium on Low Noise Oscillators and Synthesizers,* IEE, pp. 4/1–4/5 (Jan. 23, 1986).

Ali, I. et al., "Doppler Characterization for LEO Satellites," *IEEE Transactions on Communications,* IEEE, vol. 46, No. 3, pp. 309–313 (Mar. 1998).

Allan, D.W., "Statistics of Atomic Frequency Standards," *Proceedings Of The IEEE Special Issue on Frequency Stability,* IEEE, pp. 221–230 (Feb. 1966).

Allstot, D.J. et al., "MOS Switched Capacitor Ladder Filters," *IEEE Journal of Solid State Circuits, IEEE,* vol. SC–13, No. 6, pp. 806–814 (Dec. 1978).

Allstot, D.J. and Black Jr. W.C., "Technological Design Considerations for Monolithic MOS Switched–Capacitor Filtering Systems," *Proceedings of the IEEE,* IEEE, vol. 71, No. 8, pp. 967–986 (Aug. 1983).

Alouini, M. et al., "Channel Characterization and Modeling for Ka–Band Very Small Aperture Terminals." *Proceedings Of the IEEE,*IEEE, vol. 85, No. 6, pp. 981–997 (Jun. 1997).

Andreyev, G.A. and Ogarev, S.A., "Phase Distortions of Keyed Millimeter–Wave Signals In the Case of Propagation in a Turbulent Atomsphere," *Telecommunications and Radio Engineering,* Scripta Technica, vol. 43, No. 12, pp. 87–90 (Dec. 1988).

Antonetti, A. et al., "Optoelectronic Sampling in the Picosecond Range," *Optics Communications,* North–Holland Publishing Company, vol. 21, No. 2, pp. 211–214 (May 1977).

Austin, J. et al., "Doppler Correction of the Telecommunication Payload Oscillators in the UK T–SAT," *18th European Microwave Conference,* Microwave Exhibitions and Publishers Ltd., pp. 851 857 (Sep. 12 15, 1988).

Auston, D.H., "Picosecond optoelectronic switching and gating in silicon," *Applied Physics Letters,* American Institute of Physics, vol. 26, No. 3, pp. 101 103 (Feb. 1, 1975).

Baher, H., "Transfer Functions for Switched–Capacitor and Wave Digital Filters," *IEEE Transactions on Circuits and Systems,* IEEE Circuits and Systems, Society, vol. CAS–33, No. 11, pp. 1138 1142 (Nov. 1986).

Baines, R., "The DSP Bottleneck," *IEEE Communications Magazine,* IEEE Communications Society, pp. 46–54 (May 1995).

Banjo, O.P. and Vilar, E., "Binary Error Probabilites on Earth–Space Links Subject to Scintillation Fading," *Electronics Letters,* IEE, vol. 21, No. 7, pp. 296–297 (Mar. 28, 1985).

Banjo, O.P. and Vilar, E., "The Dependence of Saint Path Amplitude Scintillations on Various Meterorological Parameters," *Fifth International Conference on Antennas and Propagation* (ICAP 87) Part 2: *Propagation,* IEE, pp. 277–280 (Mar. 30 –Apr. 2, 1987).

Banjo. O.P. and Vilar, E. "Measurement and Modeling of Scintillations on Low–Elevations Earth–Space Paths and Impact on Communication Systems." *IEEE Transactions on Communications,* IEEE Communications Society, vol. COM–34, No. 8, pp. 774–780 (Aug. 1986).

Banjo, O.P. et al., "Troposheric Amplitude Spectra Due to Absorption and Scattering in Earth Space Paths," *Fourth International Conference on Antennas and Propagation* (ICAP 85), IEE, pp. 77–82 (Apr. 16–19, 1985).

Baslli, P. et al., "Case Study of Intense Scintillation Events on the OTS Path," *IEEE Transactions on Antennas and Propagation,* IEEE, vol. 38, No. 1, pp. 107–113 (Jan. 1990).

Basilli, P. et al., "Observation of High C^2 and Turbulent Path Length on OTS Space–Earth Link," *Electronics Letters,* IEE, vol. 24, No. 17, pp. 1114–1116 (Aug. 18, 1988).

Blakey, J.R. et al., "Measurement of Atmospheric Millimetre–Wave Phase Scintillations in an Absorption Region," *Electronics Letters,* vol. 21, No. 11, pp. 486–487 (May 23, 1985).

Burgueño, A. et al., "Influence of rain gauage integration time on the rain rate statistics used in microwave communications," *annales des tèlècommunications,* International Union of Radio Science, pp. 522–527 (Sep./Oct. 1988).

Burgueño, "Long–Term Joint Statistical Analysis of Duration and intensity of Rainfall Rate Return Periods in the Context of Microwave Communications," *Sixth International Conference on Antennas and Propagation* (ICAP 89) Part 2: Propagation, IEE, pp. 297–301 (Apr. 4–7, 1989).

Burguño, et al., "Long Term Statistics of Precipitation Rate Return Periods in the Context of Microwave Communications," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation,* IEE, pp. 297–301 (Apr. 4–7, 1989).

Burgueño, A. et al., "Spectral Analysis of 49 Years of Rainfall Rate and Relation to Fade Dynamics," *IEEE Transactions on Communications,* IEEE Communications Society, vol. 38, No. 9, pp. 1359–1366 (Sep. 1990).

Catalan, C. and Vitar, E., "Approach for satellite slant path remote sensing," *Electronics Letters,* IEE, vol. 34, No. 12, pp. 1238–1240 (Jun. 11, 1998).

Chan, P. et al., "Highly Linear 1–GHz CMOS Downconversion Mixer," *European Solid State Circuits Conference,* IEEE Communication Society, pp. 210–213 (Sep. 22–24, 1993).

Copy of Declaration of Michael J. Bultman filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.

Copy of Declaration of Robert W. Cook filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.

Copy of Declaration of Alex Holtz filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 3 pages.

Copy of Declaration of Richard C. Looke filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.

Copy of Declaration of Charley D. Moses, Jr. filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.

Copy of Declaration of Jeffrey L. Parker and David F. Sorrells, with attachment Exhibit 1, filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 130 pages.

Dewey, R.J. and Collier, C.J., "Multi Mode Radio Receiver," *Electronics Division Colloqium on Digitally Implemented Radios,* IEE, pp. 3/1–3/5 (Oct. 18, 1985).

Dialog File 347 (Japio) English Language Patent Abstract for JP 2–276351, 1 page (Nov. 13, 1990–Date of publication of application).

Dialog File 347 (JAPIO) English Language Patent Abstract for JP 2–131629, 1 page (May 21, 1990 –Date of publication of application).

Dialog File 347 (JAPIO) English Language Patent Abstract for JP 2–39632, 1 page (Feb. 8, 1990 –Date of publication of application).

Dialog File 348 (European Patents) English Language Patent Abstract for EP 0 785 635 A1, 3 pages (Dec. 26, 1996 –Date of publication of application).

Dialog File 348 (European Patents) English Language Patent Abstract for EP 35166 A1, 2 pages (Feb. 18, 1981 –Date of publication of application).

"DSO takes sampling rate to 1 Ghz," *Electronic Engineering,* Morgan Grampian Publishers, vol. 59, No. 723, pp. 77 and 79 (Mar. 1987).

Erdi, G. and Henneuse, P.R., "A Precision FET–Less Sample–and–Hold with High Charge–to–Droop Current Ratio," *IEEE Journal of Solid–State Circuits,* IEEE, vol. SC–13, No. 6, pp. 864–873 (Dec. 1978).

Faulkner, N.D. and Vitar, E., "Subharmonic Sampling for the Measurement of Short Term Stability of Microwave Oscillators," *IEEE Transactions on Instrumentation and Measurement,* IEEE, vol. IM–32, No. 1, pp. 208–213 (Mar. 1983).

Faulkner, N.D. et al., "Sub Harmonic Sampling for the Accurate Measurement of Frequency Stability of Microwave Oscillators," *CPEM 82 Digest: Conference on Precision Electromagnetic Measurements,* IEEE, pp. M–10 and M–11 (1982).

Faulkner, N.D. and Vilar, E., "Time Domain Analysis of Frequency Stability Using Non–Zero Dead–Time Counter Techniques," *CPEM 84 Digest Conference on Precision Electromagnetic Measurements,* IEEE, pp. 81–82 (1984).

Filip, M. and Vilar, E., "Optimum Utilization of the Channel Capacity of a Satellite Link in the Presence of Amplitude Scintillations and Rain Attenuation," *IEEE Transactions on Communications,* IEEE Communications Society, vol. 38, No. 11, pp. 1958–1965 (Nov. 1990).

Fukahori, K., "CMOS Narrow–Band Signaling Filter with Q Reduction," *IEEE Journal of Solid–State Circuits,* IEEE, vol. SC–19, No. 6, pp. 926–932 (Dec. 1984).

Fukuchi, H. and Otsu, y., "Available time statistics of rain attenuation on earth space path," *IEE Proceedings H: Microwaves, Antennas and Propagation,* IEE, vol. 135, Pt. H, No. 6, 387–390 (Dec. 1988).

Gibbons, C.J. and Chadha, R., "Millimetre–wave propagation through hydrocarbon flame," *IEE Proceedings,* IEE, vol. 134, Pt. H, No. 2, pp. 169–173 (Apr. 1987).

Gilchrist, B. et al., "Sampling hikes performance of frequency syntheizers," *Microwaves & RF,* Hayden Publishing, vol. 23, No. 1, pp. 93 94 and 110 (Jan. 1984).

Gossard, E.E., "Clear weather meteorological on propagation at frequencies above 1 Ghz," *Radio Science,* American Geophysical Union, vol. 16, No. 5, pp. 589–608 (Sep.–Oct. 1981).

Gregorian, R. et al., "Switched–Capacitor Circuits Design," *Proceedings of the IEEE, IEEE,* vol. 71, No. 8, pp. 941–966 (Aug. 1983).

Groshong et al., "Undersampling Techniques Simplify Digital Radio," *Electronic Design,* Penton Publishing, pp. 67–68, 70, 73–75 and 78 (May 23, 1991).

Grove, W.M., "Sampling for Oscilloscope and Other RF Systems: Dc through X–Band," *IEEE Transactions on Microwave Theory and Techniques,* IEEE, pp. 629–635 (Dec. 1966).

Haddon, J. et al., "Measurement of Microwave Scintillations on a Satellite Down Link at X Band," *Antennas and Propagation,* IEE, pp. 113–117 (1981).

Haddon, J. and Vilar, E., "Scattering Induced Microwave Scintillations from Clear Air and Rain on Earth Space Paths and the Influence of Antenna Aperture," *IEEE Transactions on Antennas and Propagation,* IEEE, vol. AP–34, No. 5, pp. 646–657 (May 1986).

Hafdallah, H. et al., "2–4 Ghz MESFET Sampler," *Electronics Letters,* IEE, vol. 24, No. 3, pp. 151 153 (Feb. 4, 1988).

Herban, M.H.A.J., "Amplitude and Phase Scintillation Measurements on 8–2 km Line–Of–Sight Path at 30 Ghz," *Electronics Letters,* IEE, vol. 18, No. 7, pp. 287–289 (Apr. 1. 1982).

Hewitt, A. et al., "An 18 Ghz Wideband LOS Multipath Experiment," *International Conference on Measurements for Telecommunication Transmission Systems* –MTTS 85, IEE, pp. 112–116 (Nov. 27–28, 1985).

Hewitt, A. et al., "An Autoregressive Approach to the Identification of Multipath Ray Parameters from Field Measurements," *IEEE Transactions on Communications,* IEEE Communications Society, vol. 37, No. 11, pp. 1136–1143 (Nov. 1989).

Hewitt, A. and Vilar, E., "Selective fading on LOS Microwave Links: Classical and Spread–Spectrum Measurement Techniques," *IEEE Transactions on Communications,* IEEE Communications Society, vol. 36, No. 7, pp. 789 796 (Jul. 1988).

Hospitalier, E., "Instruments for Recording and Observing Rapidly Varying Phenomena," *Science Abstracts,* IEE, vol. VII, pp. 22–23 (1904).

Howard, I.M. and Swansson, N.S., "Demodulating High Frequency Resonance Signals for Bearing Fault Detection," *The Institution of Engineers Australia Vibration and Noise Conference,* Institution of Engineers, Australia, pp. 115–121 (Sep. 18–20, 1990).

Hu, X., *A Switched–Current Sample–and–Hold Amplifier for FM Demodulation,* Thesis for Master of Applied Science, Dept. of Electrical and Computer Engineering, University of Toronto, UMI Dissertation Services, pp. 1–64 (1995).

Hung, H–L, A. et al., "Characterization of Microwave Integrated Circuits Using An Optical Phase–Locking and Sampling System," *IEEE MTT–S Digest,* IEEE, pp. 507–510 (1991).

Hurst, P.J., "Shifting the Frequency Response of Switched–Capacitor Filters by Nonuniform Sampling," *IEEE Transactions on Circuits and Systems,* IEEE Circuits and Systems Society, vol. 38, No. 1, pp. 12–19 (Jan. 1991).

Itakura, T., "Effects of the sampling pulse width on the frequency characteristics of a sample–and–hold circuits," *IEE Proceedings Circuits, Devices and Systems,* IEE, vol. 141, No. 4, pp. 328–336 (Aug. 1994).

Janssen, J.M.L., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: I. Fundamentals," *Phillips Technical Review,* Philips Research Laboratories, vol. 12, No. 2, pp. 52 59 (Aug. 1950).

Janssen, J.M.L. and Michels, A.J., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: II. Electrical Build–up," *Philips Technical Review,* Philips Research Laboratories, vol. 12, No. 3, pp. 73–82 (Sep. 1950).

Jondral, V.F. et al., "Doppler Profiles for Communications Satellites," *Frequenz,* Herausberger, pp. 111–116 (May–Jun. 1996).

Kaleh, G.K., "A Frequency Diversity Spread Spectrum System for Communication in the Presence of In–band Interference," *1995 IEEE Globecom,* IEEE Communication Society, pp. 66–70 (1995).

Merkelo, J. and Hall, R.D., "Broad–Band–Thin–Film Signal Sampler," *IEEE Journal of Solid State Cicuits,* IEEE, vol. SC 7, No. 1, pp. 50 54 (Feb. 1972).

Merlo, U. et al., "Amplitude Scintillation Cycles in a Sirlo Satellite–Earth Link," *Electronics Letters,* IEE, vol. 21, No. 23, pp. 1094–1096 (Nov. 7, 1985).

Morris, D., "Radio–holographic reflector measurement of the 30–m millimeter radio telescope at 22 Ghz with a cosmic signal source," *Astronomy and Astrophysics,* Springer–Vertag, vol. 203, No. 2, pp. 399–406 (Sep. (II) 1988).

Moulsley, T.J. et al., "The efficient acquisition and processing of propagation statistics," *Journal of the Institution of Electronic and Radio Engineers,* IERE, vol. 55, No. 3, pp. 97–103 (Mar. 1985).

Ndzi, D. et al., "Wide–Band Statistical Characterization of an Over–the–Sea Experimental Transhorizon Link," *IEE Colloquium on Radio Communications at Microwave and Millimetre Wave Frequencies,* IEE, pp. 1/1–1/6 (Dec. 16, 1996).

Ndzi, D. et al., "Wideband Statistics of Signal Levels and Doppler Spread on am Over–The–Sea Transhorizon Link," *IEE Colloquium on Propagation Characteristics and Related System Techniques for Beyond Line of Sight Radio,* IEE, pp. 9/1–9/6 (Nov. 24, 1997).

"New zero IF chipset from Philips," *Electronic Engineering,* United News & Media, vol. 67, No. 825, p. 10 (Sep. 1995).

Ohara, H. et al., "First monolithic PCM filter cuts of telecomm systems," *Electronic Design,* Hayden Publishing Company, vol. 27, No. 8, pp. 130–135 (Apr. 12, 1979).

Oppenheim, A.V. et al., *Signals and Systems,* Prentice–Hall, pp. 527–562 and 561–562 (1983).

Ortgies, G., "Experimental Parameters Affecting Amplitude Scintillation Measurements on Satellite Links," *Electronics Letters,* IEE, vol. 21, No. 17, pp. 771–772 (Aug. 15, 1985).

Pärssinen et al., "A 2–GHz Subharmonic Sampler for Signal Downconversion," *IEEE Transactions on Microwave Theory and Techniques,* IEEE, vol. 45, No. 12, 7 pages (Dec. 1997).

Peeters, G. et al., "Evaluation of Statistical Models for Clear–Air Scintillation Prediction Using Olympus Satellite Measurements," *International Journal of Satellite Communications,* John Wiley and Sons, vol. 15, No. 2, pp. 73–88 (Mar. Apr. 1997).

Perrey, A.G. and Schoenwetter, H.K., *NBS Technical Note 1121: A Schottky Diode Bridge Sampling Gate,* U.S. Dept. of Commerce, pp. 1 14 (May 1980).

Poulton, K. et al., "A 1–Ghz 6–bit ADC System," *IEEE Journal of Solid–State Circuits,* IEEE, vol. SC–22, No. 6, pp. 962 969 (Dec. 1987).

Press Release, "Parkervision, Inc. Announces Fiscal 1993 Results," Lippert/Hellshorn and Associates, 2 Pages (Apr. 6, 1994).

Press Release, "Parkervision, Inc. Announces the Appointment of Michael Baker to the New Position of National Sales Manager," Lippert/Heilshorn and Associates, 1 Page (Apr. 7, 1994).

Press Release, "Parkervision's Cameraman Well–Received By Learning Market," Lippert/Hellshorn and Associates, 2 Pages (Apr. 8, 1994).

Press Release, "Parkervision, Inc. Announces First Quarter Financial," Lippert/Hellshorn and Associates, 2 Pages (Apr. 26, 1994).

Press Release, "Parkvision, Inc. Announces The Retirement of William H. Fletcher, Chief Financial Officer," Lippert/Heilshorn and Associates, 1 Page (May 11, 1994).

Press Release, "Parkervision, Inc. Announces New Cameraman System II ™ At Infocomm Trade Show," Lippert/Hellshorn and Associates, 3 Pages (Jun. 9, 1994).

Press Release, "Parkvision, Inc. Announces Appointments to its National Sales Force," Lippert/Hellishorn and Associates, 2 Pages (Jun. 17, 1994).

Press Release, "Parkvision, Inc. Announces Second Quarter and Six Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (Aug. 9, 1994).

Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (Oct. 28, 1994).

Press Release, "Parkervision, Inc. Announces First Significent Dealer Sale of its *Cameraman*● System II," Lippert/Heilshorn and Associates, 2 Pages (Nov. 7, 1994).

Press Release, "Parkvision, Inc. Announces Fourth Quarter and Year End Results," Lippert/Heilshorn and Associates, 2 Pages (Mar. 1, 1995).

Press Release, "Parkervision, Inc. Announces Joint Products Developments With VTEL," Lippert/Heilshorn and Associates, 2 Pages (Mar. 21, 1995).

Press Release, "Parkervision, Inc., Announces First Quarters Financial Results," Lippert/Heilshorn and Associates, 3 Pages (Apr. 28, 1995).

Press Release, "Parkvision Wins Top 100 Product Districts'Choice Award," Parkervision Marketing and Manufacturing Headquarters, 1 Page (Jun. 29, 1995).

Press Release, "Parkervision National Sales Manager Next President of USDLA," Parkervision Marketing and Manufacturing Headquarters, 1 Page (Jul. 6, 1995).

Press Release, "Parkervision Granted New Patent," Parkervision Marketing and Manufacturing Headquarters, 1 Page (Jul. 21, 1995).

Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Page (Jul. 31, 1995).

Press Release, "Parkervision, Inc. Expands Its Cameraman System II Product Line," Pakervision Marketing and Manufacturing Headquarters, 2 Pages (Sep. 22, 1995).

Press Release, "Parkervision Announces New Camera Control Camera Technology," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Oct. 25, 1995).

Press Release, "Parkervision, Inc. Announces Completion of VTEL/PArkervision Joint Product Line" Parkervision Marketing and Manufacturing Headquarters, 2 Pages (Oct. 30 , 1995).

Press Release "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manfacturing Headquarters, 2 Pages (Oct. 30, 1995).

Press Release, "Parkervision's Cameraman Personal Locator Camera System Wins Telecon XV Award," Parkvision Marketing and Manufacturing Headquarters, 2 pages (Nov. 1, 1995).

Press Release, "Parkervision, Inc. Announces Purchase Commitment From VTEL Corporation," Parkervision Marketing and Manufacturing Headquarters, 1 page (Feb. 26, 1996).

Press Release, "ParkVision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 2 page (Feb. 27, 1996).

Press Release, "Parkervision, Inc. Expands its Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Mar. 7, 1996).

Press Release, "ParkerVision Files Patents for its Research of Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 1 page (Mar. 28, 1996).

Press Release, "Parkervision, Inc. Announces First Significant Sale of its Cameraman● Three–Chip System," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Apr. 12, 1996).

Press Release, "Parkervision, Inc. Introduces New Product Line For Studio Production Market," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Apr. 15, 1996).

Press Release, "Parkervision, Inc. Announces Private Placement of 800,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 1 page (Apr. 15, 1996).

Press Release, "Parkervision, Inc. Announces First Quarters Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Apr. 30, 1996).

Press Release, "ParkerVision's New Studio Product Wins Award," Parkvision Marketing and Manufacturing Headquarters, 2 pages (Jun. 5, 1996).

Press Release, "Parkvision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manfacturing Headquarters, 3 pages (Aug. 1, 1996).

Press Release, "Parkvision, Inc. Announces Third Quarters and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Oct. 29, 1996).

Press Release, "PictureTel and ParkVision Sign Reseller Agreement," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Oct. 30, 1996).

Press Release, "CLI and Parkervision Bring Enhanced Ease–of–Use to Videoconferencing," CLI/Parkervision, 2 pp. (Jan. 20, 1997).

Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Hedquarters, 3 pages (Feb. 27, 1997).

Press Release, "Parkervision, Inc. Announces First Quarter Financial results," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Apr. 29, 1997).

Press Release, "NEC and Parkervision Make Distance Learning Closer," NEC America, 2 pages (Jun. 18, 1997).

Press Release, "Parkervision Supplies JPL with Robotic Cameras, Cameraman Shoot Director for Mars Mission," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Jul. 8, 1997).

Press Release, "Parkervision and IBM Join Forces to Create Wireless Computer Peripherals," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Jul. 23, 1997).

Press Release, "Parkervision, Inc. Announces Second Quarters and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Jul. 13, 1997).

Press Release, "Parkervision, Inc. Announces Private Placement of 990,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Sep. 8, 1997).

Press Release, "Wal–Mart Chooses Parkervision for Broadcast Production," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Oct. 24, 1997).

Press Release, "Parkervision, Inc. Announces Third Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Oct. 30, 1997).

Press Release, "Parkervision Announces Breakthrough in Wireless Radio Frequency Technology," Parkervision Marketing Headquarters, 3 pages (Dec. 10, 1997).

Press Release, "Parkervision, Inc. Announces the Appointment of Joseph F. Skovron to the Position of Vice President, Licensing –Wireless Technologies," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Jan. 9, 1998).

Press Release, "Parkervision Announces Existing Agreement with IBM Terminates– Company Continues with Strategic Focus Announced in Dec." Parkervision Marketing and Manufacturing Headquarters, 2 pages (Jan. 27, 1998).

Press Release, "Laboratory Tests Verify Pakervision Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Mar. 3, 1998).

Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Finanical Results," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Mar. 5, 1998).

Press Release, "Pakervision Awarded Editors'Pick of Show for NAB 98," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Apr. 15, 1998).

Press Release, "Parkervision Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 pages (May 4, 1998).

Press Release, "Parkervision 'DIRECT2DATA'Introduced in Response to Market Demand," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Jul. 9, 1998).

Press Release, "Parkervision Expands Senior Management Team," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Jul. 29, 1998).

Press Release, "Parkervision Announces Second Quarter and Six Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 4 pages (Jul 30, 1998).

Press Release, "Parkervision Announces Third Quarter and Nine Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Oct. 30, 1998).

Press Release, "Questar Infocomm, Inc. Invests $ Million in Parkervision Common Stock," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Dec. 2, 1998).

Press Release, "Parkervision Adds Two New Directors," Parkervision Marketing and Marketing Headquarters, 2 pages (Mar. 5, 1999).

Press Release, "Parkervision Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 pages (Mar. 5, 1999).

Press Release, "Joint Marketing Agreement Offers New Automated Production Solution," Parkervision Marketing and Manufacturing Headquarters, 2 pages (Apr. 13, 1999).

"Project COST 205: Scintillations in Earth–satellite links," *Alta Frequenza: Scientific Review in Electronics,* AEI, vol. LIV, No. 3, pp. 209–211 (May–Jun. 1985).

Razavi, B., *RF Microelectronics,* Prentice–Hall, pp. 147–149 (1998).

Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 1), " *Electronic Engineering,* Morgan Brothers Limited, vol. 31, No. 373, pp. 130–137 (Mar. 1959).

Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 2)," *Electronic Engineering,* Morgan Brothers Limited, vol. 31, No. 374, pp. 204 212 (Apr. 1959).

Rein, H.M. and Zahn, M. "Subnanosecond–Pulse Generator with Variable Pulsewidth Using Avalanche Transistors," *Electronics Letters,* IEE, vol. 11, No. 1, pp. 21–23 (Jan. 9, 1975).

Riad, S.M. and Nahman, N.S., "Modeling of the Feed–through Wideband (DC to 12.4 Ghz) Sampling–Head," *IEEE MTT–S International Microwave Symposium Digest,* IEEE, pp. 267–269 (Jun. 27–29, 1978).

RIzzoli, V. et al., "Computer–Aided Noise Analysis of MESFET and HEMT Mixers," *IEEE Transactions on Microwave Theory and Techniques,* IEEE, vol. 37, No. 9, pp. 1401–1410 (Sep. 1989).

Rowe, H.E., *Signal and Noise in Communication Systems,* D. Van Nostrand Company, Inc., Princeton, New Jersey, including, for example, Chapter V, Pulse Modulation Systems (1965).

Rucker, F. and Dintelmann, F., "Effect of Antenna Size on OTS Signal Scintillations and Their Seasonal Dependence," *Electronics Letters,* IEE, vol. 19, No. 24, pp. 1032–1034 (Nov. 24, 1983).

Russell, R. and Hoare, L. "Millimeter Wave Phase Locked Oscillators," *Military Microwave '78 Conference Proceedings,* Microwave Exhibitions and Publishers, pp. 238–242 (Oct. 25–27, 1978).

Sabel, L.P., "A DSP Implementation of a Robust Flexible Receiver/Demultiplexer for Broadcast Data Satellite Communications," *The Institution of Engineers Australia Communications Conference,* Institution of Engineers, Australia, pp. 218 223 (Oct. 16 18, 1990).

Salous, S., "IF digital generation of FMCW waveforms for wideband channel characterization," *IEE Proceedings–I,* IEE, vol. 139, No. 3, pp. 281–288 (Jun. 1992).

"Sampling Loops Lock Sources to 23 Ghz," *Microwaves & RF,* Penton Publishing, p. 212 (Sep. 1990).

Sassikumer, M. et al., "Active Compensation in the Switched–Capacitor Biquad," *Proceedings of the IEEE,* IEEE, vol. 71, No. 8, pp. 1008–1009 (Aug. 1983).

Saul, P.H., "A GaAs MESFET Sample and Hold Switch," *Fifth European Solid State Circuits Conference–ESSCIRC 79,* IEE, pp. 5–7 (1979).

Shen, D.H. et al., "A 900–MHZ RF Front–End Integrated Discrete–Time Filtering," *IEEE Journal of Solid–State Circuits,* IEEE Solid State Circuits Council, vol. 31, No. 12, pp. 1945 1954 (Dec. 1996).

Shen, X.D. and Vitar, E., "Anomalous transhorizon propagation and meterological processes of a multlink path," *Radio Science, American Geophysical Union,* vol. 30, No. 5, pp. 1467–1479 (Sep.–Oct. 1995).

Shen, X. and Tawfik, A.N., "Dynamic Behavior of Radio Channels Due to Trans Horizon Propagation Mechanisms," *Electronics Letters,* IEE, vol. 29, No. 17, pp. 1582 1583 (Aug. 19, 1993).

Shen, X. et al., "Modeling Enhanced Spherical Diffraction and Troposcattering on a Transhorizon Path with aid of the parabolic Equation and Ray Tracing Methods," *IEE Colloquium on Common modeling techniques for electromagnetic wave and acoustic wave propagation,* IEE, pp. 4/1–4/7 (Mar. 8, 1996).

Shen, X. and Vilar, E., "Path loss statistics and mechanisms of transhorizon propagation over a sea path," *Electronics Letters,* IEE, vol. 32, No. 3, pp. 259–261 (Feb. 1, 1996).

Shen, D. et al., "A 900 MIIZ Integrated Discrete–Time Filtering RF Front–End," *IEEE International Solid State Circuits Conference,* IEEE, vol. 39, pp. 54–55 and 417 (Feb. 1996).

Spillard, C. et al., "X–Band Troposheric Transhorizon Propagation Under Differing Meteorological Conditions," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation,* IEE, pp. 451–455 (Apr. 4–7, 1989).

Strafford, K.R. et al., "A Complete Monolithic Sample/Hold Amplifier," *IEEE Journal of Solid–State Cicuits,* IEEE, vol. SC 9, No. 6, pp. 381–387 (Dec. 1974).

Staruk, W. Jr. et al., "Pushing HF Data Rates," *Defense Electronics,* EW Communications, vol. 17, No. 5, pp. 211, 213, 215, 217, 220 and 222 (May 1985).

Stephenson, A.G., "Digitizing multiple RF signals requires an optimum sampling rate," *Electronics,* McGraw–Hill, pp. 106–110 (Mar. 27, 1972).

Sugarman, R., "Sampling Oscilloscope for Statistically Varying Pulses," *The Review of Scientific Instruments,* American Institute of Physics, vol. 28, No. 11, pp. 933–938 (Nov. 1957).

Sylvain, M., "Experimental probing of multipath microwave channels," *Radio Science,* American Geophysical Union, vol. No. 2, pp. 160–178 (Mar.–Arp. 1989).

Takano, T., "Novel GaAs Pet Phase Dectector Operable To Ka Band," *IEEE MT–S Digest,* IEEE, pp. 381–383 (1984).

Tan, M.A., "Biquadratic Transconductance Switched–Capacitor Filters," *IEEE Transactions on Circuits and Systems–I: Fundamental Theory and Applications,* IEEE Circuits and Systems Society, vol. 40, pp. 272–275 (Apr. 1993).

Tanaka, K. et al., "Single Chip Multisystem AM Stereo Decoder IC," *IEEE Transactions on Consumer Electronics,* IEEE Consumer Electronics Society, vol. CE–32, No. 3, pp. 482 496 (Aug. 1986).

Tawfik, A.N., "Amplitude, Duration and Predictability of Long Hop Trans–Horizon X–band Signals Over the Sea," *Electronics Letters,* IEE, vol. 28, No. 6, pp. 571–572 (Mar. 12, 1992).

Tawfik, A.N. and Vilar, E., "Correlation of Transhorizon Signal Level Strength with Localized Surface Meteorological Parameters," *Eighth International Conference on Antennas and Propagation,* Electronics Division of the IEE, pp. 335–339 (Mar. 30–Apr. 2, 1993).

Tawfik, A.N. and Vilar, E., "Dynamic Structure of a Transhorizon Signal at X–band Over a Sea Path,"*Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation,* IEE, pp. 446–450 (Apr. 4–7, 1989).

Tawfik, A.N. and Vilar, E., "Statistics of Duration and Intensity of Path Loss in a Microwave Transhorizon Sea-Path," *Electronics Letters,* IEE, vol. 26, No. 7, pp. 474 476 (Mar. 29, 1990).

Tawfik, A. N. and Vilar, E., "X–Band Transhorizon Measurements of CW Transmissions Over the Sea–Part 1: Path Loss, Duration of Events, and Their Modelings," *IEEE Transactions on Antennas and Propagation,* IEEE Antennas and Propagation Society, vol. 41, No. 11, pp. 1491–1500 (Nov. 1993).

Temes, G.C. and Tsividis, T., "The Special Section on Switched–Capacitor Circuits," *Proceedings of the IEEE,* IEEE, vol. 71, No. 8, pp. 915–916 (Aug. 1983).

Thomas, G.B., *Calculus and Analytic Geometry,* Third Edition, Addison Wesley Publishing, pp. 119 133 (1960).

Tomassetti, Q., "An Unusual Microwave Mixer," *16th European Microwave Conference,* Microwave Exhibitions and Publishers, pp. 754–759 (Sep. 8–12, 1986).

Tortoli, P. et al., "Bidirectional Doppler Signal Analysis is Based on a Single RF Sampling Channel," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control,* IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, vol. 41, No. 1, pp. 1 3 (Jan. 1984).

Tsividis, Y. and Antognetti, P. (Ed.), *Design of MOS VLSI Circuits for Telecommunications,* Prentice–Hall, p. 304 (1985).

Tsividis, Y., "Principles of Operation and Analysis of Switched–Capacitor Circuits," *Proceedings of the IEEE,* IEEE, vol. 71, No. 8, pp. 926–940 (Aug. 1983).

Tsurumi, H. and Maeda, T., "Design Study on a Direct Conversion Receiver Front–End for 280 MHZ, 900 MHZ, and 2.6 Ghz Band Radio Communication Systems," *41st IEEE Vehicular Technology Conference,* IEEE Vehicular Technology Society, pp. 457–462 (May 19–22, 1991).

Valdmanis, J. A. et al., "Picosecond and Subpicosend Optoelectronics for Measurements of Future High Speed Electronic Devices," *IEDM Technical Digest,* IEEE, pp. 597–600 (Dec. 5–7, 1983).

van de Kamp, M.M.J.L., "Asymmetric signal level distribution due to tropospheric scintillation," *Electronics Letters,* IEE, vol. 34, No. 11, pp. 1145–1146 (May 28, 1998).

Vasseur, H. and Vanoenacker, D., "Charaterization of tropospheric turbulent layers from radiosonde data," *Electronics Letters,* IEE, vol. 34, No. 4, pp. 318–319 (Feb. 19, 1998).

Verdone, R., "Outage Probability Analysis for Short–Range Communication Systems at 60 Ghz in ATT Urban Environments," *IEEE Transactions on Vehicular Technology,* IEEE Vehicular Technology Society, vol. 46, No. 4, pp. 1027–1039 (Nov. 1997).

Vierira–Ribeiro, S. A. *Single–IF DECT Receiver Architecture using a Quadrature Sub–Sampling Band–Pass Sigma–Delta Modulator,* Thesis for Degree of Master's of Engineering, Carleton University, UMI Dissertation Services, pp. 1–180 (Apr. 1995).

Vilar, E. et al., "A Comprehensive/Selective MM–Wave Satellite Downlink Experiment on Fade Dynamics," *Tenth International Conference on Antennas and Propagation,* Electronics Division of the IEE, pp. 2.98–2. 101 (Apr. 14–17, 1997).

Vilar, E. et al., "A System to Measure LOS Atmospheric Transmittance at 19 Ghz," *AGARD Conference Proceedings No. 346: Characteristics of the Lower Atmosphere Influencing Radio Wave Propagation,* AGARD, pp. 8–1 –8–16 (Oct. 4–7, 1983).

Vilar, E. and Smith, H., "A Theoretical and Experimental Study of Angular Scintillations in Earth Space Paths,"*IEEE Transactions on Antennas and Propagation,* IEEE, vol. AP–34, No. 1, pp. 2–10 (Jan. 1986).

Vilar, E. et al., "A Wide Band Transhorizon Experiment at 11.6 Ghz," *Eigth International Conference on Antennas and Propagation,* Electronics Division of the IEE, pp. 441–445 (Mar. 30–Apr. 2, 1993).

Vilar, E. and Matthews, P. A., "Amplitude Dependence of Frequency in Oscillators," *Electronics Letters,* IEE, Vol. 8, No. 20, pp. 509–511 (Oct. 5, 1972).

Vilar, E. et al., "An experimental mm–wave receiver system for measuring phase noise due to atmospheric turbulence," *Proceedings of the 25th European Microwave Conference,* Nexus House, pp. 114–119 (1995).

Vilar, E. and Burgueño, A., "Analysis and Modeling of Time Intervals Between Rain Rate Exceedances in the Context of Fade Dynamics," *IEEE Transactions on Communications,* IEEE Communications Society, vol. 39, No. 9, pp. 1306–1312 (Sep. 1991).

Vilar, E. et al., "Angle of Arrival Fluctuations in High and Low Elevation Earth Space Paths," *Fourth International Conference on Antennas and Propagation* (ICAP 85). Electronics Division of the IEE, pp. 83 88 (Apr. 16 19, 1985).

Vilar, E., "Antennas and Propagation: A Telecommunications Systems Subject," *Electronics Division Colloquim on Teaching Antennas and Propagation to Undergraduates,* IEE, pp. 7/1–7/6 (Mar. 8, 1988).

Vilar, E. et al., "CERS★. Millimetere–Wave Beacon Package and Related Payload Doppler Correction Strategies," *Electronics Division Colloquim on CERS–Communication Engineering Research Satellite,* IEE, pp. 10/1–10/10 (Apr. 10, 1984).

Vilar, E. and Moulsley, T.J., "Comment and Reply: Probability Density Function and Amplitude Scintillations," *Electronics Letters,* IEE, vol. 21, No. 14, pp. 620–622 (Jul. 4, 1985).

Vilar, E. et al., "Comparsion of Rainfall Rate Duration Distributions for ILE–IFE and Barcelona," *Electronics Letters,* vol. 28, No. 20, pp. 1922–1924 (Sep. 24, 1992).

Vilar, E., "Depolarization and Field Transmittances in Indoor Communications," *Electronics Letters,* IEE, vol. 27, No. 9. pp. 732–733 (Apr. 25, 1991).

Vilar, E. and Larsen, J. R., "Elevation Dependence of Amplitude Scintillations on Low Elevation Earth Space Paths," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation,* IEE, pp. 150–154 (Apr. 4–7, 1989).

Vilar, E. et al., "Experimental System and Measurements of Transhorizon Signal Levels at 11 Ghz," *18th* European Microwave Conference, Microwave Exhibitions and Publishers Ltd., pp. 429–435 (Sep. 12–15, 1988).

Vilar, E. and Matthews, P.A., "Importance of Amplitude Scintillations in Millimetric Radio Links," *Proceedings of the 4th European Microwave Conference, Microwave Exhibitions and Publishers,* pp. 202–206 (Sep. 10–13, 1974).

Vilar, E. and Haddon, J., "Measurement and Modeling of Scintillation Intensity to Estimate Turbulance Parameters in an Earth Space Path," *IEEE Transactions on Antennas and Propagation,* IEEE Antennas and Propagation Society, vol. AP–32, No. 4, pp. 340–346 (Apr. 1984).

Vilar, E. and Matthews, P. A., "Measurement of Phase Fluctuations on Millimetric Radiowave Propagation," *Electronics Letters,* IEE, vol. 7, No. 18, pp. 566–568 (Sep. 9, 1971).

Vilar, E. and Wan, K. W. , "Narrow and Wide Band Estimates of Field Strenght for Indoor Communications in the Millimetre Band," *Electronics Division Colloquim on Radiocommunications in the Range 30–60 Ghz,* IEE, pp. 5/1–5/8 (Jan. 17, 1991).

Vilar, E. and Faulkner, N. D., "Phase Noise and Frequency Stability Measurements. Numerical Techniques and Limitations," *Electronics Division Colloquim on Low Noise Oscillators and Synthesizer,* IEE, 5 pages (Jan. 23, 1986).

Vilar, E. and Senin, S., "Propagation phase noise identified using 40 Ghz satellite downlink," *Electronics Letters,* IEE, vol. 33, No. 22, pp. 1901–1902 (Oct. 23, 1997).

Vilar, E. et al., "Scattering and Extinction; Dependence Upon Raindrop Size Distribution in Temperate (Barcelona) and Tropical (Belem) Regions," *Tenth International Conference on Antennas and Propagation,* Electronics Division of the IEE, pp. 2.230 2.233 (Apr. 14 17, 1997).

Vilar, E. and Haddon, J., "Scintillation Modeling and Measurement –A Tool for Remote–Sensing Slant Paths," *AGARD Conference Proceedings No. 332: Propagation Aspects of Frequency Sharing, Interference And System Diversity,* AGARD, pp. 27 1 27 13 (Oct. 18 22, 1982).

Vilar, E., "Some Limitations on Digital Transmission Through Turbulent Atmosphere," *International Conference on Satellite Communication Systems Technology,* Electronics Division of the IEE, pp. 169 187 (Apr. 7 10, 1975).

Vilar, E. and Matthews, P. A., "Summary of Scintillation Observations in a 36 Ghz Link Across London," *International Conference on Antennas and Propagation Part 2: Propagation,* IEE, pp. 36–40 (Nov. 28–30, 1978).

Vilar, E. et al., "Wideband Characterization of Scattering Channels," *Tenth International Conference on Antennas and Propagation,* Electronics Division of the IEE, pp. 2.353–2.358 (Apr. 14–17, 1997).

Voltmer, A., "Complete GPS Receiver Fits on Two Chips," *Electronic Design,* Publishing, pp. 50, 52, 54 and 56 (Jul. 6, 1998).

Voltage and Time Resolution in Digitizing Oscilloscopes: Application Note 348, Hewlett Packard, pp. 1 11 (Nov. 1986).

Wan, K. W. et al., "A Novel Approach to the Simultaneous Measurement of Phase and Amplitude Nosies in Oscillator," *Proceedings of the 19th European Microwave Conference,* Microwave Exhibitions and Publishers Ltd., pp. 809–813 (Sep. 4–7, 1989).

Wan, K. W. et al., "Extended Variances and Autoregressive/Moving Average Algorithm for the Measurement and Synthesis of Oscillator Phase Noise," *Proceedings of the 43rd Annual Symposium on Frequency Control,* IEEE, pp. 331–335 (1989).

U.S. Appl. No. 09/525,615, filed Mar. 14, 2000, Sorrells et al.

U.S. Appl. No. 09/632,855, filed Aug. 14, 2000, Sorrells et al.

U.S. Appl. No. 09/632,857, filed Aug. 14, 2000, Sorrells et al.

Wan, K. W. et al., "Wideband Transhorizon Channel Sounder at 11 Ghz," *Electronics Division Colloquim on High Bit Rate UHF/SHF Channel Sounders –Technology and Measurement,* IEE, pp. 3/1–3/5 (Dec. 3, 1993).

Wang, H., "A 1–V Multigahertz RF Mixer Core in 0.5 –μm CMOS," *IEEE Journal of Solid–State Circuits,* IEEE Solid–State Circuits Society, vol. 33, No. 12, pp. 2265–2267 (Dec. 1998).

Watson, A.W.D. et al., "Digital Conversion and Signal Processing for High Performance Communications Receivers," *Digital Processing of Signals in Communications,* Institution of Electronic and Radio Engineers, pp. 367–373 (Apr. 22nd 26th, 1985).

Weast, R. C. et al. (Ed.), *Handbook of Mathematical Tables,* Second Edition, The Chemical Rubber Co., pp. 480–485 (1964).

Wiley, R. G., "Approximate FM Demodulation Using Zero Crossings," *IEEE Transactions on Communications,* IEEE, vol. COM–29, No. 7, pp. 1061–1065 (Jul. 1981).

Worthman, W., "Convergence. . . Again," *RF Design,* Primedia, p. 102 (Mar. 1999).

Young, I. A. and Hodges, D. A., "MOS Switched–Capacitor Analog Sampled–Data Direct–Form Recursive Filters," *IEEE Journal of Solid–State Cicuits,* IEEE, vol. SC–14, No. 6, pp. 1020–1033 (Dec. 1979).

Translation of Specification and Claims of FR Patent No. 2245130, 3 pages.

Fest, Jean–Pierre, "Le Convertissur A/N Revolutions Le Recepteur Radio," *Electronique,* JMJ (Publisher), No. 54, pp. 40–42 (Dec. 1995).

Translation of DE Patent No. 35 41 031 A1, 22 pages.

Translation of EP Patent No. 0 732 803 A1, 9 pages.

Fest, Jean–Pierre, "The A/D Converter Revolutionizes the Radio Receiver,"*Electronique,* JMJ (Publisher), No. 54, 3 pages (Dec. 1995). (Translation of Doc. AQ50).

Translation of German Patent No. DE 197 35 798 C1, 8 pages.

Miki, S. and Nagahama, R., *Modulation System II,* Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146–154 (Apr. 30, 1956).

Miki, S. and Nagahama, R., *Modulation System II,* Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146–149 (Apr. 30, 1956). (Partial Translation of Doc. AQ51).
Rabiner, L. R. and Gold, B., *Theory And Application Of Digital Signal Processing,* Prentice–Hall, Inc., pp. xiii–xii and 40–46 (1975).
English–language Abstract of Japanese Patent Publcation No. 08–032556, from http://www1.ipdl.jpo.go.jp, 2 Pages (Feb. 2, 1996 –Date of publication of application).
English–language Abstract of Japanese Patent Publication No. 08–139524, from http://www1.ipdl.jpo.go.jp, 2 Pages (May 31, 1996 –Date of publication of application).
English–language Abstract of Japanese Patent Publication No. 59–144249, from http://www1.ipdl.jpo.go.jp, 2 Pages (Aug. 18, 1984 –Date of publication of application).
English language Abstract of Japanese Patent Publication No. 63–054002, from http://www1.ipdl.jpo.go.jp, 2 Pages (Mar. 8, 1988 –Date of publcation of application).
English–language Abstract of Japanese of Patent Publication No. 06–237276, from http://www.1ipdl.jpo.go.jp, 2 Pages (Aug. 23, 1994 –Date of publication of application).
English–langauge Abstract of Japanese Patent Publication No. 08–023359, from http://www1.ipdl.jpo.go.jp, 2 Pages (Jan. 23, 1996 –Date of publication of application).
Translation of Japanese Patent Publication No. 47–2314, 7 pages.
Partial Translation of Japanese Patent Publication No. 58–79003, 3 pages.
English –language Abstract of Japanese Patent Publication No. 58–133004, from http://www1.ipdl.jpo.go.jp, 2 Pages (Aug. 8, 1993 –Date of publication of application).
English–language Abstract of Japanese Patent Publication No. 60–058705, from http://www1.ipdl.jpo.go.jp, 2 Pages (Apr. 4, 1985 –Date of pubication of application).
English–language Abstract of Japanese Patent Publication No. 04–123614, from http://www1.ipdl.jpo.go.jp, 2 Pages (Apr. 23, 1992 –Date of Publication of application).
English–language Abstract of Japanese Patent Publication No. 04–127601, from http://www1.ipdl.jpo.go.jp, 2 Pages (Apr. 28, 1992 –Date of publication of application).
English–language Abstract of Japanese Patent Publication No. 05–175730, from http://www1.pdl.jpo.go.jp, 2 Pages (Jul. 13, 1993 –Date of publication of application).
English–language Abstract of Japanese Patent Publication No. 05–175734, from http://www1.ipdl.jpo.go.jp, 2 Pages (Jul. 13, 1993 –Date of publication of application).
English–language Abstract of Japannese Patent Publication No. 07 154344, from http://www1.ipdl.jpo.go.jp, 2 Pages (Jun. 16, 1995 Date of Publication of application).
English–language Abstract of Japanese Patent Publication No. 07–307620, from http://www1.pdl.jpo.go.jp, 2 Pages (Nov. 21, 1995 –Date of publication of application).
Oppenheim, A. V. and Schafer, R. W., *Digital Signal Processing,* Prentice–Hall, pp. vii–x, 6–35, 45–78, 87–121 and 136–165 (1975).
English–language Abstract of Japanese Patent Publication No. 55–066057, from http://www1.ipdl.jpo.go.jp, 1 Page (May 19, 1980 –Date of Publication of application).
English–language Abstract of Japanese Patent Publication No. 63 065587, from http://www1.ipdl.jpo.go.jp, 1 Page (Mar. 24, 1988 –Date of publication of application).
English–language Abstract of Japanese Patent Publication No. 63–153691, from http://www1.ipdl.jpo.go.jp, 1 Page (Jun. 27, 1988 –Date of publication of application).
Translation of Japanese Patent Publication No. 60–130203, 3 pages (Jul. 11, 1985–Date of publication of application).
Razavi, B., "A 900–MHz/1.8–Ghz CMOS Transmitter for Dual–Band Applications," *Symposium on VLSI Circuits Digest of Technical Papers,* Papers, IEEE, pp. 128–131 (1998).
Ritter, G. M., "SDA, A New Solution for Transceivers," *16th European Microwave Conference,* Microwave Exhibitions and Publishers, pp. 729–733 (Sep. 8, 1986).
Dialog File 351 (Derwent WPI) English Language Patent Abstract for FR 2 669 787, 1 page (May 29, 1992–Date of publication of application).
Akos, D. M. et al., "Direct Bandpass Sampling of Multiple Distinct RF Signals," *IEEE Transactions on Communications,* IEEE, vol. 47, No. 7, pp. 983–988 (Jul. 1999).
Patel, M. et al., "Bandpass Sampling for Software Radio Receivers, and the Effect of Oversampling on Aperture Jitter," *VTC 2002,* IEEE, pp. 1901–1905 (2002).
English–language Abstract of Japanese Patent Publication No. 61–030821, 1 Page (Feb. 13, 1986–Date of publication of application).
English–language Abstract of Japanese Patent Publication No. 05–327356, 1 Page (Dec. 10, 1993 –Date of publication of application).
Tayloe, D., "A Low–noise, High–performance Zero IF Quadrature Detector/Preamplifier," *RF Design,* Primedia Business Magazines & Media, Inc., pp. 58, 60, 62 and 69 (Mar. 2003).
Dines, J. A. B., "Smart Pixel Optoelectronic Receiver Based on a Charge Sensitive Amplifier Design," *IEEE Journal of Selected Topics in Quantum Electronics,* IEEE, vol. 2, No. 1, pp. 117–120 (Apr. 1996).
Simioni, A. et al., "A Digital Camera for Machine Vision," *20th International Conference on Industrial Electronics, Control and Instrumentation,* , IEEE, pp. 879–883 (Sep. 1994).
Stewart, R. W. and Pfann, E., "Oversampling and sigma–delta strategies for data conversion," *Electronics & Communication Engineering Journal,* IEEE, pp. 37–47 (Feb. 1998).
Rudell, J. C. et al. "A 1.9Ghz Wide–Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid–State Circuits,* IEEE, vol. 32, No. 12, pp. 2071–2088 (Dec. 1997).
English–language Abstract of Japanese Patent Publication No. 09–036664, from http://www1.ipdl.jpo.go.jp, 2 Pages (Feb. 7, 1997 –Date of publication of application).
Simoni, A. et al., "A Single–Chip Optical Sensor with Analog Memory for Motion Detection," *IEEE Journal of Solid–State Circuits,* IEEE, vol. 30, No. 7, pp. 800–806 (Jul. 1995).
Deboo, Gordon J., *Intergrated Circuits and Semiconductor Devices,* 2nd Edition, McGraw–Hill, Inc., pp. 41–45 (1977).

* cited by examiner

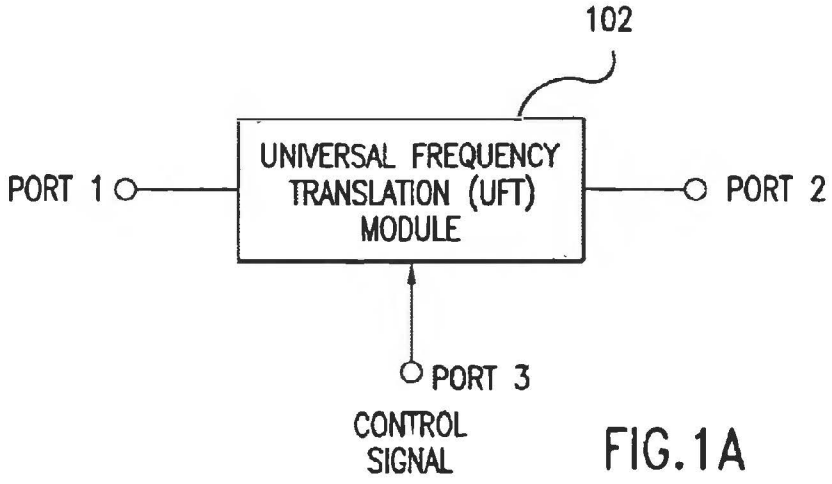

102
UNIVERSAL FREQUENCY TRANSLATION (UFT) MODULE
PORT 1
PORT 2
PORT 3
CONTROL SIGNAL

FIG.1A

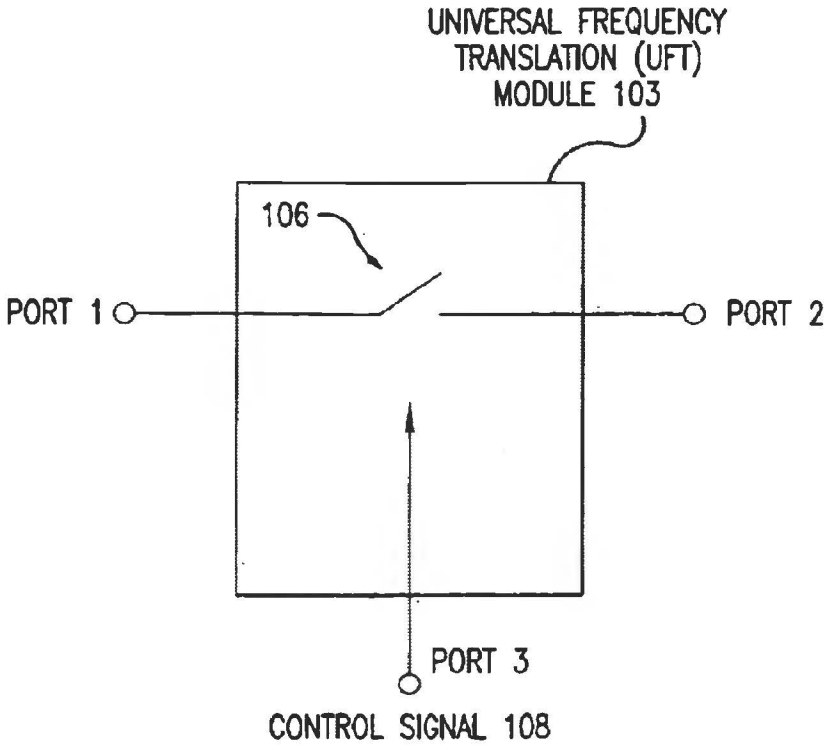

UNIVERSAL FREQUENCY TRANSLATION (UFT) MODULE 103
106
PORT 1
PORT 2
PORT 3
CONTROL SIGNAL 108

FIG.1B

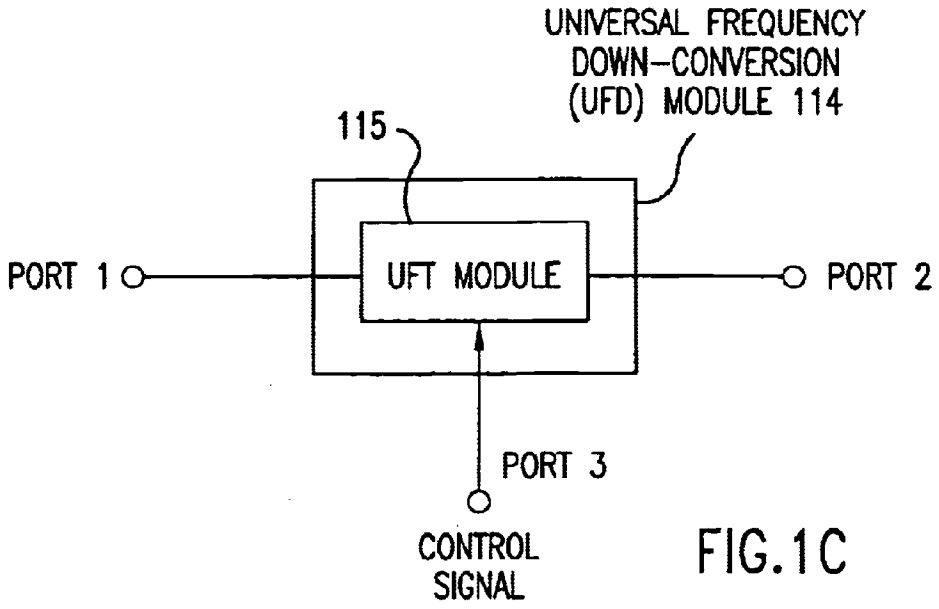

UNIVERSAL FREQUENCY
DOWN-CONVERSION
(UFD) MODULE 114
115
UFT MODULE
PORT 1
PORT 2
PORT 3
CONTROL
SIGNAL

FIG.1C

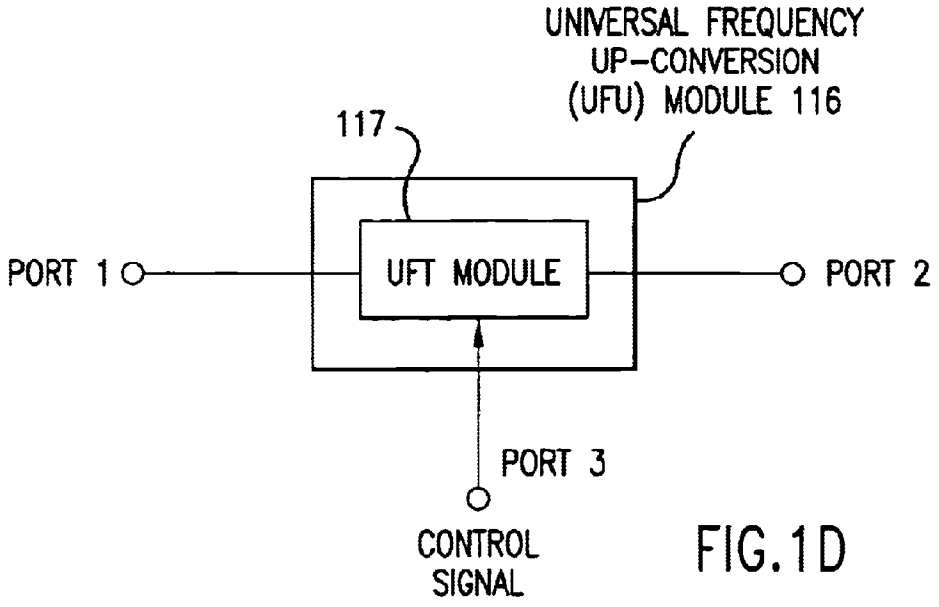

UNIVERSAL FREQUENCY
UP-CONVERSION
(UFU) MODULE 116
117
UFT MODULE
PORT 1
PORT 2
PORT 3
CONTROL
SIGNAL

FIG.1D

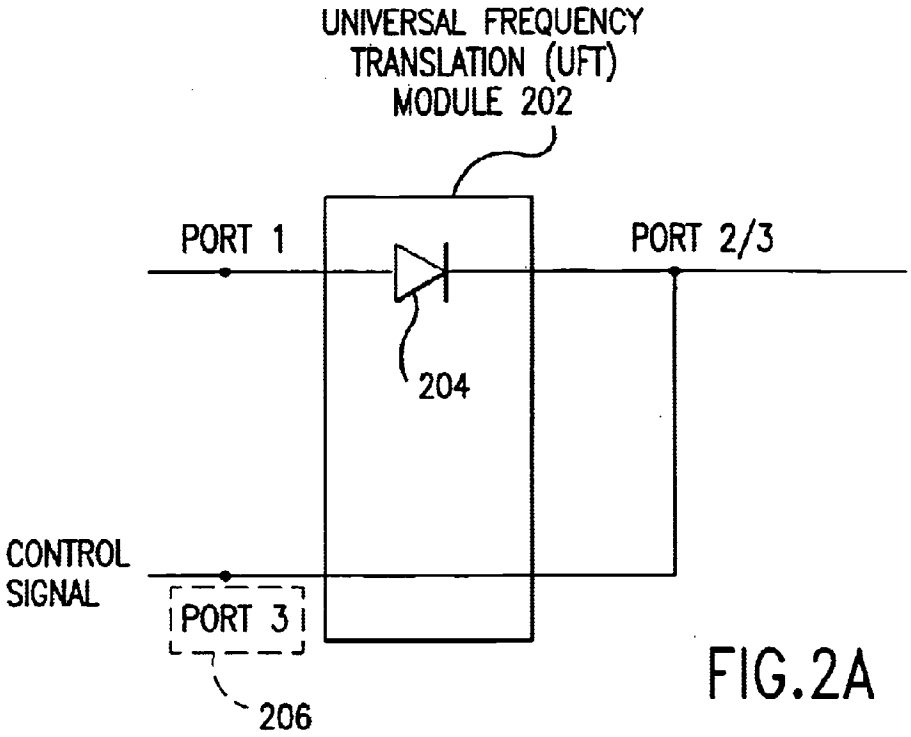

UNIVERSAL FREQUENCY
TRANSLATION (UFT)
MODULE 202
PORT 1
PORT 2/3
204
CONTROL
SIGNAL
PORT 3
206

FIG.2A

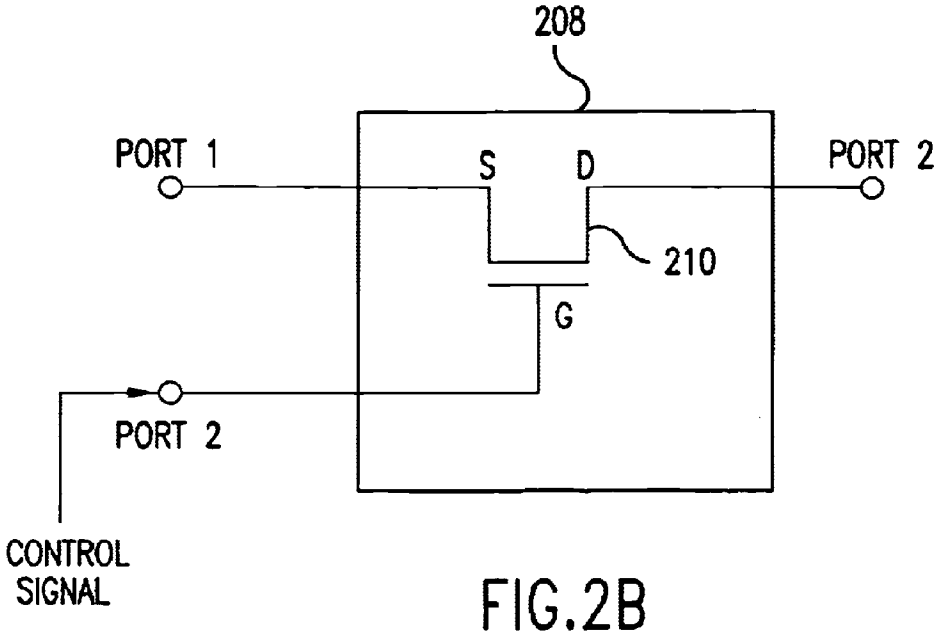

208
PORT 1
S
D
PORT 2
210
G
PORT 2
CONTROL
SIGNAL

FIG.2B

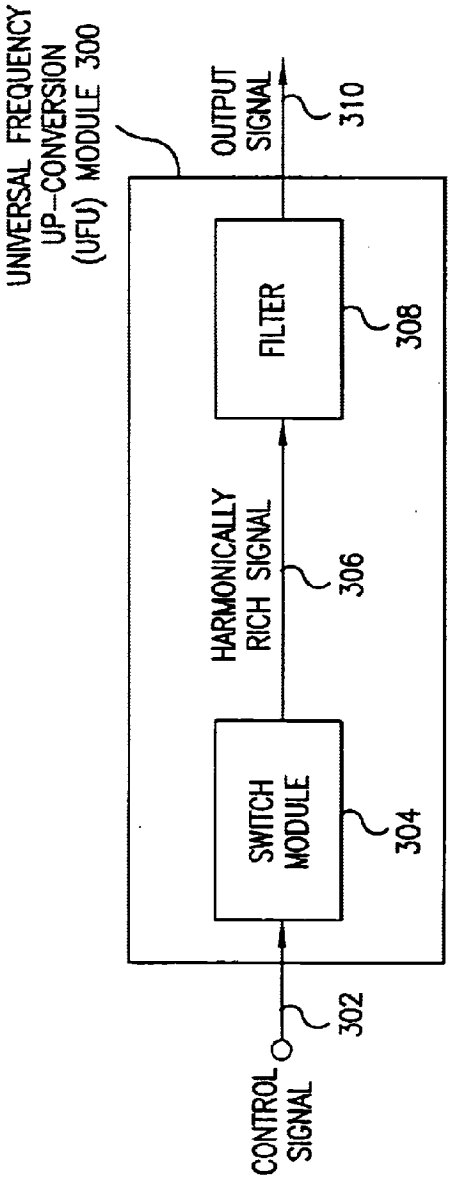

UNIVERSAL FREQUENCY UP-CONVERSION (UFU) MODULE 300
OUTPUT SIGNAL
310
FILTER
308
HARMONICALLY RICH SIGNAL
306
SWITCH MODULE
304
CONTROL SIGNAL
302

FIG.3

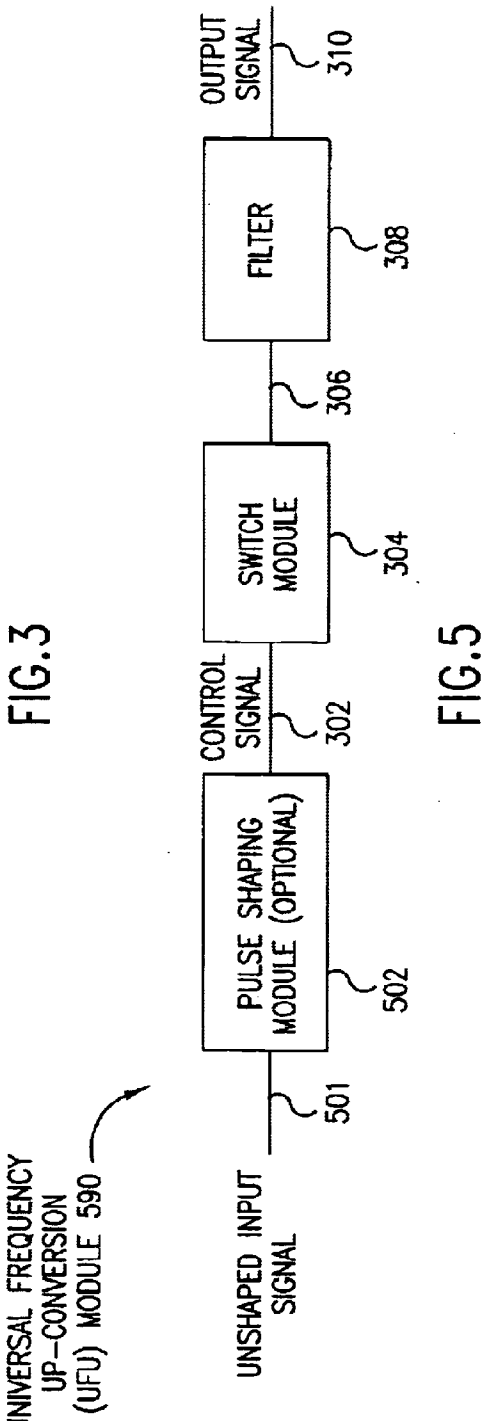

OUTPUT SIGNAL
310
FILTER
308
306
SWITCH MODULE
304
CONTROL SIGNAL
302
PULSE SHAPING MODULE (OPTIONAL)
502
501
UNSHAPED INPUT SIGNAL
UNIVERSAL FREQUENCY UP-CONVERSION (UFU) MODULE 590

FIG.5

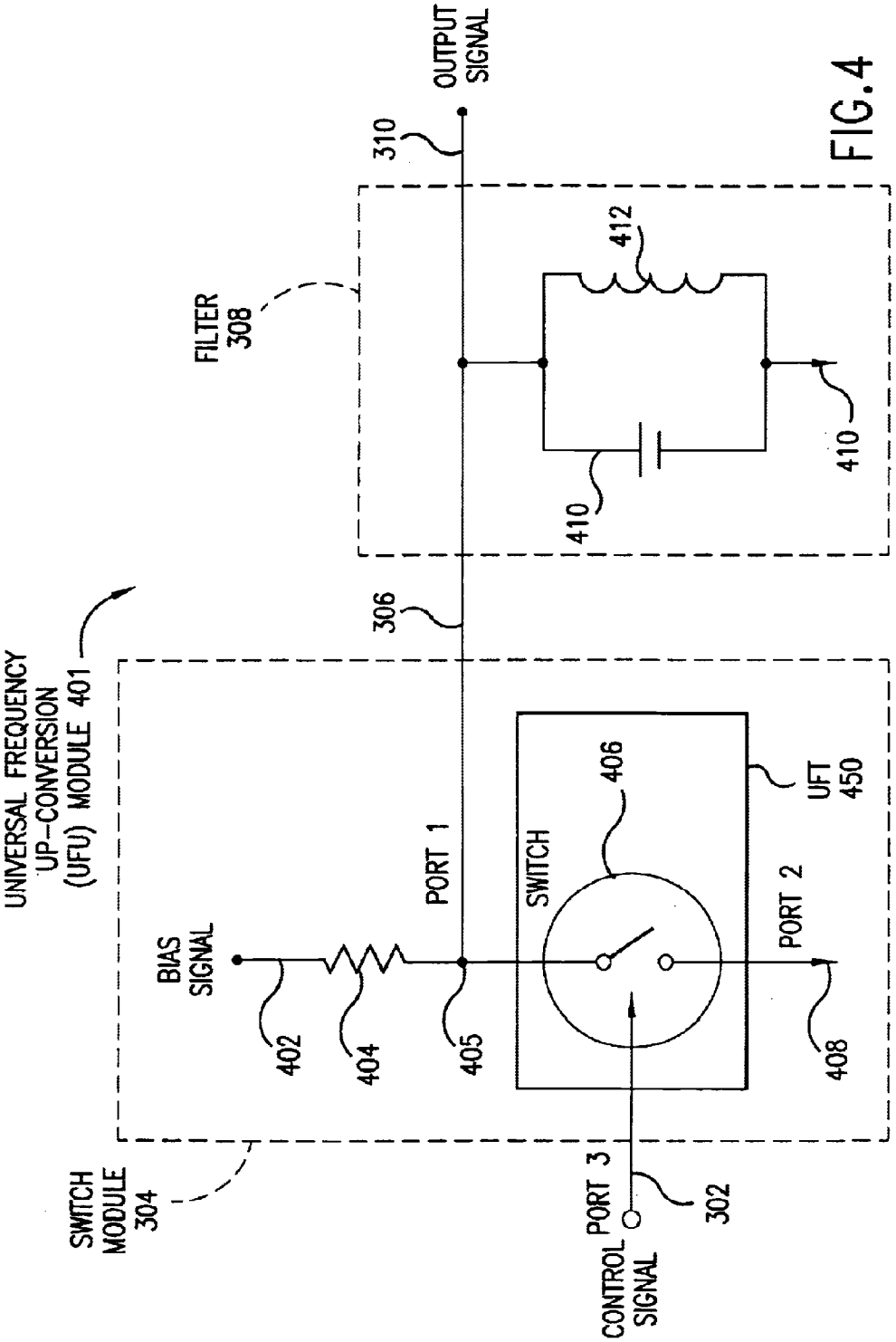

OUTPUT SIGNAL
310
FILTER 308
412
410
410
306
UNIVERSAL FREQUENCY UP-CONVERSION (UFU) MODULE 401
BIAS SIGNAL
402
404
405
PORT 1
SWITCH
406
PORT 2
UFT 450
408
SWITCH MODULE 304
PORT 3
302
CONTROL SIGNAL

FIG. 4

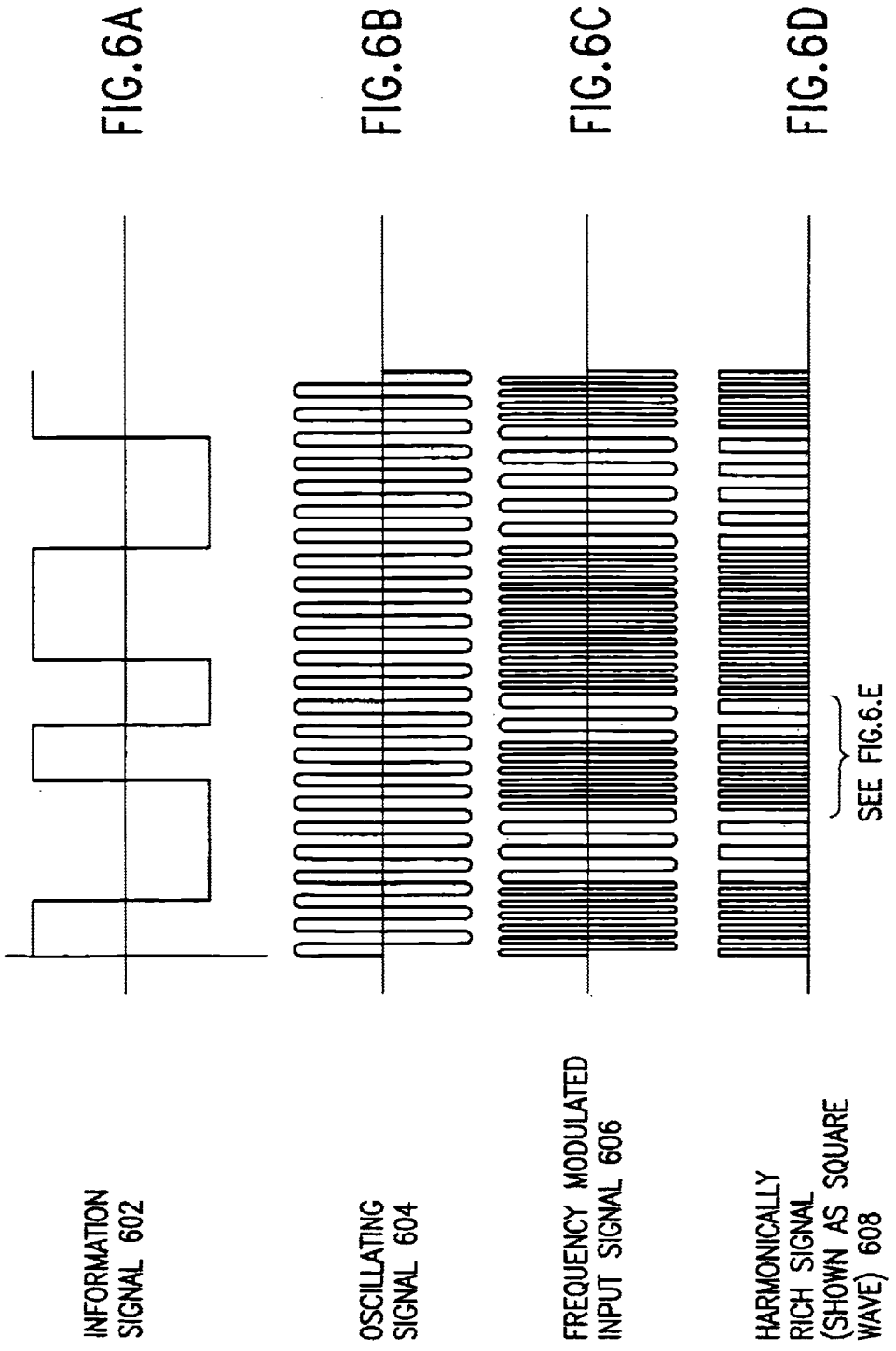
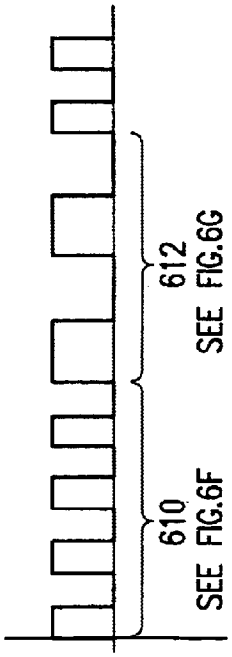

FIG.6A
FIG.6B
FIG.6C
FIG.6D
SEE FIG.6.E
INFORMATION SIGNAL 602
OSCILLATING SIGNAL 604
FREQUENCY MODULATED INPUT SIGNAL 606
HARMONICALLY RICH SIGNAL (SHOWN AS SQUARE WAVE) 608

FIG.6E



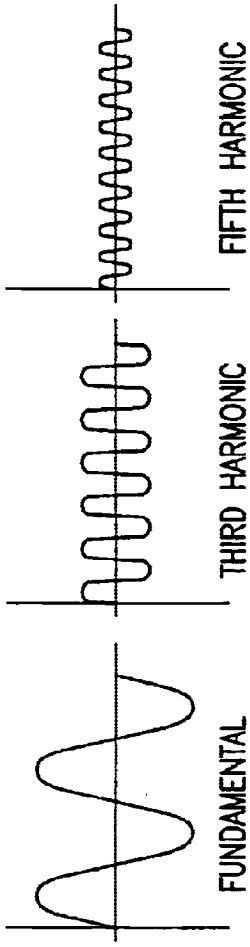
EXPANDED VIEW OF HARMONICALLY RICH SIGNAL 608

FIG.6F



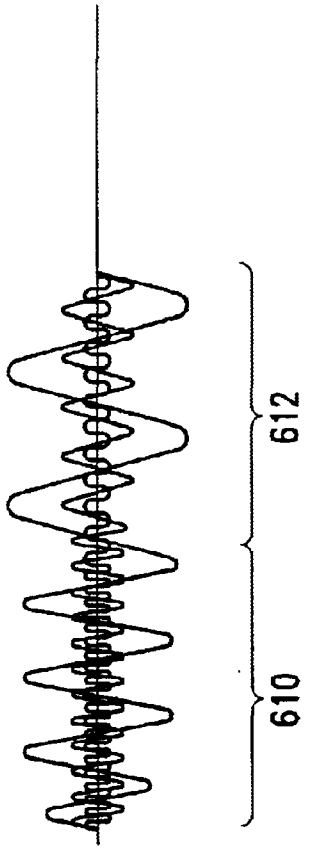
HARMONICS OF SIGNAL 610 (SHOWN SEPARATELY)

FIG.6G



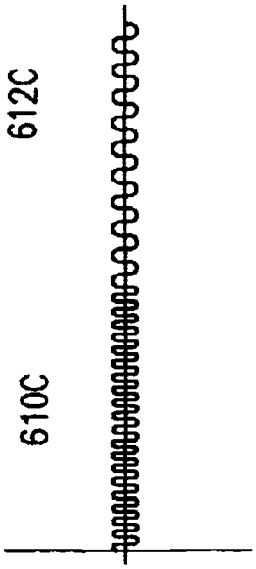
HARMONICS OF SIGNAL 612 (SHOWN SEPARATELY)

FIG.6H



HARMONICS OF SIGNALS 610 AND 612 (SHOWN SIMULTANEOUSLY BUT NOT SUMMED)

FIG.6I



FILTERED OUTPUT SIGNAL 614

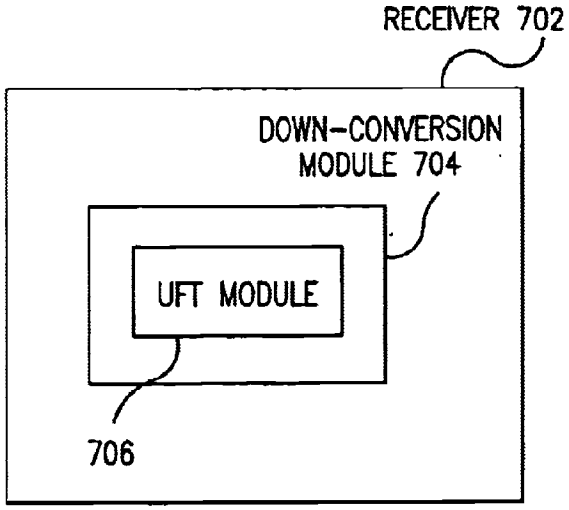


FIG.7

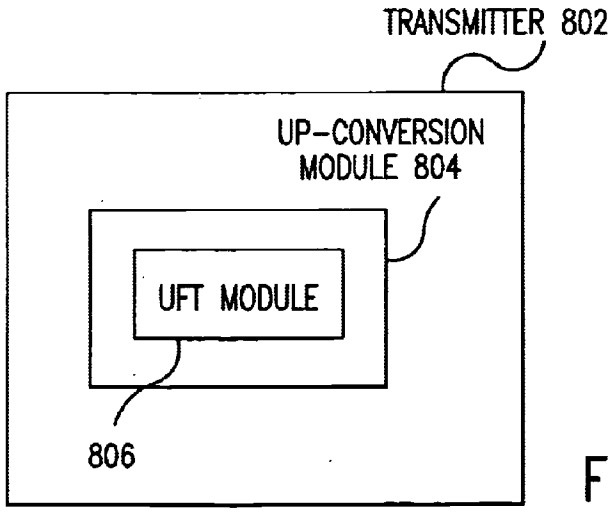


FIG.8

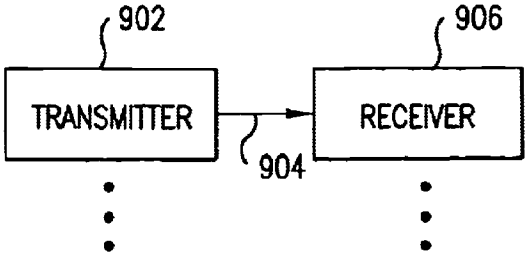


FIG.9

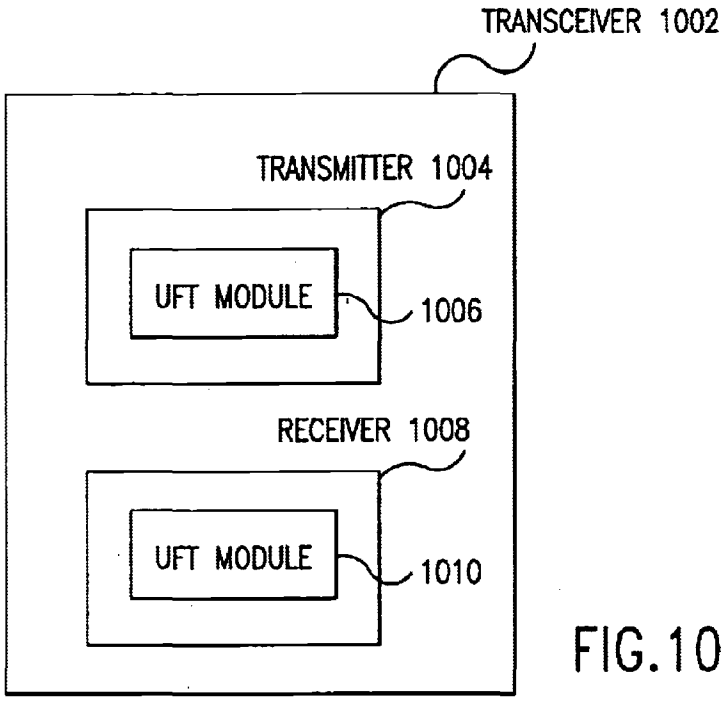

TRANSCEIVER 1002
TRANSMITTER 1004
UFT MODULE
1006
RECEIVER 1008
UFT MODULE
1010

FIG.10

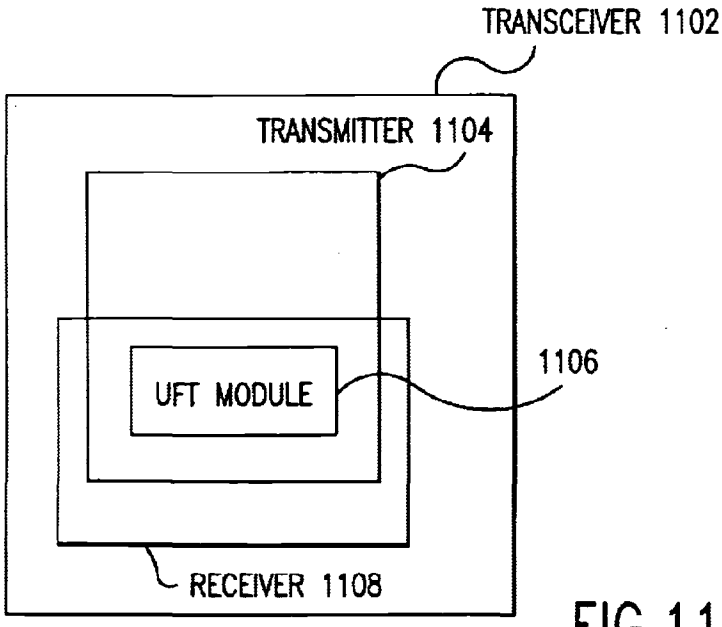

TRANSCEIVER 1102
TRANSMITTER 1104
UFT MODULE
1106
RECEIVER 1108

FIG.11

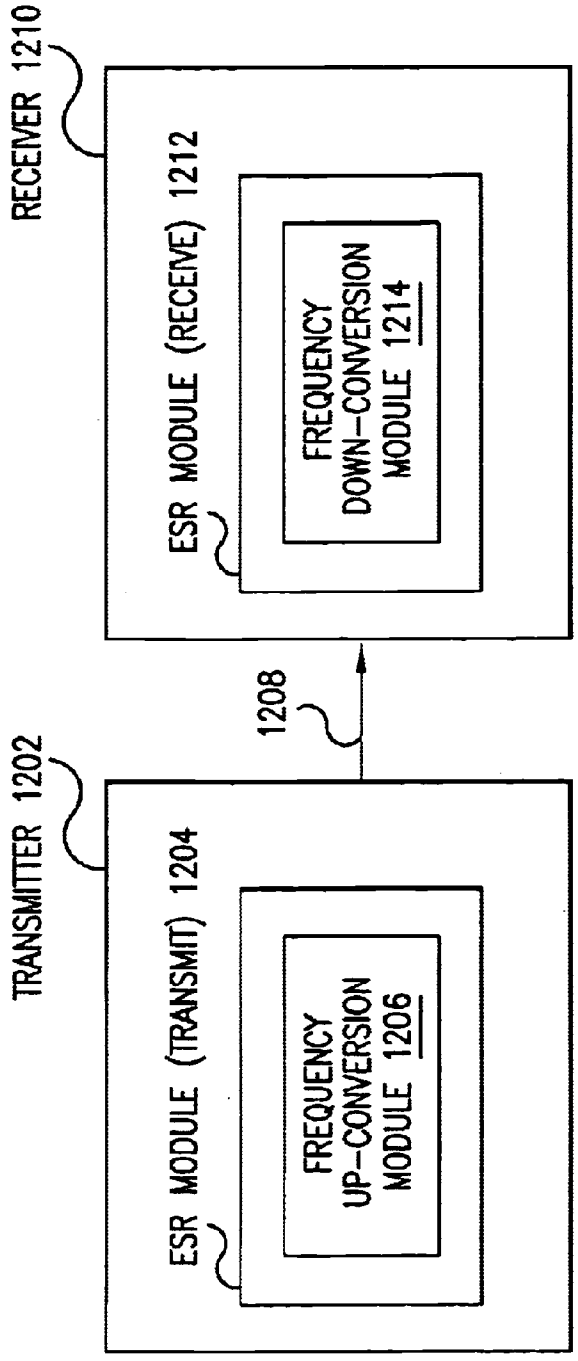

RECEIVER 1210
ESR MODULE (RECEIVE) 1212
FREQUENCY DOWN-CONVERSION MODULE 1214
1208
TRANSMITTER 1202
ESR MODULE (TRANSMIT) 1204
FREQUENCY UP-CONVERSION MODULE 1206

FIG.12

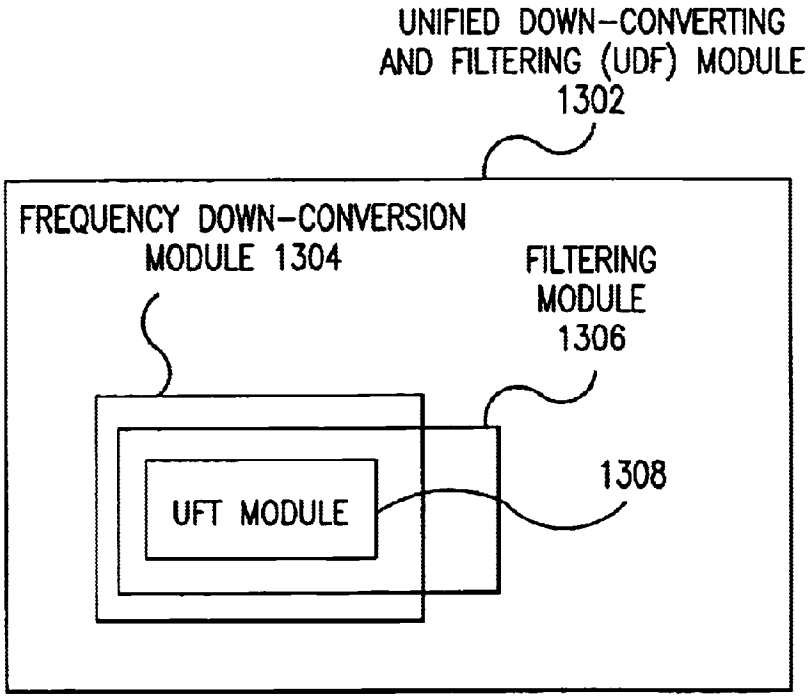

UNIFIED DOWN-CONVERTING
AND FILTERING (UDF) MODULE
1302
FREQUENCY DOWN-CONVERSION
MODULE 1304
FILTERING
MODULE
1306
1308
UFT MODULE

FIG.13

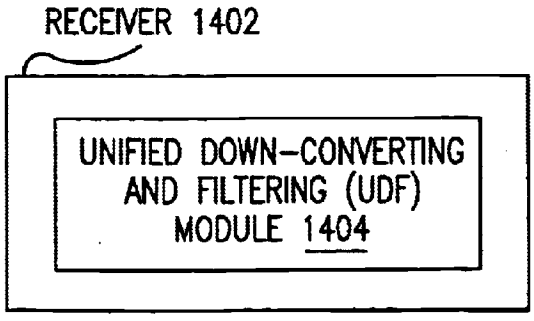

RECEIVER 1402
UNIFIED DOWN-CONVERTING
AND FILTERING (UDF)
MODULE 1404

FIG.14

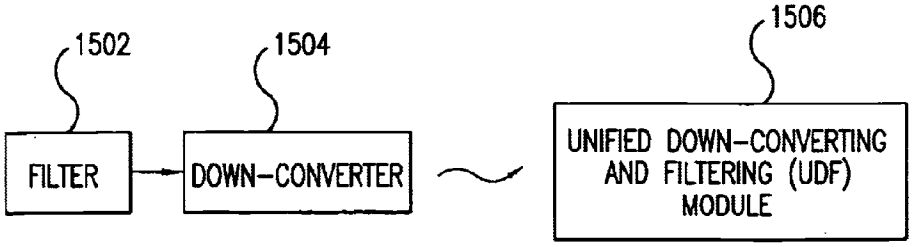


FIG.15A

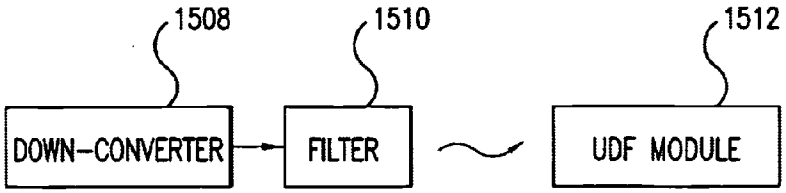


FIG.15B

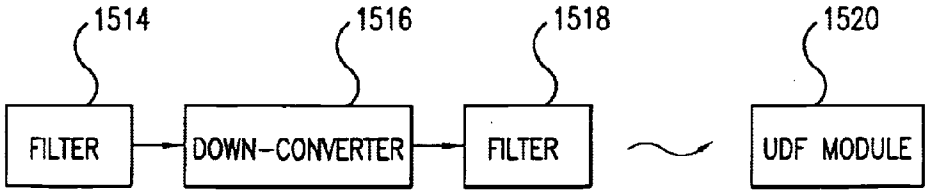


FIG.15C

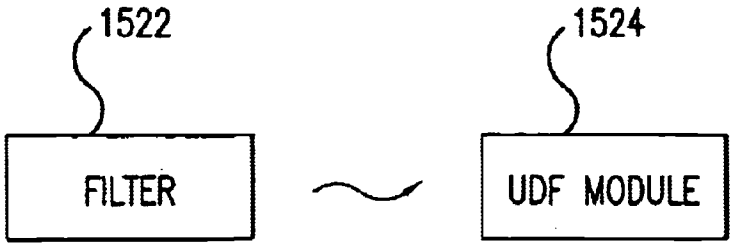


FIG.15D

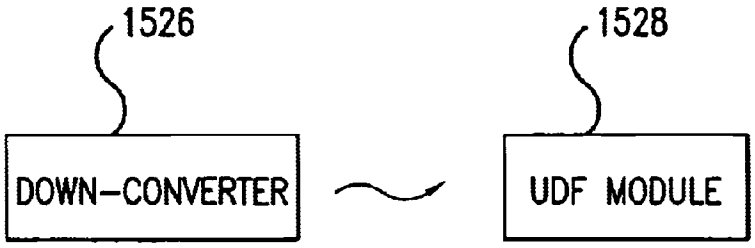


FIG.15E

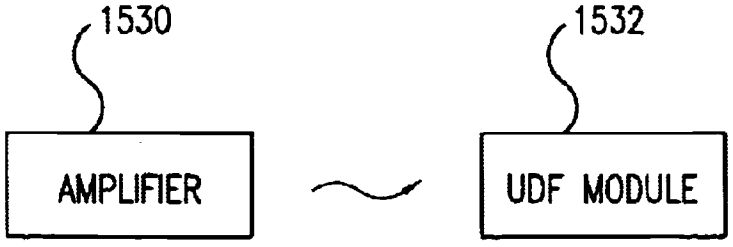


FIG.15F

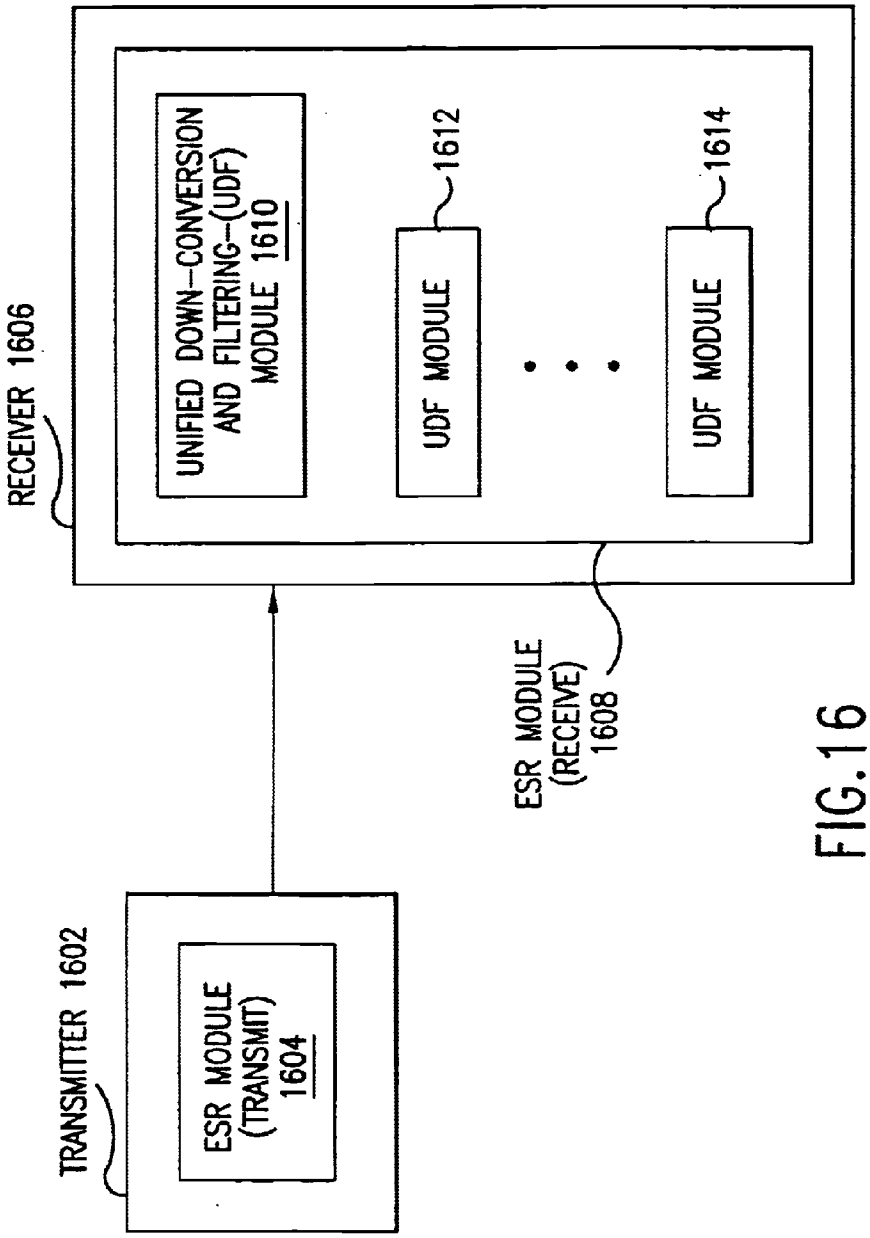

RECEIVER 1606
UNIFIED DOWN-CONVERSION AND FILTERING-(UDF) MODULE 1610
UDF MODULE
1612
UDF MODULE
1614
ESR MODULE (RECEIVE) 1608
TRANSMITTER 1602
ESR MODULE (TRANSMIT) 1604

FIG.16

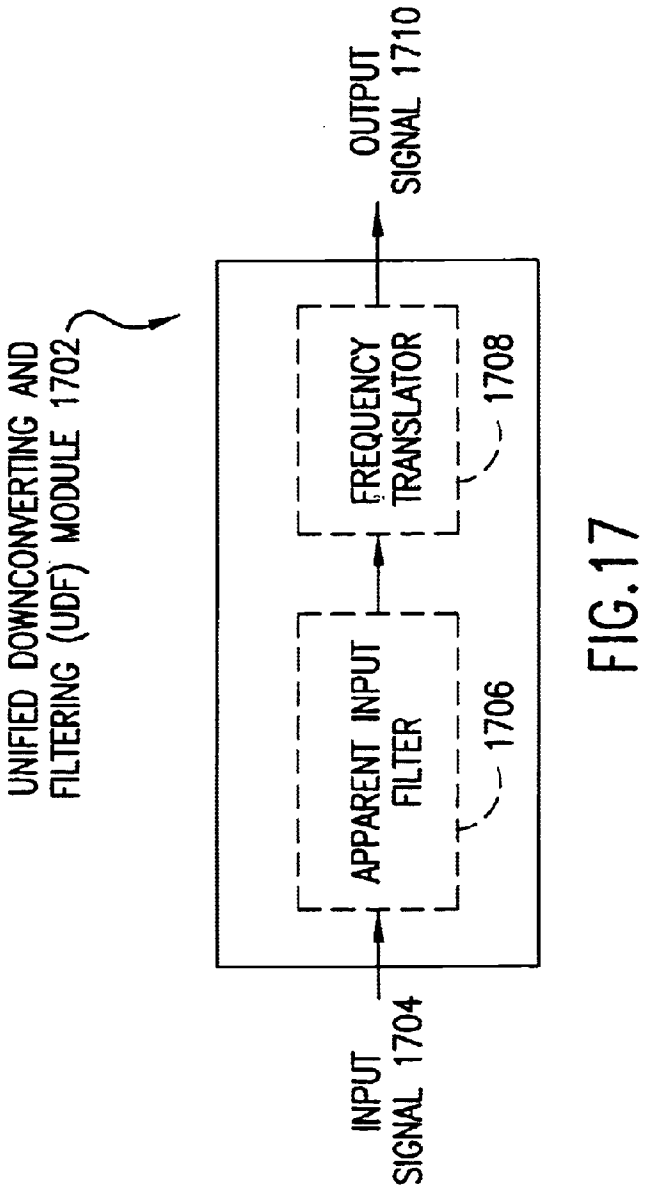

UNIFIED DOWNCONVERTING AND FILTERING (UDF) MODULE 1702
INPUT SIGNAL 1704
APPARENT INPUT FILTER
1706
FREQUENCY TRANSLATOR
1708
OUTPUT SIGNAL 1710

FIG.17

1802

TIME NODE	t-1 (RISING EDGE OF Φ_1)		t-1 (RISING EDGE OF Φ_2)		t (RISING EDGE OF Φ_1)		t (RISING EDGE OF Φ_2)		t+1 (RISING EDGE OF Φ_1)	
1902	VI_{t-1}	1804	VI_{t-1}	1808	VI_t	1816	VI_t	1826	VI_{t+1}	1838
1904	—		VI_{t-1}	1810	VI_{t-1}	1818	VI_t	1828	VI_t	1840
1906	VO_{t-1}	1806	VO_{t-1}	1812	VO_t	1820	VO_t	1830	VO_{t+1}	1842
1908	—		VO_{t-1}	1814	VO_{t-1}	1822	VO_t	1832	VO_t	1844
1910	—	1807	—		VO_{t-1}	1824	VO_{t-1}	1834	VO_t	1846
1912	—		—	1815	—		VO_{t-1}	1836	VO_{t-1}	1848
1918	—		—		—		—		VI_{t^-} 0.1 * VO_F 0.8 * VO_{t-1}	1850

FIG. 18

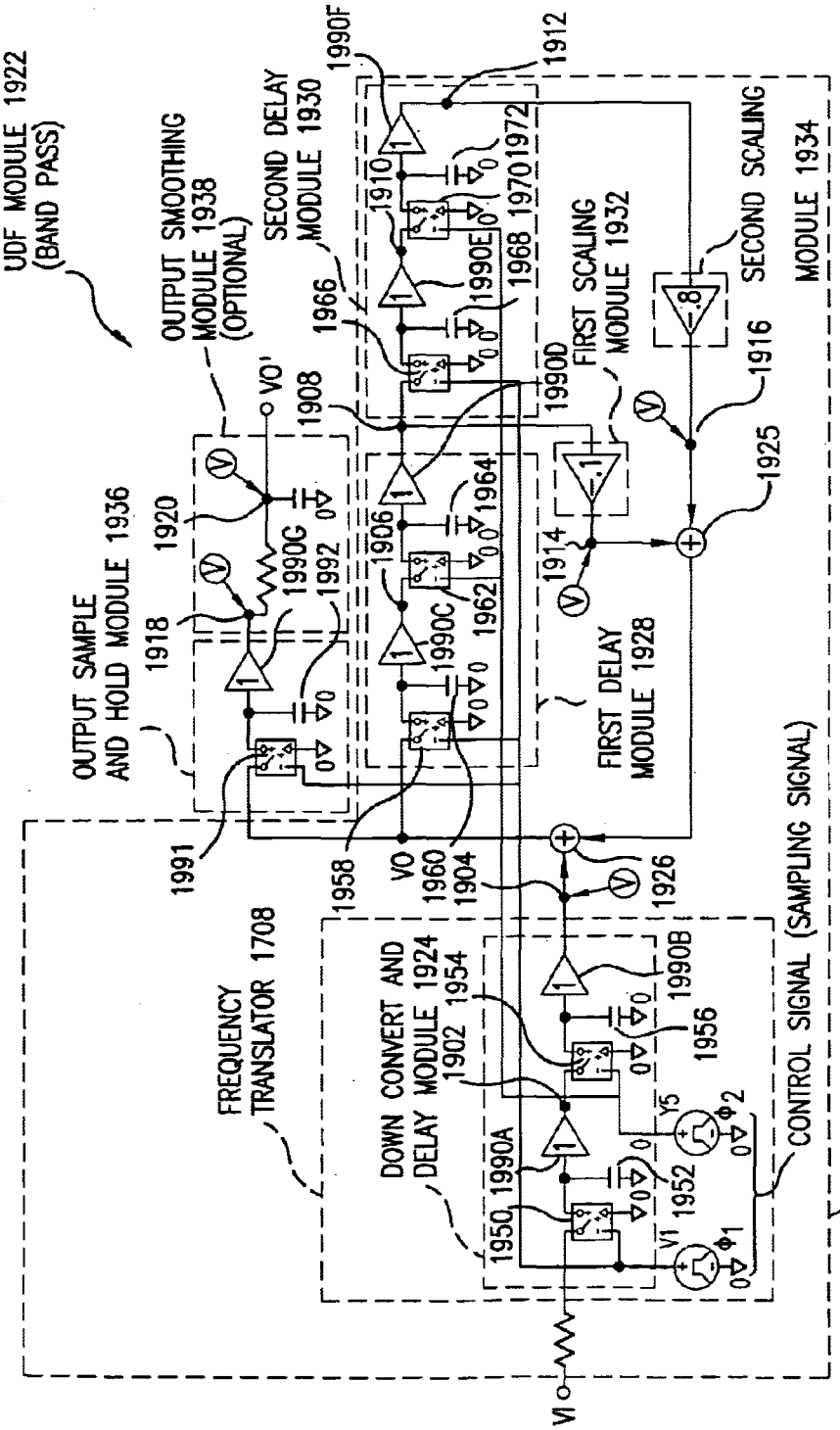

UDF MODULE 1922
(BAND PASS)
OUTPUT SMOOTHING
MODULE 1938
(OPTIONAL)
SECOND DELAY
MODULE 1930
FIRST SCALING
MODULE 1932
SECOND SCALING
MODULE 1934
OUTPUT SAMPLE
AND HOLD MODULE 1936
FIRST DELAY
MODULE 1928
FREQUENCY
TRANSLATOR 1708
DOWN CONVERT AND
DELAY MODULE 1924
CONTROL SIGNAL (SAMPLING SIGNAL)
INPUT FILTER 1706
VO'
VO
VI
1908
1910
1912
1914
1916
1918
1920
1925
1926
1958
1960
1962
1964
1966
1968
1970
1972
1902
1904
1906
1950
1952
1954
1956
1990A
1990B
1990C
1990D
1990E
1990F
1991
1992
Y5
Y1
Φ1
Φ2
.8
-.1

FIG. 19

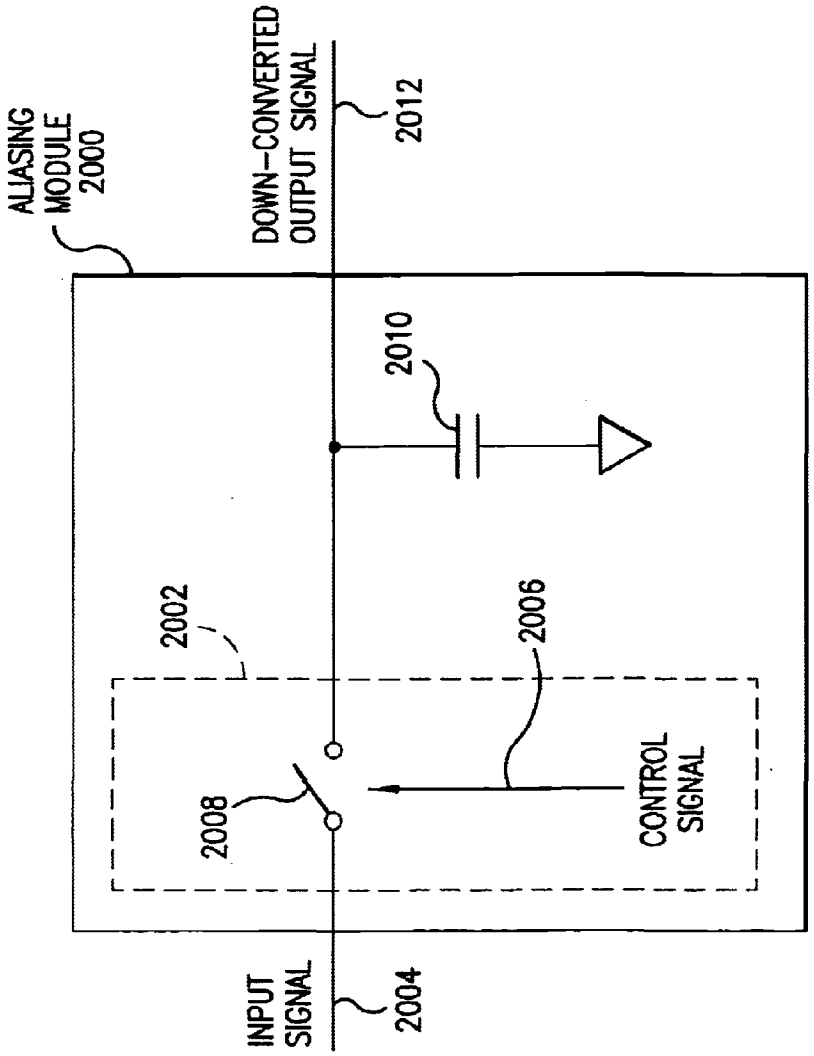

ALIASING MODULE 2000
DOWN-CONVERTED OUTPUT SIGNAL
2012
2010
2002
2006
2008
CONTROL SIGNAL
INPUT SIGNAL
2004

FIG.20A

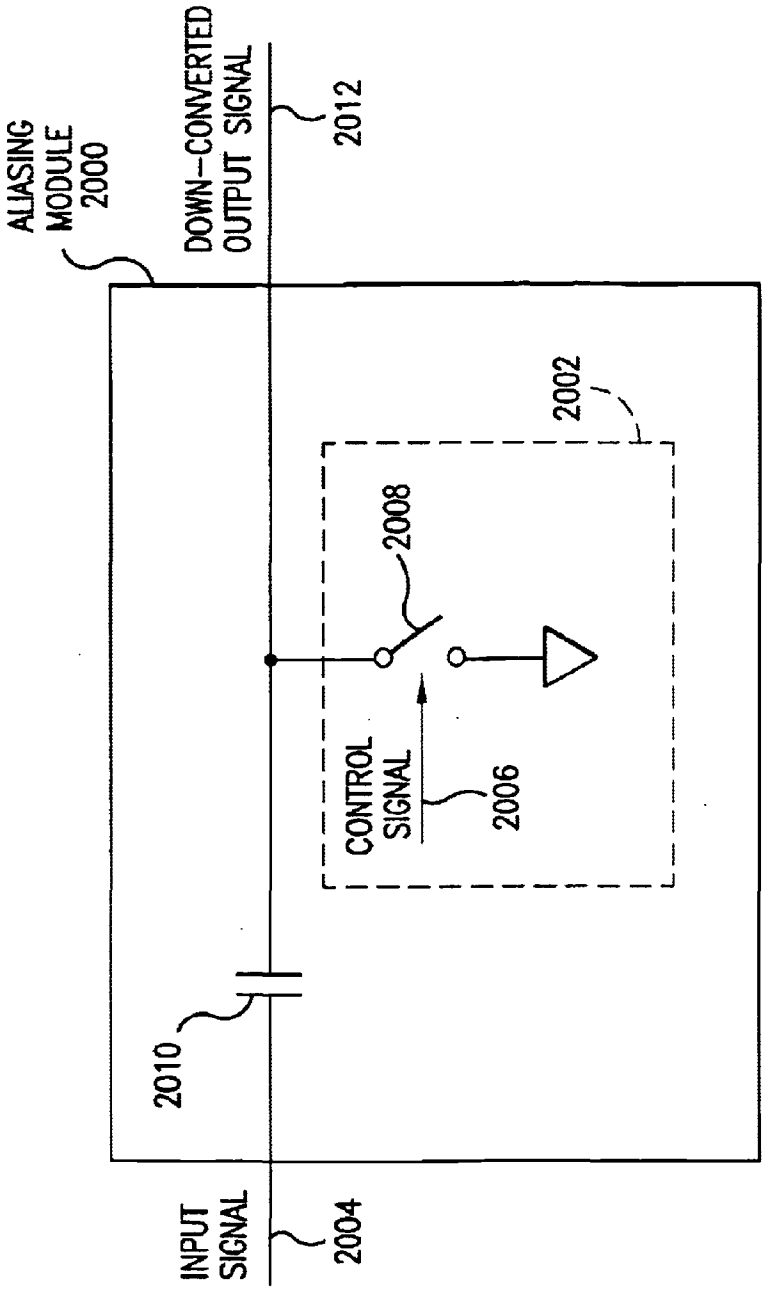

ALIASING MODULE 2000
DOWN-CONVERTED OUTPUT SIGNAL
2012
2002
2008
CONTROL SIGNAL
2006
2010
INPUT SIGNAL
2004

FIG.20A-1

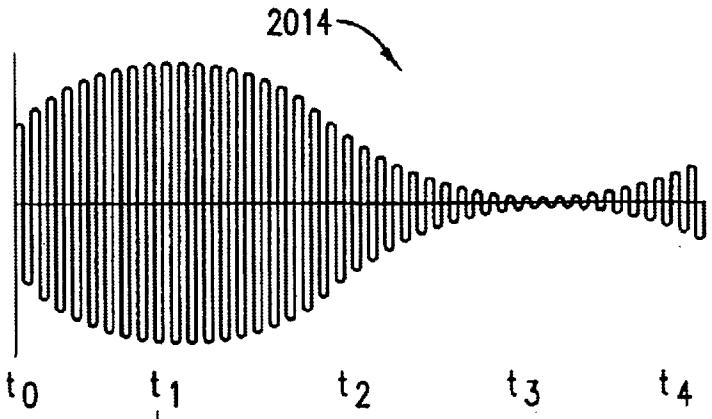


FIG.20B

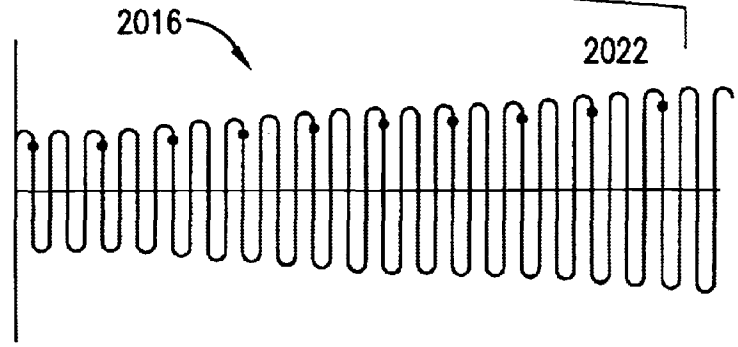


FIG.20C

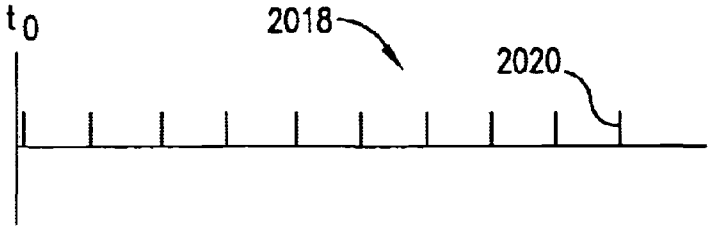


FIG.20D

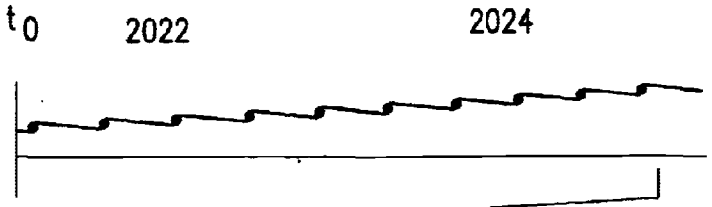


FIG.20E



FIG.20F

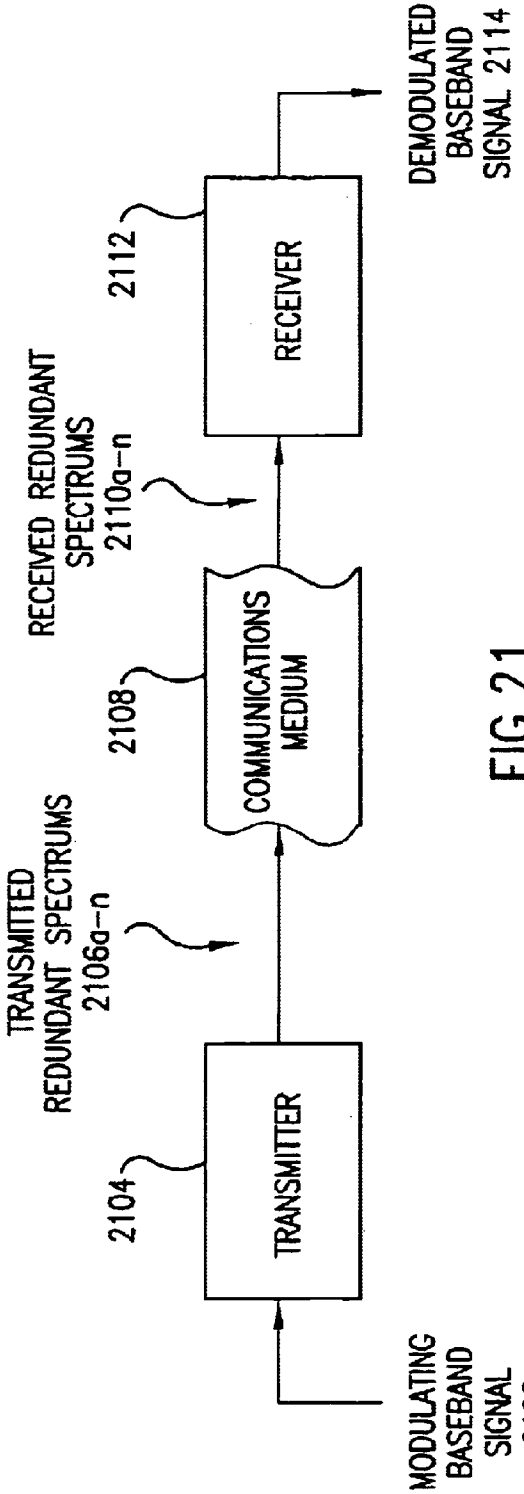

MODULATING BASEBAND SIGNAL 2102
2104
TRANSMITTER
TRANSMITTED REDUNDANT SPECTRUMS 2106a-n
2108
COMMUNICATIONS MEDIUM
RECEIVED REDUNDANT SPECTRUMS 2110a-n
2112
RECEIVER
DEMODULATED BASEBAND SIGNAL 2114

FIG.21

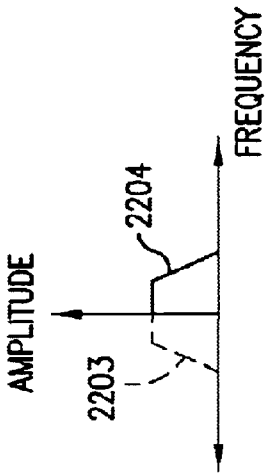


FIG.22B

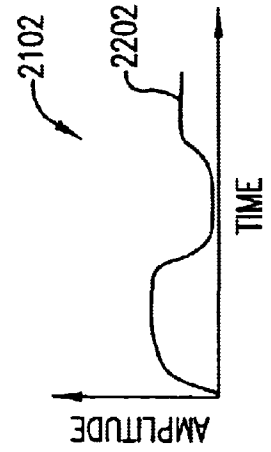


FIG.22A

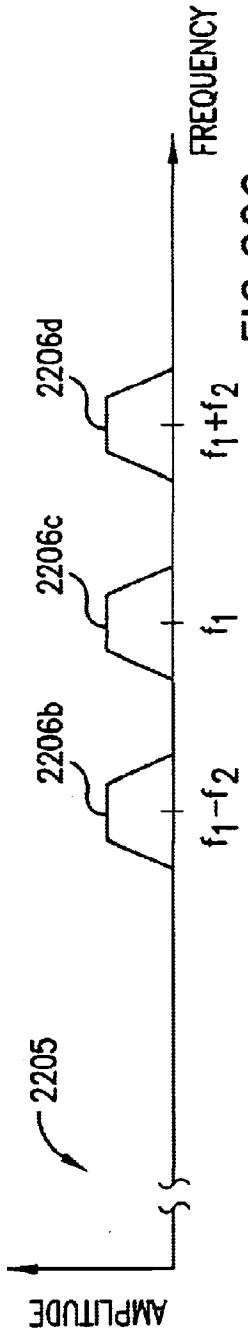


FIG.22C

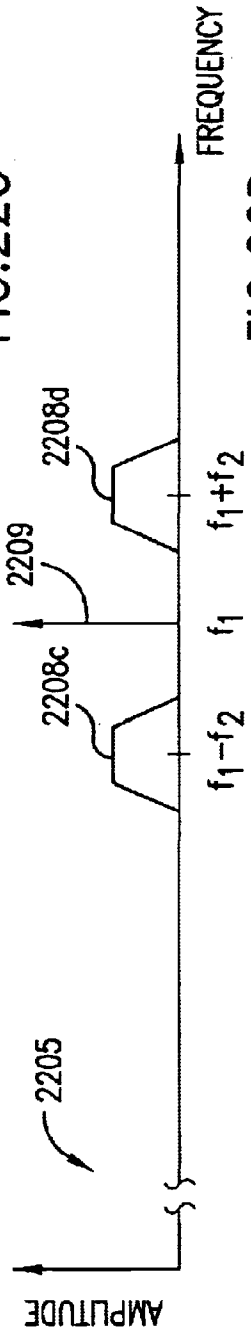


FIG.22D

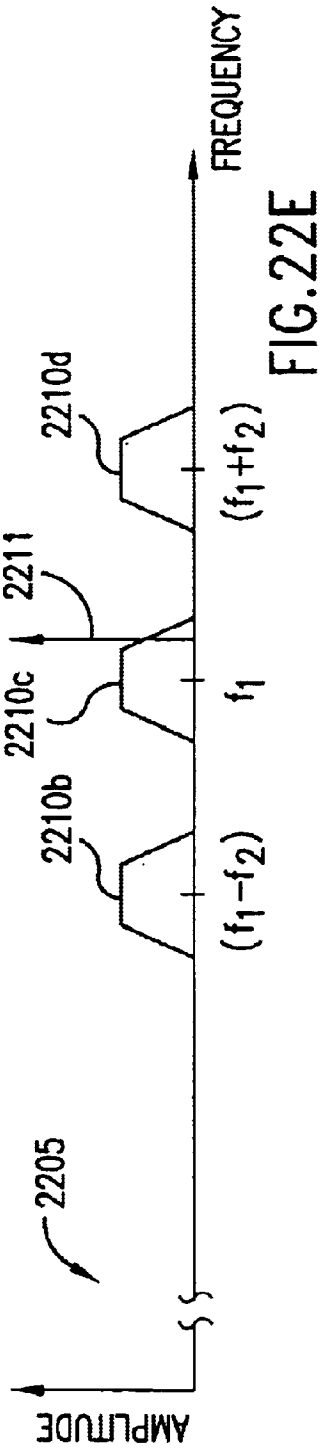


FIG.22E

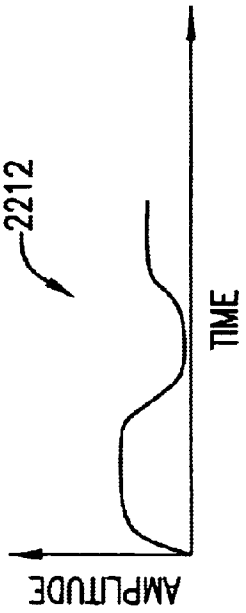


FIG.22F

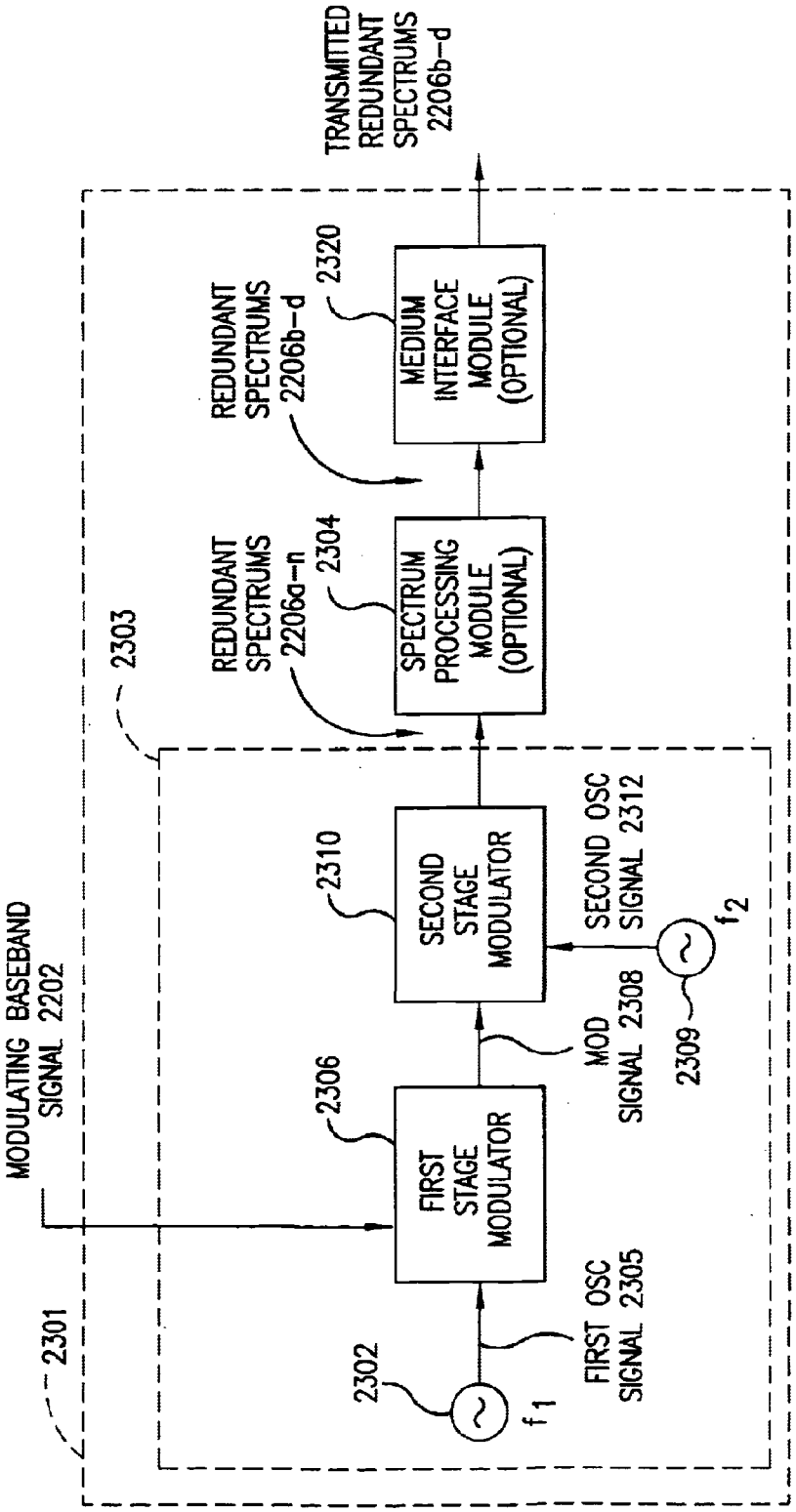

TRANSMITTED REDUNDANT SPECTRUMS 2206b–d
REDUNDANT SPECTRUMS 2206b–d
2320
MEDIUM INTERFACE MODULE (OPTIONAL)
REDUNDANT SPECTRUMS 2206a–n
2304
SPECTRUM PROCESSING MODULE (OPTIONAL)
2303
2310
SECOND STAGE MODULATOR
SECOND OSC SIGNAL 2312
f_2
2309
MOD SIGNAL 2308
MODULATING BASEBAND SIGNAL 2202
2306
FIRST STAGE MODULATOR
FIRST OSC SIGNAL 2305
2302
f_1
2301

FIG.23A

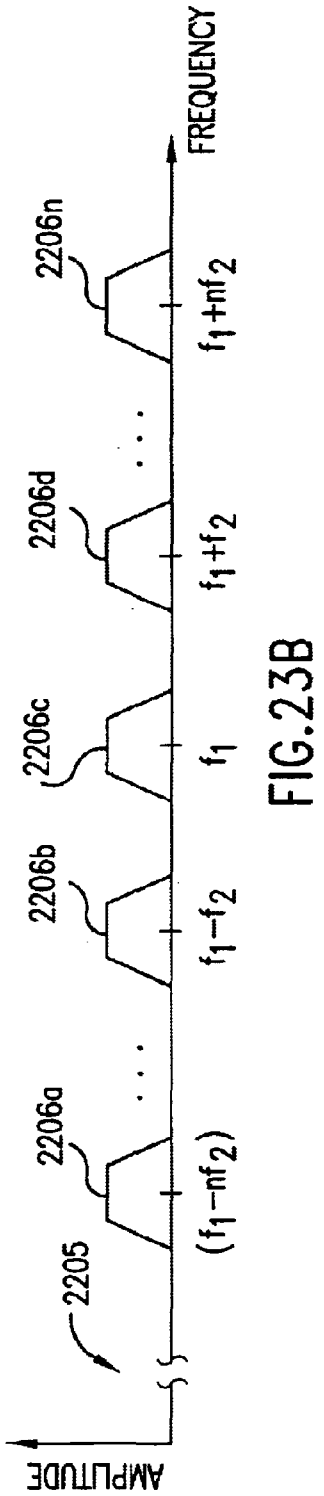


FIG.23B

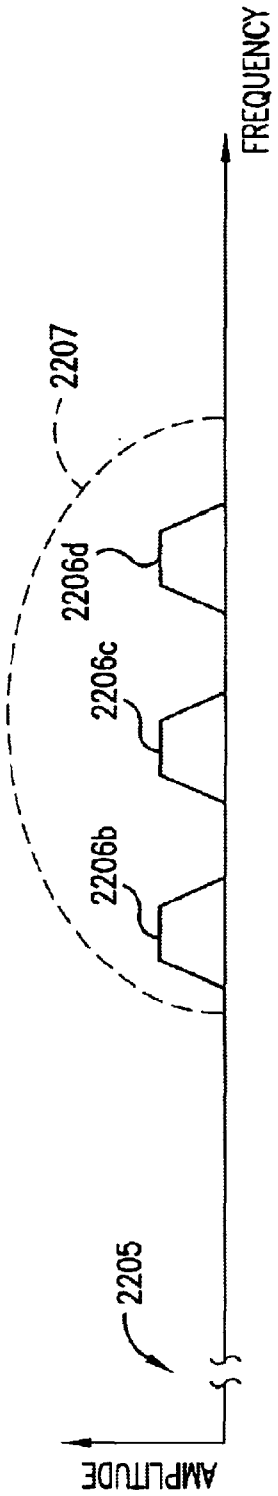


FIG.23C

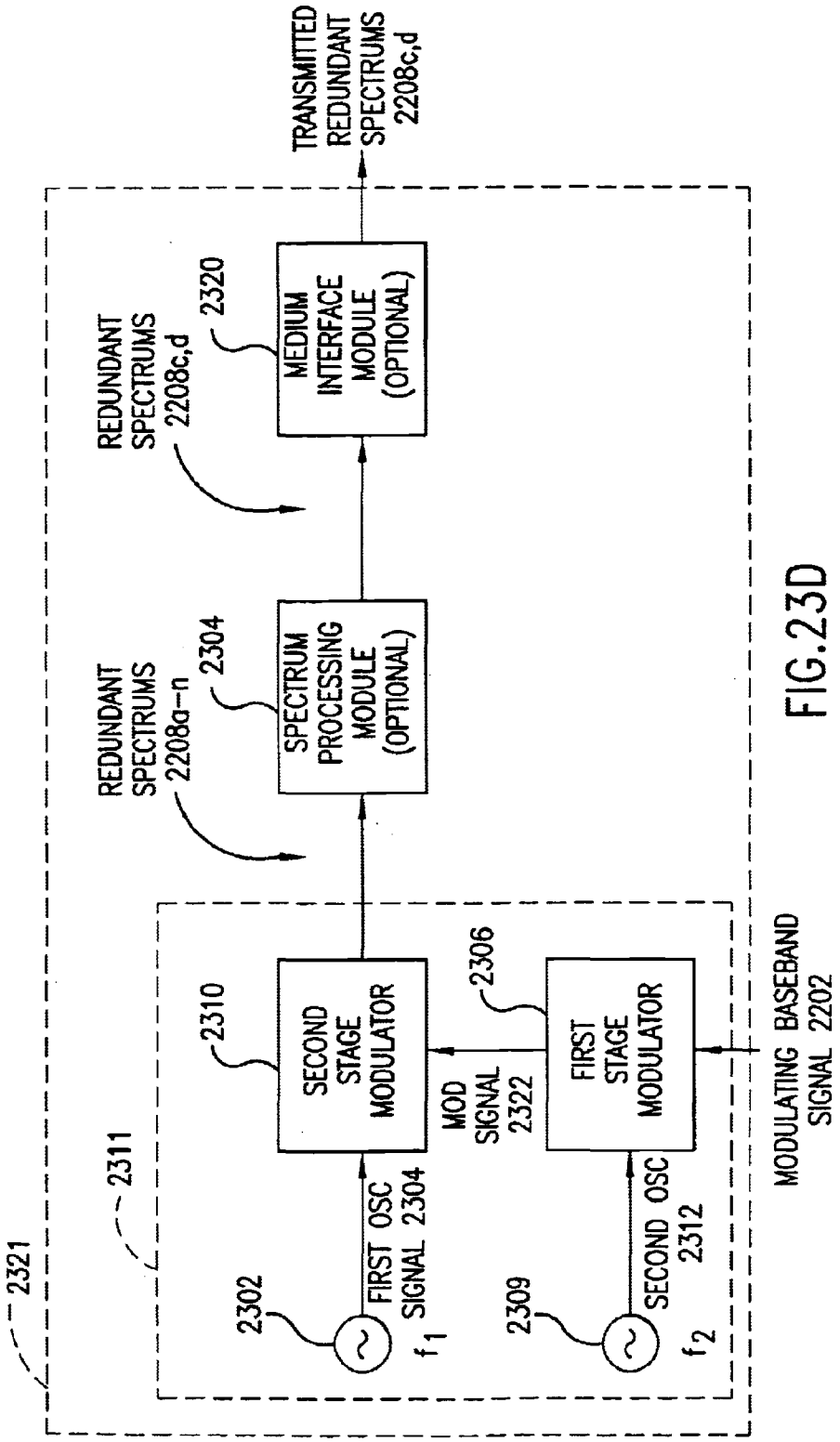

TRANSMITTED REDUNDANT SPECTRUMS 2208c,d
REDUNDANT SPECTRUMS 2208c,d
2320
MEDIUM INTERFACE MODULE (OPTIONAL)
REDUNDANT SPECTRUMS 2208a–n
2304
SPECTRUM PROCESSING MODULE (OPTIONAL)
2310
SECOND STAGE MODULATOR
2306
MOD SIGNAL 2322
FIRST STAGE MODULATOR
MODULATING BASEBAND SIGNAL 2202
2311
2321
2302
FIRST OSC SIGNAL 2304
f_1
2309
SECOND OSC 2312
f_2

FIG.23D

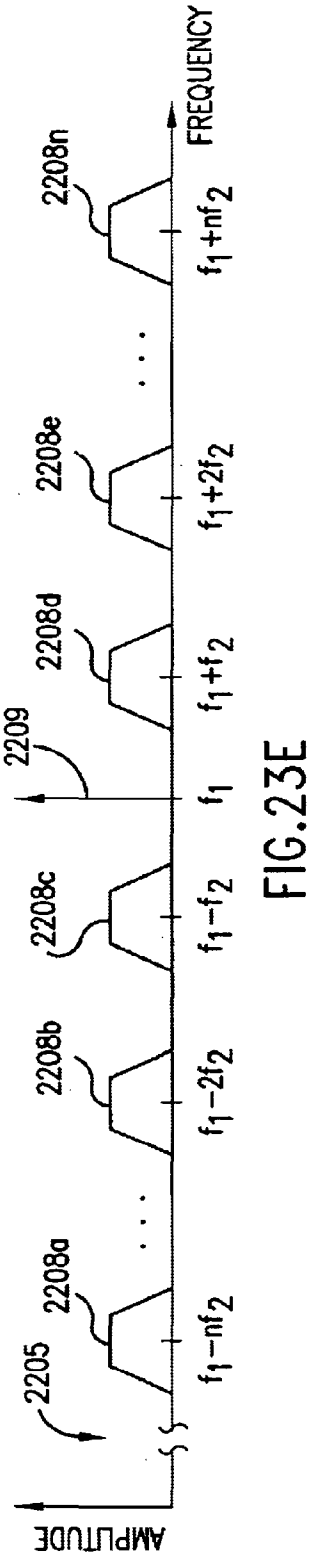


FIG.23E

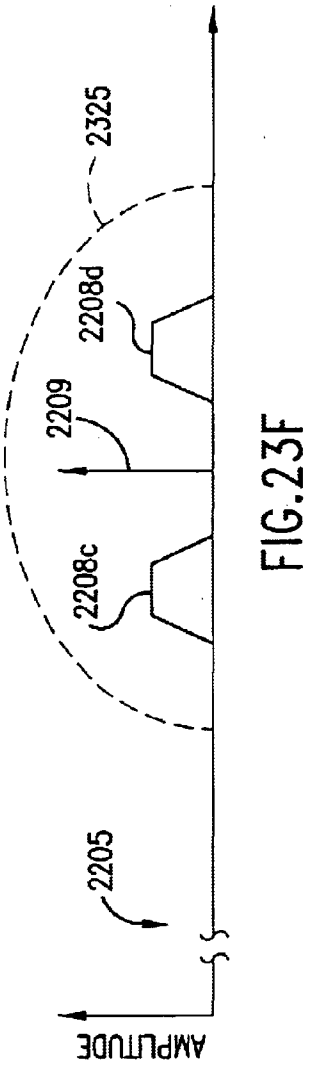


FIG.23F

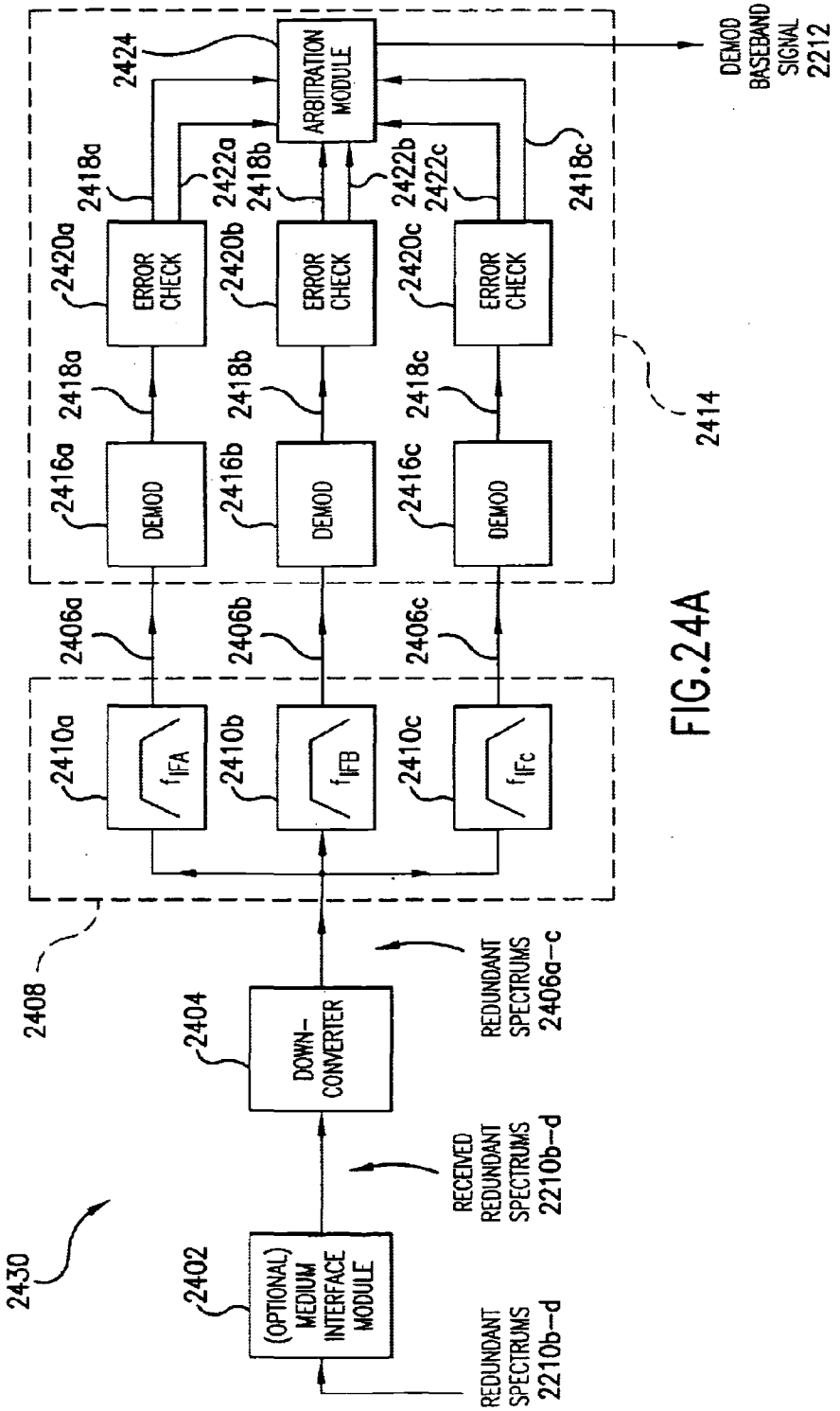

2430
2402
(OPTIONAL) MEDIUM INTERFACE MODULE
REDUNDANT SPECTRUMS 2210b–d
RECEIVED REDUNDANT SPECTRUMS 2210b–d
2404
DOWN-CONVERTER
REDUNDANT SPECTRUMS 2406a–c
2408
2410a
f_{IFA}
2410b
f_{IFB}
2410c
f_{IFC}
2406a
2406b
2406c
2414
2416a
DEMOD
2416b
DEMOD
2416c
DEMOD
2418a
2418b
2418c
2420a
ERROR CHECK
2420b
ERROR CHECK
2420c
ERROR CHECK
2422a
2422b
2422c
2424
ARBITRATION MODULE
DEMOD BASEBAND SIGNAL 2212

FIG.24A

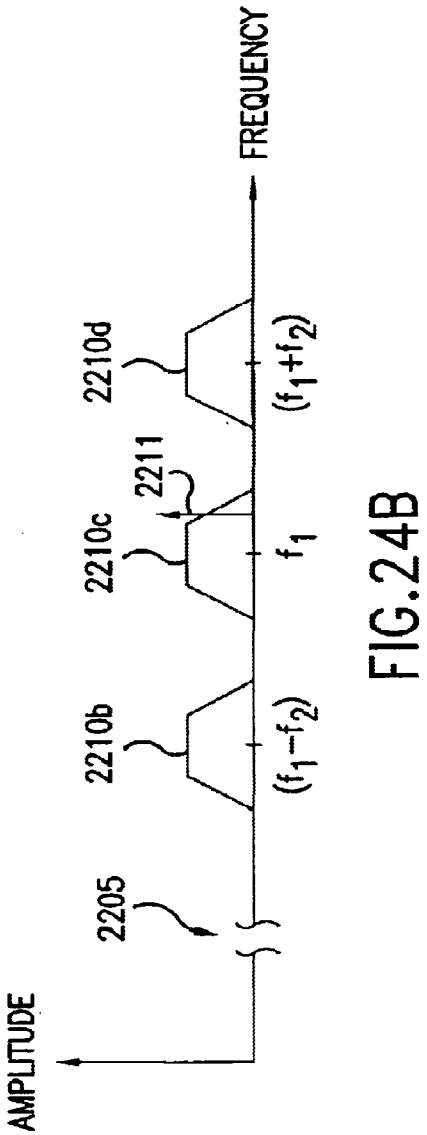


FIG.24B

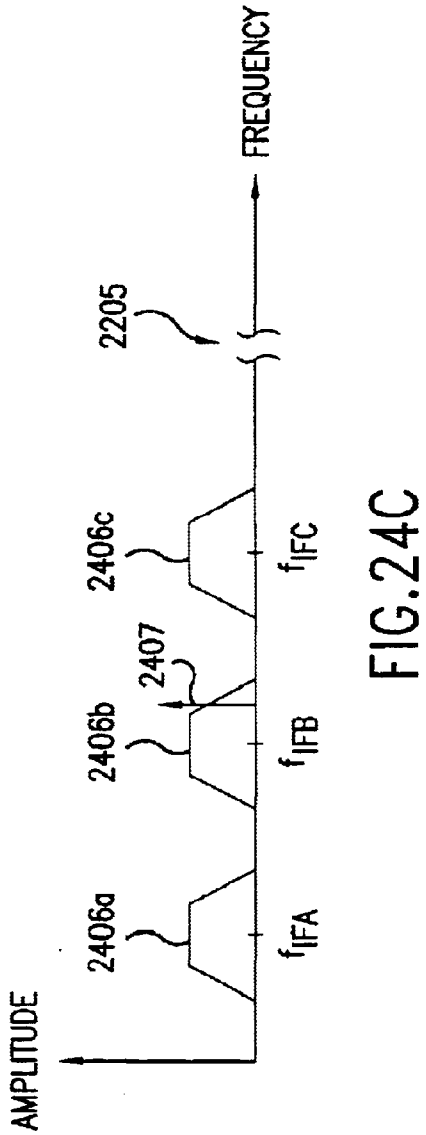


FIG.24C

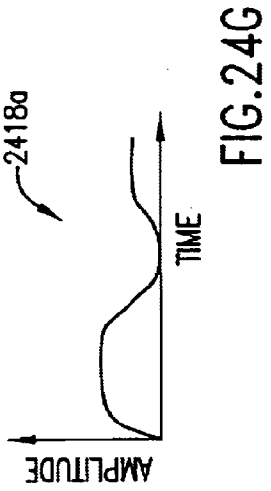


FIG.24G

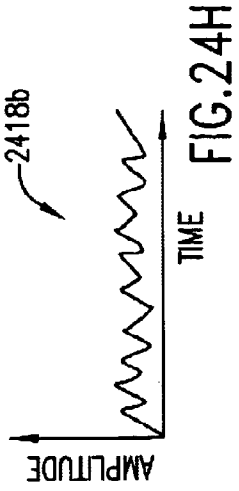


FIG.24H

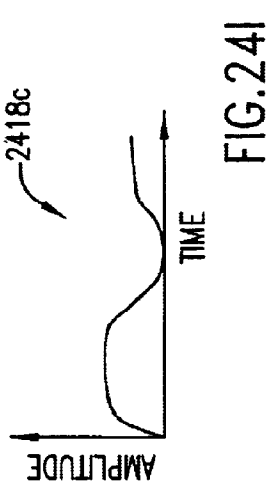


FIG.24I

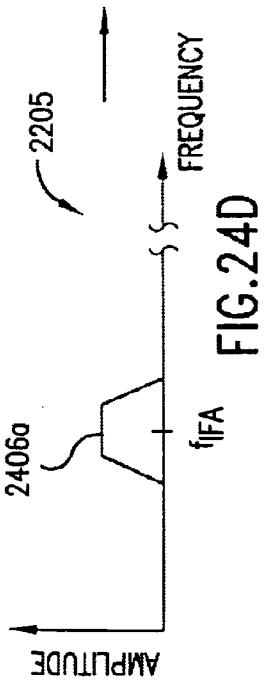


FIG.24D

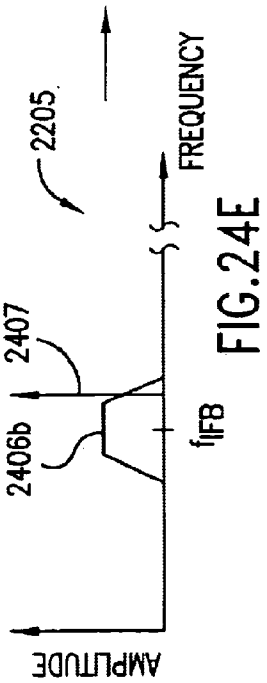


FIG.24E

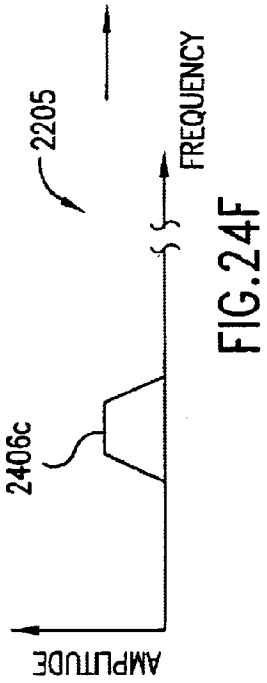


FIG.24F

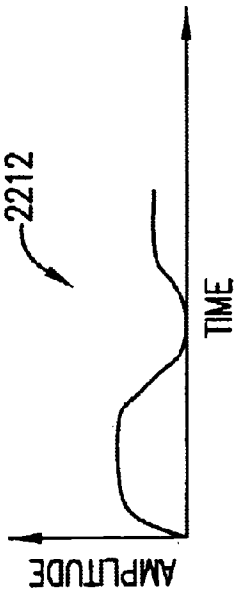


FIG. 24J

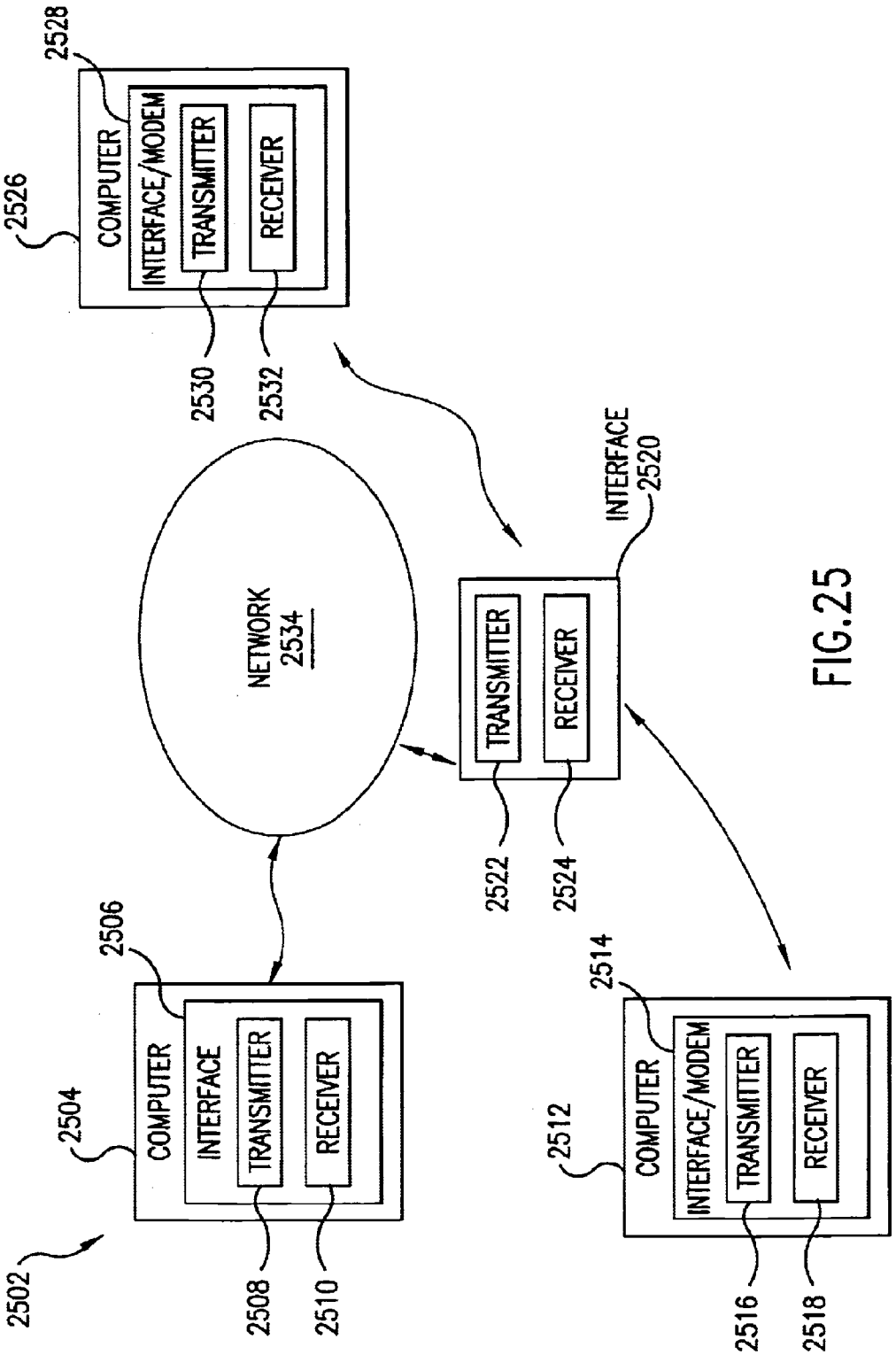

2528
COMPUTER
INTERFACE/MODEM
TRANSMITTER
RECEIVER
2526
2530
2532
NETWORK
2534
INTERFACE
2520
TRANSMITTER
RECEIVER
2522
2524
2506
2504
COMPUTER
INTERFACE
TRANSMITTER
RECEIVER
2502
2508
2510
2514
2512
COMPUTER
INTERFACE/MODEM
TRANSMITTER
RECEIVER
2516
2518

FIG.25

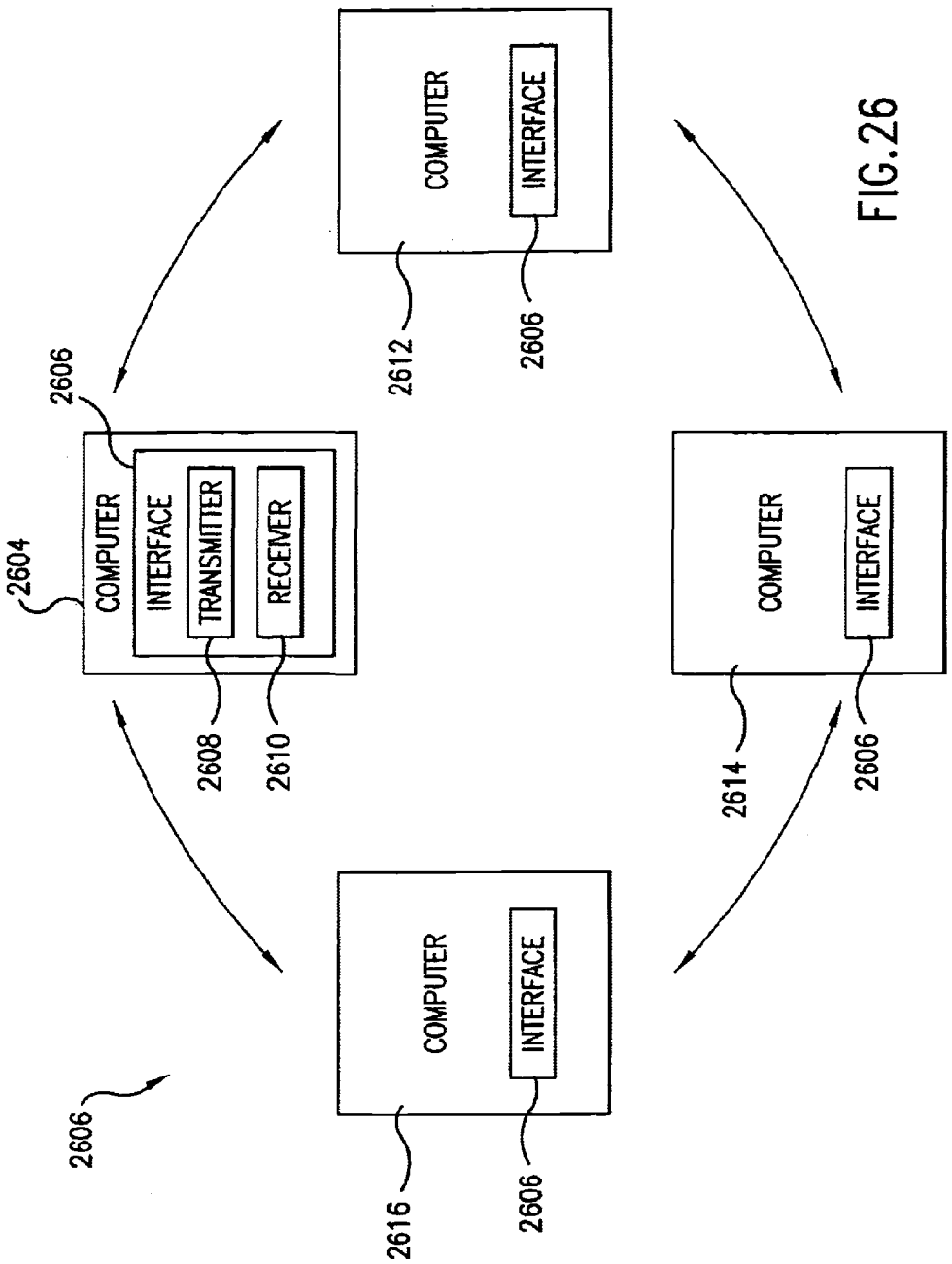

COMPUTER
INTERFACE
2612
2606
2606
2604
COMPUTER
INTERFACE
TRANSMITTER
RECEIVER
2608
2610
COMPUTER
INTERFACE
2614
2606
2606
COMPUTER
INTERFACE
2616
2606

FIG.26

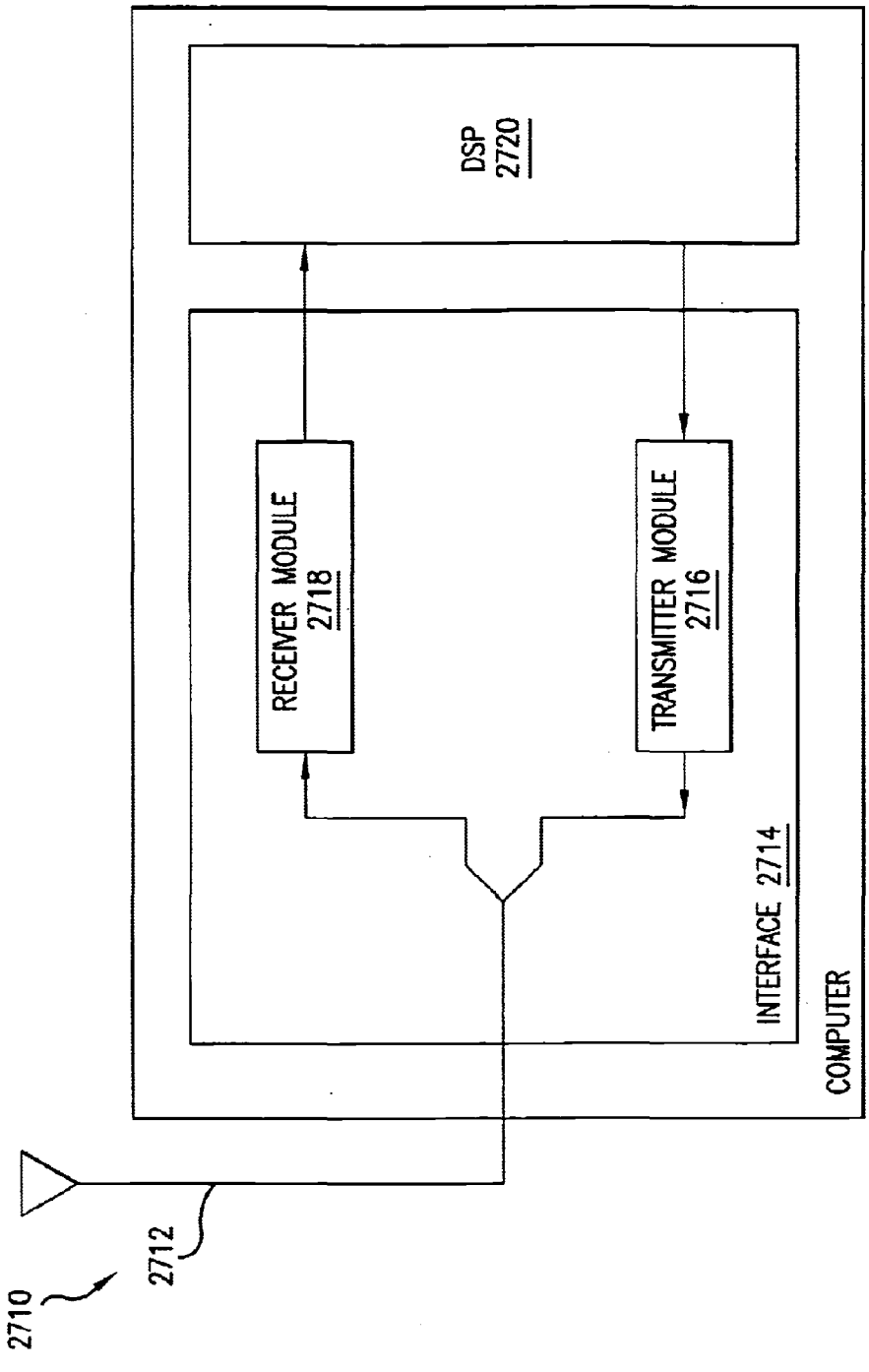

DSP
2720
RECEIVER MODULE
2718
TRANSMITTER MODULE
2716
INTERFACE 2714
COMPUTER
2712
2710

FIG.27

FIG.28

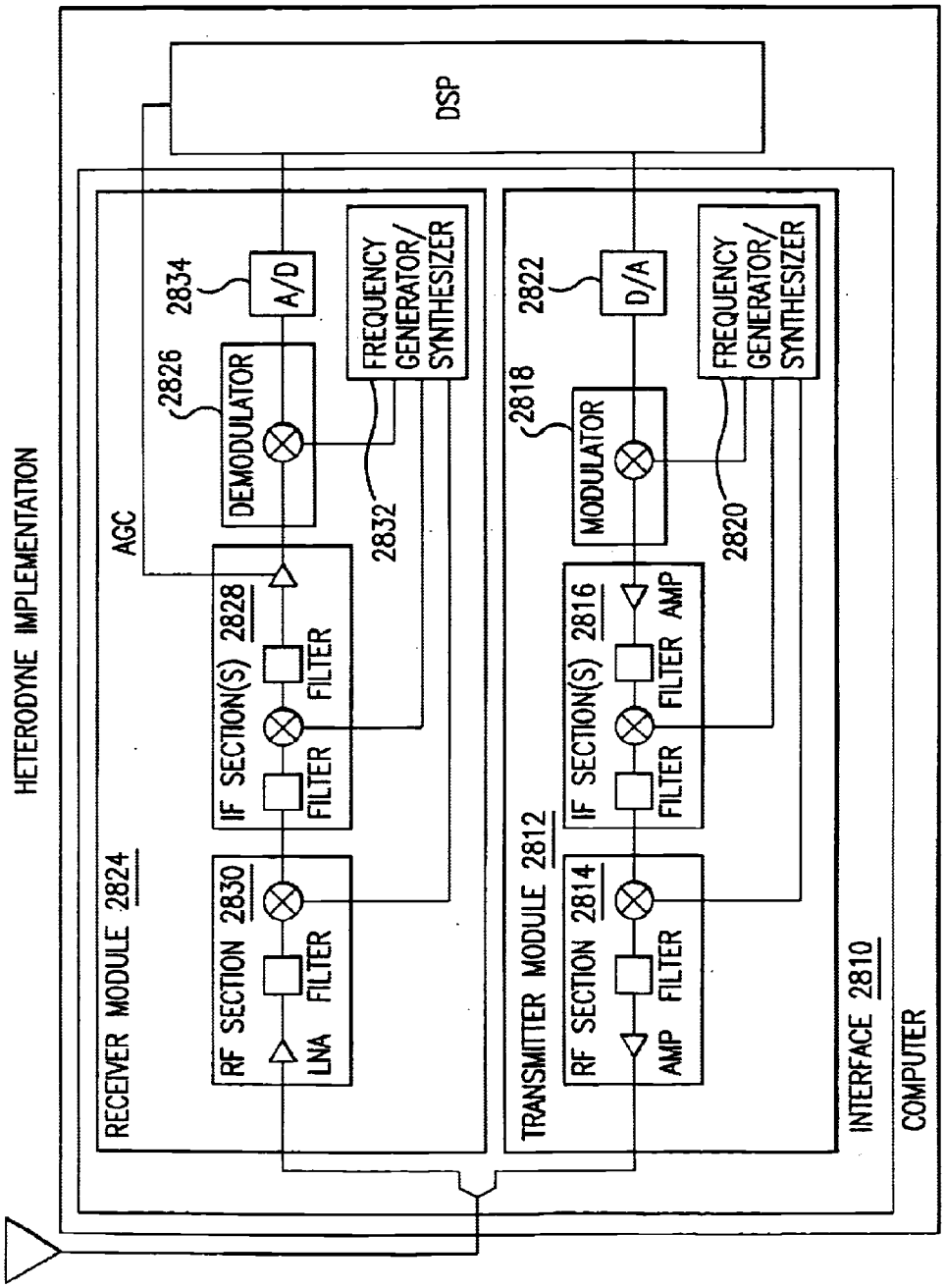
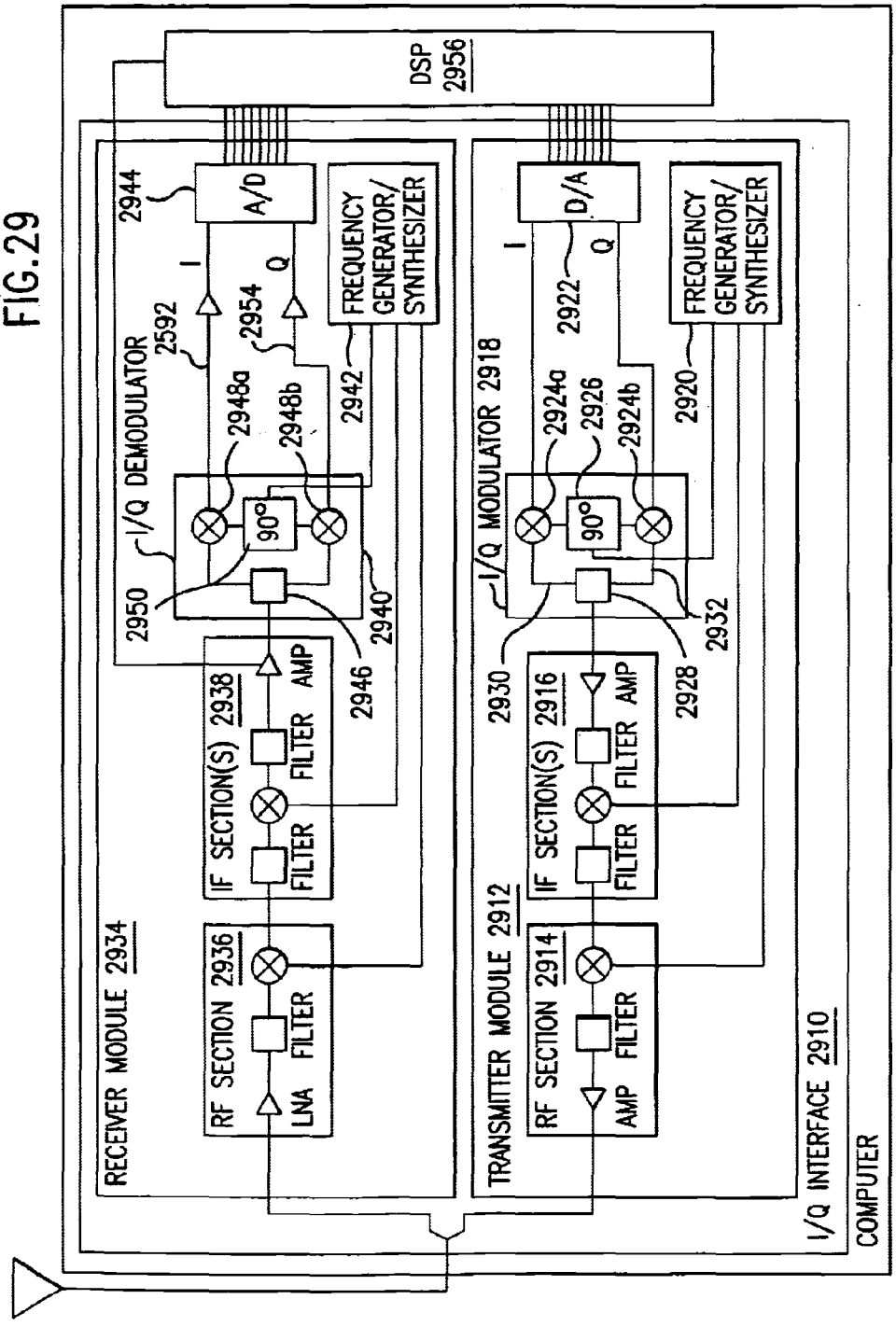

HETERODYNE IMPLEMENTATION
DSP
RECEIVER MODULE 2824
AGC
2834
A/D
2826
DEMODULATOR
FREQUENCY GENERATOR/ SYNTHESIZER
2832
IF SECTION(S) 2828
FILTER
FILTER
RF SECTION 2830
LNA FILTER
TRANSMITTER MODULE 2812
2822
D/A
2818
MODULATOR
FREQUENCY GENERATOR/ SYNTHESIZER
2820
IF SECTION(S) 2816
FILTER AMP
FILTER
RF SECTION 2814
AMP FILTER
INTERFACE 2810
COMPUTER

FIG.29


DSP 2956
RECEIVER MODULE 2934
TRANSMITTER MODULE 2912
I/Q INTERFACE 2910
COMPUTER
A/D
D/A
2944
2922
I
Q
2592
2954
2942
2920
2948a
2948b
2924a
2926
2924b
I/Q DEMODULATOR
I/Q MODULATOR 2918
FREQUENCY GENERATOR/ SYNTHESIZER
90°
2950
2940
2946
2930
2932
2928
IF SECTION(S) 2938
IF SECTION(S) 2916
FILTER
AMP
RF SECTION 2936
RF SECTION 2914
LNA
AMP

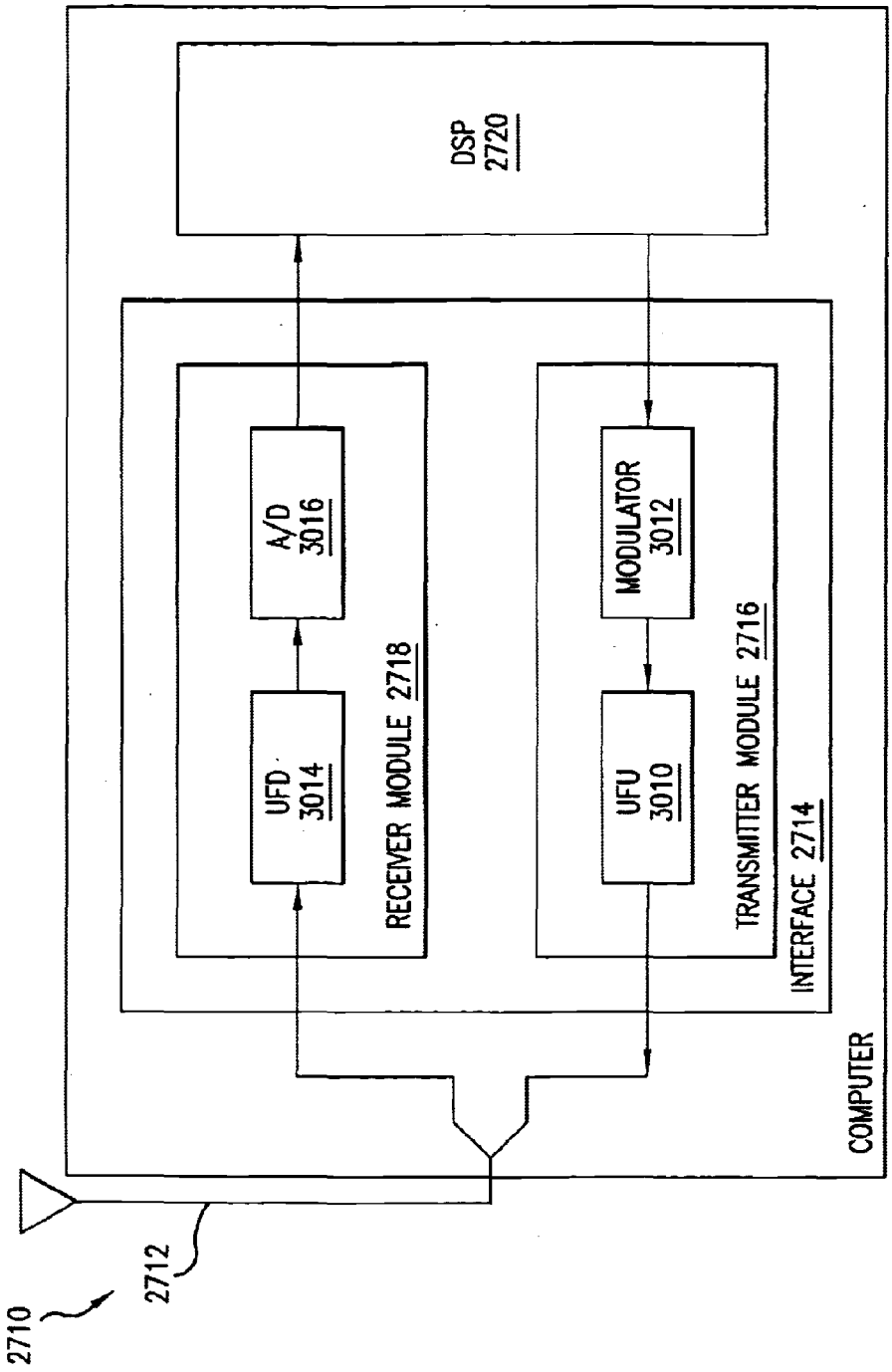

DSP
2720
A/D
3016
UFD
3014
RECEIVER MODULE 2718
MODULATOR
3012
UFU
3010
TRANSMITTER MODULE 2716
INTERFACE 2714
COMPUTER
2712
2710

FIG.30

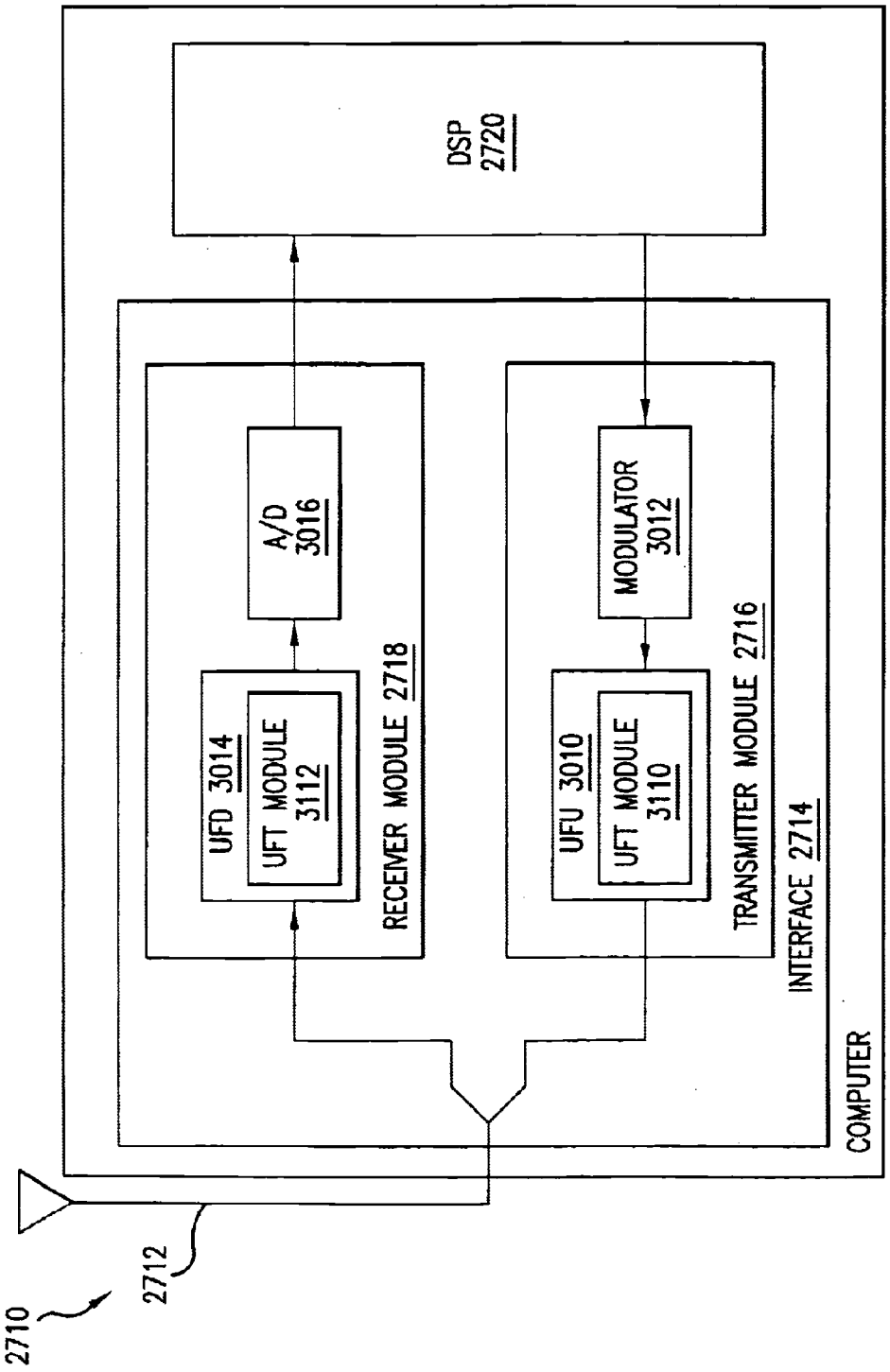
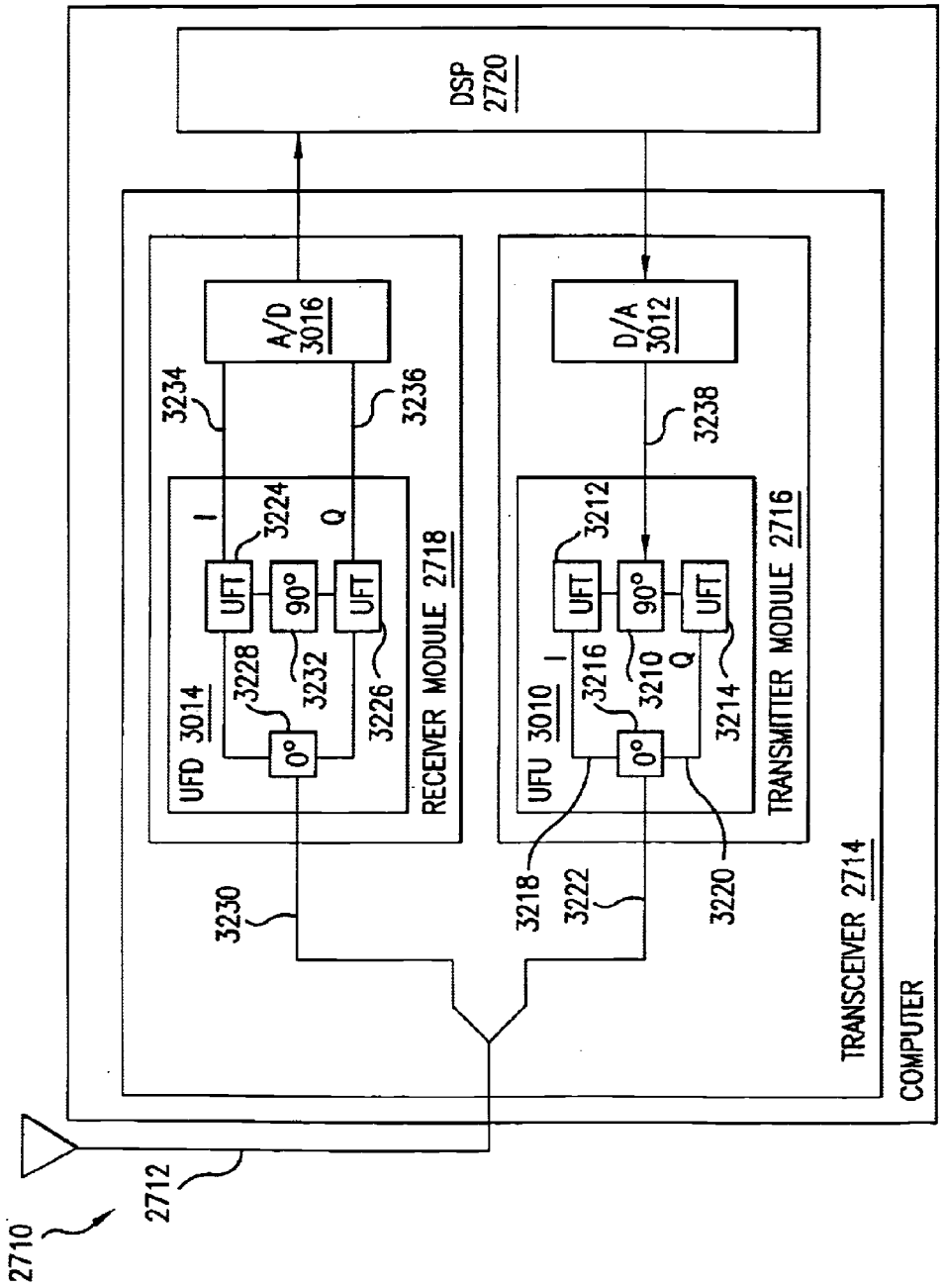

DSP
2720
A/D
3016
MODULATOR
3012
UFD 3014
UFT MODULE
3112
RECEIVER MODULE 2718
UFU 3010
UFT MODULE
3110
TRANSMITTER MODULE 2716
INTERFACE 2714
COMPUTER
2712
2710

FIG.31

FIG.32


DSP 2720
A/D 3016
D/A 3012
3234
3236
3238
I
Q
3224
3212
UFT
90°
UFT
UFD 3014
3228
3232
3226
0°
RECEIVER MODULE 2718
UFU 3010
3216
3210
3214
TRANSMITTER MODULE 2716
3230
3218
3222
3220
TRANSCEIVER 2714
COMPUTER
2712
2710

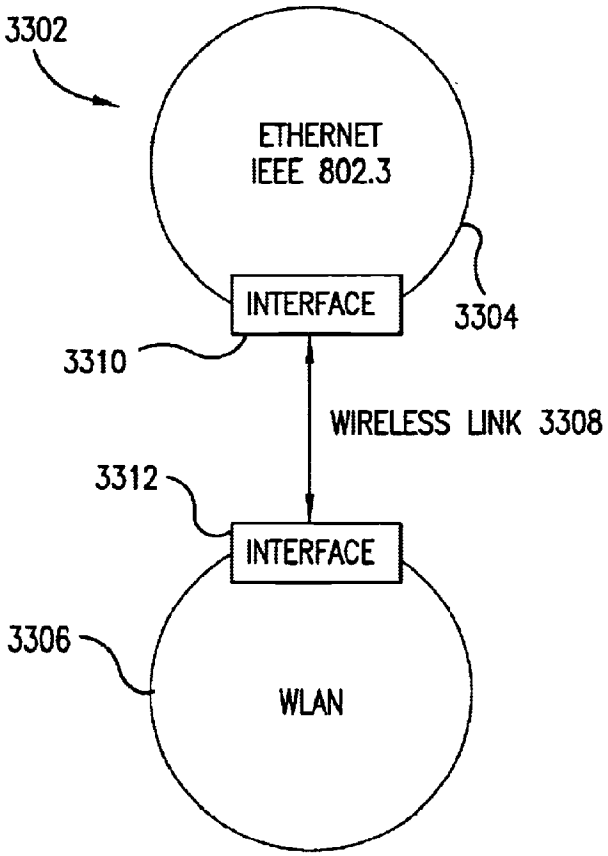

3302
ETHERNET
IEEE 802.3
INTERFACE
3304
3310
WIRELESS LINK 3308
3312
INTERFACE
3306
WLAN

FIG.33

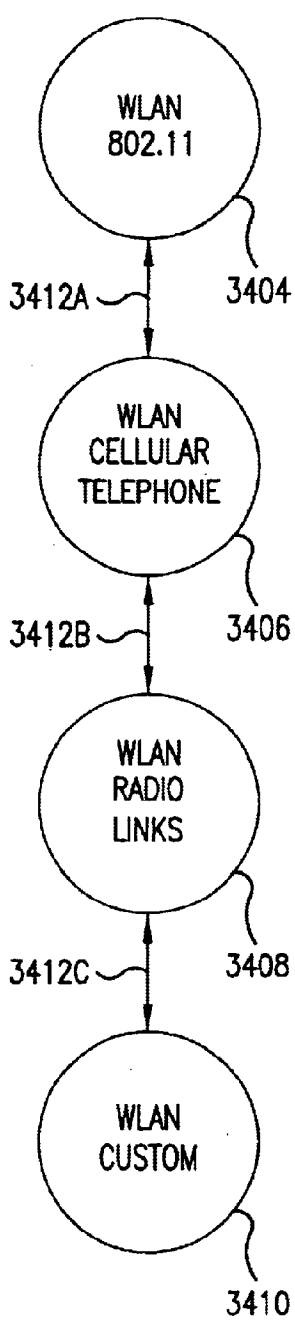

3402
WLAN
802.11
3412A
3404
WLAN
CELLULAR
TELEPHONE
3412B
3406
WLAN
RADIO
LINKS
3412C
3408
WLAN
CUSTOM
3410

FIG.34

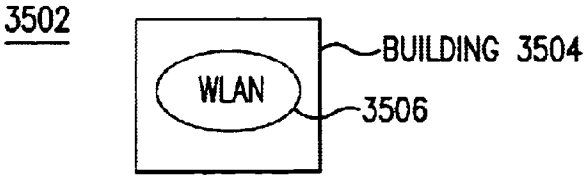


FIG.35

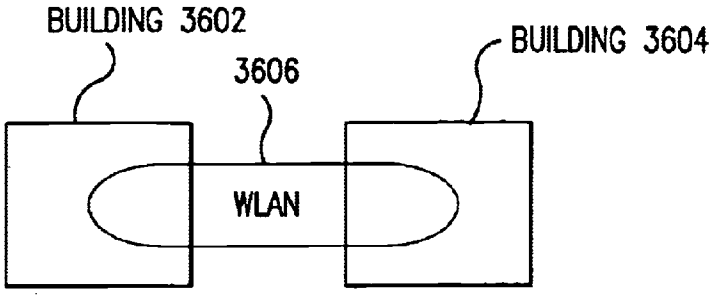


FIG.36

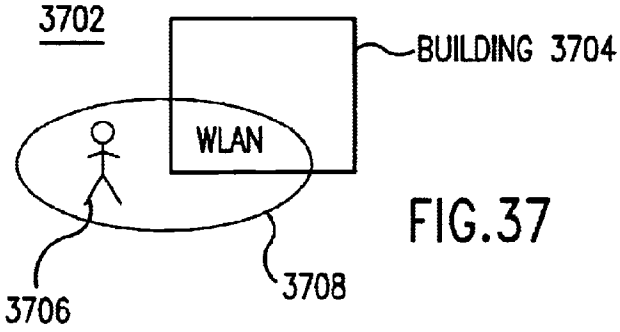


FIG.37

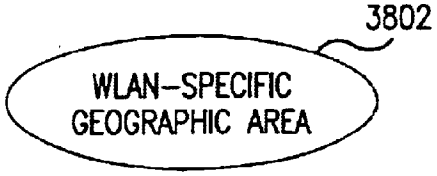


FIG.38

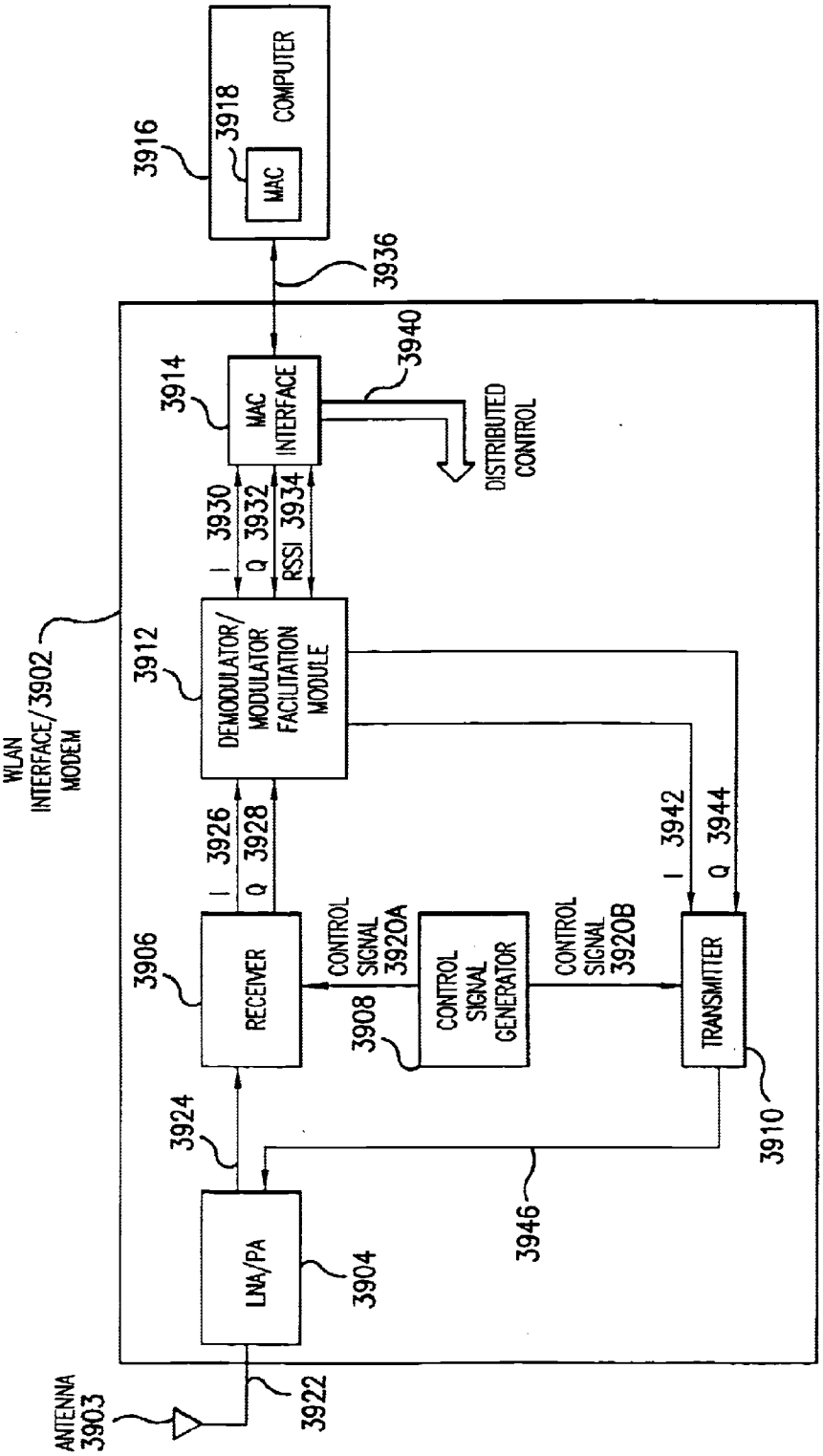

3916
3918
COMPUTER
MAC
3936
3940
3914
MAC INTERFACE
DISTRIBUTED CONTROL
I 3930
Q 3932
RSSI 3934
WLAN INTERFACE/3902 MODEM
3912
DEMODULATOR/ MODULATOR FACILITATION MODULE
I 3926
Q 3928
I 3942
Q 3944
3906
RECEIVER
CONTROL SIGNAL 3920A
3908
CONTROL SIGNAL GENERATOR
CONTROL SIGNAL 3920B
TRANSMITTER
3910
3924
3946
LNA/PA
3904
ANTENNA 3903
3922

FIG.39

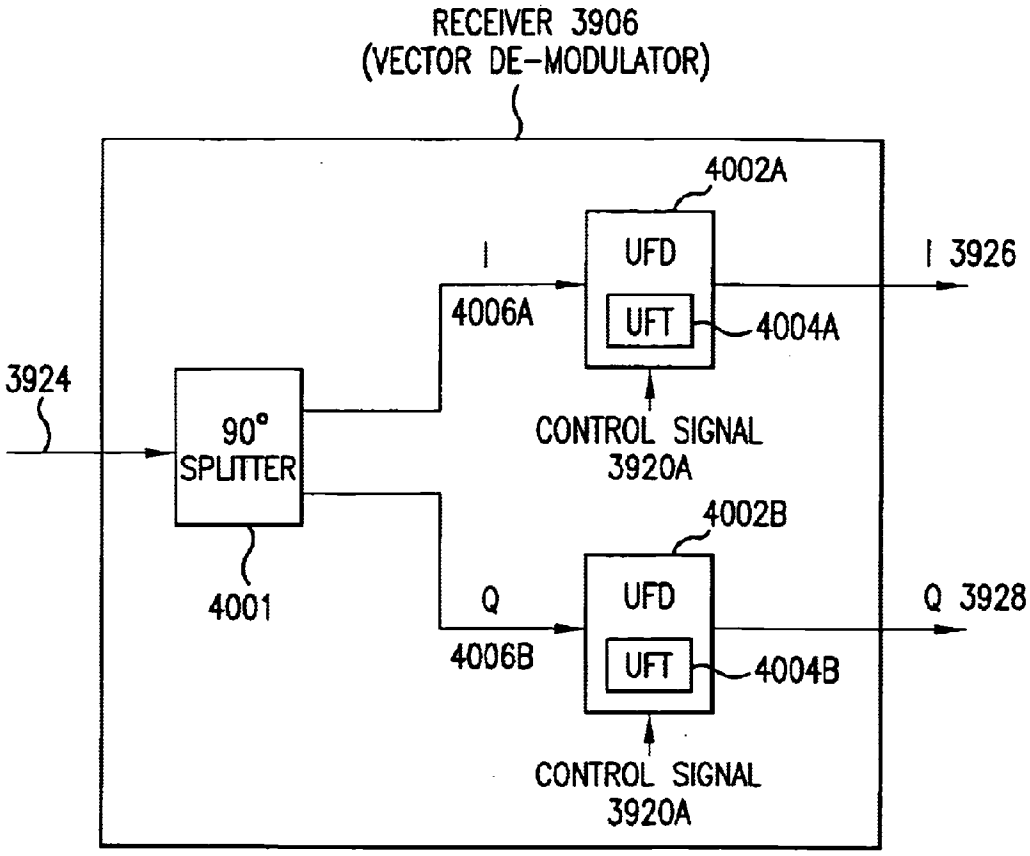

RECEIVER 3906
(VECTOR DE-MODULATOR)
4002A
UFD
UFT
4004A
I
4006A
I 3926
3924
90°
SPLITTER
4001
CONTROL SIGNAL
3920A
4002B
UFD
UFT
4004B
Q
4006B
Q 3928
CONTROL SIGNAL
3920A

FIG.40

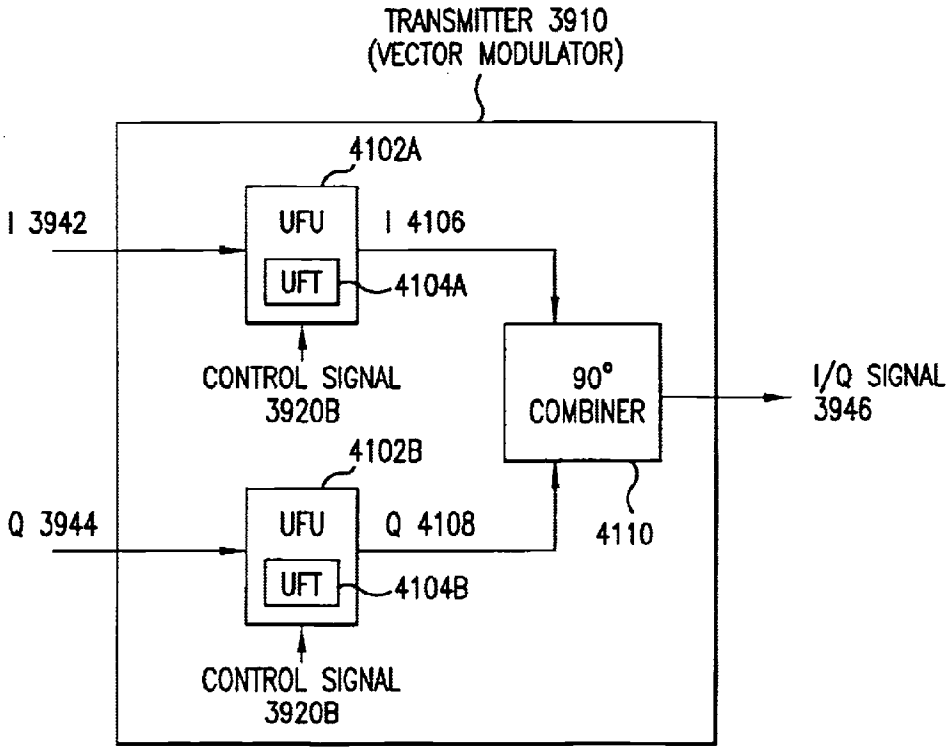

TRANSMITTER 3910
(VECTOR MODULATOR)
4102A
I 3942
UFU
UFT
I 4106
4104A
CONTROL SIGNAL
3920B
90°
COMBINER
I/Q SIGNAL
3946
4102B
Q 3944
UFU
UFT
Q 4108
4110
4104B
CONTROL SIGNAL
3920B

FIG.41

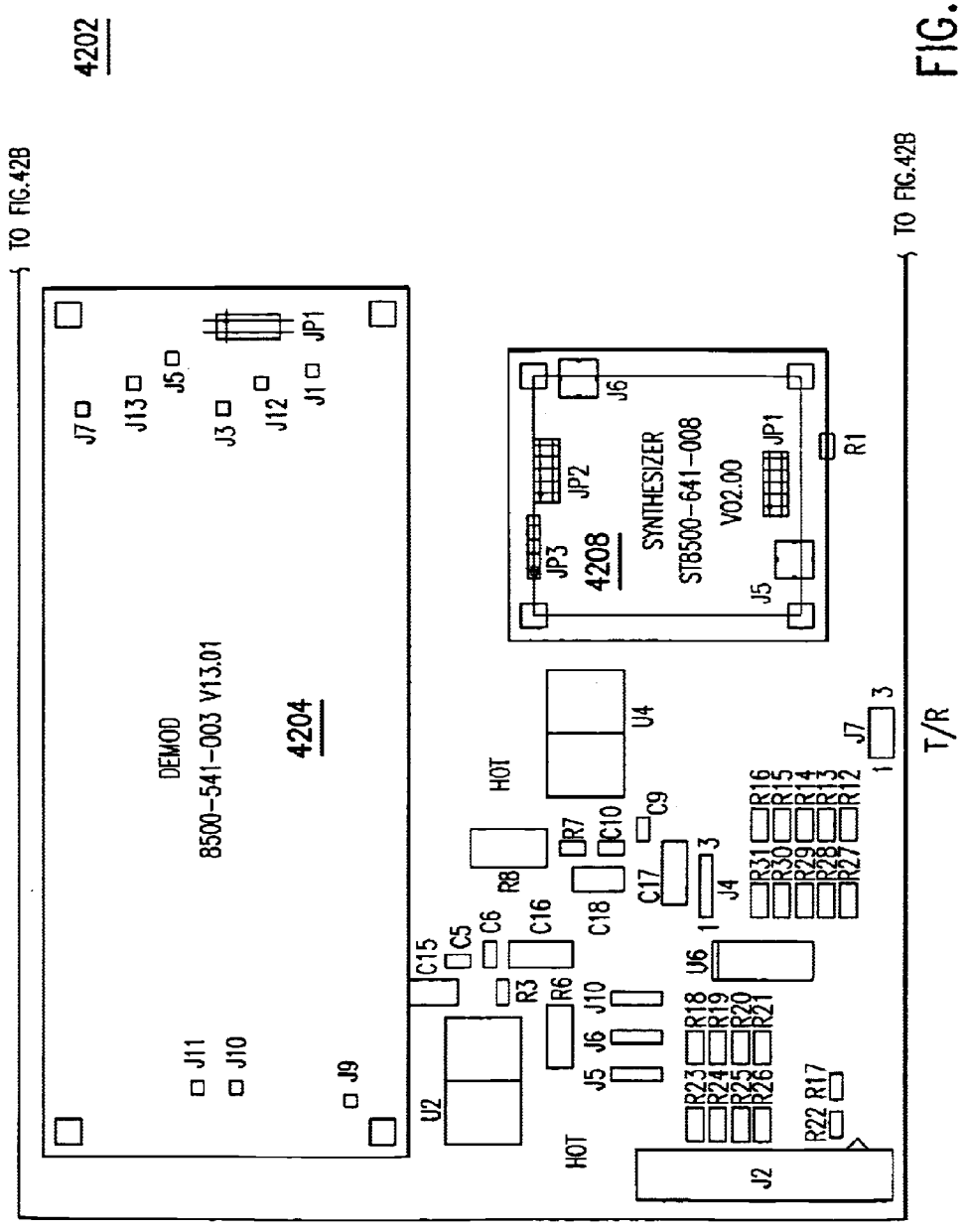

4202
TO FIG.42B
TO FIG.42B
DEMOD
8500-541-003 V13.01
4204
SYNTHESIZER
ST8500-641-008
V02.00
4208
HOT
HOT
T/R
J1
J2
J3
J4
J5
J6
J7
J9
J10
J11
J12
J13
JP1
JP2
JP3
U2
U4
U6
C5
C6
C9
C10
C15
C16
C17
C18
R1
R3
R6
R7
R8
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31

FIG.42A

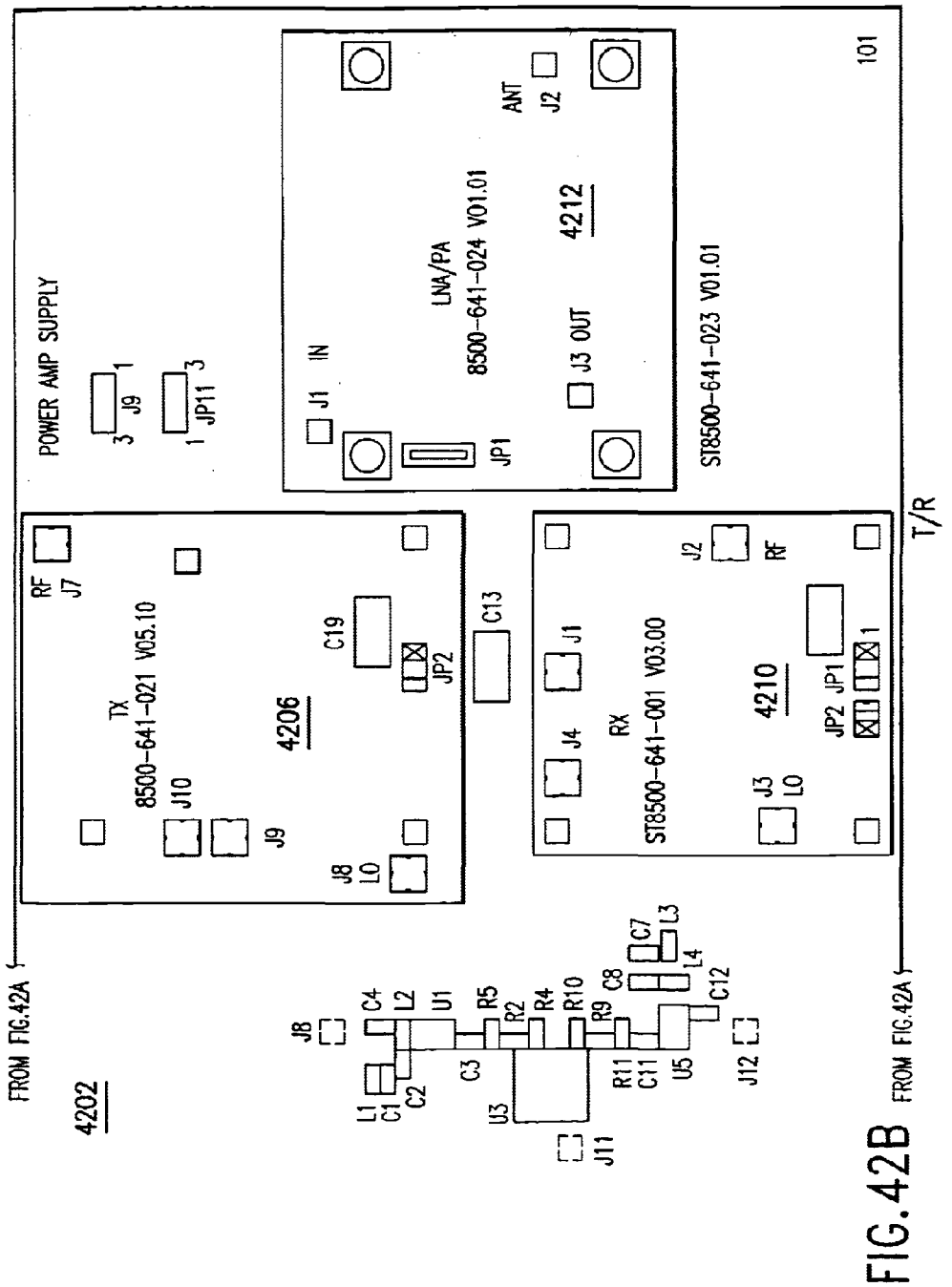

101
POWER AMP SUPPLY
J9
JP11
LNA/PA
8500-641-024 V01.01
4212
ANT
J2
J1 IN
J3 OUT
JP1
ST8500-641-023 V01.01
RF
J7
TX
8500-641-021 V05.10
4206
C19
JP2
C13
J10
J9
J8
LO
J2
RF
J1
J4
RX
ST8500-641-001 V03.00
4210
JP1
JP2
J3
LO
T/R
FROM FIG.42A
4202
C4
L2
U1
R5
R2
R4
R10
R9
C8
C7
L3
L4
C12
J8
C3
R11
C11
U5
J12
L1
C1
C2
U3
J11
FROM FIG.42A

FIG. 42B

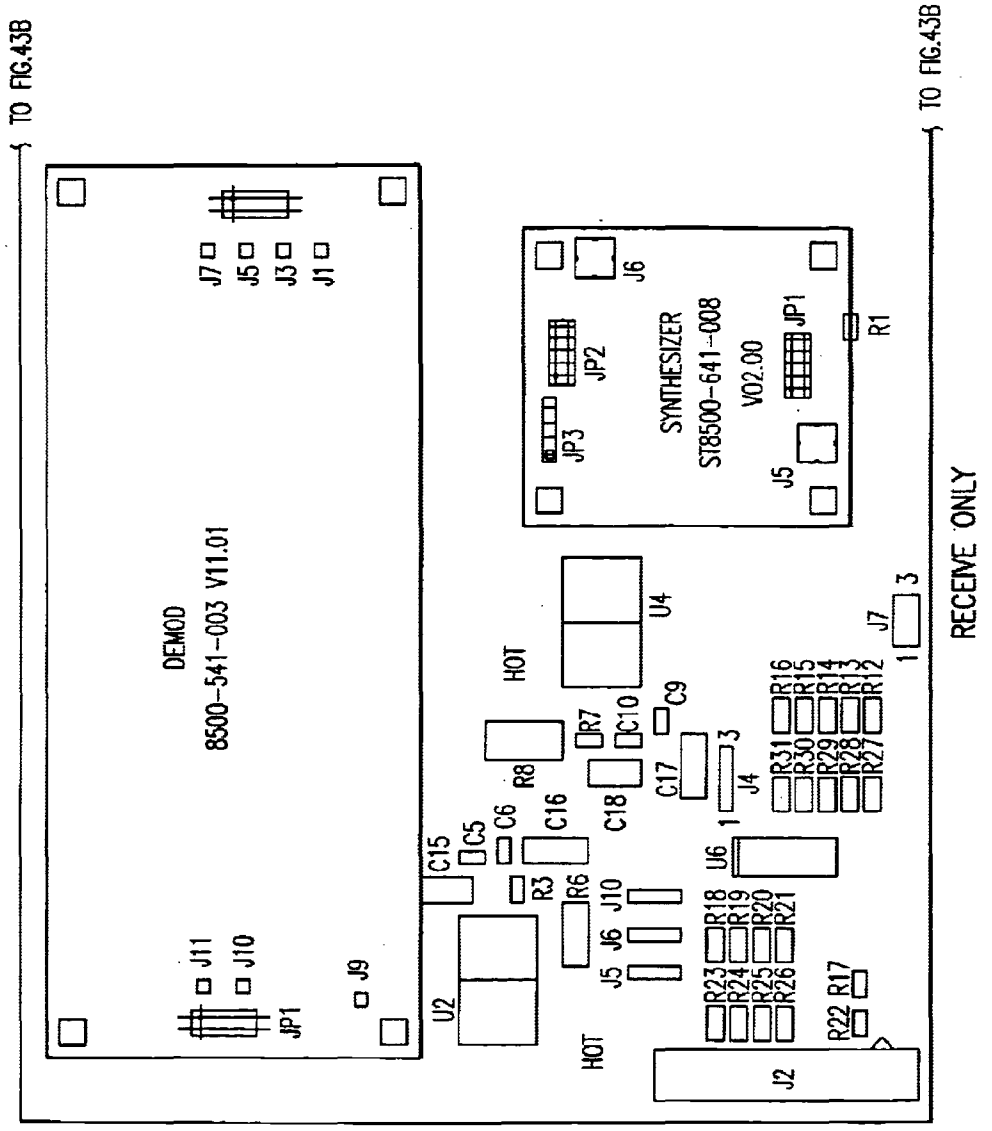

4302
TO FIG.43B
TO FIG.43B
DEMOD
8500-541-003 V11.01
SYNTHESIZER
ST8500-641-008
V02.00
RECEIVE ONLY
HOT
HOT
J7
J5
J3
J1
J11
J10
J9
JP1
JP2
JP3
J6
J5
JP1
R1
U4
U2
U6
J4
J2
C15
C5
C6
C16
C18
C17
C9
C10
R7
R8
R3
R6
J10
J6
J5
R18
R19
R20
R21
R23
R24
R25
R26
R22
R17
R16
R15
R14
R13
R12
R31
R30
R29
R28
R27
J7
1
3

FIG.43A

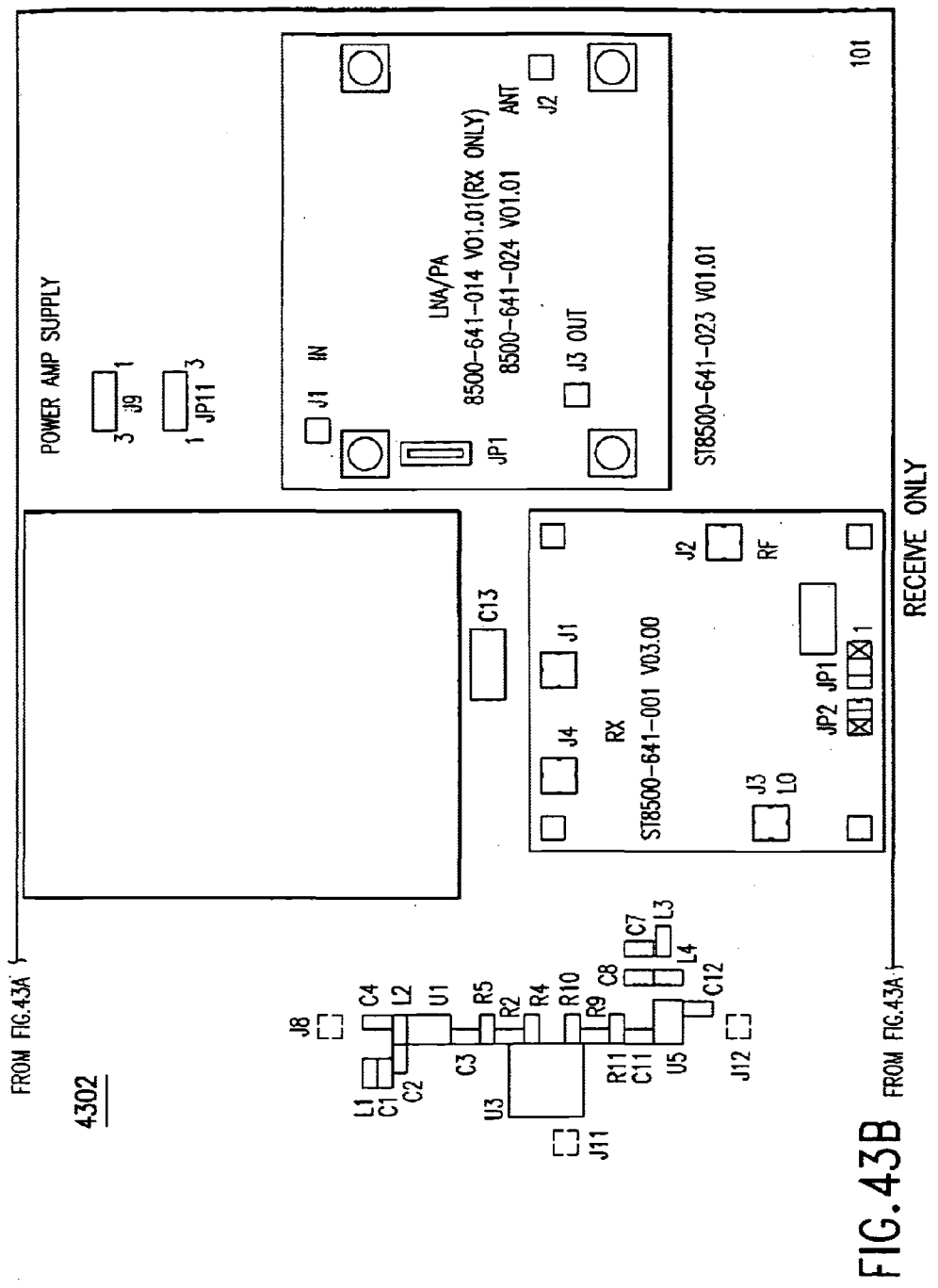

POWER AMP SUPPLY
J9
JP11
J1 IN
LNA/PA
8500-641-014 V01.01(RX ONLY)
8500-641-024 V01.01
JP1
J3 OUT
ANT
J2
ST8500-641-023 V01.01
101
C13
J1
J4
RX
ST8500-641-001 V03.00
J2
RF
JP1
JP2
J3
LO
RECEIVE ONLY
FROM FIG.43A
4302
J8
C4
L2
U1
R5
R2
R4
R10
R9
C8
C7
L3
L4
C12
C3
R11
C11
U5
J12
L1
C1
C2
U3
J11
FROM FIG.43A

FIG.43B

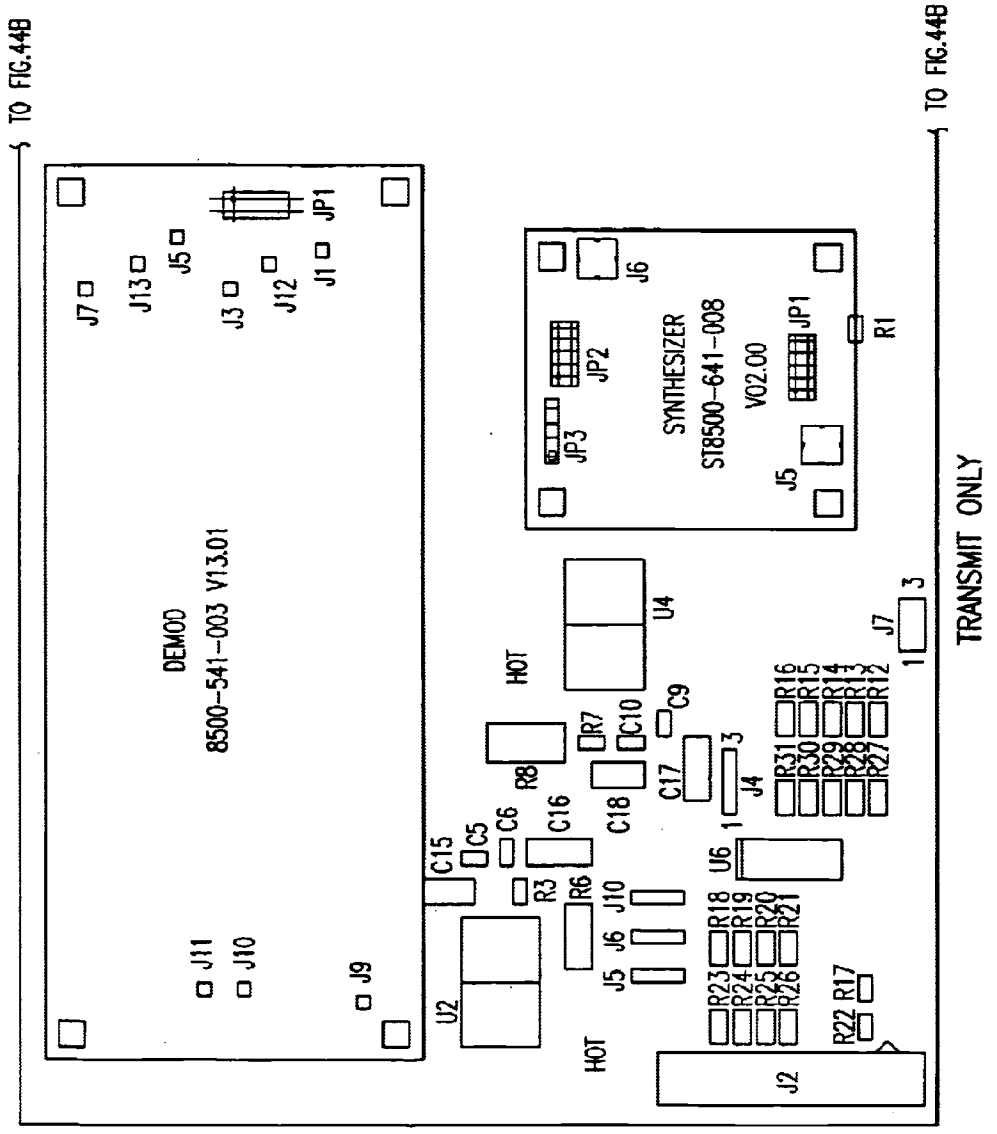

4402
TO FIG.44B
TO FIG.44B
TRANSMIT ONLY
DEMOD
8500-541-003 V13.01
SYNTHESIZER
ST8500-641-008
V02.00
HOT
HOT
J1
J2
J3
J4
J5
J6
J7
J9
J10
J11
J12
J13
JP1
JP2
JP3
U2
U4
U6
R1
R3
R6
R7
R8
C5
C6
C9
C10
C15
C16
C17
C18
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31

FIG.44A

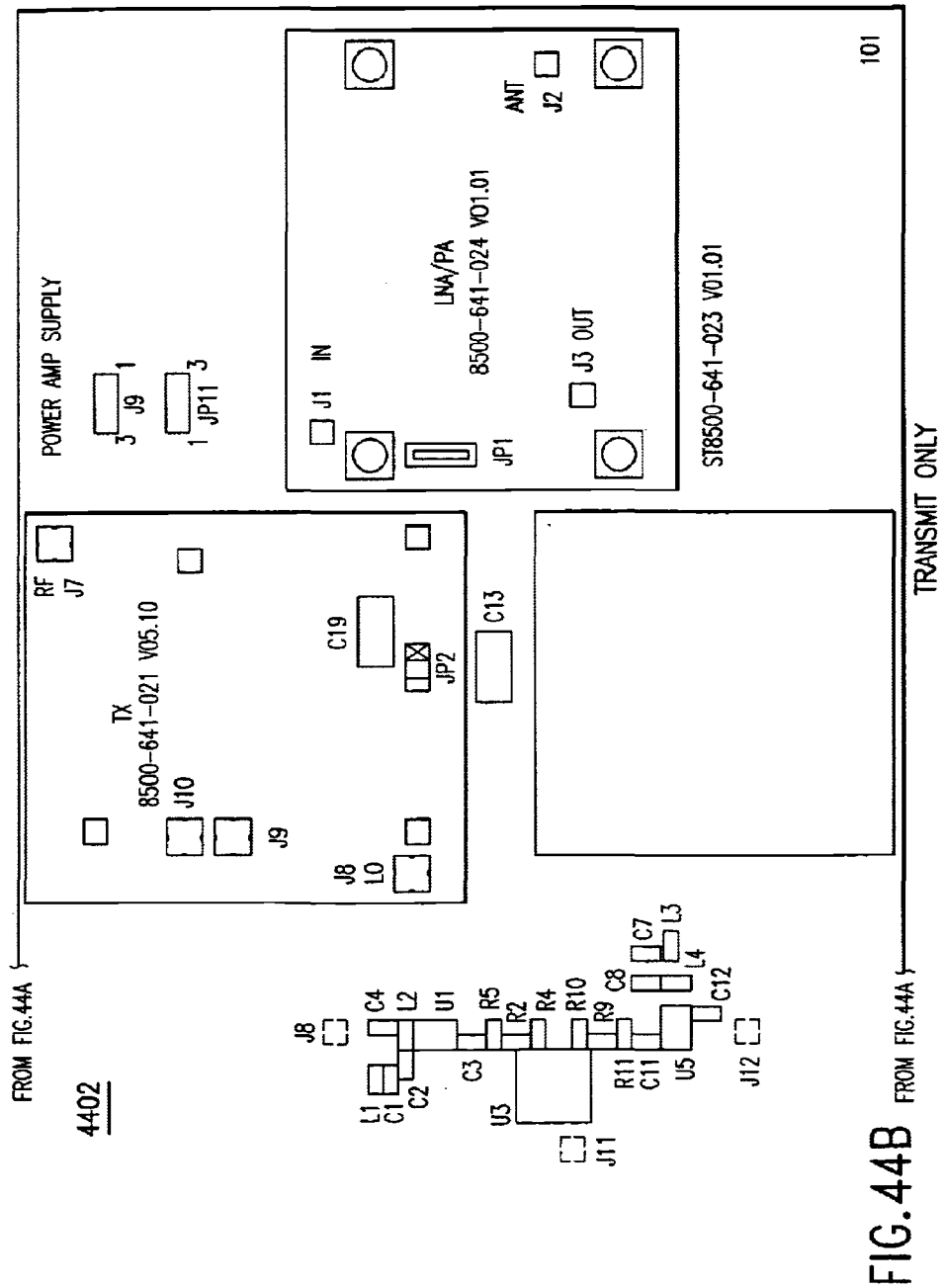

101
POWER AMP SUPPLY
J9
JP11
LNA/PA
8500-641-024 V01.01
ANT
J2
J1 IN
J3 OUT
JP1
ST8500-641-023 V01.01
TRANSMIT ONLY
RF
J7
TX
8500-641-021 V05.10
J10
J9
J8
LO
C19
JP2
C13
FROM FIG.44A
4402
C4
L2
U1
R5
R2
R4
R10
R9
C8
C7
L3
L4
C12
J8
C3
U5
R11
C11
J12
L1
C1
C2
U3
J11
FROM FIG.44A

FIG. 44B

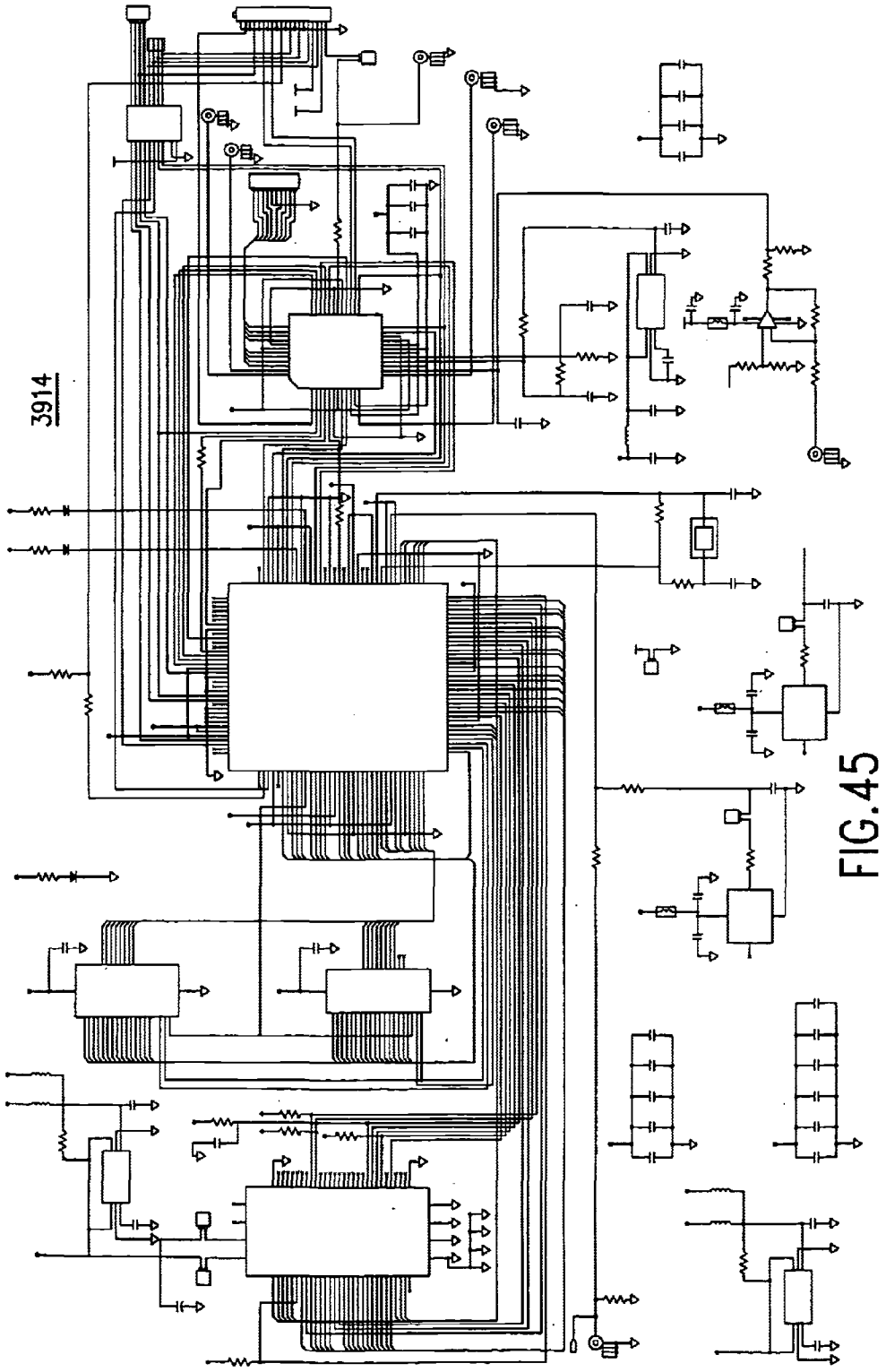


FIG.45

Item	Quantity	Reference	Part Description	Part Number	Manufacturer
1	1	C123	10uF CAP 6032, TANTALUM, 20%	TAJT106K010R	KEMET
2	3	C263, C273, C275, C282	4.7uF CAP 6032, TANTALUM, 20%	T491A475M006AS	KEMET
3	25	C120, C125, C126, C127, C128, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C147, C148, C149, C264, C272, C274, C279, C280, C281, C283	0.1uF CAP 0603, X7R, 10%	GRM39X7R104K050AD	MURATA
4	3	C146, C269, C276	.01uF CAP 0603, X7R, 10%	GRM39X7R103K050AD	MURATA
5	5	C124, C132, C133, C271, C278	100pF CAP 0603, X7R, 10%	GRM39COG101K050AD	MURATA
6	1	C129	47pF CAP 0603, X7R, 10%	GRM39COG470J100AD	MURATA
7	2	C270, C277	27pF CAP 0603, X7R, 10%	GRM39COG270K050AD	MURATA
8	1	C130	22pF CAP 0603, X7R, 10%	GRM39COG220K050AD	MURATA
9	1	C131	10pF CAP 0603, X7R, 10%	GMR39COG100D050AD	MURATA
10	1	DS1	LED GREEN	597-3311-420	DIALIGHT
11	1	DS2	LED YELLOW	597-3401-420	DIALIGHT
12	1	DS3	LED RED	597-3111-420	DIALIGHT
13	6	JP12, JP13, JP14, JP15, JP16, JP17	CONNECTOR HEADER 2PIN	2MS-19-33-01	SPECIALITY ELECTRONICS
14	1	JP11	CONNECTOR HEADER 4PIN	100/VH/TM1SQ/W.100/4	BLKCON

FIG.46A

15	7	J16, J20, J21, J22, J23, J24, J25	CONNECTOR 82MMCX	82MMCX-50-0-1	HUBER/SHUNER		
16	1	J18	CONNECTOR HEADER 10	TMS-110-01-G-S	SAMTEC		
17	1	J19	CONNECTOR WITH EJECTOR	EHT-1-10-01-S-D	SAMTEC		
18	1	P1	CONNECTOR 34X2PCMCIA	DICMJ-68S-SPC-M08	ITT CANON		
19	7	L59, L60, L61, L63, L64, L65, L66	FERRITE BEAD	BLM11A121S	MURATA		
20							
21	1	R112	10M, RESISTOR, 0603, 5%				
22	1	R114	390K, RESISTOR, 0603, 5%	ERJ-3GSYJ394V	PANASONIC		
23	1	R105	100K, RESISTOR, 0603, 5%	ERJ-3GSYJ104V	PANASONIC		
24	4	R106, R107, R108, R111	15K, RESISTOR, 0603, 5%	ERJ-3GSYJ153V	PANASONIC		
25	1	R116	9.1K, RESISTOR, 0603, 5%	ERJ-3GSYJ912V	PANASONIC		
26	1	R115	8.2K, RESISTOR, 0603, 5%	ERJ-3GSYJ822V	PANASONIC		
27	1	R113	3.9K, RESISTOR, 0603, 5%	ERJ-3GSYJ392V	PANASONIC		
28	1	R101	750, RESISTOR, 0630, 5%	ERJ-3GSYJ751V	PANASONIC		
29	1	R110	560, RESISTOR, 0603, 5%	ERJ-3GSYJ561V	PANASONIC		
30	2	R99, R100	330, RESISTOR, 0603, 5%	ERJ-3GSYJ331V	PANASONIC		
31	1	R119	50, RESISTOR, 0603, 5%	ERJ-3GSYJ500V	PANASONIC		
32	2	R128, R129	10, RESISTOR, 0603, 5%	ERJ-3GSYJ100V	PANASONIC		
33	8	R102, R103, R104, R109, R117, R118, R120, R127,	0, RESISTOR, 0603, 5%	RM732Z1J000ZT	ERJ KOA		
				3GSYJ000V	PANASONIC		
34	6	R121, R122, R123, R124, R125, R126	TBD, RESISTOR, 0603, 5%	R	PANASONIC		
35	1	U10	SRAM	KM62256DLTG-5L	SAMSUNG		
				M5M5256CVP-55LL	MITSUBUSHI		
36	1	U12	MAC	AM79C930	AMD		

FIG.46B

37	1	U13	BASEBAND PROCESSOR	HFA3842A1	HARRIS
38	1	U14	FLASH RAM	AM29F010-55EC	AMD
39	1	U15	32 KHz CRYSTAL	CX-6V-SM2-32.768KHzC/1	STATEK
40	2	U45	BUS BUFFER	DS3862	NATIONAL
41	1	U48	REGULATOR 3.5 V	TK11235BMC	TOKO
42	1	U49	22MHz OSCILLATOR	FOX F3346-22MHz	FOX
43	1	U50	2 VOLT REFERENCE	TK11220BMC	TOKO
44	1	U51	40MHz OSCILLATOR	CXO-M-10N-40MHz A/1	STATEK

FIG.46C

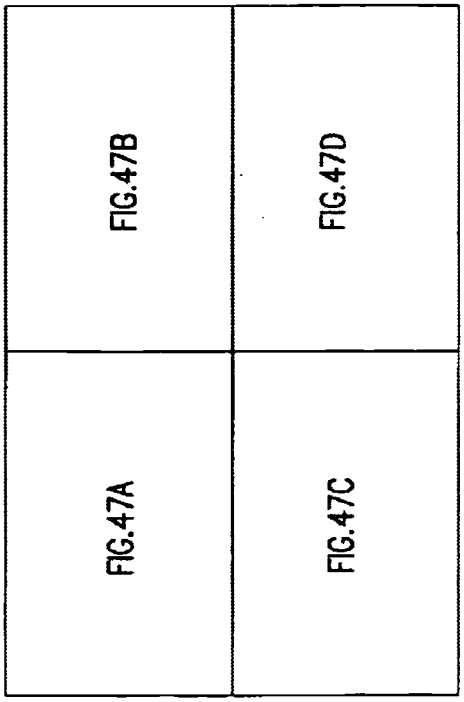


FIG. 47

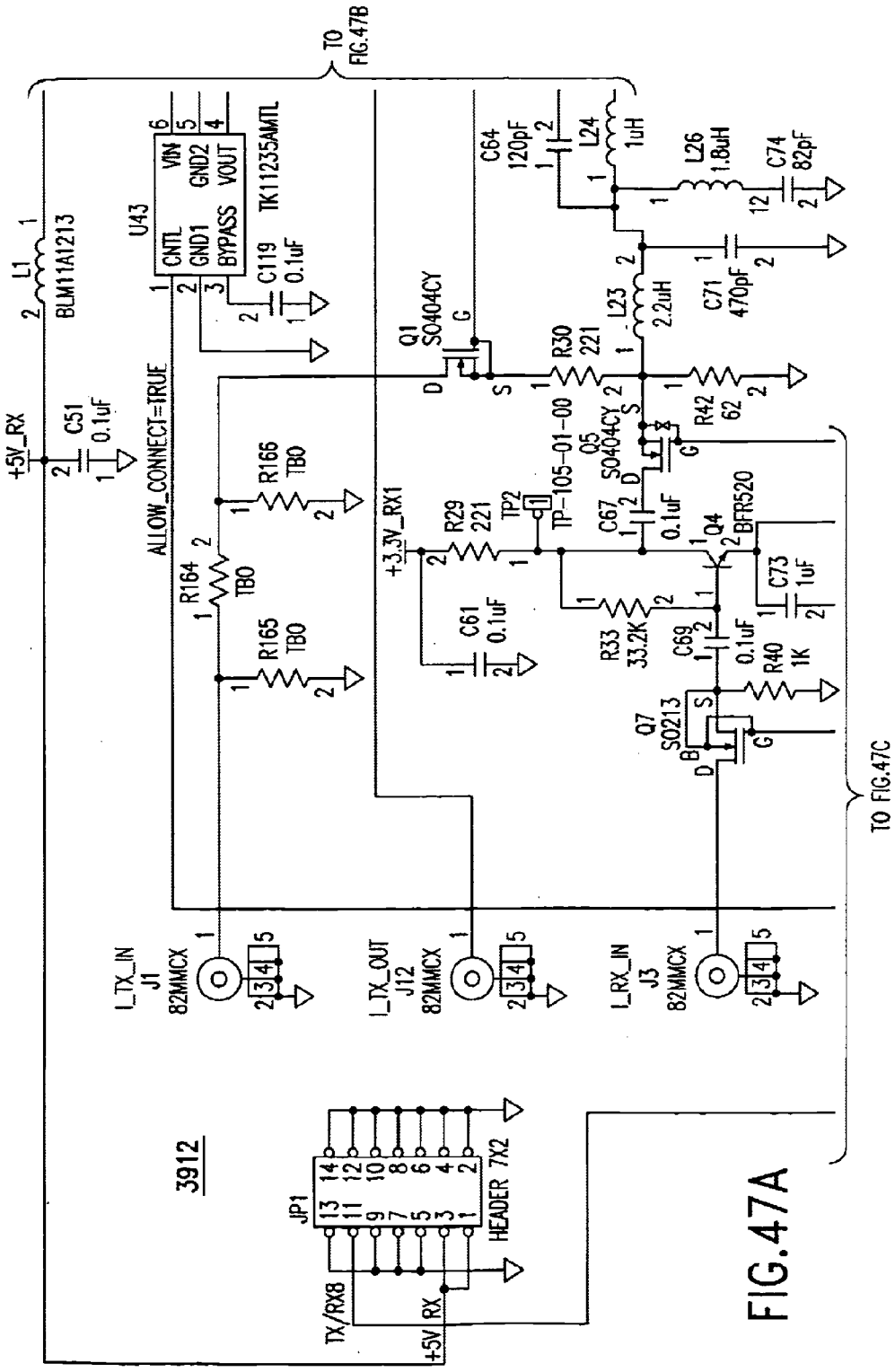

TO FIG.47B
TO FIG.47C
3912
+5V_RX
C51 0.1uF
L1 BLM11A1213
U43 TK11235AMTL
CNTL GND1 BYPASS VIN GND2 VOUT
C119 0.1uF
ALLOW_CONNECT=TRUE
R166 TBO
R164 TBO
R165 TBO
+3.3V_RX1
R29 221
TP2 TP-105-01-00
C61 0.1uF
Q1 SO404CY
R30 221
C64 120pF
L24 1uH
L26 1.8uH
C74 82pF
L23 2.2uH
C71 470pF
Q5 SO404CY
R42 62
C67 0.1uF
Q4 BFR520
C73 1uF
R33 33.2K
C69 0.1uF
R40 1K
Q7 SO213
L_TX_IN J1 82MMCX
L_TX_OUT J12 82MMCX
L_RX_IN J3 82MMCX
JP1 HEADER 7X2
TX/RX8
RX
+5V

FIG.47A

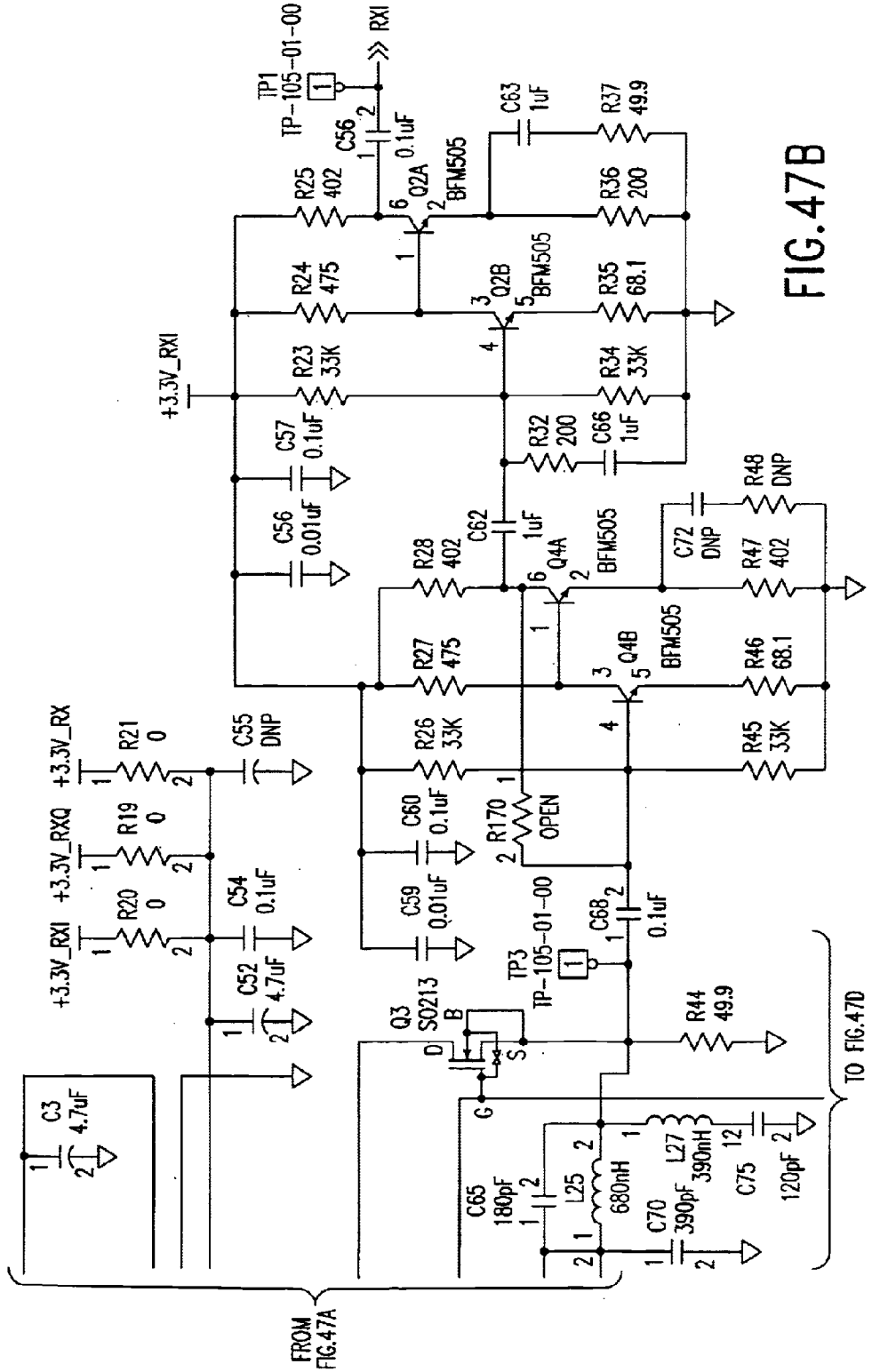

TP1
TP-105-01-00
RXI
C56 0.1uF
C63 1uF
R37 49.9
R25 402
Q2A BFM505
R36 200
R24 475
Q2B BFM505
R35 68.1
+3.3V_RXI
R23 33K
R34 33K
C57 0.1uF
R32 200
C66 1uF
C56 0.01uF
C62 1uF
R48 DNP
C72 DNP
R28 402
Q4A BFM505
R47 402
R27 475
Q4B BFM505
R46 68.1
+3.3V_RX
R21 0
C55 DNP
R26 33K
R45 33K
+3.3V_RXQ
R19 0
C60 0.1uF
R170 OPEN
+3.3V_RXI
R20 0
C54 0.1uF
C59 0.01uF
C68 0.1uF
C52 4.7uF
TP3
TP-105-01-00
Q3 SO213
R44 49.9
C3 4.7uF
C65 180pF
L25 680nH
C70 390pF
L27 390nH
C75 120pF
FROM FIG.47A
TO FIG.47D

FIG.47B

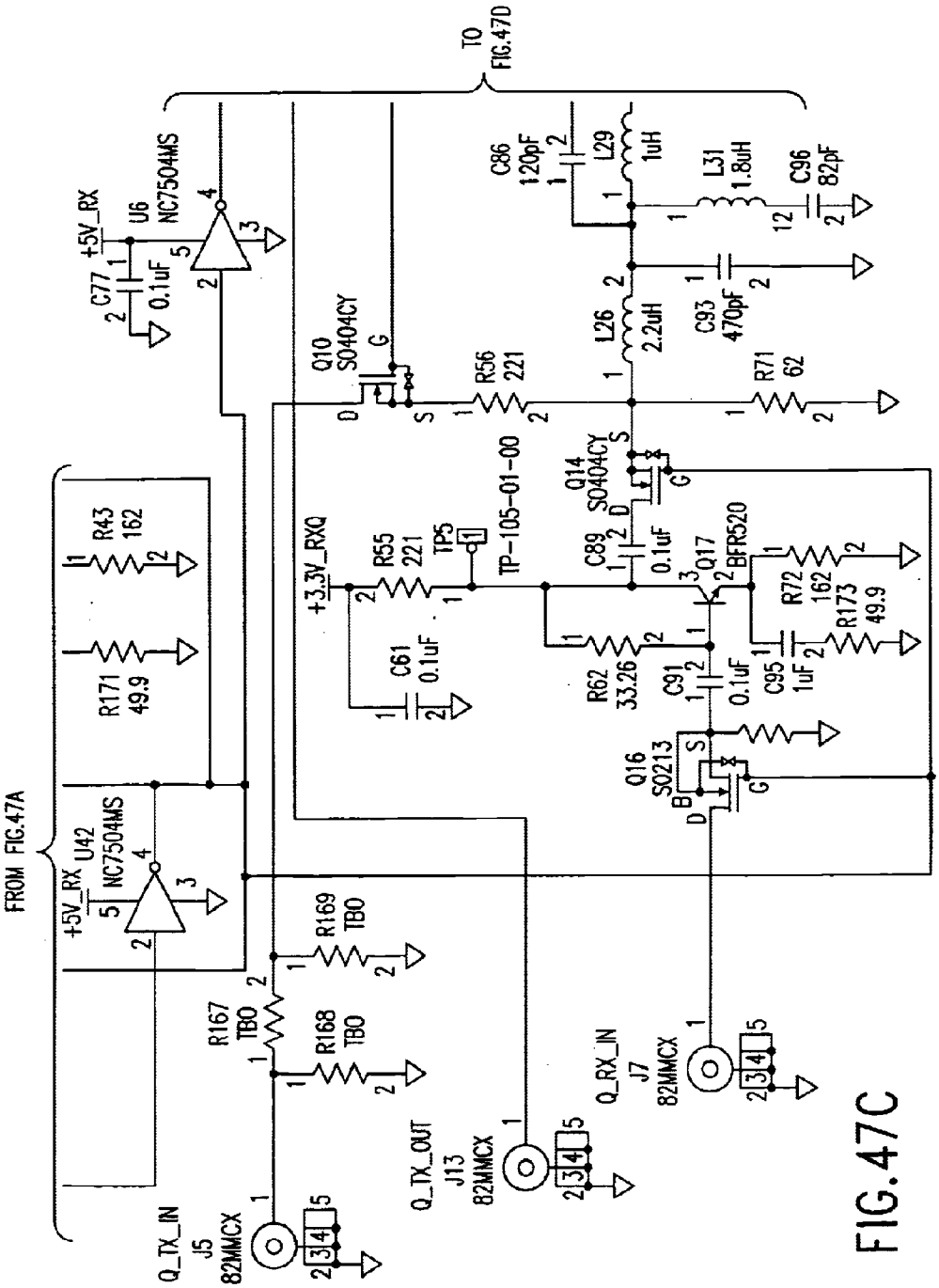

TO FIG.47D
FROM FIG.47A
+5V_RX
U6 NC7504MS
C77 0.1uF
U42 NC7504MS
R43 162
R171 49.9
Q10 SO404CY
R56 221
L26 2.2uH
C86 120pF
L29 1uH
L31 1.8uH
C96 82pF
C93 470pF
R71 62
Q14 SO404CY
+3.3V_RXQ
R55 221
TP5 TP-105-01-00
C89 0.1uF
Q17 BFR520
R72 162
R173 49.9
C61 0.1uF
R62 33.26
C91 0.1uF
C95 1uF
Q16 SO213
R169 TBO
R167 TBO
R168 TBO
Q_TX_IN J5 82MMCX
Q_TX_OUT J13 82MMCX
Q_RX_IN J7 82MMCX

FIG.47C

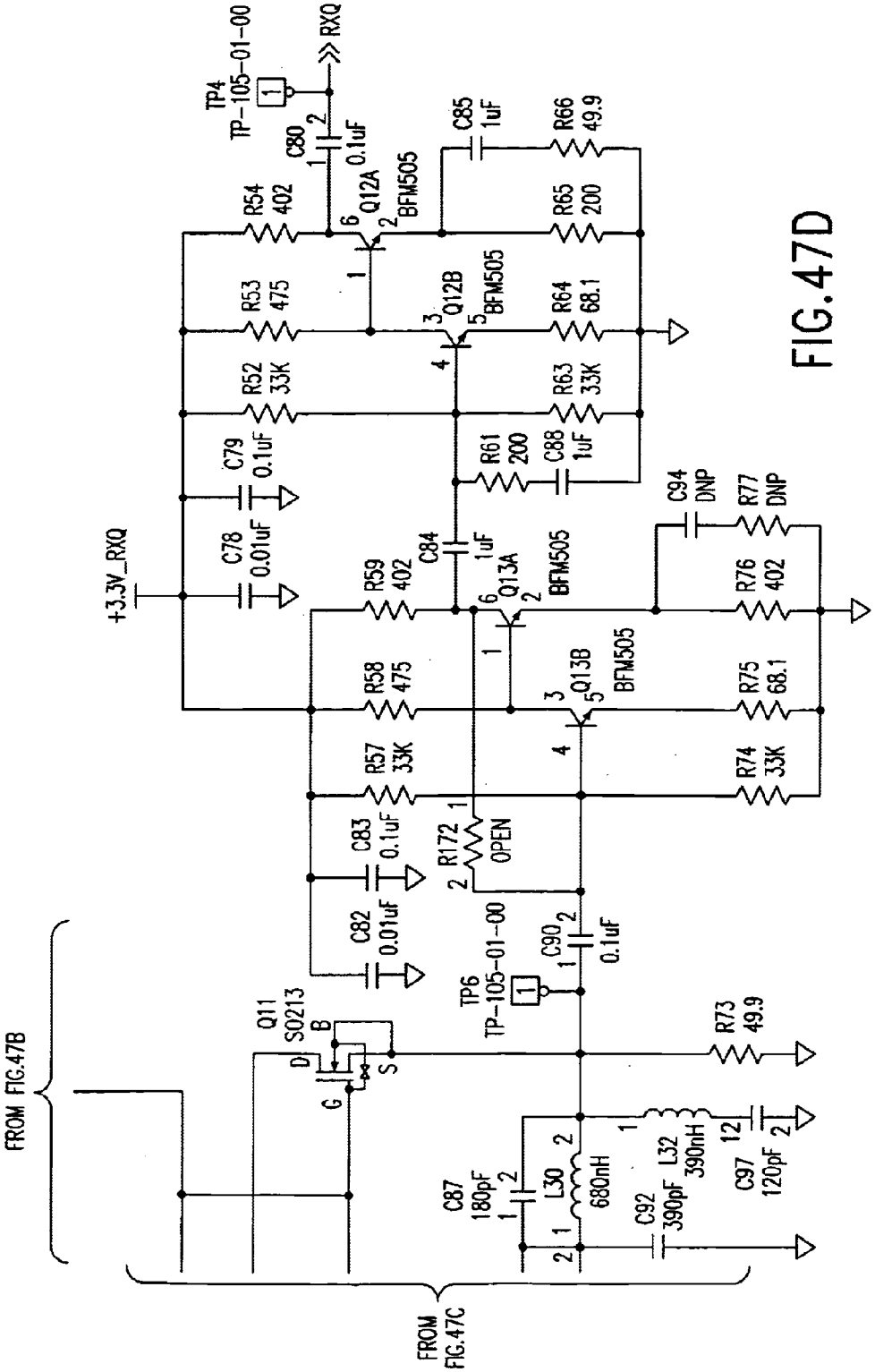

TP4
TP-105-01-00
RXQ
C80
0.1uF
C85
1uF
R66
49.9
R54
402
Q12A
BFM505
R65
200
R53
475
Q12B
BFM505
R64
68.1
R52
33K
R63
33K
C79
0.1uF
R61
200
C88
1uF
C94
DNP
R77
DNP
+3.3V_RXQ
C78
0.01uF
C84
1uF
R59
402
Q13A
BFM505
R76
402
R58
475
Q13B
BFM505
R75
68.1
R57
33K
R74
33K
C83
0.1uF
R172
OPEN
C82
0.01uF
C90
0.1uF
TP6
TP-105-01-00
Q11
SO213
R73
49.9
FROM FIG.47B
C87
180pF
L30
680nH
C92
390pF
L32
390nH
C97
120pF
FROM FIG.47C

FIG.47D

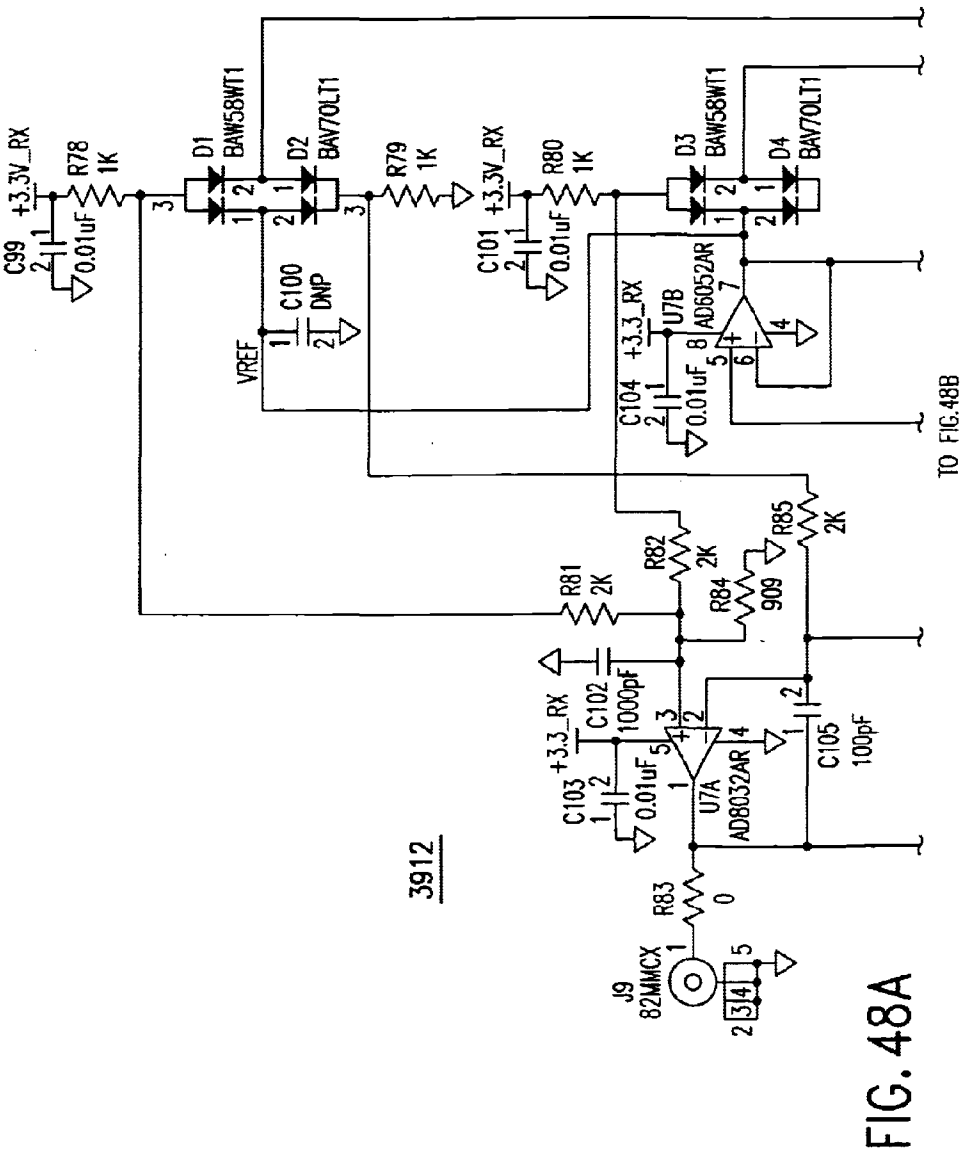

3912
+3.3V_RX
R78 1K
C99 0.01uF
D1 BAW56WT1
D2 BAV70LT1
R79 1K
C100 DNP
VREF
+3.3V_RX
R80 1K
C101 0.01uF
D3 BAW56WT1
D4 BAV70LT1
U7B AD8052AR
+3.3_RX
C104 0.01uF
TO FIG.48B
R81 2K
R82 2K
R84 909
R85 2K
C102 1000pF
+3.3_RX
C103 0.01uF
U7A AD8032AR
C105 100pF
R83 0
J9 82MMCX

FIG. 48A

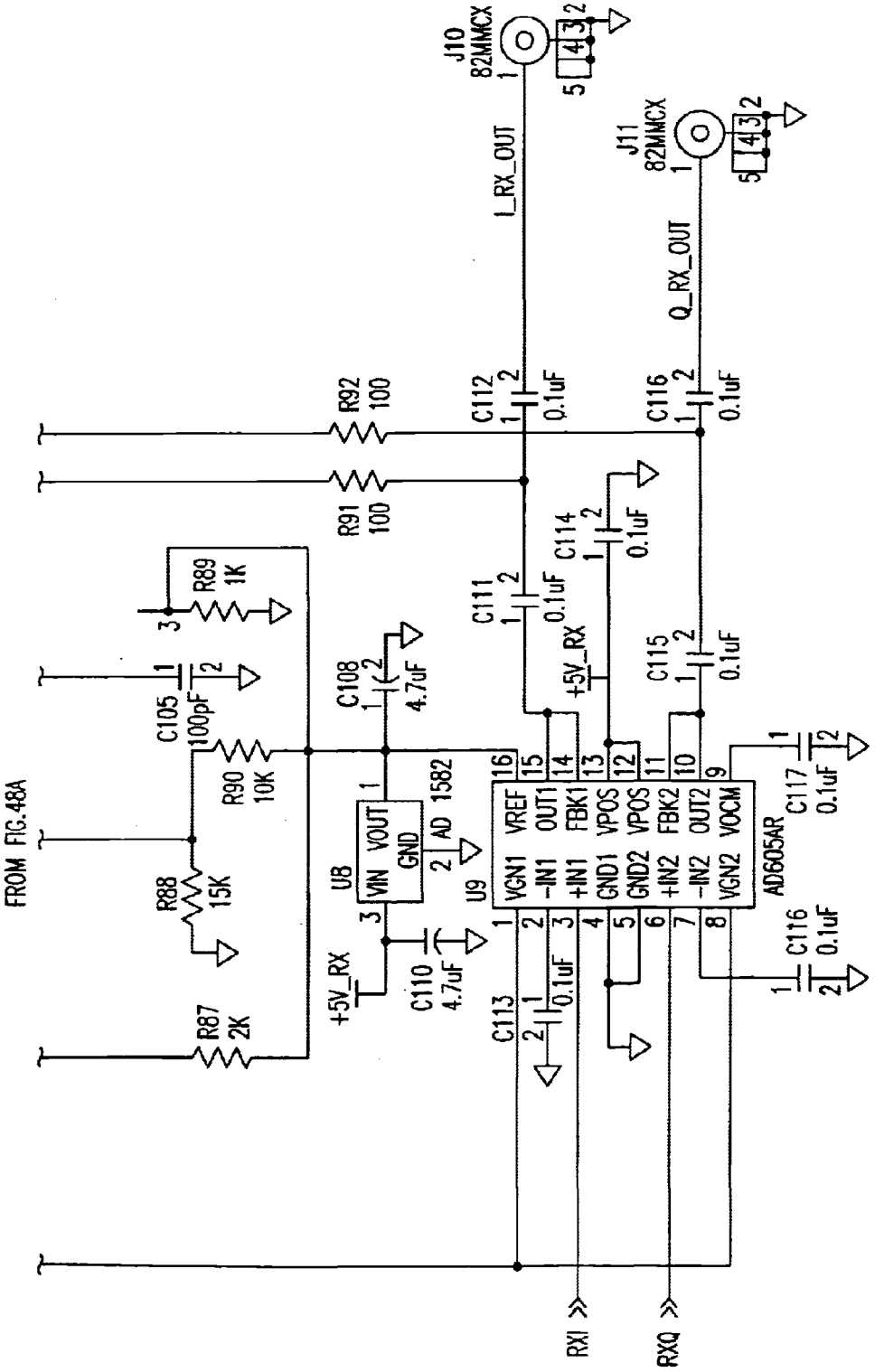

J10
82MMCX
J11
82MMCX
I_RX_OUT
Q_RX_OUT
R92 100
R91 100
C112 0.1uF
C116 0.1uF
C111 0.1uF
C114 0.1uF
C115 0.1uF
C117 0.1uF
R89 1K
C105 100pF
C108 4.7uF
R90 10K
R88 15K
R87 2K
C110 4.7uF
C113 0.1uF
+5V_RX
FROM FIG.48A
U8
AD 1582
VIN VOUT GND
U9
AD605AR
VREF OUT1 FBK1 VPOS VPOS FBK2 OUT2 VOCM
VGN1 -IN1 +IN1 GND1 GND2 +IN2 -IN2 VGN2
RXI
RXQ

FIG. 48B

FIG.49A

ITEM	QUANT.	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	4	C3,C52,C108,C110	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61, C67,C68,C69,C77,C79,C80, C81,C83,C89,C90,C91,C111, C112,C113,C114,C115,C116, C117,C118,C119	0.1uF	GRM39Y5V104Z016	MURATA
3	1	C55	DNP	T491A475K006AS	KEMET
4	8	C56,C59,C78,C82,C99,C101, C103,C104	0.01uF	GRM39X7R103K050	MURATA
5	8	C62,C63,C66,C73,C84,C85, C88,C95	1uF	GRM40Y5V105Z016	MURATA
6	4	C64,C75,C86,C97	120pF	GRM39C0G121J050	MURATA
7	2	C65,C87	180pF	GRM39C0C181J050	MURATA
8	2	C70,C92	390pF	GRM39C0G391J050	MURATA
9	2	C71,C93	470pF	GRM39C0G471J050	MURATA
10	2	C72,C94	DNP	GRM40Y5V105Z016	MURATA
11	2	C74,C96	82pF	GRM39C0G820J050	MURATA
12	2	C100,C106	DNP	DNP	MURATA
13	2	C105,C102	1000pF	GRM39C0G102K050	MURATA
14	2	D3,D1	BAW56WT1	BAW56WT1	MOTOROLA
15	2	D4,D2	BAV70LT1	BAV70LT1	MOTOROLA
16	1	JP1	HEADER 7X2	FTSH-107-02-L-D	SAMTEC
17	9	J1,J3,J5,J7,J9,J10,J11, J12,J13	82MMCX	82MMCX-50-0-1	SUHNER
18	1	L1	BLM11A121S	BLM11A121S	MURATA
19	2	L23,L28	2.2uH	LQG21N2R2K10	MURATA
20	2	L29,L24	1uH	LQG21N1R0K10	MURATA
21	2	L30,L25	680nH	LQG21NR68K10	MURATA

FIG.49B

22	2	L26,L31	1.8uH	LQG21N1R8K10	MURATA	
23	2	L32,L27	390nH	LQG21NR39K10	MURATA	
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	CALOGIC	
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	PHILIPS	
26	4	Q3,Q7,Q11,Q16	SD213	SD213	CALOGIC	
27	2	Q17,Q8	BFR520	BFR520	PHILIPS	
28	4	R19,R20,R21,R83	0	ERJ3GSY0R00	PANASONIC	
29	8	R23,R26,R34,R45,R52,R57, R63,R74	33K	ERJ3GSYJ333	PANASONIC	
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	PANASONIC	
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	PANASONIC	
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	PANASONIC	
33	2	R32,R61	200	ERJ3GSYJ201	PANASONIC	
34	2	R33,R62	33.2K	ERJ3GSYJ333	PANASONIC	
35	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	PANASONIC	
36	2	R36,R65	200	ERJ3EKF2000	PANASONIC	
37	6	R37,R44,R66,R73,R171, R173	49.9	ERJ3EKF49R9	PANASONIC	
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	PANASONIC	
39	2	R42,R71	62	ERJ3EGSYJ620	PANASONIC	
40	2	R43,R72	162	ERJ3EKF1620	PANASONIC	
41	2	R77,R48	DNP	ERJ3GSYJ330	PANASONIC	
42	4	R81,R82,R85,R87	2K	ERJ3EKF2001	PANASONIC	
43	1	R84	909	ERJ3EKF9090	PANASONIC	
44	1	R88	15K	ERJ3EJF1502	PANASONIC	
45	1	R90	10K	ERJ3EKF1002	PANASONIC	
46	2	R91,R92	100	ERJ3EKF1000	PANASONIC	
47	6	R164,R165,R166,R167,R168, R169	TBD		PANASONIC	
48	2	R170,R172	OPEN		PANASONIC	

FIG.49C

49	6	TP1, TP2, TP3, TP4, TP5, TP6	TP-105-01-00		
50	2	U42, U6	NC7S04M5	NC7S04M5	NATIONAL SEMICONDUCTOR
51	1	U7	AD8052AR	AD8052AR	ANALOG DEVICES
52	1	U8	AD1582	AD1582	ANALOG DEVICES
53	1	U9	AD605AR	AD605AR	ANALOG DEVICES
54	1	U43	TK11235AMTL	TK11235BM	TOKO
55	1		BOARD	8500.541.003.V13.01	

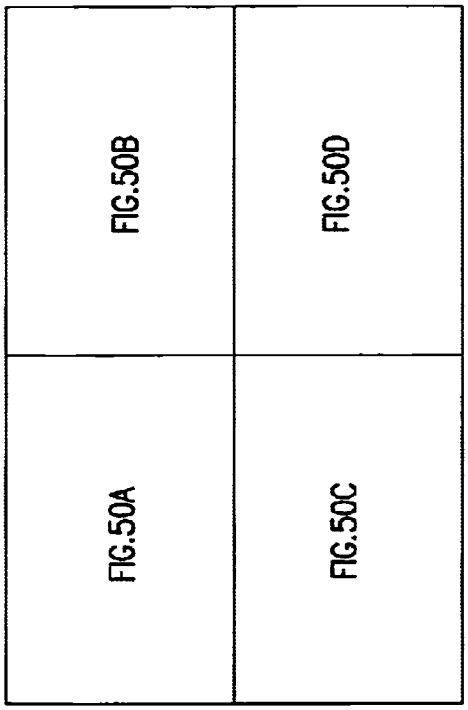


FIG. 50

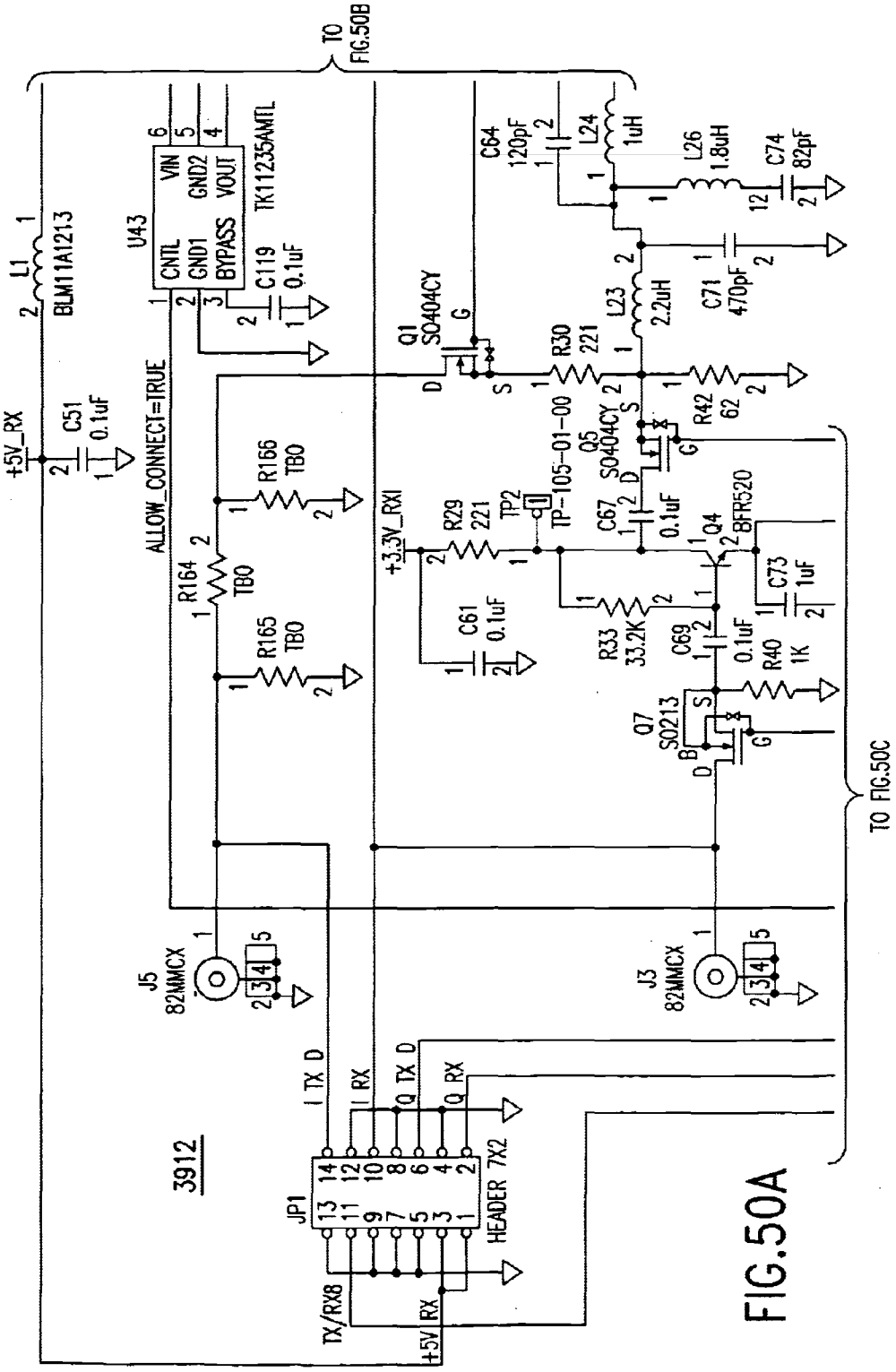

TO FIG.50B
+5V_RX
C51 0.1uF
L1 BLM11A1213
U43 TK11235AMTL
CNTL
GND1
BYPASS
VIN
GND2
VOUT
C119 0.1uF
ALLOW_CONNECT=TRUE
Q1 SO404CY
C64 120pF
L24 1uH
L26 1.8uH
C74 82pF
L23 2.2uH
C71 470pF
R30 221
R42 62
Q5 SO404CY
TP-105-01-00
TP2
R166 TBO
R164 TBO
R165 TBO
+3.3V_RXI
R29 221
C67 0.1uF
Q4 BFR520
C73 1uF
C61 0.1uF
R33 33.2K
C69 0.1uF
R40 1K
Q7 SO213
J5 82MMCX
J3 82MMCX
TX D
RX
TX D
RX
JP1 HEADER 7X2
TX/RX8
+5V
RX
3912
TO FIG.50C

FIG.50A

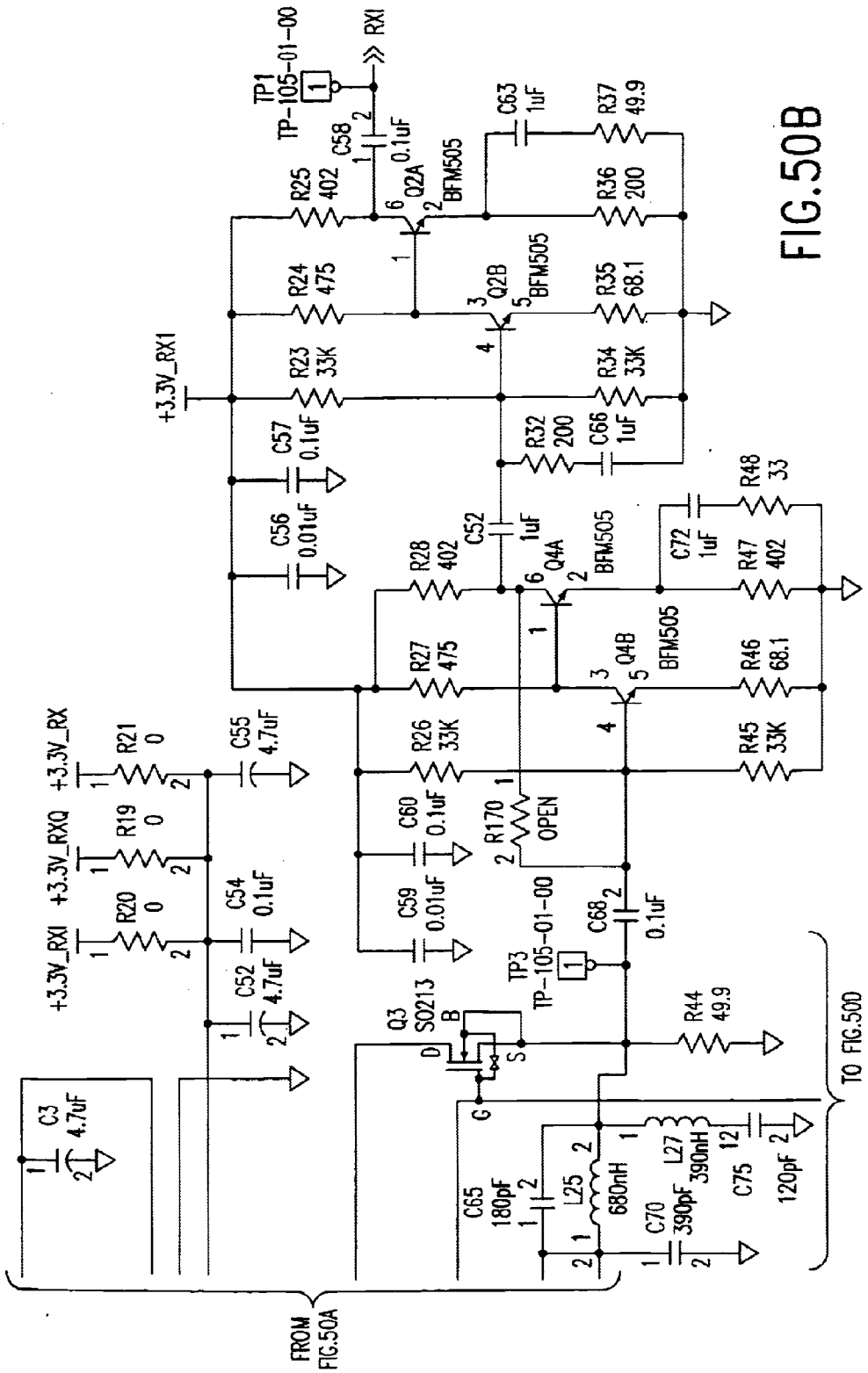

TP1
TP-105-01-00
RXI
C58
0.1uF
C63
1uF
R37
49.9
R25
402
Q2A
BFM505
R36
200
R24
475
Q2B
BFM505
R35
68.1
+3.3V_RXI
R23
33K
R34
33K
C57
0.1uF
R32
200
C66
1uF
C56
0.01uF
C52
1uF
R48
33
R28
402
Q4A
BFM505
C72
1uF
R47
402
R27
475
Q4B
BFM505
R46
68.1
+3.3V_RX
R21
0
C55
4.7uF
R26
33K
R45
33K
+3.3V_RXQ
R19
0
C60
0.1uF
R170
OPEN
+3.3V_RXI
R20
0
C54
0.1uF
C59
0.01uF
C68
0.1uF
C52
4.7uF
TP3
TP-105-01-00
Q3
SO213
R44
49.9
C3
4.7uF
C65
180pF
L25
680nH
C70
390pF
L27
390nH
C75
120pF
FROM FIG.50A
TO FIG.50D

FIG.50B

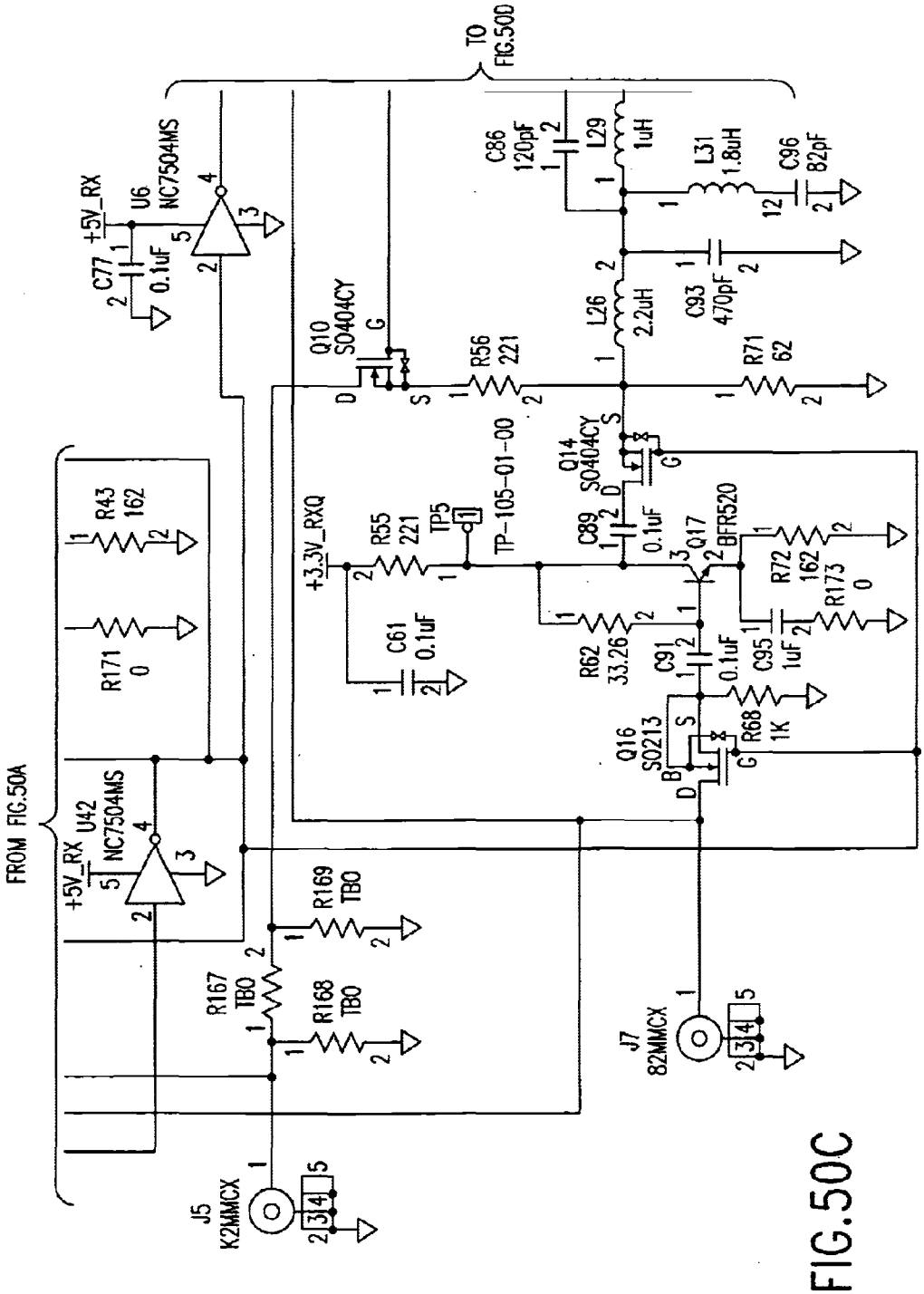

TO FIG.50D
FROM FIG.50A
+5V_RX
U6 NC7504MS
U42 NC7504MS
C77 0.1uF
C86 120pF
L29 1uH
L31 1.8uH
C96 82pF
C93 470pF
L26 2.2uH
Q10 SO404CY
Q14 SO404CY
R56 221
R71 62
R43 162
R171 0
+3.3V_RXQ
R55 221
TP5
TP-105-01-00
C89 0.1uF
Q17 BFR520
R72 162
R173 0
C61 0.1uF
R62 33.26
C91 0.1uF
C95 1uF
Q16 SO213
R68 1K
R169 TBD
R167 TBD
R168 TBD
J7 82MMCX
J5 K2MMCX

FIG.50C

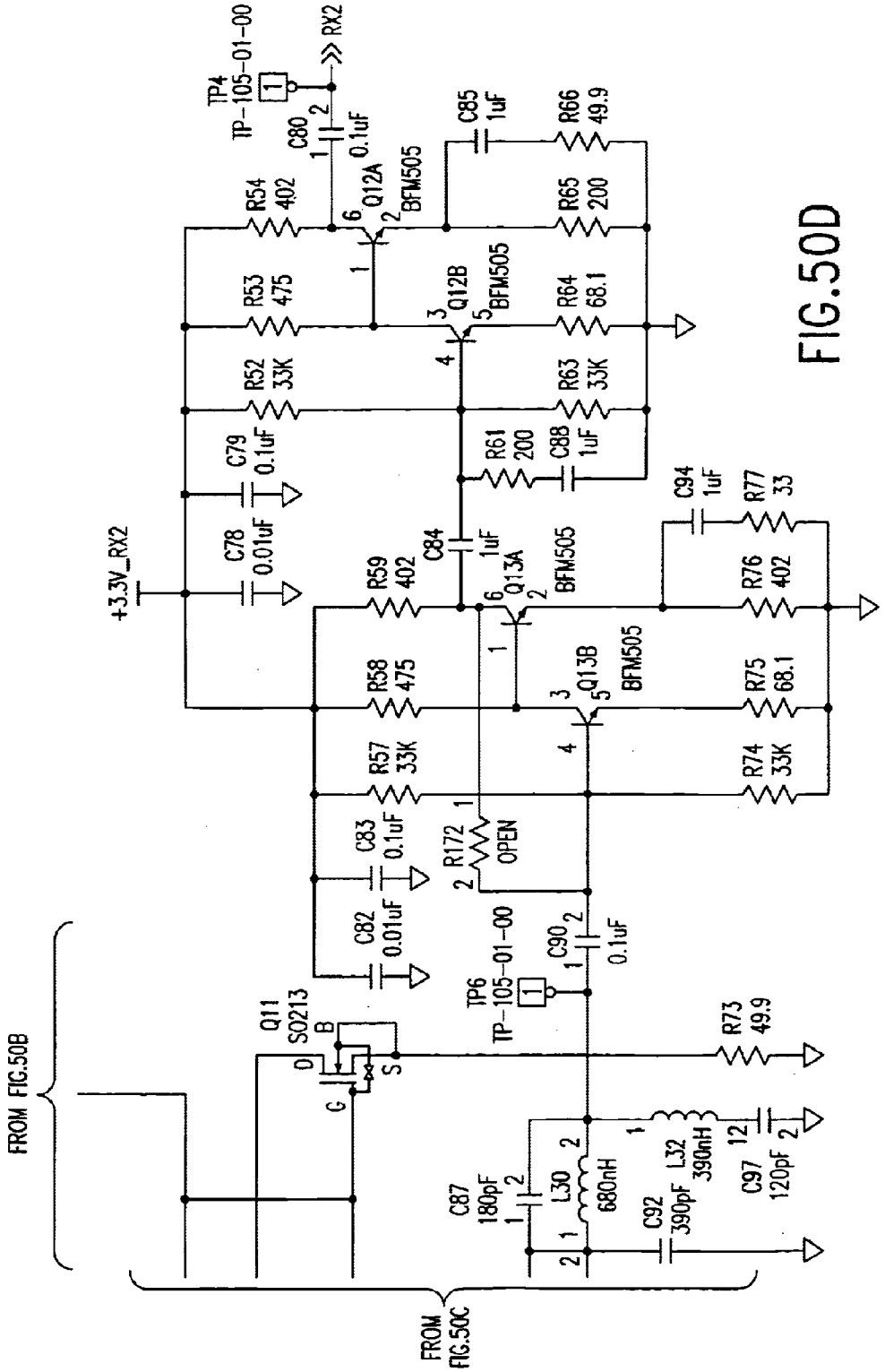

TP4
TP-105-01-00
>> RX2
C80
0.1uF
C85
1uF
R66
49.9
R54
402
Q12A
BFM505
R65
200
R53
475
Q12B
BFM505
R64
68.1
R52
33K
R63
33K
C79
0.1uF
R61
200
C88
1uF
C94
1uF
R77
33
+3.3V_RX2
C78
0.01uF
C84
1uF
R59
402
Q13A
BFM505
R76
402
R58
475
Q13B
BFM505
R75
68.1
R57
33K
R74
33K
C83
0.1uF
R172
OPEN
C82
0.01uF
C90
0.1uF
TP6
TP-105-01-00
Q11
SO213
R73
49.9
FROM FIG.50B
C87
180pF
L30
680nH
C92
390pF
L32
390nH
C97
120pF
FROM FIG.50C

FIG.50D

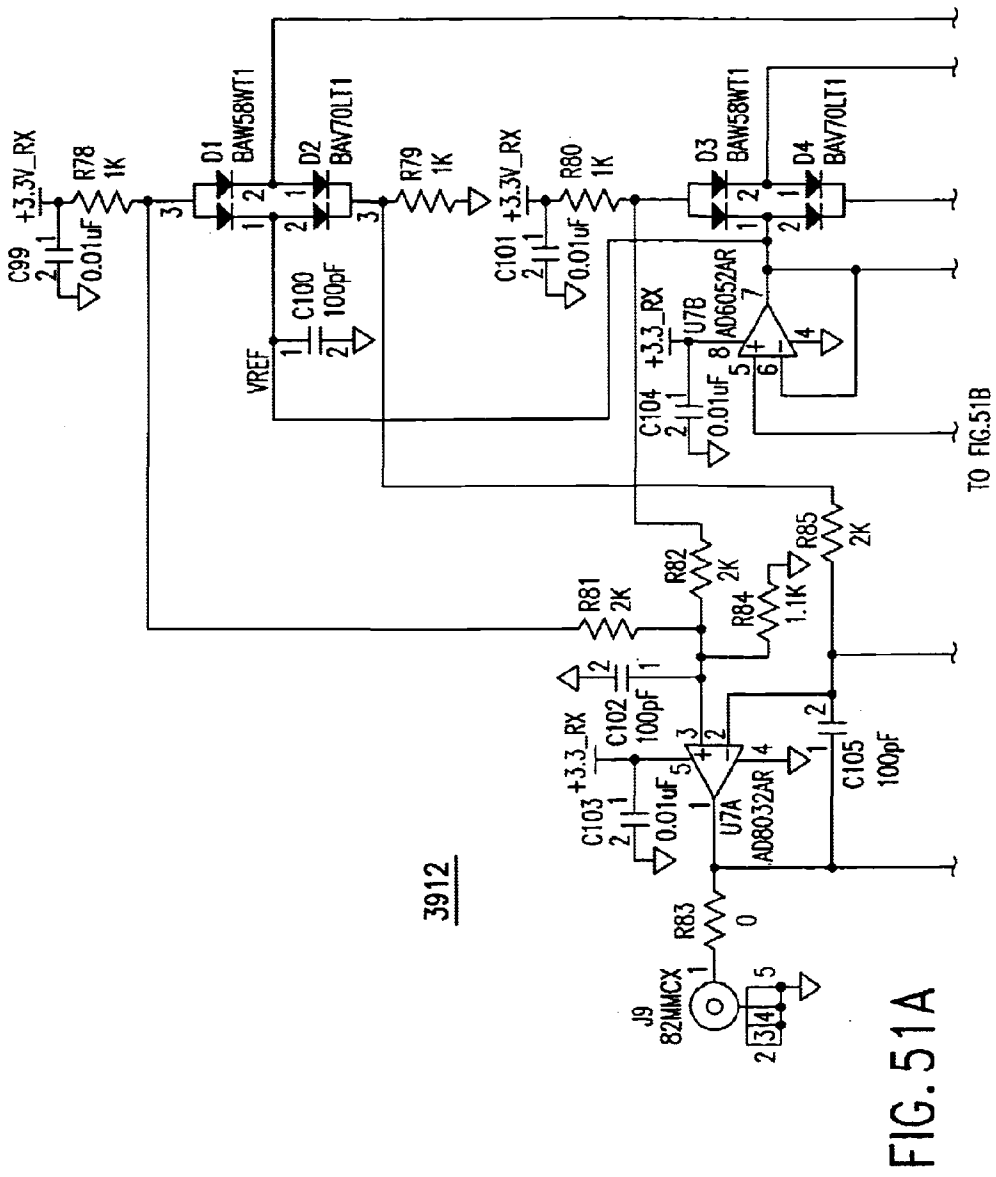

+3.3V_RX
R78 1K
C99 0.01uF
D1 BAW56WT1
D2 BAV70LT1
R79 1K
+3.3V_RX
R80 1K
C101 0.01uF
D3 BAW56WT1
D4 BAV70LT1
VREF
C100 100pF
+3.3_RX
U7B AD6052AR
C104 0.01uF
TO FIG.51B
R85 2K
R82 2K
R84 1.1K
R81 2K
C102 100pF
+3.3_RX
C103 0.01uF
U7A AD8032AR
C105 100pF
3912
R83 0
J9 82MMCX

FIG. 51A

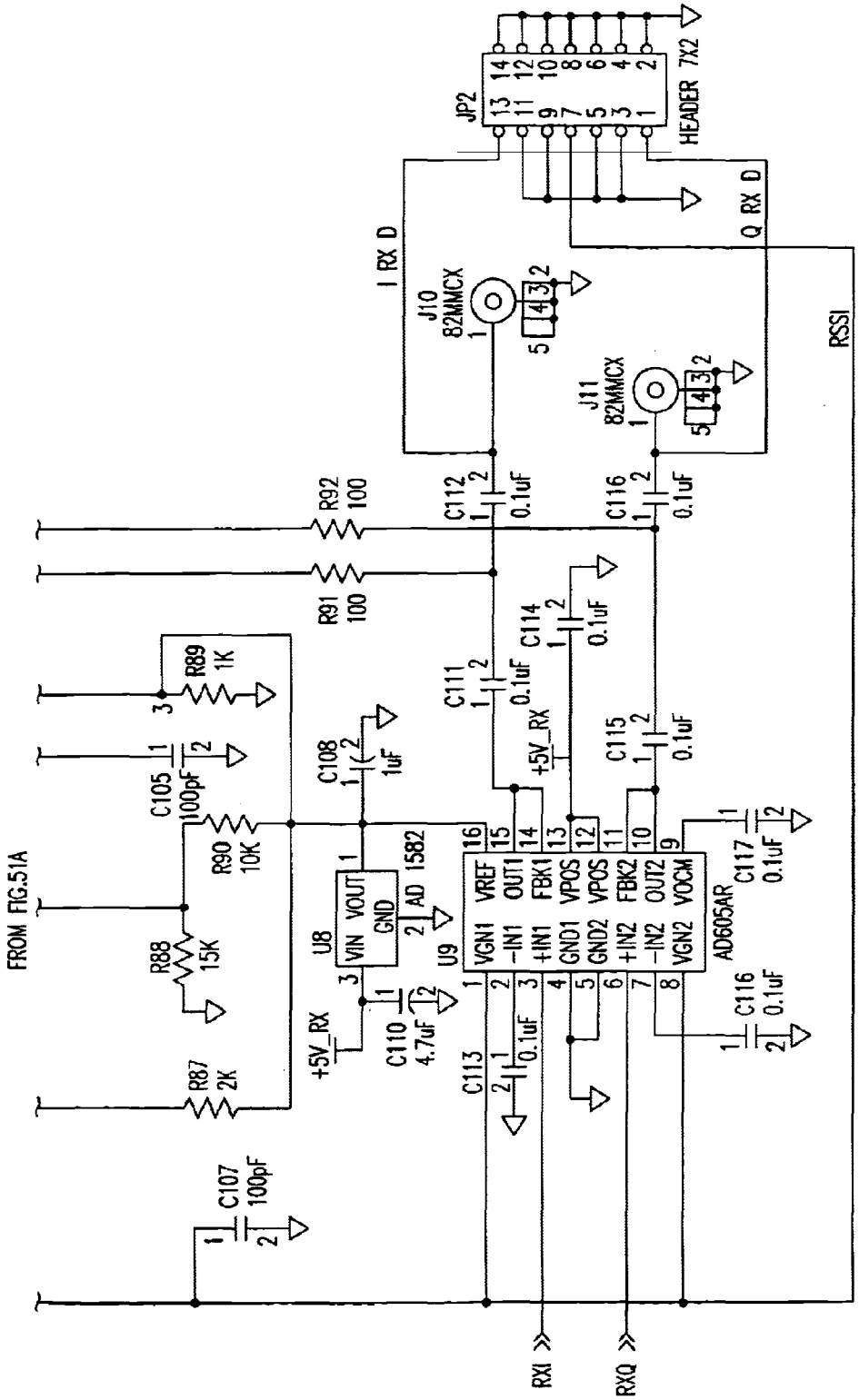

JP2
HEADER 7X2
I RX D
Q RX D
RSSI
J10
82MMCX
J11
82MMCX
R92
100
R91
100
C112
0.1uF
C116
0.1uF
C114
0.1uF
C111
0.1uF
C115
0.1uF
R89
1K
C105
100pF
C108
1uF
+5V_RX
R90
10K
R88
15K
R87
2K
C107
100pF
C110
4.7uF
C113
0.1uF
C117
0.1uF
C116
0.1uF
U8
AD 1582
VIN VOUT GND
U9
AD605AR
VREF OUT1 FBK1 VPOS VPOS FBK2 OUT2 VOCM
VGN1 -IN1 +IN1 GND1 GND2 +IN2 -IN2 VGN2
FROM FIG.51A
RXI
RXQ

FIG. 51B

FIG.52A

ITEM	QTY	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	3	C3,C52,C55	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61, C67,C68,C69,C77,C79,C80, C81,C83,C89,C90,C91,C111, C112,C113,C114,C115,C116, C117,C118,C119	0.1uF	GRM39Y5V104Z016	MURATA
3	8	C56,C59,C78,C82,C99,C101, C103,C104	0.01uF	GRM39X7R103K050	MURATA
4	10	C62,C63,C66,C72,C73,C84, C85,C88,C94,C95	1uf	GRM40Y5V105Z016	MURATA
5	4	C64,C75,C86,C97	120pF	GRM39C0G121J050	MURATA
6	2	C87,C65	180pF	GRM39C0G181J050	MURATA
7	2	C70,C92	390pF	GRM39C0G391J050	MURATA
8	2	C71,C93	470pF	GRM39C0G471J050	MURATA
9	2	C96,C74	82pF	GRM39C0G820J050	MURATA
10	5	C100,C102,C105,C106,C107	100pF	GRM39C0G101K050	MURATA
11	1	C108	1uF		
12	1	C110	4.7uF		
13	2	D3,D1	BAW56WT1	BAW56WT1	MOTOROLA
14	2	D4,D2	BAV70LT1	BAV70LT1	MOTOROLA
15	2	JP2,JP1	HEADER 7X2		
16	6	J1,J3,J5,J7,J10,J11	82MMCX	142-0701-231	JOHNSON
17	1	J9	82MMCX	82MMCX-50-0-1	SUHNER
18	1	L1	BLM11A121S	BLM11A121S	MURATA
19	2	L28,L23	2.2uH	LQG21N2R2K10	MURATA
20	2	L24,L29	1uH	LQG21N1R0K10	MURATA
21	2	L30,L25	680nH	LQG21NR68K10	MURATA
22	2	L26,L31	1.8uH	LQG21N1R8K10	MURATA

FIG.52B

23	2	L27,L32	390nH	LQG21NR39K10	MURATA	
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	CALOGIC	
25	4	Q2,Q4,Q12,Q13	BFW505	BFW505	PHILIPS	
26	4	Q3,Q7,Q11,Q16	SD213	SD213	CALOGIC	
27	2	Q17,Q8	BFR520	BFR505	PHILIPS	
28	5	R19,R20,R21,R171,R173	0			
29	8	R23,R26,R34,R45,R52,R57, R63,R74	33K	ERJ3GSYJ333	PANASONIC	
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	PANASONIC	
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	PANASONIC	
32	4	R29,R30,R55,R56	221	ERF3EKF2210	PANASONIC	
33	2	R32,R61	200	ERJ3GSYJ201	PANASONIC	
34	2	R33,R62	33.2K	ERJ3GSYJ333	PANASONIC	
35	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	PANASONIC	
36	2	R36,R65	200	ERJ3EKF2000	PANASONIC	
37	2	R66,R37	49.9	ERJ3EKF49R9	PANASONIC	
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	PANASONIC	
39	2	R42,R71	62	ERJ3GSYJ620	PANASONIC	
40	2	R43,R72	162	ERJ3EKF6810	PANASONIC	
41	2	R44,R73	49.9	ERJ3EKF1001	PANASONIC	
42	2	R77,R48	33	ERJ3GSYJ330	PANASONIC	
43	4	R81,R82,R85,R87	2K	ERJ3EKF2001	PANASONIC	
44	1	R83	0	ERJGSY0R00	PANASONIC	
45	1	R84	1.1K	ERJ3EKF2001	PANASONIC	
46	1	R88	15K	ERJ3EKF1502	PANASONIC	
47	1	R90	10K	ERJ3EKF1002	PANASONIC	
48	2	R91,R92	100	ERJ3EKF1000	PANASONIC	
49	6	R164,R165,R166,R167,R168, R169	TBD			
50	2	R170,R172	OPEN			

51	0	TP1, TP2, TP3, TP4, TP5, TP6	TP-105-01-00		
52	2	U42, U6	NC7SO4M5		NATIONAL SEMICONDUCTOR
53	1	U7	AD8032AR	AD8032AR	ANALOG DEVICES
54	1	U8	AD1582	AD1582	ANALOG DEVICES
55	1	U9	AD605AR	AD605AR	ANALOG DEVICES
56	1	U43	TK11235AMTL	TK11235AMTL	TOKO

FIG.52B-1

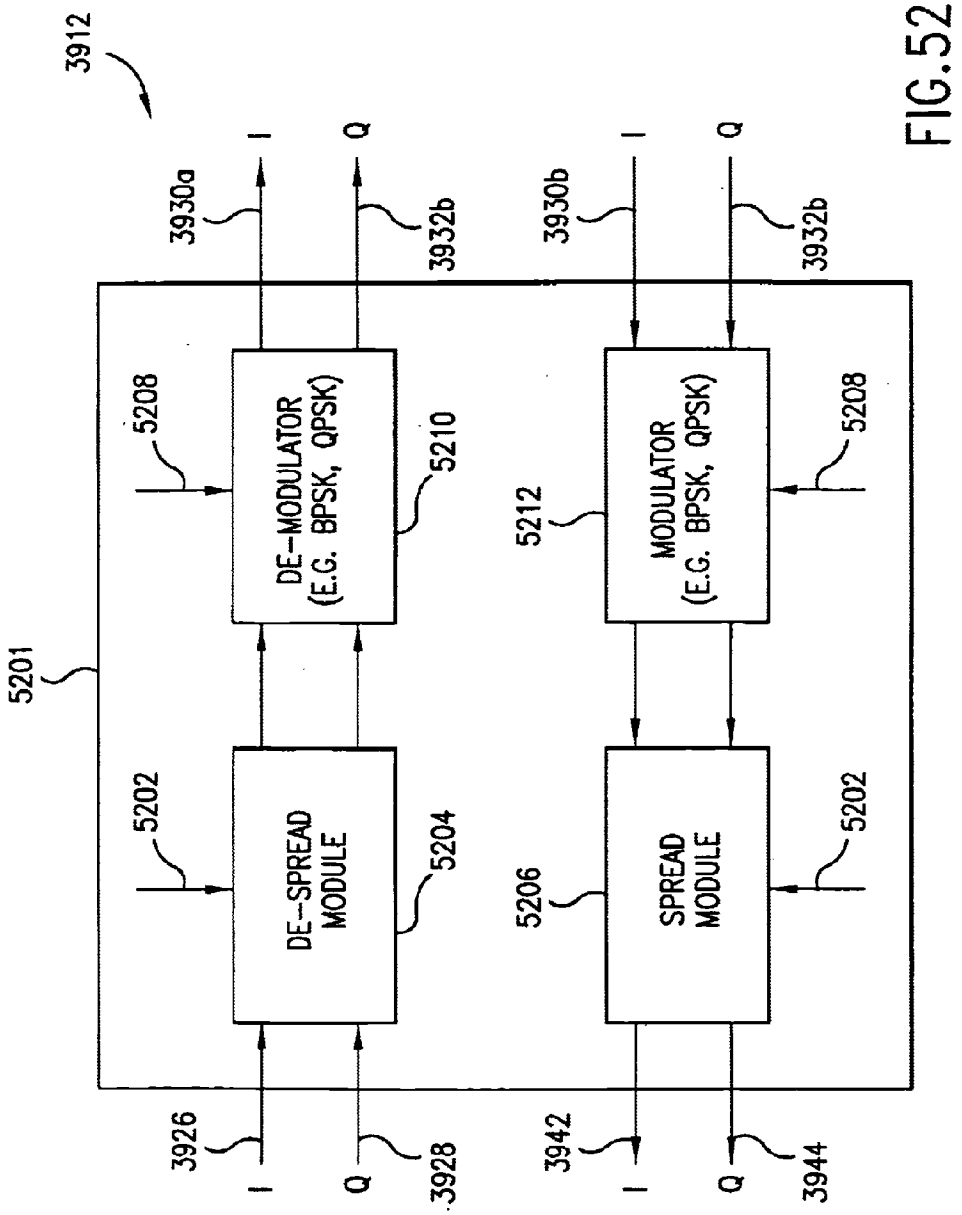
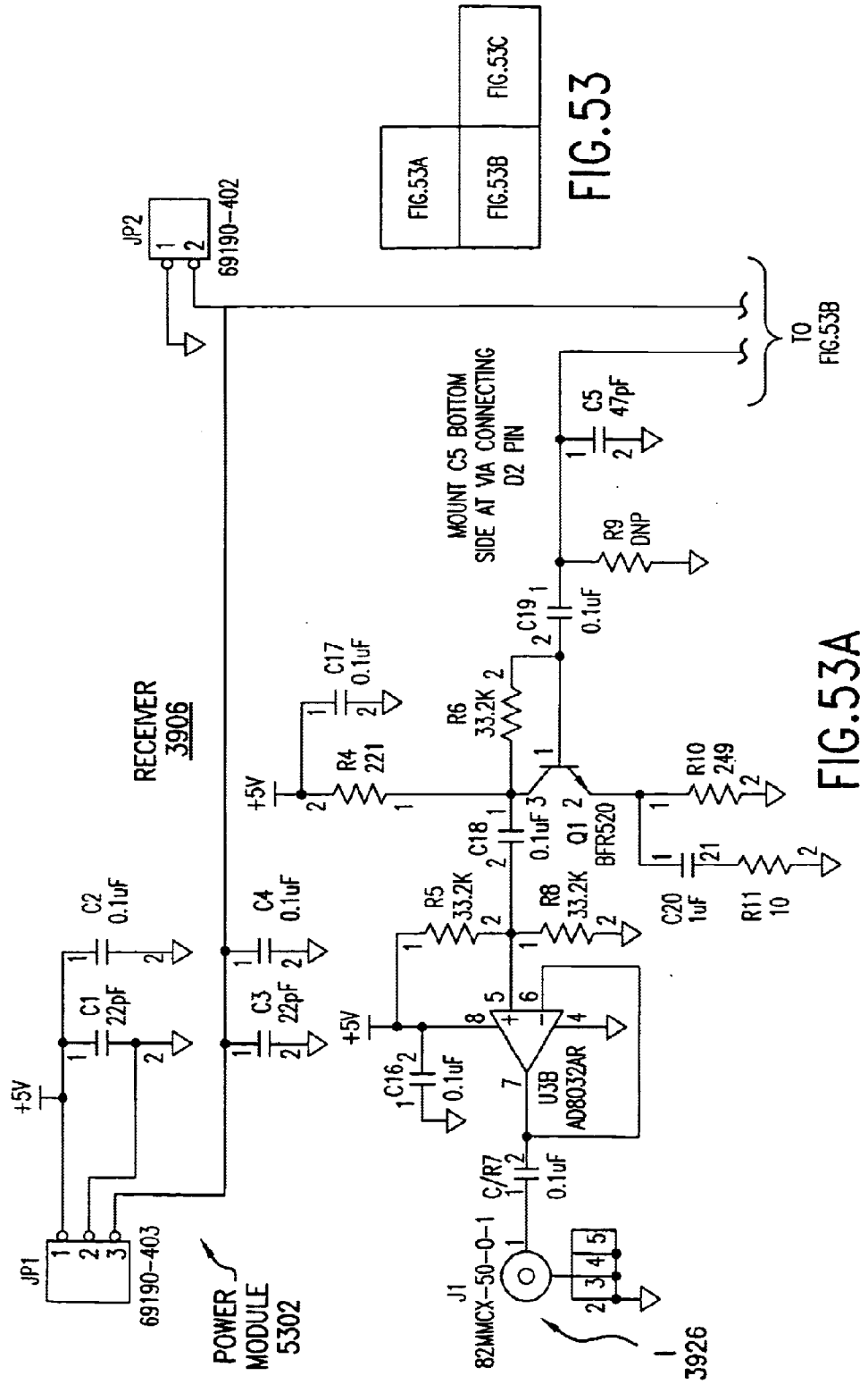

3912
3930a
I
Q
3932b
3930b
I
Q
3932b
5208
DE-MODULATOR (E.G. BPSK, QPSK)
5210
5212
MODULATOR (E.G. BPSK, QPSK)
5208
5201
5202
DE-SPREAD MODULE
5204
5206
SPREAD MODULE
5202
3926
I
Q
3928
3942
I
Q
3944

FIG.52C


FIG.53
FIG.53A
FIG.53B
FIG.53C
JP2
69190-402
TO FIG.53B
MOUNT C5 BOTTOM SIDE AT VIA CONNECTING D2 PIN
C5 47pF
R9 DNP
C19 0.1uF
C17 0.1uF
R6 33.2K
R4 221
+5V
RECEIVER 3906
R10 249
C18 0.1uF
Q1 BFR520
C20 1uF
R11 10
C2 0.1uF
C4 0.1uF
R5 33.2K
R8 33.2K
C1 22pF
C3 22pF
+5V
C16 0.1uF
U3B AD8032AR
C/R7 0.1uF
+5V
JP1
69190-403
POWER MODULE 5302
J1
82MMCX-50-0-1
3926

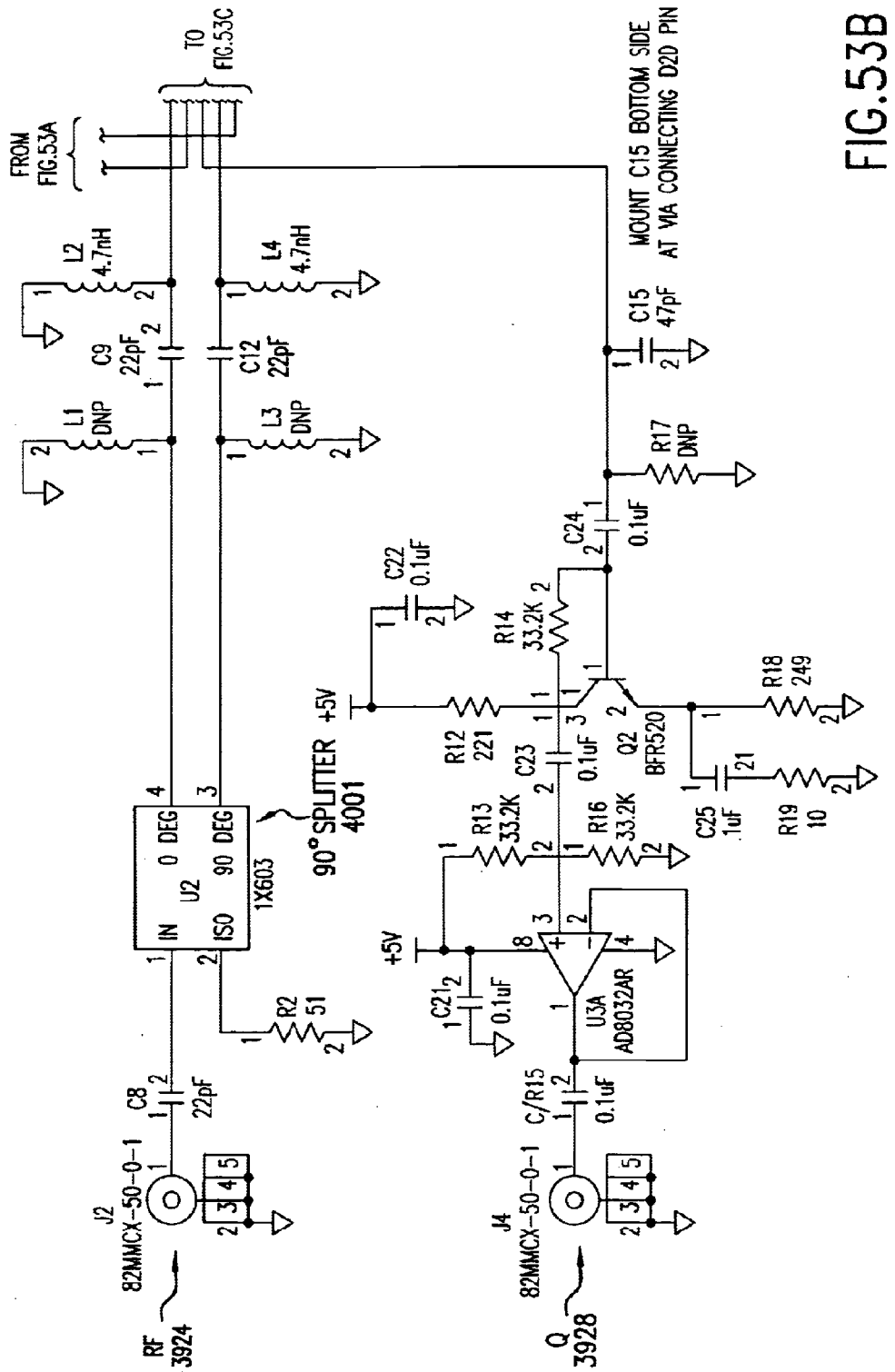

FROM FIG.53A
TO FIG.53C
L2 4.7nH
L4 4.7nH
C9 22pF
C12 22pF
L1 DNP
L3 DNP
C15 47pF
MOUNT C15 BOTTOM SIDE AT VIA CONNECTING D2D PIN
R17 DNP
C24 0.1uF
C22 0.1uF
R14 33.2K
+5V
R12 221
C23 0.1uF
Q2 BFR520
R18 249
R19 10
C25 1uF
R13 33.2K
R16 33.2K
U2 1X603
IN ISO 0 DEG 90 DEG
90° SPLITTER 4001
R2 51
C21 0.1uF
U3A AD8032AR
C8 22pF
C/R15 0.1uF
J2 82MMCX-50-0-1
J4 82MMCX-50-0-1
RF 3924
Q 3928

FIG.53B

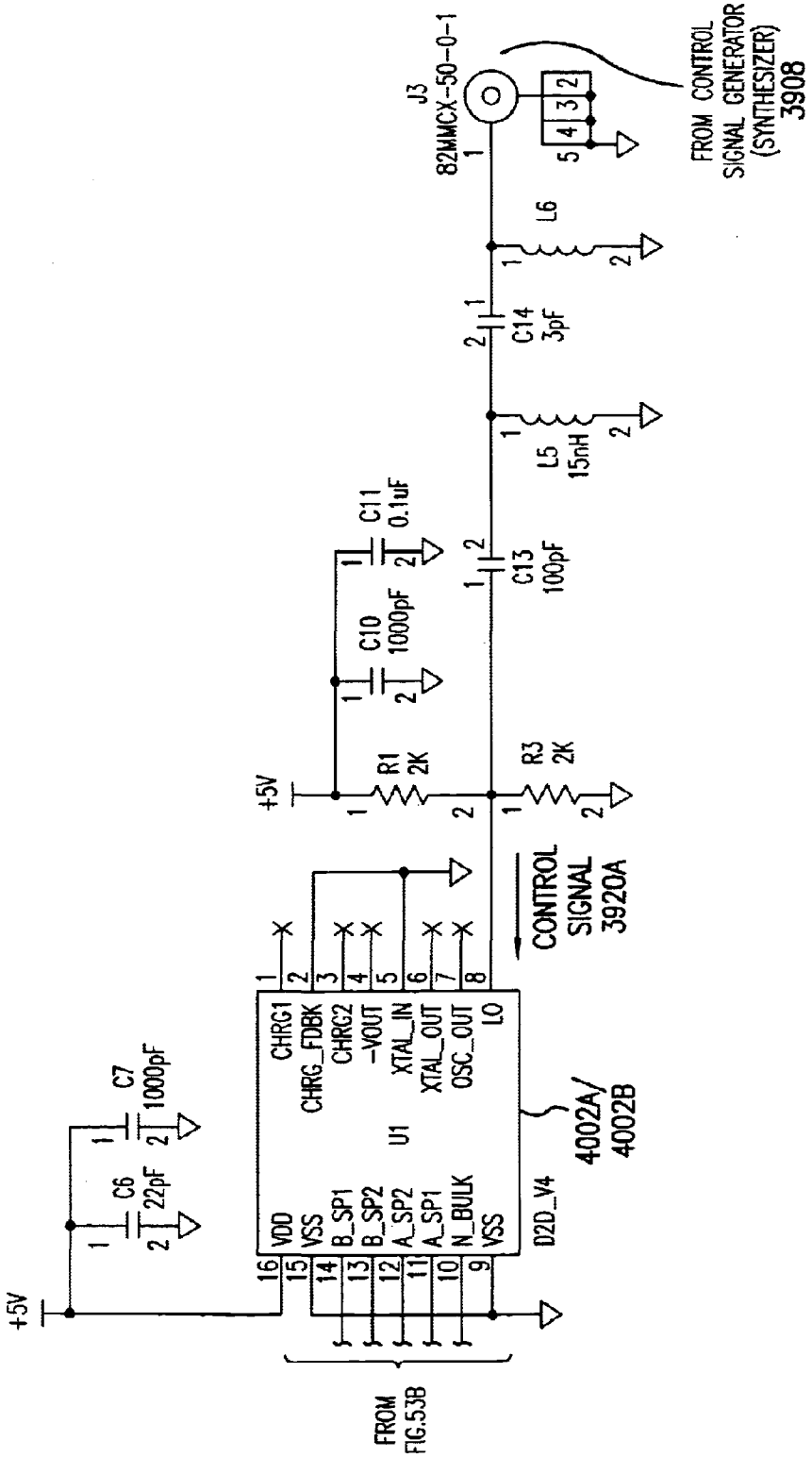

J3
82MMCX-50-0-1
FROM CONTROL SIGNAL GENERATOR (SYNTHESIZER) 3908
L6
C14 3pF
L5 15nH
C13 100pF
C11 0.1uF
C10 1000pF
R1 2K
R3 2K
+5V
CONTROL SIGNAL 3920A
U1
CHRG1
CHRG_FDBK
CHRG2
-VOUT
XTAL_IN
XTAL_OUT
OSC_OUT
LO
VDD
VSS
B_SP1
B_SP2
A_SP2
A_SP1
N_BULK
VSS
D2D_V4
4002A/ 4002B
C7 1000pF
C6 22pF
+5V
FROM FIG.53B

FIG.53C

FIG.54

ITEM	QTY	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	10	C7,C7,C15,C16,C17,C18	0.1uF	GRM39Y5V104Z016	MURATA
		C19,C21,C22,C23,C24			
2	6	C1,C3,C6,C8,C9,C12	22pF	GRM39COG220J050	MURATA
3	3	C2,C4,C11	0.1uF	GRM39X7R104K016	MURATA
4	2	C5,C15	47pF	GRM39COG470J050	MURATA
5	2	C10,C7	1000pF	GRM39X7R102K050	MURATA
6	1	C13	100pF	GRM39X7R101J050	MURATA
7	1	C14	3pF	GRM40COG030B50V	MURATA
8	2	C20,C25	1uF	GRM40Y5V105Z016	MURATA
9	1	JP1	69190-403	69190-403	BERG
10	1	JP2	69190-402	69190-402	BERG
11	4	J1,J2,J3,J4	82MMCX-50-0-1	82MMCX-50-0-1	SUHNER
12	2	L3,L1	DNP	L	TOKO
13	2	L4,L2	4.7nH	LL1608-F4N7K	TOKO
14	1	L5	15nH	LL2012FH15NJ	TOKO
15	1	L6	DNP	DNP	TOKO
16	2	Q1,Q2	BFR520	BFR520	PHILIPS
17	2	R1,R3	2K	ERJ3GSYJ202	PANASONIC
18	1	R2	51	ERJ3GSYJ510	PANASONIC
19	2	R4,R12	221	ERJ3EKF2210	PANASONIC
20	6	R5,R6,R8,R13,R14,R16	33.2K	ERJ3EKF3322	PANASONIC
21	2	R9,R17	DNP	ERJ3EKF1001	PANASONIC
22	2	R10,R18	249	ERJ3EKF2490	PANASONIC
23	2	R11,R19	10	ERJ3GSYJ100	PANASONIC
24	1	U1	D2D_V4	D2D_V4	PARKER VISION
25	1	U2	1X603	1X603	ANAREN
26	1	U3	AD8032AR	AD8032AR	ANALOG DEVICES
27	1		BOARD	STB500.641.001 V03.00	

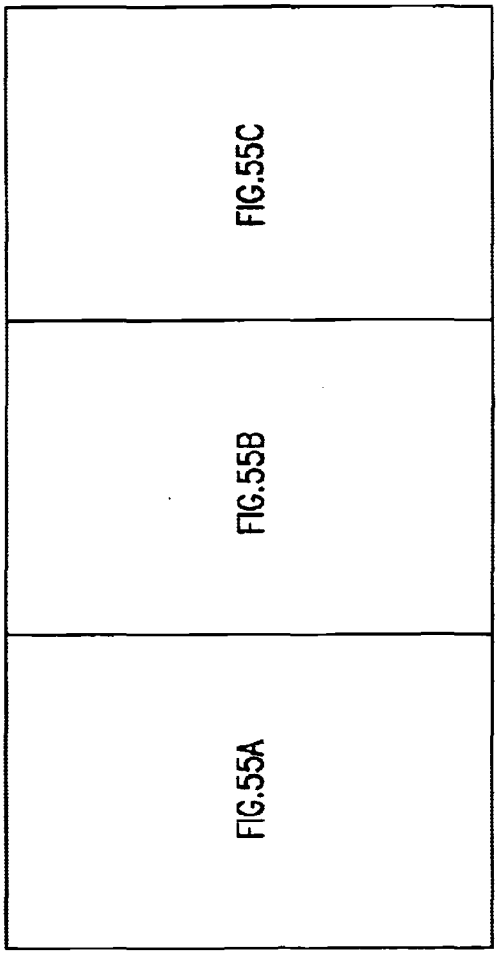


FIG.55

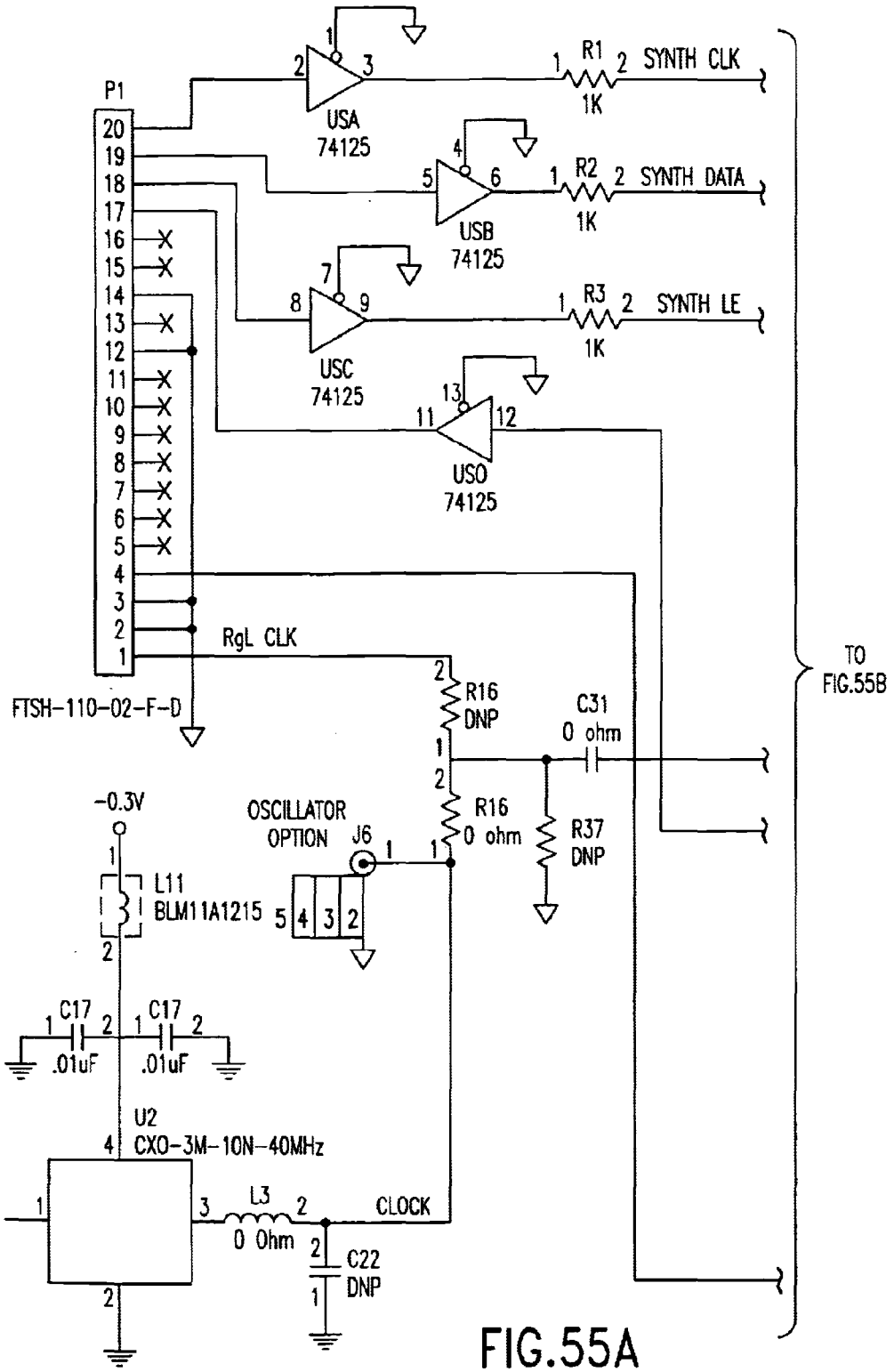

P1
FTSH-110-02-F-D
USA
74125
USB
74125
USC
74125
USO
74125
R1
1K
SYNTH CLK
R2
1K
SYNTH DATA
R3
1K
SYNTH LE
RgL CLK
R16
DNP
C31
0 ohm
R16
0 ohm
R37
DNP
TO
FIG.55B
-0.3V
OSCILLATOR
OPTION
J6
L11
BLM11A1215
C17
.01uF
C17
.01uF
U2
CXO-3M-10N-40MHz
L3
0 Ohm
CLOCK
C22
DNP

FIG.55A

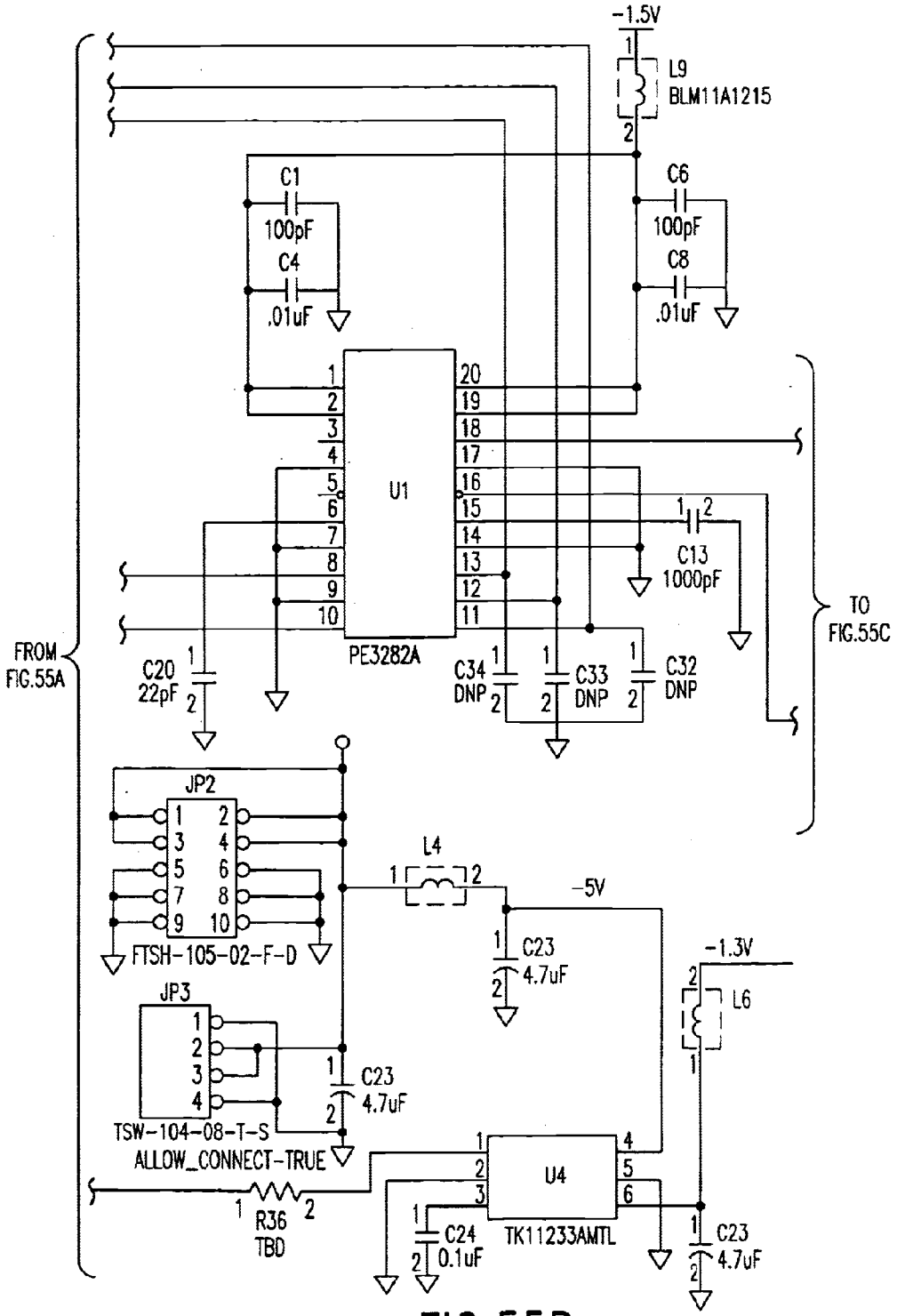

-1.5V
L9
BLM11A1215
C1
100pF
C4
.01uF
C6
100pF
C8
.01uF
U1
PE3282A
C13
1000pF
TO
FIG.55C
FROM
FIG.55A
C20
22pF
C34
DNP
C33
DNP
C32
DNP
JP2
FTSH-105-02-F-D
L4
-5V
C23
4.7uF
-1.3V
L6
JP3
TSW-104-08-T-S
ALLOW_CONNECT-TRUE
C23
4.7uF
U4
TK11233AMTL
R36
TBD
C24
0.1uF
C23
4.7uF

FIG.55B

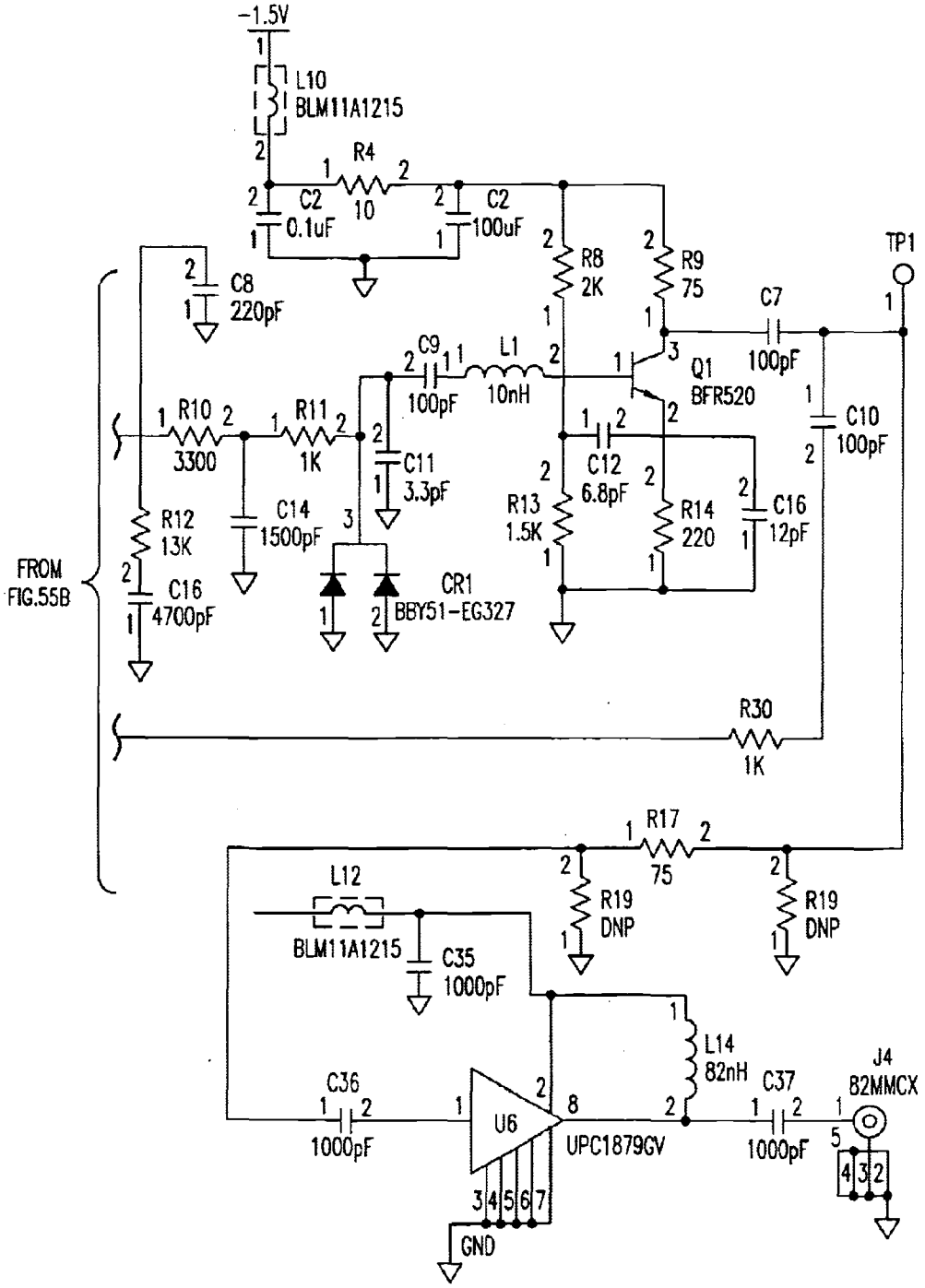

-1.5V
L10
BLM11A1215
R4
10
C2
0.1uF
C2
100uF
C8
220pF
R8
2K
R9
75
C7
100pF
TP1
C9
100pF
L1
10nH
Q1
BFR520
C10
100pF
R10
3300
R11
1K
C11
3.3pF
C12
6.8pF
R13
1.5K
R14
220
C16
12pF
R12
13K
C14
1500pF
C16
4700pF
CR1
BBY51-EG327
FROM
FIG.55B
R30
1K
R17
75
L12
BLM11A1215
C35
1000pF
R19
DNP
R19
DNP
L14
82nH
C36
1000pF
U6
UPC1879GV
C37
1000pF
J4
B2MMCX
GND

FIG.55C

ITEM	QTY	REFERENCE	PART	DESCRIPTION	PART NUMBER	MANUFACT.
1	1	CR1	BBY51-E6327	DIODE, VARACTOR	BBY51-E6327	SIEMENS
2	6	C1,C3,C5,C7,C9,C10	100pF	CAPACITOR,CERAMIC,100pF,10%,COG,0603	GRM39COG101K050	MURATA
3	2	C29,C2	0.1uF	CAPACITOR,CERAMIC,.1uF,10%,X7R,0603	GRM39X7R104K016AD	MURATA
4	3	C4,C8,C17	.01uF	CAPACITOR,CERAMIC,.01uF,10%,X7R,0603	GRM39X7R103K050	MURATA
5	1	C6	220pF	CAPACITOR,CERAMIC,220pF,5%,COG,0603	GRM39COG221J025	MURATA
6	1	C11	3.3pF	CAPACITOR,CERAMIC,3.3pF,5%,COG,0603	GRM39COG3R3B100V	MURATA
7	1	C12	6.8pF	CAPACITOR,CERAMIC,6.8pF,+/-.25pF,COG,0603	GRM39COG6R8C100V	MURATA
8	4	C13,C35,C36,C37	1000pF	CAPACITOR,CERAMIC,1000pF,10%,X7R,0603	GRM39X7R102K016	MURATA
9	1	C14	1500pF	CAPACITOR,CERAMIC,1500Pf,10%,X7R,0603	GRM39X7R152K016	MURATA
10	1	C15	12pF	CAPACITOR,CERAMIC,12pF,5%,COG,0603	GRM39COG120J050	MURATA
11	1	C16	4700pF	CAPACITOR,CERAMIC,4700pF,10%,0603	GRM39X7R472K016	MURATA
12	2	C20,C18	22pF	CAPACITOR,CERAMIC,22pF,10%,COG,0603	GRM36COG220K050	MURATA
13	4	C22,C32,C33,C34	DNP	CAPACITOR,CERAMIC,,,,,0603		MURATA
14	3	C23,C24,C27	4.7uF	CAPACITOR,TANTALUM,4.7uF,10%,3216	T491A475K006AS	KEMET
15	3	R16,C31,R17	0 OHM	RESISTOR,ZERO OHM,0603	ERJ3GSY0R00	PANASONIC
16	1	JP1	FTSH-110-02-F-D	HEADER,DUAL ROW 10X2,.050X.050	FTSH-110-02-F-D	SAMTEC
17	1	JP2	FTSH-105-02-F-D	HEADER,DUAL ROW 5X2,.050X.050	FTSH-105-02-F-D	SAMTEC
18	1	JP3	TSW-104-08-T-S	HEADER, SINGLE ROW 4 PIN, .100"	TSW-104-08-T-S	BERG
19	2	J5,J6	82MMCX	RF CONNECTOR	82MMCX-50-0-1	SUHNER
20	1	L1	18nH	INDUCTOR,18nH,10%, 0805	0805CS-180XJBC	COILCRAFT
21	1	L3	0 OHM	ZERO OHM JUMPER	RM73Z1JT	KOA
22	6	L4,L6,L9,L10,L11,L12	BLM11A121S	FERRITE BEAD, 0603	BLM11A121S	MURATA
23	1	L14	82nH	INDUCTOR, 82nH,10%,0805	LL2012-F82NK	TOKO
24	1	Q1	BFR520	TRANSISTOR, NPN	BFR520	PHILIPS
25	5	R1,R2,R3,R11,R30	1K	RESISTOR, 1K,5%,0603	ERF3GSYJ102	PANASONIC
26	1	R4	10	RESISTOR, 10 OHM,5%,0603	ERJ3GSYJ1R0	PANASONIC

FIG.56A

27	1	R8	2K	RESISTOR, 2K, 5%, 0603	ERJ3GSYJ202	PANASONIC
28	1	R9	75	RESISTOR, 75 OHM, 5%, 0603	ERJ3GSYJ750	PANASONIC
29	1	R10	3300	RESISTOR, 3.3K, 5%, 0603	ERJ3GSYJ332	PANASONIC
30	1	R12	13K	RESISTOR, 13K, 5%, 0603	ERJ3GSYJ133	PANASONIC
31	1	R13	1.5K	RESISTOR, 1.5K, 5%, 0603	ERJ3GSYJ152	PANASONIC
32	1	R14	220	RESISTOR, 220 OHM, 5%, 0603	ERJ3GSYJ221	PANASONIC
33	1	R15	DNP	RESISTOR, ZERO OHM, 0603	ERJ3GSY0R00	PANASONIC
34	2	R18, R19	DNP	RESISTOR, 91 OHM, 5%, 0603	ERJ3GSYJ910	PANASONIC
35	1	R36	TBD	RESISTOR, ZERO OHM, 0603	ERJ3GSY0R00	PANASONIC
36	1	R37	DNP	RESISTOR, , , 0603		PANASONIC
37	1	TP1	TEST POINT			
38	1	U1	PE3282A	IC, SYNTHESIZER	PE3282A	PEREGRINE
39	1	U2	CXO-3M-10N-40MHz	XTAL OSC, 40MHz	CXO-3M-10N-40MHZ A/I	STATEK
40	1	U4	TK11233AMTL	VOLTAGE REGULATOR, 3.5V	TK11235BM	TOKO
41	1	U5	74125	IC, BUFFER	MC74LCX125DT	MOTOROLA
42	1	U6	UPC1678GV	IC, RF AMPLIFIER	UPC1678GV	NEC
43	1		STB500.641.008 V03.00	BOARD		

FIG.56B

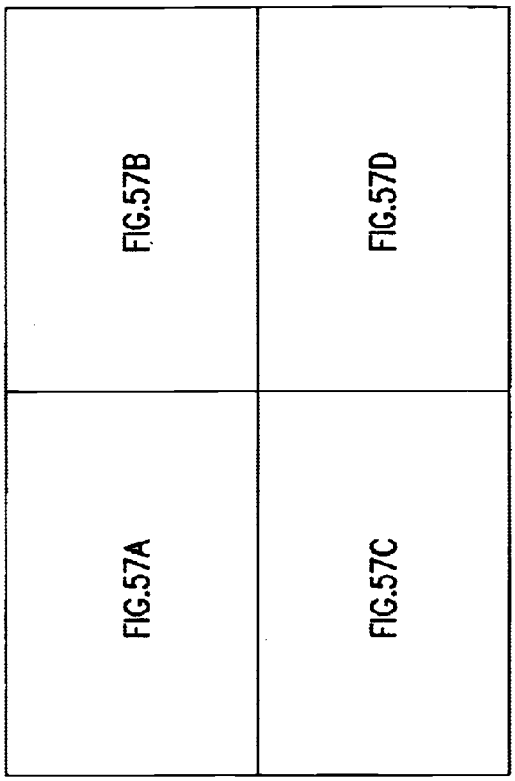


FIG.57

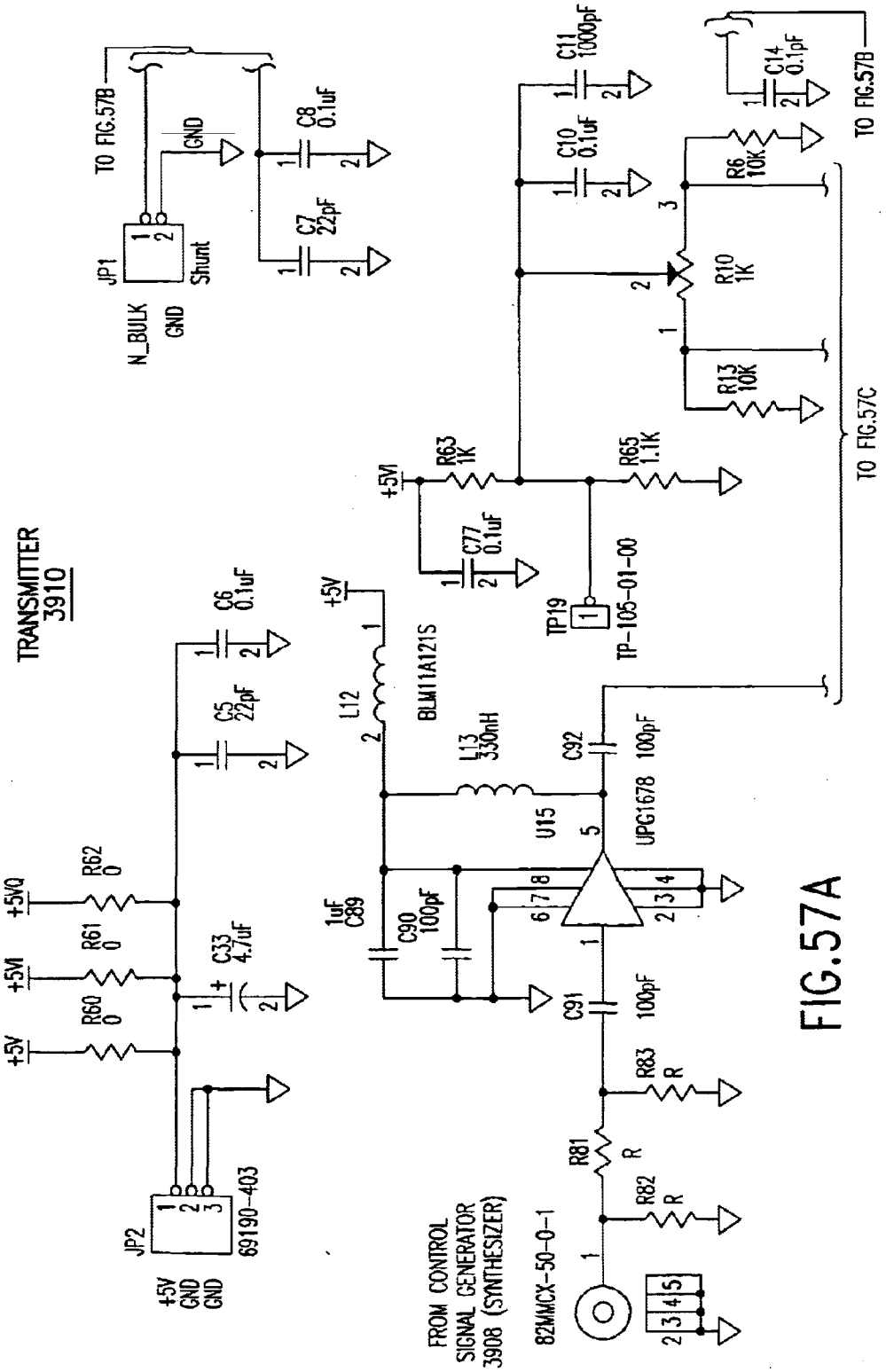

TRANSMITTER
3910
TO FIG.57B
GND
JP1
Shunt
N_BULK
GND
C8
0.1uF
C7
22pF
C11
1000pF
C10
0.1uF
C14
0.1pF
R6
10K
R10
1K
R13
10K
TO FIG.57B
TO FIG.57C
+5M
R63
1K
R65
1.1K
C77
0.1uF
TP19
TP-105-01-00
+5V
L12
BLM11A121S
L13
330nH
C92
100pF
U15
UPG1678
C6
0.1uF
C5
22pF
+5VQ
R62
0
R61
0
+5M
C33
4.7uF
R60
0
+5V
1uF
C89
C90
100pF
C91
100pF
R83
R
R81
R
R82
R
JP2
69190-403
+5V
GND
GND
FROM CONTROL
SIGNAL GENERATOR
3908 (SYNTHESIZER)
82MMCX-50-0-1

FIG.57A

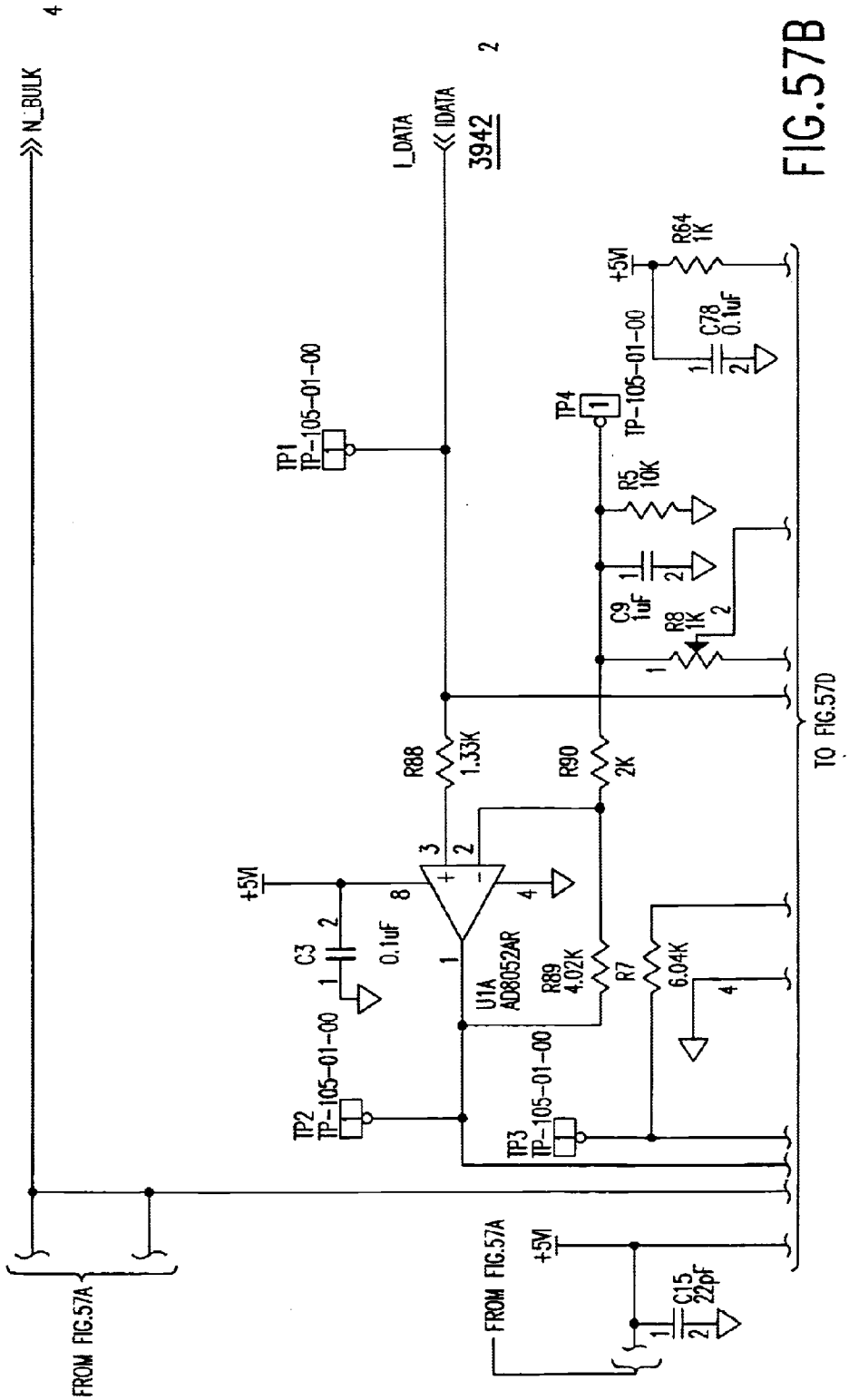

N_BULK
I_DATA
IDATA
3942
TP1
TP-105-01-00
TP2
TP-105-01-00
TP3
TP-105-01-00
TP4
TP-105-01-00
+5V
C3
0.1uF
C78
0.1uF
C9
1uF
C15
22pF
R64
1K
R5
10K
R8
1K
R88
1.33K
R90
2K
R89
4.02K
R7
6.04K
U1A
AD8052AR
FROM FIG.57A
FROM FIG.57A
TO FIG.57D

FIG.57B

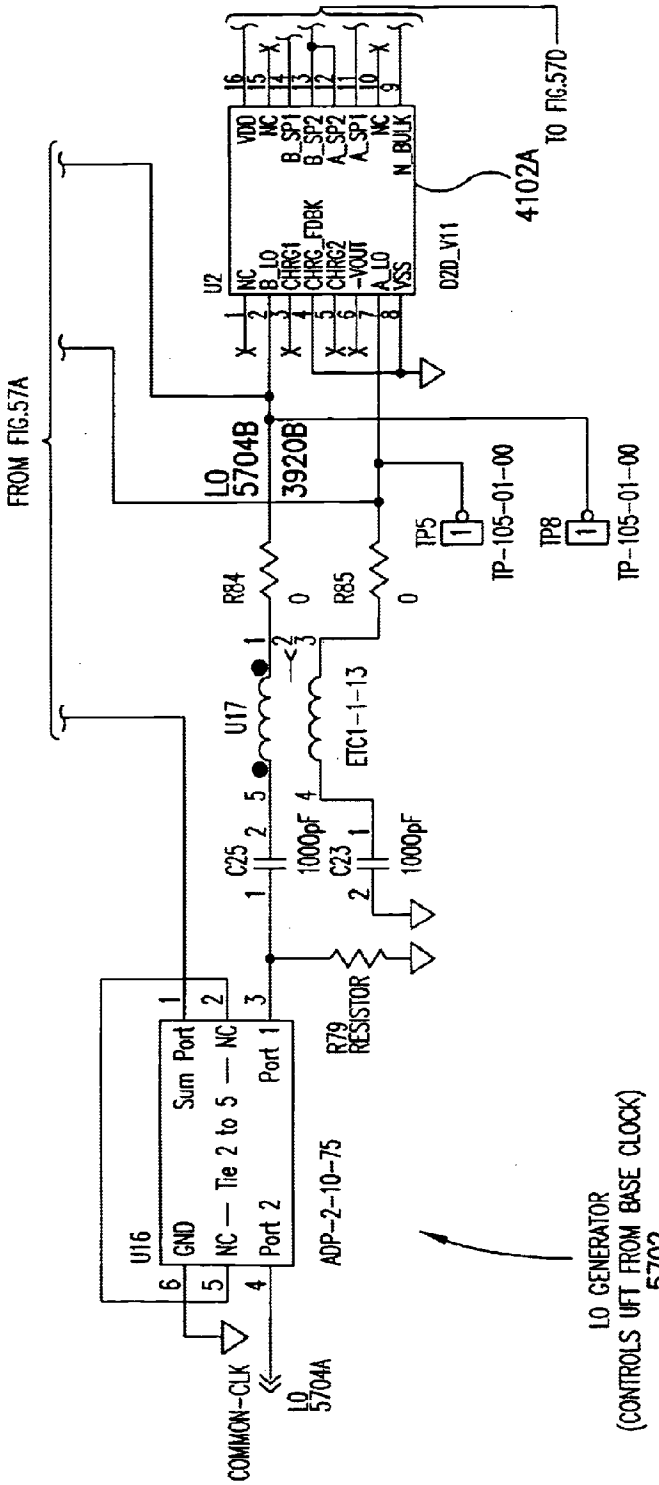

FROM FIG.57A
LO 5704B
3920B
U2
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
NC
B_SP1
B_SP2
A_SP1
NC
N_BULK
D2D_V11
4102A
TO FIG.57D
TP5
TP-105-01-00
TP8
TP-105-01-00
R84
0
R85
0
U17
ETC1-1-13
C25
1000pF
C23
1000pF
R79
RESISTOR
U16
GND
NC — Tie 2 to 5 — NC
Port 2
Sum Port
Port 1
ADP-2-10-75
COMMON-CLK
LO 5704A
LO GENERATOR
(CONTROLS UFT FROM BASE CLOCK)
5702

FIG.57C

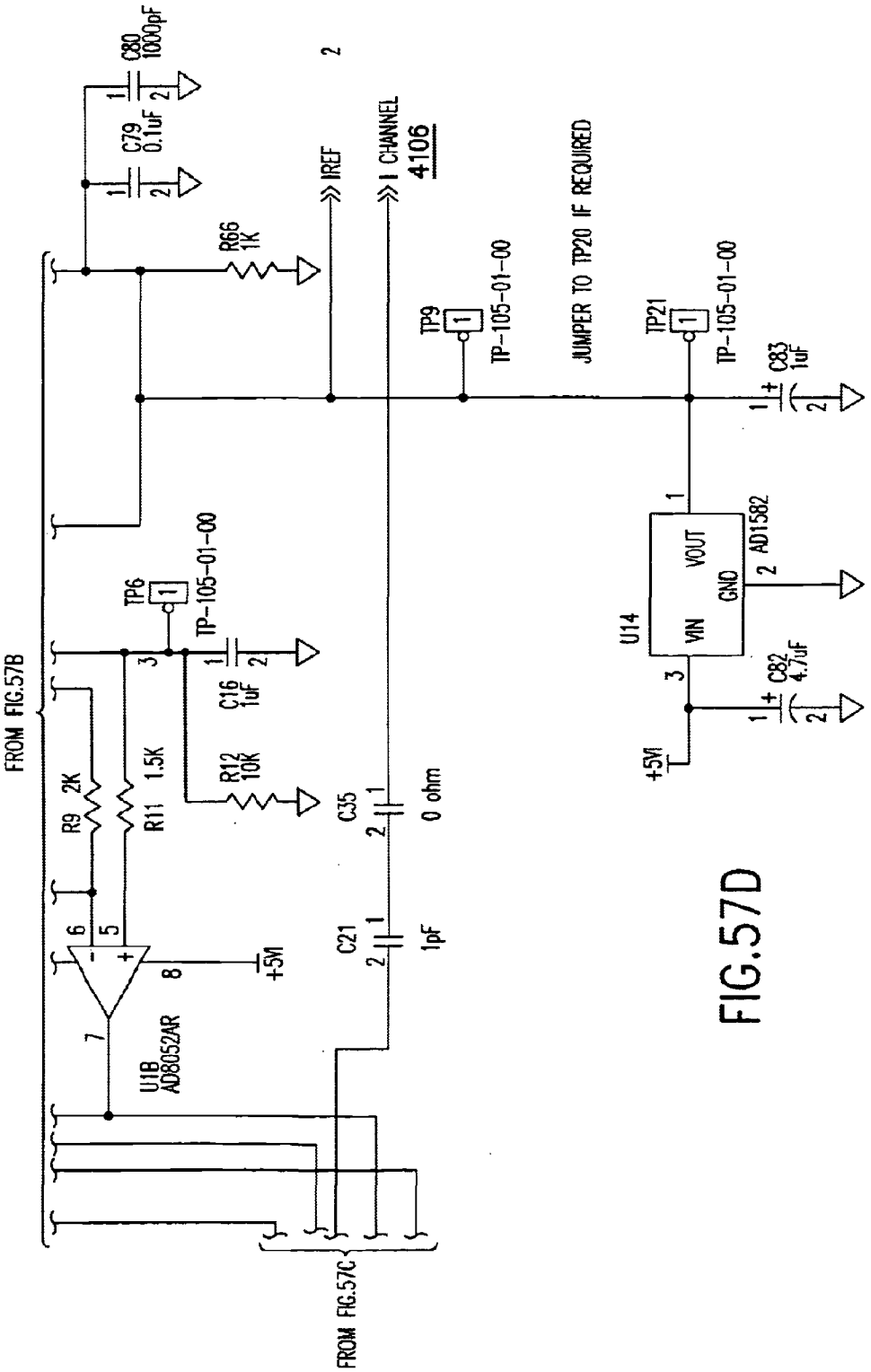

C80 1000pF
C79 0.1uF
R66 1K
IREF
I CHANNEL
4106
JUMPER TO TP20 IF REQUIRED
TP9
TP-105-01-00
TP21
TP-105-01-00
C83 1uF
TP6
TP-105-01-00
C16 1uF
R12 10K
R9 2K
R11 1.5K
C35 0 ohm
C21 1pF
U1B AD8052AR
+5V
FROM FIG.57B
FROM FIG.57C
U14
VIN
VOUT
GND
AD1582
C82 4.7uF
+5V

FIG.57D

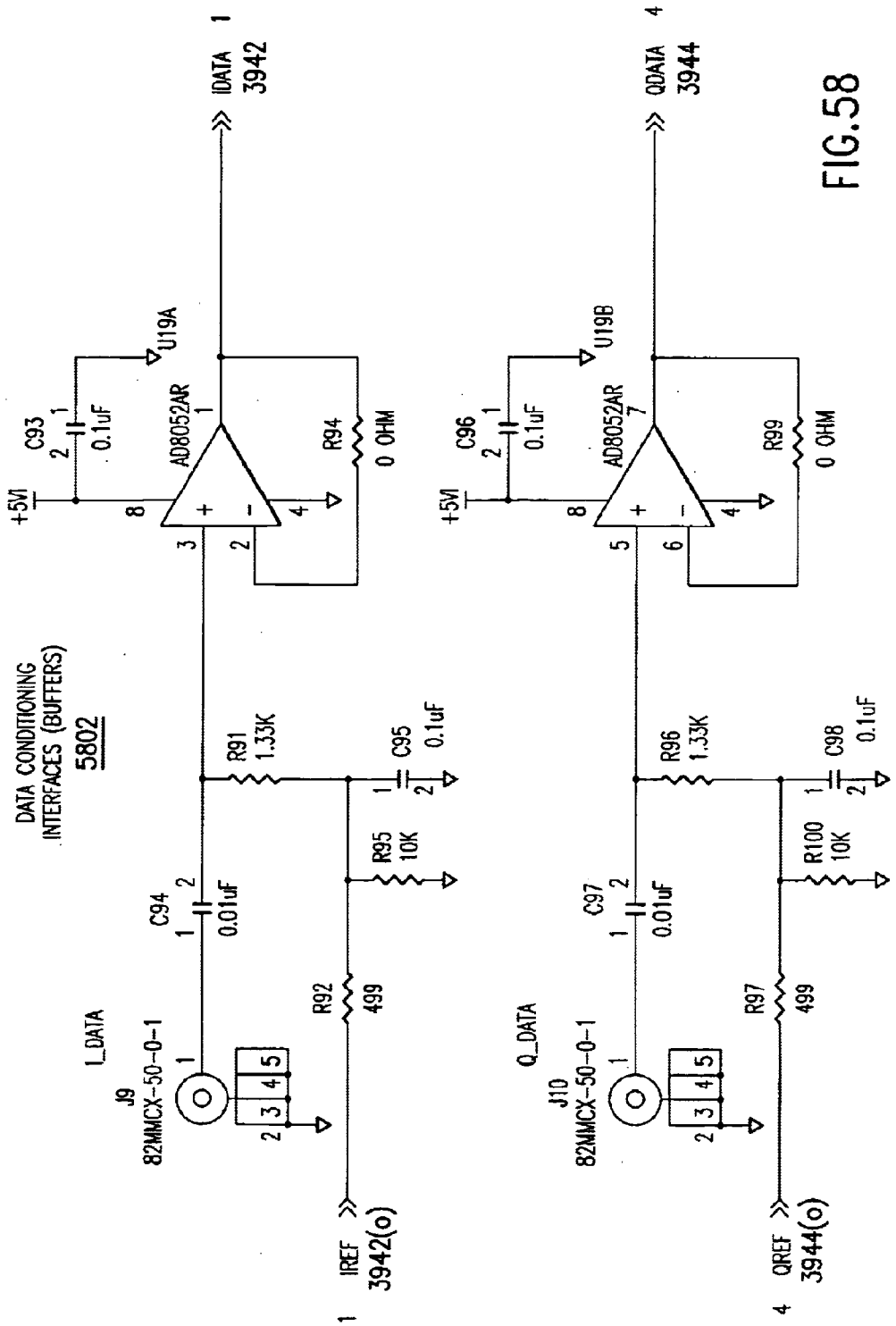

IDATA
3942
QDATA
3944
U19A
U19B
AD8052AR
C93
C96
0.1uF
+5VI
R94
R99
0 OHM
DATA CONDITIONING
INTERFACES (BUFFERS)
5802
R91
R96
1.33K
C95
C98
R95
R100
10K
C94
C97
0.01uF
I_DATA
Q_DATA
J9
J10
82MMCX-50-0-1
R92
R97
499
IREF
3942(o)
QREF
3944(o)

FIG.58

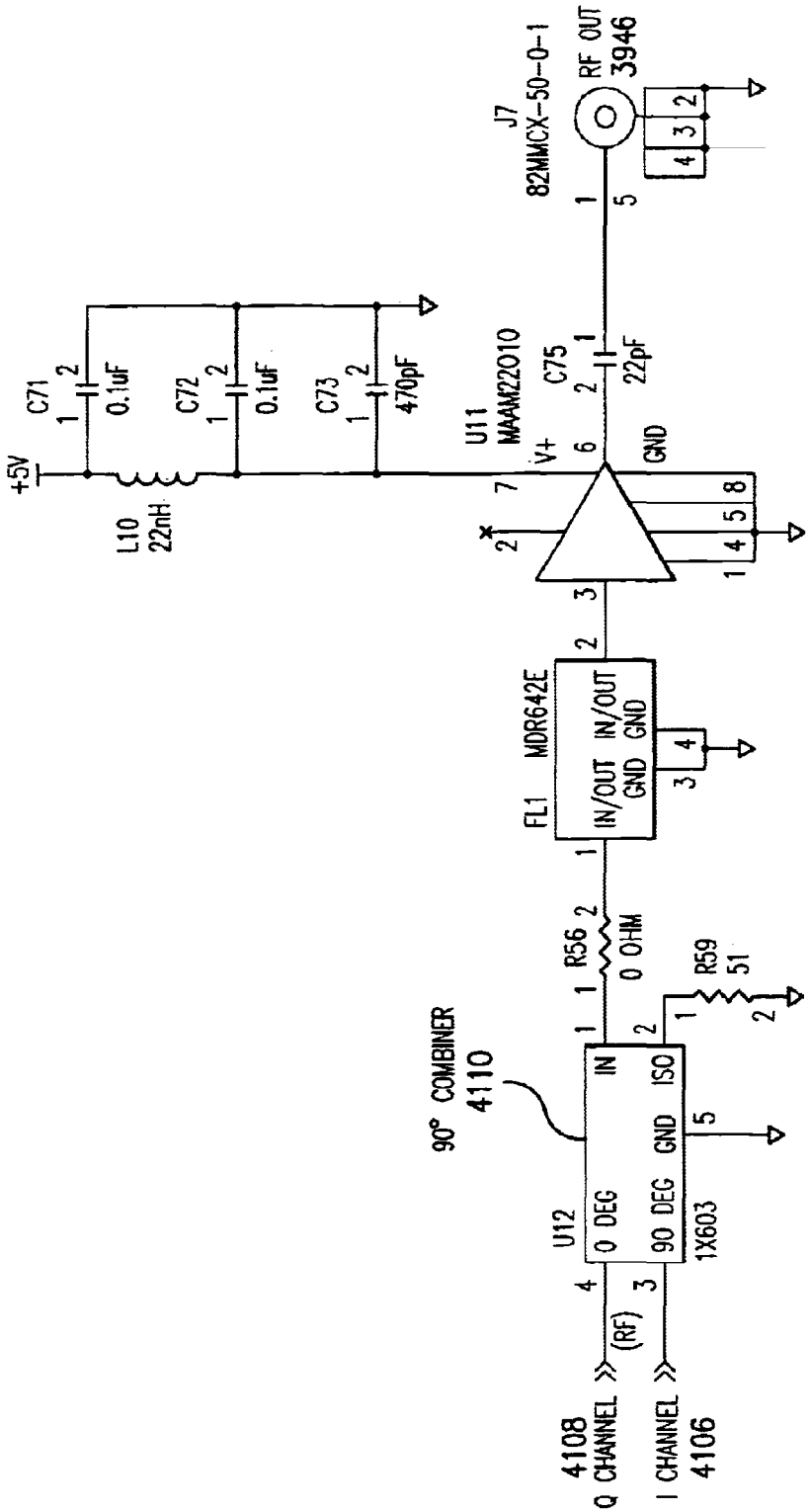

J7
82MMCX-50-0-1
RF OUT
3946
C71
0.1uF
C72
0.1uF
C73
470pF
C75
22pF
+5V
L10
22nH
U11
MAAM22010
V+
GND
FL1
MDR642E
IN/OUT
GND
R56
0 OHM
R59
51
90° COMBINER
4110
IN
ISO
GND
U12
0 DEG
90 DEG
1X603
(RF)
4108
Q CHANNEL
I CHANNEL
4106

FIG.59

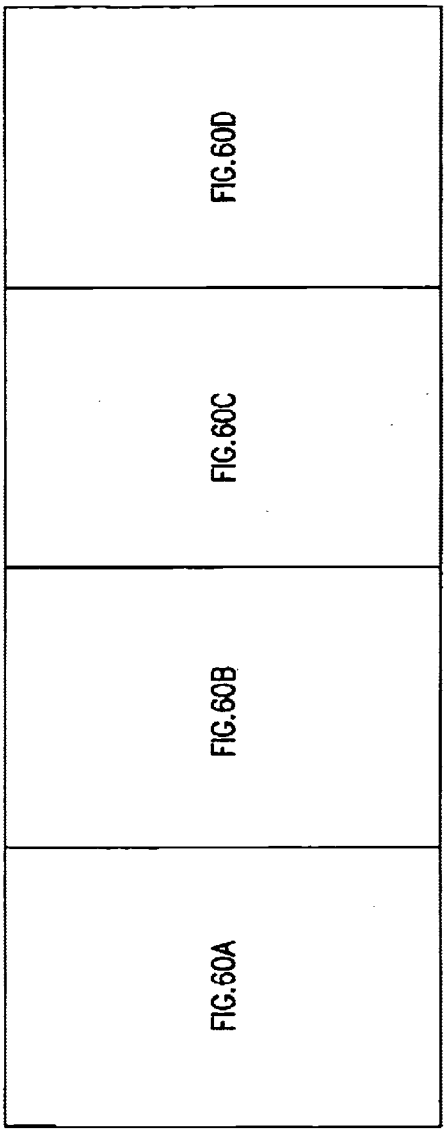


FIG.60

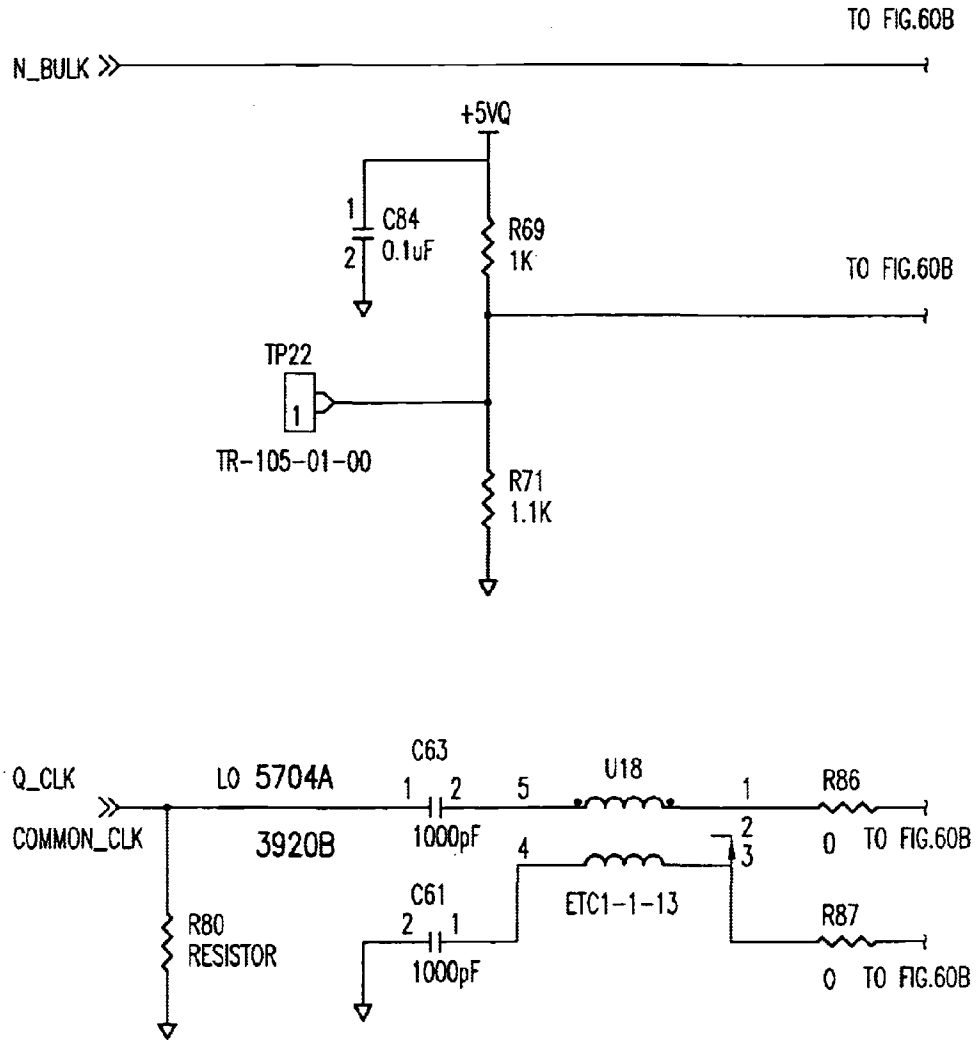

TO FIG.60B
N_BULK
+5VQ
C84
0.1uF
R69
1K
TO FIG.60B
TP22
TR-105-01-00
R71
1.1K
Q_CLK
COMMON_CLK
LO 5704A
3920B
C63
1000pF
U18
R86
0 TO FIG.60B
C61
1000pF
ETC1-1-13
R87
0 TO FIG.60B
R80
RESISTOR

FIG.60A

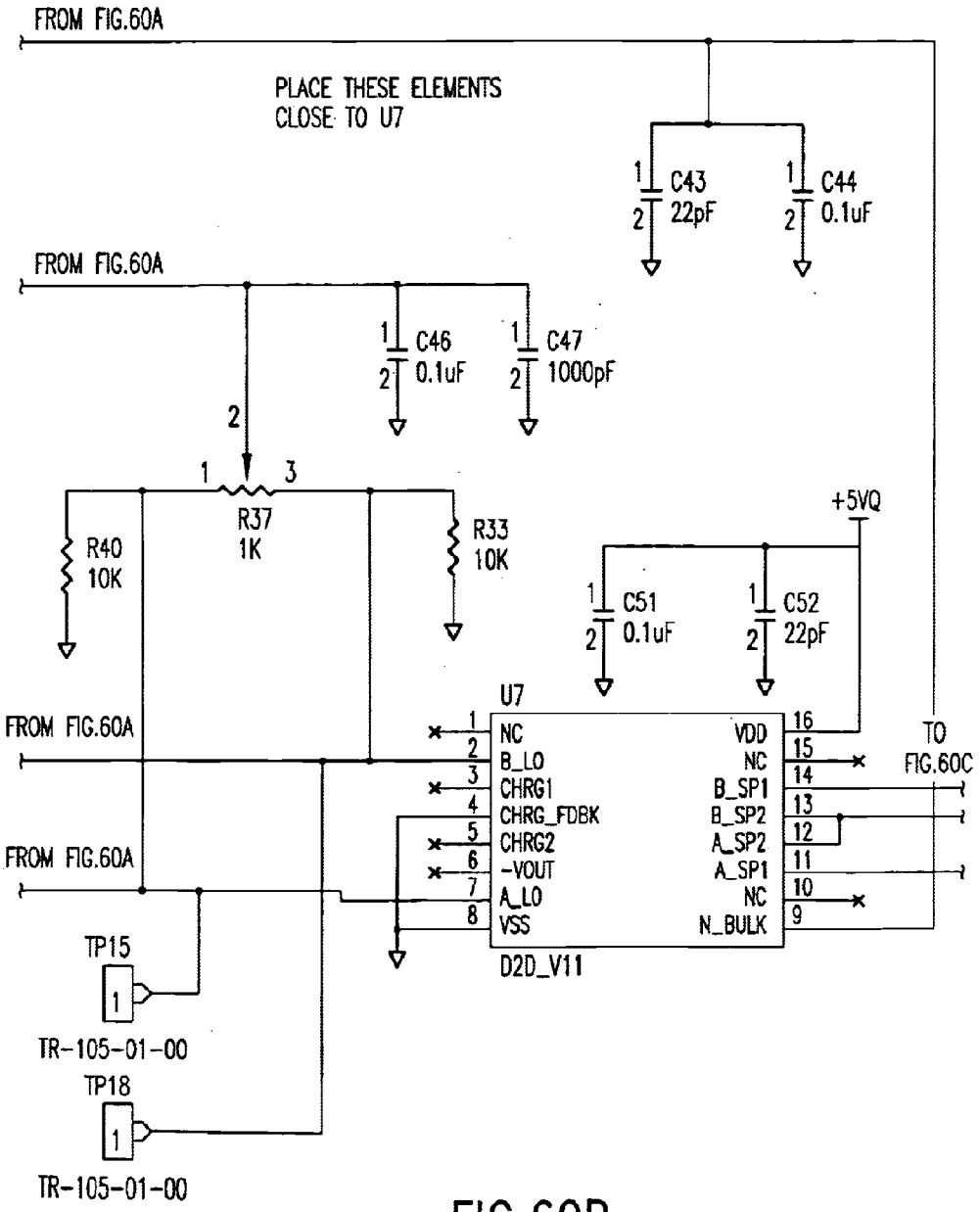

FROM FIG.60A
PLACE THESE ELEMENTS
CLOSE TO U7
C43
22pF
C44
0.1uF
FROM FIG.60A
C46
0.1uF
C47
1000pF
R37
1K
R40
10K
R33
10K
+5VQ
C51
0.1uF
C52
22pF
U7
FROM FIG.60A
FROM FIG.60A
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
NC
B_SP1
B_SP2
A_SP2
A_SP1
NC
N_BULK
D2D_V11
TO
FIG.60C
TP15
TR-105-01-00
TP18
TR-105-01-00

FIG.60B

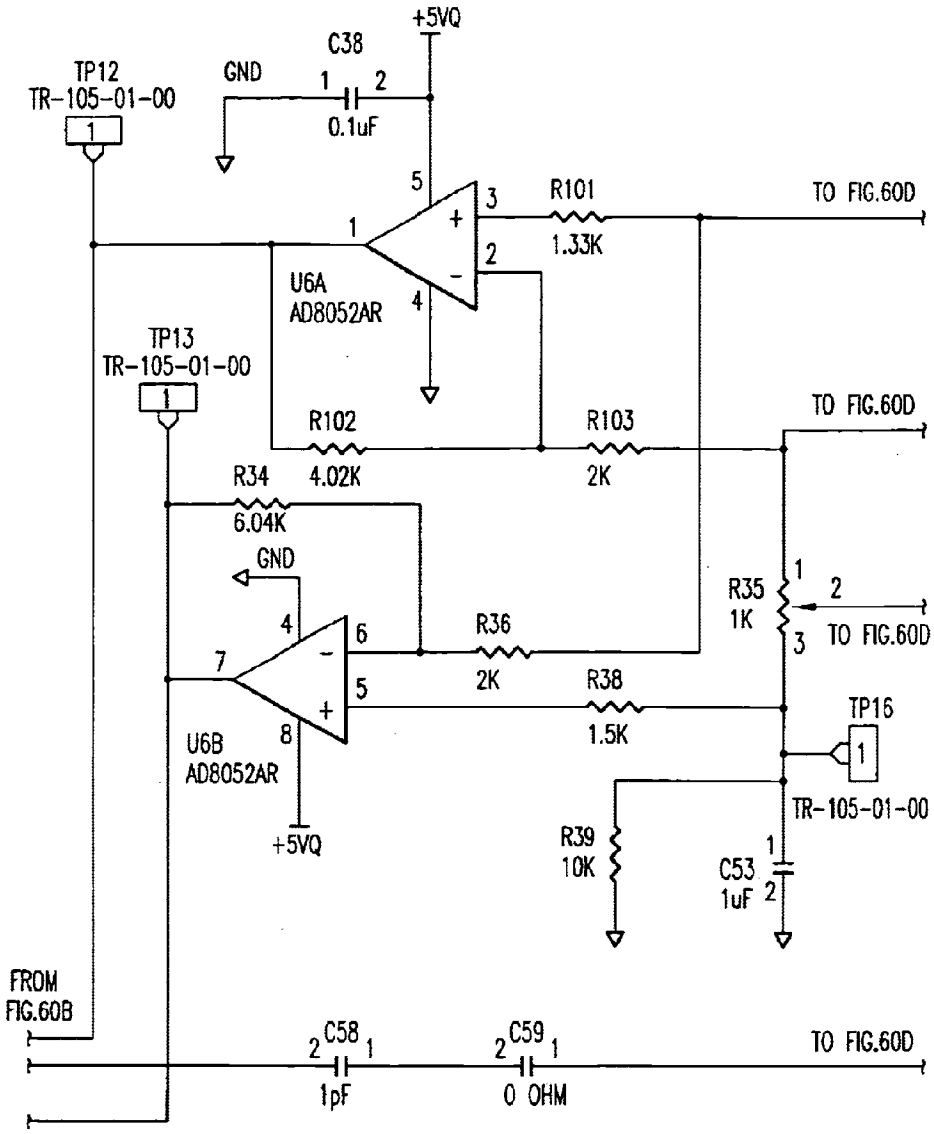

+5VQ
C38
TP12
TR-105-01-00
GND
0.1uF
R101
1.33K
TO FIG.60D
U6A
AD8052AR
TP13
TR-105-01-00
R102
4.02K
R103
2K
TO FIG.60D
R34
6.04K
GND
R35
1K
TO FIG.60D
R36
2K
R38
1.5K
TP16
U6B
AD8052AR
+5VQ
TR-105-01-00
R39
10K
C53
1uF
FROM
FIG.60B
C58
1pF
C59
0 OHM
TO FIG.60D

FIG.60C

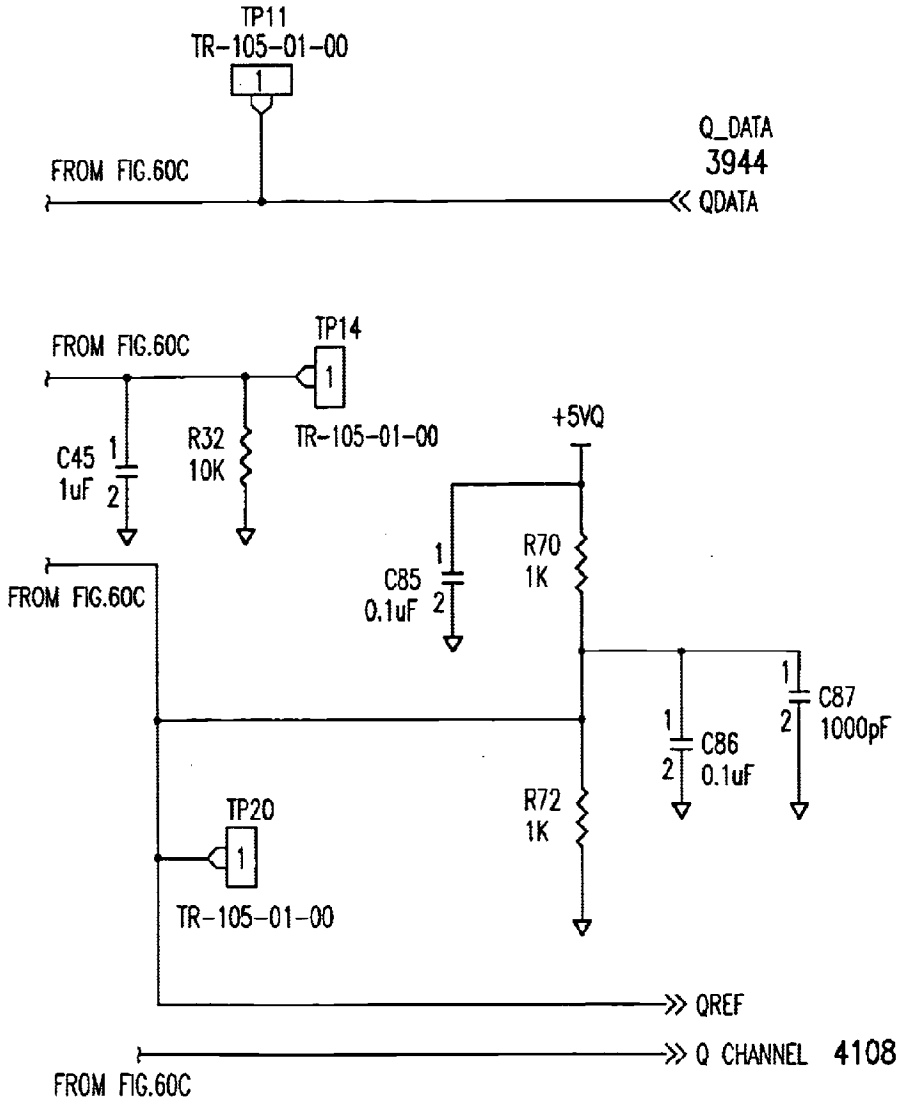

TP11
TR-105-01-00
1
Q_DATA
3944
FROM FIG.60C
QDATA
FROM FIG.60C
TP14
1
TR-105-01-00
+5VQ
C45
1uF
1
2
R32
10K
C85
0.1uF
R70
1K
FROM FIG.60C
C87
1000pF
C86
0.1uF
TP20
R72
1K
TR-105-01-00
QREF
Q CHANNEL
4108
FROM FIG.60C

FIG.60D

FIG.61A

ITEM	QTY	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	21	C3,C6,C8,C10,C14,C38,C44,	0.1uF	GRM39X7R104K016	MURATA
		C46,C51,C71,C72,C77,C78,			
		C79,C84,C85,C86,C93,C95,			
		C96,C98			
2	6	C5,C7,C15,C43,C52,C75	22pF	GRM39C0G220J050	MURATA
3	5	C9,C16,C45,C53,C89	1uF	GRM40Y5V105Z016	MURATA
4	8	C11,C23,C25,C47,C61,C63	1000pF	GRM39X7R102K050	MURATA
		C80,C87			
5	2	C58,C21	1pF	GRM39C0G010B50V	MURATA
6	2	C82,C33	4.7uF	T491A475K006AS	KEMET
7	2	C59,C35	0 ohm	GRM39C0Gxxxx50V	MURATA
8	1	C73	470pF	GRM39C0G471J050	MURATA
9	1	C83	1uF	T491A105M016AS	KEMET
10	3	C90,C91,C92	100pF	ECU-V1H101JCV	
11	2	C94,C97	0.01uF	GRM39X7R103K016	MURATA
12	1	FL1	MDR642E	MDR642E	SOSHIN
13	1	JP1	Shunt	69190-402	BERG
14	1	JP2	69190-403	69190-403	BERG
15	4	J7,J8,J9,J10	82MMCX-50-0-1	82MMCX-50-0-1	SUHNER
16	1	L10	22nH	LL1608-F22NK	COILCRAFT
17	1	L12	BLM11A121S	BLM11A121S	MURATA
18	1	L13	330nH	LL2012-FR33K	
19	10	R5,R6,R12,R13,R32,R33,	10K	ERJ3EKF1002	PANASONIC
		R39,R40,R95,R100			
20	2	R34,R7	6.04K	ERJ3EKF6041	PANASONIC
21	4	R8,R10,R35,R37	1K	3224W-1-102	BOURNS
22	4	R9,R36,R90,R103	2K	ERJ3EKF2001	PANASONIC
23	2	R38,R11	1.5K	ERJ3EKF1501	PANASONIC
24	3	R56,R94,R99	0 ohm	ERJ3GSY0R00	PANASONIC

25	1	R59	51	ERJ3GSYJ510	PANASONIC	
26	7	R60,R61,R62,R84,R85,R86,	0	ERJ3GSY0R00	PANASONIC	
		R87				
27	6	R63,R64,R66,R69,R70,R72	1K	ERJ3EKF1001	PANASONIC	
28	2	R71,R65	1.1K	ERJ3EKF1101	PANASONIC	
29	2	R80,R79	RESISTOR			
30	3	R81,R82,R83	R			
31	4	R88,R91,R96,R101	1.33K	ERJ3EKF1331	PANASONIC	
32	2	R102,R89	4.02K	ERJ3EKF4021	PANASONIC	
33	2	R92,R97	499	ERJ3EKF4990	PANASONIC	
34	19	TP1,TP2,TP3,TP4,TP5,TP6,	TP-105-01-00			
		TP8,TP9,TP11,TP12,TP13,				
		TP14,TP15,TP16,TP18,TP19,				
		TP20,TP21,TP22				
35	3	U1,U6,U19	AD8052AR	AD8052AR	ANALOG DEVICES	
36	2	U7,U2	D2D_V11	D2D_V11	PARKER VISION	
37	1	U11	MAAM22010	MAAM22010	MACOM	
38	1	U12	1X603	1X603	ANAREN	
39	1	U14	AD1582	AD1582	ANALOG DEVICES	
40	1	U15	UPG1678	UPG1678GV	NEC	
41	1	U16	ADP-2-10-75	ADP-2-10-75	MINI-CIRCUITS	
42	1		BOARD	8500.641.021	V05.10	

FIG.61B

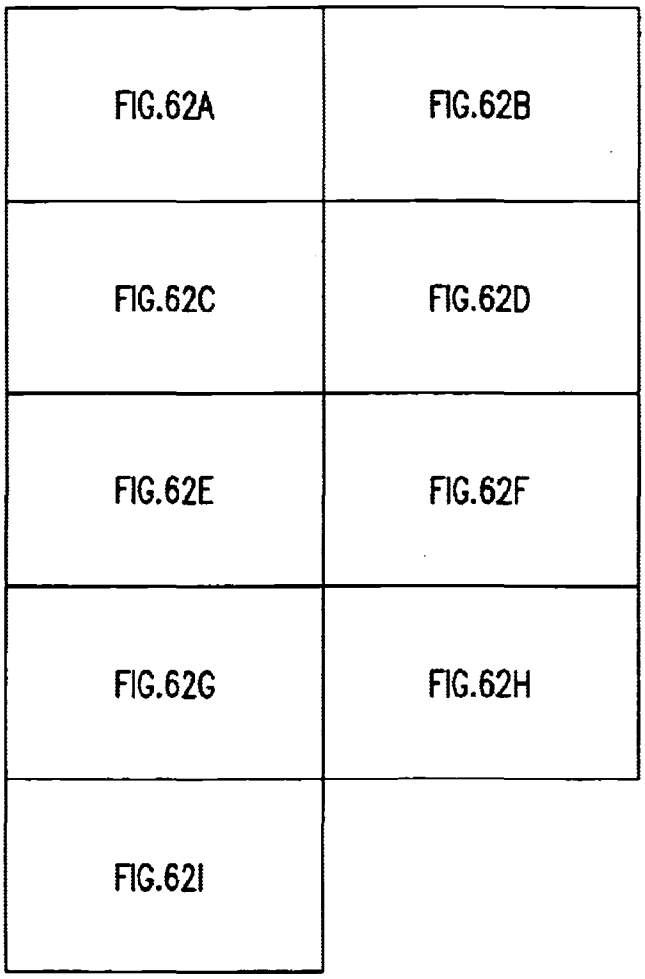

FIG.62A
FIG.62B
FIG.62C
FIG.62D
FIG.62E
FIG.62F
FIG.62G
FIG.62H
FIG.62I

FIG. 62

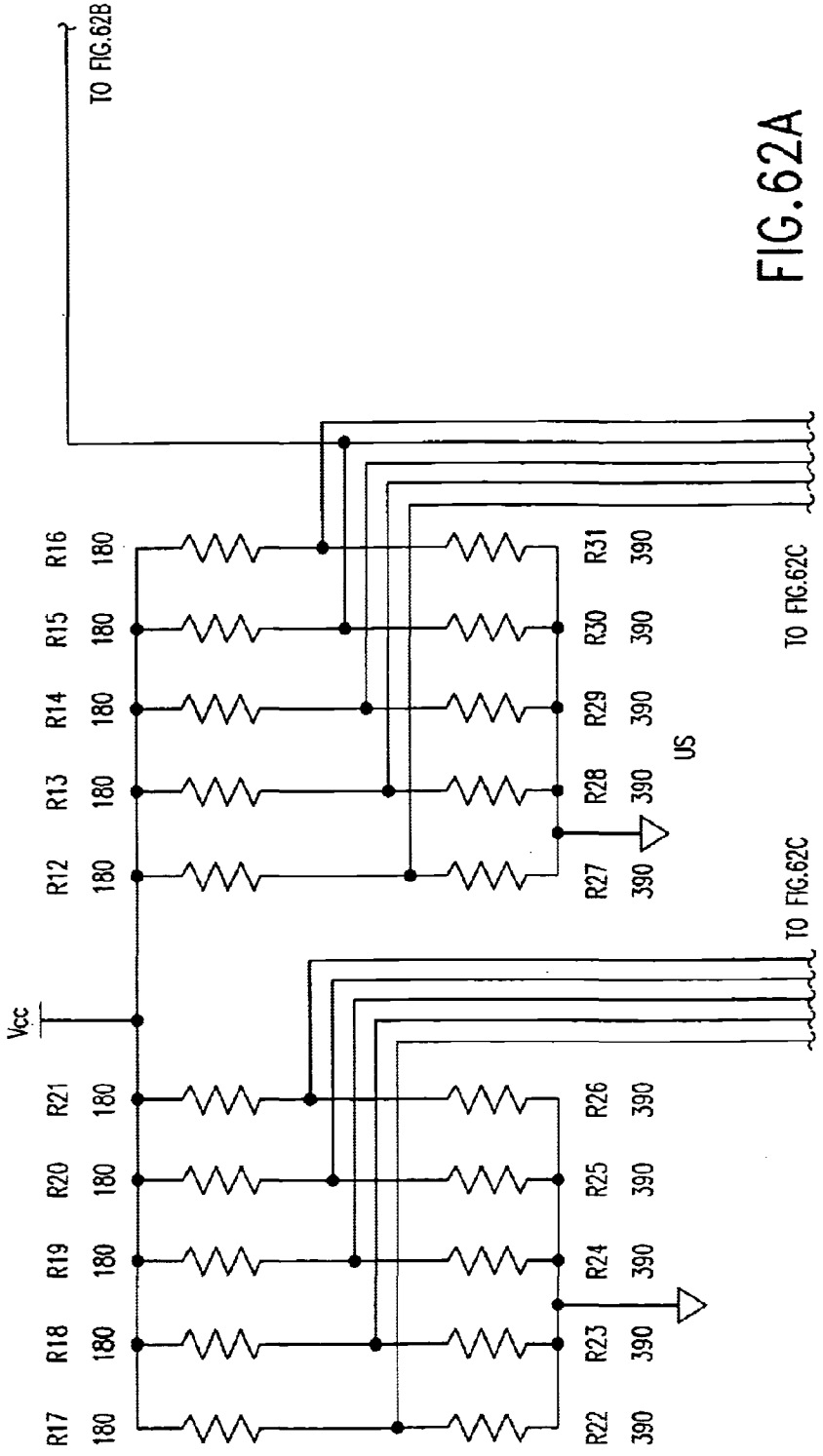
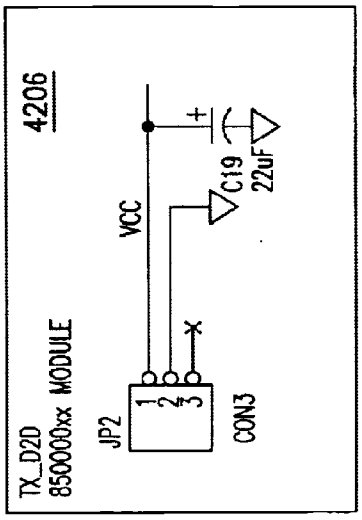
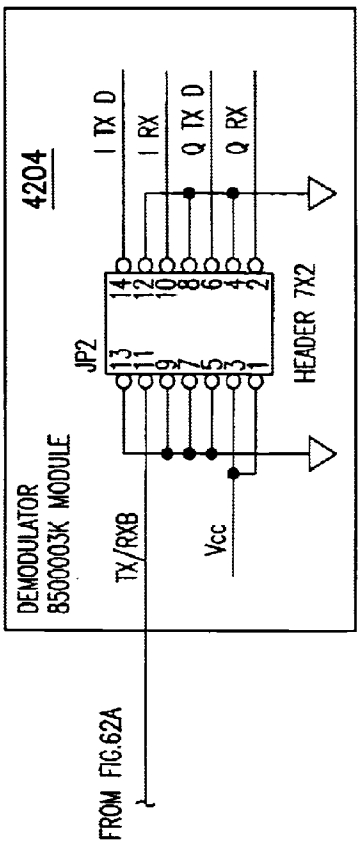

TO FIG.62B
TO FIG.62C
TO FIG.62C
Vcc
R16 180
R15 180
R14 180
R13 180
R12 180
R31 390
R30 390
R29 390
R28 390
R27 390
US
R21 180
R20 180
R19 180
R18 180
R17 180
R26 390
R25 390
R24 390
R23 390
R22 390

FIG.62A


TX_D2D
8500000xx MODULE
4206
JP2
CON3
VCC
C19
22uF


DEMODULATOR
8500003K MODULE
4204
JP2
HEADER 7X2
I TX D
I RX
Q TX D
Q RX
TX/RXB
Vcc
FROM FIG.62A

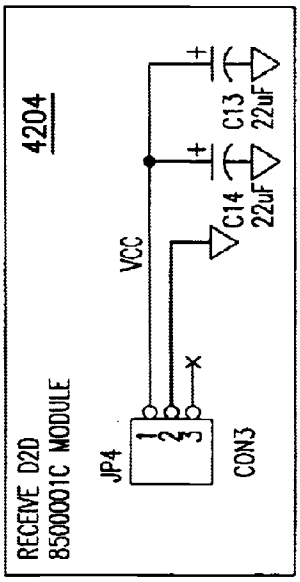

RECEIVE D2D
8500001C MODULE
4204
JP4
CON3
VCC
C14
22uF
C13
22uF

FIG.62B

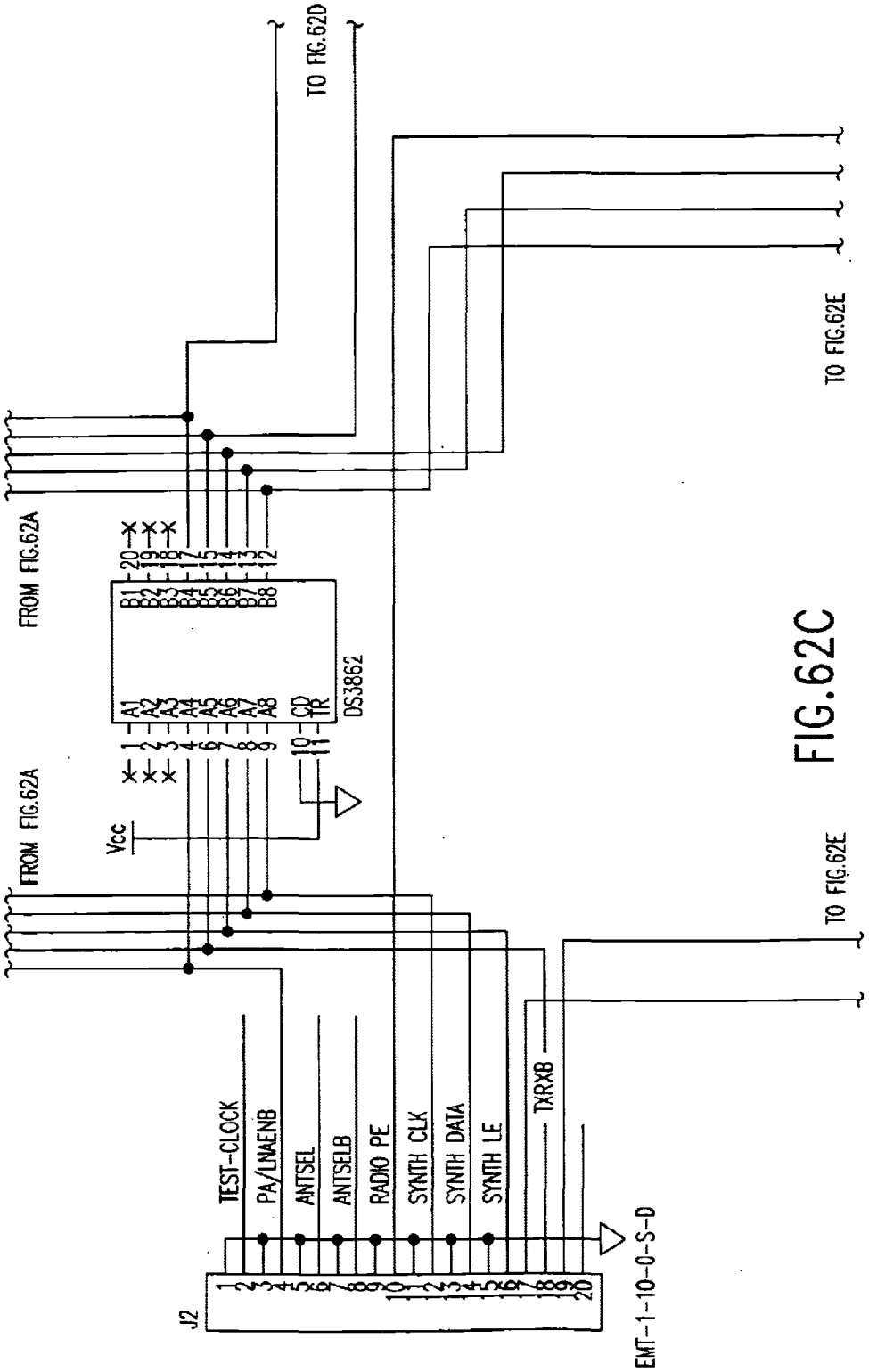

TO FIG.62D
TO FIG.62E
TO FIG.62E
FROM FIG.62A
FROM FIG.62A
DS3862
Vcc
J2
EMT-1-10-0-S-D
TEST-CLOCK
PA/LNAENB
ANTSEL
ANTSELB
RADIO PE
SYNTH CLK
SYNTH DATA
SYNTH LE
TXRXB

FIG.62C

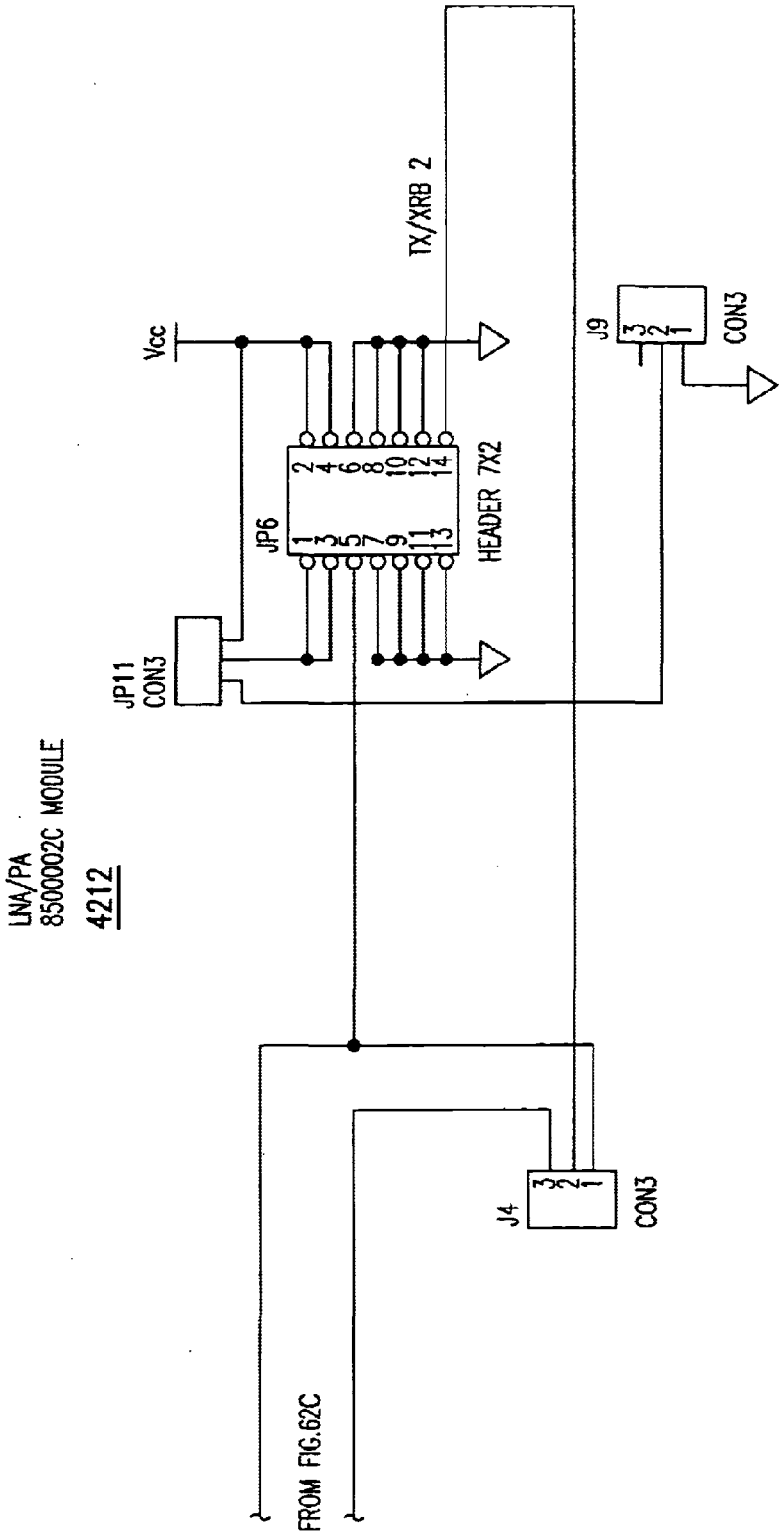

LNA/PA
8500002C MODULE
4212
JP11
CON3
JP6
HEADER 7X2
Vcc
TX/XRB 2
J9
CON3
J4
CON3
FROM FIG.62C

FIG.62D

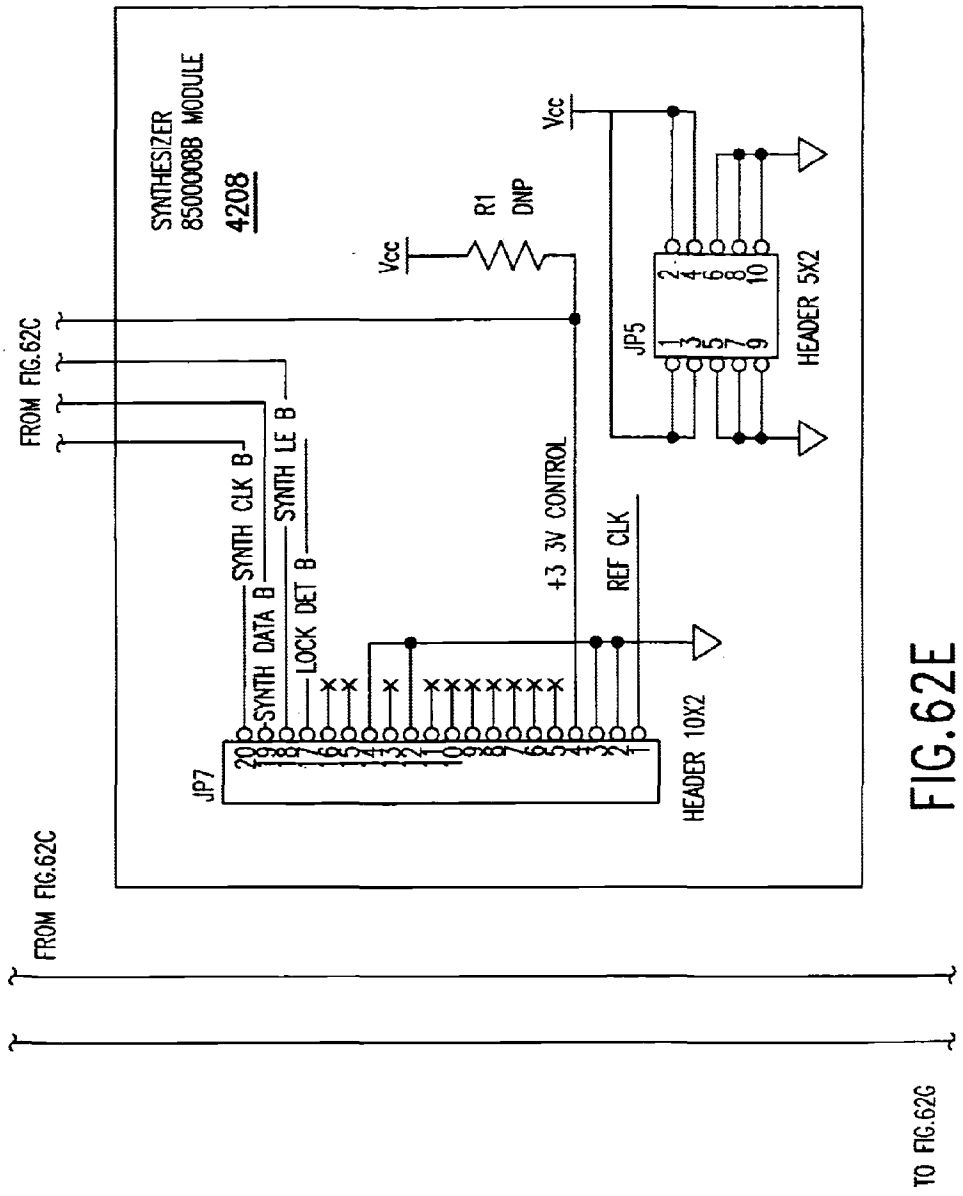

SYNTHESIZER
8500908B MODULE
4208
Vcc
R1
DNP
Vcc
JP5
HEADER 5X2
FROM FIG.62C
SYNTH CLK B
SYNTH LE B
SYNTH DATA B
LOCK DET B
+3 3V CONTROL
REF CLK
JP7
HEADER 10X2
FROM FIG.62C
TO FIG.62G

FIG.62E

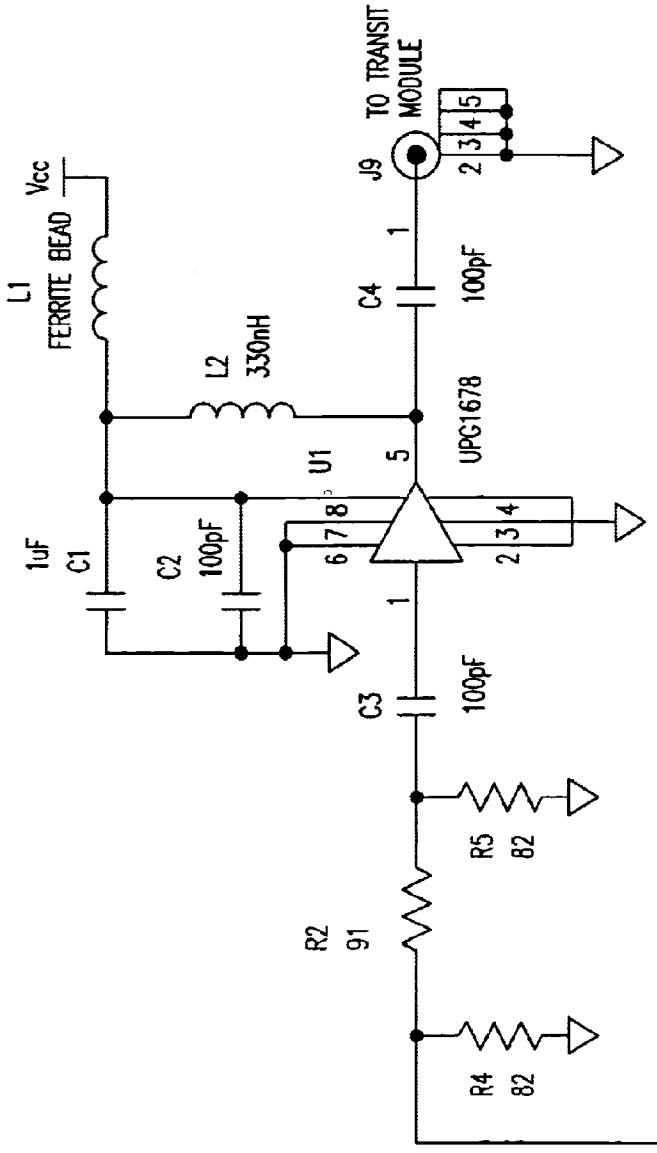

TO TRANSIT MODULE
J9
2 3 4 5
Vcc
L1
FERRITE BEAD
L2
330nH
C4
1
100pF
U1
UPC1678
5
6 7 8
2 3 4
1uF
C1
C2
100pF
1
C3
100pF
R5
82
R2
91
R4
82
TO FIG.62H

FIG.62F

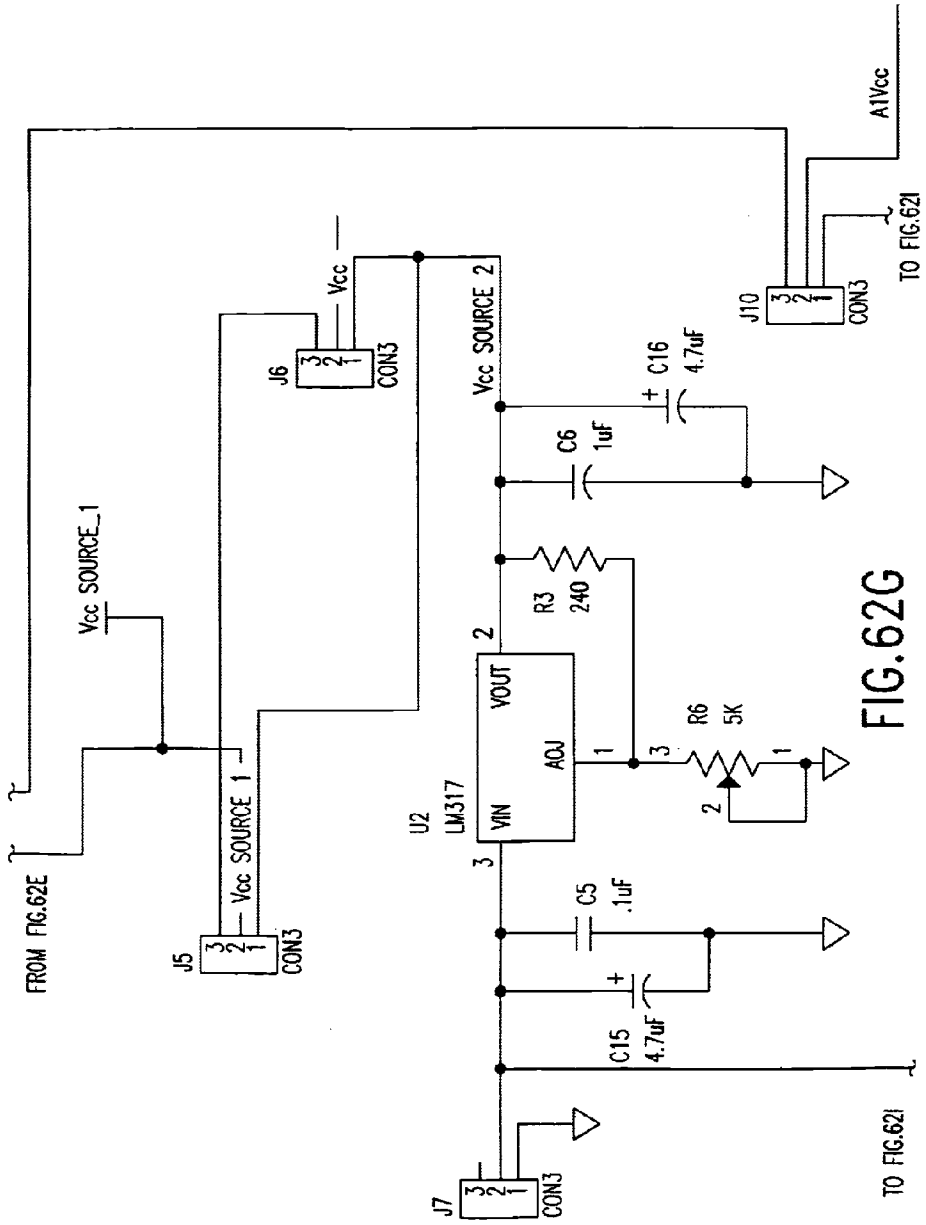

A1Vcc
TO FIG.62I
J10
CON3
Vcc
J6
CON3
Vcc SOURCE 2
C16
4.7uF
C6
1uF
Vcc SOURCE_1
R3
240
2
VOUT
ADJ
1
3
R6
5K
U2
LM317
VIN
3
C5
.1uF
C15
4.7uF
FROM FIG.62E
J5
Vcc SOURCE 1
CON3
J7
CON3
TO FIG.62I

FIG.62G

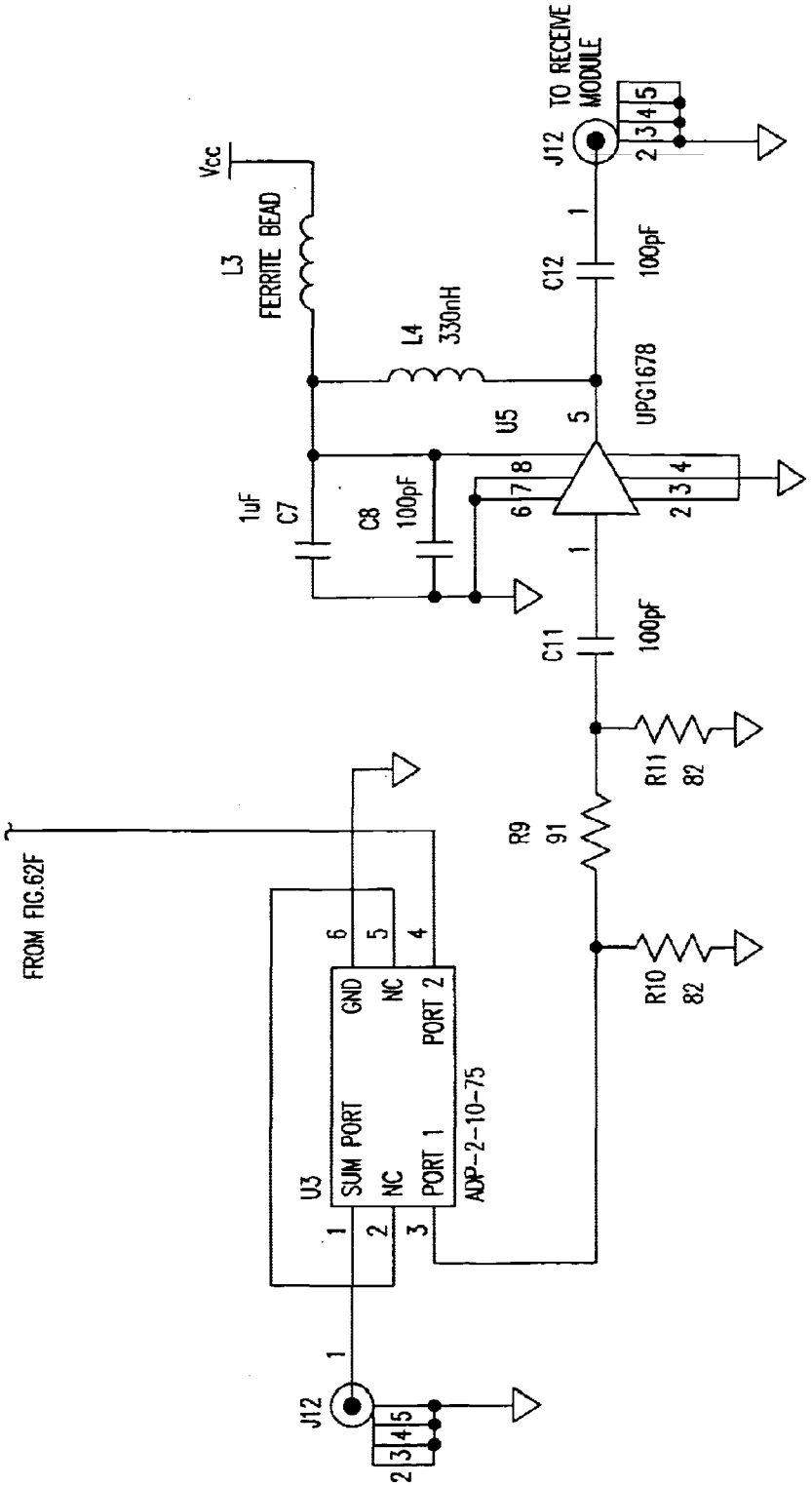

FROM FIG.62F
U3
SUM PORT
NC
PORT 1
GND
NC
PORT 2
ADP-2-10-75
J12
J12
TO RECEIVE MODULE
Vcc
L3
FERRITE BEAD
L4
330nH
C7
1uF
C8
100pF
U5
UPG1678
C11
100pF
C12
100pF
R9
91
R10
82
R11
82

FIG.62H

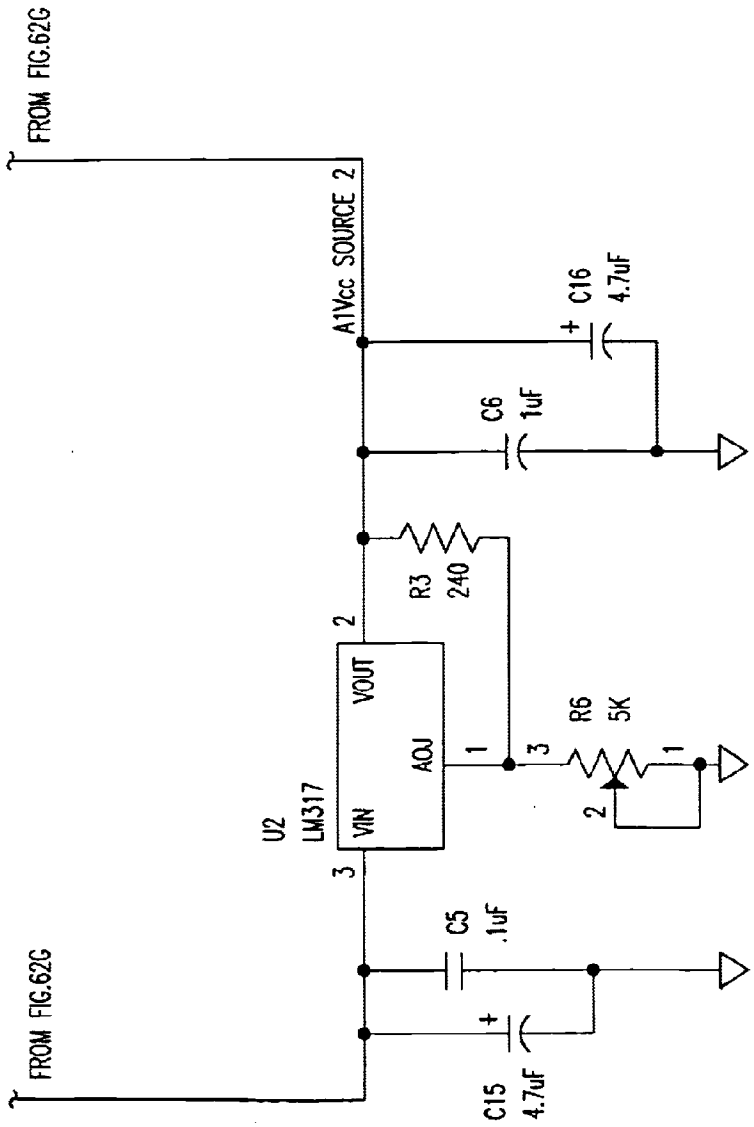

FROM FIG.62G
A1Vcc SOURCE 2
C16
4.7uF
C6
1uF
R3
240
2
VOUT
ADJ
1
3
R6
5K
1
2
U2
LM317
VIN
3
C5
.1uF
FROM FIG.62G
C15
4.7uF

FIG.62I

FIG.63

ITEM	QTY	REFERENCE	PART	DESCRIPTION	PART NUMBER	VENDOR
1	4	C1,C6,C7,C10	1uF	Cap, 1uF, +80-20%,0805	GRM40Y5V105Z016AD	MURATA
2	6	C2,C3,C4,C8,C11,C12	100pF	Cap, 100pF, 5%, COG, 0603	ECU-V1H101JCV	PANASONIC
3	2	C5,C9	.1uF	Cap, .1uF, +80-20%, Y5V, 0603		MURATA
4	3	C13,C14,C19	22uF	Cap, Tant, 22uF, 20%, 20V	T491D226M020AS	KEMET
5	4	C15,C16,C17,C18	4.7uF	Cap, Tant, 4.7uF, 20%, 20V	T491C475M020AS	KEMET
6	2	JP2,JP6	HEADER 7X2	Receptacle, 7x2pin, .050	SFMC-107-L1-S-D	SAMTEK
7	9	JP4, J4, J5, J6, J7, JP9, J9, J10, JP11	CON3	Header, 3pin, .100''	69190-403	BERG
8	1	JP7	HEADER 10X2	Receptacle, 10X2pin, .050	SFMC-110-L1-S-D	SAMTEK
9	1	JP8	HEADER 5X2	Receptacle, 5X2pin, .050	SFMC-105-L1-S-D	SAMTEK
10	1	J2	EHT-1-10-01-S-D	Header, ribbon, 10X2pin, 2mm	EHT-1-10-01-S-D	SAMTEK
11	3	J8,J11,J12	82MMCX-50-0-1	Connector,RF	82MMCX-50-0-1	SUHNER
12	2	L3,L1	Ferrite Bead	Ferrite Bead, 0805	BLM21A121S	MURATA
13	2	L4,L2	330nH	Ind, 330nH, 10%, 0805	LL2012-FR33K	TOKO
14	1	R1	DNP	Res, 0603		PANASONIC
15	2	R9,R2	91	Res, 91 Ohm, 5%, 0603	ERJ-3GSYJ910	PANASONIC
16	2	R7,R3	240	Res, 240 Ohm, 5%, 0603	ERJ-3GSYJ241	PANASONIC
17	4	R4,R5,R10,R11	82	Res, 82 Ohm, 5%, 0603	ERJ-3GSYJ820	PANASONIC
18	2	R8,R6	5K	Var Res, 5K, 10%	3296W001502	BOURNS
19	10	R12, R13, R14, R15, R16, R17, R18, R19, R20, R21	180	Res, 180 Ohm, 5%, 0603	ERJ-3GSYJ181	PANASONIC
20	10	R22, R23, R24, R25, R26, R27, R28, R29, R30, R31	390	Res, 390 Ohm, 5%, 0603	ERJ-3GSYJ391	PANASONIC
21	2	U5,U1	UPG1678	IC, RF Buffer	UPG1678GV	NEC
22	2	U4,U2	LM317	IC, Voltage Regulator	LM317T	NATIONAL
23	1	U3	ADP-2-10-75	RF Splitter	ADP-2-10-75	MINICIRCUITS
24	1	U6	DS3862	IC, Buffer	DS3862WM	NATIONAL
25	1			BOARD	ST8500.641.023V0L01	

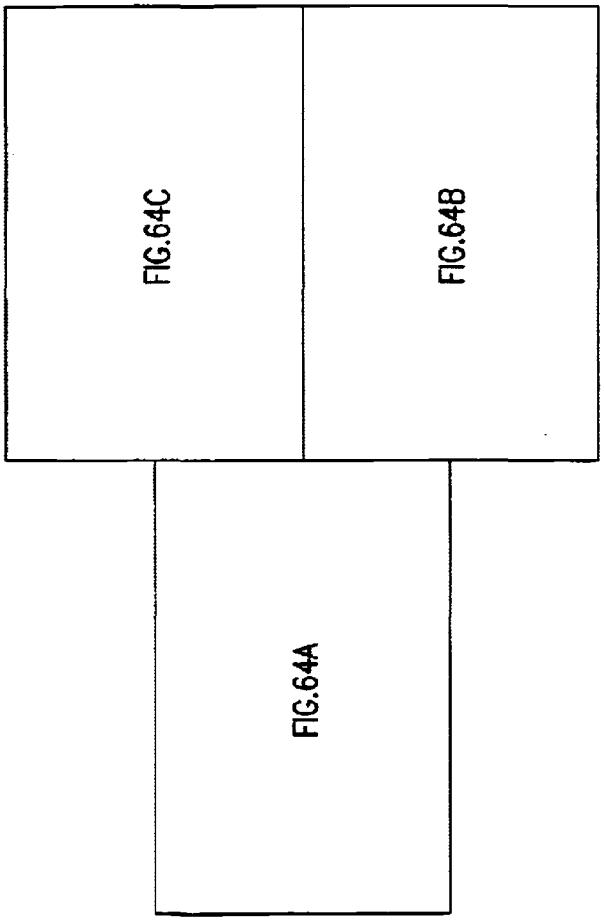


FIG.64

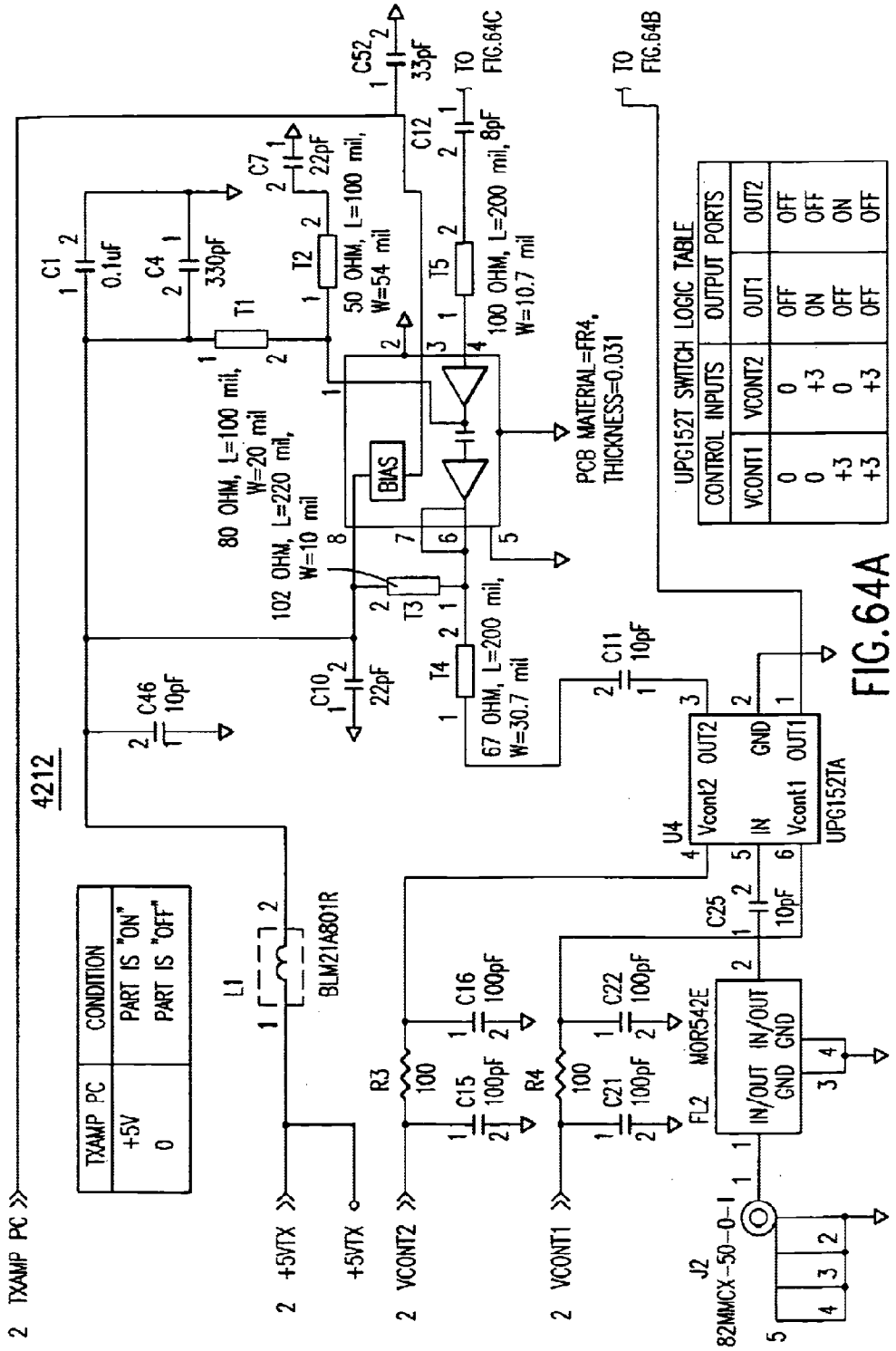

4212
2 TXAMP PC
TXAMP PC | CONDITION
+5V | PART IS "ON"
0 | PART IS "OFF"
C1 0.1uF
C4 330pF
T1
80 OHM, L=100 mil, W=20 mil
102 OHM, L=220 mil, W=10 mil
T2 50 OHM, L=100 mil, W=54 mil
C7 22pF
C52 33pF
C12 8pF
T5 100 OHM, L=200 mil, W=10.7 mil
T3
T4 67 OHM, L=200 mil, W=30.7 mil
C10 22pF
C46 10pF
C11 10pF
BIAS
PCB MATERIAL=FR4, THICKNESS=0.031
TO FIG.64C
TO FIG.64B
UPG152T SWITCH LOGIC TABLE
CONTROL INPUTS | OUTPUT PORTS
VCONT1 | VCONT2 | OUT1 | OUT2
0 | 0 | OFF | OFF
0 | +3 | ON | OFF
+3 | 0 | OFF | ON
+3 | +3 | OFF | OFF
U4 UPG152TA
Vcont2 OUT2 GND
IN Vcont1 OUT1
L1 BLM21A801R
2 +5VTX
+5VTX
2 VCONT2
2 VCONT1
R3 100
R4 100
C15 100pF
C16 100pF
C21 100pF
C22 100pF
C25 10pF
FL2 MOR542E
IN/OUT IN/OUT
GND GND
J2 82MMCX-50-0-1

FIG.64A

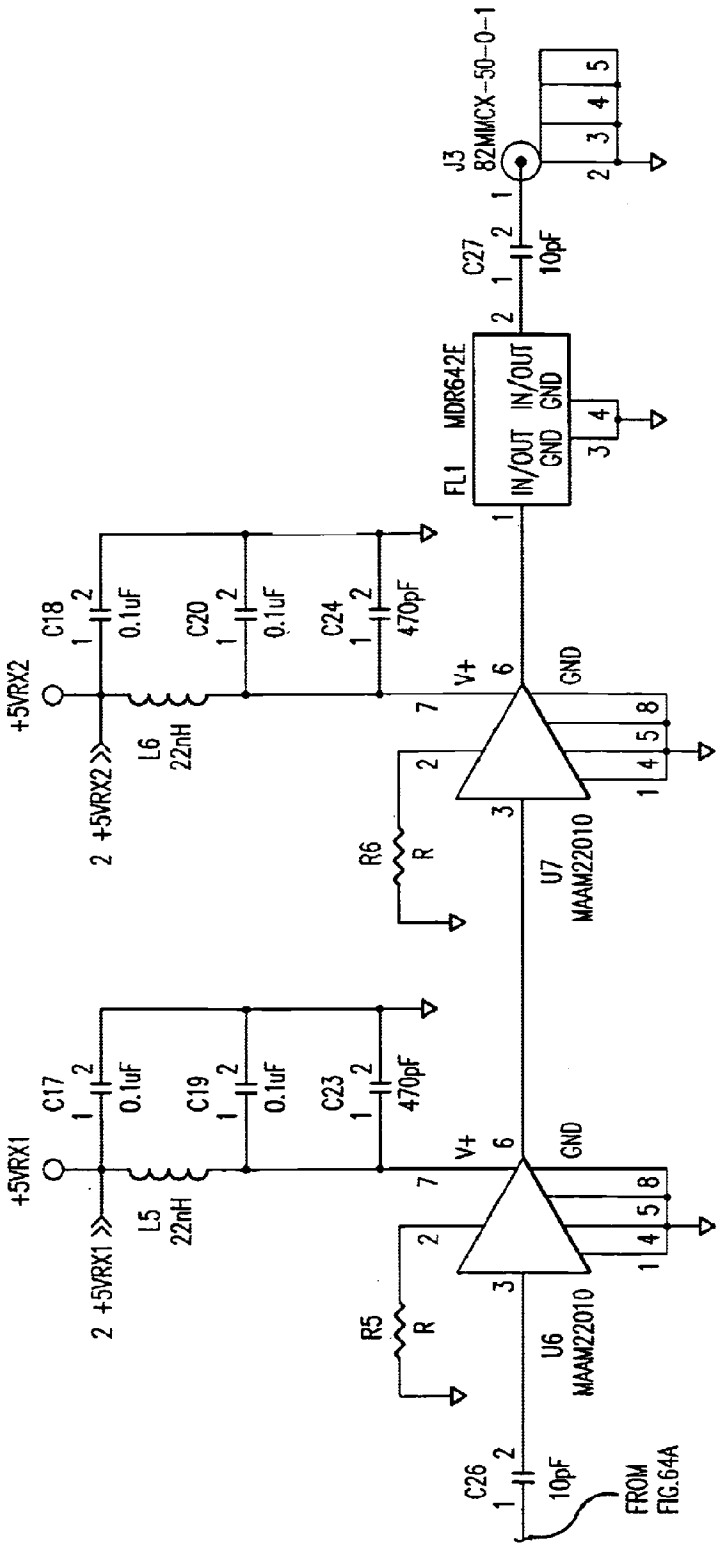

J3
82MMCX-50-0-1
C27
10pF
FL1
MDR642E
IN/OUT
GND
IN/OUT
GND
C18
0.1uF
C20
0.1uF
C24
470pF
+5VRX2
L6
22nH
2 +5VRX2
V+
GND
R6
R
U7
MAAM22010
C17
0.1uF
C19
0.1uF
C23
470pF
+5VRX1
L5
22nH
2 +5VRX1
R5
R
U6
MAAM22010
C26
10pF
FROM
FIG.64A

FIG.64B

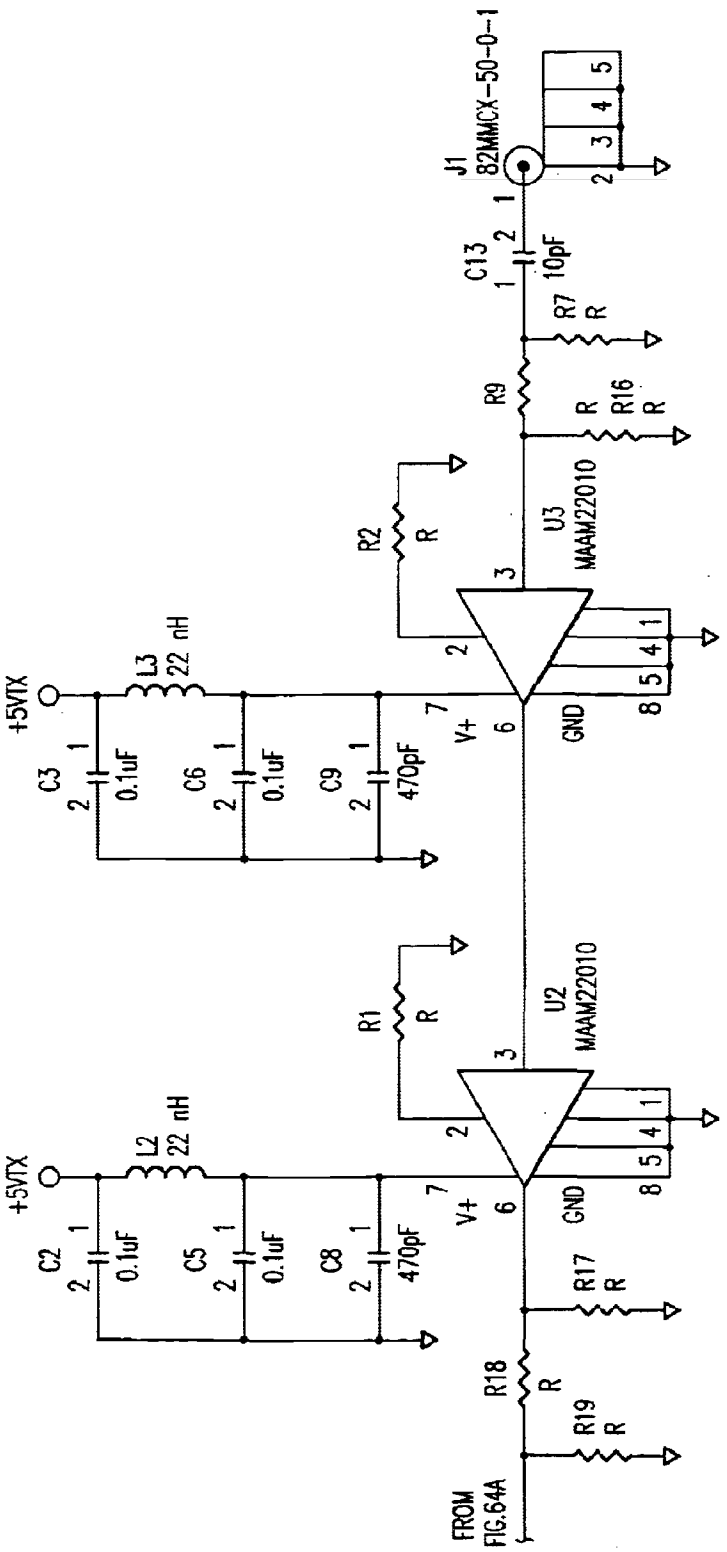

J1
82MMCX-50-0-1
C13
10pF
R7
R
R9
R
R16
R
U3
MAAM22010
R2
R
L3
22 nH
+5VTX
C3
0.1uF
C6
0.1uF
C9
470pF
V+
GND
U2
MAAM22010
R1
R
L2
22 nH
+5VTX
C2
0.1uF
C5
0.1uF
C8
470pF
V+
GND
R17
R
R18
R
R19
R
FROM
FIG.64A

FIG.64C

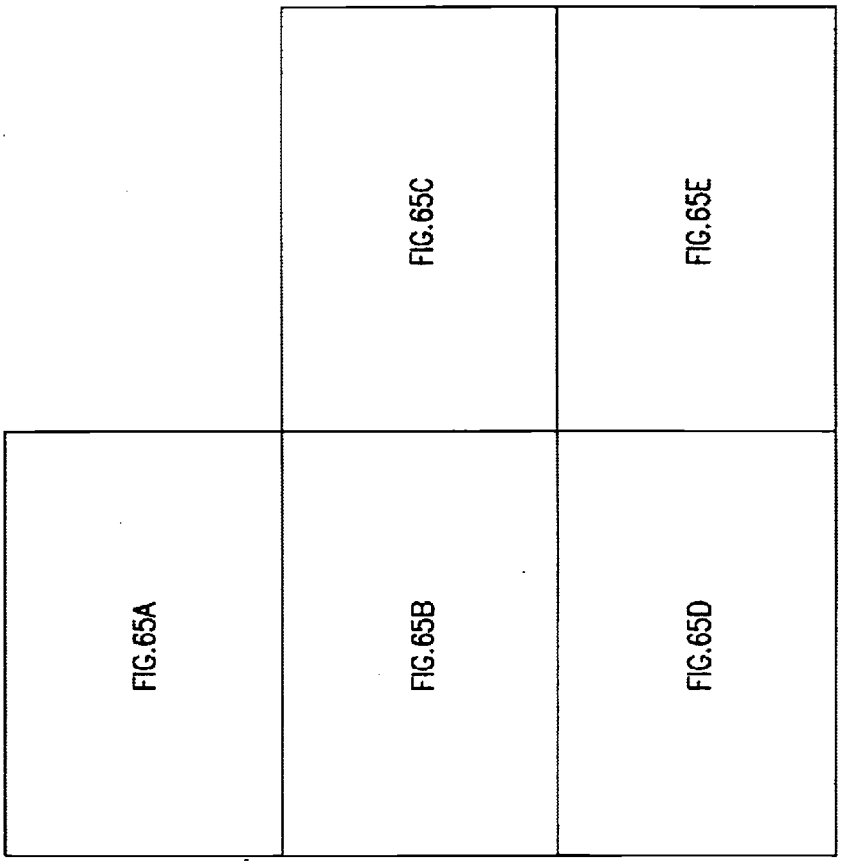


FIG.65

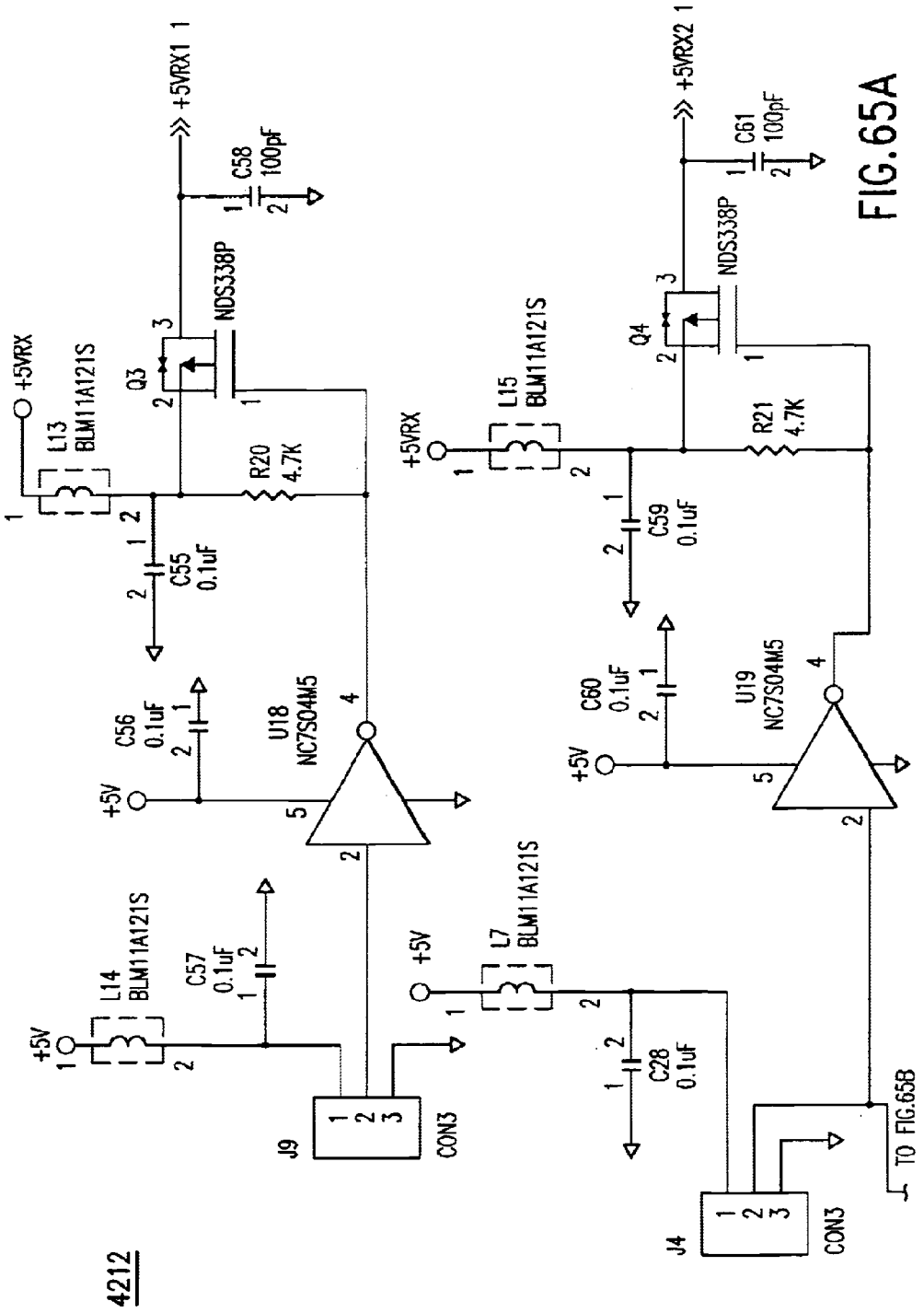

+5VRX
L13 BLM11A121S
Q3 NDS338P
+5VRX1
C58 100pF
R20 4.7K
C55 0.1uF
C56 0.1uF
U18 NC7S04M5
+5V
L14 BLM11A121S
C57 0.1uF
J9 CON3
+5VRX
L15 BLM11A121S
Q4 NDS338P
+5VRX2
C61 100pF
R21 4.7K
C59 0.1uF
C60 0.1uF
U19 NC7S04M5
+5V
L7 BLM11A121S
C28 0.1uF
J4 CON3
TO FIG.65B
4212

FIG.65A

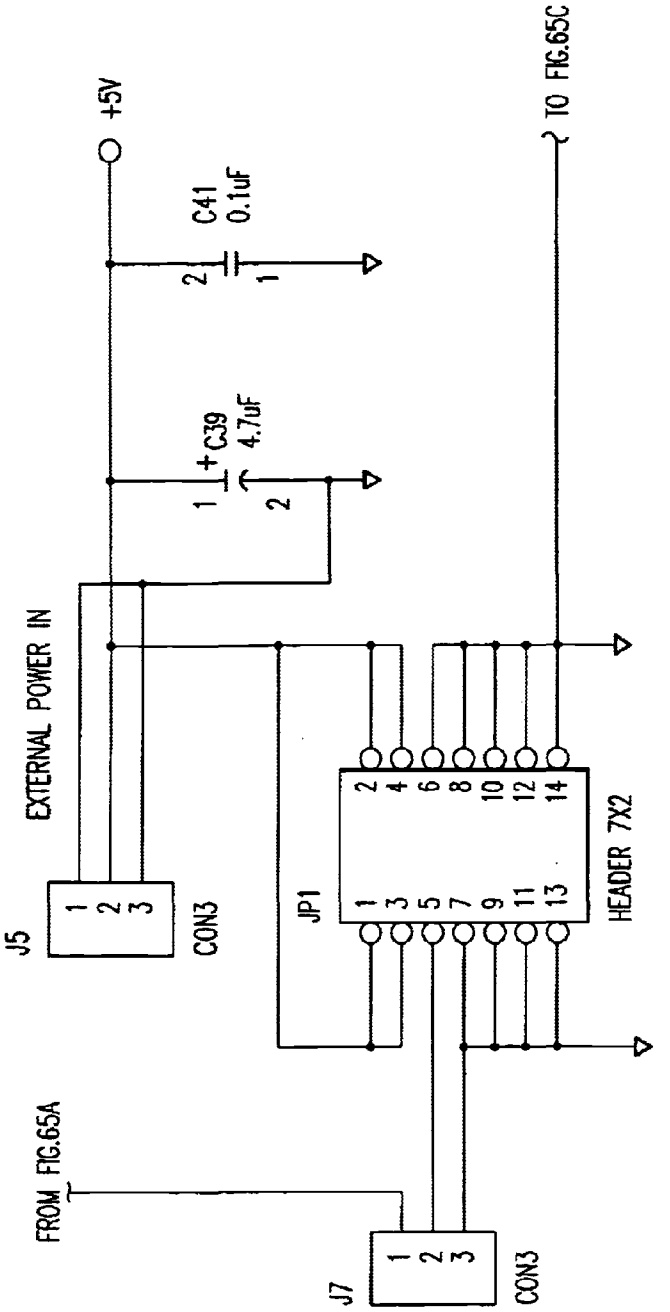

+5V
C41
0.1uF
2
1
TO FIG.65C
+C39
4.7uF
1
2
EXTERNAL POWER IN
J5
1
2
3
CON3
JP1
2 4 6 8 10 12 14
1 3 5 7 9 11 13
HEADER 7X2
FROM FIG.65A
J7
1
2
3
CON3

FIG.65B

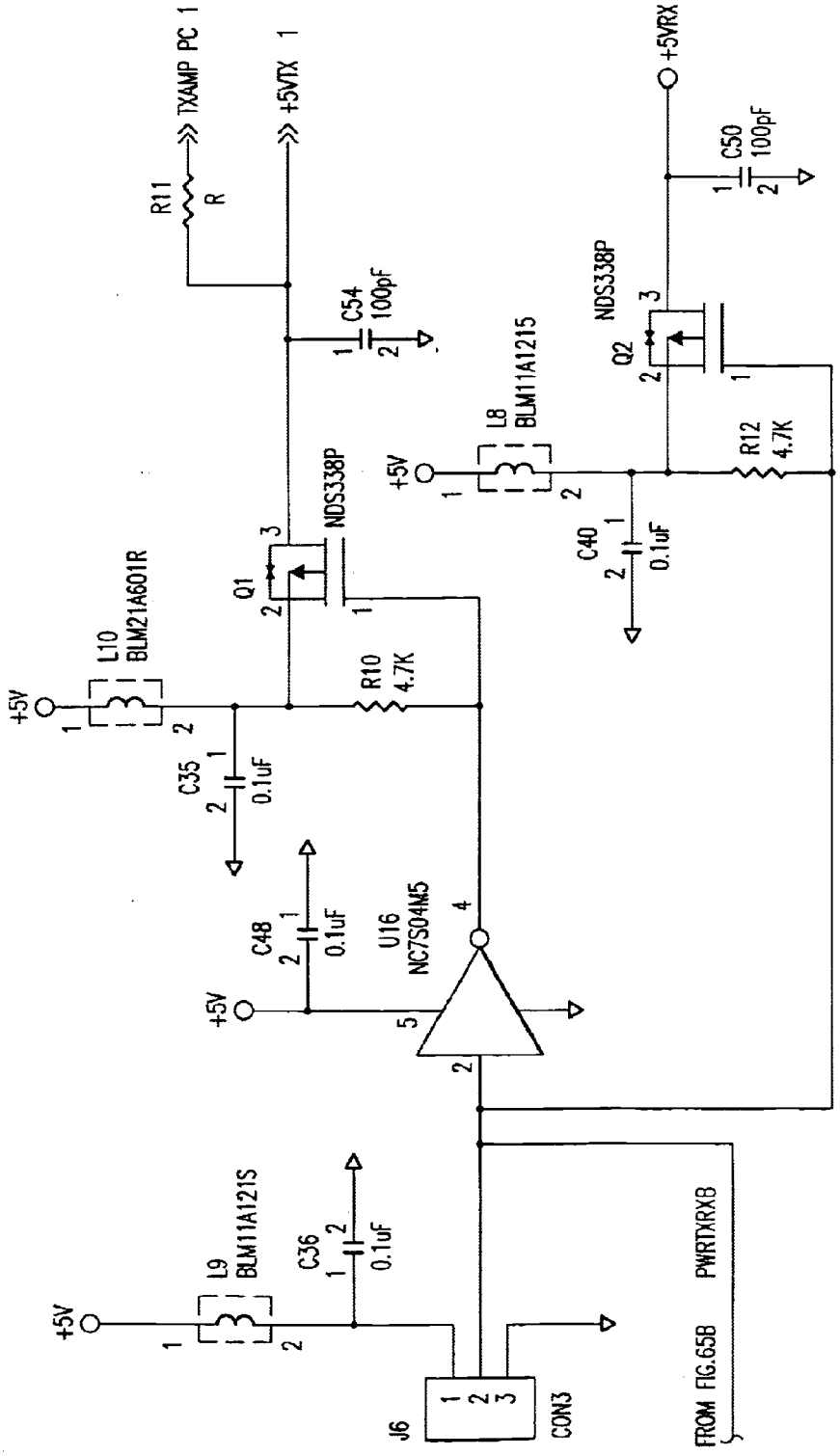

TXAMP PC 1
+5VTX 1
+5VRX
R11
R
C54
100pF
C50
100pF
NDS338P
Q2
L8
BLM11A1215
+5V
R12
4.7K
C40
0.1uF
NDS338P
Q1
L10
BLM21A601R
R10
4.7K
C35
0.1uF
C48
0.1uF
U16
NC7S04M5
L9
BLM11A121S
C36
0.1uF
J6
CON3
PWRTXRXB
FROM FIG.65B

FIG.65C

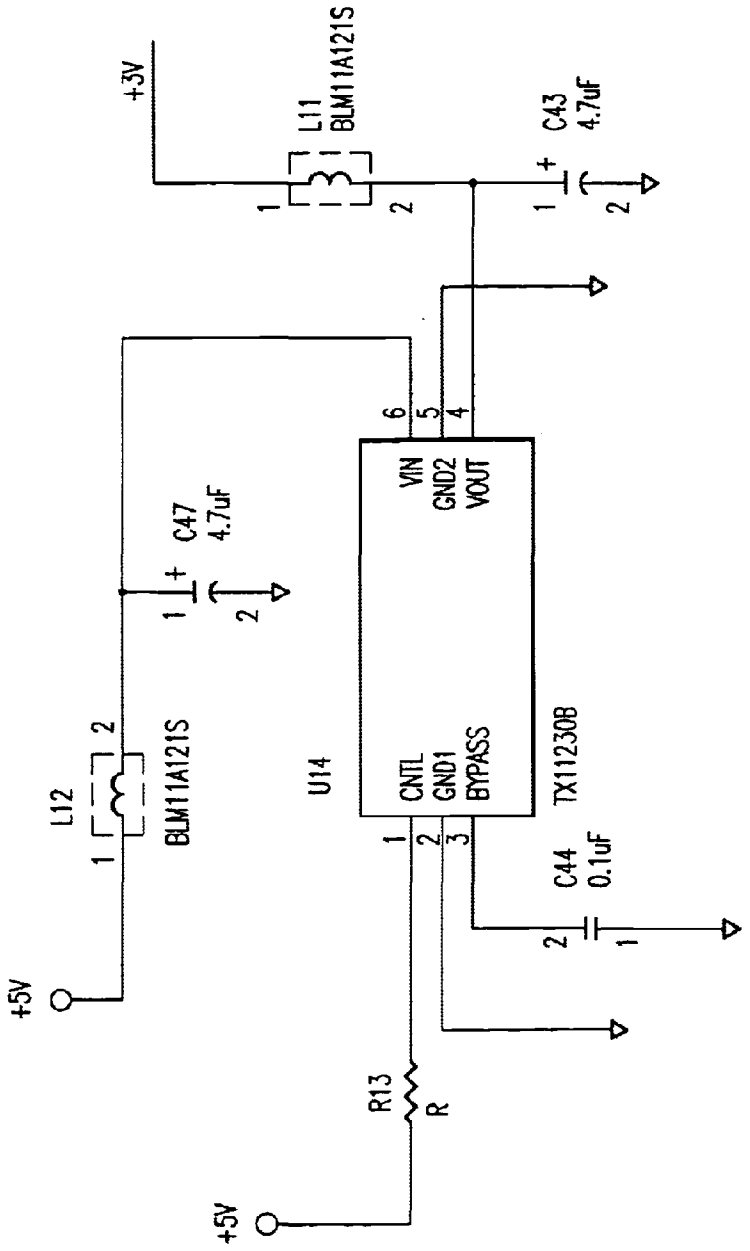

+3V
L11
BLM11A121S
C43
4.7uF
C47
4.7uF
L12
BLM11A121S
U14
VIN
GND2
VOUT
CNTL
GND1
BYPASS
TX11230B
C44
0.1uF
+5V
+5V
R13
R

FIG.65D

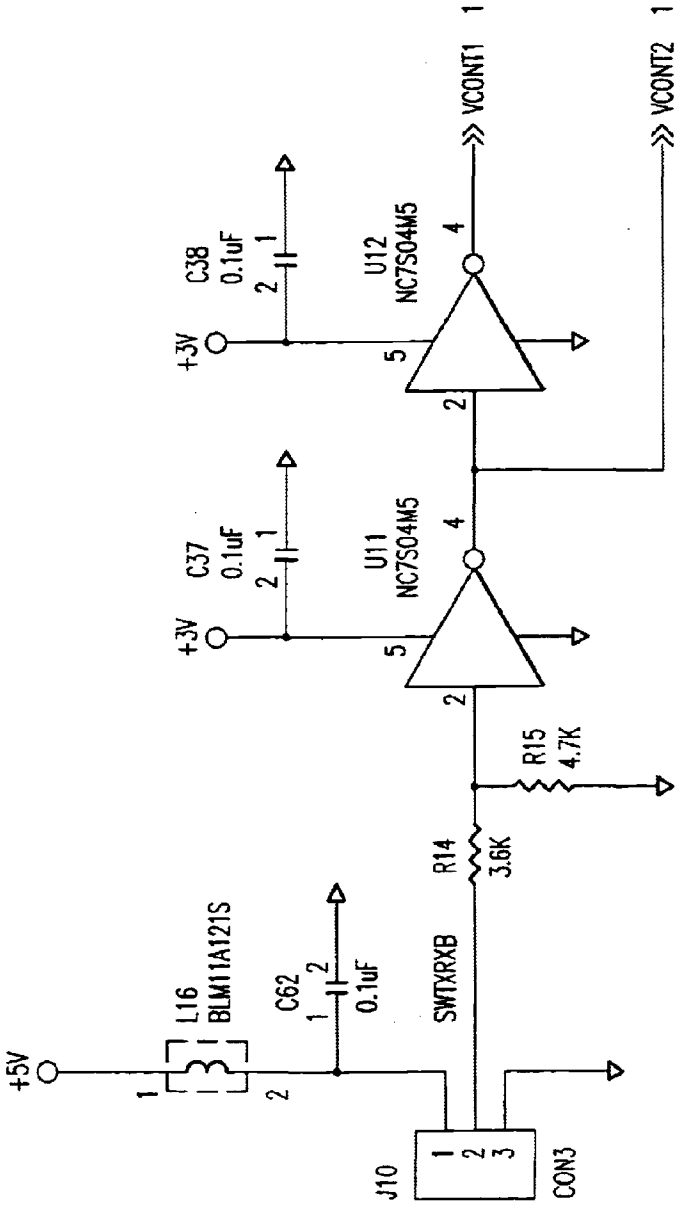

VCONT1
VCONT2
U12
NC7SO4M5
U11
NC7SO4M5
C38
0.1uF
C37
0.1uF
C62
0.1uF
+3V
+3V
+5V
L16
BLM11A121S
R15
4.7K
R14
3.6K
SWTXRXB
J10
CON3

FIG.65E

ITEM	QTY	REFERENCE	PART	MANUFACT.	PART DESCRIPTION	PART NUMBER
1	24	C1,C2,C3,C5,C6,C17,C18, C19,C20,C28,C35,C36,C37, C38,C40,C41,C44,C48,C55, C56,C57,C59,C60,C62	0.1uF	MURATA	.1uF,0603,X7R,20%,16V	GRM39X7R104M016
2	1	C4	330pF	MURATA	330pF,0603,COG,10%,50	GRM39COG331K050
3	2	C10,C7	22pF	MURATA	22pF,0603,COG,10%,50	GRM39COG220K050
4	4	C8,C9,C23,C24	470pF	MURATA	470pF,0603,COG,10%,50	GRM39COG471K050
5	6	C11,C13,C25,C26,C27,C46	10pF	MURATA	10pF,0603,COG,10%,50	GRM39COG100K050
6	1	C12	8pF	MURATA	8pF,0603,COG,10%,50	GRM39COG080K050
7	8	C15,C16,C21,C22,C50,C54 C58,C61	100pF	MURATA	100pF,0603,COG,10%,50	GRM39COG101K050
8	3	C39,C43,C47	4.7uF	PANASONIC	4.7uF TANTALUM,16V	ECS-T1CY475R
9	1	C52	33pF	MURATA	330pF,0603,COG,10%,50	GRM3COG330K050
10	2	FL1,FL2	MDR642E	SOSHIN	2.4-2.5GHz BPF	MDR642E
11	1	JP1	HEADER 7X2	SAMTEC	DUAL ROW, 7 PINS PER ROW	FTSH-107-01-F-D
12	3	J1,J2,J3	82MMCX-50-0-1	SUHNER	RF CONNECTOR	82MMCX-50-0-1
13	6	J4,J5,J6,J7,J9,J10	CON3	BERG	3 PIN HEADER W RETENTIVE LEG	69190-403H
14	2	L10,L1	BLM21A601R	MURATA	600 OHMS@100MHz,500mA FERRITE BEAD	BLM21A601R
15	4	L2,L3,L5,L6	22nH	COILCRAFT	22nH,0805CS (2012),5%	0805CS-220X-BC
16	9	L7,L8,L9,L11,L12,L13,L14, L15,L16	BLM11A121S	MURATA	RF BEAD	BLM11A121S
17	4	Q1,Q2,Q3,Q4	NDS336P	NATIONAL	P-CHANNEL FET	NDS336P
18	12	R1,R2,R5,R6,R7,R9,R11, R13,R16,R17,R18,R19	R	PANASONIC		
19	2	R3,R4	100	PANASONIC	0603,100,5%,1/16W	ERJ-3GSY-J-101
20	5	R10,R12,R15,R20,R21	4.7K	PANASONIC	0603,4.7K,5%,1/16W	ERJ-3GSY-J-472

FIG.66A

21	1	R14	3.6K	PANASONIC	0603,3.6K,5%,1/16W	ERJ-3GSY-J-362
22	1	T1	80 OHM,L=100 MIL,W=20 MIL		80 OHM,L=100 MIL,W=20 MIL	
23	1	T2	50 OHM,L=100 MIL,W=54 MIL		50 OHM,L=100 MIL,W=54 MIL	
24	1	T3	102 OHM,L=220 MIL,W=10 MIL		102 OHM,L=220 MIL,W=10 MIL	
25	1	T4	67 OHM,L=200 MIL,W=30.7 MIL		67 OHM,L=200 MIL,W=30.7 MIL	
26	1	T5	100 OHM,L=200 MIL,W=10.7MIL		100 OHM,L=200 MIL,W=10.7 MIL	
27	4	U2,U3,U6,U7	MAAM22010	MACOM	2.4-2.5 GHz LNA	MAAM22010
28	1	U4	UPG152TA	NEC	RF SWITCH	UPG152TA
29	5	U11,U12,U16,U18,U19	NC7S04M5	NATIONAL	INVERTER	NC7S04M5
30	1	U14	TKN11230B	TOKO	VOLTAGE REGULATOR	TK11230B
31	1	U17	RF2128P	RFMD	MEDIUM POWER LINEAR AMPLIFIER	RF2128P
32	1				BOARD	B500.641.024 VOL.

FIG.66B

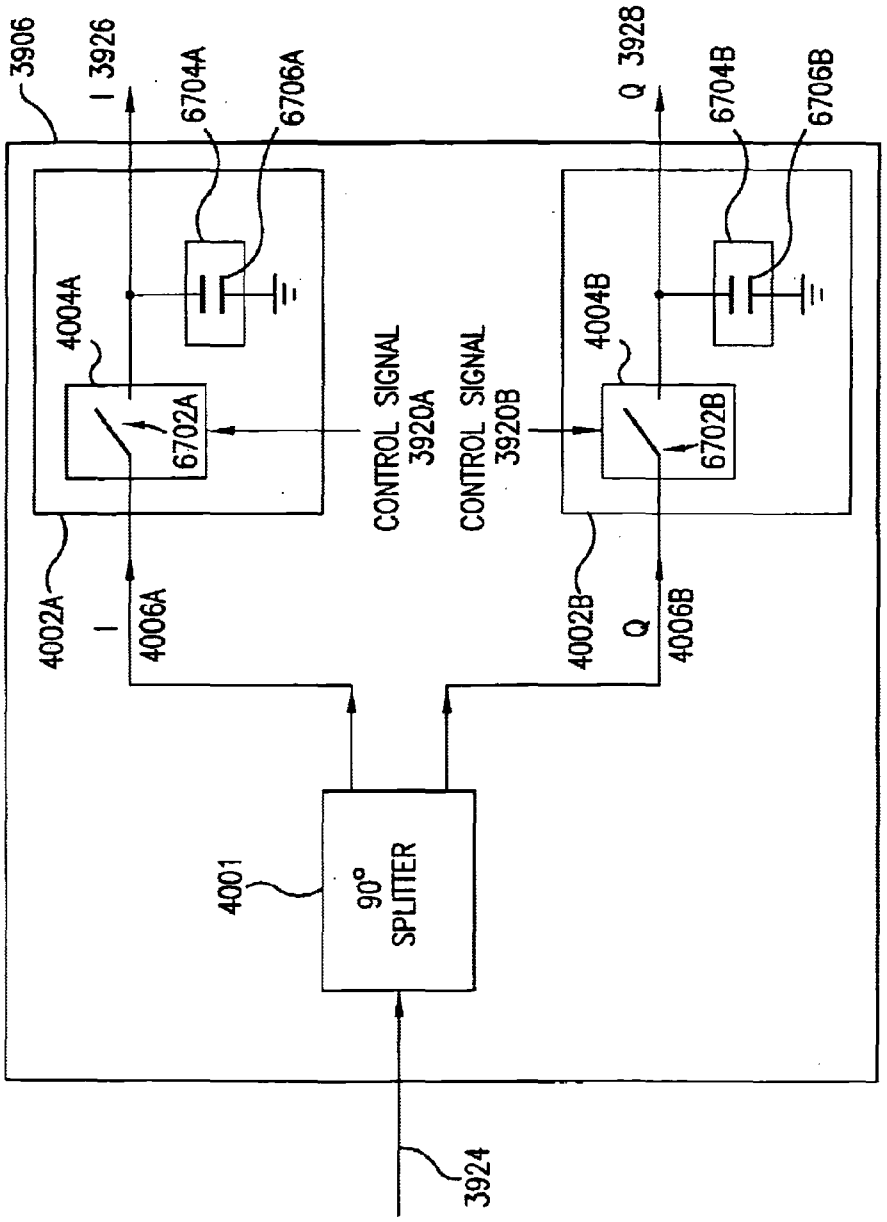

3906
I 3926
6704A
6706A
Q 3928
6704B
6706B
4004A
4004B
CONTROL SIGNAL 3920A
CONTROL SIGNAL 3920B
6702A
6702B
4002A
I
4006A
4002B
Q
4006B
4001
90° SPLITTER
3924

FIG.67A

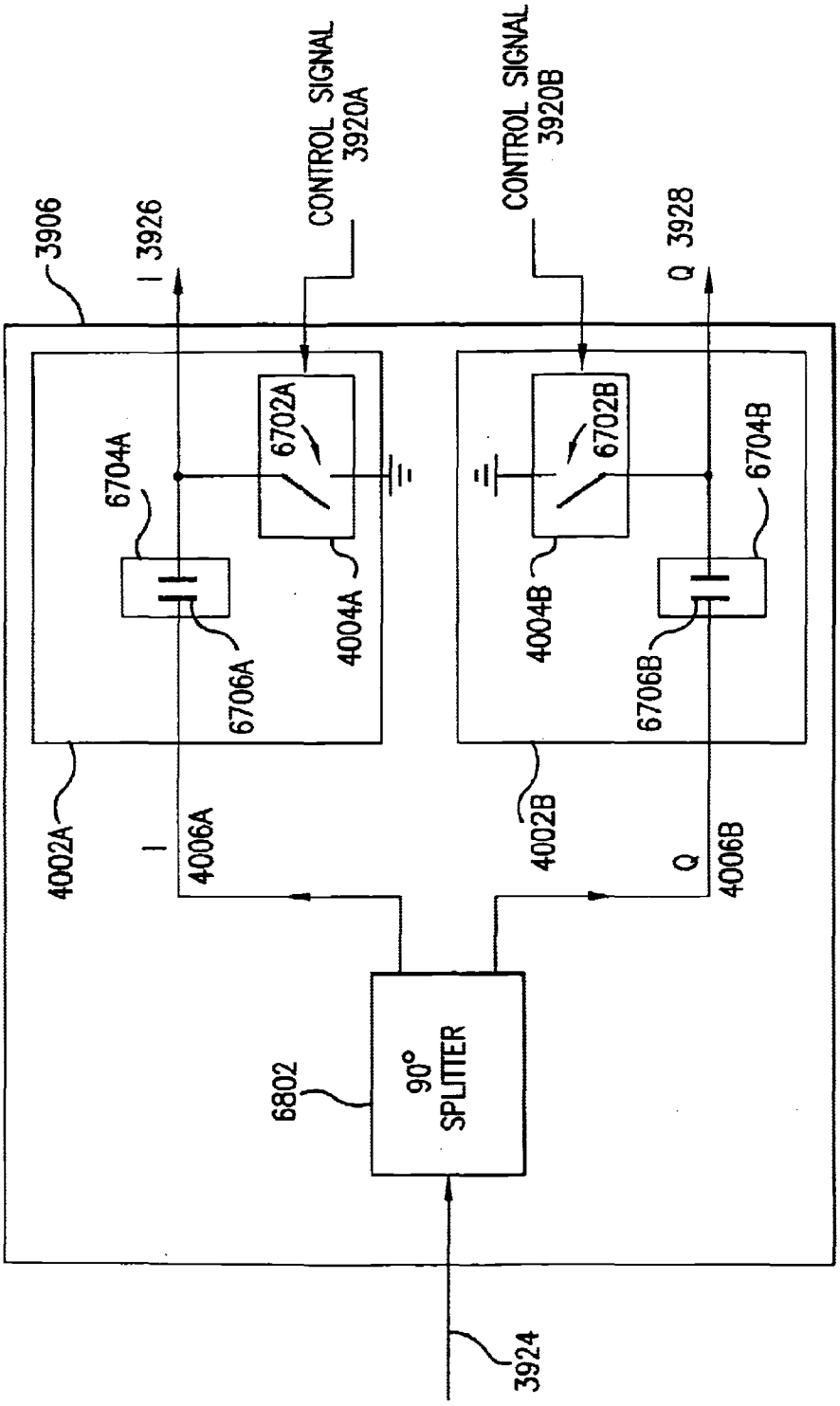
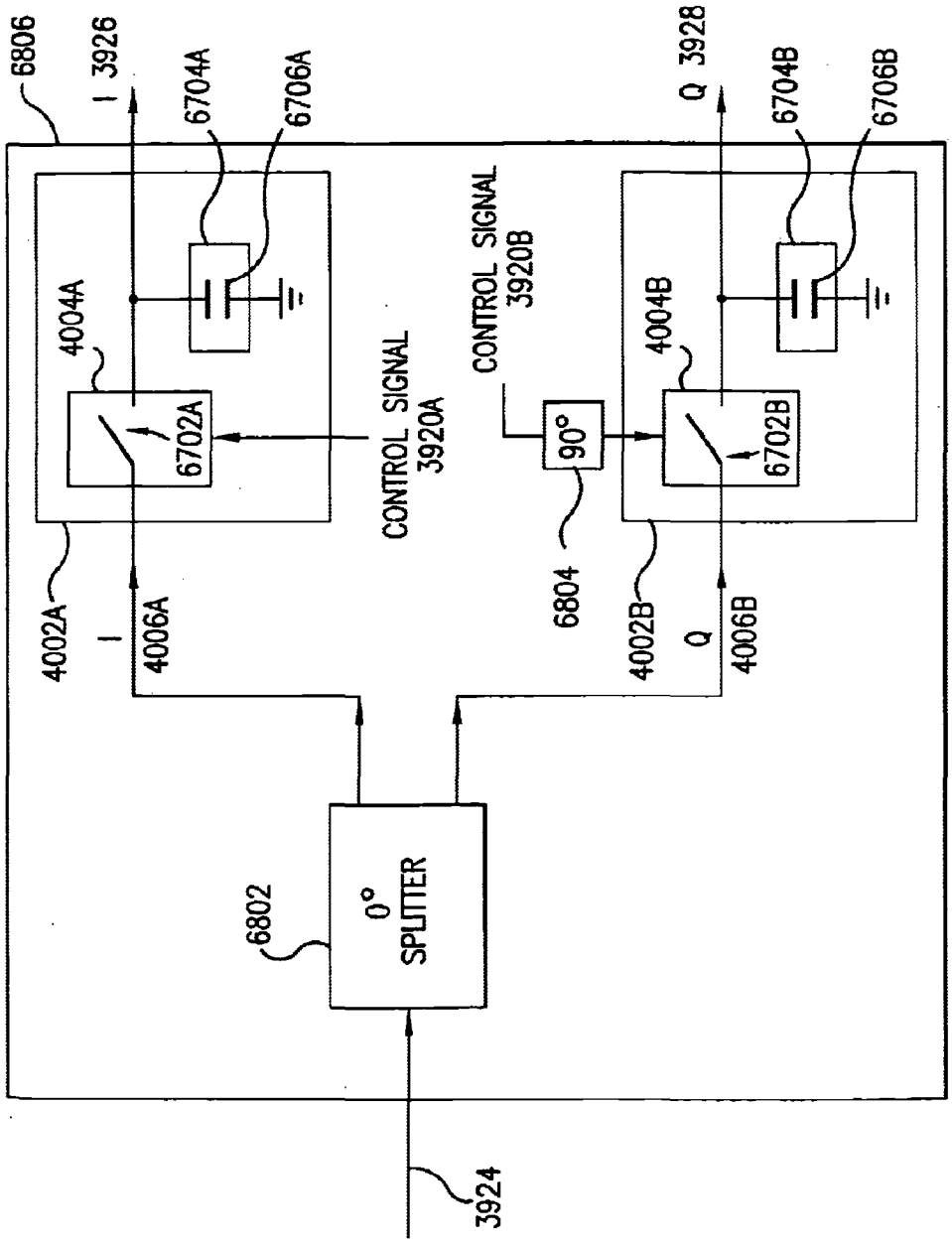

3906
I 3926
CONTROL SIGNAL 3920A
CONTROL SIGNAL 3920B
Q 3928
6704A
6702A
6702B
6704B
4004A
4004B
6706A
6706B
4002A
I
4006A
4002B
Q
4006B
6802
90° SPLITTER
3924

FIG.67B

FIG.68A


6806
I 3926
6704A
6706A
Q 3928
6704B
6706B
4004A
6702A
CONTROL SIGNAL 3920A
CONTROL SIGNAL 3920B
4004B
6702B
90°
6804
4002A
I
4006A
4002B
Q
4006B
6802
0° SPLITTER
3924

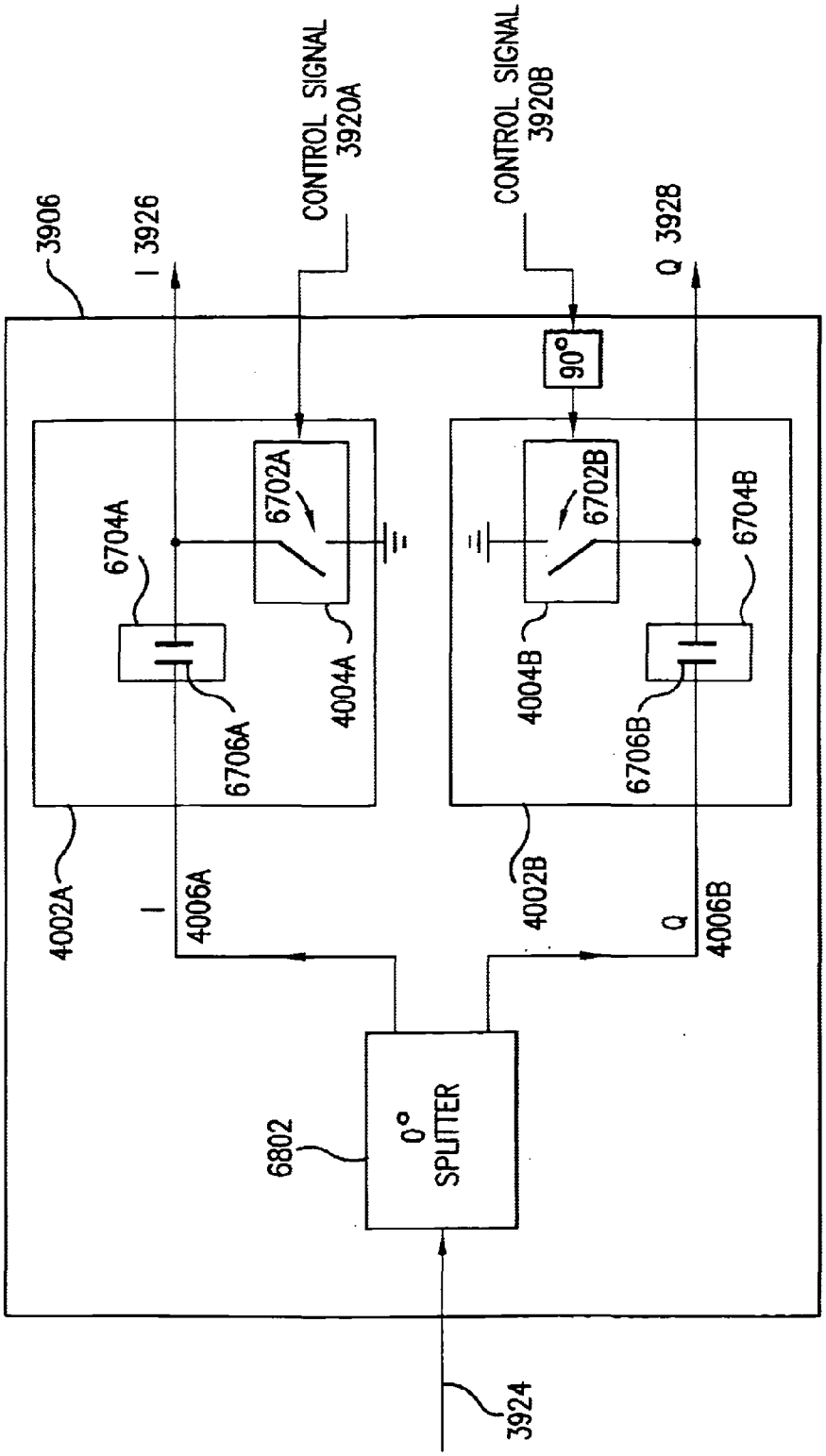
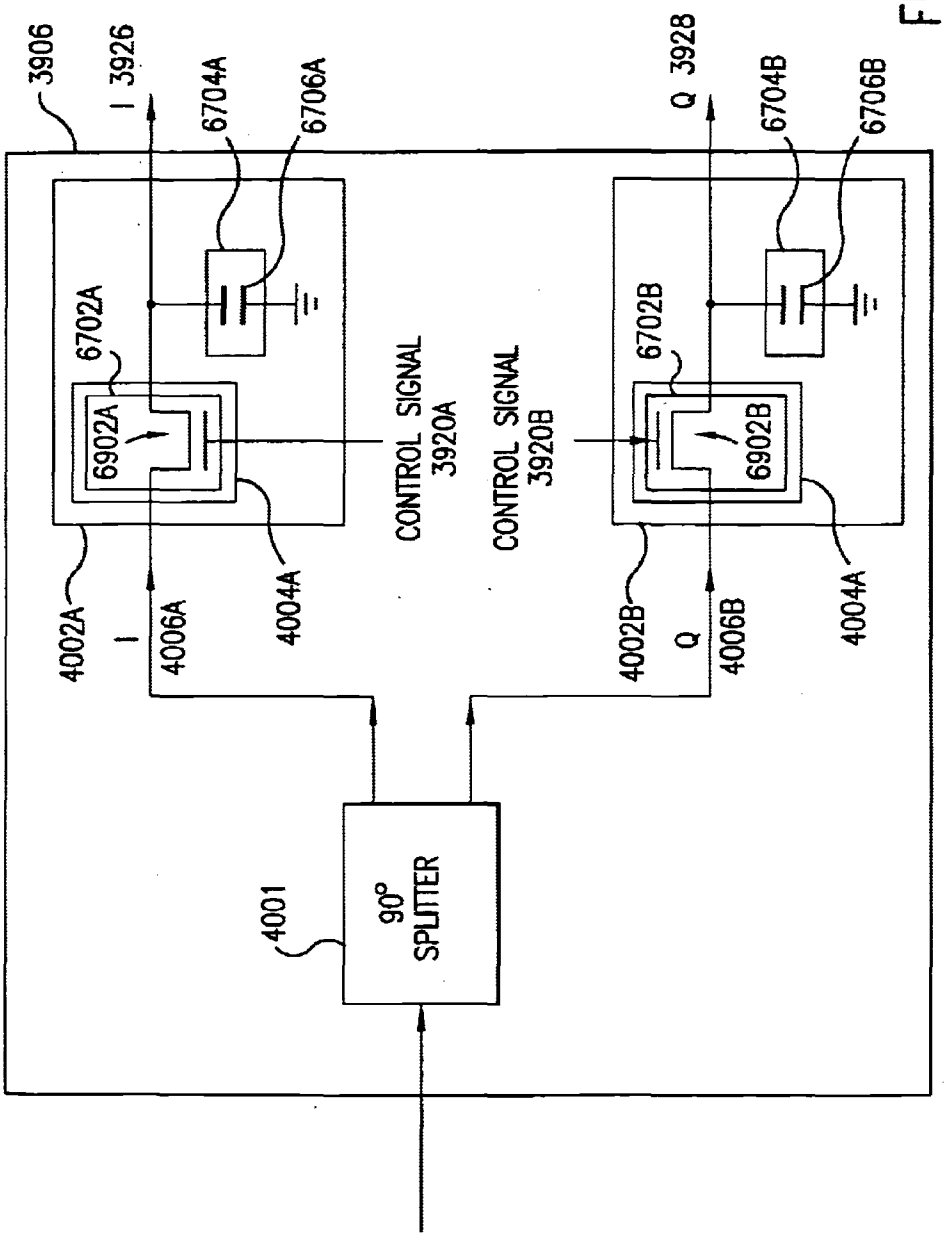

3906
I 3926
CONTROL SIGNAL 3920A
CONTROL SIGNAL 3920B
Q 3928
90°
6702A
6702B
6704A
6704B
4004A
4004B
6706A
6706B
4002A
4002B
I
4006A
Q
4006B
6802
0° SPLITTER
3924

FIG.68B

FIG.69A


3906
I 3926
6704A
6706A
Q 3928
6704B
6706B
6702A
6902A
CONTROL SIGNAL 3920A
CONTROL SIGNAL 3920B
6702B
6902B
4002A
I
4006A
4004A
4002B
Q
4006B
4004A
4001
90° SPLITTER

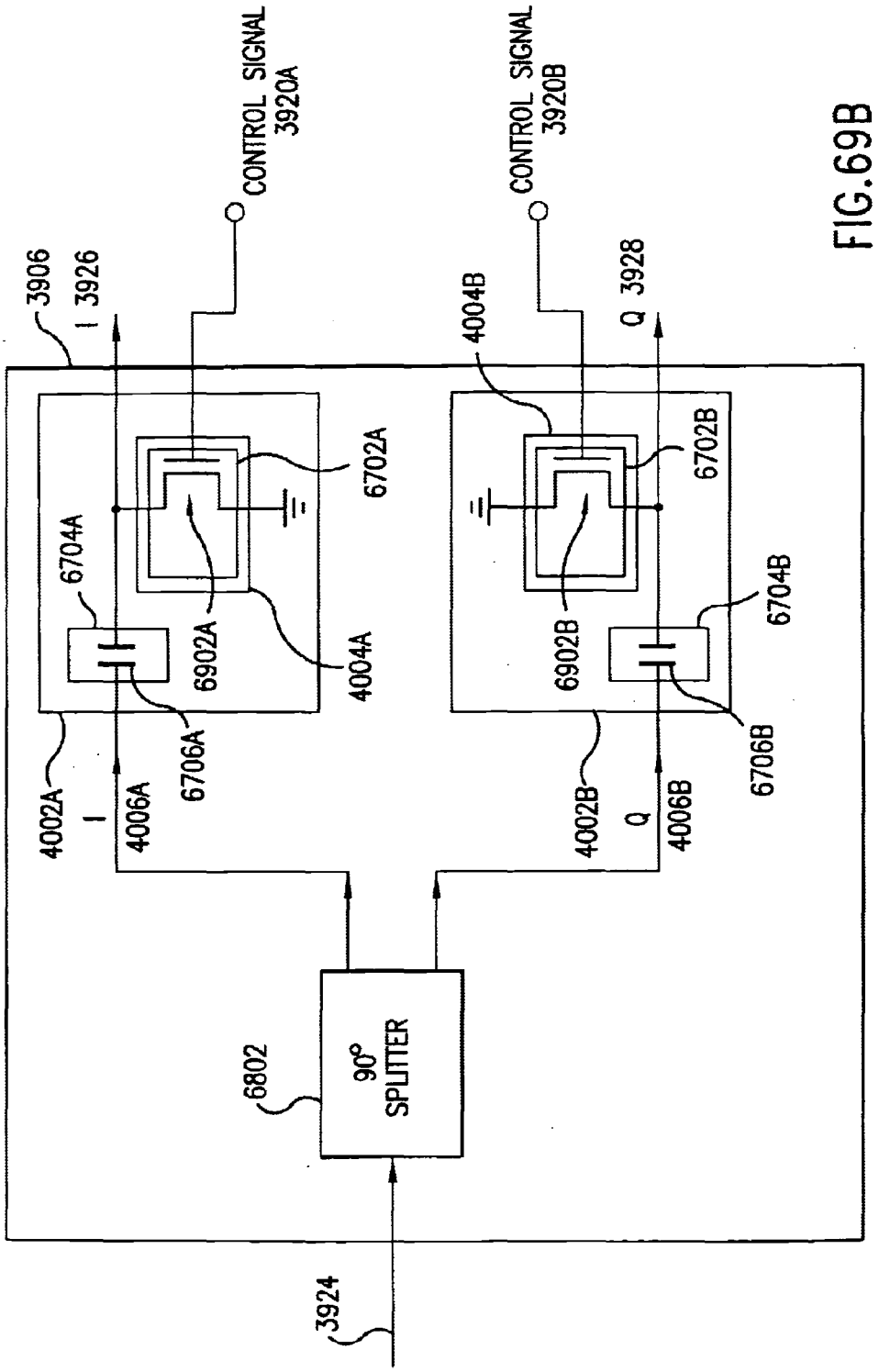

CONTROL SIGNAL 3920A
CONTROL SIGNAL 3920B
3906
I 3926
Q 3928
4004B
6702A
6702B
6704A
6704B
6902A
6902B
4004A
6706A
6706B
4002A
I
4006A
4002B
Q
4006B
6802
90° SPLITTER
3924

FIG.69B

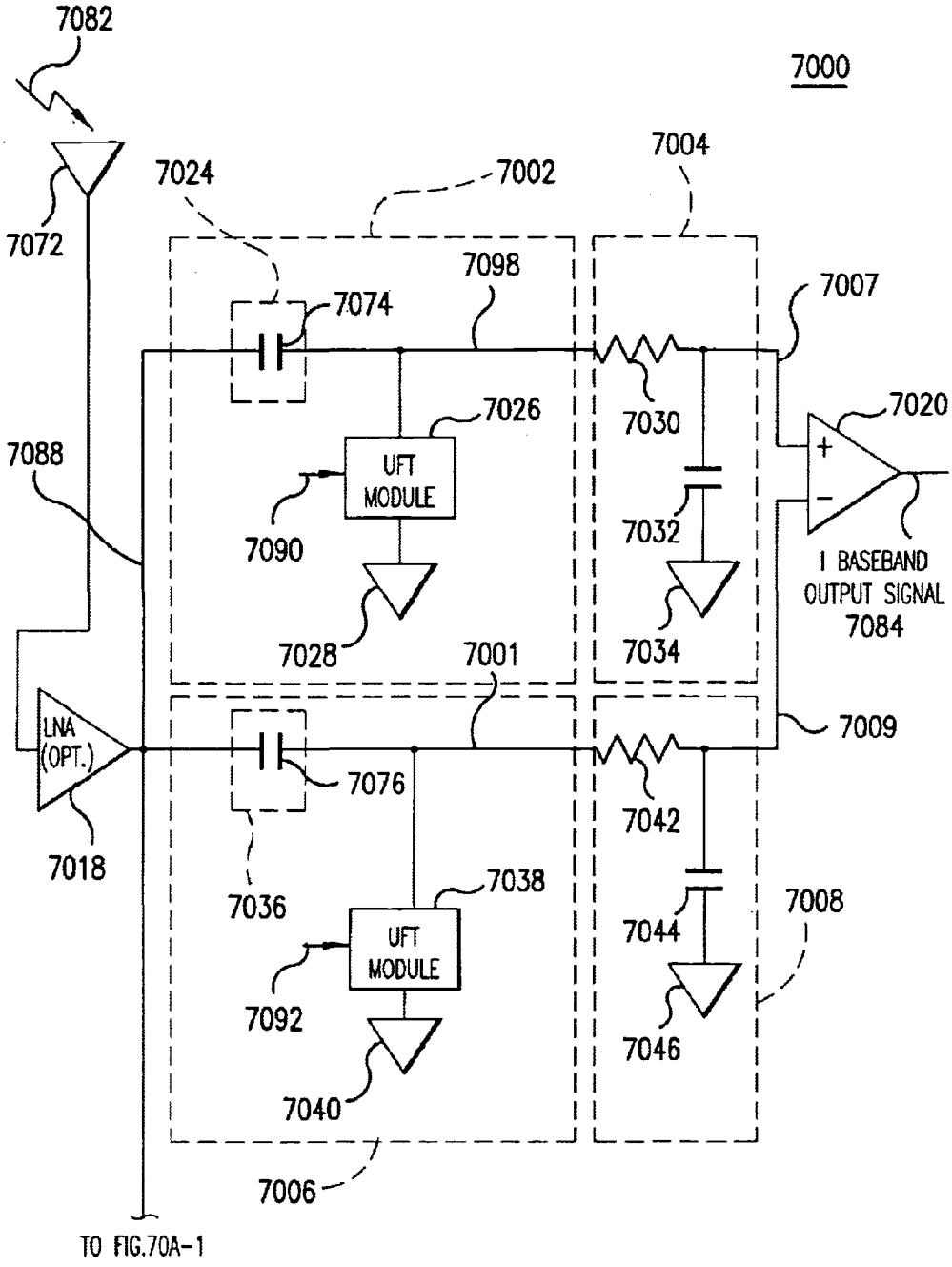

7082
7000
7004
7024
7002
7072
7098
7007
7074
7026
7030
7020
7088
UFT MODULE
7090
7032
I BASEBAND OUTPUT SIGNAL 7084
7028
7001
7034
LNA (OPT.)
7009
7076
7042
7018
7036
7038
7008
7044
UFT MODULE
7092
7046
7040
7006
TO FIG.70A-1

FIG.70A

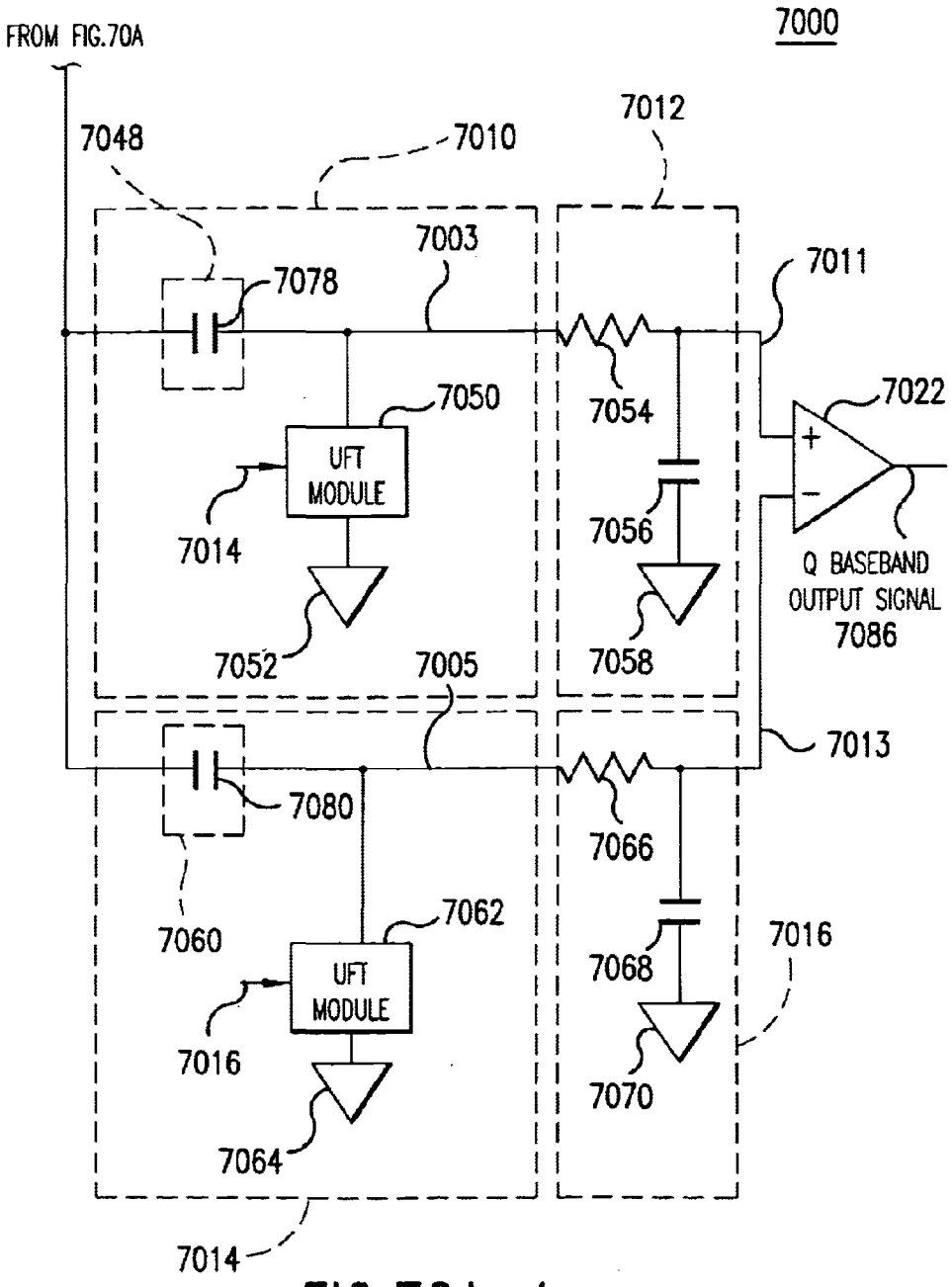

FROM FIG.70A
7000
7048
7010
7012
7003
7078
7011
7050
7054
7022
UFT MODULE
7014
7056
Q BASEBAND OUTPUT SIGNAL 7086
7052
7005
7058
7013
7080
7066
7060
7062
7016
7068
UFT MODULE
7016
7070
7064
7014

FIG.70A-1

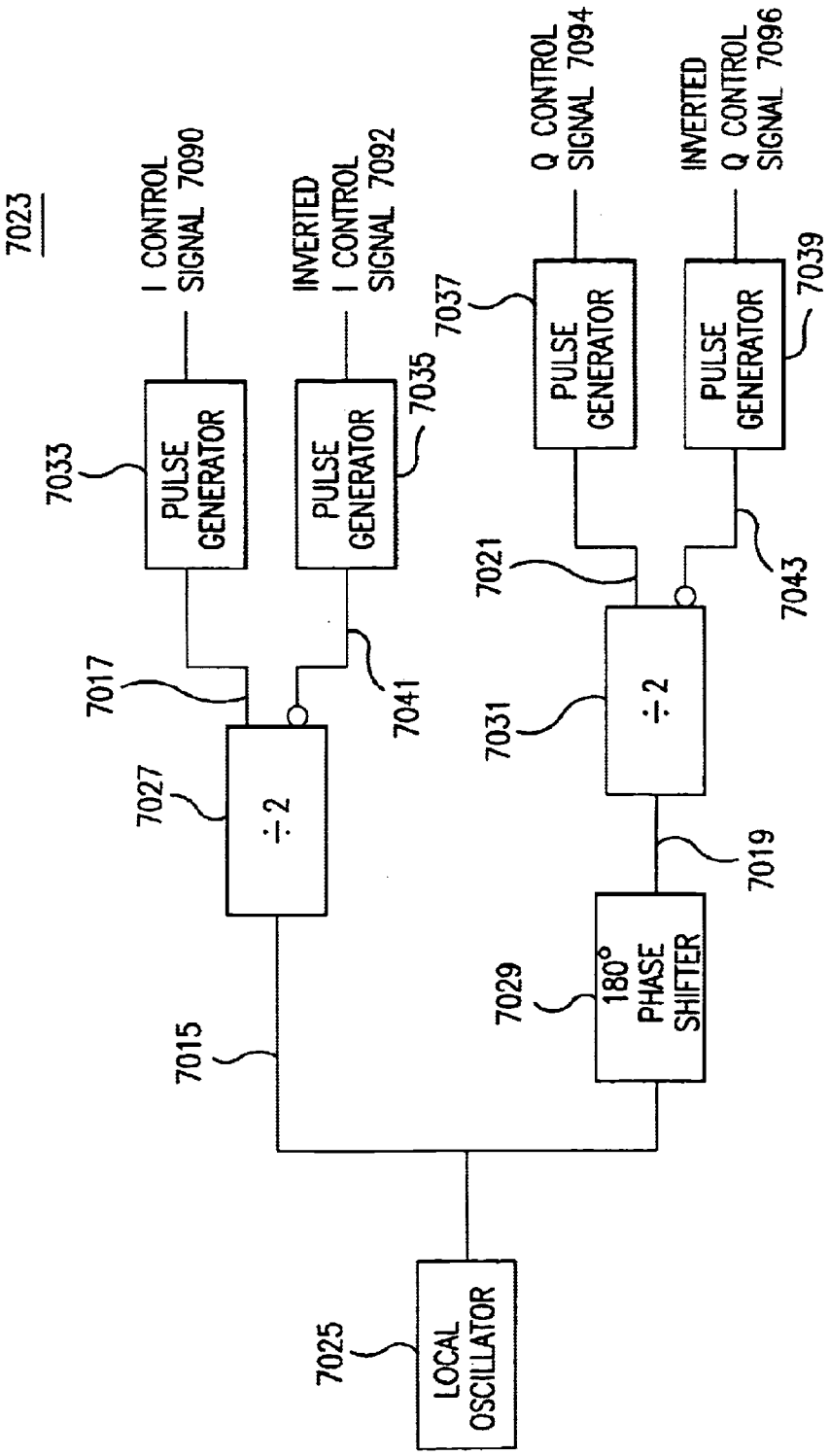

7023
I CONTROL SIGNAL 7090
INVERTED I CONTROL SIGNAL 7092
Q CONTROL SIGNAL 7094
INVERTED Q CONTROL SIGNAL 7096
7033
PULSE GENERATOR
7035
PULSE GENERATOR
7037
PULSE GENERATOR
7039
PULSE GENERATOR
7017
7041
7021
7043
÷ 2
7027
÷ 2
7031
7019
7029
180° PHASE SHIFTER
7015
7025
LOCAL OSCILLATOR

FIG.70B

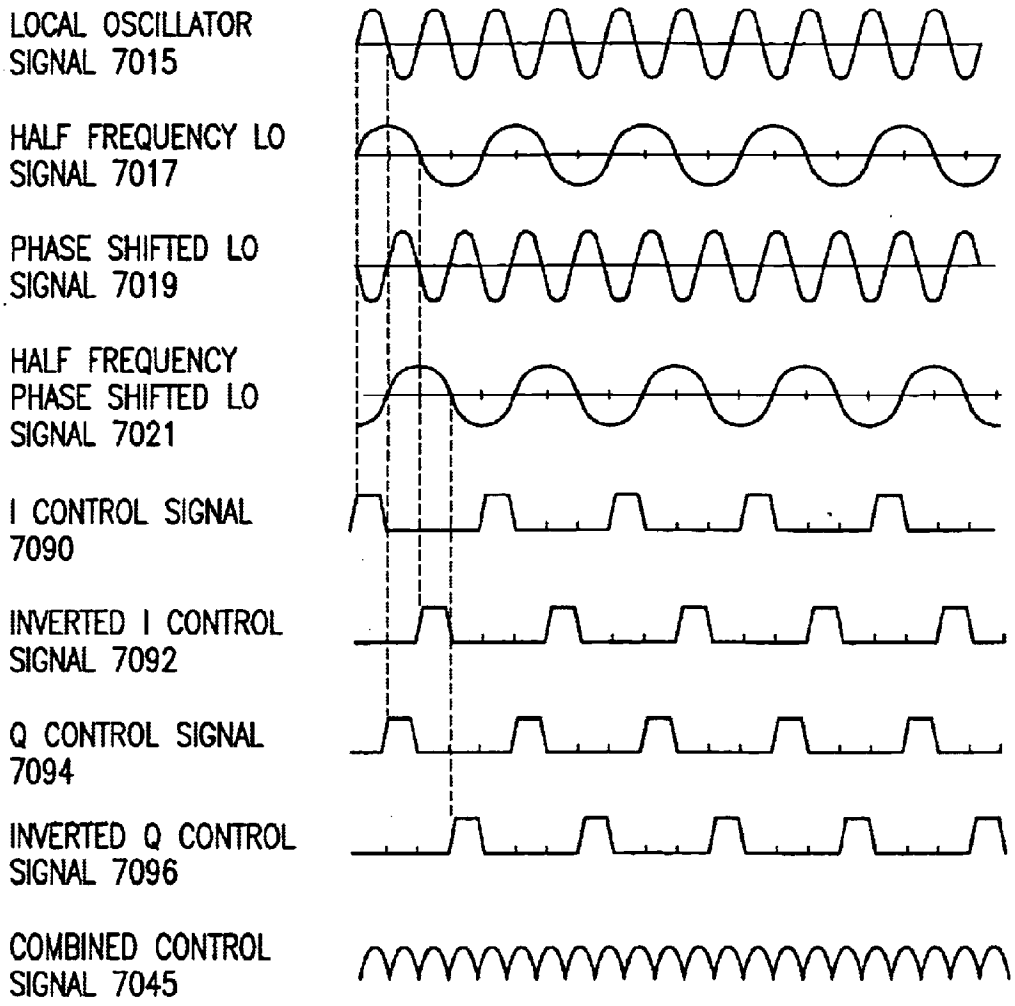

LOCAL OSCILLATOR SIGNAL 7015
HALF FREQUENCY LO SIGNAL 7017
PHASE SHIFTED LO SIGNAL 7019
HALF FREQUENCY PHASE SHIFTED LO SIGNAL 7021
I CONTROL SIGNAL 7090
INVERTED I CONTROL SIGNAL 7092
Q CONTROL SIGNAL 7094
INVERTED Q CONTROL SIGNAL 7096
COMBINED CONTROL SIGNAL 7045

FIG.70C

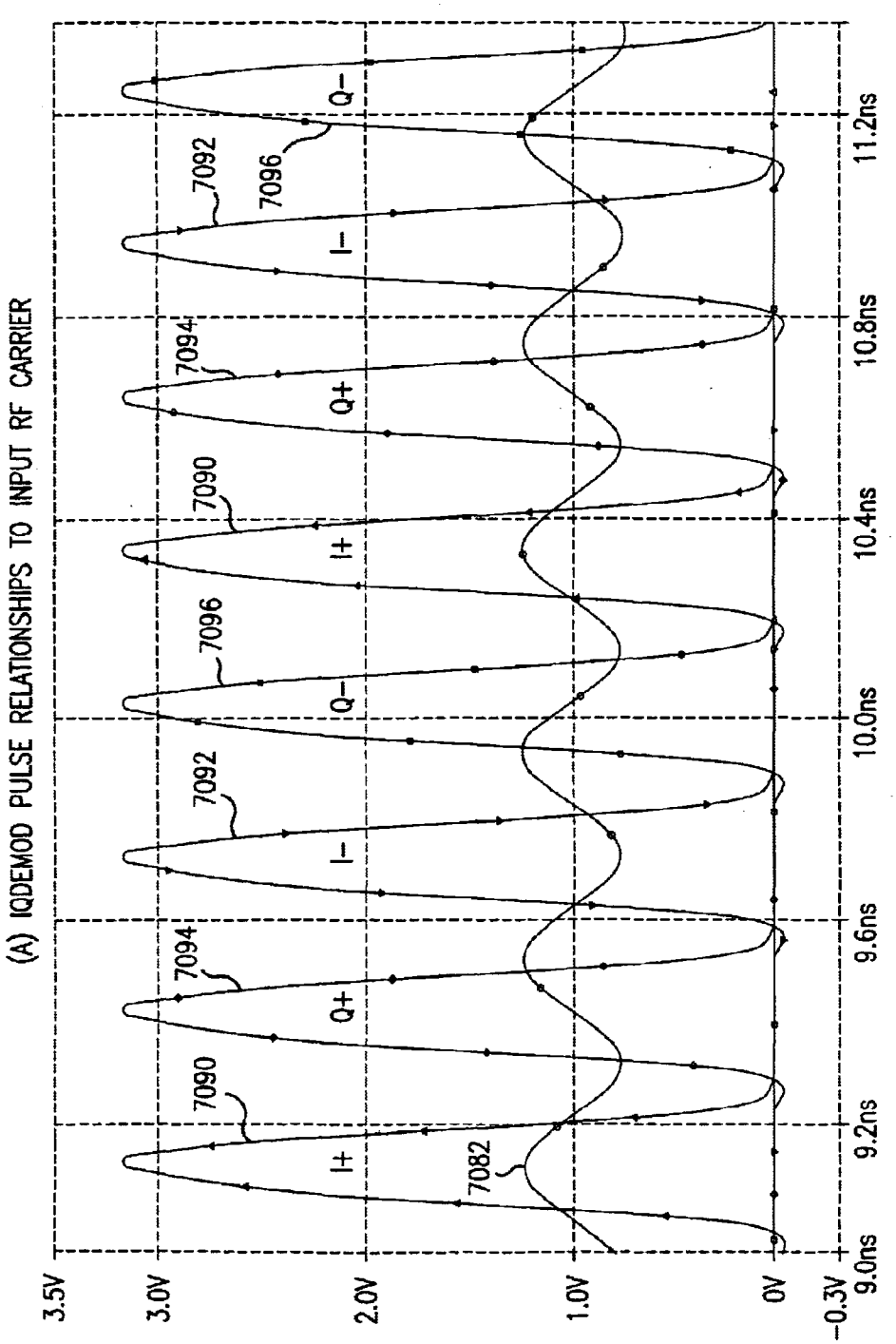

(A) IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER
3.5V
3.0V
2.0V
1.0V
0V
-0.3V
9.0ns
9.2ns
9.6ns
10.0ns
10.4ns
10.8ns
11.2ns
7082
7090
I+
7094
Q+
7092
I-
7096
Q-

FIG.70D

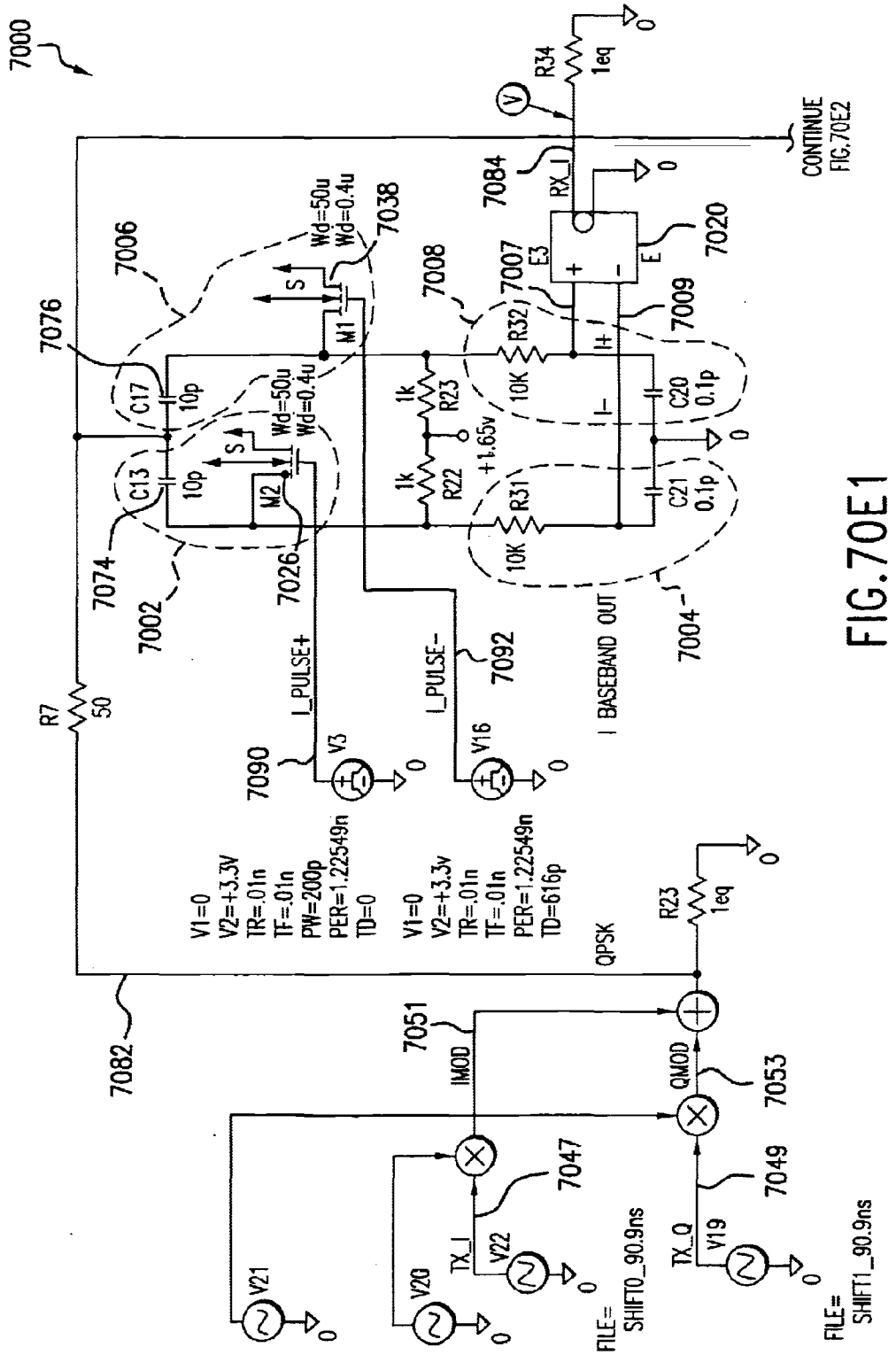

7000
R34
1eq
CONTINUE
FIG.70E2
7084
RX_I
7020
7007
E3
7008
7009
R32
10K
C20
0.1p
I+
I-
7006
7038
Wd=50u
Wd=0.4u
M1
S
7076
C17
10p
1k
R23
+1.65v
1k
R22
10K
R31
C21
0.1p
C13
10p
M2
7074
7002
7026
7004
I BASEBAND OUT
R7
50
I_PULSE+
I_PULSE-
7092
7090
V3
V16
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=0
V1=0
V2=+3.3v
TR=.01n
TF=.01n
PER=1.22549n
TD=616p
QPSK
R23
1eq
7082
7051
IMOD
QMOD
7053
7047
7049
TX_I
TX_Q
V22
V19
V20
V21
FILE=
SHIFT0_90.9ns
FILE=
SHIFT1_90.9ns

FIG.70E1

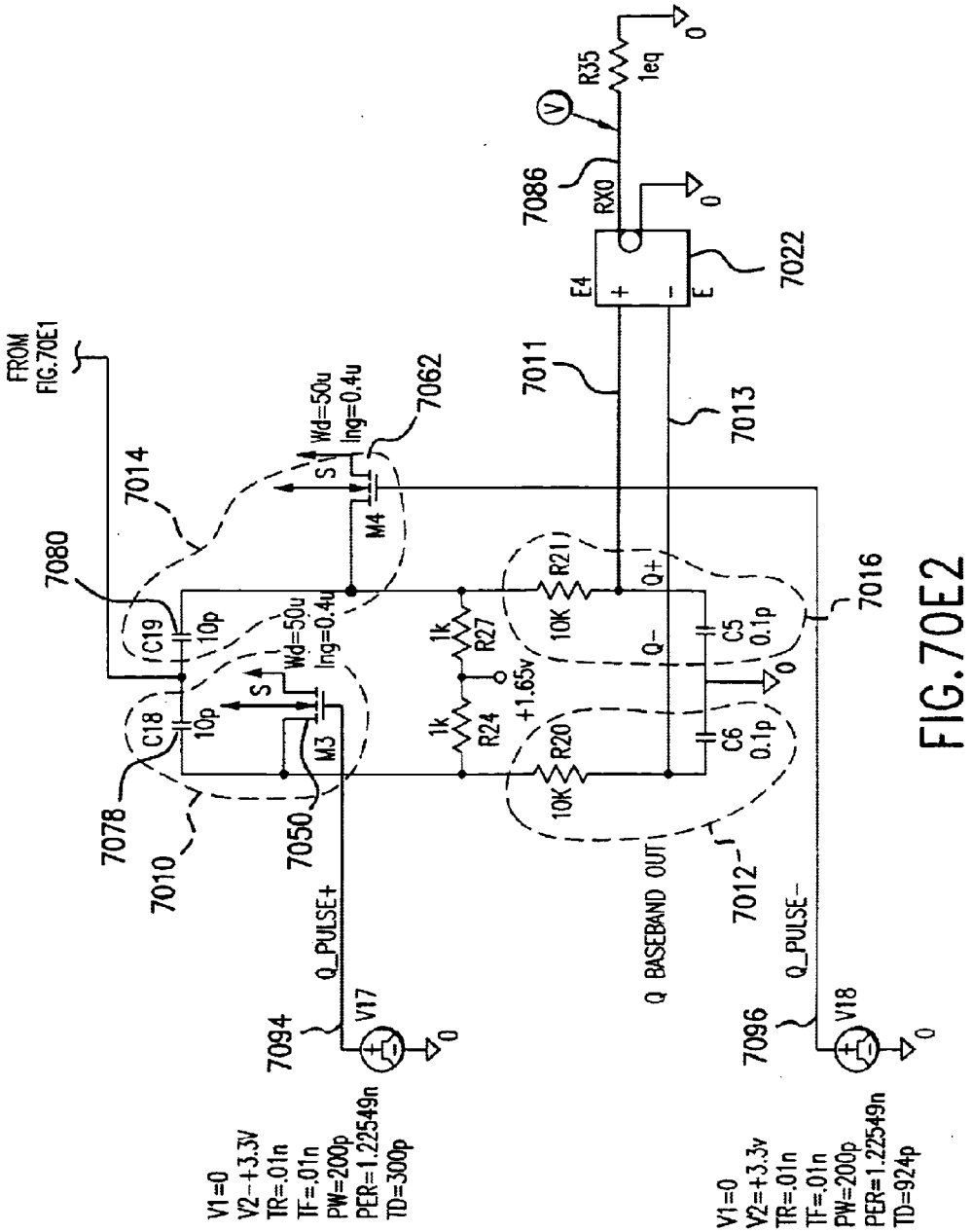

FROM FIG.70E1
7080
7014
7062
Wd=50u
lng=0.4u
M4
7011
7013
7086
RX0
R35
1eq
E4
7022
7016
C19
10p
C18
10p
M3
R21
10K
R27
1k
R24
1k
R20
10K
+1.65v
C5
0.1p
C6
0.1p
Q+
Q-
7078
7010
7050
7012
Q BASEBAND OUT
Q_PULSE+
Q_PULSE-
7094
7096
V17
V18
V1=0
V2=+3.3v
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=300p
TD=924p

FIG.70E2

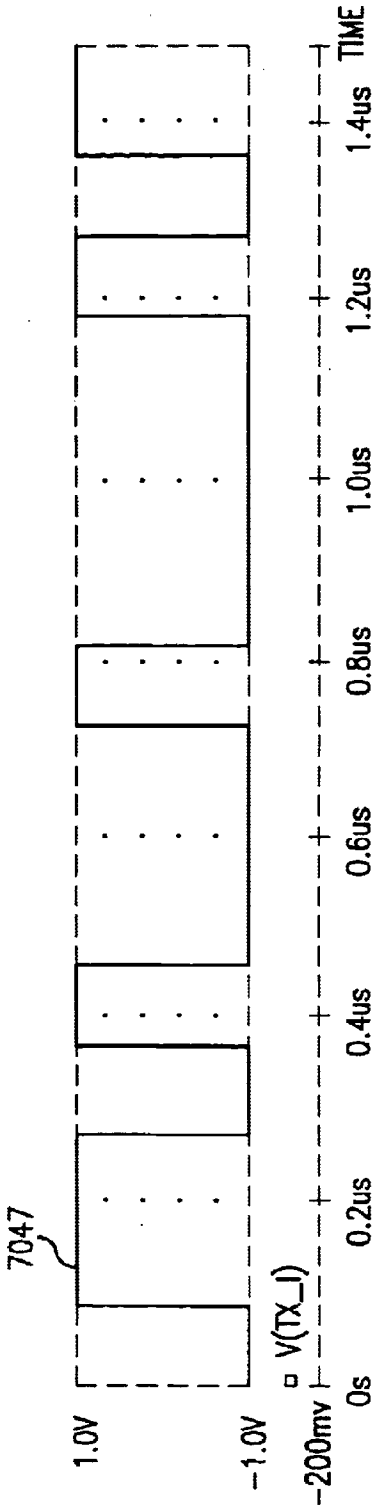


FIG.70F

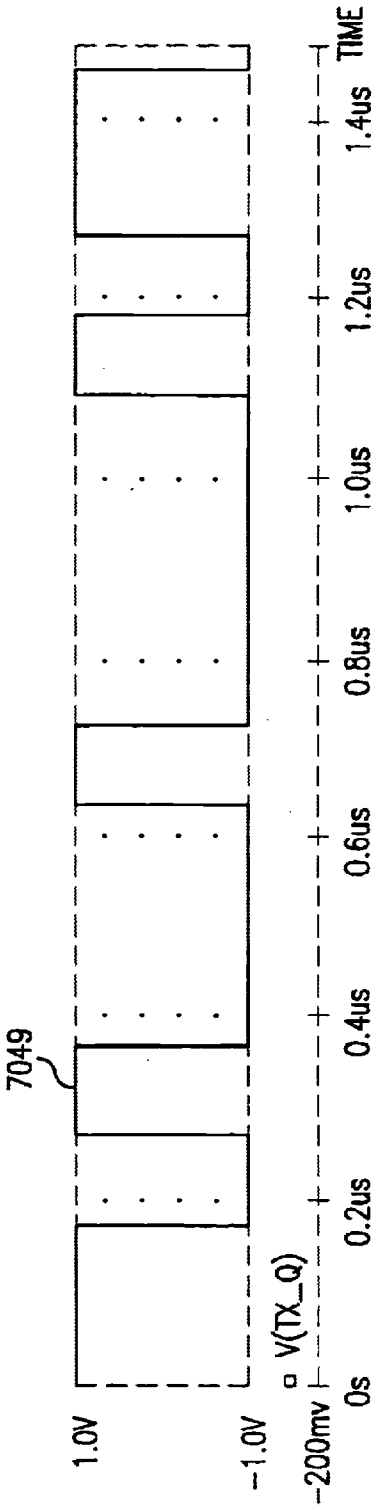


FIG.70G

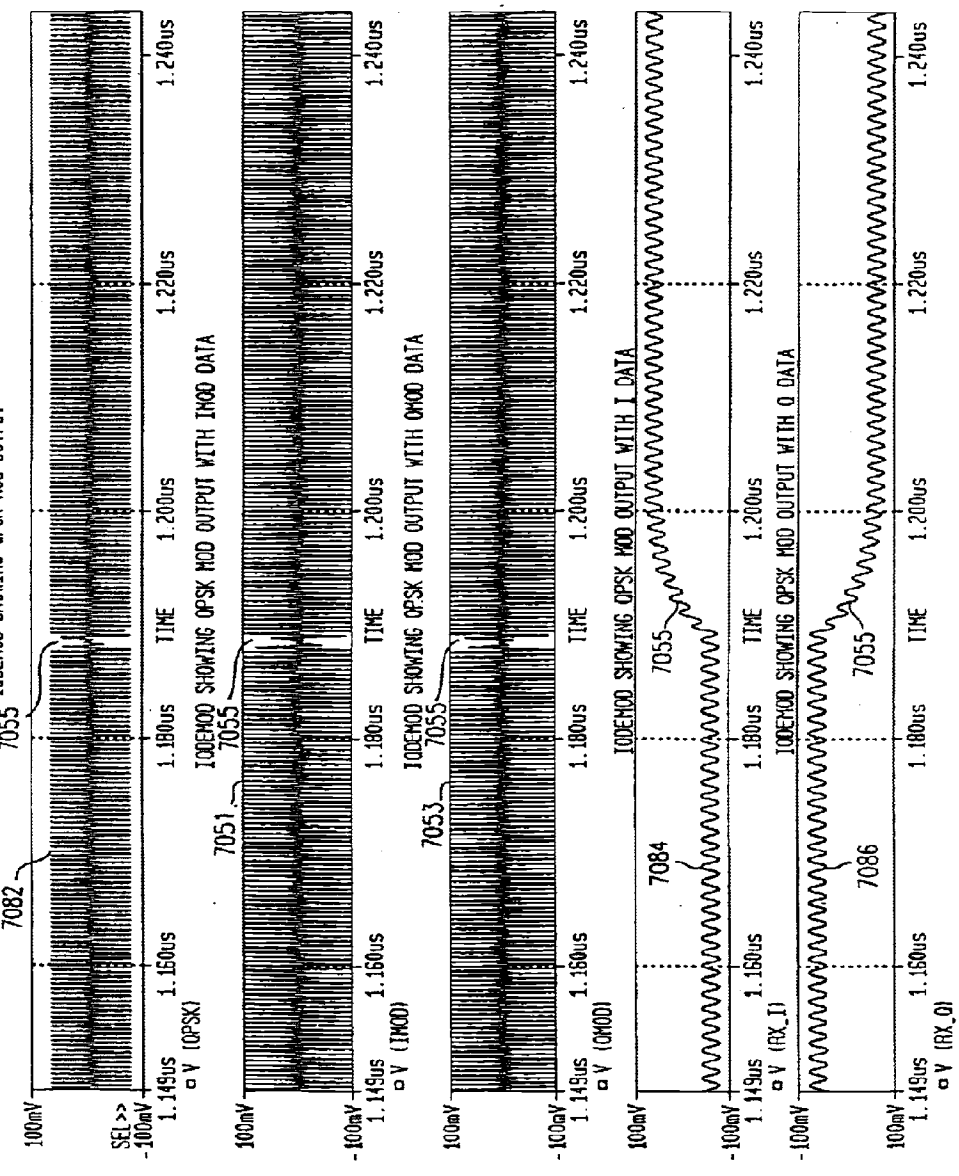


FIG. 70H

FIG. 70I

FIG. 70J

FIG. 70K

FIG. 70L

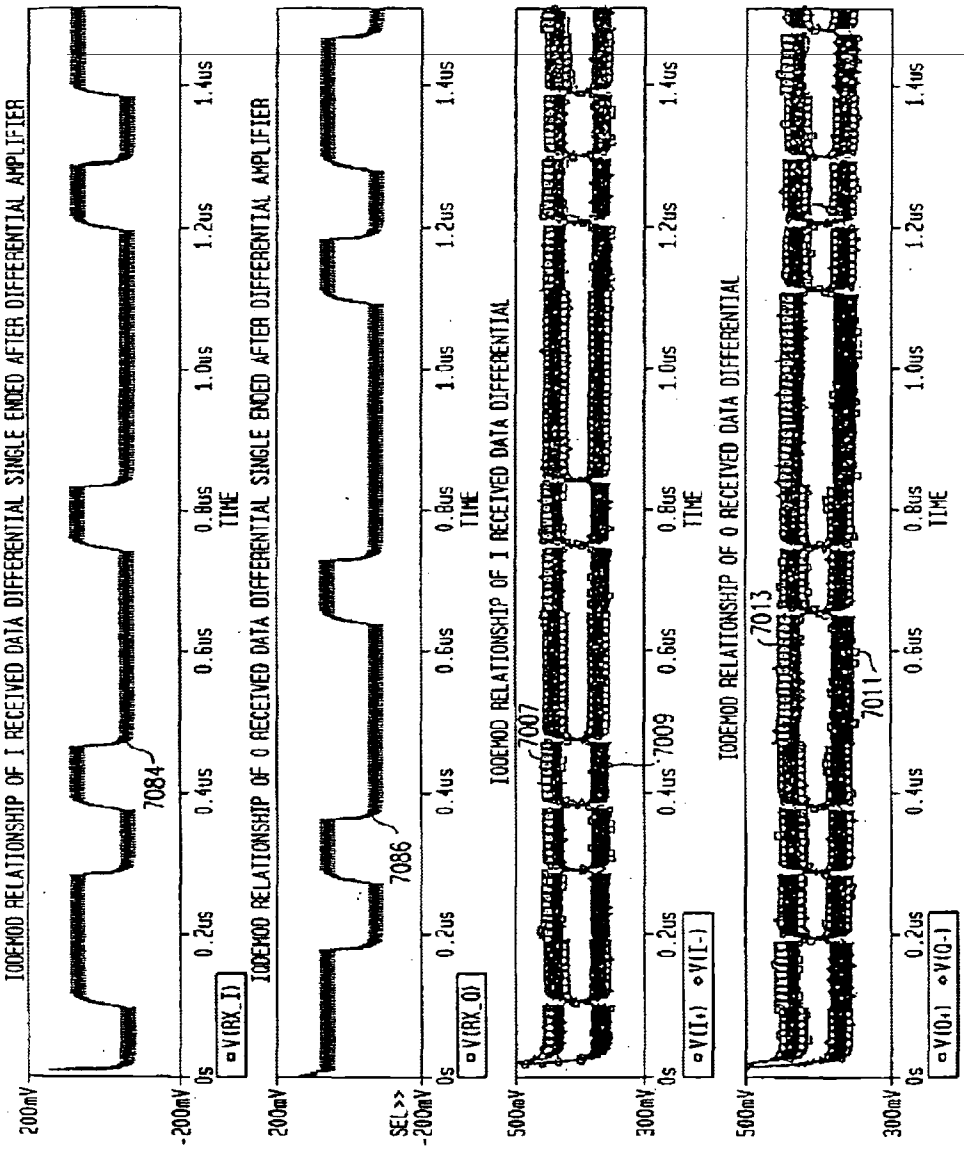


FIG. 70M

FIG. 70N

FIG. 70O

FIG. 70P

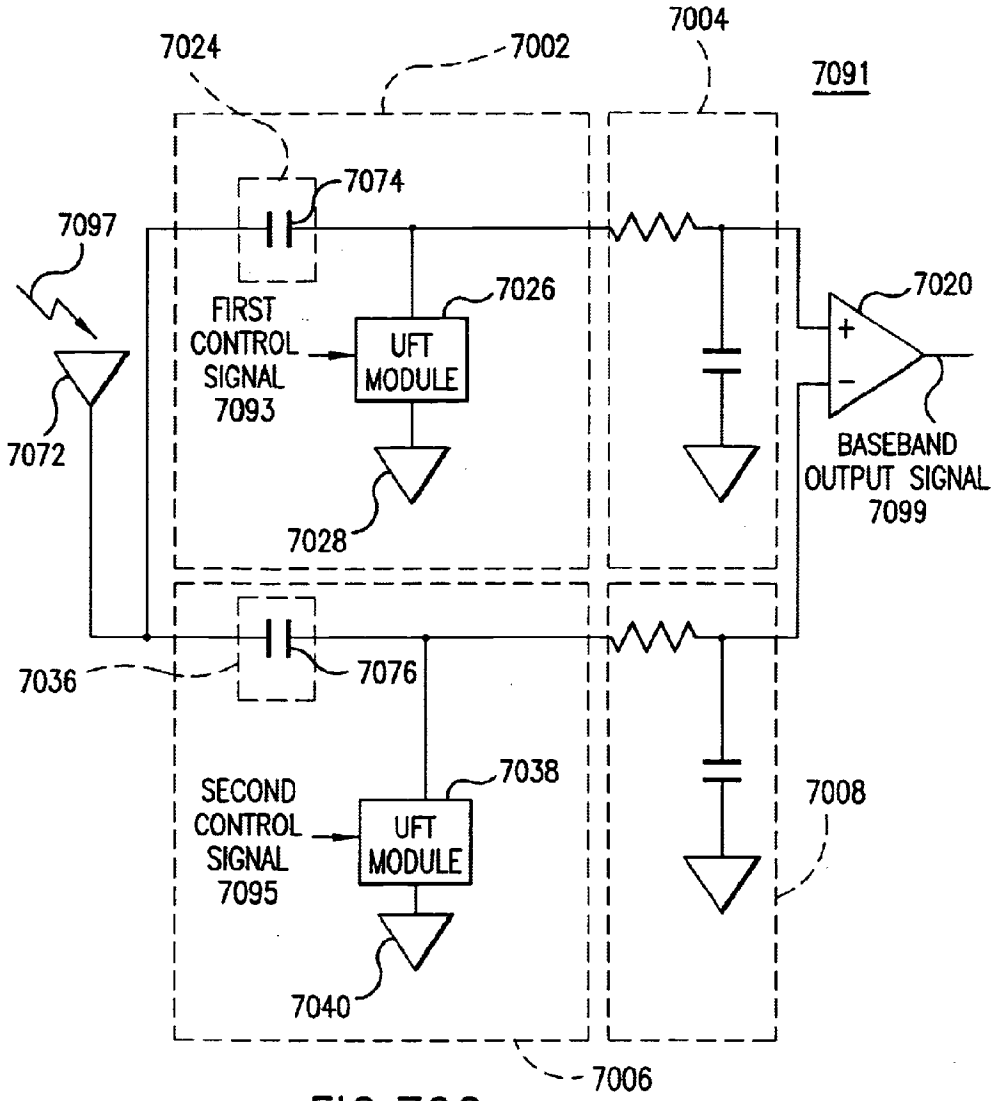

7024
7002
7004
7091
7074
7097
7026
FIRST CONTROL SIGNAL 7093
UFT MODULE
7020
7072
7028
BASEBAND OUTPUT SIGNAL 7099
7036
7076
7038
SECOND CONTROL SIGNAL 7095
UFT MODULE
7008
7040
7006

FIG.70Q

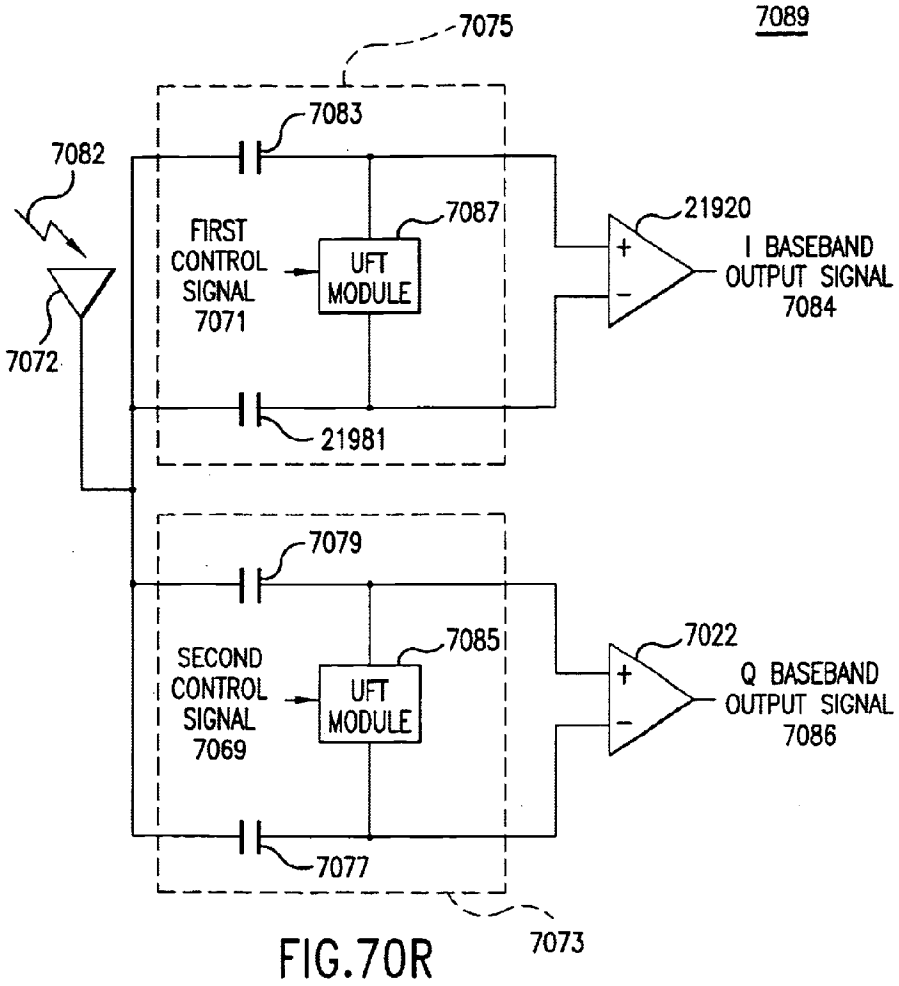

7089
7075
7083
7082
7087
21920
FIRST CONTROL SIGNAL 7071
UFT MODULE
I BASEBAND OUTPUT SIGNAL 7084
7072
21981
7079
7085
7022
SECOND CONTROL SIGNAL 7069
UFT MODULE
Q BASEBAND OUTPUT SIGNAL 7086
7077
7073

FIG.70R

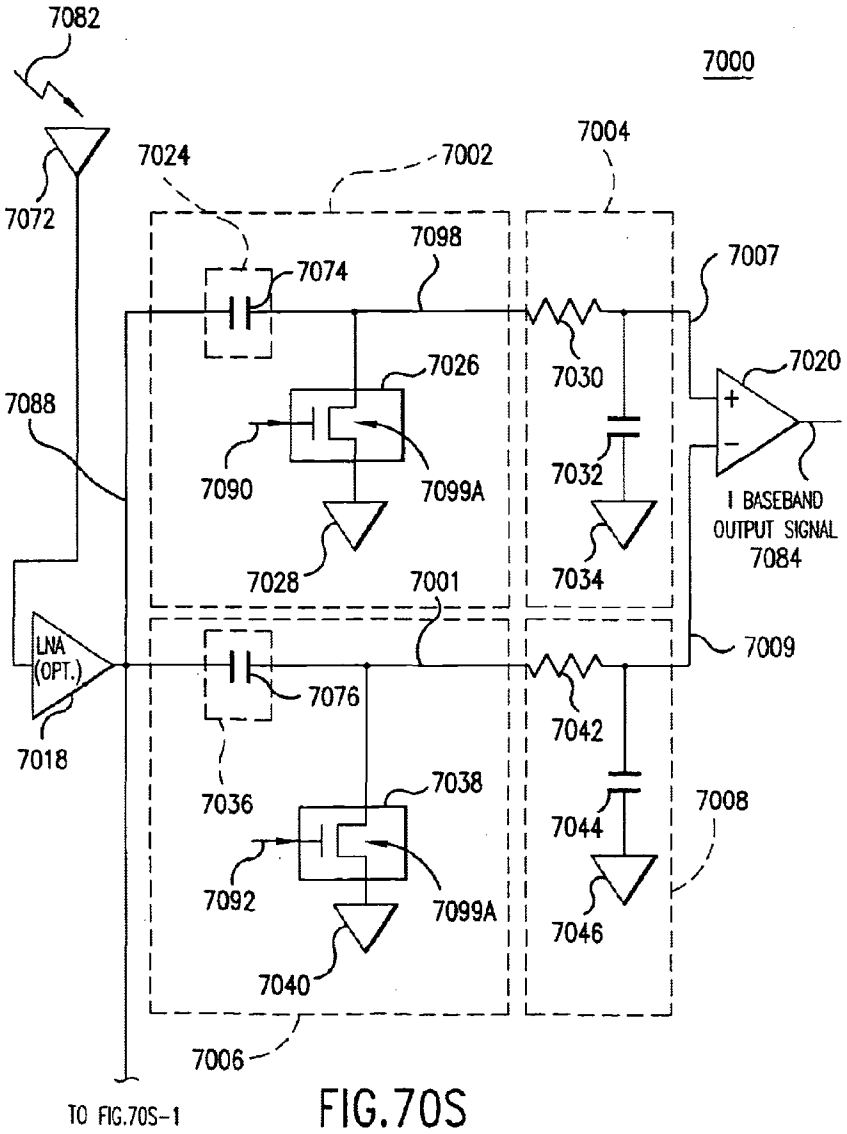

7082
7000
7004
7024
7002
7072
7098
7007
7074
7026
7030
7020
7088
7090
7099A
7032
I BASEBAND
OUTPUT SIGNAL
7084
7028
7001
7034
LNA
(OPT.)
7009
7076
7042
7018
7036
7038
7008
7044
7092
7099A
7046
7040
7006
TO FIG.70S-1

FIG.70S

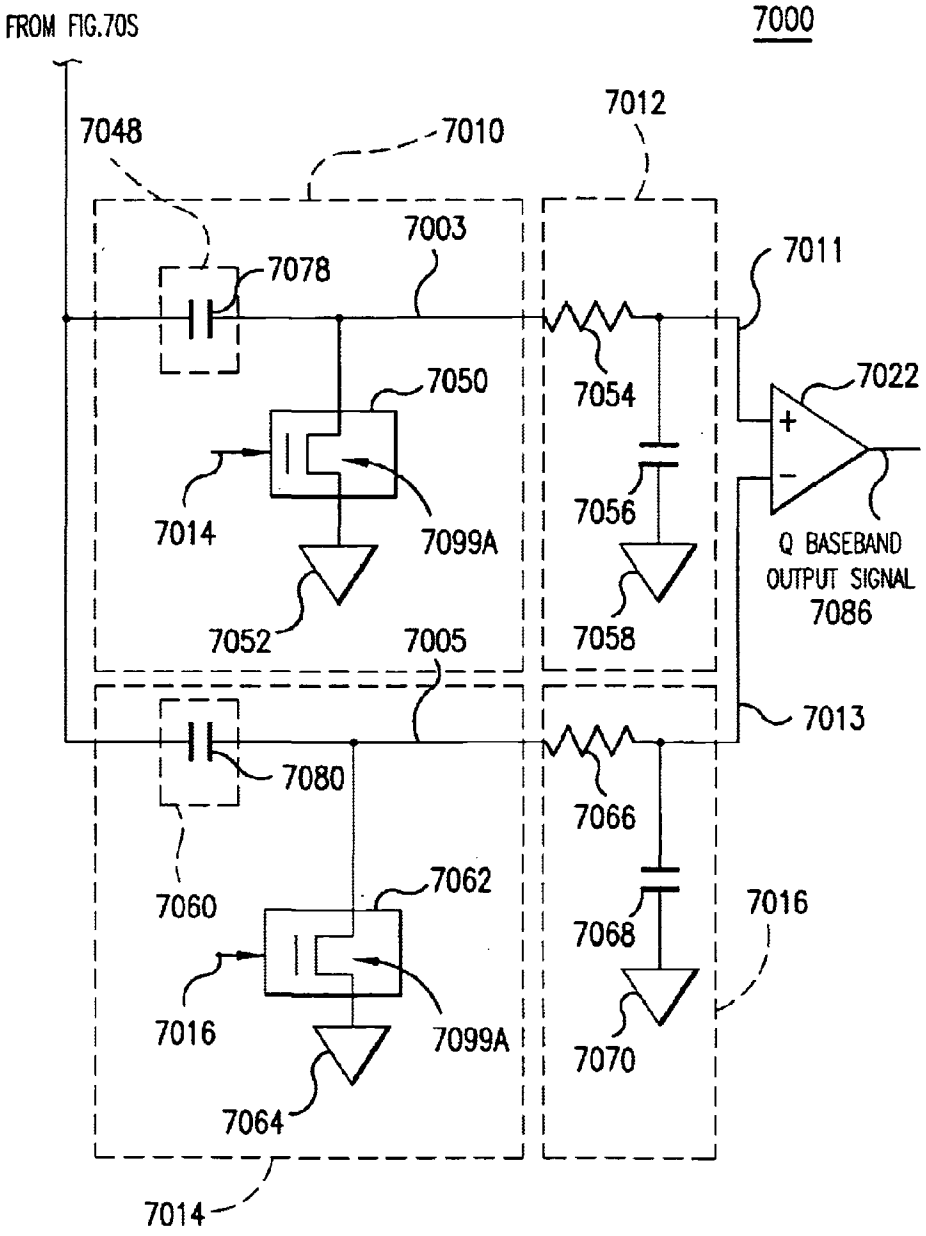

FROM FIG.70S
7000
7048
7010
7012
7003
7078
7011
7050
7054
7022
7014
7099A
7056
Q BASEBAND
OUTPUT SIGNAL
7086
7052
7005
7058
7013
7080
7066
7060
7062
7068
7016
7016
7099A
7070
7064
7014

FIG.70S-1

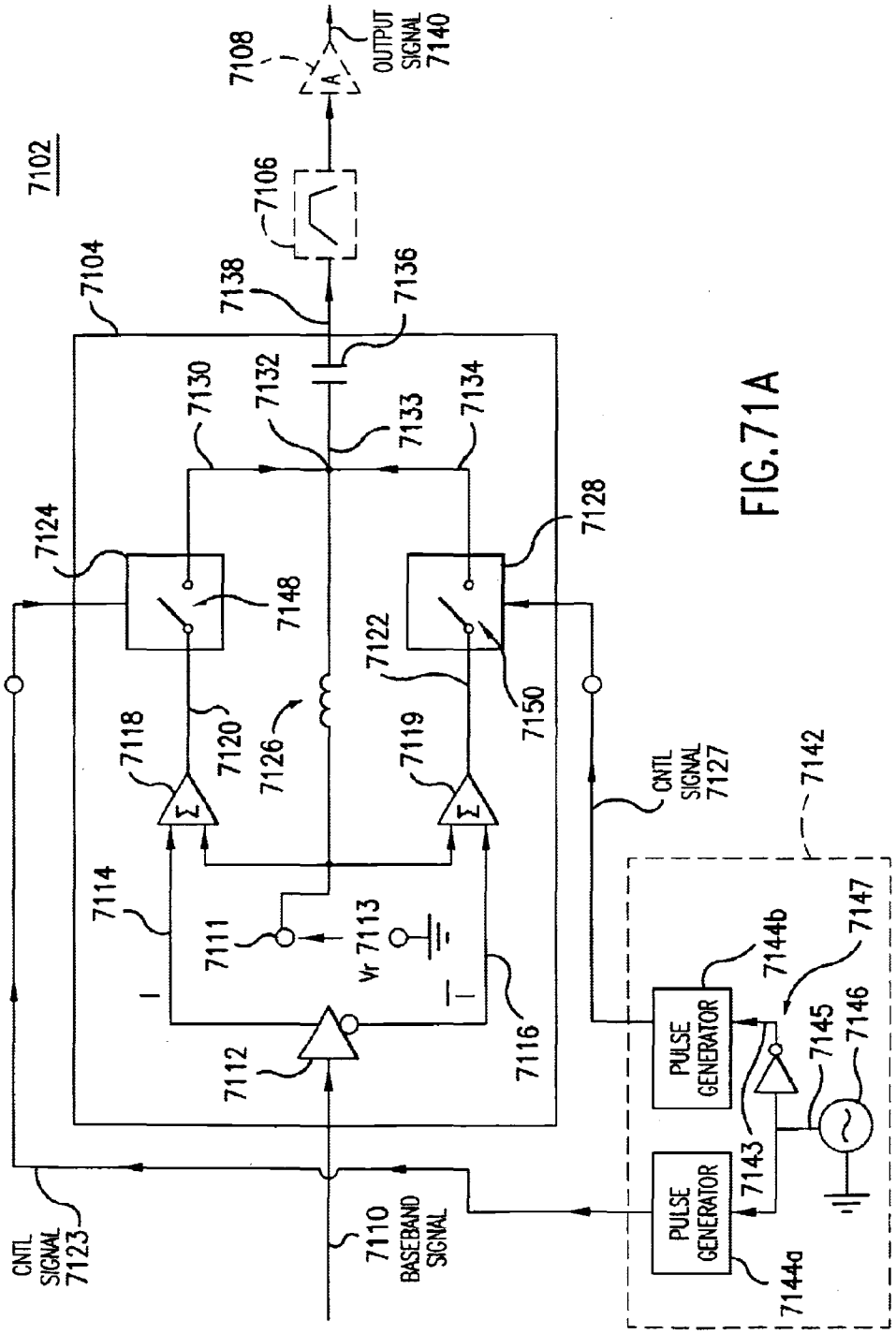

7102
7104
7106
7108
OUTPUT SIGNAL 7140
7110 BASEBAND SIGNAL
CNTL SIGNAL 7123
CNTL SIGNAL 7127
7111
7112
7113
Vr
7114
7116
7118
7119
7120
7122
7124
7126
7128
7130
7132
7133
7134
7136
7138
7142
7143
7144a
7144b
7145
7146
7147
7148
7150
PULSE GENERATOR
PULSE GENERATOR

FIG.71A

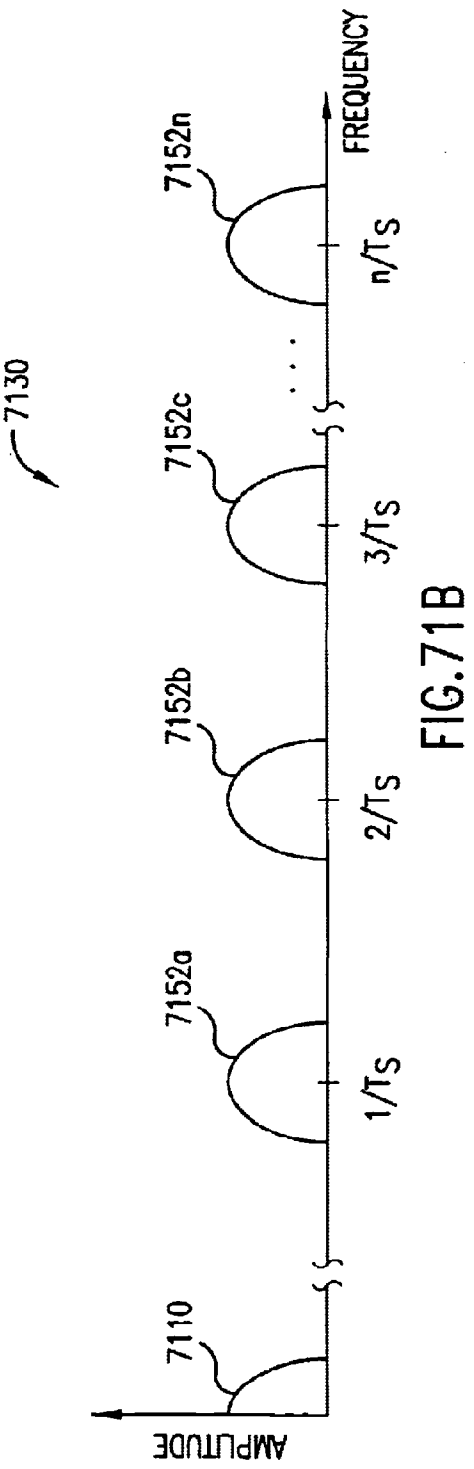


FIG.71B

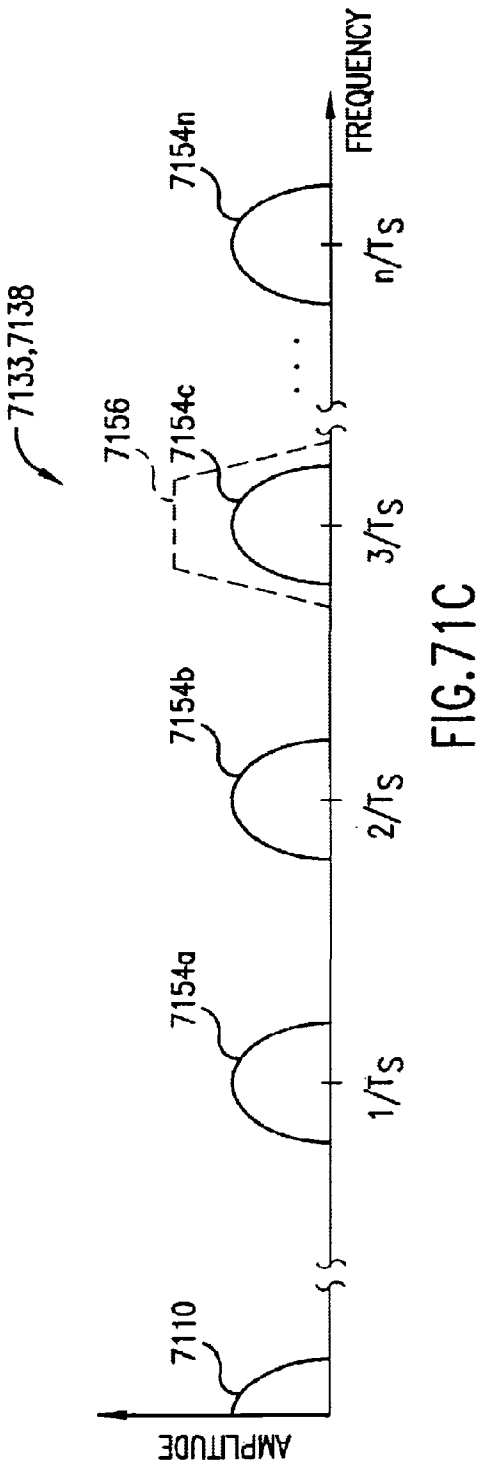


FIG.71C

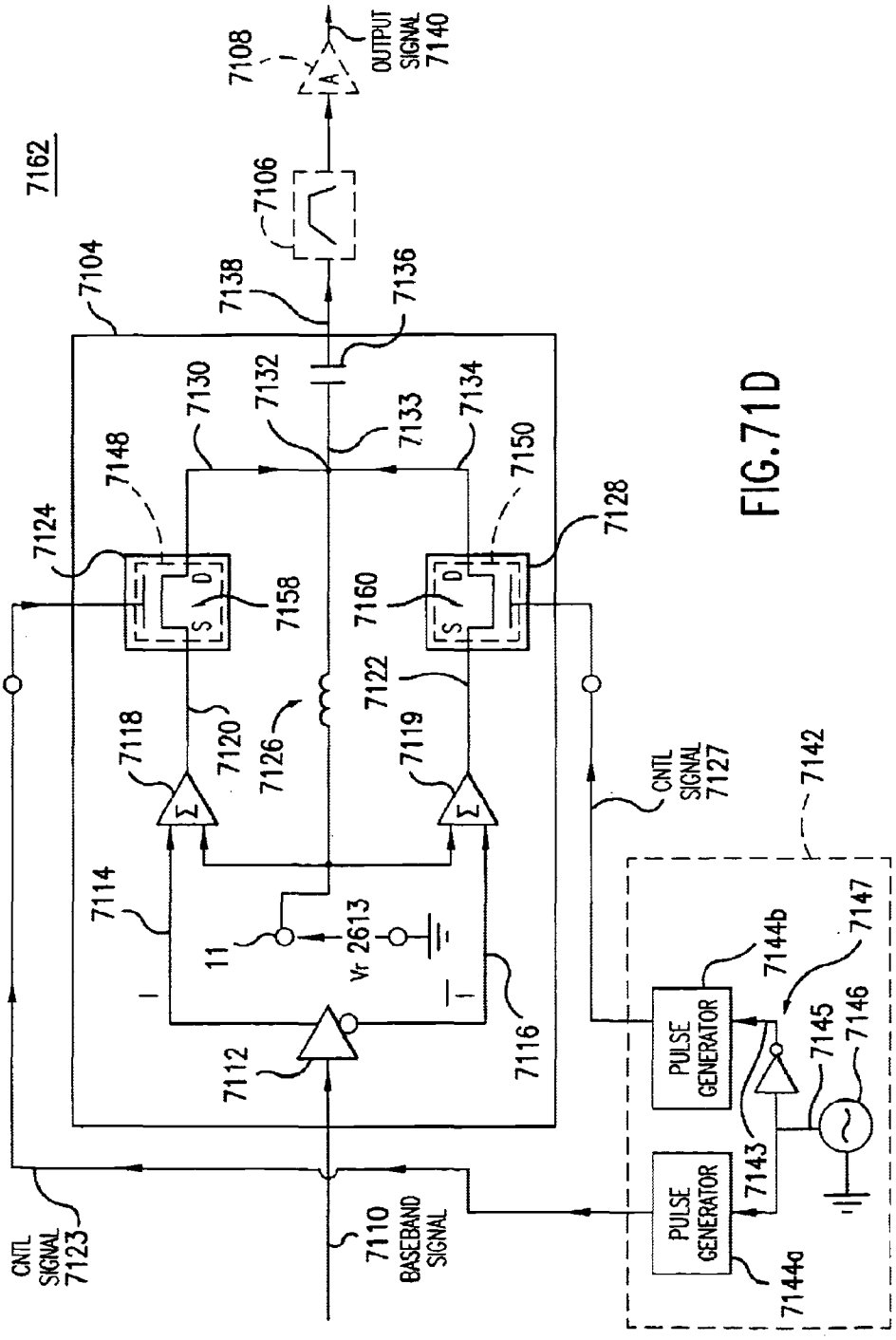

7162
7108
OUTPUT SIGNAL 7140
7106
7104
7138
7136
7130
7132
7133
7134
7148
7150
7124
7128
7158
7160
7122
7118
7120
7126
7119
CNTL SIGNAL 7127
7142
7114
11
Vr 2613
7144b
7147
7145
7146
7112
7116
PULSE GENERATOR
7143
CNTL SIGNAL 7123
7110 BASEBAND SIGNAL
7144a

FIG.71D

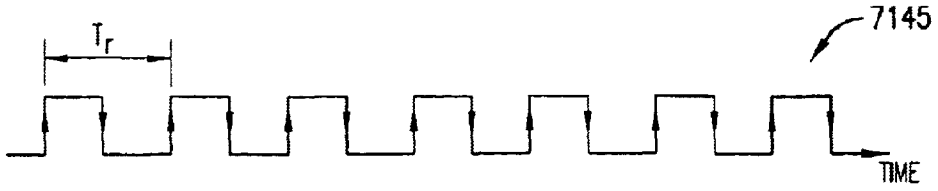


FIG.72A

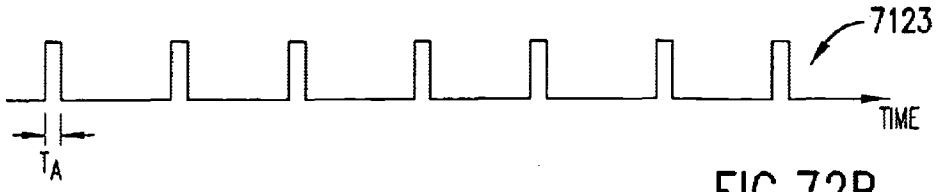


FIG.72B

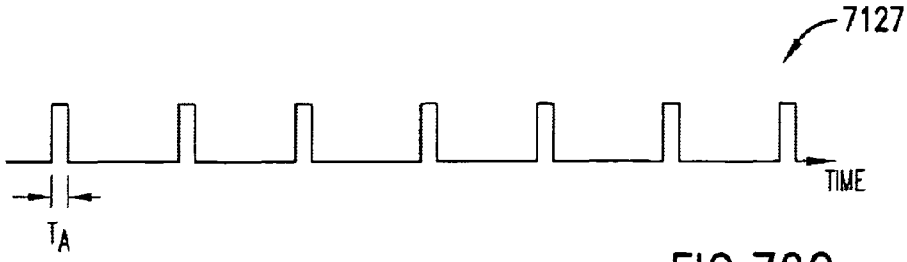


FIG.72C

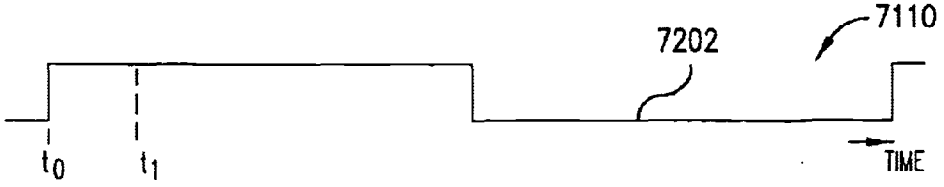


FIG.72D

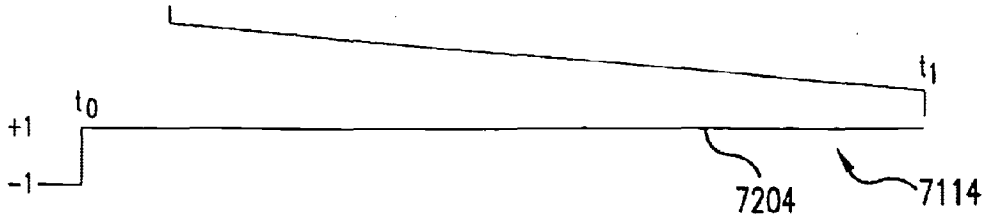


FIG.72E

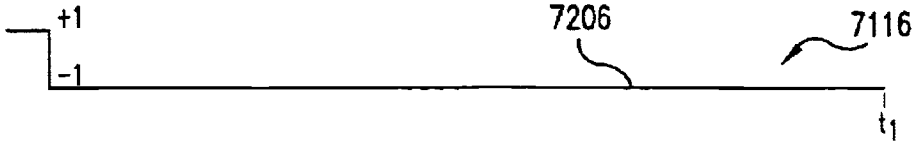


FIG.72F

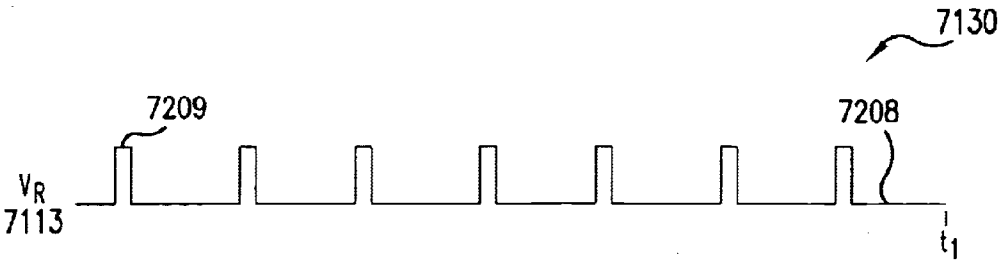


FIG.72G

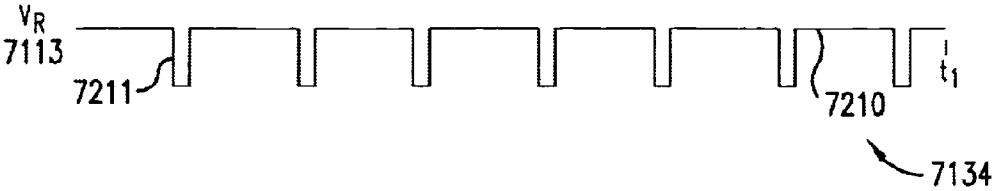


FIG.72H

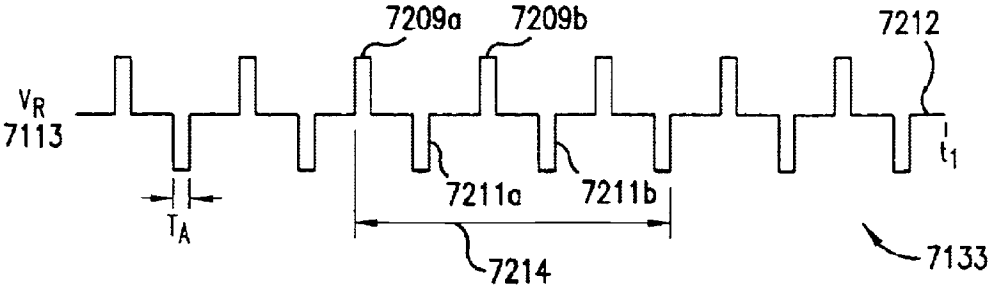


FIG.72I

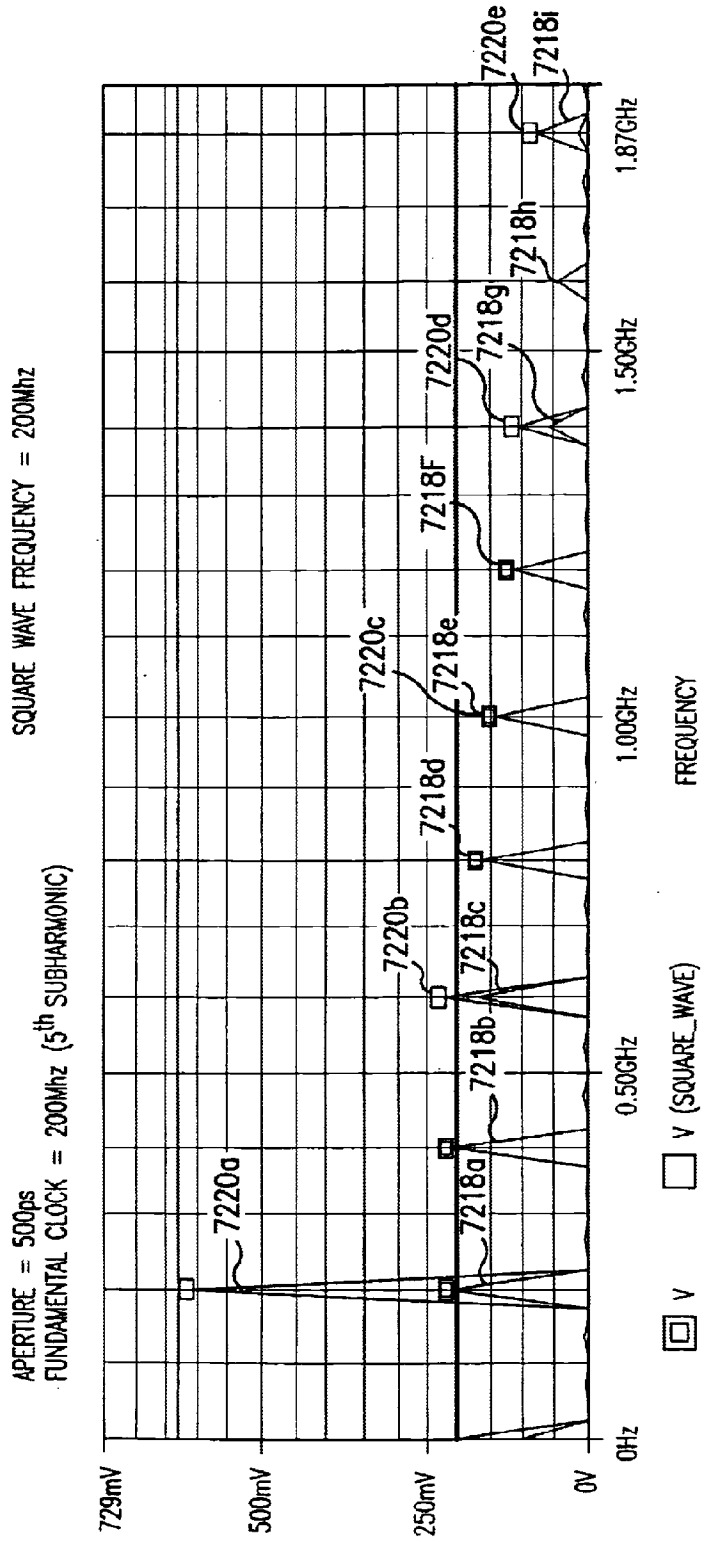

SQUARE WAVE FREQUENCY = 200Mhz
APERTURE = 500ps
FUNDAMENTAL CLOCK = 200Mhz (5th SUBHARMONIC)
729mV
500mV
250mV
0V
0Hz
0.50GHz
1.00GHz
1.50GHz
1.87GHz
FREQUENCY
V
V (SQUARE_WAVE)
7220a
7220b
7220c
7220d
7220e
7218a
7218b
7218c
7218d
7218e
7218F
7218g
7218h
7218i

FIG.72J

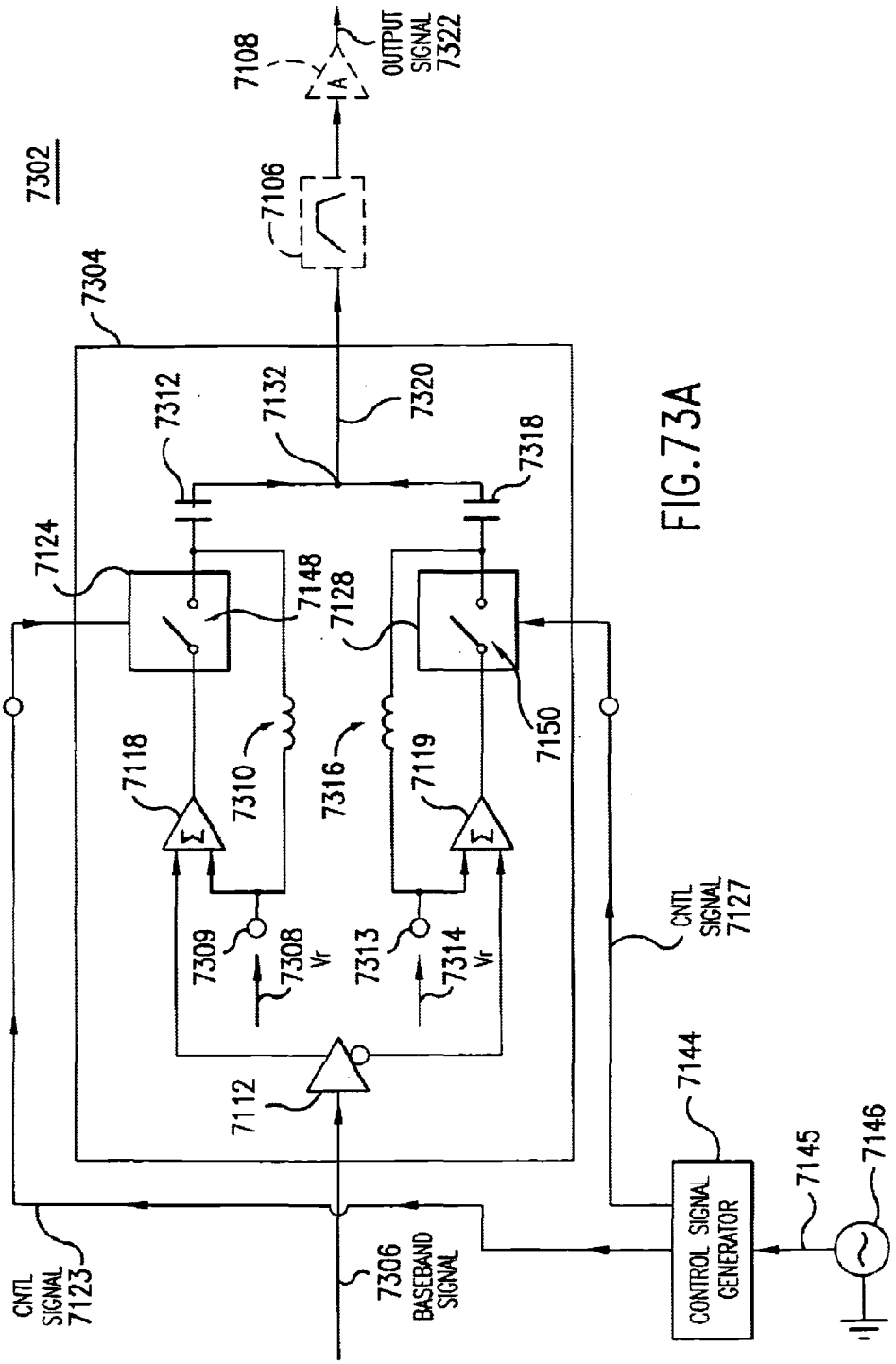

7302
7304
7108
OUTPUT SIGNAL 7322
7106
7312
7132
7320
7318
7124
7148
7128
7150
7118
7310
7316
7119
7309
7308 Vr
7313
7314 Vr
7112
CNTL SIGNAL 7127
7144
7145
7146
CONTROL SIGNAL GENERATOR
CNTL SIGNAL 7123
7306 BASEBAND SIGNAL

FIG.73A

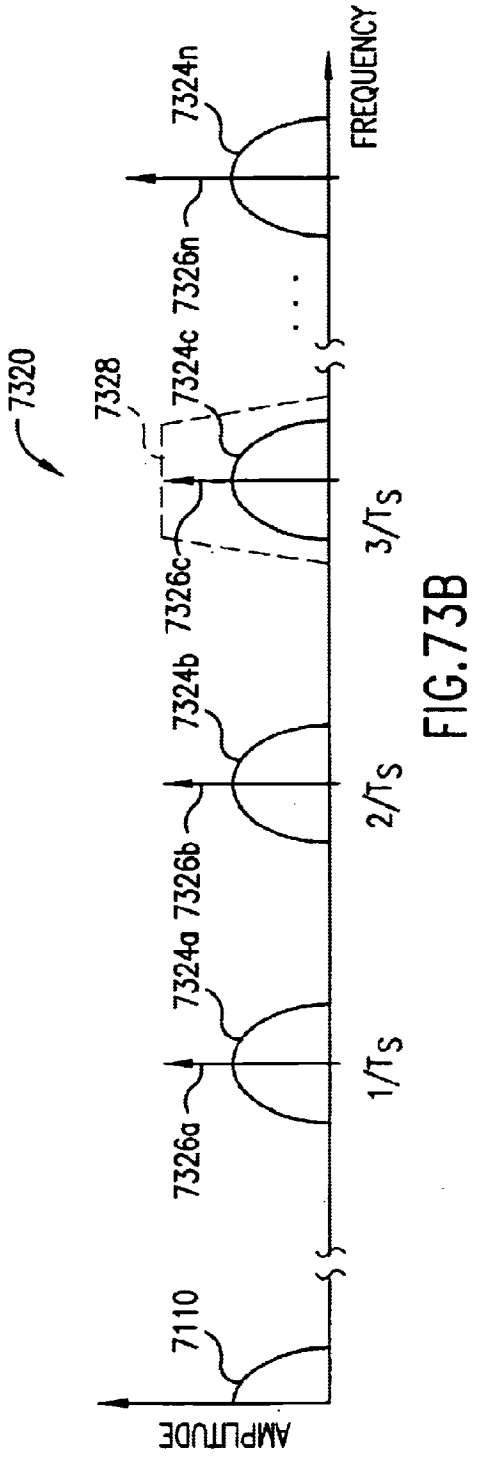

7320
7328
7324n
7326n
7324c
7326c
7324b
7326b
7324a
7326a
7110
FREQUENCY
AMPLITUDE
3/Ts
2/Ts
1/Ts

FIG.73B

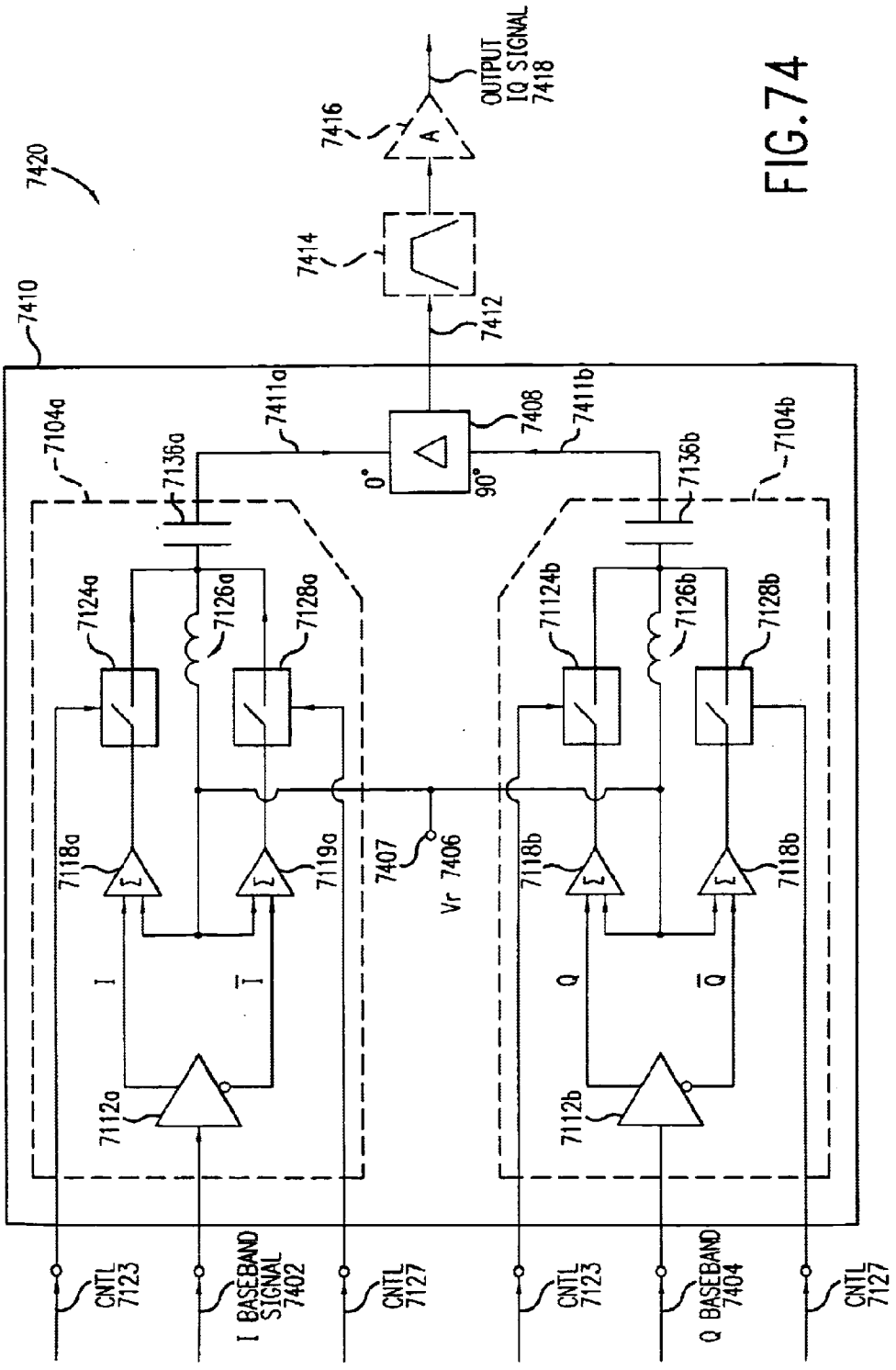

7420
7410
7416
A
OUTPUT IQ SIGNAL 7418
7414
7412
7104a
7136a
7411a
7408
7411b
7136b
7104b
0°
90°
7124a
7126a
7128a
7124b
7126b
7128b
7118a
7119a
7407
Vr 7406
7118b
I
Q
7112a
7112b
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
CNTL 7123
Q BASEBAND 7404
CNTL 7127

FIG. 74

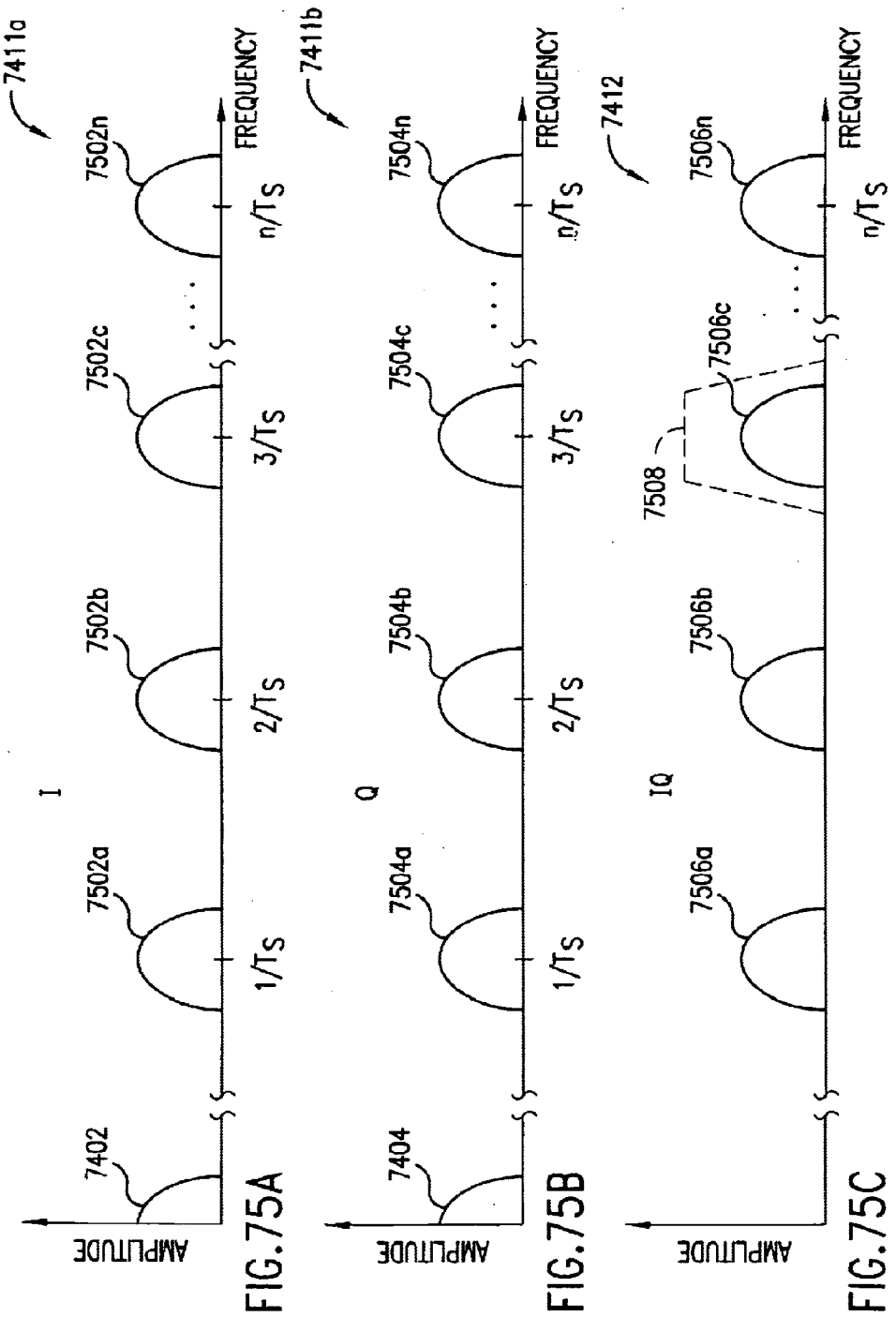


FIG.75A FIG.75B FIG.75C

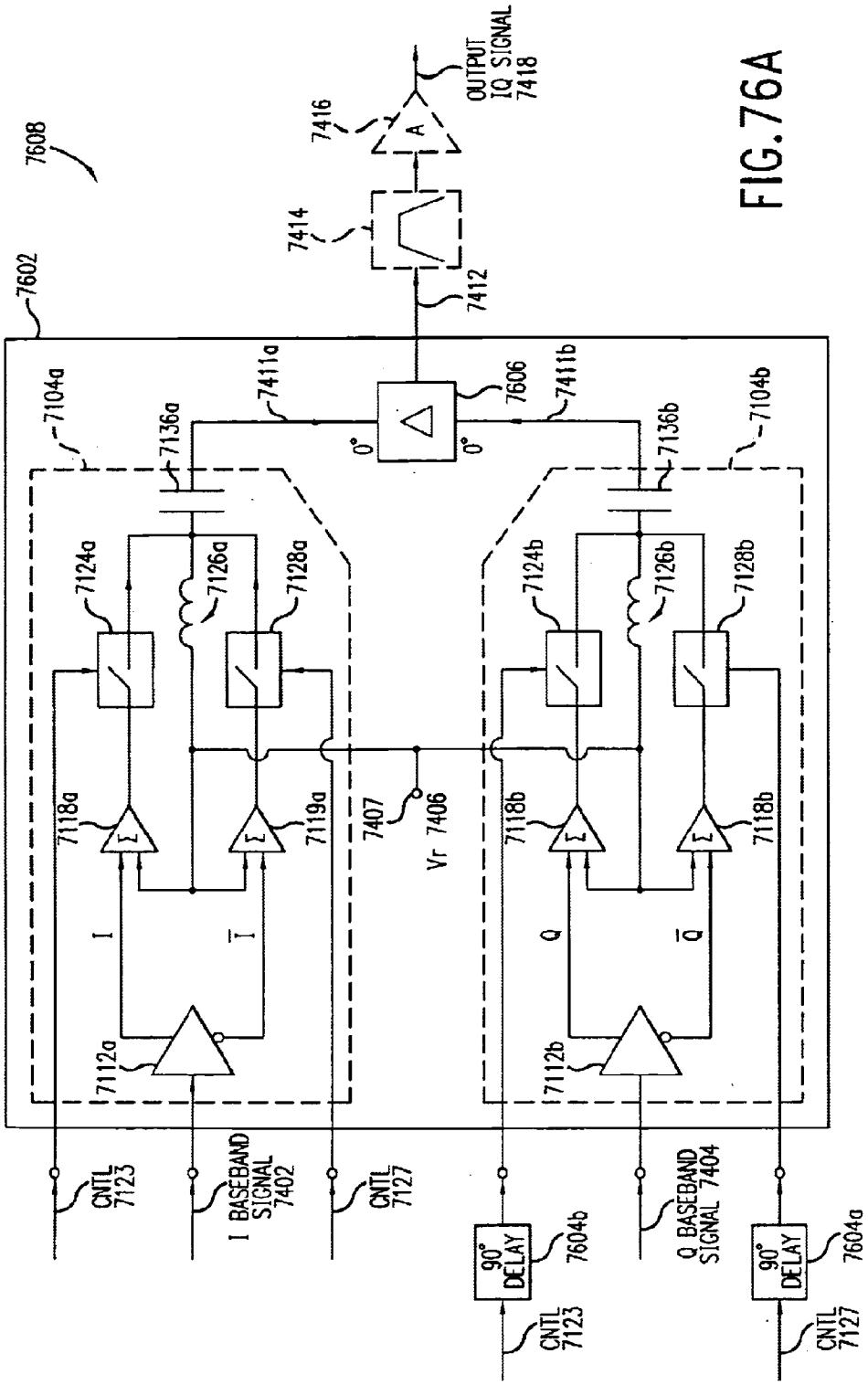

7608
7602
7104a
7104b
7136a
7136b
7411a
7411b
7606
7414
7412
7416
A
OUTPUT IQ SIGNAL 7418
0°
0°
7124a
7126a
7128a
7124b
7126b
7128b
7118a
7119a
7118b
7407
Vr 7406
I
Ī
Q
Q̄
7112a
7112b
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
Q BASEBAND SIGNAL 7404
90° DELAY
7604b
7604a
CNTL 7123
CNTL 7127

FIG. 76A

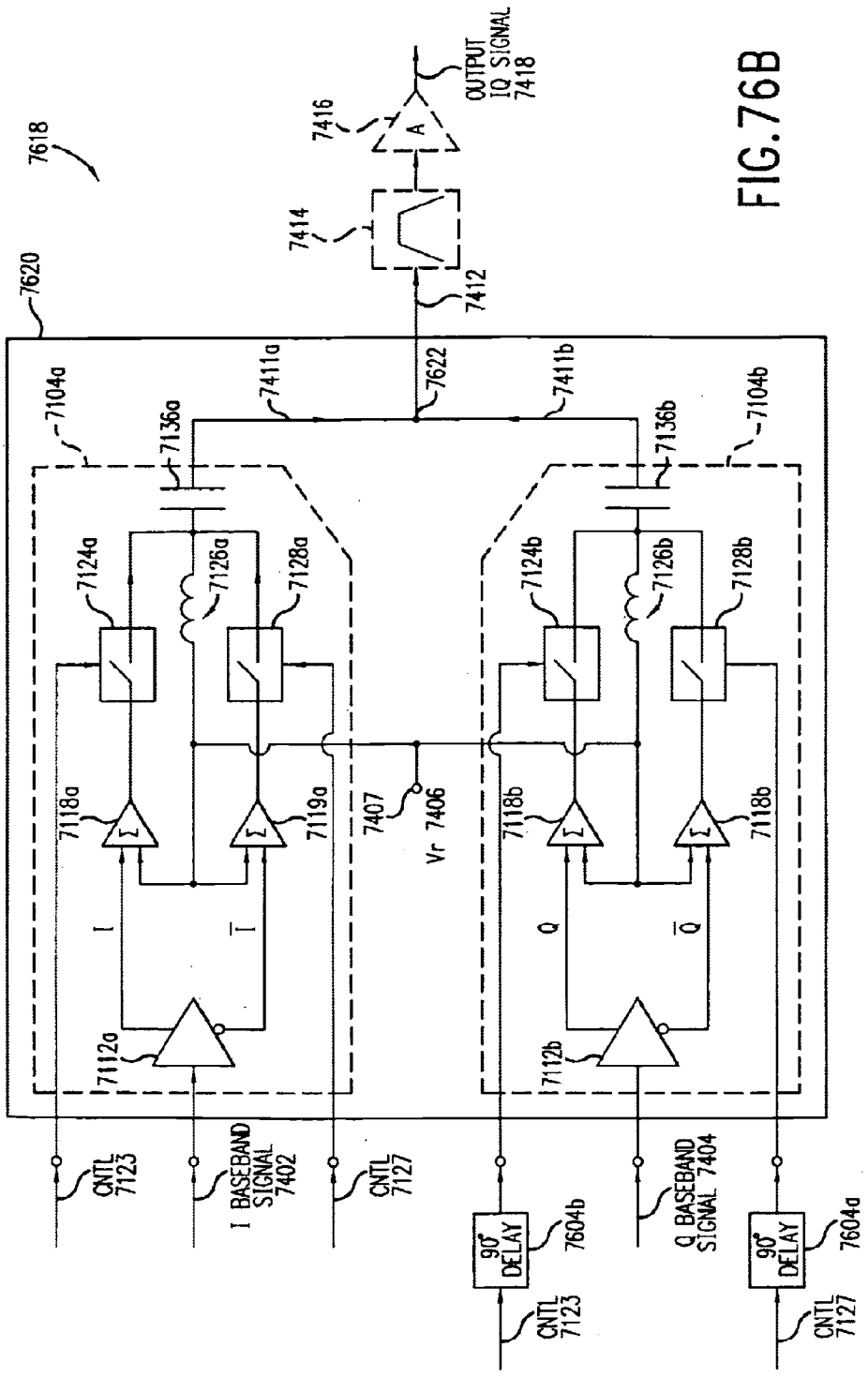

7618
7620
7416
A
OUTPUT IQ SIGNAL 7418
7414
7412
7622
7411a
7411b
7104a
7104b
7136a
7136b
7124a
7126a
7128a
7124b
7126b
7128b
7118a
7119a
7407
Vr 7406
7118b
7118b
I
Ī
Q
Q̄
7112a
7112b
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
90° DELAY
7604b
Q BASEBAND SIGNAL 7404
90° DELAY
7604a
CNTL 7123
CNTL 7127

FIG. 76B

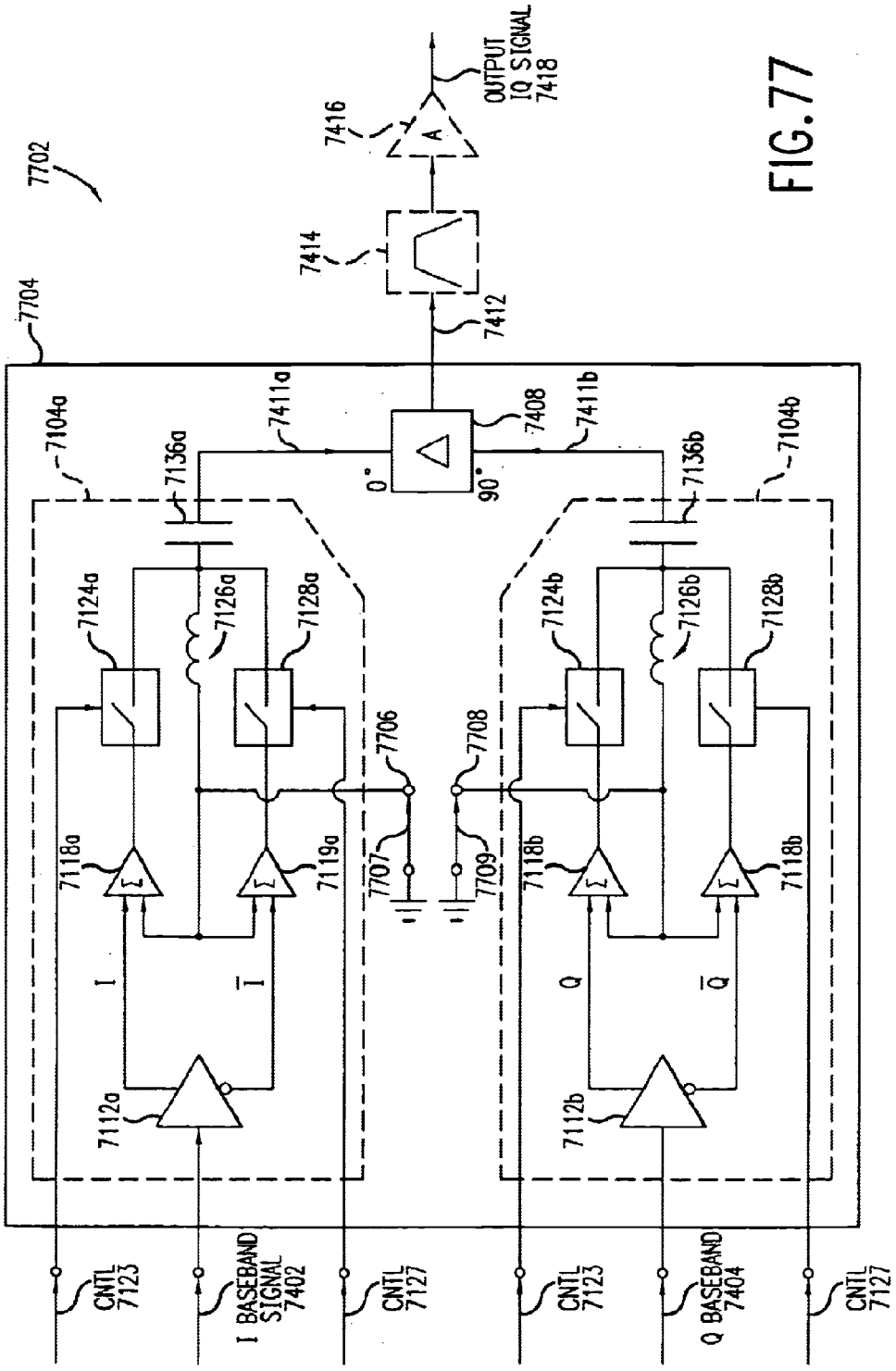

7702
7704
7416
A
OUTPUT IQ SIGNAL 7418
7414
7412
7104a
7104b
7411a
7411b
7408
7136a
7136b
0°
90°
7124a
7126a
7128a
7124b
7126b
7128b
7706
7708
7707
7709
7118a
7119a
7118b
I
Ī
Q
Q̄
7112a
7112b
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
CNTL 7123
Q BASEBAND 7404
CNTL 7127

FIG. 77

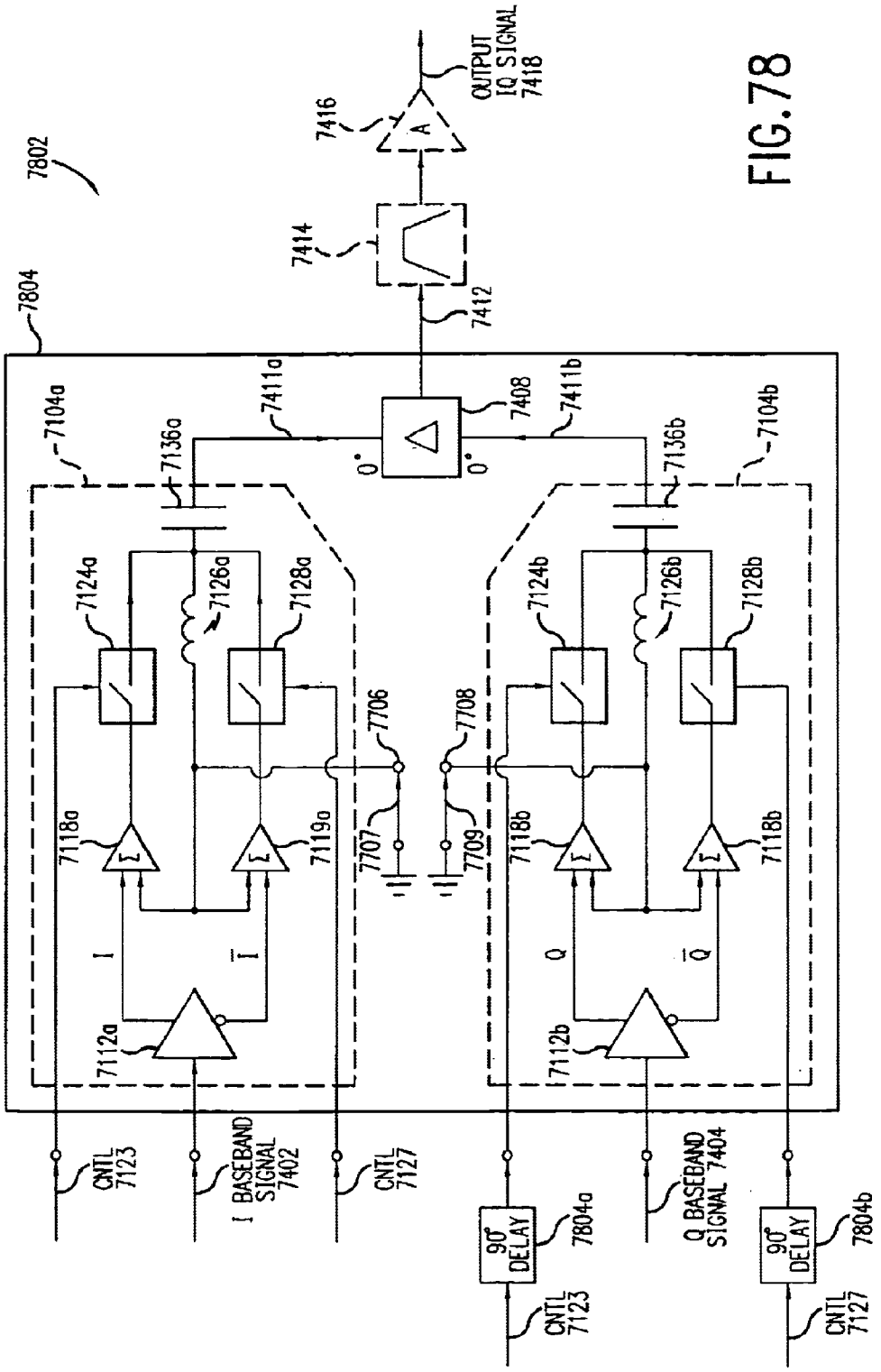

7802
7804
7104a
7104b
7136a
7136b
7411a
7411b
7408
7412
7414
7416
OUTPUT IQ SIGNAL 7418
0°
0°
7124a
7126a
7128a
7124b
7126b
7128b
7706
7707
7708
7709
7118a
7119a
7118b
7112a
7112b
I
Ī
Q
Q̄
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
Q BASEBAND SIGNAL 7404
90° DELAY
7804a
7804b

FIG. 78

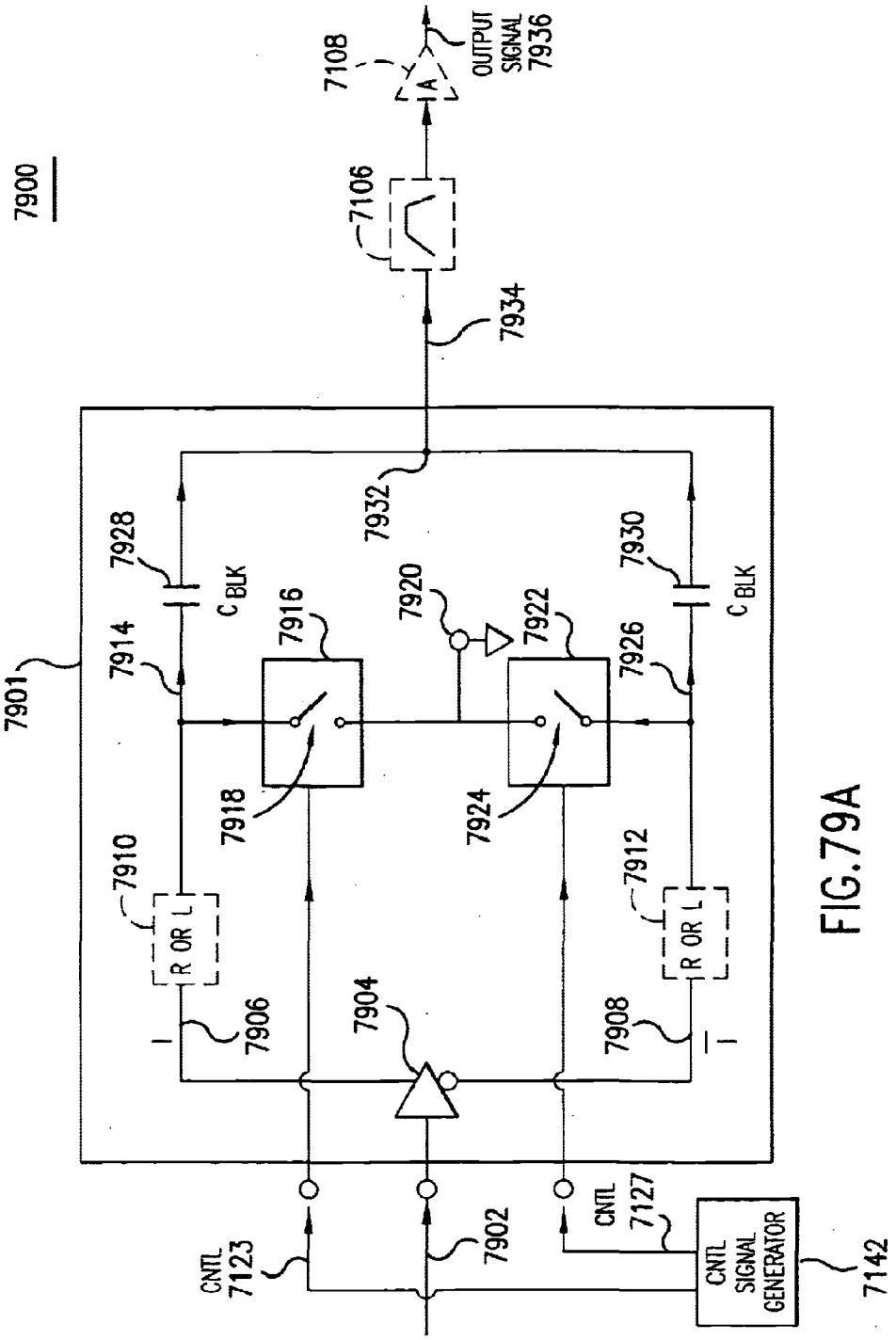

7900
7108
OUTPUT SIGNAL 7936
7106
7934
7932
7928
7930
7914
7916
7920
7922
7926
7901
C_{BLK}
C_{BLK}
7918
7924
7910
7912
R OR L
R OR L
7906
7904
7908
CNTL 7123
7902
CNTL 7127
CNTL SIGNAL GENERATOR
7142

FIG.79A

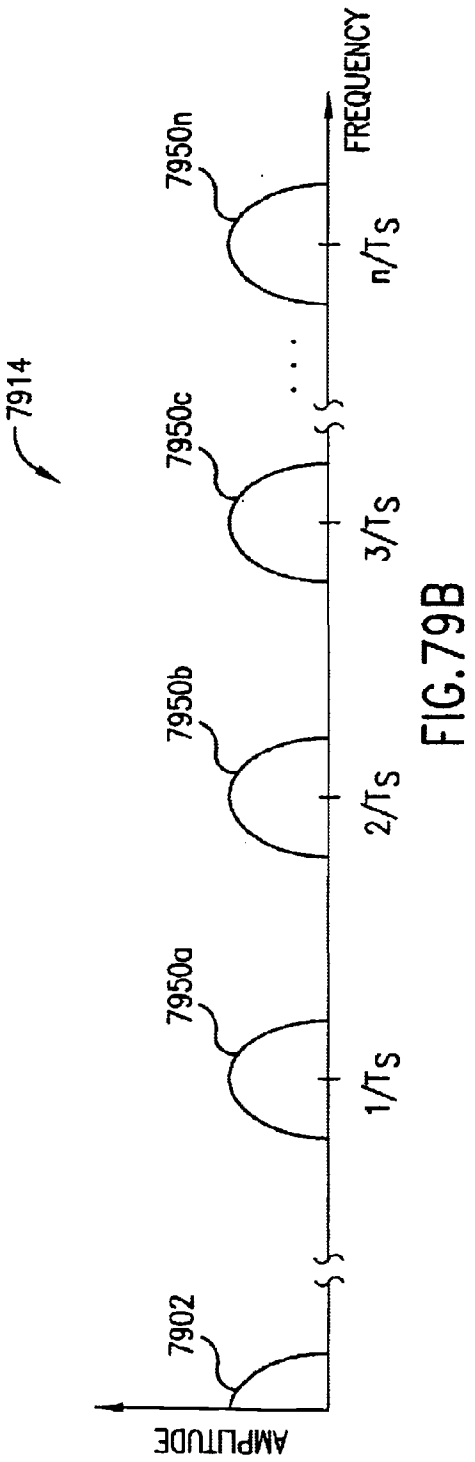


FIG.79B

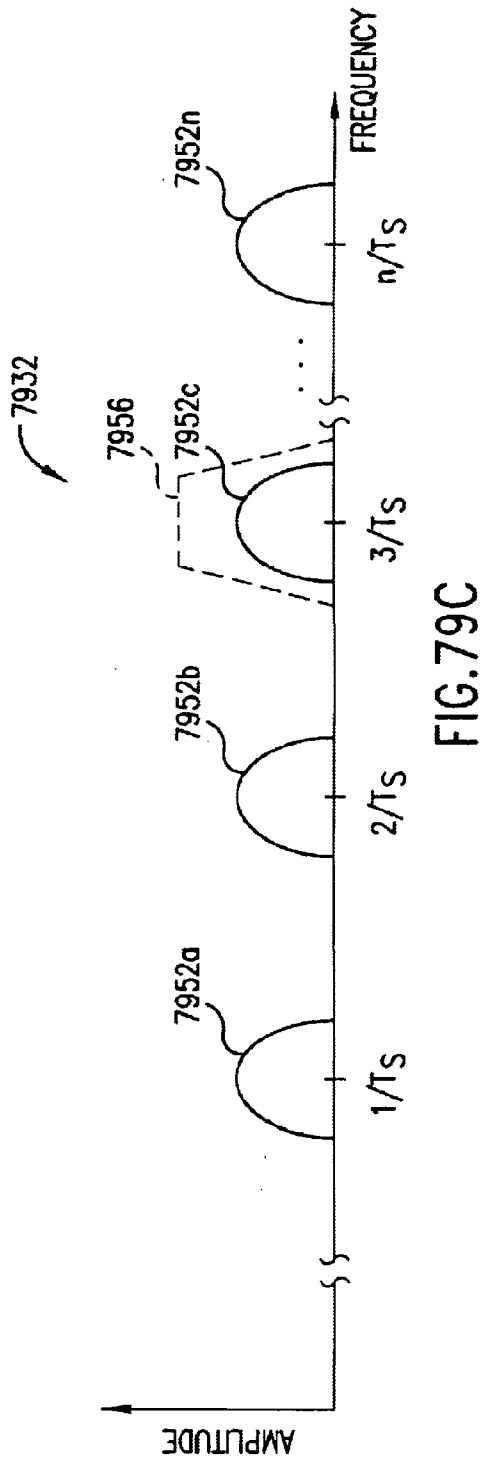


FIG.79C

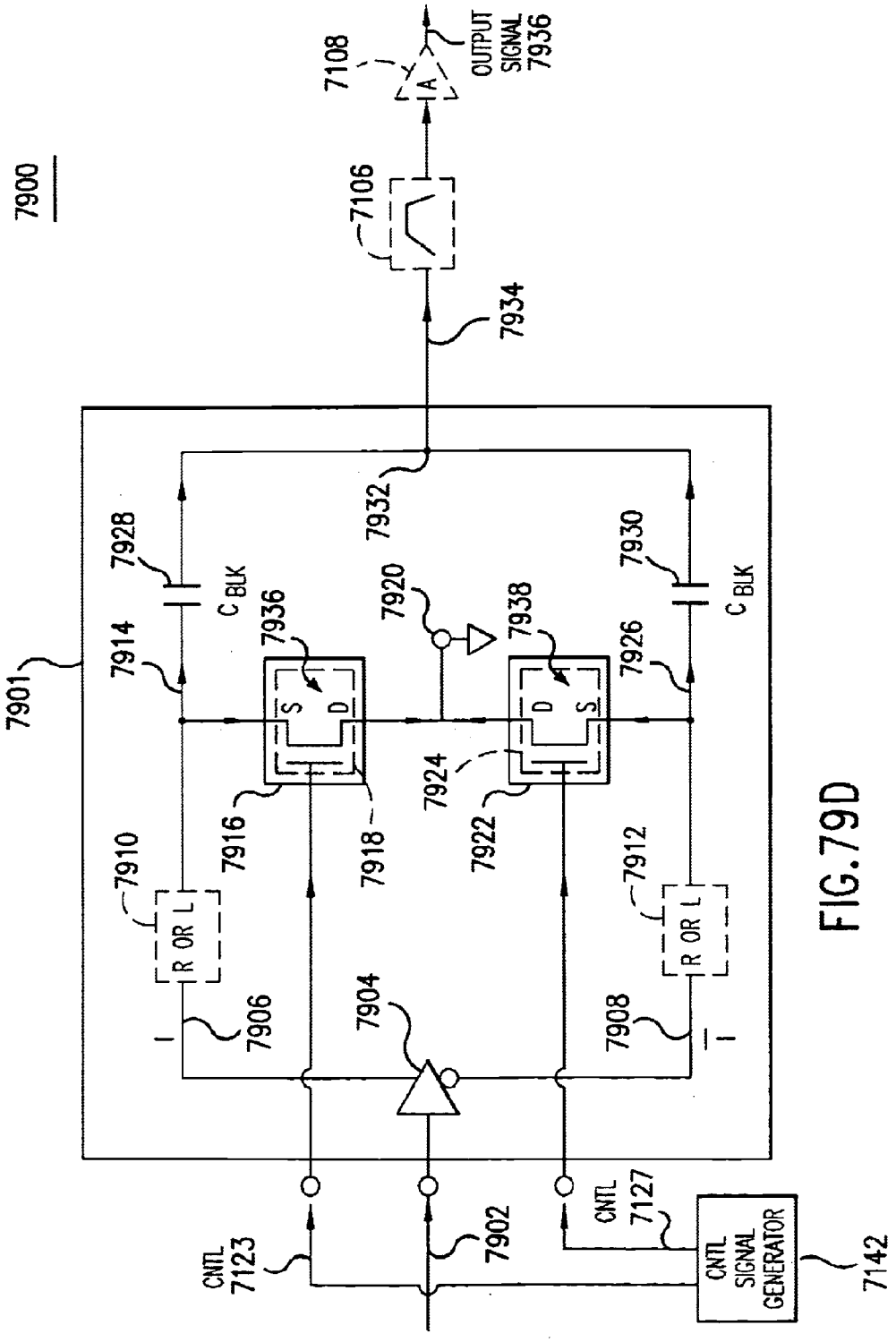

7900
7108
OUTPUT SIGNAL 7936
7106
7934
7932
7928
7930
C BLK
C BLK
7936
7920
7938
7914
7926
7901
S
D
D
S
7924
7916
7918
7922
7910
7912
R OR L
R OR L
7906
7904
7908
CNTL 7123
7902
CNTL 7127
CNTL SIGNAL GENERATOR
7142

FIG.79D

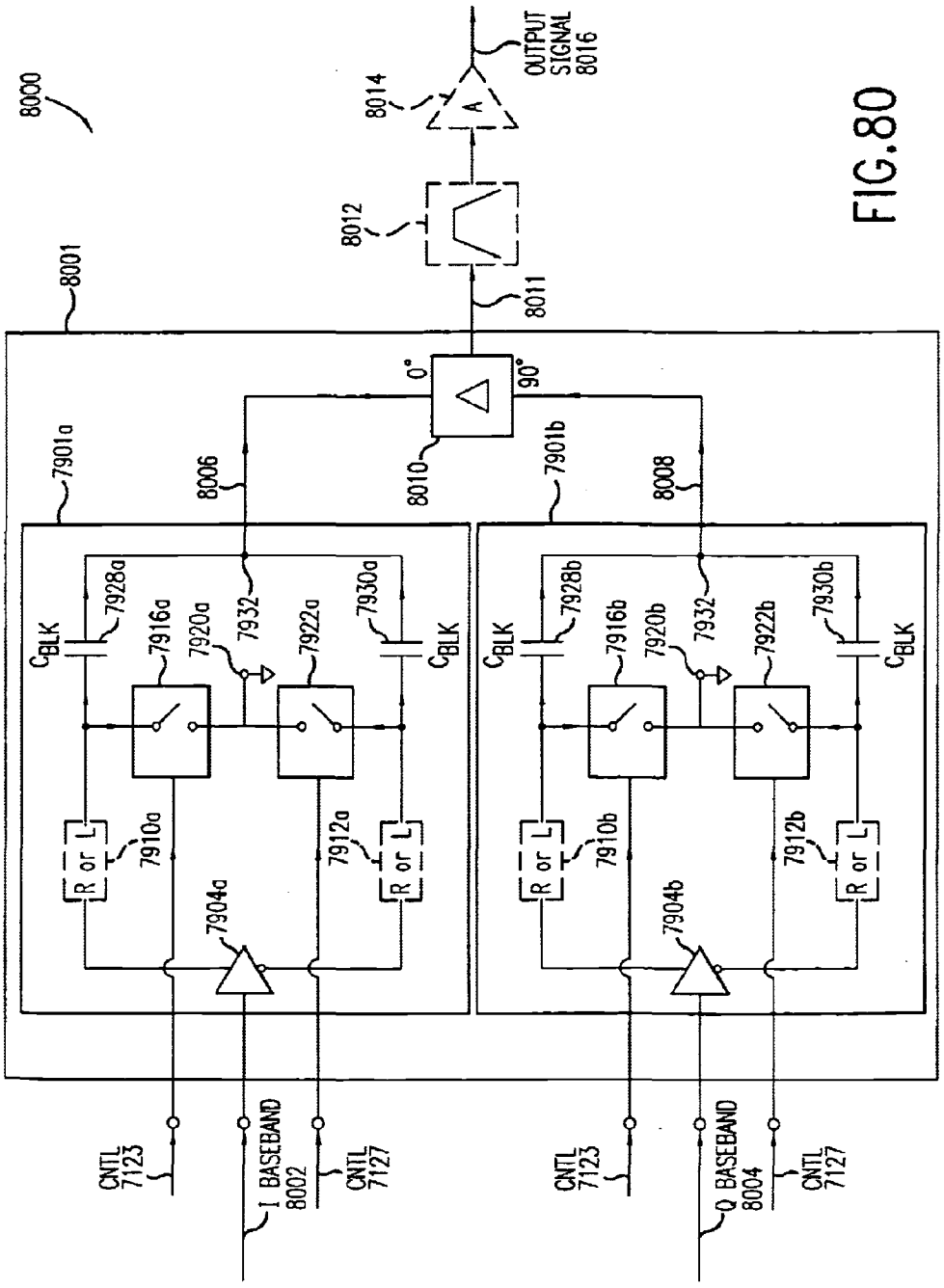

8000
8014
OUTPUT SIGNAL 8016
8012
8001
8011
0°
90°
7901a
8006
8010
7901b
8008
C_BLK
7928a
7916a
7920a
7932
7922a
7930a
7928b
7916b
7920b
7922b
7930b
R or L
7910a
7912a
7904a
7910b
7912b
7904b
CNTL 7123
I BASEBAND 8002
CNTL 7127
Q BASEBAND 8004

FIG.80

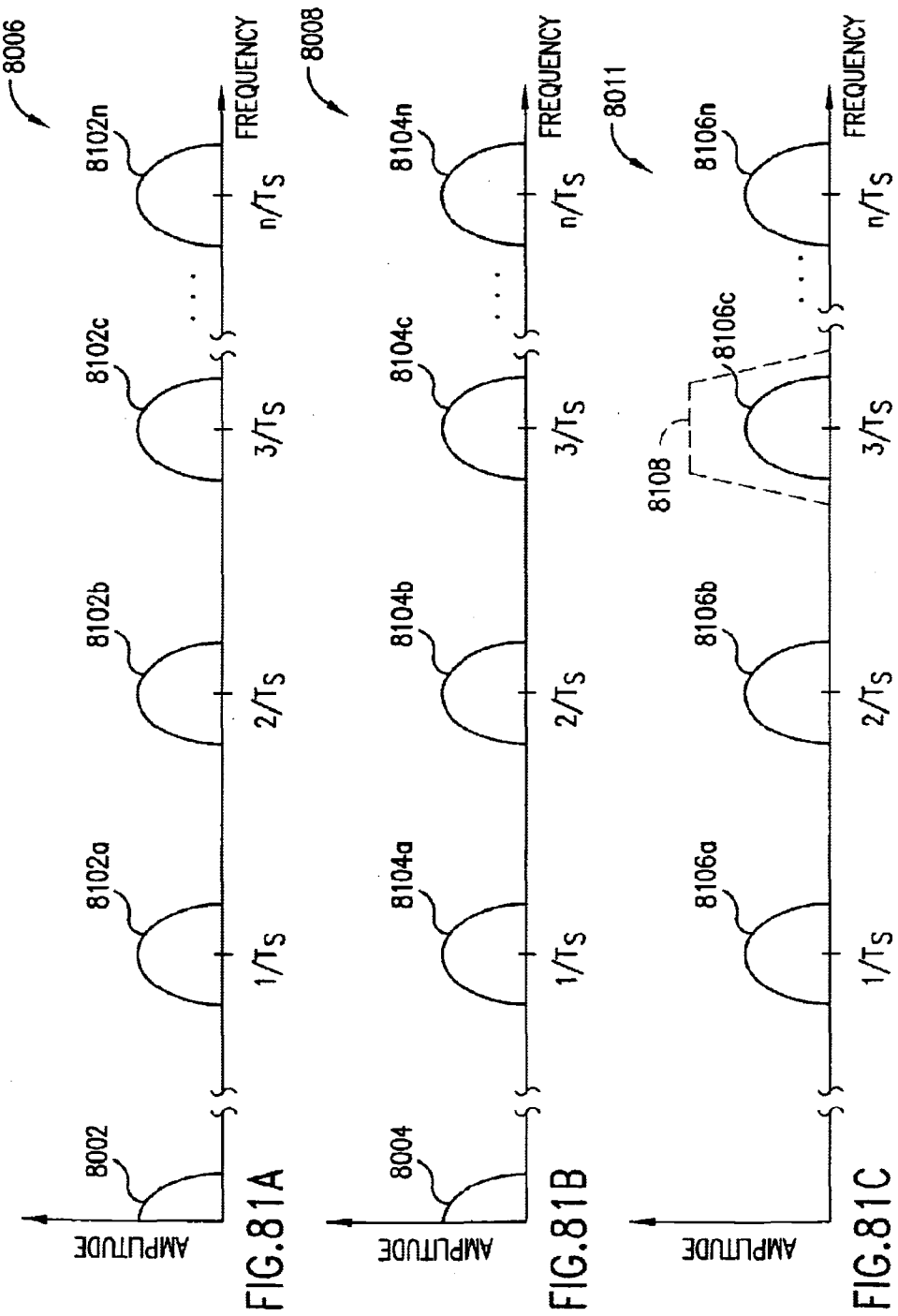


FIG.81A FIG.81B FIG.81C

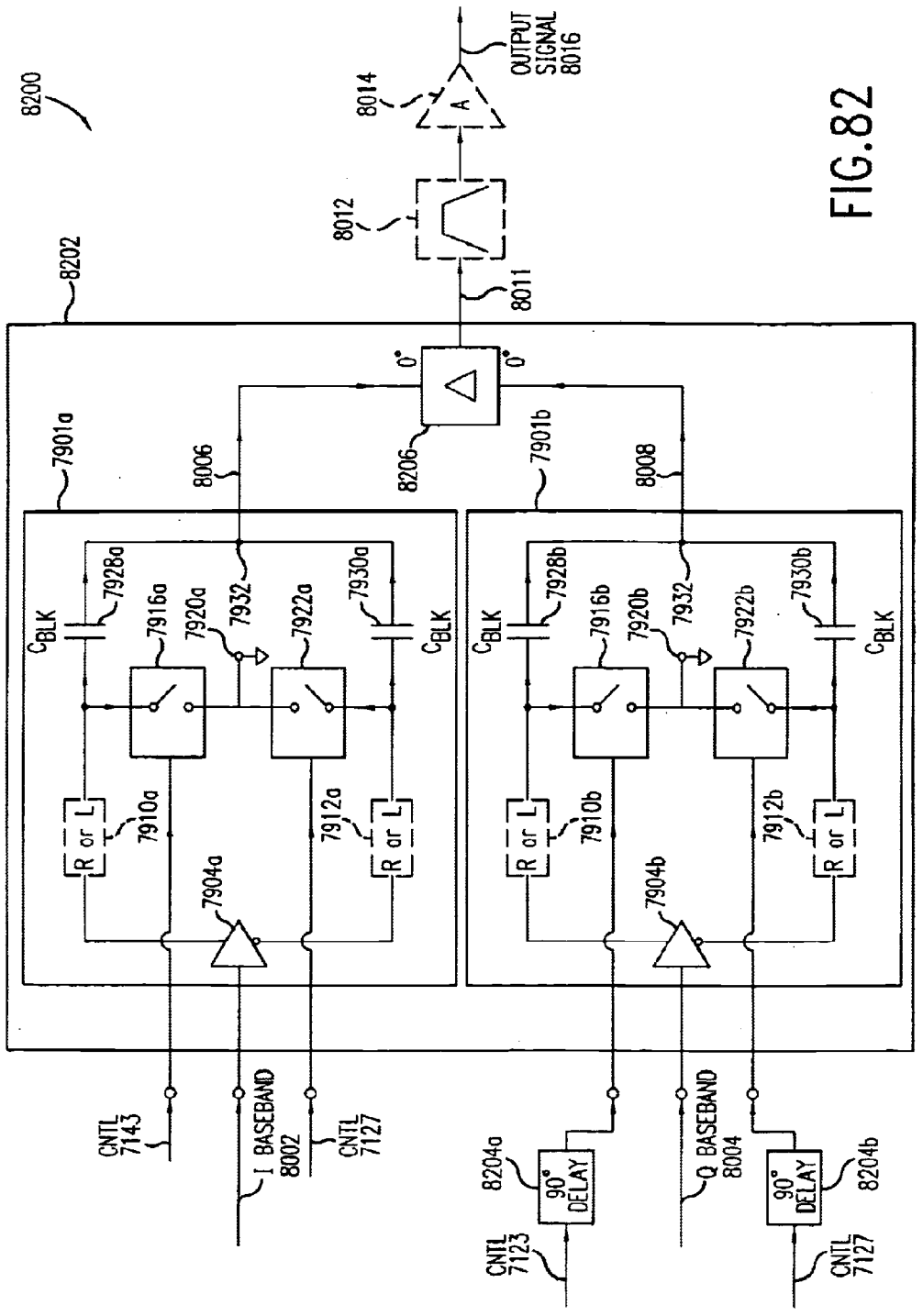

8200
8014
OUTPUT SIGNAL 8016
8012
8011
8202
0°
0°
8206
7901a
7901b
8006
8008
7928a
7916a
7920a
7932
7922a
7930a
C_BLK
7928b
7916b
7920b
7922b
7930b
R or L
7910a
7912a
7904a
7910b
7912b
7904b
CNTL 7143
I BASEBAND 8002
CNTL 7127
8204a
90° DELAY
CNTL 7123
Q BASEBAND 8004
8204b

FIG.82

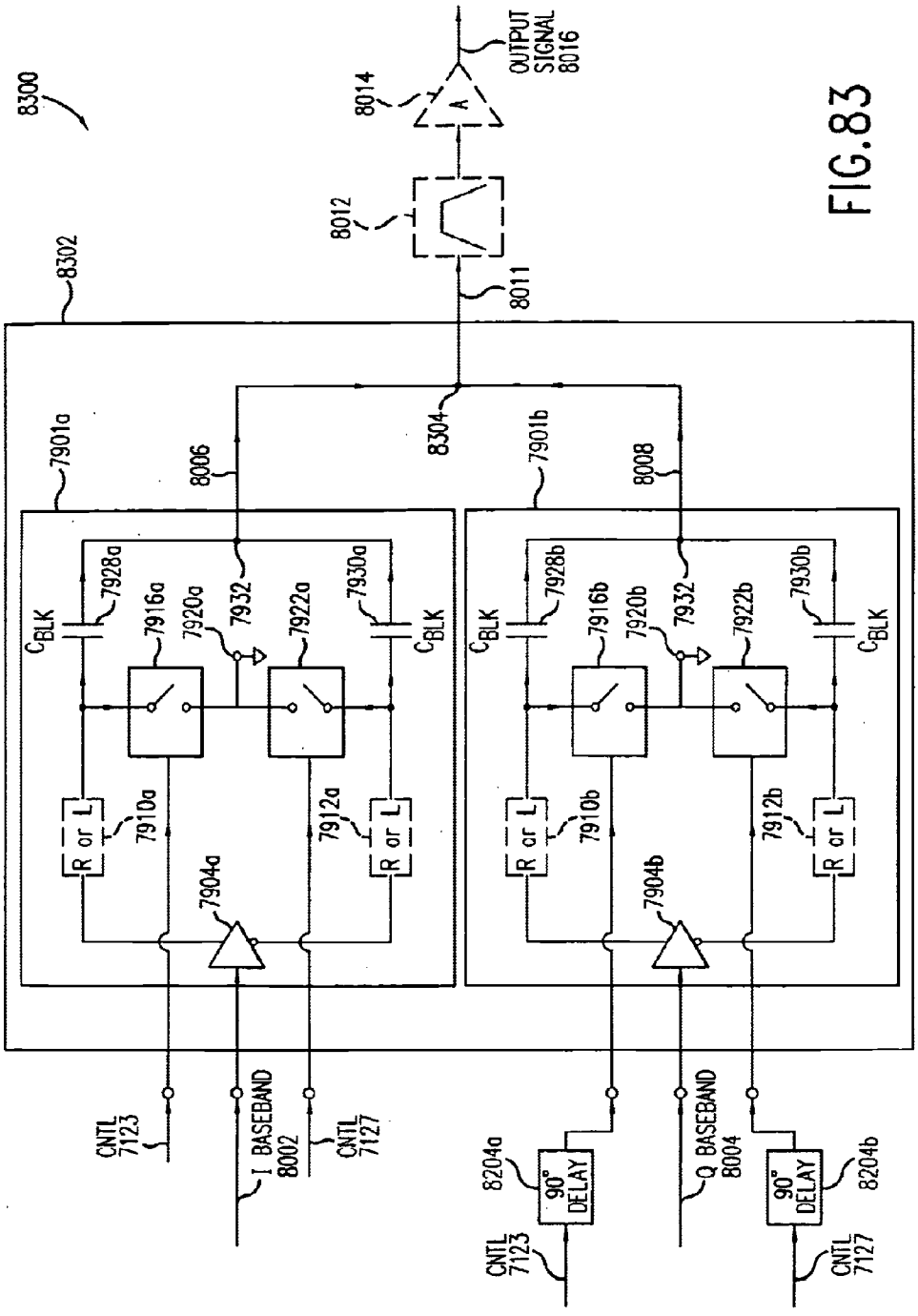

8300
8014
OUTPUT SIGNAL 8016
8012
8011
8302
8304
7901a
8006
7901b
8008
7928a
7916a
7920a
7932
7922a
7930a
C_BLK
7910a
7912a
R or L
7904a
7928b
7916b
7920b
7922b
7930b
7910b
7912b
7904b
CNTL 7123
I BASEBAND 8002
CNTL 7127
Q BASEBAND 8004
8204a
8204b
90° DELAY

FIG.83

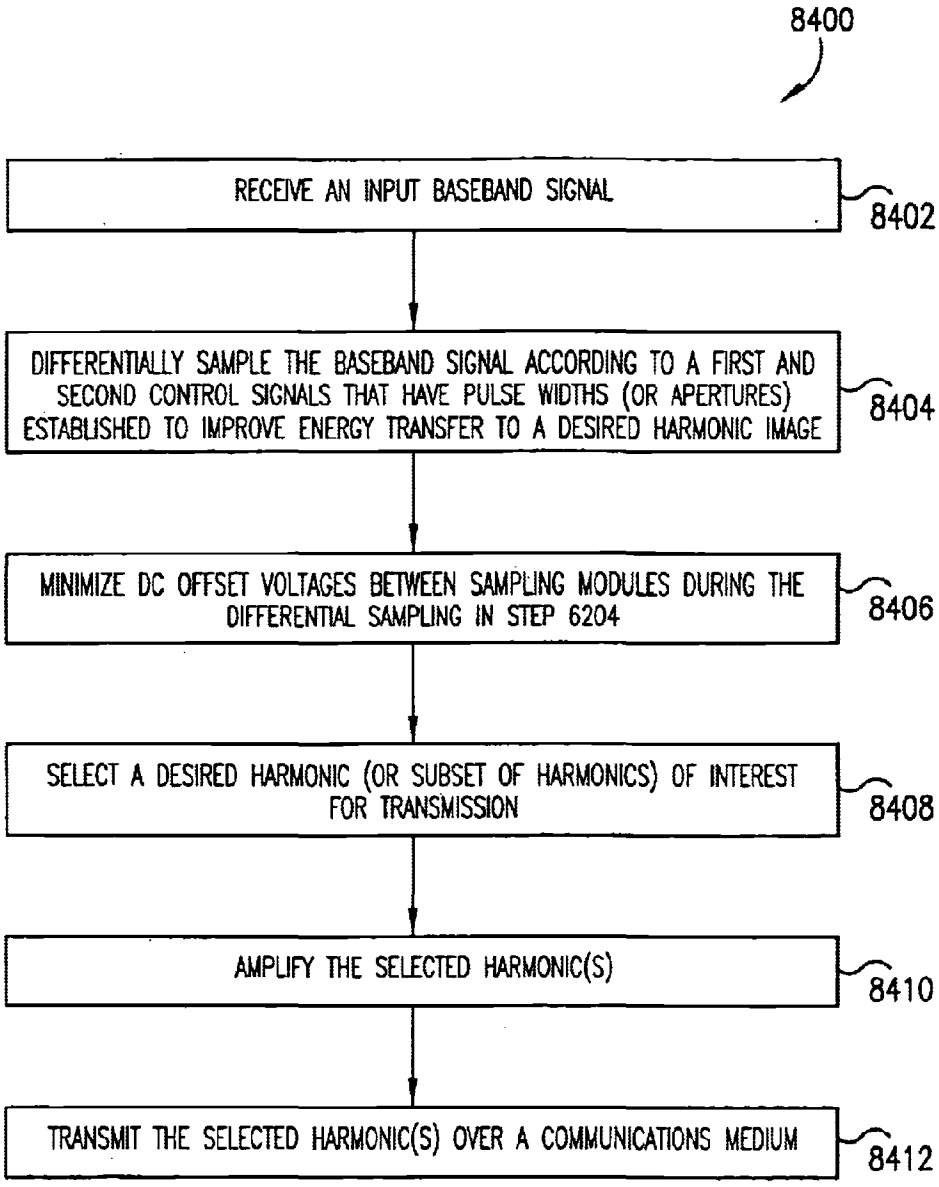

8400
RECEIVE AN INPUT BASEBAND SIGNAL
8402
DIFFERENTIALLY SAMPLE THE BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE
8404
MINIMIZE DC OFFSET VOLTAGES BETWEEN SAMPLING MODULES DURING THE DIFFERENTIAL SAMPLING IN STEP 6204
8406
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8408
AMPLIFY THE SELECTED HARMONIC(S)
8410
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8412

FIG.84

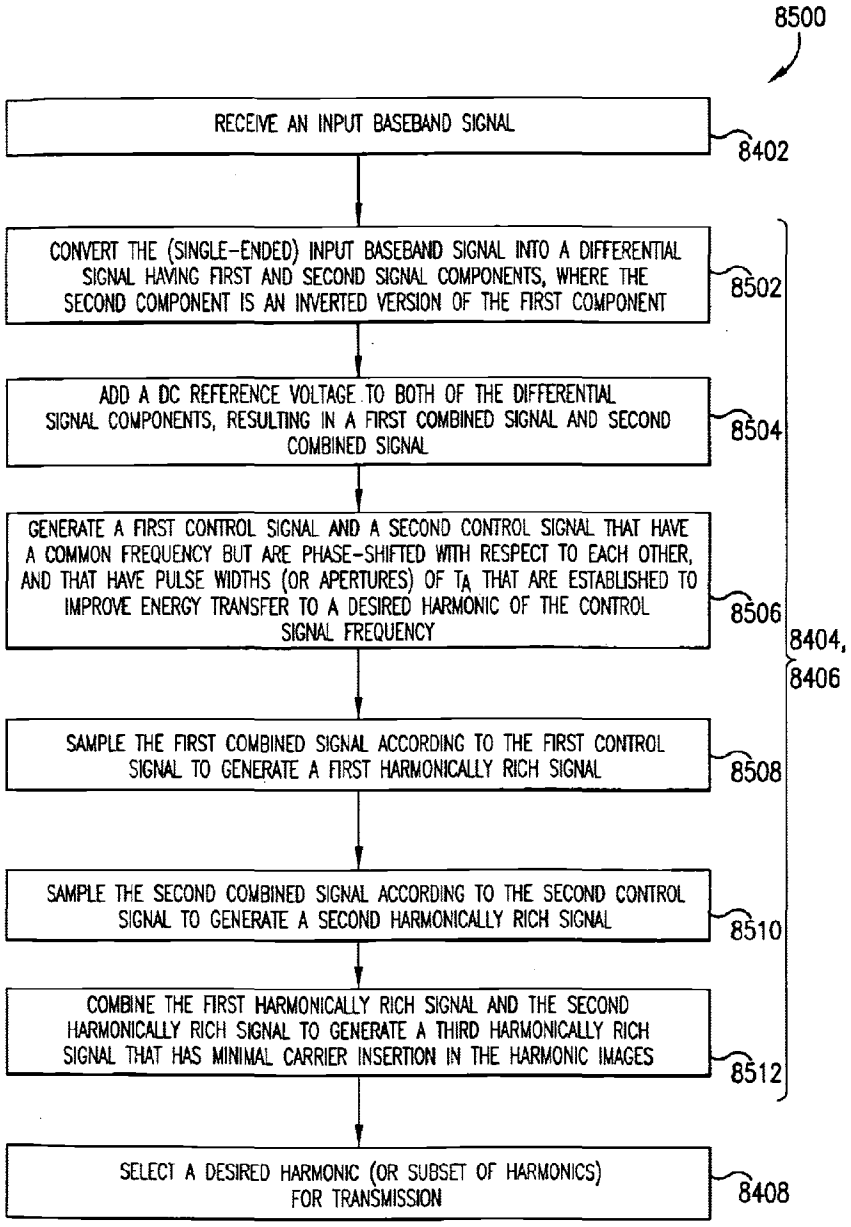

8500
RECEIVE AN INPUT BASEBAND SIGNAL
8402
CONVERT THE (SINGLE-ENDED) INPUT BASEBAND SIGNAL INTO A DIFFERENTIAL SIGNAL HAVING FIRST AND SECOND SIGNAL COMPONENTS, WHERE THE SECOND COMPONENT IS AN INVERTED VERSION OF THE FIRST COMPONENT
8502
ADD A DC REFERENCE VOLTAGE TO BOTH OF THE DIFFERENTIAL SIGNAL COMPONENTS, RESULTING IN A FIRST COMBINED SIGNAL AND SECOND COMBINED SIGNAL
8504
GENERATE A FIRST CONTROL SIGNAL AND A SECOND CONTROL SIGNAL THAT HAVE A COMMON FREQUENCY BUT ARE PHASE-SHIFTED WITH RESPECT TO EACH OTHER, AND THAT HAVE PULSE WIDTHS (OR APERTURES) OF T_A THAT ARE ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC OF THE CONTROL SIGNAL FREQUENCY
8506
8404, 8406
SAMPLE THE FIRST COMBINED SIGNAL ACCORDING TO THE FIRST CONTROL SIGNAL TO GENERATE A FIRST HARMONICALLY RICH SIGNAL
8508
SAMPLE THE SECOND COMBINED SIGNAL ACCORDING TO THE SECOND CONTROL SIGNAL TO GENERATE A SECOND HARMONICALLY RICH SIGNAL
8510
COMBINE THE FIRST HARMONICALLY RICH SIGNAL AND THE SECOND HARMONICALLY RICH SIGNAL TO GENERATE A THIRD HARMONICALLY RICH SIGNAL THAT HAS MINIMAL CARRIER INSERTION IN THE HARMONIC IMAGES
8512
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) FOR TRANSMISSION
8408

FIG.85

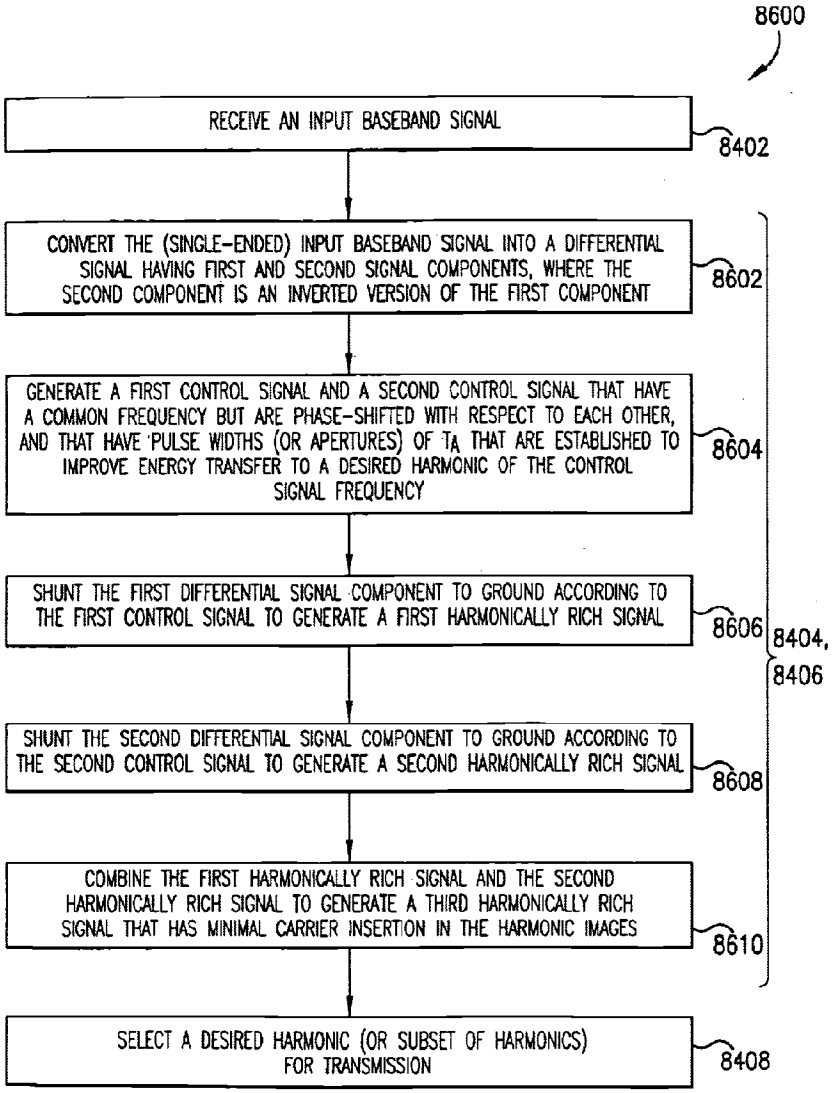

8600
RECEIVE AN INPUT BASEBAND SIGNAL
8402
CONVERT THE (SINGLE-ENDED) INPUT BASEBAND SIGNAL INTO A DIFFERENTIAL SIGNAL HAVING FIRST AND SECOND SIGNAL COMPONENTS, WHERE THE SECOND COMPONENT IS AN INVERTED VERSION OF THE FIRST COMPONENT
8602
GENERATE A FIRST CONTROL SIGNAL AND A SECOND CONTROL SIGNAL THAT HAVE A COMMON FREQUENCY BUT ARE PHASE-SHIFTED WITH RESPECT TO EACH OTHER, AND THAT HAVE PULSE WIDTHS (OR APERTURES) OF T_A THAT ARE ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC OF THE CONTROL SIGNAL FREQUENCY
8604
SHUNT THE FIRST DIFFERENTIAL SIGNAL COMPONENT TO GROUND ACCORDING TO THE FIRST CONTROL SIGNAL TO GENERATE A FIRST HARMONICALLY RICH SIGNAL
8606
SHUNT THE SECOND DIFFERENTIAL SIGNAL COMPONENT TO GROUND ACCORDING TO THE SECOND CONTROL SIGNAL TO GENERATE A SECOND HARMONICALLY RICH SIGNAL
8608
COMBINE THE FIRST HARMONICALLY RICH SIGNAL AND THE SECOND HARMONICALLY RICH SIGNAL TO GENERATE A THIRD HARMONICALLY RICH SIGNAL THAT HAS MINIMAL CARRIER INSERTION IN THE HARMONIC IMAGES
8610
8404, 8406
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) FOR TRANSMISSION
8408

FIG.86

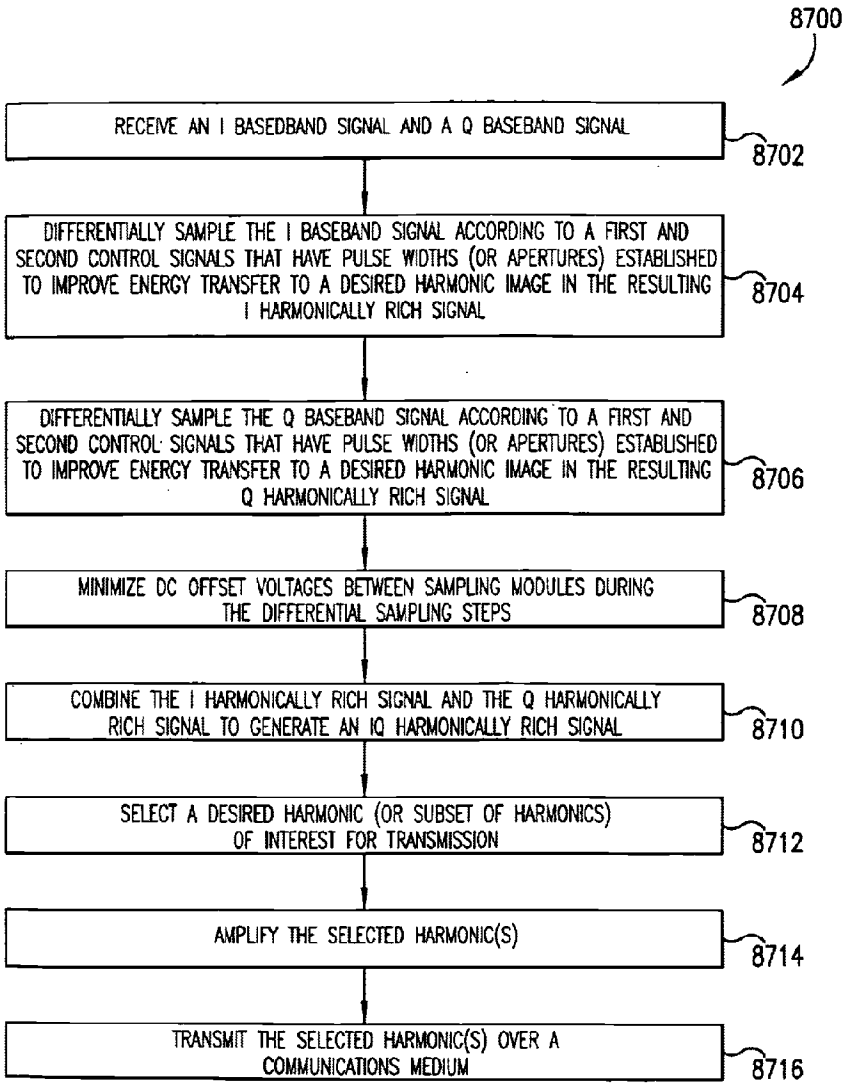

8700
RECEIVE AN I BASEDBAND SIGNAL AND A Q BASEBAND SIGNAL
8702
DIFFERENTIALLY SAMPLE THE I BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING I HARMONICALLY RICH SIGNAL
8704
DIFFERENTIALLY SAMPLE THE Q BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING Q HARMONICALLY RICH SIGNAL
8706
MINIMIZE DC OFFSET VOLTAGES BETWEEN SAMPLING MODULES DURING THE DIFFERENTIAL SAMPLING STEPS
8708
COMBINE THE I HARMONICALLY RICH SIGNAL AND THE Q HARMONICALLY RICH SIGNAL TO GENERATE AN IQ HARMONICALLY RICH SIGNAL
8710
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8712
AMPLIFY THE SELECTED HARMONIC(S)
8714
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8716

FIG.87

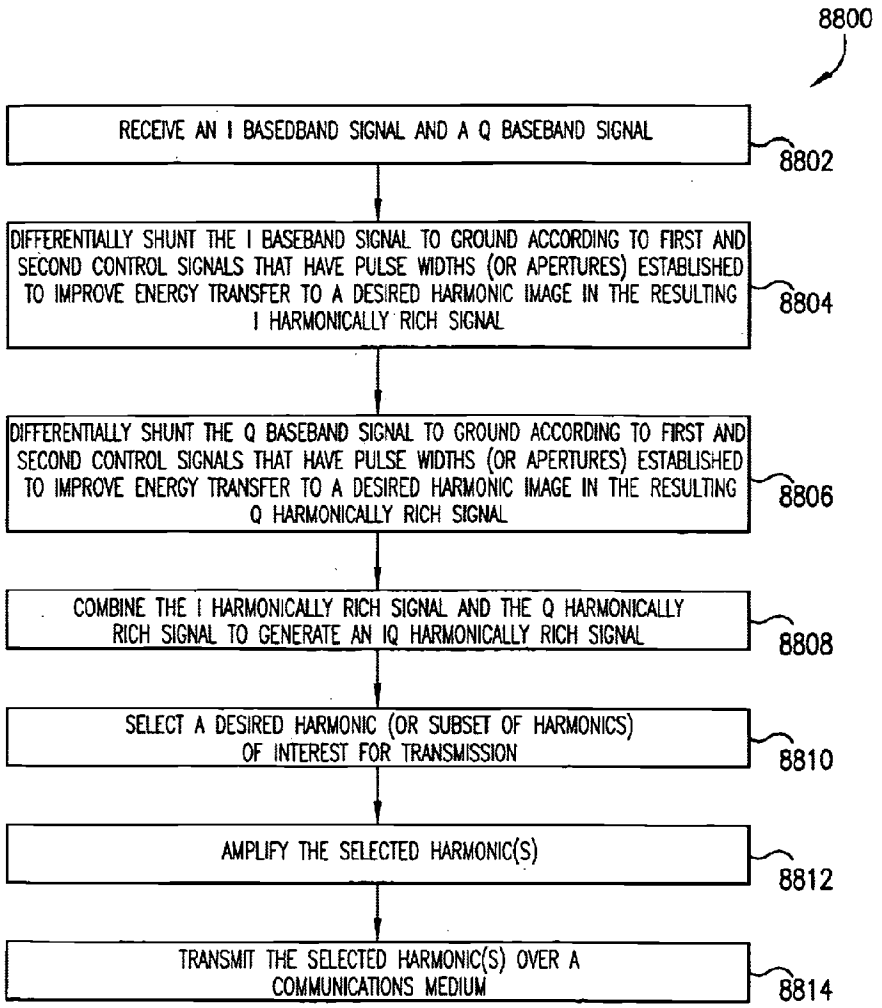

8800
RECEIVE AN I BASEDBAND SIGNAL AND A Q BASEBAND SIGNAL
8802
DIFFERENTIALLY SHUNT THE I BASEBAND SIGNAL TO GROUND ACCORDING TO FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING I HARMONICALLY RICH SIGNAL
8804
DIFFERENTIALLY SHUNT THE Q BASEBAND SIGNAL TO GROUND ACCORDING TO FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING Q HARMONICALLY RICH SIGNAL
8806
COMBINE THE I HARMONICALLY RICH SIGNAL AND THE Q HARMONICALLY RICH SIGNAL TO GENERATE AN IQ HARMONICALLY RICH SIGNAL
8808
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8810
AMPLIFY THE SELECTED HARMONIC(S)
8812
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8814

FIG.88

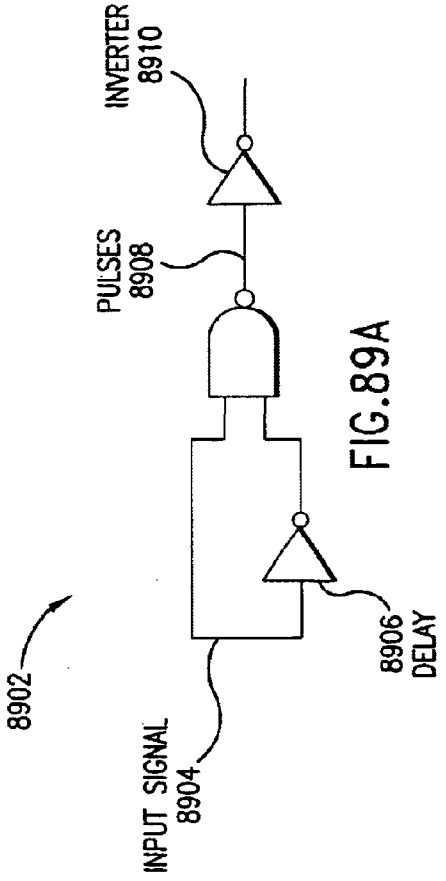


FIG.89A

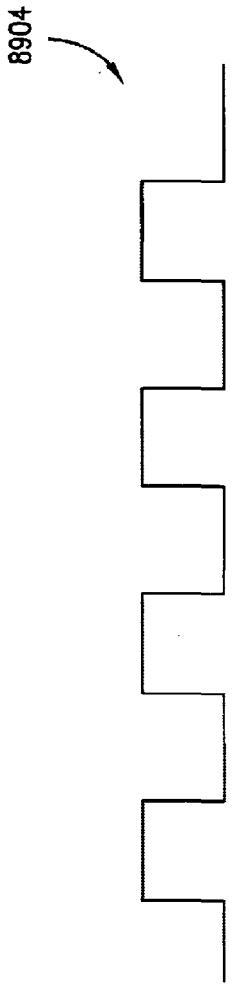


FIG.89B

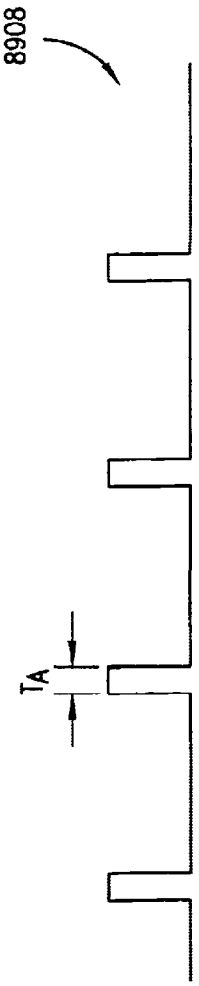


FIG.89C

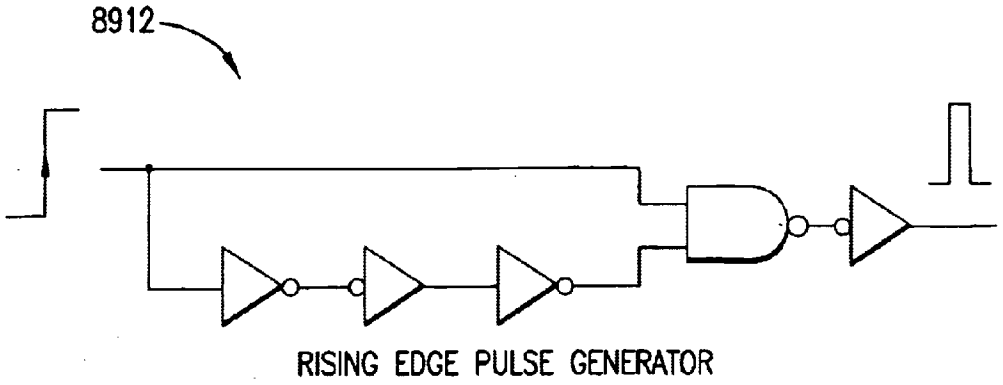


FIG.89D

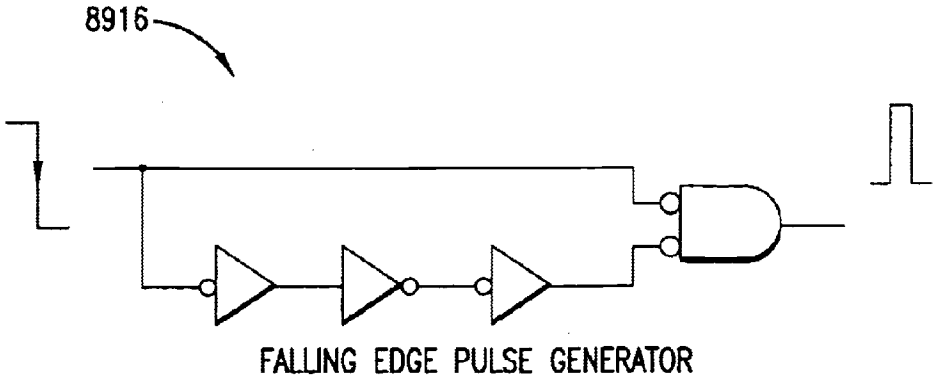


FIG.89E

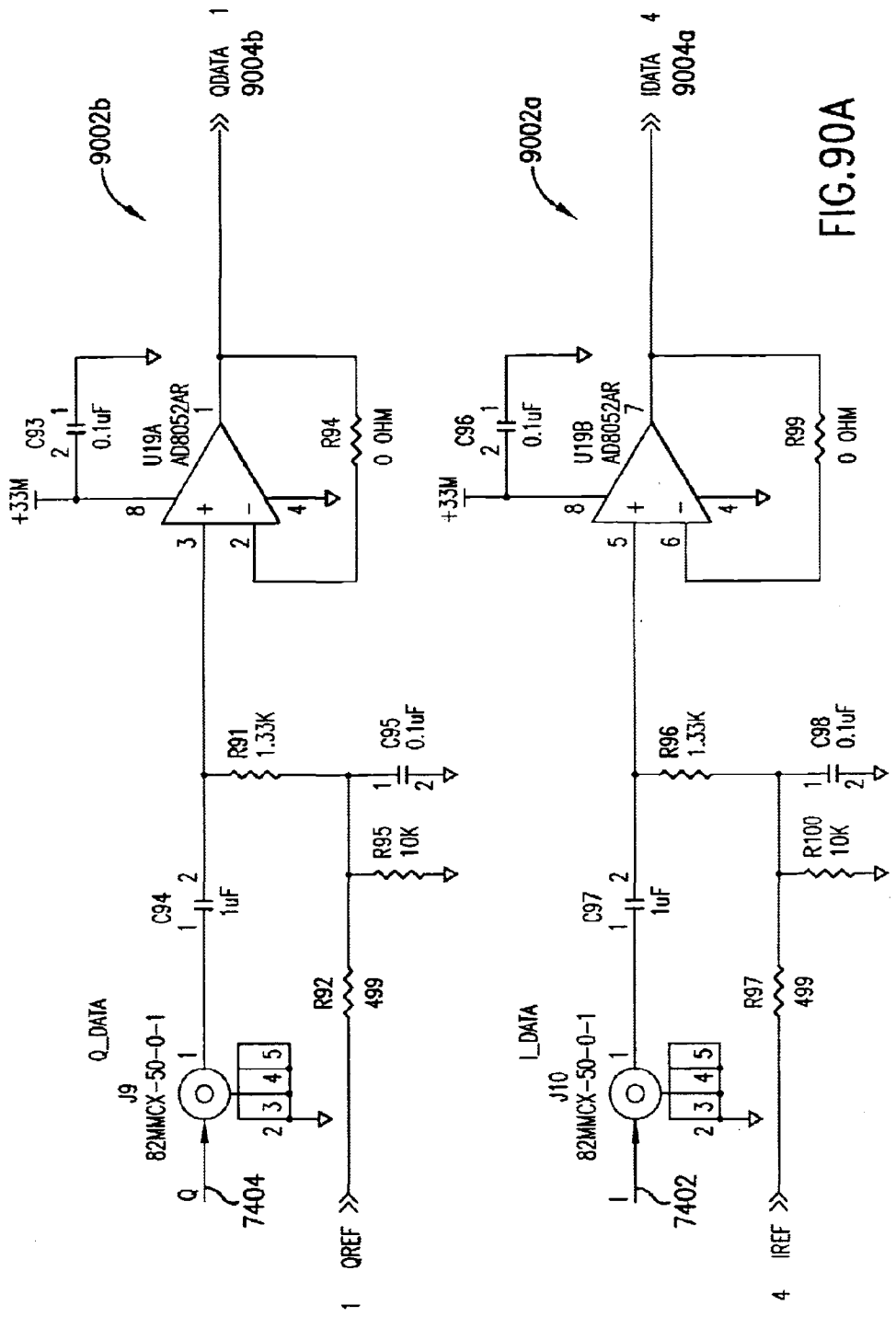

9002b
9004b
QDATA
C93
0.1uF
U19A
AD8052AR
+33M
R94
0 OHM
R91
1.33K
C95
0.1uF
R95
10K
C94
1uF
R92
499
Q_DATA
J9
82MMCX-50-0-1
Q
7404
QREF
9002a
9004a
IDATA
C96
0.1uF
U19B
AD8052AR
+33M
R99
0 OHM
R96
1.33K
C98
0.1uF
R100
10K
C97
1uF
R97
499
I_DATA
J10
82MMCX-50-0-1
7402
IREF

FIG.90A

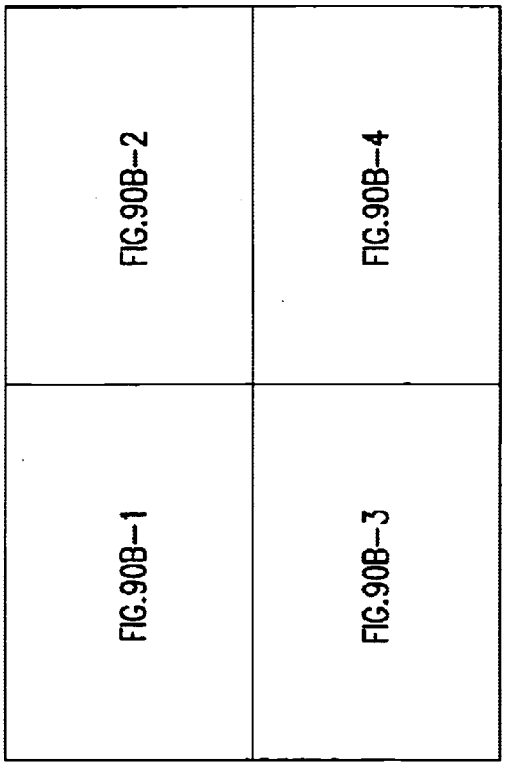


FIG.90B

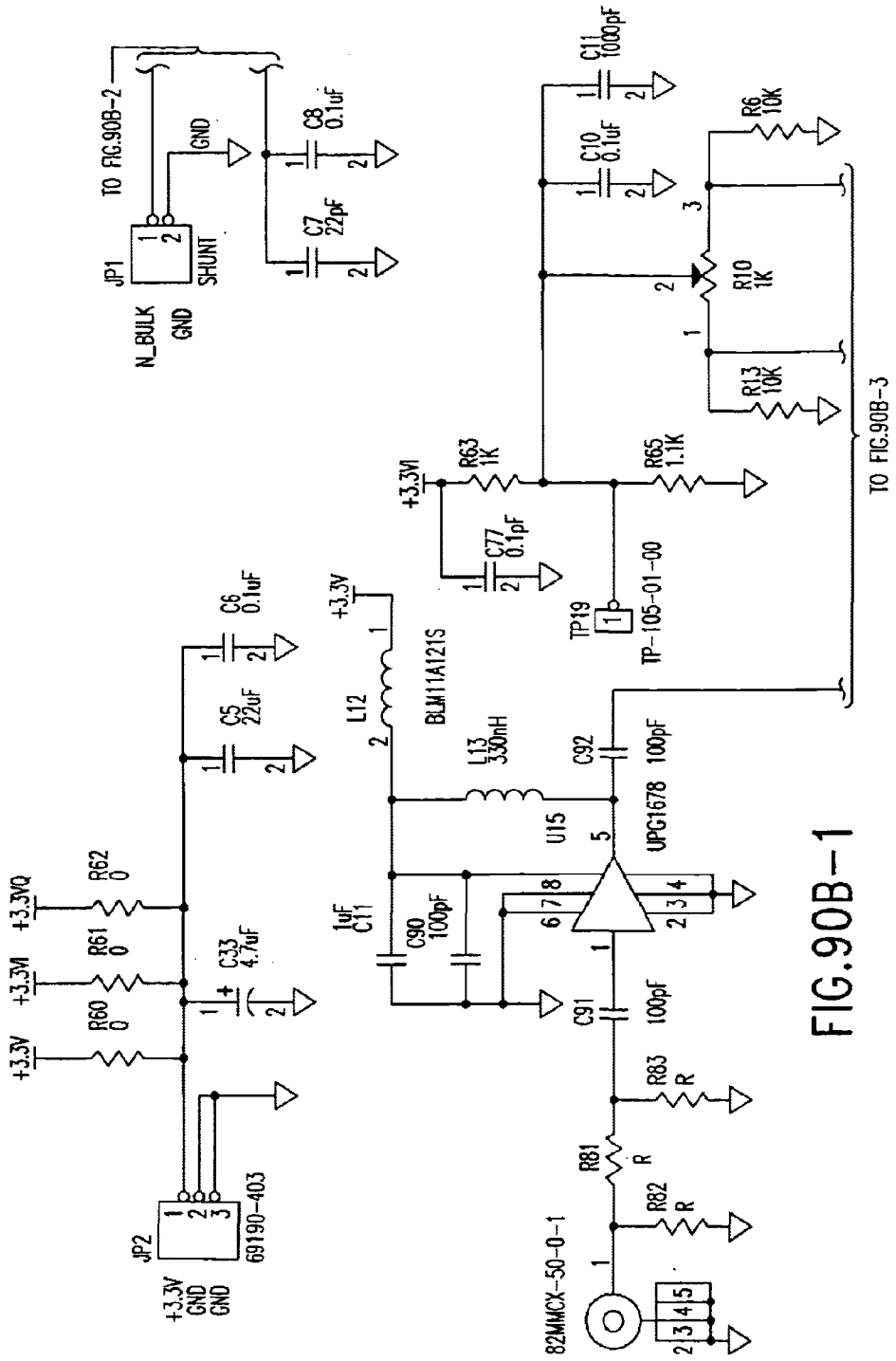
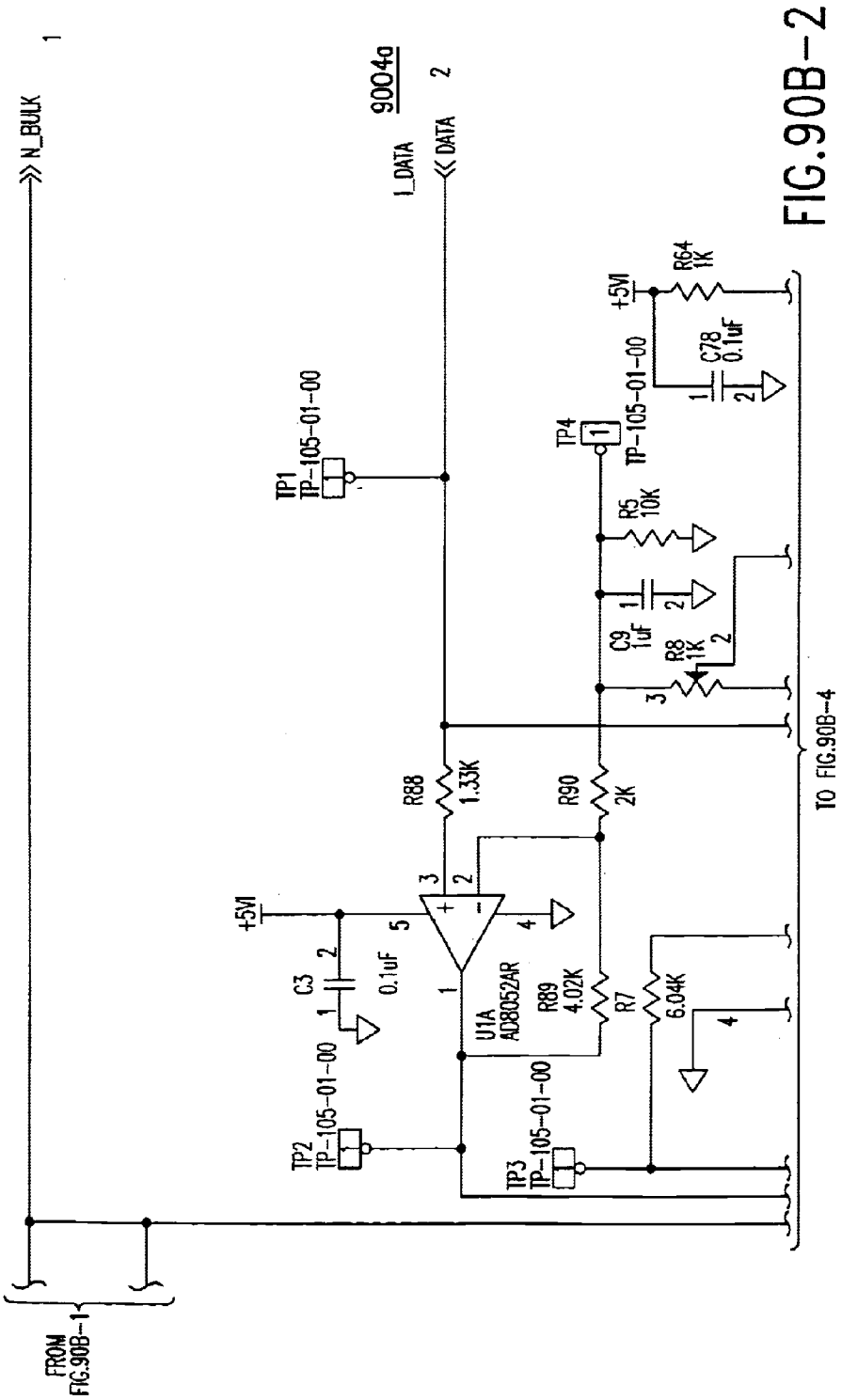

TO FIG.90B-2
JP1
SHUNT
N_BULK
GND
GND
C8 0.1uF
C7 22pF
C11 1000pF
C10 0.1uF
R6 10K
R10 1K
R13 10K
TO FIG.90B-3
+3.3VI
R63 1K
R65 1.1K
C77 0.1pF
TP19
TP-105-01-00
C6 0.1uF
C5 22uF
+3.3V
L12
BLM11A121S
L13 330nH
C92 100pF
U15
UPG1678
R62 0
R61 0
R60 0
+3.3VQ
+3.3M
+3.3V
C33 4.7uF
C11 1uF
C90 100pF
C91 100pF
R83 R
R81 R
R82 R
JP2
69190-403
+3.3V
GND
GND
82MMCX-50-0-1

FIG.90B-1


FIG.90B-2
90040
N_BULK
I_DATA
DATA
TP1
TP-105-01-00
TP2
TP-105-01-00
TP3
TP-105-01-00
TP4
TP-105-01-00
+5VI
C3
0.1uF
C78
0.1uF
C9
1uF
R64
1K
R5
10K
R8
1K
R88
1.33K
R90
2K
R89
4.02K
R7
6.04K
U1A
AD8052AR
FROM FIG.90B-1
TO FIG.90B-4

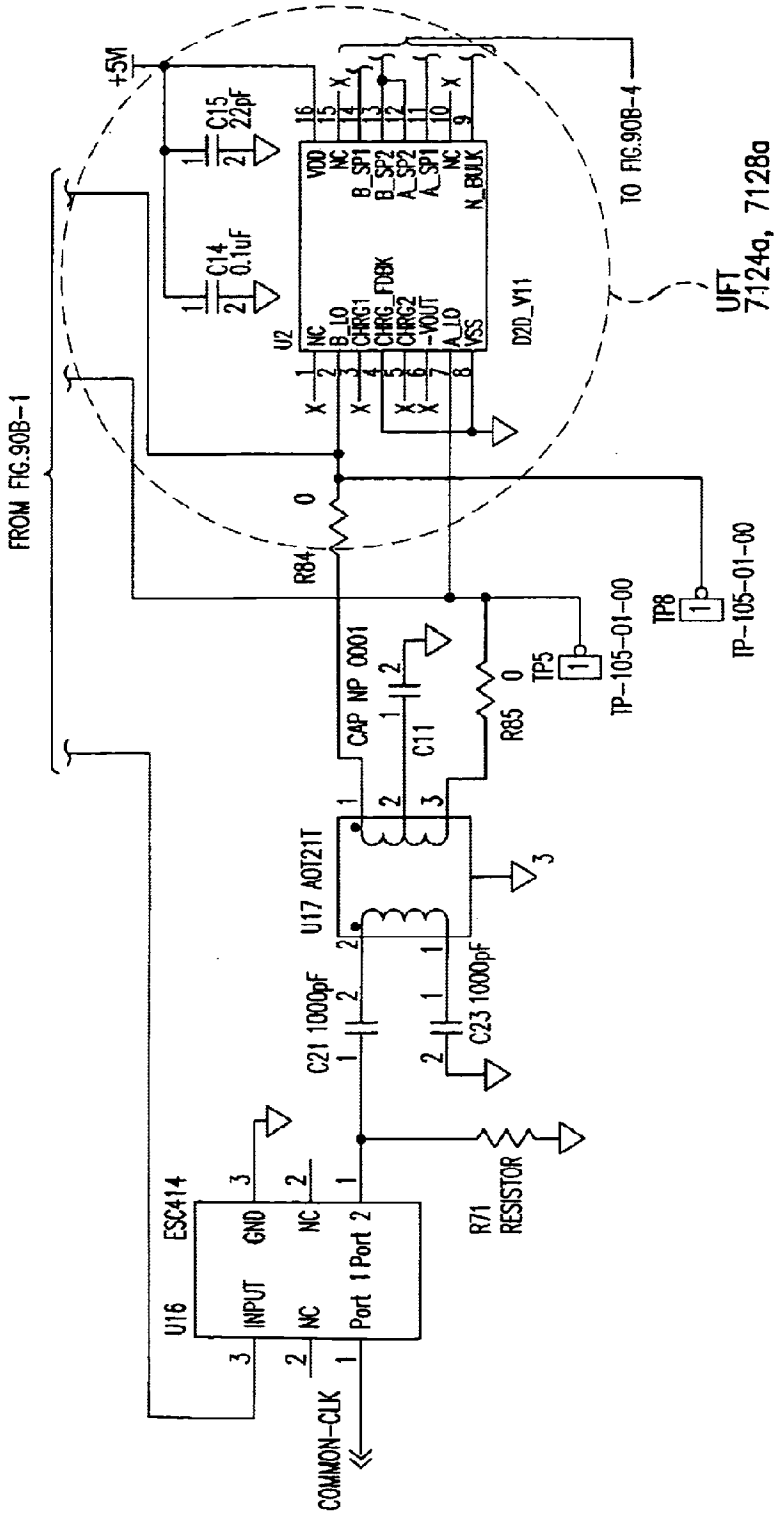

+5M
C15 22pF
C14 0.1uF
U2
D2D_V11
VDD
NC
B_SP1
B_SP2
A_SP1
NC
N_BULK
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
TO FIG.90B-4
UFT 7124a, 7128a
FROM FIG.90B-1
R84 0
TP8
TP-105-01-00
TP5
TP-105-01-00
R85 0
CAP NP 0001
C11
U17 A0T21T
C21 1000pF
C23 1000pF
R71 RESISTOR
U16 ESC414
INPUT
GND
NC
NC
Port 1
Port 2
COMMON-CLK

FIG.90B-3

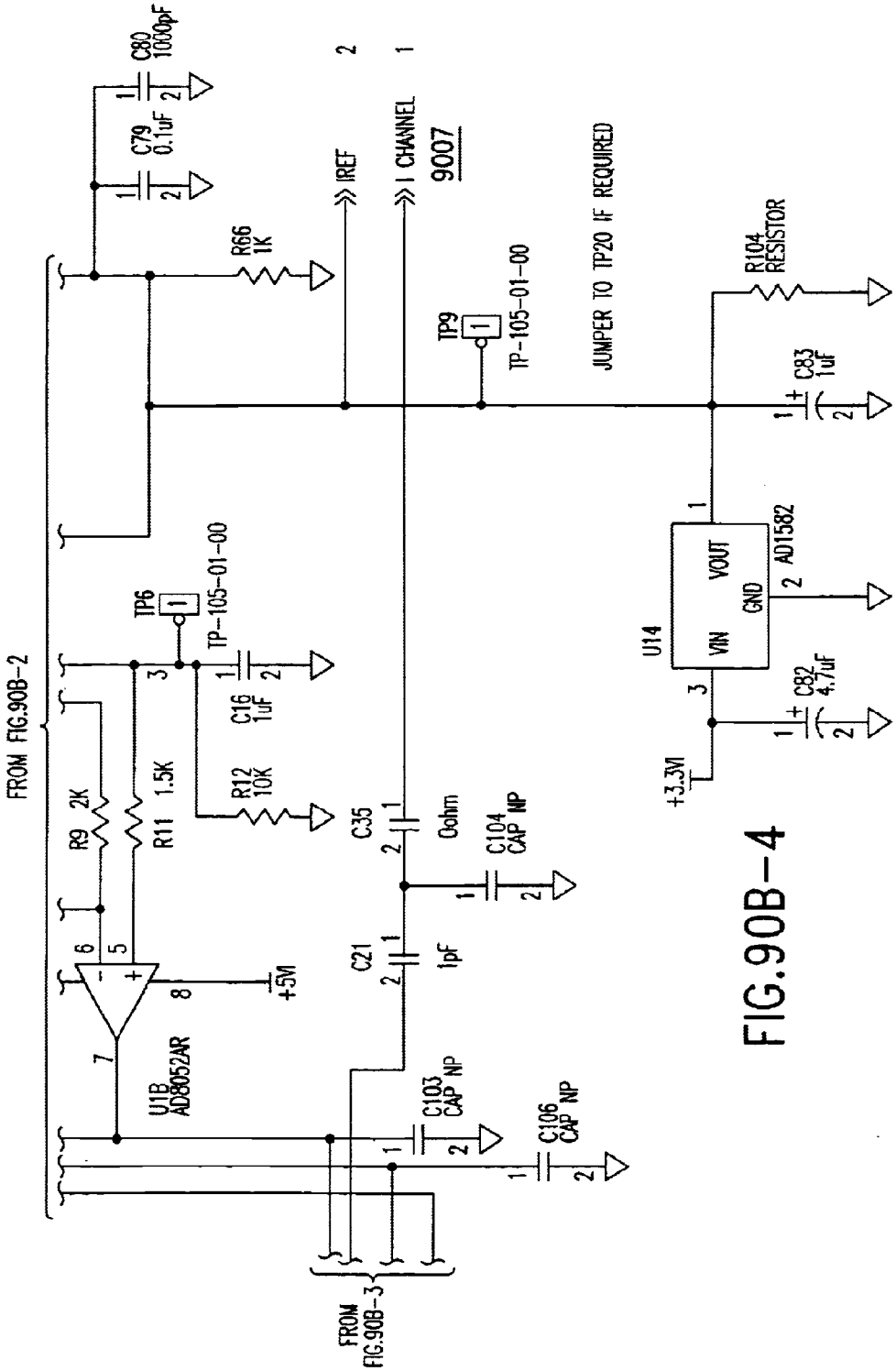

C80 1000pF
C79 0.1uF
R66 1K
IREF
I CHANNEL
9007
JUMPER TO TP20 IF REQUIRED
R104 RESISTOR
TP9
TP-105-01-00
C83 1uF
U14
VIN
VOUT
GND
AD1582
C82 4.7uF
+3.3VI
TP6
TP-105-01-00
C16 1uF
R12 10K
FROM FIG.90B-2
R9 2K
R11 1.5K
C35 0ohm
C104 CAP NP
C21 1pF
+5V
U1B AD8052AR
C103 CAP NP
C106 CAP NP
FROM FIG.90B-3

FIG.90B-4

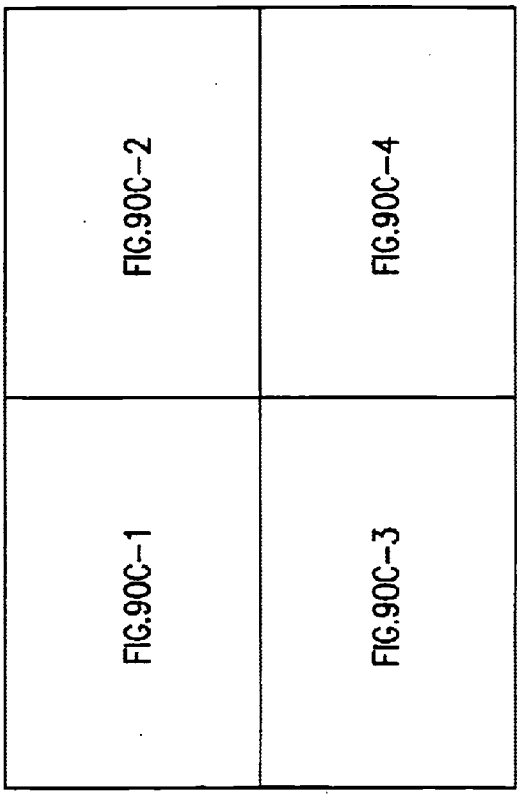


FIG.90C

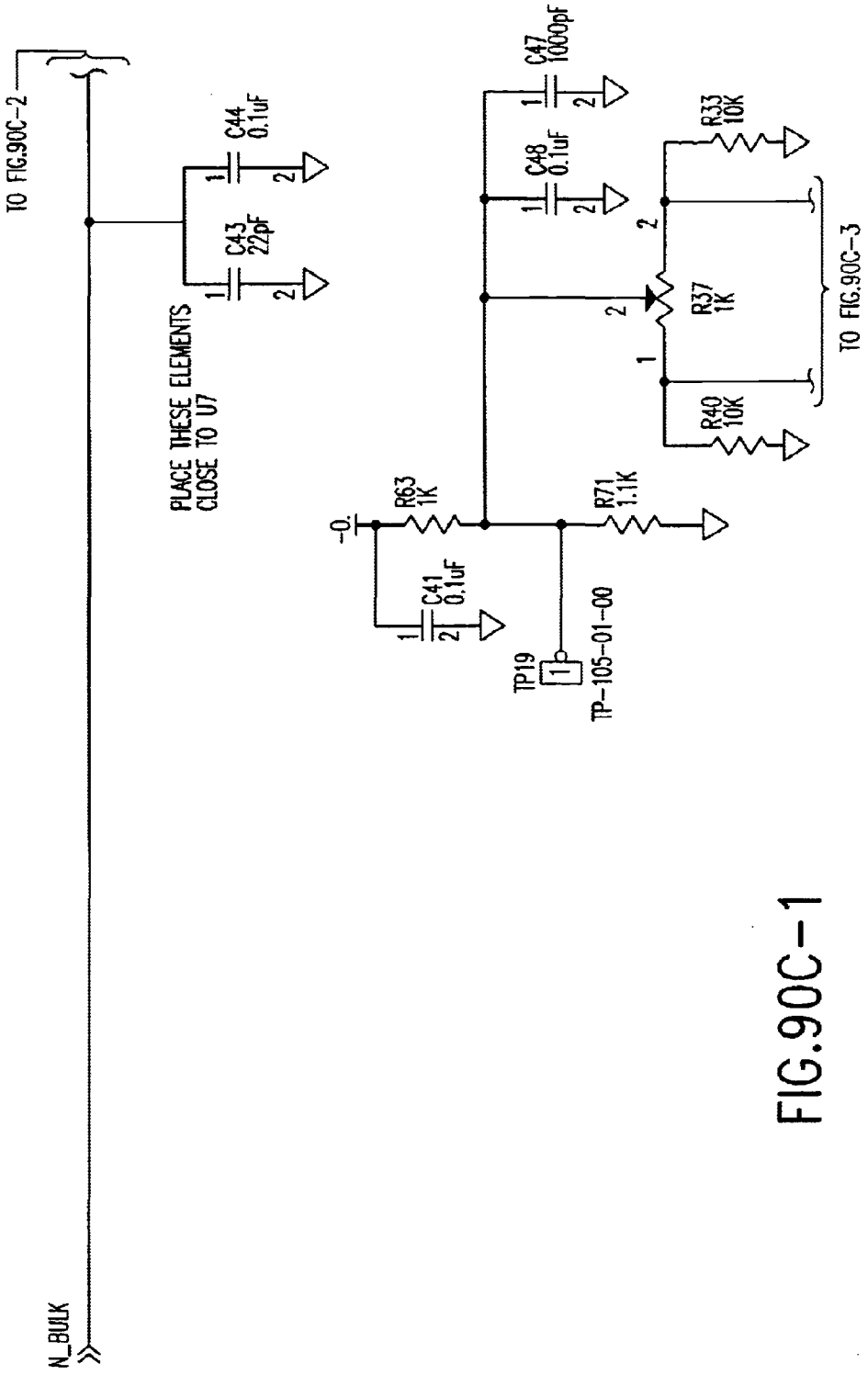
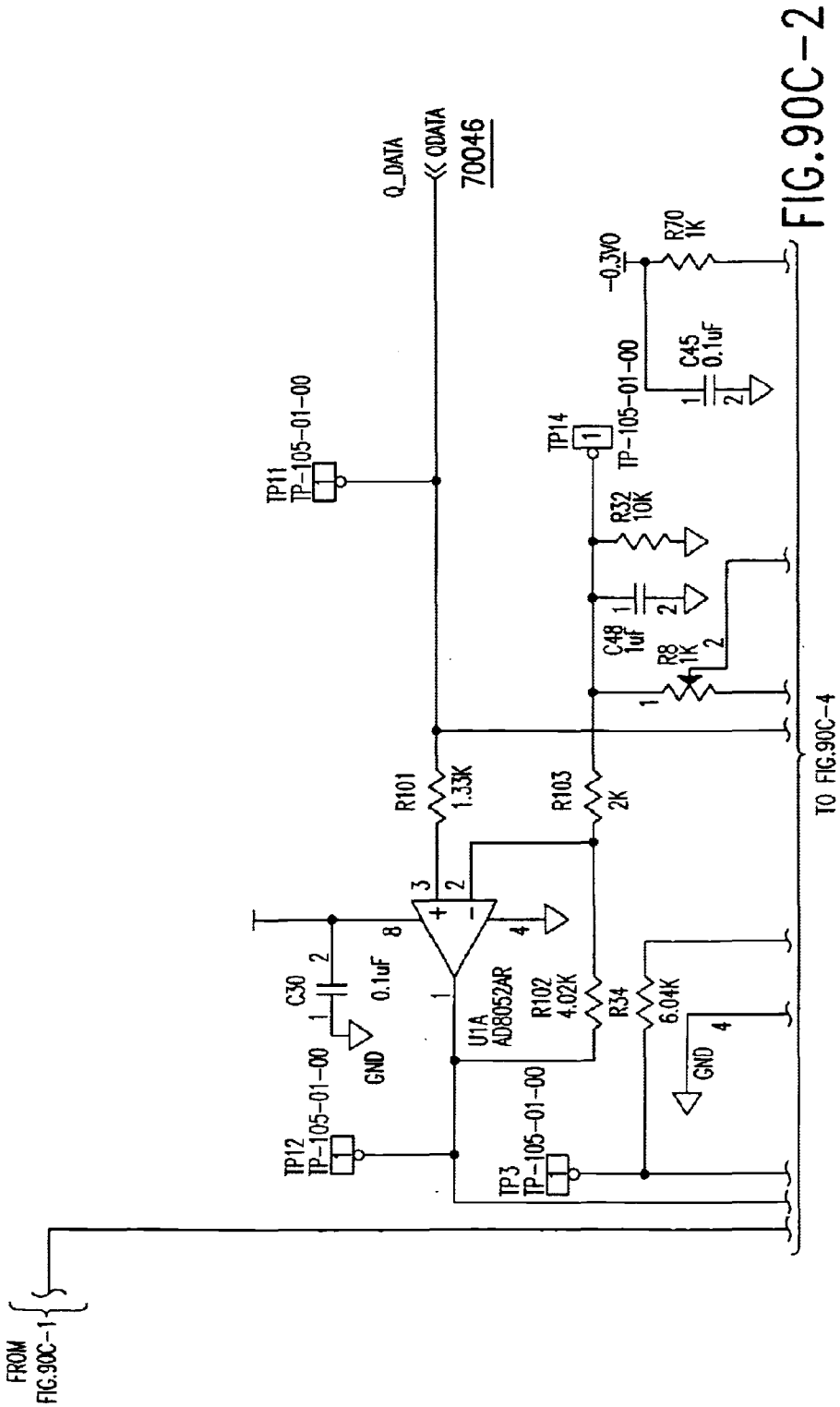

TO FIG.90C-2
C44 0.1uF
C43 22pF
PLACE THESE ELEMENTS CLOSE TO U7
C47 1000pF
C48 0.1uF
R33 10K
R37 1K
R40 10K
TO FIG.90C-3
R63 1K
R71 1.1K
C41 0.1uF
TP19
TP-105-01-00
N_BULK

FIG.90C-1


FIG.90C-2
Q_DATA
<< QDATA
70046
TP11
TP-105-01-00
TP14
TP-105-01-00
-0.3VO
R70
1K
C45
0.1uF
R32
10K
C48
1uF
R8
1K
R101
1.33K
R103
2K
C30
0.1uF
U1A
AD8052AR
R102
4.02K
R34
6.04K
GND
GND
TP12
TP-105-01-00
TP3
TP-105-01-00
TO FIG.90C-4
FROM
FIG.90C-1

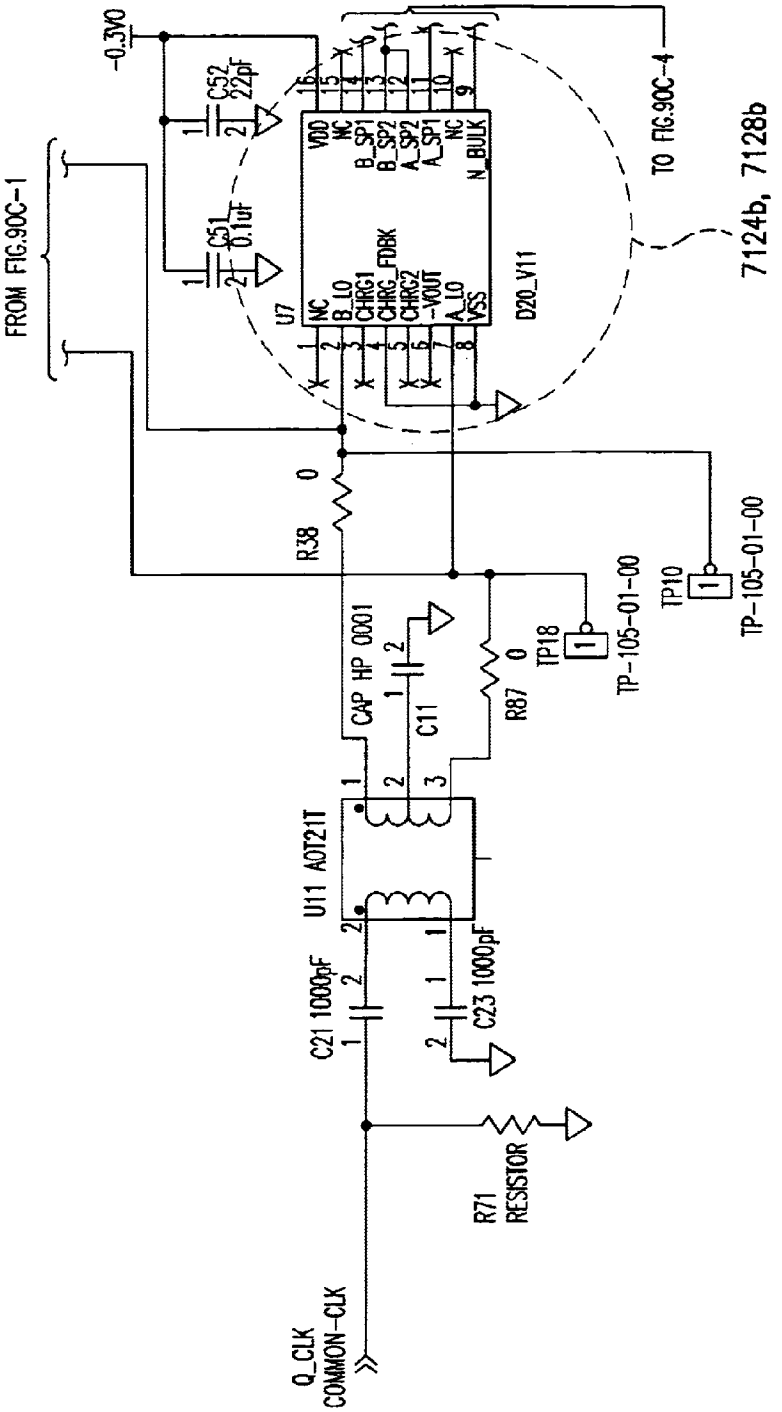

FROM FIG.90C-1
-0_3V0
C52 22pF
C51 0.1uF
U7
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
NC
B_SP1
B_SP2
A_SP1
NC
N_BULK
D20_V11
TO FIG.90C-4
7124b, 7128b
R38 0
CAP HP 0001
C11
R87 0
TP18
TP-105-01-00
TP10
TP-105-01-00
U11 A0T21T
C21 1000pF
C23 1000pF
R71 RESISTOR
Q_CLK
COMMON-CLK

FIG.90C-3

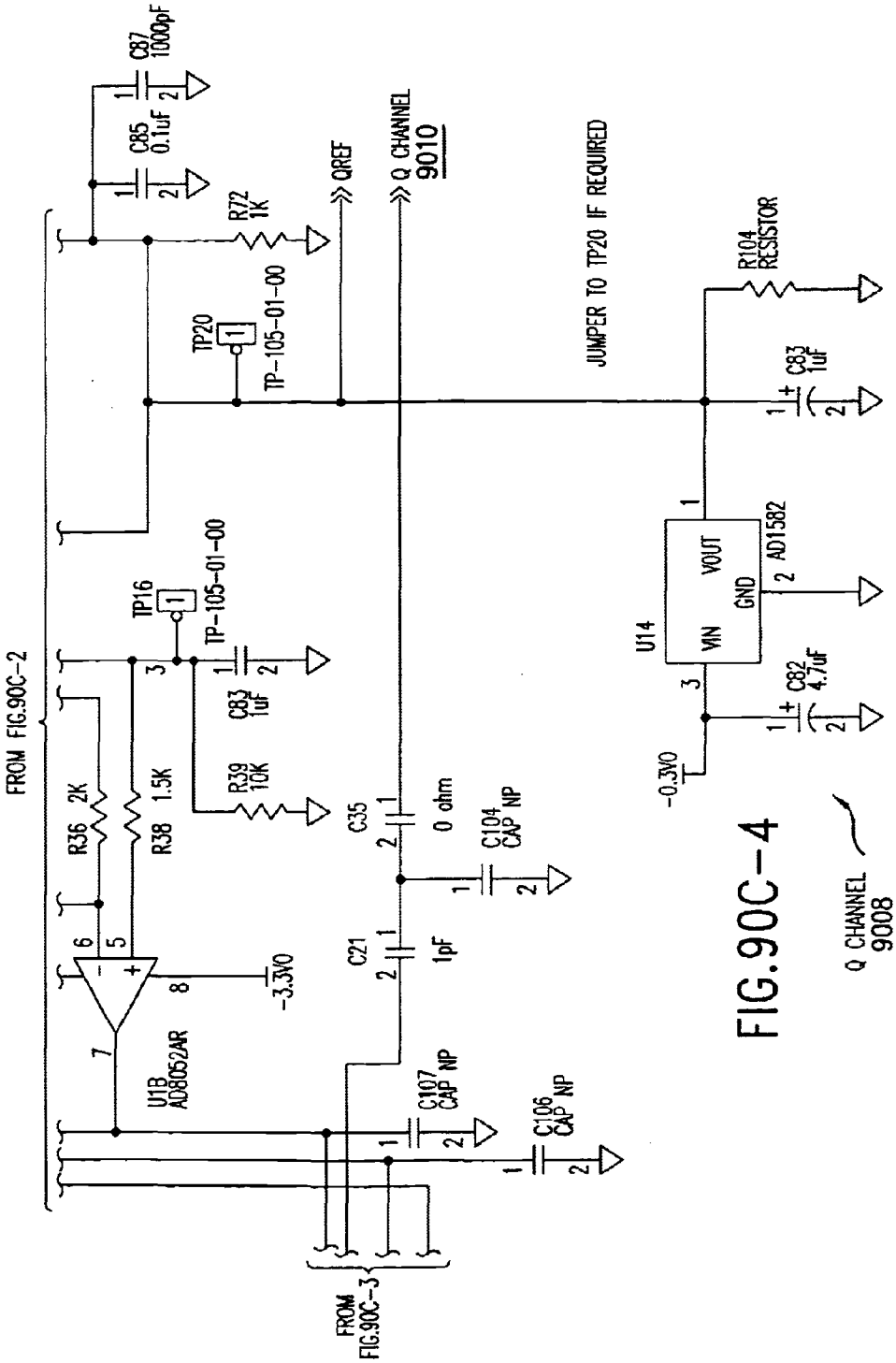

FROM FIG.90C-2
C87 1000pF
C85 0.1uF
R72 1K
QREF
Q CHANNEL 9010
JUMPER TO TP20 IF REQUIRED
R104 RESISTOR
TP20
TP-105-01-00
C83 1uF
TP16
TP-105-01-00
C83 1uF
U14
VIN
VOUT
GND
AD1582
C82 4.7uF
-0.3VO
R36 2K
R38 1.5K
R39 10K
C35 0 ohm
C104 CAP NP
C21 1pF
-3.3VO
U1B AD8052AR
C107 CAP NP
C106 CAP NP
FROM FIG.90C-3
Q CHANNEL 9008

FIG.90C-4

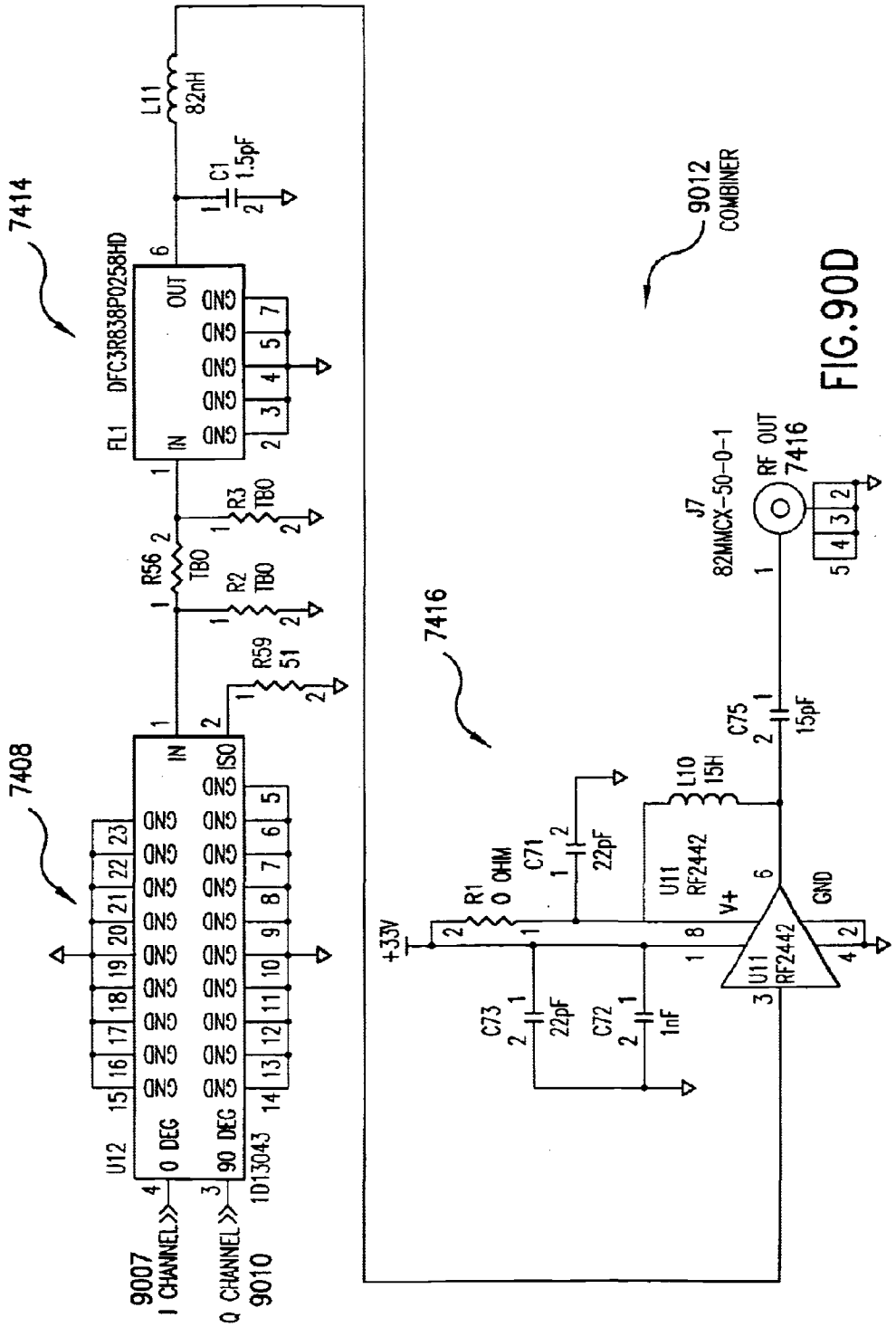

7414
DFC3R838P0258HD
FL1
IN
OUT
GND
L11
82nH
C1
1.5pF
R56
TBO
R3
TBO
R2
TBO
R59
51
7408
U12
1D13043
0 DEG
90 DEG
IN
ISO
9007
I CHANNEL
9010
Q CHANNEL
7416
9012
COMBINER
J7
82MMCX-50-0-1
RF OUT
7416
R1
0 OHM
C71
22pF
C73
22pF
C72
1nF
L10
15H
C75
15pF
U11
RF2442
V+
GND
+3.3V

FIG.90D

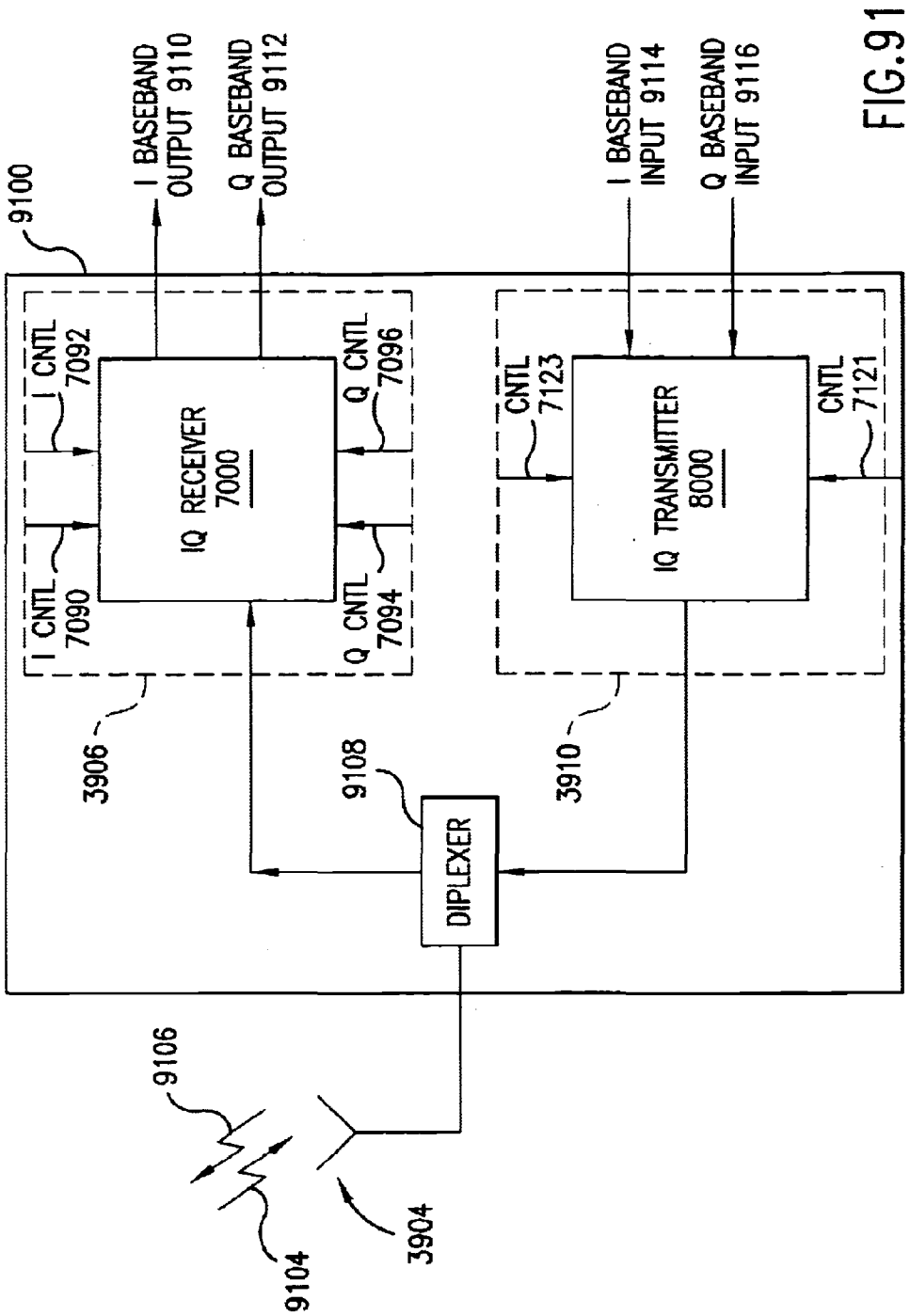

9100
I BASEBAND OUTPUT 9110
Q BASEBAND OUTPUT 9112
I BASEBAND INPUT 9114
Q BASEBAND INPUT 9116
I CNTL 7092
Q CNTL 7096
IQ RECEIVER 7000
I CNTL 7090
Q CNTL 7094
CNTL 7123
CNTL 7121
IQ TRANSMITTER 8000
3906
9108
3910
DIPLEXER
9106
9104
3904

FIG.91

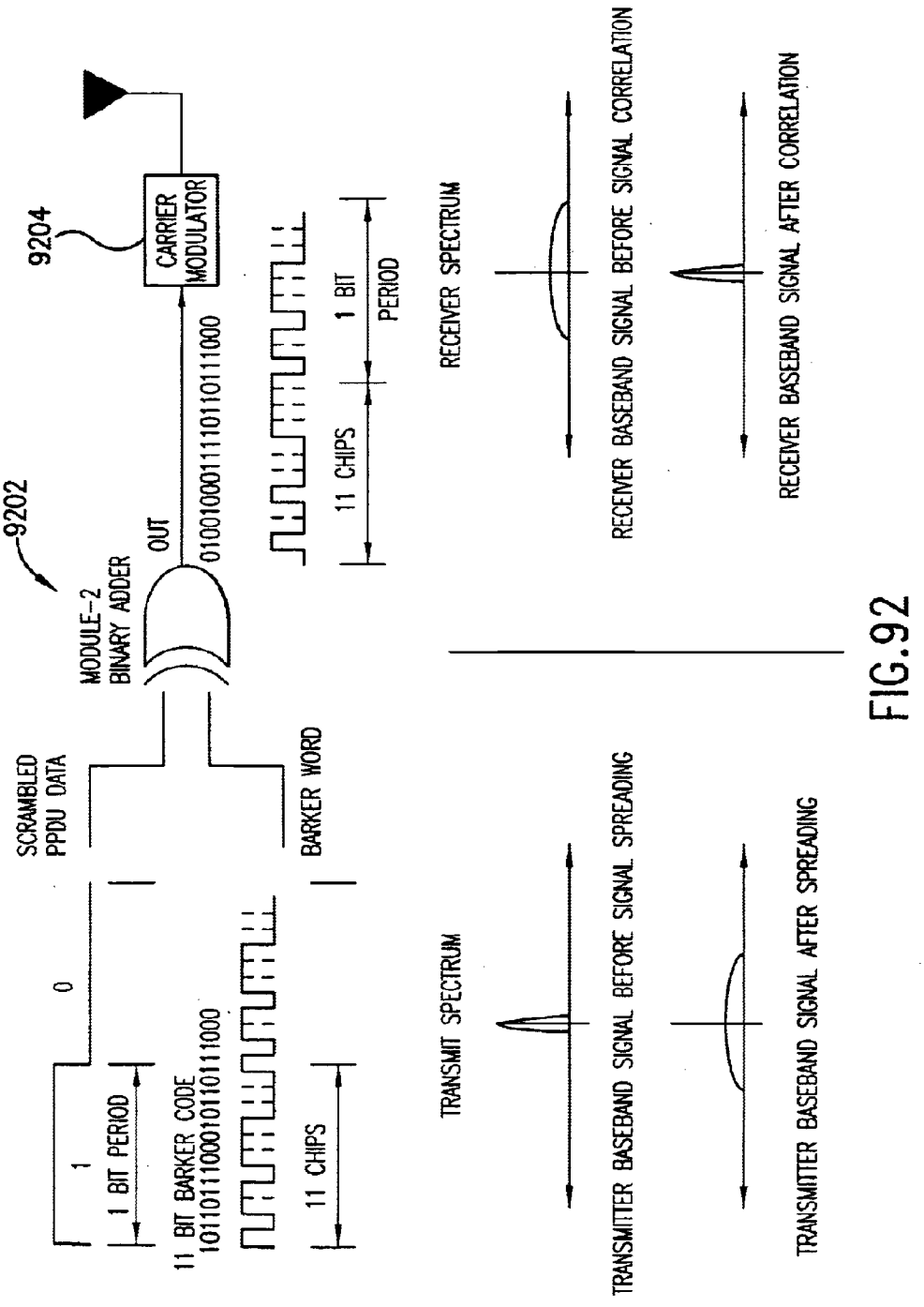

9202
MODULE-2 BINARY ADDER
OUT
01001000111101101110000
9204
CARRIER MODULATOR
SCRAMBLED PPDU DATA
0
1
1 BIT PERIOD
11 BIT BARKER CODE
10110111000101101110000
11 CHIPS
BARKER WORD
11 CHIPS
1 BIT PERIOD
RECEIVER SPECTRUM
RECEIVER BASEBAND SIGNAL BEFORE SIGNAL CORRELATION
RECEIVER BASEBAND SIGNAL AFTER CORRELATION
TRANSMIT SPECTRUM
TRANSMITTER BASEBAND SIGNAL BEFORE SIGNAL SPREADING
TRANSMITTER BASEBAND SIGNAL AFTER SPREADING

FIG.92

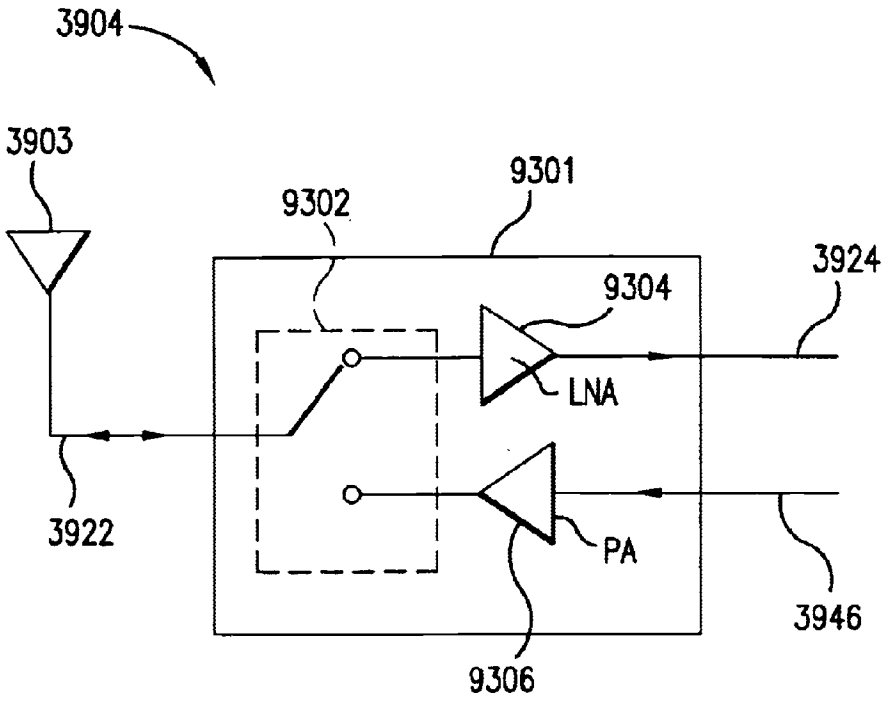


FIG.93

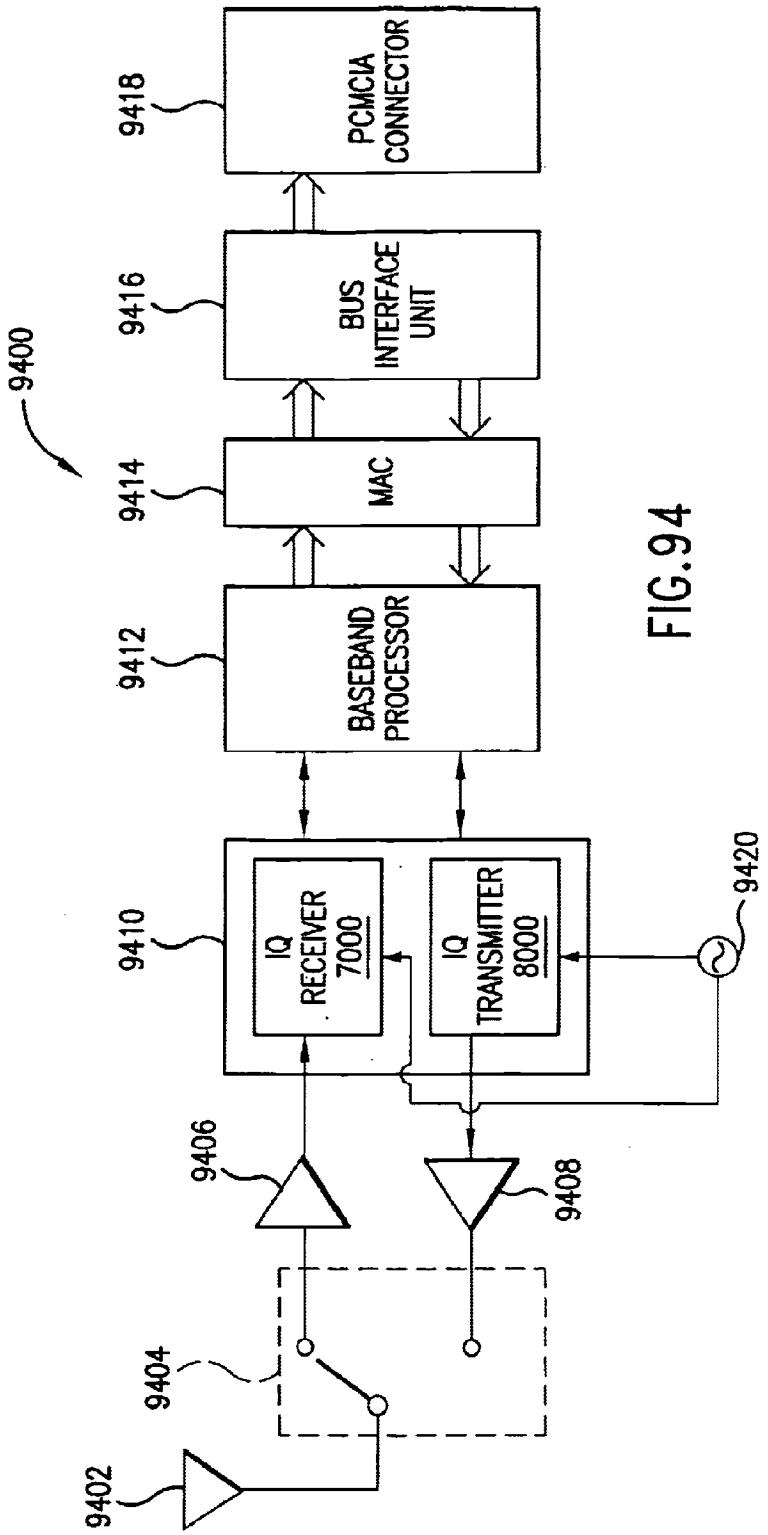

9400
9418
PCMCIA CONNECTOR
9416
BUS INTERFACE UNIT
9414
MAC
9412
BASEBAND PROCESSOR
9410
IQ RECEIVER 7000
IQ TRANSMITTER 8000
9420
9406
9408
9404
9402

FIG.94

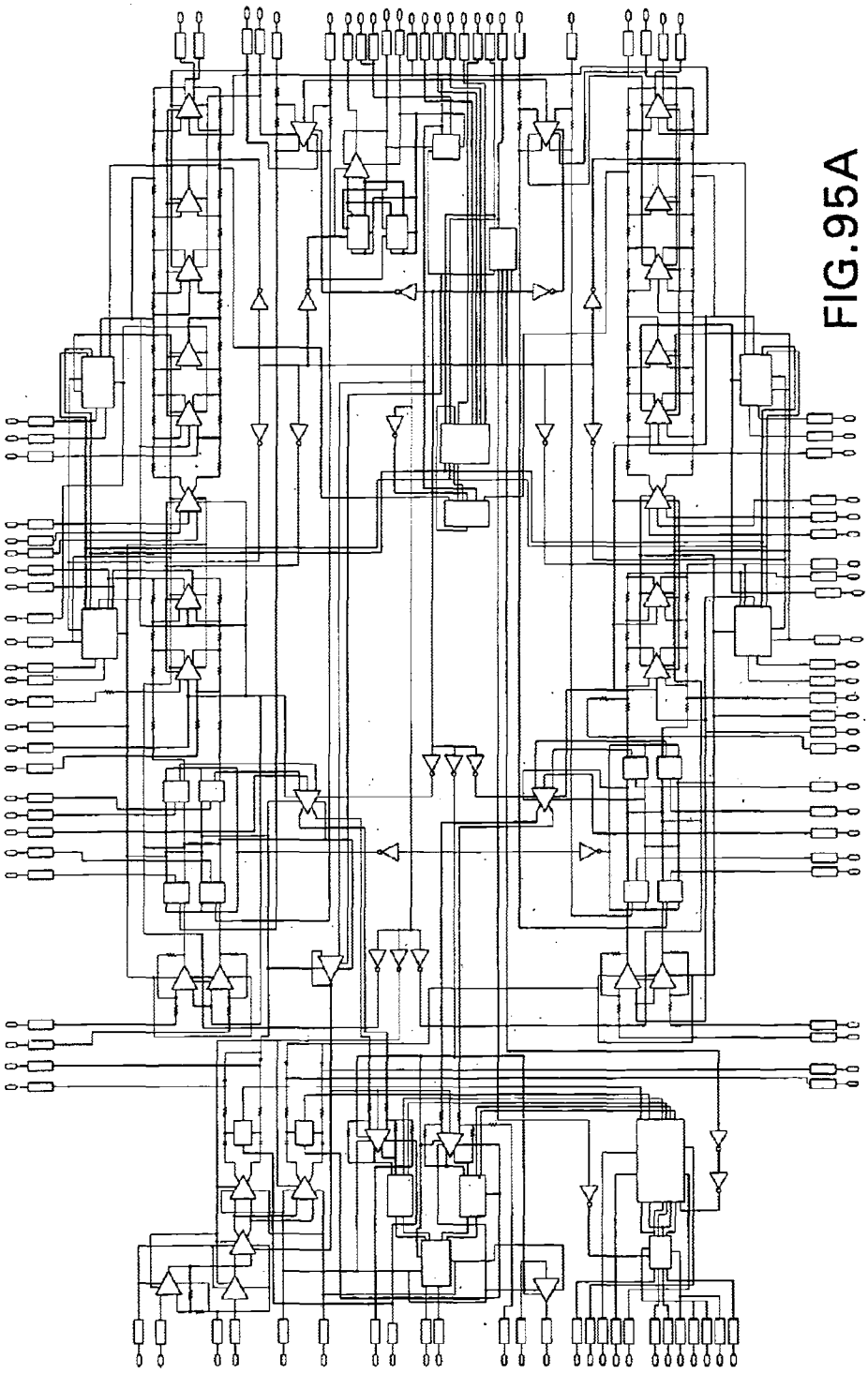


FIG.95A

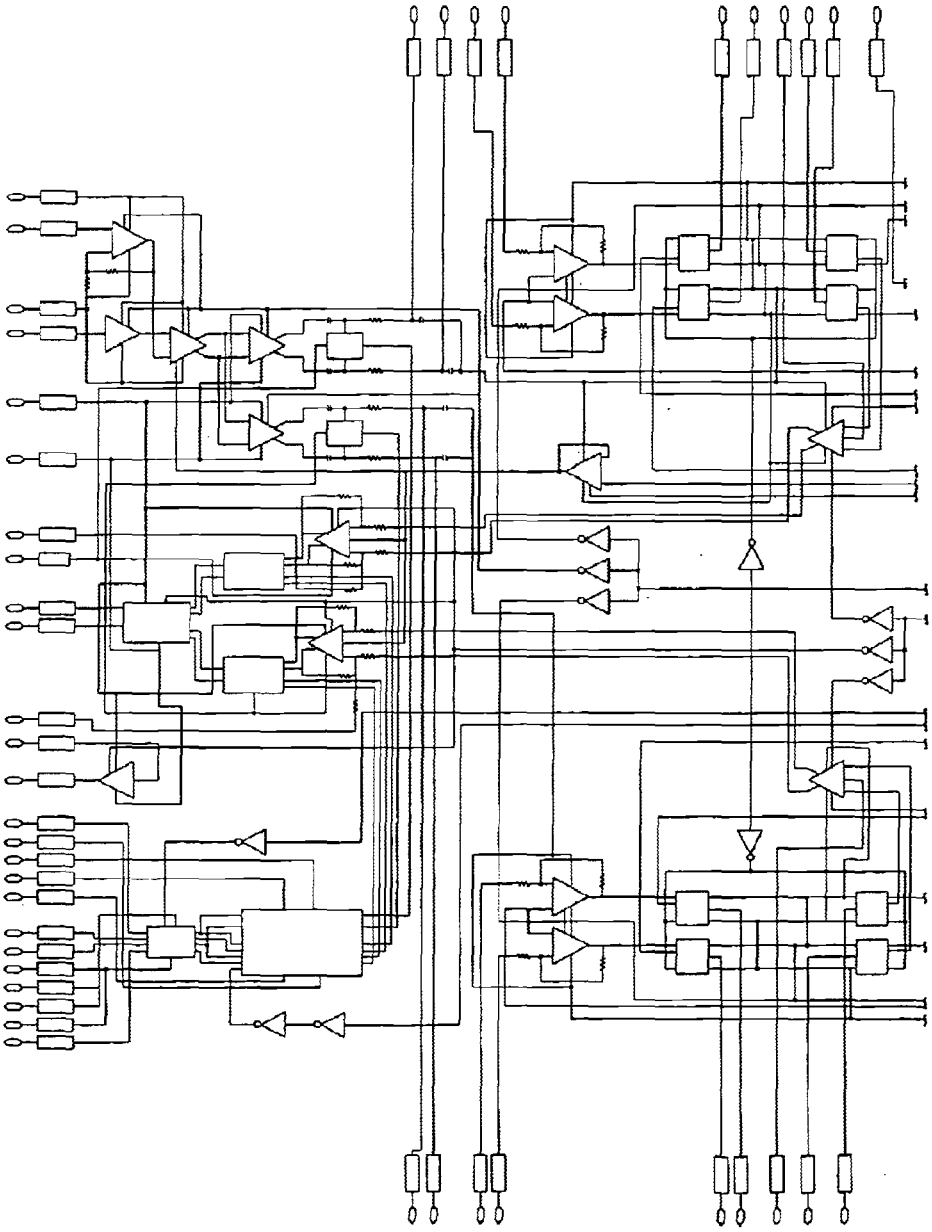


FIG.95B

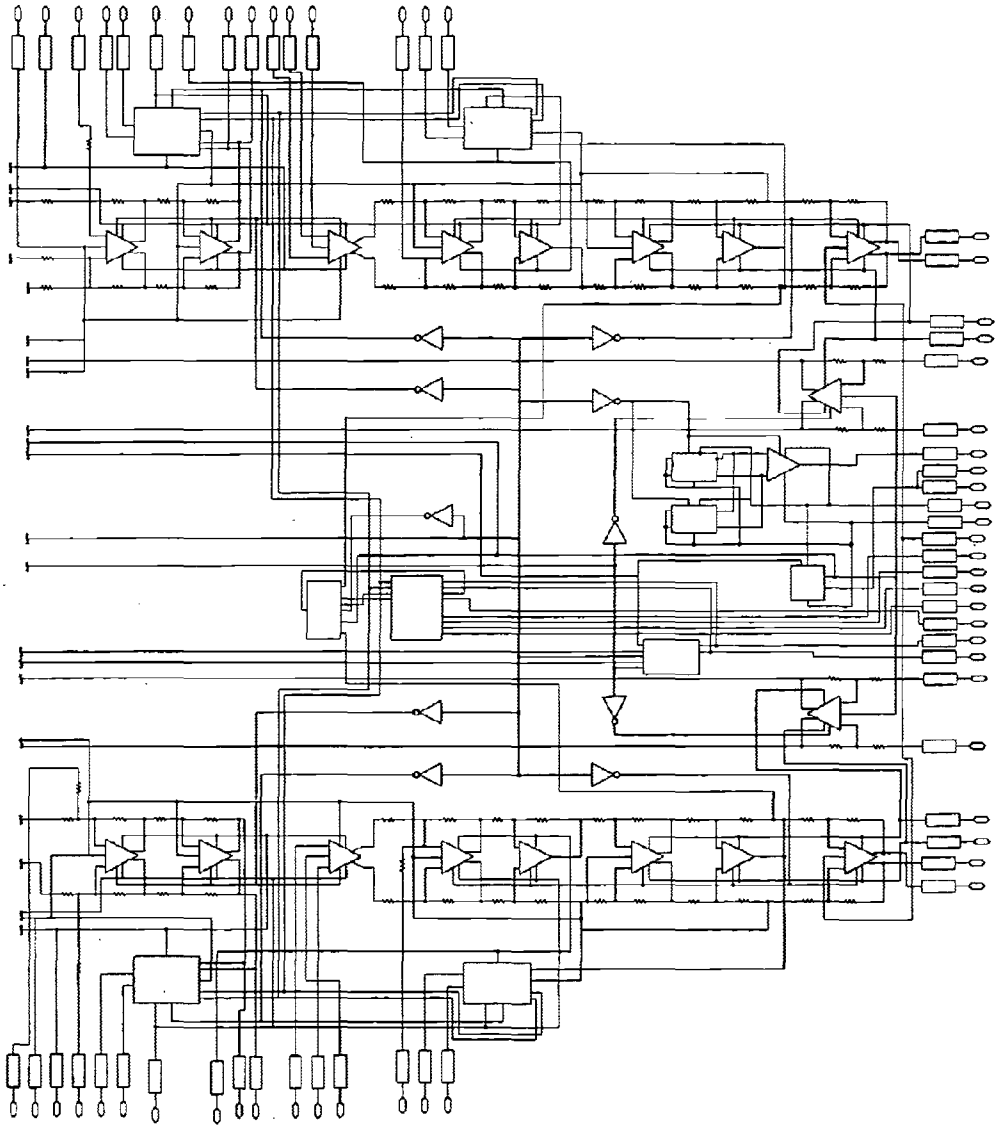


FIG.95C

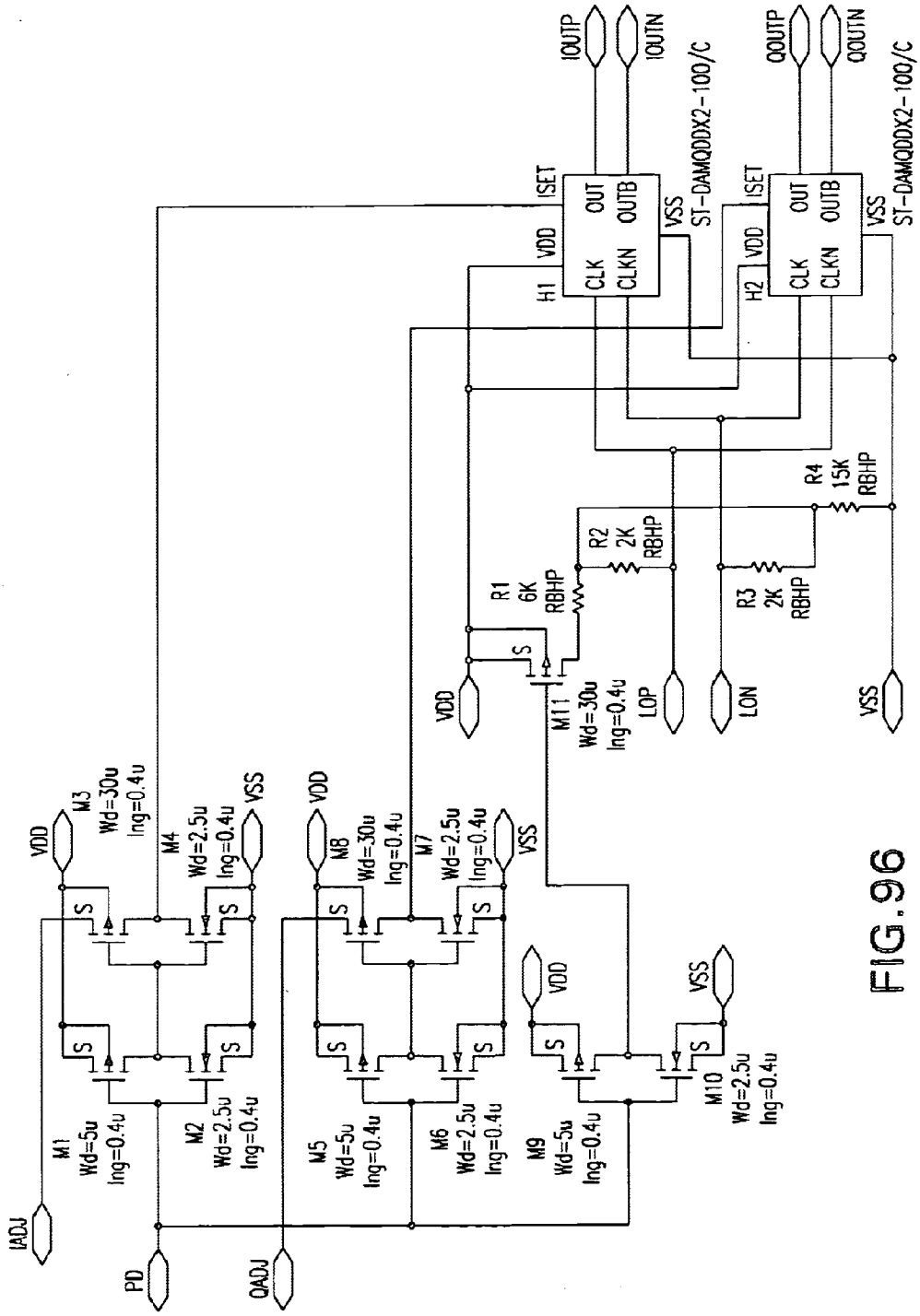

IOUTP
IOUTN
QOUTP
QOUTN
ISET
OUT
OUTB
VSS
ST-DAMQDDX2-100/C
VDD
CLK
CLKN
H1
H2
R1 6K RBHP
R2 2K RBHP
R3 2K RBHP
R4 15K RBHP
M11 Wd=30u lng=0.4u
LOP
LON
M1 Wd=5u lng=0.4u
M2 Wd=2.5u lng=0.4u
M3 Wd=30u lng=0.4u
M4 Wd=2.5u lng=0.4u
M5 Wd=5u lng=0.4u
M6 Wd=2.5u lng=0.4u
M7 Wd=2.5u lng=0.4u
M8 Wd=30u lng=0.4u
M9 Wd=5u lng=0.4u
M10 Wd=2.5u lng=0.4u
IADJ
QADJ
PD

FIG. 96

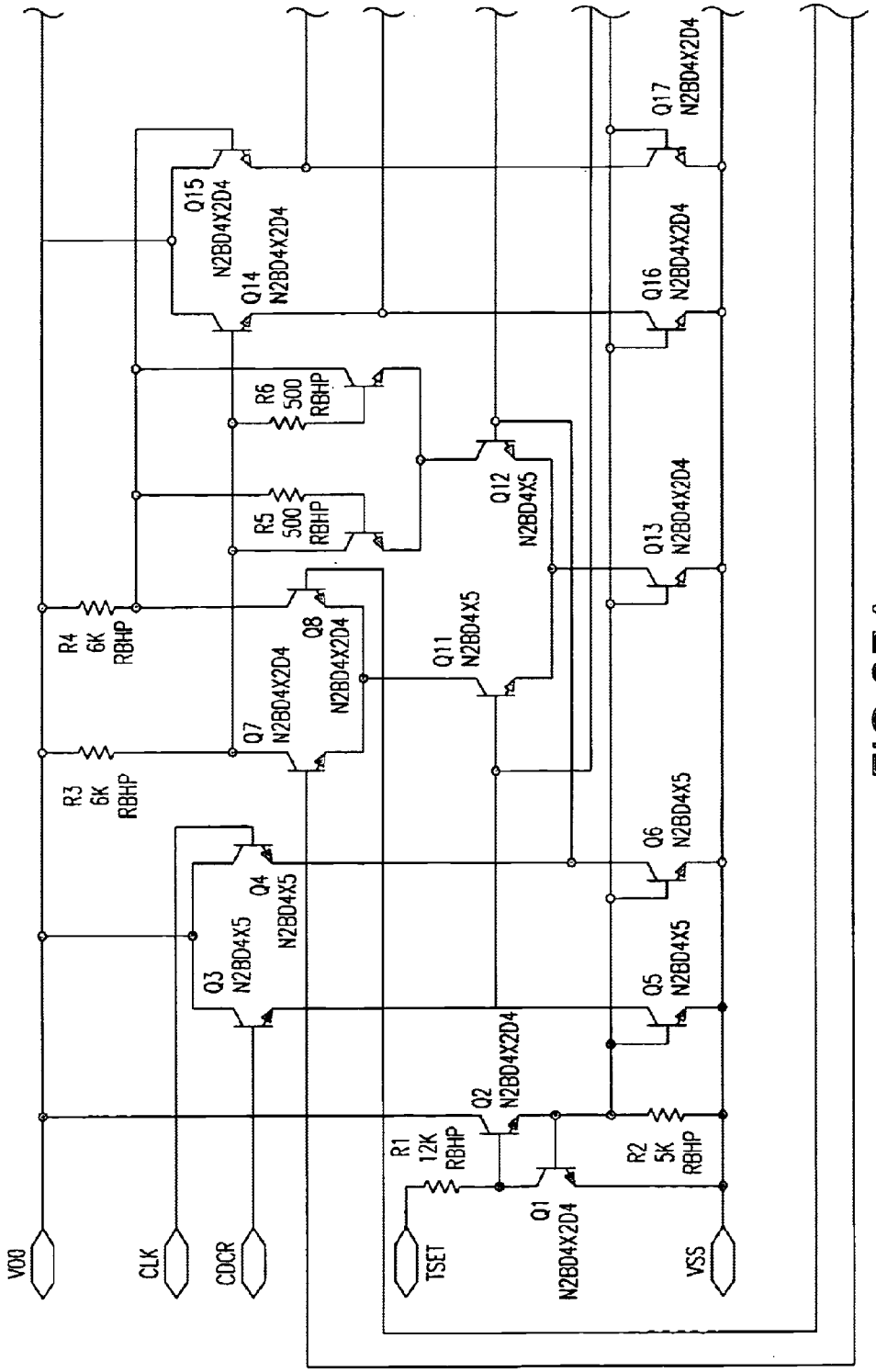

VDD
CLK
CDCR
TSET
VSS
Q1 N2BD4X2D4
Q2 N2BD4X2D4
Q3 N2BD4X5
Q4 N2BD4X5
Q5 N2BD4X5
Q6 N2BD4X5
Q7 N2BD4X2D4
Q8 N2BD4X2D4
Q11 N2BD4X5
Q12 N2BD4X5
Q13 N2BD4X2D4
Q14 N2BD4X2D4
Q15 N2BD4X2D4
Q16 N2BD4X2D4
Q17 N2BD4X2D4
R1 12K RBHP
R2 5K RBHP
R3 6K RBHP
R4 6K RBHP
R5 500 RBHP
R6 500 RBHP

FIG.97A

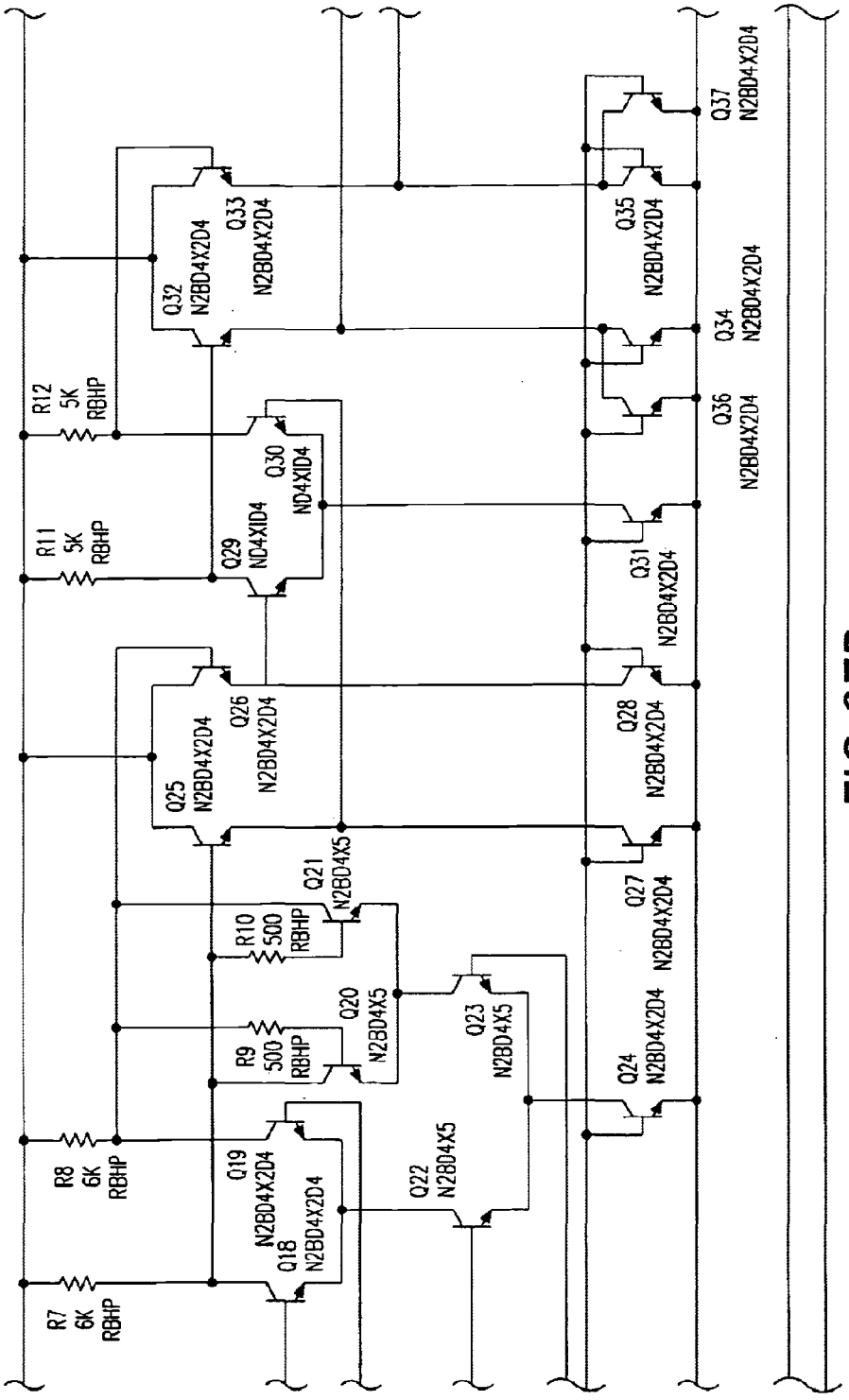

R12 5K RBHP
R11 5K RBHP
R8 6K RBHP
R7 6K RBHP
R10 500 RBHP
R9 500 RBHP
Q32 N2BD4X2D4
Q33 N2BD4X2D4
Q30 ND4XID4
Q29 ND4XID4
Q25 N2BD4X2D4
Q26 N2BD4X2D4
Q21 N2BD4X5
Q20 N2BD4X5
Q19 N2BD4X2D4
Q18 N2BD4X2D4
Q23 N2BD4X5
Q22 N2BD4X5
Q37 N2BD4X2D4
Q35 N2BD4X2D4
Q34 N2BD4X2D4
Q36 N2BD4X2D4
Q31 N2BD4X2D4
Q28 N2BD4X2D4
Q27 N2BD4X2D4
Q24 N2BD4X2D4

FIG.97B

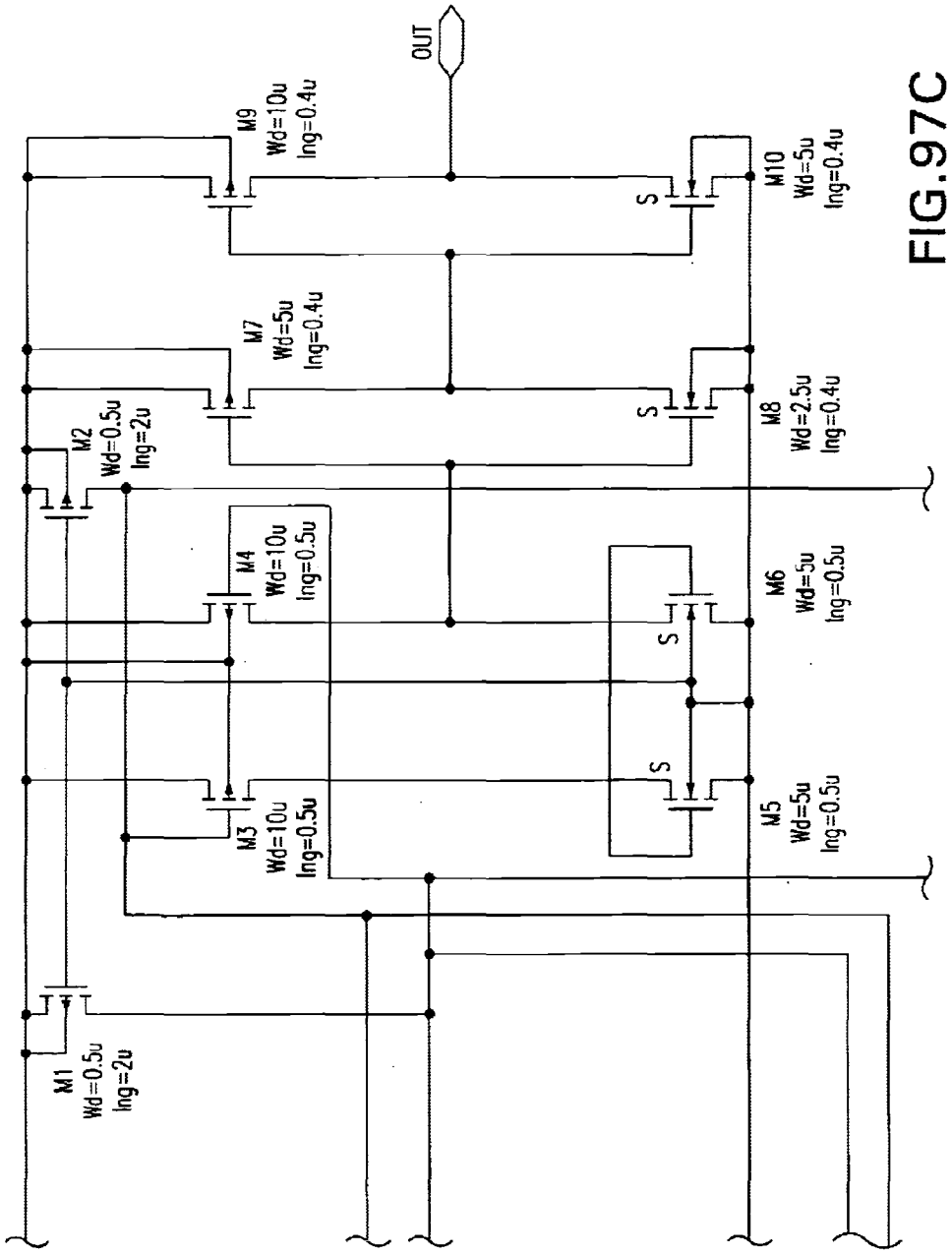

OUT
M9
Wd=10u
lng=0.4u
M10
Wd=5u
lng=0.4u
M7
Wd=5u
lng=0.4u
M8
Wd=2.5u
lng=0.4u
M2
Wd=0.5u
lng=2u
M4
Wd=10u
lng=0.5u
M6
Wd=5u
lng=0.5u
M3
Wd=10u
lng=0.5u
M5
Wd=5u
lng=0.5u
M1
Wd=0.5u
lng=2u

FIG.97C

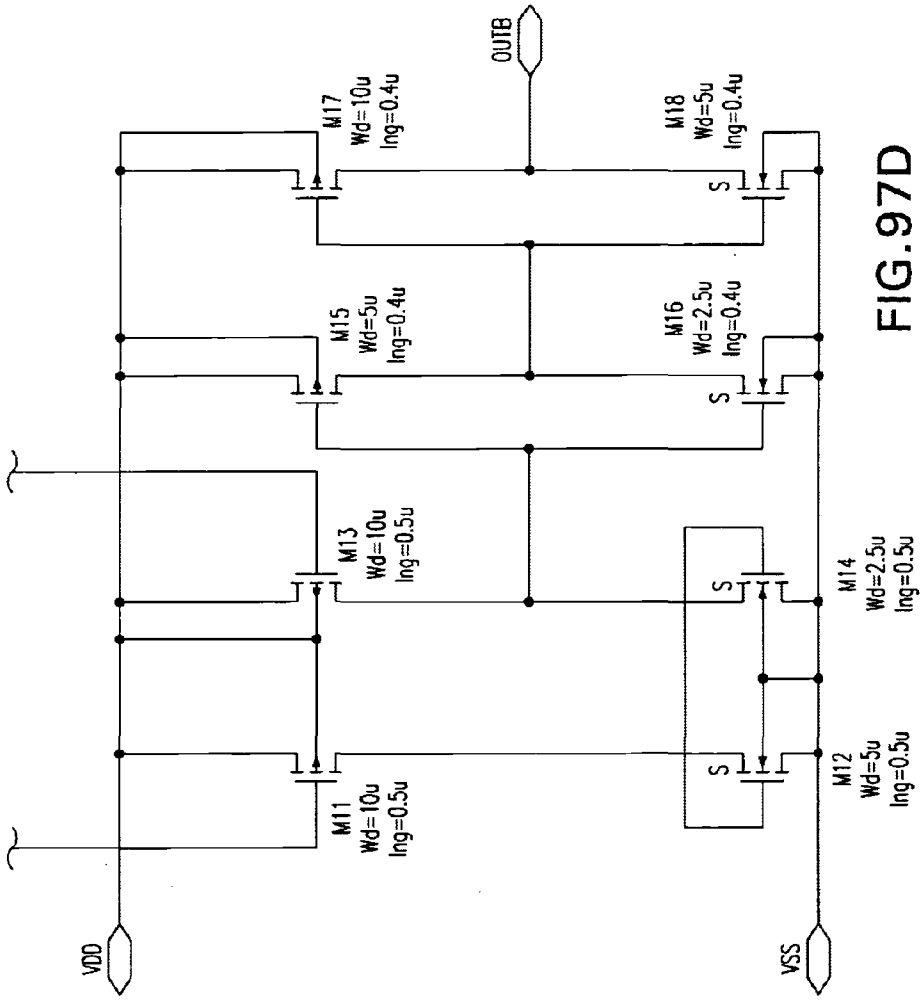

OUTB
M17
Wd=10u
lng=0.4u
M18
Wd=5u
lng=0.4u
M15
Wd=5u
lng=0.4u
M16
Wd=2.5u
lng=0.4u
M13
Wd=10u
lng=0.5u
M14
Wd=2.5u
lng=0.5u
M12
Wd=5u
lng=0.5u
M11
Wd=10u
lng=0.5u
VDD
VSS

FIG.97D

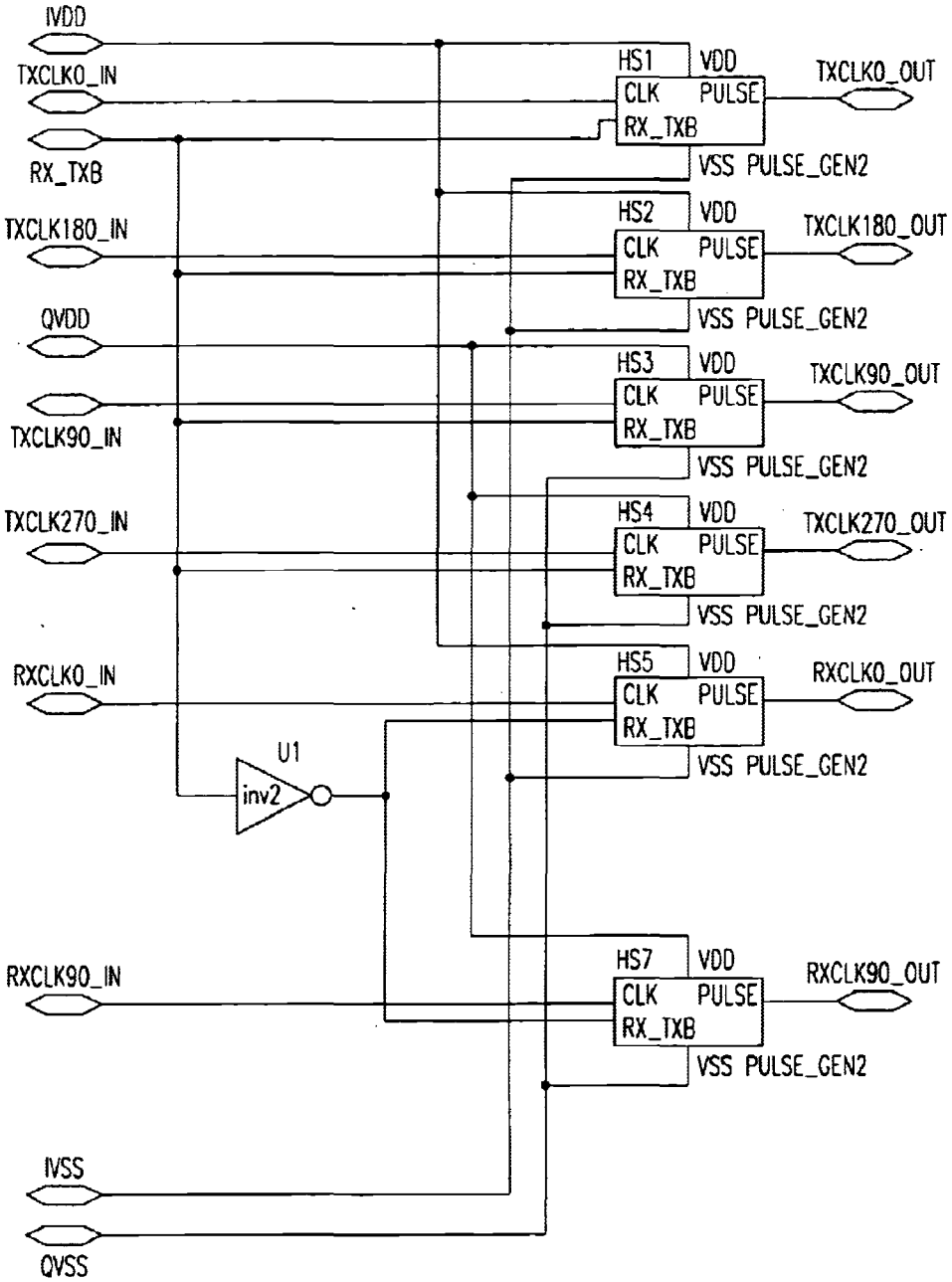

IVDD
TXCLK0_IN
RX_TXB
TXCLK180_IN
QVDD
TXCLK90_IN
TXCLK270_IN
RXCLK0_IN
RXCLK90_IN
IVSS
QVSS
U1
inv2
HS1
HS2
HS3
HS4
HS5
HS7
VDD
CLK
PULSE
RX_TXB
VSS PULSE_GEN2
TXCLK0_OUT
TXCLK180_OUT
TXCLK90_OUT
TXCLK270_OUT
RXCLK0_OUT
RXCLK90_OUT

FIG.98

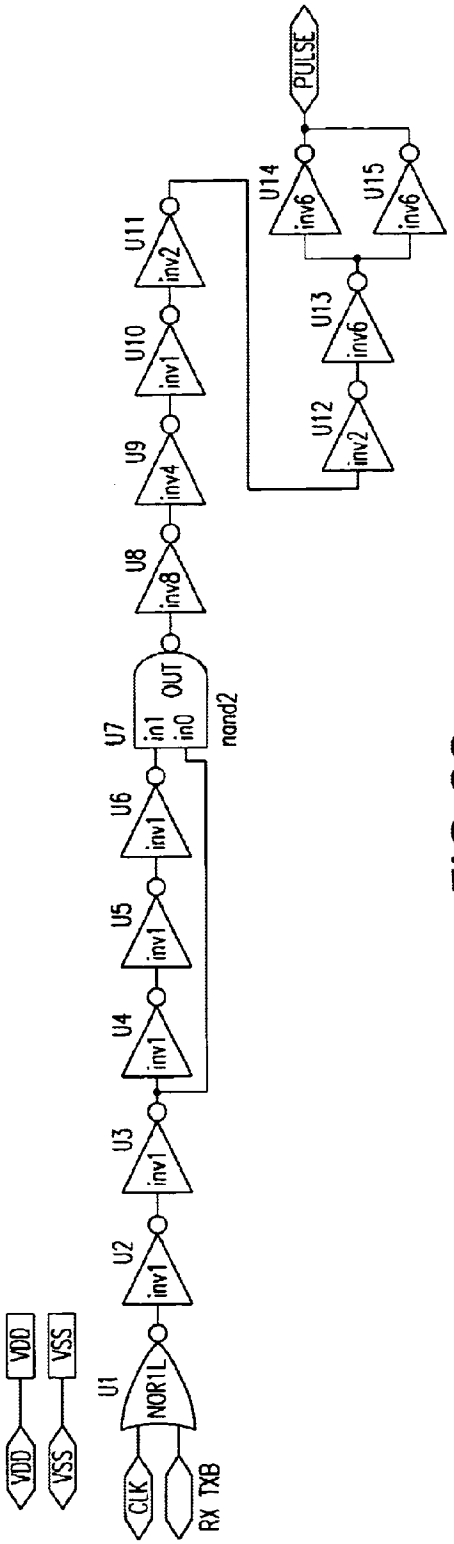

PULSE
U14
inv6
U15
inv6
U13
inv6
U12
inv2
U11
inv2
U10
inv1
U9
inv4
U8
inv8
U7
nand2
in1
in0
OUT
U6
inv1
U5
inv1
U4
inv1
U3
inv1
U2
inv1
U1
NOR1L
VDD
VSS
VDD
VSS
CLK
RX TXB

FIG.99

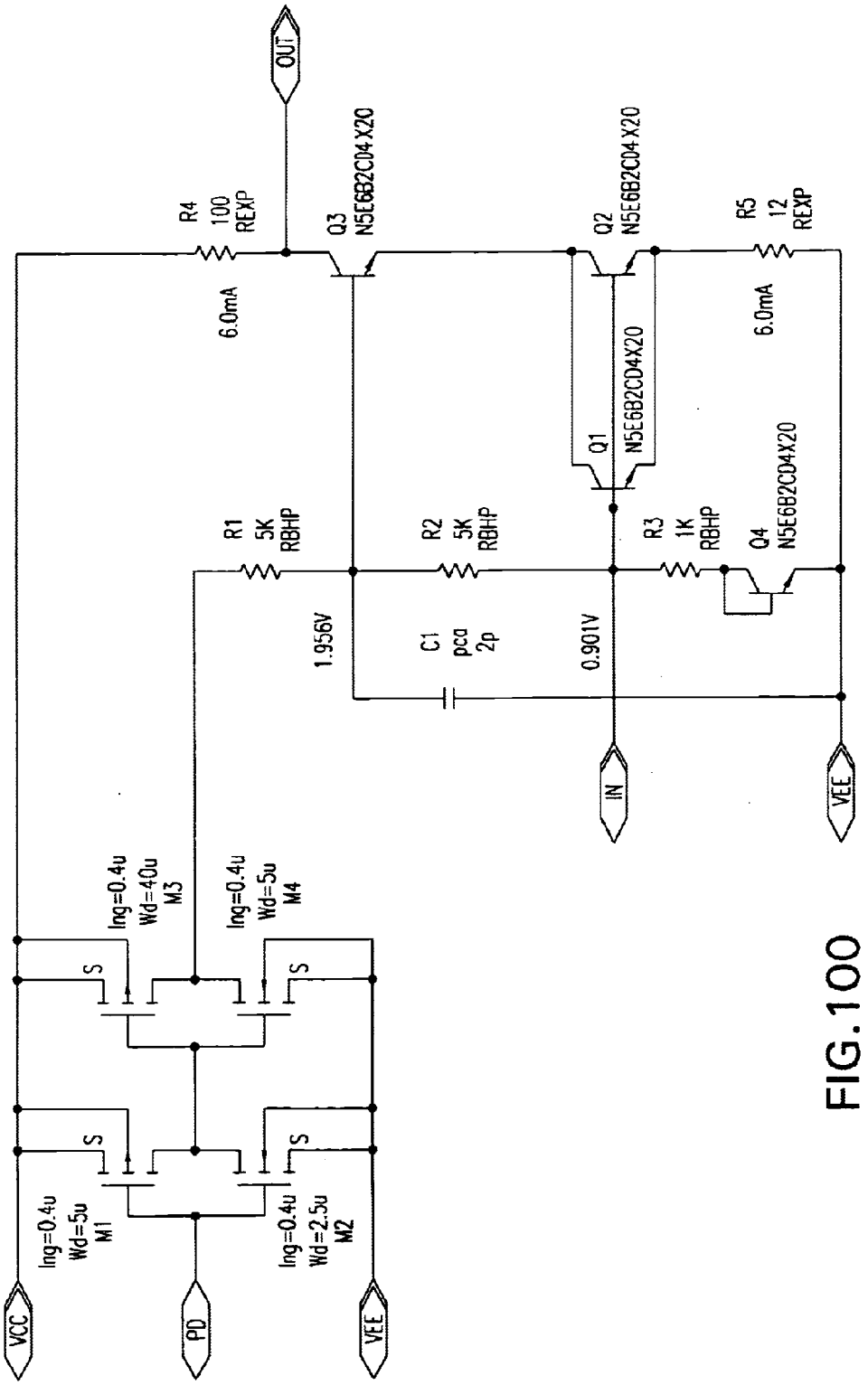

OUT
R4
100
REXP
Q3
N5E6B2C04X20
Q2
N5E6B2C04X20
R5
12
REXP
6.0mA
6.0mA
Q1
N5E6B2C04X20
Q4
N5E6B2C04X20
R1
5K
RBHP
R2
5K
RBHP
R3
1K
RBHP
1.956V
C1
pca
2p
0.901V
IN
VEE
lng=0.4u
Wd=40u
M3
lng=0.4u
Wd=5u
M4
S
S
S
S
lng=0.4u
Wd=5u
M1
lng=0.4u
Wd=2.5u
M2
VCC
PD
VEE

FIG. 100

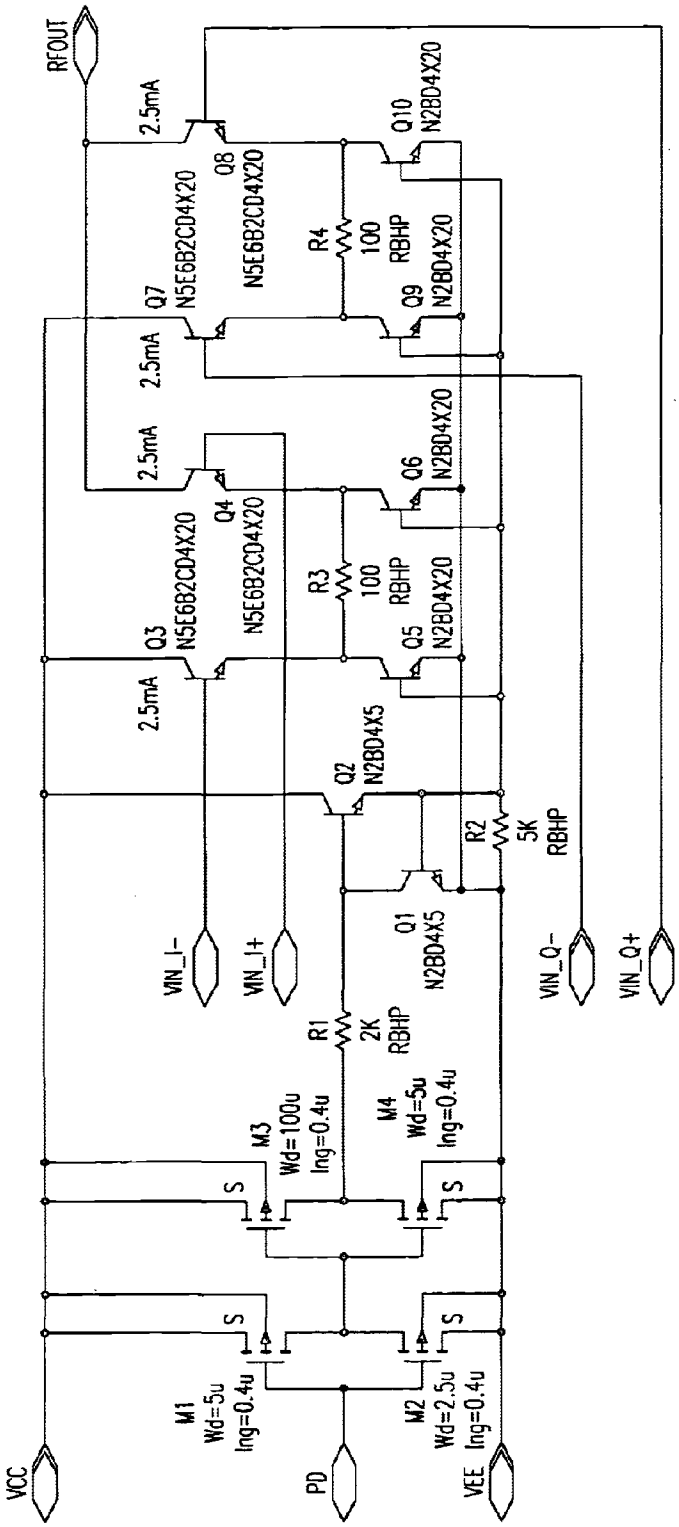

RFOUT
2.5mA
Q8
N5E6B2CD4X20
Q10
N2BD4X20
R4
100
RBHP
Q7
N5E6B2CD4X20
Q9
N2BD4X20
2.5mA
2.5mA
Q6
N2BD4X20
Q4
N5E6B2CD4X20
R3
100
RBHP
Q3
N5E6B2CD4X20
Q5
N2BD4X20
2.5mA
Q2
N2BD4X5
R2
5K
RBHP
VIN_I-
VIN_I+
Q1
N2BD4X5
VIN_Q-
VIN_Q+
R1
2K
RBHP
M3
Wd=100u
lng=0.4u
M4
Wd=5u
lng=0.4u
S
S
S
S
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
VCC
PD
VEE

FIG. 101

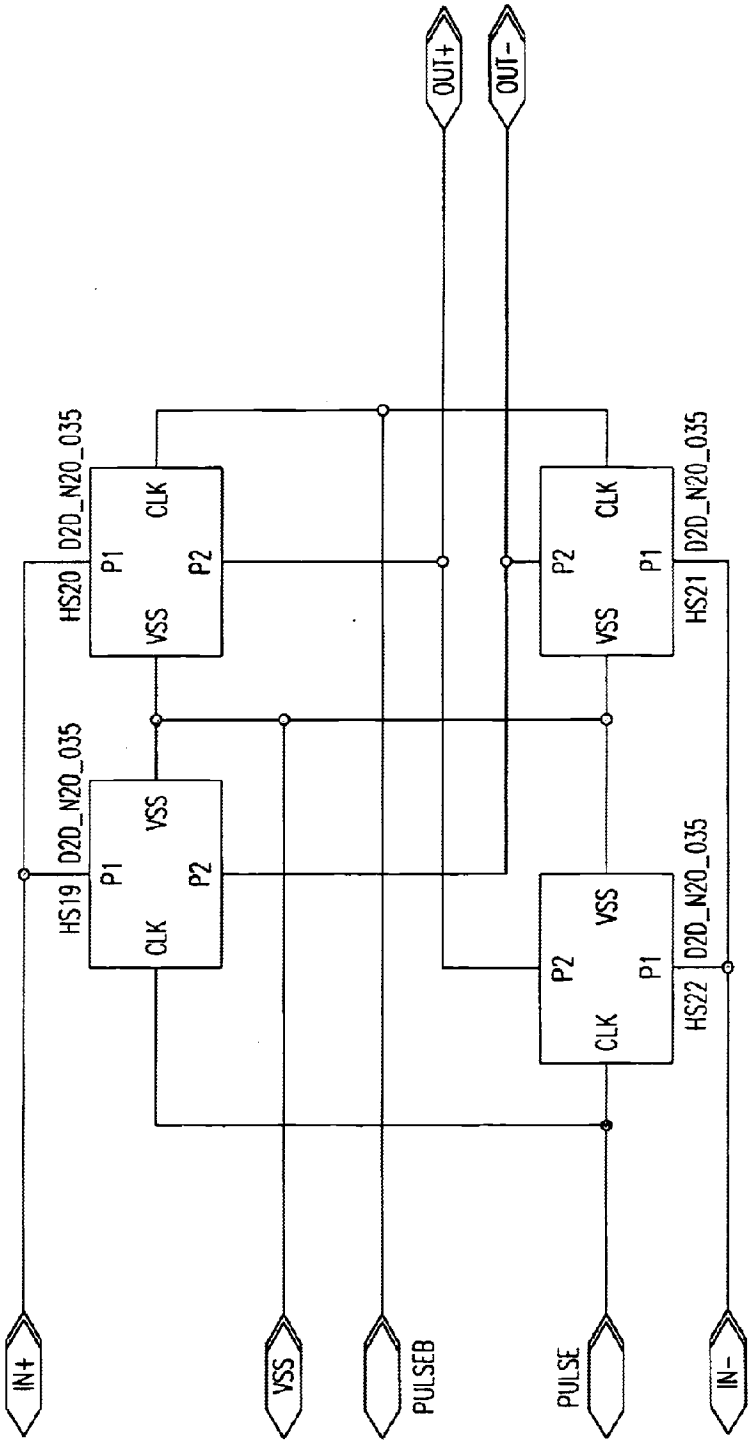

OUT+
OUT-
D2D_N20_035
HS20
P1
CLK
P2
VSS
D2D_N20_035
HS21
P2
CLK
P1
VSS
D2D_N20_035
HS19
P1
VSS
P2
CLK
D2D_N20_035
HS22
P2
VSS
P1
CLK
IN+
VSS
PULSEB
PULSE
IN-

FIG.102

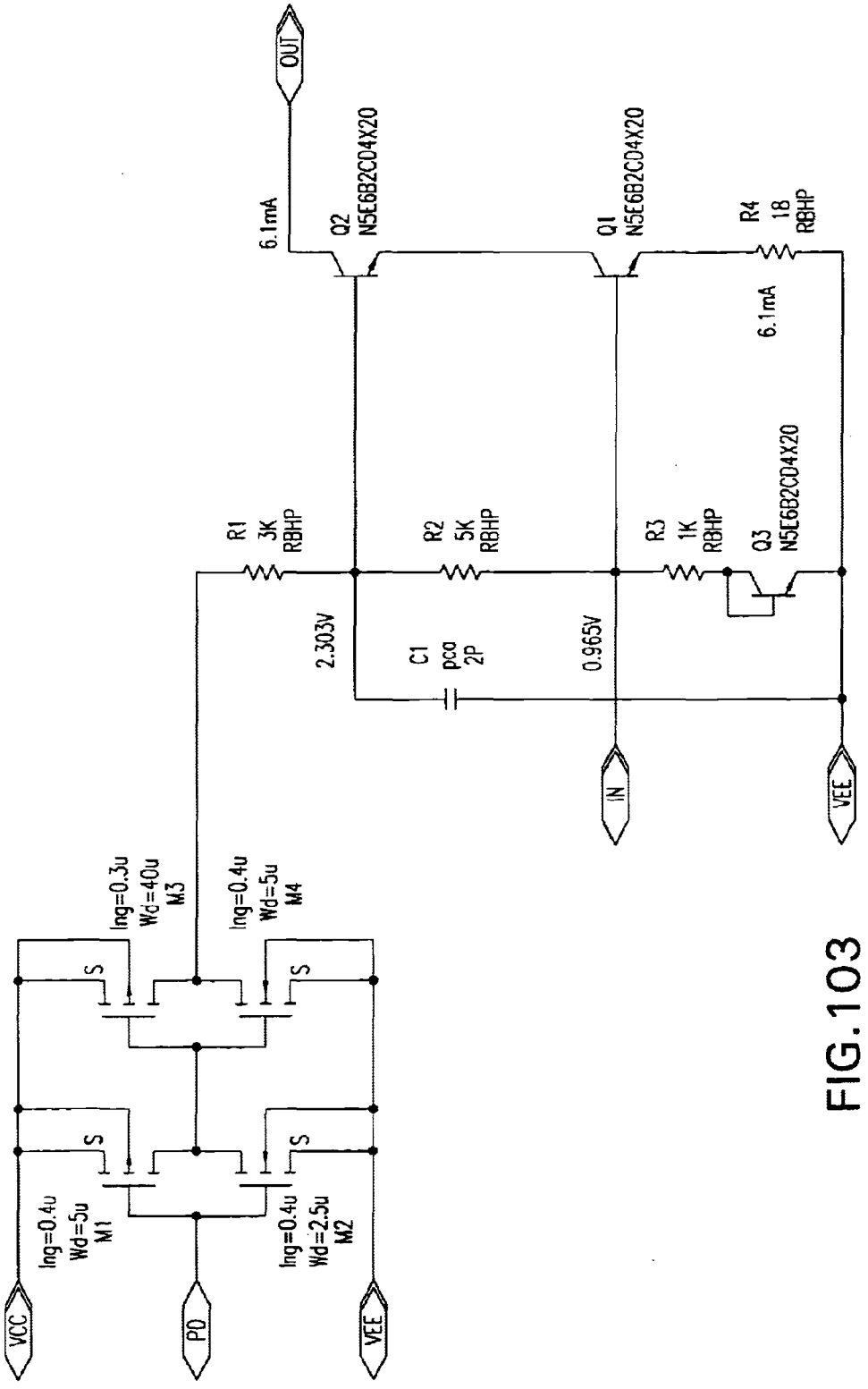

OUT
6.1mA
Q2
N5E6B2C04X20
Q1
N5E6B2C04X20
R4
18
RBHP
6.1mA
R1
3K
RBHP
R2
5K
RBHP
R3
1K
RBHP
Q3
N5E6B2C04X20
2.303V
C1
pca
2P
0.965V
IN
VEE
lng=0.3u
Wd=40u
M3
lng=0.4u
Wd=5u
M4
S
lng=0.4u
Wd=5u
M1
lng=0.4u
Wd=2.5u
M2
VCC
PD
VEE

FIG.103

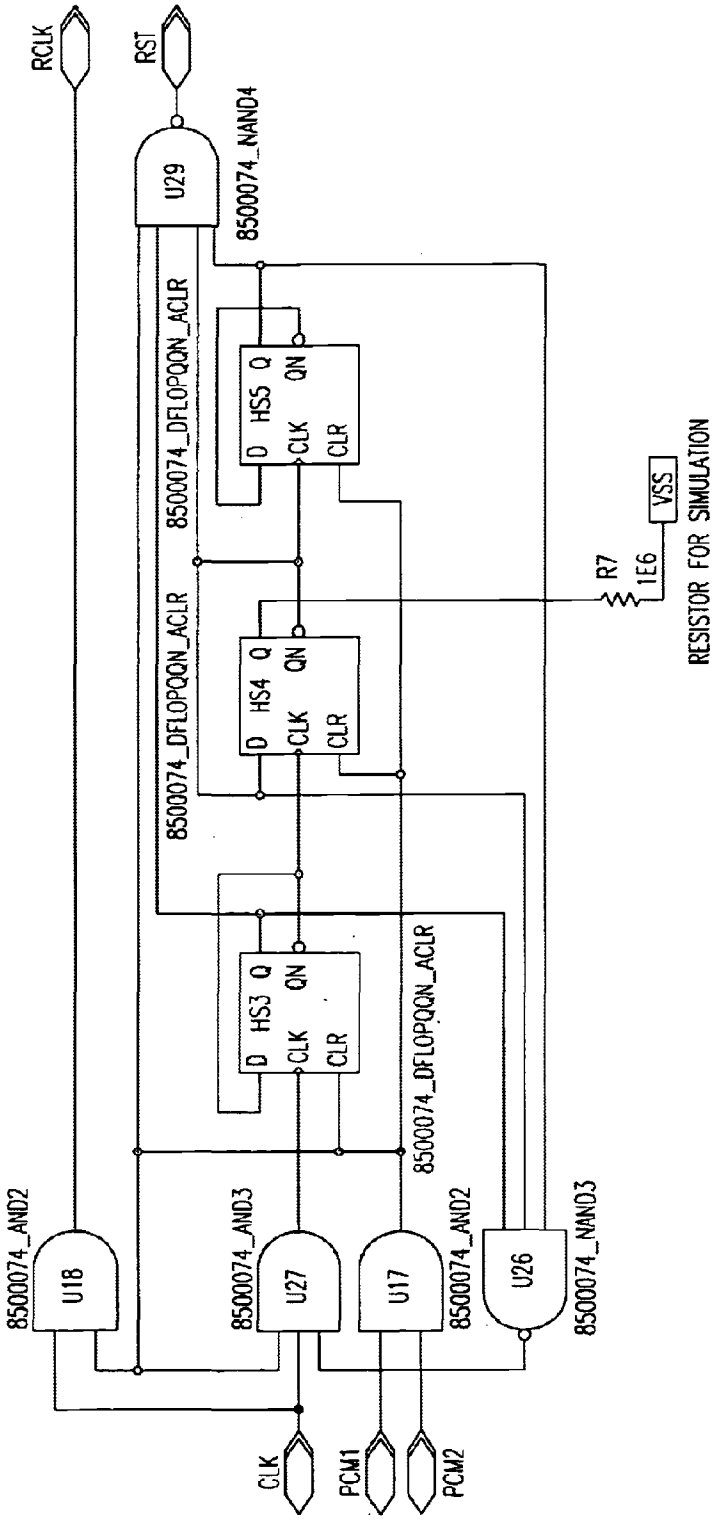

RCLK
RST
U29
8500074_NAND4
8500074_DFLOPQQN_ACLR
D HS5 Q
CLK QN
CLR
D HS4 Q
CLK QN
CLR
D HS3 Q
CLK QN
CLR
R7
1E6
VSS
RESISTOR FOR SIMULATION
8500074_AND2
U18
8500074_AND3
U27
U17
8500074_AND2
U26
8500074_NAND3
CLK
PCM1
PCM2

FIG. 104

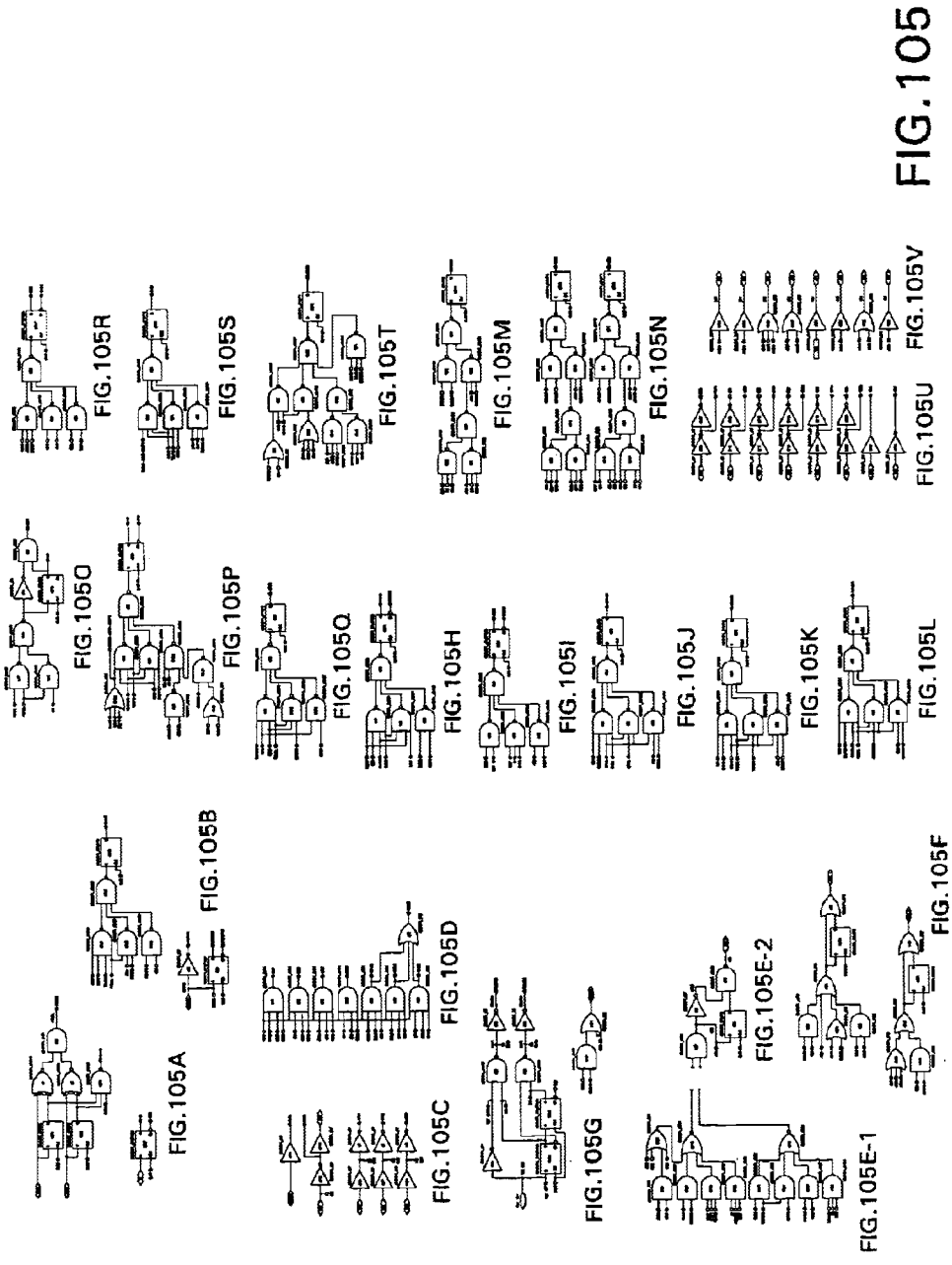
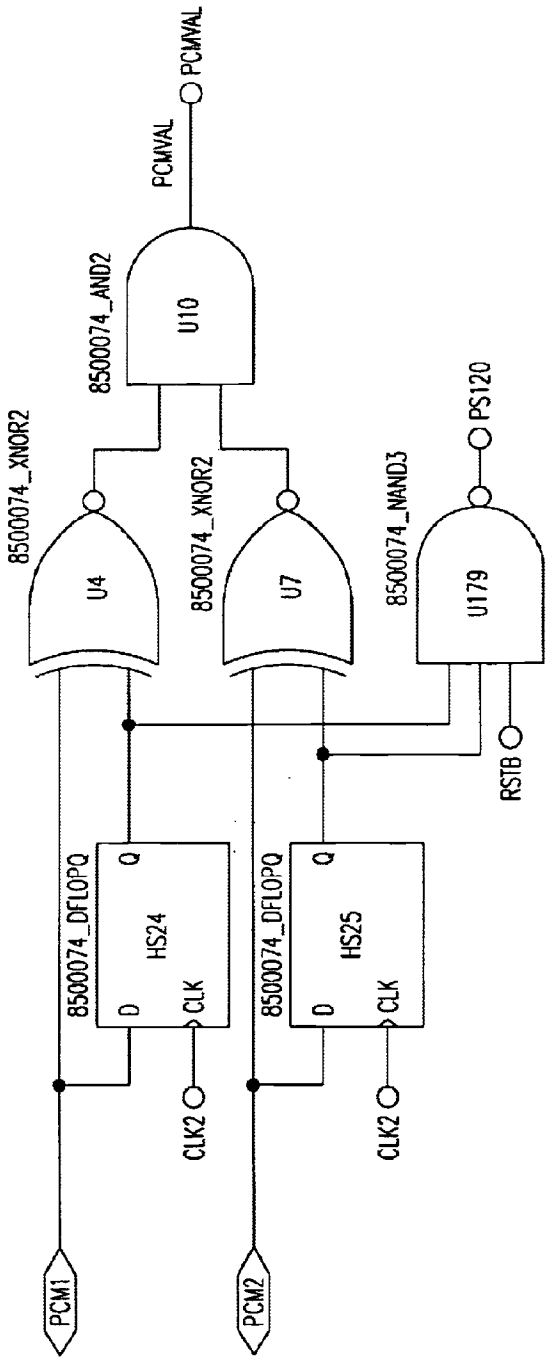

FIG.105A
FIG.105B
FIG.105C
FIG.105D
FIG.105E-1
FIG.105E-2
FIG.105F
FIG.105G
FIG.105H
FIG.105I
FIG.105J
FIG.105K
FIG.105L
FIG.105M
FIG.105N
FIG.105O
FIG.105P
FIG.105Q
FIG.105R
FIG.105S
FIG.105T
FIG.105U
FIG.105V

FIG.105


PCMVAL
PCMVAL
8500074_AND2
U10
8500074_XNOR2
U4
8500074_XNOR2
U7
8500074_NAND3
U179
PS120
RSTB
8500074_DFLOPQ
HS24
D
Q
CLK
CLK2
8500074_DFLOPQ
HS25
D
Q
CLK
CLK2
PCM1
PCM2

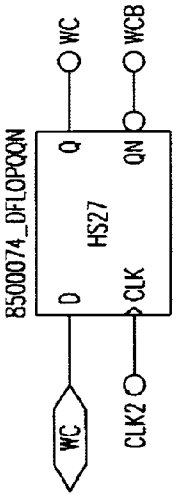

WC
WCB
8500074_DFLOPQQN
HS27
D
Q
QN
CLK
WC
CLK2

FIG.105A

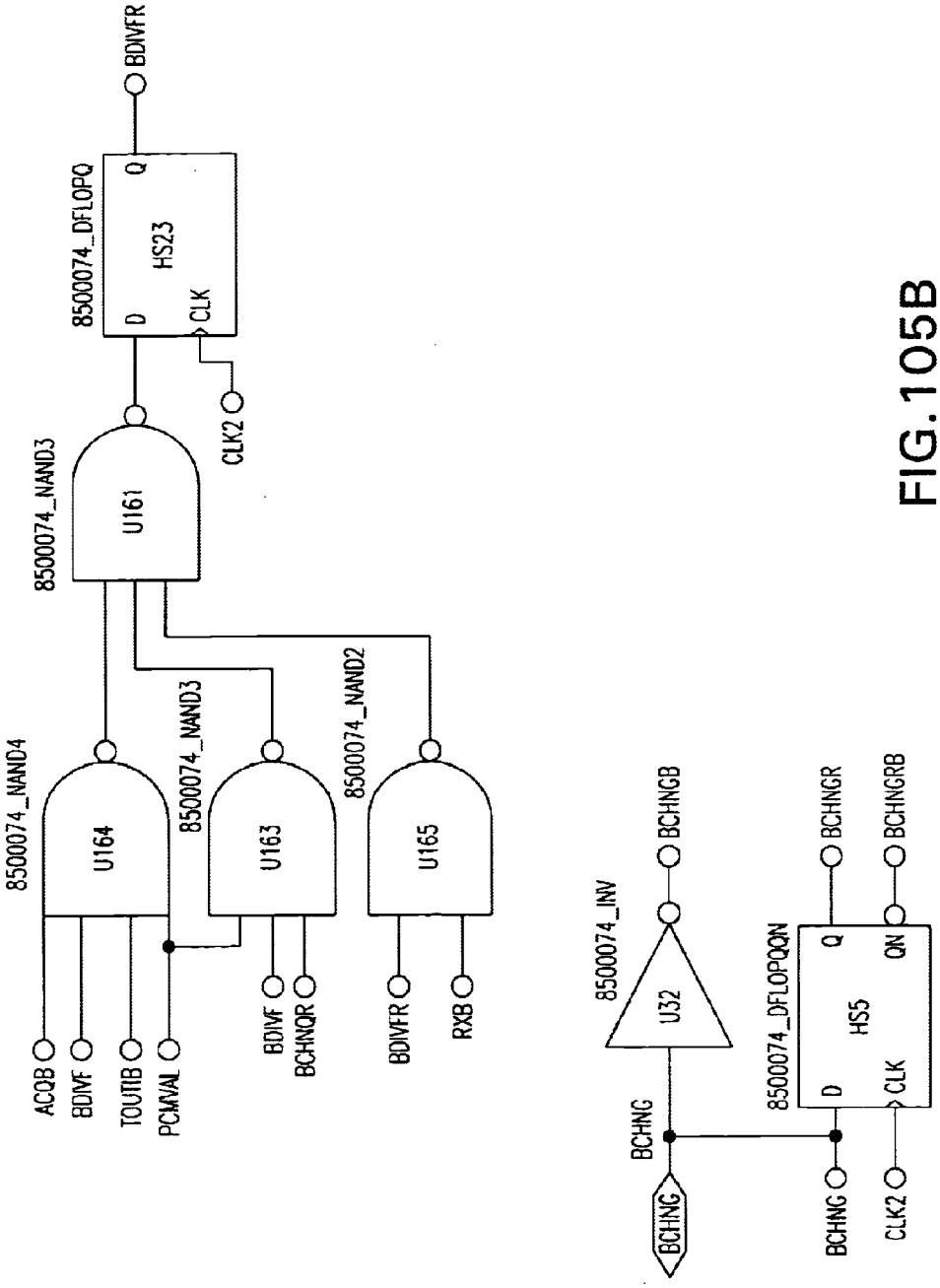

BDIVFR
8500074_DFLOPQ
HS23
Q
D
CLK
CLK2
8500074_NAND3
U161
8500074_NAND4
U164
8500074_NAND3
U163
8500074_NAND2
U165
ACQB
BDIVF
TOUTIB
PCMVAL
BDIVF
BCHNQR
BDIVFR
RXB
BCHNGB
8500074_INV
U32
BCHNG
BCHNG
8500074_DFLOPQQN
HS5
BCHNGR
BCHNGRB
QN
BCHNG
CLK2

FIG.105B

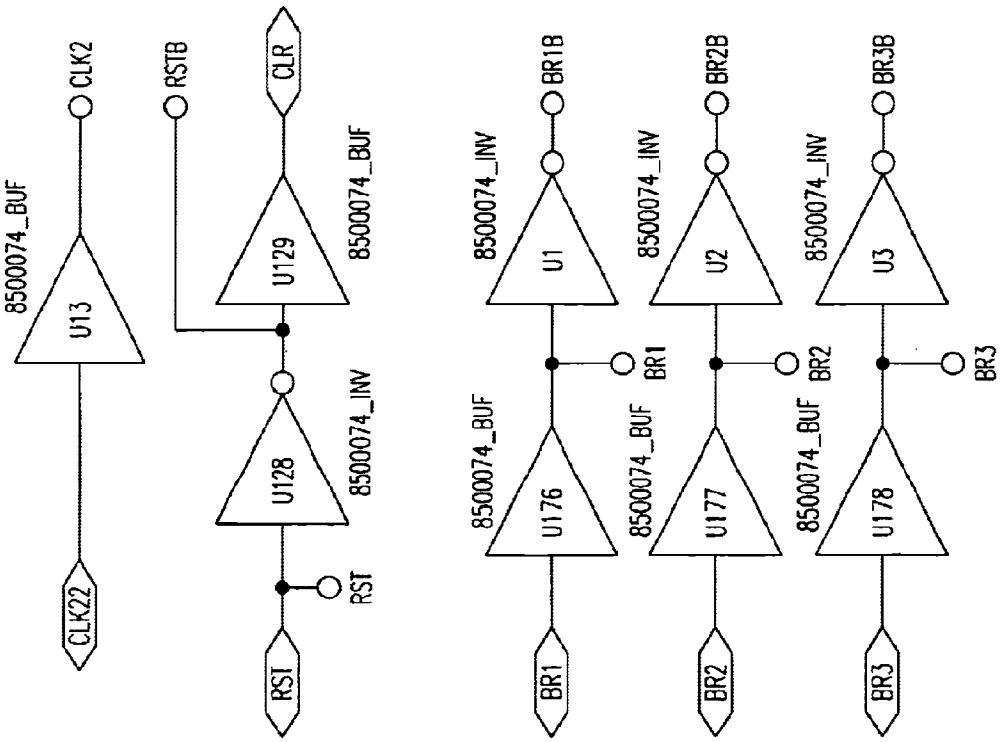

CLK2
8500074_BUF
U13
CLK22
RSTB
CLR
8500074_BUF
U129
8500074_INV
U128
RST
RST1
BR1B
8500074_INV
U1
BR1
8500074_BUF
U176
BR1
BR2B
8500074_INV
U2
BR2
8500074_BUF
U177
BR2
BR3B
8500074_INV
U3
BR3
8500074_BUF
U178
BR3

FIG.105C

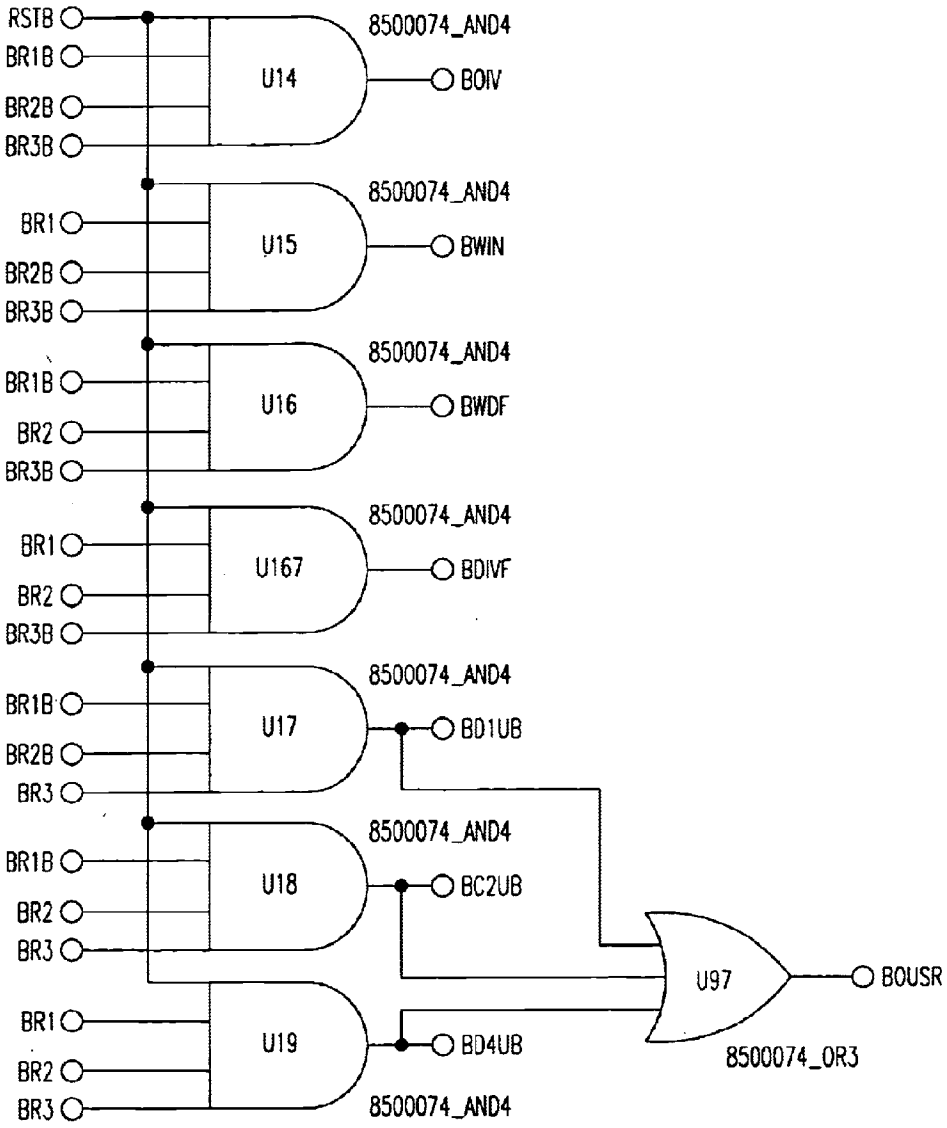

RSTB
BR1B
BR2B
BR3B
U14
8500074_AND4
BOIV
BR1
BR2B
BR3B
U15
8500074_AND4
BWIN
BR1B
BR2
BR3B
U16
8500074_AND4
BWDF
BR1
BR2
BR3B
U167
8500074_AND4
BDIVF
BR1B
BR2B
BR3
U17
8500074_AND4
BD1UB
BR1B
BR2
BR3
U18
8500074_AND4
BC2UB
BR1
BR2
BR3
U19
8500074_AND4
BD4UB
U97
BOUSR
8500074_OR3

FIG.105D

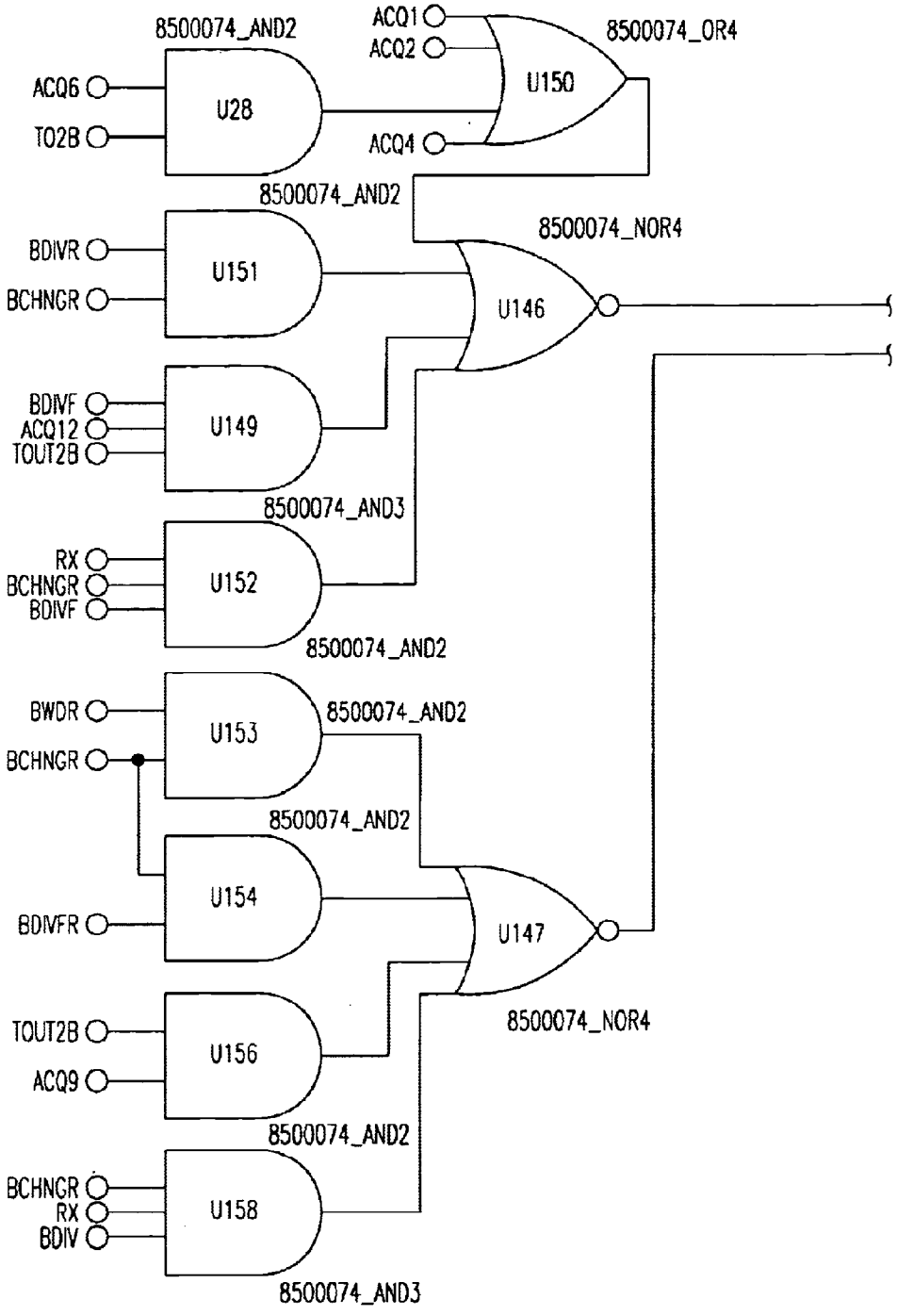

8500074_AND2
ACQ6
TO2B
U28
ACQ1
ACQ2
ACQ4
U150
8500074_OR4
8500074_AND2
BDIVR
BCHNGR
U151
8500074_NOR4
U146
BDIVF
ACQ12
TOUT2B
U149
8500074_AND3
RX
BCHNGR
BDIVF
U152
8500074_AND2
BWDR
BCHNGR
U153
8500074_AND2
8500074_AND2
U154
BDIVFR
U147
8500074_NOR4
TOUT2B
ACQ9
U156
8500074_AND2
BCHNGR
RX
BDIV
U158
8500074_AND3

FIG.105E-1

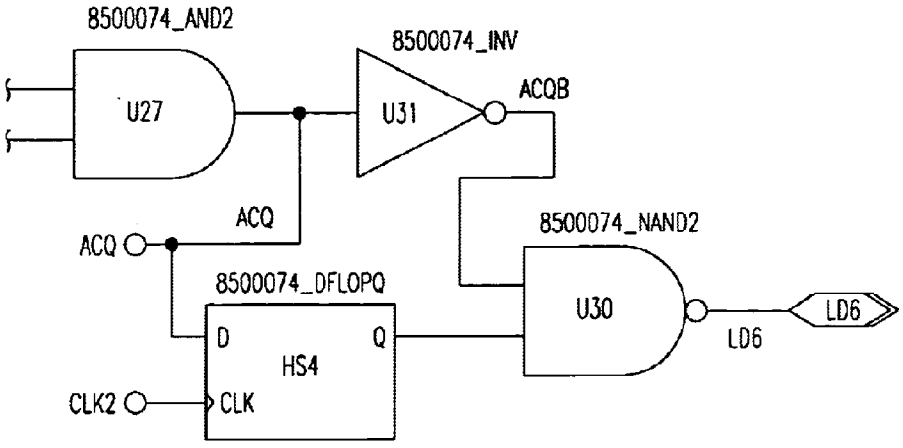

8500074_AND2
U27
8500074_INV
U31
ACQB
ACQ
ACQ
8500074_NAND2
8500074_DFLOPQ
U30
LD6
LD6
D
Q
HS4
CLK2
CLK

FIG.105E-2

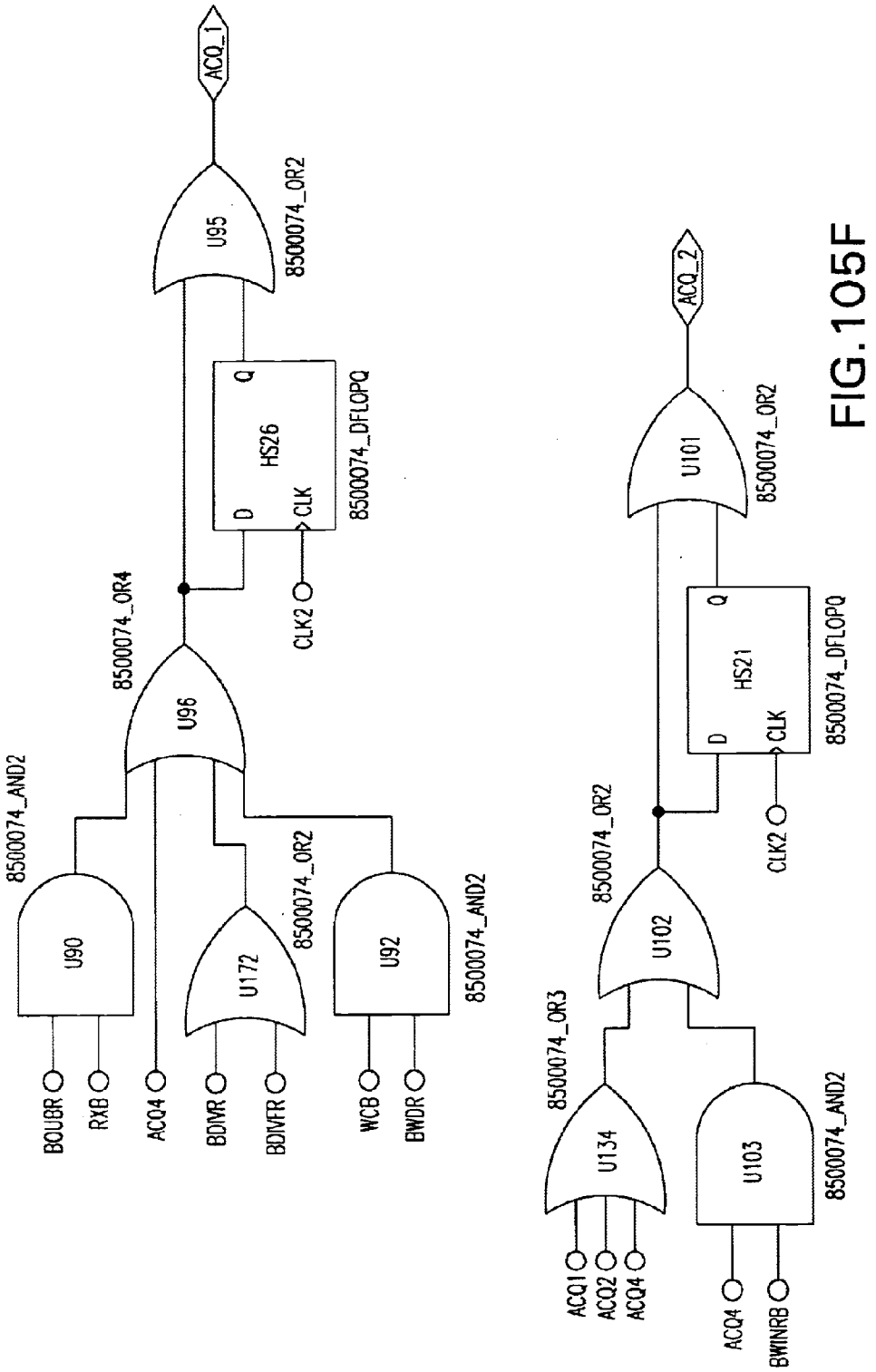

ACQ_1
U95
8500074_OR2
HS26
Q
D
CLK
8500074_DFLOPQ
CLK2
8500074_OR4
U96
8500074_AND2
U90
BOUBR
RXB
ACQ4
8500074_OR2
U172
BDIVR
BDIVFR
U92
8500074_AND2
WCB
BWDR
ACQ_2
U101
8500074_OR2
HS21
Q
D
CLK
8500074_DFLOPQ
CLK2
8500074_OR2
U102
8500074_OR3
U134
ACQ1
ACQ2
ACQ4
U103
8500074_AND2
ACQ4
BWINRB

FIG.105F

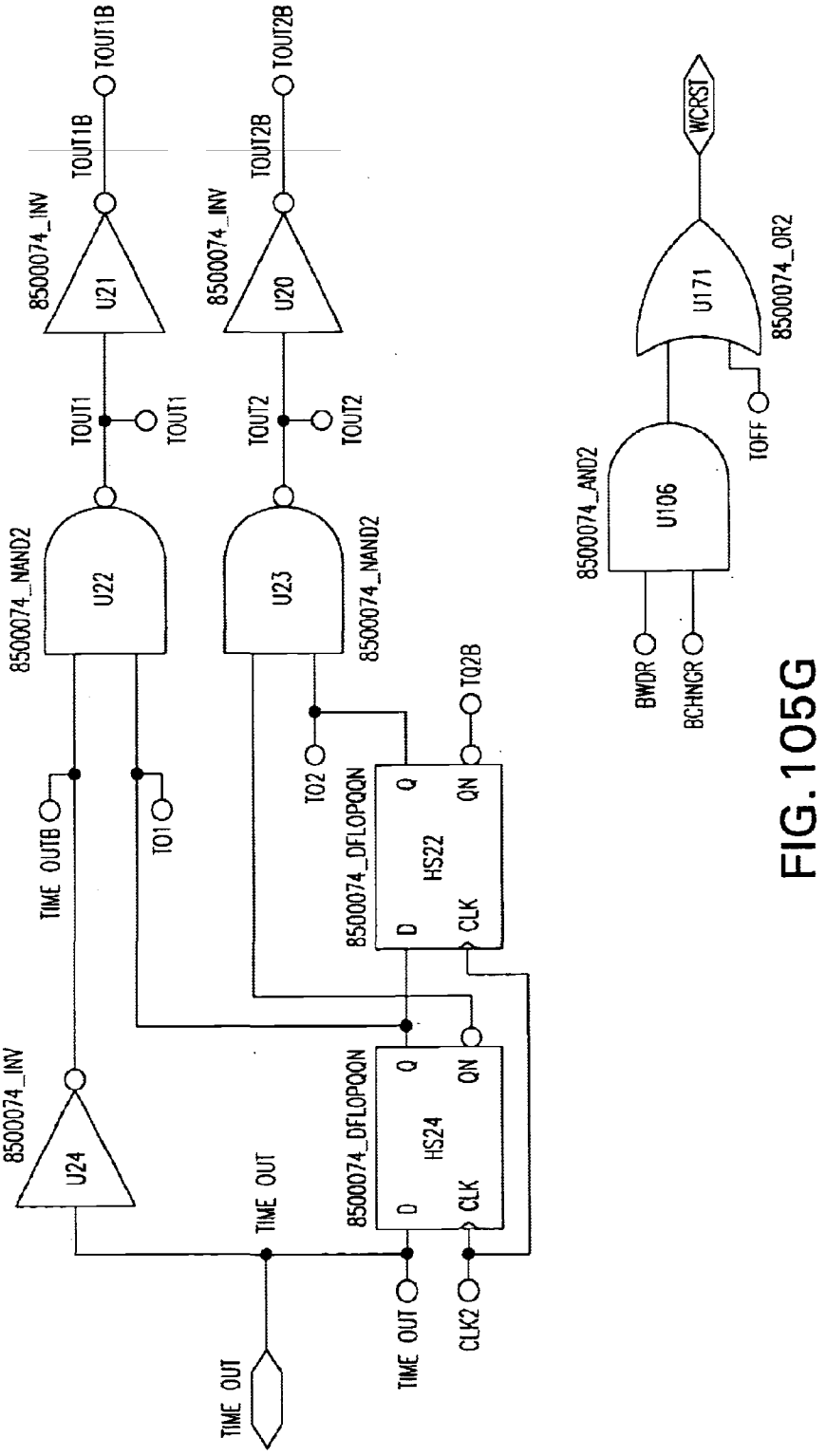

TOUT1B
TOUT1B
8500074_INV
U21
TOUT2B
TOUT2B
8500074_INV
U20
WCRST
U171
8500074_OR2
TOUT1
TOUT1
TOUT2
TOUT2
TOFF
8500074_AND2
U106
8500074_NAND2
U22
8500074_NAND2
U23
BWDR
BCHNGR
TQ2B
TIME OUTB
TO1
TO2
8500074_DFLOPQQN
HS22
Q
QN
D
CLK
8500074_INV
U24
TIME OUT
8500074_DFLOPQQN
HS24
Q
QN
D
CLK
TIME OUT
TIME OUT
CLK2

FIG.105G

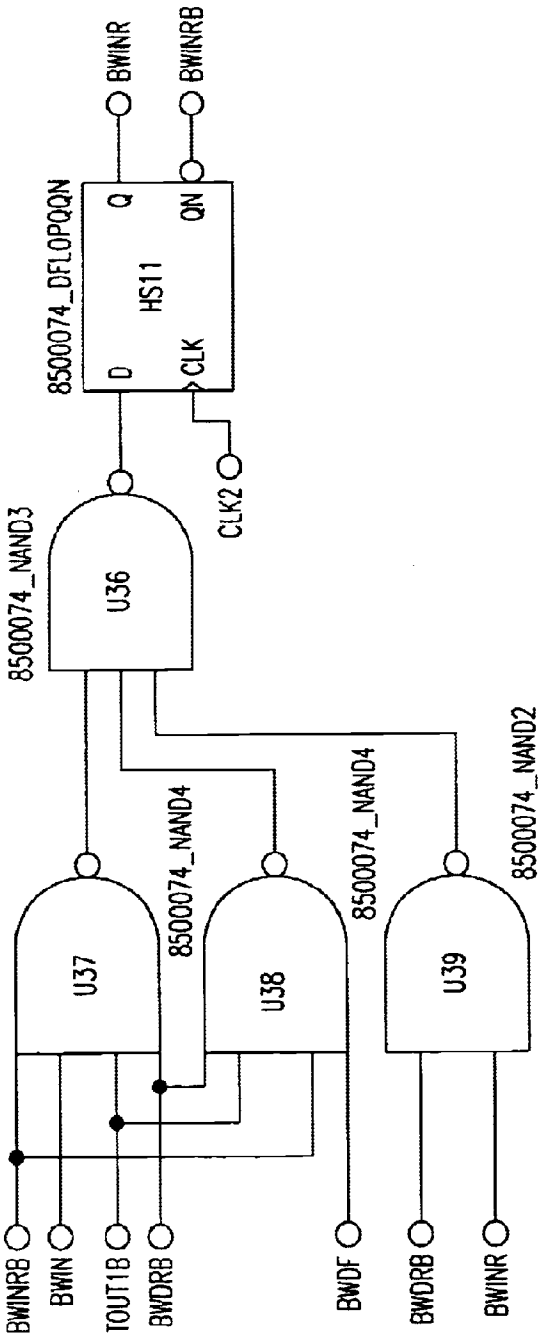

BWINR
BWINRB
8500074_DFLOPQQN
Q
QN
HS11
D
CLK
CLK2
8500074_NAND3
U36
8500074_NAND4
U37
8500074_NAND4
U38
8500074_NAND2
U39
BWINRB
BWIN
TOUT1B
BWDRB
BWDF
BWDRB
BWINR

FIG.105H

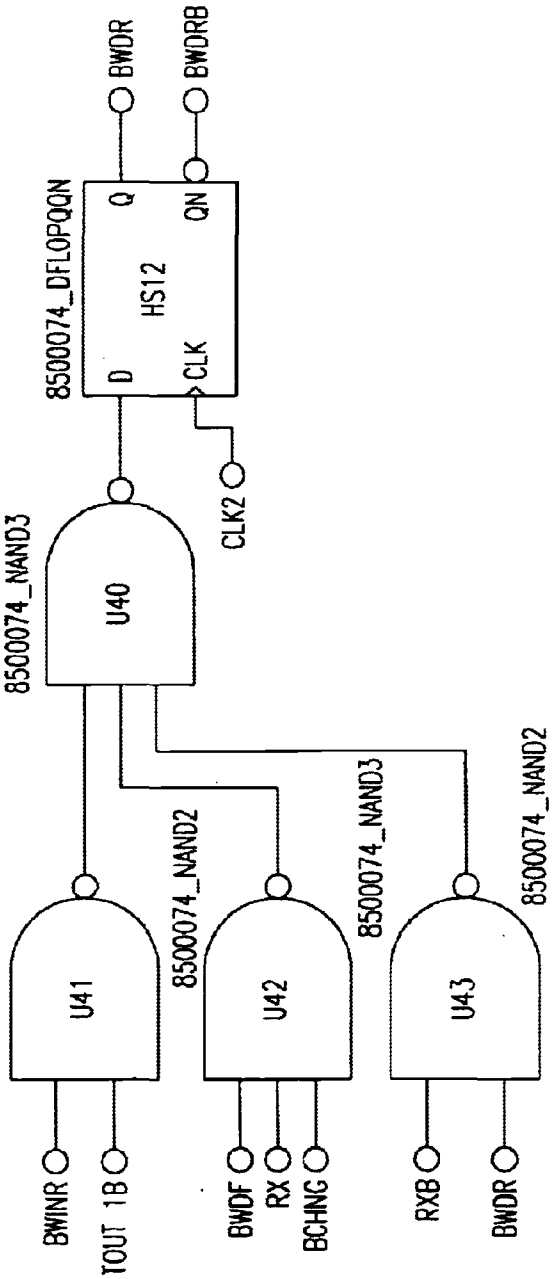

BWDR
BWDRB
8500074_DFLOPQQN
Q
QN
HS12
D
CLK
CLK2
8500074_NAND3
U40
8500074_NAND2
8500074_NAND3
8500074_NAND2
U41
U42
U43
BWINR
TOUT 1B
BWDF
RX
BCHNG
RXB
BWDR

FIG. 105I

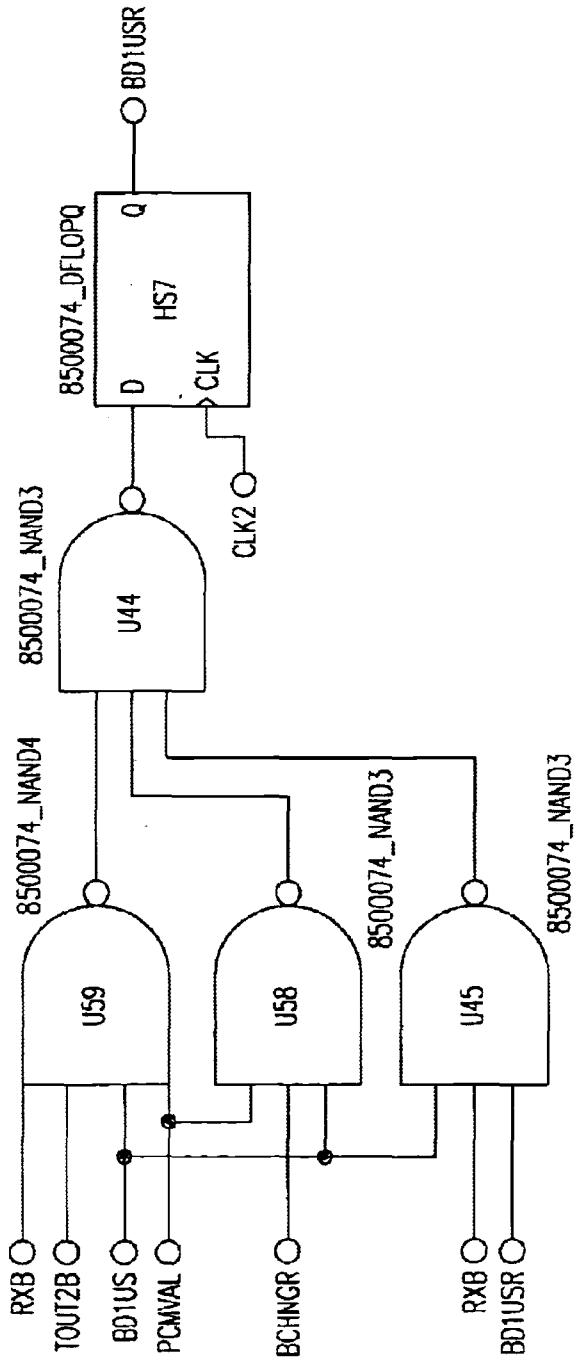

BD1USR
8500074_DFLOPQ
HS7
Q
D
CLK
CLK2
8500074_NAND3
U44
8500074_NAND4
U59
8500074_NAND3
U58
8500074_NAND3
U45
RXB
TOUT2B
BD1US
PCMVAL
BCHNGR
RXB
BD1USR

FIG. 105J

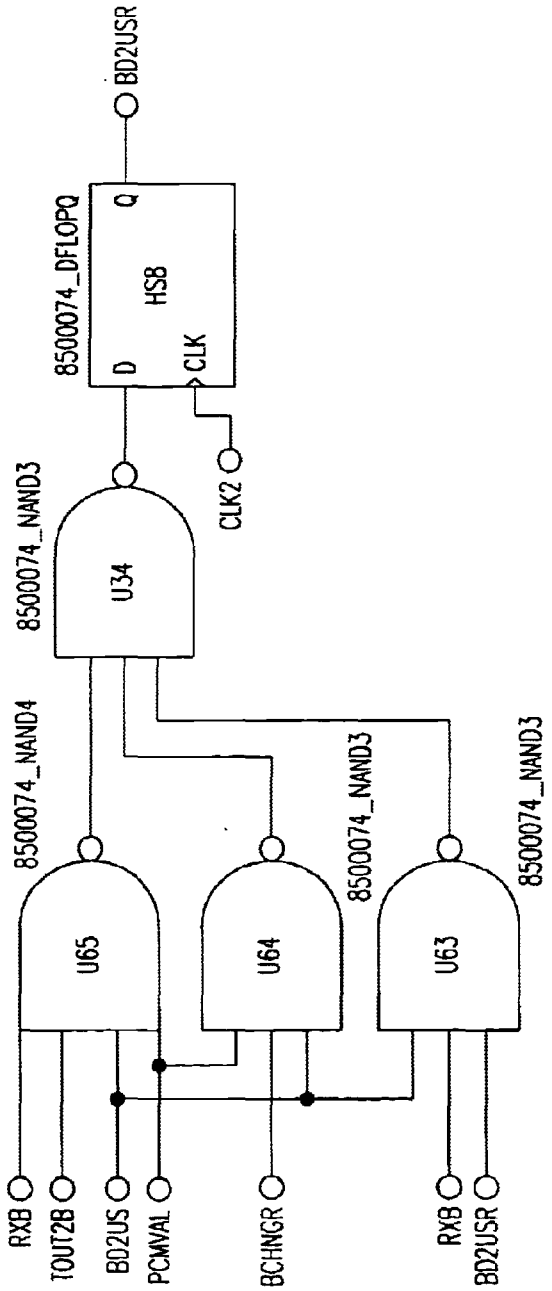

BD2USR
8500074_DFLOPQ
Q
HSB
D
CLK
CLK2
8500074_NAND3
U34
8500074_NAND4
U65
U64
U63
8500074_NAND3
8500074_NAND3
RXB
TOUT2B
BD2US
PCMVAL
BCHNGR
RXB
BD2USR

FIG. 105K

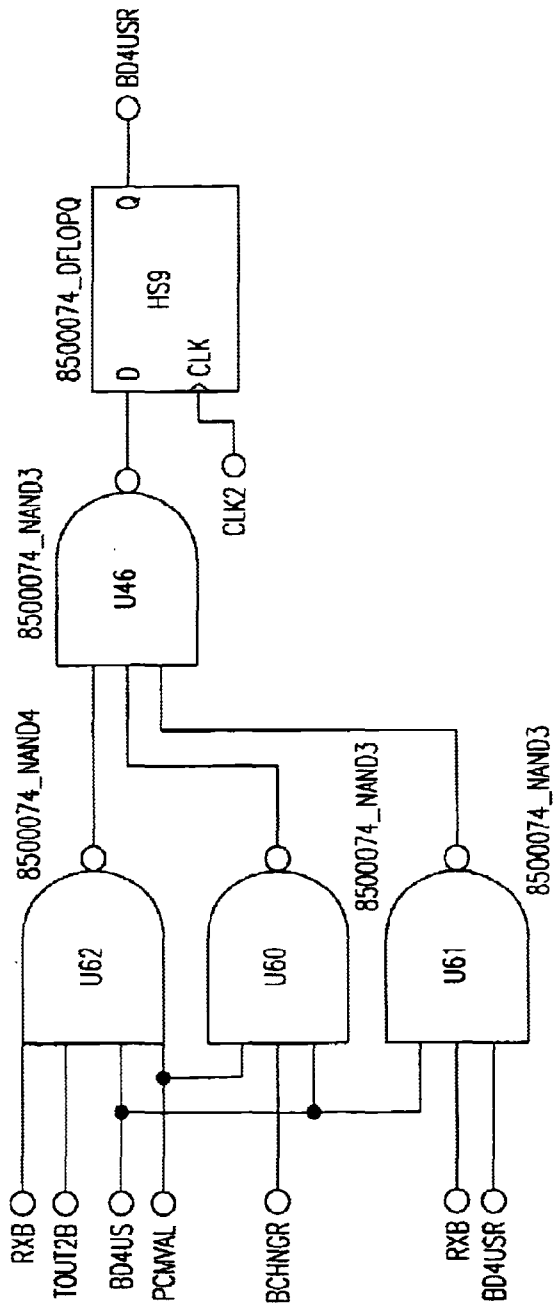

BD4USR
8500074_DFLOPQ
HS9
Q
D
CLK
CLK2
8500074_NAND3
U46
8500074_NAND4
U62
U60
8500074_NAND3
U61
8500074_NAND3
RXB
TOUT2B
BD4US
PCMVAL
BCHNGR
RXB
BD4USR

FIG.105L

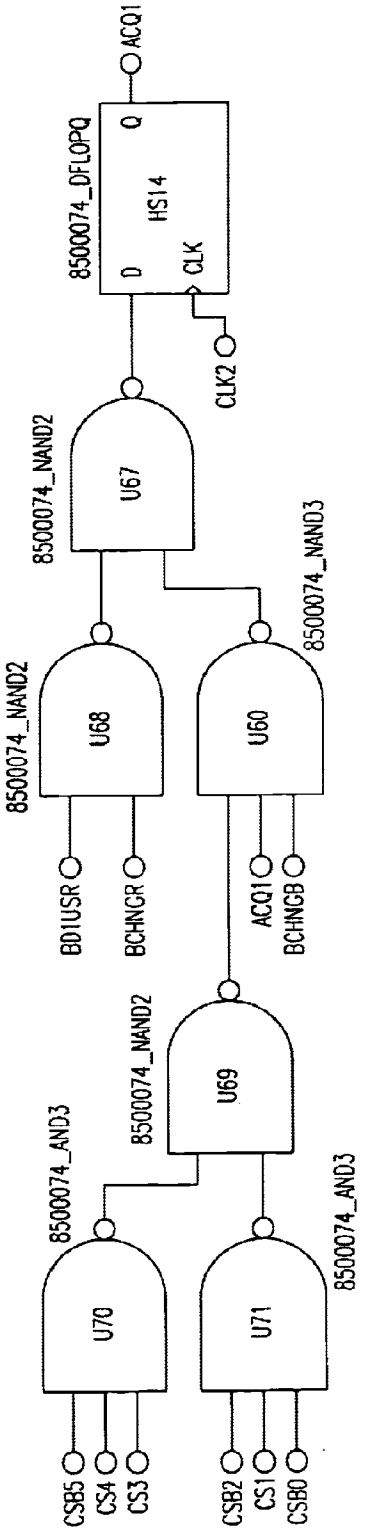

ACQ1
8500074_DFLOPQ
Q
HS14
D
CLK
CLK2
8500074_NAND2
U67
8500074_NAND2
U68
8500074_NAND3
U60
BD1USR
BCHNGR
ACQ1
BCHNGB
8500074_NAND2
U69
8500074_AND3
U70
8500074_AND3
U71
CSB5
CS4
CS3
CSB2
CS1
CSB0

FIG.105M

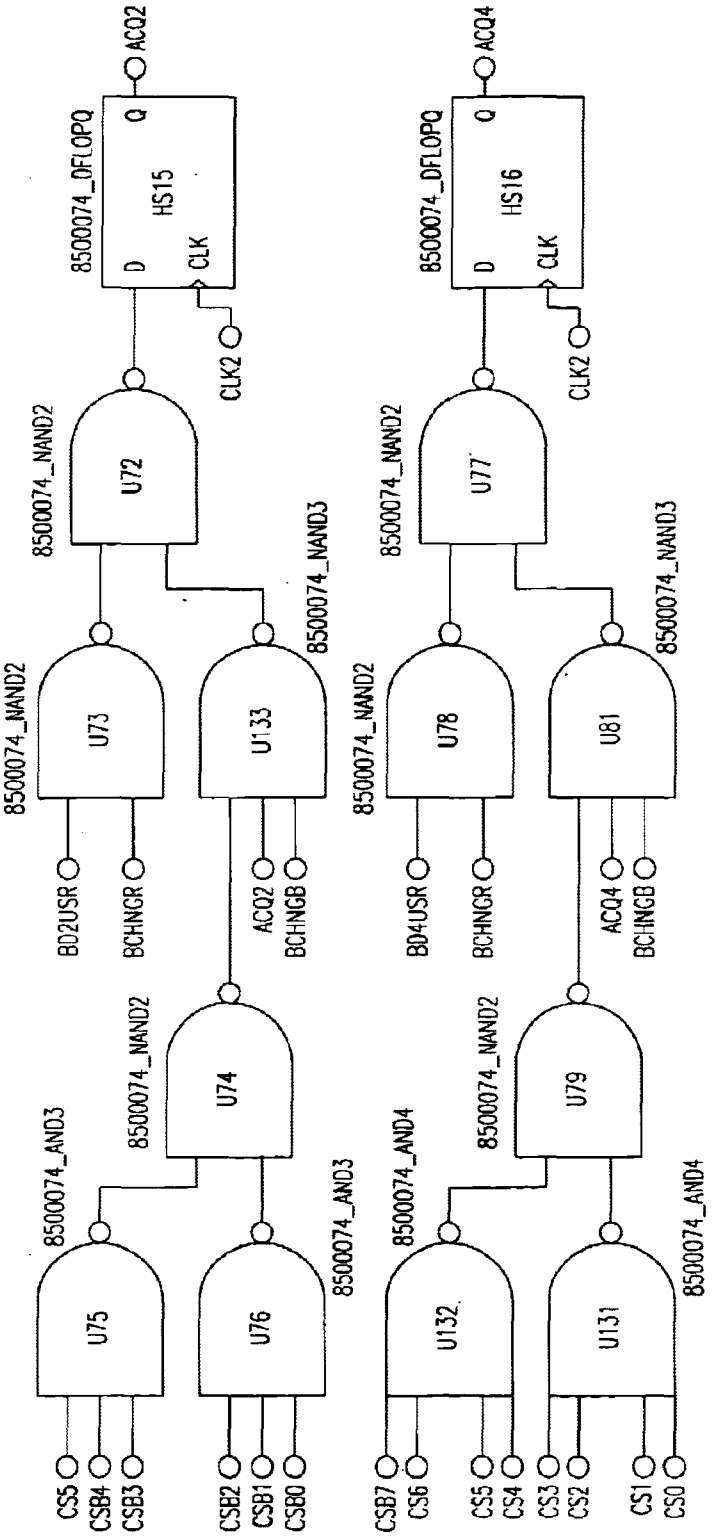

ACQ2
8500074_DFLOPQ
HS15
D
Q
CLK
CLK2
8500074_NAND2
U72
8500074_NAND3
U73
U133
BD2USR
BCHNGR
ACQ2
BCHNGB
8500074_NAND2
U74
8500074_AND3
U75
8500074_AND3
U76
CSB5
CSB4
CSB3
CSB2
CSB1
CSB0
ACQ4
8500074_DFLOPQ
HS16
D
Q
CLK
CLK2
8500074_NAND2
U77
8500074_NAND3
U78
U81
BD4USR
BCHNGR
ACQ4
BCHNGB
8500074_NAND2
U79
8500074_AND4
U132
8500074_AND4
U131
CSB7
CS6
CS5
CS4
CS3
CS2
CS1
CS0

FIG. 105N

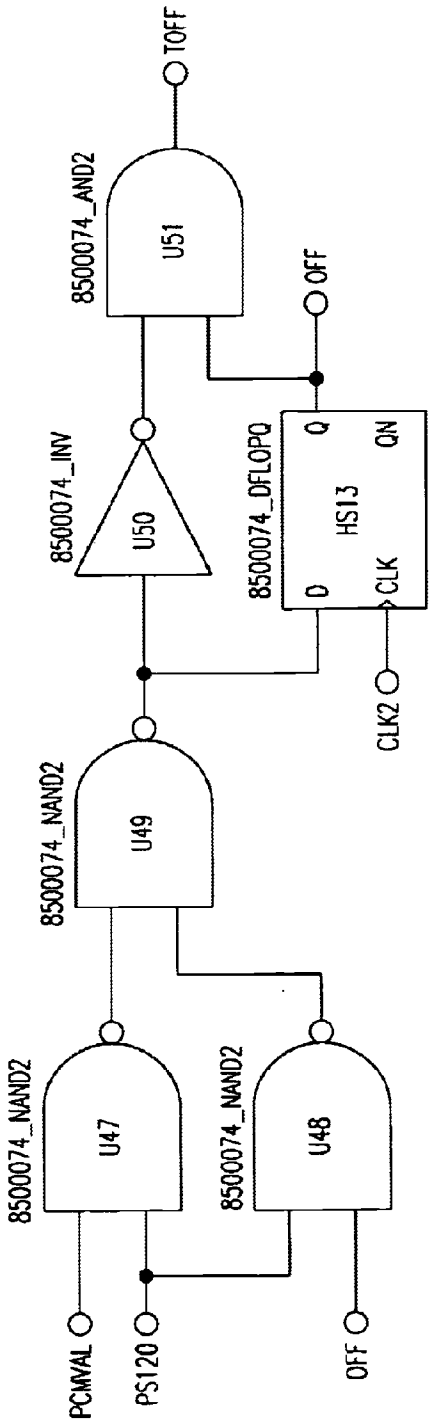

TOFF
8500074_AND2
U51
OFF
8500074_INV
U50
8500074_DFLOPQ
HS13
Q
QN
D
CLK
CLK2
8500074_NAND2
U49
8500074_NAND2
U47
8500074_NAND2
U48
PCMVAL
PS120
OFF

FIG.1050

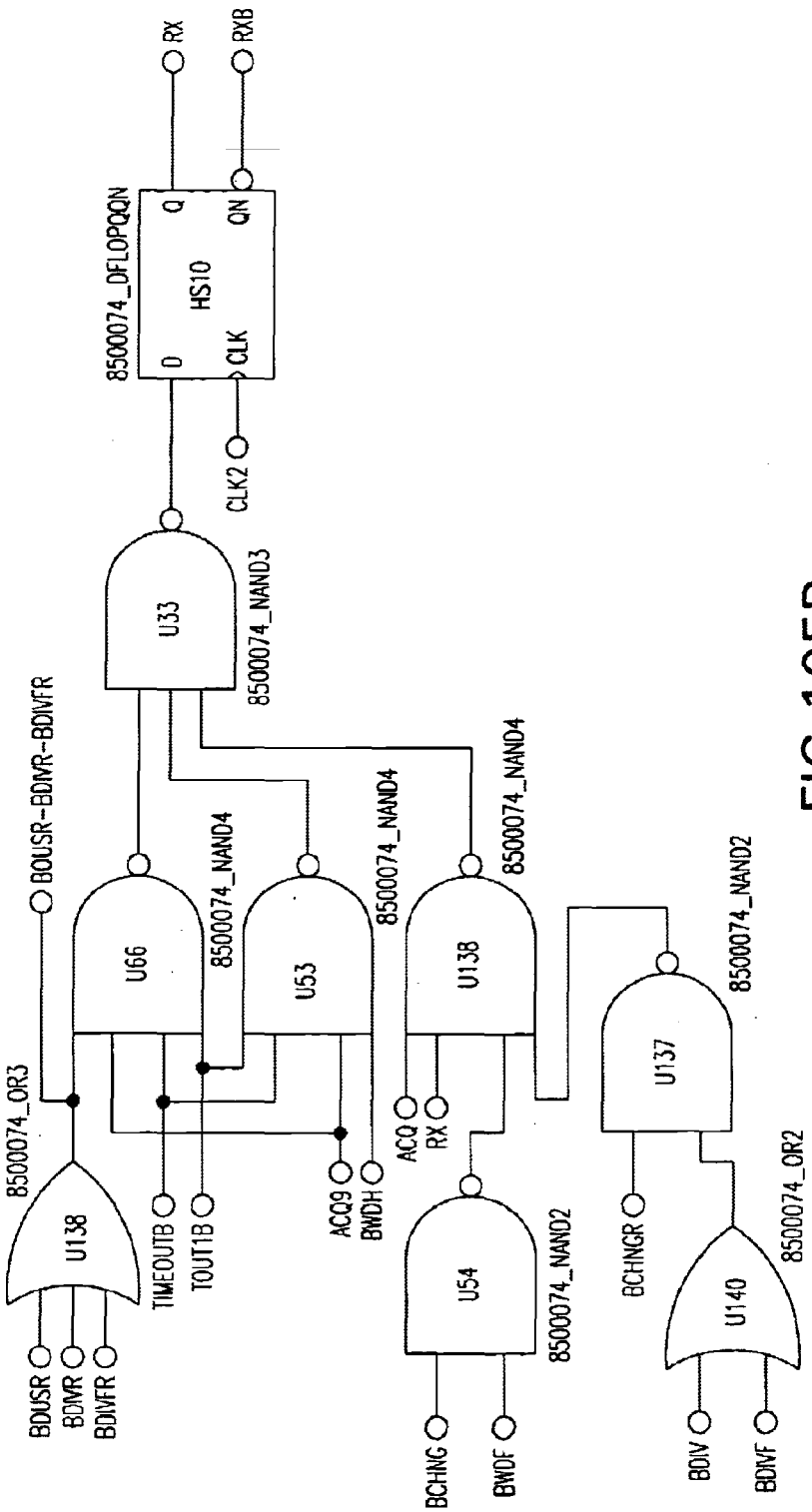

RX
RXB
8500074_DFLOPQQN
Q
QN
HS10
D
CLK
CLK2
U33
8500074_NAND3
BOUSR-BDMR-BDMFR
U66
8500074_NAND4
U53
8500074_NAND4
U138
8500074_NAND4
U137
8500074_NAND2
8500074_OR3
U138
TIMEOUTB
TOUT1B
ACQ9
BMDH
ACQ
RX
U54
8500074_NAND2
BCHNGR
U140
8500074_OR2
BDUSR
BDMR
BDMFR
BCHNG
BMDF
BDIV
BDMF

FIG. 105P

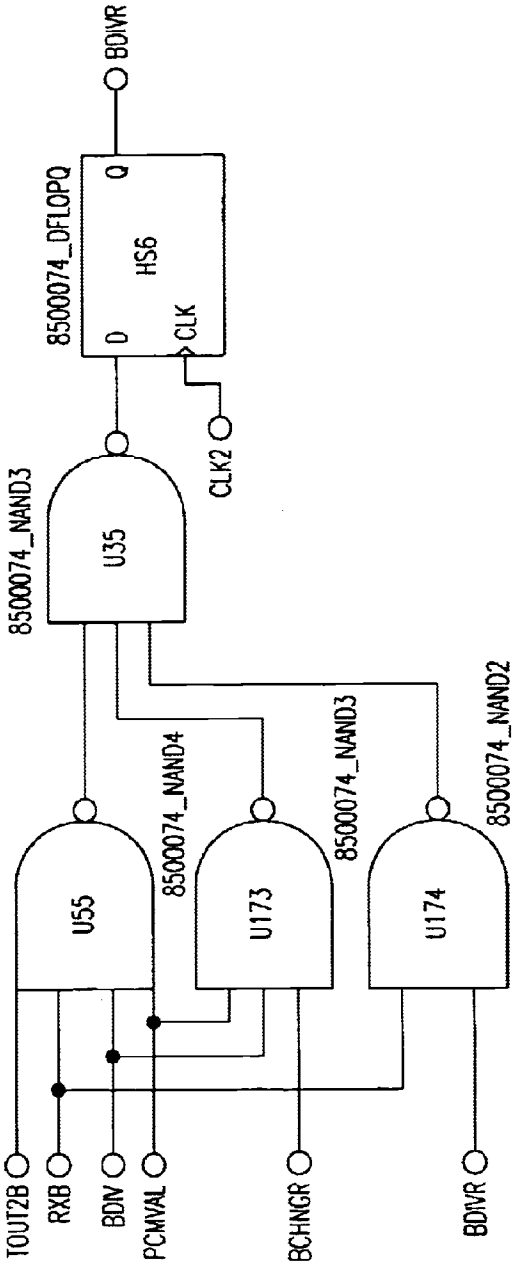

BDWR
8500074_DFLOPQ
HS6
Q
D
CLK
CLK2
8500074_NAND3
U35
8500074_NAND4
U55
8500074_NAND3
U173
8500074_NAND2
U174
TOUT2B
RXB
BDIV
PCMVAL
BCHNGR
BDWR

FIG.105Q

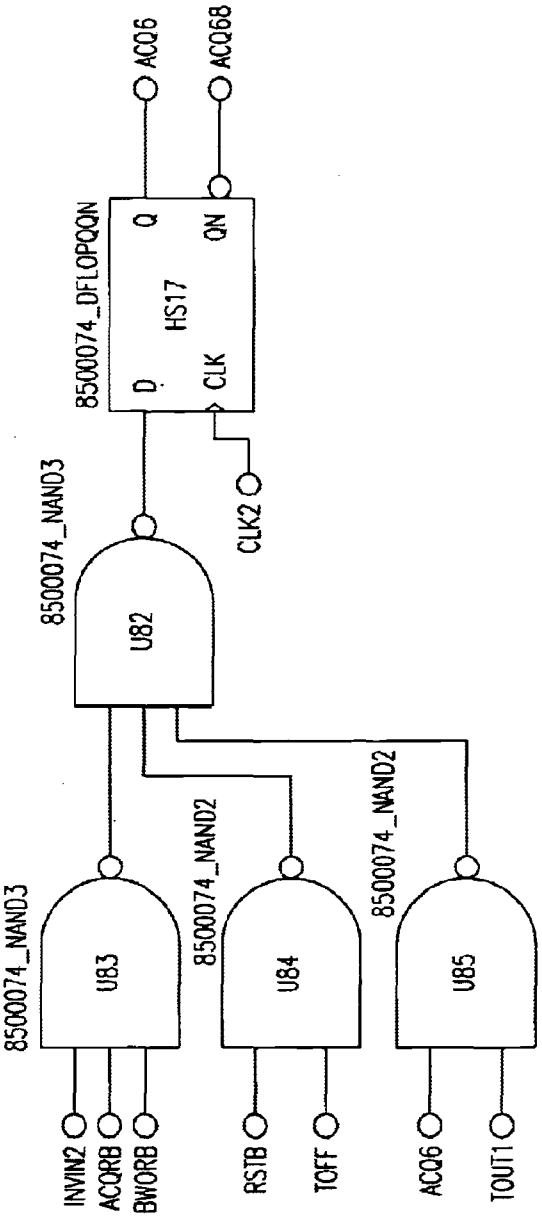

ACQ6
ACQ6B
8500074_DFLOPQQN
Q
QN
HS17
D
CLK
CLK2
8500074_NAND3
U82
8500074_NAND3
U83
8500074_NAND2
U84
8500074_NAND2
U85
INVIN2
ACQRB
BWORB
RSTB
TOFF
ACQ6
TOUT1

FIG.105R

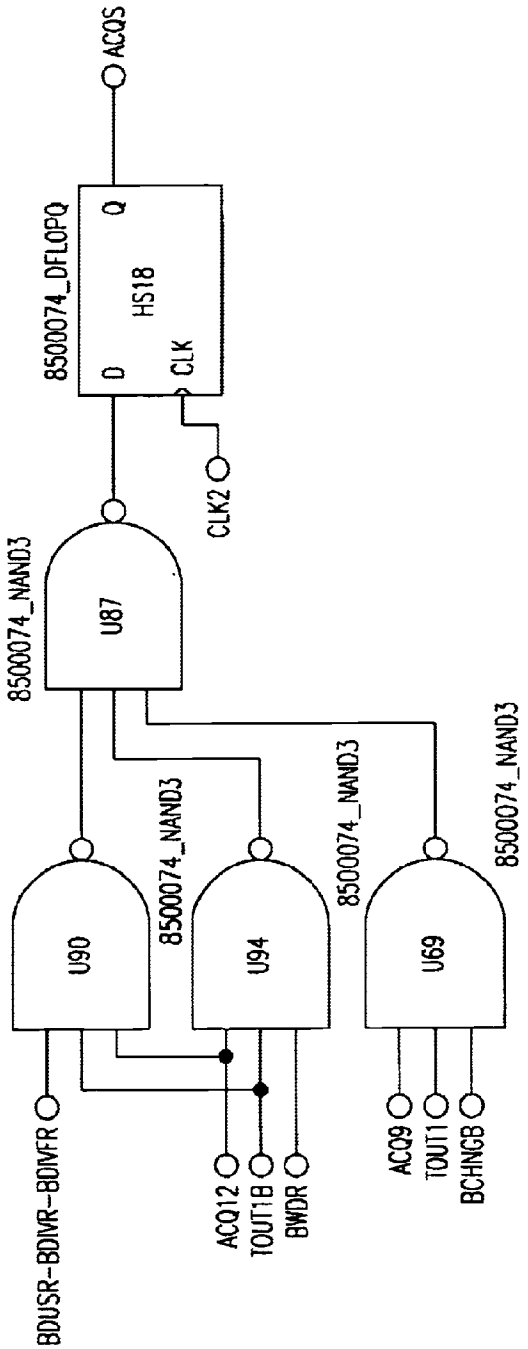

ACQS
8500074_DFLOPQ
Q
HS18
D
CLK
CLK2
8500074_NAND3
U87
8500074_NAND3
U90
8500074_NAND3
U94
8500074_NAND3
U69
BDUSR-BDIVR-BDIVFR
ACQ12
TOUT1B
BWDR
ACQ9
TOUT1
BCHNGB

FIG.105S

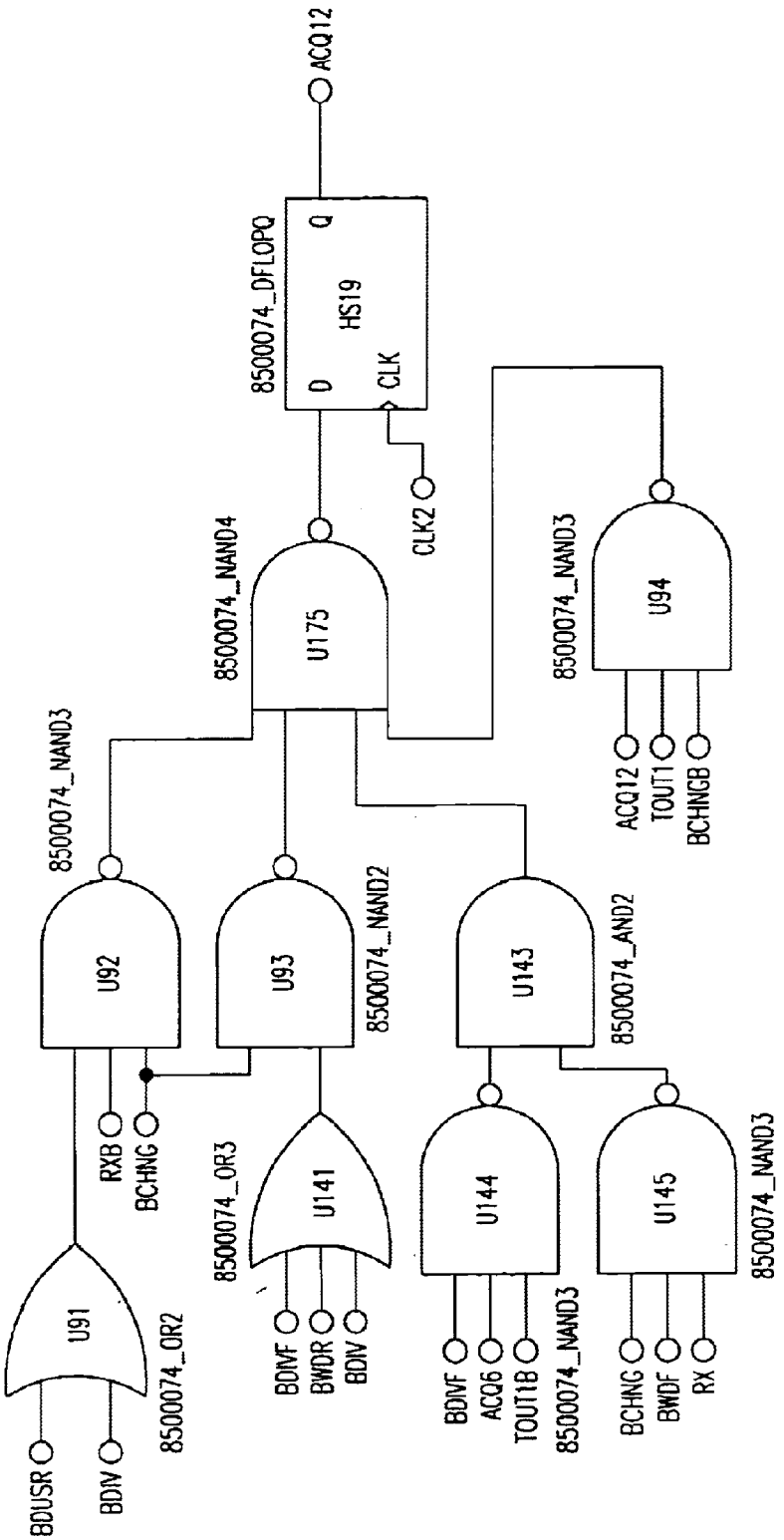

ACQ12
8500074_DFLOPQ
HS19
D
CLK
Q
CLK2
8500074_NAND4
U175
8500074_NAND3
U94
ACQ12
TOUT1
BCHNGB
8500074_NAND3
U92
U93
8500074_NAND2
U143
8500074_AND2
RXB
BCHNG
8500074_OR3
U141
U144
U145
8500074_NAND3
U91
8500074_OR2
BDUSR
BDIV
BDIVF
BWDR
BDIV
BDIVF
ACQ6
TOUT1B
BCHNG
BWDF
RX

FIG. 105T

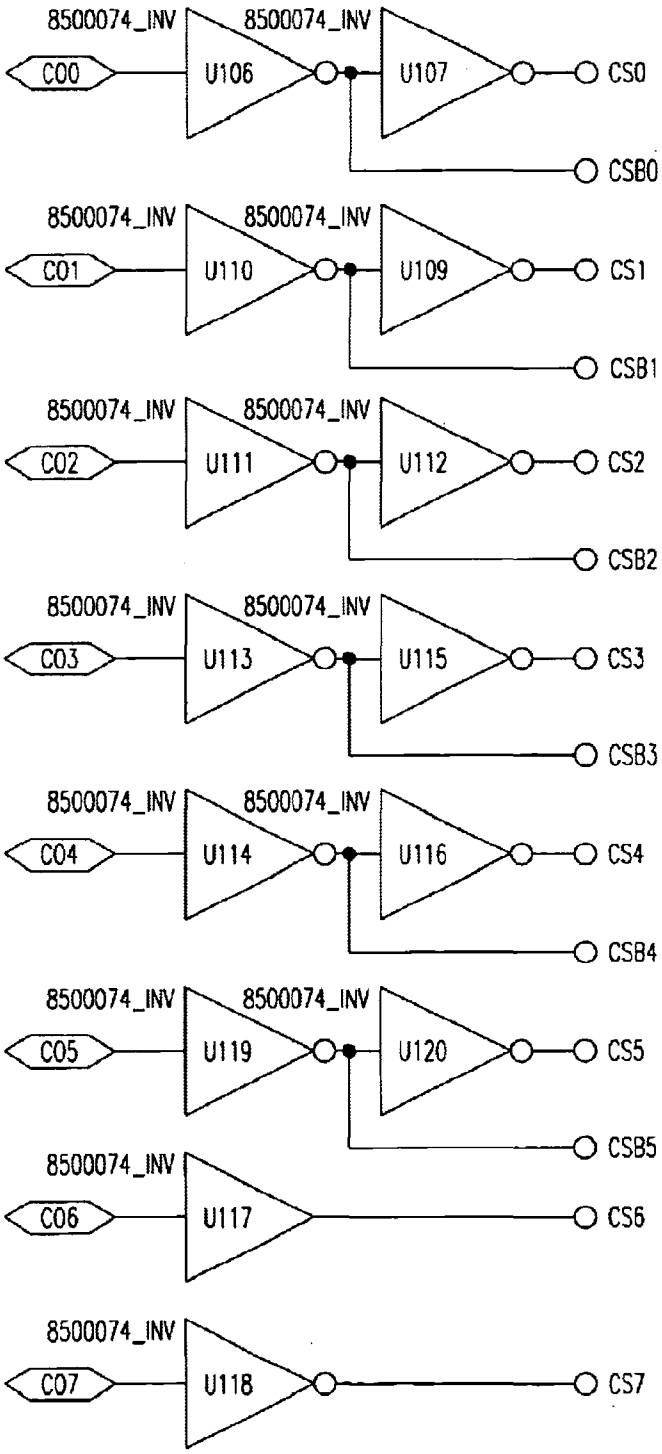

8500074_INV
C00
U106
8500074_INV
U107
CS0
CSB0
8500074_INV
C01
U110
8500074_INV
U109
CS1
CSB1
8500074_INV
C02
U111
8500074_INV
U112
CS2
CSB2
8500074_INV
C03
U113
8500074_INV
U115
CS3
CSB3
8500074_INV
C04
U114
8500074_INV
U116
CS4
CSB4
8500074_INV
C05
U119
8500074_INV
U120
CS5
CSB5
8500074_INV
C06
U117
CS6
8500074_INV
C07
U118
CS7

FIG.105U

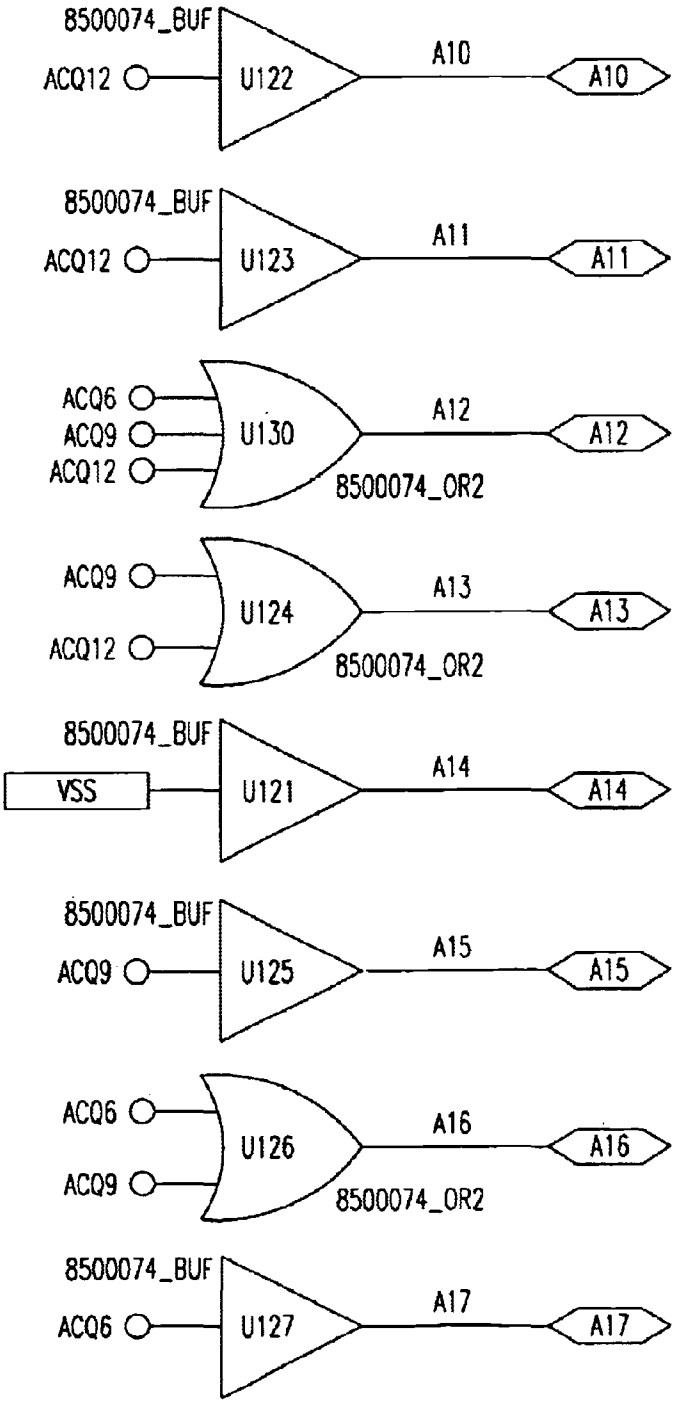

8500074_BUF
ACQ12
U122
A10
A10
8500074_BUF
ACQ12
U123
A11
A11
ACQ6
ACQ9
ACQ12
U130
A12
A12
8500074_OR2
ACQ9
ACQ12
U124
A13
A13
8500074_OR2
8500074_BUF
VSS
U121
A14
A14
8500074_BUF
ACQ9
U125
A15
A15
ACQ6
ACQ9
U126
A16
A16
8500074_OR2
8500074_BUF
ACQ6
U127
A17
A17

FIG.105V

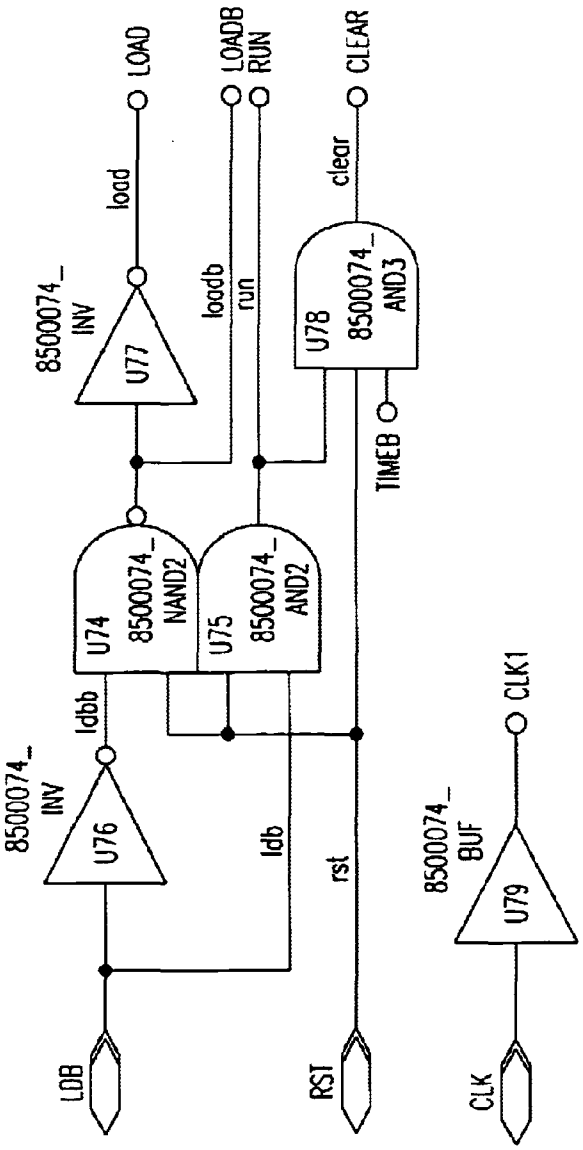

LOAD
LOADB
RUN
CLEAR
load
clear
loadb
run
8500074_
INV
U77
U78
8500074_
AND3
TIMEB
U74
8500074_
NAND2
U75
8500074_
AND2
ldbb
8500074_
INV
U76
ldb
rst
8500074_
BUF
U79
CLK1
LDB
RST
CLK

FIG.106A

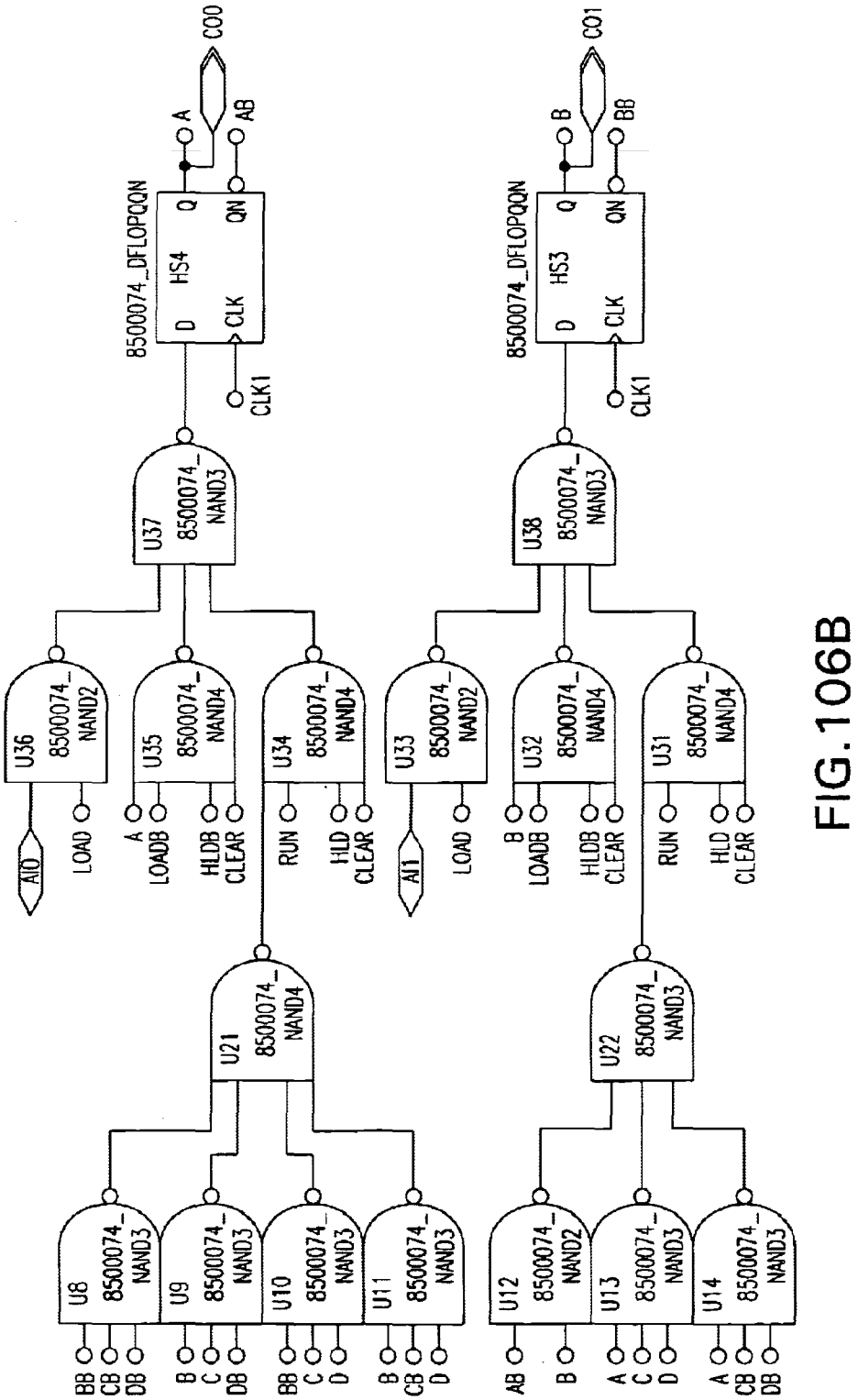

CO0
A
AB
8500074_DFLOPQQN
D
HS4
Q
QN
CLK
CLK1
CO1
B
BB
HS3
U37
U38
8500074_NAND3
U36
U35
U34
U33
U32
U31
8500074_NAND2
8500074_NAND4
AI0
AI1
LOAD
LOADB
HLDB
CLEAR
RUN
HLD
U21
U22
U8
U9
U10
U11
U12
U13
U14
8500074_NAND3
BB
CB
DB
B
C
D
AB
A

FIG. 106B

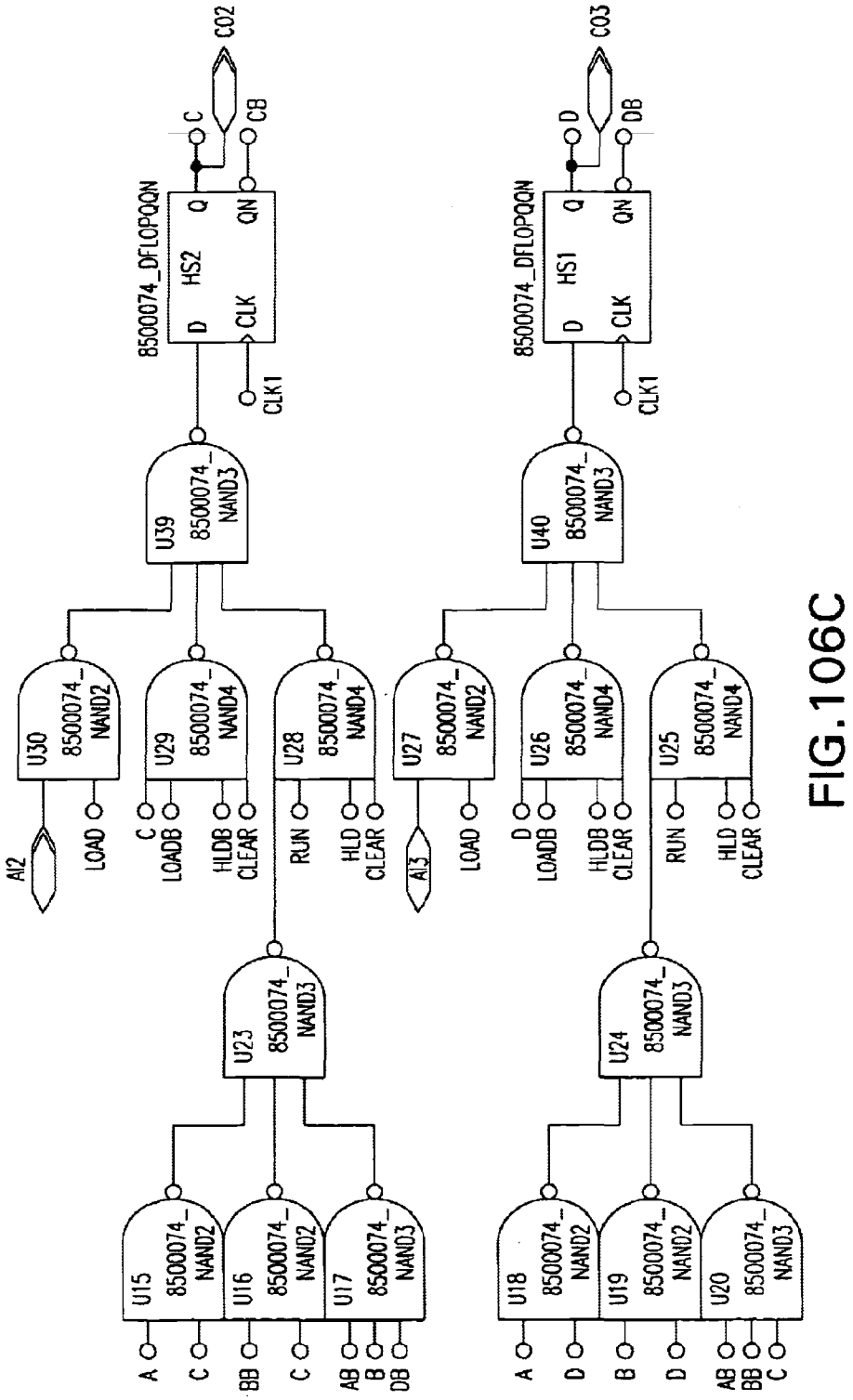

C02
C
CB
8500074_DFLOPQQN
HS2
D
Q
QN
CLK
CLK1
C03
D
DB
HS1
U39 8500074_NAND3
U40 8500074_NAND3
U30 8500074_NAND2
U29 8500074_NAND4
U28 8500074_NAND4
U27 8500074_NAND2
U26 8500074_NAND4
U25 8500074_NAND4
A12
A13
LOAD
LOADB
HLDB
CLEAR
RUN
HLD
U23 8500074_NAND3
U24 8500074_NAND3
U15 8500074_NAND2
U16 8500074_NAND2
U17 8500074_NAND3
U18 8500074_NAND2
U19 8500074_NAND2
U20 8500074_NAND3
A
C
BB
AB
B
DB
D

FIG.106C

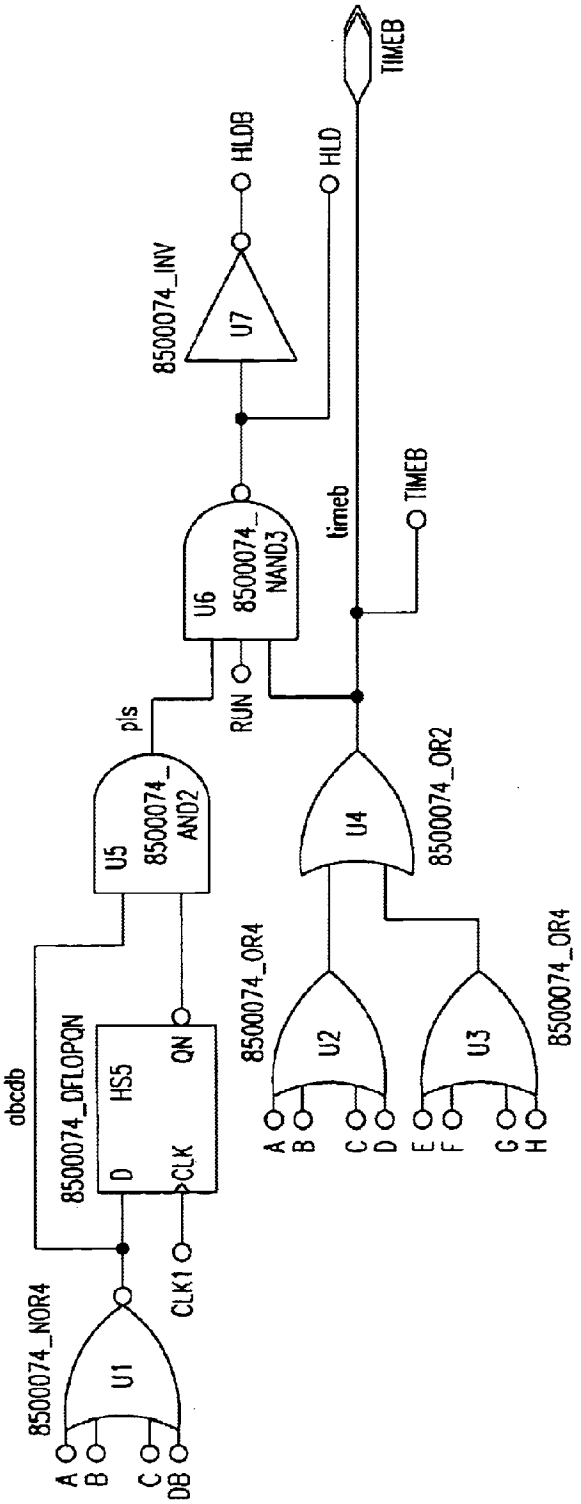

TIMEB
HLDB
HLD
8500074_INV
U7
timeb
TIMEB
U6
8500074_
NAND3
RUN
pls
U5
8500074_
AND2
U4
8500074_OR2
8500074_OR4
U2
A
B
C
D
8500074_OR4
U3
E
F
G
H
abcdb
8500074_DFLOPQN
HS5
D
CLK
QN
CLK1
8500074_NOR4
U1
A
B
C
DB

FIG.106D

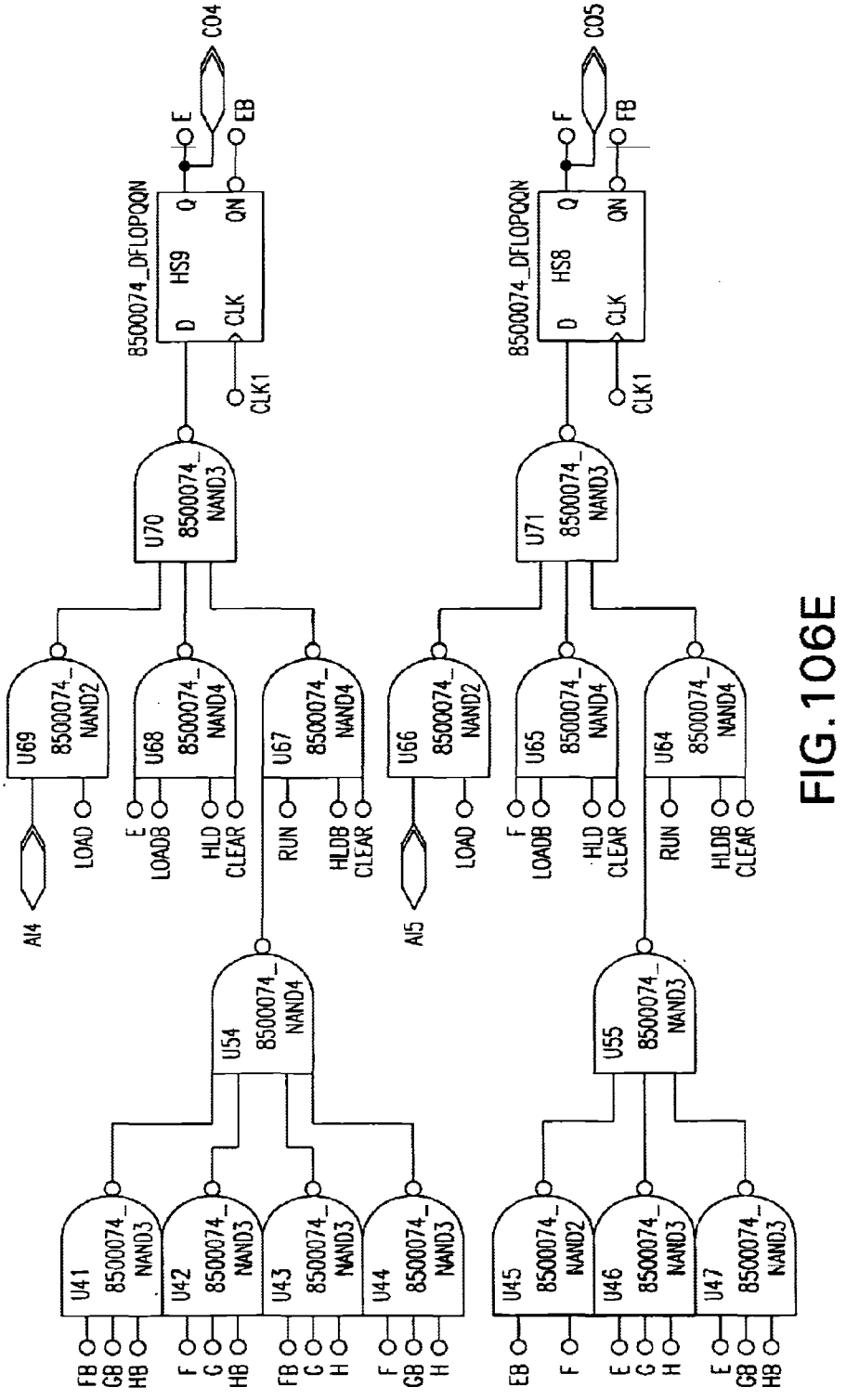
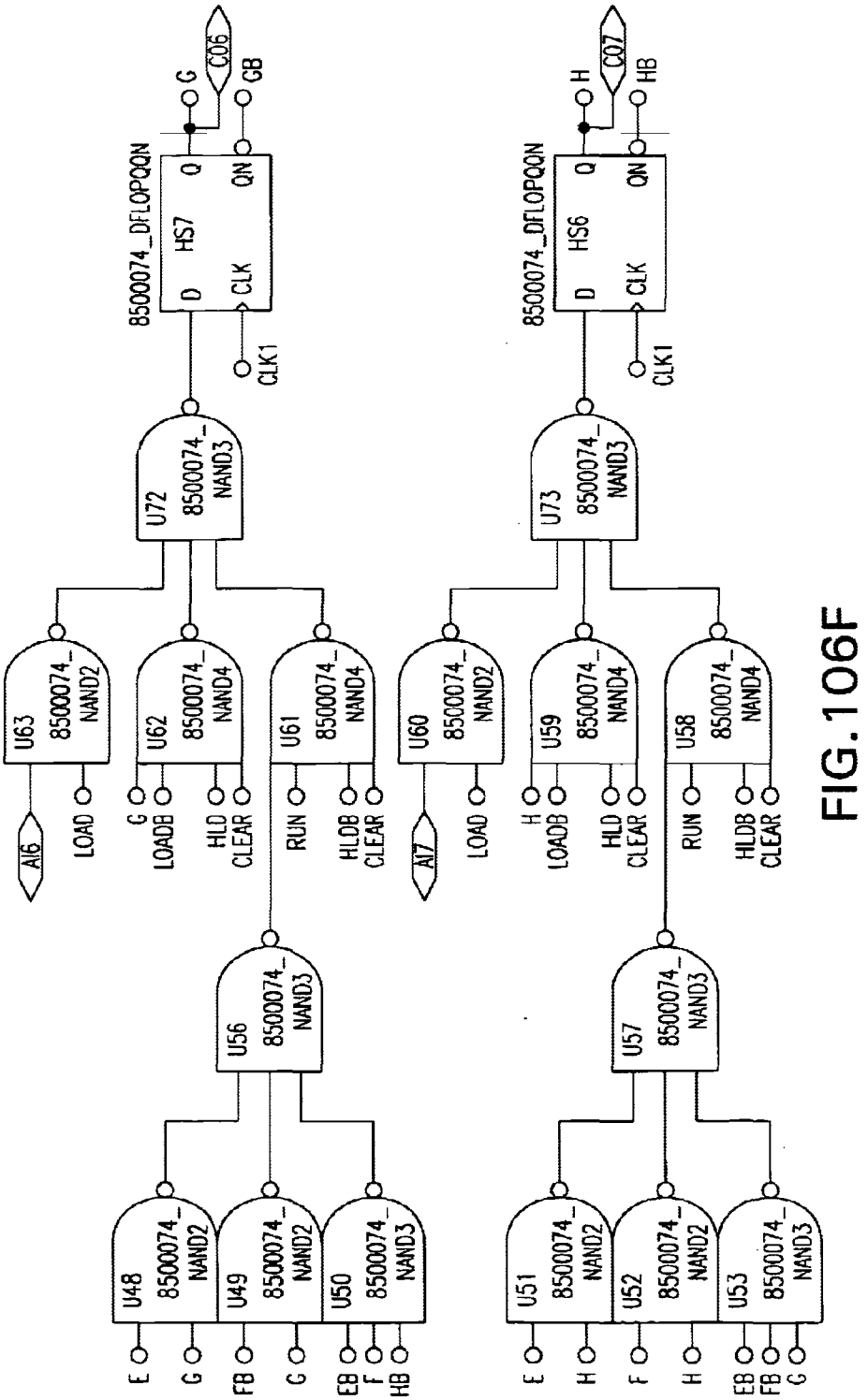

C04
C05
E
EB
F
FB
8500074_DFLOPQQN
HS9
HS8
D
Q
QN
CLK
CLK1
U70
U71
8500074_NAND3
U69
U68
U67
U66
U65
U64
8500074_NAND2
8500074_NAND4
A14
A15
LOAD
LOADB
HLD
CLEAR
HLDB
RUN
U54
U55
U41
U42
U43
U44
U45
U46
U47
FB
GB
HB
F
G
H
EB
E

FIG.106E


C06
G
GB
8500074_DFLOPQQN
HS7
D
Q
QN
CLK
CLK1
C07
H
HB
HS6
U72
U73
8500074_NAND3
U63
U60
8500074_NAND2
U62
U59
U58
8500074_NAND4
U61
A16
A17
LOAD
G
LOADB
H
HLD
CLEAR
RUN
HLDB
U56
U57
U48
U49
U50
U51
U52
U53
E
F
FB
EB
HB
FIG.106F

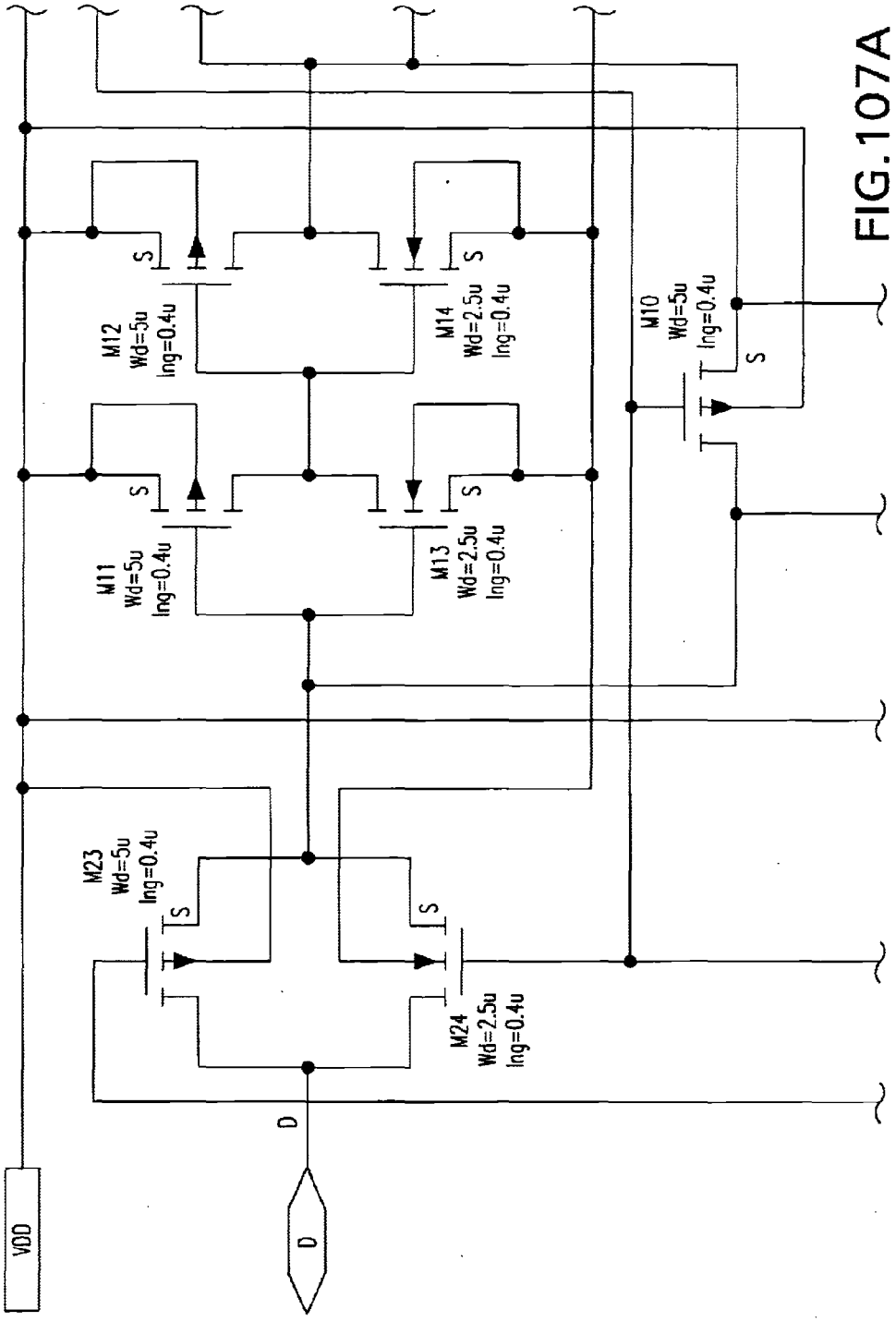

M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.107A

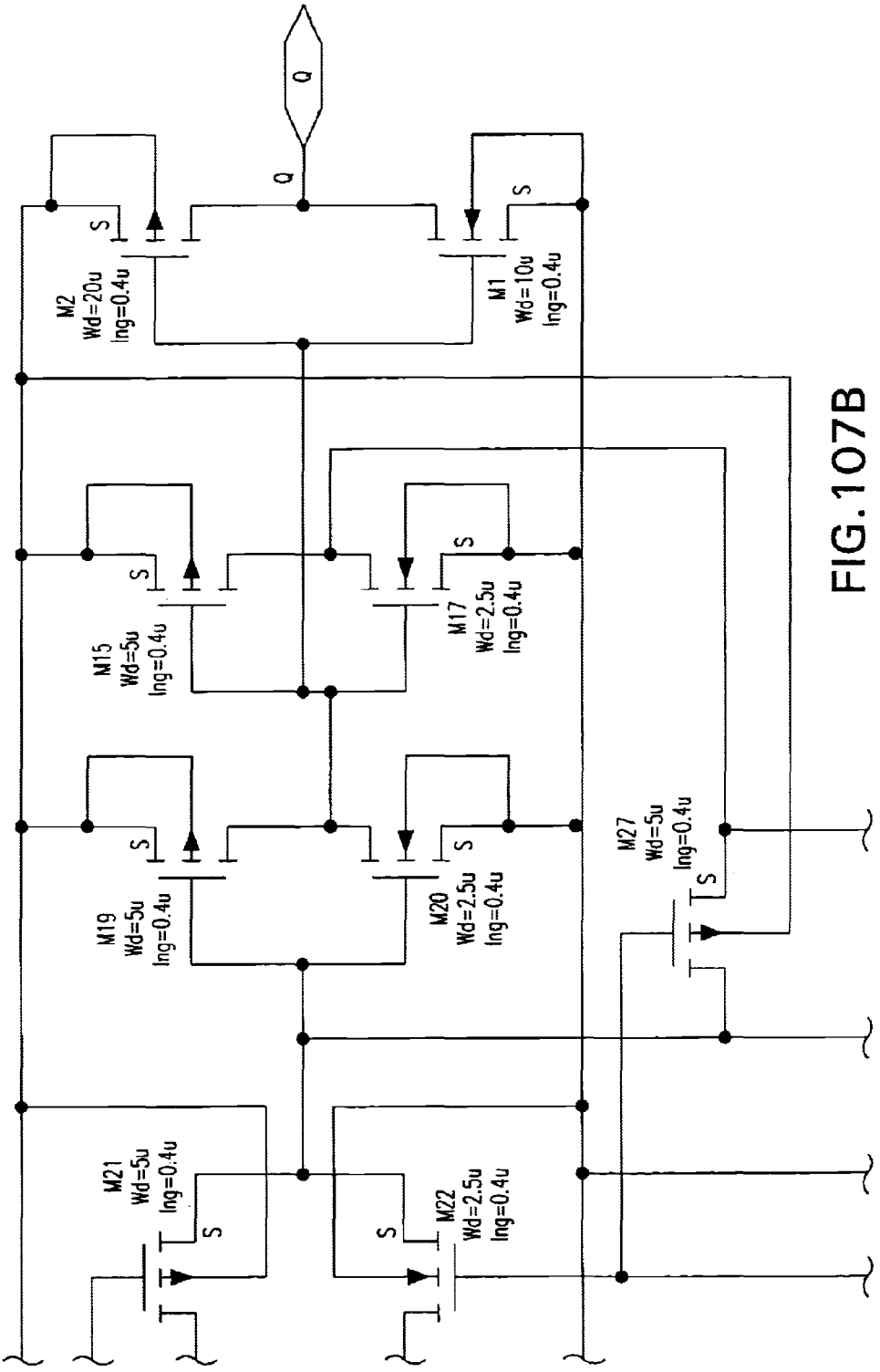

Q
Q
S
M2
Wd=20u
lng=0.4u
S
M1
Wd=10u
lng=0.4u
S
M15
Wd=5u
lng=0.4u
S
M17
Wd=2.5u
lng=0.4u
S
M19
Wd=5u
lng=0.4u
S
M20
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
S
M21
Wd=5u
lng=0.4u
S
S
M22
Wd=2.5u
lng=0.4u

FIG.107B

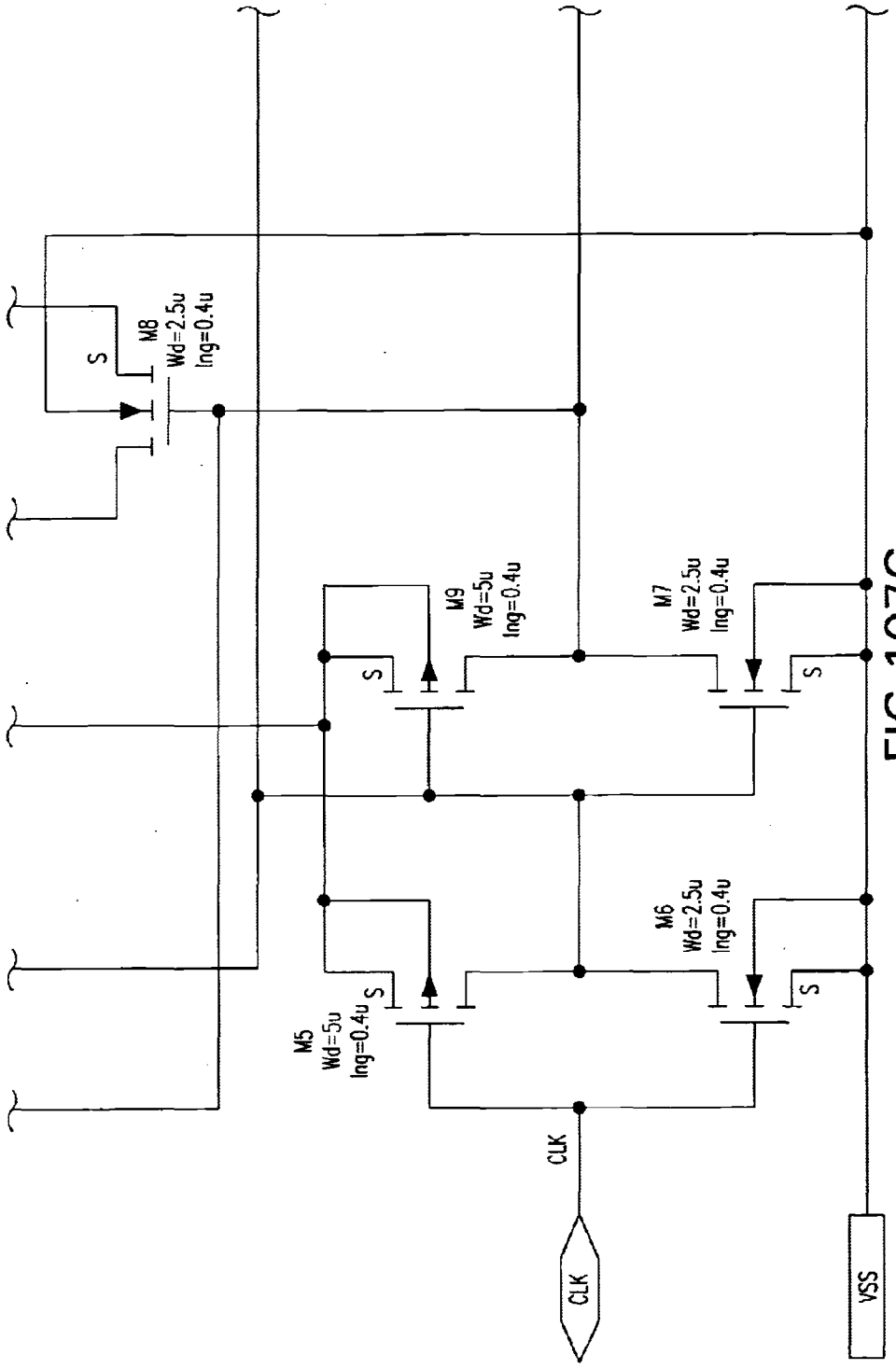

M8
Wd=2.5u
lng=0.4u
S
M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M5
Wd=5u
lng=0.4u
CLK
CLK
VSS

FIG.107C

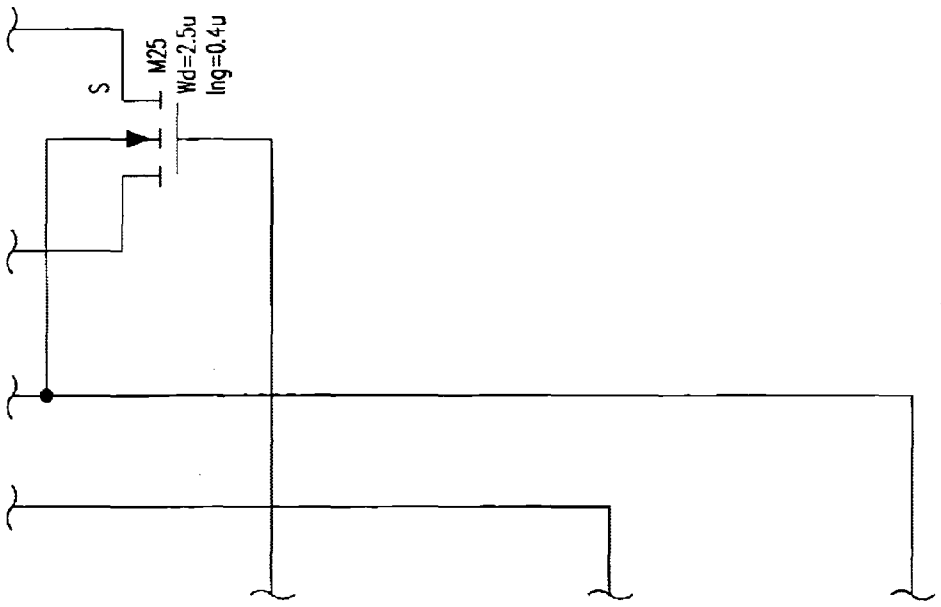


FIG.107D

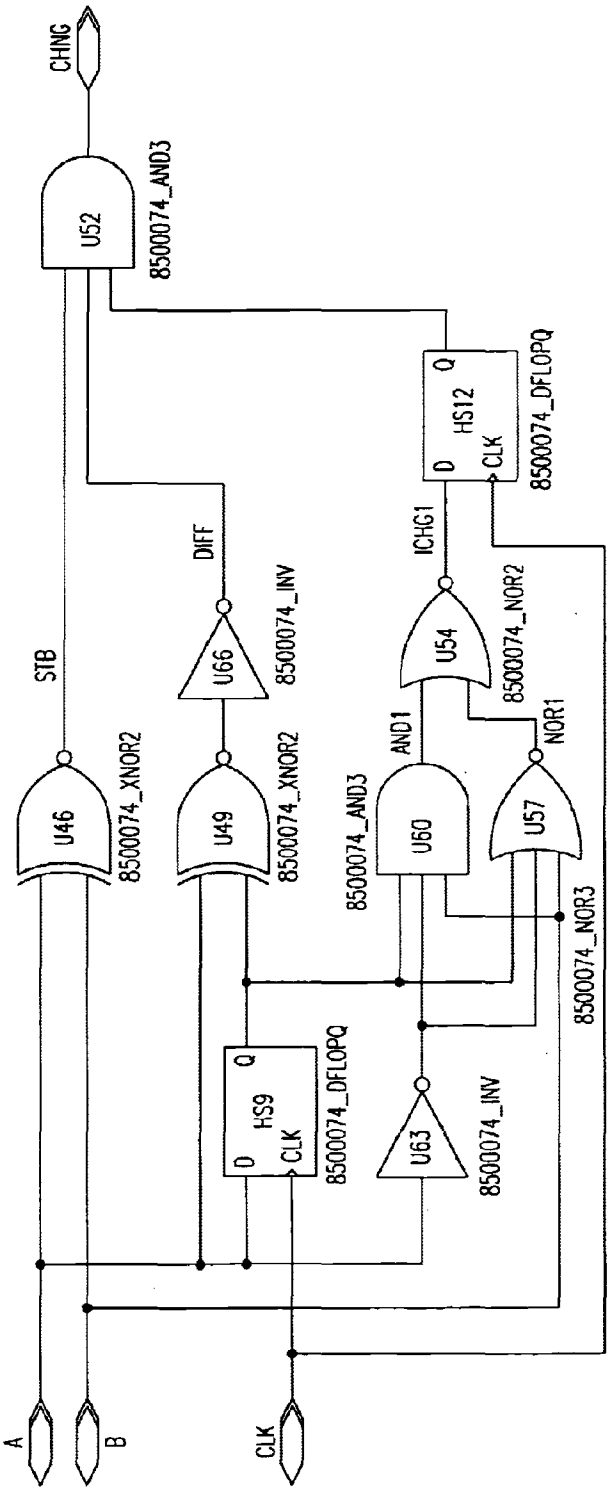

CHNG
U52
8500074_AND3
STB
DIFF
U66
8500074_INV
U46
8500074_XNOR2
U49
8500074_XNOR2
HS12
D
Q
CLK
8500074_DFLOPQ
ICHG1
U54
8500074_NOR2
AND1
NOR1
8500074_AND3
U60
U57
8500074_NOR3
HS9
D
Q
CLK
8500074_DFLOPQ
U63
8500074_INV
A
B
CLK

FIG.108

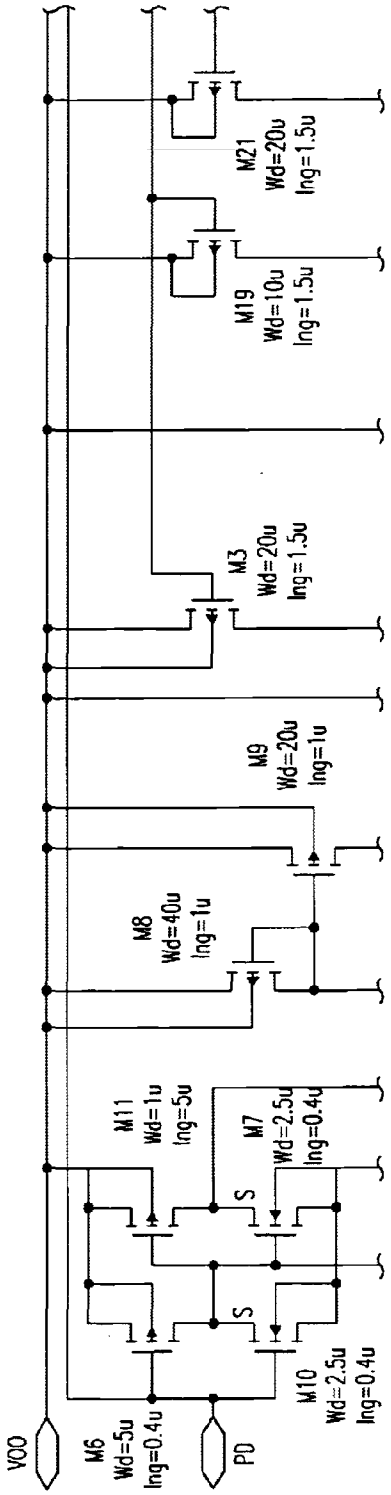

M21
Wd=20u
lng=1.5u
M19
Wd=10u
lng=1.5u
M3
Wd=20u
lng=1.5u
M9
Wd=20u
lng=1u
M8
Wd=40u
lng=1u
M11
Wd=1u
lng=5u
M7
Wd=2.5u
lng=0.4u
S
S
M10
Wd=2.5u
lng=0.4u
VDD
M6
Wd=5u
lng=0.4u
PD

FIG.109A

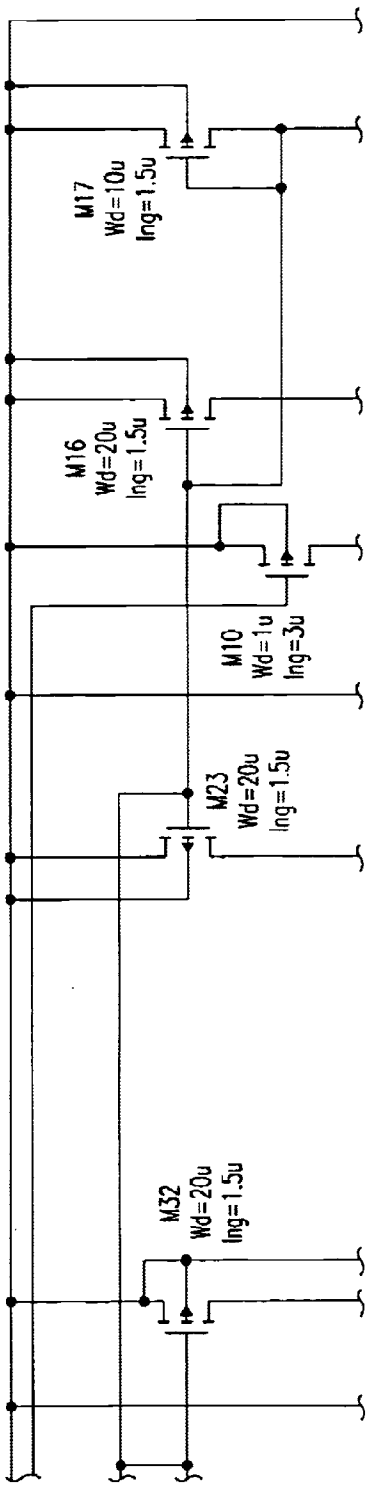

M17
Wd=10u
lng=1.5u
M16
Wd=20u
lng=1.5u
M10
Wd=1u
lng=3u
M23
Wd=20u
lng=1.5u
M32
Wd=20u
lng=1.5u

FIG.109B

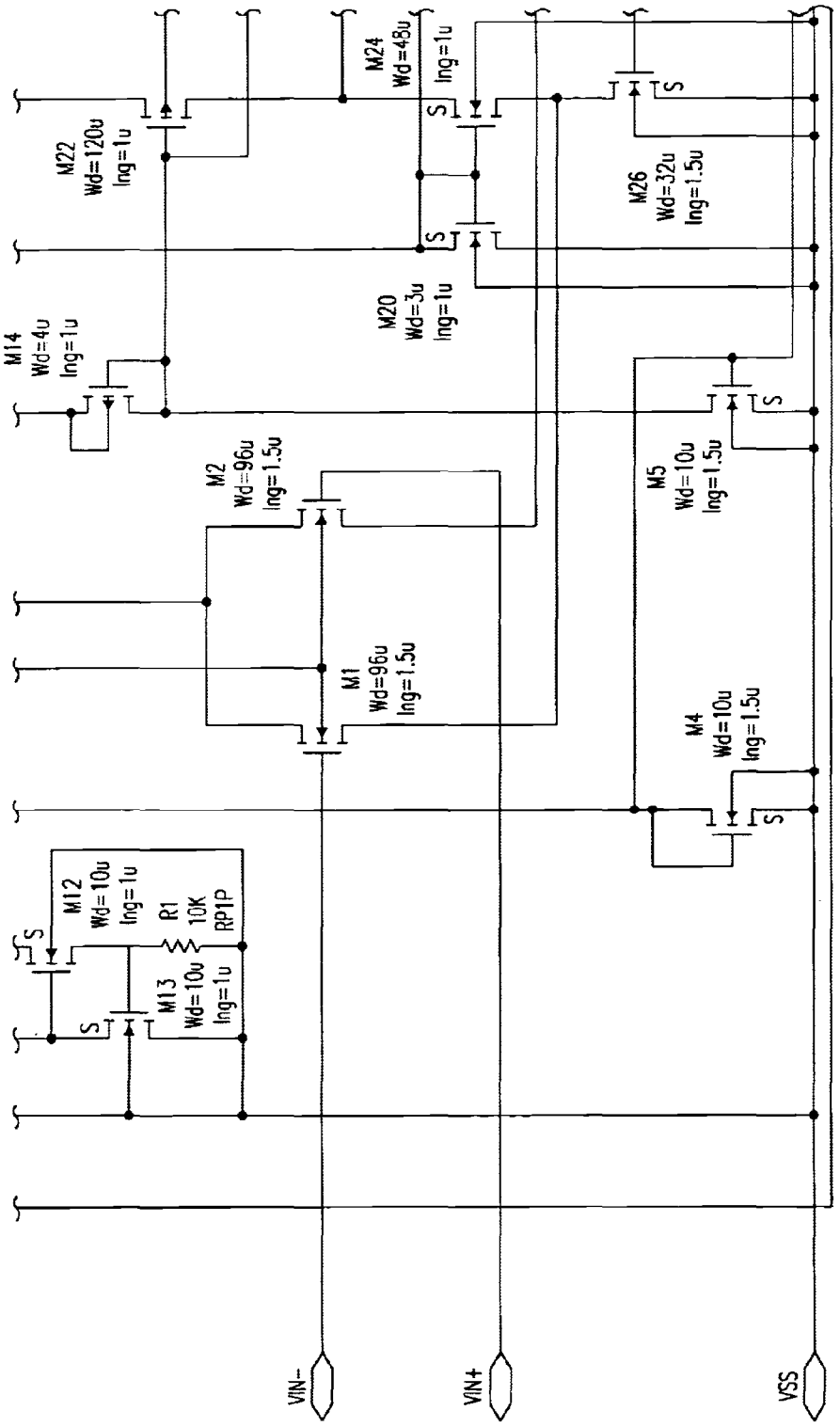

M24
Wd=48u
lng=1u
M22
Wd=120u
lng=1u
M26
Wd=32u
lng=1.5u
M20
Wd=3u
lng=1u
M14
Wd=4u
lng=1u
M2
Wd=96u
lng=1.5u
M5
Wd=10u
lng=1.5u
M1
Wd=96u
lng=1.5u
M4
Wd=10u
lng=1.5u
M12
Wd=10u
lng=1u
R1
10K
RPIP
M13
Wd=10u
lng=1u
S
VIN-
VIN+
VSS

FIG.109C

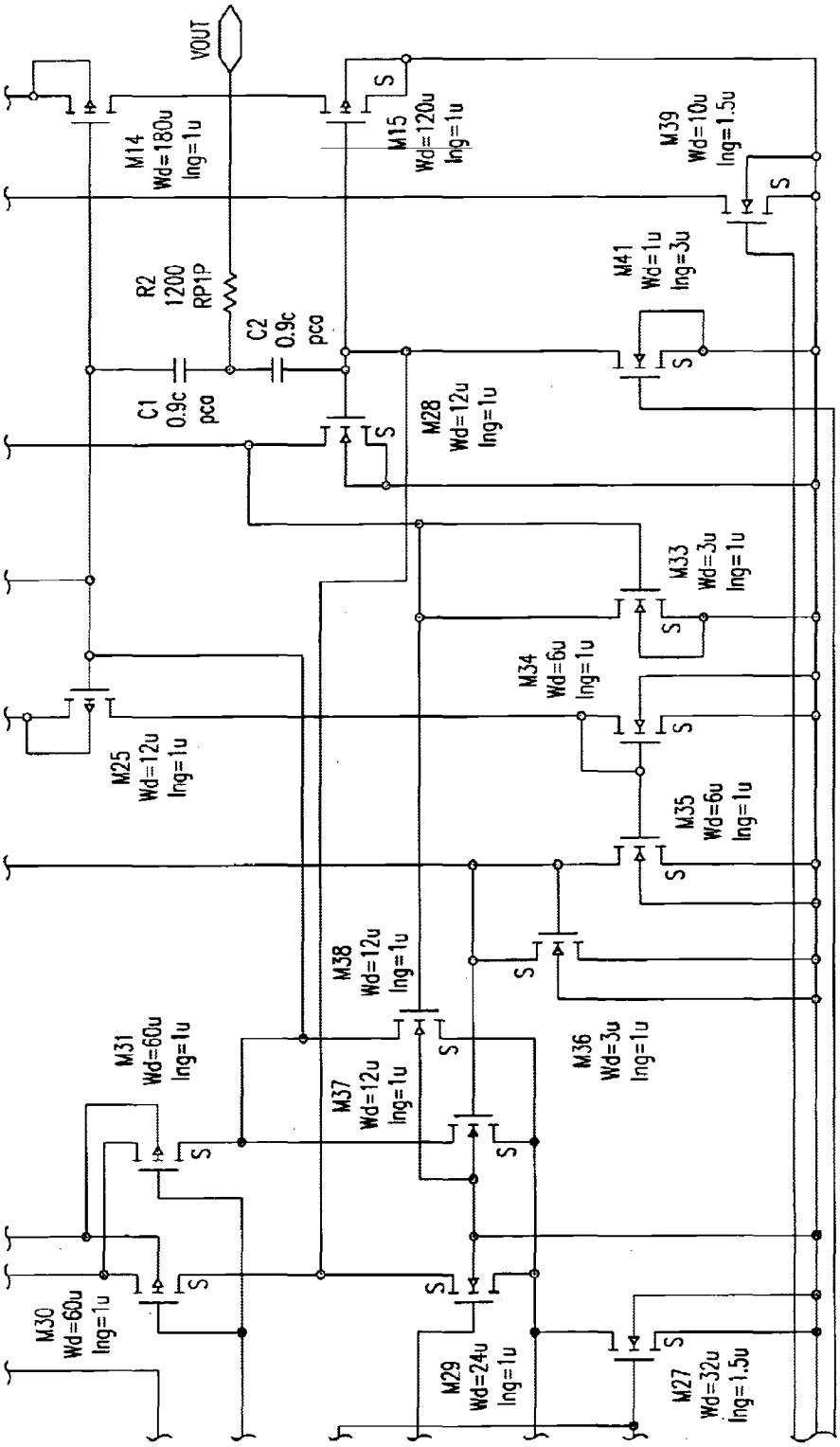

VOUT
M14 Wd=180u lng=1u
M15 Wd=120u lng=1u
M39 Wd=10u lng=1.5u
R2 1200 RP1P
C2 0.9c pca
C1 0.9c pca
M41 Wd=1u lng=3u
M28 Wd=12u lng=1u
M33 Wd=3u lng=1u
M34 Wd=6u lng=1u
M25 Wd=12u lng=1u
M35 Wd=6u lng=1u
M38 Wd=12u lng=1u
M31 Wd=60u lng=1u
M37 Wd=12u lng=1u
M36 Wd=3u lng=1u
M30 Wd=60u lng=1u
M29 Wd=24u lng=1u
M27 Wd=32u lng=1.5u

FIG. 109D

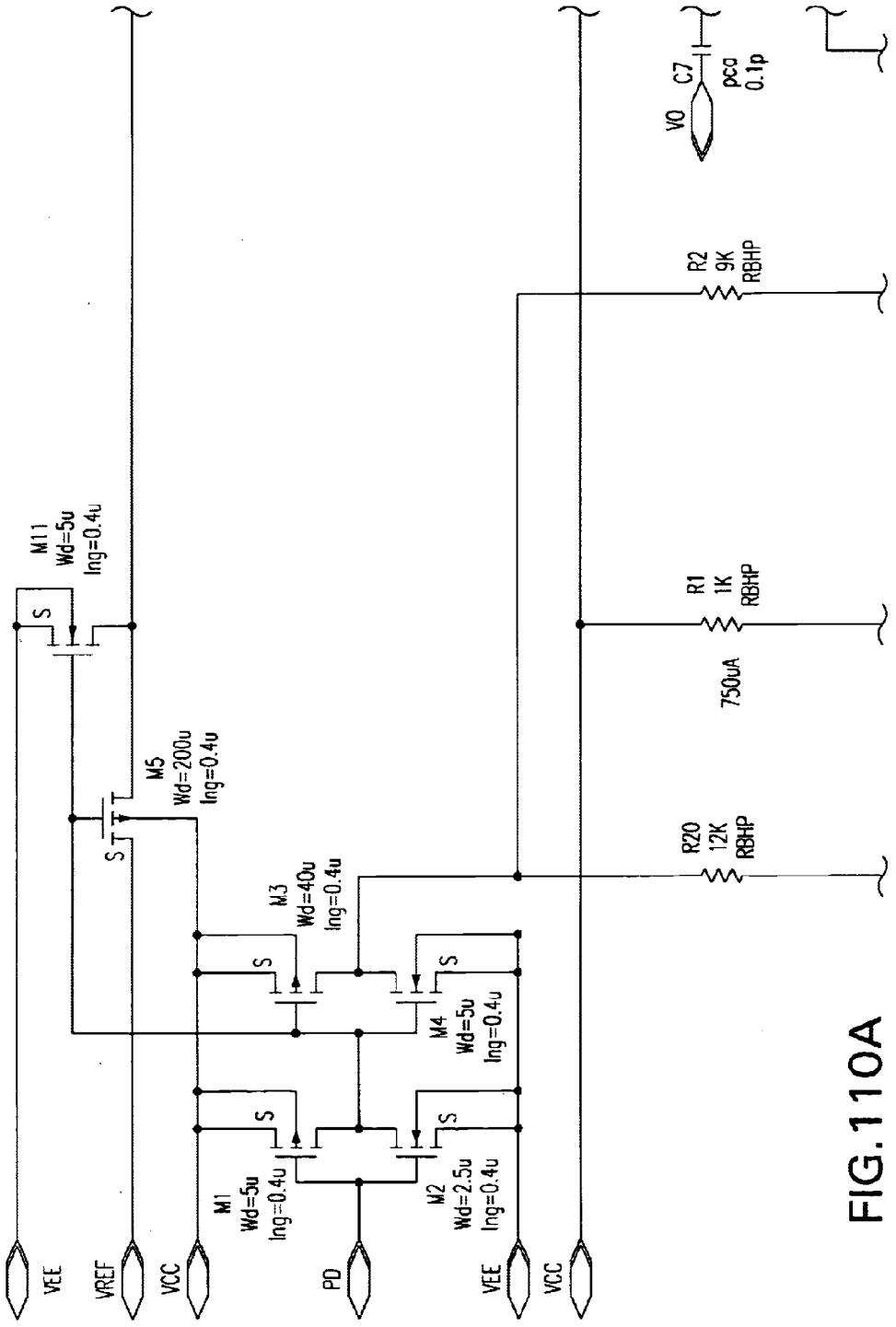

VEE
VREF
VCC
PD
VEE
VCC
M11 Wd=5u lng=0.4u
M5 Wd=200u lng=0.4u
M3 Wd=40u lng=0.4u
M4 Wd=5u lng=0.4u
M1 Wd=5u lng=0.4u
M2 Wd=2.5u lng=0.4u
S
R2 9K RBHP
R1 1K RBHP
750uA
R20 12K RBHP
V0
C7 pca 0.1p

FIG.110A

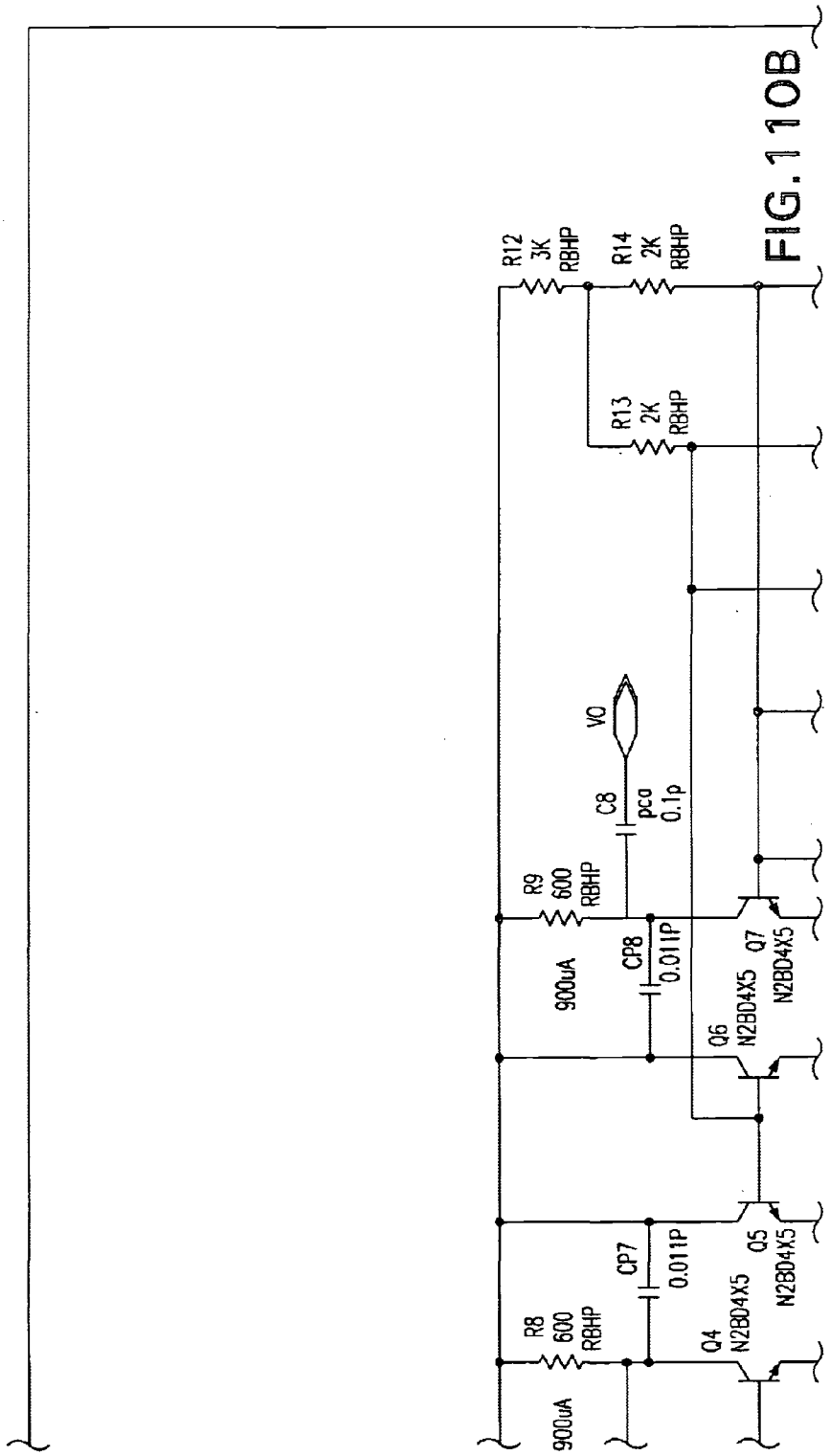

R12
3K
RBHP
R14
2K
RBHP
R13
2K
RBHP
VO
C8
pca
0.1p
R9
600
RBHP
900uA
CP8
0.011P
Q7
N2BD4X5
Q6
N2BD4X5
CP7
0.011P
Q5
N2BD4X5
R8
600
RBHP
900uA
Q4
N2BD4X5

FIG. 110B

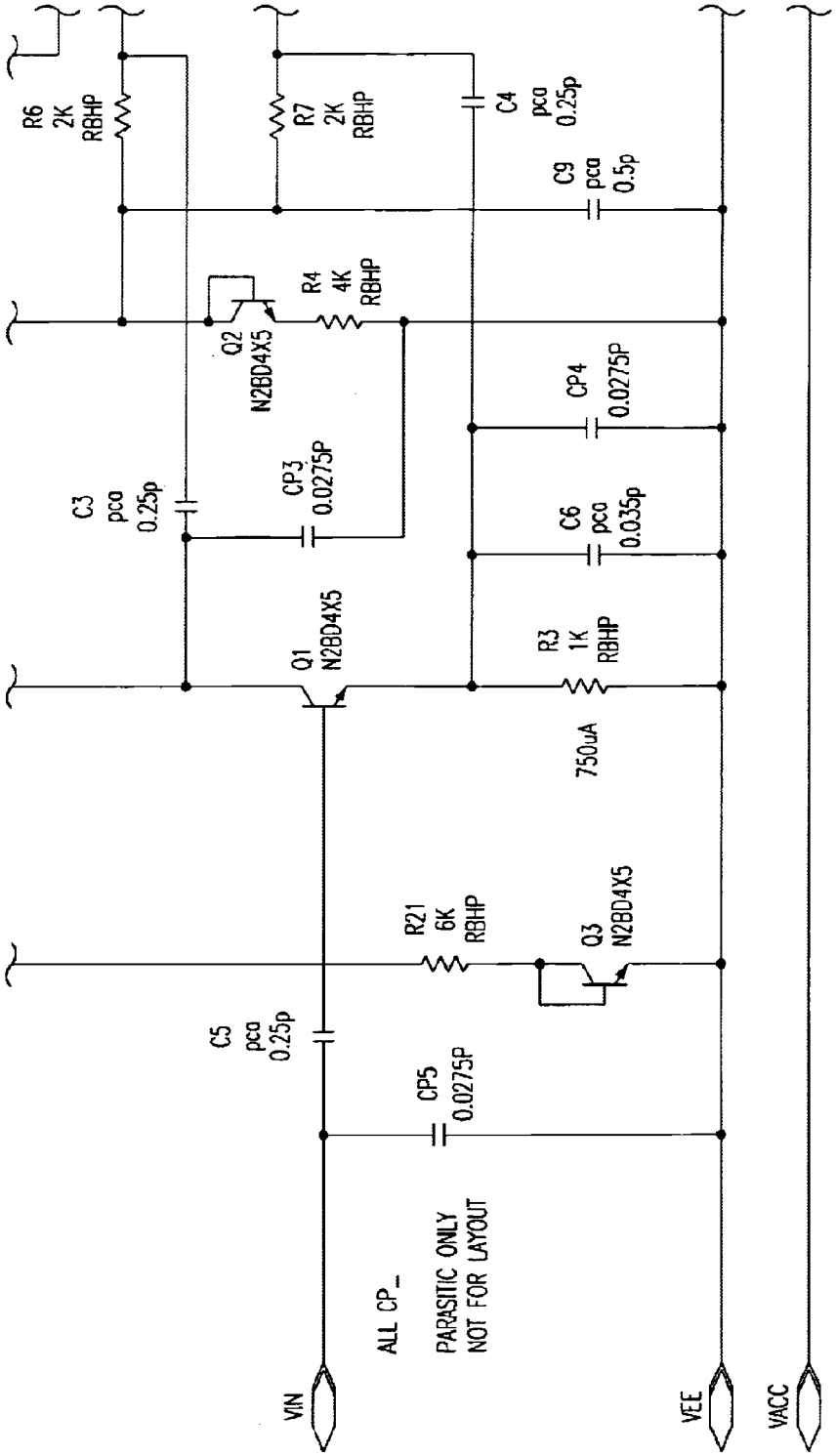

R6
2K
RBHP
R7
2K
RBHP
C4
pca
0.25p
C9
pca
0.5p
R4
4K
RBHP
Q2
N2BD4X5
CP4
0.0275P
C3
pca
0.25p
CP3
0.0275P
C6
pca
0.035p
Q1
N2BD4X5
R3
1K
RBHP
750uA
R21
6K
RBHP
Q3
N2BD4X5
C5
pca
0.25p
CP5
0.0275P
ALL CP_
PARASITIC ONLY
NOT FOR LAYOUT
VIN
VEE
VACC

FIG.110C

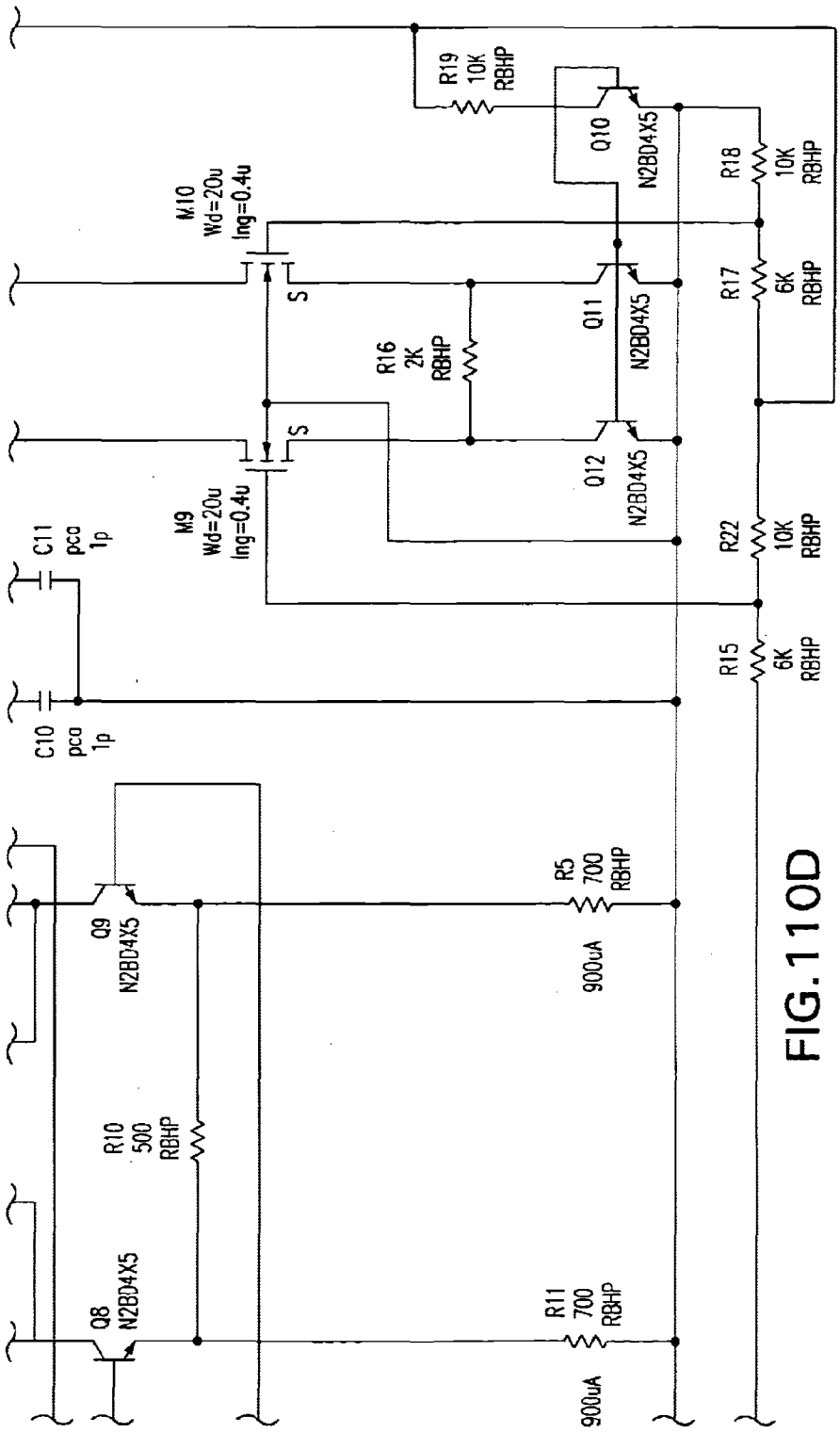

R19
10K
RBHP
Q10
N2BD4X5
R18
10K
RBHP
M10
Wd=20u
lng=0.4u
S
Q11
N2BD4X5
R17
6K
RBHP
R16
2K
RBHP
S
Q12
N2BD4X5
M9
Wd=20u
lng=0.4u
C11
pca
1p
R22
10K
RBHP
R15
6K
RBHP
C10
pca
1p
R5
700
RBHP
Q9
N2BD4X5
900uA
R10
500
RBHP
Q8
N2BD4X5
R11
700
RBHP
900uA

FIG.110D

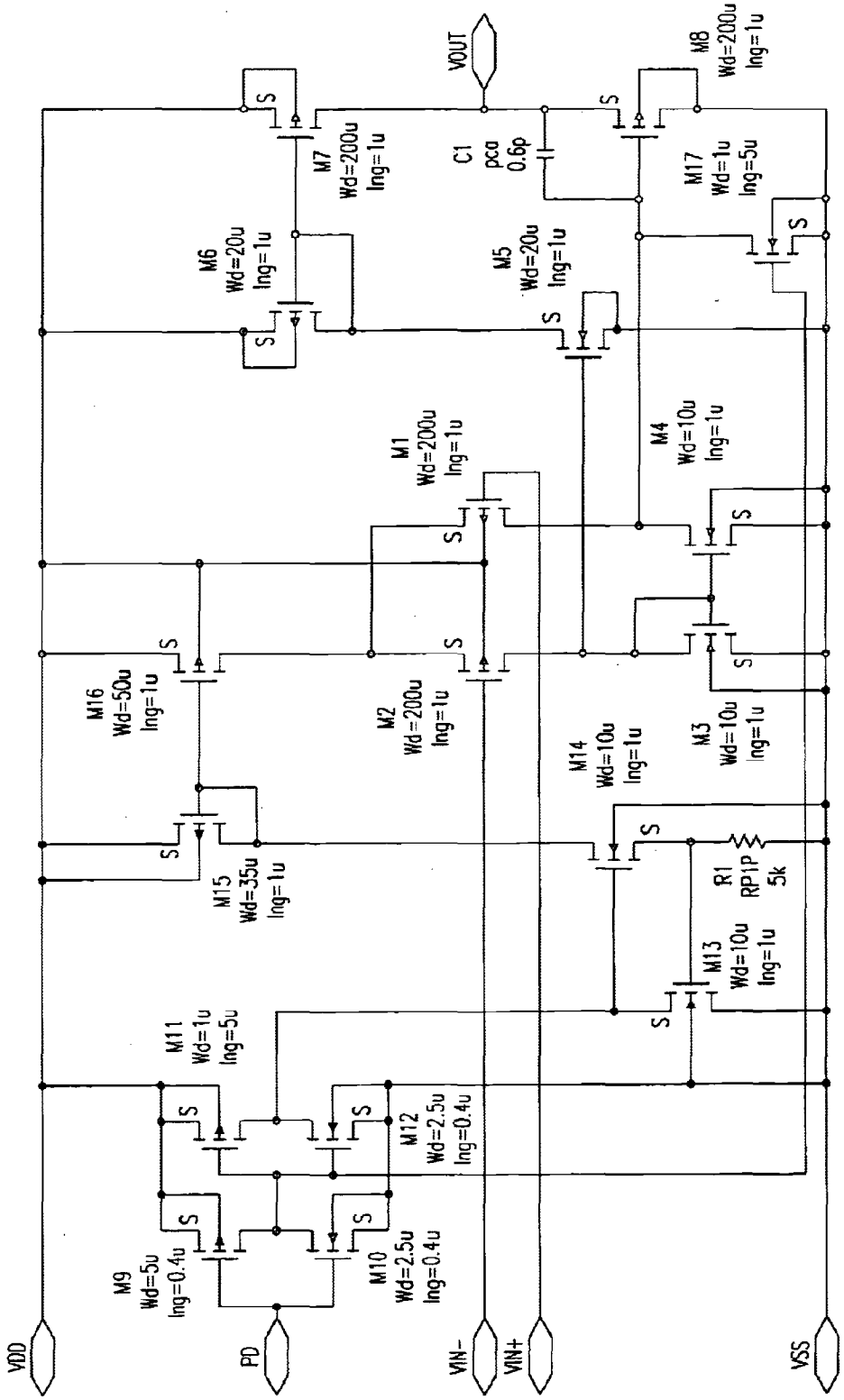

VOUT
M8 Wd=200u lng=1u
M7 Wd=200u lng=1u
C1 pca 0.6p
M17 Wd=1u lng=5u
M6 Wd=20u lng=1u
M5 Wd=20u lng=1u
M1 Wd=200u lng=1u
M4 Wd=10u lng=1u
M16 Wd=50u lng=1u
M2 Wd=200u lng=1u
M3 Wd=10u lng=1u
M14 Wd=10u lng=1u
M15 Wd=35u lng=1u
R1 RP1P 5k
M13 Wd=10u lng=1u
M11 Wd=1u lng=5u
M12 Wd=2.5u lng=0.4u
M9 Wd=5u lng=0.4u
M10 Wd=2.5u lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG. 111

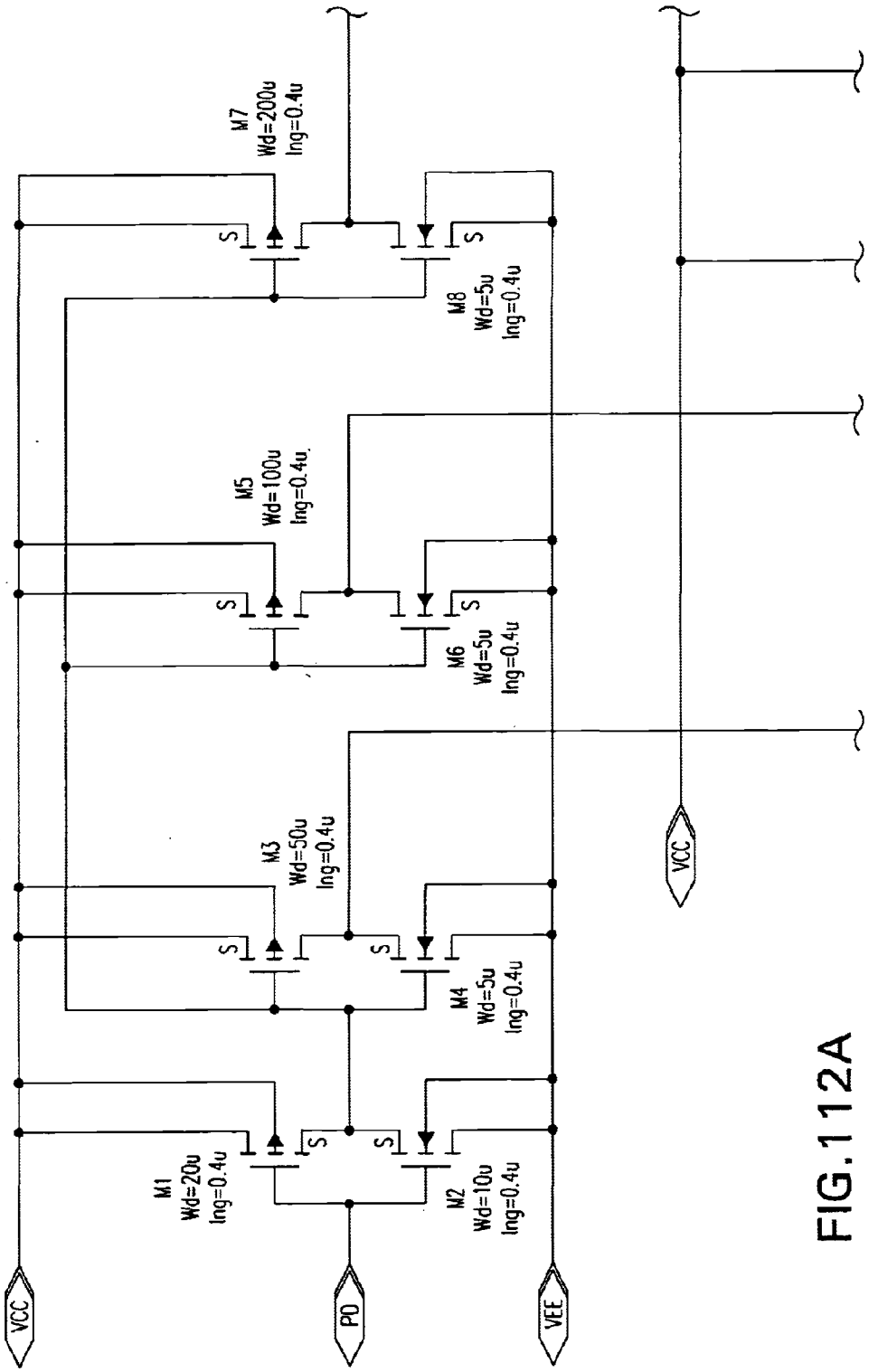
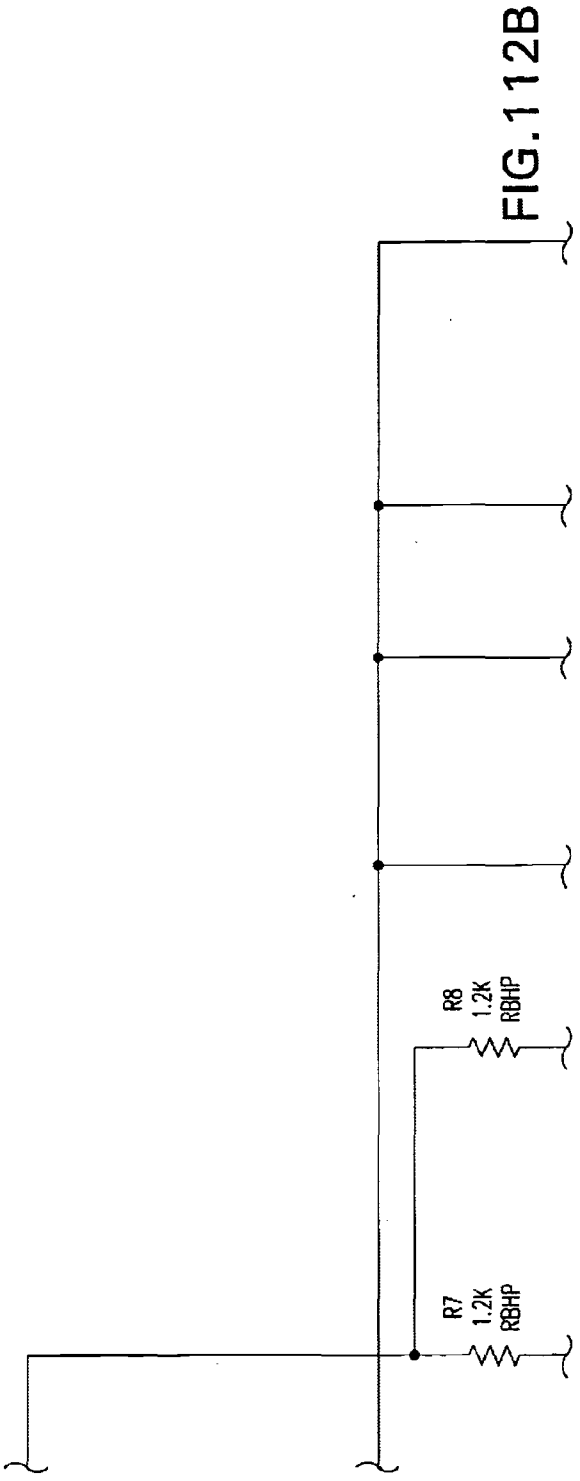

M7
Wd=200u
lng=0.4u
M8
Wd=5u
lng=0.4u
M5
Wd=100u
lng=0.4u
M6
Wd=5u
lng=0.4u
M3
Wd=50u
lng=0.4u
M4
Wd=5u
lng=0.4u
M1
Wd=20u
lng=0.4u
M2
Wd=10u
lng=0.4u
S
VCC
PD
VEE
VCC

FIG.112A

FIG.112B



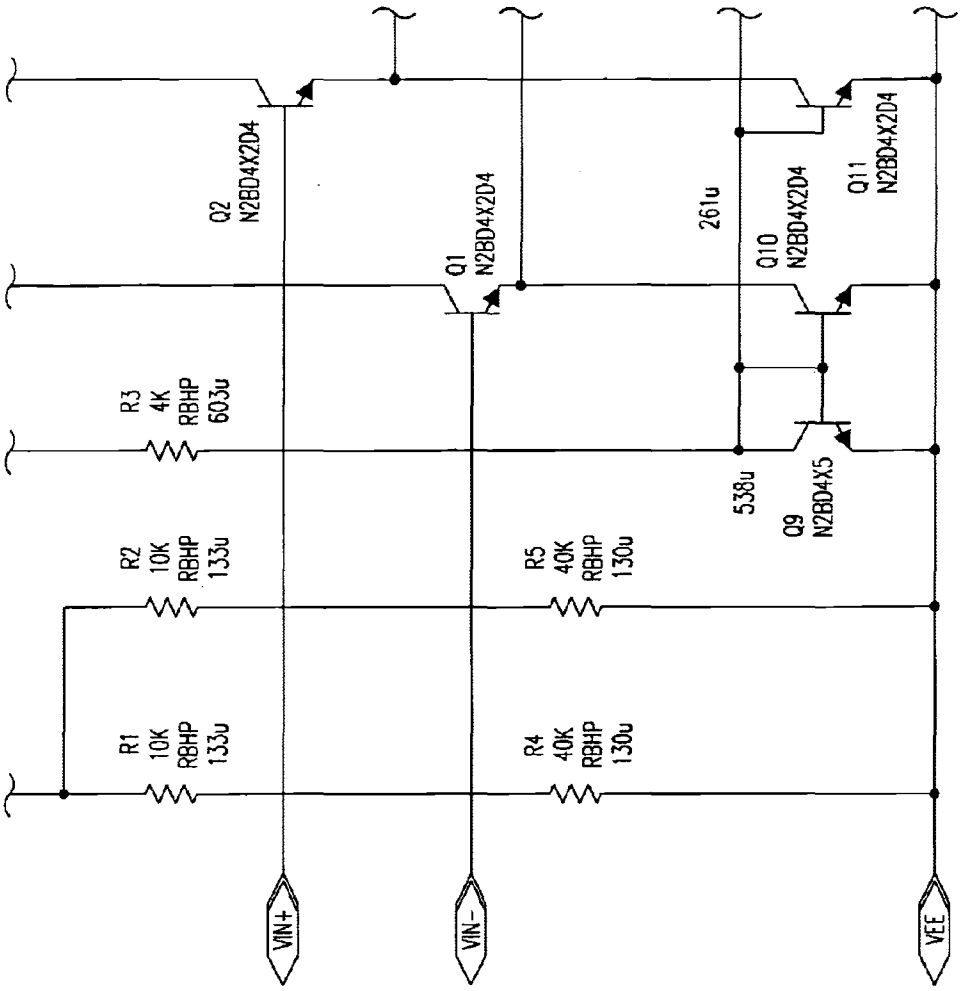

Q2
N2BD4X2D4
Q1
N2BD4X2D4
261u
Q10
N2BD4X2D4
Q11
N2BD4X2D4
R3
4K
RBHP
603u
538u
Q9
N2BD4X5
R2
10K
RBHP
133u
R5
40K
RBHP
130u
R1
10K
RBHP
133u
R4
40K
RBHP
130u
VIN+
VIN-
VEE

FIG.112C

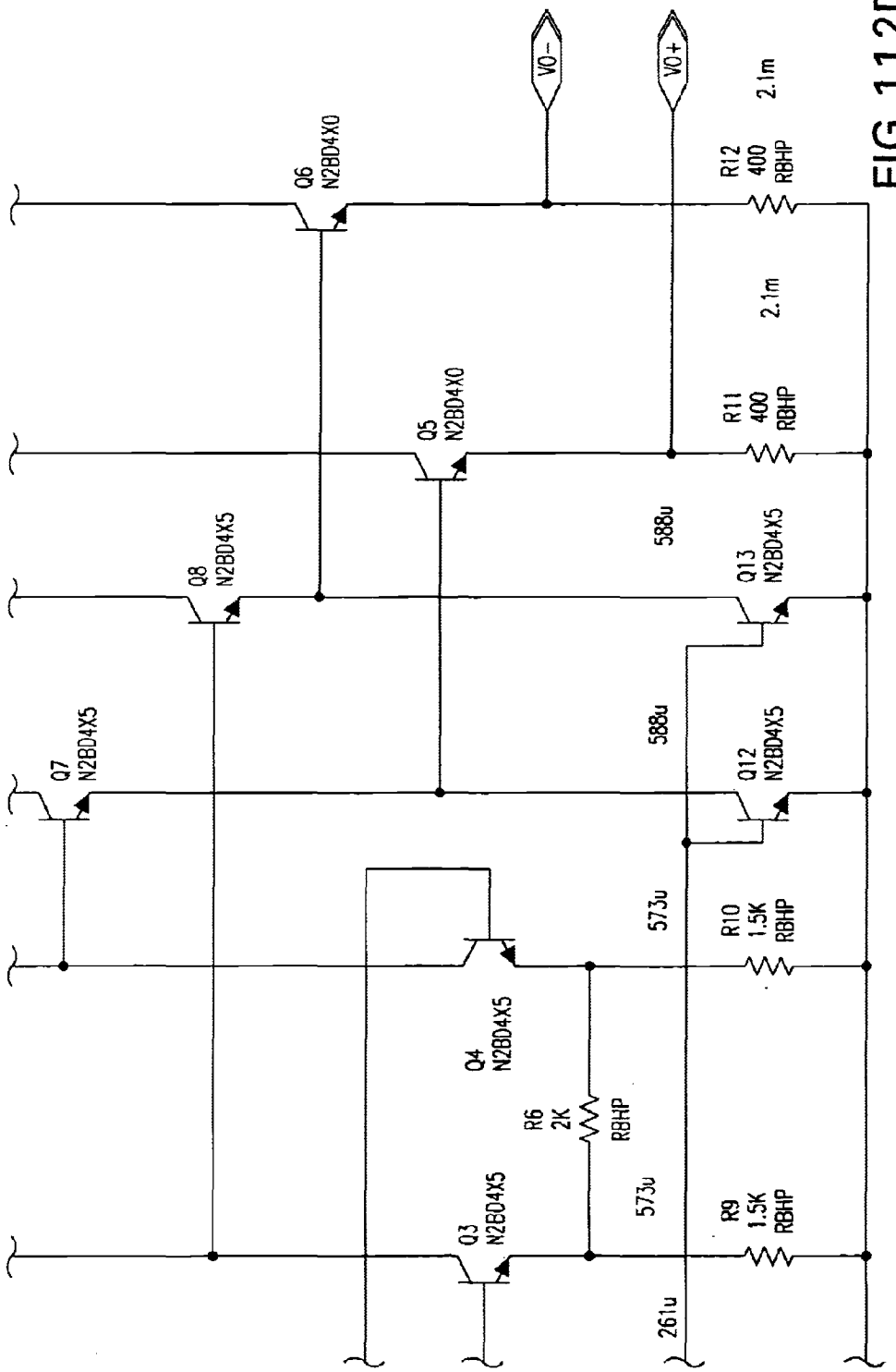

VO-
VO+
Q6 N2BD4X0
R12 400 RBHP
2.1m
Q5 N2BD4X0
R11 400 RBHP
2.1m
Q8 N2BD4X5
Q13 N2BD4X5
588u
Q7 N2BD4X5
Q12 N2BD4X5
588u
R10 1.5K RBHP
573u
Q4 N2BD4X5
R6 2K RBHP
Q3 N2BD4X5
R9 1.5K RBHP
573u
261u

FIG. 112D

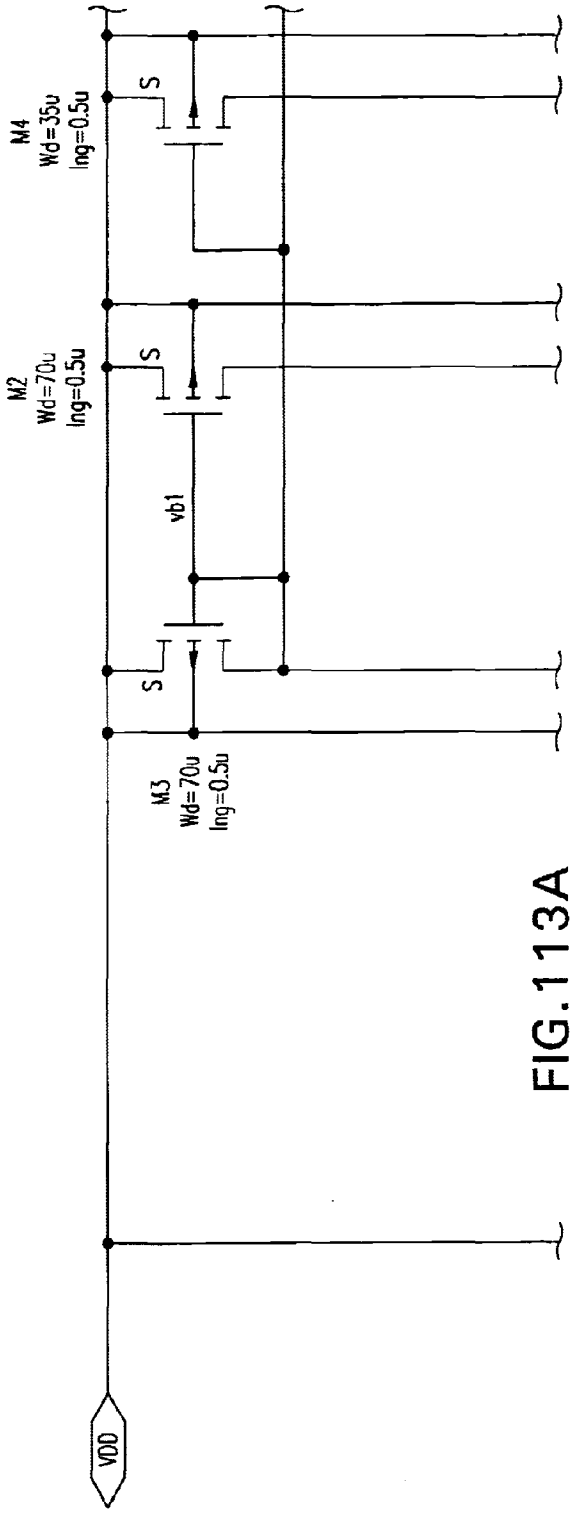


FIG. 113A

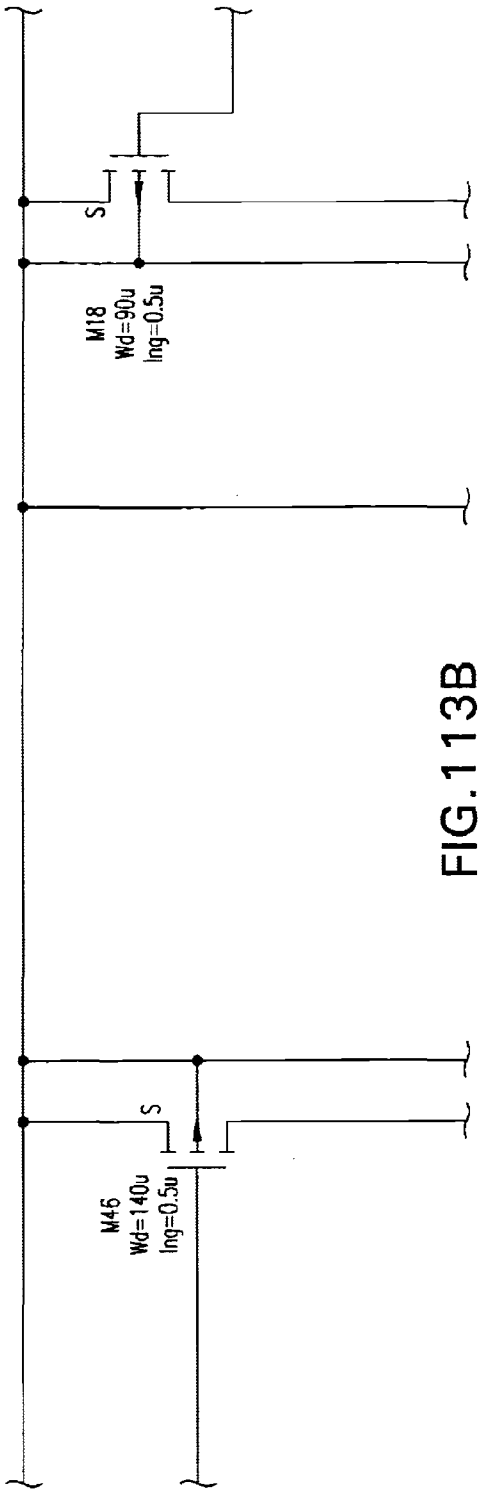


FIG.113B

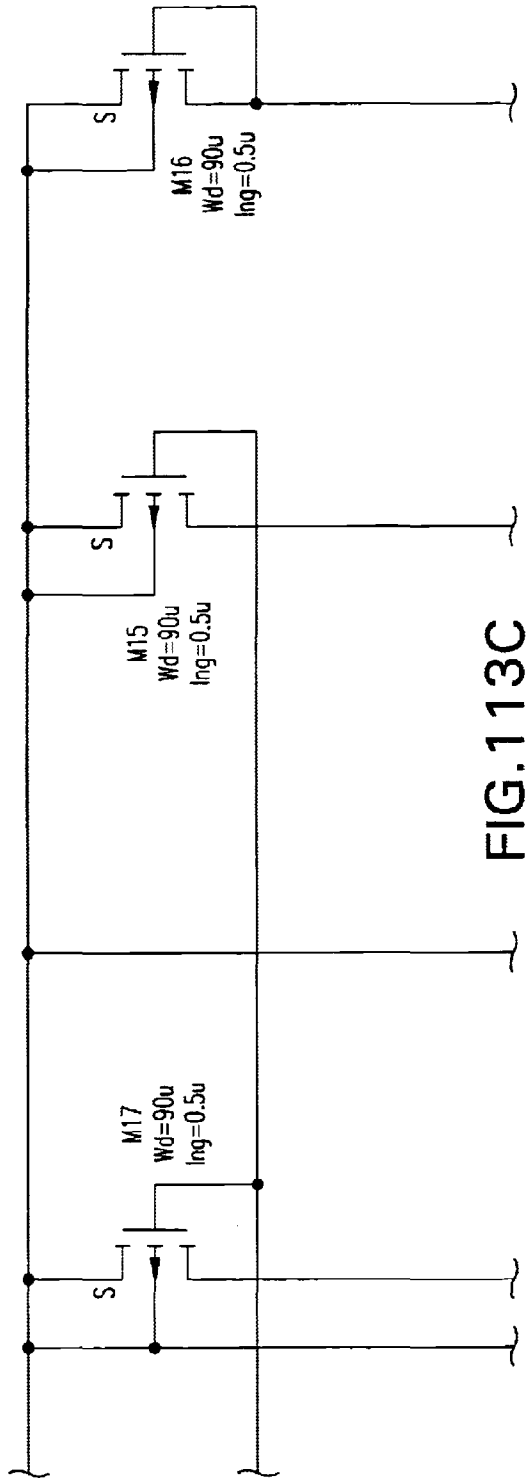


FIG.113C

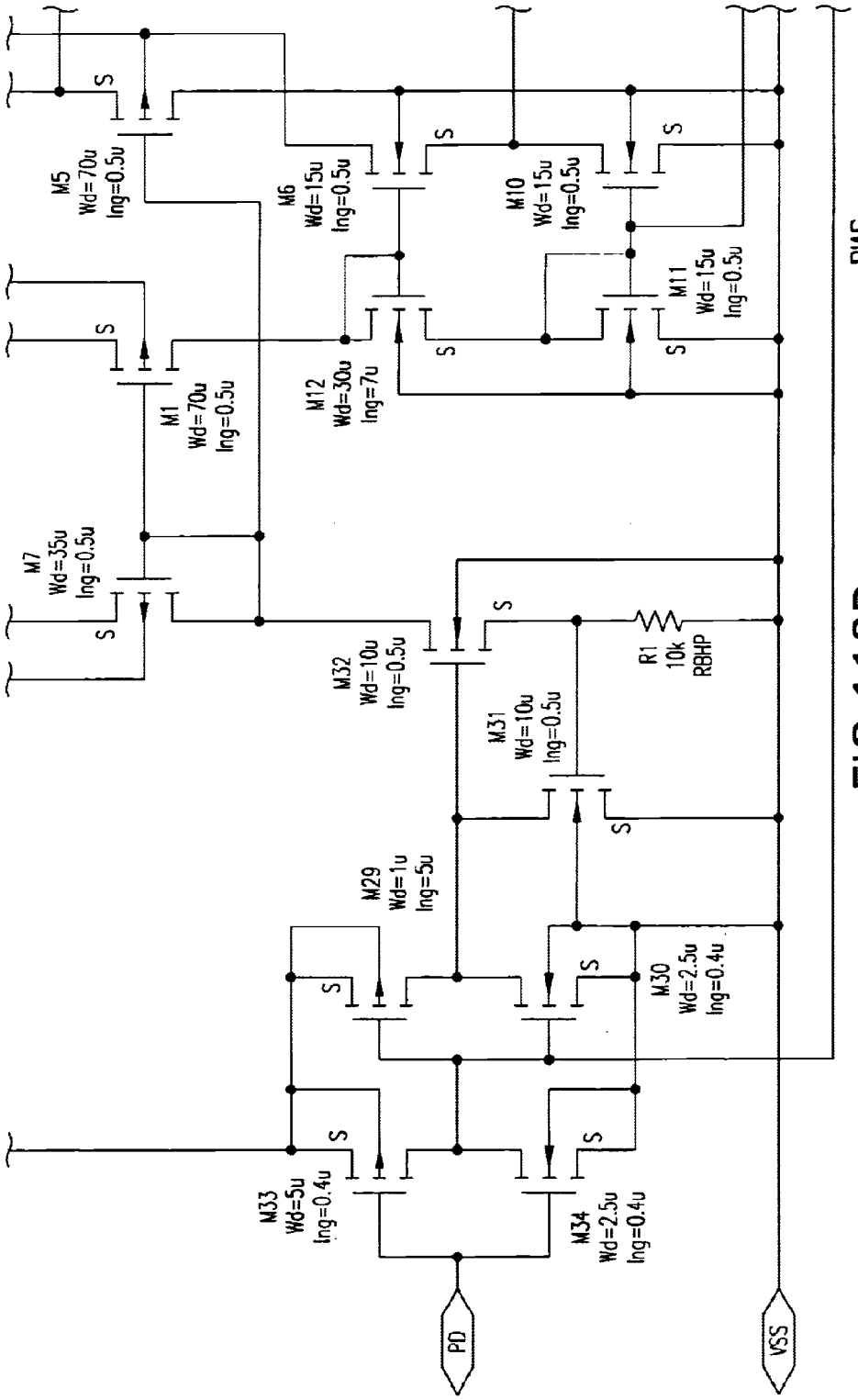

M5
Wd=70u
lng=0.5u
M6
Wd=15u
lng=0.5u
M10
Wd=15u
lng=0.5u
M11
Wd=15u
lng=0.5u
BIAS
M12
Wd=30u
lng=7u
M1
Wd=70u
lng=0.5u
M7
Wd=35u
lng=0.5u
M32
Wd=10u
lng=0.5u
R1
10k
RBHP
M31
Wd=10u
lng=0.5u
M29
Wd=1u
lng=5u
M30
Wd=2.5u
lng=0.4u
M33
Wd=5u
lng=0.4u
M34
Wd=2.5u
lng=0.4u
PD
VSS

FIG.113D

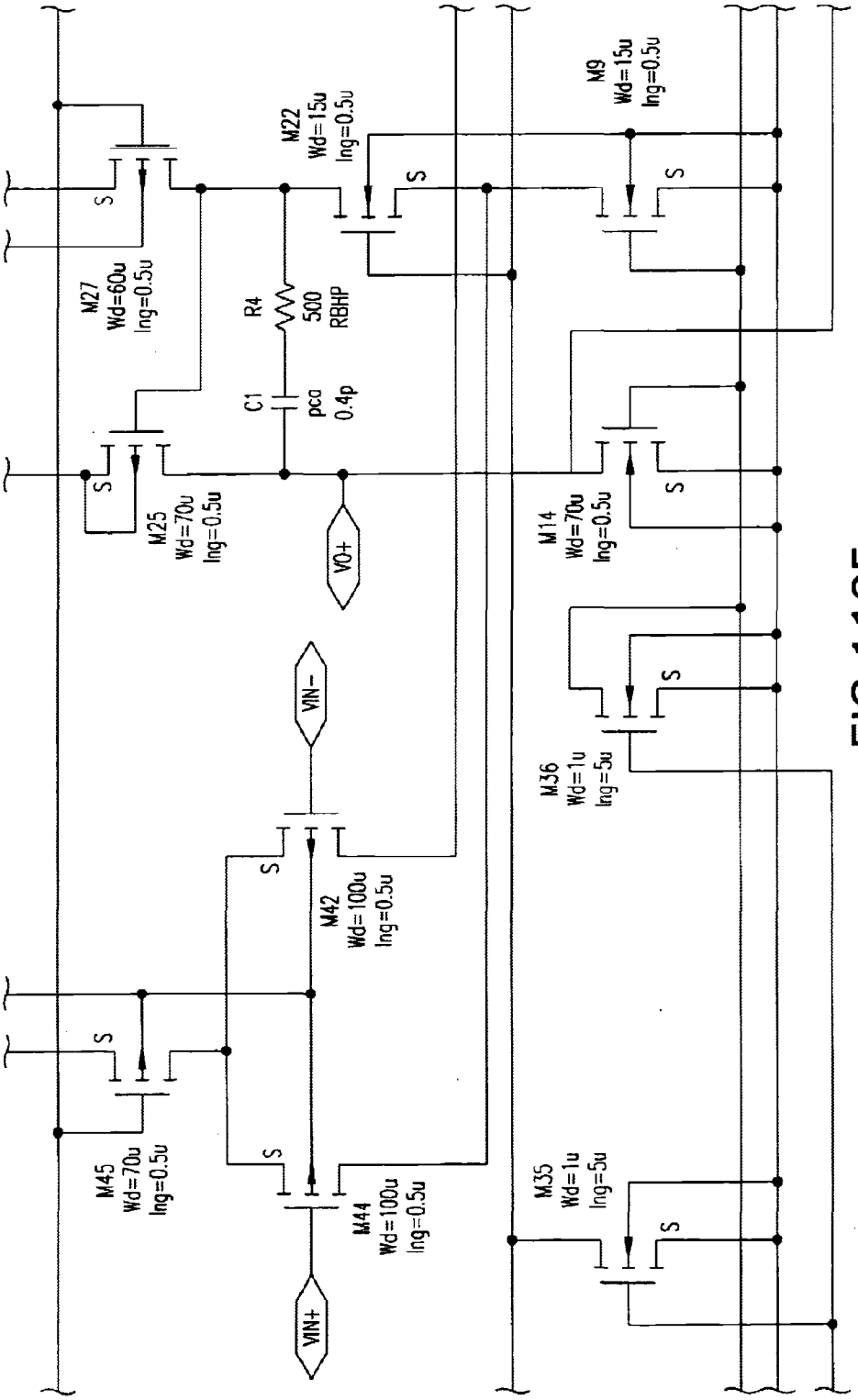

M22
Wd=15u
lng=0.5u
M9
Wd=15u
lng=0.5u
M27
Wd=60u
lng=0.5u
R4
500
RBHP
C1
pca
0.4p
M25
Wd=70u
lng=0.5u
VO+
M14
Wd=70u
lng=0.5u
VIN-
M36
Wd=1u
lng=5u
M42
Wd=100u
lng=0.5u
M45
Wd=70u
lng=0.5u
M44
Wd=100u
lng=0.5u
M35
Wd=1u
lng=5u
VIN+
S

FIG.113E

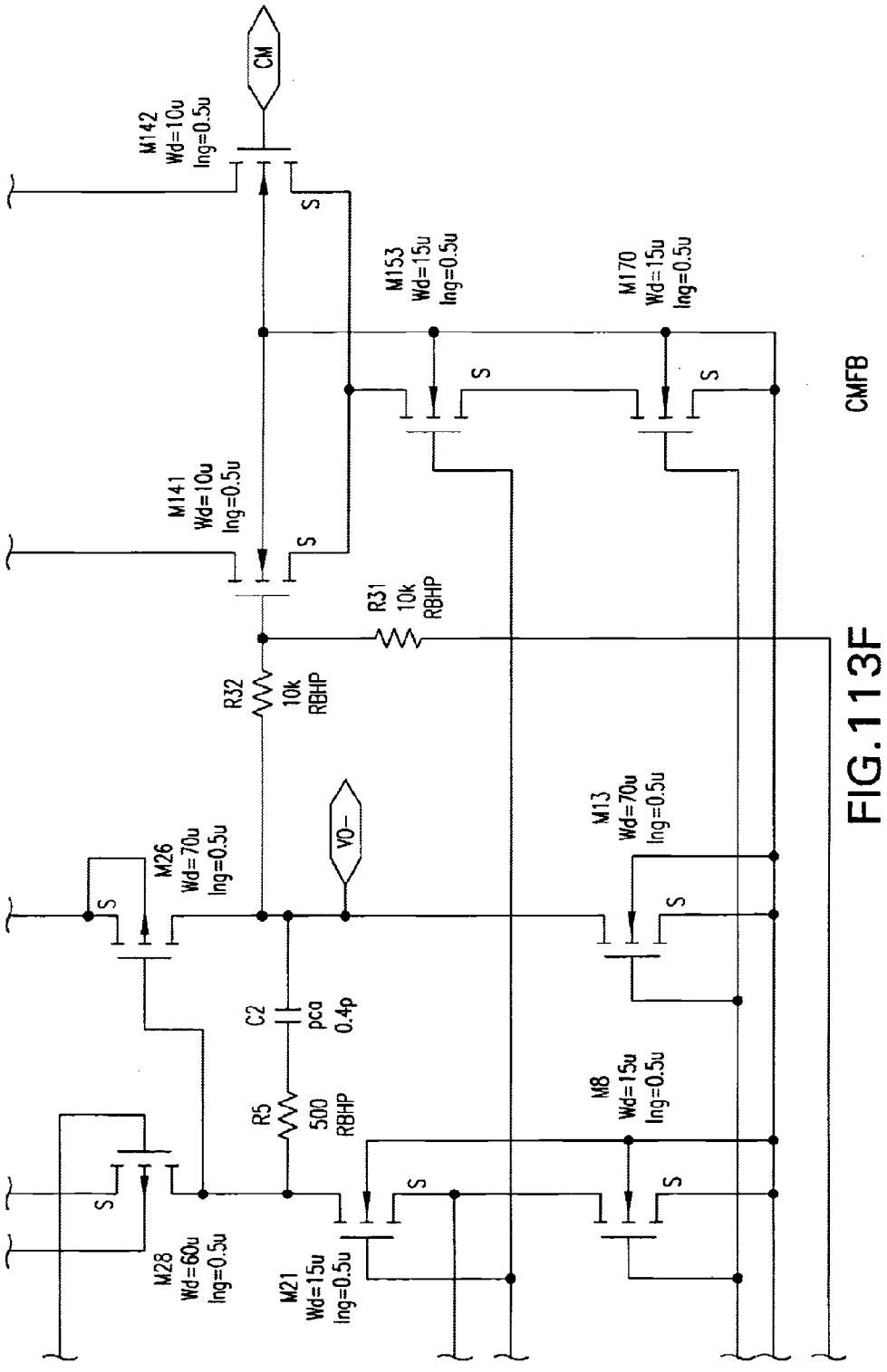

CM
M142
Wd=10u
lng=0.5u
M153
Wd=15u
lng=0.5u
M170
Wd=15u
lng=0.5u
CMFB
M141
Wd=10u
lng=0.5u
R31
10k
RBHP
R32
10k
RBHP
VO-
M26
Wd=70u
lng=0.5u
M13
Wd=70u
lng=0.5u
C2
pca
0.4p
R5
500
RBHP
M8
Wd=15u
lng=0.5u
M28
Wd=60u
lng=0.5u
M21
Wd=15u
lng=0.5u
S

FIG.113F

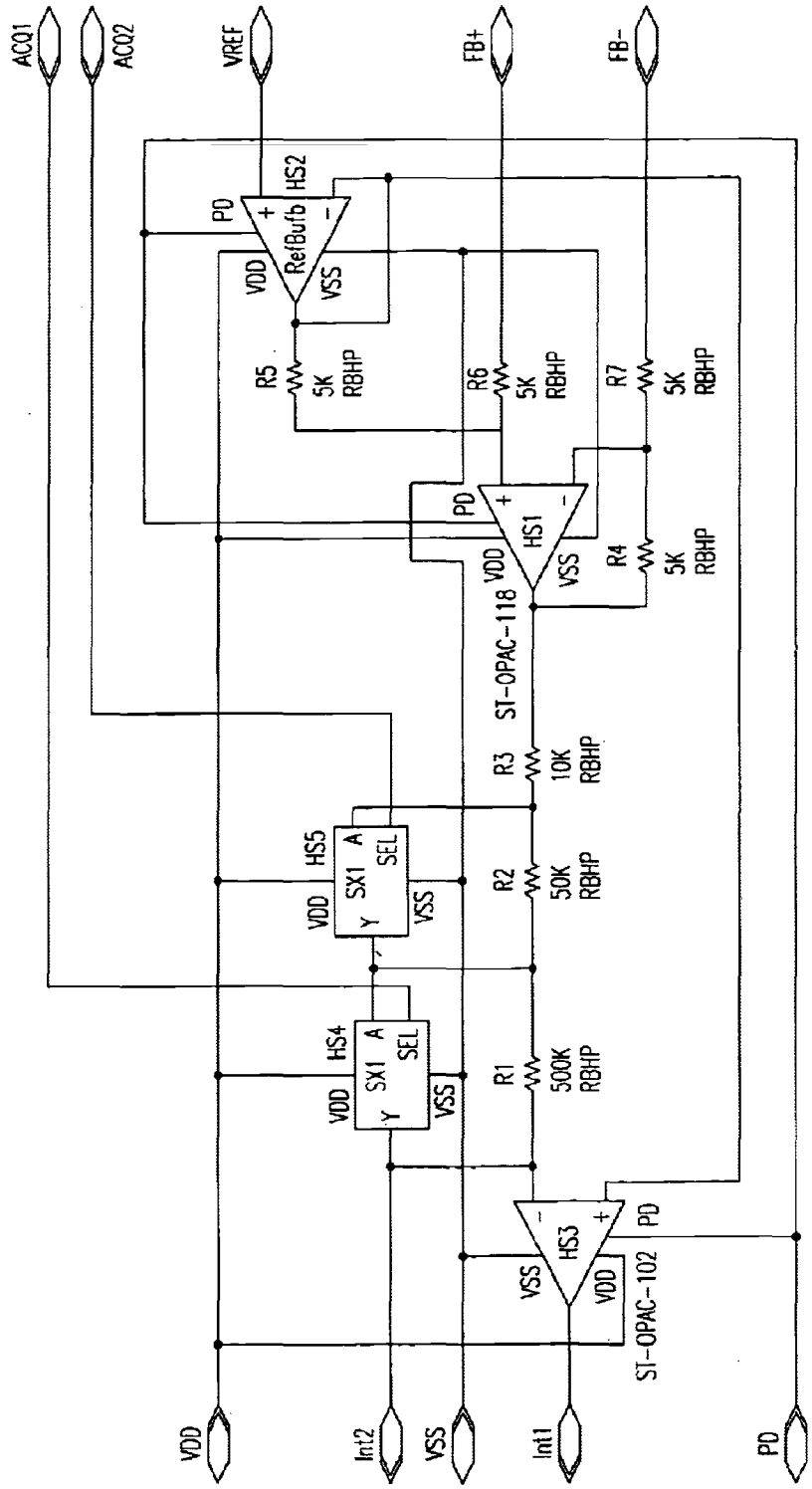

ACQ1
ACQ2
VREF
FB+
FB-
PD
HS2
RefBufb
VDD
VSS
R5
5K
RBHP
R6
5K
RBHP
R7
5K
RBHP
HS1
R4
5K
RBHP
ST-OPAC-118
R3
10K
RBHP
HS5
SX1
A
SEL
Y
R2
50K
RBHP
HS4
R1
500K
RBHP
HS3
ST-OPAC-102
Int2
Int1

FIG.114

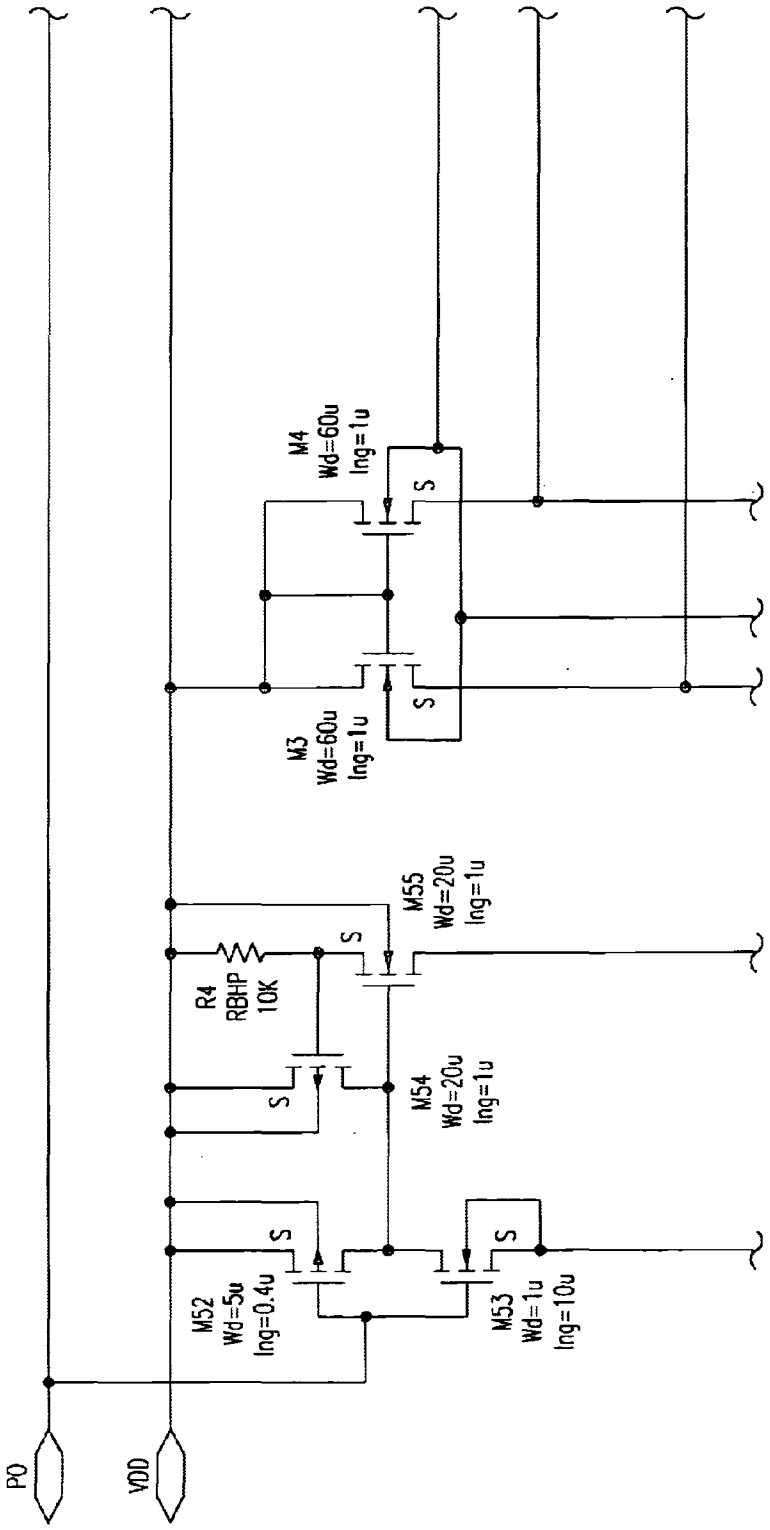

M4
Wd=60u
lng=1u
S
M3
Wd=60u
lng=1u
M55
Wd=20u
lng=1u
R4
RBHP
10K
M54
Wd=20u
lng=1u
M52
Wd=5u
lng=0.4u
M53
Wd=1u
lng=10u
PD
VDD

FIG. 115A

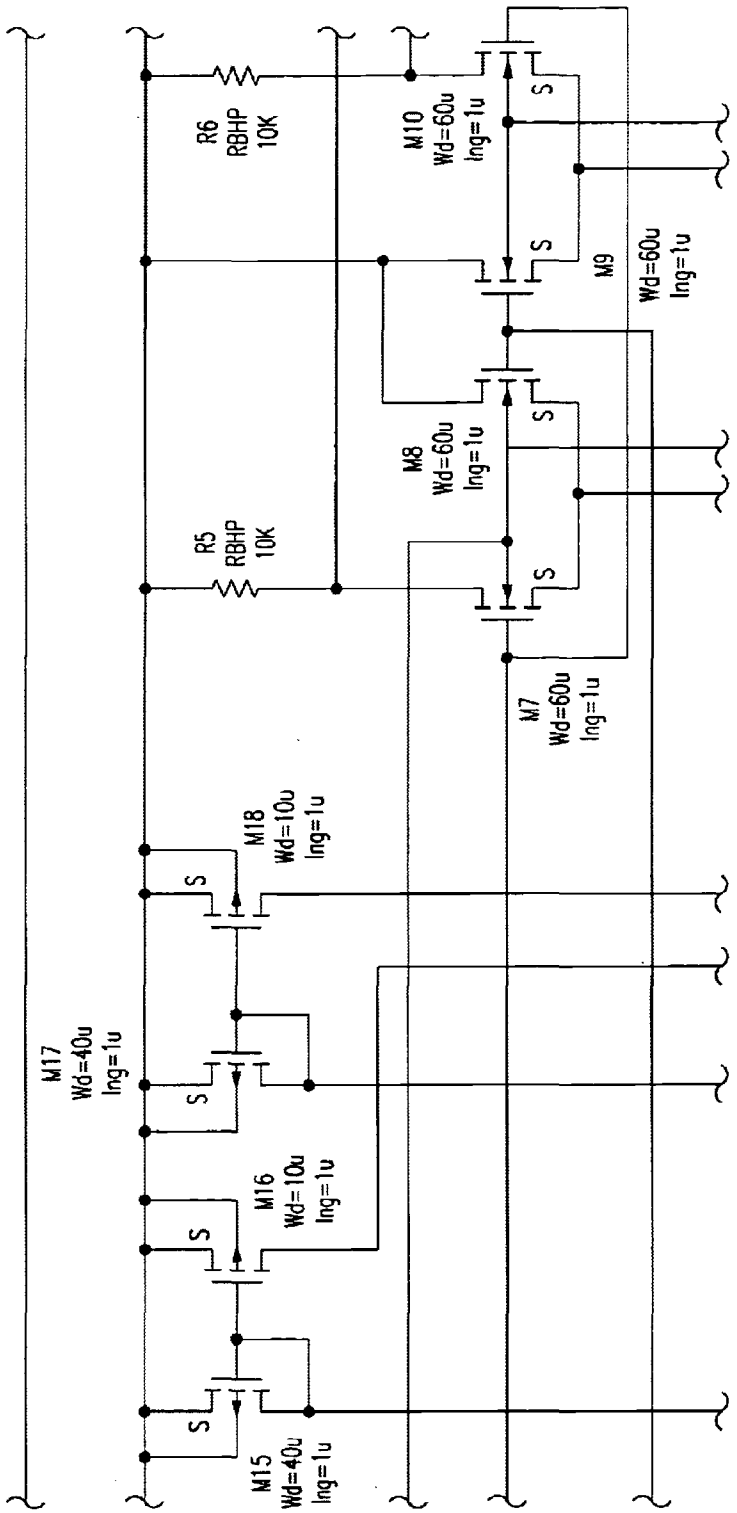

R6
RBHP
10K
M10
Wd=60u
lng=1u
S
M9
Wd=60u
lng=1u
M8
Wd=60u
lng=1u
R5
RBHP
10K
M7
Wd=60u
lng=1u
M18
Wd=10u
lng=1u
M17
Wd=40u
lng=1u
M16
Wd=10u
lng=1u
M15
Wd=40u
lng=1u

FIG.115B

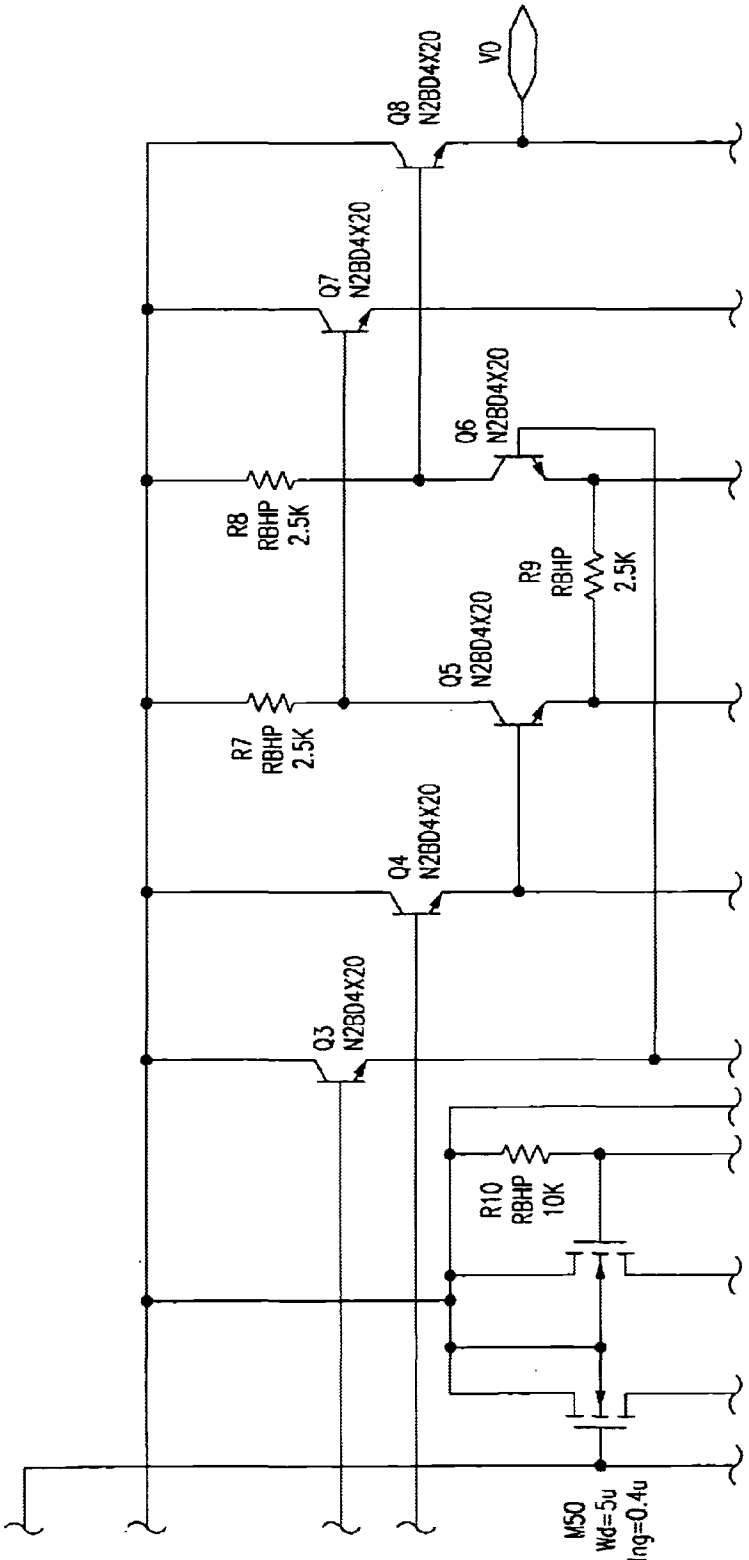

VO
Q8 N2BD4X20
Q7 N2BD4X20
Q6 N2BD4X20
R8 RBHP 2.5K
R9 RBHP 2.5K
Q5 N2BD4X20
R7 RBHP 2.5K
Q4 N2BD4X20
Q3 N2BD4X20
R10 RBHP 10K
M50 Wd=5u lng=0.4u

FIG.115C

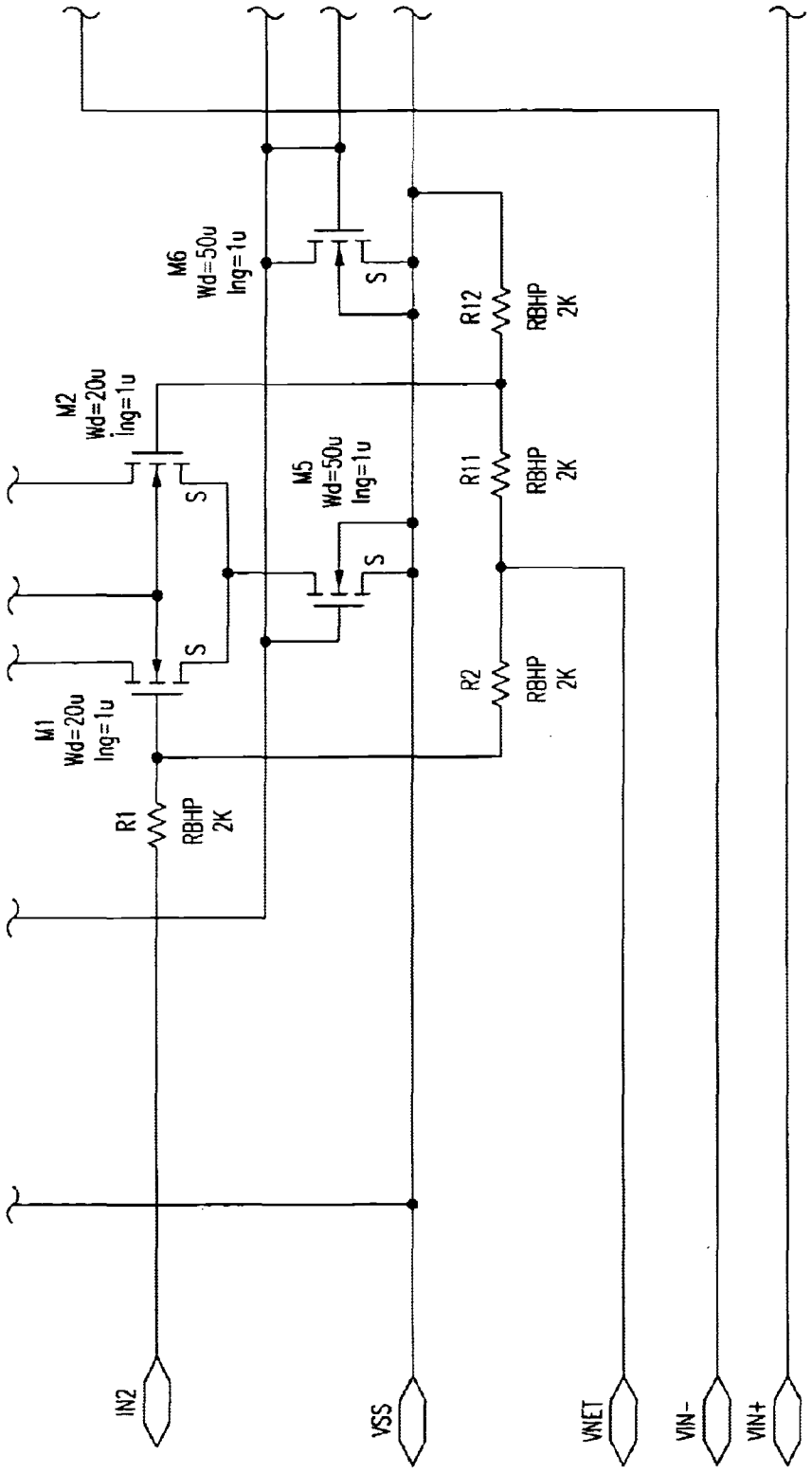

M6
Wd=50u
lng=1u
S
R12
RBHP
2K
M2
Wd=20u
lng=1u
M5
Wd=50u
lng=1u
R11
RBHP
2K
S
S
S
R2
RBHP
2K
M1
Wd=20u
lng=1u
R1
RBHP
2K
IN2
VSS
VNET
VIN-
VIN+

FIG.115D

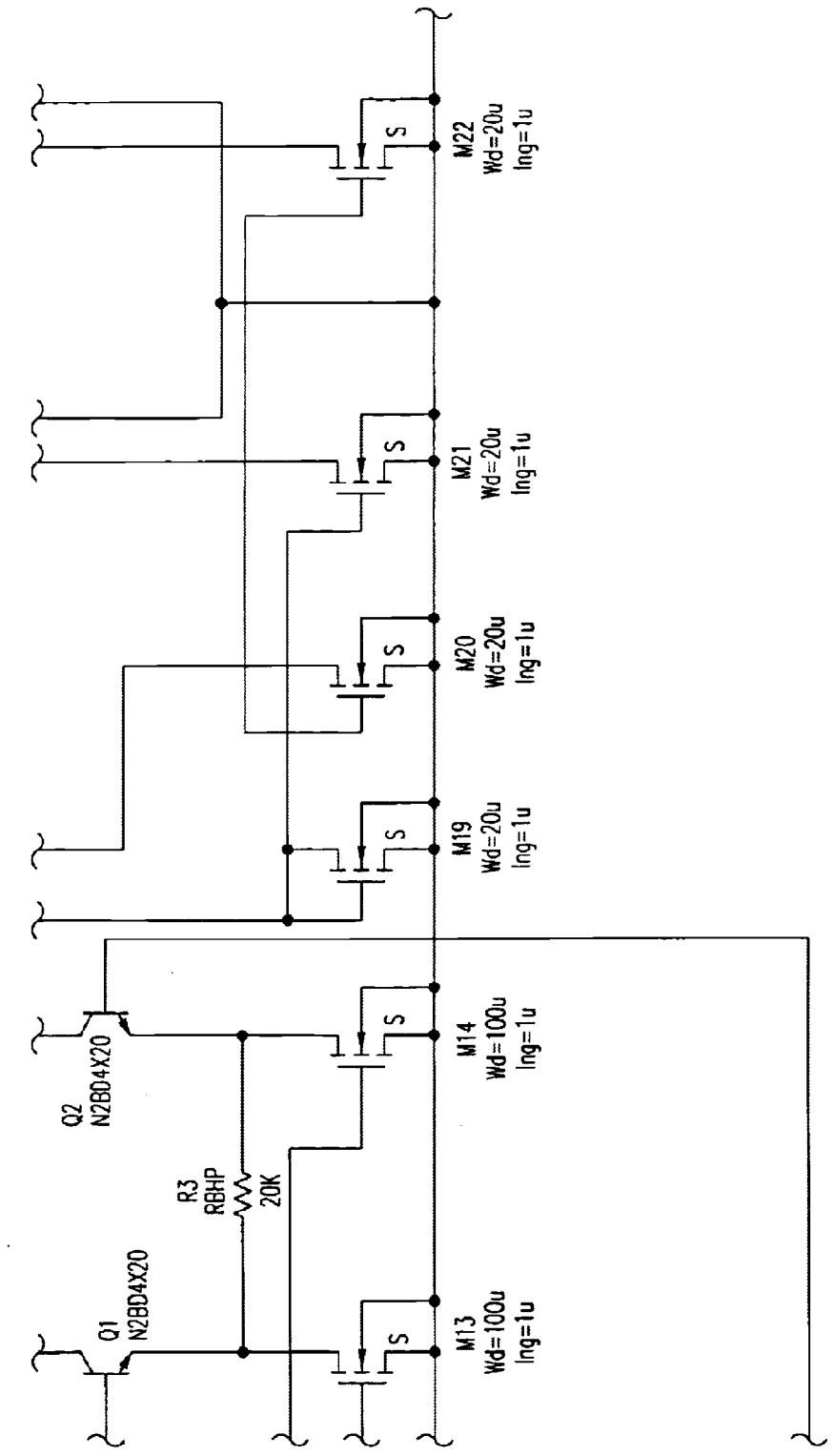

M22
Wd=20u
lng=1u
M21
Wd=20u
lng=1u
M20
Wd=20u
lng=1u
M19
Wd=20u
lng=1u
M14
Wd=100u
lng=1u
M13
Wd=100u
lng=1u
Q2
N2BD4X20
Q1
N2BD4X20
R3
RBHP
20K

FIG.115E

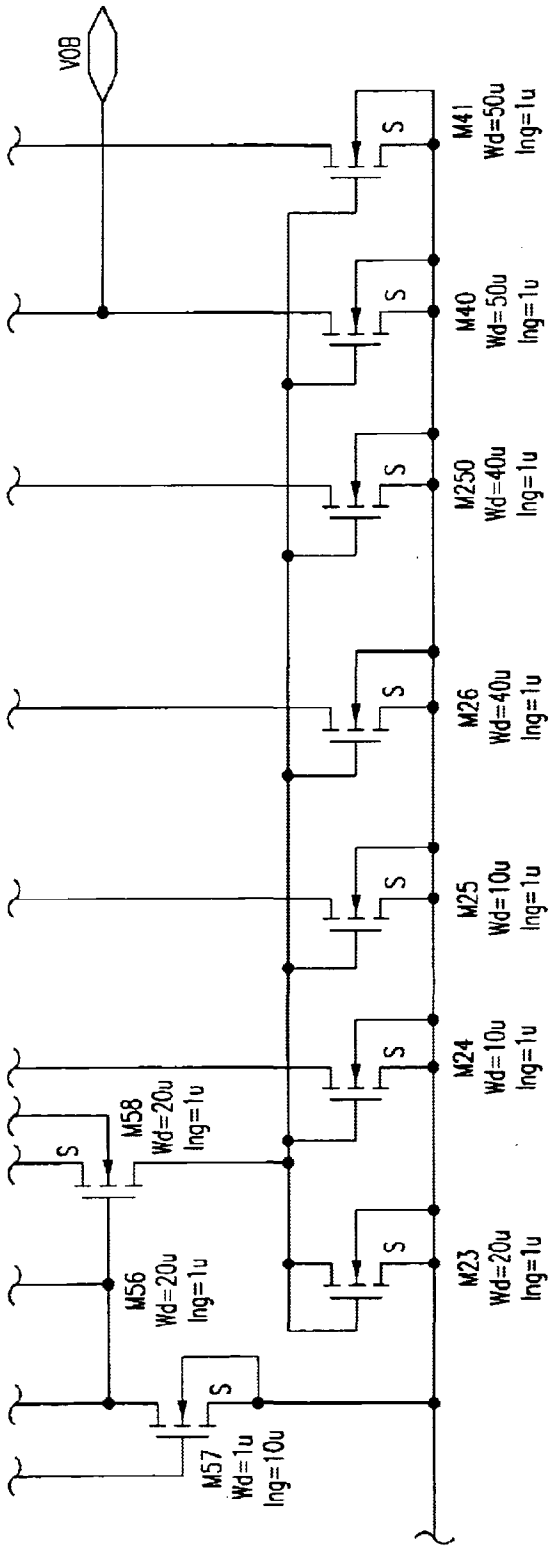

VOB
M41 Wd=50u lng=1u
M40 Wd=50u lng=1u
M250 Wd=40u lng=1u
M26 Wd=40u lng=1u
M25 Wd=10u lng=1u
M24 Wd=10u lng=1u
M23 Wd=20u lng=1u
M58 Wd=20u lng=1u
M56 Wd=20u lng=1u
M57 Wd=1u lng=10u
S

FIG.115F

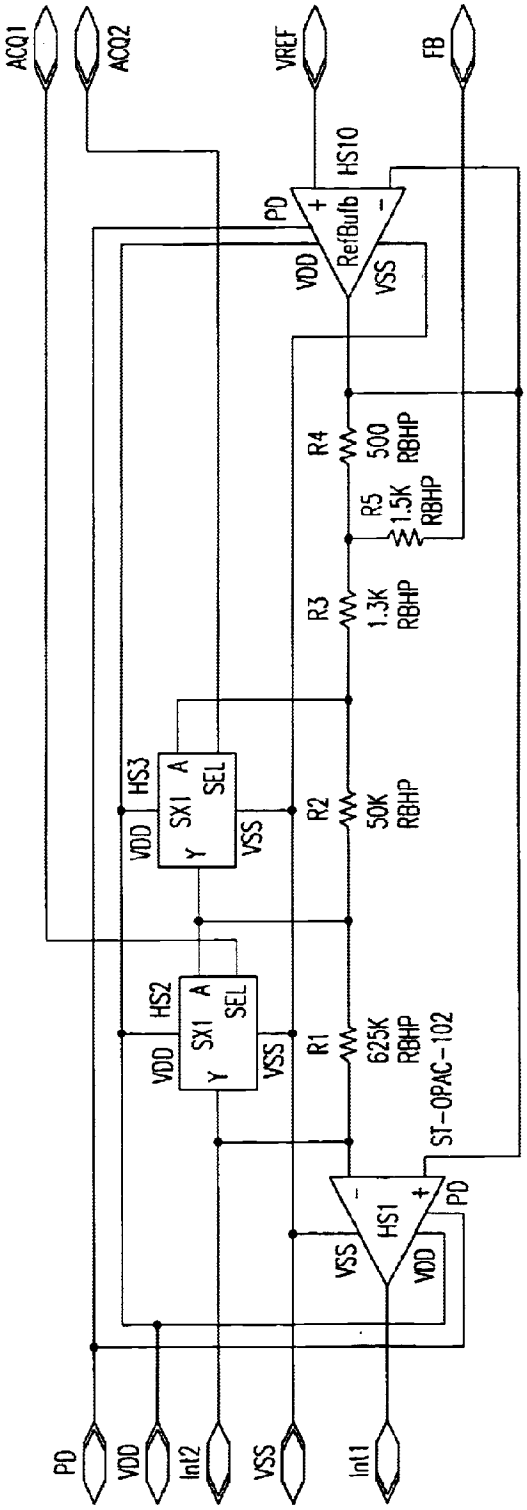

ACQ1
ACQ2
VREF
FB
HS10
PD
RefBufb
VDD
VSS
R4
500
RBHP
R5
1.5K
RBHP
R3
1.3K
RBHP
HS3
SX1
A
SEL
Y
R2
50K
RBHP
HS2
R1
625K
RBHP
ST-OPAC-102
HS1
Int2
Int1

FIG.116

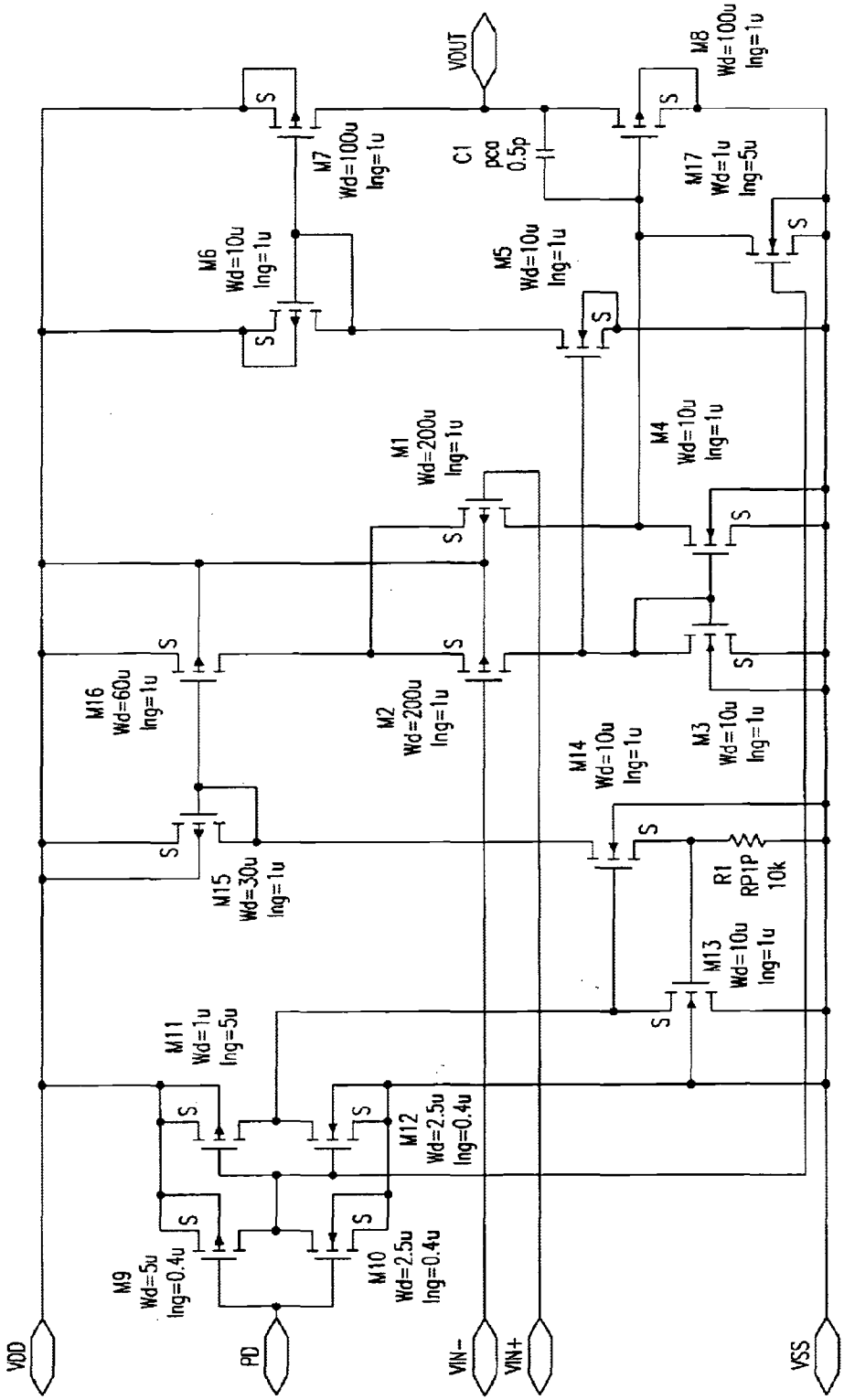

VOUT
M8 Wd=100u lng=1u
M7 Wd=100u lng=1u
C1 pca 0.5p
M17 Wd=1u lng=5u
M6 Wd=10u lng=1u
M5 Wd=10u lng=1u
M1 Wd=200u lng=1u
M4 Wd=10u lng=1u
M16 Wd=60u lng=1u
M2 Wd=200u lng=1u
M3 Wd=10u lng=1u
M14 Wd=10u lng=1u
M15 Wd=30u lng=1u
R1 RP1P 10k
M13 Wd=10u lng=1u
M11 Wd=1u lng=5u
M12 Wd=2.5u lng=0.4u
M9 Wd=5u lng=0.4u
M10 Wd=2.5u lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG. 117

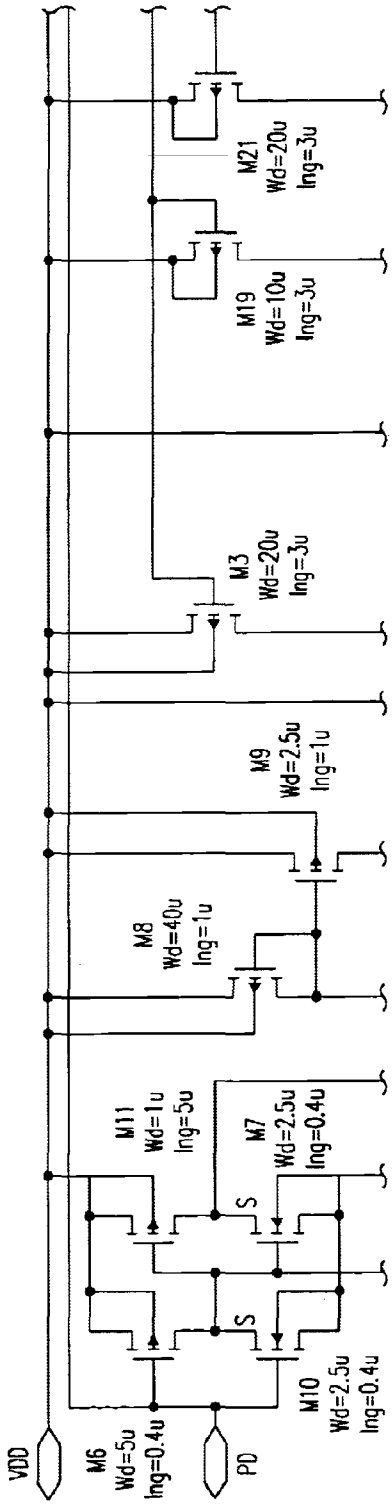

M21
Wd=20u
lng=3u
M19
Wd=10u
lng=3u
M3
Wd=20u
lng=3u
M9
Wd=2.5u
lng=1u
M8
Wd=40u
lng=1u
M11
Wd=1u
lng=5u
M7
Wd=2.5u
lng=0.4u
S
S
M10
Wd=2.5u
lng=0.4u
VDD
M6
Wd=5u
lng=0.4u
PD

FIG.118A

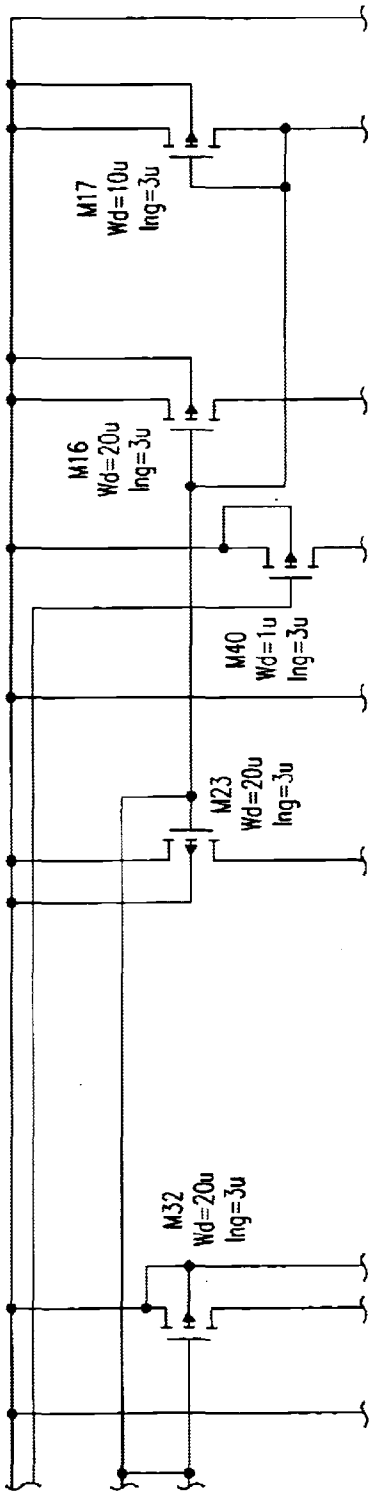

M17
Wd=10u
lng=3u
M16
Wd=20u
lng=3u
M40
Wd=1u
lng=3u
M23
Wd=20u
lng=3u
M32
Wd=20u
lng=3u

FIG.118B

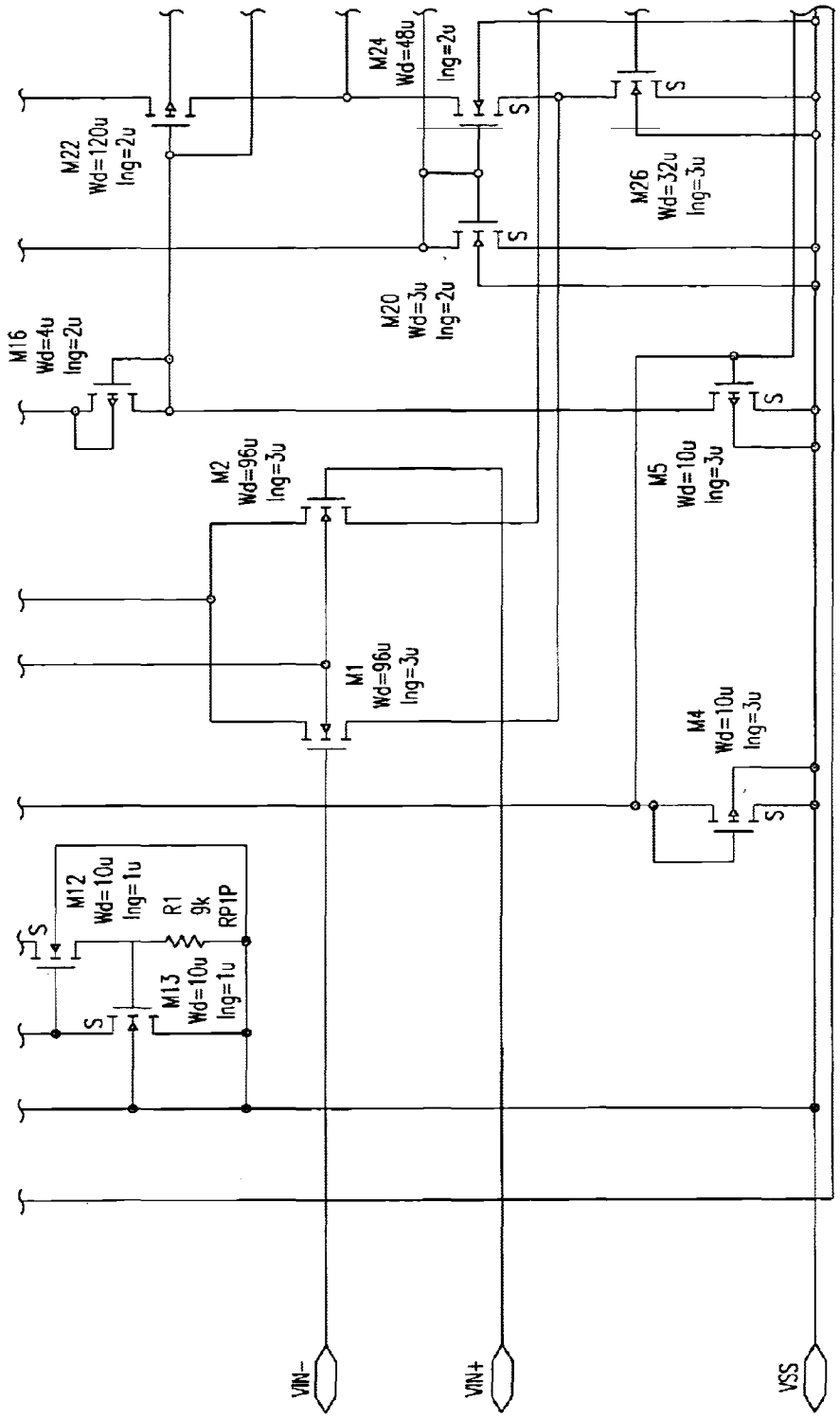

M22
Wd=120u
lng=2u
M24
Wd=48u
lng=2u
M26
Wd=32u
lng=3u
M20
Wd=3u
lng=2u
M16
Wd=4u
lng=2u
M2
Wd=96u
lng=3u
M5
Wd=10u
lng=3u
M1
Wd=96u
lng=3u
M4
Wd=10u
lng=3u
M12
Wd=10u
lng=1u
R1
9k
RP1P
M13
Wd=10u
lng=1u
S
VIN-
VIN+
VSS

FIG. 118C

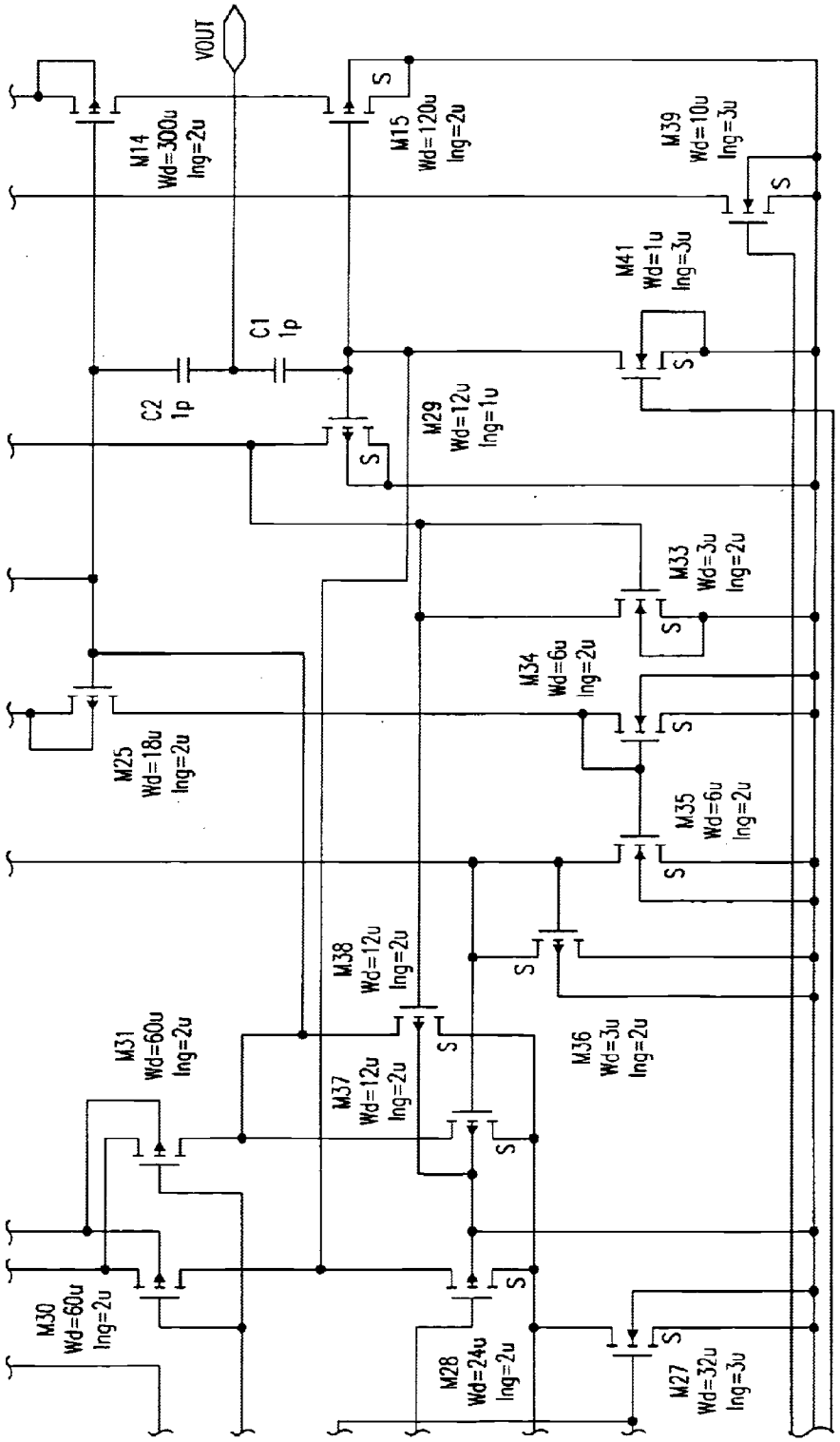

VOUT
M14 Wd=300u lng=2u
M15 Wd=120u lng=2u
M39 Wd=10u lng=3u
M41 Wd=1u lng=3u
C1 1p
C2 1p
M29 Wd=12u lng=1u
M33 Wd=3u lng=2u
M34 Wd=6u lng=2u
M25 Wd=18u lng=2u
M35 Wd=6u lng=2u
M38 Wd=12u lng=2u
M31 Wd=60u lng=2u
M36 Wd=3u lng=2u
M37 Wd=12u lng=2u
M30 Wd=60u lng=2u
M28 Wd=24u lng=2u
M27 Wd=32u lng=3u
S

FIG.118D

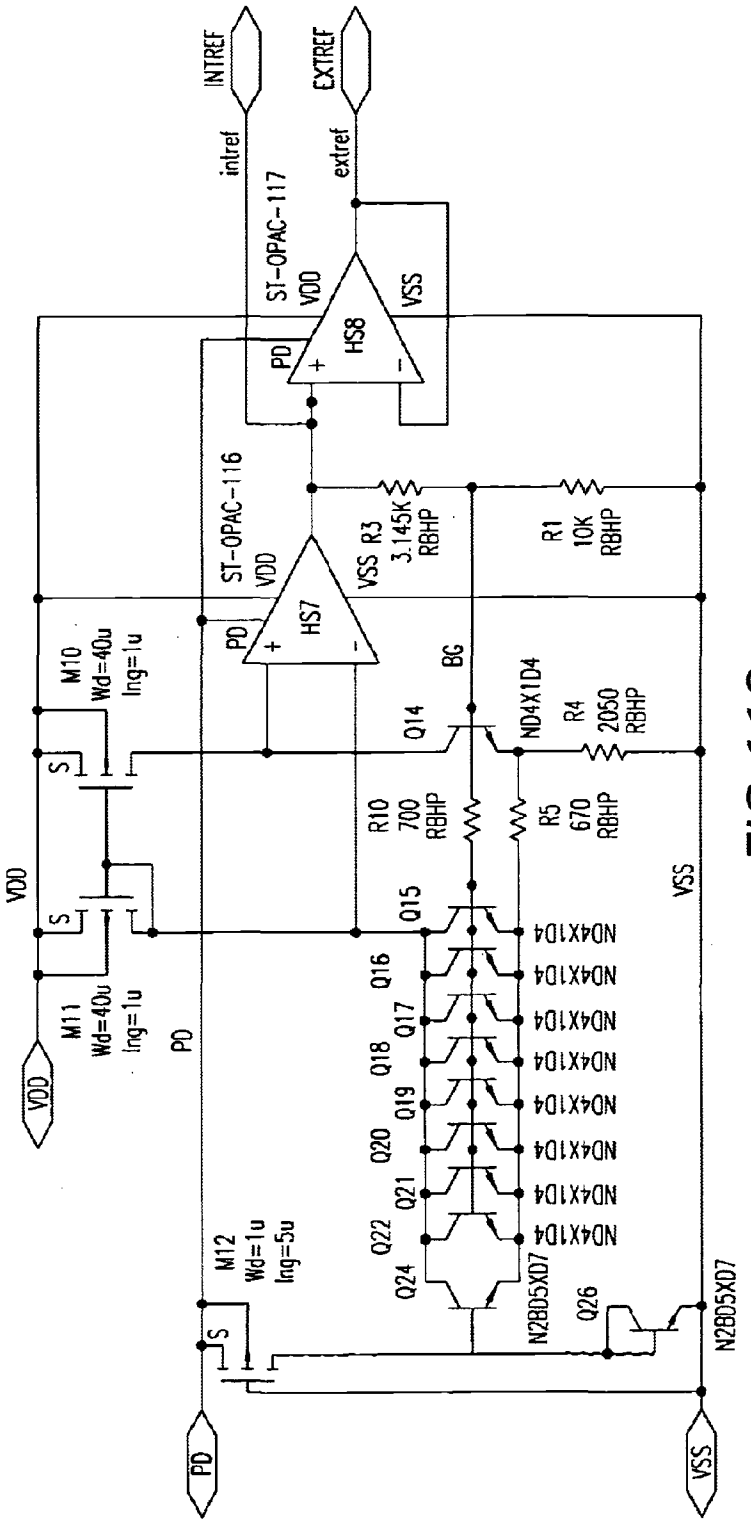

INTREF
EXTREF
intref
extref
ST-OPAC-117
VDD
VSS
HS8
PD
ST-OPAC-116
HS7
R3
3.145K
RBHP
R1
10K
RBHP
M10
Wd=40u
lng=1u
BG
Q14
ND4X1D4
R4
2050
RBHP
R10
700
RBHP
R5
670
RBHP
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q24
M11
M12
Wd=1u
lng=5u
Wd=40u
N2B05XD7
Q26

FIG.119

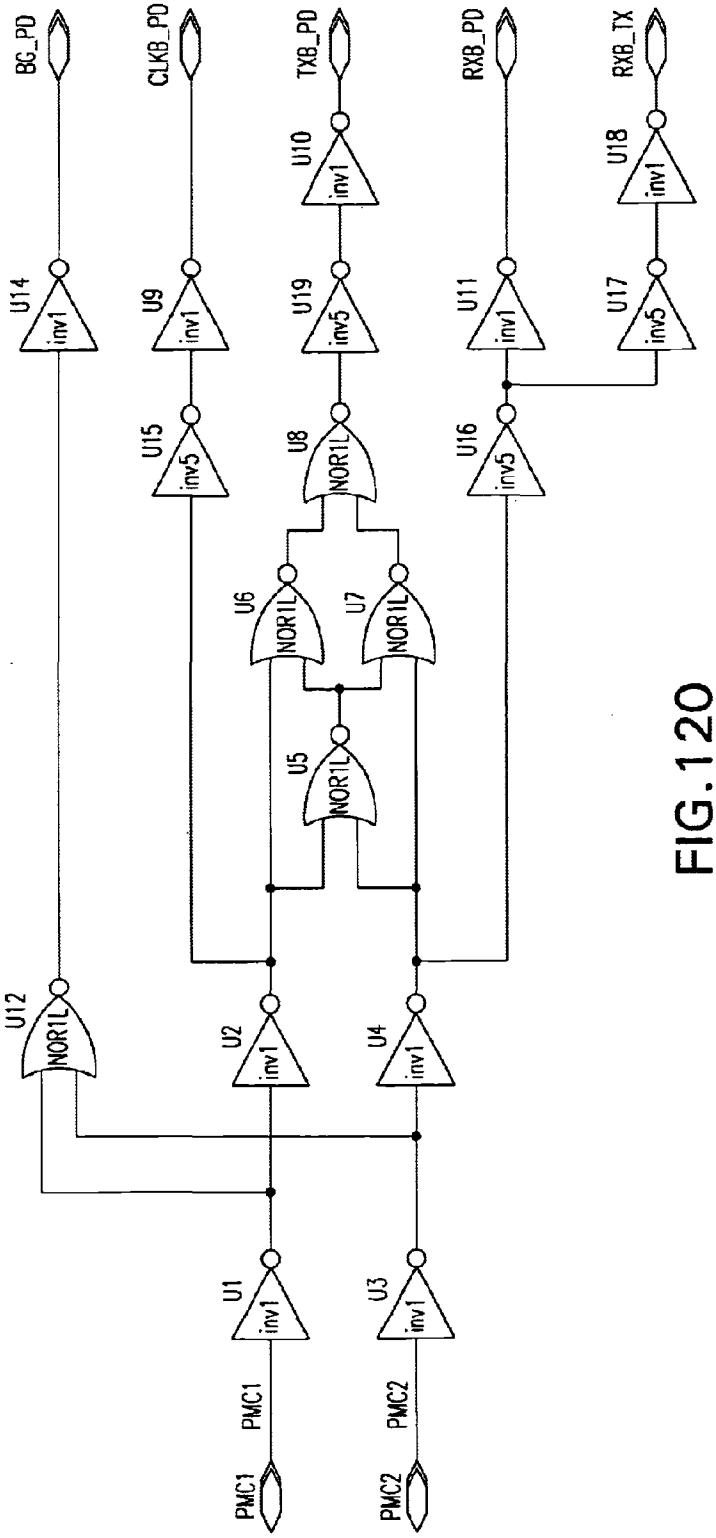

BG_PD
CLKB_PD
TXB_PD
RXB_PD
RXB_TX
U14 inv1
U9 inv1
U10 inv1
U19 inv5
U11 inv1
U18 inv1
U17 inv5
U15 inv5
U8 NOR1L
U16 inv5
U6 NOR1L
U7 NOR1L
U5 NOR1L
U12 NOR1L
U2 inv1
U4 inv1
U1 inv1
U3 inv1
PMC1
PMC2
PMC1
PMC2

FIG. 120

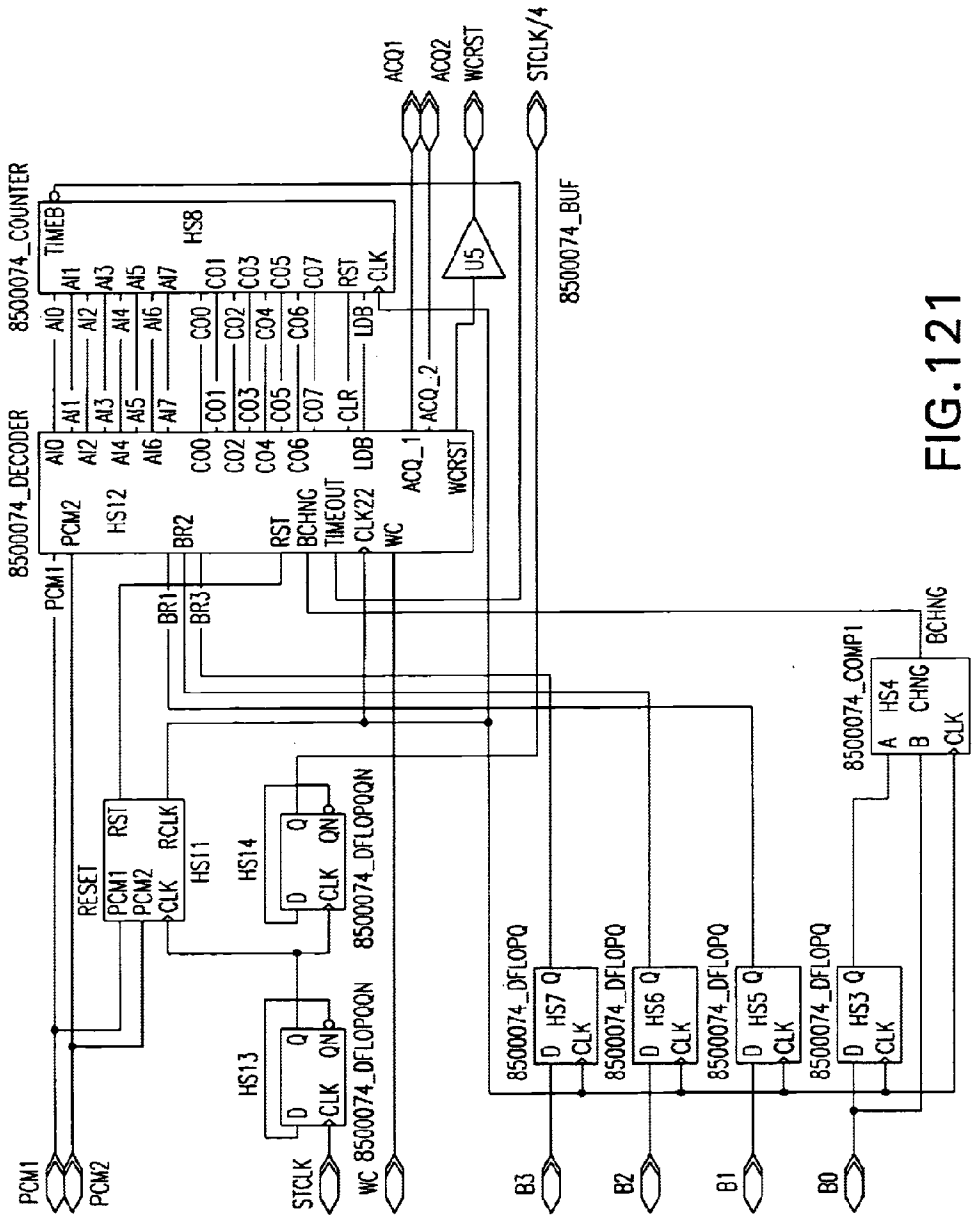

ACQ1
ACQ2
WCRST
STCLK/4
8500074_COUNTER
TIMEB
HS8
U5
8500074_BUF
8500074_DECODER
HS12
PCM1
PCM2
BR1
BR2
BR3
RST
BCHNG
TIMEOUT
CLK22
WC
ACQ_1
ACQ_2
WCRST
CLR
LDB
RESET
HS11
HS13
HS14
8500074_DFLOPQN
8500074_DFLOPQ
HS7
HS6
HS5
HS3
8500074_COMP1
HS4
CHNG
B3
B2
B1
B0
STCLK
WC

FIG.121

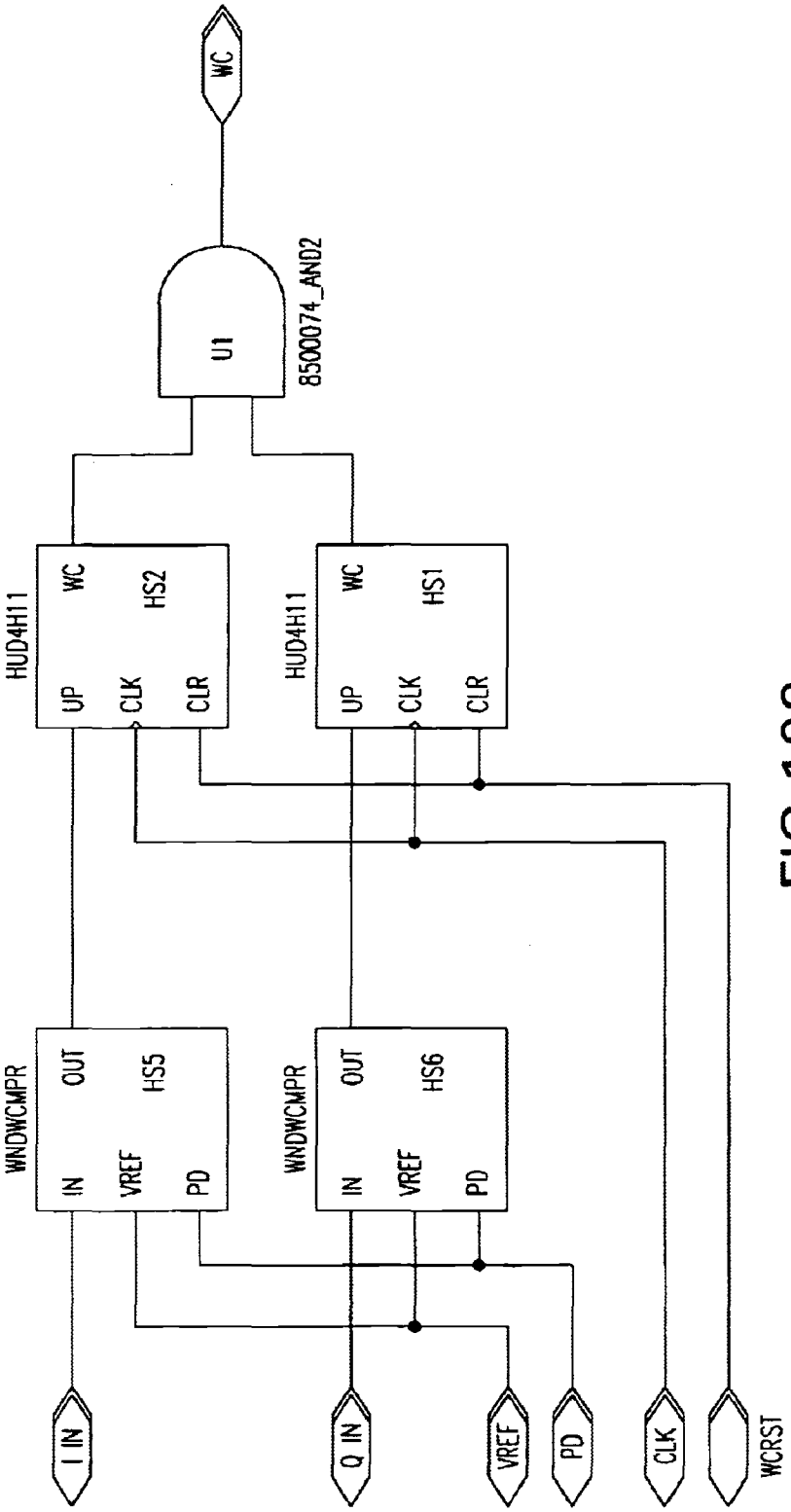

WC
U1
8500074_AND2
HUD4H11
WC
HS2
UP
CLK
CLR
HUD4H11
WC
HS1
UP
CLK
CLR
WNDWCMPR
OUT
HS5
IN
VREF
PD
WNDWCMPR
OUT
HS6
IN
VREF
PD
I IN
Q IN
VREF
PD
CLK
WCRST

FIG. 122

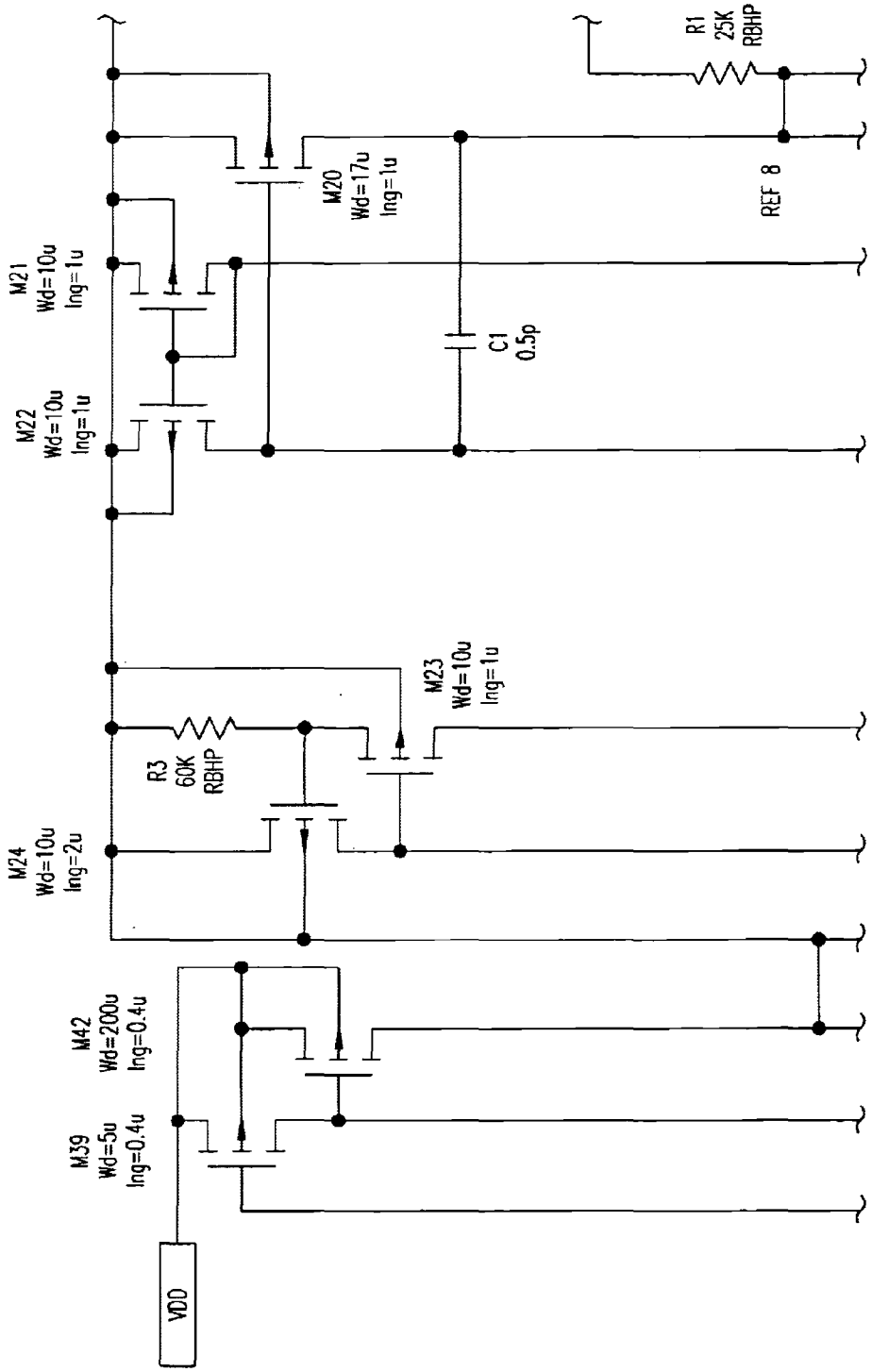

R1
25K
RBHP
M20
Wd=17u
lng=1u
REF 8
M21
Wd=10u
lng=1u
C1
0.5p
M22
Wd=10u
lng=1u
M23
Wd=10u
lng=1u
R3
60K
RBHP
M24
Wd=10u
lng=2u
M42
Wd=200u
lng=0.4u
M39
Wd=5u
lng=0.4u
VDD

FIG.123A

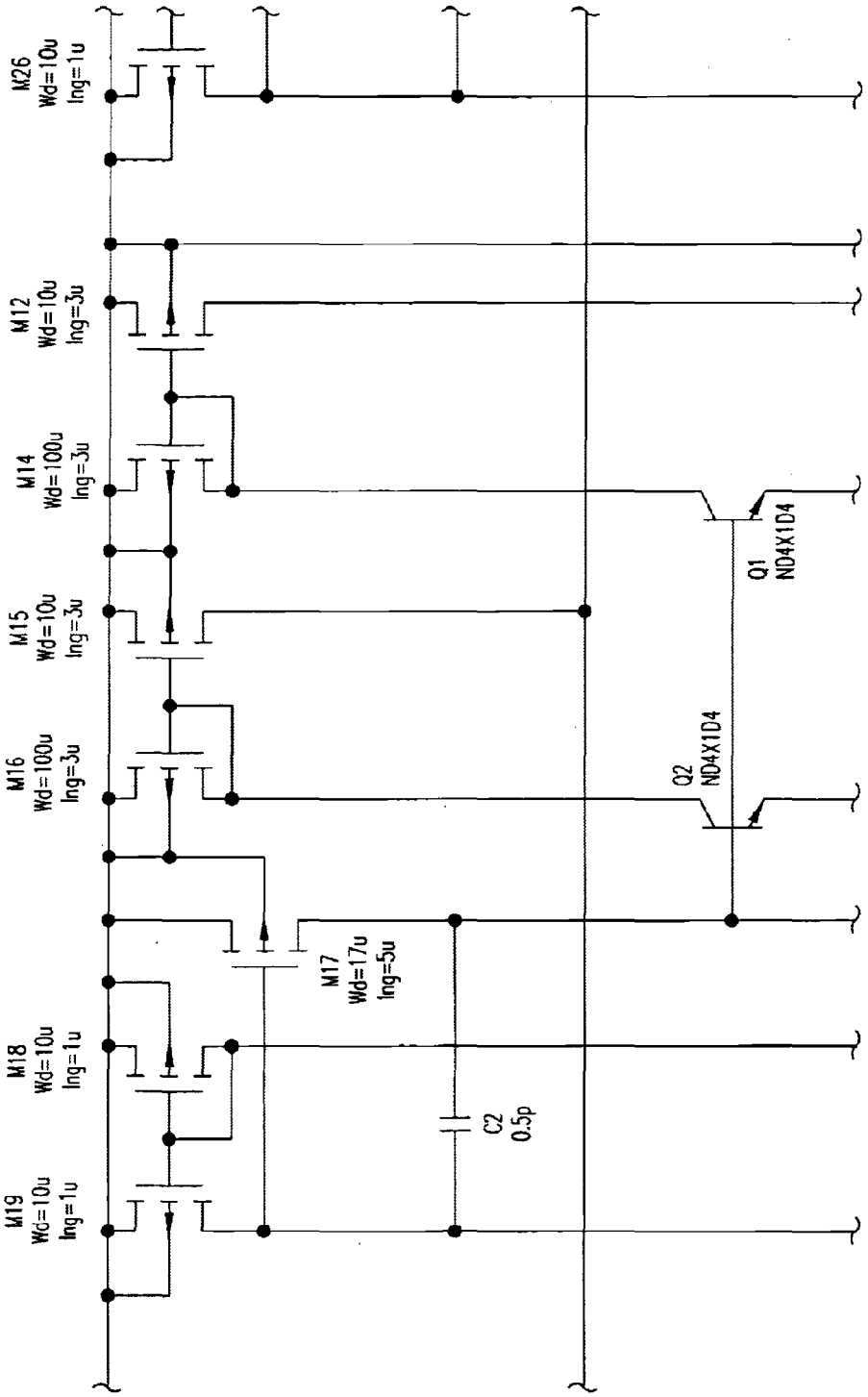

M26
Wd=10u
lng=1u
M12
Wd=10u
lng=3u
M14
Wd=100u
lng=3u
M15
Wd=10u
lng=3u
M16
Wd=100u
lng=3u
M17
Wd=17u
lng=5u
M18
Wd=10u
lng=1u
M19
Wd=10u
lng=1u
C2
0.5p
Q1
ND4X1D4
Q2
ND4X1D4

FIG.123B

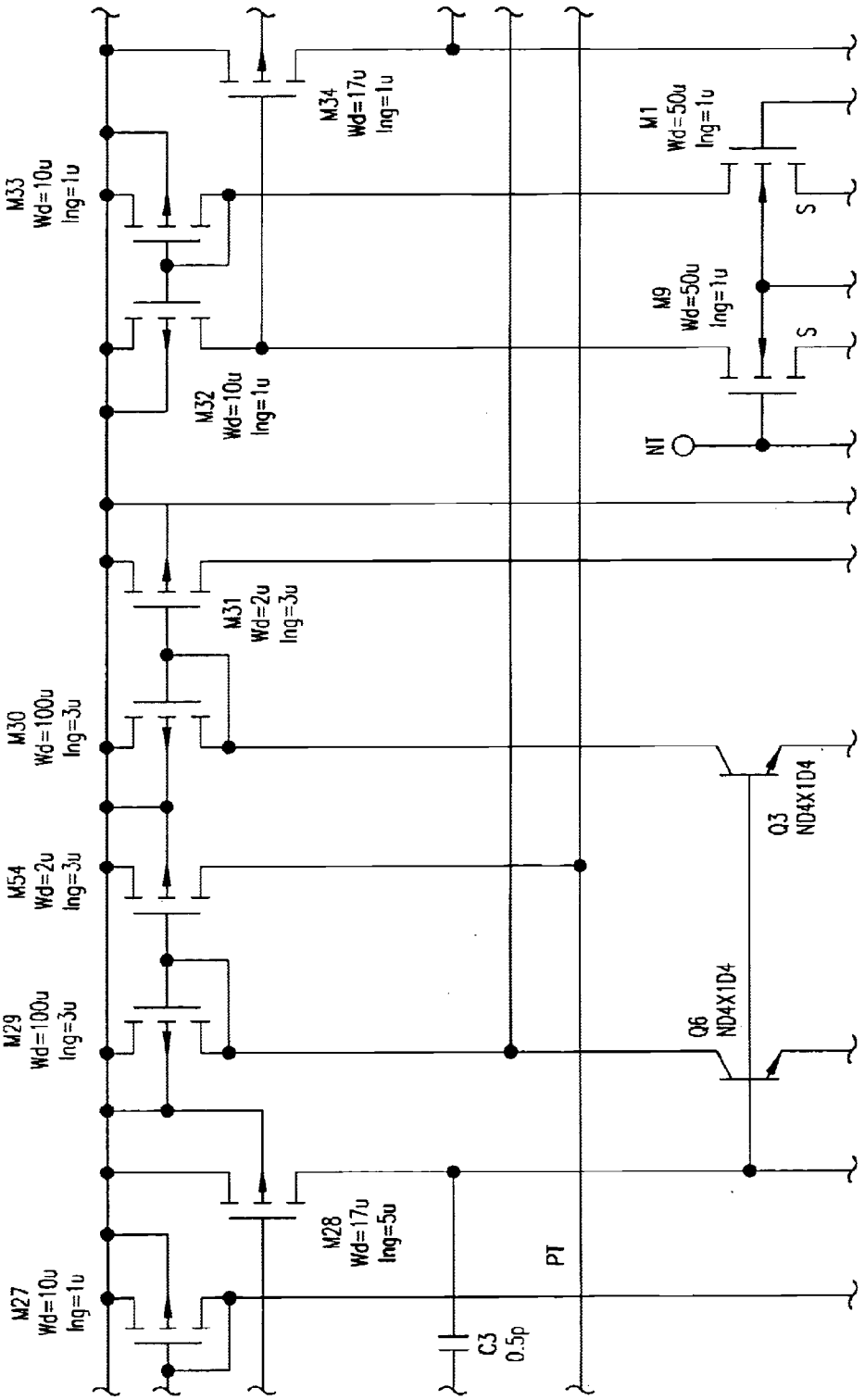

M33
Wd=10u
lng=1u
M34
Wd=17u
lng=1u
M1
Wd=50u
lng=1u
S
M9
Wd=50u
lng=1u
S
M32
Wd=10u
lng=1u
NT
M31
Wd=2u
lng=3u
M30
Wd=100u
lng=3u
Q3
ND4X1D4
M54
Wd=2u
lng=3u
M29
Wd=100u
lng=3u
Q6
ND4X1D4
M28
Wd=17u
lng=5u
M27
Wd=10u
lng=1u
PT
C3
0.5p

FIG.123C

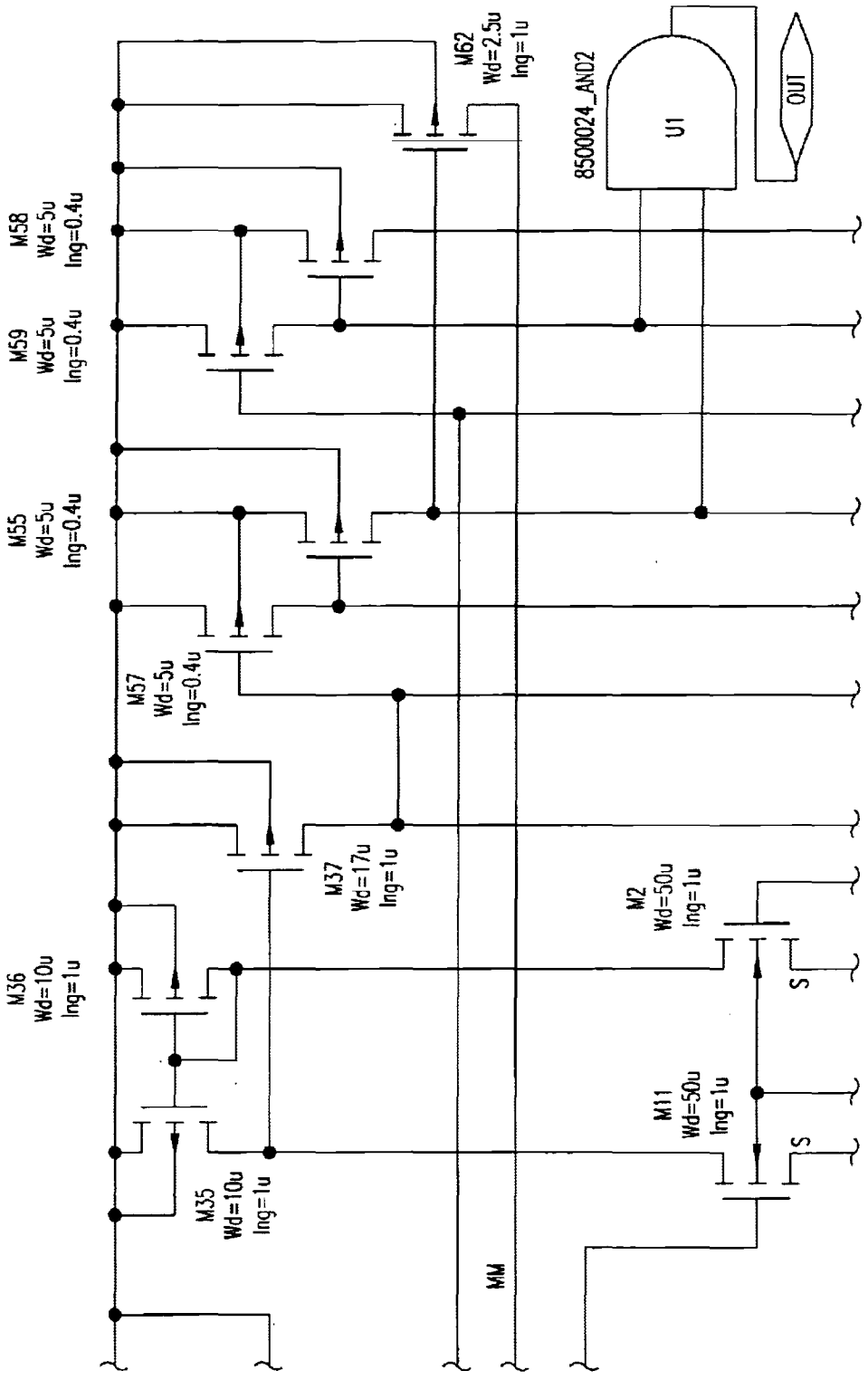

M62
Wd=2.5u
lng=1u
8500024_AND2
U1
OUT
M58
Wd=5u
lng=0.4u
M59
Wd=5u
lng=0.4u
M55
Wd=5u
lng=0.4u
M57
Wd=5u
lng=0.4u
M37
Wd=17u
lng=1u
M2
Wd=50u
lng=1u
S
M36
Wd=10u
lng=1u
M11
Wd=50u
lng=1u
S
M35
Wd=10u
lng=1u
MM

FIG.123D

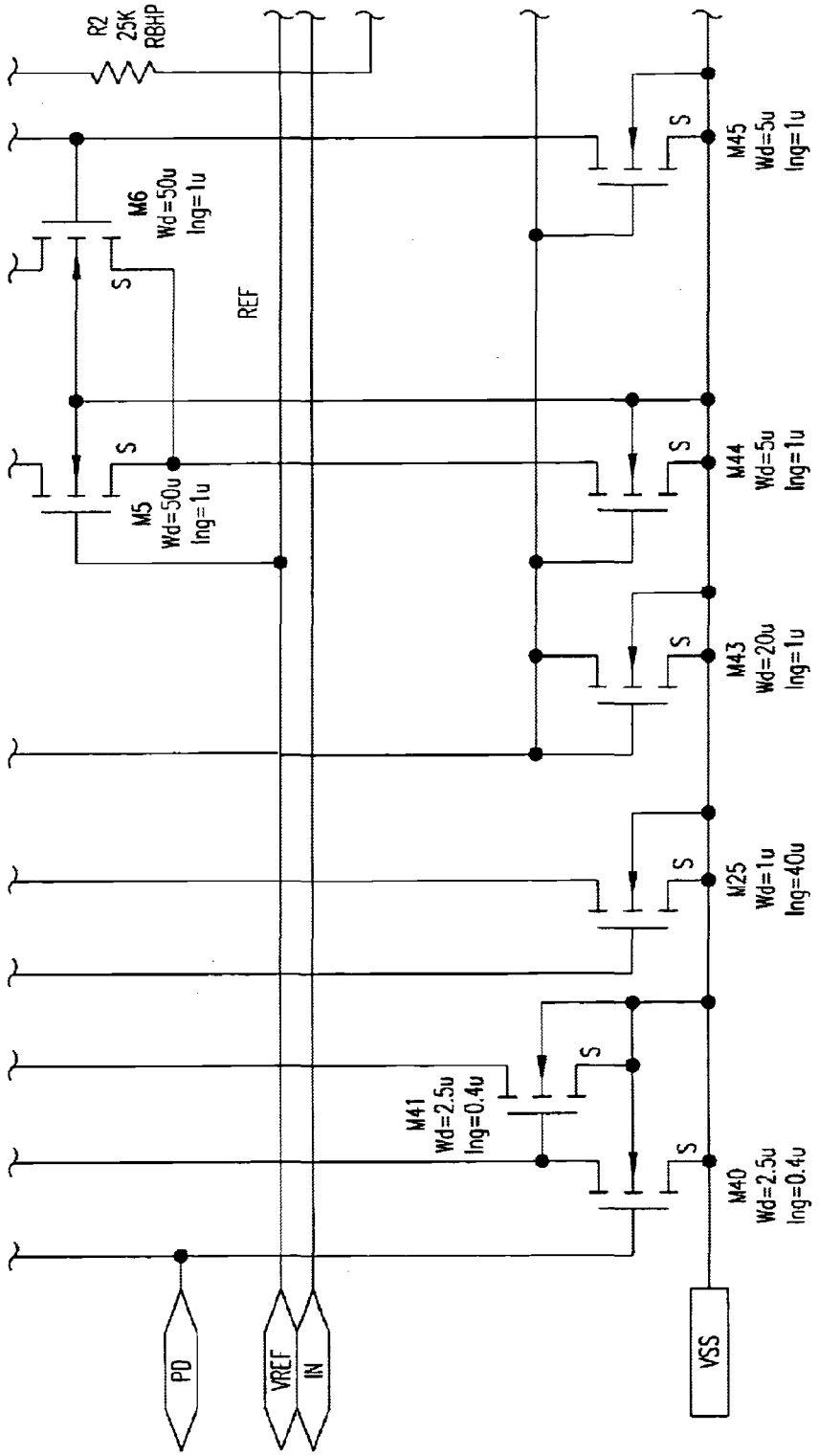

R2
25K
RBHP
M6
Wd=50u
lng=1u
S
REF
M5
Wd=50u
lng=1u
M45
Wd=5u
lng=1u
M44
Wd=5u
lng=1u
M43
Wd=20u
lng=1u
M25
Wd=1u
lng=40u
M41
Wd=2.5u
lng=0.4u
M40
Wd=2.5u
lng=0.4u
OP AMP
BIAS
2 INVERTERS
PD
VREF
IN
VSS

FIG.123E

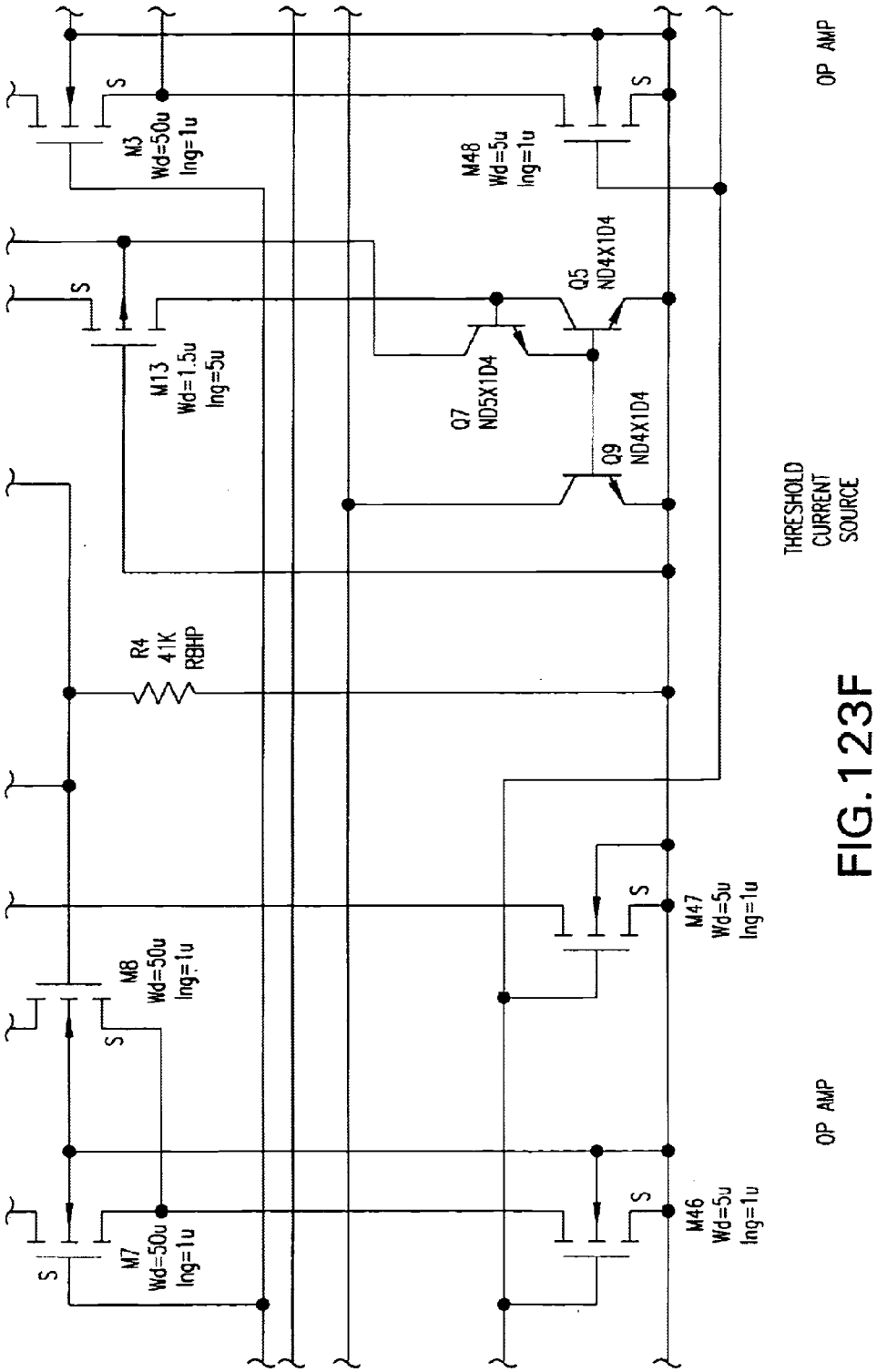

OP AMP
M3
Wd=50u
lng=1u
M48
Wd=5u
lng=1u
Q5
ND4X1D4
Q7
ND5X1D4
Q9
ND4X1D4
M13
Wd=1.5u
lng=5u
R4
41K
RBHP
THRESHOLD
CURRENT
SOURCE
M8
Wd=50u
lng=1u
M47
Wd=5u
lng=1u
M7
Wd=50u
lng=1u
M46
Wd=5u
lng=1u
OP AMP
S

FIG.123F

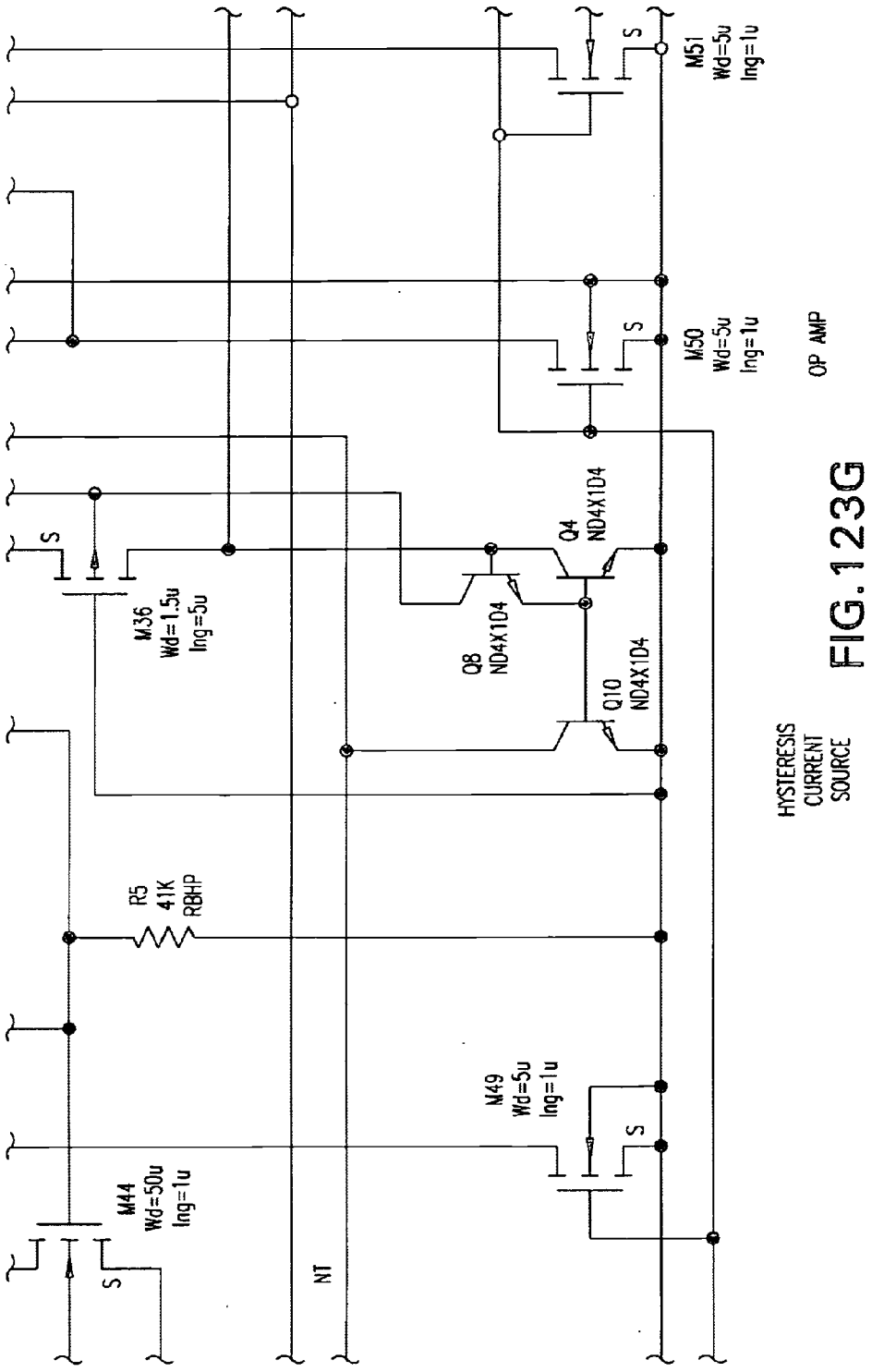

M51
Wd=5u
lng=1u
S
M50
Wd=5u
lng=1u
OP AMP
Q4
ND4X1D4
Q8
ND4X1D4
Q10
ND4X1D4
M36
Wd=1.5u
lng=5u
HYSTERESIS
CURRENT
SOURCE
R5
41K
RBHP
M49
Wd=5u
lng=1u
M44
Wd=50u
lng=1u
NT

FIG. 123G

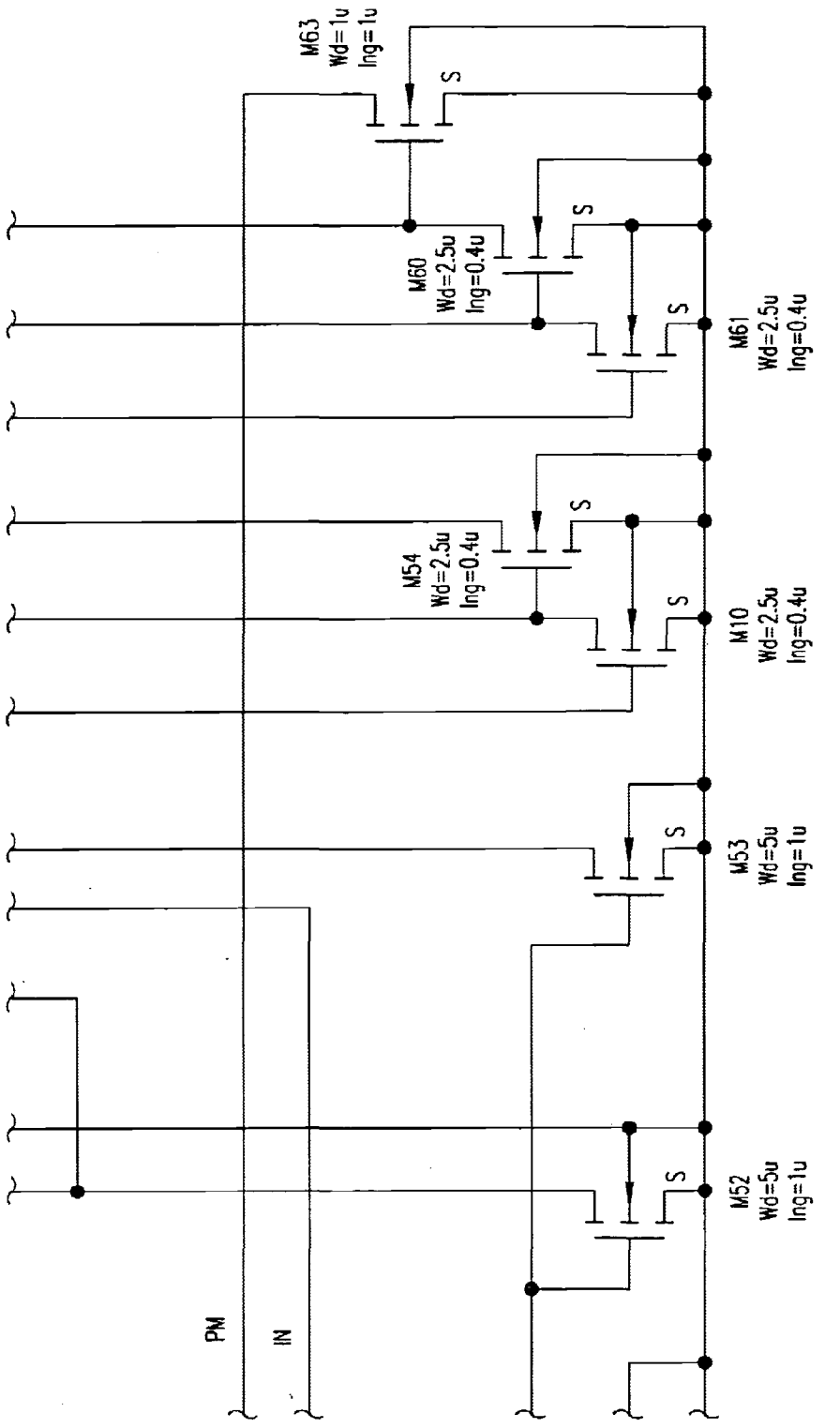

M63
Wd=1u
lng=1u
M60
Wd=2.5u
lng=0.4u
M61
Wd=2.5u
lng=0.4u
M54
Wd=2.5u
lng=0.4u
M10
Wd=2.5u
lng=0.4u
M53
Wd=5u
lng=1u
M52
Wd=5u
lng=1u
S
PW
IN
4 INVERTERS
OP AMP

FIG. 123H

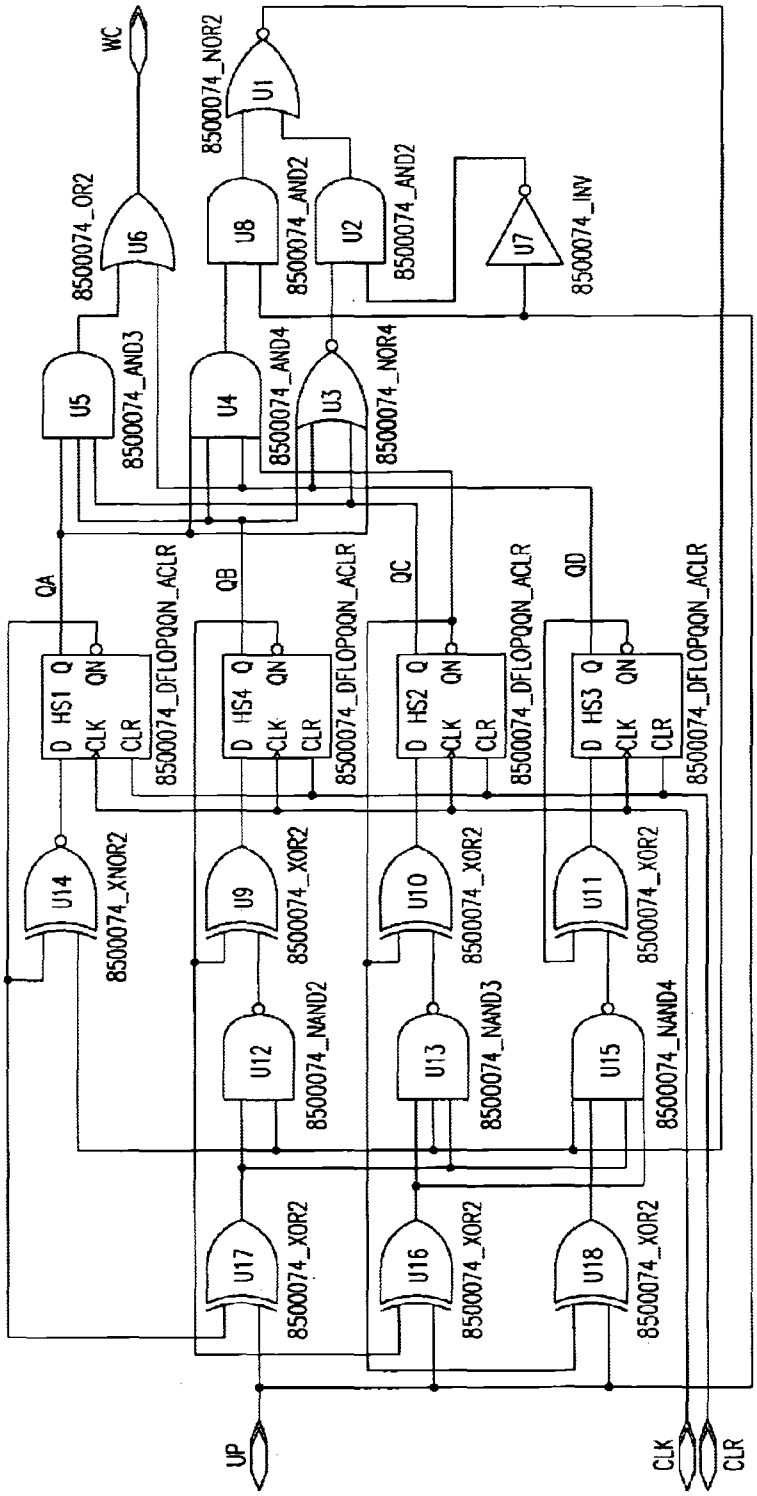

WC
8500074_NOR2
U1
8500074_OR2
U6
8500074_AND2
U8
8500074_AND2
U2
8500074_INV
U7
8500074_AND3
U5
8500074_AND4
U4
8500074_NOR4
U3
QA
QB
QC
QD
8500074_DFLOPQQN_ACLR
D HS1 Q QN
CLK CLR
D HS4 Q QN
CLK CLR
D HS2 Q QN
CLK CLR
D HS3 Q QN
CLK CLR
8500074_XNOR2
U14
8500074_XOR2
U9
8500074_XOR2
U10
8500074_XOR2
U11
8500074_NAND2
U12
8500074_NAND3
U13
8500074_NAND4
U15
8500074_XOR2
U17
8500074_XOR2
U16
8500074_XOR2
U18
UP
CLK
CLR

FIG.124

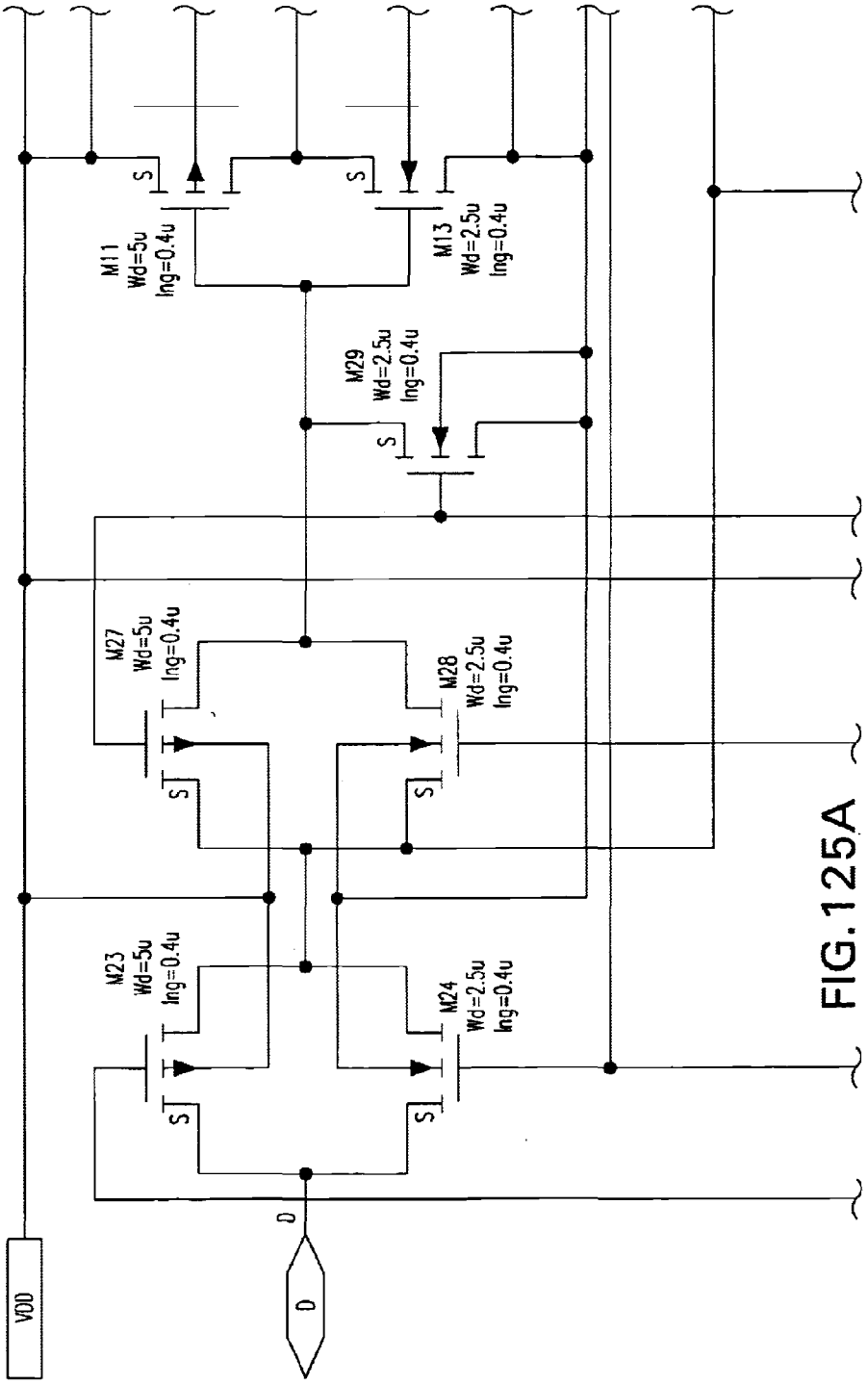

M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M29
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M28
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG. 125A

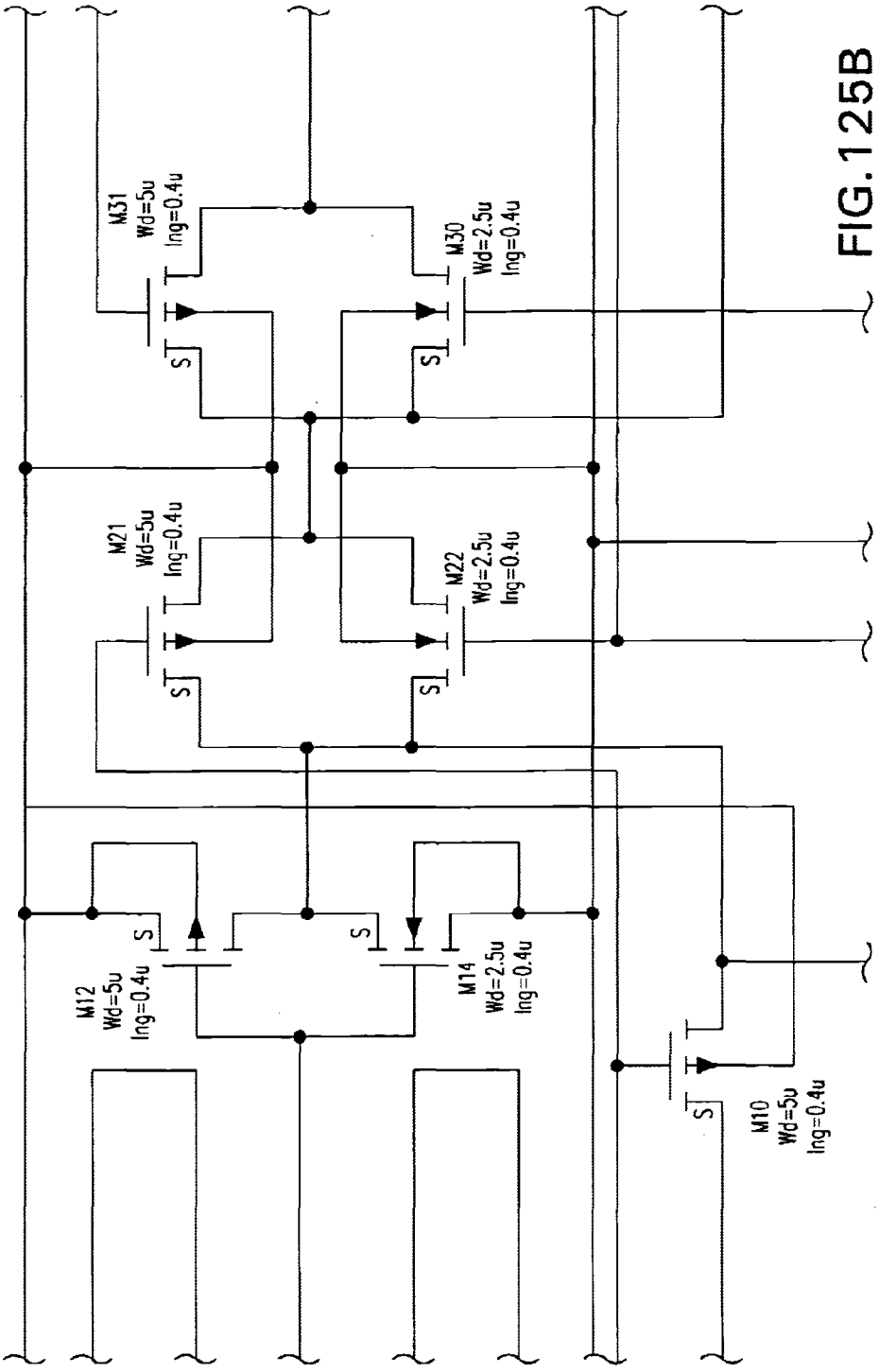

M31
Wd=5u
lng=0.4u
M30
Wd=2.5u
lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
S

FIG. 125B

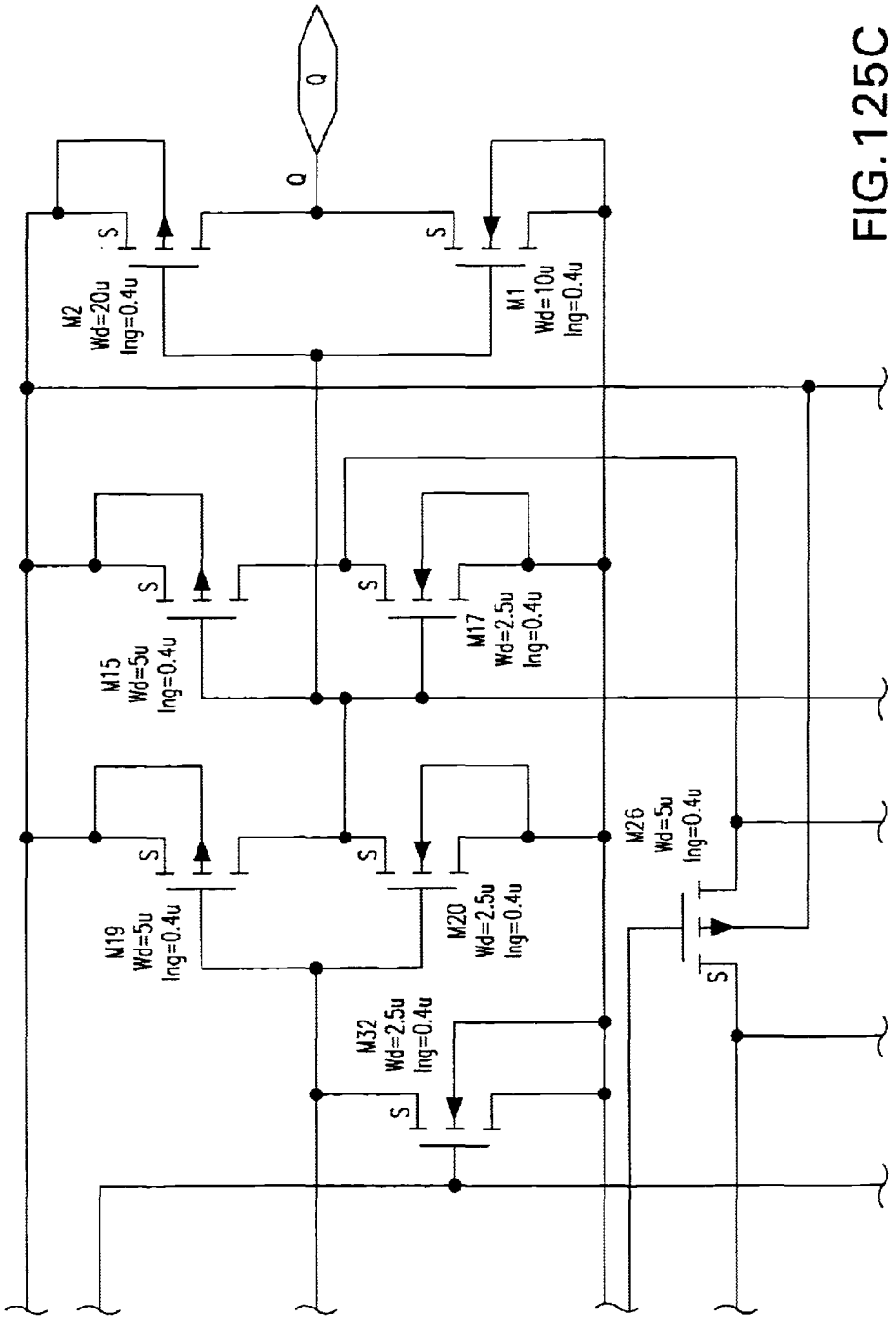

Q
Q
S
S
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
S
S
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
S
S
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
S
M32
Wd=2.5u
lng=0.4u
S

FIG.125C

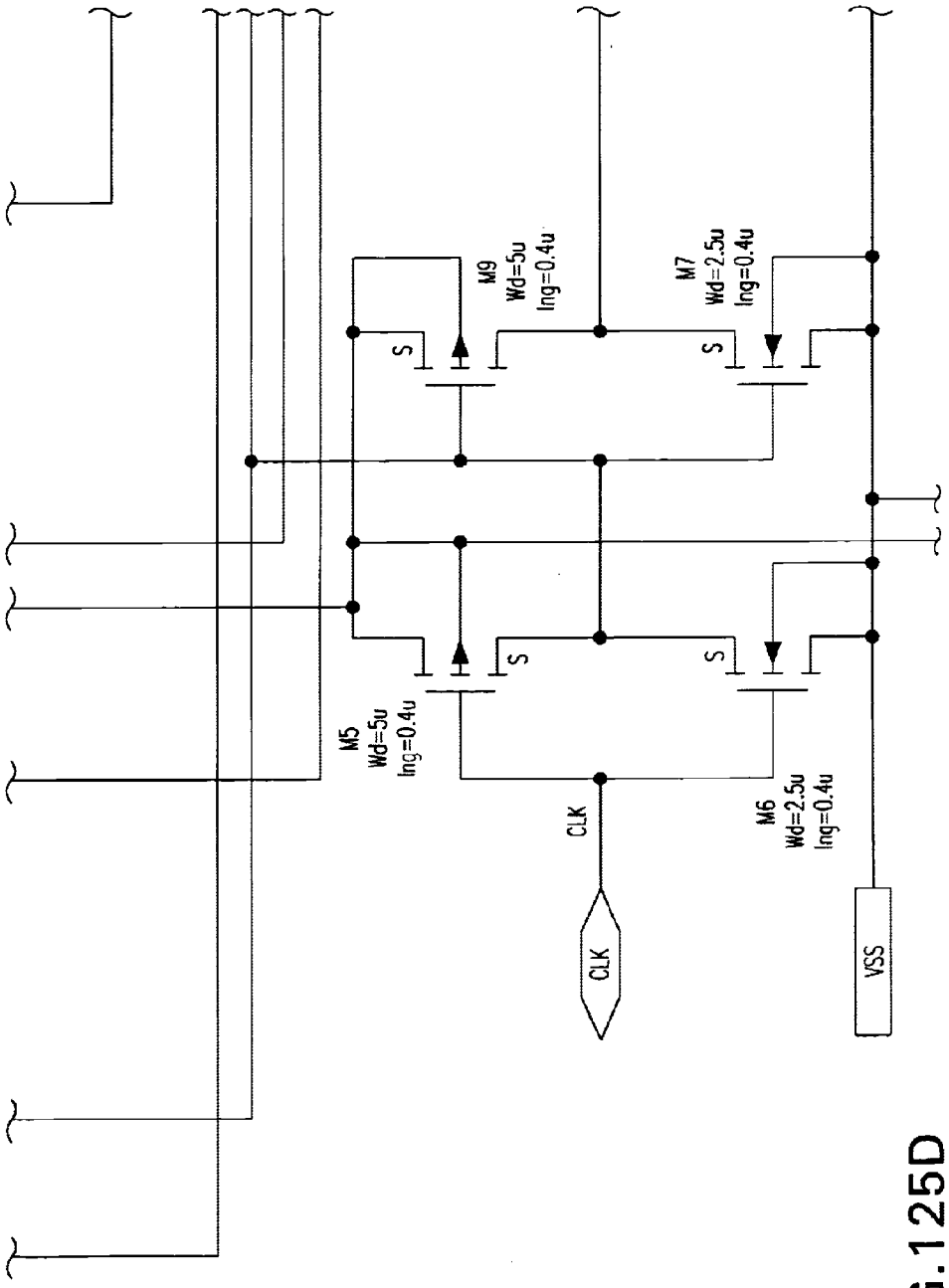

M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
S
S
S
S
M5
Wd=5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
CLK
CLK
VSS

FIG.125D

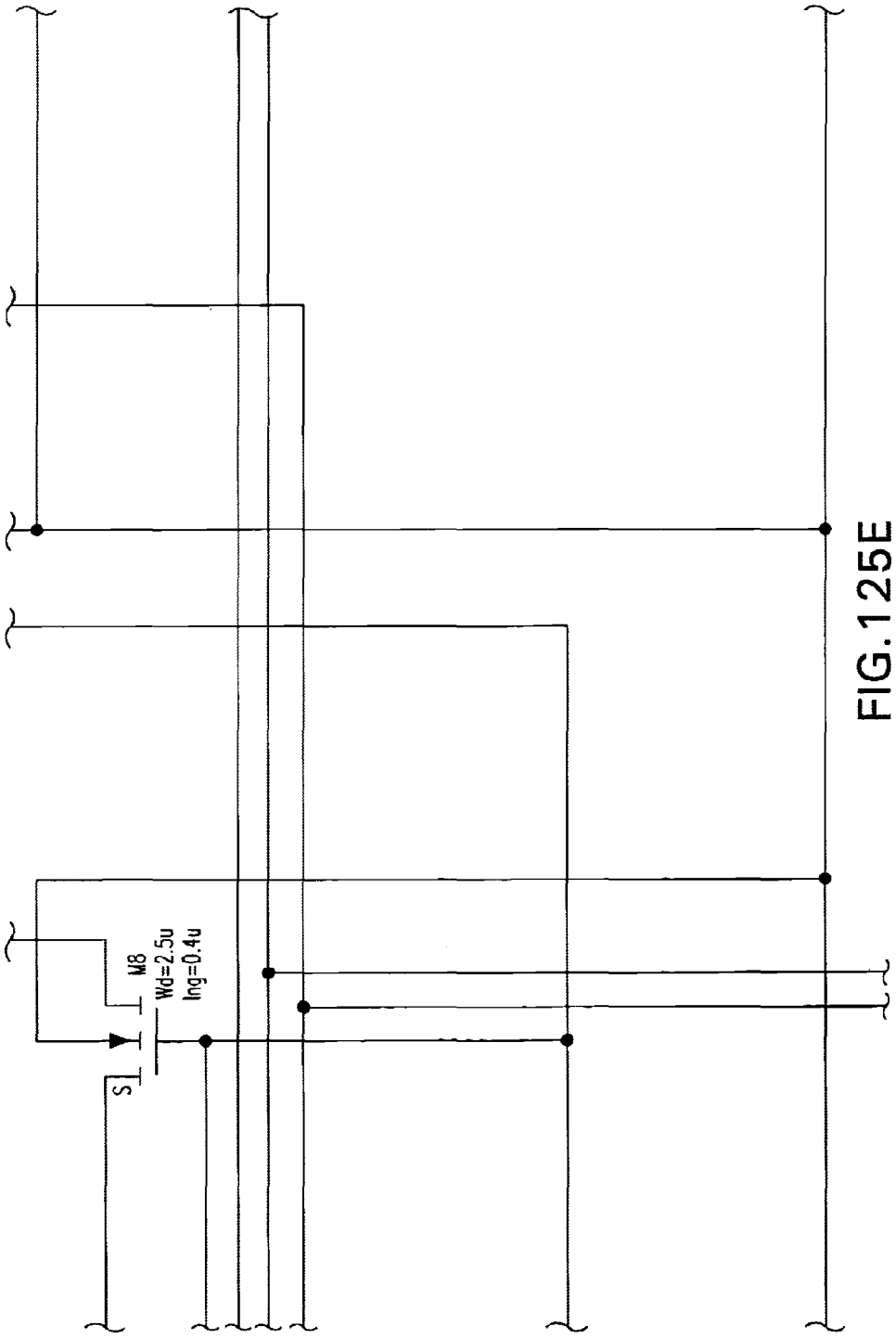


FIG.125E

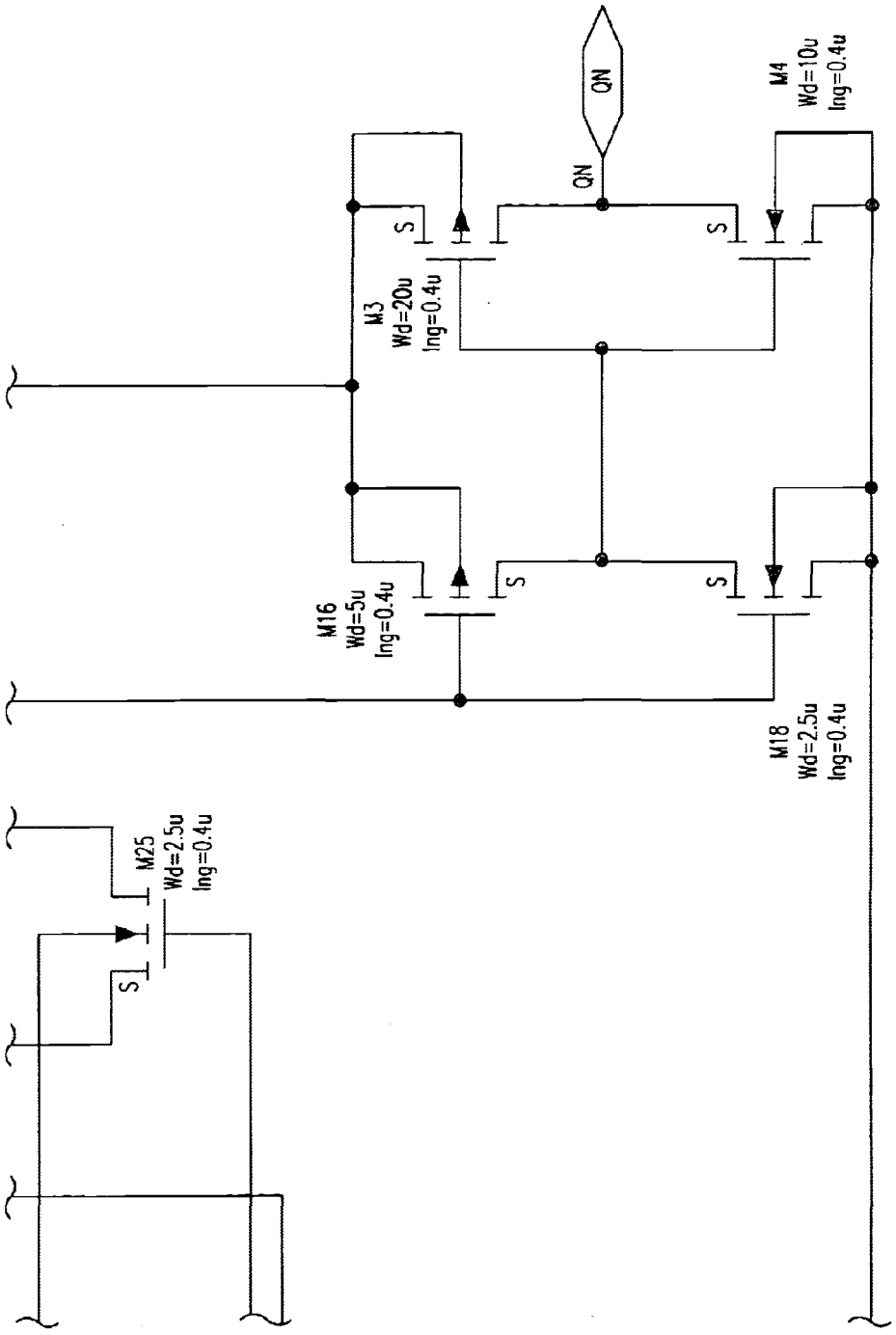

QN
QN
M4
Wd=10u
lng=0.4u
M3
Wd=20u
lng=0.4u
M16
Wd=5u
lng=0.4u
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S
S
S
S
S

FIG.125F

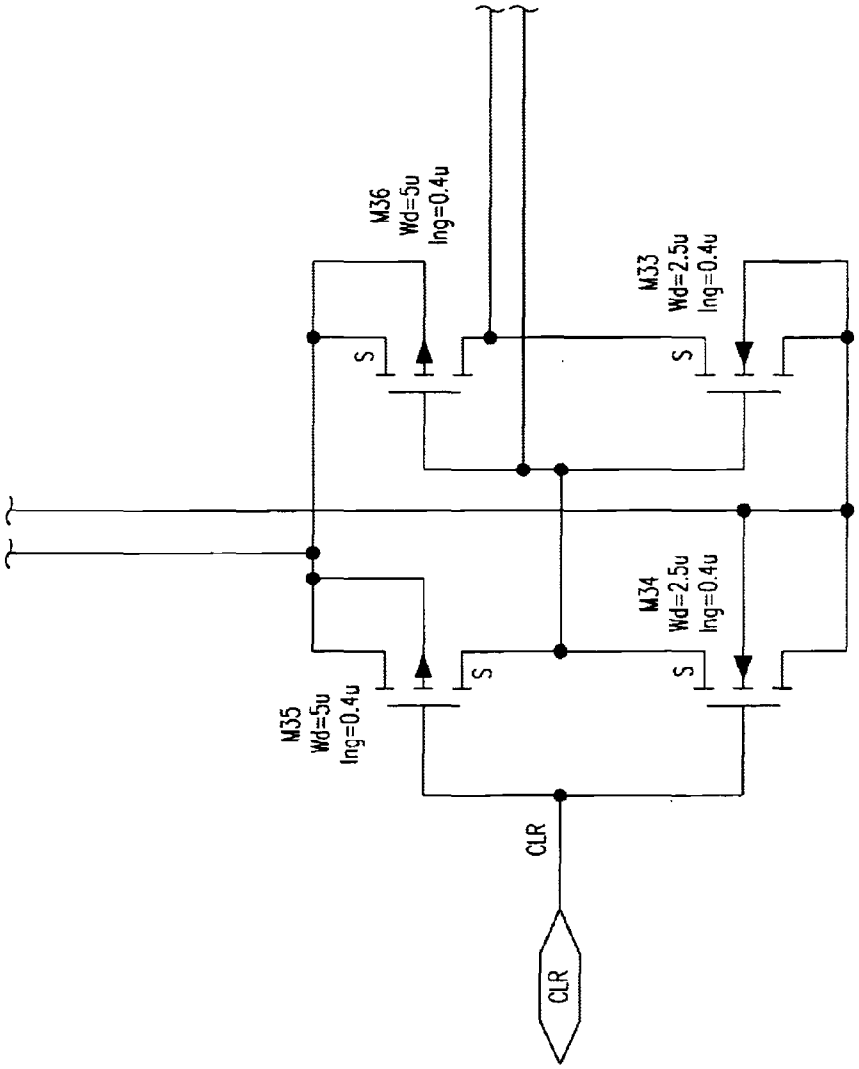
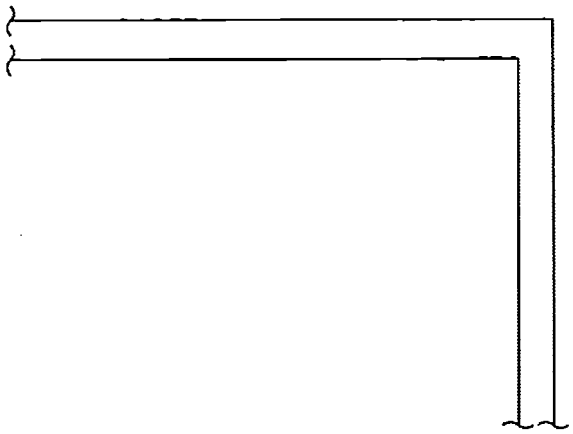

M36
Wd=5u
lng=0.4u
M33
Wd=2.5u
lng=0.4u
S
S
M34
Wd=2.5u
lng=0.4u
S
S
M35
Wd=5u
lng=0.4u
CLR
CLR

FIG.125G

FIG. 125H



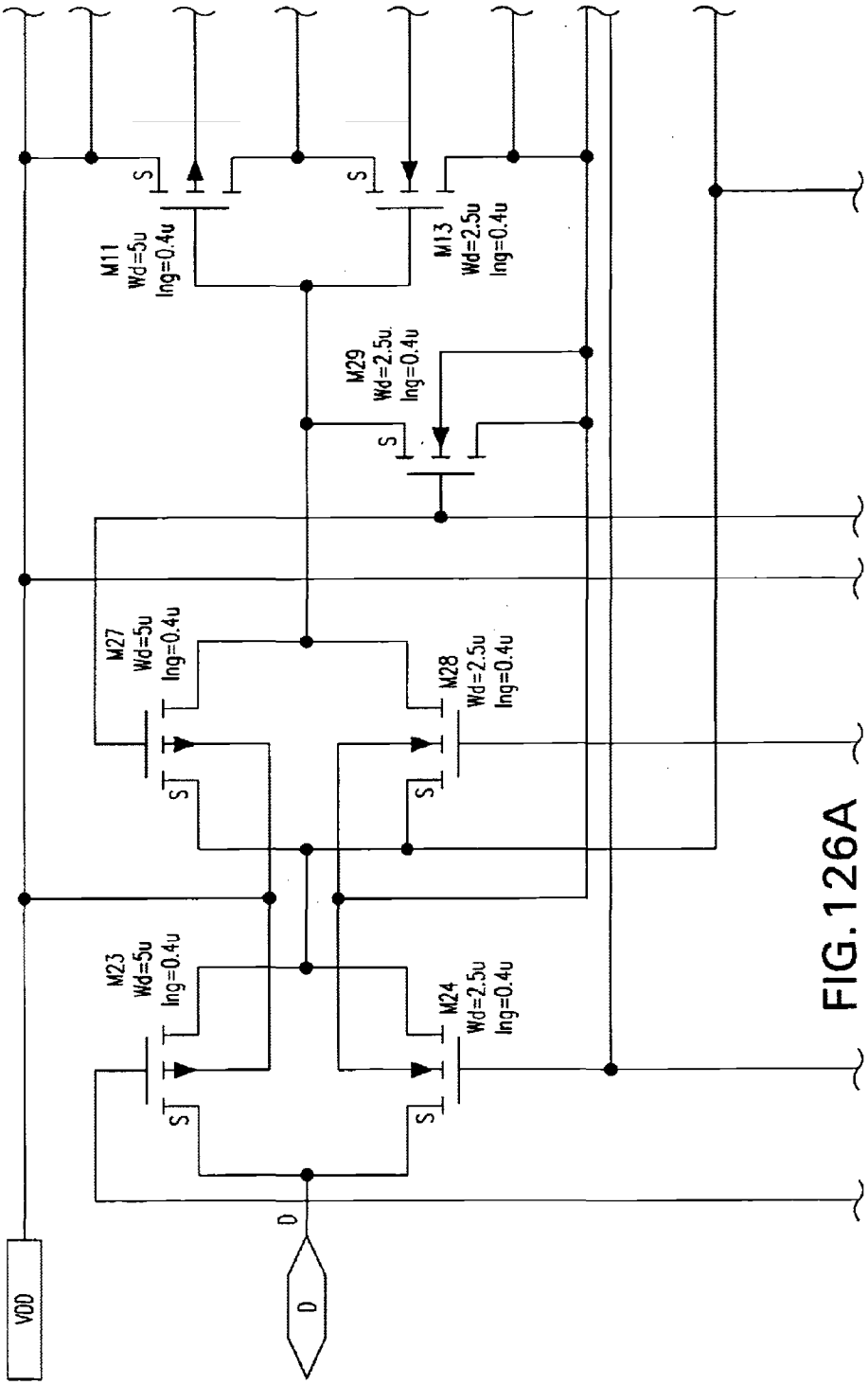

M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M29
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M28
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG. 126A

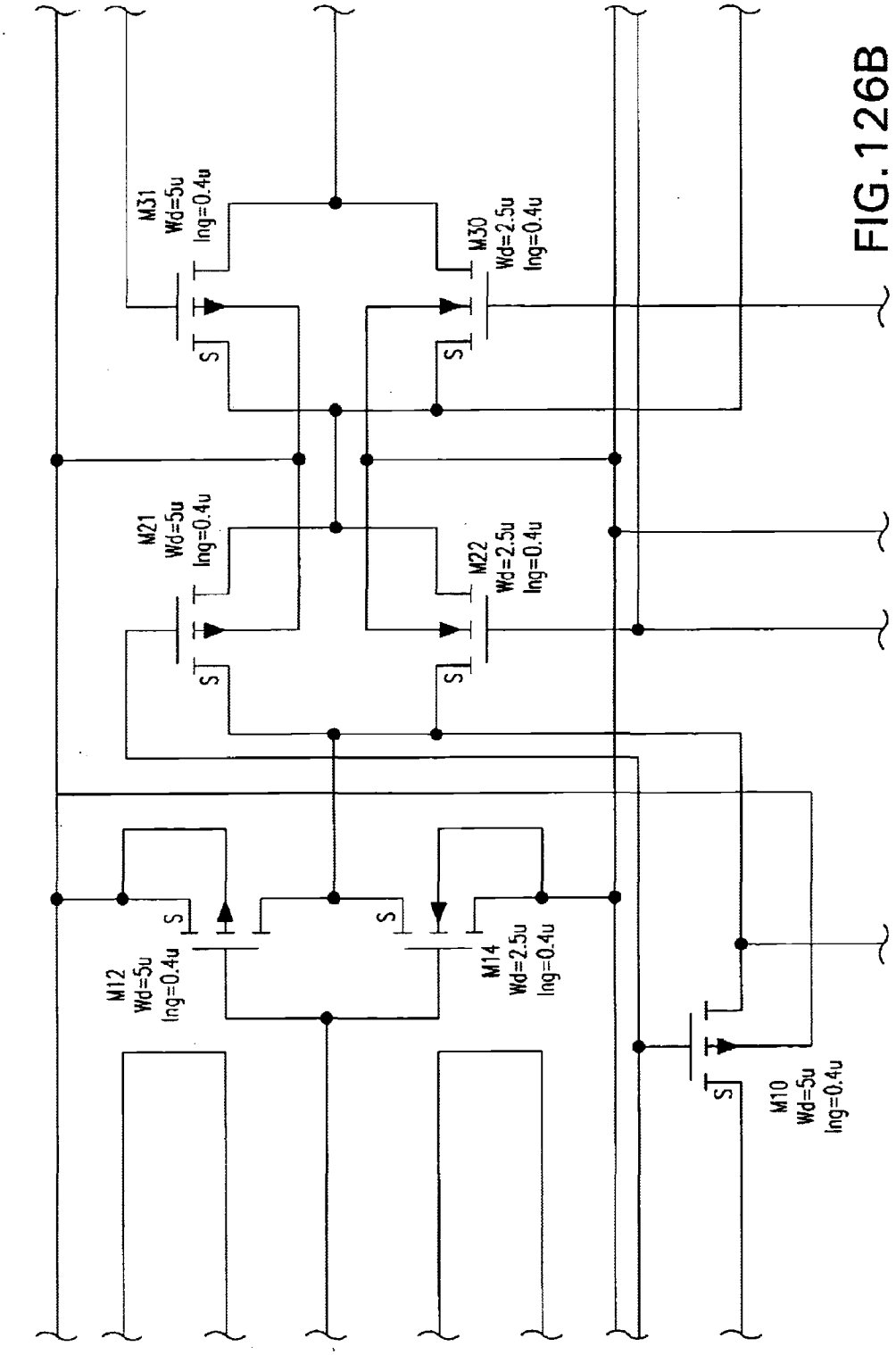

M31
Wd=5u
lng=0.4u
M30
Wd=2.5u
lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
S

FIG. 126B

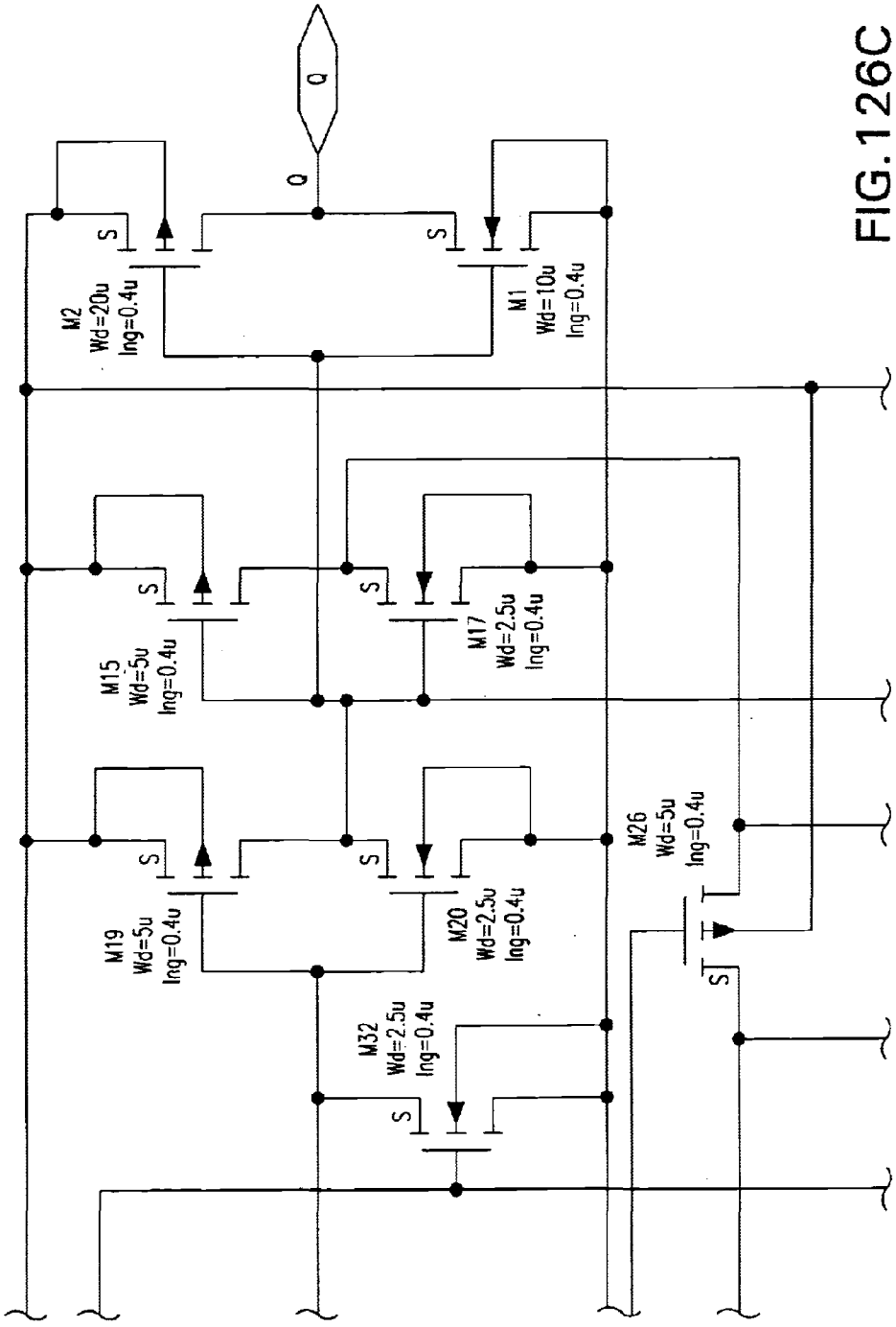

Q
Q
S
S
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
S
S
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
S
S
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
S
M32
Wd=2.5u
lng=0.4u
S

FIG. 126C

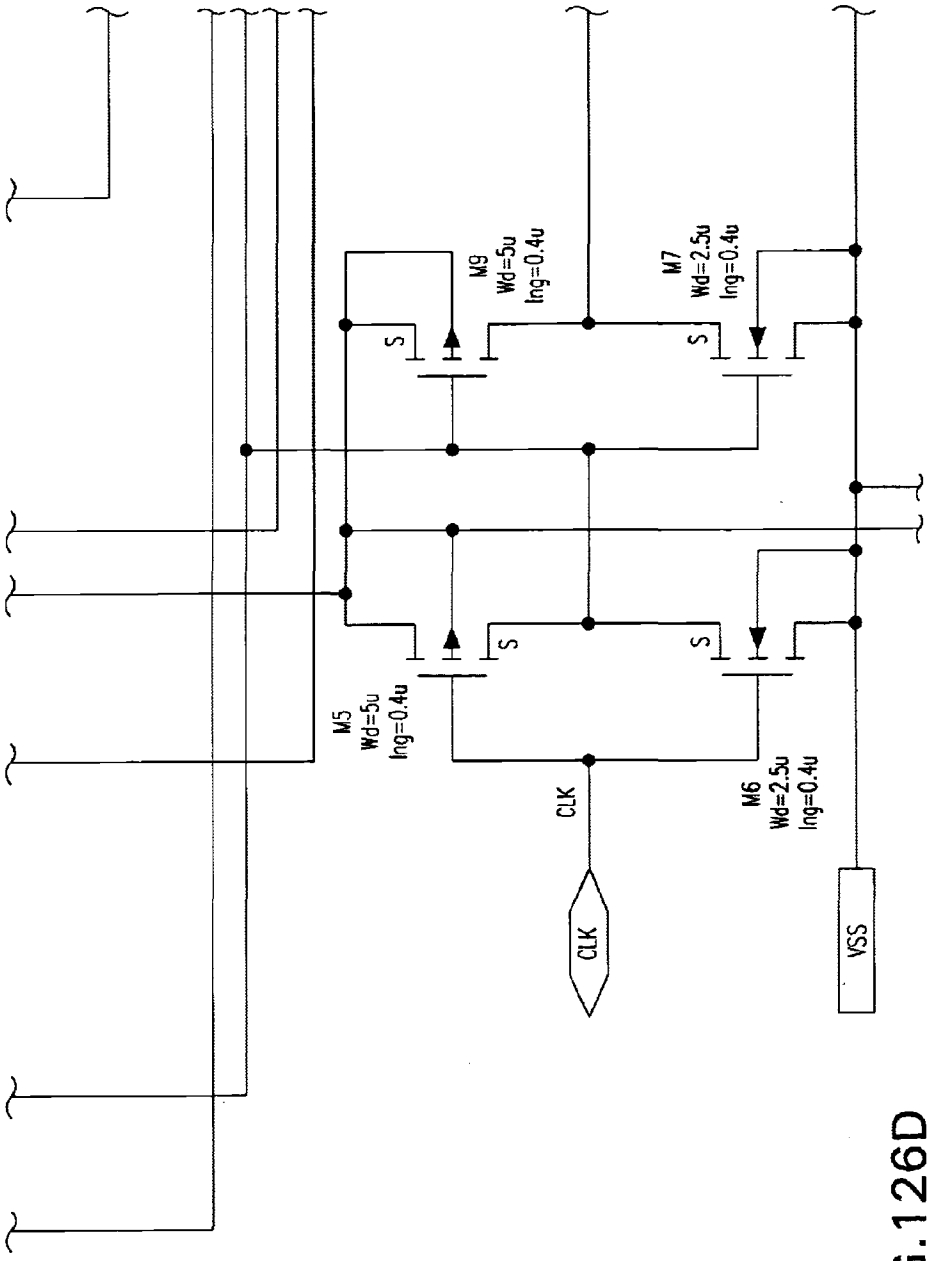

M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
S
S
S
S
M5
Wd=5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
CLK
CLK
VSS

FIG.126D

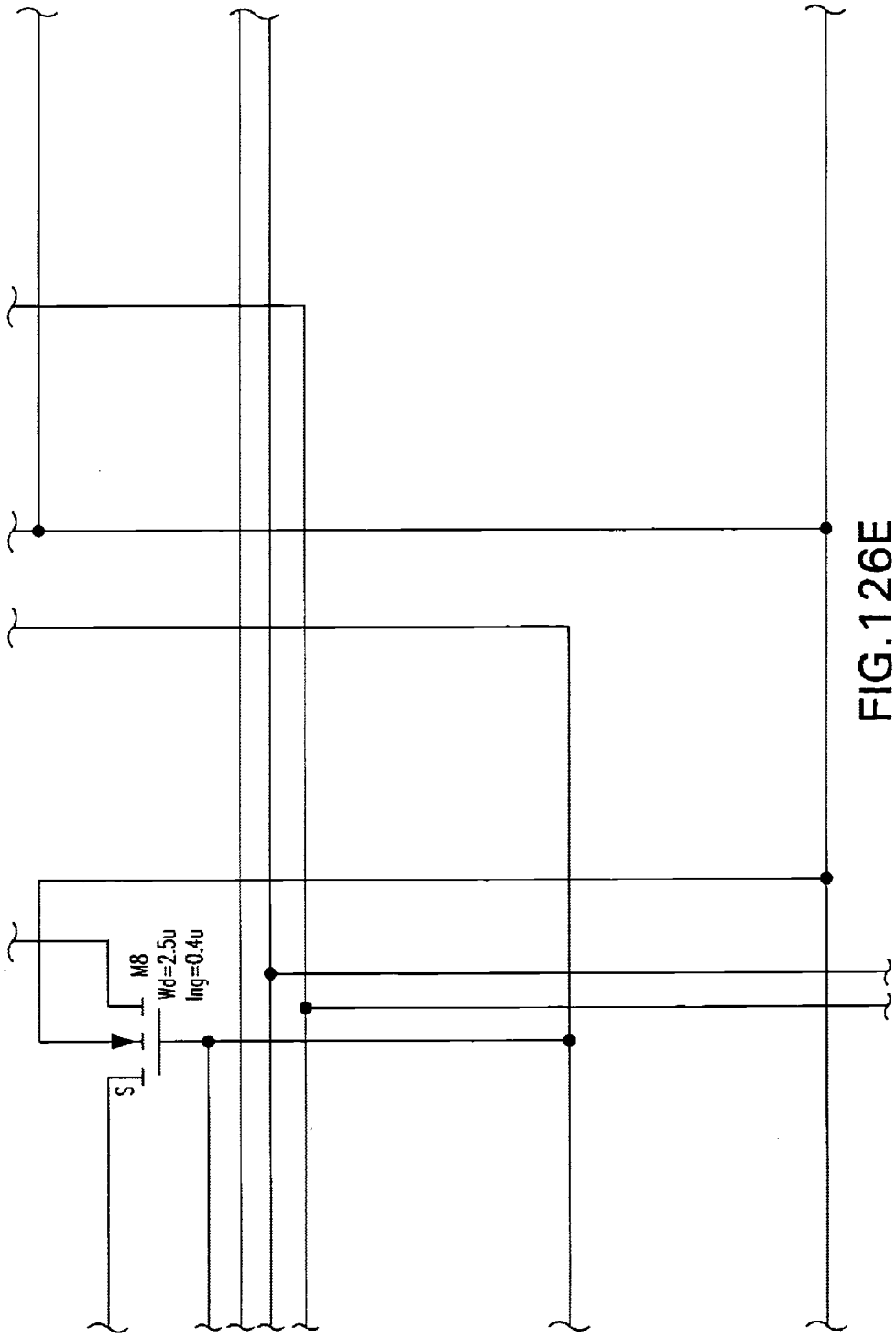


FIG.126E

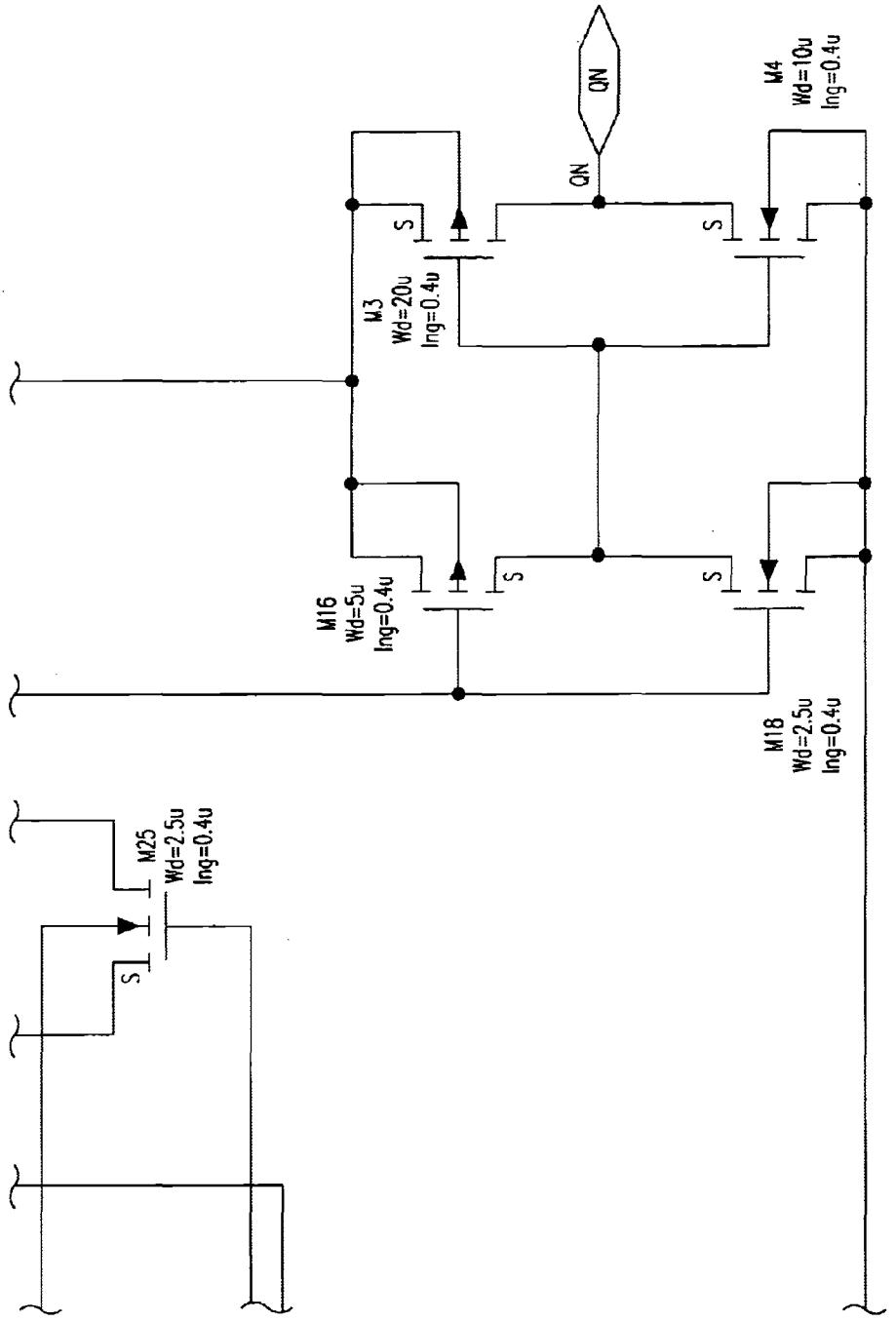

QN
QN
M4
Wd=10u
Lng=0.4u
M3
Wd=20u
Lng=0.4u
M16
Wd=5u
Lng=0.4u
M18
Wd=2.5u
Lng=0.4u
M25
Wd=2.5u
Lng=0.4u
S

FIG.126F

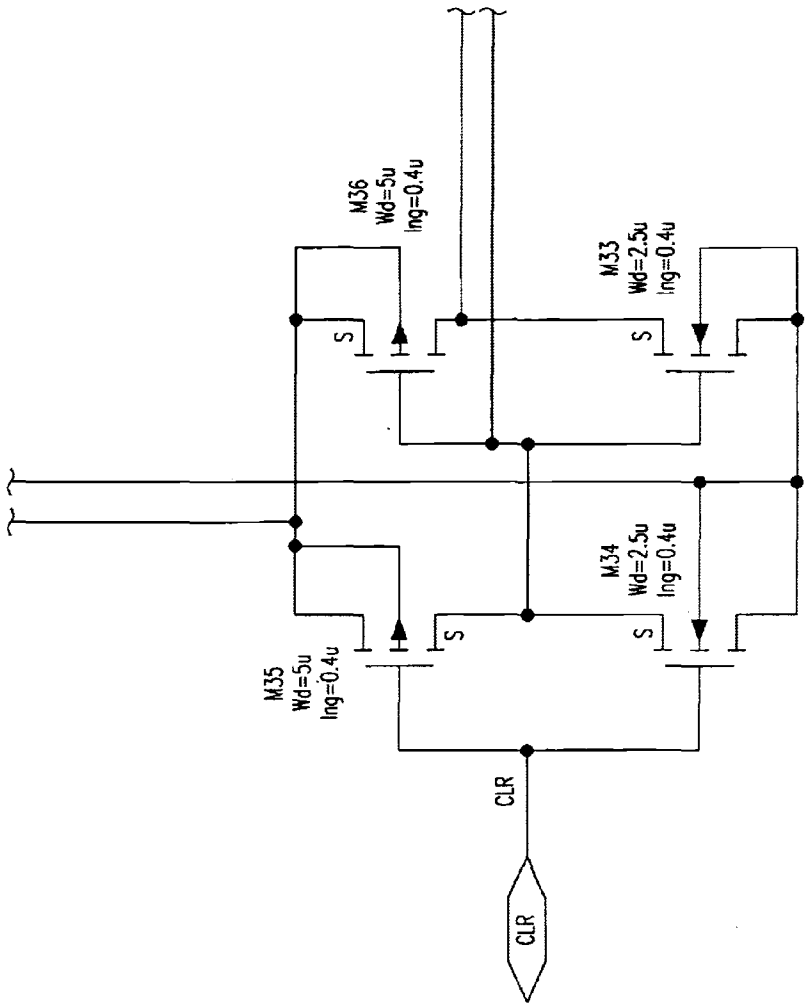
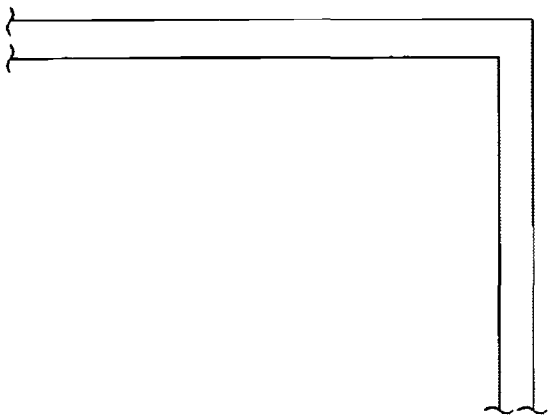

M36
Wd=5u
lng=0.4u
M33
Wd=2.5u
lng=0.4u
M34
Wd=2.5u
lng=0.4u
M35
Wd=5u
lng=0.4u
S
CLR
CLR

FIG.126G

FIG. 126H



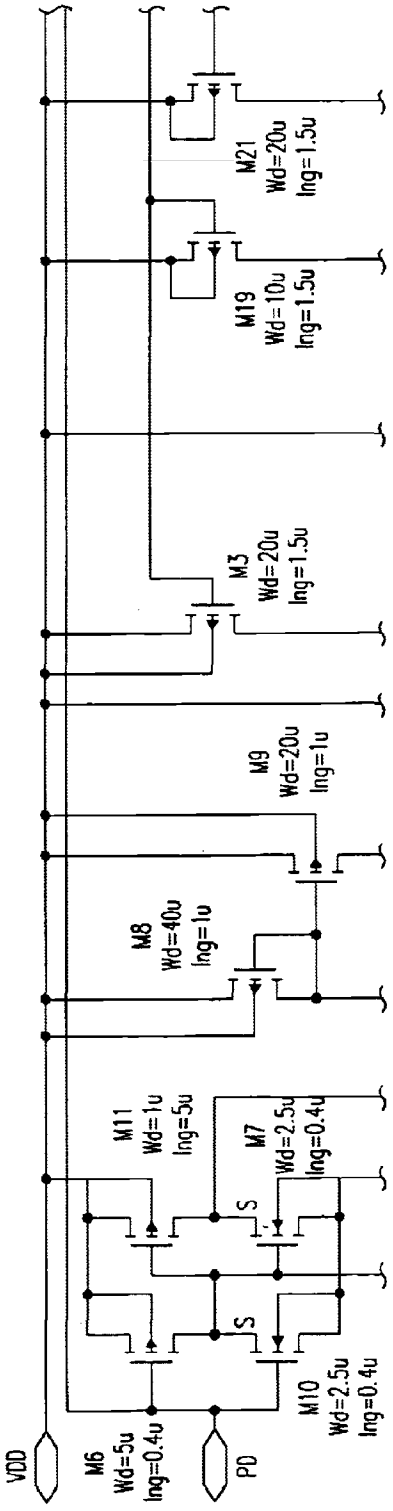

M21
Wd=20u
lng=1.5u
M19
Wd=10u
lng=1.5u
M3
Wd=20u
lng=1.5u
M9
Wd=20u
lng=1u
M8
Wd=40u
lng=1u
M11
Wd=1u
lng=5u
M7
Wd=2.5u
lng=0.4u
S
S
M10
Wd=2.5u
lng=0.4u
VDD
M6
Wd=5u
lng=0.4u
PD

FIG. 127A

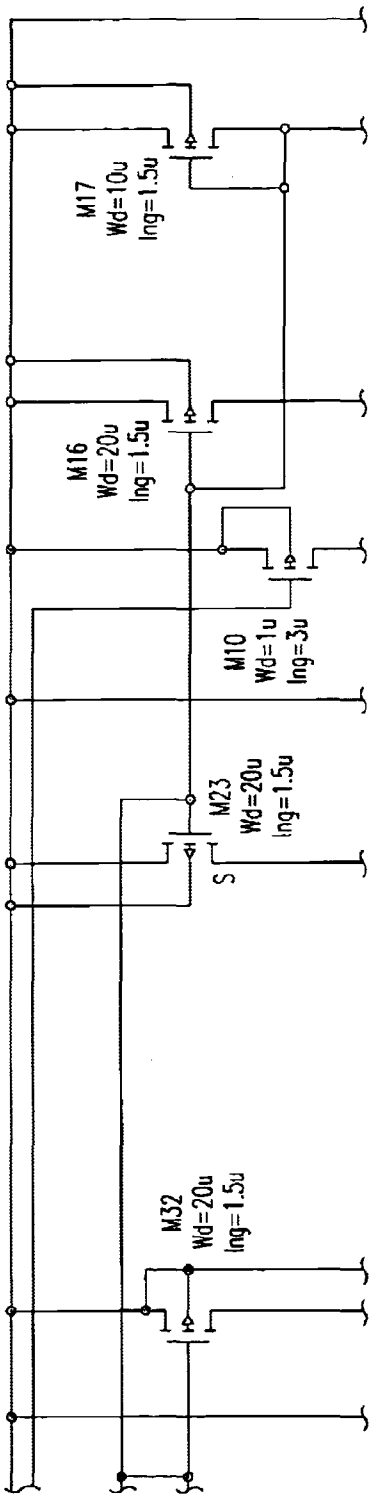

M17
Wd=10u
lng=1.5u
M16
Wd=20u
lng=1.5u
M10
Wd=1u
lng=3u
M23
Wd=20u
lng=1.5u
S
M32
Wd=20u
lng=1.5u

FIG. 127B

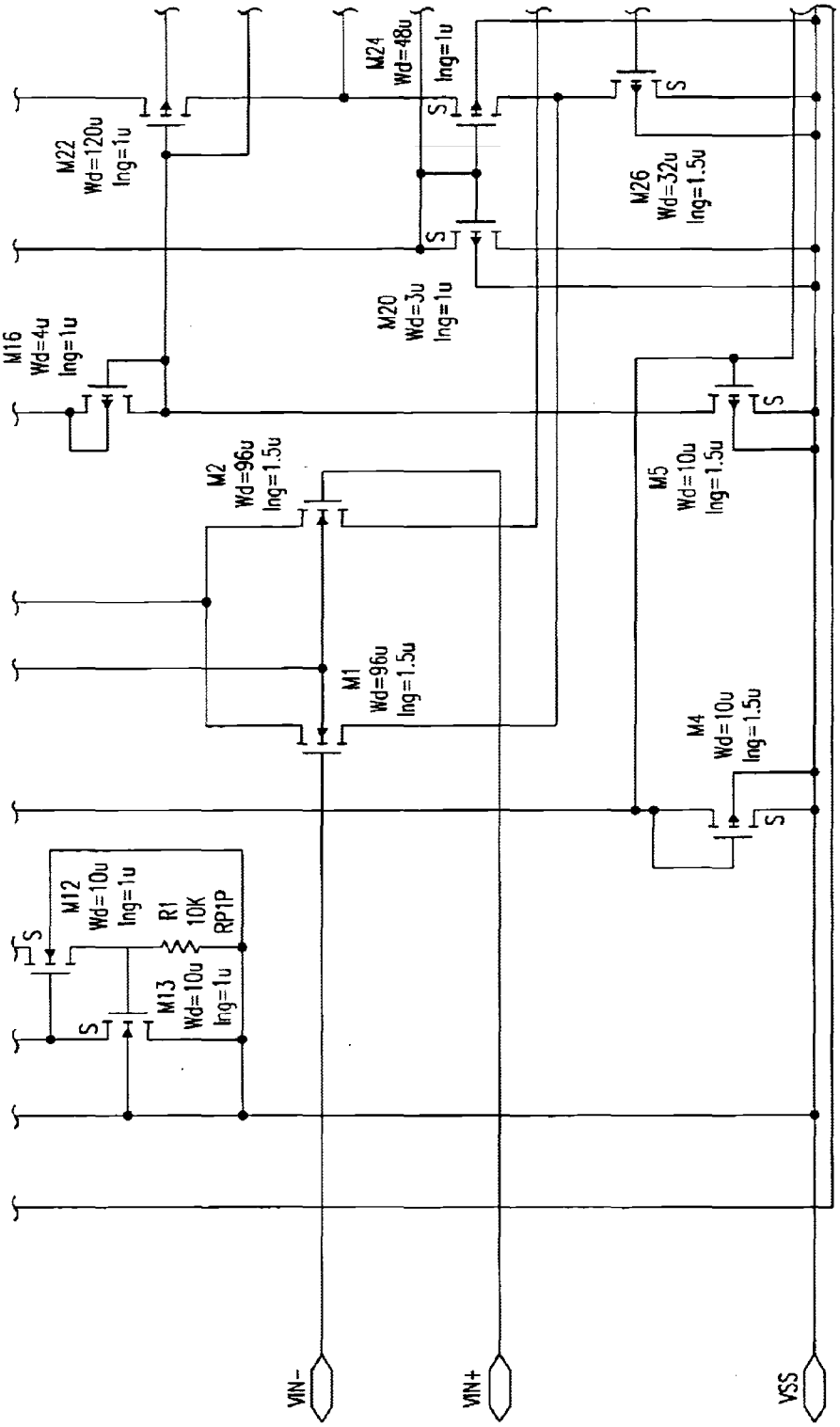

M24
Wd=48u
lng=1u
M22
Wd=120u
lng=1u
M26
Wd=32u
lng=1.5u
M20
Wd=3u
lng=1u
M16
Wd=4u
lng=1u
M2
Wd=96u
lng=1.5u
M5
Wd=10u
lng=1.5u
M1
Wd=96u
lng=1.5u
M4
Wd=10u
lng=1.5u
M12
Wd=10u
lng=1u
R1
10K
RP1P
M13
Wd=10u
lng=1u
S
VIN-
VIN+
VSS

FIG.127C

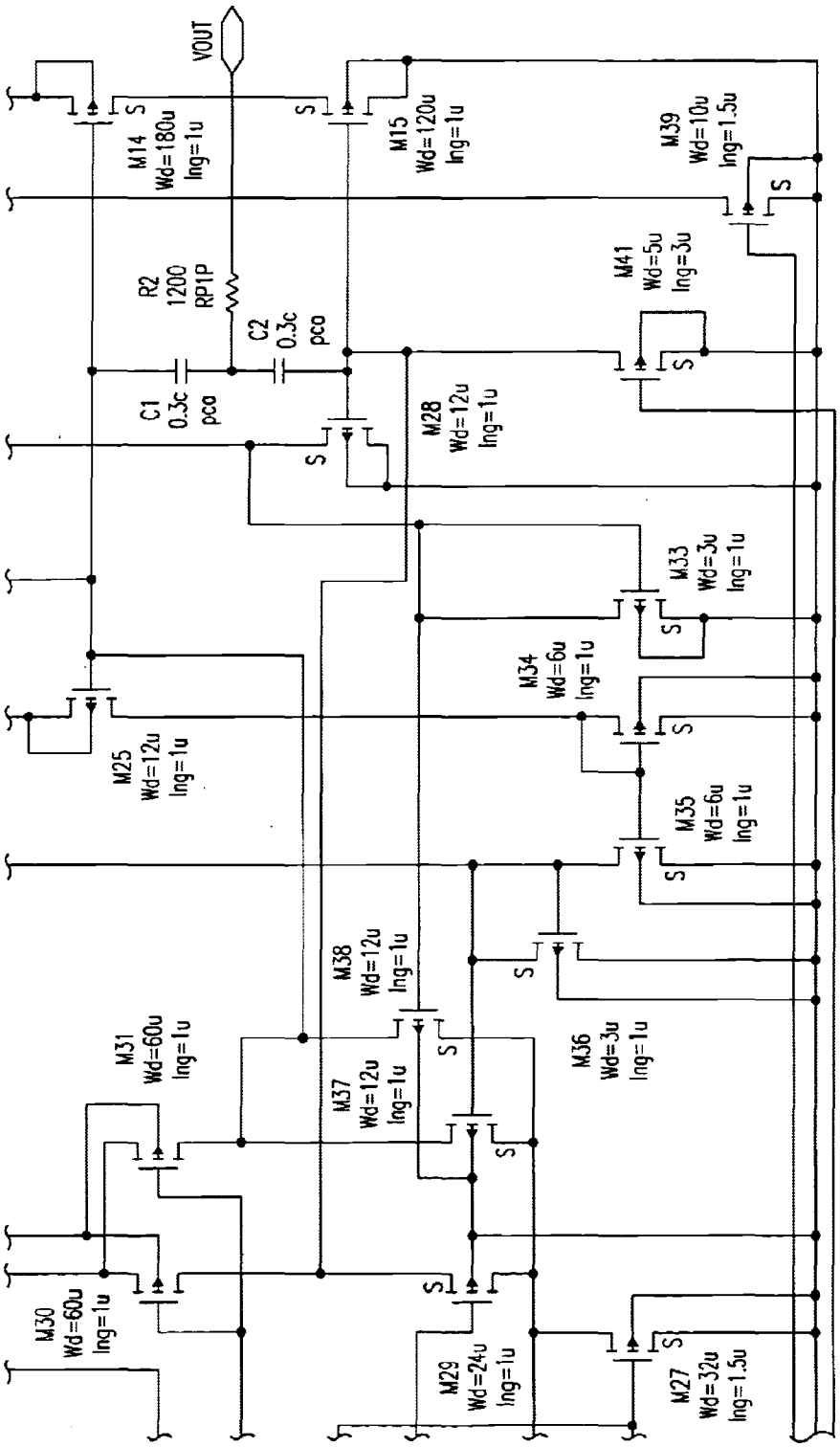

VOUT
M14 Wd=180u lng=1u
M15 Wd=120u lng=1u
M39 Wd=10u lng=1.5u
R2 1200 RPIP
C2 0.3c pca
C1 0.3c pca
M41 Wd=5u lng=3u
M28 Wd=12u lng=1u
M33 Wd=3u lng=1u
M34 Wd=6u lng=1u
M25 Wd=12u lng=1u
M35 Wd=6u lng=1u
M38 Wd=12u lng=1u
M31 Wd=60u lng=1u
M36 Wd=3u lng=1u
M37 Wd=12u lng=1u
M30 Wd=60u lng=1u
M29 Wd=24u lng=1u
M27 Wd=32u lng=1.5u
S

FIG.127D

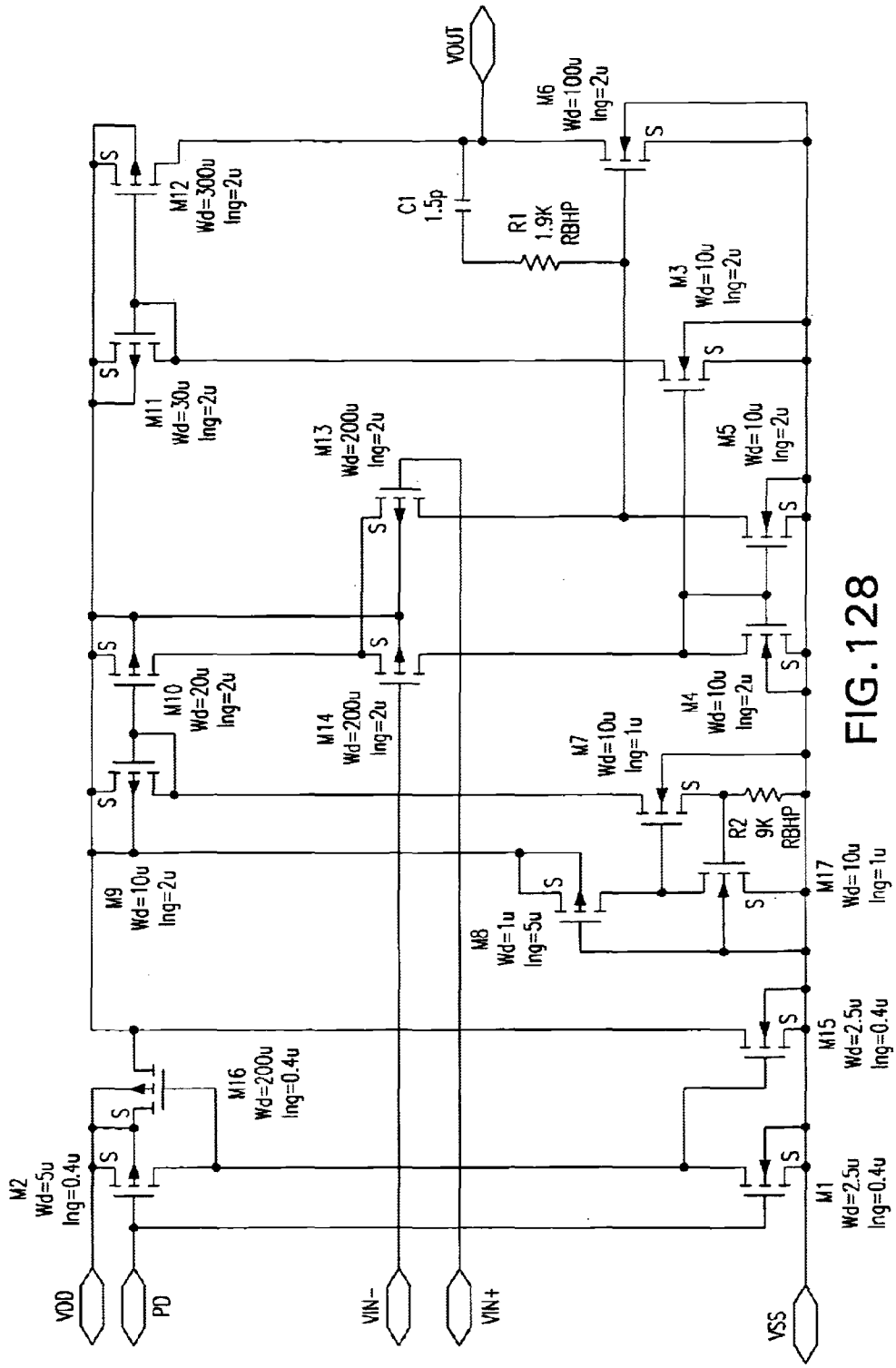

VOUT
M6 Wd=100u lng=2u
M12 Wd=300u lng=2u
C1 1.5p
R1 1.9K RBHP
M3 Wd=10u lng=2u
M11 Wd=30u lng=2u
M13 Wd=200u lng=2u
M5 Wd=10u lng=2u
M10 Wd=20u lng=2u
M14 Wd=200u lng=2u
M4 Wd=10u lng=2u
M7 Wd=10u lng=1u
R2 9K RBHP
M9 Wd=10u lng=2u
M8 Wd=1u lng=5u
M17 Wd=10u lng=1u
M15 Wd=2.5u lng=0.4u
M16 Wd=200u lng=0.4u
M2 Wd=5u lng=0.4u
M1 Wd=2.5u lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG. 128

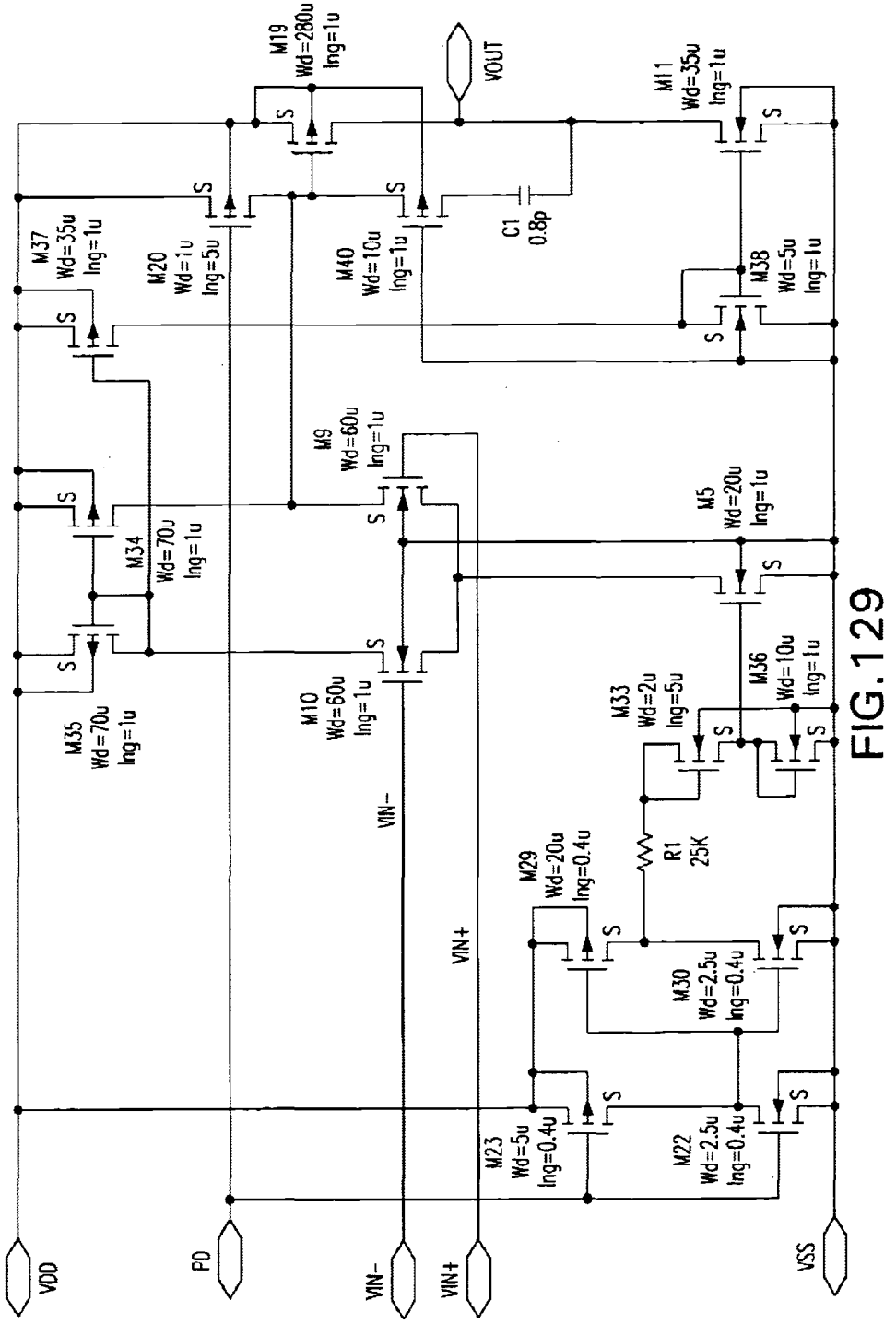

M19 Wd=280u lng=1u
VOUT
M11 Wd=35u lng=1u
M37 Wd=35u lng=1u
M20 Wd=1u lng=5u
M40 Wd=10u lng=1u
C1 0.8p
M38 Wd=5u lng=1u
M9 Wd=60u lng=1u
M5 Wd=20u lng=1u
M34 Wd=70u lng=1u
M36 Wd=10u lng=1u
M33 Wd=2u lng=5u
M10 Wd=60u lng=1u
M35 Wd=70u lng=1u
VIN-
R1 25K
M29 Wd=20u lng=0.4u
VIN+
M30 Wd=2.5u lng=0.4u
M23 Wd=5u lng=0.4u
M22 Wd=2.5u lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG.129

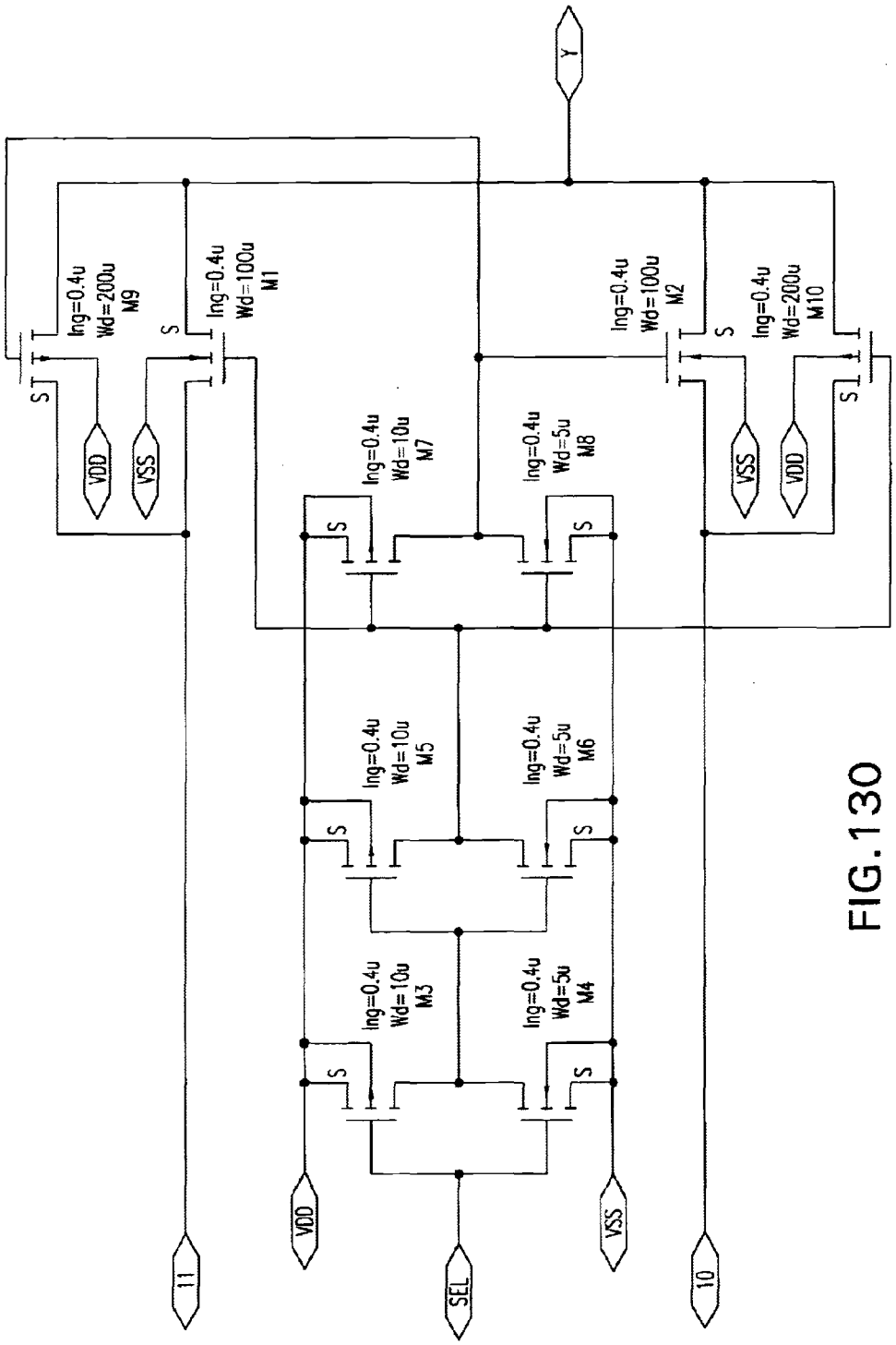

Y
lng=0.4u Wd=200u M9
lng=0.4u Wd=100u M1
lng=0.4u Wd=100u M2
lng=0.4u Wd=200u M10
lng=0.4u Wd=10u M7
lng=0.4u Wd=5u M8
lng=0.4u Wd=10u M5
lng=0.4u Wd=5u M6
lng=0.4u Wd=10u M3
lng=0.4u Wd=5u M4
S
VDD
VSS
11
SEL
10

FIG. 130

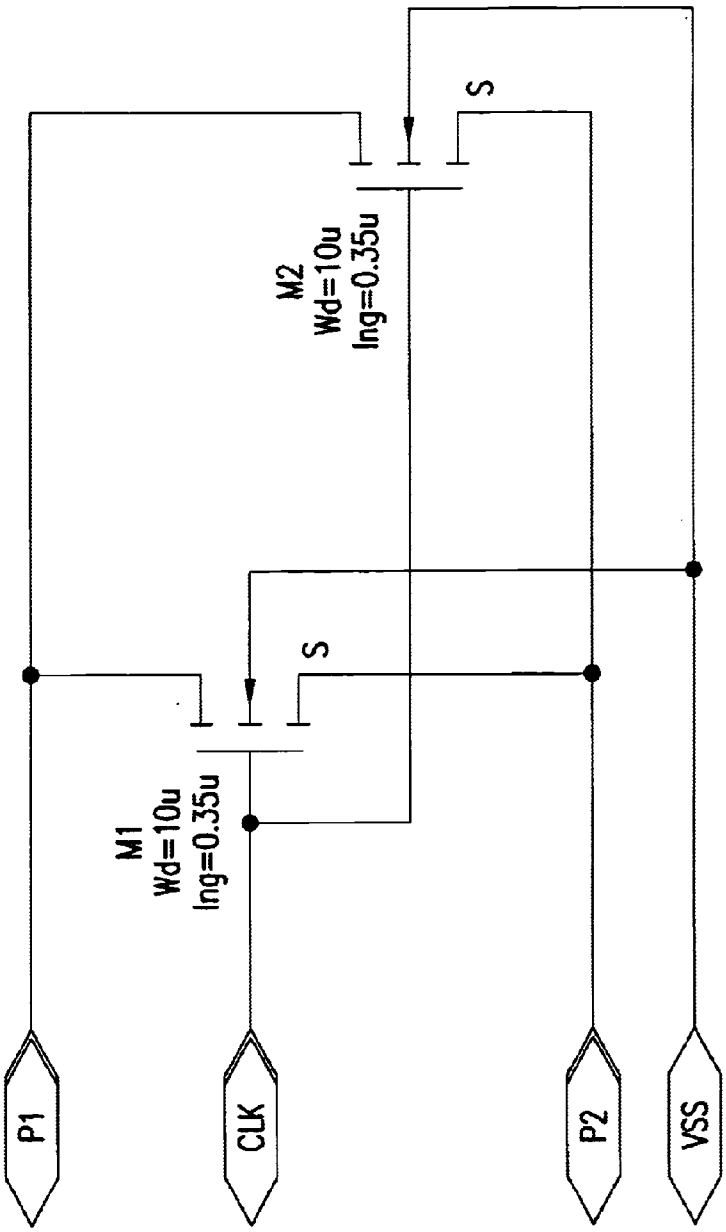


FIG. 131

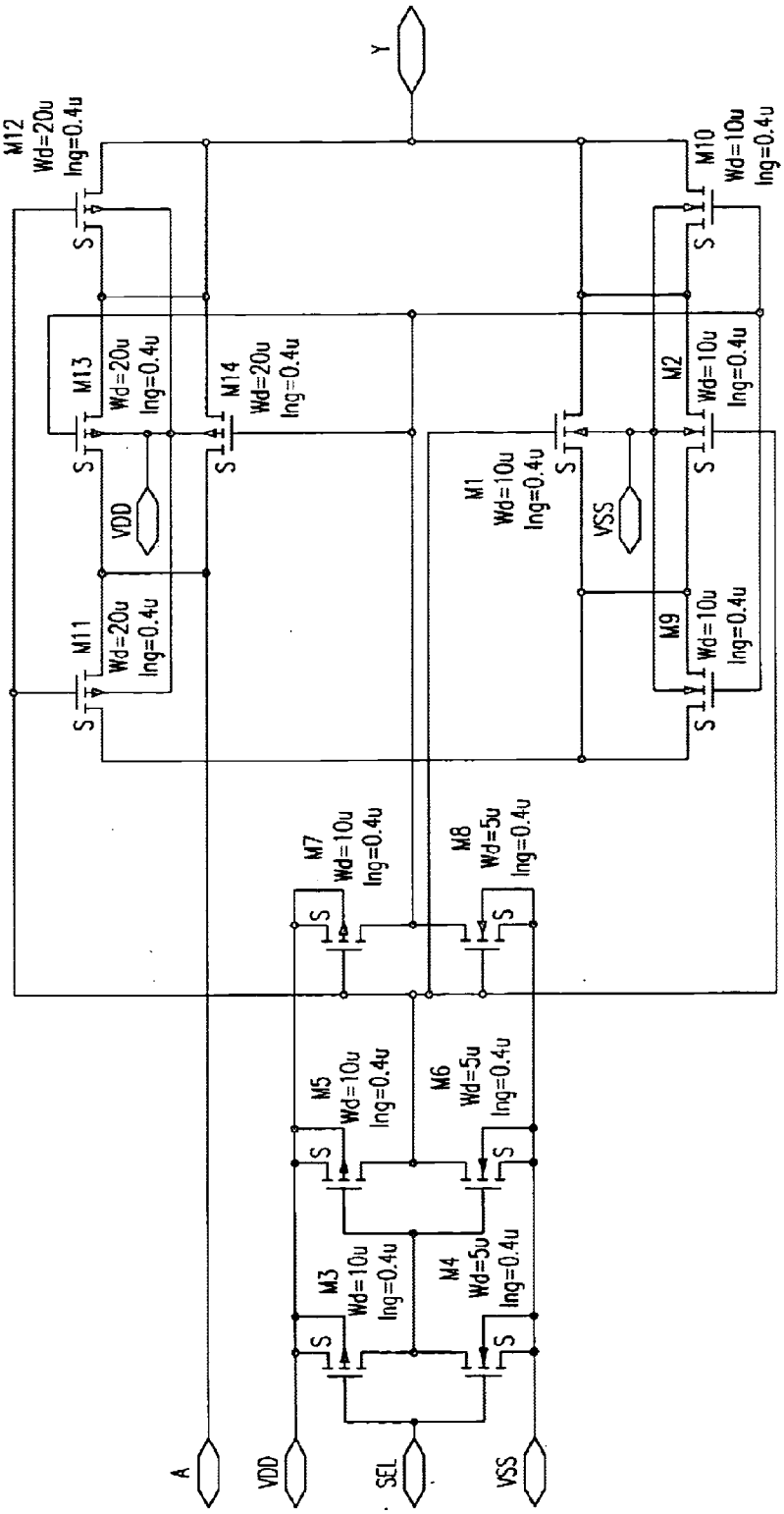

Y
M12 Wd=20u lng=0.4u
M10 Wd=10u lng=0.4u
M13 Wd=20u lng=0.4u
M14 Wd=20u lng=0.4u
M2 Wd=10u lng=0.4u
M1 Wd=10u lng=0.4u
VDD
VSS
M11 Wd=20u lng=0.4u
M9 Wd=10u lng=0.4u
M7 Wd=10u lng=0.4u
M8 Wd=5u lng=0.4u
M5 Wd=10u lng=0.4u
M6 Wd=5u lng=0.4u
M3 Wd=10u lng=0.4u
M4 Wd=5u lng=0.4u
S
A
VDD
SEL
VSS

FIG. 132

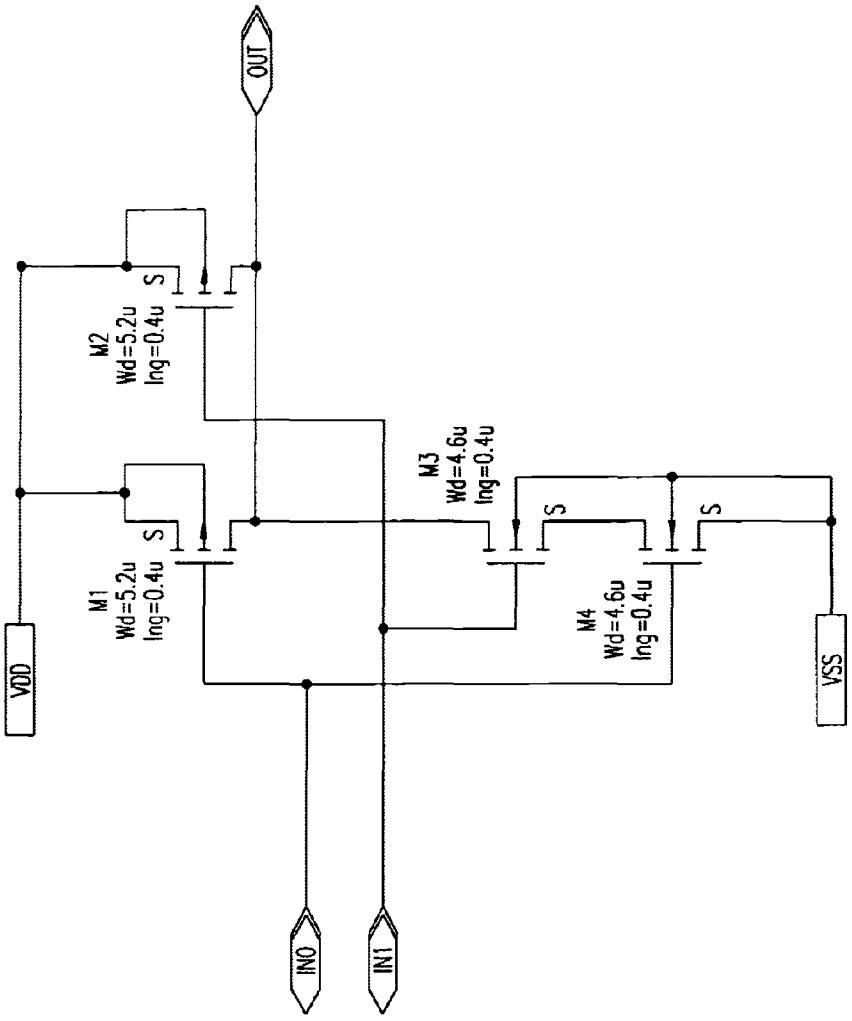

OUT
M2
Wd=5.2u
lng=0.4u
S
M3
Wd=4.6u
lng=0.4u
S
S
M1
Wd=5.2u
lng=0.4u
S
M4
Wd=4.6u
lng=0.4u
VDD
VSS
IN0
IN1

FIG.133

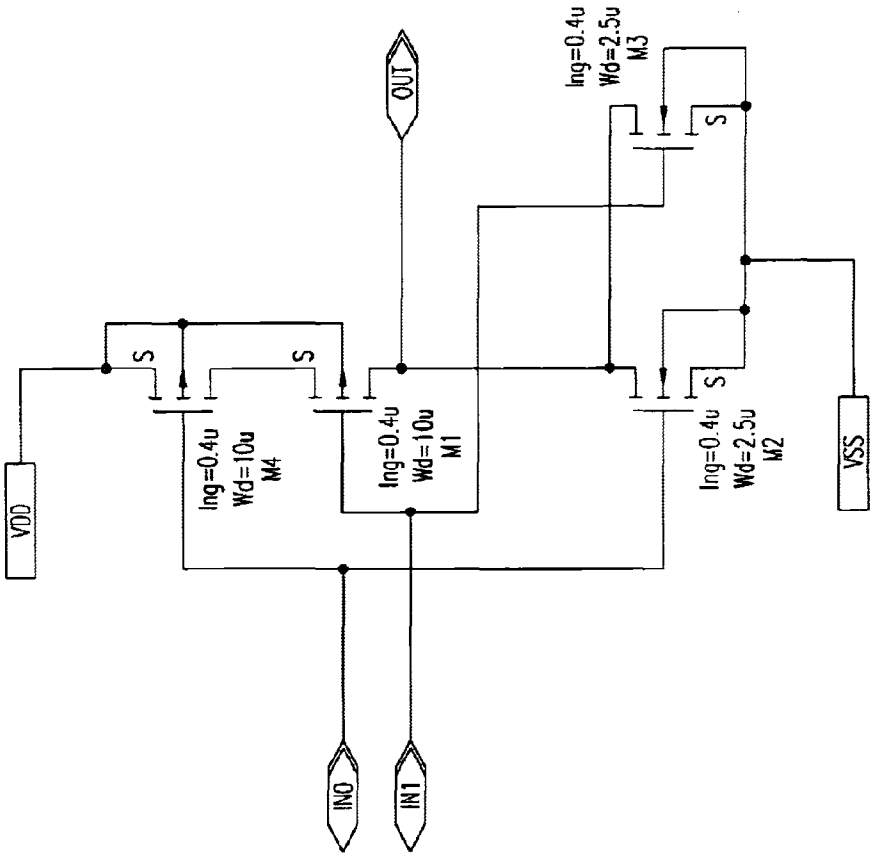

VDD
S
lng=0.4u
Wd=10u
M4
S
lng=0.4u
Wd=10u
M1
OUT
lng=0.4u
Wd=2.5u
M3
S
S
lng=0.4u
Wd=2.5u
M2
VSS
IN0
IN1

FIG. 134

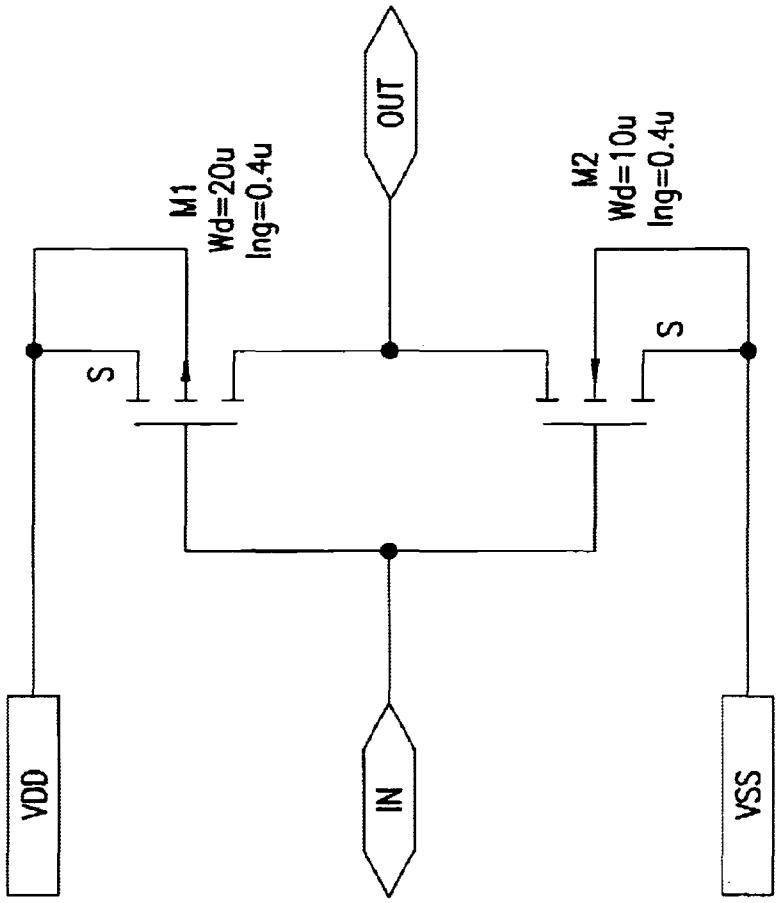


FIG.135

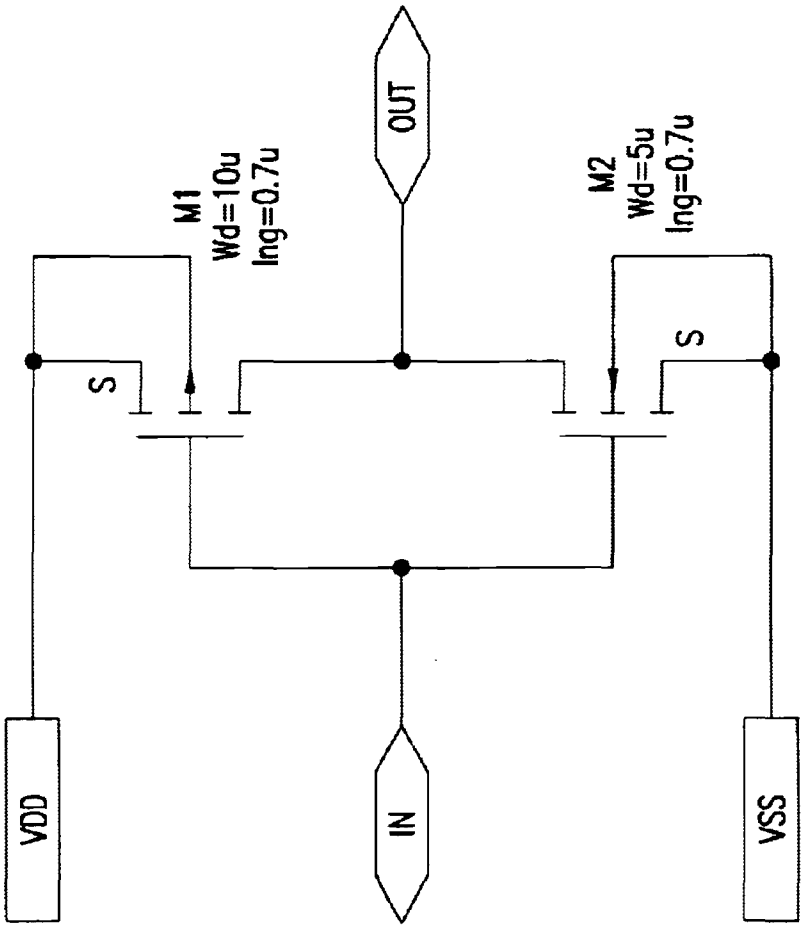


FIG.136

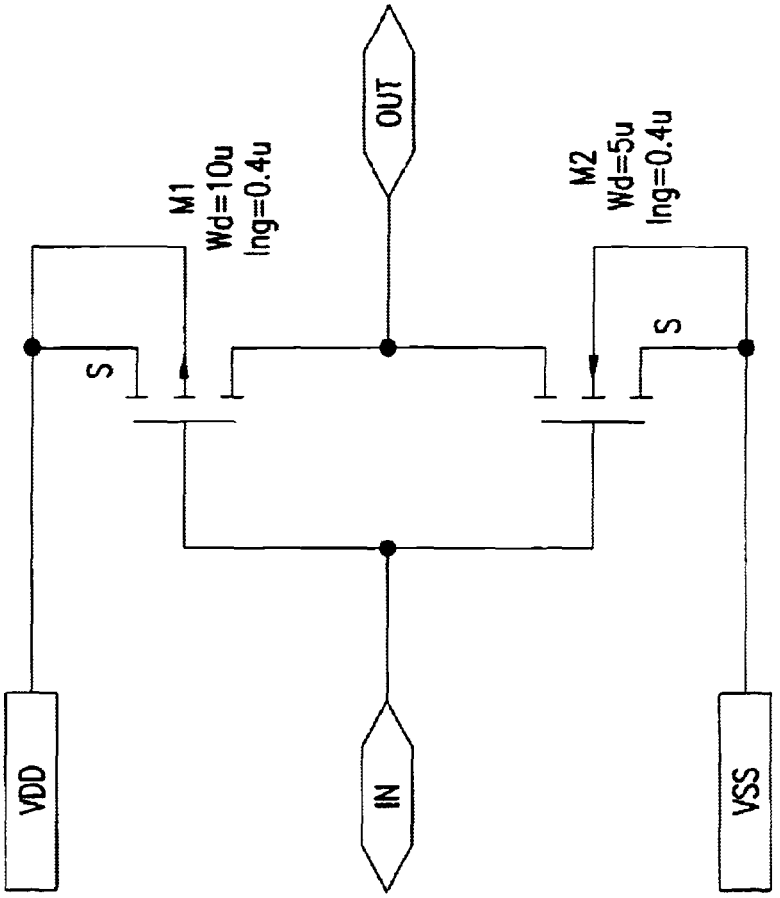


FIG. 137

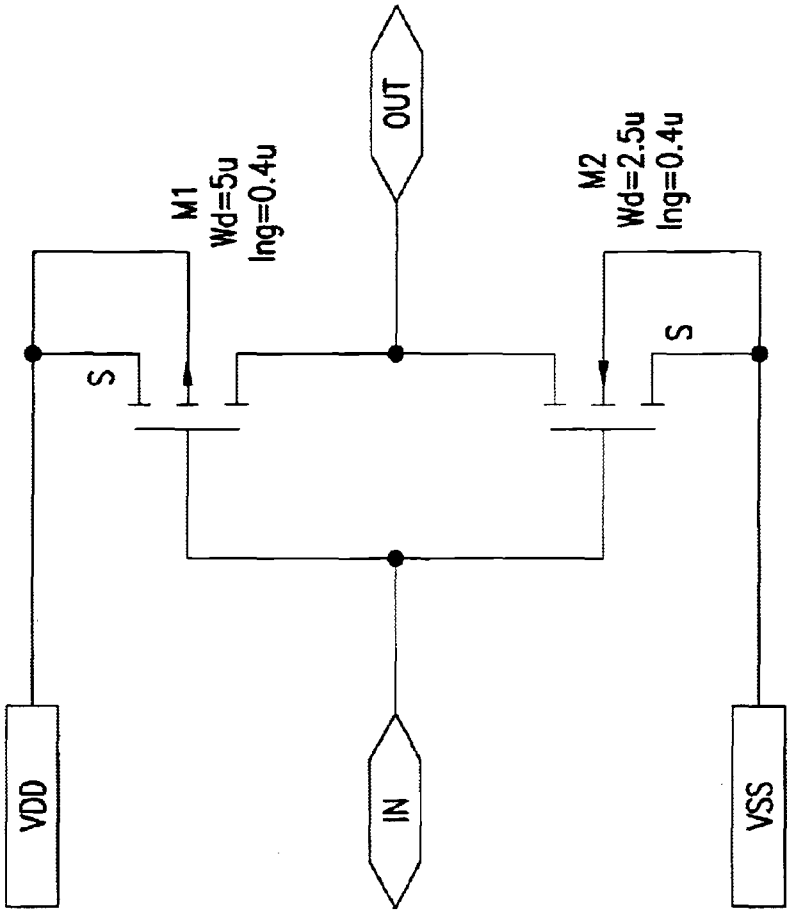


FIG.138

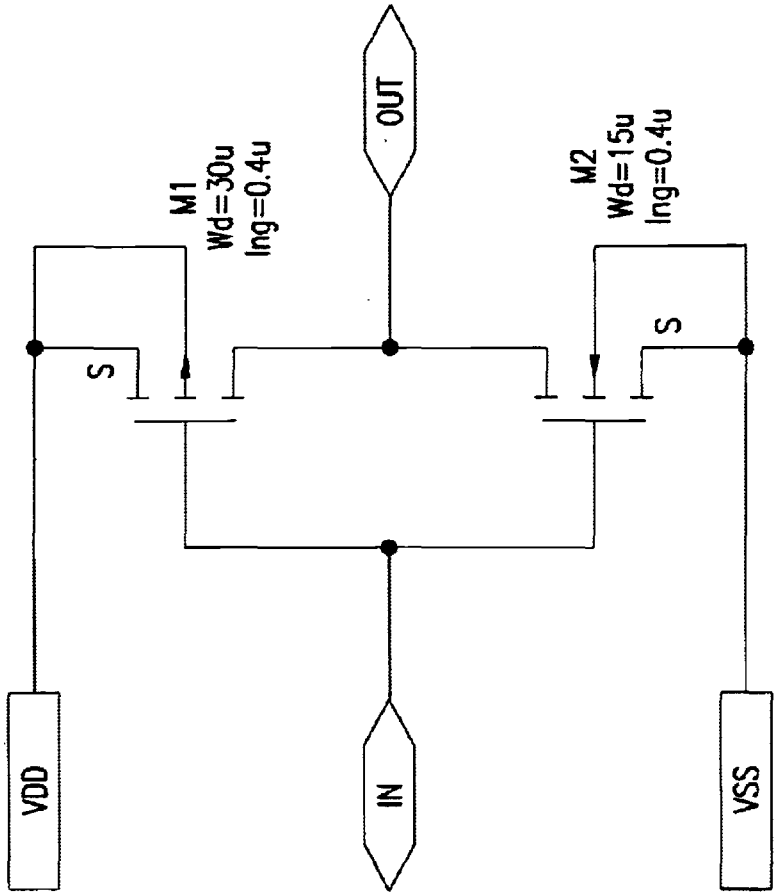


FIG.139

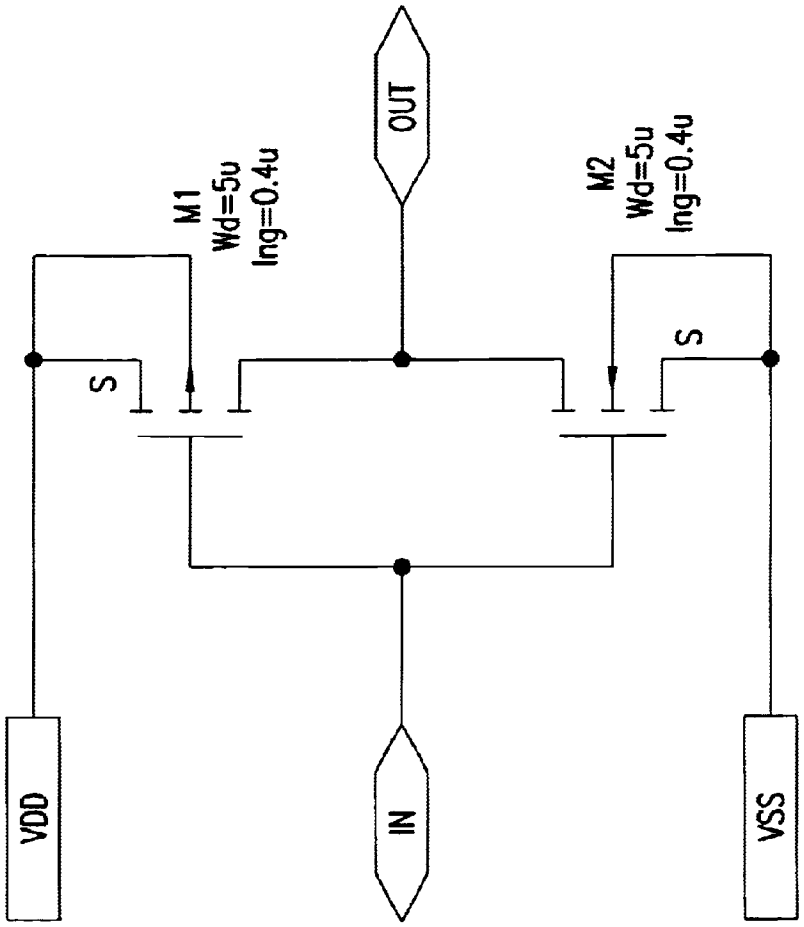


FIG.140

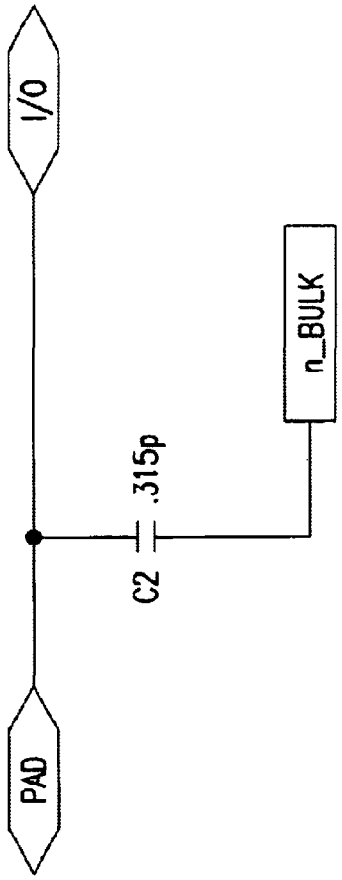


FIG. 141

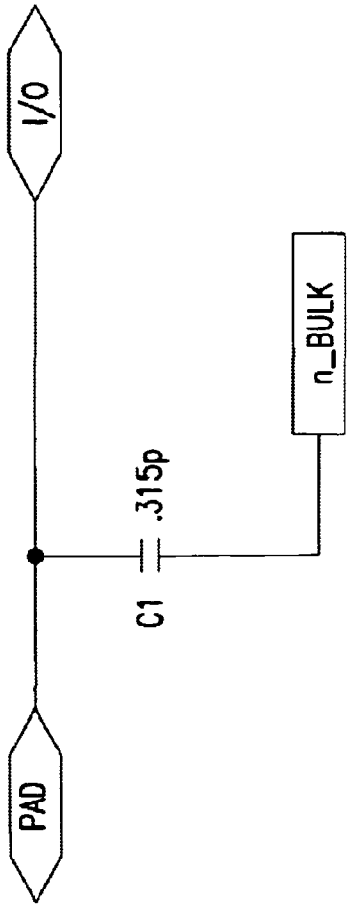


FIG.142

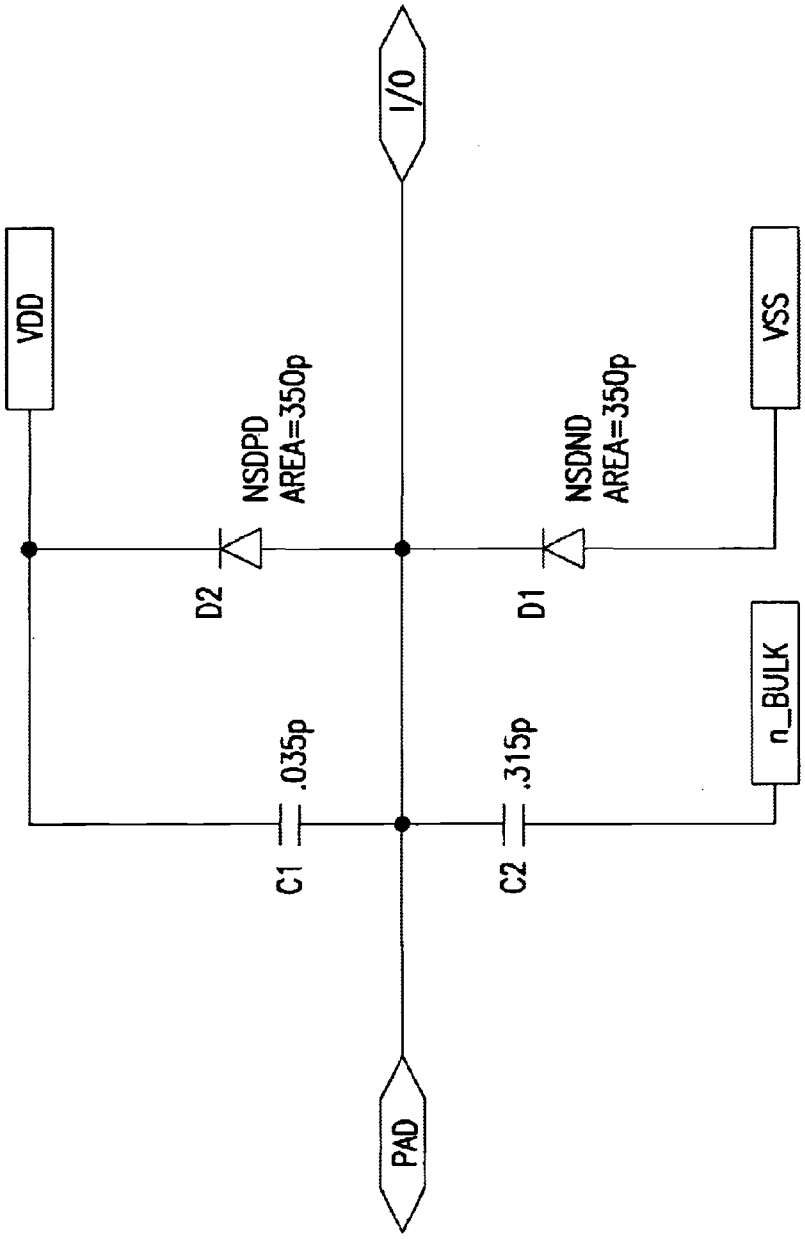

I/O
VDD
VSS
NSDPD
AREA=350p
NSDND
AREA=350p
D2
D1
n_BULK
.035p
.315p
C1
C2
PAD

FIG.143

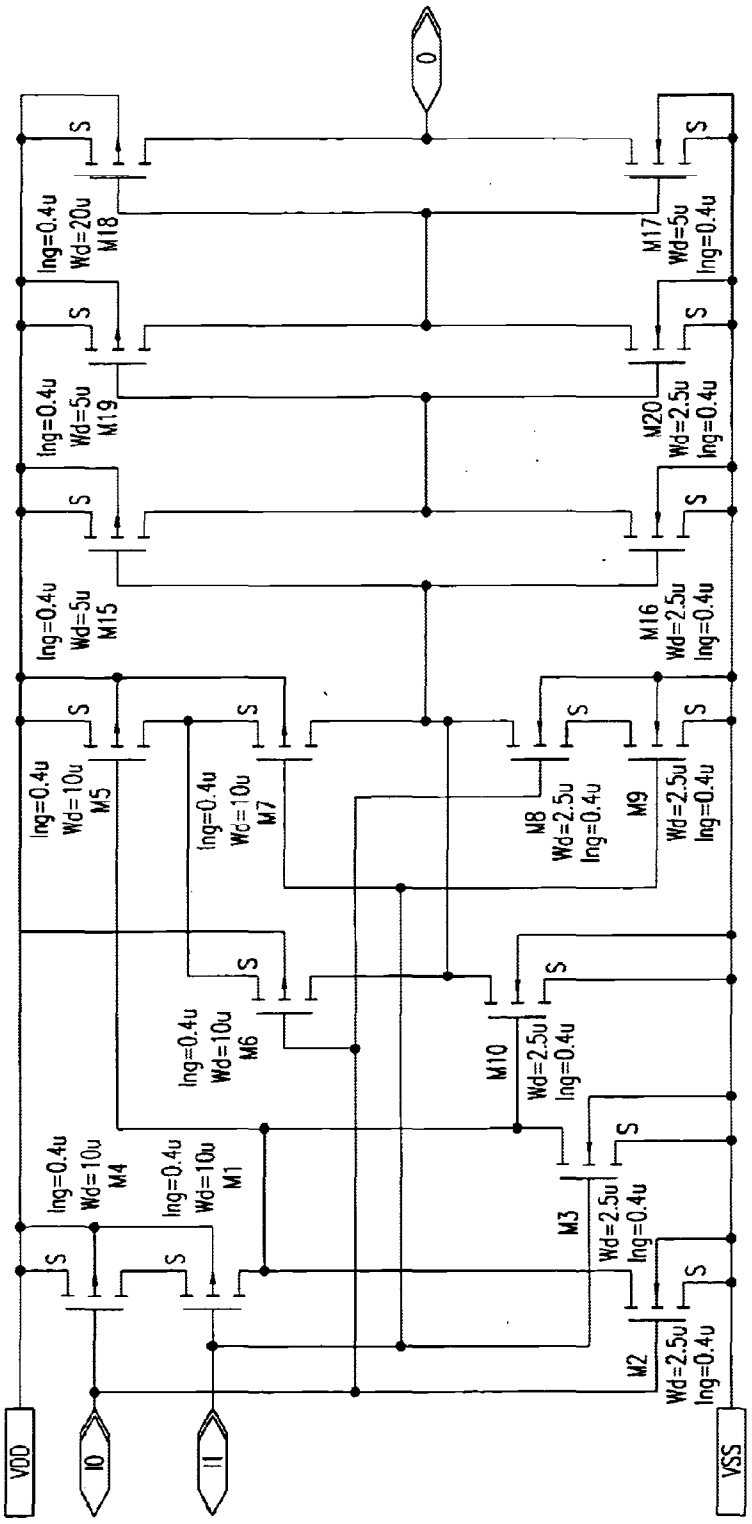

O
lng=0.4u Wd=20u M18
M17 Wd=5u lng=0.4u
lng=0.4u Wd=5u M19
M20 Wd=2.5u lng=0.4u
lng=0.4u Wd=5u M15
M16 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M5
lng=0.4u Wd=10u M7
M8 Wd=2.5u lng=0.4u
M9 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M6
M10 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M4
lng=0.4u Wd=10u M1
M3 Wd=2.5u lng=0.4u
M2 Wd=2.5u lng=0.4u
VDD
I0
I1
VSS

FIG. 144

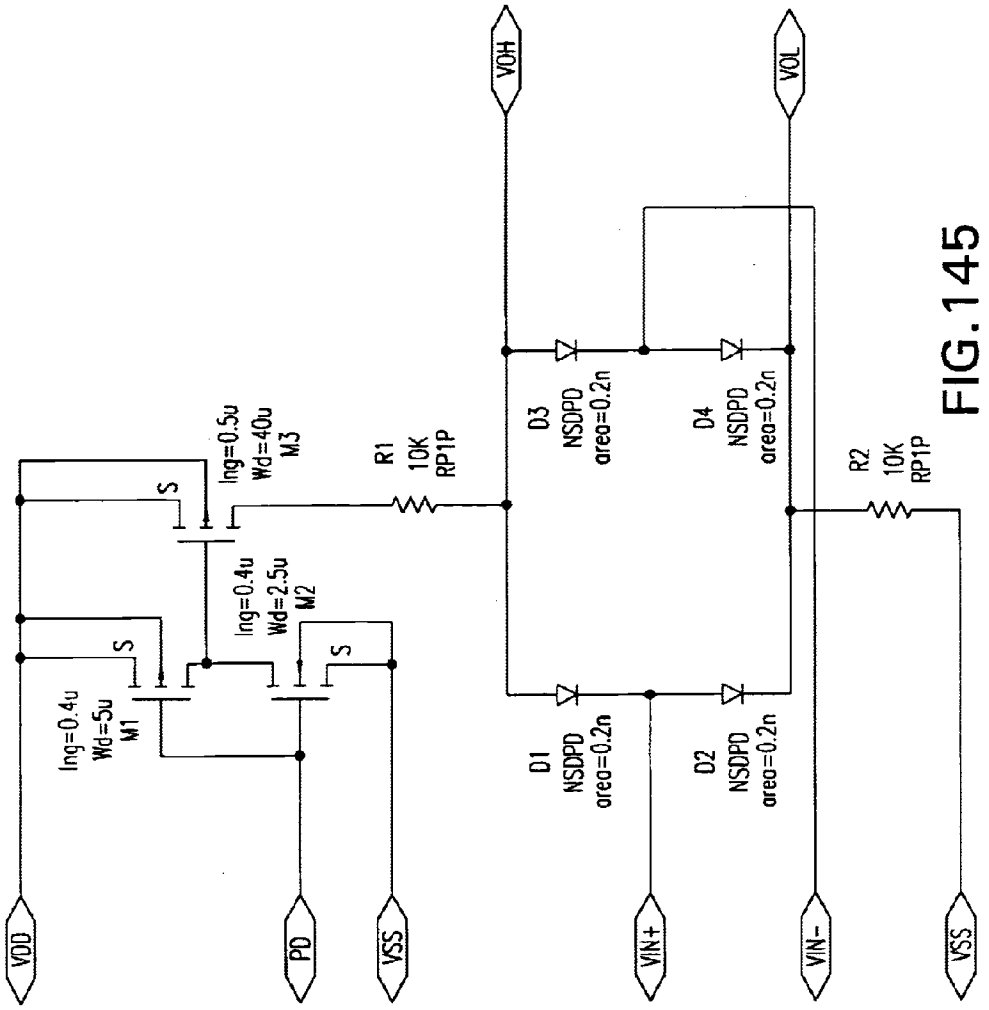

VOH
VOL
R1
10K
RP1P
R2
10K
RP1P
D3
NSDPD
area=0.2n
D4
NSDPD
area=0.2n
D1
NSDPD
area=0.2n
D2
NSDPD
area=0.2n
lng=0.5u
Wd=40u
M3
lng=0.4u
Wd=2.5u
M2
lng=0.4u
Wd=5u
M1
S
VDD
PD
VSS
VIN+
VIN-
VSS

FIG. 145

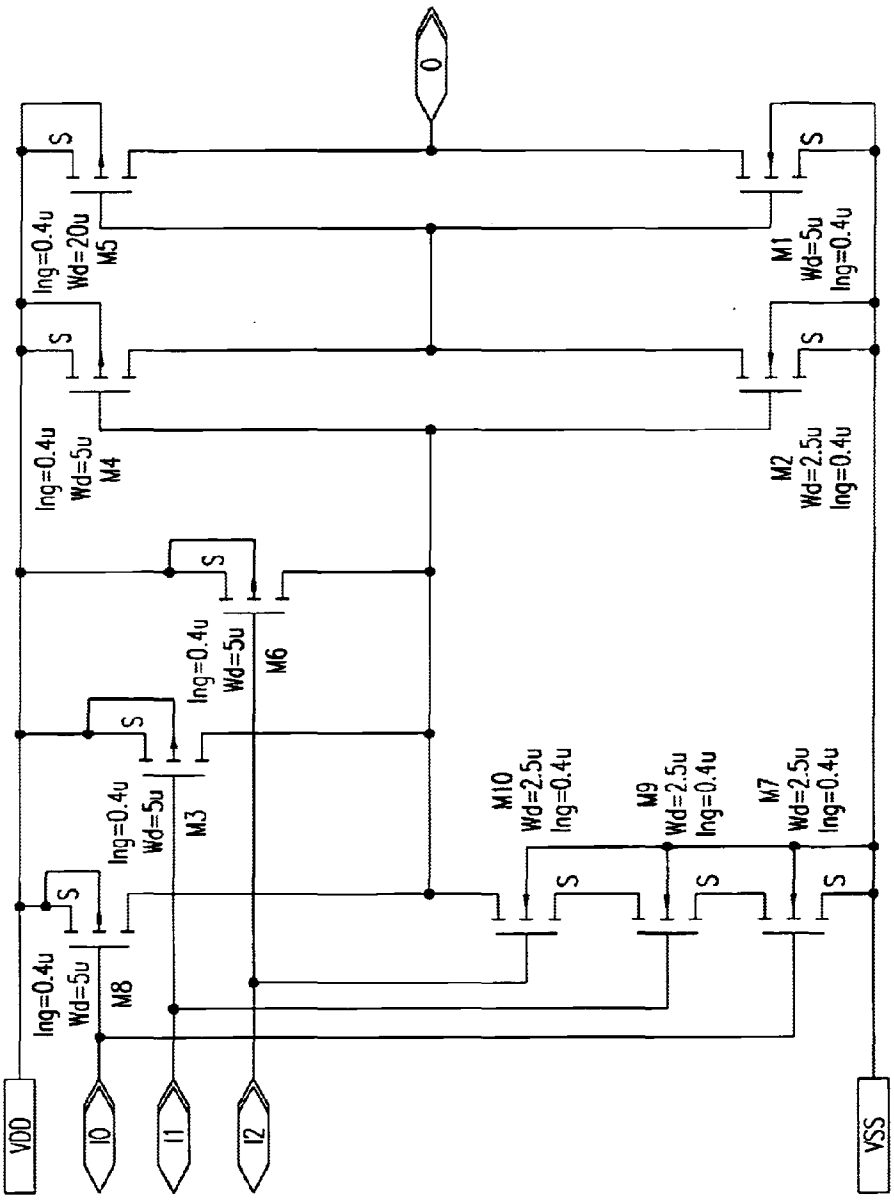

0
S
lng=0.4u
Wd=20u
M5
M1
Wd=5u
lng=0.4u
M4
M2
Wd=2.5u
M6
M3
M10
M9
M7
M8
VDD
I0
I1
I2
VSS

FIG.146

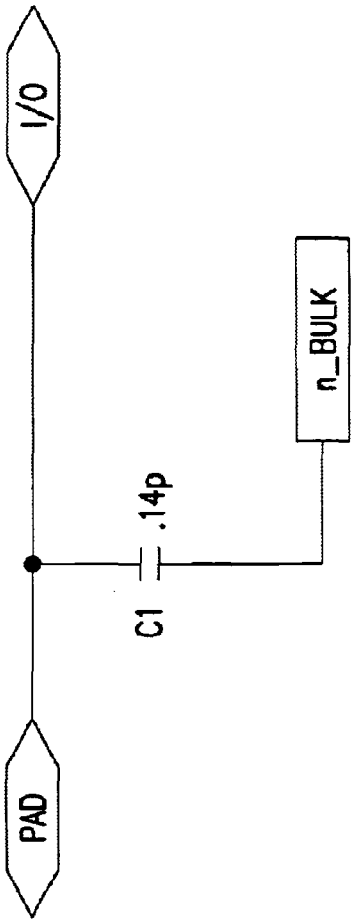


FIG. 147

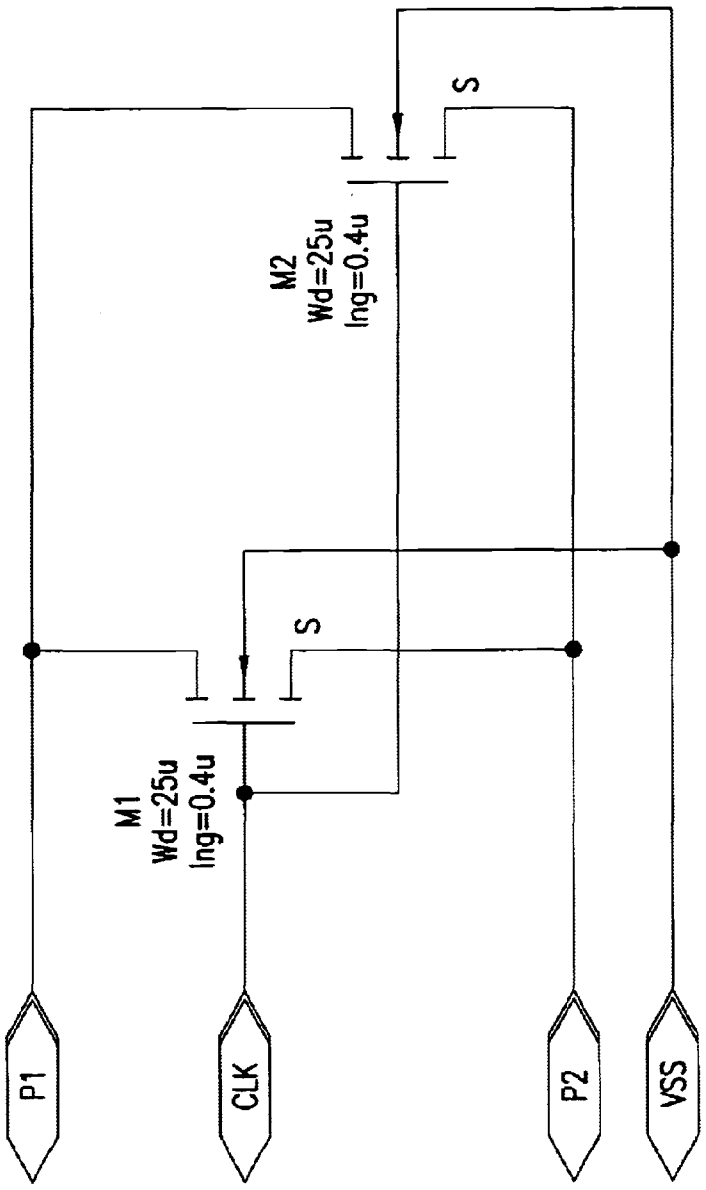


FIG.148

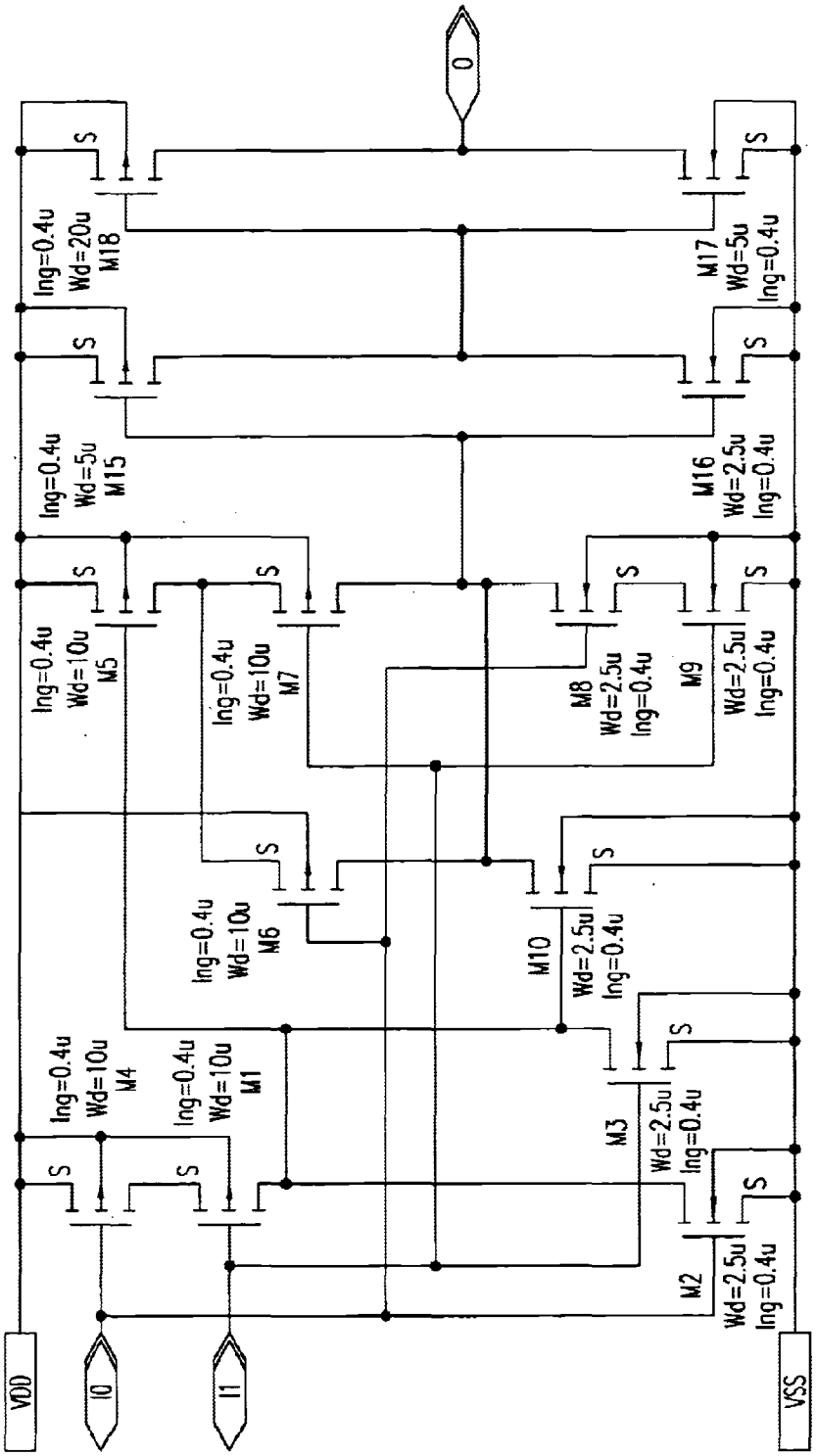

O
lng=0.4u Wd=20u M18
M17 Wd=5u lng=0.4u
lng=0.4u Wd=5u M15
M16 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M5
lng=0.4u Wd=10u M7
M8 Wd=2.5u lng=0.4u
M9 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M6
M10 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M4
lng=0.4u Wd=10u M1
M3 Wd=2.5u lng=0.4u
M2 Wd=2.5u lng=0.4u
VDD
I0
I1
VSS

FIG.149

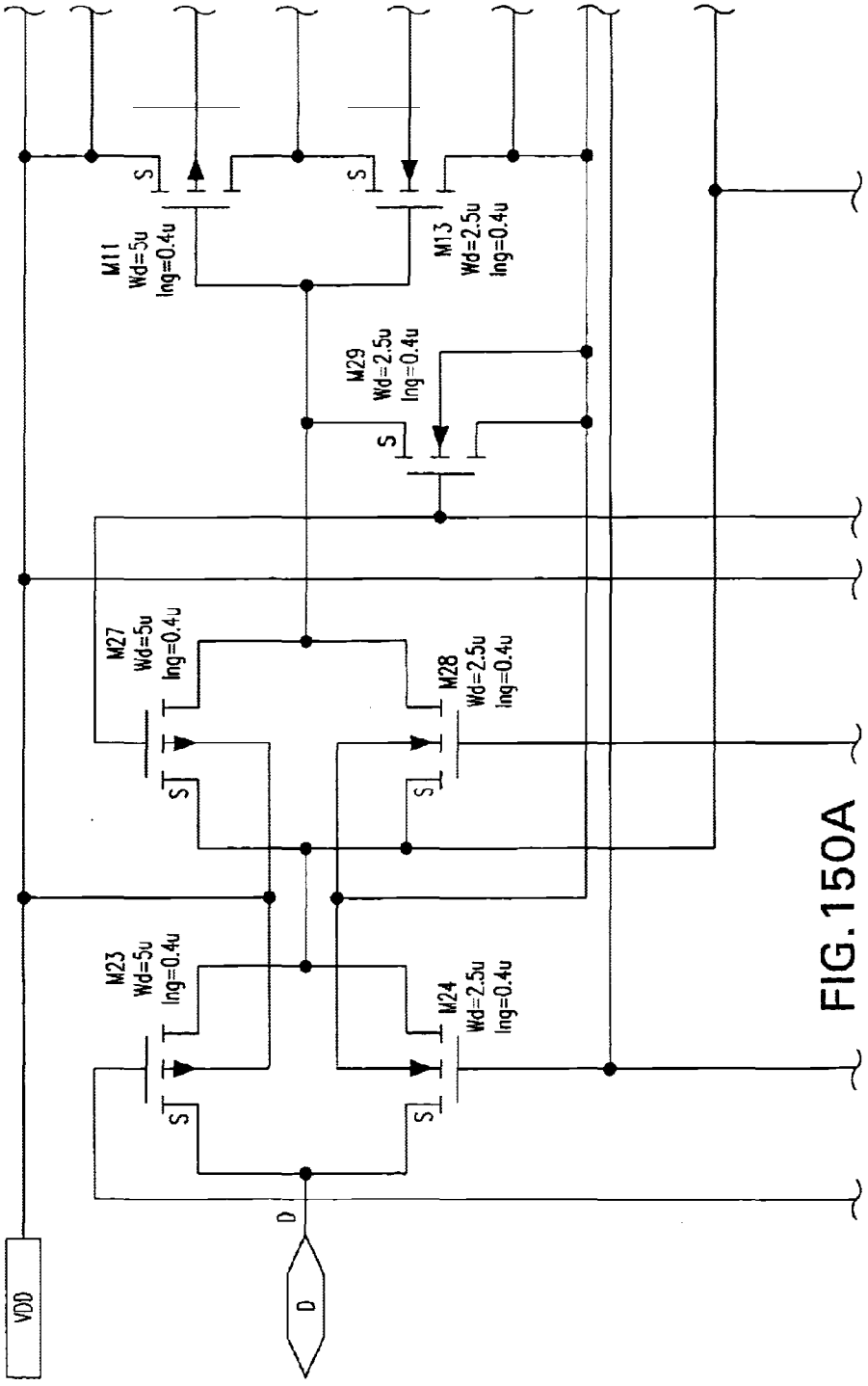

M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M29
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M28
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG. 150A

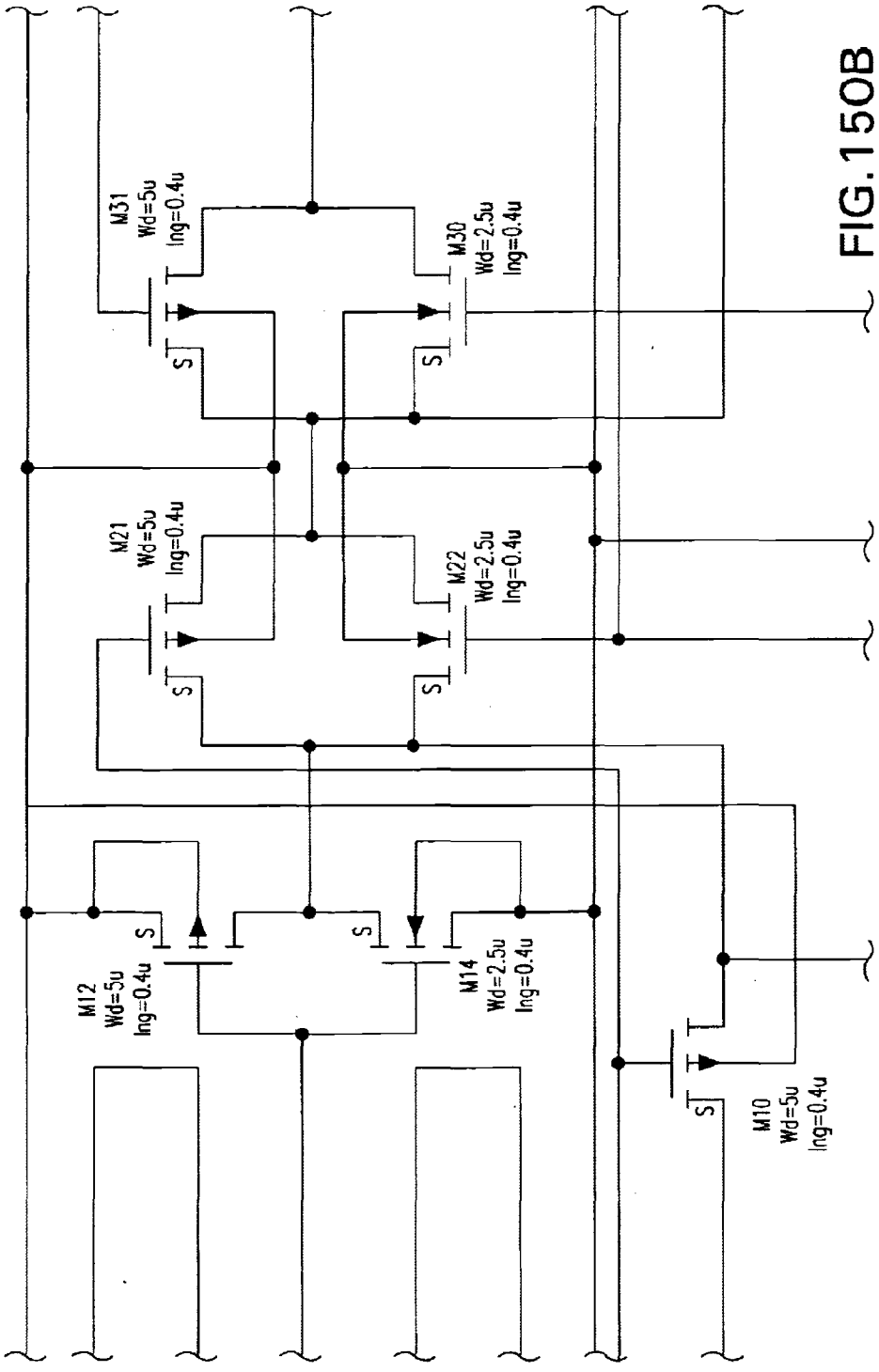

M31
Wd=5u
lng=0.4u
M30
Wd=2.5u
lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
S

FIG. 150B

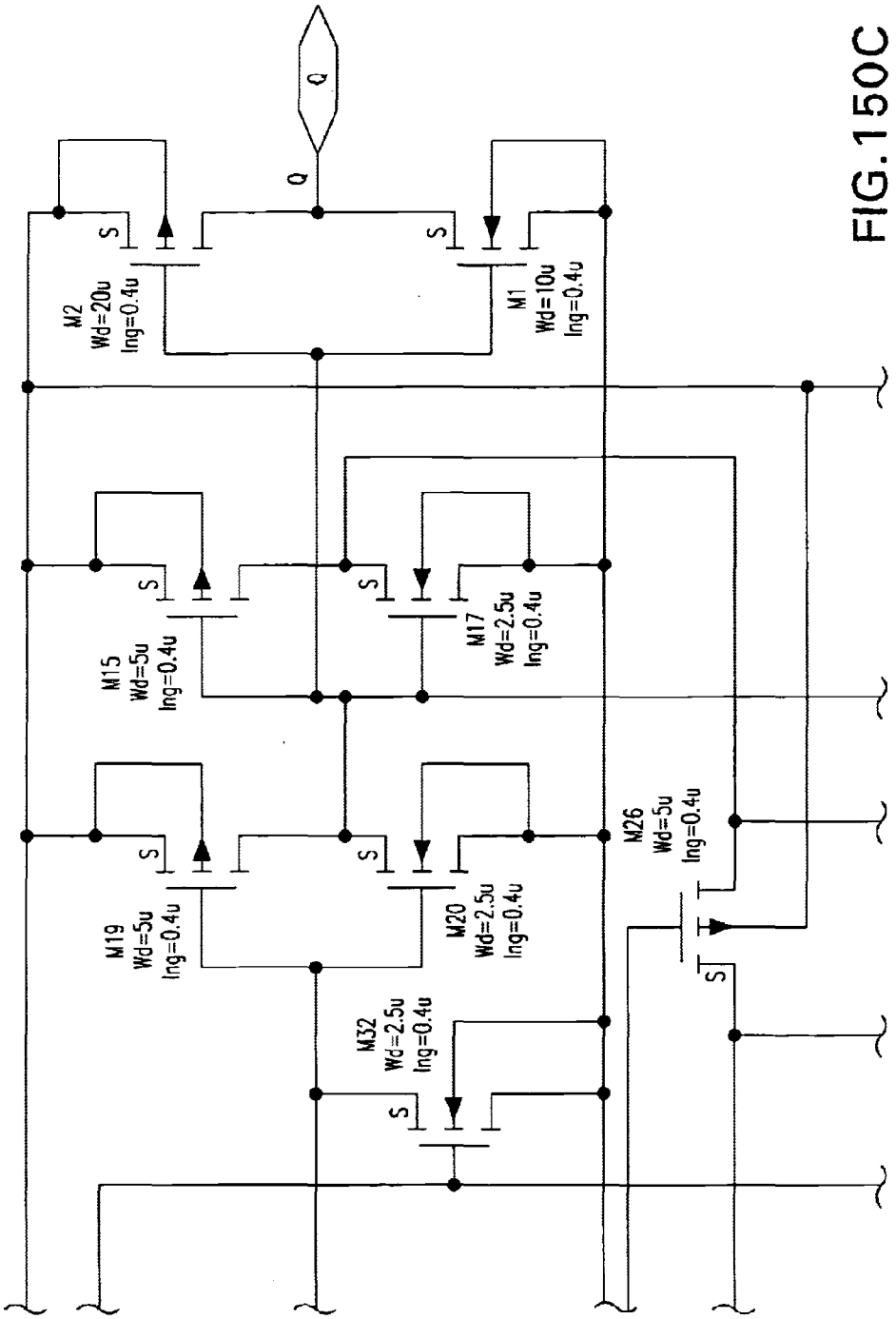

Q
Q
S
S
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
S
S
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
S
S
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
S
M32
Wd=2.5u
lng=0.4u
S

FIG. 150C

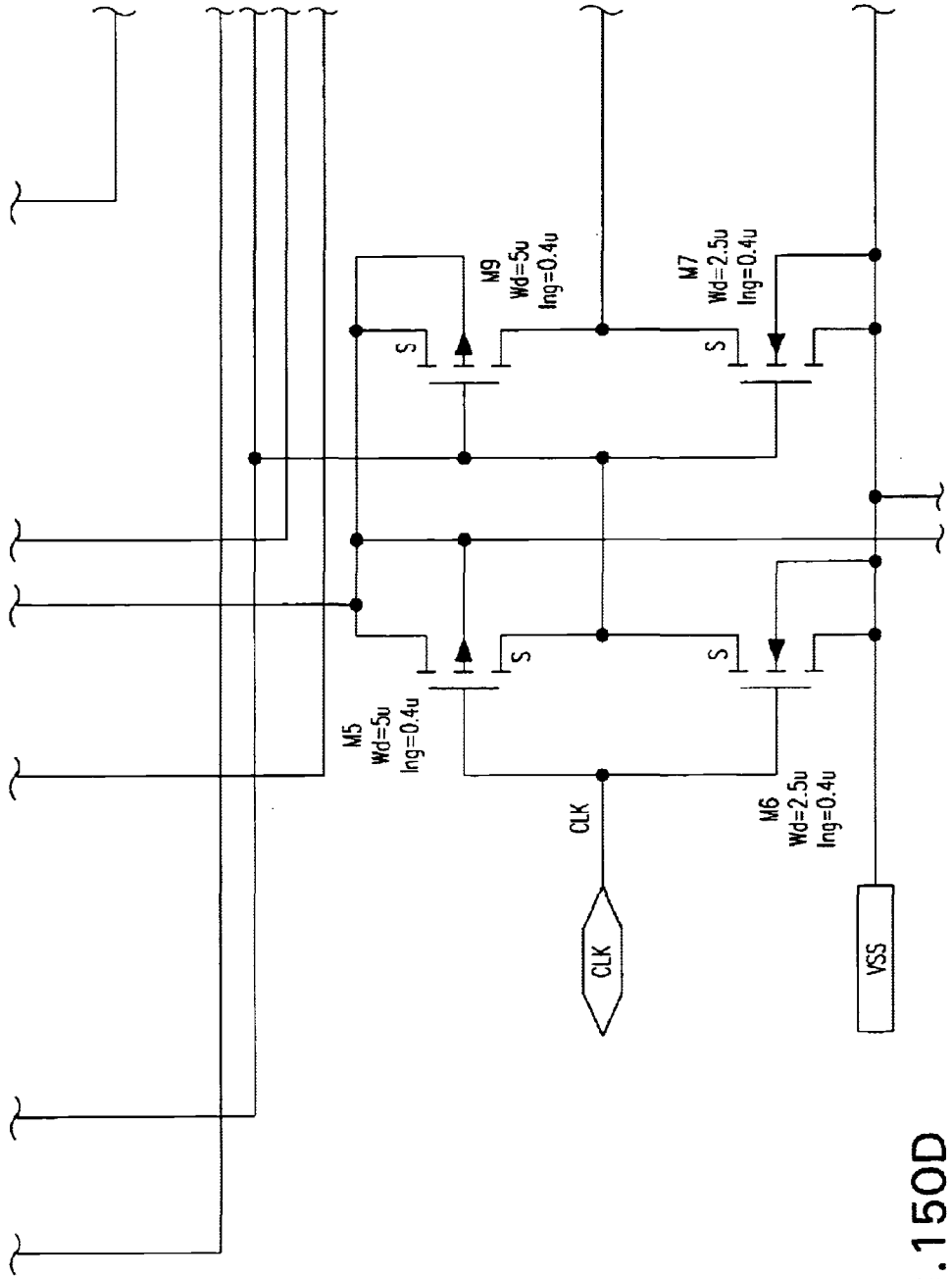

M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
S
S
S
S
M5
Wd=5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
CLK
CLK
VSS

FIG. 150D

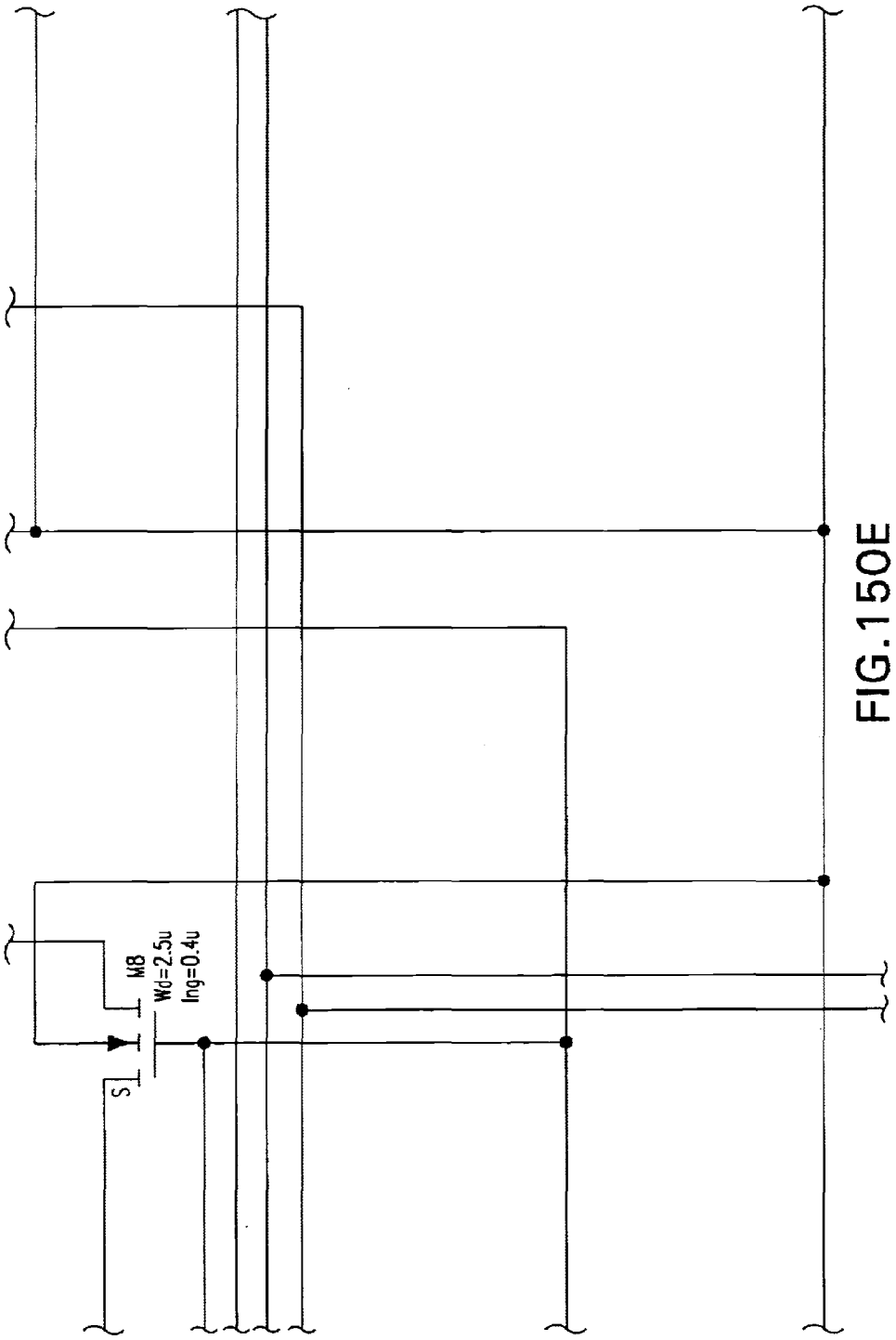


FIG.150E

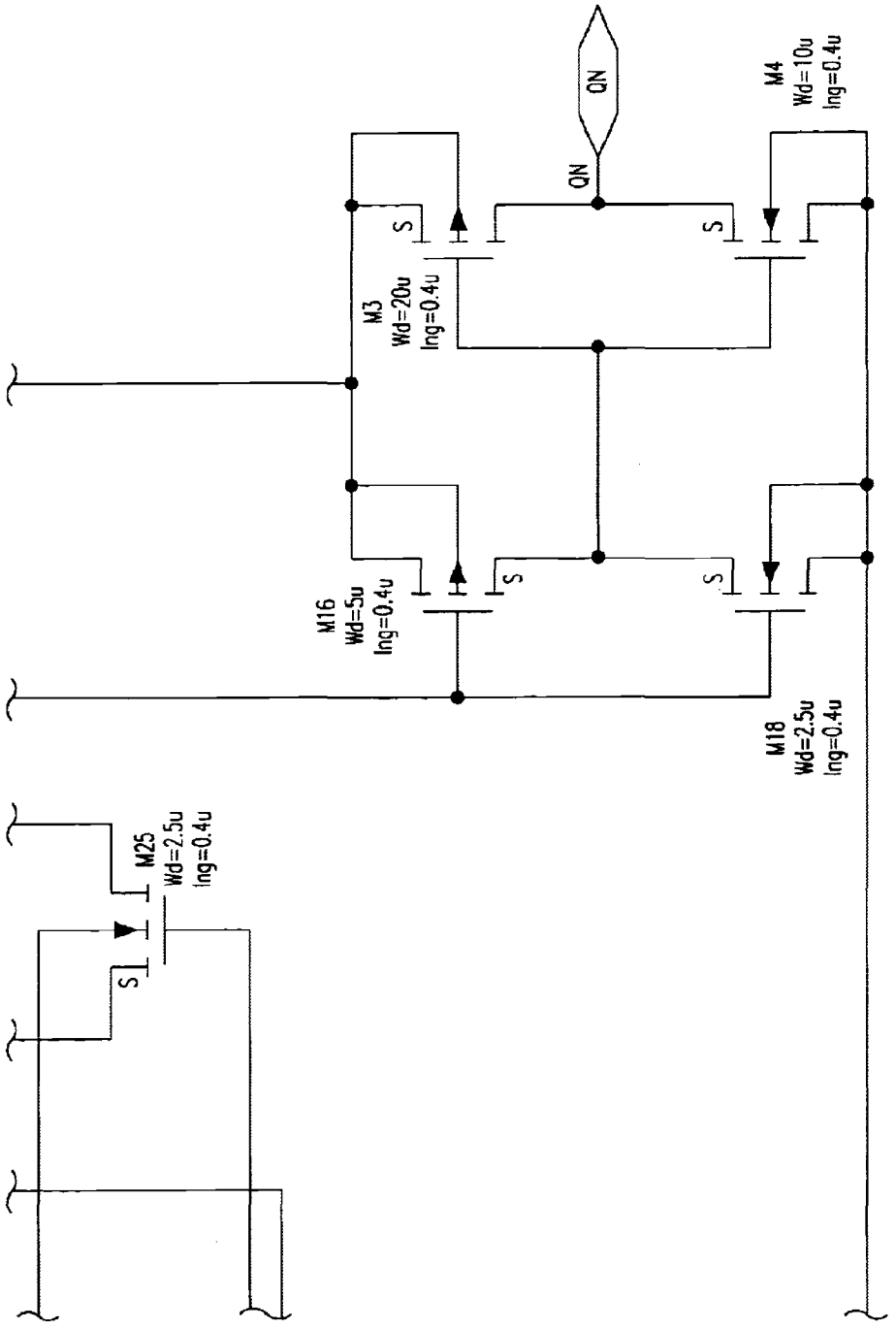

QN
QN
M4
Wd=10u
lng=0.4u
M3
Wd=20u
lng=0.4u
M16
Wd=5u
lng=0.4u
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S
S
S
S
S

FIG.150F

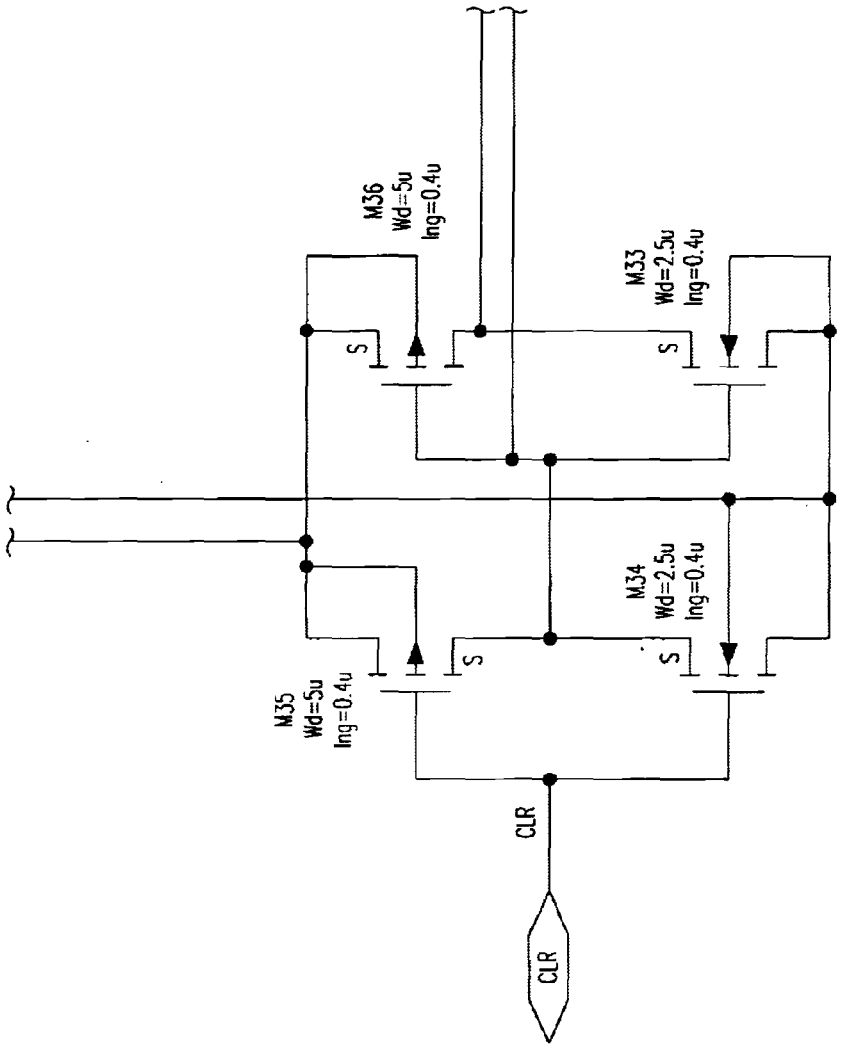
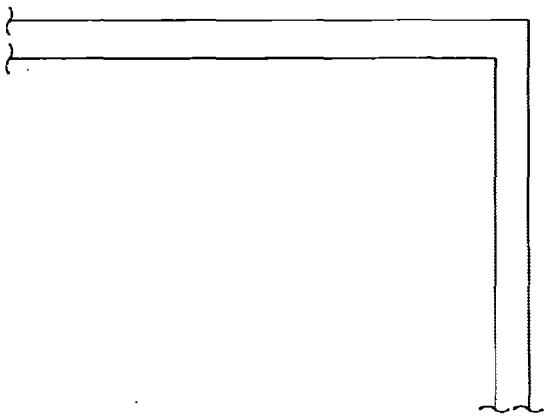

M36
Wd=5u
lng=0.4u
M33
Wd=2.5u
lng=0.4u
S
S
M34
Wd=2.5u
lng=0.4u
S
S
M35
Wd=5u
lng=0.4u
CLR
CLR

FIG. 150G

FIG. 150H



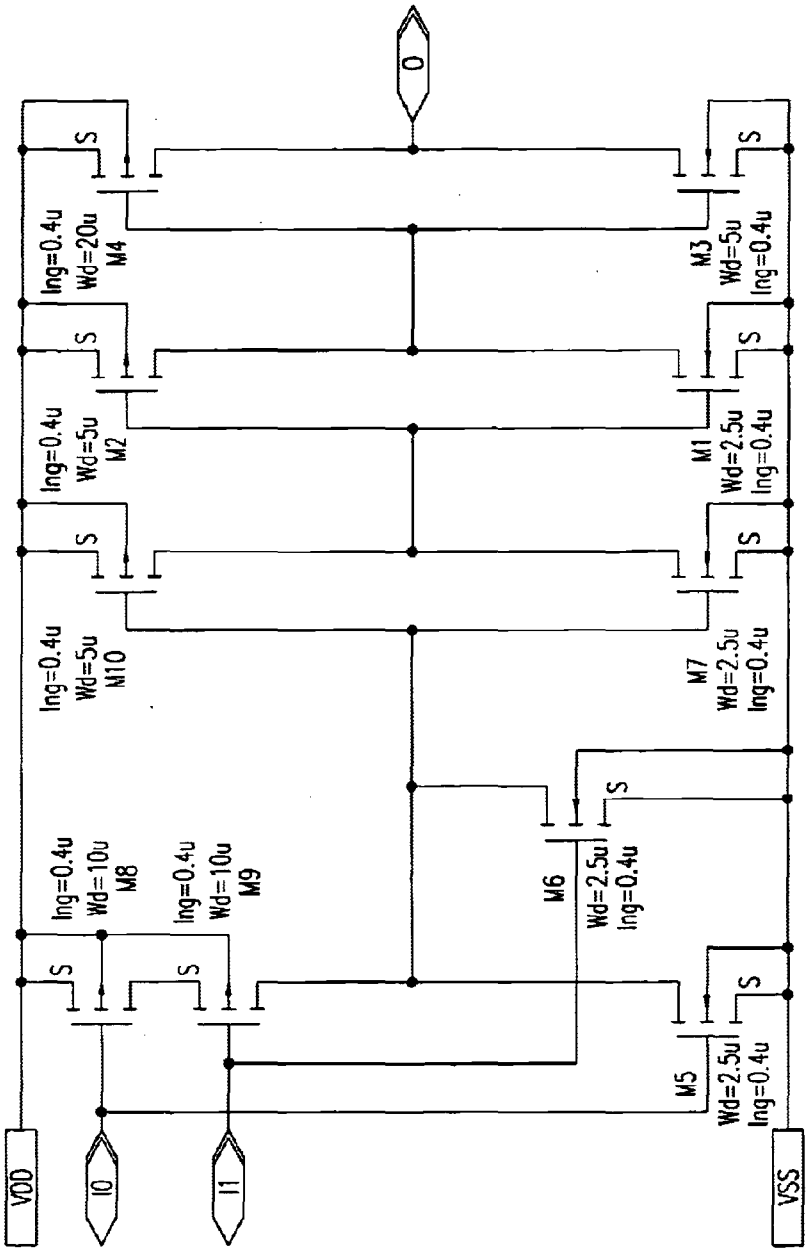

O
S
lng=0.4u
Wd=20u
M4
M3
Wd=5u
lng=0.4u
lng=0.4u
Wd=5u
M2
M1
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M10
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=10u
M8
lng=0.4u
Wd=10u
M9
M5
Wd=2.5u
lng=0.4u
VDD
I0
I1
VSS

FIG.151

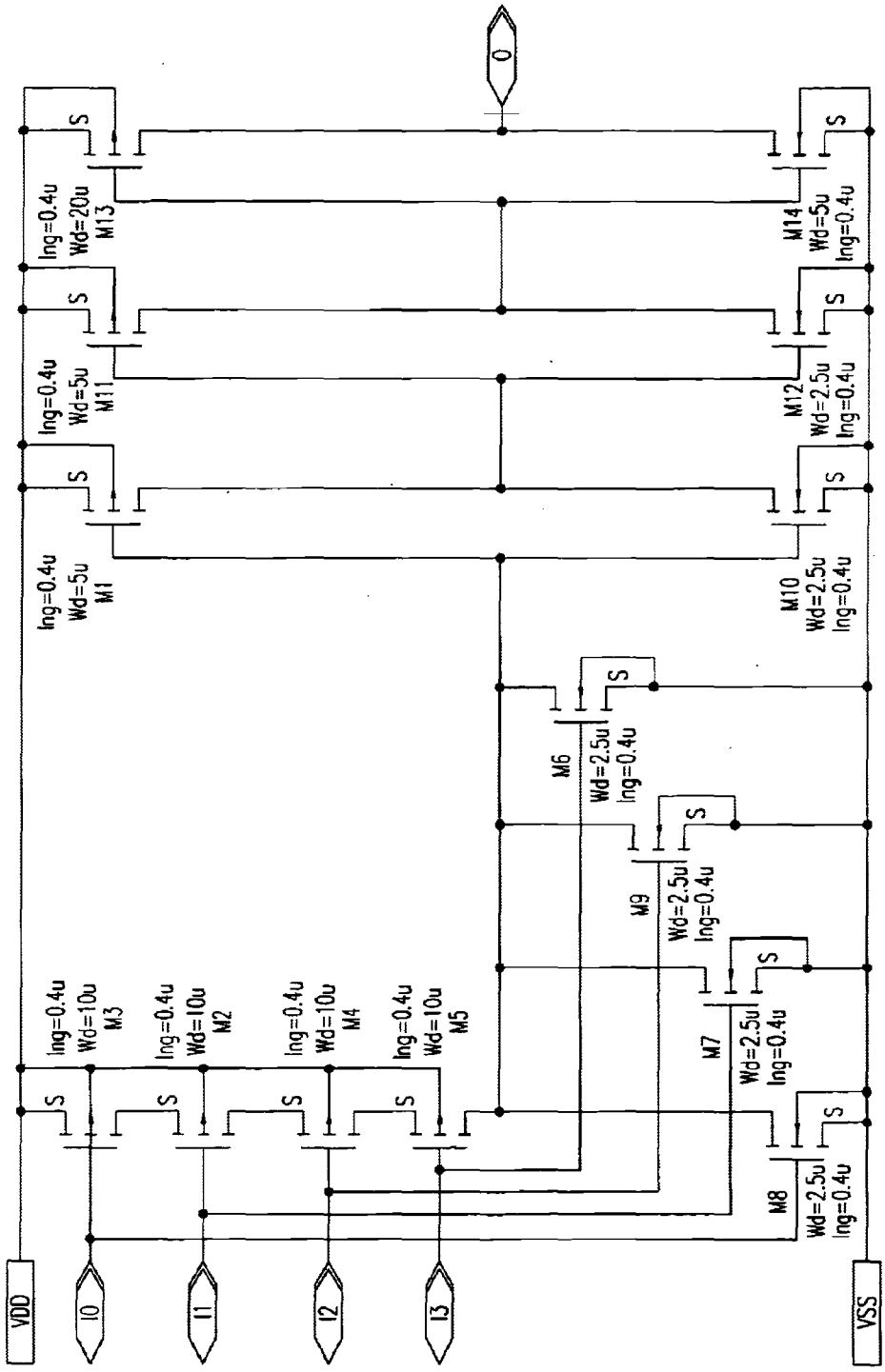

O
S
lng=0.4u
Wd=20u
M13
M14
Wd=5u
lng=0.4u
lng=0.4u
Wd=5u
M11
M12
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M1
M10
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M9
Wd=2.5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M8
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=10u
M3
lng=0.4u
Wd=10u
M2
lng=0.4u
Wd=10u
M4
lng=0.4u
Wd=10u
M5
VDD
I0
I1
I2
I3
VSS

FIG.152

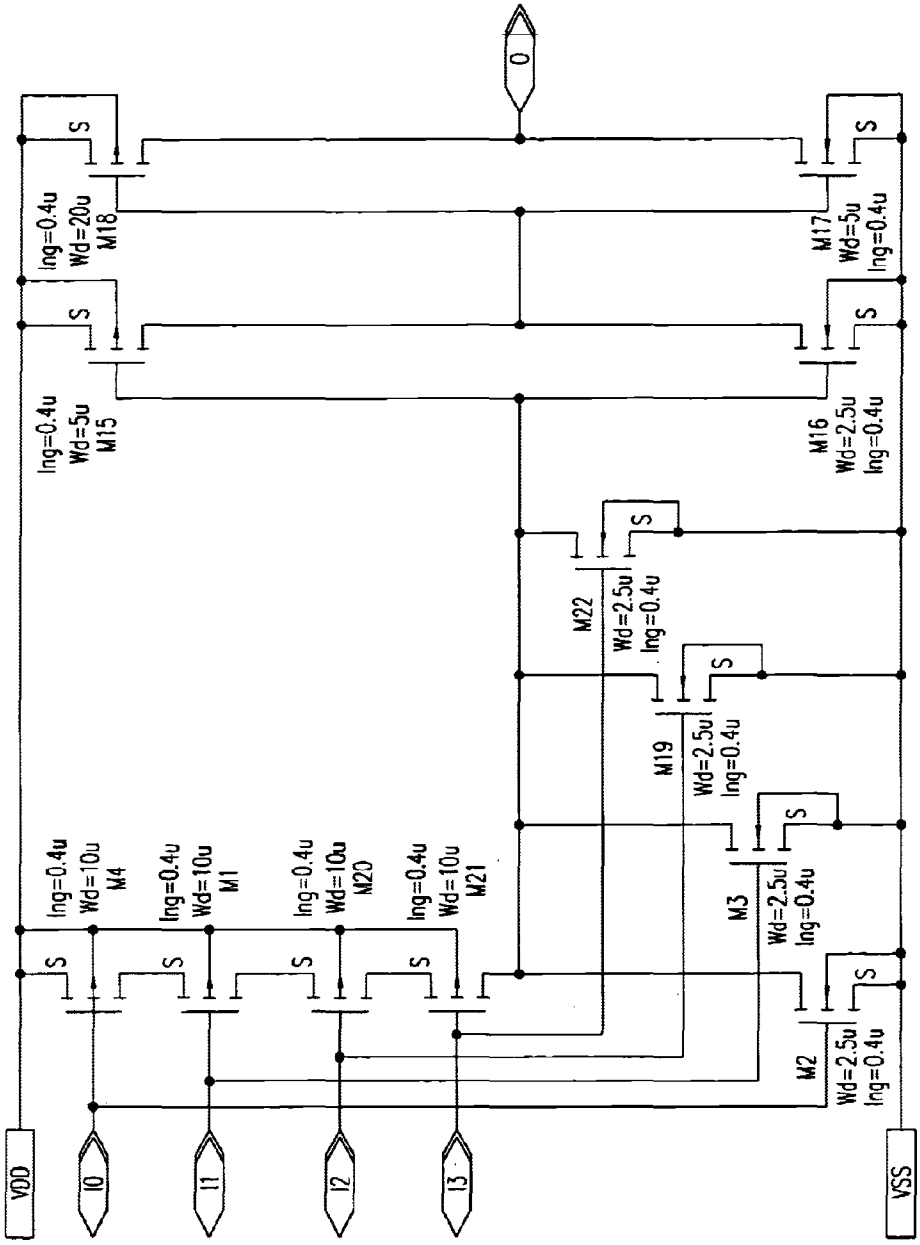

O
M18 lng=0.4u Wd=20u
M17 Wd=5u lng=0.4u
M15 lng=0.4u Wd=5u
M16 Wd=2.5u lng=0.4u
M22 Wd=2.5u lng=0.4u
M19 Wd=2.5u lng=0.4u
M3 Wd=2.5u lng=0.4u
M2 Wd=2.5u lng=0.4u
M4 lng=0.4u Wd=10u
M1 lng=0.4u Wd=10u
M20 lng=0.4u Wd=10u
M21 lng=0.4u Wd=10u
S
VDD
I0
I1
I2
I3
VSS

FIG. 153

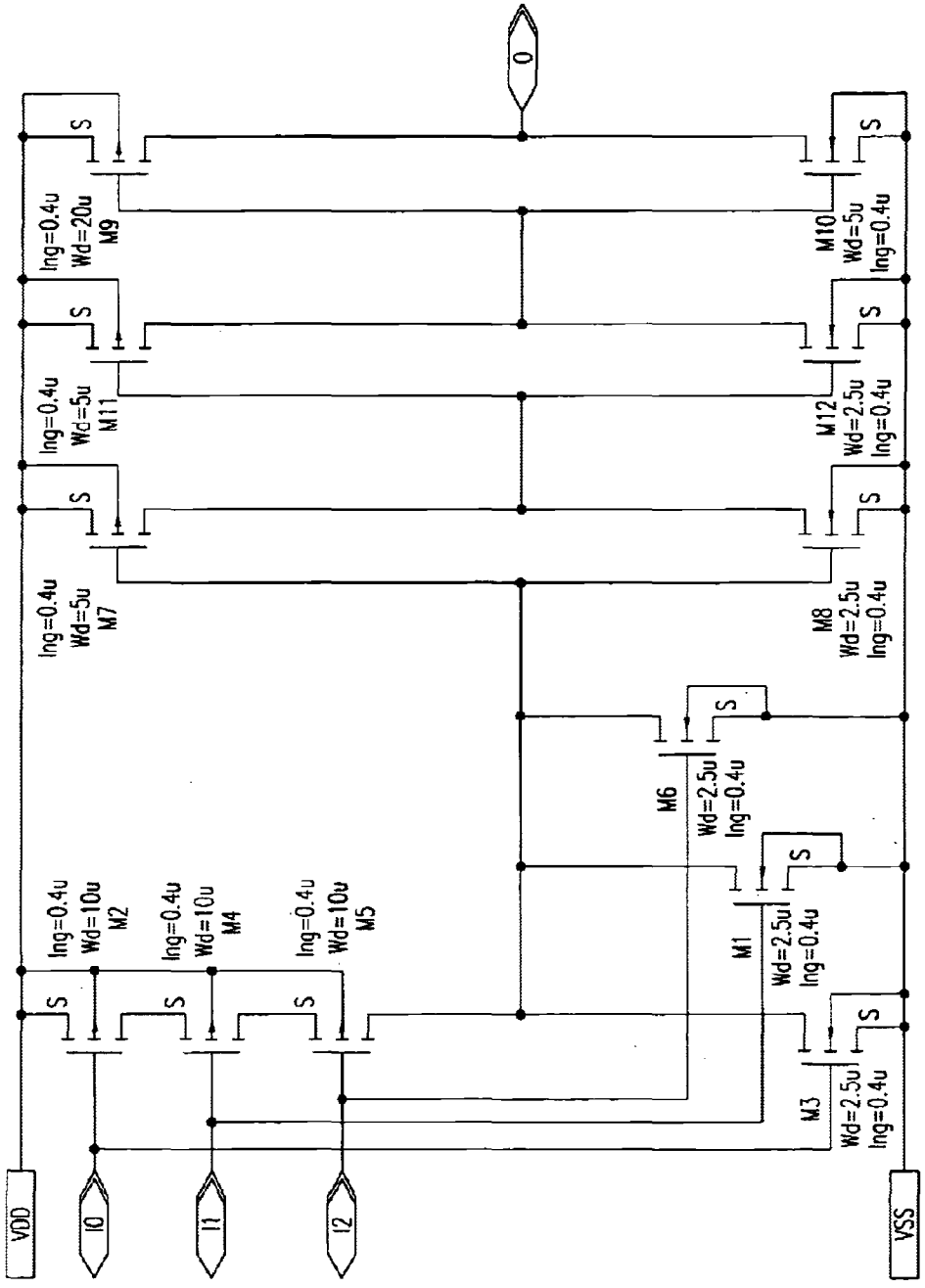

O
M9 lng=0.4u Wd=20u
M10 Wd=5u lng=0.4u
M11 lng=0.4u Wd=5u
M12 Wd=2.5u lng=0.4u
M7 lng=0.4u Wd=5u
M8 Wd=2.5u lng=0.4u
M6 Wd=2.5u lng=0.4u
M1 Wd=2.5u lng=0.4u
M3 Wd=2.5u lng=0.4u
M2 lng=0.4u Wd=10u
M4 lng=0.4u Wd=10u
M5 lng=0.4u Wd=10u
S
VDD
I0
I1
I2
VSS

FIG.154

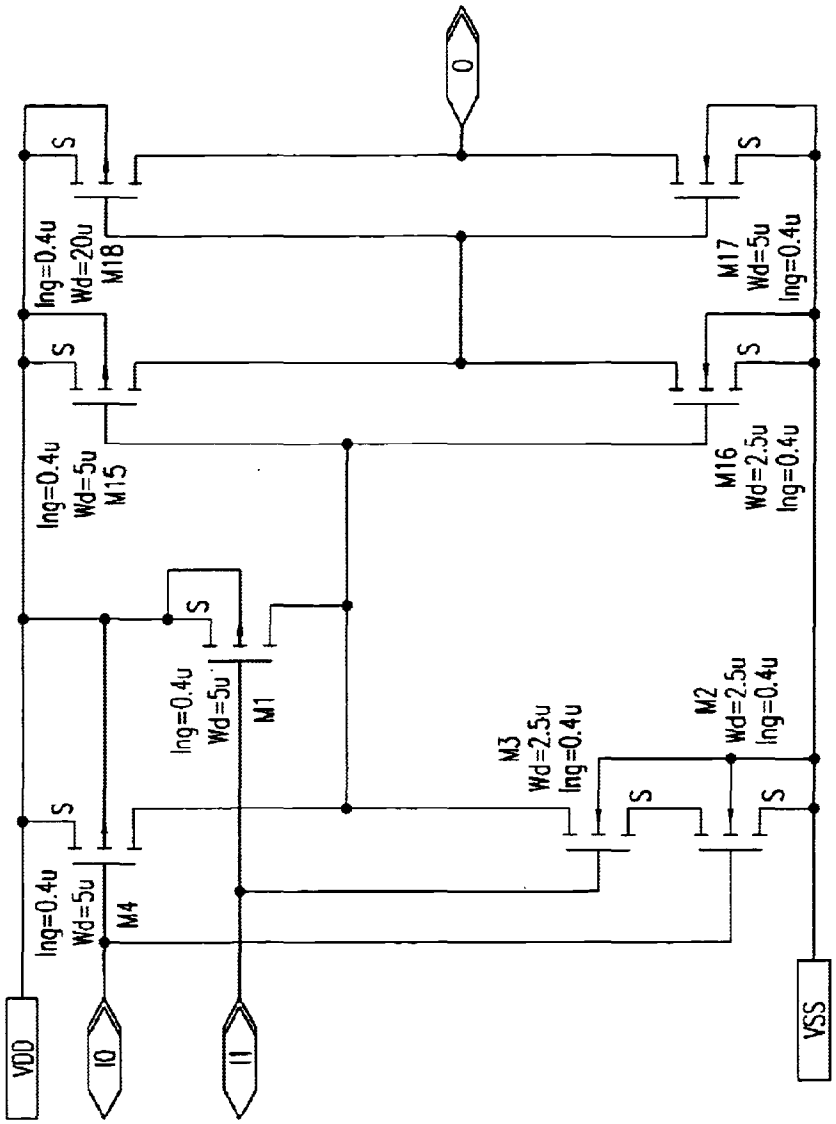

O
S
lng=0.4u
Wd=20u
M18
M17
Wd=5u
lng=0.4u
M15
Wd=5u
M16
Wd=2.5u
M1
M3
Wd=2.5u
M2
M4
VDD
I0
I1
VSS

FIG. 155

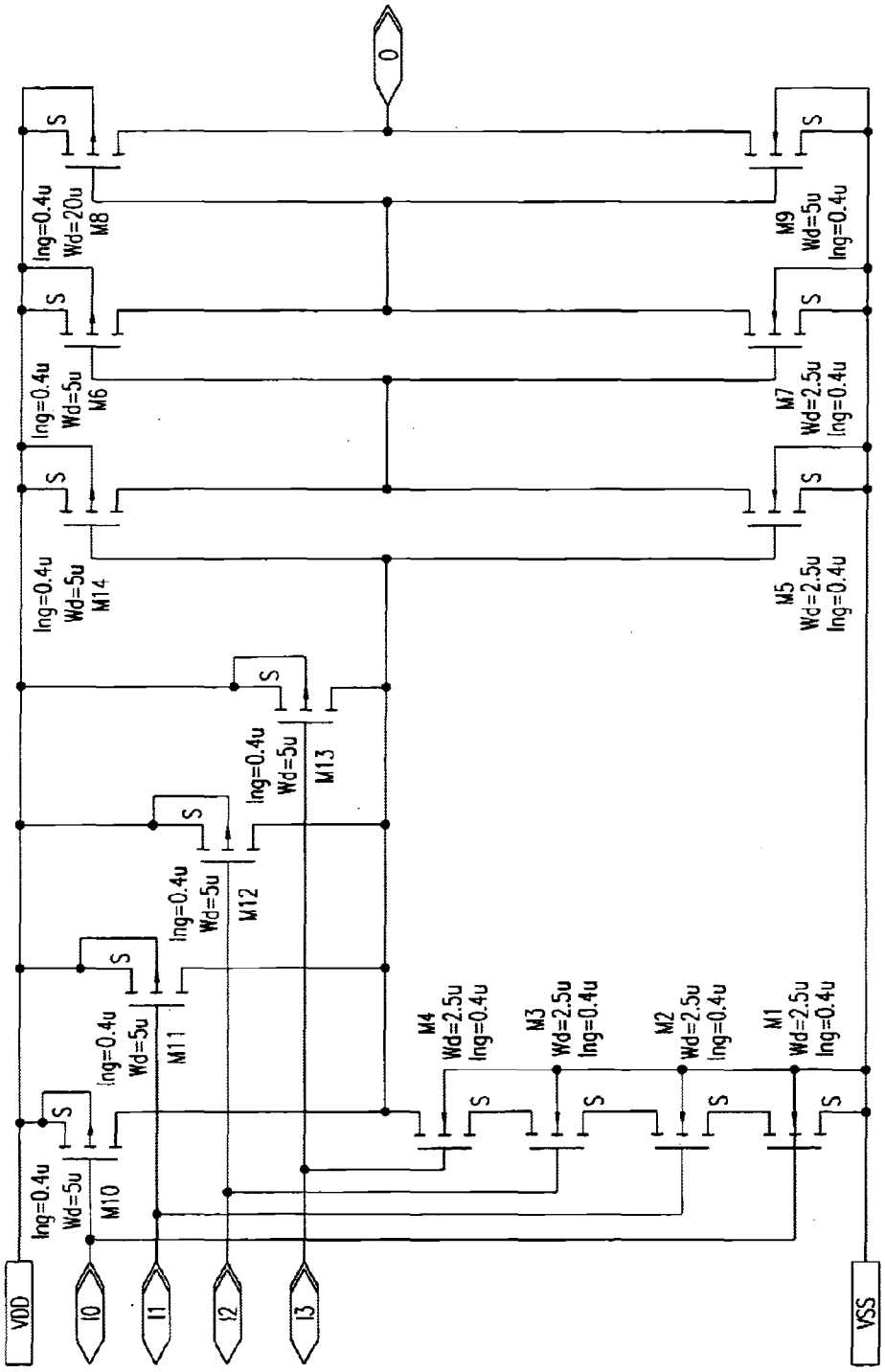

O
M8 lng=0.4u Wd=20u
M9 Wd=5u lng=0.4u
M6 lng=0.4u Wd=5u
M7 Wd=2.5u lng=0.4u
M14 lng=0.4u Wd=5u
M5 Wd=2.5u lng=0.4u
M13 lng=0.4u Wd=5u
M12 lng=0.4u Wd=5u
M11 lng=0.4u Wd=5u
M10 lng=0.4u Wd=5u
M4 Wd=2.5u lng=0.4u
M3 Wd=2.5u lng=0.4u
M2 Wd=2.5u lng=0.4u
M1 Wd=2.5u lng=0.4u
S
VDD
I0
I1
I2
I3
VSS

FIG. 156

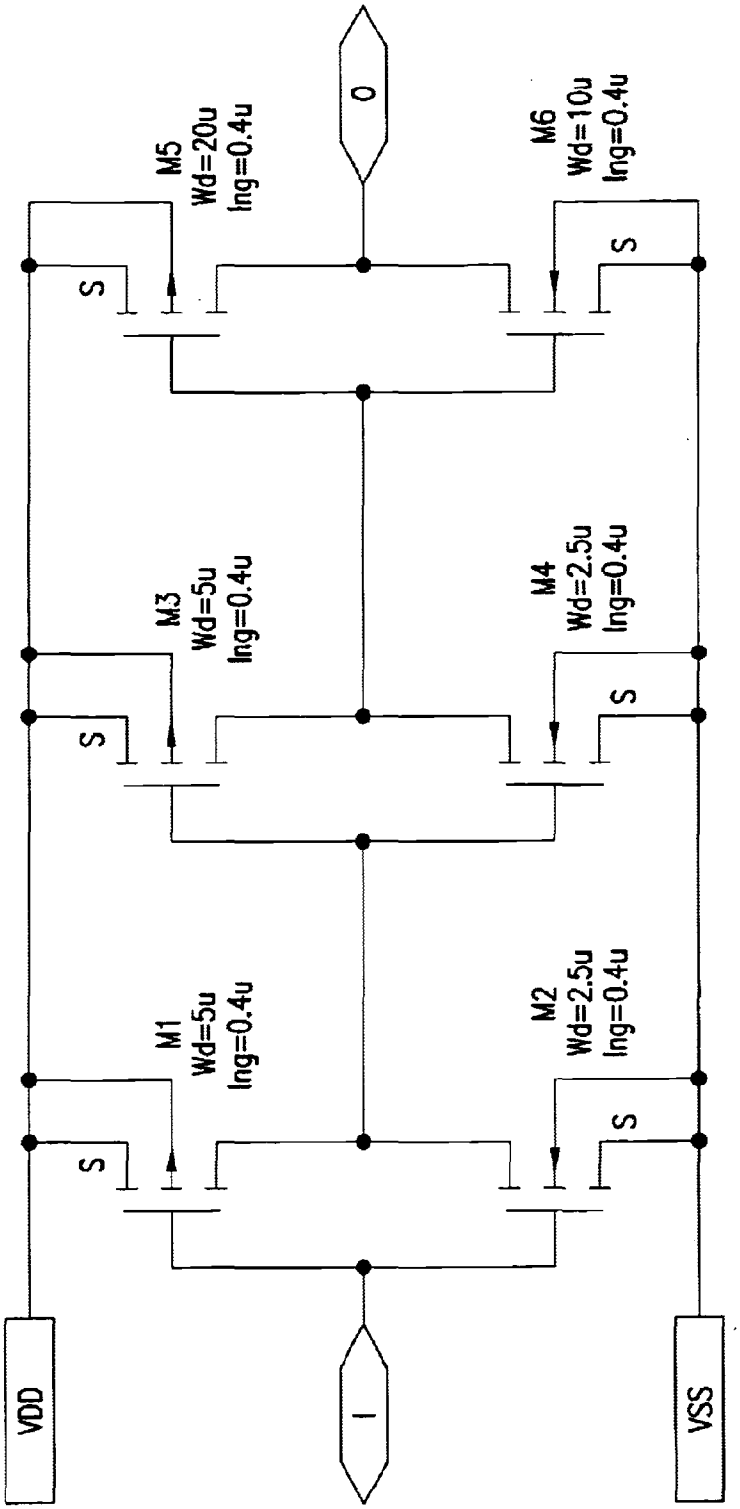

O
M5
Wd=20u
lng=0.4u
M6
Wd=10u
lng=0.4u
S
S
M3
Wd=5u
lng=0.4u
M4
Wd=2.5u
lng=0.4u
S
S
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
S
S
VDD
I
VSS

FIG.157

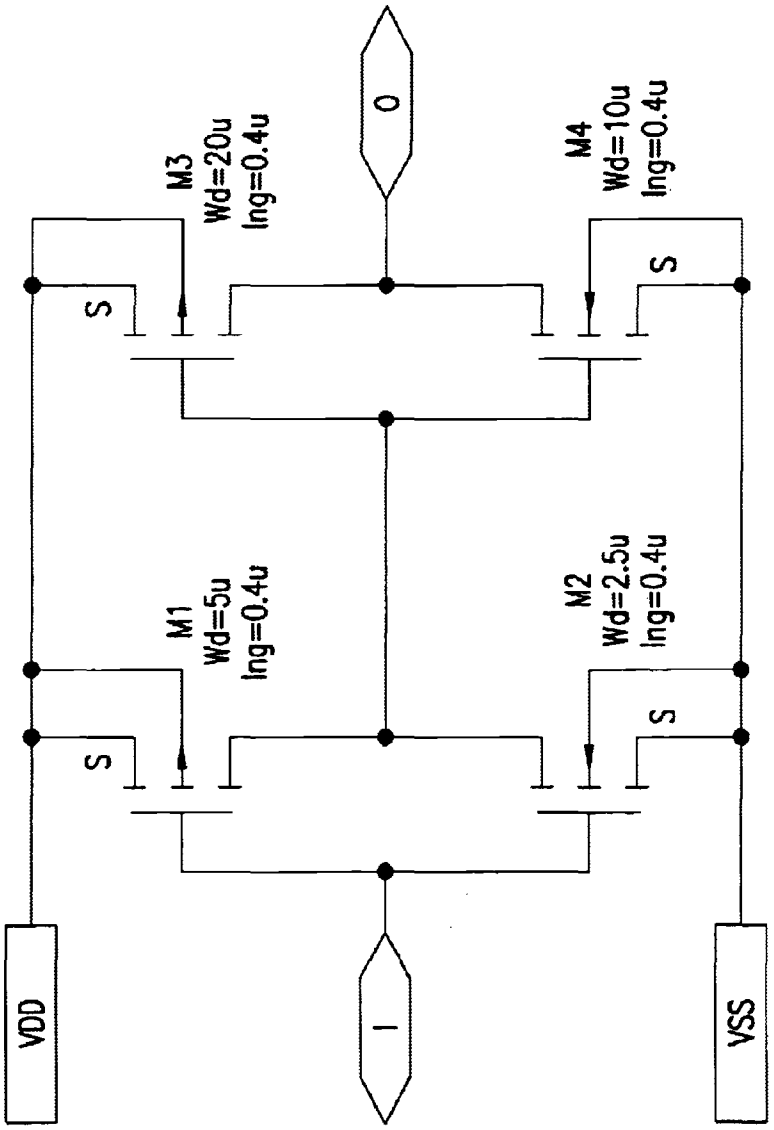

0
M3
Wd=20u
lng=0.4u
M4
Wd=10u
lng=0.4u
S
S
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
S
S
VDD
I
VSS

FIG.158

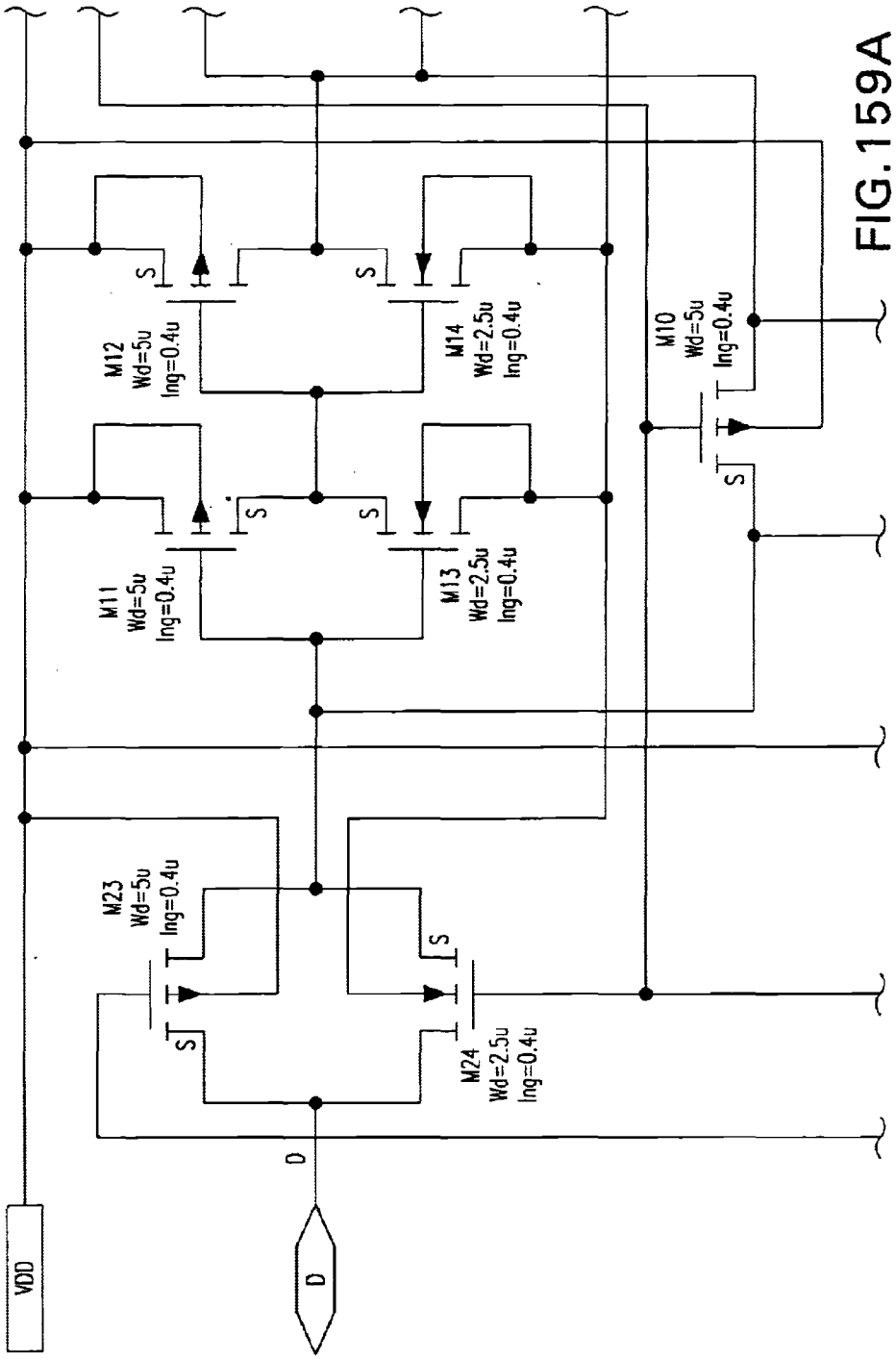

M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.159A

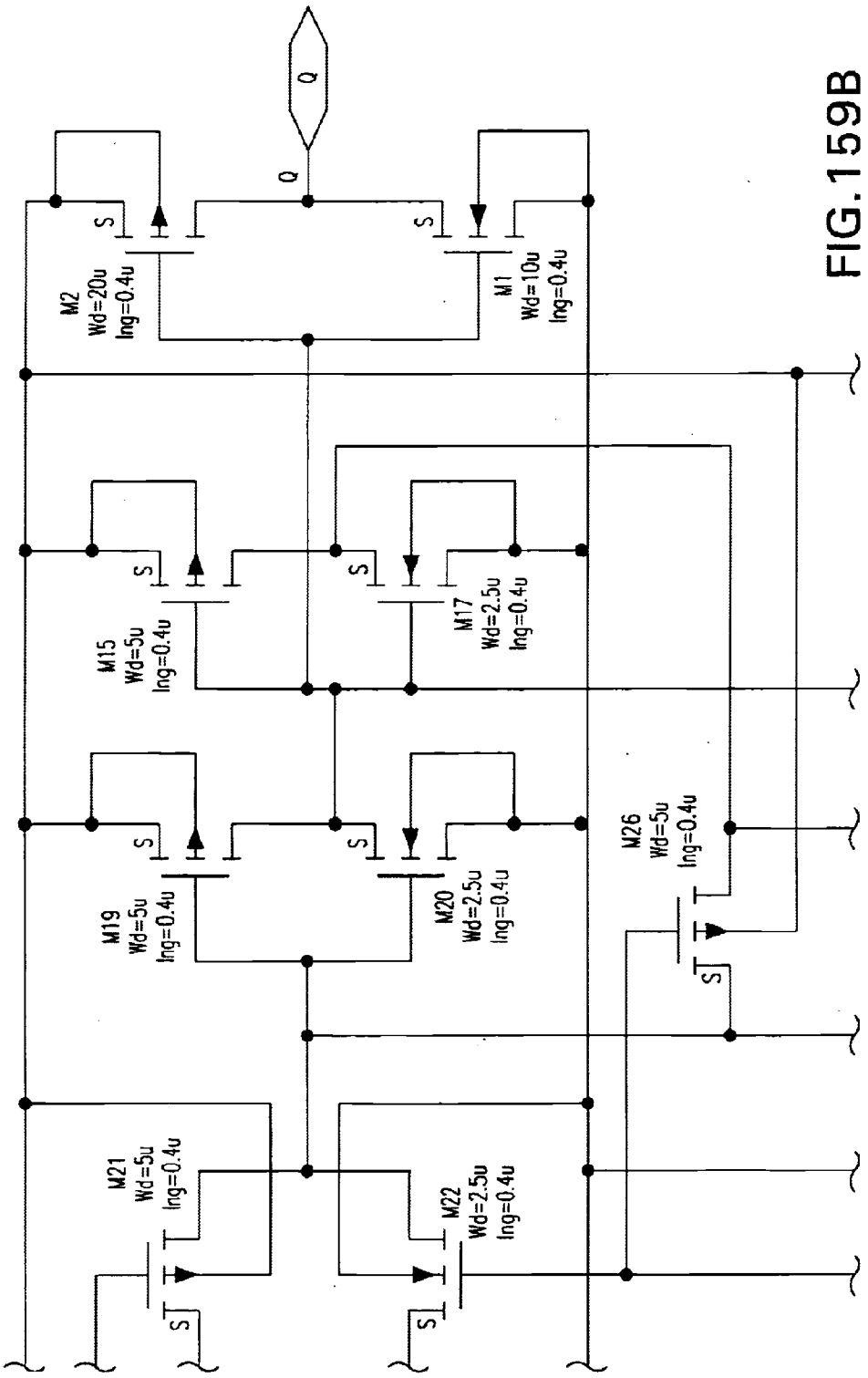

Q
Q
S
S
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
S
S
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
S
S
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
S
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
S
S

FIG.159B

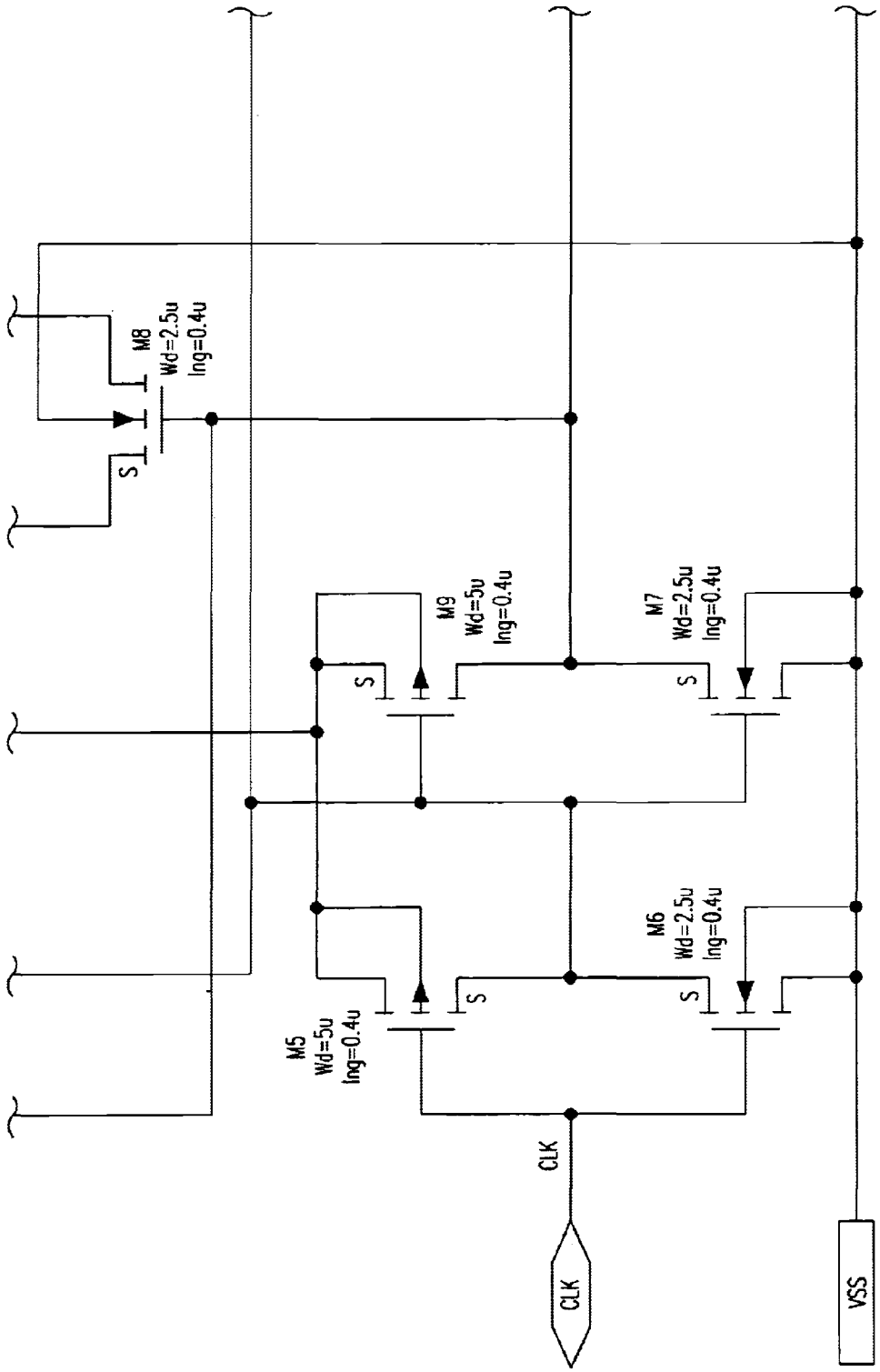

M8
Wd=2.5u
lng=0.4u
S
M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M5
Wd=5u
lng=0.4u
CLK
CLK
VSS

FIG.159C

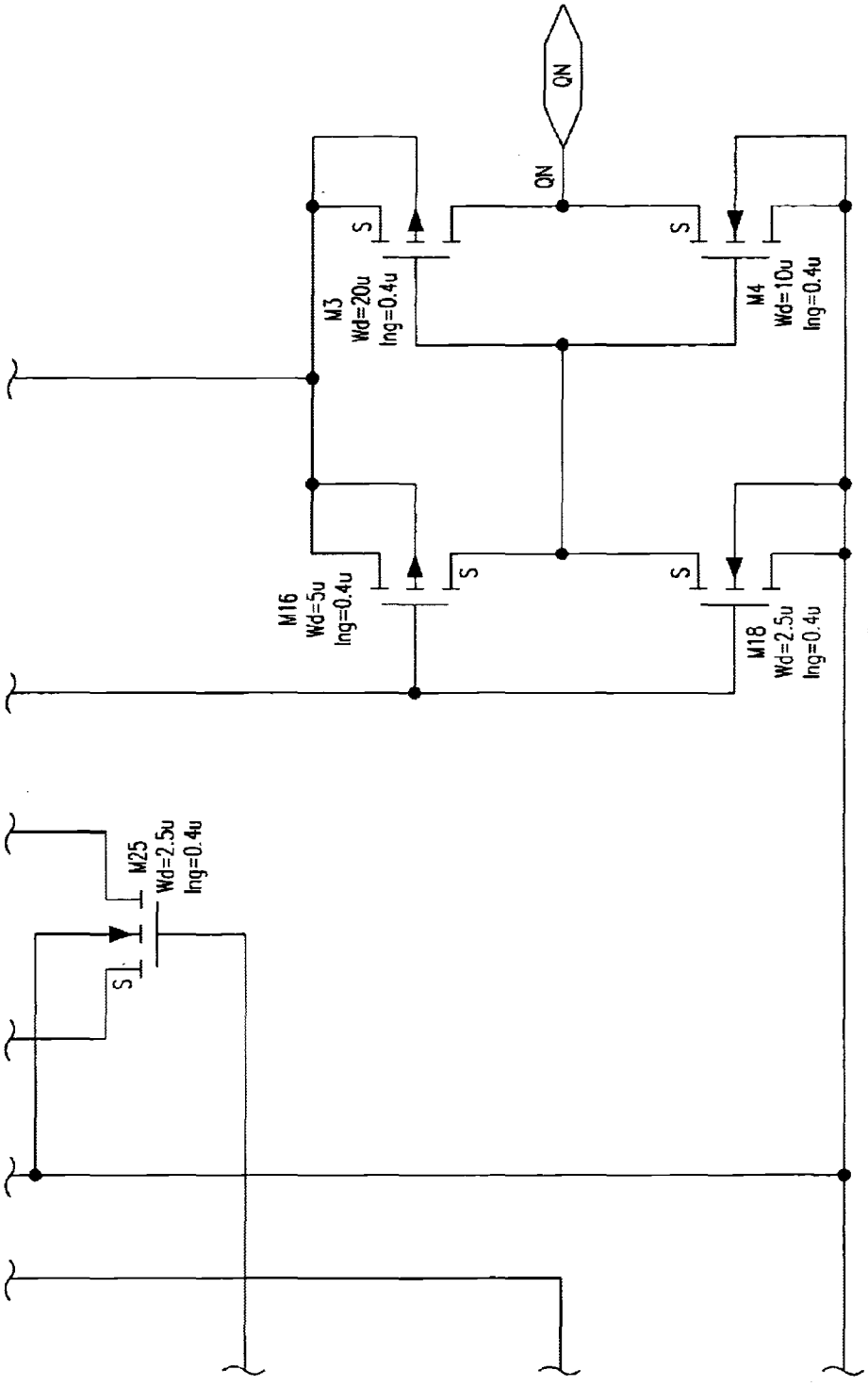

QN
QN
S
S
M3
Wd=20u
lng=0.4u
M4
Wd=10u
lng=0.4u
S
S
M16
Wd=5u
lng=0.4u
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S

FIG.159D

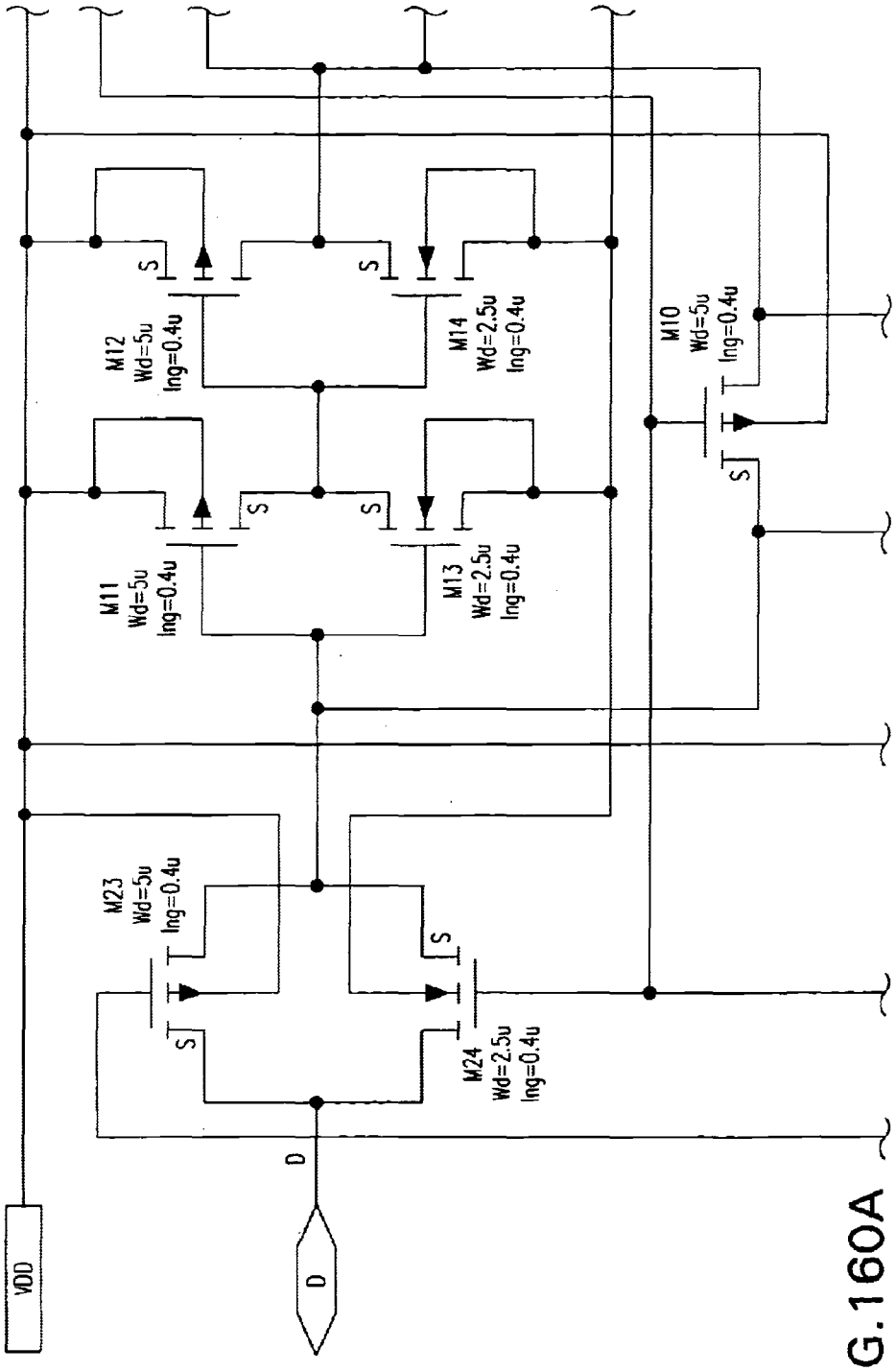

M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.160A

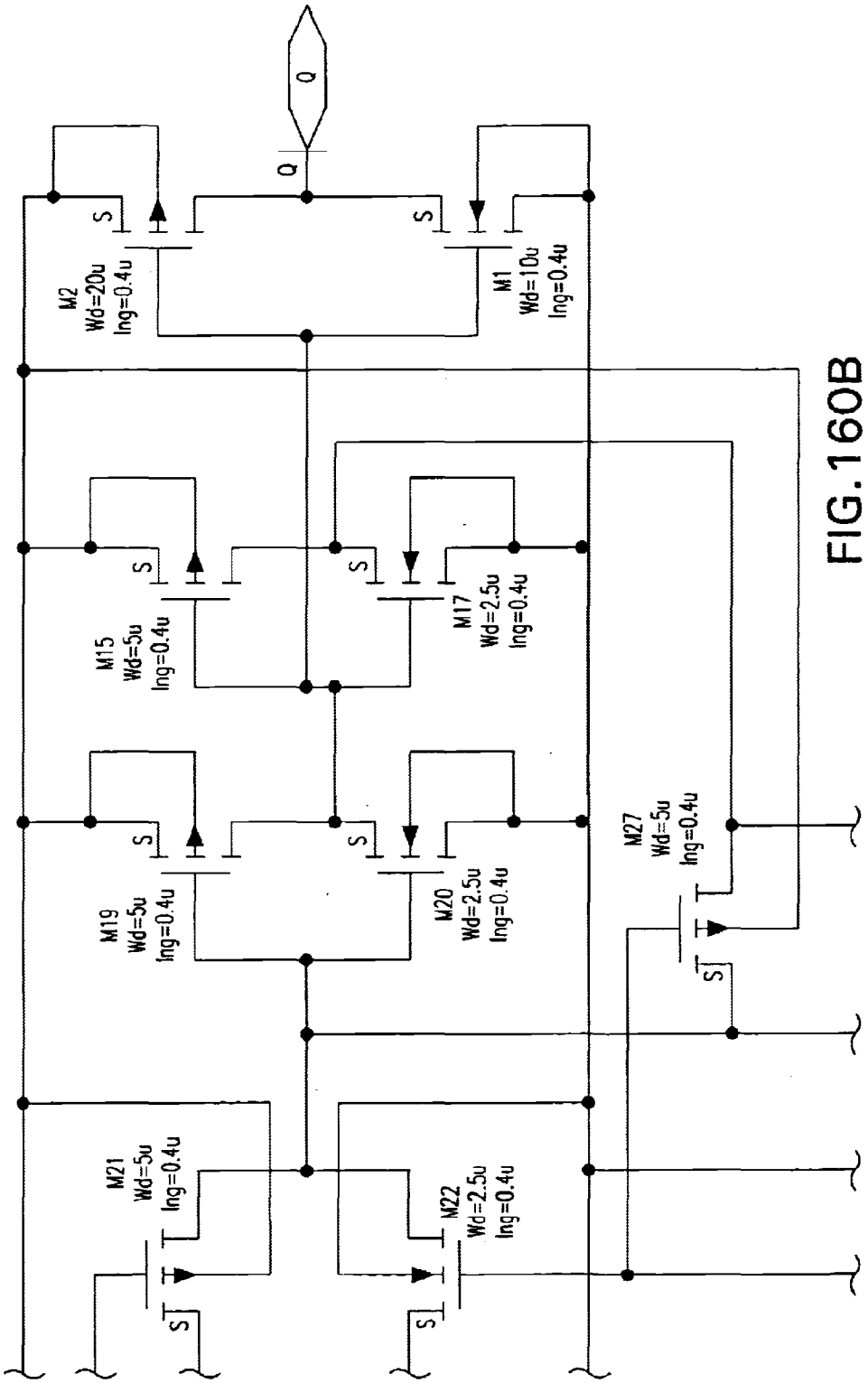

Q
Q
S
S
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
S
S
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
S
S
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
S
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
S
S

FIG.160B

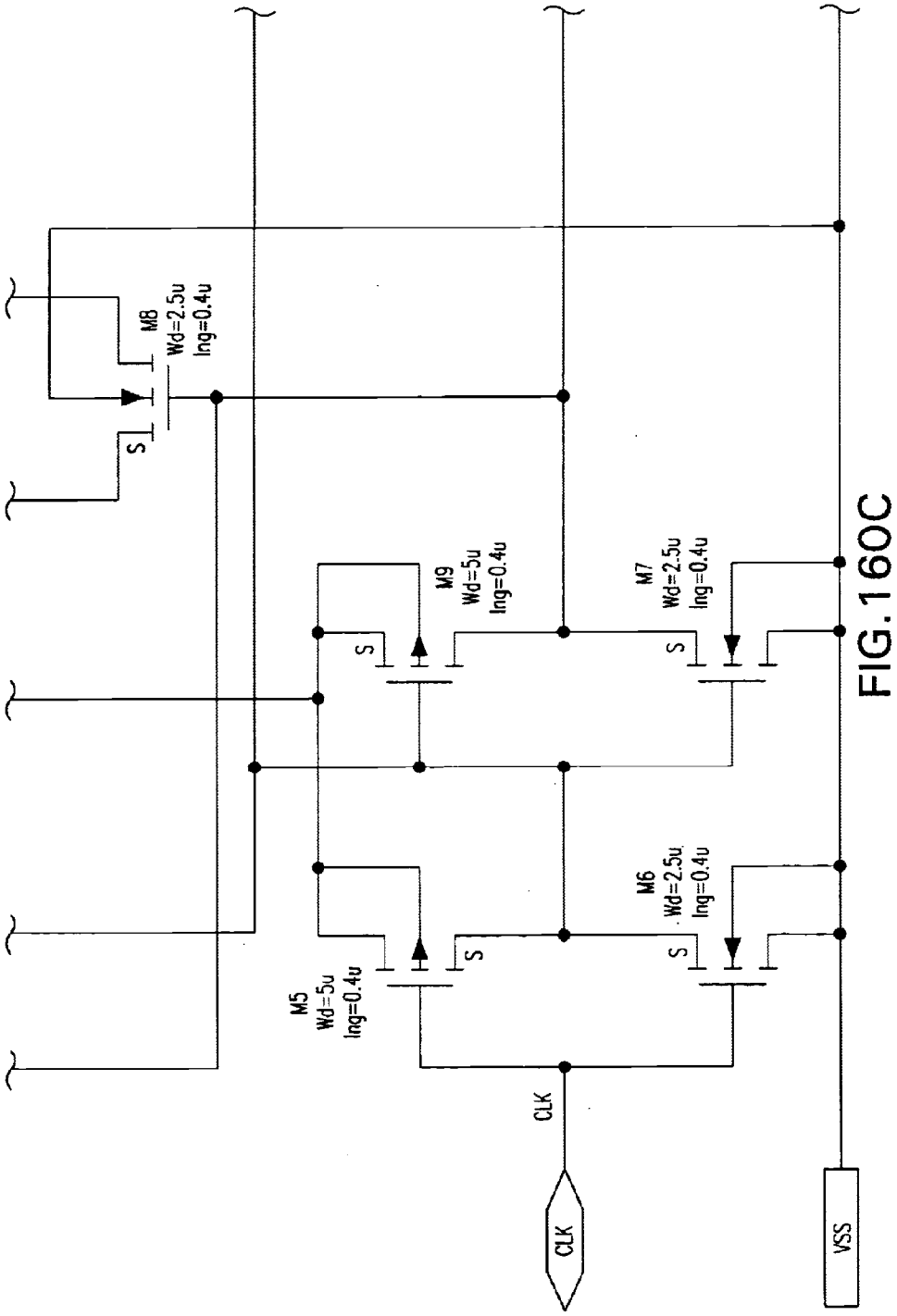

M8
Wd=2.5u
lng=0.4u
S
M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M5
Wd=5u
lng=0.4u
CLK
CLK
VSS

FIG. 160C

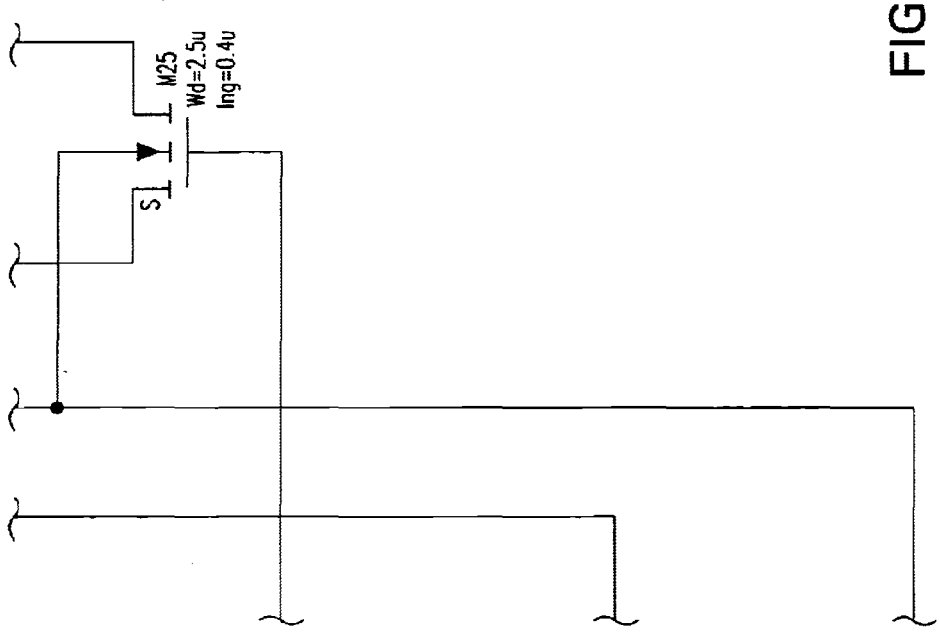


FIG. 160D

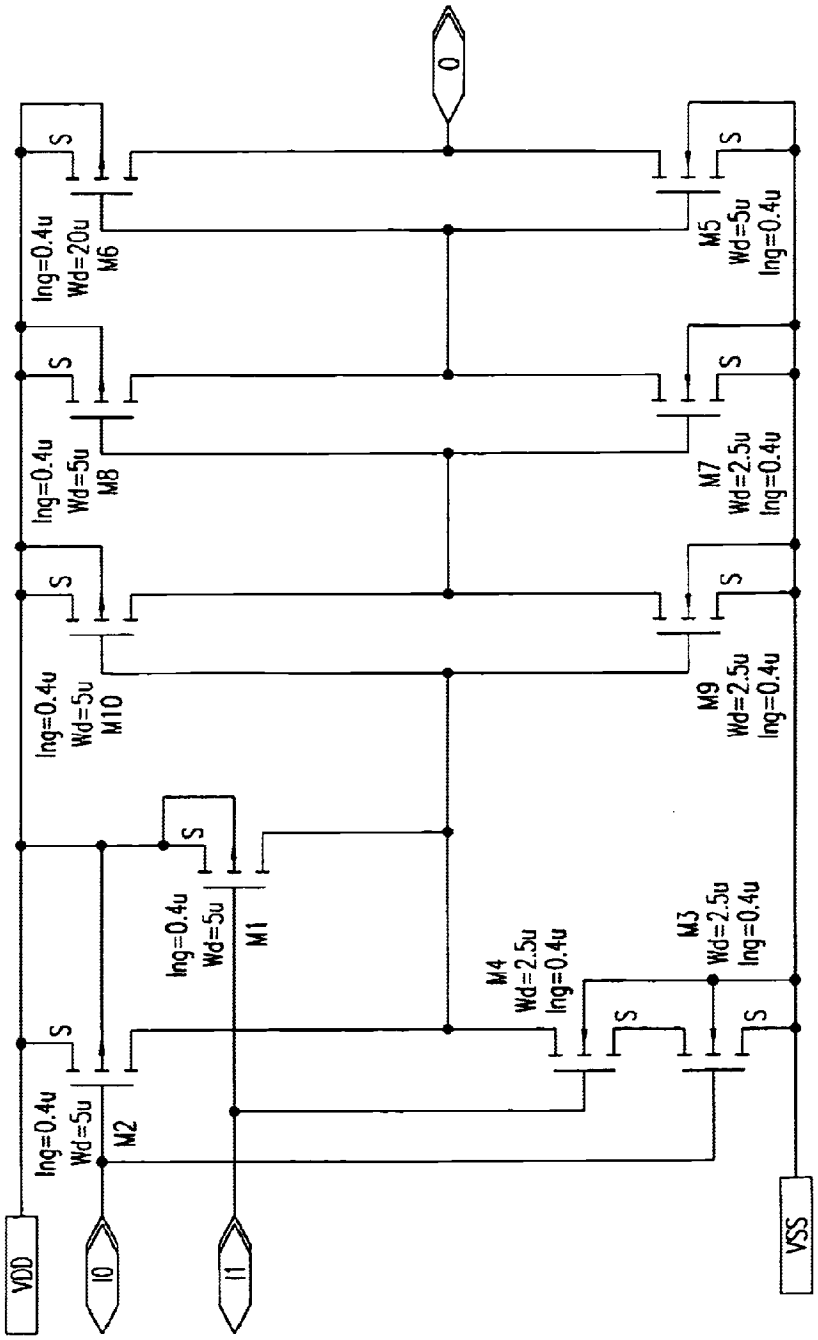

O
S
lng=0.4u
Wd=20u
M6
M5
Wd=5u
lng=0.4u
M8
M7
Wd=2.5u
M10
M9
M1
M4
M3
M2
VDD
I0
I1
VSS

FIG.161

WIRELESS LOCAL AREA NETWORK (WLAN) USING UNIVERSAL FREQUENCY TRANSLATION TECHNOLOGY INCLUDING MULTI-PHASE EMBODIMENTS AND CIRCUIT IMPLEMENTATIONS

CROSS-REFERENCE TO OTHER APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/147,129, filed on Aug. 4, 1999; and this application is a continuation-in-part of U.S. application Ser. No. 09/525,615, filed on Mar. 14, 2000; and this application is a continuation-in-part of U.S. application Ser. No. 09/526,041, filed on Mar. 14, 2000, all of which are incorporated herein by reference in their entireties.

The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

"Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,061,551 on May 9, 2000.

"Method and System for Down-Converting Electromagnetic Signals Having Optimized Switch Structures," Ser. No. 09/293,095, filed Apr. 16, 1999.

"Method and System for Down-Converting Electromagnetic Signals Including Resonant Structures for Enhanced Energy Transfer," Ser. No. 09/293,342, filed Apr. 16, 1999.

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,091,940 on Jul. 18, 2000.

"Method and System for Frequency Up-Conversion Having Optimized Switch Structures," Ser. No. 09/293,097, filed Apr. 16, 1999.

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,061,555 on May 9, 2000.

"Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,049,706 on Apr. 11, 2000.

"Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," Ser. No. 09/293,283, filed Apr. 16, 1999.

"Applications of Universal Frequency Translation," Ser. No. 09/261,129, filed Mar. 3, 1999.

"Method and System for Down-Converting an Electromagnetic Signal, Transforms For Same, and Aperture Relationships", Ser. No. 09/550,644, filed on Apr. 14, 2000.

"Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation", Ser. No. 09/632,857, filed on Aug. 4, 2000.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is generally related to wireless local area networks (WLANs), and more particularly, to WLANs that utilize universal frequency translation technology for frequency translation, and applications of same.

2. Related Art

Wireless LANs exist for receiving and transmitting information to/from mobile terminals using electromagnetic (EM) signals. Conventional wireless communications circuitry is complex and has a large number of circuit parts. This complexity and high parts count increases overall cost.

Additionally, higher part counts result in higher power consumption, which is undesirable, particularly in battery powered wireless units. Additionally, various communication components exist for performing frequency down-conversion, frequency up-conversion, and filtering. Also, schemes exist for signal reception in the face of potential jamming signals.

SUMMARY OF THE INVENTION

The present invention is directed to a wireless local area network (WLAN) that includes one or more WLAN devices (also called stations, terminals, access points, client devices, or infrastructure devices) for effecting wireless communications over the WLAN. The WLAN device includes at least an antenna, a receiver, and a transmitter for effecting wireless communications over the WLAN. Additionally, the WLAN device may also include a LNA/PA module, a control signal generator, a demodulation/modulation facilitation module, and a media access control (MAC) interface. The WLAN receiver includes at least one universal frequency translation module that frequency down-converts a received electromagnetic (EM) signal. In embodiments, the UFT based receiver is configured in a multi-phase embodiment to reduce or eliminate re-radiation that is caused by DC offset. The WLAN transmitter includes at least one universal frequency translation module that frequency up-converts a baseband signal in preparation for transmission over the WLAN. In embodiments, the UFT based transmitter is configured in a differential and/or multi-phase embodiment to reduce carrier insertion and spectral growth in the transmitted signal.

WLANs exhibit multiple advantages by using UFT modules for frequency translation. These advantages include, but are not limited to: lower power consumption, longer battery life, fewer parts, lower cost, less tuning, and more effective signal transmission and reception. These advantages are possible because the UFT module enables direct frequency conversion in an efficient manner with minimal signal distortion. The structure and operation of embodiments of the UFT module, and various applications of the same are described in detail in the following sections.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost character(s) and/or digit(s) in the corresponding reference number.

BRIEF DESCRIPTION OF THE FIGURES

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. **1**A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. **1**B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. **1**C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention;

FIG. **1**D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIGS. **2**A–**2**B illustrate block diagrams of universal frequency translation (UFT) modules according to an embodiment of the invention;

FIG. **3** is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. **4** is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. **5** is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention;

FIGS. **6**A–**6**I illustrate example waveforms used to describe the operation of the UFU module;

FIG. **7** illustrates a UFT module used in a receiver according to an embodiment of the invention;

FIG. **8** illustrates a UFT module used in a transmitter according to an embodiment of the invention;

FIG. **9** illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using a UFT module of the invention;

FIG. **10** illustrates a transceiver according to an embodiment of the invention;

FIG. **11** illustrates a transceiver according to an alternative embodiment of the invention;

FIG. **12** illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention;

FIG. **13** illustrates a UFT module used in a unified down-conversion and filtering (UDF) module according to an embodiment of the invention;

FIG. **14** illustrates an example receiver implemented using a UDF module according to an embodiment of the invention;

FIGS. **15**A–**15**F illustrate example applications of the UDF module according to embodiments of the invention;

FIG. **16** illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention, wherein the receiver may be further implemented using one or more UFD modules of the invention;

FIG. **17** illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention;

FIG. **18** is a table of example values at nodes in the UDF module of FIG. **19**;

FIG. **19** is a detailed diagram of an example UDF module according to an embodiment of the invention;

FIGS. **20**A and **20**A-**1** are example aliasing modules according to embodiments of the invention;

FIGS. **20**B **20**F are example waveforms used to describe the operation of the aliasing modules of FIGS. **20**A and **20**A-**1**;

FIG. **21** illustrates an enhanced signal reception system according to an embodiment of the invention;

FIGS. **22**A–**22**F are example waveforms used to describe the system of FIG. **21**;

FIG. **23**A illustrates an example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. **23**B and **23**C are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. **23**D illustrates another example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. **23**E and **23**F are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. **24**A illustrates an example receiver in an enhanced signal reception system according to an embodiment of the invention;

FIGS. **24**B–**24**J are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. **25** illustrates a block diagram of an example computer network;

FIG. **26** illustrates a block diagram of an example computer network;

FIG. **27** illustrates a block diagram of an example wireless interface;

FIG. **28** illustrates an example heterodyne implementation of the wireless interface illustrated in FIG. **27**;

FIG. **29** illustrates an example in-phase/quadrature-phase (I/Q) heterodyne implementation of the interface illustrated in FIG. **27**;

FIG. **30** illustrates an example high level block diagram of the interface illustrated in FIG. **27**, in accordance with the present invention;

FIG. **31** illustrates a example block diagram of the interface illustrated in FIG. **29**, in accordance with the invention;

FIG. **32** illustrates an example I/Q implementation of the interface illustrated in FIG. **31**;

FIGS. **33**–**38** illustrate example environments encompassed by the invention;

FIG. **39** illustrates a block diagram of a WLAN interface according to an embodiment of the invention;

FIG. **40** illustrates a WLAN receiver according to an embodiment of the invention;

FIG. **41** illustrates a WLAN transmitter according to an embodiment of the invention;

FIGS. **42**–**44** are example implementations of a WLAN interface: FIG. **42** includes FIGS. **42**A and **42**B and should be referred to for all references to FIG. **42** in the specification.

FIG. **43** includes FIGS. **43**A and **43**B and should be referred to for all references to FIG. **43** in the specification.

FIG. **44** includes FIGS. **44**A and **44**B and should be referred to for all references to FIG. **44** in the specification.

FIGS. **45**, **46**A, and **46**B and **46**C relate to an example MAC interface for an example WLAN interface embodiment;

FIGS. **47**, **48**, **49**A, and **49**B and **49**C relate to an example demodulator/modulator facilitation module for an example WLAN interface embodiment; FIG. **47** includes FIGS. **47**A–D and should be referred to for all references to FIG. **47** in the specification. FIG. **48** includes FIGS. **48**A–B and should be referred to for all references to FIG. **47** in the specification.

FIGS. **50**, **51**, **52**A, **52**B, and **52**C relate to an example alternate demodulator/modulator facilitation module for an example WLAN interface embodiment; FIG. **50** includes FIGS. **50**A–D and should be referred to for all references to FIG. **50** in the specification. FIG. **51** includes FIGS **51**A–B and should be referred to for all references to FIG. **51** in the specification. FIG. **52**B includes FIG. **52**B-**1** and should be referred to for for all references to FIG. **52**B in the specification.

FIGS. **53** and **54** relate to an example receiver for an example WLAN interface embodiment; FIG. **53** includes

FIGS. **53**A–C and should be referred to for all references to FIG. **53** in the specification.

FIGS. **55**, **56**A, and **56**B relate to an example synthesizer for an example WLAN interface embodiment; FIG. **55** includes FIGS. **55**A–C and should be referred to for all references to FIG. **55** in the specification.

FIGS. **57**, **58**, **59**, **60**, **61**A, and **61**B relate to an example transmitter for an example WLAN interface embodiment; FIG. **57** includes FIGS. **57**A–D and should be referred to for all references to FIG. **57** in the specification. FIG. **60** includes FIGS. **60**A D and should be referred to for all references to FIG. **60** in the specification.

FIGS. **62** and **63** relate to an example motherboard for an example WLAN interface embodiment; FIG. **62** includes FIGS. **62**A–I and should be referred to for all references to FIG. **62** in the specification.

FIGS. **64**–**66** relate to example LNAs for an example WLAN interface embodiment; FIG. **64** includes FIGS. **64**A–C and should be referred to for all references to FIG. **64** in the specification. FIG. **65** includes FIGS **65**A–E and should be referred to for all references to FIG. **65** in the specification. FIG. **66** includes FIG. **66**A–B and should be referred to for all referrences to FIG. **66** in the specification.

FIGS. **67**A B illustrate IQ receivers having UFT modules in a series and shunt configurations, according to embodiments of the invention;

FIGS. **68**A–B illustrate IQ receivers having UFT modules with delayed control signals for quadrature implementation, according to embodiments of the present invention;

FIGS. **69**A–B illustrate IQ receivers having FET implementations, according to embodiments of the invention;

FIG. **70**A illustrates an IQ receiver having shunt UFT modules according to embodiments of the invention; FIG. **70**A includes FIGS **70**A-**1** and should be referred to for all references to FIG. **70**A in the specification

FIG. **70**B illustrates control signal generator embodiments for receiver **7000** according to embodiments of the invention;

FIGS. **70**C–D illustrate various control signal waveforms according to embodiments of the invention;

FIG. **70**E illustrates an example IQ modulation receiver embodiment according to embodiments of the invention; FIG. **70**E includes FIG **70**E**1** and FIG. **70**E**2** and should be referred to for all references to FIG. **70**E in the specification.

FIGS. **70**F–P illustrate example waveforms that are representative of the IQ receiver in FIG. **70**E;

FIGS. **70**Q–R illustrate single channel receiver embodiments according to embodiments of the invention;

FIG. **70**S illustrates a FET configuration of an IQ receiver embodiment according to embodiments of the invention; FIG. **70**S includes FIGS **70**S-**1** and should be referred to for all references to FIG. **70**S in the specification.

FIG. **71**A illustrate a balanced transmitter **7102**, according to an embodiment of the present invention;

FIGS. **71**B–C illustrate example waveforms that are associated with the balanced transmitter **7102**, according to an embodiment of the present invention;

FIG. **71**D illustrates example FET configurations of the balanced transmitter **7102**, according to embodiments of the present invention;

FIGS. **72**A–I illustrate various example timing diagrams that are associated with the transmitter **7102**, according to embodiments of the present invention;

FIG. **72**J illustrates an example frequency spectrum that is associated with a modulator **7104**, according to embodiments of the present invention;

FIG. **73**A illustrate a transmitter **7302** that is configured for carrier insertion, according to embodiments of the present invention;

FIG. **73**B illustrates example signals associated with the transmitter **7302**, according to embodiments of the invention;

FIG. **74** illustrates an IQ balanced transmitter **7420**, according to embodiments of the present invention;

FIGS. **75**A–C illustrate various example signal diagrams associated with the balanced transmitter **7420** in FIG. **74**;

FIG. **76**A illustrates an IQ balanced transmitter **7608** according to embodiments of the invention;

FIG. **76**B illustrates an IQ balanced modulator **7618** according to embodiments of the invention;

FIG. **77** illustrates an IQ balanced modulator **7702** configured for carrier insertion according to embodiments of the invention;

FIG. **78** illustrates an IQ balanced modulator **7802** configured for carrier insertion according to embodiments of the invention;

FIG. **79**A illustrate a transmitter **7900**, according to embodiments of the present invention;

FIGS. **79**B–C illustrate various frequency spectrums that are associated with the transmitter **7900**;

FIG. **79**D illustrates a FET configuration for the transmitter **7900**, according to embodiments of the present invention;

FIG. **80** illustrates an IQ transmitter **8000**, according to embodiments of the present invention;

FIGS. **81**A–C illustrate various frequency spectrums that are associated with the IQ transmitter **8000**, according to embodiments of the present invention;

FIG. **82** illustrates an IQ transmitter **8200**, according to embodiments of the present invention;

FIG. **83** illustrates an IQ transmitter **8300**, according to embodiments of the invention;

FIG. **84** illustrates a flowchart **8400** that is associated with the transmitter **7102** in the FIG. **71**A, according to embodiments of the invention;

FIG. **85** illustrates a flowchart **8500** that further defines the flowchart **8400** in the FIG. **84**, and is associated with the transmitter **7102** according to embodiments of the invention;

FIG. **86** illustrates a flowchart **8600** that is associated with the transmitter **7900** and further defines the flowchart **8400** in the FIG. **84**, according to embodiments of the invention;

FIG. **87** illustrates a flowchart **8700**, that is associated with the transmitter **7420** in the FIG. **74**, according to embodiments of the invention;

FIG. **88** illustrates a flowchart **8800** that is associated with the transmitter **8000**, according to embodiments of the invention;

FIG. **89**A illustrate a pulse generator according to embodiments of the invention;

FIGS. **89**B–C illustrate various example signal diagrams associated with the pulse generator in FIG. **89**A, according to embodiments of the invention;

FIGS. **89**D–E illustrate various example pulse generators according to embodiments of the present invention;

FIGS. **90**A–D illustrate various implementation circuits for the modulator **7410**, according to embodiments of the

present invention; FIG. **90**B includes FIGS. **90B-1**, **90B-2**, **90B-3**, and **90B-4** and should be referred to for all references to FIG. **90**B in the specification. FIG. **90**C includes FIGS. **90C-1**, **90C-2**, **90C-3** and **90C-4** and should be referred to for all referneces to FIG. **90**C in the specification.

FIG. **91** illustrates an IQ transceiver **9100** according to embodiments of the present invention;

FIG. **92** illustrates direct sequence spread spectrum according to embodiments of the present invention;

FIG. **93** illustrates the LNA/PA module **3904** according to embodiments of the present invention;

FIG. **94** illustrates a WLAN device **9400**, according to embodiments of the invention of the present invention; and

FIGS. **95**A C, and FIGS. **96** **161** illustrate schematics for an integrated circuit implementation example of the present invention. FIG. **97** includes FIGS. **97**A–D and should be referred to for all references to FIG. **97** in the specification. FIG. **105** includes FIGS. **105**A–D, **105** E1-E2, and **105**F–V, and should be referred to for all references to FIG. **105** in the specification. FIG. **106** includes FIGS. **106**A–F and should be referred to for all references to FIG. **106** in the specification. FIG. **107** includes FIGS. **107**A D and should be referred to for all referrences to FIG. **107** in the specification. FIG. **109** includes FIGS. **109**A–D and should be referred to for all references to FIG. **109** in the specification. FIG. **110** includes FIGS. **110**A–D and should be referred to for all references to FIG. **110** in the specification. FIG. **112**A–D and should be referred to for all references to FIG. **112** in the specification. FIG. **113** includes FIGS. **113**A–F and should be referred to for all references to FIG. **113** in the specification. FIG. **115** includes FIGS. **115**A F and should be referred to for all references to FIG. **115** in the specification. FIG. **118** includes FIG. **118**A–D and should be referred to for all references to FIG **118** in the specification. FIG. **123** includes FIGS. **123**A–H and should be referred to for all references to FIG. **123** in the specification. FIG. **125** includes FIGS. **125**A–H and should be referred to for all references to FIGS **125** in the specification. FIG. **126** includes FIGS. **126**A–H and should be referred to for all references to FIG. **126** in the specification. FIG. **127** includes FIGS **127**A–D and should be referred to for all references to FIG. **127** in the specification. FIG. **150** includes FIGS. **150**A–H and should be referred to for all references to FIG. **150** in the specification. FIG. **150** includes FIGS. **159**A–D and should be referred to for all references to FIG. **159** in the specification. FIG. **160** includes FIGS. **160**A–D and should be referred to for all references ti FIG. **160** in the specification.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

TABLE OF CONTENTS

1. Universal Frequency Translation
2. Frequency Down-Conversion
3. Frequency Up-Conversion
4. Enhanced Signal Reception
5. Unified Down-Conversion and Filtering
6. Example Application Embodiments of the Invention
   - 6.1 Data Communication
     - 6.1.1 Example Implementations: Interfaces, Wireless Modems, Wireless LANs, etc.
     - 6.1.2 Example Modifications
   - 6.2 Other Example Applications
7.0 Example WLAN Implementation Embodiments

-continued

TABLE OF CONTENTS

- 7.1 Architecture
- 7.2 Receiver
  - 7.2.1 IQ Receiver
  - 7.2.2 Multi-Phase IQ Receiver
    - 7.2.2.1 Example I/Q Modulation Control Signal Generator Embodiments
    - 7.2.2.2 Implementation of Multi-phase I/Q Modulation Receiver Embodiment with Exemplary Waveforms
    - 7.2.2.3 Example Single Channel Receiver Embodiment
    - 7.2.2.4 Alternative Example I/Q Modulation Receiver Embodiment
- 7.3 Transmitter
  - 7.3.1 Universal Transmitter with 2 UFT Modules
    - 7.3.1.1 Balanced Modulator Detailed Description
    - 7.3.1.2 Balanced Modulator Example Signal Diagrams and Mathematical Description
    - 7.3.1.3 Balanced Modulator Having a Shunt Configuration
    - 7.3.1.4 Balanced Modulator FET Configuration
    - 7.3.1.5 Universal Transmitter Configured for Carrier Insertion
  - 7.3.2 Universal Transmitter In IQ Configuration
    - 7.3.2.1 IQ Transmitter Using Series-Type Balanced Modulator
    - 7.3.2.2 IQ Transmitter Using Shunt-Type Balanced Modulator
    - 7.3.2.3 IQ Transmitters Configured for Carrier Insertion
- 7.4 Transceiver Embodiments
- 7.5 Demodulator/Modulator Facilitation Module
- 7.6 MAC Interface
- 7.7 Control Signal Generator - Synthesizer
- 7.8 LNA/PA

8.0 802.11 Physical Layer Configurations

9.0 Appendix

10.0 Conclusion

1. Universal Frequency Translation

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

FIG. **1**A illustrates a universal frequency translation (UFT) module **102** according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

As indicated by the example of FIG. **1**A, some embodiments of the UFT module **102** include three ports (nodes), designated in FIG. **1**A as Port **1**, Port **2**, and Port **3**. Other UFT embodiments include other than three ports.

Generally, the UFT module **102** (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module **102** (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

An example embodiment of the UFT module **103** is generally illustrated in FIG. **1**B. Generally, the UFT module **103** includes a switch **106** controlled by a control signal **108**. The switch **106** is said to be a controlled switch.

As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. **2** illustrates an example UFT module **202**. The example UFT

module **202** includes a diode **204** having two ports, designated as Port **1** and Port **2/3**. This embodiment does not include a third port, as indicated by the dotted line around the "Port **3**" label.

The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

For example, a UFT module **115** can be used in a universal frequency down-conversion (UFD) module **114**, an example of which is shown in FIG. **1**C. In this capacity, the UFT module **115** frequency down-converts an input signal to an output signal.

As another example, as shown in FIG. **1**D, a UFT module **117** can be used in a universal frequency up-conversion (UFU) module **116**. In this capacity, the UFT module **117** frequency up-converts an input signal to an output signal.

These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2. Frequency Down-Conversion

The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in co-pending U.S. Patent Application entitled "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,061,551 on May 9, 2000, the full disclosure of which is incorporated herein by reference. A relevant portion of the above mentioned patent application is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. **20**A illustrates an aliasing module **2000** (also called a universal frequency down-conversion module) for down-conversion using a universal frequency translation (UFT) module **2002** which down-converts an EM input signal **2004**. In particular embodiments, aliasing module **2000** includes a switch **2008** and a capacitor **2010**. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch **2008** is in series with input signal **2004** and capacitor **2010** is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. **20**A-**1**), the capacitor **2010** is in series with the input signal **2004** and the switch **2008** is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module **2000** with UFT module **2002** can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal **2004**.

In one implementation, aliasing module **2000** down-converts the input signal **2004** to an intermediate frequency (IF) signal. In another implementation, the aliasing module **2000** down-converts the input signal **2004** to a demodulated baseband signal. In yet another implementation, the input signal **2004** is a frequency modulated (FM) signal, and the aliasing module **2000** down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal **2006** includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal **2004**. In this embodiment, the control signal **2006** is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal **2004**. Preferably, the frequency of control signal **2006** is much less than the input signal **2004**.

A train of pulses **2018** as shown in FIG. **20**D controls the switch **2008** to alias the input signal **2004** with the control signal **2006** to generate a down-converted output signal **2012**. More specifically, in an embodiment, switch **2008** closes on a first edge of each pulse **2020** of FIG. **20**D and opens on a second edge of each pulse. When the switch **2008** is closed, the input signal **2004** is coupled to the capacitor **2010**, and charge is transferred from the input signal to the capacitor **2010**. The charge stored during successive pulses forms down-converted output signal **2012**.

Exemplary waveforms are shown in FIGS. **20**B–**20**F.

FIG. **20**B illustrates an analog amplitude modulated (AM) carrier signal **2014** that is an example of input signal **2004**. For illustrative purposes, in FIG. **20**C, an analog AM carrier signal portion **2016** illustrates a portion of the analog AM carrier signal **2014** on an expanded time scale. The analog AM carrier signal portion **2016** illustrates the analog AM carrier signal **2014** from time t_0 to time t_1.

FIG. **20**D illustrates an exemplary aliasing signal **2018** that is an example of control signal **2006**. Aliasing signal **2018** is on approximately the same time scale as the analog AM carrier signal portion **2016**. In the example shown in FIG. **20**D, the aliasing signal **2018** includes a train of pulses **2020** having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses **2020** repeat at an aliasing rate, or pulse repetition rate of aliasing signal **2018**. The aliasing rate is determined as described below, and further described in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," application Ser. No. 09/176,022, issued as U.S. Pat. No. 6,061,551 on May 9, 2000.

As noted above, the train of pulses **2020** (i.e., control signal **2006**) control the switch **2008** to alias the analog AM carrier signal **2016** (i.e., input signal **2004**) at the aliasing rate of the aliasing signal **2018**. Specifically, in this embodiment, the switch **2008** closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch **2008** is closed, input signal **2004** is coupled to the capacitor **2010**, and charge is transferred from the input signal **2004** to the capacitor **2010**. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples **2022** form down-converted signal portion **2024** (FIG. **20**E) that corresponds to the analog AM carrier signal portion **2016** (FIG. **20**C) and the train of pulses **2020** (FIG. **20**D). The charge stored during successive under-samples of AM carrier signal **2014** form the down-converted signal **2024** (FIG. **20**E) that is an example of down-converted output signal **2012** (FIG. **20**A). In FIG. **20**F, a demodulated baseband signal **2026** represents the demodulated baseband signal **2024** after filtering on a compressed time scale. As illustrated, down-converted signal **2026** has substantially the same "amplitude envelope" as AM carrier signal **2014**. Therefore, FIGS. **20**B–**20**F illustrate down-conversion of AM carrier signal **2014**.

The waveforms shown in FIGS. **20**B–**20**F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," application Ser. No. 09/176,022, issued as U.S. Pat. No. 6,061,551 on May 9, 2000.

The aliasing rate of control signal **2006** determines whether the input signal **2004** is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal **2004**, the aliasing rate of the control signal **2006**, and the down-converted output signal **2012** are illustrated below:

(Freq. of input signal **2004**)=*n*·(Freq. of control signal **2006**)±(Freq. of down-converted output signal **2012**)

For the examples contained herein, only the "+" condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal **2004** (e.g., n=0.5, 1, 2, 3, . . .).

When the aliasing rate of control signal **2006** is off-set from the frequency of input signal **2004**, or off-set from a harmonic or sub-harmonic thereof, input signal **2004** is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal **2004**. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal **2004** includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal **2006** would be calculated as follows:

$$(Freq_{input}-Freq_{IF})/n=Freq_{control}$$

$$(901\ MHZ-1\ MHZ)/n=900/n$$

For n=0.5, 1, 2, 3, 4, etc., the frequency of the control signal **2006** would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signals, and exemplary methods and systems thereof, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," application Ser. No. 09/176,022, issued as U.S. Pat. No. 6,061,551 on May 9, 2000.

Alternatively, when the aliasing rate of the control signal **2006** is substantially equal to the frequency of the input signal **2004**, or substantially equal to a harmonic or sub-harmonic thereof, input signal **2004** is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-sampling pulses occur at the same point of subsequent cycles of the input signal **2004**. As a result, the under-samples form a constant output baseband signal. If the input signal **2004** includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal **2006** would be calculated as follows:

$$(Freq_{input}-Freq_{IF})/n=Freq_{control}$$

$$(900\ MHZ-0\ MHZ)/n=900\ MHZ/n$$

For n=0.5, 1, 2, 3, 4, etc., the frequency of the control signal **2006** should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," application Ser. No. 09/176,022, issued as U.S. Pat. No. 6,061,551 on May 9, 2000.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1+F_2)\div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal **2006** would be calculated as follows:

$$\begin{aligned}\text{Frequency of the input} &= (F_1 + F_2) \div 2\\ &= (899\ MHZ + 901\ MHZ) \div 2\\ &= 900\ MHZ\end{aligned}$$

Frequency of the down-converted signal=0 (i.e., baseband)

$$(Freq_{input}-Freq_{IF})/n=Freq_{control}$$

$$(900\ MHZ-0\ MHZ)/n=900\ MHZ/n$$

For n=0.5, 1, 2, 3, etc., the frequency of the control signal **2006** should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal **2006** should be substantially equal to:

$$(900\ MHZ-0\ MHZ)/n=900\ MHZ/n,$$

or

$$(901\ MHZ-0\ MHZ)/n=901\ MHZ/n.$$

For the former case of 900 MHZ/n, and for n=0.5, 1, 2, 3, 4, etc., the frequency of the control signal **2006** should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/n, and for n=0.5, 1, 2, 3, 4, etc., the frequency of the control signal **2006** should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The frequency of the down-converted AM signal is substantially

equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," application Ser. No. 09/176,022, issued as U.S. Pat. No. 6,061,551 on May 9, 2000.

In an embodiment, the pulses of the control signal **2006** have negligible apertures that tend towards zero. This makes the UFT module **2002** a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal **2006** have non-negligible apertures that tend away from zero. This makes the UFT module **2002** a lower input impedance device. This allows the lower input impedance of the UFT module **2002** to be substantially matched with a source impedance of the input signal **2004**. This also improves the energy transfer from the input signal **2004** to the down-converted output signal **2012**, and hence the efficiency and signal to noise (s/n) ratio of UFT module **2002**.

Exemplary systems and methods for generating and optimizing the control signal **2006** and for otherwise improving energy transfer and s/n ratio, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," application Ser. No. 09/176,022, issued as U.S. Pat. No. 6,061,551 on May 9, 2000.

3. Frequency Up-Conversion

The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

An example frequency up-conversion system **300** is illustrated in FIG. **3**. The frequency up-conversion system **300** is now described.

An input signal **302** (designated as "Control Signal" in FIG. **3**) is accepted by a switch module **304**. For purposes of example only, assume that the input signal **302** is a FM input signal **606**, an example of which is shown in FIG. **6**C. FM input signal **606** may have been generated by modulating information signal **602** onto oscillating signal **604** (FIGS. **6**A and **6**B). It should be understood that the invention is not limited to this embodiment. The information signal **602** can be analog, digital, or any combination thereof, and any modulation scheme can be used.

The output of switch module **304** is a harmonically rich signal **306**, shown for example in FIG. **6**D as a harmonically rich signal **608**. The harmonically rich signal **608** has a continuous and periodic waveform.

FIG. **6**E is an expanded view of two sections of harmonically rich signal **608**, section **610** and section **612**. The harmonically rich signal **608** may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

Harmonically rich signal **608** is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal **608**. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. **6**F and FIG. **6**G show separately the sinusoidal components making up the first, third, and fifth harmonics of section **610** and section **612**. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal **608** is shown as a square wave, there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. **6**H.

The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal **306** and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal **306**. According to an embodiment of the invention, the input signal **606** may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

A filter **308** filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal **310**, shown for example as a filtered output signal **614** in FIG. **6**I.

FIG. **4** illustrates an example universal frequency up-conversion (UFU) module **401**. The UFU module **401** includes an example switch module **304**, which comprises a bias signal **402**, a resistor or impedance **404**, a universal frequency translator (UFT) **450**, and a ground **408**. The UFT **450** includes a switch **406**. The input signal **302** (designated as "Control Signal" in FIG. **4**) controls the switch **406** in the UFT **450**, and causes it to close and open. Harmonically rich signal **306** is generated at a node **405** located between the resistor or impedance **404** and the switch **406**.

Also in FIG. **4**, it can be seen that an example filter **308** is comprised of a capacitor **410** and an inductor **412** shunted to a ground **414**. The filter is designed to filter out the undesired harmonics of harmonically rich signal **306**.

The invention is not limited to the UFU embodiment shown in FIG. **4**.

For example, in an alternate embodiment shown in FIG. **5**, an unshaped input signal **501** is routed to a pulse shaping module **502**. The pulse shaping module **502** modifies the unshaped input signal **501** to generate a (modified) input signal **302** (designated as the "Control Signal" in FIG. **5**). The input signal **302** is routed to the switch module **304**, which operates in the manner described above. Also, the filter **308** of FIG. **5** operates in the manner described above.

The purpose of the pulse shaping module **502** is to define the pulse width of the input signal **302**. Recall that the input signal **302** controls the opening and closing of the switch **406** in switch module **304**. During such operation, the pulse width of the input signal **302** establishes the pulse width of the harmonically rich signal **306**. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal **306** are a function of at least the pulse width of the harmonically rich signal **306**. As such, the pulse width of the input signal **302** contributes to setting the relative amplitudes of the harmonics of harmonically rich signal **306**.

Further details of up-conversion as described in this section are presented in pending U.S. application "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed Oct. 21, 1998, incorporated herein by reference in its entirety.

4. Enhanced Signal Reception

The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same.

Referring to FIG. **21**, transmitter **2104** accepts a modulating baseband signal **2102** and generates (transmitted)

redundant spectrums **2106***a–n*, which are sent over communications medium **2108**. Receiver **2112** recovers a demodulated baseband signal **2114** from (received) redundant spectrums **2110***a–n*. Demodulated baseband signal **2114** is representative of the modulating baseband signal **2102**, where the level of similarity between the modulating baseband signal **2114** and the modulating baseband signal **2102** is application dependent.

Modulating baseband signal **2102** is preferably any information signal desired for transmission and/or reception. An example modulating baseband signal **2202** is illustrated in FIG. **22**A, and has an associated modulating baseband spectrum **2204** and image spectrum **2203** that are illustrated in FIG. **22**B. Modulating baseband signal **2202** is illustrated as an analog signal in FIG. **22***a*, but could also be a digital signal, or combination thereof. Modulating baseband signal **2202** could be a voltage (or current) characterization of any number of real world occurrences, including for example and without limitation, the voltage (or current) representation for a voice signal.

Each transmitted redundant spectrum **2106***a–n* contains the necessary information to substantially reconstruct the modulating baseband signal **2102**. In other words, each redundant spectrum **2106***a–n* contains the necessary amplitude, phase, and frequency information to reconstruct the modulating baseband signal **2102**.

FIG. **22**C illustrates example transmitted redundant spectrums **2206***b–d*. Transmitted redundant spectrums **2206***b–d* are illustrated to contain three redundant spectrums for illustration purposes only. Any number of redundant spectrums could be generated and transmitted as will be explained in following discussions.

Transmitted redundant spectrums **2206***b–d* are centered at f_1, with a frequency spacing f_2 between adjacent spectrums. Frequencies f_1 and f_2 are dynamically adjustable in real-time as will be shown below. FIG. **22**D illustrates an alternate embodiment, where redundant spectrums **2208***c,d* are centered on unmodulated oscillating signal **2209** at f_1 (Hz). Oscillating signal **2209** may be suppressed if desired using, for example, phasing techniques or filtering techniques. Transmitted redundant spectrums are preferably above baseband frequencies as is represented by break **2205** in the frequency axis of FIGS. **22**C and **22**D.

Received redundant spectrums **2110***a–n* are substantially similar to transmitted redundant spectrums **2106***a–n*, except for the changes introduced by the communications medium **2108**. Such changes can include but are not limited to signal attenuation, and signal interference. FIG. **22**E illustrates example received redundant spectrums **2210***b–d*. Received redundant spectrums **2210***b–d* are substantially similar to transmitted redundant spectrums **2206***b–d*, except that redundant spectrum **2210***c* includes an undesired jamming signal spectrum **2211** in order to illustrate some advantages of the present invention. Jamming signal spectrum **2211** is a frequency spectrum associated with a jamming signal. For purposes of this invention, a "jamming signal" refers to any unwanted signal, regardless of origin, that may interfere with the proper reception and reconstruction of an intended signal. Furthermore, the jamming signal is not limited to tones as depicted by spectrum **2211**, and can have any spectral shape, as will be understood by those skilled in the art(s).

As stated above, demodulated baseband signal **2114** is extracted from one or more of received redundant spectrums **2210***b–d*. FIG. **22**F illustrates example demodulated baseband signal **2212** that is, in this example, substantially similar to modulating baseband signal **2202** (FIG. **22**A); where in practice, the degree of similarity is application dependent.

An advantage of the present invention should now be apparent. The recovery of modulating baseband signal **2202** can be accomplished by receiver **2112** in spite of the fact that high strength jamming signal(s) (e.g. jamming signal spectrum **2211**) exist on the communications medium. The intended baseband signal can be recovered because multiple redundant spectrums are transmitted, where each redundant spectrum carries the necessary information to reconstruct the baseband signal. At the destination, the redundant spectrums are isolated from each other so that the baseband signal can be recovered even if one or more of the redundant spectrums are corrupted by a jamming signal.

Transmitter **2104** will now be explored in greater detail. FIG. **23**A illustrates transmitter **2301**, which is one embodiment of transmitter **2104** that generates redundant spectrums configured similar to redundant spectrums **2206***b–d*. Transmitter **2301** includes generator **2303**, optional spectrum processing module **2304**, and optional medium interface module **2320**. Generator **2303** includes: first oscillator **2302**, second oscillator **2309**, first stage modulator **2306**, and second stage modulator **2310**.

Transmitter **2301** operates as follows. First oscillator **2302** and second oscillator **2309** generate a first oscillating signal **2305** and second oscillating signal **2312**, respectively. First stage modulator **2306** modulates first oscillating signal **2305** with modulating baseband signal **2202**, resulting in modulated signal **2308**. First stage modulator **2306** may implement any type of modulation including but not limited to: amplitude modulation, frequency modulation, phase modulation, combinations thereof, or any other type of modulation. Second stage modulator **2310** modulates modulated signal **2308** with second oscillating signal **2312**, resulting in multiple redundant spectrums **2206***a–n* shown in FIG. **23**B. Second stage modulator **2310** is preferably a phase modulator, or a frequency modulator, although other types of modulation may be implemented including but not limited to amplitude modulation. Each redundant spectrum **2206***a–n* contains the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal **2202**.

Redundant spectrums **2206***a–n* are substantially centered around f_1, which is the characteristic frequency of first oscillating signal **2305**. Also, each redundant spectrum **2206***a–n* (except for **2206***c*) is offset from f_1 by approximately a multiple of f_2 (Hz), where f_2 is the frequency of the second oscillating signal **2312**. Thus, each redundant spectrum **2206***a–n* is offset from an adjacent redundant spectrum by f_2 (Hz). This allows the spacing between adjacent redundant spectrums to be adjusted (or tuned) by changing f_2 that is associated with second oscillator **2309**. Adjusting the spacing between adjacent redundant spectrums allows for dynamic real-time tuning of the bandwidth occupied by redundant spectrums **2206***a–n*.

In one embodiment, the number of redundant spectrums **2206***a–n* generated by transmitter **2301** is arbitrary and may be unlimited as indicated by the "a–n" designation for redundant spectrums **2206***a–n*. However, a typical communications medium will have a physical and/or administrative limitations (i.e. FCC regulations) that restrict the number of redundant spectrums that can be practically transmitted over the communications medium. Also, there may be other reasons to limit the number of redundant spectrums transmitted. Therefore, preferably, the transmitter **2301** will include an optional spectrum processing module **2304** to process the redundant spectrums **2206***a–n* prior to transmission over communications medium **2108**.

In one embodiment, spectrum processing module **2304** includes a filter with a passband **2207** (FIG. **23**C) to select

redundant spectrums **2206***b–d* for transmission. This will substantially limit the frequency bandwidth occupied by the redundant spectrums to the passband **2207**. In one embodiment, spectrum processing module **2304** also up converts redundant spectrums and/or amplifies redundant spectrums prior to transmission over the communications medium **2108**. Finally, medium interface module **2320** transmits redundant spectrums over the communications medium **2108**. In one embodiment, communications medium **2108** is an over-the-air link and medium interface module **2320** is an antenna. Other embodiments for communications medium **2108** and medium interface module **2320** will be understood based on the teachings contained herein.

FIG. **23**D illustrates transmitter **2321**, which is one embodiment of transmitter **2104** that generates redundant spectrums configured similar to redundant spectrums **2208***c–d* and unmodulated spectrum **2209**. Transmitter **2321** includes generator **2311**, spectrum processing module **2304**, and (optional) medium interface module **2320**. Generator **2311** includes: first oscillator **2302**, second oscillator **2309**, first stage modulator **2306**, and second stage modulator **2310**.

As shown in FIG. **23**D, many of the components in transmitter **2321** are similar to those in transmitter **2301**. However, in this embodiment, modulating baseband signal **2202** modulates second oscillating signal **2312**. Transmitter **2321** operates as follows. First stage modulator **2306** modulates second oscillating signal **2312** with modulating baseband signal **2202**, resulting in modulated signal **2322**. As described earlier, first stage modulator **2306** can effect any type of modulation including but not limited to: amplitude modulation frequency modulation, combinations thereof, or any other type of modulation. Second stage modulator **2310** modulates first oscillating signal **2304** with modulated signal **2322**, resulting in redundant spectrums **2208***a–n*, as shown in FIG. **23**E. Second stage modulator **2310** is preferably a phase or frequency modulator, although other modulators could used including but not limited to an amplitude modulator.

Redundant spectrums **2208***a–n* are centered on unmodulated spectrum **2209** (at f_1 Hz), and adjacent spectrums are separated by f_2 Hz. The number of redundant spectrums **2208***a–n* generated by generator **2311** is arbitrary and unlimited, similar to spectrums **2206***a–n* discussed above. Therefore, optional spectrum processing module **2304** may also include a filter with passband **2325** to select, for example, spectrums **2208***c,d* for transmission over communications medium **2108**. In addition, optional spectrum processing module **2304** may also include a filter (such as a bandstop filter) to attenuate unmodulated spectrum **2209**. Alternatively, unmodulated spectrum **2209** may be attenuated by using phasing techniques during redundant spectrum generation. Finally, (optional) medium interface module **2320** transmits redundant spectrums **2208***c,d* over communications medium **2108**.

Receiver **2112** will now be explored in greater detail to illustrate recovery of a demodulated baseband signal from received redundant spectrums. FIG. **24**A illustrates receiver **2430**, which is one embodiment of receiver **2112**. Receiver **2430** includes optional medium interface module **2402**, down-converter **2404**, spectrum isolation module **2408**, and data extraction module **2414**. Spectrum isolation module **2408** includes filters **2410***a–c*. Data extraction module **2414** includes demodulators **2416***a–c*, error check modules **2420***a–c*, and arbitration module **2424**. Receiver **2430** will be discussed in relation to the signal diagrams in FIGS. **24**B–**24**J.

In one embodiment, optional medium interface module **2402** receives redundant spectrums **2210***b–d* (FIG. **22**E, and FIG. **24**B). Each redundant spectrum **2210***b–d* includes the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal used to generated the redundant spectrums. However, in the present example, spectrum **2210***c* also contains jamming signal **2211**, which may interfere with the recovery of a baseband signal from spectrum **2210***c*. Down-converter **2404** down-converts received redundant spectrums **2210***b–d* to lower intermediate frequencies, resulting in redundant spectrums **2406***a–c* (FIG. **24**C). Jamming signal **2211** is also down-converted to jamming signal **2407**, as it is contained within redundant spectrum **2406***b*. Spectrum isolation module **2408** includes filters **2410***a–c* that isolate redundant spectrums **2406***a–c* from each other (FIGS. **24**D–**24**F, respectively). Demodulators **2416***a–c* independently demodulate spectrums **2406***a–c*, resulting in demodulated baseband signals **2418***a–c*, respectively (FIGS. **24**G–**241**). Error check modules **2420***a–c* analyze demodulate baseband signal **2418***a–c* to detect any errors. In one embodiment, each error check module **2420***a–c* sets an error flag **2422***a–c* whenever an error is detected in a demodulated baseband signal. Arbitration module **2424** accepts the demodulated baseband signals and associated error flags, and selects a substantially error-free demodulated baseband signal (FIG. **24**J). In one embodiment, the substantially error-free demodulated baseband signal will be substantially similar to the modulating baseband signal used to generate the received redundant spectrums, where the degree of similarity is application dependent.

Referring to FIGS. **24**G–I, arbitration module **2424** will select either demodulated baseband signal **2418***a* or **2418***c*, because error check module **2420***b* will set the error flag **2422***b* that is associated with demodulated baseband signal **2418***b*.

The error detection schemes implemented by the error detection modules include but are not limited to: cyclic redundancy check (CRC) and parity check for digital signals, and various error detections schemes for analog signal.

Further details of enhanced signal reception as described in this section are presented in pending U.S. application "Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,061,555 on May 9, 2000.

5. Unified Down-Conversion and Filtering

The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

FIG. **17** is a conceptual block diagram of a UDF module **1702** according to an embodiment of the present invention. The UDF module **1702** performs at least frequency translation and frequency selectivity.

The effect achieved by the UDF module **1702** is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module **1702** effectively performs input filtering.

According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals **1704** received by the UDF module **1702** are at radio frequencies. The UDF module **1702** effectively operates to input filter these RF input signals **1704**. Specifically, in these embodiments, the UDF module **1702** effectively performs input, channel select filtering of the RF input signal **1704**. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module **1702** effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module **1702** includes a frequency translator **1708**. The frequency translator **1708** conceptually represents that portion of the UDF module **1702** that performs frequency translation (down conversion).

The UDF module **1702** also conceptually includes an apparent input filter **1706** (also sometimes called an input filtering emulator). Conceptually, the apparent input filter **1706** represents that portion of the UDF module **1702** that performs input filtering.

In practice, the input filtering operation performed by the UDF module **1702** is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter **1706** is herein referred to as an "apparent" input filter **1706**.

The UDF module **1702** of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module **1702**. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module **1702** can be designed with a filter center frequency f_c on the order of 900 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_c of the UDF module **1702** can be electrically adjusted, either statically or dynamically.

Also, the UDF module **1702** can be designed to amplify input signals.

Further, the UDF module **1702** can be implemented without large resistors, capacitors, or inductors. Also, the UDF module **1702** does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module **1702** is friendly to integrated circuit design techniques and processes.

The features and advantages exhibited by the UDF module **1702** are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module **1702** performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and samples/instances of the output signal.

More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

Next, the input sample is held (that is, delayed).

Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

FIG. **19** illustrates an example implementation of the unified down-converting and filtering (UDF) module **1922**. The UDF module **1922** performs the frequency translation operation and the frequency selectivity operation in an integrated, unified manner as described above, and as further described below.

In the example of FIG. **19**, the frequency selectivity operation performed by the UDF module **1922** comprises a band-pass filtering operation according to EQ. 1, below, which is an example representation of a band-pass filtering transfer function.

$$VO=\alpha_1 z^{-1} VI-\beta_1 z^{-1} VO-\beta_0 z^{-2} VO \qquad \text{EQ. 1}$$

It should be noted, however, that the invention is not limited to band-pass filtering. Instead, the invention effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof. As will be appreciated, there are many representations of any given filter type. The invention is applicable to these filter representations. Thus, EQ. 1 is referred to herein for illustrative purposes only, and is not limiting.

The UDF module **1922** includes a down-convert and delay module **1924**, first and second delay modules **1928** and **1930**, first and second scaling modules **1932** and **1934**, an output sample and hold module **1936**, and an (optional) output smoothing module **1938**. Other embodiments of the UDF module will have these components in different

configurations, and/or a subset of these components, and/or additional components. For example, and without limitation, in the configuration shown in FIG. **19**, the output smoothing module **1938** is optional.

As further described below, in the example of FIG. **19**, the down-convert and delay module **1924** and the first and second delay modules **1928** and **1930** include switches that are controlled by a clock having two phases, ϕ_1 and ϕ_2. ϕ_1 and ϕ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low.

Preferably, each of these switches closes on a rising edge of ϕ_1 or ϕ_2, and opens on the next corresponding falling edge of ϕ_1 or ϕ_2. However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. **19**, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module **1924** is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The example UDF module **1922** has a filter center frequency of 900.2 MHZ and a filter bandwidth of 570 KHz. The pass band of the UDF module **1922** is on the order of 899.915 MHZ to 900.485 MHZ. The Q factor of the UDF module **1922** is approximately 1879 (i.e., 900.2 MHZ divided by 570 KHz).

The operation of the UDF module **1922** shall now be described with reference to a Table **1802** (FIG. **18**) that indicates example values at nodes in the UDF module **1922** at a number of consecutive time increments. It is assumed in Table **1802** that the UDF module **1922** begins operating at time t−1. As indicated below, the UDF module **1922** reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

At the rising edge of ϕ_1 at time t−1, a switch **1950** in the down-convert and delay module **1924** closes. This allows a capacitor **1952** to charge to the current value of an input signal, VI_{t-1}, such that node **1902** is at VI_{t-1}. This is indicated by cell **1804** in FIG. **18**. In effect, the combination of the switch **1950** and the capacitor **1952** in the down-convert and delay module **1924** operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor **1952** represents an instance of a down-converted image of the input signal VI.

The manner in which the down-convert and delay module **1924** performs frequency down-conversion is further described elsewhere in this application, and is additionally described in pending U.S. application "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,061,551 on May 9, 2000, which is herein incorporated by reference in its entirety.

Also at the rising edge of ϕ_1 at time t−1, a switch **1958** in the first delay module **1928** closes, allowing a capacitor **1960** to charge to VO_{t-1}, such that node **1906** is at VO_{t-1}. This is indicated by cell **1806** in Table **1802**. (In practice, VO_{t-1} is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

Also at the rising edge of ϕ_1 at time t−1, a switch **1966** in the second delay module **1930** closes, allowing a capacitor **1968** to charge to a value stored in a capacitor **1964**. At this time, however, the value in capacitor **1964** is undefined, so the value in capacitor **1968** is undefined. This is indicated by cell **1807** in table **1802**.

At the rising edge of ϕ_2 at time t−1, a switch **1954** in the down-convert and delay module **1924** closes, allowing a capacitor **1956** to charge to the level of the capacitor **1952**. Accordingly, the capacitor **1956** charges to VI_{t-1}, such that node **1904** is at VI_{t-1}. This is indicated by cell **1810** in Table **1802**.

The UDF module **1922** may optionally include a unity gain module **1990**A between capacitors **1952** and **1956**. The unity gain module **1990**A operates as a current source to enable capacitor **1956** to charge without draining the charge from capacitor **1952**. For a similar reason, the UDF module **1922** may include other unity gain modules **1990**B–**1990**G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules **1990**A–**1990**G are optional. The structure and operation of the unity gain modules **1990** will be apparent to persons skilled in the relevant art(s).

Also at the rising edge of ϕ_2 at time t−1, a switch **1962** in the first delay module **1928** closes, allowing a capacitor **1964** to charge to the level of the capacitor **1960**. Accordingly, the capacitor **1964** charges to VO_{t-1}, such that node **1908** is at VO_{t-1}. This is indicated by cell **1814** in Table **1802**.

Also at the rising edge of ϕ_2 at time t−1, a switch **1970** in the second delay module **1930** closes, allowing a capacitor **1972** to charge to a value stored in a capacitor **1968**. At this time, however, the value in capacitor **1968** is undefined, so the value in capacitor **1972** is undefined. This is indicated by cell **1815** in table **1802**.

At time t, at the rising edge of ϕ_1, the switch **1950** in the down-convert and delay module **1924** closes. This allows the capacitor **1952** to charge to VI_t, such that node **1902** is at VI_t. This is indicated in cell **1816** of Table **1802**.

Also at the rising edge of ϕ_1 at time t, the switch **1958** in the first delay module **1928** closes, thereby allowing the capacitor **1960** to charge to VO_t. Accordingly, node **1906** is at VO_t. This is indicated in cell **1820** in Table **1802**.

Further at the rising edge of ϕ_1 at time t, the switch **1966** in the second delay module **1930** closes, allowing a capacitor **1968** to charge to the level of the capacitor **1964**. Therefore, the capacitor **1968** charges to VO_{t-1}, such that node **1910** is at VO_{t-1}. This is indicated by cell **1824** in Table **1802**.

At the rising edge of ϕ_2 at time t, the switch **1954** in the down-convert and delay module **1924** closes, allowing the capacitor **1956** to charge to the level of the capacitor **1952**. Accordingly, the capacitor **1956** charges to VI_t, such that node **1904** is at VI_t. This is indicated by cell **1828** in Table **1802**.

Also at the rising edge of ϕ_2 at time t, the switch **1962** in the first delay module **1928** closes, allowing the capacitor **1964** to charge to the level in the capacitor **1960**. Therefore, the capacitor **1964** charges to VO_t, such that node **1908** is at VO_t. This is indicated by cell **1832** in Table **1802**.

Further at the rising edge of ϕ_2 at time t, the switch **1970** in the second delay module **1930** closes, allowing the capacitor **1972** in the second delay module **1930** to charge to the level of the capacitor **1968** in the second delay module

1930. Therefore, the capacitor 1972 charges to VO_{t-1}, such that node 1912 is at VO_{t-1}. This is indicated in cell 1836 of FIG. 18.

At time t+1, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes, allowing the capacitor 1952 to charge to VI_{t+1}. Therefore, node 1902 is at VI_{t+1}, as indicated by cell 1838 of Table 1802.

Also at the rising edge of ϕ_1 at time t+1, the switch 1958 in the first delay module 1928 closes, allowing the capacitor 1960 to charge to VO_{t+1}. Accordingly, node 1906 is at VO_{t+1}, as indicated by cell 1842 in Table 1802.

Further at the rising edge of ϕ_1 at time t+1, the switch 1966 in the second delay module 1930 closes, allowing the capacitor 1968 to charge to the level of the capacitor 1964. Accordingly, the capacitor 1968 charges to VO_t, as indicated by cell 1846 of Table 1802.

In the example of FIG. 19, the first scaling module 1932 scales the value at node 1908 (i.e., the output of the first delay module 1928) by a scaling factor of −0.1. Accordingly, the value present at node 1914 at time t+1 is $-0.1*VO_t$. Similarly, the second scaling module 1934 scales the value present at node 1912 (i.e., the output of the second scaling module 1930) by a scaling factor of −0.8. Accordingly, the value present at node 1916 is $-0.8*VO_{t-1}$ at time t+1.

At time t+1, the values at the inputs of the summer 1926 are: VI_t at node 1904, $-0.1*VO_t$ at node 1914, and $-0.8*VO_{t-1}$ at node 1916 (in the example of FIG. 19, the values at nodes 1914 and 1916 are summed by a second summer 1925, and this sum is presented to the summer 1926). Accordingly, at time t+1, the summer generates a signal equal to $VI_t-0.1*VO_t-0.8*VO_{t-1}$.

At the rising edge of ϕ_1 at time t+1, a switch 1991 in the output sample and hold module 1936 closes, thereby allowing a capacitor 1992 to charge to VO_{t+1}. Accordingly, the capacitor 1992 charges to VO_{t+1}, which is equal to the sum generated by the adder 1926. As just noted, this value is equal to: $VI_t-0.1*VO_t-0.8*VO_{t-1}$. This is indicated in cell 1850 of Table 1802. This value is presented to the optional output smoothing module 1938, which smooths the signal to thereby generate the instance of the output signal VO_{t+1}. It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. 1.

Further details of unified down-conversion and filtering as described in this section are presented in pending U.S. application "Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,049,706 on Apr. 11, 2000, incorporated herein by reference in its entirety.

6. Example Application Embodiments of the Invention

As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

Example applications of the UFT module were described above. In particular, frequency down-conversion, frequency up-conversion, enhanced signal reception, and unified down-conversion and filtering applications of the UFT module were summarized above, and are further described below. These applications of the UFT module are discussed herein for illustrative purposes. The invention is not limited to these example applications. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s), based on the teachings contained herein.

For example, the present invention can be used in applications that involve frequency down-conversion. This is shown in FIG. 1C, for example, where an example UFT module 115 is used in a down-conversion module 114. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal. This is also shown in FIG. 7, for example, where an example UFT module 706 is part of a down-conversion module 704, which is part of a receiver 702.

The present invention can be used in applications that involve frequency up-conversion. This is shown in FIG. 1D, for example, where an example UFT module 117 is used in a frequency up-conversion module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal. This is also shown in FIG. 8, for example, where an example UFT module 806 is part of up-conversion module 804, which is part of a transmitter 802.

The present invention can be used in environments having one or more transmitters 902 and one or more receivers 906, as illustrated in FIG. 9. In such environments, one or more of the transmitters 902 may be implemented using a UFT module, as shown for example in FIG. 8. Also, one or more of the receivers 906 may be implemented using a UFT module, as shown for example in FIG. 7.

The invention can be used to implement a transceiver. An example transceiver 1002 is illustrated in FIG. 10. The transceiver 1002 includes a transmitter 1004 and a receiver 1008. Either the transmitter 1004 or the receiver 1008 can be implemented using a UFT module. Alternatively, the transmitter 1004 can be implemented using a UFT module 1006, and the receiver 1008 can be implemented using a UFT module 1010. This embodiment is shown in FIG. 10.

Another transceiver embodiment according to the invention is shown in FIG. 11. In this transceiver 1102, the transmitter 1104 and the receiver 1108 are implemented using a single UFT module 1106. In other words, the transmitter 1104 and the receiver 1108 share a UFT module 1106.

As described elsewhere in this application, the invention is directed to methods and systems for enhanced signal reception (ESR). Various ESR embodiments include an ESR module (transmit) in a transmitter 1202, and an ESR module (receive) in a receiver 1210. An example ESR embodiment configured in this manner is illustrated in FIG. 12.

The ESR module (transmit) 1204 includes a frequency up-conversion module 1206. Some embodiments of this frequency up-conversion module 1206 may be implemented using a UFT module, such as that shown in FIG. 1D.

The ESR module (receive) 1212 includes a frequency down-conversion module 1214. Some embodiments of this frequency down-conversion module 1214 may be implemented using a UFT module, such as that shown in FIG. 1C.

As described elsewhere in this application, the invention is directed to methods and systems for unified down-conversion and filtering (UDF). An example unified down-conversion and filtering module 1302 is illustrated in FIG. 13. The unified down-conversion and filtering module 1302 includes a frequency down-conversion module 1304 and a filtering module 1306. According to the invention, the frequency down-conversion module 1304 and the filtering module 1306 are implemented using a UFT module 1308, as indicated in FIG. 13.

Unified down-conversion and filtering according to the invention is useful in applications involving filtering and/or frequency down-conversion. This is depicted, for example, in FIGS. 15A–15F. FIGS. 15A–15C indicate that unified down-conversion and filtering according to the invention is useful in applications where filtering precedes, follows, or both precedes and follows frequency down-conversion. FIG.

15D indicates that a unified down-conversion and filtering module **1524** according to the invention can be utilized as a filter **1522** (i.e., where the extent of frequency down-conversion by the down-converter in the unified down-conversion and filtering module **1524** is minimized). FIG. **15**E indicates that a unified down-conversion and filtering module **1528** according to the invention can be utilized as a down-converter **1526** (i.e., where the filter in the unified down-conversion and filtering module **1528** passes substantially all frequencies). FIG. **15**F illustrates that the unified down-conversion and filtering module **1532** can be used as an amplifier. It is noted that one or more UDF modules can be used in applications that involve at least one or more of filtering, frequency translation, and amplification.

For example, receivers, which typically perform filtering, down-conversion, and filtering operations, can be implemented using one or more unified down-conversion and filtering modules. This is illustrated, for example, in FIG. **14**.

The methods and systems of unified down-conversion and filtering of the invention have many other applications. For example, as discussed herein, the enhanced signal reception (ESR) module (receive) operates to down-convert a signal containing a plurality of spectrums. The ESR module (receive) also operates to isolate the spectrums in the down-converted signal, where such isolation is implemented via filtering in some embodiments. According to embodiments of the invention, the ESR module (receive) is implemented using one or more unified down-conversion and filtering (UDF) modules. This is illustrated, for example, in FIG. **16**. In the example of FIG. **16**, one or more of the UDF modules **1610**, **1612**, **1614** operates to down-convert a received signal. The UDF modules **1610**, **1612**, **1614** also operate to filter the down-converted signal so as to isolate the spectrum(s) contained therein. As noted above, the UDF modules **1610**, **1612**, **1614** are implemented using the universal frequency translation (UFT) modules of the invention.

The invention is not limited to the applications of the UFT module described above. For example, and without limitation, subsets of the applications (methods and/or structures) described herein (and others that would be apparent to persons skilled in the relevant art(s) based on the herein teachings) can be associated to form useful combinations.

For example, transmitters and receivers are two applications of the UFT module. FIG. **10** illustrates a transceiver **1002** that is formed by combining these two applications of the UFT module, i.e., by combining a transmitter **1004** with a receiver **1008**.

Also, ESR (enhanced signal reception) and unified down-conversion and filtering are two other applications of the UFT module. FIG. **16** illustrates an example where ESR and unified down-conversion and filtering are combined to form a modified enhanced signal reception system.

The invention is not limited to the example applications of the UFT module discussed herein. Also, the invention is not limited to the example combinations of applications of the UFT module discussed herein. These examples were provided for illustrative purposes only, and are not limiting. Other applications and combinations of such applications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion; (4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals.

Additional example applications are described below.

6.1 Data Communication

The invention is directed to data communication among data processing devices. For example, and without limitation, the invention is directed to computer networks such as, for example, local area networks (LANs), wide area networks (WANs), including wireless LANs (WLANs) and wireless WANs, modulator/demodulators (modems), including wireless modems, etc.

FIG. **25** illustrates an example environment **2502** wherein computers **2504**, **2512**, and **2526** communicate with one another via a computer network **2534**. It is noted that the invention is not limited to computers, but encompasses any data processing and/or communications device or other device where communications with external devices is desired. Also, the invention includes but si not limited to WLAN client (also called mobile terminals, and/or stations) and infrastructure devices (also called access points). In the example of FIG. **25**, computer **2504** is communicating with the network **2534** via a wired link, whereas computers **2512** and **2526** are communicating with the network **2534** via wireless links.

In the teachings contained herein, for illustrative purposes, a link may be designated as being a wired link or a wireless link. Such designations are for example purposes only, and are not limiting. A link designated as being wireless may alternatively be wired. Similarly, a link designated as being wired may alternatively be wireless. This is applicable throughout the entire application.

The computers **2504**, **2512** and **2526** each include an interface **2506**, **2514**, and **2528**, respectively, for communicating with the network **2534**. The interfaces **2506**, **2514**, and **2528** include transmitters **2508**, **2516**, and **2530** respectively. Also, the interfaces **2506**, **2514** and **2528** include receivers **2510**, **2518**, and **2532** respectively. In embodiments of the invention, the transmitters **2508**, **2516** and **2530** are implemented using UFT modules for performing frequency up-conversion operations (see, for example, FIG. **8**). In embodiments, the receivers **2510**, **2518** and **2532** are implemented using UFT modules for performing frequency down-conversion operations (see, for example, FIG. **7**).

As noted above, the computers **2512** and **2526** interact with the network **2534** via wireless links. In embodiments of the invention, the interfaces **2514**, **2528** in computers **2512**, **2526** represent modulator/demodulators (modems).

In embodiments, the network **2534** includes an interface or modem **2520** for communicating with the modems **2514**, **2528** in the computers **2512**, **2526**. In embodiments, the interface **2520** includes a transmitter **2522**, and a receiver **2524**. Either or both of the transmitter **2522**, and the receiver **2524** are implemented using UFT modules for performing frequency translation operations (see, for example, FIGS. **7** and **8**).

In alternative embodiments, one or more of the interfaces **2506**, **2514**, **2520**, and **2528** are implemented using transceivers that employ one or more UFT modules for performing frequency translation operations (see, for example, FIGS. **10** and **11**).

FIG. **26** illustrates another example data communication embodiment **2602**. Each of a plurality of computers **2604**, **2612**, **2614** and **2616** includes an interface, such as an interface **2606** shown in the computer **2604**. It should be understood that the other computers **2612**, **2614**, **2616** also include an interface such as an interface **2606**. The computers **2604**, **2612**, **2614** and **2616** communicate with each other

via interfaces **2606** and wireless or wired links, thereby collectively representing a data communication network.

The interfaces **2606** may represent any computer interface or port, such as but not limited to a high speed internal interface, a wireless serial port, a wireless PS2 port, a wireless USB port, PCMCIA port, etc.

The interface **2606** includes a transmitter **2608** and a receiver **2610**. In embodiments of the invention, either or both of the transmitter **2608** and the receiver **2610** are implemented using UFT modules for frequency up-conversion and down-conversion (see, for example, FIGS. **7** and **8**). Alternatively, the interfaces **2806** can be implemented using a transceiver having one or more UFT modules for performing frequency translation operations (see, for example, FIGS. **10** and **11**).

FIGS. **33–38** illustrate other scenarios envisioned and encompassed by the invention. FIG. **33** illustrates a data processing environment **3302** wherein a wired network, such as an Ethernet network **3304**, is linked to another network, such as a WLAN **3306**, via a wireless link **3308**. The wireless link **3308** is established via interfaces **3310**, **3312** which are preferably implemented using universal frequency translation modules.

FIGS. **35–38** illustrate that the present invention supports WLANs that are located in one or more buildings or over any defined geographical area, as shown in FIGS. **35–38**.

The invention includes multiple networks linked together. The invention also envisions wireless networks conforming to any known or custom standard or specification. This is shown in FIG. **34**, for example, where any combination of WLANs conforming to any WLAN standard or configuration, such as IEEE 802.11 and Bluetooth (or other relatively short range communication specification or standard), any WAN cellular or telephone standard or specification, any type of radio links, any custom standard or specification, etc., or combination thereof, can be implemented using the universal frequency translation technology described herein. Also, any combination of these networks may be coupled together, as illustrated in FIG. **34**.

The invention supports WLANs that are located in one or multiple buildings, as shown in FIGS. **35** and **36**. The invention also supports WLANs that are located in an area including and external to one or more buildings, as shown in FIG. **37**. In fact, the invention is directed to networks that cover any defined geographical area, as shown in FIG. **38**. In the embodiments described above, wireless links are preferably established using WLAN interfaces as described herein.

More generally, the invention is directed to WLAN client devices and WLAN infrastructure devices. "WLAN Client Devices" refers to, for example, any data processing and/or communication devices in which wired or wireless communication functionality is desired, such as but not limited to computers, personal data assistants (PDAs), automatic identification data collection devices (such as bar code scanners/readers, electronic article surveillance readers, and radio frequency identification readers), telephones, network devices, etc., and combinations thereof. "WLAN Infrastructure Devices" refers to, for example, Access Points and other devices used to provide the ability for WLAN Client Devices (as well as potentially other devices) to connect to wired and/or wireless networks and/or to provide the network functionality of a WLAN. "WLAN" refers to, for example, a Wireless Local Area Network that is implemented according to and that operates within WLAN standards and/or specifications, such as but not limited to IEEE 802.11, IEEE 802.11a, IEEE 802.11b, HomeRF, Proxim Range LAN, Proxim Range LAN2, Symbol Spectrum 1, Symbol Spectrum 24 as it existed prior to adoption of IEEE 802.11, HiperLAN1, or HiperLAN2. WLAN client devices and/or WLAN infrastructure devices may operate in a multi-mode capacity. For example, a device may include WLAN and WAN functionality. Another device may include WLAN and short range communication (such as but not limited to Blue Tooth) functionality. Another device may include WLAN and WAN and short range communication functionality. It is noted that the above definitions and examples are provided for illustrative purposes, and are not limiting. Equivalents to that described above will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.1.1. Example Implementations: Interfaces, Wireless Modems, Wireless LANs, etc.

The present invention is now described as implemented in an interface, such as a wireless modem or other device (such as client or infrastructure device), which can be utilized to implement or interact with a wireless local area network (WLAN) or wireless wide area network (WWAN), for example. In an embodiment, the present invention is implemented in a WLAN to support IEEE WLAN Standard 802.11, but this embodiment is mentioned for illustrative purposes only. The invention is not limited to this standard.

Conventional wireless modems are described in, for example, U.S. Pat. No. 5,764,693, titled, "Wireless Radio Modem with Minimal Inter-Device RF Interference," incorporated herein by reference in its entirety. The present invention replaces a substantial portion of conventional wireless modems with one or more universal frequency translators (UFTs). The resultant improved wireless modem consumes less power that conventional wireless modems and is easier and less expensive to design and build. A wireless modem in accordance with the present invention can be implemented in a PC-MCIA card or within a main housing of a computer, for example.

FIG. **27** illustrates an example block diagram of a computer system **2710**, which can be wirelessly coupled to a LAN, as illustrated in FIGS. **25** and **26**. The computer system **2710** includes an interface **2714** and an antenna **2712**. The interface **2714** includes a transmitter module **2716** that receives information from a digital signal processor (DSP) **2720**, and modulates and up-converts the information for transmission from the antenna **2712**. The interface **2714** also includes a receiver module **2718** that receives modulated carrier signals via the antenna **2712**. The receiver module **2718** down-converts and demodulates the modulated carrier signals to baseband information, and provides the baseband information to the DSP **2720**. The DSP **2720** can include a central processing unit (CPU) and other components of the computer **2712**. Conventionally, the interface **2714** is implemented with heterodyne components.

FIG. **28** illustrates an example interface **2810** implemented with heterodyne components. The interface **2810** includes a transmitter module **2812** and a receiver module **2824**. The receiver module **2824** includes an RF section **2830**, one or more IF sections **2828**, a demodulator section **2826**, an optional analog to digital (A/D) converter **2834**, and a frequency generator/synthesizer **2832**. The transmitter module **2812** includes an optional digital to analog (D/A) converter **2822**, a modulator \section **2818**, one or more IF sections **2816**, an RF section **2814**, and a frequency generator/synthesizer **2820**. Operation of the interface **2810** will be apparent to one skilled in the relevant art(s), based on the description herein.

FIG. **29** illustrates an example in-phase/quadrature-phase (I/Q) interface **2910** implemented with heterodyne compo-

nents. I/Q implementations allow two channels of information to be communicated on a carrier signal and thus can be utilized to increase data transmission.

The interface **2910** includes a transmitter module **2912** and a receiver module **2934**. The receiver module **2934** includes an RF section **2936**, one or more IF sections **2938**, an I/Q demodulator section **2940**, an optional A/D converter **2944**, and a frequency generator/synthesizer **2942**. The I/Q demodulator section **2940** includes a signal splitter **2946**, mixers **2948**, and a phase shifter **2950**. The signal splitter **2946** provides a received signal to the mixers **2948**. The phase shifter **2950** operates the mixers **2948** ninety degrees out of phase with one another to generate I and Q information channels **2952** and **2954**, respectively, which are provided to a DSP **2956** through the optional A/D converter **2944**.

The transmitter module **2912** includes an optional D/A converter **2922**, an I/Q modulator section **2918**, one or more IF sections **2916**, an RF section **2914**, and a frequency generator/synthesizer **2920**. The I/Q modulator section **2918** includes mixers **2924**, a phase shifter **2926**, and a signal combiner **2928**. The phase shifter **2926** operates the mixers **2924** ninety degrees out of phase with one another to generate I and Q modulated information signals **2930** and **2932**, respectively, which are combined by the signal combiner **2928**. The IF section(s) **2916** and RF section **2914** up-convert the combined I and Q modulated information signals **2930** and **2932** to RF for transmission by the antenna, in a manner well known in the relevant art(s).

Heterodyne implementations, such as those illustrated in FIGS. **28** and **29**, are expensive and difficult to design, manufacture and tune. In accordance with the present invention, therefore, the interface **2714** (FIG. **27**) is preferably implemented with one or more universal frequency translation (UFT) modules, such as the UFT module **102** (FIG. 1A). Thus previously described benefits of the present invention are obtained in wireless modems, WLANs, etc.

FIG. **30** illustrates an example block diagram embodiment of the interface **2714** that is associated with a computer or any other data processing and/or communications device. In FIG. **30**, the receiver module **2718** includes a universal frequency down-converter (UFD) module **3014** and an optional analog to digital (A/D) converter **3016**, which converts an analog output from the UFD **3014** to a digital format for the DSP **2720**. The transmitter module **2716** includes an optional modulator **3012** and a universal frequency up-converter (UFU) module **3010**. The optional modulator **3012** can be a variety of types of modulators, including conventional modulators. Alternatively, the UFU module **3010** includes modulator functionality. The example implementation of FIG. **30** operates substantially as described above and in co-pending U.S. Patent Applications titled, "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,061,551 on May 9, 2000, and "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,091,940 on Jul. 18, 2000, as well as other cited documents.

FIG. **31** illustrates an example implementation of the interface **2714** illustrated in FIG. **30**, wherein the receiver UFD **3014** includes a UFT module **3112**, and the transmitter UFU **3010** includes a universal frequency translation (UFT) module **3110**. This example implementation operates substantially as described above and in co-pending U.S. Patent Applications titled, "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,061,551 on May 9, 2000, and "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed Oct. 21, 1998, "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed Oct. 21, 1998, issued as U.S. Pat. No. 6,091,940 on Jul. 18, 2000, as well as other cited documents.

FIG. **32** illustrates an example I/Q implementation of the interface module **2710**. Other I/Q implementations are also contemplated and are within the scope of the present invention.

In the example of FIG. **32**, the receiver UFD module **3014** includes a signal divider **3228** that provides a received I/Q modulated carrier signal **3230** between a third UFT module **3224** and a fourth UFT module **3226**. A phase shifter **3232**, illustrated here as a 90 degree phase shifter, controls the third and fourth UFT modules **3224** and **3226** to operate 90 degrees out of phase with one another. As a result, the third and fourth UFT modules **3224** and **3226** down-convert and demodulate the received I/Q modulated carrier signal **3230**, and output I and Q channels **3234** and **3236**, respectively, which are provided to the DSP **2720** through the optional A/D converter **3016**.

In the example of FIG. **32**, the transmitter UFU module **3010** includes first and second UFT modules **3212** and **3214** and a phase shifter **3210**, which is illustrated here as a 90 degree phase shifter. The phase shifter **3210** receives a lower frequency modulated carrier signal **3238** from the modulator **3012**. The phase shifter **3210** controls the first and second UFT modules **3212** and **3214** to operate 90 degrees out of phase with one another. The first and second UFT modules **3212** and **3214** up-convert the lower frequency modulated carrier signal **3238**, which are output as higher frequency modulated I and Q carrier channels **3218** and **3220**, respectively. A signal combiner **3216** combines the higher frequency modulated I and Q carrier channels **3218** and **3220** into a single higher frequency modulated I/Q carrier signal **3222** for transmitting by the antenna **2712**.

The example implementations of the interfaces described above, and variations thereof, can also be used to implement network interfaces, such as the network interface **2520** illustrated in FIG. **25**.

6.1.2. Example Modifications

The RF modem applications, WLAN applications, etc., described herein, can be modified by incorporating one or more of the enhanced signal reception (ESR) techniques described herein. Use of ESR embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The RF modem applications, WLAN applications, etc., described herein can be enhanced by incorporating one or more of the unified down-conversion and filtering (UDF) techniques described herein. Use of UDF embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.2. Other Example Applications

The application embodiments described above are provided for purposes of illustration. These applications and embodiments are not intended to limit the invention. Alternate and additional applications and embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, such alternate and additional applications and embodiments include combinations of those described above. Such combinations will be apparent to persons skilled in the relevant art(s) based on the herein teachings.

7.0. Example WLAN Implementation Embodiments

7.1 Architecture

FIG. **39** is a block diagram of a WLAN interface **3902** (also referred to as a WLAN modem herein) according to an embodiment of the invention. The WLAN interface/modem **3902** includes an antenna **3904**, a low noise amplifier or power amplifier (LNA/PA) **3904**, a receiver **3906**, a transmitter **3910**, a control signal generator **3908**, a demodulator/modulator facilitation module **3912**, and a media access controller (MAC) interface **3914**. Other embodiments may include different elements. The MAC interface **3914** couples the WLAN interface/modem **3902** to a computer **3916** or other data processing device. The computer **3916** preferably includes a MAC **3918**.

The WLAN interface/modem **3902** represents a transmit and receive application that utilizes the universal frequency translation technology described herein. It also represents a zero IF (or direct-to-data) WLAN architecture.

The WLAN interface/modem **3902** also represents a vector modulator and a vector demodulator using the universal frequency translation (UFT) technology described herein. Use of the UFT technology enhances the flexibility of the WLAN application (i.e., makes it universal).

In the embodiment shown in FIG. **39**, the WLAN interface/modem **3902** is compliant with WLAN standard IEEE 802.11. However, the invention is not limited to this standard. The invention is applicable to any communication standard or specification, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein. Any modifications to the invention to operate with other standards or specifications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. **39**, the WLAN interface/modem **3902** provides half duplex communication. However, the invention is not limited to this communication mode. The invention is applicable and directed to other communication modes, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. **39**, the modulation/demodulation performed by the WLAN interface/modem **3902** is preferably direct sequence spread spectrum QPSK (quadrature phase shift keying) with differential encoding. However, the invention is not limited to this modulation/demodulation mode. The invention is applicable and directed to other modulation and demodulation modes, such as but not limited to those described herein, as well as frequency hopping according to IEEE 802.11, OFDM (orthogonal frequency division multiplexing), as well as others. These modulation/demodulation modes will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

The operation of the WLAN interface/modem **3902** when receiving shall now be described.

Signals **3922** received by the antenna **3903** are amplified by the LNA/PA **3904**. The amplified signals **3924** are down-converted and demodulated by the receiver **3906**. The receiver **3906** outputs I signal **3926** and Q signal **3928**.

FIG. **40** illustrates an example receiver **3906** according to an embodiment of the invention. It is noted that the receiver **3906** shown in FIG. **40** represents a vector modulator. The "receiving" function performed by the WLAN interface/modem **3902** can be considered to be all processing performed by the WLAN interface/modem **3902** from the LNA/PA **3904** to generation of baseband information.

Signal **3924** is split by a 90 degree splitter **4001** to produce an I signal **4006**A and Q signal **4006**B that are preferably 90 degrees apart in phase. I and Q signals **4006**A, **4006**B are down-converted by UFD (universal frequency down-conversion) modules **4002**A, **4002**B. The UDF modules **4002**A, **4002**B output down-converted I and Q signals **3926**, **3928**. The UFD modules **4002**A, **4002**B each includes at least one UFT (universal frequency translation) module **4004**A. UFD and UFT modules are described above. An example implementation of the receiver **3906** (vector demodulator) is shown in FIG. **53**. An example BOM list for the receiver **3906** of FIG. **53** is shown in FIG. **54**.

The demodulator/modulator facilitation module **3912** receives the I and Q signals **3926**, **3928**. The demodulator/modulator facilitation module **3912** amplifies and filters the I and Q signals **3926**, **3928**. The demodulator/modulator facilitation module **3912** also performs automatic gain control (AGC) functions. The AGC function is coupled with the universal frequency translation technology described herein. The demodulator/modulator facilitation module **3912** outputs processed I and Q signals **3930**, **3932**.

The MAC interface **3914** receives the processed I and Q signals **3930**, **3932**. The MAC interface **3914** preferably includes a baseband processor. The MAC interface **3914** preferably performs functions such as combining the I and Q signals **3930**, **3932**, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface **3914** and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The MAC interface **3914** outputs the baseband information signal, which is received and processed by the computer **3916** in an implementation and application specific manner.

In the example embodiment of FIG. **39**, the demodulation function is distributed among the receiver **3906**, the demodulator/modulator facilitation module **3912**, and a baseband processor contained in the MAC interface **3914**. The functions collectively performed by these components include, but are not limited to, despreading the information, differentially decoding the information, tracking the carrier phase, descrambling, recreating the data clock, and combining the I and Q signals. The invention is not limited to this arrangement. These demodulation-type functions can be centralized in a single component, or distributed in other ways.

The operation of the WLAN interface/modem **3902** when transmitting shall now be described.

A baseband information signal **3936** is received by the MAC interface **3914** from the computer **3916**. The MAC interface **3914** preferably performs functions such as splitting the baseband information signal to form I and Q signals **3930**, **3932**, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface **3914** and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The demodulator/modulator facilitation module **3912** filters and amplifies the I and Q signals **3930**, **3932**. The demodulator/modulator facilitation module **3912** outputs processed I and Q signals **3942**, **3944**. Preferably, at least some filtering and/or amplifying components in the demodulator/modulator facilitation module **3912** are used for both the transmit and receive paths.

The transmitter **3910** up-converts the processed I and Q signals **3942**, **3944**, and combines the up-converted I and Q signals. This up-converted/combined signal is amplified by the LNA/PA **3904**, and then transmitted via the antenna **3904**.

FIG. **41** illustrates an example transmitter **3910** according to an embodiment of the invention. The device in FIG. **41** can also be called a vector modulator. In an embodiment, the "transmit" function performed by the WLAN interface/modem **3902** can be considered to be all processing performed by the WLAN interface/modem **3902** from receipt of baseband information through the LNA/PA **3904**. An example implementation of the transmitter **3910** (vector modulator) is shown in FIGS. **57–60**. The data conditioning interfaces **5802** in FIG. **58** effectively pre-process the I and Q signals **3942**, **3944** before being received by the UFU modules **4102**. An example BOM list for the transmitter **3910** of FIGS. **57–60** is shown in FIGS. **61**A and **61**B.

I and Q signals **3942**, **3944** are received by UFU (universal frequency up-conversion) modules **4102**A, **4102**B. The UFU modules **4102**A, **4102**B each includes at least one UFT module **4104**A, **4104**B. The UFU modules **4102**A, **4102**B up-convert I and Q signals **3942**, **3944**. The UFU modules **4102**A, **4102**B output up-converted I and Q signals **4106**, **4108**. The 90 degree combiner **4110** effectively phase shifts either the I signal **4106** or the Q signal **4108** by 90 degrees, and then combines the phase shifted signal with the unshifted signal to generate a combined, up-converted I/Q signal **3946**.

In the example embodiment of FIG. **39**, the modulation function is distributed among the transmitter **3910**, the demodulator/modulator facilitation module **3912**, and a baseband processor contained in the MAC interface **3914**. The functions collectively performed by these components include, but are not limited to, differentially encoding data, splitting the baseband information signal into I and Q signals, scrambling data, and data spreading. The invention is not limited to this arrangement. These modulation-type functions can be centralized in a single component, or distributed in other ways.

An example implementation of the transmitter **3910** (vector modulator) is shown in FIGS. **57–60**. The data conditioning interfaces **5802** in FIG. **58** effectively pre-process the I and Q signals **3942**, **3944** before being received by the UFU modules **4102**. An example BOM list for the transmitter **3910** of FIGS. **57–60** is shown in FIGS. **61**A and **61**B.

The components in the WLAN interface/modem **3902** are preferably controlled by the MAC interface **3914** in operation with the MAC **3918** in the computer **3916**. This is represented by the distributed control arrow **3940** in FIG. **39**. Such control includes setting the frequency, data rate, whether receiving or transmitting, and other communication characteristics/modes that will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In embodiments, control signals are sent over the corresponding wireless medium and received by the antenna **3904**, and sent to the MAC **3918**.

FIG. **42** illustrates an example implementation of the WLAN interface/modem **3902**. It is noted that in this implementation example, the MAC interface **3914** is located on a different board. FIG. **62** is an example motherboard corresponding to FIG. **42**. FIG. **63** is an example bill-of-materials (BOM) list for the motherboard of FIG. **62**. This and other implementations are provided herein for example purposes only. Other implementations will be apparent to persons skilled in the relevant art(s), and the invention is directed to such other implementations.

FIG. **102** illustrates an alternate example PCMCIA test bed assembly for a WLAN interface/modem **3902** according to an embodiment of the invention. In this embodiment, the baseband processor **10202** is separate from the MAC interface **3914**.

In some applications, it is desired to separate the receive path and the transmit path. FIG. **43** illustrates an example receive implementation, and FIG. **44** illustrates an example transmit implementation.

7.2 Receiver

Example embodiments and implementations of the IQ receiver **3906** will be discussed as follows. The example embodiments and implementations include multi-phase embodiments that are useful for reducing or eliminating unwanted DC offsets and circuit re-radiation. The invention is not limited to these example receiver embodiments. Other receiver embodiments will be understood by those skilled in the relevant arts based on the discussion given herein. These other embodiments are within the scope and spirit of the present invention.

7.2.1 IQ Receiver

An example embodiment of the receiver **3906** is shown in FIG. **67**A. Referring to FIG. **67**A, the UFD module **4002**A (FIG. **40**) is configured so that the UFT module **4004**A is coupled to a storage module **6704**A. The UFT module **4004**A is a controlled switch **6702**A that is controlled by the control signal **3920**A. The storage module **6704**A is a capacitor **6706**A. However, other storage modules could be used including, an inductor, as will be understood by those skilled in the relevant arts. Likewise, the UFD module **4002**B (FIG. **40**) is configured so that the UFT module **4004**B is coupled to a storage module **6704**B. The UFT module **4004**B is a controlled switch **6702**B that is controlled by the control signal **3920**B. The storage module **6704**B is a capacitor **6706**B. However, other storage modules could be used including an inductor, as will be understood by those skilled in the relevant arts. The operation of the receiver **3906** is discussed as follows.

The 90 degree splitter **4001** receives the received signal **3924** from the LNA/PA module **3904**. The 90 degree splitter **4001** divides the signal **3924** into an I signal **4006**A and a Q signal **4006**B.

The UFD module **4002**A receives the I signal **4006**A and down-converts the I signal **4006**A using the control signal **3920**A to a lower frequency signal I **3926**. More specifically, the controlled switch **6702**A samples the I signal **4006**A according to the control signal **3920**A, transferring charge (or energy) to the storage module **6704**A. The charge stored during successive samples of the I signal **4006**A, results in the down-converted signal I signal **3926**. Likewise, UFD module **4002**B receives the Q signal **4006**B and down-converts the Q signal **4006**B using the control signal **3920**B to a lower frequency signal Q **3928**. More specifically, the controlled switch **6702**B samples the Q signal **4006**B according to the control signal **3920**B, resulting in charge (or energy) that is stored in the storage module **6704**B. The charge stored during successive samples of the I signal **4006**A, results in the down-converted signal Q signal **3928**.

Down-conversion utilizing a UFD module (also called an aliasing module) is further described in the above referenced applications, such as "Method and System for Down-converting Electromagnetic Signals," Ser. No. 09/176,022, now U.S. Pat. No. 6,061,551. As discussed in the '551 patent, the control signals **3920**A, B can be configured as a plurality of pulses that are established to improve energy transfer from the signals **4006**A, B to the down-converted signals **3926** and **3928**, respectively. In other words, the pulse widths of the control signals **3920** can be adjusted to increase and/or optimize the energy transfer from the signals **4006** to the down-converted output signals **3926** and **3938**, respectively. Additionally, matched filter principles can be implemented to shape the sampling pulses of the control

signal **3920**, and therefore further improve energy transfer to the down-converted output signal **3106**. Matched filter principle and energy transfer are further described in the above referenced applications, such as U.S. patent application titled, "Method and System for Down-Converting an Electromagnetic Signal, Transforms For Same, and Aperture Relationships", Ser. No. 09/550,644, filed on Apr. 14, 2000.

The configuration of the UFT based receiver **3906** is flexible. In FIG. **67**A, the controlled switches **6702** are in a series configuration relative to the signals **4006**. Alternatively, FIG. **67**B illustrates the controlled switches **6702** in a shunt configuration so that the switches **6702** shunt the signals **4006** to ground.

Additionally in FIGS. **67**A–B, the 90 degree phase shift between the I and Q channels is realized with the 90 degree splitter **4001**. Alternatively, FIG. **68**A illustrates a receiver **6806** in series configuration, where the 90 degree phase shift is realized by shifting the control signal **3920**B by 90 degrees relative to the control signal **3920**A. More specifically, the 90 degree shifter **6804** is added to shift the control signal **3920**B by 90 degrees relative to the control signal **3920**A. As such, the splitter **6802** is an in-phase (i.e. 0 degree) signal splitter. FIG. **68**B illustrates an embodiment of the receiver **3906** of the receiver **3906** in a shunt configuration with 90 degree delays on the control signal.

Furthermore, the configuration of the controlled switch **6702** is also flexible. More specifically, the controlled switches **6702** can be implemented in many different ways, including transistor switches. FIG. **69**A illustrates the UFT modules **6702** in a series configuration and implemented as FETs **6902**, where the gate of each FET **6902** is controlled by the respective control signal **3920**. As such, the FET **6902** samples the respective signal **4006**, according to the respective control signal **3920**. FIG. **69**B illustrates the shunt configuration.

7.2.2 Multi-Phase IQ Receiver

FIG. **70**A illustrates an exemplary I/Q modulation receiver **7000**, according to an embodiment of the present invention. I/Q modulation receiver **7000** has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation. As will be apparent, the IQ receiver **7000** can be described as a multi-phase receiver to those skilled in the arts.

I/Q modulation receiver **7000** comprises a first UFD module **7002**, a first optional filter **7004**, a second UFD module **7006**, a second optional filter **7008**, a third UFD module **7010**, a third optional filter **7012**, a fourth UFD module **7014**, a fourth filter **7016**, an optional LNA **7018**, a first differential amplifier **7020**, a second differential amplifier **7022**, and an antenna **7072**.

I/Q modulation receiver **7000** receives, down-converts, and demodulates a I/Q modulated RF input signal **7082** to an I baseband output signal **7084**, and a Q baseband output signal **7086**. I/Q modulated RF input signal **7082** comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal **7084** comprises the first baseband information signal. Q baseband output signal **7086** comprises the second baseband information signal.

Antenna **7072** receives I/Q modulated RF input signal **7082**. I/Q modulated RF input signal **7082** is output by antenna **7072** and received by optional LNA **7018**. When present, LNA **7018** amplifies I/Q modulated RF input signal **7082**, and outputs amplified I/Q signal **7088**.

First UFD module **7002** receives amplified I/Q signal **7088**. First UFD module **7002** down-converts the I-phase signal portion of amplified input I/Q signal **7088** according to an I control signal **7090**. First UFD module **7002** outputs an I output signal **7098**.

In an embodiment, first UFD module **7002** comprises a first storage module **7024**, a first UFT module **7026**, and a first voltage reference **7028**. In an embodiment, a switch contained within first UFT module **7026** opens and closes as a function of I control signal **7090**. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module **7024** to and from first voltage reference **7028**, a down-converted signal, referred to as I output signal **7098**, results. First voltage reference **7028** may be any reference voltage, and is preferably ground. I output signal **7098** is stored by first storage module **7024**.

In an embodiment, first storage module **7024** comprises a first capacitor **7074**. In addition to storing I output signal **7098**, first capacitor **7074** reduces or prevents a DC offset voltage resulting from charge injection from appearing on I output signal **7098**.

I output signal **7098** is received by optional first filter **7004**. When present, first filter **7004** is in some embodiments a high pass filter to at least filter I output signal **7098** to remove any carrier signal "bleed through". In a preferred embodiment, when present, first filter **7004** comprises a first resistor **7030**, a first filter capacitor **7032**, and a first filter voltage reference **7034**. Preferably, first resistor **7030** is coupled between I output signal **7098** and a filtered I output signal **7007**, and first filter capacitor **7032** is coupled between filtered I output signal **7007** and first filter voltage reference **7034**. Alternately, first filter **7004** may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). First filter **7004** outputs filtered I output signal **7007**.

Second UFD module **7006** receives amplified I/Q signal **7088**. Second UFD module **7006** down-converts the inverted I-phase signal portion of amplified input I/Q signal **7088** according to an inverted I control signal **7092**. Second UFD module **7006** outputs an inverted I output signal **7001**.

In an embodiment, second UFD module **7006** comprises a second storage module **7036**, a second UFT module **7038**, and a second voltage reference **7040**. In an embodiment, a switch contained within second UFT module **7038** opens and closes as a function of inverted I control signal **7092**. As a result of the opening and closing of this switch, which respectively couples and de-couples second storage module **7036** to and from second voltage reference **7040**, a down-converted signal, referred to as inverted I output signal **7001**, results. Second voltage reference **7040** may be any reference voltage, and is preferably ground. Inverted I output signal **7001** is stored by second storage module **7036**.

In an embodiment, second storage module **7036** comprises a second capacitor **7076**. In addition to storing inverted I output signal **7001**, second capacitor **7076** reduces or prevents a DC offset voltage resulting from charge injection from appearing on inverted I output signal **7001**.

Inverted I output signal **7001** is received by optional second filter **7008**. When present, second filter **7008** is a high pass filter to at least filter inverted I output signal **7001** to remove any carrier signal "bleed through". In a preferred embodiment, when present, second filter **7008** comprises a second resistor **7042**, a second filter capacitor **7044**, and a second filter voltage reference **7046**. Preferably, second resistor **7042** is coupled between inverted I output signal **7001** and a filtered inverted I output signal **7009**, and second filter capacitor **7044** is coupled between filtered inverted I output signal **7009** and second filter voltage reference **7046**. Alternately, second filter **7008** may comprise any other applicable filter configuration as would be understood by

persons skilled in the relevant art(s). Second filter **7008** outputs filtered inverted I output signal **7009**.

First differential amplifier **7020** receives filtered I output signal **7007** at its non-inverting input and receives filtered inverted I output signal **7009** at its inverting input. First differential amplifier **7020** subtracts filtered inverted I output signal **7009** from filtered I output signal **7007**, amplifies the result, and outputs I baseband output signal **7084**. Because filtered inverted I output signal **7009** is substantially equal to an inverted version of filtered I output signal **7007**, I baseband output signal **7084** is substantially equal to filtered I output signal **7009**, with its amplitude doubled. Furthermore, filtered I output signal **7007** and filtered inverted I output signal **7009** may comprise substantially equal noise and DC offset contributions from prior down-conversion circuitry, including first UFD module **7002** and second UFD module **7006**, respectively. When first differential amplifier **7020** subtracts filtered inverted I output signal **7009** from filtered I output signal **7007**, these noise and DC offset contributions substantially cancel each other.

Third UFD module **7010** receives amplified I/Q signal **7088**. Third UFD module **7010** down-converts the Q-phase signal portion of amplified input I/Q signal **7088** according to an Q control signal **7094**. Third UFD module **7010** outputs an Q output signal **7003**.

In an embodiment, third UFD module **7010** comprises a third storage module **7048**, a third UFT module **7050**, and a third voltage reference **7052**. In an embodiment, a switch contained within third UFT module **7050** opens and closes as a function of Q control signal **7094**. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module **7048** to and from third voltage reference **7052**, a down-converted signal, referred to as Q output signal **7003**, results. Third voltage reference **7052** may be any reference voltage, and is preferably ground. Q output signal **7003** is stored by third storage module **7048**.

In an embodiment, third storage module **7048** comprises a third capacitor **7078**. In addition to storing Q output signal **7003**, third capacitor **7078** reduces or prevents a DC offset voltage resulting from charge injection from appearing on Q output signal **7003**.

Q output signal **7003** is received by optional third filter **7012**. When present, in an embodiment, third filter **7012** is a high pass filter to at least filter Q output signal **7003** to remove any carrier signal "bleed through". In an embodiment, when present, third filter **7012** comprises a third resistor **7054**, a third filter capacitor **7056**, and a third filter voltage reference **7058**. Preferably, third resistor **7054** is coupled between Q output signal **7003** and a filtered Q output signal **7011**, and third filter capacitor **7056** is coupled between filtered Q output signal **7011** and third filter voltage reference **7058**. Alternately, third filter **7012** may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Third filter **7012** outputs filtered Q output signal **7011**.

Fourth UFD module **7014** receives amplified I/Q signal **7088**. Fourth UFD module **7014** down-converts the inverted Q-phase signal portion of amplified input I/Q signal **7088** according to an inverted Q control signal **7096**. Fourth UFD module **7014** outputs an inverted Q output signal **7005**.

In an embodiment, fourth UFD module **7014** comprises a fourth storage module **7060**, a fourth UFT module **7062**, and a fourth voltage reference **7064**. In an embodiment, a switch contained within fourth UFT module **7062** opens and closes as a function of inverted Q control signal **7096**. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module **7060** to and from fourth voltage reference **7064**, a down-converted signal, referred to as inverted Q output signal **7005**, results. Fourth voltage reference **7064** may be any reference voltage, and is preferably ground. Inverted Q output signal **7005** is stored by fourth storage module **7060**.

In an embodiment, fourth storage module **7060** comprises a fourth capacitor **7080**. In addition to storing inverted Q output signal **7005**, fourth capacitor **7080** reduces or prevents a DC offset voltage resulting from charge injection from appearing on inverted Q output signal **7005**.

Inverted Q output signal **7005** is received by optional fourth filter **7016**. When present, fourth filter **7016** is a high pass filter to at least filter inverted Q output signal **7005** to remove any carrier signal "bleed through". In a preferred embodiment, when present, fourth filter **7016** comprises a fourth resistor **7066**, a fourth filter capacitor **7068**, and a fourth filter voltage reference **7070**. Preferably, fourth resistor **7066** is coupled between inverted Q output signal **7005** and a filtered inverted Q output signal **7013**, and fourth filter capacitor **7068** is coupled between filtered inverted Q output signal **7013** and fourth filter voltage reference **7070**. Alternately, fourth filter **7016** may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Fourth filter **7016** outputs filtered inverted Q output signal **7013**.

Second differential amplifier **7022** receives filtered Q output signal **7011** at its non-inverting input and receives filtered inverted Q output signal **7013** at its inverting input. Second differential amplifier **7022** subtracts filtered inverted Q output signal **7013** from filtered Q output signal **7011**, amplifies the result, and outputs Q baseband output signal **7086**. Because filtered inverted Q output signal **7013** is substantially equal to an inverted version of filtered Q output signal **7011**, Q baseband output signal **7086** is substantially equal to filtered Q output signal **7013**, with its amplitude doubled. Furthermore, filtered Q output signal **7011** and filtered inverted Q output signal **7013** may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third UFD module **7010** and fourth UFD module **7014**, respectively. When second differential amplifier **7022** subtracts filtered inverted Q output signal **7013** from filtered Q output signal **7011**, these noise and DC offset contributions substantially cancel each other.

Additional embodiments relating to addressing DC offset and re-radiation concerns, applicable to the present invention, are described in co-pending patent application Ser. No. 09/526,041, entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," which is herein incorporated by reference in its entirety.

7.2.2.1 Example I/Q Modulation Control Signal Generator Embodiments

FIG. **70**B illustrates an exemplary block diagram for I/Q modulation control signal generator **7023**, according to an embodiment of the present invention. I/Q modulation control signal generator **7023** generates I control signal **7090**, inverted I control signal **7092**, Q control signal **7094**, and inverted Q control signal **7096** used by I/Q modulation receiver **7000** of FIG. **70**A. I control signal **7090** and inverted I control signal **7092** operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal **7094** and inverted Q control signal **7096** act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator **7023** has the advantage of generating

control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator **7023** comprises a local oscillator **7025**, a first divide-by-two module **7027**, a 180 degree phase shifter **7029**, a second divide-by-two module **7031**, a first pulse generator **7033**, a second pulse generator **7035**, a third pulse generator **7037**, and a fourth pulse generator **7039**.

Local oscillator **7025** outputs an oscillating signal **7015**. FIG. **70**C shows an exemplary oscillating signal **7015**.

First divide-by-two module **7027** receives oscillating signal **7015**, divides oscillating signal **7015** by two, and outputs a half frequency LO signal **7017** and a half frequency inverted LO signal **7041**. FIG. **70**C shows an exemplary half frequency LO signal **7017**. Half frequency inverted LO signal **7041** is an inverted version of half frequency LO signal **7017**. First divide-by-two module **7027** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

180 degree phase shifter **7029** receives oscillating signal **7015**, shifts the phase of oscillating signal **7015** by 180 degrees, and outputs phase shifted LO signal **7019**. 180 degree phase shifter **7029** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s). In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module **7031** receives phase shifted LO signal **7019**, divides phase shifted LO signal **7019** by two, and outputs a half frequency phase shifted LO signal **7021** and a half frequency inverted phase shifted LO signal **7043**. FIG. **70**C shows an exemplary half frequency phase shifted LO signal **7021**. Half frequency inverted phase shifted LO signal **7043** is an inverted version of half frequency phase shifted LO signal **7021**. Second divide-by-two module **7031** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

First pulse generator **7033** receives half frequency LO signal **7017**, generates an output pulse whenever a rising edge is received on half frequency LO signal **7017**, and outputs I control signal **7090**. FIG. **70**C shows an exemplary I control signal **7090**.

Second pulse generator **7035** receives half frequency inverted LO signal **7041**, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal **7041**, and outputs inverted I control signal **7092**. FIG. **70**C shows an exemplary inverted I control signal **7092**.

Third pulse generator **7037** receives half frequency phase shifted LO signal **7021**, generates an output pulse whenever a rising edge is received on half frequency phase shifted LO signal **7021**, and outputs Q control signal **7094**. FIG. **70**C shows an exemplary Q control signal **7094**.

Fourth pulse generator **7039** receives half frequency inverted phase shifted LO signal **7043**, generates an output pulse whenever a rising edge is received on half frequency inverted phase shifted LO signal **7043**, and outputs inverted Q control signal **7096**. FIG. **70**C shows an exemplary inverted Q control signal **7096**.

In an embodiment, control signals **7090**, **7021**, **7041** and **7043** include pulses having a width equal to one-half of a period of I/Q modulated RF input signal **7082**. The invention, however, is not limited to these pulse widths, and control signals **7090**, **7021**, **7041**, and **7043** may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal **7082**.

First, second, third, and fourth pulse generators **7033**, **7035**, **7037**, and **7039** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

As shown in FIG. **70**C, in an embodiment, control signals **7090**, **7021**, **7041**, and **7043** comprise pulses that are non-overlapping in other embodiments the pulses may overlap. Furthermore, in this example, pulses appear on these signals in the following order: I control signal **7090**, Q control signal **7094**, inverted I control signal **7092**, and inverted Q control signal **7096**. Potential circuit re-radiation from VQ modulation receiver **7000** may comprise frequency components from a combination of these control signals.

For example, FIG. **70**D shows an overlay of pulses from I control signal **7090**, Q control signal **7094**, inverted I control signal **7092**, and inverted Q control signal **7096**. When pulses from these control signals leak through first, second, third, and/or fourth UFD modules **7002**, **7006**, **7010**, and **7014** to antenna **7072** (shown in FIG. **70**A), they may be radiated from I/Q modulation receiver **7000**, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals **7090**, **7021**, **7041**, and **7043**. FIG. **70** shows an example combined control signal **7045**.

FIG. **70**D also shows an example I/Q modulation RF input signal **7082** overlaid upon control signals **7090**, **7094**, **7092**, and **7096**. As shown in FIG. **70**D, pulses on I control signal **7090** overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal **7082**. Pulses on inverted I control signal **7092** overlay and act to down-convert a negative I-phase portion of I/Q modulation RF input signal **7082**. Pulses on Q control signal **7094** overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal **7082**. Pulses on inverted Q control signal **7096** overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal **7082**.

As FIG. **70**D further shows in this example, the frequency ratio between the combination of control signals **7090**, **7021**, **7041**, and **7043** and I/Q modulation RF input signal **7082** is approximately 4:3. Because the frequency of the potentially re-radiated signal, i.e., combined control signal **7045**, is substantially different from that of the signal being down-converted, i.e., I/Q modulation RF input signal **7082**, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver **7000** reduces problems due to circuit re-radiation. As will be understood by persons skilled in the relevant art(s) from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator **7023** will be apparent to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the present invention.

FIG. **70**S illustrates the receiver **7000**, where the UFT modules **7028**, **7038**, **7050**, and **7062** are configured with FETs **7099***a–d*.

Additional embodiments relating to addressing DC offset and re-radiation concerns, applicable to the present invention, are described in co-pending patent application Ser. No. 09/526,041, entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," which is herein incorporated by reference in its entirety.

7.2.2.2 Implementation of Multi-phase I/Q Modulation Receiver Embodiment with Exemplary Waveforms

FIG. **70**E illustrates a more detailed example circuit implementation of I/Q modulation receiver **7000**, according to an embodiment of the present invention. FIGS. **70**F–P show example waveforms related to an example implementation of I/Q modulation receiver **7000** of FIG. **70**E.

FIGS. **70**F and **70**G show first and second input data signals **7047** and **7049** to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. **70**I and **70**J show the signals of FIG. **70**F and **70**G after modulation with a RF carrier signal frequency, respectively, as I-modulated signal **7051** and Q-modulated signal **7053**.

FIG. **70**H shows an I/Q modulation RF input signal **7082** formed from I-modulated signal **7051** and Q-modulated signal **7053** of FIGS. **70**I and **70**J, respectively.

FIG. **70**O shows an overlaid view of filtered I output signal **7007** and filtered inverted I output signal **7009**.

FIG. **70**P shows an overlaid view of filtered Q output signal **7011** and filtered inverted Q output signal **7013**.

FIGS. **70**K and **70**L show I baseband output signal **7084** and Q baseband output signal **7086**, respectfully. A data transition **7055** is indicated in both I baseband output signal **7084** and Q baseband output signal **7086**. The corresponding data transition **7055** is indicated in I-modulated signal **7051** of FIG. **70**I, Q-modulated signal **7053** of FIG. **70**J, and I/Q modulation RF input signal **7082** of FIG. **70**H.

FIGS. **70**M and **70**N show I baseband output signal **7084** and Q baseband output signal **7086** over a wider time interval.

7.2.2.3 Example Single Channel Receiver Embodiment

FIG. **70**Q illustrates an example single channel receiver **7091**, corresponding to either the I or Q channel of I/Q modulation receiver **7000**, according to an embodiment of the present invention. Single channel receiver **7091** can down-convert an input RF signal **7097** modulated according to AM, PM, FM, and other modulation schemes. Refer to section 7.2.1 above for further description on the operation of single channel receiver **7091**. In other words, the single channel receiver **7091** is a one channel of the IQ receiver **7000** that was discussed in section 7.2.1.

7.2.2.4 Alternative Example I/Q Modulation Receiver Embodiment

FIG. **70**R illustrates an exemplary I/Q modulation receiver **7089**, according to an embodiment of the present invention. I/Q modulation receiver **7089** receives, down-converts, and demodulates an I/Q modulated RF input signal **7082** to an I baseband output signal **7084**, and a Q baseband output signal **7086**. I/Q modulation receiver **7089** has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation, in a similar fashion to that of I/Q modulation receiver **7000** described above.

7.3 Transmitter

Example embodiments and implementations of the IQ transmitter **3910** will be discussed as follows. The example embodiments and implementations include multi-phase embodiments that are useful for reducing or eliminating unwanted DC offsets that can result in unwanted carrier insertion.

7.3.1 Universal Transmitter with 2 UFT Modules

FIG. **71**A illustrates a transmitter **7102** according to embodiments of the present invention. Transmitter **7102** includes a balanced modulator/up-converter **7104**, a control signal generator **7142**, an optional filter **7106**, and an optional amplifier **7108**. Transmitter **7102** up-converts a baseband signal **7110** to produce an output signal **7140** that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator **7104** receives the baseband signal **7110** and samples the baseband signal in a differential and balanced fashion to generate a harmonically rich signal **7138**. The harmonically rich signal **7138** includes multiple harmonic images, where each image contains the baseband information in the baseband signal **7110** The optional bandpass filter **7106** may be included to select a harmonic of interest (or a subset of harmonics) in the signal **7138** for transmission. The optional amplifier **7108** may be included to amplify the selected harmonic prior to transmission. The universal transmitter is further described at a high level by the flowchart **8400** that is shown in FIG. **84**. A more detailed structural and operational description of the balanced modulator follows thereafter.

Referring to flowchart **8400**, in step **8402**, the balanced modulator **7104** receives the baseband signal **7110**.

In step **8404**, the balanced modulator **7104** samples the baseband signal in a differential and balanced fashion according to a first and second control signals that are phase shifted with respect to each other. The resulting harmonically rich signal **7138** includes multiple harmonic images that repeat at harmonics of the sampling frequency, where each image contains the necessary amplitude and frequency information to reconstruct the baseband signal **7110**.

In embodiments of the invention, the control signals include pulses having pulse widths (or apertures) that are established to improve energy transfer to a desired harmonic of the harmonically rich signal **7138**. In further embodiments of the invention, DC offset voltages are minimized between sampling modules as indicated in step **8406**, thereby minimizing carrier insertion in the harmonic images of the harmonically rich signal **7138**.

In step **8408**, the optional bandpass filter **7106** selects the desired harmonic of interest (or a subset of harmonics) in from the harmonically rich signal **7138** for transmission.

In step **8410**, the optional amplifier **7108** amplifies the selected harmonic(s) prior to transmission.

In step **8412**, the selected harmonic(s) is transmitted over a communications medium.

7.3.1.1 Balanced Modulator Detailed Description

Referring to the example embodiment shown in FIG. **71**A, the balanced modulator **7104** includes the following components: a buffer/inverter **7112**; summer amplifiers **7118**, **7119**; UFT modules **7124** and **7128** having controlled switches **7148** and **7150**, respectively; an inductor **7126**; a blocking capacitor **7136**; and a DC terminal **7111**. As stated above, the balanced modulator **7104** differentially samples the baseband signal **7110** to generate a harmonically rich signal **7138**. More specifically, the UFT modules **7124** and **7128** sample the baseband signal in differential fashion according to control signals **7123** and **7127**, respectively. A DC reference voltage **7113** is applied to terminal **7111** and is uniformly distributed to the UFT modules **7124** and **7128**. The distributed DC voltage **7113** prevents any DC offset voltages from developing between the UFT modules, which can lead to carrier insertion in the harmonically rich signal **7138**. The operation of the balanced modulator **7104** is discussed in greater detail with reference to flowchart **8500** (FIG. **85**), as follows.

In step **8402**, the buffer/inverter **7112** receives the input baseband signal **7110** and generates input signal **7114** and inverted input signal **7116**. Input signal **7114** is substantially similar to signal **7110**, and inverted signal **7116** is an inverted version of signal **7114**. As such, the buffer/inverter **7112** converts the (single-ended) baseband signal **7110** into differential input signals **7114** and **7116** that will be sampled by the UFT modules. Buffer/inverter **7112** can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step **8504**, the summer amplifier **7118** sums the DC reference voltage **7113** applied to terminal **7111** with the input signal **7114**, to generate a combined signal **7120**. Likewise, the summer amplifier **7119** sums the DC reference voltage **7113** with the inverted input signal **7116** to generate a combined signal **7122**. Summer amplifiers **7118** and **7119** can be implemented using known op amp summer circuits, and can be designed to have a specified gain or attenuation, including unity gain, although the invention is not limited to this example. The DC reference voltage **7113** is also distributed to the outputs of both UFT modules **7124** and **7128** through the inductor **7126** as is shown.

In step **8506**, the control signal generator **7142** generates control signals **7123** and **7127** that are shown by way of example in FIG. **72**B and FIG. **72**C, respectively. As illustrated, both control signals **7123** and **7127** have the same period T_S as a master clock signal **7145** (FIG.72A), but have a pulse width (or aperture) of T_A. In the example, control signal **7123** triggers on the rising pulse edge of the master clock signal **7145**, and control signal **7127** triggers on the falling pulse edge of the master clock signal **7145**. Therefore, control signals **7123** and **7127** are shifted in time by 180 degrees relative to each other. In embodiments of invention, the master clock signal **7145** (and therefore the control signals **7123** and **7127**) have a frequency that is a sub-harmonic of the desired output signal **7140**. The invention is not limited to the example of FIGS. **72**A–**72**C.

In one embodiment, the control signal generator **7142** includes an oscillator **7146**, pulse generators **7144***a* and **7144***b*, and an inverter **7147** as shown. In operation, the oscillator **7146** generates the master clock signal **7145**, which is illustrated in FIG. **72**A as a periodic square wave having pulses with a period of T_S. Other clock signals could be used including but not limited to sinusoidal waves, as will be understood by those skilled in the arts. Pulse generator **7144***a* receives the master clock signal **7145** and triggers on the rising pulse edge, to generate the control signal **7123**. Inverter **7147** inverts the clock signal **7145** to generate an inverted clock signal **7143**. The pulse generator **7144***b* receives the inverted clock signal **7143** and triggers on the rising pulse edge (which is the falling edge of clock signal **7145**), to generate the control signal **7127**.

FIG. **89**A-E illustrate example embodiments for the pulse generator **7144**. FIG. **89**A illustrates a pulse generator **8902**. The pulse generator **8902** generates pulses **8908** having pulse width T_A from an input signal **8904**. Example input signals **8904** and pulses **8908** are depicted in FIGS. **89**B and **89**C, respectively. The input signal **8904** can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave etc. The pulse width (or aperture) T_A of the pulses **8908** is determined by delay **8906** of the pulse generator **8902**. The pulse generator **8902** also includes an optional inverter **8910**, which is optionally added for polarity considerations as understood by those skilled in the arts. The example logic and implementation shown for the pulse generator **8902** is provided for illustrative purposes only, and is not limiting. The actual logic employed can take many forms. Additional examples of pulse generation logic are shown in FIGS. **89**D and **89**E. FIG. **89**D illustrates a rising edge pulse generator **8912** that triggers on the rising edge of input signal **8904**. FIG. **89**E illustrates a falling edge pulse generator **8916** that triggers on the falling edge of the input signal **8904**.

In step **8508**, the UFT module **7124** samples the combined signal **7120** according to the control signal **7123** to generate harmonically rich signal **7130**. More specifically, the switch **7148** closes during the pulse widths T_A of the control signal **7123** to sample the combined signal **7120** resulting in the harmonically rich signal **7130**. FIG. **71**B illustrates an exemplary frequency spectrum for the harmonically rich signal **7130** having harmonic images **7152***a–n*. The images **7152** repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image **7152** contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal **7110**. As discussed further below, the relative amplitude of the frequency images is generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic **7152** can be increased (or decreased) by adjusting the pulse width T_A of the control signal **7123**. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGS. **3**–**6**. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in the co-pending patent application titled, "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, field on Oct. 21, 1998, and incorporated herein by reference.

In step **8510**, the UFT module **7128** samples the combined signal **7122** according to the control signal **7127** to generate harmonically rich signal **7134**. More specifically, the switch **7150** closes during the pulse widths T_A of the control signal **7127** to sample the combined signal **7122** resulting in the harmonically rich signal **7134**. The harmonically rich signal **7134** includes multiple frequency images of baseband signal **7110** that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal **7130**. However, the images in the signal **7134** are phase-shifted compared to those in signal **7130** because of the inversion of signal **7116** compared to signal **7114**, and because of the relative phase shift between the control signals **7123** and **7127**.

In step **8512**, the node **7132** sums the harmonically rich signals **7130** and **7134** to generate harmonically rich signal **7133**. FIG. **71**C illustrates an exemplary frequency spectrum for the harmonically rich signal **7133** that has multiple images **7154***a–n* that repeat at harmonics of the sampling frequency $1/T_S$. Each image **7154** includes the necessary amplitude, frequency and phase information to reconstruct the baseband signal **7110**. The capacitor **7136** operates as a DC blocking capacitor and substantially passes the harmonics in the harmonically rich signal **7133** to generate harmonically rich signal **7138** at the output of the modulator **7104**.

In step **8408**, the optional filter **7106** can be used to select a desired harmonic image for transmission. This is represented for example by a passband **7156** that selects the harmonic image **7154***c* for transmission in FIG. **71**C.

An advantage of the modulator **7104** is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules **7124** and **7128**. DC offset is minimized because the reference voltage **7113** contributes a consistent DC component to the input signals **7120** and **7122** through the summing amplifiers **7118** and **7119**, respectively. Furthermore, the reference voltage **7113** is also directly coupled to the outputs of the UFT modules **7124** and **7128** through the inductor **7126** and the node **7132**. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal **7138**. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

7.3.1.2 Balanced Modulator Example Signal Diagrams and Mathematical Description

In order to further describe the invention, FIGS. **72**D–**72**I illustrate various example signal diagrams (vs. time) that are representative of the invention. These signal diagrams are meant for example purposes only and are not meant to be limiting. FIG. **72**D illustrates a signal **7202** that is representative of the input baseband signal **7110** (FIG. **71**A). FIG. **72**E illustrates a step function **7204** that is an expanded portion of the signal **7202** from time t_0 to t_1, and represents signal **7114** at the output of the buffer/inverter **7112**. Similarly, FIG. **72**F illustrates a signal **7206** that is an inverted version of the signal **7204**, and represents the signal **7116** at the inverted output of buffer/inverter **7112**. For analysis purposes, a step function is a good approximation for a portion of a single bit of data (for the baseband signal **7110**) because the clock rates of the control signals **7123** and **7127** are significantly higher than the data rates of the baseband signal **7110**. For example, if the data rate is in the KHz frequency range, then the clock rate will preferably be in MHZ frequency range in order to generate an output signal in the Ghz frequency range.

Still referring to FIGS. **72**D–I, FIG. **72**G illustrates a signal **7208** that an example of the harmonically rich signal **7130** when the step function **7204** is sampled according to the control signal **7123** in FIG. **72**B. The signal **7208** includes positive pulses **7209** as referenced to the DC voltage **7113**. Likewise, FIG. **72**H illustrates a signal **7210** that is an example of the harmonically rich signal **7134** when the step function **7206** is sampled according to the control signal **7127**. The signal **7210** includes negative pulses **7211** as referenced to the DC voltage **7113**, which are time-shifted relative the positive pulses **7209** in signal **7208**.

Still referring to FIGS. **72**D I, the FIG. **72**I illustrates a signal **7212** that is the combination of signal **7208** (FIG. **72**G) and the signal **7210** (FIG. **72**H), and is an example of the harmonically rich signal **7133** at the output of the summing node **7132**. As illustrated, the signal **7212** spends approximately as much time above the DC reference voltage **7113** as below the DC reference voltage **7113** over a limited time period. For example, over a time period **7214**, the energy in the positive pulses **7209***a–b* is canceled out by the energy in the negative pulses **7211***a–b*. This is indicative of minimal (or zero) DC offset between the UFT modules **7124** and **7128**, which results in minimal carrier insertion during the sampling process.

Still referring to FIG. **72**I, the time axis of the signal **7212** can be phased in such a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is readily calculated to obtain:

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4 \sin\left(\frac{n\pi T_A}{T_S}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot \sin\left(\frac{2n\pi t}{T_S}\right). \quad \text{Equation 1}$$

where:

T_S=period of the master clock **7145**

T_A=pulse width of the control signals **7123** and **7127**

n=harmonic number

As shown by Equation 1, the relative amplitude of the frequency images is generally a function of the harmonic number n, and the ratio of T_A/T_S. As indicated, the T_A/T_S ratio represents the ratio of the pulse width of the control signals relative to the period of the sub-harmonic master clock. The T_A/T_S ratio can be optimized in order to maximize the amplitude of the frequency image at a given harmonic. For example, if a passband waveform is desired to be created at 5× the frequency of the sub-harmonic clock, then a baseline power for that harmonic extraction may be calculated for the fifth harmonic (n=5) as:

$$I_c(t) = \left(\frac{4 \sin\left(\frac{5\pi T_A}{T_S}\right)}{5\pi} \right) \cdot \sin(5\omega_S t). \quad \text{Equation 2}$$

As shown by Equation 2, $I_C(t)$ for the fifth harmonic is a sinusoidal function having an amplitude that is proportional to the $\sin(5\pi T_A/T_S)$. The signal amplitude can be maximized by setting $T_A=(1/10 \cdot T_S)$ so that $\sin(5\pi T_A/T_S)=\sin(\pi/2)=1$. Doing so results in the equation:

$$I_c(t)|_{n=5} = \frac{4}{5\pi}(\sin(5\omega_S t)). \quad \text{Equation 3}$$

This component is a frequency at 5× of the sampling frequency of sub-harmonic clock, and can be extracted from the Fourier series via a bandpass filter (such as bandpass filter **7106**) that is centered around $5f_S$. The extracted frequency component can then be optionally amplified by the amplifier **7108** prior to transmission on a wireless or wire-line communications channel or channels.

Equation 3 can be extended to reflect the inclusion of a message signal as illustrated by equation 4 below:

$$m(t) \cdot I_c(t)|_{\substack{n=5 \\ \theta=\theta(t)}} = \frac{4 \cdot m(t)}{5\pi}(\sin(5\omega_S t + 5\theta(t))). \quad \text{Equation 4}$$

Equation 4 illustrates that a message signal can be carried in harmonically rich signals **7133** such that both amplitude and phase can be modulated. In other words, m(t) is modulated for amplitude and θ(t) is modulated for phase. In such cases, it should be noted that 0(t) is augmented modulo n while the amplitude modulation m(t) is simply scaled. Therefore, complex waveforms may be reconstructed from their Fourier series with multiple aperture UFT combinations.

As discussed above, the signal amplitude for the 5th harmonic was maximized by setting the sampling aperture width $T_A=1/10T_S$, where T_S is the period of the master clock signal. This can be restated and generalized as setting $T_A=1/2$ the period (or π radians) at the harmonic of interest. In other words, the signal amplitude of any harmonic n can be maximized by sampling the input waveform with a sampling aperture of $T_A=1/2$ the period of the harmonic of interest (n). Based on this discussion, it is apparent that varying the

aperture changes the harmonic and amplitude content of the output waveform. For example, if the sub-harmonic clock has a frequency of 200 MHZ, then the fifth harmonic is at 1 Ghz. The amplitude of the fifth harmonic is maximized by setting the aperture width T_A=500 picoseconds, which equates to ½ the period (or π radians) at 1 Ghz.

FIG. **72**J depicts a frequency plot **7216** that graphically illustrates the effect of varying the sampling aperture of the control signals on the harmonically rich signal **7133** given a 200 MHZ harmonic clock. The frequency plot **7216** compares two frequency spectrums **7218** and **7220** for different control signal apertures given a 200 MHZ clock. More specifically, the frequency spectrum **7218** is an example spectrum for signal **7133** given the 200 MHZ clock with the aperture T_A=500 psec (where 500 psec is π radians at the 5th harmonic of 1 GHz). Similarly, the frequency spectrum **7220** is an example spectrum for signal **7133** given a 200 MHZ clock that is a square wave (so T_A=5000 psec). The spectrum **7218** includes multiple harmonics **7218***a*–I, and the frequency spectrum **7220** includes multiple harmonics **7220***a–e*. [It is noted that spectrum **7220** includes only the odd harmonics as predicted by Fourier analysis for a square wave.] At 1 Ghz (which is the 5th harmonic), the signal amplitude of the two frequency spectrums **7218***e* and **7220***c* are approximately equal. However, at 200 MHZ, the frequency spectrum **7218***a* has a much lower amplitude than the frequency spectrum **7220***a*, and therefore the frequency spectrum **7218** is more efficient than the frequency spectrum **7220**, assuming the desired harmonic is the 5th harmonic. In other words, assuming 1 Ghz is the desired harmonic, the frequency spectrum **7218** wastes less energy at the 200 MHZ fundamental than does the frequency spectrum **7218**.

7.3.1.3 Balanced Modulator Having a Shunt Configuration

FIG. **79**A illustrates a universal transmitter **7900** that is a second embodiment of a universal transmitter having two balanced UFT modules in a shunt configuration. (In contrast, the balanced modulator **7104** can be described as having a series configuration based on the orientation of the UFT modules.) Transmitter **7900** includes a balanced modulator **7901**, the control signal generator **7142**, the optional bandpass filter **7106**, and the optional amplifier **7108**. The transmitter **7900** up-converts a baseband signal **7902** to produce an output signal **7936** that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator **7901** receives the baseband signal **7902** and shunts the baseband signal to ground in a differential and balanced fashion to generate a harmonically rich signal **7934**. The harmonically rich signal **7934** includes multiple harmonic images, where each image contains the baseband information in the baseband signal **7902**. In other words, each harmonic image includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal **7902**. The optional bandpass filter **7106** may be included to select a harmonic of interest (or a subset of harmonics) in the signal **7934** for transmission. The optional amplifier **7108** may be included to amplify the selected harmonic prior to transmission, resulting in the output signal **7936**.

The balanced modulator **7901** includes the following components: a buffer/inverter **7904**; optional impedances **7910**, **7912**; UFT modules **7916** and **7922** having controlled switches **7918** and **7924**, respectively; blocking capacitors **7928** and **7930**; and a terminal **7920** that is tied to ground. As stated above, the balanced modulator **7901** differentially shunts the baseband signal **7902** to ground, resulting in a harmonically rich signal **7934**. More specifically, the UFT modules **7916** and **7922** alternately shunts the baseband signal to terminal **7920** according to control signals **7123** and **7127**, respectively. Terminal **7920** is tied to ground and prevents any DC offset voltages from developing between the UFT modules **7916** and **7922**. As described above, a DC offset voltage can lead to undesired carrier insertion. The operation of the balanced modulator **7901** is described in greater detail according to the flowchart **8600** (FIG. **86**) as follows.

In step **8402**, the buffer/inverter **7904** receives the input baseband signal **7902** and generates I signal **7906** and inverted I signal **7908**. I signal **7906** is substantially similar to the baseband signal **7902**, and the inverted I signal **7908** is an inverted version of signal **7902**. As such, the buffer/inverter **7904** converts the (single-ended) baseband signal **7902** into differential signals **7906** and **7908** that are sampled by the UFT modules. Buffer/inverter **7904** can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step **8604**, the control signal generator **7142** generates control signals **7123** and **7127** from the master clock signal **7145**. Examples of the master clock signal **7145**, control signal **7123**, and control signal **7127** are shown in FIGS. **72**A–C, respectively. As illustrated, both control signals **7123** and **7127** have the same period T_S as a master clock signal **7145**, but have a pulse width (or aperture) of T_A. Control signal **7123** triggers on the rising pulse edge of the master clock signal **7145**, and control signal **7127** triggers on the falling pulse edge of the master clock signal **7145**. Therefore, control signals **7123** and **7127** are shifted in time by 180 degrees relative to each other. A specific embodiment of the control signal generator **7142** is illustrated in FIG. **71**A, and was discussed in detail above.

In step **8606**, the UFT module **7916** shunts the signal **7906** to ground according to the control signal **7123**, to generate a harmonically rich signal **7914**. More specifically, the switch **7918** closes and shorts the signal **7906** to ground (at terminal **7920**) during the aperture width T_A of the control signal **7123**, to generate the harmonically rich signal **7914**. FIG. **79**B illustrates an exemplary frequency spectrum for the harmonically rich signal **7918** having harmonic images **7950***a–n*. The images **7950** repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image **7950** contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal **7902**. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGS. **3**–**6**. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in the co-pending patent application titled, "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, field on Oct. 21, 1998, and incorporated herein by reference.

The relative amplitude of the frequency images **7950** are generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic **7950** can be increased (or decreased) by adjusting the pulse width T_A of the control signal **7123**. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics, as described by equations 1–4 above. Additionally, the relative amplitude of a particular harmonic **7950** can also be adjusted by adding/tuning an optional impedance **7910**. Impedance **7910** operates as a filter that emphasizes a particular harmonic in the harmonically rich signal **7914**.

In step **8608**, the UFT module **7922** shunts the inverted signal **7908** to ground according to the control signal **7127**, to generate a harmonically rich signal **7926**. More specifically, the switch **7924** closes during the pulse widths T_4 and shorts the inverted I signal **7908** to ground (at terminal **7920**), to generate the harmonically rich signal **7926**. At any given time, only one of input signals **7906** or **7908** is shorted to ground because the pulses in the control signals **7123** and **7127** are phase shifted with respect to each other, as shown in FIGS. 72B and 72C.

The harmonically rich signal **7926** includes multiple frequency images of baseband signal **7902** that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal **7914**. However, the images in the signal **7926** are phase-shifted compared to those in signal **7914** because of the inversion of the signal **7908** compared to the signal **7906**, and because of the relative phase shift between the control signals **7123** and **7127**. The optional impedance **7912** can be included to emphasis a particular harmonic of interest, and is similar to the impedance **7910** above.

In step **8610**, the node **7932** sums the harmonically rich signals **7914** and **7926** to generate the harmonically rich signal **7934**. The capacitors **7928** and **7930** operate as blocking capacitors that substantially pass the respective harmonically rich signals **7914** and **7926** to the node **7932**. (The capacitor values may be chosen to substantially block baseband frequency components as well.) FIG. **79**C illustrates an exemplary frequency spectrum for the harmonically rich signal **7934** that has multiple images **7952***a–n* that repeat at harmonics of the sampling frequency $1/T_S$. Each image **7952** includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal **7902**. The optional filter **7106** can be used to select the harmonic image of interest for transmission. This is represented by a passband **7956** that selects the harmonic image **7932***c* for transmission.

An advantage of the modulator **7901** is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules **7912** and **7914**. DC offset is minimized because the UFT modules **7916** and **7922** are both connected to ground at terminal **7920**. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal **7934**. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

7.3.1.4 Balanced Modulator FET Configuration

As described above, the balanced modulators **7104** and **7901** utilize two balanced UFT modules to sample the input baseband signals to generate harmonically rich signals that contain the up-converted baseband information. More specifically, the UFT modules include controlled switches that sample the baseband signal in a balanced and differential fashion. FIGS. **71**D and **79**D illustrate embodiments of the controlled switch in the UFT module.

FIG. **71**D illustrates an example embodiment of the modulator **7104** (FIG. **71**B) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches **7148** and **7128** are embodied as FET **7158** and FET **7160**, respectively. The FET **7158** and **7160** are oriented so that their gates are controlled by the control signals **7123** and **7127**, so that the control signals control the FET conductance. For the FET **7158**, the combined baseband signal **7120** is received at the source of the FET **7158** and is sampled according to the control signal **7123** to produce the harmonically rich signal **7130** at the drain of the FET **7158**. Likewise, the combined baseband signal **7122** is received at the source of the FET **7160** and is sampled according to the control signal **7127** to produce the harmonically rich signal **7134** at the drain of FET **7160**. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs. In other words, the combined baseband signal can be received at the drain of the FETs, and the harmonically rich signals can be taken from the source of the FETs, as will be understood by those skilled in the relevant arts.

FIG. **79**D illustrates an embodiment of the modulator **7900** (FIG. **79**A) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches **7918** and **7924** are embodied as FET **7936** and FET **7938**, respectively. The FETs **7936** and **7938** are oriented so that their gates are controlled by the control signals **7123** and **7127**, respectively, so that the control signals determine FET conductance. For the FET **7936**, the baseband signal **7906** is received at the source of the FET **7936** and shunted to ground according to the control signal **7123**, to produce the harmonically rich signal **7914**. Likewise, the baseband signal **7908** is received at the source of the FET **7938** and is shunted to grounding according to the control signal **7127**, to produce the harmonically rich signal **7926**. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs, as will be understood by those skilled in the relevant arts.

7.3.1.5 Universal Transmitter Configured for Carrier Insertion

As discussed above, the transmitters **7102** and **7900** have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the output signal **7140**. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, the present invention can be configured to provide the necessary carrier insertion by implementing a DC offset between the two sampling UFT modules.

FIG. **73**A illustrates a transmitter **7302** that up-converts a baseband signal **7306** to an output signal **7322** having carrier insertion. As is shown, the transmitter **7302** is similar to the transmitter **7102** (FIG. **71**A) with the exception that the up-converter/modulator **7304** is configured to accept two DC references voltages. In contrast, modulator **7104** was configured to accept only one DC reference voltage. More specifically, the modulator **7304** includes a terminal **7309** to accept a DC reference voltage **7308**, and a terminal **7313** to accept a DC reference voltage **7314**. Vr **7308** appears at the UFT module **7124** though summer amplifier **7118** and the inductor **7310**. Vr **7314** appears at UFT module **7128** through the summer amplifier **7119** and the inductor **7316**. Capacitors **7312** and **7318** operate as blocking capacitors. If Vr **7308** is different from Vr **7314** then a DC offset voltage will be exist between UFT module **7124** and UFT module **7128**, which will be up-converted at the carrier frequency in the harmonically rich signal **7320**. More specifically, each harmonic image in the harmonically rich signal **7320** will include a carrier signal as depicted in FIG. **73**B.

FIG. **73**B illustrates an exemplary frequency spectrum for the harmonically rich signal **7320** that has multiple harmonic

images **7324***a–n*. In addition to carrying the baseband information in the sidebands, each harmonic image **7324** also includes a carrier signal **7326** that exists at respective harmonic of the sampling frequency $1/T_S$. The amplitude of the carrier signal increases with increasing DC offset voltage. Therefore, as the difference between Vr **7308** and Vr **7314** widens, the amplitude of each carrier signal **7326** increases. Likewise, as the difference between Vr **7308** and Vr **7314** shrinks, the amplitude of each carrier signal **7326** shrinks. As with transmitter **7302**, the optional bandpass filter **7106** can be included to select a desired harmonic image for transmission. This is represented by passband **7328** in FIG. **73**B.

7.3.2 Universal Transmitter In I Q Configuration

As described above, the balanced modulators **7104** and **7901** up-convert a baseband signal to a harmonically rich signal having multiple harmonic images of the baseband information. By combining two balanced modulators, IQ configurations can be formed for up-converting I and Q baseband signals. In doing so, either the (series type) balanced modulator **7104** or the (shunt type) balanced modulator **7901** can be utilized. IQ modulators having both series and shunt configurations are described below.

7.3.2.1 IQ Transmitter Using Series-Type Balanced Modulator

FIG. **74** illustrates an IQ transmitter **7420** with an in-phase (I) and quadrature (Q) configuration according to embodiments of the invention. The transmitter **7420** includes an IQ balanced modulator **7410**, an optional filter **7414**, and an optional amplifier **7416**. The transmitter **7420** is useful for transmitting complex I Q waveforms and does so in a balanced manner to control DC offset and carrier insertion. In doing so, the modulator **7410** receives an I baseband signal **7402** and a Q baseband signal **7404** and up-converts these signals to generate a combined harmonically rich signal **7412**. The harmonically rich signal **7412** includes multiple harmonics images, where each image contains the baseband information in the I signal **7402** and the Q signal **7404**. The optional bandpass filter **7414** may be included to select a harmonic of interest (or subset of harmonics) from the signal **7412** for transmission. The optional amplifier **7416** may be included to amplify the selected harmonic prior to transmission, to generate the IQ output signal **7418**.

As stated above, the balanced IQ modulator **7410** up-converts the I baseband signal **7402** and the Q baseband signal **7404** in a balanced manner to generate the combined harmonically rich signal **7412** that carriers the I and Q baseband information. To do so, the modulator **7410** utilizes two balanced modulators **7104** from FIG. **71**A, a signal combiner **7408**, and a DC terminal **7407**. The operation of the balanced modulator **7410** and other circuits in the transmitter is described according to the flowchart **8700** in FIG. **87**, as follows.

In step **8702**, the IQ modulator **7410** receives the I baseband signal **7402** and the Q baseband signal **7404**.

In step **8704**, the I balanced modulator **7104***a* samples the I baseband signal **7402** in a differential fashion using the control signals **7123** and **7127** to generate a harmonically rich signal **7411***a*. The harmonically rich signal **7411** a contains multiple harmonic images of the I baseband information, similar to the harmonically rich signal **7130** in FIG. **71**B.

In step **8706**, the balanced modulator **7104***b* samples the Q baseband signal **7404** in a differential fashion using control signals **7123** and **7127** to generate harmonically rich signal **7411***b*, where the harmonically rich signal **7411***b* contains multiple harmonic images of the Q baseband signal **7404**. The operation of the balanced modulator **7104** and the generation of harmonically rich signals was fully described above and illustrated in FIGS. **71**A–C, to which the reader is referred for further details.

In step **8708**, the DC terminal **7407** receives a DC voltage **7406** that is distributed to both modulators **7104***a* and **7104***b*. The DC voltage **7406** is distributed to both the input and output of both UFT modules **7124** and **7128** in each modulator **7104**. This minimizes (or prevents) DC offset voltages from developing between the four UFT modules, and thereby minimizes or prevents any carrier insertion during the sampling steps **8704** and **8706**.

In step **8710**, the 90 degree signal combiner **7408** combines the harmonically rich signals **7411***a* and **7411***b* to generate IQ harmonically rich signal **7412**. This is further illustrated in FIGS. **75**A–C. FIG. **75**A depicts an exemplary frequency spectrum for the harmonically rich signal **7411** a having harmonic images **7502***a–n*. The images **7502** repeat at harmonics of the sampling frequency $1/T_S$, where each image **7502** contains the necessary amplitude and frequency information to reconstruct the I baseband signal **7402**. Likewise, FIG. **75**B depicts an exemplary frequency spectrum for the harmonically rich signal **7411***b* having harmonic images **7504***a–n*. The harmonic images **7504***a–n* also repeat at harmonics of the sampling frequency $1/T_S$, where each image **7504** contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal **7404**. FIG. **75**C illustrates an exemplary frequency spectrum for the combined harmonically rich signal **7412** having images **7506**. Each image **7506** carries the I baseband information and the Q baseband information from the corresponding images **7502** and **7504**, respectively, without substantially increasing the frequency bandwidth occupied by each harmonic **7506**. This can occur because the signal combiner **7408** phase shifts the Q signal **7411** b by 90 degrees relative to the I signal **7411***a*. The result is that the images **7502***a–n* and **7504***a–n* effectively share the signal bandwidth do to their orthogonal relationship. For example, the images **7502***a* and **7504***a* effectively share the frequency spectrum that is represented by the image **7506***a*.

In step **8712**, the optional filter **7414** can be included to select a harmonic of interest, as represented by the passband **7508** selecting the image **7506***c* in FIG. **75***c*.

In step **8714**, the optional amplifier **7416** can be included to amplify the harmonic (or harmonics) of interest prior to transmission.

In step **8716**, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. **76**A illustrates a transmitter **7608** that is a second embodiment for an I Q transmitter having a balanced configuration. Transmitter **7608** is similar to the transmitter **7420** except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays **7604***a* and **7604***b* delay the control signals **7123** and **7127** for the Q channel modulator **7104***b* by 90 degrees relative the control signals for the I channel modulator **7104***a*. As a result, the Q modulator **7104***b* samples the Q baseband signal **7404** with 90 degree delay relative to the sampling of the I baseband signal **7402** by the I channel modulator **7104***a*. Therefore, the Q harmonically rich signal **7411***b* is phase shifted by 90 degrees relative to the I harmonically rich signal. Since the phase shift is achieved using the control signals, an in-phase signal combiner **7606** combines the harmonically rich signals **7411***a* and **7411***b*, to generate the harmonically rich signal **7412**.

FIG. **76**B illustrates a transmitter **7618** that is similar to transmitter **7608** in FIG. **76**A. The difference being that the transmitter **7618** has a modulator **7620** that utilizes a summing node **7622** to sum the signals **7411***a* and **7411***b* instead of the in-phase signal combiner **7606** that is used in modulator **7602** of transmitter **7608**.

FIG. **90**A–**90**D illustrate various detailed circuit implementations of the transmitter **7420** in FIG. **74**. These circuit implementations are meant for example purposes only, and are not meant to be limiting.

FIG. **90**A illustrates I input circuitry **9002***a* and Q input circuitry **9002***b* that receive the I and Q input signals **7402** and **7404**, respectively.

FIG. **90**B illustrates the I channel circuitry **9006** that processes an I data **9004***a* from the I input circuit **9002***a*.

FIG. **90**C illustrates the Q channel circuitry **9008** that processes the Q data **9004***b* from the Q input circuit **9002***b*.

FIG. **90**D illustrates the output combiner circuit **9012** that combines the I channel data **9007** and the Q channel data **9010** to generate the output signal **7418**.

7.3.2.2 IQ Transmitter Using Shunt-Type Balanced Modulator

FIG. **80** illustrates an IQ transmitter **8000** that is another IQ transmitter embodiment according to the present invention. The transmitter **8000** includes an IQ balanced modulator **8001**, an optional filter **8012**, and an optional amplifier **8014**. During operation, the modulator **8001** up-converts an I baseband signal **8002** and a Q baseband signal **8004** to generate a combined harmonically rich signal **8011**. The harmonically rich signal **8011** includes multiple harmonics images, where each image contains the baseband information in the I signal **8002** and the Q signal **8004**. The optional bandpass filter **8012** may be included to select a harmonic of interest (or subset of harmonics) from the harmonically rich signal **8011** for transmission. The optional amplifier **8014** may be included to amplify the selected harmonic prior to transmission, to generate the IQ output signal **8016**.

The IQ modulator **8001** includes two shunt balanced modulators **7901** from FIG. **79**A, and a 90 degree signal combiner **8010** as shown. The operation of the IQ modulator **8001** is described in reference to the flowchart **8800** (FIG. **88**), as follows. The order of the steps in flowchart **8800** is not limiting.

In step **8802**, the balanced modulator **8001** receives the I baseband signal **8002** and the Q baseband signal **8004**.

In step **8804**, the balanced modulator **7901***a* differentially shunts the I baseband signal **8002** to ground according the control signals **7123** and **7127**, to generate a harmonically rich signal **8006**. More specifically, the UFT modules **7916***a* and **7922***a* alternately shunt the I baseband signal **8002** and an inverted version of the I baseband signal **8002** to ground according to the control signals **7123** and **7127**, respectively. The operation of the balanced modulator **7901** and the generation of harmonically rich signals was fully described above and is illustrated in FIGS. **79**A–C, to which the reader is referred for further details. As such, the harmonically rich signal **8006** contains multiple harmonic images of the I baseband information as described above.

In step **8806**, the balanced modulator **7901***b* differentially shunts the Q baseband signal **8004** to ground according to control signals **7123** and **7127**, to generate harmonically rich signal **8008**. More specifically, the UFT modules **7916***b* and **7922***b* alternately shunt the Q baseband signal **8004** and an inverted version of the Q baseband signal **8004** to ground, according to the control signals **7123** and **7127**, respectively. As such, the harmonically rich signal **8008** contains multiple harmonic images that contain the Q baseband information.

In step **8808**, the 90 degree signal combiner **8010** combines the harmonically rich signals **8006** and **8008** to generate IQ harmonically rich signal **8011**. This is further illustrated in FIGS. **81**A–C. FIG. **81**A depicts an exemplary frequency spectrum for the harmonically rich signal **8006** having harmonic images **8102***a–n*. The harmonic images **8102** repeat at harmonics of the sampling frequency $1/T_S$, where each image **8102** contains the necessary amplitude, frequency, and phase information to reconstruct the I baseband signal **8002**. Likewise, FIG. **81**B depicts an exemplary frequency spectrum for the harmonically rich signal **8008** having harmonic images **8104***a–n*. The harmonic images **8104***a–n* also repeat at harmonics of the sampling frequency $1/T_S$, where each image **8104** contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal **8004**. FIG. **81**C illustrates an exemplary frequency spectrum for the IQ harmonically rich signal **8011** having images **8106***a–n*. Each image **8106** carries the I baseband information and the Q baseband information from the corresponding images **8102** and **8104**, respectively, without substantially increasing the frequency bandwidth occupied by each image **8106**. This can occur because the signal combiner **8010** phase shifts the Q signal **8008** by 90 degrees relative to the I signal **8006**.

In step **8810**, the optional filter **8012** may be included to select a harmonic of interest, as represented by the passband **8108** selecting the image **8106***c* in FIG. **81**C.

In step **8812**, the optional amplifier **8014** can be included to amplify the selected harmonic image **8106** prior to transmission.

In step **8814**, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. **82** illustrates a transmitter **8200** that is another embodiment for an IQ transmitter having a balanced configuration. Transmitter **8200** is similar to the transmitter **8000** except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays **8204***a* and **8204***b* delay the control signals **7123** and **7127** for the Q channel modulator **7901***b* by 90 degrees relative the control signals for the I channel modulator **7901***a*. As a result, the Q modulator **7901***b* samples the Q baseband signal **8004** with a 90 degree delay relative to the sampling of the I baseband signal **8002** by the I channel modulator **7901***a*. Therefore, the Q harmonically rich signal **8008** is phase shifted by 90 degrees relative to the I harmonically rich signal **8006**. Since the phase shift is achieved using the control signals, an in-phase signal combiner **8206** combines the harmonically rich signals **8006** and **8008**, to generate the harmonically rich signal **8011**.

FIG. **83** illustrates a transmitter **8300** that is similar to transmitter **8200** in FIG. **82**. The difference being that the transmitter **8300** has a balanced modulator **8302** that utilizes a summing node **8304** to sum the I harmonically rich signal **8006** and the Q harmonically rich signal **8008** instead of the in-phase signal combiner **8206** that is used in the modulator **8202** of transmitter **8200**. The 90 degree phase shift between the I and Q channels is implemented by delaying the Q clock signals using 90 degree delays **8204**, as shown.

7.3.2.3 IQ Transmitters Configured for Carrier Insertion

The transmitters **7420** (FIG. **74**) and **7608** (FIG. **76**A) have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the IQ output signal **7418**. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter

efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, FIG. **77** illustrates a transmitter **7702** to provide any necessary carrier insertion by implementing a DC offset between the two sets of sampling UFT modules.

Transmitter **7702** is similar to the transmitter **7420** with the exception that a modulator **7704** in transmitter **7702** is configured to accept two DC reference voltages so that the I channel modulator **7104***a* can be biased separately from the Q channel modulator **7104***b*. More specifically, modulator **7704** includes a terminal **7706** to accept a DC voltage reference **7707**, and a terminal **7708** to accept a DC voltage reference **7709**. Voltage **7707** biases the UFT modules **7124***a* and **7128***a* in the I channel modulator **7104***a*. Likewise, voltage **7709** biases the UFT modules **7124***b* and **7128***b* in the Q channel modulator **7104***b*. When voltage **7707** is different from voltage **7709**, then a DC offset will appear between the I channel modulator **7104***a* and the Q channel modulator **7104***b*, which results in carrier insertion in the IQ harmonically rich signal **7412**. The relative amplitude of the carrier frequency energy increases in proportion to the amount of DC offset.

FIG. **78** illustrates a transmitter **7802** that is a second embodiment of an IQ transmitter having two DC terminals to cause DC offset, and therefore carrier insertion. Transmitter **7802** is similar to transmitter **7702** except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals, similar to that done in transmitter **7608**. More specifically, delays **7804***a* and **7804***b* phase shift the control signals **7123** and **7127** for the Q channel modulator **7104***b* relative to those of the I channel modulator **7104***a*. As a result, the Q modulator **7104***b* samples the Q baseband signal **7404** with 90 degree delay relative to the sampling of the I baseband signal **7402** by the I channel modulator **7104***a*. Therefore, the Q harmonically rich signal **7411***b* is phase shifted by 90 degrees relative to the I harmonically rich signal **7411***a*, which are combined by the in-phase combiner **7806**.

7.4 Transceiver Embodiments

Referring to FIG. **39**, in embodiments the receiver **3906**, transmitter **3910**, and LNA/PA **3904** are configured as a transceiver, such as but not limited to transceiver **9100**, that is shown in FIG. **91**.

Referring to FIG. **91**, the transceiver **9100** includes a diplexer **9108**, the IQ receiver **7000**, and the IQ transmitter **8000**. Transceiver **9100** up-converts an I baseband signal **9114** and a Q baseband signal **9116** using the IQ transmitter **8000** (FIG. **80**) to generate an IQ RF output signal **9106**. A detailed description of the IQ transmitter **8000** is included for example in section 7.3.2.2, to which the reader is referred for further details. Additionally, the transceiver **9100** also down-converts a received RF signal **9104** using the IQ Receiver **7000**, resulting in I baseband output signal **9110** and a Q baseband output signal **9112**. A detailed description of the IQ receiver **7000** is included in section 7.2.2, to which the reader is referred for further details.

7.5 Demodulator/Modulator Facilitation Module

An example demodulator/modulator facilitation module **3912** is shown in FIGS. **47** and **48**. A corresponding BOM list is shown in FIGS. **49**A and **49**B.

An alternate example demodulator/modulator facilitation module **3912** is shown in FIGS. **50** and **51**. A corresponding BOM list is shown in FIGS. **52**A and **52**B.

FIG. **52**C illustrates an exemplary demodulator/modulator facilitation module **5201**. Facilitation module **5201** includes the following: de-spread module **5204**, spread module **5206**, de-modulator **5210**, and modulator **5212**.

For receive, the de-spread module **5204** de-spreads received spread signals **3926** and **3928** using a spreading code **5202**. Separate spreading codes can be used for the I and Q channels as will be understood by those skilled in the arts. The demodulator **5210** uses a signal **5208** to demodulate the de-spread received signals from the de-spread module **5204**, to generate the I baseband signal **3930***a* and the Q baseband signal **3932***a*.

For transmit, the modulator **5212** modulates the I baseband signal **3930***b* and the Q baseband signal **3932***b* using a modulation signal **5208**. The resulting modulated signals are then spread by the spread module **5206**, to generate I spread signal **3942** and Q spread signal **3944**.

In embodiments, the modulation scheme that is utilized is differential binary phase shift keying (DBPSK) or differential quadrature phase shift keying (DQPSK), and is compliant with the various versions of IEEE 802.11. Other modulation schemes could be utilized besides DBPSK or DQPSK, as will understood by those skilled in arts based on the discussion herein.

In embodiments, the spreading code **5202** is a Barker spreading code, and is compliant with the various versions of IEEE 802.11. More specifically, in embodiments, an 11-bit Barker word is utilized for spreading/de-spreading. Other spreading codes could be utilized as will be understood by those skilled in the arts based on the discussion herein.

7.6 MAC Interface

An example MAC interface **3914** is shown in FIG. **45**. A corresponding BOM list is shown in FIGS. **46**A and **46**B.

In embodiments, the MAC **3918** and MAC interface **3914** supply the functionality required to provide a reliable delivery mechanism for user data over noisy, and unreliable wireless media. This is done this while also providing advanced LAN services, equal to or beyond those of existing wired LANs.

The first functionality of the MAC is to provide a reliable data delivery service to users of the MAC. Through a frame exchange protocol at the MAC level, the MAC significantly improves on the reliability of data delivery services over wireless media, as compared to earlier WLANs. More specifically, the MAC implements a frame exchange protocol to allow the source of a frame to determine when the frame has been successfully received at the destination. This frame exchange protocol adds some overhead beyond that of other MAC protocols, like IEEE 802.3, because it is not sufficient to simply transmit a frame and expect that the destination has received it correctly on the wireless media. In addition, it cannot be expected that every station in the WLAN is able to communicate with every other station in the WLAN. If the source does not receive this acknowledgment, then the source will attempt to transmit the frame again. This retransmission of frame by the source effectively reduces the effective error rate of the medium at the cost of additional bandwidth consumption.

The minimal MAC frame exchange protocol consists of two frames, a frame sent from the source to the destination and an acknowledgment from the destination that the frame was received correctly. The frame and its acknowledgment are an atomic unit of the MAC protocol. As such, they cannot be interrupted by the transmission from any other station. Additionally, a second set of frames may be added to the minimal MAC frame exchange. The two added frames are a request to send frame and a clear to send frame. The source sends a request to send to the destination. The destination returns a clear to send to the source. Each of these frames contains information that allows other stations

receiving them to be notified of the upcoming frame transmission, and therefore to delay any transmission their own. The request to send and clear frames serve to announce to all stations in the neighborhood of both the source and the destination about the pending transmission from the source to the destination. When the source receives the clear to send from the destination, the real frame that the source wants delivered to the destination is sent. If the frame is correctly received at the destination, then the destination will return an acknowledgment completing the frame exchange protocol. While this four way frame exchange protocol is a required function of the MAC, it may be disabled by an attribute in the management information base.

The second functionality of the MAC is to fairly control access to the shared wireless medium. It performs this function through two different access mechanisms: the basic access mechanism, call the distribution coordination system function, and a centrally controlled access mechanism, called the point coordination function.

The basic access mechanism is a carrier sense multiple access with collision avoidance (CSMA/CA) with binary exponential backoff. This access mechanism is similar to that used for IEEE 802.3, with some variations. CSMA/CA is a "listen before talk" (LBT) access mechanism. In this type of access mechanism, a station will listen to the medium before beginning a transmission. If the medium is already carrying a transmission, then the station that listening will not begin its own transmission. More specifically, if a listening station detects an existing transmission in progress, the listening station enters a transmit deferral period determined by the binary exponential backoff algorithm. The binary exponential backoff mechanism chooses a random number which represents the amount of time that must elapse while there are not any transmission. In other words, the medium is idle before the listening station may attempt to begin its transmission again. The MAC may also implement a network allocation vector (NAV). The NAV is the value that indicates to a station that amount of time that remains before a medium becomes available. The NAV is kept current through duration values that are transmitted in all frames. By examining the NAV, a station may avoid transmitting, even when the medium does not appear to be carrying a transmission in the physical sense.

The centrally controlled access mechanism uses a poll and response protocol to eliminate the possibility of contention for the medium. This access mechanism is called the point coordination function (PCF). A point coordinator (PC) controls the PCF. The PC is always located in an AP. Generally, the PCF operates by stations requesting that the PC register them on a polling list, and the PC then regularly polls the stations for traffic while also delivering traffic to the stations. With proper planning, the PCF is able to deliver near isochronous service to the stations on the polling list.

The third function of the MAC is to protect the data that it delivers. Because it is difficult to contain wireless WLAN signals to a particular physical area, the MAC provides a privacy service, called Wired Equivalent Privacy (WEP), which encrypts the data sent over the wireless medium. The level of encryption chosen approximates the level of protection data might have on a wireless LAN in a building with controlled access that prevents physically connecting to the LAN without authorization.

7.7 Control Signal Generator—Synthesizer

In an embodiment, the control signal generator **3908** is preferably implemented using a synthesizer. An example synthesizer is shown in FIG. **55**. A corresponding BOM list is shown in FIGS. **56**A and **56**B.

7.8 LNA/PA

An example LNA/PA **3904** is shown in FIGS. **64** and **65**. A corresponding BOM list is shown in FIG. **66**.

Additionally, FIG. **93** illustrates a LNA/PA module **9301** that is another embodiment of the LNA/PA **3904**. LNA/PA module **9301** includes a switch **9302**, a LNA **9304**, and a PA **9306**. The switch **9302** connects either the LNA **9304** or the PA **9306** to the antenna **3903**, as shown. The switch **9302** can be controlled by an on-board processor that is not shown.

8.0 802.11 Physical Layer Configurations

The 802.11 WLAN standard specifies two RF physical layers: frequency hopped spread spectrum (FHSS) and direct sequence spread spectrum (DSSS). The invention is not limited to these specific examples. Both DSSS and FHSS support 1 Mbps and 2 Mbps data rates and operate in the 2.400–2.835 GHz band for wireless communications in accordance to FCC part 15 and ESTI-300 rules. Additionally, 802.11 has added an 11 Mbps standard that operates at 5 GHz and utilizes OFDM modulation.

The DSSS configuration supports the 1 MBPS data rate utilizing differential binary phase shift keying (DBPSK) modulation, and supports 2 MBPS utilizing differential quadrature phase shift keying modulation. In embodiments, an 11-bit Barker word is used as the spreading sequence that is utilized by the stations in the 802.11 network. A Barker word has a relatively short sequence, and is known to have very good correlation properties, and includes the following sequence: +1, −1, +1, +1, −1, +1, +1, +1, −1, −1, −1. The Barker word used for 802.11 is not to be confused with the spreading codes used for code division multiple access (CDMA) and global positioning system (GPS). CDMA and GPS use orthogonal spreading codes, which allow multiple users to operate on the same channel frequency. Generally, CDMA codes have longer sequences and have richer correlation properties.

During transmission, the 11-bit barker word is exclusive-ored (EX-OR) with each of the information bits using a modulo-2 adder, as illustrated by modulo-2 adder **9202** in FIG. **92**. Referring to FIG. **92**, the11-bit (at 11 MBPS) Barker word is applied to a modulo-2 adder together with each one (at 1 MBPS) of the information bits (in the PPDU data). The Ex-OR function combines both signals by performing a modulo-2 addition of each information bit with each Barker bit (or chip). The output of the modulo-2 adder results in a signal with a data rate that is 10× higher than the information rate. The result in the frequency domain signal is a signal that is spread over a wider bandwidth at a reduced RF power level. At the receiver, the DSSS signal is convolved with an 11-bit Barker word and correlated. As shown in FIG. **92**, the correlation recovers the information bits at the transmitted information rate, and the undesired interfering in-band signals are spread out-of-band. The spreading and despreading of narrowband to wideband signal is commonly referred to as processing gain and is measured in decibels (dB). Processing gain is the ratio of DSSS signal rate information rate. In embodiments, the minimum requirement for processing gain is 10 dB.

The second RF physical layer that is specified by the IEEE 802.11 standard is frequency hopping spread spectrum (FHSS). A set of hop sequences is defined in IEEE 802.11 for use in the 2.4 GHz frequency band. The channels are evenly spaced across the band over a span of 83.5 MHz. During the development of IEEE 802.11, the hop sequences listed in the standard were pre-approved for operation in North America, Europe, and Japan. In North America and Europe (excluding Spain and France), the required number of hop channels is 79. The number of hopped channels for

Spain and France is 23 and 35, respectively. In Japan, the required number of hopped channels is 23. The hopped center channels are spaced uniformly across the 2.4 GHz frequency band occupying a bandwidth of 1 MHz. In North America and Europe (excluding Spain and France), the hopped channels operate from 2.402 GHz to 2.480 GHz. In Japan, the hopped channels operate from 2.447 GHz to 2.473 GHz. The modulation scheme called out for FHSS by 802.11 is 2-level Gaussian Phase Shift Keying (GFSK) for the 1 MBps data rate, and 4-level GFSK for the 2 MBps data rate.

In addition to DSSS and FHSS RF layer standards, the IEEE 802.11 Executive Committee approved two projects for higher rate physical layer extensions. The first extension, IEEE 802.11a defines requirements for a physical layer operating in the 5.0 GHz frequency band, and data rates ranging from 6 MBps to 54 MBps. This 802.11a draft standard is based on Orthogonal Frequency Division Multiplexing (OFDM) and uses 48 carriers as a phase reference (so coherent), with 20 MHZ spacing between the channels. The second extension, IEEE 802.11b, defines a set of physical layer specifications operating in the 2.4 GHz ISM frequency band. This 802.11b utilizes complementary code keying (CCK), and extends the data rate up to 5.5 Mbps and 11 Mbps.

The transmitter and receiver circuits described herein can be operated in all of the WLAN physical layer embodiments described herein, including the DSSS and FHSS embodiments described herein. However, the present invention is not limited to being operated in WLAN physical layer embodiments that were described herein, as the invention could be configured in other physical layer embodiments.

FIG. **94** illustrates a block diagram of an IEEE 802.11 DSSS radio transceiver **9400** using UFT Zero IF technology. DSSS transceiver **9400** includes: antenna **9402**, switch **9404**, amplifiers **9406** and **9408**, transceivers **9410**, baseband processor **9412**, MAC **9414**, bus interface unit **9416**, and PCMCIA connector **9418**. The DSSS transceiver **9400** includes an IQ receiver **7000** and an IQ transmitter **8000**, which are described herein. UFT technology interfaces directly to the baseband processor **9412** of the physical layer. In the receive path, the IQ receiver **7000** transforms a 2.4 GHz RF signal-of-interest into I/Q analog baseband signals in a single step and passes the signals to the baseband processor **9412**, where the baseband processor is then responsible for de-spreading and demodulating the signal. In embodiments, the IQ receiver **7000** includes all of the circuitry necessary for accommodating AGC, baseband filtering and baseband amplification. In the transmit path, the transmitter **8000** transforms the I/Q analog baseband signals to a 2.4 GHz RF carrier directly in a single step. The signal conversion clock is derived from a single synthesized local oscillator (LO) **9420**. The selection of the clock frequency is determined by choosing a sub-harmonic of the carrier frequency. For example, a 5th harmonic of 490 MHZ was used, which corresponds to a RF channel frequency of 2.450 GHz. Using UFT technology simplifies the requirements and complexity of the synthesizer design.

9. Appendix

The attached Appendix contained in FIGS. **95**A–C, **96**–**161**, which forms part of this patent application, includes schematics of an integrated circuit (IC) implementation example of the present invention. This example embodiment is provided solely for illustrative purposes, and is not limiting. Other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings herein. FIG. **95**A illustrates a schematic for a WLAN modulator/demodulator IC according to embodiments of the invention. FIGS. **95**B and **95**C illustrate an expanded view of the circuit in FIG. **95**A. FIGS. **96**–**161** further illustrate detailed circuit schematics of the WLAN modulator/demodulator integrated circuit.

10. Conclusions

Example implementations of the systems and components of the invention have been described herein. As noted elsewhere, these example implementations have been described for illustrative purposes only, and are not limiting. Other implementation embodiments are possible and covered by the invention, such as but not limited to software and software/hardware implementations of the systems and components of the invention. Such implementation embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

While various application embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What is claimed is:

1. A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

wherein said second control signal is delayed relative to said first control signal by (0.5+n) cycles of said input signal, wherein n is an integer greater than or equal to 1.

2. A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

wherein said first frequency down-conversion module under-samples said input signal according to said first control signal, and said second frequency down-conversion module under-samples said input signal according to said second control signal.

3. A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

wherein said first and said second frequency down-conversion modules each comprise a switch and a storage element.

4. The apparatus of claim 3, wherein said storage elements comprises a capacitor that reduces a DC offset voltage in said first down-converted signal and said second down-converted signal.

5. The apparatus of claim 1, wherein said subtractor module comprises a differential amplifier.

6. A wireless modem apparatus, comprising:

a receiver for frequency down-converting an input signal including,

a first frequency down-conversion module to down-convert the input signal, wherein said first frequency down-conversion module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second frequency down-conversion module to down-convert said input signal, wherein said second frequency down-conversion module down-converts said input signal according to a second control signal and outputs a second down-converted signal;

a subtractor module that subtracts said second down-converted signal from said first down-converted signal and outputs a down-converted signal;

a transmitter for up-converting a baseband signal and coupled to said receiver, including,

an inverter, to receive said baseband signal and generate an inverted baseband signal;

a first controlled switch, coupled to a non-inverting output of said inverter, said first controlled switch to sample said baseband signal according to a third control signal, resulting in a first harmonically rich signal;

a second controlled switch, coupled to an inverting output of said inverter, said second controlled switch to sample said inverted baseband signal according to a fourth control signal, resulting in a second harmonically rich signal; and

a combiner, coupled to an output of said first controlled switch and an output of said second controlled switch, said combiner to combine said first harmonically rich signal and said second harmonically rich signal, resulting in a third harmonically rich signal.

7. The apparatus of claim 6, wherein said fourth control signal is phase shifted with respect to said third control signal.

8. The apparatus of claim 6, wherein said fourth control signal is phase shifted by 180 degrees with respect to said third control signal.

9. The apparatus of claim 6, further comprising a filter coupled to an output of said combiner, wherein said filter outputs a desired harmonic from said third harmonically rich signal.

10. The apparatus of claim 6, wherein said apparatus is an infrastructure device.

11. The apparatus of claim 6, wherein said apparatus is a client device.

12. The apparatus of claim 6, wherein said first controlled switch shunts said baseband signal to a reference potential according to said third control signal, and wherein said second controlled switch shunts said inverted baseband signal to said reference potential according to said fourth control signal.

13. The apparatus of claim 6, further comprising an antenna coupled to said transmitter and said receiver.

14. The apparatus of claim 13, further comprising a switch, said switch selectively connecting said transmitter or said receiver to said antenna.

15. The apparatus of claim 6, further comprising a baseband processor coupled to said transmitter and said receiver.

16. The apparatus of claim 6, further comprising a media access controller (MAC) coupled to said transmitter and said receiver.

17. The apparatus of claim 16, wherein said MAC comprises a means for controlling accessing to a WLAN medium.

18. The apparatus of claim 17, wherein said means for controlling includes carrier sense multiple access with collision avoidance (CSMA/CA).

19. The apparatus of claim 6, further comprising a demodulator/modulator facilitation module coupled to said transmitter and receiver.

20. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using differential binary phase shift keying (DBPSK).

21. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down-converted signal using differential binary phase shift keying (DBPSK).

22. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for spreading said baseband signal.

23. The apparatus of claim 22, wherein said means for spreading comprises a means for spreading said baseband signal using a Barker code.

24. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for de-spreading said down-converted signal.

25. The apparatus of claim 24, wherein said means for de-spreading comprises a means for de-spreading said down-converted signal using a Barker code.

26. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using Gaussian phase shift keying (GPSK).

27. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Gaussian phase shift keying (GPSK).

28. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for modulating said baseband signal using Orthogonal Frequency Division Multiplexing (OFDM).

29. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Orthogonal Frequency Division Multiplexing (OFDM).

30. The apparatus of claim 19, wherein said demodulator/modulator facilitation module comprises a means for modu-

lating said baseband signal using Complimentary Code Keying (CCK).

31. The apparatus of claim **19**, wherein said demodulator/modulator facilitation module comprises a means for de-modulating said down converted signal using Complimentary Code Keying (CCK).

32. In a wireless LAN device, a method of down-converting a received RF signal, comprising:

down-converting said received RF signal according to a first control signal and a second control signal, resulting in a down-converted signal, wherein said second control signal is delayed relative to said first control signal by (0.5+n) cycles of said received RF signal, wherein n is an integer greater than or equal to 1;

de-spreading said down-converted signal using a spreading code, resulting in a de-spread signal; and

de-modulating said de-spread signal, resulting in a de-modulated signal.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

ON TITLE PAGE

Item (56)

Under "U.S. Patent Documents", please insert the following citations:

4,870,659	09/1989	Oishi et al.
4,871,987	10/1989	Kawase
4,885,587	12/1989	Wiegand et al.
4,885,756	12/1989	Fontanes et al.
4,888,557	12/1989	Puckette, IV et al.
4,890,302	12/1989	Muilwijk
4,893,316	01/1990	Janc et al.
4,893,341	01/1990	Gehring
4,894,766	01/1990	De Agro
4,896,152	01/1990	Tiemann
4,902,979	02/1990	Puckette, IV
4,908,579	03/1990	Tawfik et al.
4,910,752	03/1990	Yester, Jr. et al.
4,914,405	04/1990	Wells
4,920,510	04/1990	Senderowicz et al.
4,922,452	05/1990	Larsen et al.
4,931,921	06/1990	Anderson
4,944,025	07/1990	Gehring et al.
4,955,079	09/1990	Connerney et al.
4,965,467	10/1990	Bilterijst
4,967,160	10/1990	Quievy et al.
4,970,703	11/1990	Hariharan et al.
4,982,353	01/1991	Jacob et al.
4,984,077	01/1991	Uchida
4,995,055	02/1991	Weinberger et al.
5,003,621	03/1991	Gailus
5,005,169	04/1991	Bronder et al.
5,006,810	04/1991	Popescu
5,010,585	04/1991	Garcia
5,014,304	05/1991	Nicollini et al.
5,015,963	05/1991	Sutton
5,017,924	05/1991	Guiberteau et al.
5,020,149	05/1991	Hemmie
5,020,154	05/1991	Zierhut
5,052,050	09/1991	Collier et al.
5,065,409	11/1991	Hughes et al.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Item (56)

Under "Foreign Patent Documents", please insert the following citations:

JP 6-237276	08/1994
JP 8-23359	01/1996
JP 47-2314	02/1972
JP 58-7903	01/1983
JP 58-133004	08/1983
JP 60-58705	04/1985
JP 4-123614	04/1992
JP 4-127601	04/1992
JP 5-175730	07/1993
JP 5-175734	07/1993
JP 7-154344	06/1995
JP 7-307620	11/1995
JP 55-66057	05/1980
JP 63-65587	03/1988
JP 63-153691	06/1988
EP 0 276 130 A2&A3	07/1988

Under "Other Publications", please insert the following citations:

Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).

Kirsten, J. and Fleming, J., "Undersampling reduces data-acquisition costs for select applications," *EDN*, Cahners Publishing, Vol. 35, No. 13, pp. 217-222, 224, 226-228 (June 21, 1990).

Lam, W.K. *et al.*, "Measurement of the Phase Noise Characteristics of an Unlocked Communications Channel Identifier," *Proceedings Of the 1993 IEEE International Frequency Control Symposium*, IEEE, pp. 283-288 (June 2-4, 1993).

Lam, W.K. *et al.*, "Wideband sounding of 11.6 Ghz transhorizon channel," *Electronics Letters*, IEE, Vol. 30, No. 9, pp. 738-739 (April 28, 1994).

Larkin, K.G, "Efficient demodulator for bandpass sampled AM signals," *Electronics Letters*, IEE, Vol. 32, No. 2, pp. 101-102 (January 18, 1996).

Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).

Lau, W.H. *et al.*, "Improved Prony Algorithm to Identify Multipath Components," *Electronics Letters*, IEE, Vol. 23, No. 20, pp. 1059-1060 (September 24, 1987).

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Item (56)

Under "Other Publications", please insert the following citations (cont'd):

Lesage, P. and Audoin, C., "Effect of Dead-Time on the Estimation of the Two-Sample Variance," *IEEE Transactions on Instrumentation and Measurement*, IEEE Instrumentation and Measurement Society, Vol. IM-28, No. 1, pp. 6-10 (March 1979).

Liechti, C.A., "Performance of Dual-gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. MTT-23, No. 6, pp. 461-469 (June 1975).

Linnenbrink, T.E. et al., "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No, 4, pp. 4443-4449 (August 1979).

Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).

Lo, P. *et al.*, "Coherent Automatic Gain Control," *IEE Colloquium on Phase Locked Techniques*, IEE, pp. 2/1-2/6 (March 26, 1980).

Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).

Lo, P.S.L.O. *et al.*, "Observations of Amplitude Scintillations on a Low-Elevation Earth-Space Path," *Electronics Letters*, IEE, Vol. 20, No. 7, pp. 307-308 (March 29, 1984).

Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).

Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).

Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).

Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

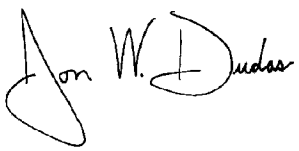
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Section (56)
Under "Other Publications", please insert the following citations (cont'd):

McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

Signed and Sealed this

Seventh Day of August, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

ON TITLE PAGE

Item (56)

Under "U.S. Patent Documents", please insert the following citations:

4,870,659	09/1989	Oishi et al.
4,871,987	10/1989	Kawase
4,885,587	12/1989	Wiegand et al.
4,885,756	12/1989	Fontanes et al.
4,888,557	12/1989	Puckette, IV et al.
4,890,302	12/1989	Muilwijk
4,893,316	01/1990	Janc et al.
4,893,341	01/1990	Gehring
4,894,766	01/1990	De Agro
4,896,152	01/1990	Tiemann
4,902,979	02/1990	Puckette, IV
4,908,579	03/1990	Tawfik et al.
4,910,752	03/1990	Yester, Jr. et al.
4,914,405	04/1990	Wells
4,920,510	04/1990	Senderowicz et al.
4,922,452	05/1990	Larsen et al.
4,931,921	06/1990	Anderson
4,944,025	07/1990	Gehring et al.
4,955,079	09/1990	Connerney et al.
4,965,467	10/1990	Bilterijst
4,967,160	10/1990	Quievy et al.
4,970,703	11/1990	Hariharan et al.
4,982,353	01/1991	Jacob et al.
4,984,077	01/1991	Uchida
4,995,055	02/1991	Weinberger et al.
5,003,621	03/1991	Gailus
5,005,169	04/1991	Bronder et al.
5,006,810	04/1991	Popescu
5,010,585	04/1991	Garcia
5,014,304	05/1991	Nicollini et al.
5,015,963	05/1991	Sutton
5,017,924	05/1991	Guiberteau et al.
5,020,149	05/1991	Hemmie
5,020,154	05/1991	Zierhut
5,052,050	09/1991	Collier et al.
5,065,409	11/1991	Hughes et al.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Item (56)

Under "Foreign Patent Documents", please insert the following citations:

JP 6-237276	08/1994
JP 8-23359	01/1996
JP 47-2314	02/1972
JP 58-7903	01/1983
JP 58-133004	08/1983
JP 60-58705	04/1985
JP 4-123614	04/1992
JP 4-127601	04/1992
JP 5-175730	07/1993
JP 5-175734	07/1993
JP 7-154344	06/1995
JP 7-307620	11/1995
JP 55-66057	05/1980
JP 63-65587	03/1988
JP 63-153691	06/1988
EP 0 276 130 A2&A3	07/1988

Under "Other Publications", please insert the following citations:

Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).

Kirsten, J. and Fleming, J., "Undersampling reduces data-acquisition costs for select applications," *EDN*, Cahners Publishing, Vol. 35, No. 13, pp. 217-222, 224, 226-228 (June 21, 1990).

Lam, W.K. *et al.*, "Measurement of the Phase Noise Characteristics of an Unlocked Communications Channel Identifier," *Proceedings Of the 1993 IEEE International Frequency Control Symposium*, IEEE, pp. 283-288 (June 2-4, 1993).

Lam, W.K. *et al.*, "Wideband sounding of 11.6 Ghz transhorizon channel," *Electronics Letters*, IEE, Vol. 30, No. 9, pp. 738-739 (April 28, 1994).

Larkin, K.G, "Efficient demodulator for bandpass sampled AM signals," *Electronics Letters*, IEE, Vol. 32, No. 2, pp. 101-102 (January 18, 1996).

Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).

Lau, W.H. *et al.*, "Improved Prony Algorithm to Identify Multipath Components," *Electronics Letters*, IEE, Vol. 23, No. 20, pp. 1059-1060 (September 24, 1987).

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Item (56)

Under "Other Publications", please insert the following citations (cont'd):

Lesage, P. and Audoin, C., "Effect of Dead-Time on the Estimation of the Two-Sample Variance," *IEEE Transactions on Instrumentation and Measurement*, IEEE Instrumentation and Measurement Society, Vol. IM-28, No. 1, pp. 6-10 (March 1979).

Liechti, C.A., "Performance of Dual-gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. MTT-23, No. 6, pp. 461-469 (June 1975).

Linnenbrink, T.E. et al., "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No, 4, pp. 4443-4449 (August 1979).

Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).

Lo, P. *et al.*, "Coherent Automatic Gain Control," *IEE Colloquium on Phase Locked Techniques*, IEE, pp. 2/1-2/6 (March 26, 1980).

Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).

Lo, P.S.L.O. *et al.*, "Observations of Amplitude Scintillations on a Low-Elevation Earth-Space Path," *Electronics Letters*, IEE, Vol. 20, No. 7, pp. 307-308 (March 29, 1984).

Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).

Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).

Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).

Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,110,444 B1
APPLICATION NO. : 09/632856
DATED : September 19, 2006
INVENTOR(S) : Sorrells et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

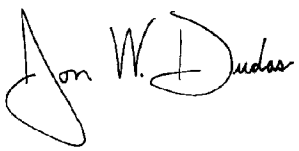
Section (56)
Under "Other Publications", please insert the following citations (cont'd):

McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

This certificate supersedes Certificate of Correction issued August 7, 2007.

Signed and Sealed this

Twenty-eighth Day of August, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

Case Number: 22-1548

Short Case Caption: PARKERVISION, INC. v. INTEL CORP.

Instructions: When computing a word, line, or page count, you may exclude any items listed as exempted under Fed. R. App. P. 5(c), Fed. R. App. P. 21(d), Fed. R. App. P. 27(d)(2), Fed. R. App. P. 32(f), or Fed. Cir. R. 32(b)(2).

The foregoing filing complies with the relevant type-volume limitation of the Federal Rules of Appellate Procedure and Federal Circuit Rules because it meets one of the following:

☑ the filing has been prepared using a proportionally-spaced typeface and includes 13,954 words.

☐ the filing has been prepared using a monospaced typeface and includes _____ lines of text.

☐ the filing contains _____ pages / _____ words / _____ lines of text, which does not exceed the maximum authorized by this court's order (ECF No. _____).

Date: 07/15/2022

Signature: /s/ Ronald M. Daignault

Name: Ronald M. Daignault

Save for Filing