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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/019,437	03/01/2024	6266518	0137616-0000005	6423
182086	7590	12/23/2024	EXAMINER	
DAIGNAULT IYER LLP			NGUYEN, MINH DIEU T	
8229 Boone Boulevard				
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VIENNA, VA 22182				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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***EX PARTE* REEXAMINATION COMMUNICATION TRANSMITTAL FORM**

REEXAMINATION CONTROL NO. 90/019,437 .

PATENT UNDER REEXAMINATION 6266518 .

ART UNIT 3992 .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Intent to Issue Ex Parte Reexamination Certificate	Control No. 90/019,437	Patent Under Reexamination 6266518	
	Examiner MINH DIEU T NGUYEN	Art Unit 3992	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of
 - (a) ☒ Patent owner's communication(s) filed: 11/12/2024.
 - (b) ☐ Patent owner's failure to file an appropriate timely response to the Office action mailed: ____.
 - (c) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
 - (d) ☐ The decision on appeal by the ☐ Board of Patent Appeals and Interferences ☐ Court dated ____
 - (e) ☐ Other: ____.
2. The Reexamination Certificate will indicate the following:
 - (a) Change in the Specification: ☐ Yes ☒ No
 - (b) Change in the Drawing(s): ☐ Yes ☒ No
 - (c) Status of the Claim(s):
 - (1) Patent claim(s) confirmed: 2-3,8,10,13-15,19,27,29,32,34 and 46-48.
 - (2) Patent claim(s) amended (including dependent on amended claim(s)): ____
 - (3) Patent claim(s) canceled: 1,82 and 90-91.
 - (4) Newly presented claim(s) patentable: ____.
 - (5) Newly presented canceled claims: ____.
 - (6) Patent claim(s) ☐ previously ☐ currently disclaimed: ____
 - (7) Patent claim(s) not subject to reexamination: 4-7,9,11-12,16-18,20-26,28,30-31,33,35-45,49-81,83-89 and 92-99.
3. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
4. ☒ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."
5. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).
6. ☒ Note attached LIST OF REFERENCES CITED (PTO/SB/08 or PTO/SB/08 substitute).
7. ☐ The drawing correction request filed on ____ is: ☐ approved ☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the certified copies have
 - ☐ been received.
 - ☐ not been received.
 - ☐ been filed in Application No. ____.
 - ☐ been filed in reexamination Control No. ____.
 - ☐ been received by the International Bureau in PCT Application No. ____.

* Certified copies not received: ____.
9. ☐ Note attached Examiner's Amendment.
10. ☐ Note attached Interview Summary (PTO-474).
11. ☐ Other: ____.

All correspondence relating to this reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

/MINH DIEU NGUYEN/ Primary Examiner, Art Unit 3992	
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cc: Requester (if third party requester)

NOTICE OF INTENT TO ISSUE REEXAMINATION CERTIFICATE

This Notice of Intent to Issue an *Ex Parte* Reexamination Certificate ("NIRC") is for claims 2-3, 8, 10, 13-15, 19, 27, 29, 32, 34 and 46-48 to Sorrells et al. ("the '518 Patent"), which were subject to *Ex parte* Reexamination.

Statement of Reasons for Confirmation

Claims 2-3, 8, 10, 13-15, 19, 27, 29, 32, 34 and 46-48 are confirmed.

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

I) Regarding claims 29, 32 and 34 not anticipated by Avitabile reference:

1) Avitabile does not disclose "integrating the energy over the aperture periods".

Avitabile discloses a sample-and-hold (voltage sampling) system.

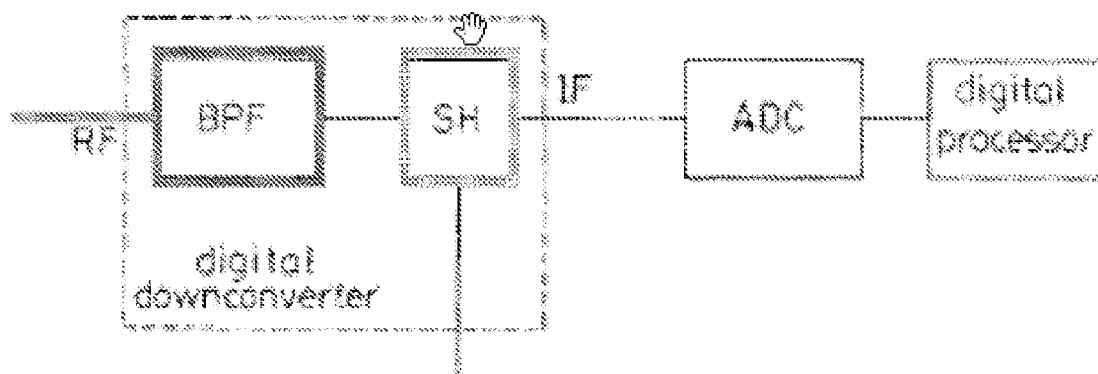


Fig. 1 *Schematic diagram*

Specifically, Avitabile describes a “digital downconverter configuration which performs complex detection by means of the sample-and-hold (SH) in a single step by using a single-channel configuration. The key element of the down-converter is a very fast sampling circuit directly operating within the S-band.” (page 337).

In Fig. 1, Avitabile discloses a block diagram of the digital down-converter configuration, including a bandpass filter (BPF) and sample-and-hold (SH) circuit. An incoming signal is filtered through a BPF and directed to the SH circuit for complex sampling. After sampling, the signal is fed to an A/D converter (ADC) for digital conversion. “As the digital conversion requires each sample to be held to a fixed value during the conversion interval, it is convenient to perform both sampling and holding operations in one step at this point. Both operations can be performed by using an SH circuit.” (page 338).

A POSITA would understand that an ADC has a high input impedance so that it can accurately measure the voltage on its input and convert this voltage into a digital signal. Therefore, a POSITA would recognize that no energy flows into the ADC or forms part of the baseband signal.

In Fig. 2, Avitabile illustrates a SH circuit including a switch, a hold capacitor (C) and load (R_L). A POSITA would understand that R_L is designed to have very high impedance, as a “buffer stage” following the SH circuit is intended to buffer the signal. This buffering function isolates the input from the output, ensuring that the signal is not disturbed by downstream components. Moreover, the buffer does not allow energy to

flow through it, rather it reads the voltage at its input and then produces that voltage at its output, isolating the output from the input.

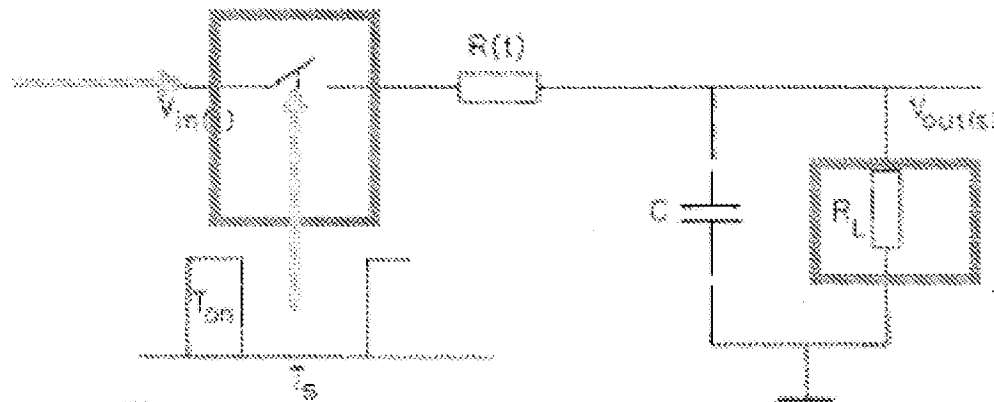


Fig. 2 *Equivalent circuit model in sampling mode*

Avitabile discusses two implementations for voltage sampling: (i) impulse sampling and (ii) track-and-hold (TH). In either implementation, an input signal is received by the switch. The switch is turned ON (closed) by sending a pulse to the switch. When the switch is ON (closed), the input signal is sent to the “hold” capacitor. When the switch is OFF (opened) the voltage at the output is held at a constant voltage level so that an ADC can read its value. A POSITA would understand that the R_L is a high impedance load, because Avitabile specifically states that “at the time the switch is turned off, nominally the whole of the input waveform drops across the hold capacitor.” (page 339). A POSITA understands that in order to hold voltage on the capacitor, R_L must be a high impedance load. The high impedance load prevents the holding capacitor from discharging.

Avitabile discloses two different SH prototypes (Fig. 4 and Fig. 8). Both prototypes follow the same operation as the SH circuit described above. In the “hold mode”, both prototypes are designed to prevent discharge from the hold capacitor C_H .

Avitabile’s system is a sample-and-hold (voltage sampling) system and the capacitor is a hold capacitor. As a sample-and-hold (voltage sampling) system, a POSITA would understand that Avitabile seeks to (i) accurately capture the voltage of the input signal at the sampling instant and (ii) hold the voltage reading on the capacitor to recreate a down-converted signal.

In order to achieve accurate voltage readings of the input signal, however, the capacitor in Avitabile cannot “integrat[e] the energy over the aperture periods,” as required by claim 29. Instead, the sample-and-hold (voltage sampling) system of Avitabile captures discrete voltage values of the input signal. The voltage held on the capacitor represents the instantaneous voltage of the input signal at that specific sample, not a cumulative value derived from energy integrated over aperture periods.

Avitabile’s sample-and-hold (voltage sampling) system is the one in which each voltage sample is independent of the previous one, so integrating (accumulating) energy over multiple aperture periods would distort the voltage representation of the input signal at each sampling instance, preventing an accurate reading of voltage and thus, preventing the baseband signal from being accurately recreated.

Accordingly, Avitabile does not teach “integrating the energy over the aperture periods”.

2) Avitabile does not disclose "generating the second signal from the integrated energy".

As discussed above, in Avitabile's voltage sampling system, the voltage across the capacitor is a snapshot of the sampled input signal at a discrete moment in time. It is recognized that this voltage is not derived from energy "integrated" (accumulated) over multiple aperture periods, but rather represents the input signal's instantaneous voltage captured at the sampling instant. Specifically, the voltage is held on the capacitor by using a high impedance load. During a "hold" period, the voltage is held at a constant voltage level so that the ADC can read its value. In other words, during the hold time, Avitabile is designed to prevent discharge from the hold capacitor. The voltage value serves as the "sample" of a discrete voltage value that the system can then use to recover the baseband signal. Thus, Avitabile is not using energy (integrated) to generate the claimed second signal. Instead, Avitabile generates a second signal based on repetitive readings of voltage values. This is different than an energy transfer (energy sampling) system, which uses the energy from the input signal provided to a low impedance load to generate a second signal (i.e., the sampled energy makes up/becomes part of the second signal).

Accordingly, Avitabile does not teach "generating a second signal from the integrated energy" as claimed.

II) Regarding claims 29, 32 and 34 not anticipated by Hulkko reference:

Hulkko discloses a sigma-delta analog-digital converter implemented in a receive arrangement of a radio phone (3:48-52).

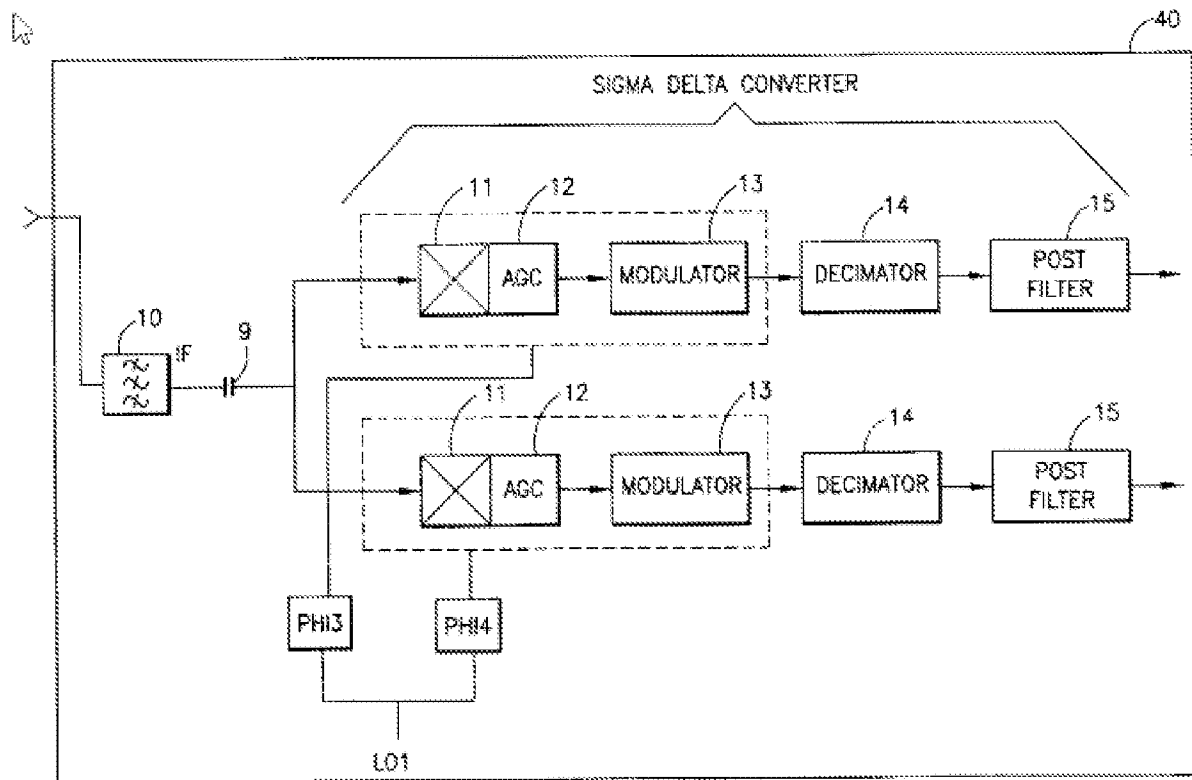


FIG.2

In Fig. 2, Hulkko illustrates a block diagram of a sigma-delta converter included in a receiver. The incoming signal is filtered through a bandpass filter 10, thereby producing an IF signal that is provided to each branch of the sigma-delta converter. In each branch, the IF signal is directed to a mixer 11 comprised of "switched capacitor switching elements 30-39 illustrated in FIG. 4" (3:48-52). The mixer 11 is driven by a square wave local oscillator signal (LO1) at the frequency of the IF signal or a subharmonic thereof. (4:26-27).

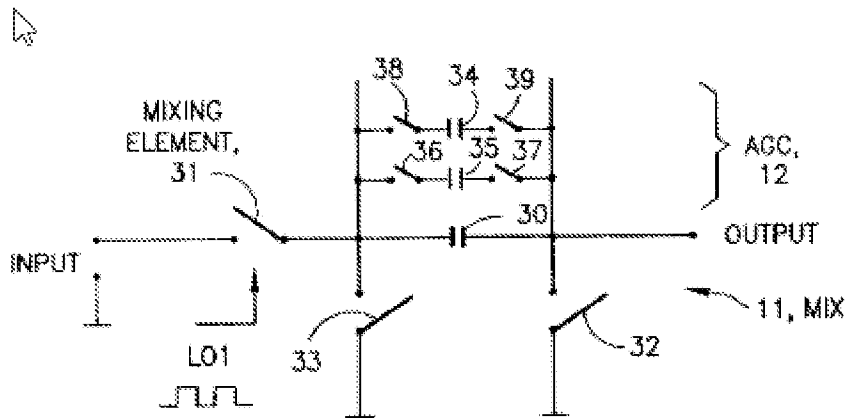


FIG.4

Fig. 4 illustrates the switched capacitor sample-and-hold circuitry of mixer 11 and automatic gain controller (AGC) 12. Hulkko describes mixer 11 "can be considered as a sample and hold circuit that samples the input signal in synchronization with the oscillator and directs the samples to the output as a signal which remains constant for the period of the sampling interval." (5:13-17).

The mixer circuit includes switches 31, 32, 33 and a capacitor 30 "used to sample and hold the incoming signal (4:61-5:12). Mixer 11 samples the IF input signal by closing switches 31 and 32. This causes capacitor 30 to develop a positive charge on the left-hand plate and negative charge on the right-hand plate. Once the IF signal has been sampled, switches 31, 32 open and switch 33 closes. This configuration presents the negative charge on the right-side plate of capacitor 30 to the output.

1) Hulkko does not disclose "integrating the energy over the aperture periods".

Hulkko's system is a sample-and-hold (voltage sampling) system with capacitor 30 as a sample-and-hold capacitor and the mixer 11 as a sample and hold circuit. As a sample-and-hold (voltage sampling) system, a POSITA would understand that Hulkko seeks to (i) accurately capture the voltage of the input signal at the sampling instant and (ii) use the voltage reading in capacitor 30 to recreate a down-converted signal.

In order to achieve accurate voltage readings of the input signal, however, the capacitor 30 cannot "integrat[e] the energy over the aperture periods," as required by claim 29. Instead, for each sample, the sample-and-hold (voltage sampling) system of Hulkko captures discrete voltage values of the input signal. It is the individual readings of voltage that is used to recreate the baseband signals.

The voltage held on the capacitor represents the instantaneous voltage of the input signal at that specific sample, not a cumulative value derived from energy integrated over aperture periods.

Fig. 4 illustrates the mixer circuitry, where switches 31, 32 and 33 control capacitor 30 to "sample and hold the incoming signal" (4:64-65). When switches 31 and 32 close, capacitor 30 samples the incoming IF signal, creating a voltage across its plates. Hulkko explicitly teaches that this sample-and-hold process is synchronized with the oscillator, producing an output "that remains constant for the period of the sampling interval." (5:13-17). Once the input signal has been sampled, switch 33 closes to provide the sampled signal to adder 16 (Fig. 3). The adder 16 sums the voltage on capacitor 30 and the feedback voltage signal f1; capacitor 30 resets to zero and the cycle starts again. Therefore, rather than accumulating energy over aperture periods,

capacitor 30 captures discrete voltage values that represent the actual voltage of the input signal at each sample.

Integrating (accumulating) energy over multiple aperture periods would distort the voltage representation of the input signal at each sampling instance, preventing an accurate reading of voltage and thus, preventing the baseband signal from being accurately recreated.

Further, the integrators 17 and 19 do not integrate energy output from the switched capacitor 30 as the adder 16 is adding voltages and they propagate to integrators 17 and 19. Integrators 17 and 19 are components of modulator 13 which converts signals from analog signals to digital signals (3:62-64). It is understood that in the context of the modulator 13, integrators 17 and 19 are designed to integrate voltages, not energy.

Accordingly, Hulkko does not teach "integrating the energy over the aperture periods".

2) Hulkko does not disclose "generating the second signal from the integrated energy".

As discussed above, in Hulkko's voltage sampling system, the voltage across the capacitor is a snapshot of the sampled input signal at a discrete moment in time. The capacitor resets after each sample.

Hulkko explicitly teaches that this sample-and-hold process is synchronized with the oscillator, producing an output “that remains constant for the period of the sampling interval.” (5:13-17). A POSITA would therefore understand that Hulkko uses a high impedance load during the sampling interval, and after sampling, the voltage is used by adder 16, which is added with the voltage of feedback signal f1. The output of adder 16 is a voltage, not energy.

Because Hulkko uses readings of voltage to recreate a second signal, the second signal is not being generated from energy (integrated). This is different than an energy transfer (energy sampling) system, which uses the energy from the input signal provided to a low impedance load to generate a second signal (i.e., the sampled energy makes up/becomes part of the second signal).

Accordingly, Hulkko does not teach “generating a second signal from the integrated energy” as claimed. Instead, Hulkko recreates the second signal based on voltage.

III) Regarding claims 46-48 not obvious in view of Hulkko reference:

Claims 46-48 each depend from claim 29. Hulkko does not render claims 46-48 obvious for the same reasons set forth above regarding claim 29.

IV) Regarding claims 2-3, 10, 13-14, 27 not obvious in view of Hulkko and Lee references:

Claims 2-3, 10, 13-14, 27 each depend from claim 1. Hulkko and Lee do not teach limitations of claim 1 which similar to claim 29 (i.e., "integrating the energy over the aperture periods" and "generating the baseband signal from the integrated energy".)

V) Regarding claims 8, 13, 15 and 19 not obvious in view of Hulkko, Lee and Schiltz references:

Claims 8, 13, 15 and 19 each depend from claim 1. Hulkko, Lee and Schiltz do not teach limitations of claim 1 which similar to claim 29 (i.e., "integrating the energy over the aperture periods" and "generating the baseband signal from the integrated energy".)

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

CORRESPONDENCE

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Any inquiry concerning this communication or earlier communications from the Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

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