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Transcript of Lawrence E. Larson, Ph.D.

Date: February 26, 2025

Case: MediaTek, Inc. -v- ParkerVision, Inc. (PTAB)

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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

- - - - - x
MEDIATEK, INC., :
Petitioner, : IPR2024-00796
v. : U.S. Patent No.
PARKERVISION, INC., : 7,483,686
Patent Owner. :

- - - - - X

Videotaped Deposition of LAWRENCE E. LARSON, Ph.D.

Conducted Virtually

Wednesday, February 26, 2025

9:03 a.m. EST

Job No.: 572653

Pages 1 - 142

Reported by: Debra A. Whitehead

1 Videotaped Deposition of LAWRENCE E. LARSON,
2 Ph.D., conducted virtually.

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4
5 Pursuant to notice, before Debra Ann Whitehead,
6 E-Notary Public in and for the Commonwealth of
7 Virginia.

A P P E A R A N C E S

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ALSO PRESENT:

MERINDA EVANS, Video Specialist

HAROLD RODRIGUEZ, A/V Technician

C O N T E N T S

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EXHIBITS MARKED IN TODAY'S SESSION

(Attached to the Transcript)

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EXHIBITS MARKED IN PRIOR SESSIONS

(Not attached)

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P R O C E E D I N G S

VIDEO SPECIALIST: Here begins Media
Number 1 in the videotaped deposition of
Dr. Lawrence E. Larson in the matter of MediaTek,
Inc., versus ParkerVision, Inc.; in the United
States Patent and Trademark Office, before the
Patent Trial and Appeals Board; Case Number
IPR2024-00796.

Today's date is February 26, 2025, and
the time on the video monitor is 9:03 a.m. eastern
standard time. The remote videographer is Merinda
Evans, representing Planet Depos. All parties of
this video deposition are attending remotely.

Would counsel please voice-identify
themselves and state whom they represent.

MS. MANDIR: This is Stephanie Mandir
from Daignault Iyer, on behalf of ParkerVision,
patent owner.

MR. DAY: Evan Day, from Petitioner
MediaTek, from Perkins Coie.

VIDEO SPECIALIST: The court reporter
today is Debbie Whitehead, representing Planet

1	Depos.	09:03:42
2	The witness will now be sworn in.	09:03:50
3	LAWRENCE E. LARSON, Ph.D.,	09:03:50
4	having been duly sworn, testified as follows:	09:03:59
5	EXAMINATION BY COUNSEL FOR PATENT OWNER	09:03:59
6	BY MS. MANDIR:	09:03:59
7	Q Good morning, Dr. Larson.	09:04:01
8	A Good morning.	09:04:05
9	Q Can you state your full name, for the	09:04:05
10	record.	09:04:07
11	A Lawrence Ernest Larson.	09:04:09
12	Q And where are you currently located for	09:04:11
13	today's deposition?	09:04:15
14	A I'm in Providence, Rhode Island.	09:04:16
15	Q Is there anyone else in the room with you	09:04:18
16	today?	09:04:21
17	A No one else is in the room with me. I'm	09:04:24
18	at home today and my wife is at home as well, but	09:04:28
19	she's not in the room with me.	09:04:32
20	Q That's fine. And do you agree not to	09:04:34
21	communicate with anyone else while questions are	09:04:37
22	being asked during today's deposition?	09:04:41

1	A	Yes, I agree not to communicate with	09:04:43
2		anyone else.	09:04:44
3	Q	And do you have any notes in front of	09:04:45
4		you?	09:04:48
5	A	I have no notes in front of me at all.	09:04:50
6	Q	So no documents or no tabs or anything	09:04:52
7		open on your computer?	09:04:56
8	A	Oh. Well, so in terms of documents, I	09:04:58
9		have a copy of my declaration and a copy of the	09:05:02
10		'686 patent right next to me here. That's all I	09:05:07
11		have next to me.	09:05:13
12		And then tabs, let me just, I'll shut	09:05:14
13		down all my browser tabs.	09:05:16
14	Q	Yeah. And as long as the copies of the	09:05:17
15		declaration and '686 patent are clean with no	09:05:20
16		markings on them, then I'll say you can keep them	09:05:23
17		in front of you. But if they do have any sort of	09:05:28
18		notes or highlights or anything I'll ask you to	09:05:31
19		put them away and I'll give you those documents	09:05:33
20		during the deposition.	09:05:35
21	A	Okay. These two documents have no	09:05:36
22		markings on them whatsoever.	09:05:37

1	Q	Okay. Then that's fine.	09:05:39
2		And you've been deposed before.	09:05:46
3		Correct?	09:05:47
4	A	Yes, I've been deposed before.	09:05:48
5	Q	So you're familiar with how this process	09:05:49
6		works, but we can just run through a few things.	09:05:53
7		So I'll be showing you some documents today. And	09:05:57
8		because this is virtual, I'll share the documents	09:05:59
9		with you in the chat. If you have any	09:06:02
10		difficulties downloading or opening the documents	09:06:05
11		just speak up, and I'll make sure you get what you	09:06:07
12		need.	09:06:10
13		And it's possible during today's	09:06:13
14		deposition that your attorney will -- you might	09:06:14
15		hear an objection to my questioning. If that	09:06:18
16		happens, please let the attorneys state their	09:06:19
17		objection, and then you can go ahead and answer my	09:06:23
18		question regardless of the objection unless your	09:06:25
19		attorney instructs you not to answer.	09:06:28
20		Does that make sense?	09:06:30
21	A	Yes, that makes sense. Thank you.	09:06:33
22	Q	And if you feel like you need a break at	09:06:34

1 any point in time, please just let me know. This 09:06:38
2 is not an endurance contest. So feel free to take 09:06:42
3 breaks. The one caveat is I ask that if a 09:06:46
4 question is pending, that you give an answer to 09:06:50
5 that pending question before we go on a break. 09:06:53

6 Is that good? 09:06:55

7 A That's good, yes. Thank you. 09:06:56

8 Q And is there any reason that you can't 09:07:00
9 give truthful and accurate testimony today? 09:07:03

10 A No reason whatsoever. I can give 09:07:07
11 truthful and accurate testimony. 09:07:10

12 Q Let's start looking at some documents 09:07:11
13 then. I believe already provided in the chat is 09:07:14
14 going to be Exhibit 1 to your deposition. 09:07:21

15 (Larson Deposition Exhibit 1 marked for 09:07:24
16 identification and is attached to the transcript.) 09:07:24

17 Q Exhibit 1 is entitled Patent Owner's 09:07:24
18 Notice of Deposition of Dr. Lawrence E. Larson. 09:07:27
19 Please let me know if you can open that and when 09:07:32
20 that's in front of you. 09:07:36

21 A Okay. I can -- I've opened it and it's 09:07:45
22 in front of me. I use a web browser to look at 09:07:47

1	PDF, files so it's on my web browser.	09:07:51
2	Q That's fine.	09:07:55
3	Have you seen this document before?	09:07:56
4	A I believe I have, yes.	09:07:59
5	Q So this is the patent owner's notice of	09:08:00
6	deposition that we submitted in this case. And	09:08:05
7	you understand that you're here to testify on	09:08:08
8	behalf of MediaTek tech as an expert in the	09:08:11
9	IPR2024-00796. Correct?	09:08:16
10	A IPR2024-00796, correct.	09:08:22
11	Q And you understand that IPR2024-00796	09:08:25
12	relates to U.S. Patent Number 7,483,686. Right?	09:08:33
13	A Yes, Patent 7,483,686. Correct.	09:08:42
14	Q And today we're going to be discussing	09:08:50
15	some of the specifics of the '686 patent. So if I	09:08:54
16	refer to the patent as the '686 patent today,	09:08:56
17	you'll understand what I'm referring to. Correct?	09:08:59
18	A Yes, that makes perfect sense, thank you.	09:09:06
19	Q So, Dr. Larson, you submitted a	09:09:09
20	declaration in this case. Correct?	09:09:11
21	A You know, if you're referring to this --	09:09:16
22	yes, I submitted a declaration in this case,	09:09:18

1	correct.	09:09:21
2	Q And you attached your CV to your	09:09:21
3	declaration. Correct?	09:09:24
4	A Yes, my CV kind of appears as maybe an	09:09:29
5	appendix to the declaration at the end.	09:09:32
6	Q Is that a reasonably up-to-date summary	09:09:35
7	of your experience?	09:09:38
8	A I'm just checking it very quickly.	09:10:00
9	Yes, it's reasonably up to date.	09:10:07
10	Q And so you're currently a professor of	09:10:09
11	engineering at Brown University. Correct?	09:10:10
12	A That's right, I'm an professor at Brown.	09:10:17
13	Q And what kind of courses do you teach at	09:10:19
14	Brown?	09:10:21
15	A Well, I teach courses in electronic	09:10:25
16	circuit design at the undergraduate level. And I	09:10:28
17	also actually teach a course in finance and	09:10:37
18	strategy for a master's program that we have in	09:10:42
19	business education, a technical engineering	09:10:47
20	management. So just to summarize, I guess	09:10:50
21	electronic circuits, electrical circuits, and then	09:10:54
22	corporate finance.	09:10:56

1	Q	And do you currently have any other jobs?	09:10:58
2	A	No, I have no other jobs at this point.	09:11:08
3	Q	You've stated in your declaration that	09:11:10
4		you have over 40 years of experience in the design	09:11:15
5		of high-performance RF circuits.	09:11:20
6		Is that accurate?	09:11:23
7	A	Yes, that's accurate.	09:11:28
8	Q	So given your experience, would you	09:11:31
9		consider yourself an expert in RF circuit design?	09:11:34
10	A	Yeah, given my experience and the length	09:11:43
11		of time and the variety of systems I've worked on	09:11:45
12		and the courses I've taught and the students I've	09:11:47
13		advised, I would consider myself an expert in RF	09:11:50
14		circuit design.	09:11:52
15	MS. MANDIR:	The next document I'm going	09:11:56
16		to introduce is your declaration. I understand	09:11:57
17		you have a copy of it in front of you already.	09:11:59
18		But just so it's on the record, the document	09:12:04
19		provided is entitled Declaration of Dr. Lawrence	09:12:08
20		E. Larson, which is marked in the right-hand	09:12:13
21		corner as MediaTek 1002.	09:12:16
22		(MediaTek Exhibit 1002, previously	09:12:20

1	marked, not attached.)	09:12:23
2	Q And since this has been previously marked	09:12:23
3	in the IPR as Exhibit 1002, I'm just going to be	09:12:26
4	referring to it today as either Exhibit 1002 or	09:12:30
5	your declaration.	09:12:35
6	Is that okay?	09:12:36
7	A Yes, that's -- that makes perfect sense.	09:12:38
8	Q So let me upload this into the chat so	09:12:41
9	that we're all looking at the same thing, make	09:12:51
10	sure that you're ...	09:12:53
11	And let me know when you receive that	09:13:10
12	document.	09:13:12
13	A Okay. It hasn't appeared in the chat	09:13:13
14	yet.	09:13:15
15	Ah, there we go. So it just popped up in	09:13:16
16	the chat. I will download it.	09:13:23
17	Okay. I just opened it up. And this	09:13:52
18	looks like the declaration.	09:13:54
19	Q So the copy of Exhibit 1002 is, in fact,	09:13:57
20	the declaration that you submitted and prepared	09:14:02
21	for the purposes of this proceeding. Correct?	09:14:04
22	A That appears to be the case, yes.	09:14:09

1 Q Were you familiar with ParkerVision prior 09:14:12
2 to working on this case? 09:14:15

3 A Yes, I was familiar with ParkerVision 09:14:20
4 prior to working on this case. 09:14:23

5 Q How did you first hear about 09:14:24
6 ParkerVision? 09:14:27

7 A Well, you know, ParkerVision is a 09:14:31
8 wireless communications company that has been 09:14:38
9 around for a number of years. And while I was a 09:14:40
10 professor at UC San Diego I, you know, heard about 09:14:45
11 them through various press releases. And, you 09:14:51
12 know, I may have visited their website at one 09:14:56
13 point. 09:14:59

14 You know, they had a lot of public claims 09:15:00
15 about various aspects of their wireless 09:15:02
16 technology. And as someone who does research in 09:15:05
17 this I was very interested in what they were 09:15:07
18 doing. And so I guess that's how I first became 09:15:13
19 aware of them. 09:15:16

20 Then, you know, about eight or nine years 09:15:17
21 ago I was contacted by Qualcomm regarding some of 09:15:21
22 the ParkerVision patents, and I believe I produced 09:15:27

1 some IPR reports as part of that, you know, case,

09:15:30

2 I guess I would call it.

09:15:38

3 And, you know, since then ParkerVision,

09:15:40

4 you know, continues to be in the news from time to

09:15:43

5 time, and so every now and then I would hear

09:15:45

6 something in the news about them. So that's kind

09:15:47

7 of my history of my knowledge of ParkerVision.

09:15:50

8 Q When would you say you first -- or you

09:15:55

9 said at the University of San Diego is when you

09:15:59

10 first heard about ParkerVision. And do you know

09:16:01

11 about what dates or year that was?

09:16:04

12 A I'm sorry, I couldn't be, you know,

09:16:08

13 precise. You know, I was -- I was at UC San Diego

09:16:10

14 from 1996 until 2011, and so it would have been,

09:16:14

15 you know, in the late 2000s? I mean, you know,

09:16:19

16 the late 2006, '07, '08, '09, '10, somewhere in

09:16:24

17 there. So I request not be anymore precise than

09:16:31

18 that, really.

09:16:35

19 Q And were you familiar with the '686

09:16:36

20 patent prior to your engagement in this case?

09:16:41

21 A Well, I can't say for certain. I mean,

09:16:46

22 as part of the Qualcomm earlier work, you know, I

09:16:50

1	may have taken a quick look at it. But I really	09:16:55
2	can't say for certain one way or the other. It	09:16:59
3	doesn't -- it didn't really jump to my mind when I	09:17:01
4	first started to work on this particular case.	09:17:04
5	Q And let's begin, let's turn to your	09:17:06
6	declaration on Page -- let's see. This is going	09:17:15
7	to be PDF Page 14. I think I'll use PDF pages,	09:17:20
8	unless you prefer otherwise.	09:17:28
9	A Okay. Thank you for doing that. I'll	09:17:30
10	try to use the PDF. It's a little weird in my	09:17:34
11	browser, but I think I can do it.	09:17:39
12	Q So if you turn to -- yeah, let me know	09:17:44
13	when you're --	09:17:48
14	A So my PDF Page 14, according to my	09:17:49
15	browser, is the introduction. So 1, Roman numeral	09:17:51
16	1 is at the top of the page.	09:17:58
17	Q Perfect. And if you could turn to	09:17:59
18	Paragraph 2. It says that your rate is \$600 an	09:18:02
19	hour. And I just want to clarify that that is	09:18:11
20	currently the rate that -- as you sit here today?	09:18:13
21	A Yes, that's the rate as I sit here today.	09:18:17
22	Q And does that rate cover both the time	09:18:20

1 for you to prepare the declaration as well as your 09:18:25

2 time providing testimony for the deposition today? 09:18:30

3 A Yes, that's -- that rate is consistent 09:18:33

4 for everything that I've done on this case. 09:18:36

5 Q And how long would you say that you 09:18:39

6 worked on your declaration? 09:18:45

7 A I would say I worked between 40 and 80 09:18:52

8 hours on the declaration. 09:18:56

9 Q Is that including reviewing all the prior 09:19:00

10 art references or just writing the actual 09:19:03

11 declaration? 09:19:05

12 A I'd say that that's including reviewing 09:19:14

13 all the prior art, as well as the writing. 09:19:17

14 Q And how did you prepare for today's 09:19:22

15 deposition? 09:19:26

16 A Well, you know, I reviewed my 09:19:30

17 declaration. I reviewed the patent, the '686 09:19:35

18 patent. I reviewed, you know, the references that 09:19:39

19 I refer to in my declaration. You know, that's 09:19:42

20 about it, really. 09:19:49

21 There are -- I guess there's some claim 09:19:52

22 construction documents that I reviewed as well to 09:19:56

1	familiarize myself with the claim construction.	09:19:58
2	And I think that's it.	09:20:01
3	Q Did you speak with any attorneys to	09:20:02
4	prepare for your deposition today?	09:20:08
5	A Yes; I spoke with Mr. Day, who's -- who's	09:20:11
6	here on the call today.	09:20:17
7	Q And how many times did you speak with	09:20:18
8	Mr. Day to prepare for the deposition?	09:20:20
9	A I guess I spoke two or three times with	09:20:29
10	Mr. Day in preparation for this deposition.	09:20:32
11	Q And how long were each of those times	09:20:34
12	that you met with Mr. Day, or spoke with Mr. Day?	09:20:41
13	A Yeah, you know -- you know, one meeting	09:20:46
14	was about four or five hours, another meeting was	09:20:51
15	two hours, maybe another meeting was an hour.	09:21:00
16	Q And other than Mr. Day, did you speak	09:21:05
17	with any other attorneys to prepare for the	09:21:08
18	deposition?	09:21:10
19	A No, I didn't speak with any other	09:21:14
20	attorneys.	09:21:16
21	MS. MANDIR: So I'm also going to put	09:21:24
22	into the chat U.S. Patent Number 7,483,686, which	09:21:27

1	has been previously marked in the right-hand	09:21:35
2	corner as MediaTek Exhibit 1001.	09:21:39
3	(MediaTek Exhibit 1001, previously	09:21:42
4	marked, not attached.)	09:21:45
5	Q And let me know when you have that in	09:21:45
6	front of you.	09:21:49
7	A Okay, it just appeared in the chat. I'll	09:22:15
8	download it. Let me bring it up.	09:22:23
9	Okay, I have it here in front of me.	09:22:42
10	Q Since this was -- or has been previously	09:22:44
11	marked in the IPR as Exhibit 1001, I'm going to	09:22:47
12	refer to this exhibit as either Exhibit 1001 or	09:22:51
13	simply the '686 patent. Okay?	09:22:55
14	A That makes perfect sense.	09:23:01
15	Q And you agree that the Exhibit 1001 is	09:23:02
16	the patent that's at issue for today's deposition.	09:23:07
17	Correct?	09:23:10
18	A Yes, it appears to be. Yes, the patent	09:23:11
19	that's at issue today.	09:23:14
20	Q So I'd like to talk about your	09:23:15
21	interpretation of some of the claim terms of the	09:23:17
22	'686 patent.	09:23:20

1	If you could turn to the claim section of	09:23:22
2	the patent which is all the way at the back. Let	09:23:25
3	me know when you're there. It should start on PDF	09:23:28
4	Page 133, if that's helpful.	09:23:44
5	A Okay. Yeah.	09:23:47
6	Yes, I am there.	09:23:51
7	Q So do you see Claim 1, which is on PDF	09:23:54
8	Page 133, and then also Claim 11, which is on the	09:23:58
9	next page, 134? If you look at Claims 1 and 11,	09:24:02
10	both recite, "A switch configured to operate	09:24:08
11	according to an energy transfer signal, and to	09:24:11
12	sub-sample and transfer energy from a first	09:24:15
13	electromagnetic (EM) signal."	09:24:17
14	Do you see that recitation in both Claims	09:24:20
15	11 and 1?	09:24:24
16	A I am just reviewing. I'm sorry, I'm	09:24:31
17	having trouble getting the thing to scroll.	09:24:46
18	So yes, I see that. That's in both	09:24:48
19	Claims 1 and 11.	09:24:53
20	Q So I would like to start with the term	09:24:54
21	"switch."	09:24:57
22	In Paragraph 78 of your declaration --	09:24:59

1	sorry, I keep making you switch back and forth.	09:25:05
2	That was probably be the whole day, so ...	09:25:08
3	A No. That's okay.	09:25:12
4	I have the clarification with Paragraph	09:25:20
5	78 in front of me now.	09:25:23
6	Q Great. So Paragraph 78 of your	09:25:24
7	declaration states that, "In my opinion, 'switch'	09:25:25
8	should be construed as an electronic device for	09:25:28
9	opening and closing a circuit."	09:25:31
10	Correct?	09:25:33
11	A Yes, that's what I wrote. Correct.	09:25:34
12	Q And did you apply this construction of	09:25:35
13	switch when you were analyzing the prior art	09:25:40
14	references?	09:25:42
15	A Yes, I analyzed -- sorry, I utilized this	09:25:44
16	construction for the prior art references.	09:25:49
17	Q How did you determine whether a component	09:25:50
18	in a prior art reference was a switch?	09:25:53
19	A Well, you know, once again, this is based	09:26:01
20	on my knowledge of electrical engineering and	09:26:03
21	microelectronic circuit design.	09:26:08
22	So, you know, a device -- the devices	09:26:11

1 that are used as switches will typically, you 09:26:13
2 know, be closed under some kind of a control and 09:26:21
3 be open under some kind of a control. 09:26:26

4 And the devices that I -- I understand 09:26:28
5 how these devices work very intimately. And so, 09:26:30
6 you know, the devices that I analyzed meet that 09:26:36
7 requirement of a switch, that they can be open or 09:26:38
8 closed under control. 09:26:41

9 Q What do you mean by "open"? 09:26:45

10 A So by open what I mean is that the switch 09:26:50
11 will not pass current, will not pass charge, or 09:26:59
12 pass very, very, very little charge. 09:27:07

13 So an open switch is a switch that 09:27:10
14 basically does not allow any current to flow 09:27:11
15 between its two terminals. 09:27:15

16 Q And what do you mean by "a closed 09:27:22
17 switch"? 09:27:25

18 A So a closed switch is when a switch is 09:27:26
19 closed, current can flow very, very easily between 09:27:31
20 the two terminals. And an ideal closed switch 09:27:36
21 would exhibit no resistance whatsoever between the 09:27:42
22 two terminals. 09:27:45

1 Q And can the current of a switch that is 09:27:46
2 closed flow between both terminals back and forth 09:27:51
3 of the switch? 09:27:56

4 A Well, the back and forth is not a 09:28:06
5 requirement. Some switches will allow current to 09:28:11
6 flow back and forth. And by "back and forth" I 09:28:15
7 mean in one direction and then in the other 09:28:19
8 direction. And some switches will only allow 09:28:21
9 current to flow in one direction when they're on. 09:28:24
10 So that limitation is not necessary for the 09:28:32
11 operation of a switch. 09:28:34

12 Q And so that is how you apply the term 09:28:36
13 "switch" to the prior art references cited in your 09:28:40
14 declaration. Correct? 09:28:43

15 A I think that that's a complete -- you 09:28:47
16 know, that represents my complete understanding of 09:28:52
17 the operation of a switch as I applied it to 09:28:55
18 these -- to this patent. 09:28:59

19 Q Okay. Let's look at the next term from 09:29:00
20 that recitation in both Claims 1 and 11. It's the 09:29:06
21 term "sub-sample." Paragraph 83 of your 09:29:12
22 declaration states, "I understand that in a 09:29:26

1 previous litigation involving related patents, a 09:29:30
2 district court adopt ParkerVision's proposal to 09:29:33
3 construe the term 'sub-sample' to refer to 09:29:36
4 sampling at an aliasing rate, i.e., at a rate that 09:29:38
5 is less than or equal to twice the frequency of 09:29:42
6 the signal being sampled. In my opinion, the 09:29:45
7 plain and ordinary meaning as would have been 09:29:48
8 understood by a POSITA encompasses this 09:29:51
9 construction, and so I have applied it in my 09:29:53
10 analysis below." 09:29:56

11 Do you see that? 09:29:57

12 A Yes, I see that in Paragraph 83. 09:29:59

13 Q So Paragraph 83 indicates -- or you 09:30:01
14 indicate that the plain and ordinary meaning of 09:30:08
15 the term "sub-sample" would encompass the 09:30:10
16 construction previously adopted by the court. 09:30:12

17 Do you mean that you applied the district 09:30:16
18 court's construction or you applied something 09:30:18
19 additional to the district court's construction? 09:30:23

20 MR. DAY: Object to form. 09:30:27

21 A Well, let me just kind of read the report 09:30:35
22 here. It says, you know, that the district court 09:30:38

1 adopted this construal of the term "sub-sample"
2 to, quote, refer to sampling at an aliasing rate,
3 i.e. at a rate less -- that is less than or equal
4 to twice the frequency of the signal being
5 sampled.

6 And I think that I've applied that
7 particular construction in my analysis. So
8 that -- that quote is the term that I used to do
9 my analysis.

10 Q In Paragraph 83 you say, The plain and
11 ordinary meaning as would have been understood by
12 a POSITA encompasses that construction.

13 So what do you mean by "the plain and
14 ordinary meaning" of the term?

15 A Well, I think all I mean, what I mean by
16 that sentence is that the plain and ordinary
17 term -- sorry, the plain and ordinary meaning of
18 sub-sampling is consistent with the district
19 court's proposal of construing that term. They're
20 very, very consistent with each other.

21 Q So you're suggesting that the plain and
22 ordinary meaning of sub-sample is sampling at an

1 aliasing rate, i.e., at a rate that is less than 09:31:56
2 or equal to twice the frequency of the signal 09:32:00
3 being sampled. 09:32:03

4 Is that right? 09:32:03

5 A Yes. And, once again, I'm just quoting 09:32:05
6 here from the -- from the district court's 09:32:07
7 language, At a rate that is less than or equal to 09:32:09
8 twice the frequency of the signal being sampled. 09:32:13

9 Q How would you -- or how -- strike that. 09:32:17
10 How do you define sampling? 09:32:22

11 A Well, you know, in my -- in my 09:32:28
12 declaration I talk a little bit about that. And 09:32:34
13 that goes -- you know, Paragraph 58 in my 09:32:39
14 declaration. And, you know, basically sampling 09:32:49
15 is -- I used the word "capturing." I think that's 09:32:56
16 very good. -- capturing the instantaneous value 09:32:59
17 of a signal, and then holding it for some period 09:33:02
18 of time. 09:33:06

19 And so you're basically taking little 09:33:12
20 instantaneous snapshots of the signal on a 09:33:14
21 periodic basis. And that's discussed in my 09:33:19
22 report, and that's my understanding, and that's 09:33:22

1 the meaning of sampling. 09:33:25

2 Q So when you were analyzing the term 09:33:26

3 "sub-sample" in the claims relevant to the prior 09:33:34

4 art, you were using your definition of sampling 09:33:37

5 plus that that sampling had to be an aliasing 09:33:41

6 rate. 09:33:45

7 Is that correct? 09:33:45

8 MR. DAY: Object to form. 09:33:46

9 A Well, I don't -- sampling, I don't -- 09:33:49

10 sampling doesn't have to be at an aliasing rate. 09:33:57

11 Sampling can be at any rate at all. So there's 09:34:00

12 no, you know, limitation on sampling to be at an 09:34:04

13 aliasing rate. 09:34:06

14 Q But the term "sub-sampling" as you've 09:34:07

15 stated in Paragraph 83 is sampling at an aliasing 09:34:12

16 rate. Correct? 09:34:16

17 MR. DAY: Object to form. 09:34:22

18 A Sub-sampling occurs at a frequency 09:34:23

19 that's, you know, as -- as I -- you know, 09:34:31

20 sub-sampling occurs per the court's construction 09:34:34

21 at a rate that's less than or equal to, you know, 09:34:37

22 the twice the frequency being sampled. That is 09:34:39

1 sometimes referred to as aliasing. 09:34:44

2 Q So is it correct to say that your 09:34:46

3 definition of sub-sampling just takes the 09:34:54

4 definition of -- that you just elaborated for 09:34:58

5 sampling, and that sampling has to be done at an 09:35:03

6 aliasing rate? 09:35:08

7 MR. DAY: Object to form. 09:35:09

8 A Yeah, well, I'm -- you know, your use of 09:35:10

9 the term "aliasing rate" is -- I'm not quite sure 09:35:14

10 what's meant by it. 09:35:21

11 When you -- when you sub-sample -- and 09:35:23

12 we've already talked about the definition of 09:35:26

13 sub-sampling -- one of the effects of sub-sampling 09:35:28

14 is something that's called aliasing. 09:35:31

15 And so sub-sampling can in some cases 09:35:37

16 result in aliasing. I'm not sure I understand the 09:35:40

17 term "aliasing rate." I guess that's a new term 09:35:45

18 to me. 09:35:47

19 Q So how did you apply your definition of 09:35:48

20 sub-sampling when analyzing the prior art in view 09:35:58

21 of the claims? 09:36:03

22 A Well, my definition of sub-sampling -- 09:36:07

1 and, you know, let's maybe go back to that very 09:36:13
2 quickly. My sub-sampling definition -- I'm sorry, 09:36:19
3 I see the term "aliasing rate" in Paragraph 83, so 09:36:24
4 I apologize for missing that earlier. 09:36:27

5 But, you know, my definition of 09:36:29
6 sub-sampling is, you know, at a rate that's less 09:36:31
7 than or equal to twice the frequency of the signal 09:36:36
8 being sampled. 09:36:41

9 So when I looked at the prior art, I 09:36:42
10 looked to see what frequency the sampling was 09:36:44
11 occurring at and what frequency the signal was 09:36:48
12 that we were sampling. And then I applied that 09:36:53
13 test. You know, is the sampling rate less than or 09:36:57
14 equal to twice the frequency of that signal being 09:37:00
15 sampled. 09:37:02

16 So that's how I used that definition and 09:37:03
17 applied it to the pieces of prior art. 09:37:09

18 Q And how did you determine that something 09:37:14
19 was sampling? 09:37:19

20 A Well, you know, once again let's maybe 09:37:28
21 turn to the -- my declaration. And if you look at 09:37:32
22 Paragraph 89 of my declaration. Paragraph 89 09:37:38

1 shows a -- the reference of Avitabile, or

09:37:44

2 Avitabile, and Figure 2 from that reference.

09:37:52

3 Now, the -- that particular figure shows

09:37:56

4 a switch that's under control of a sampling

09:38:01

5 signal. And then that -- so that operation of

09:38:11

6 that switch from the sampling is characteristic of

09:38:13

7 a sampling circuit. You close the switch

09:38:20

8 periodically to measure the voltage.

09:38:24

9 And then to the right of that switch is a

09:38:29

10 capacitor, C. And the voltage at the input is

09:38:31

11 transferred to the capacitor for that brief

09:38:39

12 interval that the switch is closed. And so that

09:38:42

13 process of closing a switch storing the voltage on

09:38:47

14 a -- on a capacitor is a classic sampling. That's

09:38:53

15 pretty much in electronics how every sampling

09:38:58

16 circuit works.

09:39:00

17 And so that's, you know -- that's how a

09:39:02

18 sample -- that's how I -- that's how I know that

09:39:07

19 sampling was going on, because this -- you know,

09:39:11

20 this particular circuit had that structure.

09:39:12

21 Q And what effect does sampling have on a

09:39:16

22 signal?

09:39:28

1	MR. DAY: Object to form.	09:39:28
2	A Well, yeah, sampling can have -- there	09:39:29
3	are many, many different types of sampling, and so	09:39:38
4	there's no single answer to your question.	09:39:42
5	But generally speaking, the act of	09:39:47
6	sampling creates several new frequencies at the --	09:39:52
7	as a result of the sampling and also changes	09:40:00
8	the -- so these new frequencies are in the	09:40:08
9	frequency domain of the signal. And if you look	09:40:15
10	at the signal in the time domain, it creates more	09:40:17
11	of a staircase kind of an output compared to	09:40:22
12	perhaps the smooth input of the original input	09:40:27
13	frequency.	09:40:29
14	So the act of sampling changes the shape	09:40:30
15	of the signal, and it also changes its frequency	09:40:33
16	characteristics.	09:40:39
17	Q Let's turn to another term in the claims.	09:40:44
18	So Claims 1 and 11 also recite the term "energy	09:41:15
19	transfer signal." Right?	09:41:19
20	A Yes, that's right, they both do.	09:41:29
21	Q And you do not provide a construction of	09:41:38
22	energy transfer signal in your declaration.	09:41:43

1	Correct?	09:41:45
2	A Yeah, I believe that's correct. Let me	09:41:47
3	just do a quick -- quick check.	09:41:50
4	That's right, I do not provide a	09:42:01
5	construction of energy transfer signal, or energy	09:42:03
6	transfer, or transfer energy. Energy transfer	09:42:06
7	signal.	09:42:10
8	Q How did you define energy transfer signal	09:42:11
9	when analyzing the prior art references cited in	09:42:20
10	your declaration?	09:42:24
11	MR. DAY: Object to form.	09:42:26
12	A Well, so I used what I believe to be the	09:42:28
13	plain and ordinary meaning of an energy transfer	09:42:37
14	signal, which is a signal that, you know,	09:42:41
15	transfers energy from one point to another point.	09:42:47
16	And in these patents -- or in this	09:42:53
17	patent, the -- they refer to a source and a	09:42:57
18	storage, you know, module or capacitor,	09:43:03
19	essentially. So for the purposes of these patents	09:43:06
20	I interpreted this to mean, you know, a signal	09:43:11
21	that -- where energy is transferred from a source	09:43:15
22	to a capacitor. So this is, I think, the kind of	09:43:19

1 plain and ordinary meaning of the term, and it

09:43:23

2 would be well understood by a person of ordinary

09:43:25

3 skill in the art.

09:43:27

4 Q So you said a signal where energy is

09:43:30

5 transferred from a source to a capacitor.

09:43:35

6 A Yes. A capacitor or a storage device.

09:43:42

7 But in this particular patent a capacitor is a --

09:43:45

8 is used.

09:43:51

9 Q So a signal that allows the transfer of

09:43:51

10 any amount of energy would be included in your

09:43:57

11 definition of energy transfer signal?

09:43:58

12 MR. DAY: Object to form.

09:44:01

13 A Well, I think any -- perhaps a way to

09:44:05

14 put -- to answer your question would be that an

09:44:10

15 energy transfer signal would transfer any

09:44:13

16 nonnegligible amount of energy, you know, to the

09:44:16

17 capacitor. So the energy would have to be

09:44:19

18 nonnegligible.

09:44:24

19 Q So when you were analyzing the prior art,

09:44:24

20 you were looking for an energy transfer signal or

09:44:31

21 a signal that transferred nonnegligible amounts of

09:44:35

22 energy from a source to a capacitor.

09:44:38

1	Is that correct?	09:44:40
2	MR. DAY: Object to form.	09:44:42
3	A Yeah, I mean, I think a good way to say	09:44:44
4	it would be that the, you know, energy transfer	09:44:46
5	signal transferred a nonnegligible energy from a	09:44:50
6	source to a storage device, a capacitor in this	09:44:53
7	case.	09:44:57
8	Q And how did you determine whether a	09:44:57
9	signal was an energy transfer signal?	09:45:07
10	A Well, you know, as I said, you know, the	09:45:15
11	definition of an energy transfer signal under the	09:45:20
12	plain and ordinary meaning is just you're	09:45:24
13	transferring a nonnegligible amount of energy from	09:45:26
14	a source to a -- to a storage device, a capacitor.	09:45:29
15	And it's nonnegligible if it's distinguishable	09:45:34
16	from noise.	09:45:37
17	And so, you know, these pieces of prior	09:45:39
18	art discuss transferring an RF signal, that's the	09:45:43
19	source, to a -- to a whole -- to a capacitor. And	09:45:48
20	so the RF source is definitely distinguishable	09:45:53
21	from noise, and so that meets the definition of an	09:45:57
22	energy transfer signal.	09:46:02

1 Q Are you -- I'm just trying to understand
2 if there's any difference between how you're
3 defining energy transfer signal and just, like, an
4 LO signal.

5 Is there a difference?

6 MR. DAY: Object to form.

7 A Could you repeat the question? I didn't
8 hear. I'm sorry.

9 Q Yeah, I'm just trying to understand if
10 there's a difference between how you've
11 interpreted energy transfer signal and just an LO
12 signal.

13 A And so you referred to the LO signal, and
14 that's the local oscillator signal. And the local
15 oscillator signal is what controls the energy
16 transfer. So that you might think of the local
17 oscillator as a controller for the switch.

18 So there are two inputs to a -- to a
19 sampler, you know, or to these systems. There's
20 the RF energy which is transferred to the hold
21 capacitor, and there's the local oscillator which
22 controls that transfer.

1 So in many cases -- not all cases, but in 09:47:39
2 many cases -- no LO energy is transferred to 09:47:43
3 the -- to the hold capacitor. The RF energy is 09:47:47
4 transferred to the hold capacitor. 09:47:51

5 Q So you said energy transfer in an amount 09:47:55
6 distinguishable from noise is how you're 09:48:15
7 interpreting nonnegligible amounts of energy. 09:48:18

8 Is that correct? 09:48:22

9 A Yes. My -- to me a nonnegligible 09:48:23
10 transfer of energy would be a transfer of energy 09:48:30
11 that is indistinguishable from noise. 09:48:33

12 Q Would you agree that the presence of 09:48:36
13 voltage on a capacitor does not necessarily mean 09:48:40
14 there's nonnegligible amounts of energy on that 09:48:42
15 capacitor? 09:48:46

16 MR. DAY: Object to form. 09:48:48

17 A I'm sorry, could you repeat the question? 09:48:49

18 Q Sure. Would you agree that the presence 09:48:51
19 of voltage on a capacitor does not necessarily 09:48:54
20 mean that there's nonnegligible amounts of energy 09:48:57
21 on that capacitor? 09:49:01

22 A Yeah, I'm sorry, there is a double 09:49:05

1	negative in that question, I'm having trouble	09:49:07
2	parsing it.	09:49:08
3	So your -- was the question voltage on a	09:49:09
4	capacitor does not mean that there is	09:49:12
5	nonnegligible energy? Was that your question?	09:49:17
6	Q Yes. The presence of --	09:49:22
7	A I'm sorry.	09:49:25
8	Q -- does not mean necessarily --	09:49:25
9	necessarily mean nonnegligible amounts of energy	09:49:28
10	transferred.	09:49:33
11	Would you agree?	09:49:33
12	A So, yeah, for some reason the parsing of	09:49:43
13	that double negative is -- I'm struggling with.	09:49:50
14	Let me answer it this way: A voltage on	09:49:56
15	the capacitor, a voltage on a capacitor, can be	09:49:59
16	either negligible or nonnegligible. If it is	09:50:06
17	negligible, it is indistinguishable from noise.	09:50:11
18	And if it's nonnegligible, it will be larger than	09:50:14
19	noise.	09:50:18
20	Q So the presence of voltage is not an	09:50:18
21	indicator of whether nonnegligible amounts of	09:50:25
22	energy has been stored on the capacitor. Correct?	09:50:29

1	MR. DAY: Object to form.	09:50:32
2	A Yeah, I mean, all capacitors will have	09:50:33
3	some voltage on them, which may be due to just	09:50:39
4	random noise. And so the presence of a voltage in	09:50:43
5	and of itself is -- may or may not be an	09:50:49
6	indication of negligible or nonnegligible amounts	09:50:56
7	of energy.	09:51:00
8	Q And you would agree that voltage is not	09:51:04
9	the same thing as energy. Correct?	09:51:05
10	MR. DAY: Object to form.	09:51:07
11	A Voltage is not the same thing as energy,	09:51:15
12	that's -- they are related to each other, and	09:51:19
13	there's a very clear relationship between the	09:51:24
14	voltage on a capacitor and the energy, but they're	09:51:28
15	not the same.	09:51:32
16	Q Right. So voltage is the potential	09:51:36
17	difference between two points measured in volts.	09:51:41
18	Correct?	09:51:45
19	A The voltage is the potential difference	09:51:50
20	between two terminals, and it is measured in	09:51:52
21	volts, that is correct.	09:51:58
22	Q And energy is measured in joules and	09:51:58

1	represents the ability to perform work.	09:52:06
2	Is that correct?	09:52:08
3	A Yes, I think that's a very good	09:52:13
4	definition of -- of energy. It's certainly	09:52:15
5	measured in joules.	09:52:21
6	Q So the energy stored on a capacitor	09:52:22
7	depends not just on the voltage, but also on the	09:52:29
8	capacitance of the capacitor.	09:52:32
9	Is that correct?	09:52:34
10	A Yes, the energy stored is the product of	09:52:38
11	the capacitance, the square of the voltage stored	09:52:44
12	on the capacitor. And then there's another factor	09:52:49
13	of a half that is multiplied in there as well.	09:52:52
14	Q So let me see if I can -- E, energy, is	09:52:58
15	equal to half capacitance voltage squared? That's	09:53:01
16	the equation?	09:53:09
17	A Yes, the equation is E equals one half CV	09:53:10
18	squared, just as you said.	09:53:15
19	Q Okay. Let's turn to another term in	09:53:16
20	Claim -- this one is in Claim 11. The term is	09:53:30
21	"storage module." And if you look at Exhibit	09:53:35
22	1001, Claim 11, recites "a storage module coupled	09:53:47

1 to said switch and configured to store said 09:53:50

2 transferred energy." 09:53:53

3 Let me know when you see that. 09:53:56

4 A Okay. Oh, I see that. 09:54:10

5 Q And so if you turn to Paragraph 76 of 09:54:21

6 your declaration, it's PDF Page 48. You said, "In 09:54:31

7 my opinion, storage module should be construed as 09:54:45

8 a module that stores nonnegligible amounts of 09:54:47

9 energy from an input electromagnetic signal." 09:54:49

10 Do you see that? 09:54:53

11 A I do. 09:54:55

12 Q Is that the construction of storage 09:54:55

13 module you used when analyzing the prior art cited 09:55:00

14 in your declaration? 09:55:03

15 A That's the construction that I used, yes. 09:55:05

16 Q And we just talked about how you define 09:55:06

17 negligible amounts of energy. For the definition 09:55:12

18 of storage module, did you also define 09:55:15

19 nonnegligible amounts of energy as energy in 09:55:20

20 amounts distinguishable from noise? 09:55:22

21 A Yes, to me I'm -- consistently use the 09:55:30

22 construction that nonnegligible amounts of energy 09:55:36

1	are indistinguishable from noise.	09:55:38
2	Q So this deals with storing the	09:55:41
3	nonnegligible amounts of energy, and the	09:55:51
4	construction of energy transfer signal dealt with	09:55:54
5	the transfer of nonnegligible amounts of energy.	09:56:01
6	Is that correct?	09:56:04
7	A Are you referring back to the claim	09:56:05
8	language here in this question?	09:56:06
9	Q Yeah. Sorry. Let me --	09:56:10
10	A Yeah.	09:56:11
11	Q -- clarify.	09:56:12
12	So we were just talking about the term	09:56:13
13	"energy transfer signal." And correct me if I'm	09:56:17
14	wrong, but you said that's a signal that transfers	09:56:22
15	nonnegligible amounts of energy from a source to a	09:56:25
16	capacitor.	09:56:28
17	Is that correct?	09:56:28
18	A Yes, I believe that's correct. An	09:56:30
19	energy transfer will transfer nonnegligible energy	09:56:32
20	from a source to a capacitor.	09:56:35
21	Q And now we are looking at the definition	09:56:37
22	of storage module, which, as you say in Paragraph	09:56:39

1	76 of your declaration, should be construed as a	09:56:46
2	module that stores nonnegligible amounts of energy	09:56:49
3	from an input electromagnetic signal. Correct?	09:56:52
4	A Yes, that's what it says.	09:56:59
5	Q So an energy transfer signal involves the	09:57:01
6	transfer of nonnegligible amounts of energy and an	09:57:05
7	energy -- or a storage module, sorry, deals with	09:57:09
8	the storage of nonnegligible amounts of energy.	09:57:12
9	Is that correct?	09:57:14
10	A Yes. You know, as my report says, you	09:57:15
11	know, a storage module should be construed as a	09:57:17
12	module that stores a nonnegligible -- stores	09:57:19
13	negligible amounts of energy from an input	09:57:24
14	electromagnetic signal.	09:57:28
15	Q And how did you determine that a	09:57:34
16	component of a -- strike that.	09:57:35
17	How did you determine the prior art did	09:57:36
18	or did not include a storage module?	09:57:41
19	A Well, you know, once again maybe you	09:57:49
20	could look at the Avitabile prior art, and Figure	09:57:52
21	2 for example, and I'm looking at Paragraph 92 of	09:58:03
22	my declaration. Figure 2 of Avitabile shows a	09:58:10

1 capacitor at the output. The capacitor is

09:58:17

2 connected between the output and ground.

09:58:24

3 And that's connected to the switch that I
4 was referring to earlier. And so a capacitor is
5 a -- you know, it's a device, a circuit component
6 that stores energy. And so it's connected to the
7 switch.

09:58:27

09:58:29

09:58:36

09:58:40

09:58:44

8 It's clear from the way the circuit is
9 configured that the capacitor stores the energy
10 that comes through that switch.

09:58:45

09:58:48

09:58:52

11 Q And how did you determine that that
12 energy was nonnegligible?

09:58:57

09:58:58

13 A Well, if you look at the paper, you know,
14 for example, the experimental results -- and once
15 again, you know, I'm looking perhaps at Page 47 of
16 my declaration, at the top. And there are some
17 very nice drawings -- sorry, not drawings. There
18 are some very nice experimental data, time domain
19 data, showing the output waveforms. And they're
20 clearly sinusoidal in nature and rather large in
21 amplitude, on the order of 10 of millivolts.

09:59:04

09:59:06

09:59:13

09:59:19

09:59:24

09:59:29

09:59:32

09:59:37

09:59:43

22 And these signal levels shown in this

09:59:50

1 particular piece of prior art are much, much

09:59:52

2 larger than noise. And so that's how I determined

09:59:54

3 that there was a nonnegligible amount of noise

09:59:58

4 being processed by this circuit.

10:00:01

5 Q Did you analyze the circuits using any

10:00:10

6 sort of equations to determine the amounts of

10:00:21

7 energy stored in the capacitors of Avitabile?

10:00:26

8 MR. DAY: Object to form.

10:00:34

9 A I did not perform any calculations or

10:00:40

10 analysis myself. However, the Avitabile reference

10:00:43

11 has lots of equations in it that describe the

10:00:50

12 various constraints on the circuit performance.

10:00:53

13 And I reviewed those equations pretty carefully,

10:00:57

14 and they seemed accurate to me.

10:00:59

15 So I -- I felt that was a very, very good

10:01:02

16 analysis.

10:01:05

17 MS. MANDIR: Let's, now that I guess

10:01:22

18 we're talking about Avitabile, why don't I drop

10:01:23

19 the actual document in the chat, and this will be

10:01:26

20 marked -- or it has been marked already as

10:01:30

21 MediaTek Exhibit 1006.

10:01:35

22 (MediaTek Exhibit 1006, previously

10:01:39

1 marked, not attached.)

10:01:40

2 Q So I'll just refer to the document as
3 Exhibit 1006 or Avitabile during the deposition.

10:01:40

10:01:42

4 Let me know when that's in front of you.

10:01:49

5 A Okay. It just popped up. I will
6 download it.

10:02:01

10:02:03

7 MS. MANDIR: And, maybe actually, we've
8 been going for about an hour. Is this a good time
9 for a break?

10:02:10

10:02:12

10:02:15

10 THE WITNESS: I can break, yeah. Five
11 minutes?

10:02:16

10:02:17

12 MS. MANDIR: Yes. Five minutes. Let's
13 go off the record.

10:02:18

10:02:22

14 VIDEO SPECIALIST: We are going off the
15 record. The time is 10:02.

10:02:22

10:02:23

16 (A recess was taken.)

10:02:25

17 VIDEO SPECIALIST: We are now back on the
18 record. The time is now 10:08 a.m.

10:08:21

10:08:29

19 You may proceed.

10:08:35

20 BY MS. MANDIR:

10:08:37

21 Q And, Dr. Larson, did you discuss the
22 substance of your deposition with anyone over the

10:08:38

10:08:40

1	break?	10:08:43
2	A No, not at all.	10:08:45
3	Q And before the break we -- or I had	10:08:46
4	dropped Exhibit 1006 into the chat, which is the	10:08:51
5	Avitabile reference. Please let me know when you	10:08:55
6	have that in front of you.	10:09:02
7	A I have it in front of me.	10:09:08
8	Q So Avitabile is titled S-band Digital	10:09:11
9	Down-Converter For Radar Applications Based on a	10:09:15
10	GaAs MMIC Fast Sample-and-Hold.	10:09:19
11	Do you see that?	10:09:24
12	A I see that, yes.	10:09:25
13	Q And what does S-band mean here?	10:09:25
14	A S-band refers to a certain range of	10:09:30
15	frequencies. I've forgotten exactly what it is.	10:09:32
16	I think it's kind of around a gigahertz. And, you	10:09:38
17	know, that has origins in the military, which had	10:09:42
18	used letter designations for different frequency	10:09:48
19	ranges for radars. And so S -- S-band refers to a	10:09:50
20	particular range of frequencies.	10:09:56
21	Q And what does the GaAs MMIC in the title	10:09:59
22	mean?	10:10:06

1	A	GaAs is an abbreviation of gallium	10:10:10
2		arsenide, which is a type of semiconductor	10:10:14
3		material. And MMIC is monolithic microwave	10:10:17
4		integrated circuit.	10:10:24
5	Q	And if you look on the first page of	10:10:31
6		Exhibit 1006, it's a few sentences down from the	10:10:34
7		Introduction subheader. It says, "This paper	10:10:44
8		describes a new digital down-converter	10:10:47
9		configuration which performs complex detection by	10:10:49
10		means of the sample-and-hold (SH) in a single step	10:10:51
11		by using a single channel configuration."	10:10:59
12		Do you see that sentence?	10:11:01
13	A	Actually, could you tell me where it is	10:11:06
14		again? I'm sorry.	10:11:07
15	Q	That's okay. The sentence is a few down	10:11:08
16		from the Introduction heading on the first page of	10:11:13
17		the exhibit.	10:11:16
18	A	Is it in the left column or the right	10:11:16
19		column?	10:11:20
20	Q	The left-hand side.	10:11:20
21	A	Thank you.	10:11:21
22	Q	And it starts, "This paper describes a	10:11:22

1	new digital down-converter."	10:11:25
2	A Oh, I'm sorry. I see it, yes.	10:11:33
3	Q Would you say that that sentence is an	10:11:38
4	accurate representation of what's described in	10:11:42
5	Avitabile?	10:11:47
6	A Yes, I think that's an accurate	10:11:54
7	description of what Avitabile talks about.	10:11:55
8	Q So if we turn to the next page, we'll see	10:12:02
9	Figure 1 of Avitabile. And Figure 1 of Avitabile	10:12:11
10	illustrates the digital down-converter	10:12:14
11	configuration.	10:12:18
12	Is that right?	10:12:18
13	MR. DAY: Object to form.	10:12:21
14	A Well, you know, Figure 1 shows a bandpass	10:12:27
15	filter and a sampling hold. And there's a little	10:12:32
16	dashed box around those two together, and that's	10:12:34
17	called the digital down-converter.	10:12:36
18	Q Now, Figure 1 is a diagram of the digital	10:12:42
19	down-converter, which is represented by a dashed	10:12:48
20	box around BPF and SH boxes.	10:12:52
21	Is that correct?	10:12:58
22	A Yeah, that's correct. And the authors	10:13:00

1	called that a digital down-converter, those two	10:13:03
2	boxes.	10:13:05
3	Q And the BPF stand for bandpass filter.	10:13:06
4	Correct?	10:13:10
5	A Yes, BPF stands for bandpass filter.	10:13:11
6	Q And the SH stands for sample-and-hold.	10:13:15
7	Correct?	10:13:19
8	A I believe that's correct, yes, SH stands	10:13:19
9	for sample-and-hold.	10:13:21
10	Q And a sample-and-hold circuit samples the	10:13:22
11	input signal by capturing instantaneous voltage	10:13:28
12	values. Correct?	10:13:34
13	MR. DAY: Object to form.	10:13:35
14	A Well, I mean, I think that's a -- I think	10:13:43
15	I would say that a sample-and-hold works by	10:13:47
16	capturing instantaneous sampling and capturing	10:13:50
17	instantaneous voltage values and then holding them	10:13:57
18	for a period of time.	10:14:00
19	Q Can you explain how the signal is	10:14:01
20	processed by the bandpass filter in the digital	10:14:14
21	down-converter of Figure 1?	10:14:20
22	A Yes. It's not shown here, but a person	10:14:28

1 of ordinary skill in the art would understand that 10:14:32
2 the RF input on the left of Figure 1 is connected 10:14:35
3 to an antenna. There might be perhaps a low noise 10:14:40
4 amplifier between the antenna and the bandpass 10:14:46
5 filter. 10:14:50

6 And the antenna collects energy from an 10:14:50
7 incredibly broad range of frequencies. The 10:14:54
8 antenna is not selective. But this particular 10:14:59
9 circuit is only intended to down-convert S-band 10:15:04
10 frequencies, or specific frequencies. 10:15:10

11 And so there has to be some circuit 10:15:13
12 between the antenna or the low noise amplifier and 10:15:16
13 the down-converter, that preserves the signals 10:15:21
14 that you want, the S-band signals, and rejects all 10:15:26
15 the other signals. 10:15:31

16 And so you need a filter that filters out 10:15:34
17 all the stuff that you don't want in the frequency 10:15:39
18 domain, and only lets the S-band signals through. 10:15:41
19 And that's what a bandpass filter does. It 10:15:44
20 conditions the input signal to the sample-and-hold 10:15:47
21 so that only the desired signals are processed. 10:15:50

22 Q So the bandpass filter filters out 10:15:57

1 frequencies prior to the signal entering the 10:16:01

2 sample-and-hold circuit? 10:16:06

3 A Yes, it filters out signals that are at 10:16:10

4 an undesired frequency prior to the 10:16:14

5 sample-and-hold circuit. 10:16:19

6 Q So if you look at the text under Figure 1 10:16:20

7 of Avitabile, the second sentence after Figure 1 10:16:26

8 says, "The incoming RF waveform, after bandpass 10:16:30

9 filtering and low-noise amplification, is fed to 10:16:36

10 the RF port. A second bandpass filter is 10:16:40

11 requested, after amplification, for outband 10:16:42

12 thermal-noise filtering." 10:16:46

13 Do you see that? 10:16:47

14 A I do, yes. 10:16:48

15 Q So this is suggesting that in Figure 1 10:16:49

16 there is additional bandpass filtering happening 10:16:53

17 before the RF filter enters the bandpass filter 10:17:00

18 illustrated in Figure 1. Correct? 10:17:05

19 A Yeah, it's a little bit -- my reading of 10:17:32

20 this, it's a little bit unclear. But the way I 10:17:34

21 interpret this, these two sentences together. And 10:17:36

22 let me just read and then I will explain what I 10:17:41

1 mean. "The incoming RF waveform, after bandpass
2 filtering and low-noise amplification, is fed to
3 the RF port. A second bandpass filter is
4 requested, after amplification, for outband
5 thermal-noise filtering."

6 Now, I think what they mean there is --
7 and I'll refer to back what I said earlier. You
8 start with an antenna. And then you -- and this
9 is a typical architecture, so it's very, very
10 common architecture. You start with the antenna,
11 and then you have a bandpass filter, which does
12 what I said before, it rejects the unwanted
13 signals. And then the output of that first
14 bandpass filter goes to an amplifier, a low noise
15 amplifier, and that amplifier amplifies the
16 signal. And that's wonderful, but it also
17 amplifies the noise as well. And so very often
18 there's a second bandpass filter after the low
19 noise amplifier. And what that does is reduce the
20 amplified noise that's out of the desired
21 bandwidth.

22 And so for these aliasing systems,

1 reducing that second noise contribution can also 10:19:01
2 be very important. 10:19:04

3 So I think that that's what they're 10:19:06
4 referring to here. It's a two-step filtering 10:19:09
5 process to make sure that the amplified noise from 10:19:12
6 the low noise amplifier is not harming the system 10:19:14
7 performance. 10:19:18

8 Q So the Figure 2 of Avitabile on the same 10:19:18
9 page would be the circuit level design of the SH 10:19:50
10 box of Figure 1. Correct? 10:19:55

11 A Yes, I believe that's correct. I think 10:20:00
12 Figure 2 is the -- like what would be inside that 10:20:02
13 SH box in Figure 1. 10:20:07

14 Q And so Figure 2 is a sample-and-hold 10:20:10
15 circuit that includes a switch, resistor R_T , a 10:20:16
16 capacitor C , another resistor R_L . Correct? 10:20:24

17 A Yes, that is correct. $R(t)$, C , and R_L . 10:20:31
18 Correct. 10:20:38

19 Q And the $R(t)$ in Figure 2 is really not a 10:20:38
20 separate resistor but is, rather, to account for 10:20:42
21 the modeling of an ideal switch, with the 10:20:51
22 resistance coming from the switch. Correct? 10:20:55

1	MR. DAY: Object to form.	10:20:58
2	A Yeah, I think that's a good way to	10:20:59
3	express it. $R(t)$ in Figure 2 models the fact that	10:21:01
4	the resistance of the switch varies with time.	10:21:06
5	And it's not an ideal perfect element. It has	10:21:11
6	some variation with time. And that variation with	10:21:14
7	time is modeled by $R_{sub T} -- R(t)$.	10:21:17
8	Q Now, the $R(t)$, it represents the like	10:21:23
9	switch internal resistance. Correct?	10:21:25
10	A Yeah, I think that's a good way to	10:21:28
11	describe it. There's a certain resistance within	10:21:31
12	the switch that varies with time.	10:21:34
13	Q And the capacitor C in Figure 2 is a hold	10:21:39
14	capacitor. Correct?	10:21:44
15	A Yeah, I think people would typically	10:21:48
16	refer to that as the hold capacitor in this -- in	10:21:49
17	this system.	10:21:52
18	Q And the resistor R_L represents the load	10:21:53
19	of a buffer stage following the sample-and-hold	10:22:05
20	circuit. Correct?	10:22:09
21	A Well, it could be a buffer stage with an	10:22:12
22	internal resistance. It could also be literally a	10:22:16

1	resistor, RL. Either would be perfectly	10:22:23
2	appropriate.	10:22:26
3	Q Let's look at, it is the second sentence	10:22:27
4	under the heading Sample Interval. And it says,	10:22:35
5	"In the circuit of Figure 2, C and RL represent	10:22:40
6	respectively the hold capacitor and the load of	10:22:44
7	the buffer stage following the SH circuit."	10:22:48
8	Do you see that?	10:22:52
9	A I do see that, yes.	10:22:54
10	Q So given that language, would you say	10:22:55
11	that the RL represents the load of a buffer stage	10:22:59
12	following the sample-and-hold circuit?	10:23:05
13	A Yes, it's clear that the authors intent	10:23:07
14	for RL to represent that. And I guess my only	10:23:12
15	point was that it could also just be a resistor.	10:23:15
16	But in this particular paper RL is modeling the	10:23:18
17	load of the buffer stage.	10:23:23
18	Q And so -- strike that.	10:23:25
19	If we go back to Figure 1, there's no	10:23:31
20	individual box for a buffer stage, or representing	10:23:34
21	a buffer stage. Correct?	10:23:38
22	A Figure 1 just has four boxes. None of	10:23:43

1	them are labeled buffer stage.	10:23:45
2	Q Would you agree that Avitabile teaches a	10:23:47
3	buffer stage between the SH box and the ADC box of	10:23:55
4	Figure 1?	10:24:00
5	MR. DAY: Object to form.	10:24:02
6	A Well, I guess I would just say that I	10:24:07
7	interpreted, you know, A-to-D converters often	10:24:10
8	have input buffers. And I interpreted Avitabile,	10:24:15
9	you know, to mean here that, you know, the A-to-D	10:24:20
10	probably had a input buffer built into its input.	10:24:23
11	And so no separate, you know, block diagram	10:24:29
12	showing the buffer stage was necessary. That's	10:24:32
13	pretty well understood by most people who do	10:24:36
14	system-level design.	10:24:39
15	Q Okay. But it would be understood that	10:24:43
16	there was a buffer between the sample-and-hold and	10:24:45
17	ADC circuit of Avitabile. Correct?	10:24:48
18	A Well, Avitabile talks about a buffer	10:24:54
19	stage following the sample-and-hold circuit. So I	10:24:57
20	think that would be well understood.	10:25:01
21	Q And the ADC refers to an	10:25:05
22	analog-to-digital converter. Right?	10:25:09

1	A Yeah, ADC is an abbreviation of	10:25:12
2	analog-to-digital converter.	10:25:16

3	Q	What is a buffer or a buffer stage as	10:25:18
4		described here?	10:25:26

5	A Well, it's something that's well	10:25:31
6	understood by practitioner in this field. And,	10:25:33
7	you know, basically a buffer stage will measure an	10:25:39
8	input voltage, usually it's an input voltage, and	10:25:49
9	produce an output voltage that is a very	10:25:53
10	accurately scaled version of the input.	10:25:56

11	And so you might think of it as an	10:26:00
12	amplifier with a gain of 1. And so it measures an	10:26:03
13	input voltage and it produces an output voltage.	10:26:07
14	So that's -- and then the output voltage in this	10:26:11
15	case of the buffer would be the input for the	10:26:14
16	analog-to-digital converter.	10:26:16

17	Q A buffer stage prevents loading effects	10:26:19
18	from downstream circuitry. Correct?	10:26:27

19	A Well, I'm not sure that I would put it	10:26:36
20	that way.	10:26:37

21	I mean, I think that a buffer stage	10:26:38
22	presents a fixed load to a circuit. And that's a	10:26:42

1 very useful thing. Because like with a 10:26:50
2 sample-and-hold, you know, the load that is 10:26:53
3 attached to that capacitor is somewhat important 10:26:58
4 for the performance of the circuit. 10:27:01

5 So you don't want that load to vary -- 10:27:04
6 sorry, you don't want variations in that load to 10:27:08
7 affect the circuit. So you put a buffer between 10:27:10
8 the output of the sample-and-hold and other stuff, 10:27:14
9 in this case an A-to-D converter. And now 10:27:19
10 variations in the load presented to the buffer 10:27:22
11 don't affect the performance of the 10:27:27
12 sample-and-hold. 10:27:29

13 So it's a way of preventing variations in 10:27:30
14 the load impedance from affecting the overall 10:27:32
15 performance of the circuit. 10:27:36

16 Q Is that because the buffer stage presents 10:27:37
17 a high-impedance load to the capacitor? 10:27:42

18 A In a typical sample-and-hold 10:27:48
19 configuration, it will be relatively high 10:27:50
20 impedance. You know, "high" is a kind of a 10:27:55
21 relative term, but a relatively high impedance is 10:27:59
22 presented by the buffer stage. 10:28:02

1 Q And the goal of the buffer stage is to 10:28:04
2 ensure that the ADC receives a stable voltage for 10:28:09
3 accurate digital conversion. Correct? 10:28:14

4 A Yeah, you want the buffer to basically 10:28:21
5 perfectly duplicate the voltage at its input at 10:28:22
6 its output, irrespective of anything that the 10:28:26
7 analog-to-digital converter is doing. It has its 10:28:28
8 own very complicated set of operations, and it can 10:28:32
9 present a very -- a highly variable load to the -- 10:28:35
10 to a circuit. So the buffer prevents that high 10:28:41
11 variability from degrading performance. 10:28:44

12 Q So if the buffer stage wasn't there, 10:28:46
13 potentially the ADC would alter the voltage held 10:29:01
14 by the capacitor, which would lead to an 10:29:03
15 inaccurate digital conversion. 10:29:07

16 Is that correct? 10:29:11

17 MR. DAY: Object to form. 10:29:13

18 A Well, it -- yeah, I mean, it's a kind of 10:29:14
19 a hypothetical, which I'd be reluctant to, you 10:29:16
20 know, give a categorical answer to. 10:29:20

21 And the reason for that is different 10:29:23
22 A-to-D converters have different types of input 10:29:25

1 impedance and different, you know, types of

10:29:28

2 operation. So it's a general statement. It's --

10:29:30

3 you know, it's not really clear.

10:29:36

4 You know, it's clear that the authors in

10:29:37

5 this case felt that a buffer stage was necessary.

10:29:40

6 Perhaps they had a particular A-to-D converter

10:29:42

7 that they were using where this was required.

10:29:45

8 Q And a buffer stage is designed to present

10:29:48

9 a high-impedance load and to hold the voltage at

10:29:51

10 the capacitor. Correct?

10:29:55

11 MR. DAY: Object to form.

10:29:59

12 A Well, yeah, in a classic sample-and-hold

10:30:00

13 design you design that the load impedance to be

10:30:02

14 high, high enough so that the capacitor maintains

10:30:07

15 its voltage at a relatively constant rate.

10:30:12

16 You know, actually, you know, Avitabile

10:30:18

17 does a very nice analysis of this, actually, this

10:30:23

18 effect, actually. And if you look at Equation 14

10:30:26

19 there is, you know, an expression that relates to

10:30:29

20 the load resistance, what you called the buffer

10:30:31

21 input, to the -- to the impedance looking into the

10:30:34

22 bridge.

10:30:37

1	So there are -- this is analyzed very	10:30:38
2	carefully in -- in the paper. And, you know, and	10:30:41
3	that equation actually would probably determine	10:30:45
4	kind of the optimum RL for the application.	10:30:47
5	Q So after the buffer stage, the signal is	10:30:56
6	then fed into an ADC or analog-to-digital	10:31:13
7	converter. Correct?	10:31:18
8	A Yes, it's fed into an analog-to-digital	10:31:20
9	converter.	10:31:22
10	Q And Page 338 of Avitabile, which is PDF	10:31:24
11	Page 2, the first sentence of the right-hand	10:31:33
12	column says, "As the digital conversion requires	10:31:38
13	each sample to be held to a fixed value during the	10:31:40
14	conversion interval, it is convenient to perform	10:31:43
15	both sampling and holding operations in one step	10:31:45
16	at this point."	10:31:48
17	Do you see that?	10:31:50
18	A Yes.	10:31:53
19	Q Can you explain what that means?	10:31:54
20	A Yeah. So let me just read down a little	10:32:02
21	bit.	10:32:11
22	Yeah, it's an odd sentence. And I think	10:33:16

1 what it means is that the A-to-D

10:33:18

2 converter -- A-to-D converters typically require

10:33:28

3 that the input be held at a constant value for at

10:33:32

4 least, like, half of the sample interval.

10:33:38

5 And so you want the sample-and-hold to be

10:33:46

6 able to do that, you want it to be able to produce

10:33:48

7 an output that's constant for a, like, half --

10:33:50

8 half clock period, you know, for example.

10:33:54

9 And so you kind of want a circuit that

10:34:00

10 will provide that constant value to the A-to-D

10:34:02

11 converter. And so that sampling and then holding

10:34:07

12 for a long period of time can be provided by an SH

10:34:11

13 circuit. So I think that that's what -- what that

10:34:16

14 means, is that you want to sample and then hold

10:34:21

15 for, you know, long enough for the A-to-D

10:34:27

16 converter to do its job. And they call that, that

10:34:30

17 time period, the conversion interval.

10:34:34

18 Q So the ADC is seeing discrete voltage

10:34:36

19 values, and that is considered the output of the

10:34:43

20 sample-and-hold circuit. Correct?

10:34:45

21 MR. DAY: Object to form.

10:34:49

22 A I'm sorry, could you ask the question

10:34:51

1	again?	10:34:52
2	Q Sure. The ADC sees discrete voltage	10:34:52
3	values, and that is considered the output of the	10:34:58
4	sample-and-hold circuit. Correct?	10:35:01
5	A Well, the -- ideally the A-to-D sees	10:35:04
6	constant -- I'm not sure "discrete" is the right	10:35:10
7	word -- constant input values. And that is the	10:35:13
8	output of the sample-and-hold circuit. Ideally.	10:35:15
9	Q So different levels of voltage are the	10:35:20
10	output. Correct?	10:35:26
11	A They're -- they're -- yes, there are	10:35:29
12	certainly different levels of output from the	10:35:31
13	sample-and-hold circuit.	10:35:36
14	Q If you turn to Avitabile, that's PDF Page	10:35:39
15	3, the -- it's a sentence in the first paragraph	10:35:55
16	in the left column. And it states, "In TH mode	10:36:06
17	the input RF signal is sampled after a convenient	10:36:17
18	acquisition time, defined as the time to settling	10:36:22
19	within one half of the LSB of the steady-state at	10:36:26
20	full-speed input signal. Thus, at the time the	10:36:30
21	switch is turned off, nominally the whole of the	10:36:33
22	input waveform drops across the hold capacitor."	10:36:37

1	Do you see that?	10:36:43
2	A I do see that, yes.	10:36:44
3	Q And when Avitabile says that the whole of	10:36:45
4	the input waveform drops across the hold	10:36:53
5	capacitor, that's referring to the fact that the	10:37:01
6	capacitor is holding a voltage. Correct?	10:37:03
7	MR. DAY: Object to form.	10:37:11
8	A Yeah, I'm sorry, could you ask the	10:37:13
9	question again?	10:37:15
10	Q The language that when the switch is	10:37:16
11	turned off, nominally the whole of the input	10:37:21
12	waveform drops across the hold capacitor, is	10:37:24
13	referring to the fact that the capacitor is	10:37:26
14	holding a voltage. Correct?	10:37:36
15	A Yes, it's referring to the fact that the	10:37:40
16	capacitor is holding a voltage. And I think that	10:37:42
17	the author says the whole of the input waveform.	10:37:48
18	And I think what that -- what they mean by that is	10:37:52
19	that the entirety of the input voltage, in other	10:37:55
20	words the input voltage and the voltage across the	10:37:58
21	capacitor, are equal to each other. So the hold	10:38:02
22	capacitor has the -- has the same voltage as the	10:38:06

1 input waveform voltage at the time the switch is 10:38:10
2 turned off. 10:38:14

3 Q So the voltage on the capacitor in 10:38:14
4 Avitabile is held steady, so the ADC can sample -- 10:38:31
5 sample it accurately. 10:38:40

6 Is that correct? 10:38:42

7 A Well, I think referring back to a few 10:38:45
8 minutes ago when we were talking about this, when 10:38:49
9 the switch -- ideally, when the switch opens, and 10:38:51
10 Avitabile here says when the switch is turned off, 10:38:58
11 but I would say when the switch opens, the input 10:39:01
12 voltage is -- is on the hold capacitor and it is 10:39:05
13 maintained there during the hold period. 10:39:10

14 Q Avitabile also describes some prototype 10:39:54
15 circuits which are found on, it looks like PDF 10:40:03
16 Page 3. Starts with discussion, and there is an 10:40:09
17 SH1 prototype and an SH2 prototype. Correct? 10:40:16

18 A Yes, there's an SH1 and an SH2 prototype. 10:40:23

19 Q And each of these prototypes functions as 10:40:27
20 we previously discussed in relation to Figure 2 of 10:40:32
21 Avitabile. Correct? 10:40:36

22 A I'm sorry, could you ask the question 10:40:43

1	again? I was trying to get to the SH2.	10:40:44
2	Q The two prototypes discussed in Avitabile	10:40:49
3	function in the same way as the circuit described	10:40:56
4	in Figure 2 of Avitabile?	10:41:01
5	MR. DAY: Object to form.	10:41:03
6	A So SH1 and SH2 are both examples of	10:41:05
7	circuits that could be modeled by the circuit in	10:41:20
8	Figure 2.	10:41:24
9	Q And the circuit, if you turn to Figure 4,	10:41:28
10	describes or illustrates the first sample-and-hold	10:41:41
11	circuit prototype. Will you describe generally	10:41:44
12	how that circuit is working?	10:41:50
13	A I'm sorry, could you repeat the question?	10:41:55
14	Q Can you describe how the circuit in	10:41:56
15	Figure 4, which is the first prototype	10:41:59
16	sample-and-hold circuit, operates?	10:42:03
17	A Yes. So I think the best place to start	10:42:07
18	is with the four diodes that appear in a ring	10:42:24
19	configuration in the middle of the drawing.	10:42:27
20	Now, when the top and bottom -- when the	10:42:31
21	top and bottom of that ring, when the top and	10:42:42
22	bottom nodes of that ring are connected to a	10:42:45

1 positive bias and a negative bias respectively, 10:42:48
2 all four diodes turn on. And, therefore, they 10:42:52
3 create a short circuit because they're on and 10:43:01
4 they're turned on very hard. They create a short 10:43:05
5 circuit, close to a short circuit, between the RF 10:43:08
6 signal on the right and the hold capacitor on the 10:43:13
7 left. 10:43:16

8 So during the time when those -- when 10:43:17
9 the -- when those diodes are on, the switch is 10:43:22
10 closed. The diode switch is closed that performs 10:43:25
11 the connection. 10:43:30

12 Now, and then, conversely, when the top 10:43:32
13 and bottom of that ring are set to the same 10:43:40
14 voltage, then the diodes are at zero volts each, 10:43:43
15 and they're off. And so when the top and bottom 10:43:48
16 of the ring is -- are at equal voltages, the 10:43:51
17 switch is open and no current flows from the 10:43:58
18 signal to the hold capacitor. 10:44:01

19 So the control for this switch is the 10:44:04
20 MESFET, which appears on the left. And the MESFET 10:44:11
21 switch controls the energy transfer of the -- of 10:44:16
22 the diode circuit from the source to the hold 10:44:22

1 capacitor. And it does this by the pulse 10:44:26
2 generator, which is on the far left there. And 10:44:33
3 the pulse generator has a little square wave, you 10:44:36
4 know, in it. And when the square wave is 10:44:47
5 negative, the MESFET switch is off. And so the 10:44:50
6 top of the ring goes up, the bottom of the ring -- 10:44:58
7 it tries to go up to V bias. The bottom of the 10:45:04
8 ring tries to go down to minus V bias. And the 10:45:07
9 diode -- diodes are on. 10:45:10

10 So the MESFET switch controls the energy 10:45:12
11 transfer through the circuit. And enables the 10:45:15
12 energy transfer. 10:45:21

13 And then when the -- and then when the 10:45:21
14 MES -- the gate to the MESFET goes high, which is 10:45:24
15 shown in that little circle in front of the -- in 10:45:27
16 the pulse generator, then the MESFET is on and the 10:45:29
17 drain -- the two terminals at the top and bottom 10:45:38
18 of that MESFET collapse to be equal to each other. 10:45:40
19 And that makes the diode, the voltages at the top 10:45:45
20 and bottom of the diode ring, to be equal to each 10:45:50
21 other, and that turns off the diodes. 10:45:55

22 So the diodes are then off under control 10:45:57

1 of the switch. And no energy can flow from the RF
2 signal to the hold capacitor.

3 And so that's I think a complete
4 explanation of how Figure 4 works.

5 Q Thank you for that.

6 Figure 4 shows the hold capacitor but
7 doesn't show the RL as was identified in Figure 2.

8 Is that correct?

9 A Yeah, RL is not included here. I mean, I
10 kind of -- it's kind of assumed, and anyone, you
11 know, reading the paper would understand that
12 there would be an RL attached there.

13 Q And then after the RL you would assume
14 that there is an ADC. Correct?

15 A And then there would be an AD -- and then
16 after the, you know, RL there would be an ADC, and
17 then there would be a digital processor. So,
18 yeah, all of that is kind of understood at this
19 schematic level of the -- of the paper.

20 Q And so basically the circuit of Figure 4
21 operates or functions substantially the same or
22 almost similar -- identical to the Figure 2

10:46:01

10:46:05

10:46:09

10:46:11

10:46:14

10:46:18

10:46:22

10:46:33

10:46:36

10:46:39

10:46:43

10:46:44

10:46:48

10:46:50

10:46:52

10:46:54

10:46:58

10:47:01

10:47:04

10:47:07

10:47:26

10:47:28

1 equivalent circuit model.

10:47:33

2 Is that -- is that accurate?

10:47:36

3 A Yeah.

10:47:38

4 MR. DAY: Objection to form.

10:47:38

5 A I feel that -- I feel that Figure 4 is
6 a -- you know, Figure 2 is a kind of a high-level
7 notional equivalent circuit, a model of a -- of a
8 sampling circuit. And then Figure 4 is the
9 transistor-level, diode-level version of that, and
10 shown in Figure 2.

10:47:39

10:47:44

10:47:49

10:47:55

10:48:01

10:48:06

11 Q And the RF signal coming into the
12 circuit, is that a modulated signal?

10:48:08

10:48:15

13 A Well, the -- you know, simply looking at
14 the schematic, you can't tell. But clearly from
15 the context of the paper and from the type of
16 problems that the paper is addressing, that RF
17 signal would be a modulated -- would most
18 typically be a modulated signal.

10:48:19

10:48:25

10:48:28

10:48:32

10:48:36

10:48:39

19 Q Would there be differences in how the
20 circuit functioned between a modulated and
21 nonmodulated RF signal?

10:48:41

10:48:45

10:48:51

22 MR. DAY: Object to form.

10:48:54

1 A So if the RF signal at the input of 10:48:56
2 Figure 4 were unmodulated, I don't believe it 10:48:58
3 would change the fundamental operation of the 10:49:03
4 circuit. It would change the output waveform and 10:49:07
5 how the output waveform looks, but it wouldn't 10:49:11
6 change the operation of the circuit. 10:49:13

7 Q Would there be any design considerations 10:49:15
8 for the LO of the circuit, given a modulated 10:49:21
9 versus unmodulated RF signal? 10:49:28

10 MR. DAY: Object to form. 10:49:30

11 A So your question is would you change -- 10:49:35
12 so on the left-hand side of this drawing is the 10:49:38
13 pulse generator, and that's the local oscillator, 10:49:40
14 or LO as you referred to it. So I guess the 10:49:42
15 question is would you change the LO if you were 10:49:44
16 using, say, an unmodulated RF signal versus a 10:49:50
17 modulated signal. And I don't see any reason why 10:49:55
18 you would have to make that change. 10:49:59

19 You know, you don't need a -- I mean, I'm 10:50:03
20 not sure what the point is of an unmodulated 10:50:07
21 signal to the input of a circuit like this, but it 10:50:11
22 certainly wouldn't change the LO design. 10:50:14

1	Q	And specifically these circuits are	10:50:16
2		designed for around a 1 gigahertz input waveform.	10:50:31
3		Is that correct?	10:50:36
4	A	Well --	10:50:39
5		MR. DAY: Object to form.	10:50:40
6	A	-- yeah, that's a really good question.	10:50:41
7		I mean, I think these circuits -- if you	10:50:45
8		look at Figure 4, that's a very, very well	10:50:48
9		understood circuit that has been around for many	10:50:54
10		decades. And it can be used at frequencies and	10:50:58
11		has been used at frequencies from 100 kilohertz to	10:51:04
12		100 gigahertz. So that structure, you know, the	10:51:07
13		schematic itself, has -- can be and has been used	10:51:13
14		over an incredibly, incredibly wide range of	10:51:18
15		frequencies.	10:51:21
16		In this particular case it's at around a	10:51:22
17		gigahertz.	10:51:25
18	Q	The bandpass filters prior to the	10:51:27
19		sample-and-hold circuit as we saw in Figure 1.	10:51:35
20		Would need to change value-wise based on the	10:51:39
21		frequency of the input waveform.	10:51:56
22		Is that accurate?	10:52:00

1 MR. DAY: Object to form. 10:52:02

2 A Yes, I think that's true. I mean, the -- 10:52:05

3 you know, the bandpass filter, if you go to higher 10:52:08

4 frequencies, you would need a higher frequency 10:52:12

5 bandpass filter. If you went to lower 10:52:14

6 frequencies, you would need a lower frequency. 10:52:16

7 So, clearly, the range of frequencies 10:52:19

8 that you want to address would potentially need to 10:52:22

9 change as you change the desired input 10:52:27

10 frequencies. 10:52:30

11 Q So depending on the desired input 10:52:32

12 frequencies, you would have to necessarily change 10:52:36

13 the bandpass filter in some way. 10:52:40

14 Is that correct? 10:52:42

15 A Depending on the desired frequencies and 10:52:46

16 also depending on the -- you know, the range of 10:52:48

17 other inputs that are kind of out there. You 10:52:53

18 know, as I mentioned before, like an antenna kind 10:52:58

19 of picks up a very, very wide range of 10:53:01

20 frequencies. 10:53:04

21 But you might have types of systems that 10:53:04

22 don't pick up wide ranges of frequencies and then 10:53:06

1 the bandpass filter requirements might be much 10:53:10
2 more modest. So it depends. Also, it depends on 10:53:14
3 the signals that you're trying to, you know, 10:53:16
4 convert or address. But it also depends on what 10:53:19
5 types of extraneous signals appear at the input as 10:53:21
6 well. 10:53:24

7 Q Does different types of modulation affect 10:53:30
8 the bandpass filter? 10:53:42

9 A Yeah, that's a good question, too. 10:53:46

10 MR. DAY: Object to form. 10:53:49

11 A So different types of modulation result 10:53:51
12 in different bandwidths of the modulated signal. 10:53:57
13 And you have to design the bandpass filter so that 10:54:03
14 it accommodates the modulation bandwidth of the 10:54:06
15 desired signal, but also rejects, you know, all of 10:54:13
16 the extraneous signals at different frequencies. 10:54:17

17 So, yes, the modulation bandwidth is one 10:54:20
18 determining factor for the design of the bandpass 10:54:25
19 filter. 10:54:28

20 Q Would the LO of the sample-and-hold 10:54:29
21 circuit need to be modified in any way, depending 10:54:42
22 on modulation of the input? 10:54:46

1	MR. DAY: Object to form.	10:54:54
2	A So I think your question is would you	10:55:05
3	change the local oscillator waveform in response	10:55:09
4	to variations in the modulation bandwidth. Or	10:55:16
5	changes in the modulation bandwidth. And	10:55:25
6	generally, no, I would say.	10:55:32
7	You know, there might be some cases where	10:55:35
8	the kind of sharpness of the edges of the local	10:55:46
9	oscillator would affect a little bit the frequency	10:55:53
10	response of the down-converted signal. And	10:55:57
11	depending on how wide the modulation bandwidth is	10:56:02
12	and how sharp those LO edges are, there might be	10:56:06
13	an effect.	10:56:11
14	So, you know, in engineering, a typical	10:56:13
15	engineer would call that a second-order effect.	10:56:17
16	It's something that, you know, is -- after doing	10:56:19
17	the initial system design, you'd have to look at	10:56:24
18	that a little bit to see if there's a possible	10:56:27
19	effect.	10:56:29
20	So there's a possible -- a possibility of	10:56:30
21	an effect that you might want to consider a little	10:56:31
22	bit in the design of the LO waveform.	10:56:35

1 Q The Avitabile reference keeps mentioning 10:56:43
2 the term "digital down-converter." Why do you 10:56:53
3 think Avitabile uses digital down-converter? 10:56:58

4 A Well, you know, I don't think that the 10:57:18
5 author is very specific on this. But I'll tell 10:57:22
6 you what I think was going on here. And this is 10:57:28
7 from a paper of 1996, so this is almost 30 years 10:57:31
8 ago now. 10:57:36

9 So, you know, at the time people were 10:57:37
10 struggling with the fact that modern communication 10:57:48
11 systems used lots of different frequencies and 10:57:54
12 lots of different modulation types and lots of 10:57:57
13 different services. And you -- there was a desire 10:58:02
14 to use just kind of one RF transceiver to address 10:58:07
15 all of these different standards. 10:58:15

16 And so this particular architecture, it's 10:58:20
17 very simple. It has the advantage that you can 10:58:27
18 change the LO frequency and, you know, 10:58:36
19 down-convert different signals at different 10:58:41
20 frequencies to baseband, simply by changing the LO 10:58:43
21 frequency. And so that's very nice for -- and 10:58:49
22 then you -- and then you do a very simple 10:58:54

1 down-conversion, as it says here, to IF. And then
2 you would have an A-to-D converter and a baseband
3 processor that would do all the different signal
4 processing.

5 So the move at the time from kind of a
6 purely analog approach to one that's a -- has a
7 minimum amount of analog circuitry and then a lot
8 of digital signal processing, that was a long-felt
9 need. And this particular architecture, you know,
10 was thought at the time to be well-suited for that
11 kind of evolution.

12 So I think that that's what they meant by
13 a digital, you know, down-conversion. It's a very
14 simple analog approach that can -- whose output
15 can go right into an A-to-D converter, and then
16 subsequent processing is done digitally.

17 Q The capacitor C -- strike that.

18 The capacitor, or the hold capacitor in
19 these circuits -- strike that.

20 Would you consider Avitabile a voltage
21 sampling system?

22 MR. DAY: Objection to form.

1 A Well, I would say that Avitabile samples 11:00:28
2 the input voltage and stores that input voltage on 11:00:32
3 the -- on the capacitor. And the capacitor, you 11:00:42
4 know, stores the energy that's transferred from 11:00:46
5 the -- from VIN. 11:00:48

6 So I guess that's what I would call it. 11:00:53
7 I would say that it samples the voltage and then 11:00:55
8 stores that voltage on the -- on the capacitor. 11:00:57

9 Q Designers would know, because the 11:00:59
10 capacitor is a hold capacitor, that that 11:01:11
11 capacitance value should be small. 11:01:14

12 Is that accurate? 11:01:19

13 MR. DAY: Object to form. 11:01:20

14 A Well, that's a -- an interesting design 11:01:22
15 constraint. And you want the capacitor to be not 11:01:26
16 too small and not too big. And you want it to be 11:01:34
17 right-sized. 11:01:40

18 And, you know, actually Avitabile has a 11:01:42
19 bunch of equations, if you look at equation, you 11:01:45
20 know, I would say, you know, like Equation 13, 11:01:52
21 which talks about the jitter a little bit, and 11:01:59
22 Equation 8, which talks about the hold variation. 11:02:02

1	So you want -- you want the capacitor to	11:02:06
2	be, you know, pretty big, because that, you know,	11:02:10
3	minimizes the noise and has good noise effects.	11:02:18
4	But you don't want it to be too big, because you	11:02:21
5	want to be able to sample the voltage accurately	11:02:23
6	on the capacitor.	11:02:26
7	And so, you know, I don't know if big or	11:02:30
8	small, it has to be right-sized. There are a	11:02:32
9	variety of design constraints that determine what	11:02:36
10	that value should be.	11:02:38
11	Q If the capacitor was on the larger size,	11:02:39
12	Avitabile would not be able to accurately sample	11:02:58
13	the voltage of the input. Correct?	11:03:01
14	MR. DAY: Object to form.	11:03:05
15	A Well, you can imagine a scenario where	11:03:07
16	that hold capacitor, which is labeled C in Figure	11:03:11
17	2, is enormous. You know, infinitely big. And if	11:03:15
18	it's infinitely big, then you would not be able to	11:03:22
19	accurately sample VIN of T on it.	11:03:29
20	So as you turn that capacitor down from a	11:03:35
21	ridiculously large value to something smaller and	11:03:39
22	smaller and smaller, you get a more accurate	11:03:42

1 representation of VIN of T, you know, on -- you 11:03:47
2 know, at VOUT. At the same time your noise is 11:03:53
3 going up, which is -- which is a bit of a problem. 11:03:56
4 And, also, your input impedance is -- is rising, 11:04:01
5 and that's -- and both of these effects are 11:04:05
6 described in the paper. 11:04:07

7 So there's a certain point where the 11:04:08
8 capacitor is the right value. VIN of T is 11:04:11
9 accurately transferred to the output voltage, the 11:04:16
10 noise is minimized, and, you know, the input 11:04:21
11 impedance is the correct value. 11:04:25

12 So these are all things that determine 11:04:27
13 what the right value of C is. 11:04:30

14 Q When the capacitor of Avitabile changes 11:04:38
15 from a first sample to a second sample, would you 11:04:53
16 agree that if that next sampled voltage is lower 11:05:04
17 than what was the voltage of the previous sample, 11:05:08
18 the charge would dissipate to ground? 11:05:14

19 MR. DAY: Object to form. 11:05:21

20 A So when VIN of T, so let me -- I'm sorry, 11:05:33
21 I'll back up. 11:05:40

22 When the -- you hold a certain voltage at 11:05:41

1	VOUT of T. And then on the next closing of the	11:05:46
2	switch VIN of T is lower, Capacitor C will	11:05:53
3	discharge to that lower value and current will	11:06:00
4	flow out of the capacitor and back to VIN of T.	11:06:08
5	And then to ground. But maybe more precisely to	11:06:18
6	VIN of T.	11:06:21
7	And so as the -- and I'm assuming at this	11:06:23
8	point that RL does not affect that charge transfer.	11:06:27
9	So VIN of T will -- the charge will flow back	11:06:34
10	through the switch to VIN of T as the voltage is	11:06:37
11	lowered.	11:06:40
12	Q You didn't perform any sort of	11:06:51
13	simulations on any of the circuits described in	11:06:53
14	Avitabile, did you?	11:06:59
15	MR. DAY: Object to form.	11:07:04
16	A I have not performed any circuit	11:07:05
17	simulations on any of the circuits in Avitabile.	11:07:07
18	Q Have you done any sort of mathematical	11:07:15
19	analysis on any of the circuits of Avitabile?	11:07:17
20	MR. DAY: Object to form.	11:07:19
21	A I haven't done any mathematical analysis.	11:07:24
22	I mean, I've reviewed, you know, equations 1	11:07:27

1 through 14, pretty carefully actually. And I have 11:07:30
2 verified that they're -- I believe that they're 11:07:38
3 correct. 11:07:41

4 Q What did you use in your determination to 11:07:49
5 say that Avitabile stores nonnegligible amounts of 11:07:58
6 energy, or the Capacitor C holds -- stores 11:08:05
7 nonnegligible amounts of energy? 11:08:10

8 MR. DAY: Object to form. 11:08:11

9 A Well, you know, as I said earlier, you 11:08:13
10 know, I -- nonnegligible energy means energy that 11:08:17
11 is distinguishable from noise. And so if you look 11:08:22
12 at Figure 6 or Figure 7 in Avitabile as a 11:08:27
13 representative example, they show outputs of the 11:08:34
14 SH1 circuit. And those waveforms, based on my 11:08:38
15 knowledge of the field and experience, are clearly 11:08:43
16 distinguishing from noise, they are periodic. And 11:08:49
17 they are at a period that corresponds to the 11:08:51
18 desired IF output. So that's clearly not noise. 11:08:52
19 Noise is completely random. And these signals are 11:08:59
20 also much, much larger than any noise signal. 11:09:02

21 So it's clear to me that in this case 11:09:06
22 Figure 6 and 7, for example, the hold capacitor is 11:09:10

1	storing a nonnegligible amount of noise -- of	11:09:13
2	signal, sorry. A nonnegligible amount.	11:09:18
3	Q The voltage on the hold capacitor in	11:09:21
4	Avitabile is not the same thing as energy storage.	11:09:29
5	Is that correct?	11:09:37
6	MR. DAY: Object to form.	11:09:38
7	A Well, energy and voltage are different	11:09:39
8	things, and we discussed this earlier, you know.	11:09:41
9	Voltage is measured in volts and joules -- and	11:09:44
10	energy is measured in joules.	11:09:46
11	The voltage in the hold capacitor --	11:09:48
12	sorry. The energy stored on the hold capacitor	11:09:56
13	has a certain voltage associated with it. And the	11:09:58
14	relationship between the energy stored on the hold	11:10:00
15	capacitor and the voltage is one half CV squared.	11:10:02
16	So they are -- when you talk about energy stored	11:10:07
17	in the capacitor, you also -- there is also an	11:10:10
18	associated voltage. And when there is a voltage	11:10:13
19	on the capacitor, there is also an associated	11:10:15
20	stored energy.	11:10:17
21	Q While the two are related, they are not	11:10:20
22	the same measurements. Correct?	11:10:31

1	MR. DAY: Object to form.	11:10:35
2	A You know, energy and voltage are	11:10:38
3	different physical quantities, and they're related	11:10:40
4	to each other directly through the equation one	11:10:43
5	half CV squared.	11:10:48
6	Q Simply looking at the voltage values on a	11:10:52
7	capacitor does not tell you the stored amounts of	11:10:58
8	energy on that capacitor if you don't have the	11:11:03
9	capacitance of the capacitor.	11:11:06
10	Is that accurate?	11:11:08
11	MR. DAY: Object to form.	11:11:09
12	A Well, you know, as I said before, you	11:11:13
13	know, the equation for energy stored in the	11:11:15
14	capacitor is one half CV squared. So in order to	11:11:18
15	know the energy -- if you know the voltage, in	11:11:22
16	order to know the energy you would have to know	11:11:27
17	the capacitance also.	11:11:28
18	MS. MANDIR: We've been going about an	11:11:46
19	hour. Is this time good for a break? We can go	11:11:48
20	off the record.	11:11:52
21	THE WITNESS: I think that would be	11:11:53
22	great.	11:11:54

1	(A discussion was held off the record.)	11:12:00
2	MS. MANDIR: Let's go off the record.	11:12:04
3	MR. DAY: Yeah.	11:12:06
4	VIDEO SPECIALIST: We are going off the	11:12:07
5	record. The time is 11:12.	11:12:08
6	(A recess was taken.)	11:12:10
7	VIDEO SPECIALIST: We are now back on the	11:19:11
8	record. The time is now 11:19.	11:19:13
9	You may proceed.	11:19:15
10	BY MS. MANDIR:	11:19:18
11	Q Dr. Larson, did you discuss the substance	11:19:19
12	of your testimony with anyone during the break?	11:19:20
13	A No, not at all.	11:19:23
14	Q Okay. Let's go back to Figure 2 of	11:19:24
15	Avitabile.	11:19:30
16	A Okay.	11:19:31
17	Q And do you agree that the impedance of RL	11:19:31
18	affects how much energy is transferred from the	11:19:43
19	switch?	11:19:51
20	MR. DAY: Object to form.	11:19:52
21	A So RL affects the amount of energy that	11:19:56
22	is transferred from VIN of T over on the far left	11:20:01

1	through the switch.	11:20:07
2	Q And a POSITA would understand that here	11:20:16
3	RL is designed to have a high impedance as a buffer	11:20:21
4	stage following the sample-and-hold circuit.	11:20:24
5	Correct?	11:20:29
6	MR. DAY: Object to form.	11:20:31
7	A Yeah, I mean, I think that RL would be a	11:20:35
8	relatively high impedance in this case, and RL	11:20:40
9	represents the buffer stage.	11:20:44
10	And, you know, with the caveat that, as I	11:20:49
11	said earlier, you know, RL has multiple affects on	11:20:54
12	the system, which are sort of described in the	11:21:00
13	various equations in Avitabile. So there's an	11:21:02
14	optimum value for RL, and that's what determines	11:21:05
15	probably what it -- the input resistance of the	11:21:09
16	buffer would be. But it would be probably	11:21:13
17	relatively high.	11:21:14
18	Q And a high impedance would -- strike	11:21:15
19	that.	11:21:29
20	A high impedance at RL would have the	11:21:30
21	effect of transferring less energy versus a lower	11:21:38
22	impedance. Correct?	11:21:44

1	MR. DAY: Object to form.	11:21:46
2	A Well, there's -- yeah, I mean, a high	11:21:50
3	RL -- an infinitely high RL would cause there to	11:22:04
4	be, you know, no energy through -- you know, into	11:22:09
5	RL. And at the same token, an infinitely low RL	11:22:17
6	would also lower the energy quite a bit. So I	11:22:24
7	guess there's an optimum value of RL to maximize	11:22:26
8	the energy.	11:22:29
9	But a high RL certainly lowers the energy	11:22:30
10	past a certain value that is delivered to RL from	11:22:36
11	VIN of T.	11:22:40
12	Q So just to clean all that up, a high RL	11:22:43
13	prevents the flow of energy from the switch	11:23:07
14	compared to if the RL was lower.	11:23:12
15	Is that correct?	11:23:17
16	MR. DAY: Object to form.	11:23:18
17	A Well, you know, it -- once again, it	11:23:20
18	depends a little bit on the specific, you know,	11:23:22
19	value of RL that we're talking about here. So this	11:23:28
20	is -- this is kind of hypothetical.	11:23:31
21	But generally speaking, the RL	11:23:33
22	representing the input resistance of the buffer is	11:23:38

1 kind of high, because you don't want to discharge 11:23:41
 2 that capacitance. And as you make RL higher and 11:23:44
 3 higher, less energy -- or less power is dissipated 11:23:49
 4 in RL. 11:23:53

5 Q And the stored energy is not equal to the 11:23:57
 6 voltage. Correct? 11:24:19

7 MR. DAY: Object to form. 11:24:21

8 A Which stored energy are you referring to 11:24:24
 9 in that question? 11:24:27

10 Q Stored energy of the hold capacitor is 11:24:27
 11 not the same as the voltage of the capacitor. 11:24:35
 12 Correct? 11:24:38

13 A So the -- you know, the energy is -- the 11:24:45
 14 energy and voltage are different physical 11:24:47
 15 quantities. Energy is measured in joules, and 11:24:49
 16 volts is measured in volts. There's a direct 11:24:52
 17 relationship between energy and voltage on a 11:24:55
 18 capacitor, which is one half CV squared. 11:24:59

19 Q To hold a voltage value during an off 11:25:34
 20 time of the switch, a POSITA understands that RL 11:25:37
 21 needs to be a high impedance load. Correct? 11:25:43

22 MR. DAY: Object to form. 11:25:47

1 A Well, I think if you asked a POSITA that 11:25:49
2 question, you know, what they would say was that 11:25:52
3 the product of RL and C should be much, much longer 11:25:56
4 than the time interval that you want to hold it 11:26:02
5 over. 11:26:04

6 So there's an equation that answers your 11:26:08
7 question very precisely, and that -- and it's true 11:26:11
8 that the larger the value of the resistor, the 11:26:14
9 more you satisfy that equation. 11:26:19

10 Q Would you agree that Avitabile discloses 11:26:27
11 a circuit which is intended to prevent the 11:26:43
12 discharge of the hold capacitor between samples? 11:26:46

13 MR. DAY: Object to form. 11:26:50

14 A Well, I would say that Avitabile, you 11:26:54
15 know, describes a circuit -- a sample-and-hold 11:26:56
16 circuit that -- and the reason I'm hesitating is 11:26:59
17 I'm looking for a good -- I'm looking for a quote 11:27:06
18 from the paper that would kind of answer your 11:27:08
19 question. 11:27:20

20 And Avitabile does a very nice job, 11:27:20
21 actually, of this. And if you look at, like, 11:27:24
22 Equation 11 in Avitabile, they talk about the drop 11:27:27

1	rate of the -- which is a measure of the error.	11:27:31
2	And it's exactly what I said before. It's the	11:27:36
3	ratio of the -- of the time to the RL C.	11:27:40
4	So if you want to have a minimum drop	11:27:45
5	rate, which is -- which is usually a good thing	11:27:47
6	for a sample-and-hold circuit, you would want RL,	11:27:50
7	the product of RL and C to be very large.	11:27:53
8	So Avitabile talks about this very	11:27:58
9	directly, that you want to minimize the drop rate.	11:28:00
10	Q And when you're referring to drop rate,	11:28:03
11	is that illustrated in Figure 7 of Avitabile,	11:28:05
12	referencing the droop?	11:28:16
13	A Yeah, so Figure 7 is a -- is a time	11:28:20
14	domain measurement of the output, really kind of	11:28:22
15	zoomed in. And it's -- I think what you see there	11:28:27
16	is the slight discharge of the hold capacitor	11:28:32
17	during the hold period. And, you know, it's	11:28:41
18	called a droop off in the paper. It's -- yeah, a	11:28:45
19	drop off or droop off, both are synonymous in this	11:28:48
20	case, I think.	11:28:52
21	So I believe that Figure 7 in Avitabile	11:28:53
22	shows this drooping effect, or dropping effect.	11:28:57

1	Q	And the droop off or the drop off is	11:29:01
2		practical implementation error, not something that	11:29:09
3		Avitabile would want. Correct?	11:29:14
4	MR. DAY:	Object to form.	11:29:17
5	A	Well, you know, that's an interesting	11:29:20
6		question. So I think you said that's an error.	11:29:22
7		And -- or a design error. And it's certainly not	11:29:30
8		something that you'd like to see.	11:29:36
9		But, you know, whether it's a bad thing	11:29:41
10		from a system perspective depends a little bit on	11:29:47
11		the application. But it -- it doesn't exactly	11:29:50
12		match the ideal waveform that a perfect	11:29:55
13		sample-and-hold would exhibit.	11:29:59
14	Q	The droop off does not contribute to the	11:30:04
15		formation of the output signal of Avitabile.	11:30:10
16		Correct?	11:30:17
17	MR. DAY:	Object to form.	11:30:19
18	A	Well, I mean, the output signal is what	11:30:21
19		it is. And the output signal includes the droop	11:30:25
20		off, so the droop off does contribute to the	11:30:28
21		output of the -- of the -- of the circuit in this	11:30:30
22		case.	11:30:36

1	Q	Ideally Avitabile circuit would have no	11:30:36
2		droop off. Correct?	11:30:41
3	A	Right. An ideal sample-and-hold circuit	11:30:43
4		would not exhibit droop off.	11:30:46
5	Q	The droop off is due to parasitics of the	11:30:50
6		capacitor.	11:31:02
7		Is that correct?	11:31:04
8	MR. DAY:	Object to form.	11:31:05
9	A	Well, it's -- it's -- once again, now	11:31:07
10		you're asking sort of what's the source of the	11:31:12
11		droop off that's shown here. And it's -- it's a	11:31:17
12		little -- you know, these are complicated systems,	11:31:23
13		complicated, you know, measurements.	11:31:29
14		So the droop off is probably not due to	11:31:33
15		the parasitics of the capacitor, because the	11:31:37
16		capacitor doesn't have, like, parallel resistance	11:31:40
17		that would cause it to droop off.	11:31:45
18		It may be due to parasitics, you know, in	11:31:48
19		other parts of the circuit, you know, like at the	11:31:51
20		diodes. There's also another effect here which	11:31:54
21		is -- which Avitabile talks about very nicely,	11:31:58
22		which is the feed-through capacitance in the off	11:32:00

1 state. And that's kind of, like, in Equation 10.

11:32:03

2 And so -- so Equation 10 talks about,
3 like, feed-through errors, and Equation 11 talks
4 about droop errors or drop errors. And when you
5 look at Figure 7 and you see that drop, it's a
6 combination of those two effects.

11:32:09

11:32:12

11:32:16

11:32:20

11:32:22

7 So some of that drop off may be due to
8 this LO feed-through issue. So hard to tell.
9 Hard to tell. But these are some of the factors
10 that would -- that will go into that drop off, or
11 droop off, as they say.

11:32:25

11:32:29

11:32:34

11:32:36

11:32:39

12 Q So the sample-and-hold circuit in
13 Avitabile takes a sample of the input signal by
14 turning the switch on and off. Correct?

11:32:40

11:32:56

11:33:01

15 A You know, you turn this diode bridge
16 switch combination on and off, and that transfers
17 energy from the RF signal to the hold capacitor.

11:33:13

11:33:16

11:33:24

18 Q The amount of energy transferred is
19 dependent upon the capacitance of the hold
20 capacitor and the impedance of the resistor R_L .

11:33:31

11:33:37

11:33:42

21 Correct?

11:33:48

22 MR. DAY: Object to form.

11:33:50

1	A	The amount of energy transferred from the	11:33:52
2		RF signal to the output does depend both on the	11:33:55
3		hold capacitor and on the -- on the load resistor	11:33:58
4		RL.	11:34:03
5	Q	The voltage values serve as a sample that	11:34:04
6		can be used to recover the baseband in Avitabile.	11:34:29
7		Correct?	11:34:36
8		MR. DAY: Object to form.	11:34:38
9	A	So the voltage samples at the output,	11:34:39
10		like the voltage samples in the hold capacitor,	11:34:41
11		you know, that's a -- that's a signal that --	11:34:46
12		yeah, Avitabile uses to generate the recovered	11:34:51
13		baseband signal. Or baseband or IF signal.	11:34:57
14	Q	Let's turn to a new reference. I'm going	11:35:13
15		to put -- actually, let's just turn to your	11:35:28
16		declaration for a discussion of Estabrook. I	11:35:35
17		believe starting on Page 125 of your declaration	11:35:43
18		is the beginning of your discussion about	11:35:49
19		Estabrook. And your declaration uses three	11:35:50
20		different Estabrook references as prior art.	11:35:58
21		Correct?	11:36:04
22	A	Yeah, I believe that's correct. It was	11:36:04

1	two papers and a Ph.D. dissertation.	11:36:06
2	Q Can you explain the differences between	11:36:16
3	the Estabrook references?	11:36:21
4	MR. DAY: Object to form.	11:36:25
5	A Yeah, so -- so let's see now. Let me --	11:36:27
6	let me just -- so this is Exhibit 1005, which is	11:36:32
7	a --	11:36:41
8	Q Yeah, I can --	11:36:42
9	A -- Ph.D. dissertation.	11:36:44
10	And that's kind of like a complete	11:36:45
11	summary of everything that Dr. Estabrook did as	11:36:47
12	part of her studies at Stanford. And then there	11:36:51
13	were two kind of -- there's a journal paper and	11:36:58
14	a -- and a conference paper.	11:37:00
15	So the -- and both of those papers are	11:37:06
16	sort of in the dissertation as well. But the	11:37:10
17	Exhibit 1016 is the conference paper. And that	11:37:14
18	was Dr. Estabrook had come up with kind of a novel	11:37:21
19	way of doing mixer analysis, using SPICE. And	11:37:25
20	mixer analysis is complicated, it's a very	11:37:33
21	complicated physical system. It's hard to analyze	11:37:36
22	accurately. And her -- her work did a very nice	11:37:39

1 job kind of advancing that. And that was 11:37:42

2 described in the -- you know, in the -- in that 11:37:44

3 conference paper. 11:37:50

4 And then the journal paper is -- I'm 11:37:51

5 sorry, they're both conference papers. Sorry. 11:37:53

6 And then the vehicular technology conference paper 11:37:55

7 was more kind of how would you build, you know, 11:37:59

8 mixers for direct conversion applications. And 11:38:04

9 that was a very important research topic at that 11:38:10

10 time, and a lot of people were doing work on it. 11:38:14

11 So that was more in the kind of circuits 11:38:16

12 and systems level. The other paper was a circuit 11:38:18

13 simulation paper. And then the thesis kind of 11:38:23

14 tied everything together. 11:38:25

15 So, very simply, that's the difference 11:38:27

16 between the three of them. 11:38:29

17 Q For one of the grounds in the petition it 11:38:30

18 uses a combination of the Estabrook thesis and 11:38:38

19 Young. I've included all of the Estabrook 11:38:50

20 references, so that's Exhibit 1005. It was 11:38:54

21 already marked as an exhibit in the IPR. 11:38:59

22 (MediaTek Exhibit 1005, previously 11:39:02

1 marked, not attached.)

11:39:04

2 Q Exhibit 1016 and Exhibit 1017 are the
3 Estabrook references.

11:39:04

4 (MediaTek Exhibit 1016 and MediaTek
5 Exhibit 1017, previously marked, not attached.)

11:39:10

6 Q But for ground 2 of the declaration and
7 the petition, it is the obviousness challenge of
8 Young in view of the Estabrook thesis. Correct?

11:39:12

11:39:12

11:39:15

11:39:24

9 A I believe that's correct. Could you
10 point me to in my declaration what you're
11 referring to?

11:39:29

11:39:30

11:39:33

12 Q Yeah. So starting on Page 110 of your
13 declaration is for the ground of -- or combination
14 of Young in view of Estabrook thesis.

11:39:35

11:39:37

11:39:44

15 A Yes. Thank you.

11:39:51

16 Q And then the ground with the combination
17 of Young in view of, let's call them the two
18 Estabrook conference papers, is starting on Page
19 170, and that is a separate ground.

11:39:52

11:39:57

11:40:01

11:40:06

20 A Yes. Yes. I believe that's correct.

11:40:08

21 Let me -- let me confirm.

11:40:12

22 Yes. Yes. Very good. I agree.

11:40:31

1 Q The Estabrook -- all three Estabrook 11:40:47
2 references are pointing to the same -- strike 11:40:49
3 that. 11:40:57

4 The circuit that you point to in all of 11:40:59
5 the Estabrook references is the same single 11:41:01
6 balance mixer. Correct? 11:41:06

7 MR. DAY: Object to form. 11:41:10

8 A So I guess you're -- so, you know, in my 11:41:11
9 declaration I refer very frequently to a 11:41:15
10 particular -- yeah. And let me just find it here 11:41:20
11 in my declaration. 11:41:28

12 So perhaps -- I refer very frequently to 11:41:34
13 Figure 14 in the thesis. And that is, yes, a 11:41:41
14 singly balanced mixer. 11:41:46

15 Q Is that the same circuit that you're 11:41:48
16 relying on between -- or among all of the 11:41:51
17 Estabrook references? 11:41:54

18 A Yeah, let me once again check my -- check 11:42:02
19 my declaration. 11:42:29

20 Yes, I believe that's correct, I use the 11:42:33
21 same circuit in all of these cases. 11:42:35

22 Q Can you please turn to, it's PDF Page 126 11:42:40

1	of your declaration. And we'll see that Figure 14	11:42:47
2	that we were just referring to in Estabrook --	11:42:53
3	A Okay.	11:42:55
4	Q -- common among all of the references.	11:42:56
5	A Page 126 you said?	11:42:58
6	Q PDF Page 126, yeah.	11:43:00
7	A Yes. Got it. So that is Declaration	11:43:01
8	Page 112 I think. And I think I'm there.	11:43:11
9	Q One -- it should be 113.	11:43:18
10	A 113. 113. Sorry. Yeah. I am there.	11:43:21
11	Q So in Paragraph -- I'm sorry, if you go	11:43:25
12	up to 112. Paragraph 120 of your declaration you	11:43:31
13	state that "Estabrook teaches a direct conversion	11:43:35
14	receiver including a single-ended mixer circuit	11:43:38
15	for down-converting received RF."	11:43:40
16	Do you see that?	11:43:43
17	A Yes, I see that. That's Paragraph 220.	11:43:45
18	Q Can you explain what a single-ended mixer	11:43:49
19	means here?	11:43:52
20	A Yeah. So our typical conception of,	11:43:59
21	like, a circuit is that there is a single input	11:44:09
22	and a single output. And a lot of circuits work	11:44:13

1 very well with just a single input and a single
2 output. 11:44:22 11:44:25

3 But in cases where you have, you know, 11:44:26
4 interference or some other kind of source of 11:44:31
5 error, we often use two signals that are -- that 11:44:39
6 are kind of out of phase with each other. And 11:44:46
7 those are sometimes called balanced circuits, or 11:44:50
8 differential circuits is also used. 11:44:53

9 And the advantage of differential 11:44:57
10 circuits is that if there's a source of 11:44:58
11 interference or noise that affects both the 11:45:01
12 positive and the negative signals, let's call them 11:45:08
13 the positive and the negative signals, then when 11:45:12
14 you subtract these two signals, even though noise 11:45:14
15 has been imposed on both of them, the noise 11:45:17
16 cancels. 11:45:20

17 So mixers are especially prone to these 11:45:21
18 interfering, you know, single-ended kind of 11:45:26
19 issues. And so sometimes people will use 11:45:31
20 a balanced mixer to minimize these effects. 11:45:38

21 And I think all Dr. Estabrook was saying 11:45:41
22 here is that she did not use any of those 11:45:43

1 techniques in her design. They weren't necessary 11:45:46
2 or, you know, they weren't necessary for the 11:45:50
3 points that she was trying to illustrate in her 11:45:53
4 research. So she was just making the point that 11:45:55
5 it's -- she just has a single input and a single 11:45:59
6 output. And there's no -- there's no cancellation 11:46:02
7 of any secondary interference effects. 11:46:11

8 Q So the single-ended mixer simply means 11:46:16
9 there's a single input, single output. Correct? 11:46:28

10 A Basically that's all it really means, 11:46:31
11 yes. And, yes, and you can see that from the 11:46:34
12 circuit schematic itself as well. 11:46:37

13 Q The schematic, or Figure 14 on Page 113 11:46:41
14 of your declaration, showed a diode in the blue 11:46:49
15 box. Correct? 11:46:54

16 A Yes, there's a diode in the blue box on 11:46:59
17 Page 113. 11:47:02

18 Q And into that diode there is a Current 11:47:04
19 Ibias, Current LO, and Current RF. Correct? 11:47:11

20 A Yes, those are three current source on -- 11:47:16
21 current sources, yes, on the left of the figure. 11:47:21

22 Q And all three of those current sources 11:47:23

1	mix?	11:47:25
2	A Oh, well. The intention of the circuit	11:47:32
3	is for the IRF and the ILO to mix. And Ibias is	11:47:36
4	not really a -- sorry, a signal or a local	11:47:47
5	oscillator. It's just a DC value that makes	11:47:50
6	the -- puts the diode in perhaps a good region	11:47:57
7	for, you know, like best performance as a mixer.	11:48:02
8	So, you know, I -- some -- some portion	11:48:07
9	of Ibias probably appears at the output, but it's	11:48:10
10	kind of not a normal consideration. And if you	11:48:13
11	look at -- actually, if you look at the simulation	11:48:16
12	results, I believe it's set to zero.	11:48:18
13	Q The diode in Estabrook has two leads.	11:48:21
14	Correct?	11:48:40
15	A Yes. So that if you look at the	11:48:43
16	schematic, you know, from Figure 4, there's a lead	11:48:45
17	on the left and a lead on the right.	11:48:48
18	Q And the -- strike that.	11:48:51
19	Estabrook's diode provides a time-varying	11:49:11
20	impedance. Correct?	11:49:16
21	A Oh, well, so the diode in this case is	11:49:21
22	acting like a switch. And, you know, you can look	11:49:27

1 at a switch as a time-varying impedance. So 11:49:30
2 that's a really interesting way of expressing it. 11:49:37
3 And you could certainly look at it from that 11:49:43
4 perspective. 11:49:45

5 You could just also simply look at it as 11:49:46
6 a switch that's opening and closing. 11:49:49

7 Q The opening and closing of the diode is 11:49:52
8 contingent on the LO and the RF signal. Correct? 11:49:58

9 A Well, the -- you know, the LO is much 11:50:10
10 larger than the RF. And so the LO is kind of 11:50:16
11 mostly determining the timing of the opening and 11:50:22
12 the closing of the switch. 11:50:28

13 The RF does have a small but very 11:50:30
14 significant impact on that as well, so they -- 11:50:34
15 that's the -- they're relative. You know, they 11:50:38
16 both impact it. The LO has a -- perhaps a larger 11:50:41
17 impact. 11:50:44

18 Q The mixing of the LO and RF happen at the 11:50:47
19 source of the diode. 11:50:50

20 Is that correct? 11:50:54

21 A Could you -- I'm not quite sure what 11:51:00
22 that -- I'm not quite sure what "the source of the 11:51:03

1 diode" is referring to. 11:51:05

2 The mixing occurs within the diode due to 11:51:08

3 the switching action of the diode or the nonlinear 11:51:15

4 action of the diode. But the mixing occurs within 11:51:19

5 the diode. 11:51:22

6 Q So the mixing of the LO and the RF 11:51:26

7 happens at the diode. 11:51:37

8 Is that correct? 11:51:39

9 A Well, I think I would say that it happens 11:51:41

10 within the diode. In other words, you know, as -- 11:51:45

11 it happens within the diode because of the 11:51:51

12 switching or not -- and/or nonlinear action of the 11:51:54

13 diode. 11:51:57

14 Q The output of the diode is a combination 11:51:59

15 of the LO and RF signals. Correct? 11:52:02

16 A Well, the output of the circuit, which 11:52:08

17 perhaps is what you're referring to as the output 11:52:11

18 of the diode -- anyway, it's the far right of the 11:52:13

19 schematic there, is a -- certainly a combination 11:52:18

20 of the LO and the RF signals. That they're 11:52:20

21 combining is what's creating the output. They're 11:52:26

22 combining within the diode. 11:52:29

1	Q	Because the LO is much larger than the RF	11:52:30
2		signal, the signal at the output of the diode	11:52:51
3		largely comes from the LO.	11:53:00
4		Would that be accurate?	11:53:03
5	MR. DAY:	Object to form.	11:53:05
6	A	Well, I'm not sure if I would	11:53:10
7		characterize it as the output of the circuit	11:53:14
8		largely comes from the LO, the output of the	11:53:17
9		circuit. And maybe let me go to -- I'm just	11:53:21
10		trying to think of a good illustration of this	11:53:27
11		from my -- from my declaration. And if you can	11:53:29
12		give me a second, I'll pull up something that I	11:53:35
13		think will help to clarify.	11:53:37
14		Okay. So, yeah, if you go to my	11:53:51
15		declaration and you look at Declaration Page 138,	11:53:53
16		Paragraph 260, it shows the output of the mixer.	11:54:01
17		So, and it shows kind of two things: It	11:54:08
18		shows the long, slow variation of the output,	11:54:14
19		which is kind of like, you know, one -- maybe one	11:54:24
20		period of sine wave, and that is the desired IF.	11:54:27
21		And that kind of comes from the -- from the RF	11:54:32
22		input. If the RF input weren't there, that sine	11:54:36

1	wave wouldn't be there.	11:54:41
2	And then you see these tiny little	11:54:43
3	sawtooth waveforms. And those are coming from the	11:54:47
4	local oscillator. And so, you know, you can see	11:54:51
5	that the output is kind of the sum of these two,	11:54:55
6	and the LO is certainly very important because of	11:55:00
7	these sawtooth, you know, things. But the RF is	11:55:05
8	also very important, too.	11:55:09
9	And, you know, is the LO bigger than the	11:55:11
10	RF? It's kind of hard to say, really. They --	11:55:13
11	there is some relative contribution of both of	11:55:17
12	them. But I -- anyway, I think that figure is a	11:55:19
13	very nice illustration of the relative	11:55:23
14	contributions of the LO and the RF.	11:55:25
15	Q The claims, or Claim 1 and 3 -- strike	11:55:28
16	that.	11:55:37
17	Claims 1 and 11 of the '686 patent	11:55:37
18	require a switch configured to operate according	11:55:42
19	to an energy transfer signal and to sub-sample and	11:55:45
20	transfer energy from a first electromagnetic	11:55:48
21	signal.	11:55:53
22	So the switch, as we talk about in the	11:55:55

1 claims, is sub-sampling and transferring energy 11:55:58

2 from a first electromagnetic signal. 11:56:01

3 Here you say that the LO is the energy 11:56:06

4 transfer signal and the RF is the first 11:56:13

5 electromagnetic signal as recited in the claim. 11:56:19

6 Correct? 11:56:22

7 A I think so. Let me just pull up the 11:56:24

8 claim language again, just to make sure we ... 11:56:26

9 So, like -- and I just wanted to repeat 11:56:32

10 what you said. A switch configured to operate 11:56:39

11 according to an energy transfer signal and to 11:56:43

12 sub-sample and transfer energy from a first 11:56:47

13 electromagnetic signal. 11:56:50

14 So to me, like, the energy transfer 11:56:50

15 signal is, you know, a signal that says, okay, 11:56:53

16 time to transfer the energy, so that's the local 11:56:56

17 oscillator in any traditional mixer. And then -- 11:56:59

18 and then to transfer energy from a first 11:57:05

19 electromagnetic signal, so I would consider that 11:57:08

20 to be, this first electromagnetic signal would be 11:57:10

21 the RF signal in a classical -- classical mixer. 11:57:13

22 Q The RF and LO signals of Estabrook are 11:57:20

1	mixing together. Correct?	11:57:28
2	MR. DAY: Object to form.	11:57:32
3	Q To effectuate down-conversion? Strike	11:57:33
4	that. Let me ask that again.	11:57:37
5	A Okay. Yeah.	11:57:38
6	Q The RF and LO signals of Estabrook mix	11:57:39
7	together at the diode to effectuate	11:57:53
8	down-conversion. Correct?	11:57:57
9	A Well, the RF and LO mix together within	11:58:02
10	the diode to, you know, affect the	11:58:12
11	down-conversion. And, you know, how that mixing	11:58:21
12	occurs, you know, I think actually the claim	11:58:23
13	language, you know, describes very nicely. You	11:58:27
14	know, the LO, you know, turns the switch on and	11:58:32
15	energy flows in, and then -- and then -- and then	11:58:35
16	that's stored on the capacitor. So that's --	11:58:39
17	that's, you know, how a diode mixer works. It,	11:58:43
18	you know, turns on and flows energy into the --	11:58:47
19	into the output from the -- from the RF circuit.	11:58:50
20	Q Why -- strike that.	11:59:01
21	Could you say that the LO signal is	11:59:10
22	actually being sampled by the RF signal in	11:59:19

1	Estabrook?	11:59:22
2	MR. DAY: Object to form.	11:59:23
3	A Could I say that the LO signal is being	11:59:25
4	sampled by the RF signal?	11:59:27
5	Q In -- strike that.	11:59:31
6	A Yeah.	11:59:35
7	Q Under how you're interpreting	11:59:35
8	sub-sampling sampling, could you say that the RF	11:59:38
9	signal is actually the energy transfer signal that	11:59:44
10	is used to sub-sample the LO signal?	11:59:54
11	MR. DAY: Object to form.	11:59:58
12	A Yeah, so I think that you're suggesting	12:00:00
13	could you reverse the RF and LO. And so the	12:00:04
14	reason that you can't do that is because of the	12:00:13
15	relative sizes of the two sources. So the ILO	12:00:16
16	is -- is really big, and it's used to turn the	12:00:23
17	diode on and off. And so the ILO sets the sample	12:00:29
18	rate of the -- of the system. And the IRF, by	12:00:36
19	contrast, is very, very small and kind of just	12:00:42
20	flows -- flows through under, you know, control of	12:00:49
21	the ILO when the ILO turns the diode on.	12:00:53
22	So, you know, they -- ILO and IRF look	12:00:57

1 interchangeably here in Figure 14, but their
2 relative magnitudes make the ILO the -- you know,
3 the control, if you will, and the IRF being the --
4 like the first electromagnetic signal.

5 Q Because the LO is relative -- or the
6 magnitude is much greater than RF, the output of
7 the diode is more so the LO, coming from the LO
8 than the RF signal?

9 MR. DAY: Object to form.

10 A Well, you know, the ILO is much bigger,
11 for sure. And I think in the Estabrook, you know,
12 it's like ten times bigger. So more of the LO
13 goes to the output than -- than the RF does.

14 Now, the relative -- we know it's bigger,
15 but we don't quite know how much bigger it is.
16 And, actually, I think that, you know, once again
17 if you go back to that Figure 14 from my -- sorry,
18 Figure 16A from Estabrook, it kind of gives a good
19 example of this.

20 Like, you can kind of see that, you know,
21 on an individual basis. You've got this sawtooth.
22 And then the way that the IF signal is created is

1 that the sawtooth just changes a little bit every 12:02:42
2 time. So more -- you know, on any kind of, like, 12:02:44
3 individual little time frame, like the interval of 12:02:51
4 an LO period, more of the LO reaches -- or the LO 12:02:55
5 signal reaches the output than the -- than the -- 12:02:57
6 than the RF does. 12:03:01

7 But without the RF there would be no -- 12:03:03
8 you know, that sawtooth is not the desired output. 12:03:06
9 The sine wave is the desired output. So although 12:03:09
10 the relative magnitudes of the LO and the RF are 12:03:13
11 small, the LO -- I mean, the LO is bigger. You 12:03:16
12 know, the RF is actually the key thing that's 12:03:20
13 determining the desired output. 12:03:22

14 So I'm just -- that's just a longer 12:03:24
15 explanation of why the LO is larger than the RF 12:03:28
16 and they're relative -- you know, in their 12:03:35
17 relative contributions to the output. 12:03:38

18 THE WITNESS: Now, I hate to raise my 12:03:40
19 hand here. Do you think we could take a lunch 12:03:42
20 break? 12:03:44

21 MS. MANDIR: Yeah. That's fine with me. 12:03:46

22 THE WITNESS: Yeah. Thank you. 12:03:47

1	MR. DAY: Okay.	12:03:49
2	THE WITNESS: Yeah. Thank you. Thank	12:03:51
3	you very much.	12:03:53
4	VIDEO SPECIALIST: Okay. We are going	12:03:54
5	off the record. The time is 12:03.	12:03:56
6	(A recess was taken.)	12:04:00
7	VIDEO SPECIALIST: We are now back on the	12:48:59
8	record. The time is now 12:49.	12:49:04
9	You may proceed.	12:49:07
10	BY MS. MANDIR:	12:49:08
11	Q Dr. Larson, did you discuss the substance	12:49:09
12	of your testimony with anyone during the break?	12:49:11
13	(Discussion off the record; technical	12:49:27
14	difficulty.)	12:49:27
15	A No, not at all. I didn't discuss it at	12:49:29
16	all. Sorry.	12:49:31
17	Q Right before the break we were talking	12:49:33
18	about the Estabrook references. Correct?	12:49:35
19	A Yes, correct.	12:49:41
20	Q Let's go back to your declaration, and	12:49:41
21	specifically Figure 14 of Estabrook.	12:49:49
22	A Okay.	12:50:35

1	Q	So Figure 14 of Estabrook's thesis is	12:50:40
2		provided on PDF Page 126 of your declaration. So	12:50:49
3		when you get there, let me know.	12:50:57
4	A	I will.	12:50:59
5		Okay, I'm there.	12:51:09
6	MR. DAY:	And just for clarity, are you	12:51:13
7		referring to Page 126 of the PDF or as numbered in	12:51:14
8		the declaration?	12:51:17
9	MS. MANDIR:	The PDF page, not the --	12:51:19
10	THE WITNESS:	Yeah. And that's Page 113	12:51:22
11		of the declaration.	12:51:24
12	Q	Sorry, did you say you were there?	12:51:30
13	A	Yes, I'm there. Thank you.	12:51:32
14	Q	So on Page 113 of the actual declaration	12:51:34
15		there is a figure above Figure 114 which is Figure	12:51:40
16		4, which shows a schematic of the direct	12:51:45
17		conversion receiver as taught by Estabrook.	12:51:49
18		Correct?	12:51:54
19	A	Yes, that was Figure 4, the top portion	12:51:59
20		of Figure 4 of Estabrook.	12:52:01
21	Q	And Figure 4 of Estabrook shows a mixer	12:52:10
22		circuit, which you've highlighted in yellow.	12:52:16

1	Correct?	12:52:18
2	A Yes, that's on the left-hand side there,	12:52:22
3	highlighted in yellow.	12:52:24
4	Q And the highlighted yellow mixer of	12:52:25
5	Figure 4 correlates to the circuit of Figure 14.	12:52:28
6	Correct?	12:52:37
7	A Yeah, I think that's -- I mean, it's --	12:52:41
8	you know, Figure -- yes, they correlate with each	12:52:50
9	other. I mean, the exact implementation details	12:52:54
10	might be a little different, but that they're	12:52:57
11	basically -- Figure 14 is meant to be -- represent	12:53:02
12	the mixer of Figure 4.	12:53:04
13	Q The mixer circuit of Figure 14 of	12:53:06
14	Estabrook, as we stated earlier, is a	12:53:22
15	single-balanced mixer. Correct?	12:53:28
16	A Yes, Dr. Estabrook referred to it as a	12:53:29
17	singly balanced mixer.	12:53:33
18	Q And how does a single-balanced mixer	12:53:36
19	differ from a double-balanced mixer in terms of	12:53:40
20	performance characteristics?	12:53:44
21	MR. DAY: Object to form.	12:53:47
22	A Well, Dr. Estabrook actually has a doubly	12:53:49

1 balanced -- or balanced, I should say, version of 12:53:55
2 this mixer in her thesis. And I can't remember, 12:53:58
3 you know, exactly where it is. I could look it 12:54:04
4 up. 12:54:06

5 But the balanced version of this circuit 12:54:07
6 would have two diodes in parallel. And, you know, 12:54:11
7 one would point the other. They would be in 12:54:19
8 parallel with each other, and the second diode 12:54:20
9 would be connected in what we call anti-parallel 12:54:22
10 configuration, or sort of pointing in the other 12:54:29
11 direction. 12:54:31

12 And, you know, the basic idea is there is 12:54:31
13 that the -- it reduces the LO -- the balanced 12:54:36
14 configuration reduces the LO feed-through at the 12:54:44
15 output, and it allows the LO current to go back 12:54:47
16 out from the -- from the output, in addition to 12:54:49
17 going in as it did previously. So that would be 12:54:54
18 the difference. 12:54:57

19 And there are, you know, pros and cons, 12:54:59
20 advantages and disadvantages, to a balanced versus 12:55:01
21 a single-ended version, which I believe 12:55:04
22 Dr. Estabrook discusses in her thesis. 12:55:07

1 Q Would a POSITA at the time of these
2 references typically prefer a double-balanced
3 mixer over a single-balanced mixer in a
4 transceiver application?

12:55:09

12:55:19

12:55:27

12:55:31

5 MR. DAY: Object to form.

12:55:32

6 A Yeah, that's a -- that's a great
7 question. Well, you know, like I said, there are
8 pros and cons to each implementation. Typically a
9 singly -- a single-balanced mixer, or just a, you
10 know, a single mixer like 14A, like 14 in
11 Estabrook, has lower noise, so that's a -- that's
12 a good thing. It -- but it might have more LO
13 feed-through, which we see in the -- in the
14 simulation results.

12:55:34

12:55:36

12:55:39

12:55:45

12:55:50

12:55:55

12:55:58

12:56:05

12:56:07

15 A balanced mixer would, like with two
16 diodes, would probably have lower LO feed-through
17 but require more LO power and might have a higher
18 noise figure.

12:56:09

12:56:13

12:56:17

12:56:21

19 So there are -- there are pros and cons.
20 I would have to say, you know, all noise and power
21 performance being equal, a balanced mixer would be
22 preferred because of the LO leakage issue that I

12:56:21

12:56:25

12:56:31

12:56:35

1	mentioned earlier.	12:56:37
2	Q Are you aware of any commercial	12:56:41
3	transceiver architectures where a single-balanced	12:56:45
4	mixer is used?	12:56:49
5	A It's a good question.	12:57:14
6	At the time there might have been some.	12:57:16
7	But today I think that most commercial systems use	12:57:19
8	balanced or -- use balanced mixers of various	12:57:25
9	types. And I am not aware of any commercial	12:57:29
10	systems today that don't use a balanced mixer.	12:57:32
11	Q A single-balanced mixer has an inferior	12:57:34
12	LO isolation and distortion performance compared	12:57:41
13	to a double-balanced mixer, doesn't it?	12:57:46
14	MR. DAY: Object to form.	12:57:50
15	A So a double-balanced mixer -- so a singly	12:57:53
16	balanced mixer, and unbalanced mixer, is -- so a	12:57:56
17	doubly balanced mixer is balanced at both ports,	12:58:03
18	RF and LO. So the performance, like, from a	12:58:06
19	feed-through perspective, I think the way to think	12:58:12
20	about it is any time you have a balance at that	12:58:15
21	port, it minimizes the feed-through to the output.	12:58:18
22	So that's the good thing.	12:58:23

1	It doesn't necessarily improve distortion	12:58:26
2	to be balanced, nor does it necessarily improve	12:58:29
3	noise figure. But it does improve this leakage of	12:58:33
4	the LO and the RF to the output. And so the	12:58:37
5	performance you have to kind of weigh, you know,	12:58:42
6	leakage, noise, gain, distortion, when you make	12:58:45
7	that determination. But having a -- having a	12:58:51
8	balanced mixer has generally proved to be the most	12:58:55
9	popular approach these days because -- because the	12:58:58
10	noise in particular degradation is very, very	12:59:03
11	small, if not completely negligible at today's --	12:59:05
12	at this stage of our technological evolution.	12:59:10
13	Q Do single-balanced mixers have a higher	12:59:12
14	second-order distortion compared to	12:59:32
15	double-balanced mixers?	12:59:34
16	A Sorry, I'm just -- I want to check one	12:59:43
17	thing in my report.	12:59:47
18	Yeah, generally, so any time you have a	13:00:25
19	balance, there is a positive signal and a negative	13:00:27
20	signal. And second-order distortion when a	13:00:29
21	positive signal is squared, it's positive, and	13:00:36
22	when a negative signal is squared, it's positive.	13:00:39

1	So second order -- a balanced configuration	13:00:41
2	intrinsically cancels out second-order distortion.	13:00:45
3	So there's -- there's kind of a an	13:00:49
4	intrinsic advantage using a balanced configuration	13:00:51
5	when you are thinking about second-order	13:00:55
6	distortion.	13:00:57
7	Now, that cancellation is never perfect.	13:00:58
8	So you don't get perfect cancellation, but you	13:01:01
9	almost always get a significant performance	13:01:03
10	improvement.	13:01:09
11	Q If you look at Figure 14 of Estabrook,	13:01:10
12	you see that at the right of the RL there is a	13:01:24
13	label that says VOUT. Correct?	13:01:32
14	A Correct.	13:01:36
15	Q Does that indicate the output of the	13:01:38
16	mixer is a voltage?	13:01:42
17	A Yes, the -- the output of this mixer is	13:01:47
18	the voltage across the capacitor, you know, CLD.	13:01:51
19	And that's where Dr. Estabrook was measuring the	13:01:55
20	output.	13:01:57
21	Q And if you look at Figure 4, which is	13:01:59
22	right above 14 in your declaration, after the	13:02:05

1	mixer symbol, there is a triangle. Correct? And	13:02:12
2	it's labeled 3.	13:02:17
3	Do you see that?	13:02:20
4	A Yes, I see that. It's at the upper left.	13:02:21
5	That is a triangle labeled 3.	13:02:24
6	Q And is that triangle, does that triangle	13:02:26
7	represent a amplifier?	13:02:30
8	A I believe it does, yes. That's the --	13:02:34
9	that's the classic symbol for an amplifier that	13:02:36
10	any -- anybody would understand.	13:02:39
11	Q A POSITA would also understand that an	13:02:45
12	amplifier exhibits a high input impedance.	13:02:48
13	Correct?	13:02:51
14	MR. DAY: Object to form.	13:02:54
15	A Yeah, well, that's a -- that's a good	13:02:55
16	question. So, you know, the input impedance of an	13:02:59
17	amplifier depends on its, you know, like, its use.	13:03:05
18	And the input impedance of an amplifier is not	13:03:11
19	always high. And actually at microwave	13:03:13
20	frequencies, more particularly it's 50 ohms, which	13:03:19
21	could be considered to be a rather low frequency.	13:03:23
22	So, now, this is a kind of design for	13:03:26

1	like, an IF, a low IF frequency, you know, I think	13:03:28
2	9 megahertz was chosen here. So it might be	13:03:33
3	higher than 50 ohms. And the only reason that I	13:03:40
4	kind of hesitate a bit is that, you know, looking	13:03:43
5	into the mixer, so the input to the mixer is	13:03:47
6	coming from this power splitter, which is labeled	13:03:49
7	on the far left of that drawing, Figure 4. And	13:03:54
8	that is a very high-frequency signal, that's, you	13:04:01
9	know, roughly a gigahertz.	13:04:04
10	So the input to the mixer should be 50	13:04:06
11	ohms. And the load impedance that's presented at	13:04:08
12	the output of the mixer is reflected back to the	13:04:12
13	input. So the load impedance at 3 is probably	13:04:16
14	chosen to be something that will allow the mixer	13:04:21
15	itself to have roughly a 50-ohm input impedance.	13:04:25
16	And it's not clear what the correct number is	13:04:32
17	there. But that value of the input impedance	13:04:35
18	looking to that amplifier is probably chosen to	13:04:38
19	help impedance match the mixer to 50 ohms. But it	13:04:41
20	could be more -- but the input impedance could be	13:04:49
21	more than 50 ohms; I just don't know how much more	13:04:52
22	than 50 ohms.	13:04:55

1	Q	So there is no value in Estabrook to let	13:04:56
2		you know whether -- or --	13:05:03
3	A	There's one --	13:05:05
4	Q	There's no value in Estabrook that	13:05:06
5		indicates whether that impedance is high or low?	13:05:10
6	A	Well, I think I would turn -- to answer	13:05:14
7		your question, I think I would turn to the SPICE	13:05:19
8		deck, which is in my report. So let me just take	13:05:22
9		a quick look in my report. I'm looking for the	13:05:24
10		SPICE deck.	13:05:32
11		So RL is 1,000 ohms in the simulation of	13:05:47
12		Estabrook. So RL is 1,000 ohms.	13:05:53
13	Q	Is 1,000 ohms a high-impedance load here?	13:06:00
14	MR. DAY:	Object to form.	13:06:03
15	A	Well, RL is -- it's higher than 50 ohms.	13:06:05
16		But, you know, it's -- is it a high impedance?	13:06:12
17		I'd say it's a medium impedance. It's higher than	13:06:16
18		50 ohms.	13:06:21
19	Q	The LO signal of Estabrook is a	13:06:30
20		sinusoidal signal. Correct?	13:06:36
21	A	Yes. And once again, if you go to the	13:06:40
22		SPICE deck on Page 131 of my report, the local	13:06:44

1	oscillator is clearly labeled as sine wave.	13:06:49
2	Q And the combination of the bias, the LO	13:06:51
3	and the RF couples to the diode and is seen as an	13:07:09
4	output. Correct?	13:07:19
5	A Well, the ILO and the IRF are kind of	13:07:20
6	added together, and then they go into the diode.	13:07:23
7	And then -- then they come out of the diode.	13:07:28
8	Q And so the current coming out of the	13:07:31
9	diode is a combination of the LO and RF. Correct?	13:07:38
10	A Yeah, I would say that ILO and IRF are	13:07:48
11	combined at the input and then, you know, flow to	13:07:52
12	the output.	13:07:54
13	Q And a diode can only conduct current in	13:07:55
14	one direction. Correct?	13:07:59
15	A Yes, a diode only conducts current in a	13:08:03
16	forward direction when it's turned on, when	13:08:05
17	that -- when that switch is on, just in the	13:08:10
18	forward direction. And on the -- on the drawing	13:08:12
19	here, that would be from -- from left to right.	13:08:14
20	Q How does the component RS of Figure 14 of	13:08:24
21	Estabrook relate or function in the system?	13:09:02
22	A Well, every, you know, microwave source,	13:09:17

1 every source of RF power, has an intrinsic
2 impedance. And it's just sort of like when you
3 think back to Avitabile, which we spoke about
4 earlier today, there was a -- an RF voltage source
5 with a resistor in series with it.

6 And that series resistance is kind of
7 intrinsic to this -- to the supply of power or
8 energy. So we often think about that as a -- as
9 that voltage -- as that energy source or power
10 source as a voltage in series with a resistor.
11 But an equivalent way of thinking about it is a
12 current source in parallel with a resistor, the
13 same resistor.

14 So the function of R_S in here is to model
15 the intrinsic resistance of the power sources, the
16 RF power sources, ILO and IRF. And, you know,
17 it's usually just modeled as a simple resistor in
18 parallel with the current source.

19 Q And when the diode switch -- strike that.

20 When the diode is closed, it passes
21 current through the diode from the combined signal
22 ILO and IRF. Correct?

1 A Yes. So when the -- when the -- you said 13:11:00
2 the -- when the switch is closed, that's a good 13:11:03
3 way of saying it. Another way of saying it is 13:11:06
4 when the diode is on, and when it's acting as a 13:11:09
5 switch, so the switch is closed, current flows 13:11:12
6 from ILO and IRF to the load, to the output, CLD 13:11:14
7 and VOUT. 13:11:22

8 Q How did you determine that Estabrook 13:11:23
9 transfers nonnegligible amounts of energy from the 13:11:40
10 RF input signal through the diode? 13:11:49

11 A Well, you know, first of all, you know, 13:11:56
12 as I pointed out earlier, the simulation results I 13:12:01
13 think show this very clearly. And this would be 13:12:06
14 on Page 138 of the -- of my report, Figure 16A of 13:12:13
15 Estabrook, which is I guess Page 71 of the thesis. 13:12:23

16 And, you know, so you asked how do I know 13:12:27
17 that a nonnegligible amount of RF energy is 13:12:30
18 appearing at the output. And so the long, slow 13:12:34
19 sine wave that is shown in -- in this figure is a 13:12:40
20 measure of the energy that is transferred from the 13:12:49
21 RF to the output. 13:12:51

22 If there were no RF energy transmitted 13:12:53

1 from the RF to the output, that would just be a 13:12:57
2 straight little sawtooth line. There would be no 13:13:01
3 long sine wave variation. But because there's a 13:13:04
4 very large and predictable variation, you can see 13:13:07
5 that -- you can see the effect of this energy 13:13:11
6 transfer. And it's clearly nonnegligible. This 13:13:14
7 is exactly what the mixer is supposed to do. And 13:13:19
8 if there were no energy transfer, it wouldn't be 13:13:22
9 doing this. 13:13:24

10 So this is how I determined that the 13:13:24
11 energy transfer from RF to the output was 13:13:27
12 nonnegligible. It's clearly distinguishable from 13:13:32
13 noise. 13:13:35

14 Q I'm sorry, can we -- let's go through 13:13:35
15 what you just said. 13:13:41

16 So we're looking at Estabrook Figure 16, 13:13:43
17 which is on PDF Page 151 of your report. Correct? 13:13:48

18 A Yeah. Yes, that's right, PDF Page 151, 13:14:06
19 report Page 138. It's at the bottom of that page. 13:14:10

20 Q And the -- strike that. 13:14:17

21 Figure 16A of Estabrook illustrates the 13:14:22
22 capacitor -- strike that. 13:14:28

1	Figure 16A of Estabrook illustrates the	13:14:30
2	VOUT of the Estabrook mixer in 14. Correct?	13:14:35
3	A Yes, this I believe is the simulation	13:14:41
4	result from -- from the circuit above, which is	13:14:43
5	Figure 14A from Estabrook.	13:14:47
6	Q So I'm asking you specifically the --	13:14:49
7	strike that.	13:14:59
8	We talked about previously that an energy	13:15:06
9	transfer -- about an energy transfer signal.	13:15:10
10	Correct?	13:15:12
11	A Yeah, we've discussed energy transfer	13:15:13
12	many times today, yes.	13:15:15
13	Q And specifically the term "energy	13:15:16
14	transfer signal." Correct?	13:15:19
15	A Yes. Yes. And I guess just to be clear,	13:15:21
16	the term "energy transfer signal" is used in the	13:15:27
17	claims, Claim 1 and 11, I think.	13:15:31
18	Q Correct.	13:15:33
19	And as recited in the claims, a switch is	13:15:38
20	configured to operate according to an energy	13:15:42
21	transfer signal. Correct?	13:15:45
22	A Yeah, let me just pull up the claim.	13:15:50

1	Yeah, like in Claim 11 it says, The	13:15:54
2	switch is configured to operate according to an	13:15:57
3	energy transfer signal. Yeah.	13:15:59
4	Q And -- strike that.	13:16:04
5	To finish off, or to recite the full	13:16:07
6	limitation in Claim 11, it's "A switch configured	13:16:10
7	to separate according to an energy transfer	13:16:13
8	signal, and to sub-sample and transfer energy from	13:16:15
9	a first electromagnetic signal."	13:16:18
10	Correct?	13:16:19
11	A Yes. Yes, that's Claim 11. Yes. I	13:16:21
12	agree.	13:16:24
13	Q You said previously that an energy	13:16:24
14	transfer signal -- you interpreted an energy	13:16:27
15	transfer signal as being a signal that can	13:16:31
16	transfer energy from the source to the capacitor.	13:16:33
17	Correct?	13:16:38
18	A Well, yeah, the energy transfer signal	13:16:39
19	controls the transfer of energy from a first	13:16:44
20	electromagnetic signal, you know, to a storage	13:16:48
21	module. I'm just reading the claims here.	13:16:51
22	Q And so with that, how, using Figure 16	13:16:55

1 which is the output rather than the transfer of
2 energy through the switch, did you determine that
3 Estabrook teaches an energy transfer signal?

13:17:04

13:17:08

13:17:13

4 MR. DAY: Object to form.

13:17:17

5 A Well, so, you know, let's look here at
6 Figure 16A.

13:17:20

13:17:26

7 So clearly energy is being transmitted,
8 transferred I should say, from the LO to the -- to
9 the output. So, you know, once again let me just
10 back up for a second.

13:17:28

13:17:33

13:17:37

13:17:40

11 The only sources of energy in this system
12 are ILO and IRF. Ibias is set to zero. So there
13 are only two sources of energy, ILO and IRF. So
14 any energy that appears at the output comes from
15 those two sources, ILO or IRF.

13:17:41

13:17:44

13:17:50

13:17:54

13:17:56

16 Now, when you look at 16A, you clearly
17 see that energy is being transferred from the LO
18 because you get this sawtooth that's at the LO
19 frequency. And that is a result of the variety of
20 things we talked about, about the -- earlier in
21 the day, the feed-through of the diode and the
22 discharging through RL.

13:17:59

13:18:03

13:18:07

13:18:11

13:18:17

13:18:23

13:18:25

1 You also see in Figure 16A a second 13:18:27
2 signal which is much slower, and that is the -- it 13:18:30
3 takes -- it's about one period of a sine wave, in 13:18:34
4 that entire simulation. And that is the IF signal 13:18:38
5 coming out. And that represents the transfer of 13:18:40
6 energy from the -- from the RF to the output. And 13:18:43
7 that -- and it is at a frequency that's the 13:18:46
8 difference between the LO and the RF. 13:18:49
9 So, and you know that that's coming from 13:18:51
10 the RF. Because if the RF didn't exist, if that 13:18:54
11 RF energy was zero, that signal wouldn't be there. 13:18:58
12 That long, slow signal wouldn't be there. So the 13:19:01
13 RF energy is being transferred to the -- to the 13:19:04
14 output to create that long, slow, you know, 13:19:07
15 desired output. 13:19:11
16 So we have two sources of energy, ILO and 13:19:13
17 IRF. They both go to the output, and contribute 13:19:16
18 to the output in different ways, which we've seen. 13:19:23
19 So I guess that's how I know that the IRF is 13:19:27
20 transmitting energy to the output. 13:19:30
21 Q Specifically how do you know it's 13:19:32
22 transferring nonnegligible amount of energy? 13:19:44

1 A Well, if it was a negligible amount of 13:19:49
2 negligible it would look like noise, or look like 13:19:51
3 zero. But this doesn't look like noise at all. 13:19:53
4 It's periodic, and its period corresponds to the 13:19:56
5 period of the local oscillator and the period of 13:19:59
6 the -- of the IF. And so it's just -- it's 13:20:02
7 obviously not noise, and therefore it's not 13:20:07
8 negligible. 13:20:12

9 Q Is there noise in the simulation of 13:20:12
10 Estabrook? 13:20:17

11 A No. Estabrook doesn't do a noise 13:20:20
12 simulation. It's -- it's -- noise is not included 13:20:22
13 in this. But, you know, values of noise are 13:20:26
14 extremely well known. And anyone with ordinary 13:20:33
15 skill in the art would know that, you know, noise 13:20:35
16 levels are typically in the you know, microvolt, 13:20:37
17 hundreds of microvolt region. And the signals 13:20:43
18 we're talking about here are like half a volt, 13:20:46
19 they are many orders of magnitude larger than the 13:20:48
20 noise levels. So it's very clear that this is at 13:20:51
21 a signal level that is way, way above a noise 13:20:55
22 level. Anyone with an ordinary skill in the art 13:20:59

1	would understand that.	13:21:06
2	Q So the nonnegligible amounts of energy	13:21:12
3	comes up twice in the claims, once relative to the	13:21:14
4	energy transfer signal, and once relative to the	13:21:17
5	construction of storage module. Correct?	13:21:23
6	MR. DAY: Object to form.	13:21:24
7	A Could you -- once again, could you, like,	13:21:26
8	refer me back to a specific claim? I just want to	13:21:27
9	read the claim that you're referring to.	13:21:29
10	Q Sure. Claim 11.	13:21:30
11	Well, Claim 11 recites a storage module.	13:21:32
12	Correct?	13:21:34
13	A Oh, I see it. "A storage module coupled	13:21:50
14	to said switch and configured to store said	13:21:52
15	transferred energy." Yes. Yes, I see that.	13:21:56
16	Q And the construction of storage module	13:21:58
17	that you identified and used is a module that	13:22:01
18	stores nonnegligible amounts of energy from the	13:22:06
19	input VIN signal. Correct?	13:22:10
20	A Yes, I mean, I interpreted -- and I think	13:22:12
21	we talked about this -- I interpreted that storage	13:22:14
22	module to mean like the capacitor that is	13:22:17

1 connected to the output of the switch. 13:22:20

2 Q So did you not take into consideration 13:22:28

3 when looking at these references that the 13:22:30

4 capacitor also had to store nonnegligible amounts 13:22:35

5 of energy from the input signal? 13:22:41

6 MR. DAY: Object to form. 13:22:42

7 A Sorry, could you ask that again? 13:22:44

8 Q When reviewing the references, did you 13:22:46

9 not take into consideration that these capacitors 13:22:49

10 had to store nonnegligible amounts of energy from 13:22:55

11 the input electromagnetic signal? 13:22:58

12 MR. DAY: Object to form. 13:23:01

13 A I'm sorry, once again you're using a 13:23:03

14 double negative and I struggle a little bit 13:23:04

15 wrapping my head around it. 13:23:09

16 Q Strike that question. 13:23:11

17 A You know, I mean, I certainly considered 13:23:14

18 the fact that the capacitor at the output had to 13:23:15

19 store nonnegligible amounts of energy as part of 13:23:21

20 this energy transfer from the first 13:23:24

21 electromagnetic signal. 13:23:28

22 Q And how did you determine that the 13:23:29

1 capacitors were storing nonnegligible amounts of
2 energy, in Estabrook?

3 A Well, you know, once again, if you look
4 at the voltage from Estabrook 16A, you see that
5 the voltage on that capacitor is .5 volts, 1 volt.
6 It's kind of in that area.

7 And Estabrook gives a value for the value
8 of that capacitance. And I think, if I remember
9 correctly, it was 2.8 pF. Yes, it's 2.8 pF.

10 So, you know, half a volt, a volt stored
11 on a 2.8 pF capacitor, is a -- is a quite a high
12 voltage. It's much higher than the background
13 noise voltage, which is like, you know, it's --
14 it's kT over 2, it's an equation. It's like many
15 tens of thousands if not millions of times higher
16 energy than is -- than is background noise. So
17 that's why I believe the capacitor is storing a
18 nonnegligible amount of energy.

19 Q The Estabrook reference -- strike that.

20 How would an RF signal modulated affect
21 the function of the Estabrook reference?

22 A So how would it -- how would a modulated

1 RF signal. How would a modulated RF signal modify
2 the operation of the Estabrook reference.

3 So I'm looking at Figure 14A now from
4 Estabrook. And I would have to say that the -- so
5 if we compare a modulated RF to an unmodulated RF
6 input to this Estabrook circuit, the operation
7 would not change significantly.

8 Any time you have a modulated signal, you
9 have to consider, you know, its bandwidth and its
10 maximum kind of excursion and frequency from the
11 carrier. But it -- that will not affect the basic
12 operation. And I think it would be unchanged if
13 you put a modulated signal through it, essentially
14 unchanged if you put a modulated signal through
15 it.

16 Q Would a circuit designer use multiple
17 single-balanced mixers in a transceiver circuit?

18 MR. DAY: Object to form.

19 A Well, you know, once again, it's a kind
20 of a hypothetical question. And I think that, you
21 know, I would say that multiple single-balanced
22 mixers can be combined to create a balanced or

1 even double-balanced mixer. So that might be one 13:27:55
2 kind of way of using multiple single mixers to 13:28:00
3 create, say, a balanced configuration. 13:28:07

4 You know, there might also be a case 13:28:10
5 where you would have a very wide-band transceiver, 13:28:13
6 like a transceiver that would have to operate over 13:28:17
7 multiple octaves or even decades of frequency 13:28:20
8 range. And you might want to use different mixers 13:28:24
9 depending on which frequency band you were 13:28:27
10 listening to. 13:28:29

11 So there are cases where, yeah, like a 13:28:31
12 single transceiver might use multiple of these 13:28:34
13 mixers, and then you would, like, switch between 13:28:37
14 them or combine their outputs in some other way. 13:28:40

15 So it's a kind of a broad hypothetical, 13:28:43
16 but you can imagine cases where the use of 13:28:45
17 multiple version of these might -- in a single 13:28:49
18 transceiver might be appropriate. 13:28:52

19 Q What design considerations would a 13:28:53
20 circuit designer have to make when putting a 13:29:02
21 receiver and transmitter together into a 13:29:04
22 transceiver? 13:29:07

1	MR. DAY: Object to form.	13:29:09
2	A So, once again, it's kind of a broad, you	13:29:12
3	know, hypothetical question. But generally	13:29:16
4	speaking, you know, receivers are all about, you	13:29:21
5	know, listening for very, very, very tiny signals,	13:29:25
6	and then amplifying them, converting them and	13:29:31
7	amplifying them. And transmitters are about	13:29:34
8	transmitting very, very, very big signals.	13:29:38
9	And the difference between those two	13:29:42
10	regimes, very, very, very big signals and very,	13:29:44
11	very, very small signals, is profound. It's, you	13:29:47
12	know, many, many orders of magnitude, like ten,	13:29:51
13	nine, ten orders of magnitude in some case	13:29:56
14	difference.	13:29:58
15	So, you know, the circuit designs are	13:29:59
16	different between the two types of structures, the	13:30:02
17	types of transistors you use are different.	13:30:06
18	System, you know, applications -- you know, system	13:30:10
19	considerations are different. If you're listening	13:30:13
20	at the same time that you're transmitting, a	13:30:17
21	transmitter can corrupt a receiver in a variety of	13:30:19
22	ways.	13:30:24

1 So there are just like a million 13:30:25
2 different -- million different design 13:30:27
3 considerations when you do a receiver and a 13:30:29
4 transmitter together. 13:30:31

5 Q Are there any disadvantages of using a 13:30:37
6 single-ended mixer in a transceiver circuit versus 13:30:45
7 a balanced mixer? 13:30:49

8 A Well, you know, as I said earlier, there 13:30:54
9 are pros and cons to a single mixer versus a 13:30:56
10 balanced mixer versus a doubly balanced mixer. 13:31:01
11 You know, a single -- and it has to do with, well, 13:31:04
12 noise and linearity and feed-through of the local 13:31:07
13 oscillator signal, feed-through of the RF signal. 13:31:14

14 Generally speaking, everything else being 13:31:17
15 equal, more balance is better. But the problem is 13:31:19
16 that creating balance adds cost that can hurt 13:31:23
17 noise, it can increase complexity. So these are 13:31:27
18 trade-offs that you have to consider when 13:31:32
19 choosing, you know, one versus the other. 13:31:34

20 Generally speaking today in 2025, most 13:31:36
21 commercial mixers are doubly balanced because the 13:31:41
22 penalties for doing so are very small. But that 13:31:43

1	was different, you know, in the earlier times.	13:31:46
2	MS. MANDIR: Let's go off the record	13:32:39
3	maybe five minutes. I might be wrapping up.	13:32:41
4	VIDEO SPECIALIST: We are going off the	13:32:46
5	record. The time is 13:32.	13:32:47
6	(A recess was taken.)	13:32:50
7	VIDEO SPECIALIST: We're now back on the	13:36:24
8	record. The time is 13:36.	13:36:33
9	You may proceed.	13:36:36
10	MS. MANDIR: All right. So no further	13:36:39
11	questions from me, Dr. Larson. I appreciate it.	13:36:41
12	Thank you for your time.	13:36:45
13	THE WITNESS: Thank you. Nice talking to	13:36:46
14	you.	13:36:48
15	MR. DAY: Nothing from me.	13:36:48
16	MS. MANDIR: All right. We can go off	13:36:52
17	the record.	13:36:53
18	VIDEO SPECIALIST: We are going off the	13:36:53
19	record. The time is 13:36. Thank you.	13:36:54
20	(Off the record at 1:36 p.m. EST.)	
21		
22		

ACKNOWLEDGMENT OF DEPONENT

I, LAWRENCE E. LARSON, Ph.D., do hereby
acknowledge that I have read and examined the
foregoing testimony, and the same is a true,
correct and complete transcription of the
testimony given by me, and any corrections appear
on the attached Errata sheet signed by me.

(DATE)

(SIGNATURE)

C E R T I F I C A T E

I, Debra Ann Whitehead, E-Notary Public in and for
the Commonwealth of Virginia, do hereby certify:

That LAWRENCE E. LARSON, Ph.D., the
witness whose deposition is hereinbefore set forth,
was duly sworn by me before the commencement of such
deposition and that such deposition was taken
virtually and is a true record of the testimony
given by such witness.

I further certify that the adverse party,
MEDIATEK, INC., was represented by counsel at the
deposition.

I further certify that the deposition of
LAWRENCE E. LARSON, Ph.D., occurred virtually, on
Wednesday, February 26, 2025, from 9:03 a.m. to 1:36
p.m. EST.

1 I further certify that I am not related to
2 any of the parties to this action by blood or
3 marriage, I am not employed by or an attorney to any
4 of the parties to this action, and that I am in no
5 way interested, financially or otherwise, in the
6 outcome of this matter.

7
8 IN WITNESS WHEREOF, I have hereunto set my
9 hand this 8th day of March, 2025.

10
11 My commission expires:

12 October 31, 2027

13
14 A handwritten signature in cursive script, appearing to read "Lawrence E. Larson".



15 -----
16 E-NOTARY PUBLIC IN AND FOR THE
17 COMMONWEALTH OF VIRGINIA
18
19
20
21
22

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