

# Subharmonic Sampling of Microwave Signal Processing Requirements

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## Introduction

Modern microwave test instruments owe much of their capabilities to powerful microwave signal processing subsystems that employ high speed sampling circuitry. These sampling heads, as they are often called, can be found at the heart of the latest sampling oscilloscopes, frequency counters, time/frequency analyzers and vector network analyzers.<sup>1-3</sup> The sophistication at which these instruments analyze complex microwave signals is a testimony to the power of sampling techniques for use in extracting frequency, phase and vector information.<sup>4</sup>

Outside of the test equipment industry, sampling techniques have been employed by phase lock oscillator and synthesizer manufacturers for many years.<sup>5</sup> The emergence of commercially available sampling phase detectors is an indication of the need for these types of microwave signal processing components. Along with this demand comes the need for design and application information on microwave sampling hardware.

In this paper the theory behind subharmonic sampling is explored and the physics of the sample-and-hold process are examined when applied to microwave frequencies. Through time domain analysis, the criteria for optimum sampling hardware performance is established. Finally, a variety of microwave sub-

harmonic sampling applications are presented.

## Basis of Subharmonic Sampling

Subharmonic sampling as a microwave signal processing technique may be best understood by studying sampling theory. The basic premise of sampling theory states that when a signal  $f(t)$  of bandwidth  $\beta$  (Hz) is sampled at a rate of  $f_c$ , which is greater than or equal to twice the signal bandwidth or  $2\beta$ , no information contained in the original signal is lost. Furthermore, taking the Fourier transform of the sampling function

$$fs(t) = f(t)S(t)$$

where  $S(t)$  is the periodic sampling function of pulse width  $\tau$  and period  $1/f_c$ , the spectrum of the sampled signal may be derived. This results in a summation of individual Fourier transforms each centered at a positive and negative integer multiple of the sampling rate

$$Fs(\omega) = dF(\omega) + d\sum \sin \frac{(n\pi d)}{n\pi d * F} (\omega - n\omega_c)$$

For all  $n = \pm \infty$  except  $n = 0$

If the sampled signal is a baseband signal center at 0, then the reconstructed signal will be centered at 0. The frequencies of the first harmonic replica of the sam-

pled signal are centered at  $0, \pm f_c$ . The succeeding replicas ( $\pm n \times f_c$ ) decrease in amplitude at the rate of  $(\sin n\pi d)/n\pi d$ . This theory is well suited for such applications as digitized voice. For this application the subharmonic sampling of a microwave signal must be considered.

In compliance with the guidelines of the sampling theory, the spectrum that results from a bandlimited microwave signal  $f(t)$  of bandwidth  $\beta$  that is sampled at the rate  $f_c$ , where  $f_c \geq 2\beta$  and is also a subharmonic of  $f(t)$ , or  $n \times f_c = f(t)$  is considered. In this case, the fundamental replicas of the sampled signal is centered at  $f(t)$  with succeeding replicas of this reconstructed signal appearing at  $\pm n \times f_c$ . The FFTs, shown in Figure 1a where  $k = 512$ , show the  $(\sin X)/X$  amplitude response of the sampled spectrum. The expanded FFT of Figure 1a, where  $k = 154$ , shows more clearly how the sampled RF input is reconstructed at the original frequency. The succeeding replicas of the RF input as shown are converted up and down in frequency and separated in frequency by the sampling rate  $F_c$  (Hz).

In this sampling simulation, the RF input was sampled at a subharmonic rate of one-tenth  $f(t)$ . This is evident in the fact that there are indeed 10 replicas of the sampled signal in either upper or lower sideband of  $F(t)$ . Typically, the baseband replica of  $F(t)$  located near DC, in this case

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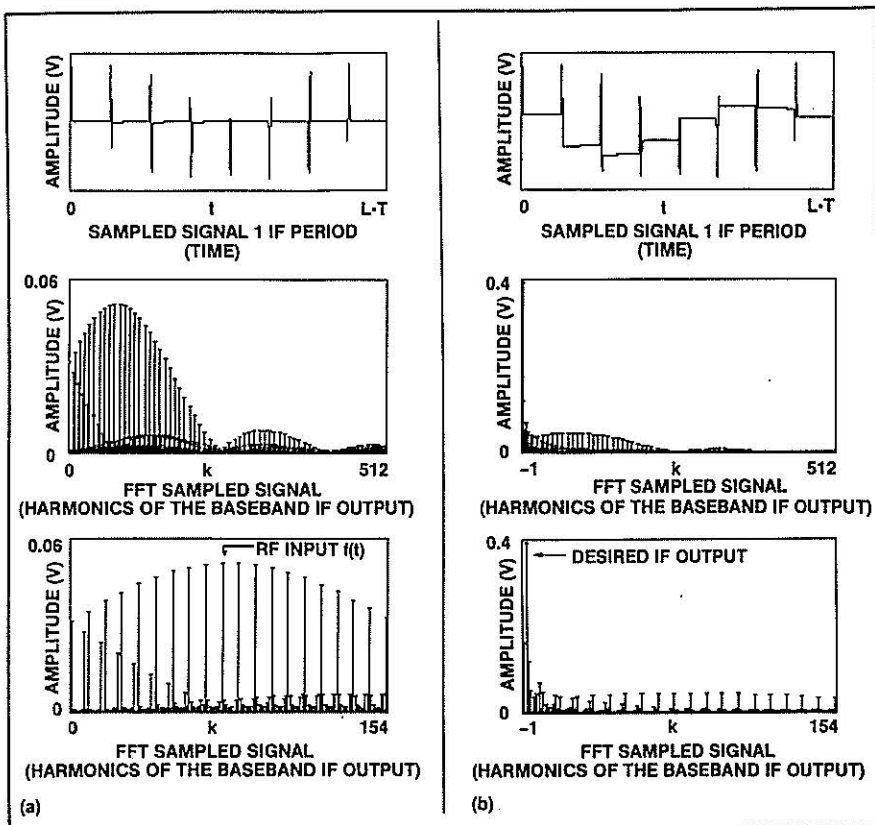


Fig. 1 Time domain analysis of the sampling process; (a)  $f_s(t) = f(t) \times S(t)$  periodic sampling, and (b) periodic sampling and hold into high impedance buffer.

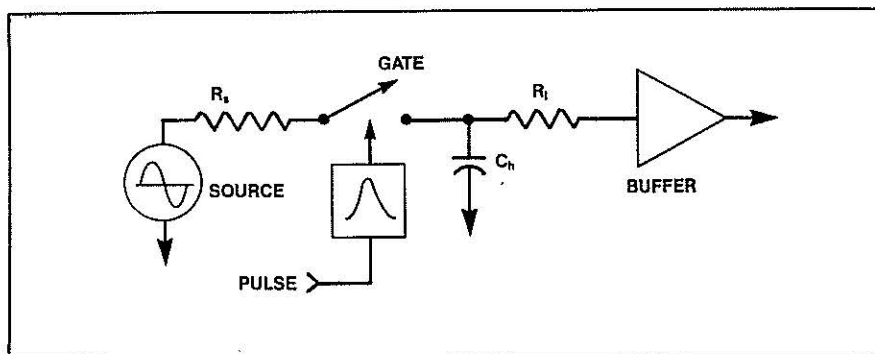


Fig. 2 An ideal subharmonic sampling model.

$f(t) - 10 \times f_c$ , is the desired output signal. Extracting this baseband signal does require some circuit improvements.

### Sample-and-Hold Circuit Offers Improvements Over Sampling

In order to perform sampling downconversion to baseband, the desired output of the FFT shown in Figure 1a would be the spectral replica at  $f(t) - 10 \times f_c$ . This is because the signal was sampled at the one-tenth subharmonic. All of the other spectral images in the FFT need to be rejected. To improve this situation, instead of multiplying  $F(t)$  by the periodic sampling function  $S(t)$ ,  $f(t)$  is

sampled when  $S(t)$  is high and  $f(t)$  is held when  $S(t)$  is low. This logic statement allows emulation of the sample-and-hold process.

The output FFT spectrum of the defined subharmonic sample-and-hold process reveals its most significant property, which is the ability to downconvert a microwave or mm-wave signal to baseband with great efficiency and without loss of fidelity. Any loss in fidelity is due to the phase noise of the sampling clock degraded by  $20 \log$  of  $n$ . The Fourier transforms of Figure 1b show how the sample-and-hold process converts most of the sampled energy to the baseband spectral replica cen-

tered at  $f(t) - n \times f_c$ . This level of performance may be achieved in actual microwave and millimeter-wave subharmonic sample-and-hold circuitry when the circuit criteria are met.

### Subharmonic Sample-and-Hold Circuit Modeling and Optimization

From the ideal subharmonic sample-and-hold model shown in Figure 2, parameters that must be considered during the design of a microwave sampling circuit may be defined. The source represents the microwave signal to be sampled. The source, defined by the function

$$f(s) = \sin(2\omega + \theta)$$

delivers a time variant voltage  $V_s$  of source impedance  $R_s \Omega$ . During the sampling cycle, the source signal is applied to the hold capacitor  $C_h$  via the gate. The sampling aperture ( $t_a$ ) is the time the gate is closed. The resistance of the gate ( $R_d$ ) has been included in the total source impedance ( $R_s$ ).

The parameters that come into play during the hold cycle include the hold capacitance ( $C_h$ ) and the load impedance of the buffer amplifier  $R_l$ . The hold time is the period of the sampling rate ( $f_c$ ) minus the sampling aperture ( $t_a$ ).

During the sample cycle, the gate closes for the duration of the sampling aperture and a charge is imposed on the hold capacitor. The charge on the hold capacitor in coulombs can be expressed by

$$q = \int f(t) \cdot t \, dt$$

Because the value for  $V_s$  is a time variant function ( $V(s) = \sin(\omega t)$ ), the integral becomes

$$q = \frac{(t_a - t_0)}{R_s} \int_{\text{over the interval of } t_a \text{ through } t_0} \sin(\omega t) \cdot e^{-\left(\frac{(t_a - t_0)}{(R_s \cdot C_h)}\right)} dt$$

Integrating this function over the sampling aperture time for a given value of  $C_h$  and  $R_s$  yields the value for charge stored on the sampling capacitor in coulombs.

The value of the hold capacitor  $C_h$  is of significance as it is a parameter that the designer can easily control. Insight into the most judicious choice of sampling capacitance can be obtained by evaluating the

[Continued on page 242]



|          |     |         |                   |
|----------|-----|---------|-------------------|
| 2.4-30   | MHz | 100 KW  | .02 DC            |
| 80-160   | MHz | 500 W   | 2-5 $\mu$ S       |
| 160-240  | MHz | 500 W   | 4-7 $\mu$ S       |
| 175-225  | MHz | 300 KW  | 1, 4, 20, $\mu$ S |
| 210-225  | MHz | 1 MW    | 5 $\mu$ S         |
| 400-420  | MHz | 14 KW   | .0002 DC          |
| 950-1550 | MHz | 1 KW    | 1 DC              |
| 900-1040 | MHz | 5/15 KW | 1 $\mu$ S         |

|           |     |         |                  |
|-----------|-----|---------|------------------|
| 2.4-3.0   | MHz | 100 KW  | .02 DC           |
| 80-160    | MHz | 500 W   | 2.5 $\mu$ S      |
| 160-240   | MHz | 500 W   | 4-7 $\mu$ S      |
| 175-225   | MHz | 300 KW  | 1/4, 20, $\mu$ S |
| 210-225   | MHz | 1 MW    | 5 $\mu$ S        |
| 400-420   | MHz | 14 KW   | .0002 DC         |
| 950-1550  | MHz | 1 KW    | 1 DC             |
| 900-1040  | MHz | 5/15 KW | 1 $\mu$ S        |
|           |     | 20 KW   | 1 $\mu$ S        |
| 1.2-1.35  | GHz | 500 KW  | 2 $\mu$ S        |
| 1.25-1.35 | GHz | 4 MW    | 2 $\mu$ S        |
| 2.1-3.8   | GHz | 100 W   | 1.5-7 $\mu$ S    |
| 3.2-3.3   | GHz | 10 KW   | .001 DC          |
| 2.7-2.9   | GHz | 250 KW  | 0.8 $\mu$ S      |
| 2.7-2.9   | GHz | 1 MW    | 1 $\mu$ S        |
| 3.1-3.6   | GHz | 1 MW    | 1.3 $\mu$ S      |
| 2.7-2.9   | GHz | 5 MW    | 2-3 $\mu$ S      |
| 5.4-5.8   | GHz | 250 KW  | .001 DC          |
| 5.4-5.9   | GHz | 500 W   | .002 DC          |
| 5.4-5.8   | GHz | 5 MW    | .001 DC          |
| 6         | GHz | 1 MW    | 1 $\mu$ S        |
| 6.2-6.6   | GHz | 200 KW  | .37 $\mu$ S      |
| 8.7-8.9   | GHz | 1.2 KW  | .045 DC          |
| 9.375     | GHz | 40 KW   | 5-1-2 $\mu$ S    |
| 8.5-9.6   | GHz | 250 KW  | .0013 DC         |
| 9.375     | GHz | 100 KW  | 5-1-2 $\mu$ S    |
| 9.1       | GHz | 400 KW  | 1.8 $\mu$ S      |
| 13.8-14.2 | GHz | 70 KW   | .001 DC          |
| 15.5-17.5 | GHz | 135 KW  | .33-1.3 $\mu$ S  |
| 24        | GHz | 40 KW   | .15 $\mu$ S      |
| 35        | GHz | 80 KW   | .001 DC          |

|          |     |        |
|----------|-----|--------|
| 17-27    | KHz | 200 W  |
| 125-450  | KHz | 4 kW   |
| 350-500  | KHz | 250 W  |
| 2-30     | MHz | 3 kW   |
| 4-21     | MHz | 40 kW  |
| 20-170   | MHz | 100 W  |
| 160-350  | MHz | 100 W  |
| 200-2000 | MHz | 40 W   |
| 385-575  | MHz | 1.5 kW |
| 750-985  | MHz | 1 kW   |
| 950-1550 | MHz | 150 W  |
| 1.5-5.0  | GHz | 150 W  |
| 1.7-2.4  | GHz | 1 kW   |
| 1.7-2.4  | GHz | 10 kW  |
| 4.4-5.0  | GHz | 1 kW   |
| 7.25-8.8 | GHz | 150 W  |
| 7-4      | GHz | 2 kW   |
| 8.5-9.6  | GHz | 1 mw   |
| 8.7-10   | GHz | 150 W  |
| 16-17    | GHz | 40 mw  |

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|-------------------|--------|------------------|
| 2 KW Line Type    | 4.2 KV | 5 A .25 $\mu$ S  |
| 5 KW Hard Tube    | 3 KV   | 2 A .11 $\mu$ S  |
| 25 KW Hard Tube   | 5 KV   | 6 A .012 DC      |
| 144 KW Hard Tube  | 12 KV  | 12 A .001 DC     |
| 250 KW Hard Tube  | 16 KV  | 16 A .002 DC     |
| 405 KW Float's Dk | 20 KV  | 20 A .1 DC       |
| 500 KW Line Type  | 22 KV  | 28 A .001 DC     |
| 1 MW Hard Tube    | 25 KV  | 40 A .002 DC     |
| 3 MW Line Type    | 50 KV  | 60 A .30 $\mu$ S |
| 10 MW Line Type   | 76 KV  | 135 A .001 DC    |
| 13 MW Line Type   | 135 KV | 112 A .3 $\mu$ S |
| 17 MW Line Type   | 17 KV  | 1000 A 5 $\mu$ S |

|        |            |             |
|--------|------------|-------------|
| 120 KW | 3KV-64A    | 12.5KV-9.5A |
| 225 KW | 3.3KV-70A  | 15KV-15A    |
| 600 KW | 5.5KV-100A | 22KV-28A    |
| 1.5 MW | 8KV-187A   | 35KV-50A    |
| 3.5 MW | 7.1KV-500A | 55KV-65A    |
| 11 MW  | 15KV-730A  | 73KV-150A   |

|      |    |        |
|------|----|--------|
| 6.3  | KV | 5.25 A |
| 0-20 | KV | 1.35 A |
| 0-35 | KV | 1.5 A  |
| 12   | KV | 800 Ma |
| 30   | KV | 230 Ma |
| 15   | KV | 2 A    |
| 16.8 | KV | 10 A   |
| 20   | KV | 50 A   |
| 60   | KV | 1 Ma   |

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Fig. 3 Sampled voltage ( $V_c$ ) and stored kinetic energy ( $K_e$ ) per sample vs. hold capacitance; (a) source  $z$  transformer (50 to 25  $\Omega$ ) and (b) source  $z$  transformer (50 to 12.5  $\Omega$ ) with  $RF_{in} = 18.5$  GHz @ 5 dBm and sampling aperture = 27 ps.

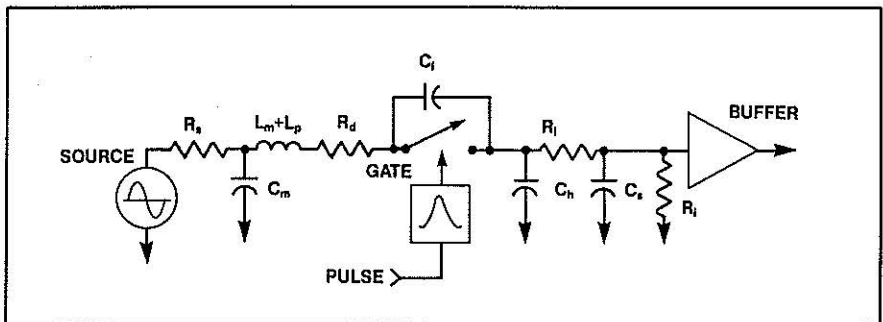


Fig. 4 An actual subharmonic sampling model.

kinetic energy stored during the sample cycle, which is equal to

$$K = \frac{(q^2)}{C_h}$$

The voltage stored on the capacitor is equal to

$$V_c = \frac{q}{C_h}$$

Figure 3 shows the effect of hold capacitance on the stored voltage  $V_c$  and the total kinetic energy for two values of  $R_s$ . The lower source impedance delivers the same kinetic energy to a larger hold capacitor that the higher impedance can only deliver to a small capacitance. The only difference for these two cases is the voltage ( $V_c$ ), which decreases by the square root of the impedance ratio or by the square root of two. By increasing the incident power on the sampling circuit by 3 dB, the original voltage will be restored and the kinetic energy will be increased two fold. The hold circuit can achieve optimum performance with a larger capacitor.

Thus, it is important for the source to offer a low impedance to the gate-

and-hold capacitor. In the actual sample-and-hold model, shown in Figure 4, the capacitor  $C_m$  has been included to demonstrate a matching structure that consists of  $C_m$  and  $L_m + L_p$ . This LC network makes convenient use of the series inductance of the bond wires in the sampling bridge diodes for the purpose of matching the  $50\ \Omega$  source impedance to the  $10\ \Omega$  gate impedance.

## Output Buffer Amplifier Design Establishes IF Response

With  $R_s$  and  $C_h$  established to give maximum kinetic energy for a given sampling aperture, the effects of the buffer amplifier impedance on the stored voltage during the hold cycle are considered. An ideal sample-and-hold buffer circuit should be capable of measuring the voltage stored on the hold capacitor for the duration of the hold cycle without discharging the capacitor. The advantage of buffer circuitry, which can as nearly as possible meet this ideal requirement, is evident in the FFT of the ideal subharmonic sample-and-hold simulation, as shown in Figure 1b. Next, one may compare this to the output of a sample-

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and-hold circuit that has a low impedance load, as shown in Figure 5.

The resulting poor hold duration manifests itself as an increasing inability of the sample-and-hold circuit to isolate the periodic sampling function discrete-line spectra from the output of the sample-and-hold circuit. On the other hand, if the buffer can be made to have a high impedance, the output signal will contain little harmonic energy and a much stronger baseband down-converted spectrum of the sampled signal.

Commercially available high impedance buffer amplifiers offer very impressive input impedances in the giga ohm ranges. However, these devices can have stray input capacitances of 3 pF. If connected in parallel with the hold capacitor, this capacitance would destroy the efficiency of the circuitry.

In a subharmonic sampling phase detector application, a 50 K $\Omega$  series input resistance connecting the hold capacitor to a high impedance op-amp with 3 pF of stray input capacitance would create a lowpass filter with a corner frequency at 1 MHz. This limited frequency response is adequate for phase lock

loops that have bandwidths of less than 100 kHz. However, in microwave signal processing, where subharmonic sampling is used to extract information from a broadband modulated carrier or to downconvert a carrier to an IF frequency, the buffer amplifier will be required to have a frequency response as high as one-half the sampling rate. In this case, the buffer amplifier will need to have both high input impedance and very low input capacitance. A

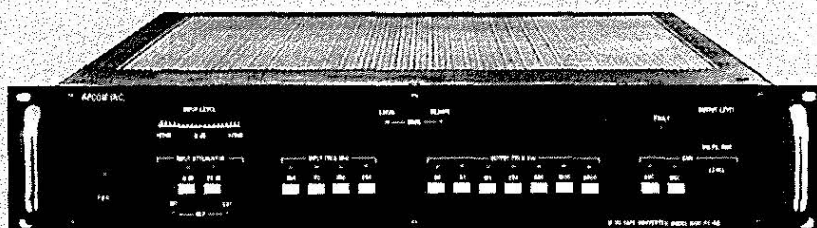
possible solution to this problem is to include the gate capacitance of a FET source follower into the total required value of hold capacitance.

#### Sampling Aperture Width Establishes Input RF Response

Maximum kinetic energy will be transferred to the hold capacitor when the sampling aperture is one-half the period of the frequency of the sampled carrier. Sampling a

[Continued on page 244]

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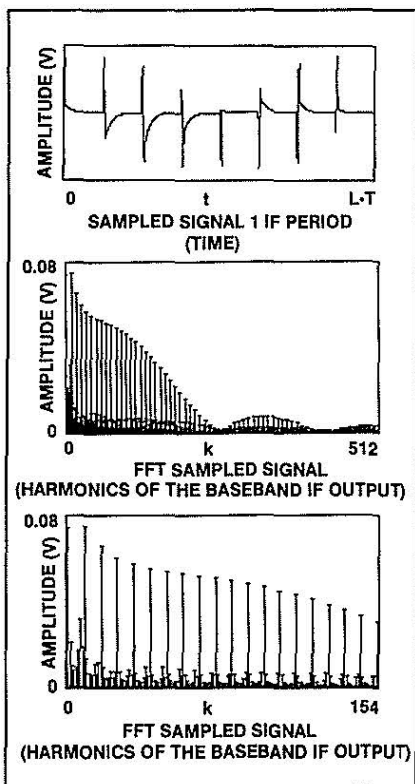


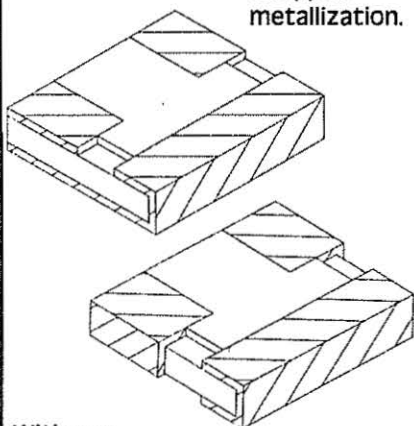
Fig. 5 Time domain analysis of periodic sampling and hold into a low impedance buffer.

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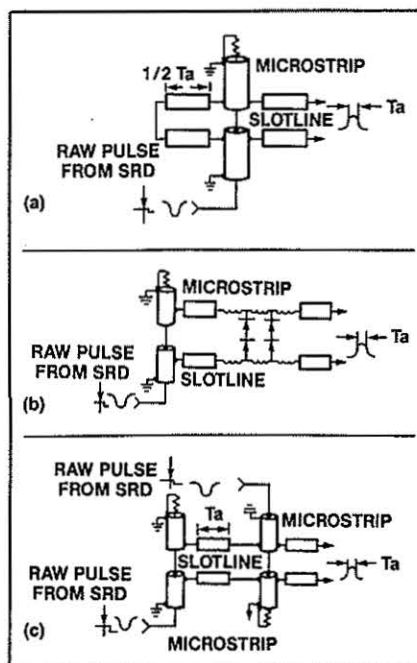


Fig. 6 Pulse compression techniques; (a) back short reflected pulse inversion, (b) nonlinear transmission line and (c) anti-parallel displaced pulses.

40 GHz carrier would require a sampling aperture of less than 15 ps. With this in mind, and to the extent of what is practical in the generation of the sampling aperture pulse, generating a pulse that is too narrow is challenging above C-band.

The best step recovery diodes (SRD) employed in pulse generation have a transition time of 35 ps, and a subsequent pulse width of 70 ps. Based on the above criteria, a sampling phase detector design that does not use a pulse compression technique will experience difficulty in operating at frequencies beyond 7 GHz.

A number of techniques can be employed to achieve the required pulse compression needed to operate at microwave and mm-wave frequencies. The ease at which the pulse compression hardware can be implemented is dependent on the type of 180° balun that is used to generate the balanced sampling aperture pulses to be applied to the sampling bridge diodes. The types of baluns that can find applications in sampling circuitry are generally those baluns employed in frequency mixers that offer multi-octave bandwidths with good 180° balance.

The most popular sampling phase detector balun is the floating dual resistive terminated balun found in

the commercially available sampling phase detectors. This balun offers minimum bandwidth at microwave frequencies, suffers from DC drift and is not easily adapted to pulse compression techniques.

A more practical balun that offers multioctave bandwidth is the slotline-to-coplanar waveguide balun. Some very effective pulse compression techniques can be applied to these types of E-plane circuits. A collection of techniques is shown in Figure 6.

In the backshort circuit, the pulse travels in both directions at the microstrip-to-slotline transition. When the pulse strikes the shorted end of the slotline, it is inverted and reflected where it combines with the trailing edge of the forward traveling pulse. The trailing inverted pulse clips the forward pulse, which shortens the effective sampling aperture.

In Figure 6b, a nonlinear transmission line is used. The nonlinear transmission line uses varactor diodes to generate a voltage dependent time delay. The higher voltages of the pulse waveform propagate faster, which leads to a steepening of the leading edge of the pulse.<sup>6</sup>

The circuit shown in Figure 6c uses anti-parallel displaced pulses that are generated simultaneously. The trailing pulse that is inverted from the leading pulse serves to initiate the end of the sampling aperture. In this circuit, the aperture of the individual pulses is of minor significance as it is the spacing between pulses that establishes the sampling aperture.

## Sampling Circuit Applications Subharmonic Sampling Phase Lock Oscillators

Perhaps the simplest and most common application for microwave sample-and-hold circuitry is in the sampling phase detector used to perform synchronization of a microwave oscillator with a high stability reference oscillator. In this hardware, the sampling circuit is periodically gated at a subharmonic of the microwave signal. During phase synchronization of the reference oscillator with the microwave VCO, the sampling circuit measures the voltage of the zero crossing of a single half cycle of the microwave signal.

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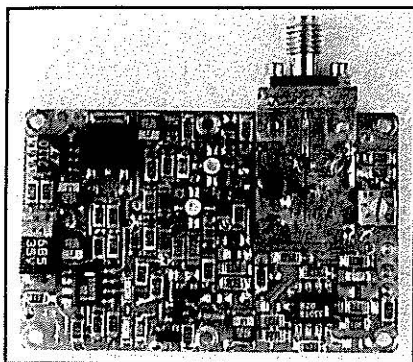


**Fig. 7 A complete sampling PLL module without the VCO.**

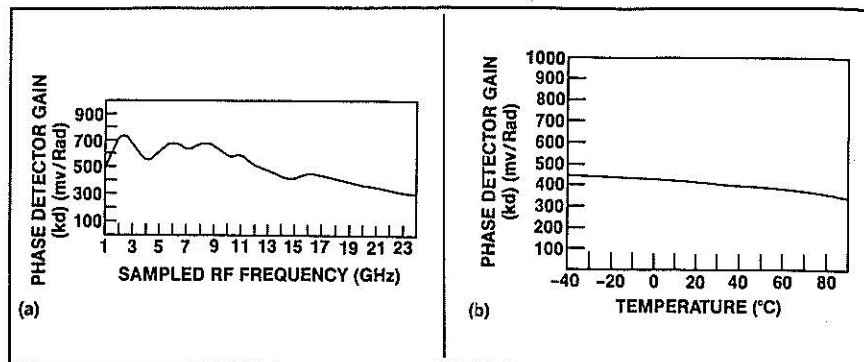


Fig. 8 Sampling phase detector performance; (a) typical gain and (b) temperature drift.

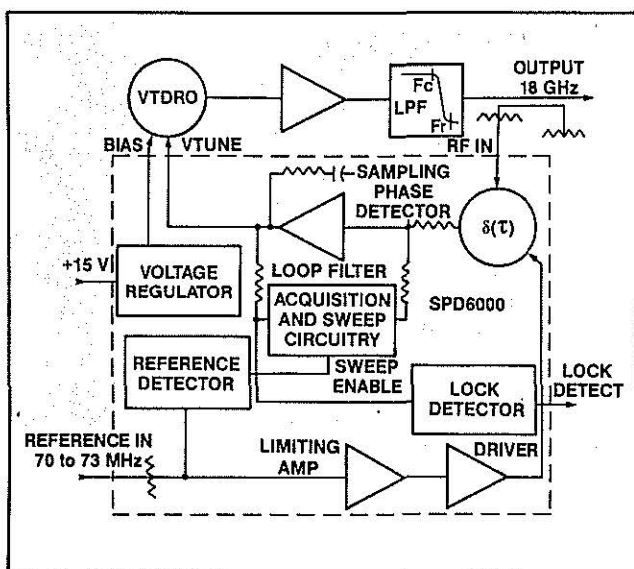


**Fig. 9** A schematic diagram of a sampling PLL module.

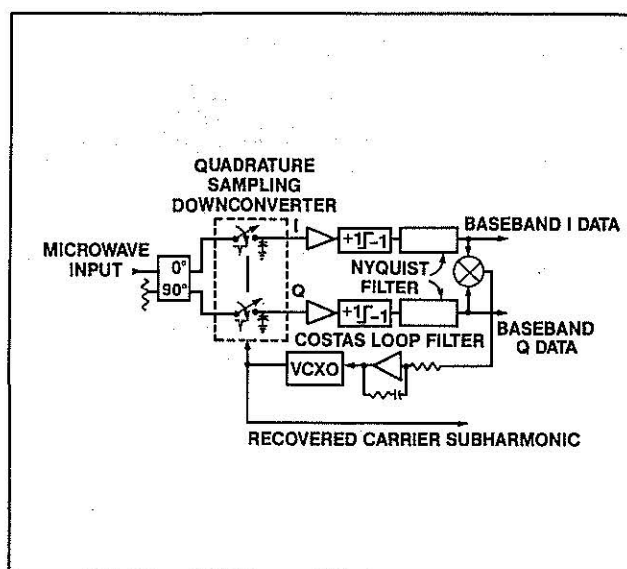


Fig. 10 A quadrature subharmonic sampling carrier recovery loop for direct demodulation of a MPSK microwave carrier.

Any advance or retardation of phase is indicated by a negative or positive DC shift at the IF output of the sample-and-hold circuit. When this signal is applied to the VCO tuning structure, the phase of the VCO can be forced to track the phase of the reference oscillator at a precise integer subharmonic.

Figure 7 is a complete sampling phase detector module measuring 1.2"  $\times$  1.9". This unit contains a sampling head that delivers a phase detector response of 400 mV/rad at 18 GHz from a 0 dBm input signal. The sampling head topology is a coplanar structure that features pulse compression of the type shown in Figure 4a. The coplanar-to-slotline balun offers multioctave bandwidth and is well suited for sampling head applications.<sup>7,8</sup> Actual performance of the sampling phase detector is shown in Figure 8.

Contained in the module is the reference driver circuitry, loop filter, sweep and acquisition circuitry, reference detector and lock detector circuitry. The module is designed to be integrated with a VCO, such as a voltage tuned DRO, to form a complete PLO subsystem, as shown in Figure 9.

## Direct Demodulation of Microwave MPSK Carriers

This commercial application employs two sampling heads and is an example that performs a great deal of microwave signal processing with a limited amount of microwave components. In Figure 10, the concept of quadrature subharmonic sampling for the purpose of coherent direct demodulation of an MPSK modulated microwave signal with suppressed carrier is introduced. Traditionally, this application would re-

quire a frequency converter with coherent microwave local oscillators and a Costas loop type of carrier recovery system. The quadrature subharmonic sampling module performs frequency conversion to baseband as well as I and Q vector demodulation, simultaneously. The carrier tracking oscillator is the sampling clock VCXO, which is operated at a subharmonic of the microwave carrier. The microwave carrier when split into quadrature and applied to the dual sampling down-converter module enables the I and Q signal to be generated, mixed and applied to the VCXO. The result of this is a quadrature subharmonically sampled carrier recovery loop (QSSCRL). The outputs of the QSSCRL can be digitized, which allows the remainder of the demodulation and decoding to be performed with conventional digital circuitry.

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Fig. 1

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The harmonic modulation process of Figure 6 has been applied to a ternary alphabet. The factor is a discrete value of 1954.<sup>9</sup> The sampled concentration wave is the window function for the FSK demodulation.

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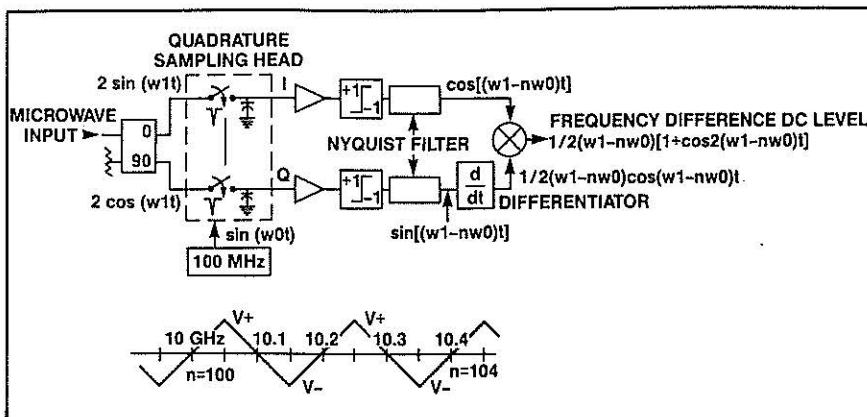


Fig. 11 (a) A subharmonically sampled quadrice correlator and (b) its DC output vs. input frequency.

### Subharmonically Sampled Quadrice correlator

The concept of quadrature subharmonic sampling for vector demodulation is used in many signal processing applications. The circuit of Figure 11 shows how quadrature subharmonic sampling can be applied to an old technique for a modern application. The quadrice correlator is a type of wideband frequency discriminator first introduced in 1954.<sup>9</sup> The subharmonically sampled quadrice correlator allows this concept to be extended to microwave frequencies. Applications of the wideband frequency discriminator might include VCO linearization for microwave FM CW radar, FSK demodulation or precision frequency marker generation.

### Conclusion

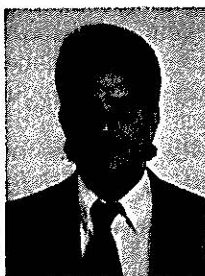
Key criteria for optimum sampling head performance have been discussed. When applied to microwave sampling hardware, the ability to perform vector demodulation of a microwave carrier is one example of the types of microwave signal processing that can be accomplished through subharmonic sampling. This blend of microwave circuitry and digital signal processing techniques represents the new age of microwave signal processing. ■

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